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MODULAR
space station
PHASE B EXTENSION

INFORMATION MANAGEMENT ADVANCED DEVELOPMENT FINAL REPORT

Volume I: Summary

PREPARED BY PROGRAM ENGINEERING
JULY 31, 1972

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Space Division
North American Rockwell

12214 Lakewood Boulevard, Downey, California 90241

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TECHNICAL REPORT INDEX/ABSTRACT

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*MODULAR SPACE STATION, *INFORMATION MANAGEMENT, *ADVANCED DEVELOPMENT, *COMMUNICATIONS, *DATA PROCESSING, *SOFTWARE, *DATA BUS, *DATA STORAGE, *BREADBOARDS, *TECHNOLOGY, *SPECIFICATIONS

ABSTRACT

THIS DOCUMENT IS VOLUME I OF THE FINAL REPORT OF THE MODULAR SPACE STATION ADVANCED DEVELOPMENT STUDY. IT SUMMARIZES THE RESULTS OF AN 18-MONTH STUDY, HARDWARE DESIGN AND TEST PROGRAM WHICH INVESTIGATED AREAS OF INFORMATION MANAGEMENT TECHNOLOGY REQUIRING ADVANCED DEVELOPMENT. THE TASKS INCLUDED THE CONSTRUCTION OF BREADBOARD MODELS OF THE 10 MEGABIT PER SECOND DATA BUS AND THE K-BAND COMMUNICATIONS TERMINAL ANTENNA-MOUNTED ELECTRONICS. THE REMAINING TASKS WERE STUDIES TO FURTHER DEFINE THE DATA PROCESSING AND SOFTWARE ASSEMBLIES RESULTING IN PERFORMANCE SPECIFICATIONS AND DEVELOPMENT PLANS/SCHEDULES FOR ADDITIONAL BREADBOARD OR PROTOTYPE EQUIPMENTS.

FOREWORD

This document is one of a series required by Contract NAS9-9953, Exhibit C, Statement of Work, for the Phase B Extension - Modular Space Station Program Definition. It has been prepared by the Space Division, North American Rockwell Corporation, and is submitted to the National Aeronautics and Space Administration's Manned Spacecraft Center, Houston, Texas, in accordance with the requirements of the Data Requirements List, (DRL) MSC-T-575, Line Item 72.

This document is Volume I of the Modular Space Station Information Management System Advanced Development Technology Report, which has been prepared in the following five volumes:

I	IMS ADT Summary	SD72-SA-0114-1
II	IMS ADT Communications Terminal Breadboard	SD72-SA-0114-2
III	IMS ADT Digital Data Bus Breadboard	SD72-SA-0114-3
IV	IMS ADT Data Processing Assembly	SD72-SA-0114-4
V	IMS ADT Software Assembly	SD72-SA-0114-5

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NR-Autonetics Anaheim, Calif. J. Jurison, Proj. Mgr.	Data Bus BB Data Processing Assy

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ILLUSTRATIONS

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ABBREVIATIONS

ADS	Advanced Data System
ADT	Advanced Development Technology
ADTX	Advanced Development Technology Extension
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
AN	Autonetics (Division of North American Rockwell Corporation)
BPF	Bandpass Filter
bps	Bits Per Second
CAIRS	Computer-Assisted Interactive Resource Scheduling
CCIR	International Radio Consultative Committee
CDR	Critical Design Review
CEI	Contract End Item
CLASP	Computer Language for Aeronautics and Space Programming
CM	Command Module (Apollo)
COMPOOL	Common Pool (of Data)
CP	Central Processor or Circular Polarization
C.P.	Computer Program
CPCEI	Computer Program Contract End Item
CPCI	Computer Program Configuration Item
CPDF	Computer Program Development Facility
CPIC (A)	Computer Program Integration Contractor (Agency)
CPT&E	Computer Programming Test and Evaluation
CR	Change Report
CRT	Cathode-Ray Tube (Display)
CSS	Crew Subsystem
CTB	Communications Terminal Breadboard
CTF	Central Test Facility
DACS	Data Acquisition and Control Subassembly
dB	Decibel
DBCU	Data Bus Control Unit
dBm	Decibel Referred to One Milli-Watt
dBW	Decibel Referred to One Watt
DCR	Design Change Request
DDB	Digital Data Bus
Demux	De-Multiplex(er)
DMS	Data Management System
DPA	Data Processing Assembly
DPSK	Dual Phase Shift Keying
DRSS	Data Relay Satellite System

ECP	Engineering Change Proposal
EDF	Experiment Data Facility
EEM	Engineering Evaluation Model
EEMP	Engineering Evaluation Model Processor
EIRP	Effective Isotropic Radiated Power
EMC	Electromagnetic Compatability
EMI	Electromagnetic Interference
EOS	Earth Orbital Shuttle
EOSS	Earth Orbital Space Station
EPS	Electrical Power Subsystem
ETC/LSS or ECLSS	Environment Control and Life Support Subsystem
EVA	Extra-Vehicular Activity
EXT	External
E_b/N_o	Energy Per Bit to Noise Density Ratio
FACS	Facsimile
FDM	Frequency-Division Multiplex
FM	Frequency Modulation
FQT	Formal Qualification Test
G&CS	Guidance and Control Subsystem
GFE	Government Furnished Equipment
GHz	Giga-Hertz
GOA	Gated Operational Amplifier
HAL	Higher-Order Aerospace Programming Language
HOL	Higher-Order Language
HOLM	Higher-Order Language Machine
Hz	Hertz
IF	Intermediate Frequency
IFRU	In-Flight Replaceable Unit
IM	Intermodulation Products
IMS	Information Management System
IMSIM	Information Management Simulation
IOC	Initial Operational Capability
IOCB	Input-Output Control Block
IOU	Input-Output Unit
I/O	Input-Output
IPA	Intermediate Power Amplifier
IQL	Interactive Query Language
IR	Infra-Red
ISS or IMS/S	Information (Management) Subsystem
ITT	International Telephone and Telegraph
K-words	Thousands of (Computer) Words
K-EAPS	Thousands of Equivalent-Add Operations Per Second
K-bps	Thousands of Bits Per Second
KH_z	Kilohertz

LEM	Lunar Excursion Module
LM	Lunar Module
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
M1, M2	(Computer) Memory Designation
Mbps	Megabits Per Second
MCB	Module Control Block
MHz	Megahertz
MOF	Mission Operations Facility
MOL	Manned Orbiting Laboratory
MSC	Manned Spacecraft lenter
MSFN	Manned Space Flight Network
MSS	Modular Space Station
MUX	Multiplexer
mW	Milli-Watts
MW	Microwave
mV	Milli-Volts
NF	Noise Figure
OBCO	On-Board Checkout
OCC	Operations Control Center (On-Board)
ODM	Operational Data Management
OM	Operating Memory
PA	Power Amplifier
PCM	Pulse Code Modulation
PDR	Preliminary Design Review
PL/1	Procedure Language
PM	Phase Modulation
PN (PRN)	Pseudo Random Noise
ppm	Parts Per Million
PQT	Preliminary Qualification Tests
PSK	Phase Shift Keying
RAM	Research and Applications Module
RACU	Remote Acquisition and Control Unit
RCS	Reaction Control Subsystem
RF	Radio Frequency
RHCP	Right-Hand Circular Polarization
RPU	Remote Processing Unit
Rx	Receive
S&C	Standards and Conventions
SCCB	Software Configuration Control Board
SCN	Specification Change Notice
SD	Space Division (of North American Rockwell Corporation)
SDC	Systems Development Corporation

S/N	Signal to Noise Ratio
SOW	Statement of Work
SPL	Space Programming Language
SRD	Step-Recovery Diode
SSCB	Solid-State Circuit-Breaker
SSS	Structures Subsystem
STE	Support Test Equipment
TAV	Test and Validation (Programs)
TBD	To Be Determined
TCXO	Temperature-Controlled Crystal Oscillator
TDA	Tunnel Diode Amplifier
TDM	Time Division Multiplexing
TDRS	Tracking and Data Relay Satellite
TIP	Test and Integration Plan
TLM, TM	Telemetry
TOOL	Test Operations Oriented Language
TRW	Thompson Ramo Woolridge Corporation
TT&C	Telemetry, Tracking and Control
TWT	Traveling Wave Tube
TWTA	Traveling Wave Tube Amplifier
Tx	Transmit
USB (E)	Unified S-Band (Equipment)
UV	Ultra-Violet
VDD	Version Description Document
VHF	Very High Frequency
VSB	Vestigal Side Band
VSWR	Voltage Standing Wave Ratio

LIST OF INTERIM REPORTS

AA-101	DPA Flow Diagrams, September 1971
AA-102	DPA Throughput and Authority Analysis, February 1972
AA-103	DPA Configuration Selection, April 1972
AS-101	Modular Space Station Computer Program Standards and Conventions, December 1971
AS-102	Modular Space Station Computer Program Specification Tree, February 1972
AS-103	Modular Space Station Computer Program Development, Test and Configuration Control Plan, May 1972
AS-104	Modular Space Station Computer-Assisted Resource Allocations and Utilization Recommendations, June 1972
CTB-101	Concepts for Multiple RF Link Mechanization, May 1971
CTB-103	Antenna-Mounted Electronics Component Design, October 1971
CTB-105/106	CTB Integration and Test and Operations Manual, June 1972
DB-101	Parametric Data for Bus Design, May 1971
DB-103	Component Performance Requirements, Schematics and Layout Drawings, December 1971
DB-104	Digital Data Bus Breadboard Final Report, May 1972
DD-102	Modular Space Station Data Processing Assembly Parametric Evaluation of Subsystems Input/Output Interface, June 1971

DD-103	Modular Space Station Data Acquisition and Control Subassembly Model Configuration (SD 71-233), July 1971
DP-101	Data Processing Assembly Configuration (Preliminary), June 1971
DP-102	Data Processing Assembly Supervisor Specification, May 1972
DP-103	DPA Processor Final Description, May 1972
DP-104	EEM DMS Processor Development Plan, June 1972
DP-105	Data Acquisition and Control Redundancy Concepts, August 1971
DP-106	Application of Redundancy Concepts to DPA, January 1971
DP-107	Data Acquisition and Control Subassembly Breadboard Design Requirements, October 1971
DP-108	Data Bus Control Unit Performance Requirements, January 1972
DP-109	Data Bus Control Design Reports, March 1971
DP-110	DBCU Acceptance Report (to be published)
EL-277	Bulk Storage Development Plan
IB-101	DPA Internal Flow and Traffic Pattern, May 28, 1971
ICD #TRW 20549	Interface Control Document - Data Bus Modem/RACU, Revision A, January 17, 1972
ICD #AN 26465	Interface Control Document - Data Bus Controller Unit to Buffer I/O, Revision January 21, 1972
MD-101	Mass Memory Parametric Data
RF-101	Modular Space Station Communications Terminal Breadboard Preliminary System Specification, October 1971

SA-101	Central Processor Operational Analysis, September 30, 1971
SA-102	Central Processor Memory Organization and Internal Bus Design, December 30, 1971
SD 71-227	Automatic Control and Onboard Checkout Final Study Report

1.0 INTRODUCTION

The NASA Modular Space Station Preliminary Definition Study (NAS9-9953) included a special emphasis task to develop selected breadboards and assembly specifications to evaluate and further define the advanced concepts incorporated in the Modular Space Station Program (MSS) information subsystem (ISS). The Space Station Program requirements for near-continuous MSS-to-ground communications, for extended automation of spacecraft subsystem functions, and for expanded autonomy to plan, schedule, and conduct a wide spectrum of experiment operations resulted in an ISS concept that included a K-band data relay satellite communications link, a sophisticated on-board data management system, and an interactive man-machine decision-aid capability. Among other items, the ISS required a 10-megabit-per-second, time-shared data bus system; a dual multiprocessor central computation facility with a complex software assembly and a 25-watt K-band power amplifier.

Since much of the success of the Space Station Program relied upon the capability of the on-board ISS, and since several of these concepts were untried or unproven at that time, the Information Management System (IMS) Advanced Development Technology (ADT) task was funded as a 17-month integrated effort to develop or further define actual equipment breadboards that could be tested and evaluated by NASA (MSC), starting in July 1972. The ADT task was to run concurrently with, support, and track the MSS Preliminary Definition Study; due to lead-time factors, the ADT task was extended in time beyond the MSS study itself so that refinements could be incorporated into the demonstration breadboard equipments to more closely represent MSS requirements.

The influence of the MSS configuration can be seen by examining Figure 1-1. A central core module provides multiple docking ports to accept other special-purpose modules. The core contains the guidance and attitude stabilization/control and the fuel cell power equipments and is divided into two isolatable pressure volumes separated by an airlock. At one end is the solar array power module, which also contains repressurization stores. The four standard modules are internally configured to provide the functions and working/sleeping areas as labeled. An additional cargo module and one or more research application modules (RAM), specialized for selected experiment disciplines, can be docked to any of the five other ports.

There are several aspects that impact the ISS. First, except for the power module, the basic configuration is that of two half-space stations, either one of which can maintain full operational capability even with one pressure volume uninhabitable or unusable for some reason. It follows that the crew's command/control capability (represented by the control center areas in SM-1 and SM-4) must also be dual and capable of operating independently in case of failure or cooperatively under normal conditions. The control center includes the central computer, the operations console, the baseband RF communications, and the internal telephone/television distribution control.

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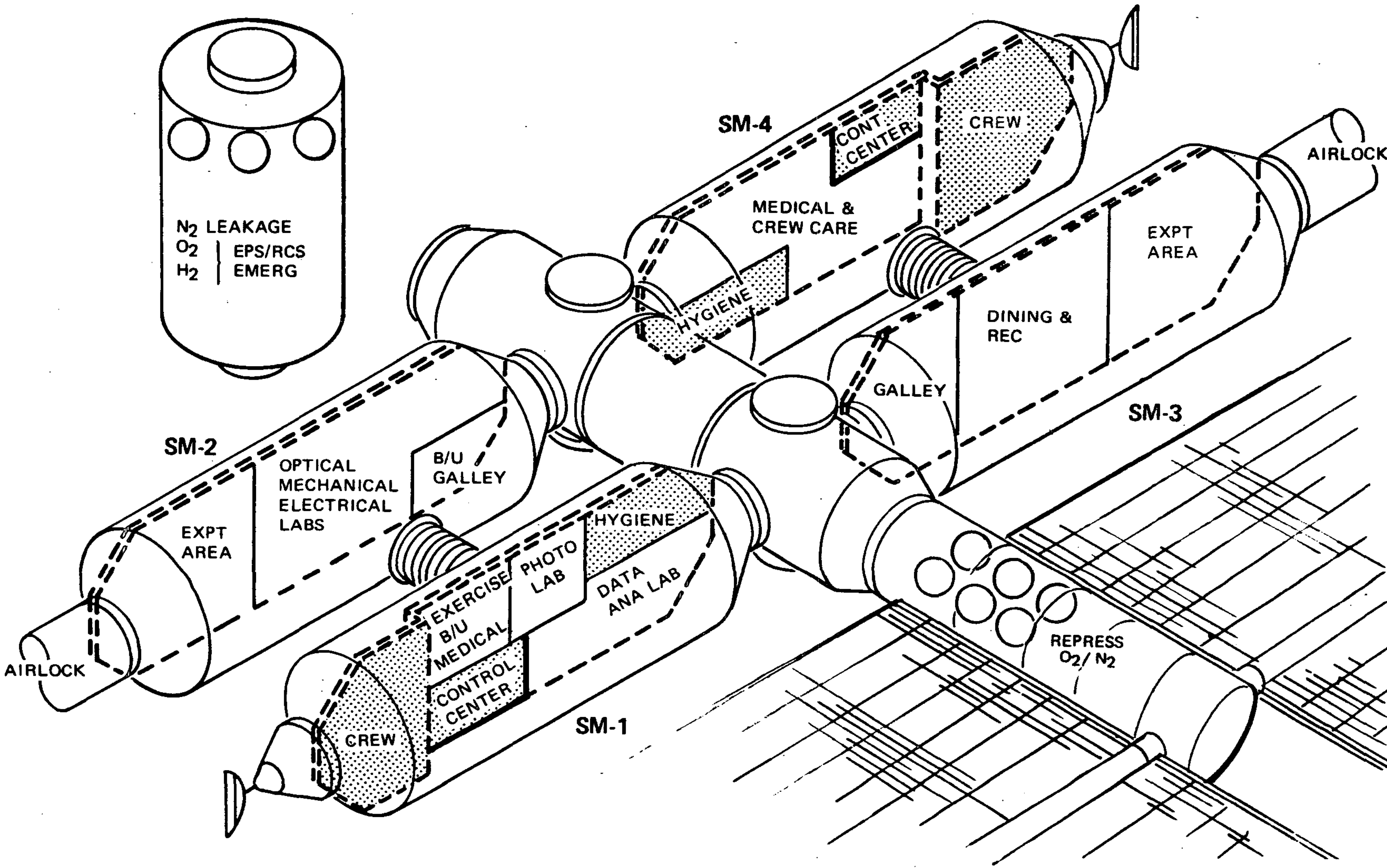


Figure 1-1. MSS Functional Allocations

Second, the MSS is assembled in orbit by successive launches via the orbiter, a procedure that requires many days. The impact is that the ISS must (1) be operable as soon as SM-1 is joined to the core/power modules to automatically control the unmanned station to this point, (2) be extended to each new module as it is docked without modification other than connecting the data bus, and (3) check out and verify the equipment functions of each module after orbital assembly. This guideline of having one spacecraft subsystem verify, certify, and control all other subsystems is indeed unique, and it imposes a failure-tolerance requirement on the ISS that is one level greater than for the other equipments.

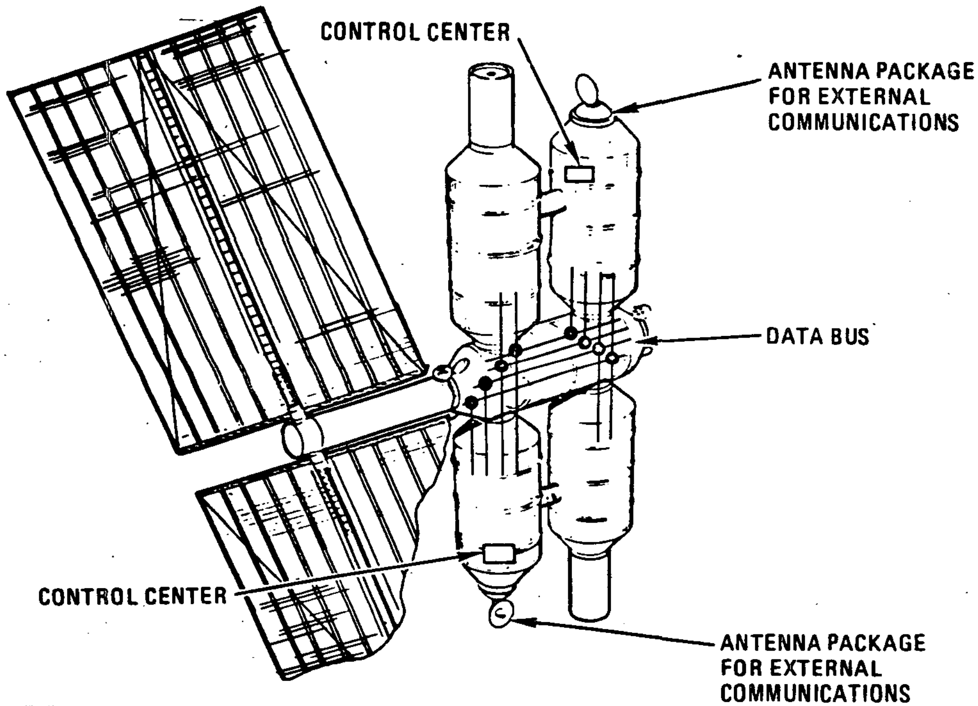
Third, communication with the data relay satellite could not require special attitude maneuvers or constraints to the station flight mode. This communication was implemented by installing two antenna packages on the outboard end of SM-1 and SM-4; the design concept was that the K-band power amplifier and K-band receiver were to be mounted external to the pressure volume (to reduce RF power losses due to cables, connectors, etc.), and that this unit would not have active thermal control. This concept, also unique, was to be demonstrated.

Figure 1-2 shows some of the more important design features of the MSS/information subsystem. Dual control centers, each having a central processor (which is, itself, dual redundant), are both linked by a quad redundant data bus that provides a dual redundant connection to every piece of active equipment. Communications incorporate redundant K-band (1 duplex channel), S-band (3 duplex channels), and VHF (1 duplex channel).

1.1 OVERVIEW

The IMS ADT task was conceived to be one step of a long-range plan (Figure 1-3) to culminate in the delivery of a data management system (DMS) prototype, including the computer (multiprocessor), operations console, executive software, and automatic communications capabilities. This prototype DMS would be used by NASA-MSC for conducting system integration/evaluation tests (including other spacecraft subsystems) and for developing the procedures, programs, and data base needed to automate, detect, and isolate failures, to conduct maintenance and repair simulations on all spacecraft subsystems, and to develop man-machine interactive operations and procedures. The dashed line at the left indicates the scope of the IMS ADT task in contributing to this long-range plan.

The IMS ADT task was divided into seven subtasks (Figure 1-4) to establish contract responsibilities. Their time-phased relationship to the Modular Space Station Definition (4.1.2), Command/Control (4.1.4) and Design (4.1.6) tasks is indicated by the arrows. The ADT subtasks (4.2.1 through 4.2.7) included operating breadboard models of the 10-megabit-per-second data bus and the K-band communications terminal antenna-mounted electronics. The remaining five subtasks were studies to further define the data processing and software assemblies to result in performance specifications and development plans/schedules for additional breadboard or prototype equipments. The dashed-line titles represent some of the expected future ADT subtasks that are considered time-critical to the Space Station Program.



DESIGN FEATURES

- DUAL CONTROL CENTERS
- DUAL CENTRAL PROCESSORS
- QUAD REDUNDANT DIGITAL BUS
- DUAL COMMUNICATION PACKAGE
  - EACH OF THREE BANDS REDUNDANT

UTILITY

- SAFETY
  - TOTAL STATION CONTROL CAPABILITY FROM EACH PRESSURE VOLUME
  - BACKUP COMMAND CONTROL & CENTRAL PROCESSOR USED FOR EXPERIMENTS OPERATIONS DURING NORMAL STATION OPERATIONS

Figure 1-2. MSS Information Subsystem

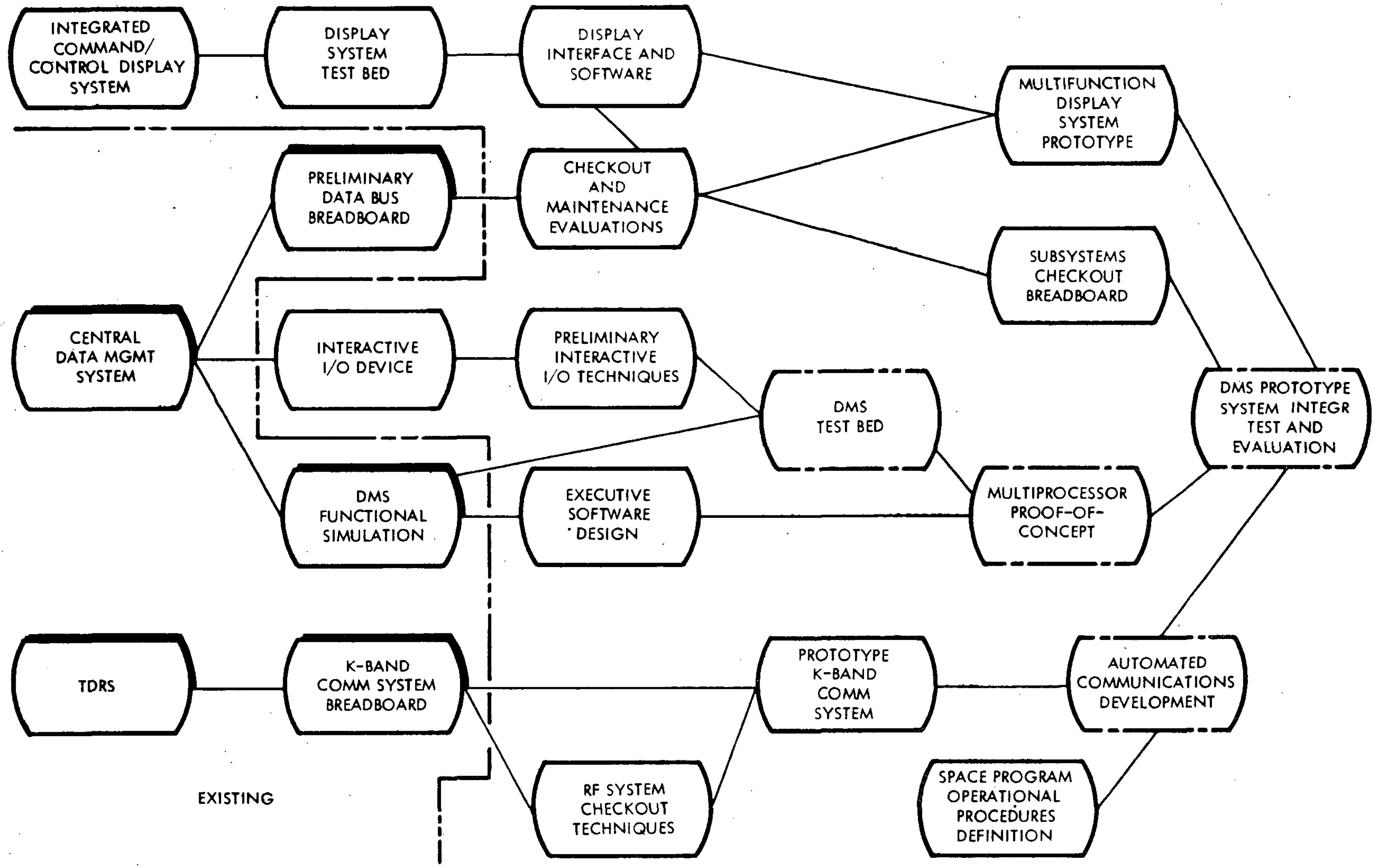


Figure 1-3. Advanced Development Technology Plan

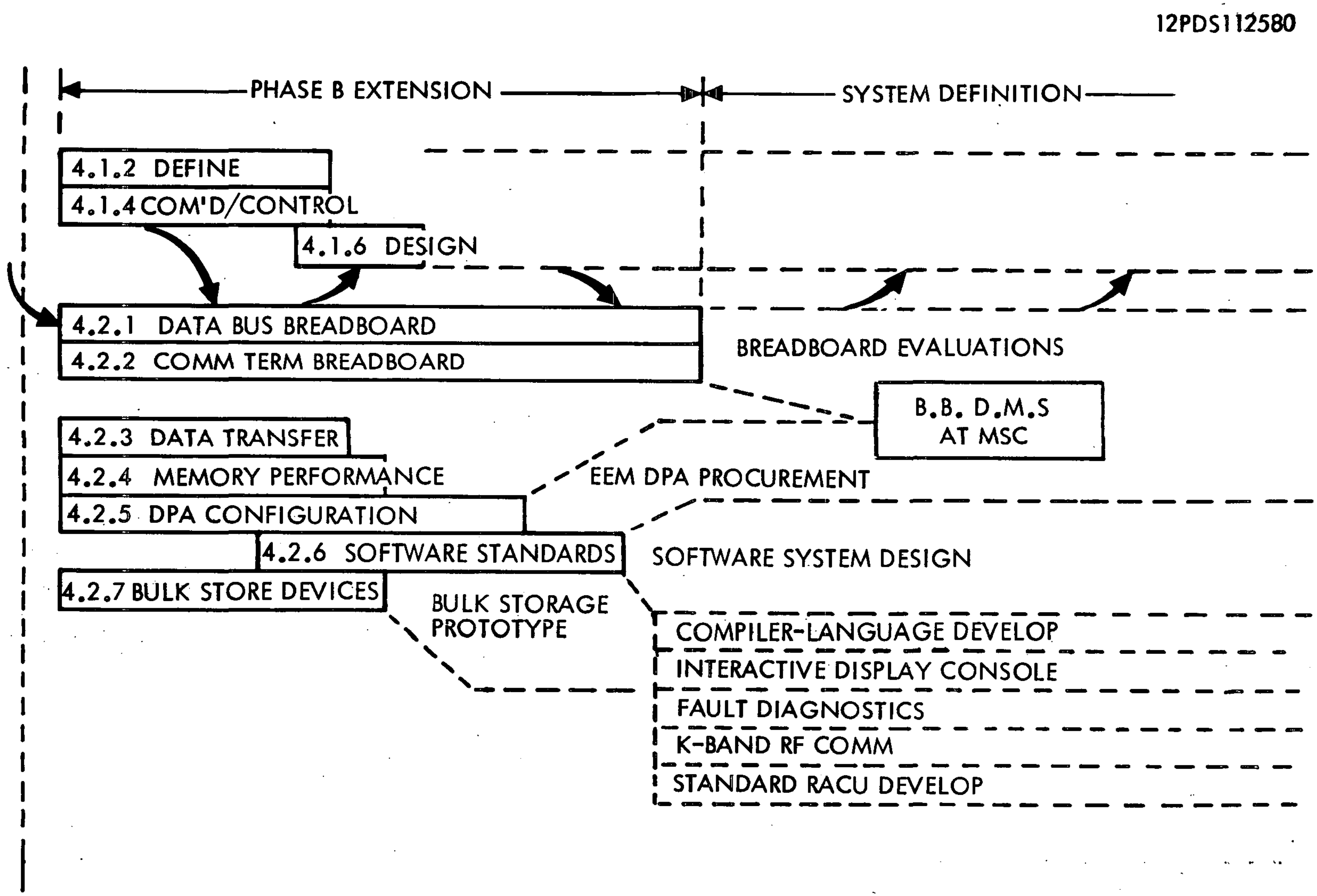


Figure 1-4. Modular Space Station/Advanced Development Interactions

The contractor (NR-SD) elected to subcontract major portions of the ADT task to encourage industry participation and maximize the benefit of considering a variety of viewpoints from specialists. The contractual subtasks (4.2.1 through 4.2.7) were further divided into many small jobs, which were compared to potential subcontractor or NR capabilities and then assembled into work packages for negotiation and administrative control. NR-SD retained the role of systems engineering and technical management, and retained some technical jobs that could best be accomplished with the cooperation of the MSS Information Systems staff and other MSS subsystem design staff. The remainder of the jobs were allocated to subcontractors as shown in Figure 1-5. The contracting agency selected TRW to supply the GFE equipment.

It was realized at the onset that the initially negotiated subcontractor work packages (Statement of Work) would have unforeseeable impacts as the ADT and MSS design studies proceeded. To accommodate these impacts, NR used a flexible management approach, as shown in Figure 1-6. The initial work packages, interim results of progressing studies, and modifications to the MSS Guidelines and Constraints were reviewed periodically by the NASA IMS Working Group, in regular subcontractor technical interchange meetings and in scheduled breadboard concept and design reviews. These meetings, attended by all involved subcontractors and by cognizant NASA-MSC personnel, provided a forum to critique the on-going efforts. Action items were made part of the minutes of these meetings, which in turn were reassessed and developed as technical directive letters to modify or clarify the individual dual subcontractors' statement of work without any cost impact. The success of this approach was due to the very cooperative participation of both subcontractor and MSC personnel.

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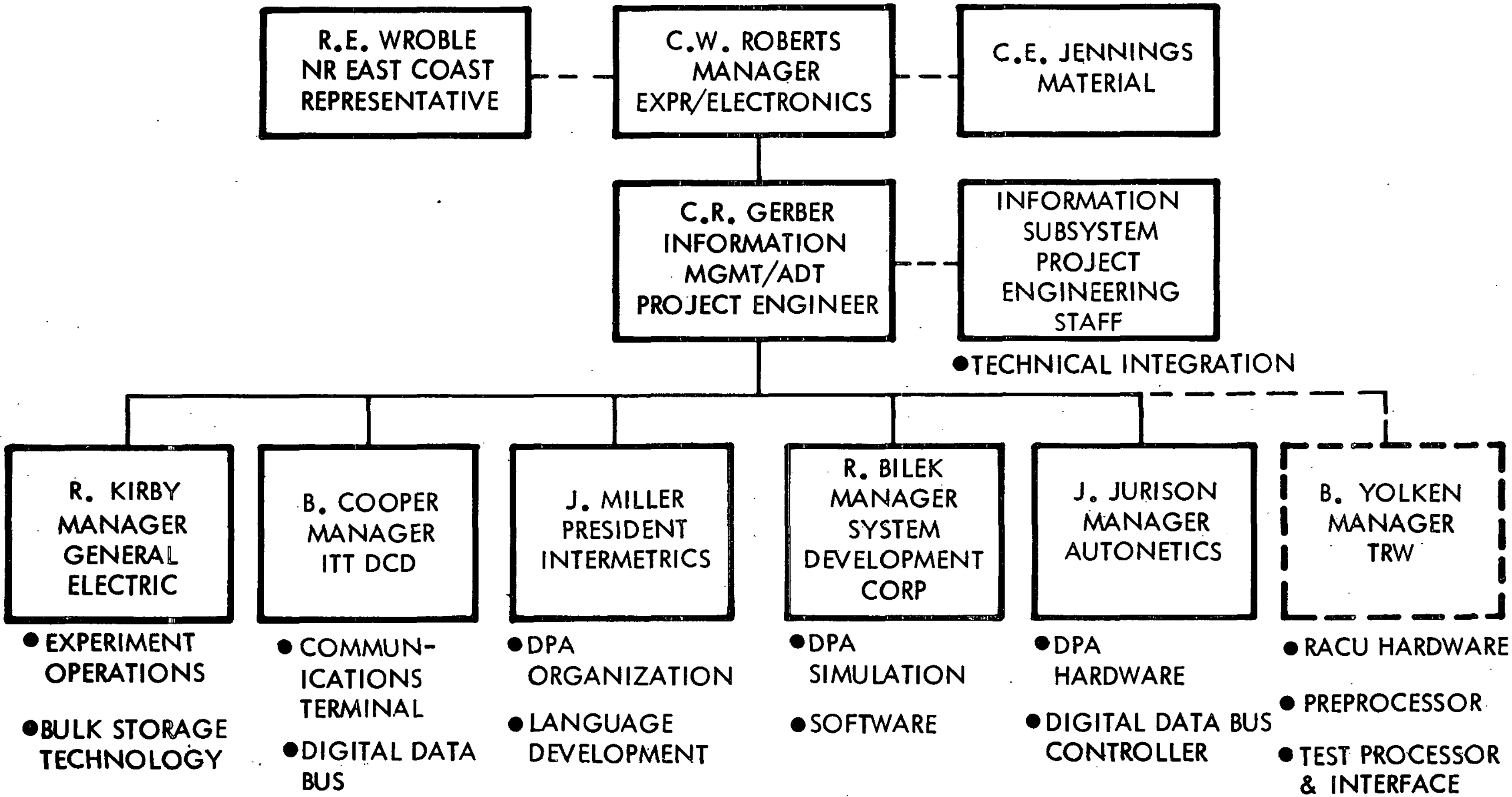

Figure 1-5. Subcontractor Organization

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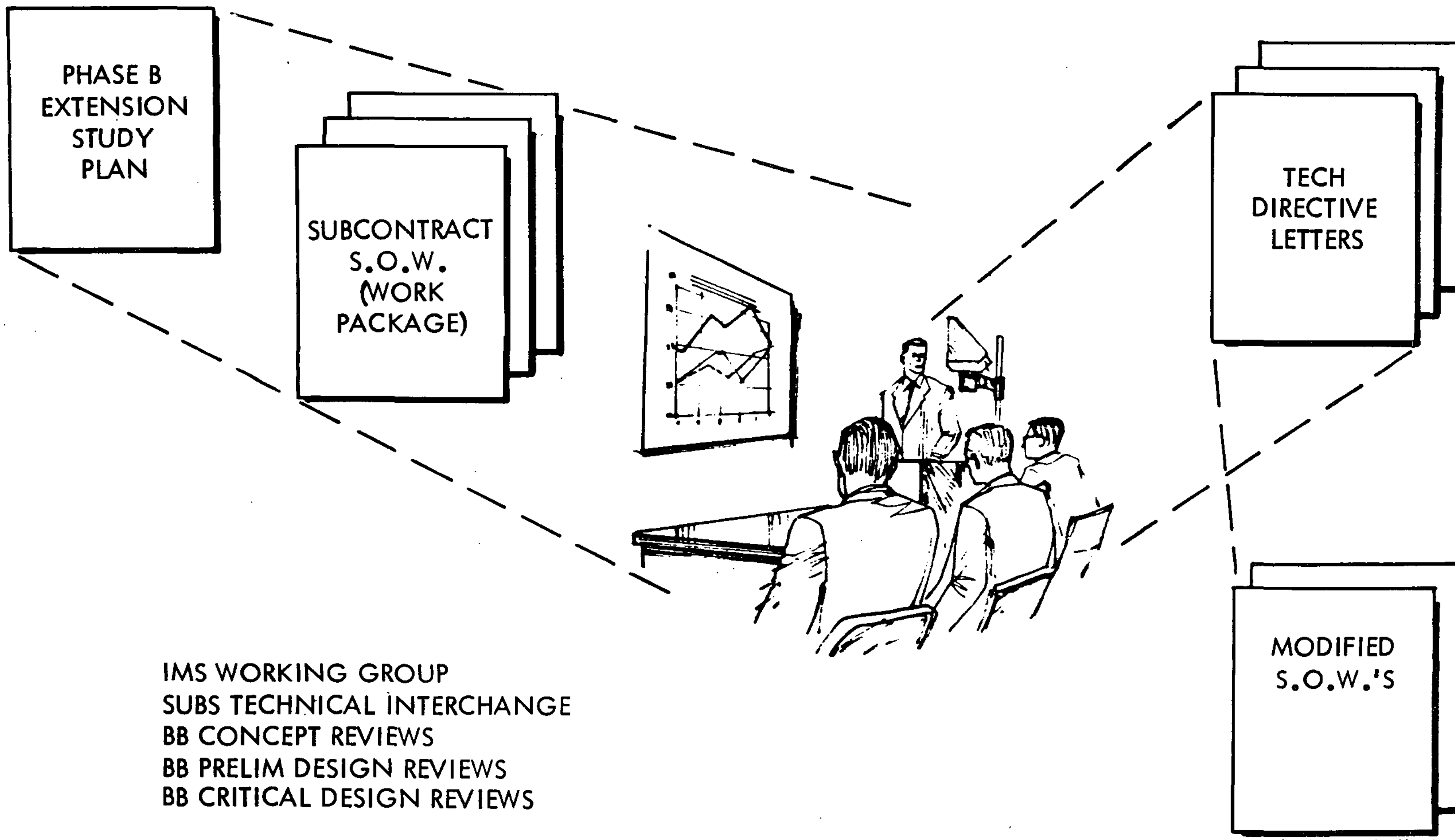

Figure 1-6. Advanced Development Work Package/TDL System

2.0 COMMUNICATIONS TERMINAL BREADBOARD

This section summarizes the results of an 18-month study and hardware design and test whose final objective was to demonstrate a technique for integrating the modular space station (MSS) external communications equipment with a high gain parabolic antenna and to demonstrate its capability to perform the MSS communications operations. This program includes preliminary analysis to define the design of an MSS concept that would be compatible with other program elements such as the earth orbital shuttle (EOS) and the tracking and data relay satellite (TDRS). Details of this analysis, the design concept of an overall communications terminal breadboard (CTB), and the design details and test results of the delivered external RF package are included in Volume II of the final report.

2.1 SUMMARY

The MSS total communications terminal includes a complex of equipment operating in three frequency bands - VHF, S, and K. Each band is used to provide specific communications links with a multiplicity of external terminals and a complex of baseband signals. These links and their signal transfer requirements are defined in Table 2-1 and Figure 2-1.

Operation of the communications system to provide the capability for multiple link frequency performance is proposed by a design that incorporates RF and baseband switching. This design is based on the MSS Phase B concept to mount the K and S-band RF power amplifiers and RF receiver preamplifiers as close to their antennas as possible. In the case of the K-band system, this involves the location of these equipments on the external, steerable, parabolic antenna. By providing up and down conversion to the K-band transmitter and receiver from S-band, low-level RF signals can be routed from the internal S-band equipment over coaxial cables to the antenna mounted equipment. In a similar manner, the S-band system using S-band power amplifiers and receiver front ends mounted close to the semi-directive antennas can be fed at low levels via coaxial cables. Efficiency of overall systems is thus improved by avoiding the RF cable losses that would result at the higher powers and higher frequencies (for the K-band system).

These concepts required the development of a K-band transmitter/receiver package capable of being operated in a space environment and of being mechanically and electrically interfaced with a five-foot parabolic antenna. Development of a concept for multiple RF link mechanization was also required.

The first task resulted in a concept for multiple RF link mechanization. Provision is made to switch between the five separate duplex RF channels which link the MSS to:

1. Tracking and data relay satellite (TDRS)

2. Earth orbital shuttle (EOS)

3. Two research application modules (RAM's)

4. Ground stations of the MSFN

Both baseband and RF switching were considered necessary to provide proper data to the desired link. Utilization of a PIN diode RF switching matrix results in a design concept for a lightweight, compact, reliable RF switching system with presently available hardware. Baseband switching and multiplexing concepts were also analyzed and recommended systems defined.

2.2 CTB GENERAL DESCRIPTION

A complete set of requirements were developed for a communications terminal breadboard (CTB) that can be used as a test bed for evaluation of the MSS terminal concept. Figure 2-2 shows the block diagram of this overall communication terminal breadboard. The antenna-mounted electronics subassembly was designed, developed, and delivered as an operating unit to these requirements. Implementation of a complete system requires the mechanization and interconnection of other subassemblies that include an antenna system, S-band converters to and from baseband, multiplexing and demultiplexing equipment, and a baseband switching system. Requirements for all of these subassemblies were developed and can be used to obtain available hardware. The antenna-mounted electronics subassembly is supplied with the necessary interconnect cables and control display unit to operate this equipment. Figure 2-3 identifies all of this hardware. A concept of the overall breadboard configuration is displayed in Figure 2-4. The overall CTB requirements definitions form the basis for ensuring that the ultimate CTB will represent a logical development of requirements and concepts. It should be emphasized that the characteristics and definitions are by no means frozen. They may vary to reflect any changes in the station concept as it evolves.

The antenna-mounted electronics subassembly contains a K-band (14.65 GHz) receiver mounted in an enclosure designed for operation in a space environment. The K-band equipment is designed to interface with S-band frequencies, specifically compatible with the LEM transceiver. Thus, a complete operating breadboard at K-band can be assembled by connecting and mounting the antenna mounted electronics subassembly to an antenna and connecting the K-band transmitter input to the LEM transmitter output at 2.2825 GHz and the K-band receiver output to the LEM receiver input at 2.1018 GHz. Up and down conversion and the necessary amplification are provided in the K-band equipment package.

The antenna mounted RF electronics subassembly, shown in Figure 2-5, has the following major characteristics:

Transmitter

Output frequency	14.65 GHz
RF power output (1)	6 watts (one TWT); 20 watts (two TWT's)
RF bandwidth	200 MHz
Input frequency	2.2825 GHz
Input RF drive required	1 MW
Input RF impedance	50 ohms

(1) When one TWT power amplifier is used. When two are connected in parallel, power output will be a minimum of 20 watts. Single TWT operation operated in the two tube circuit results in a 3 db loss in the hybrid circuit.

Receiver

Input frequency	13.6 GHz
Input RF signal level	83 dBm
RF bandwidth	200 MHz
Receiver system noise figure	<7 dB
Output frequency	2.1018 GHz
Output S-band power level	-33 dBm (min.)
Output RF impedance	50 ohms

2.3 TECHNOLOGY GOALS

Detailed design of the antenna-mounted electronics subassembly was based on the performance requirements that were structured from a set of technological goals established by NASA. Evaluation of this equipment and its operation will define the adequacy of these concepts for application to the MSS communications terminal design. An effective laboratory and operational test program and the resultant evaluation will provide data for avoidance of future design and operational problems.

The total CTB can be expanded to address other technical and operational problems associated with future concepts and practices for the MSS communication terminal. Addition of RF switching, S-band terminals, and the associated baseband switching would allow evaluation of frequency spectrum management, simultaneous multiple links, and EMI problems.

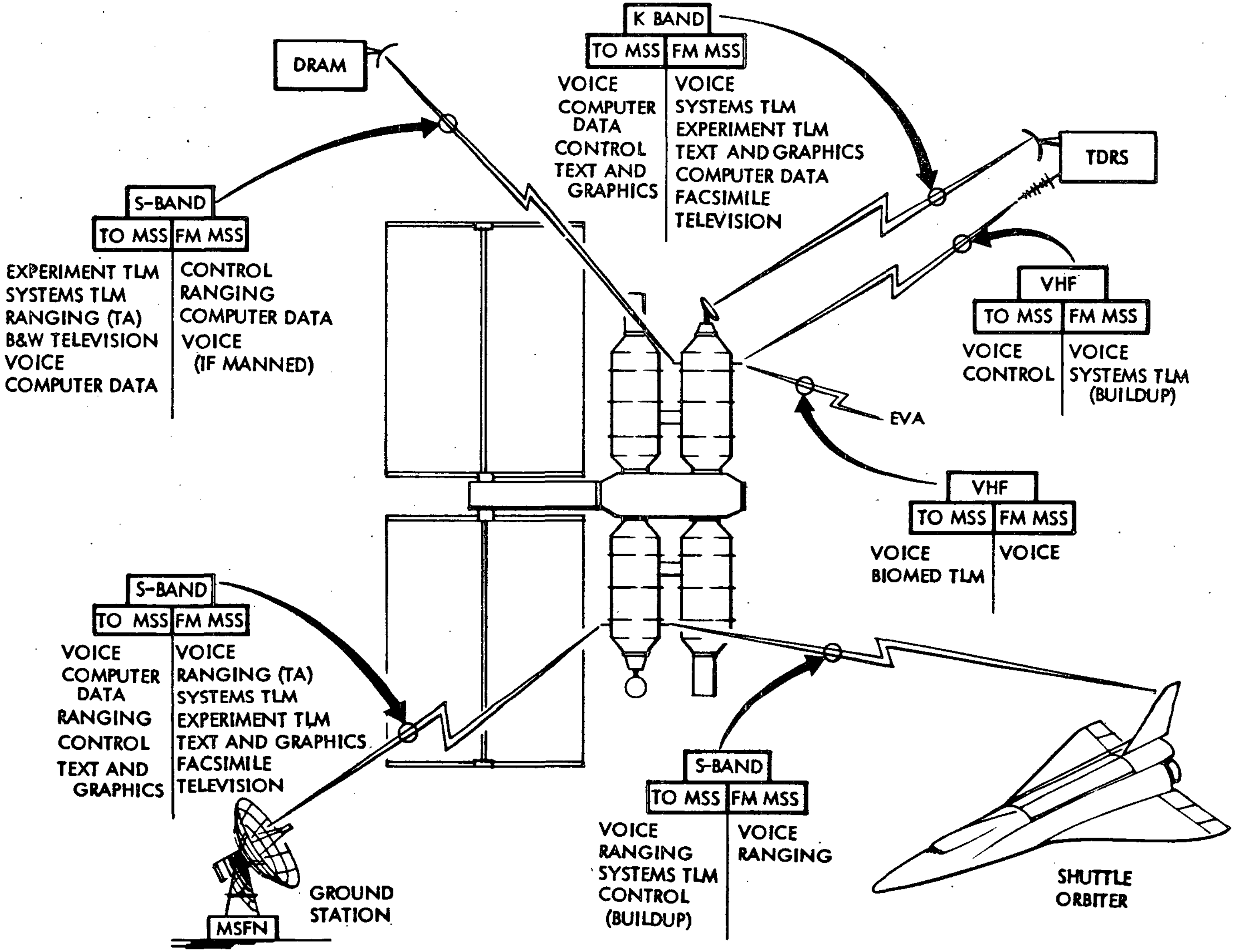

Figure 2-1. External Communication Link Requirements

Table 2-1. External Communication Data Characteristics

		RF Channel	Voice	Television	System TLM	Computer Data	Experiment Data	Text/ Graphics	Command Data	EVA TLM	Facsmile	Ranging: Measure	Ranging: Respond
From Space Station To	Detached RAM	S-band	(1) 300-4000 Hz						10 kbps			0.5 mbps	
	Shuttle orbiter	S-band	(1) 300-4000 Hz		50 kbps							0.5 mbps	0.5 mbps
	MSFN ground terminal direct	S-band	(3) 300-4000 Hz	4.5 MHz	500 kbps	500 kbps	2.0 mbps	1.0 kbps		200 bps			0.5 mbps
	Ground terminal via TDRS	VHF	(1) 300-4000 Hz		10 kbps								
	Ground terminal via TDRS	K-band	(3) 300-4000 Hz	4.5 MHz	500 kbps	500 kbps	2.0 mbps	1.0 kbps		200 bps	0.5 MHz		0.5 mbps
	EVA	VHF	(1) 300-4000 Hz										
To Space Station From	Detached RAM	S-band	(1) 300-4000 Hz	2.9 MHz	50 kbps	500 kbps	Part of system TLM						0.5 mbps
	Shuttle orbiter	S-band	(1) 300-4000 Hz						1.0 kbps			0.5 mbps	0.5 mbps
	MSFN Ground Terminal Direct	S-band	(4)* 300-4000 Hz			500 kbps		1.0 kbps	1.0 kbps			0.5 mbps	
	Ground Terminal via TDRS	VHF	(1) 300-4000 Hz						1.0 kbps				
	Ground Terminal via TDRS	K-band	(4)* 300-4000 Hz			500 kbps		1.0 kbps	1.0 kbps				
	EVA	VHF	(1) 300-4000 Hz							200 bps			

*One of the four voice channels - ground to MSS - is a high-fidelity channel 30-10,000 Hz for entertainment.

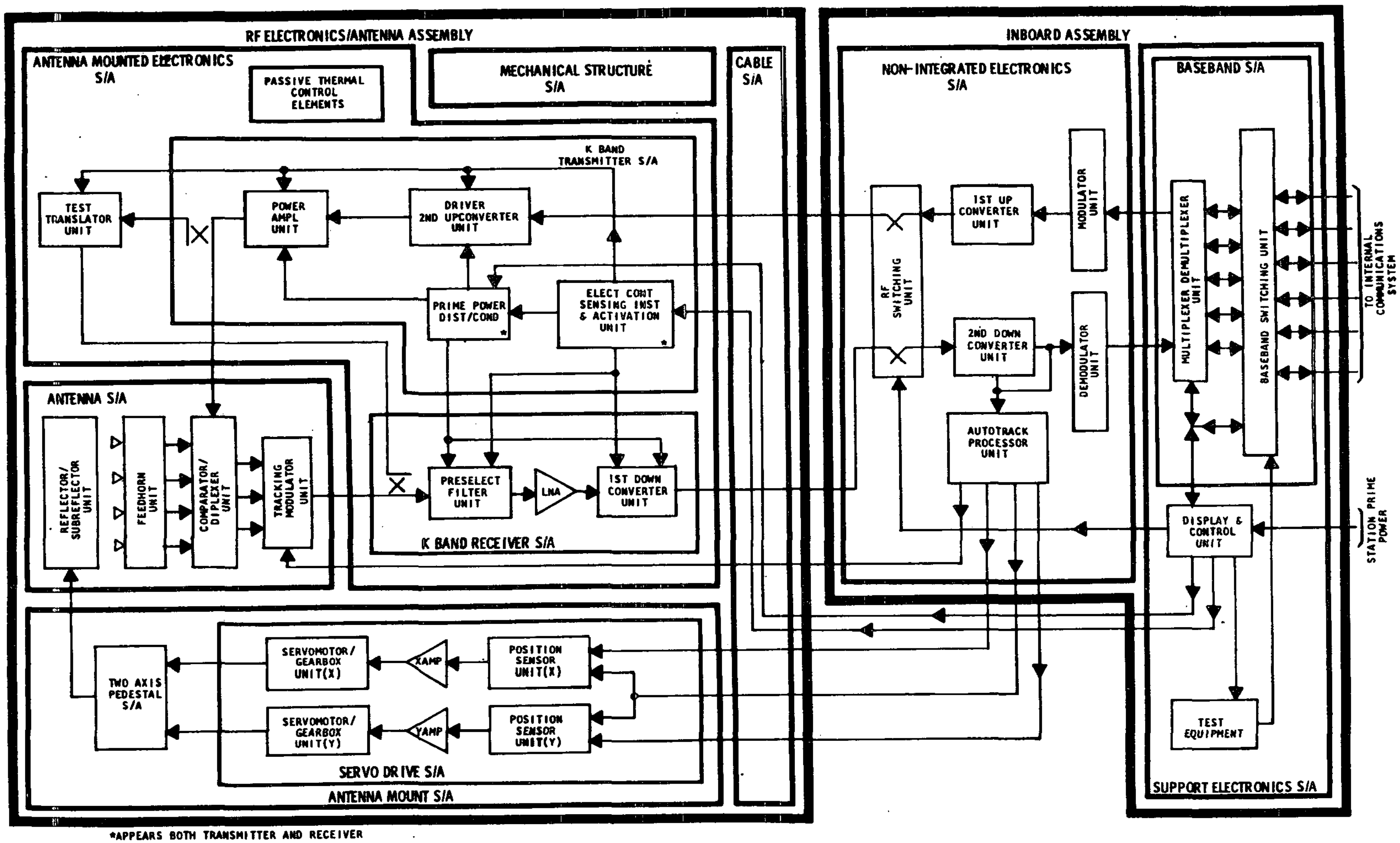

Figure 2-2. Communications Terminal Breadboard, Block Diagram

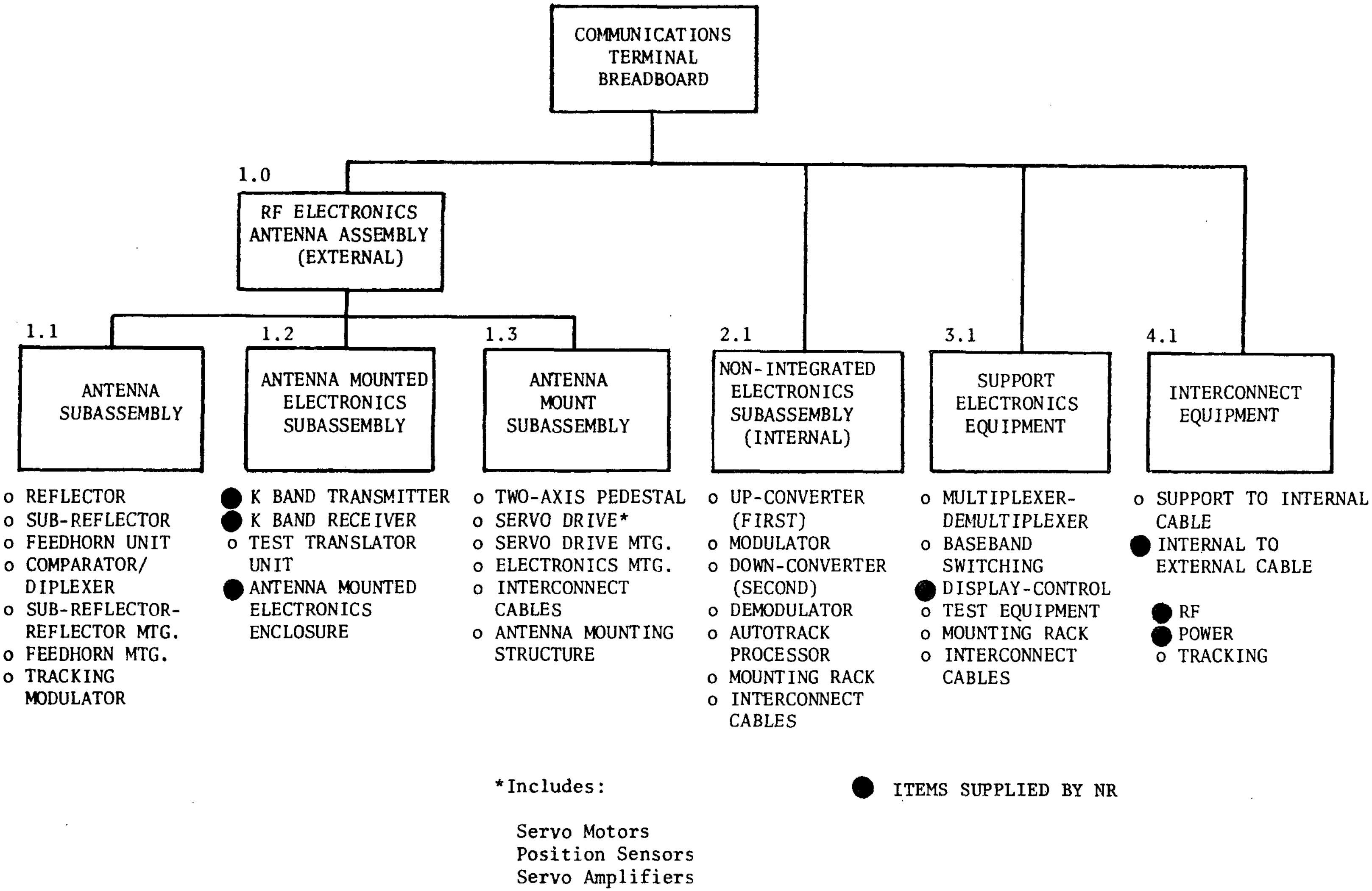

Figure 2-3. CTB Hardware Identification

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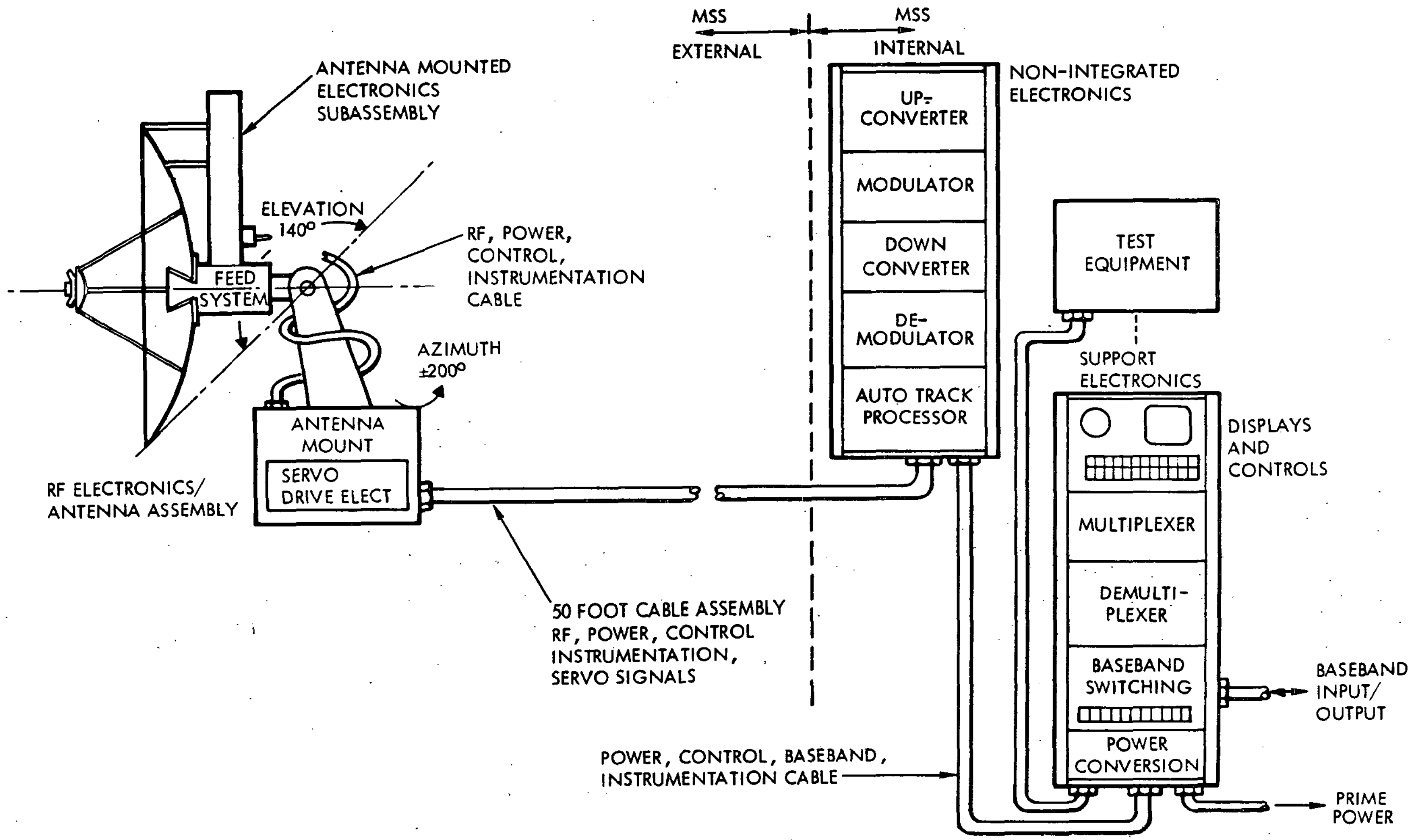

Figure 2-4. Communications Terminal Breadboard System (CTB)

ITT 69918

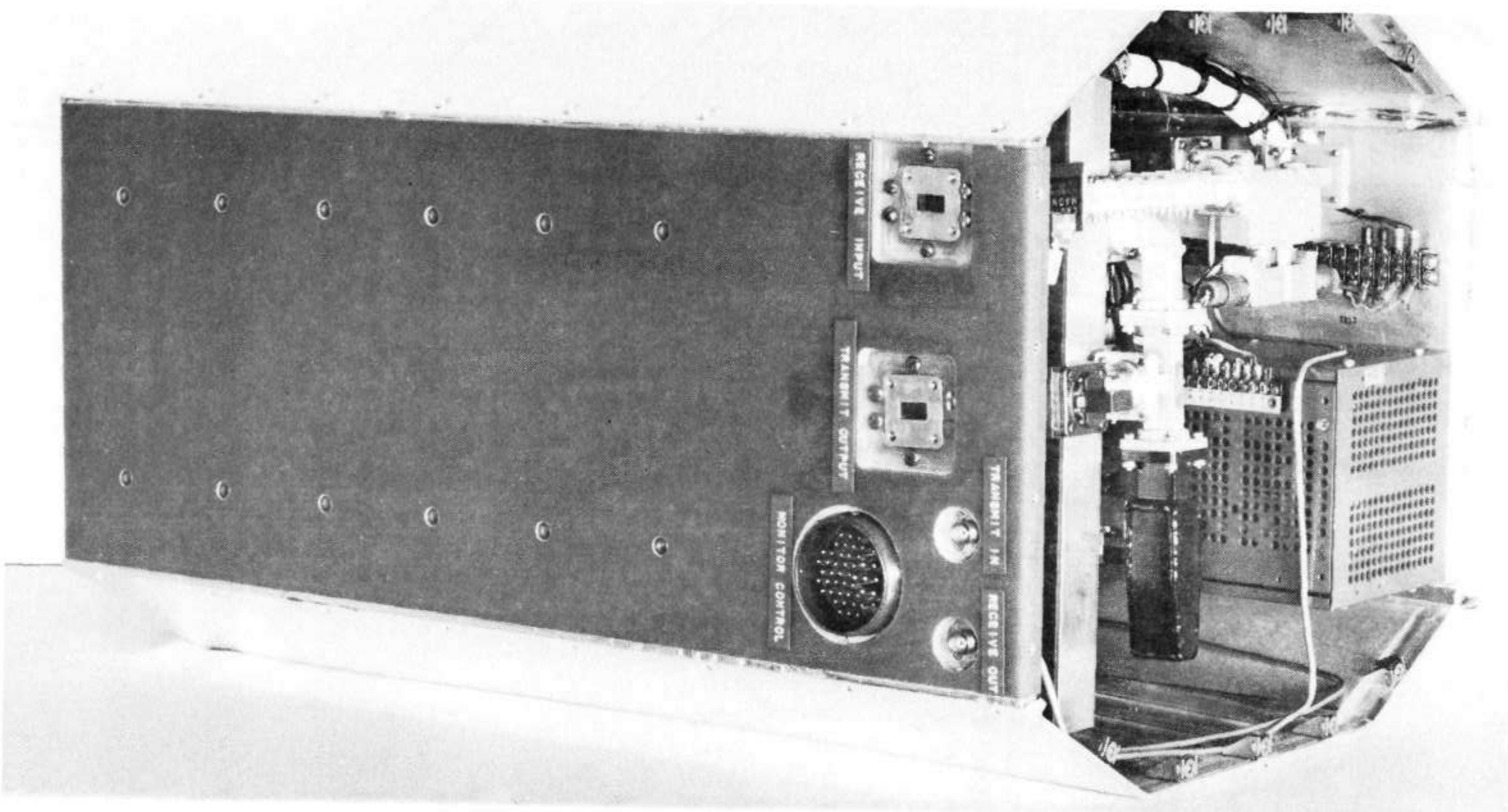

Figure 2-5. CTB Antenna Mounted Electronics Subassembly Package - Oblique View, Mounting and Interconnect Face

As indicated by the technology goals, CTB/antenna compatibility and techniques for automatic checkout and control can be investigated by means of the equipment specified herein.

2.4 HISTORY

At the inception of this program, the CTB was conceived as an S-band system with a solid-state, 20-watt transmitter power amplifier. With the development of the TDRS concept as the high-data rate relay satellite for MSS to ground, it was decided to change the emphasis for operational frequency to K-band - the TDRS frequency band. S-band equipment of the type proposed was already available as off-the-shelf type equipment. K-band equipment with a 20-watt RF transmitter power output and low noise K-band receiver equipment needed to be developed and evaluated. These factors led to the decision to design and build a K-band system after the statement of work had been negotiated with ITT for the CTB. Final negotiations with MSC and ITT resulted in reduction of analysis tasks and complete emphasis on the development, design, production, test, and delivery of the K-band, antenna-mounted RF electronics assembly. Full use was made of concept development activity in the specification of K-band hardware. This more closely followed the intent of the program - the demonstration of required new technologies.

3.0 DIGITAL DATA BUS BREADBOARD

3.1 DACS REQUIREMENTS SUMMARY

In the Modular space station, the data processing assembly (DPA) is highly distributed. The concept of two pressure volumes results in the division of the central processor between two control centers in such a way that the computations associated with station operations and experiments can be performed in either volume. Similarly, the subsystems and experiments are divided between the two pressure volumes; and what is more, the subsystems are distributed throughout the modules that make up a 6-man or a 12-man configuration. Some of these subsystems require on-the-spot computations; these are provided in the DPA design by remote processing units (RPU's). All subsystems require computational support from the DPA. Therefore, the DPA must acquire data from these distributed subsystems and return data, instructions, and commands.

A significant portion of the ADT effort has been devoted to the analysis and breadboarding of a data acquisition and control subassembly (DACS) to provide the necessary interflow of data between the two central processors, the subsystems and the experiment equipment. The DACS has been defined to include the digital data bus (DDB), the data bus control unit (DBCU), and the remote acquisition and control unit (RACU). Two of these have been analyzed and breadboarded as a part of the ADT effort; these are the DBCU and the DDB.

Figure 3-1 presents the task breakdown and flow which was followed in ultimately delivering breadboards of the DBCU and the DDB. Note that a RACU/RPU breadboard is government-furnished equipment (GFE).

The primary objective of the DACS breadboard is to verify the digital data bus concept for the modular space station. It will demonstrate the availability of technology to provide accuracy of data transfer, reconfigurability, failure tolerance, long useful life, and standardization of interfaces.

The data acquisition and control analyses began with a theoretical analysis of the parameters pertinent to the design and usage of data buses. The result of this analysis was a design handbook covering the significant aspects of wide-band digital and analog data buses. A model was defined for the data acquisition and control subassembly (DACS) breadboard. The purpose of this definition was to provide data to serve as a basis for the design of a DACS breadboard. It identifies the objectives of the breadboard, some potential vehicle related design problems, and a simplified implementation concept.

The analysis of DACS redundancy concepts covers the advantages and disadvantages of a general range of concepts and methods applicable to the DACS. Recommendations of methods were made and justified. The overriding requirements were found to be the single and triple failure tolerance requirements and

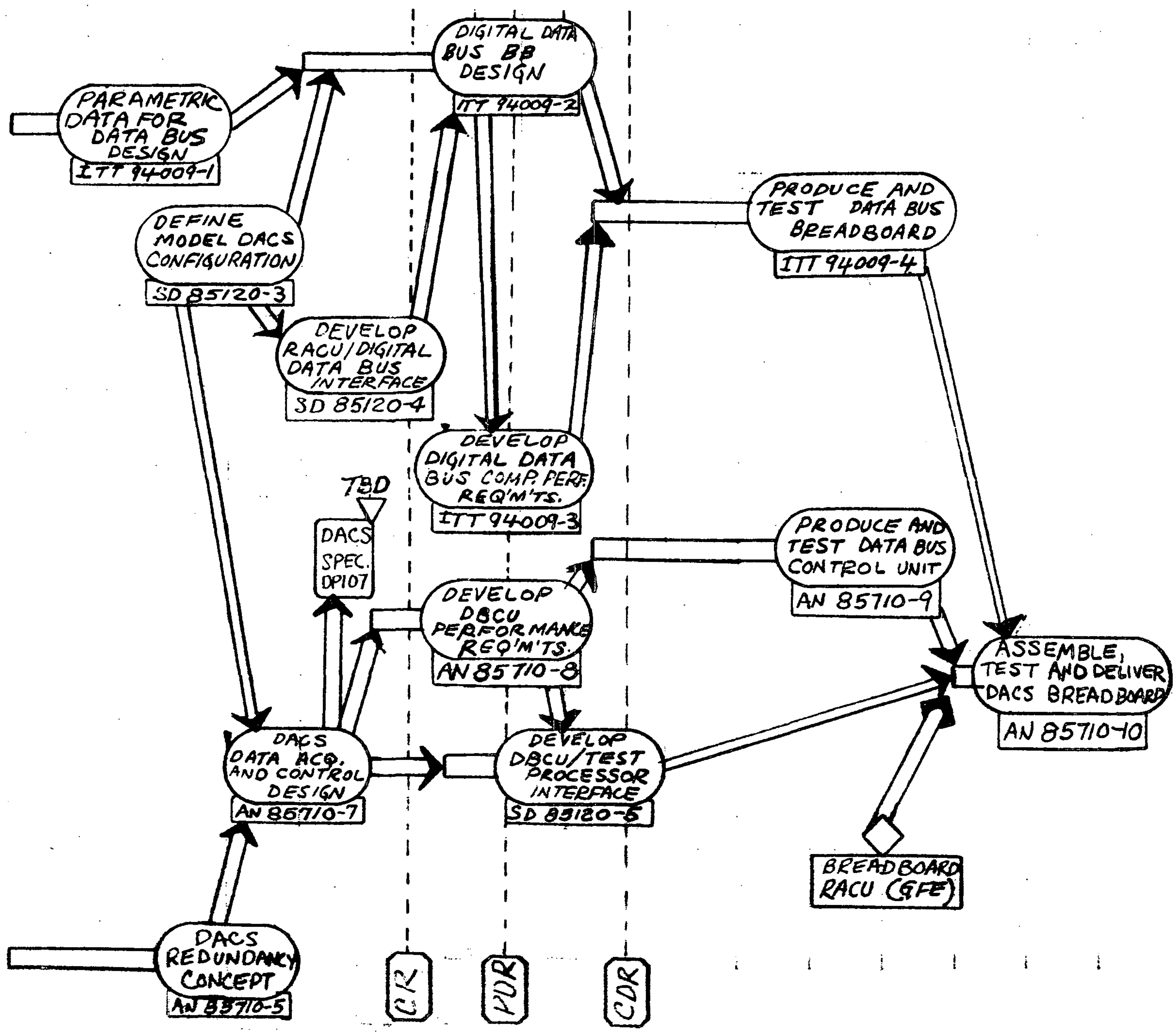

Figure 3-1. DACS Work Breakdown and Flow

the physical separation of redundant subsystems into pressure isolatable volumes.

The recommendations for the degree, level, and type of redundancy for each DACS element are presented in Vol. III. These recommendations include the split between hardware and/or software techniques, the utilization of error protection coding, the replacement/repair methods and a definition of the replaceable items, and the rationale for each selected candidate DACS element.

The following redundancy requirements were imposed on the station subsystems:

1. A capability must be provided for each non-critical function to fail safe for the first failure.

2. For a critical function a capability must be provided for:

   a. Full operation subsequent to a first failure (fail operational)
   b. Reduced or out-of-spec performance subsequent to a third failure (fail emergency)

3. Time critical functions require active (on-line continuous operation) redundancy. Non-time critical functions require at least standby redundancy (wired in and activated with automatic or manual switchover.)

Figure 3-2 presents the recommended implementation of the DACS that will satisfy the failure criteria (redundancy requirements). The RACU interconnect is shown for one complete critical subsystem functional loop model Type B. Only a small portion of the data bus assembly DB-1 is shown. The RACU interconnect, as recommended and pictured, allows two of the RACU's and their associated subsystem functional loop to be in a standby mode while the other two are active. This is true for both time-critical and non-time critical models of Type B.

The overall recommended DACS utilizes parallel and serial redundancy in many combinations. Distributed and functional redundancy are utilized to the extent possible. BITE is used extensively to aid in failure detection and isolation. Serial redundancy is used for transient error protection throughout the subsystem. The DPA multiprocessor and its software is utilized for all higher level BITE analysis, failure determination, fault isolation and crew notification for repair by replacement.

This recommended DACS configuration is very sensitive to the two basic overriding requirements; these are the single- and triple-failure tolerance requirements and the separation of all redundant items into two pressure isolatable volumes. The recommendations are also quite sensitive to the IFRU maintenance philosophy and somewhat sensitive to the other critical function requirements.

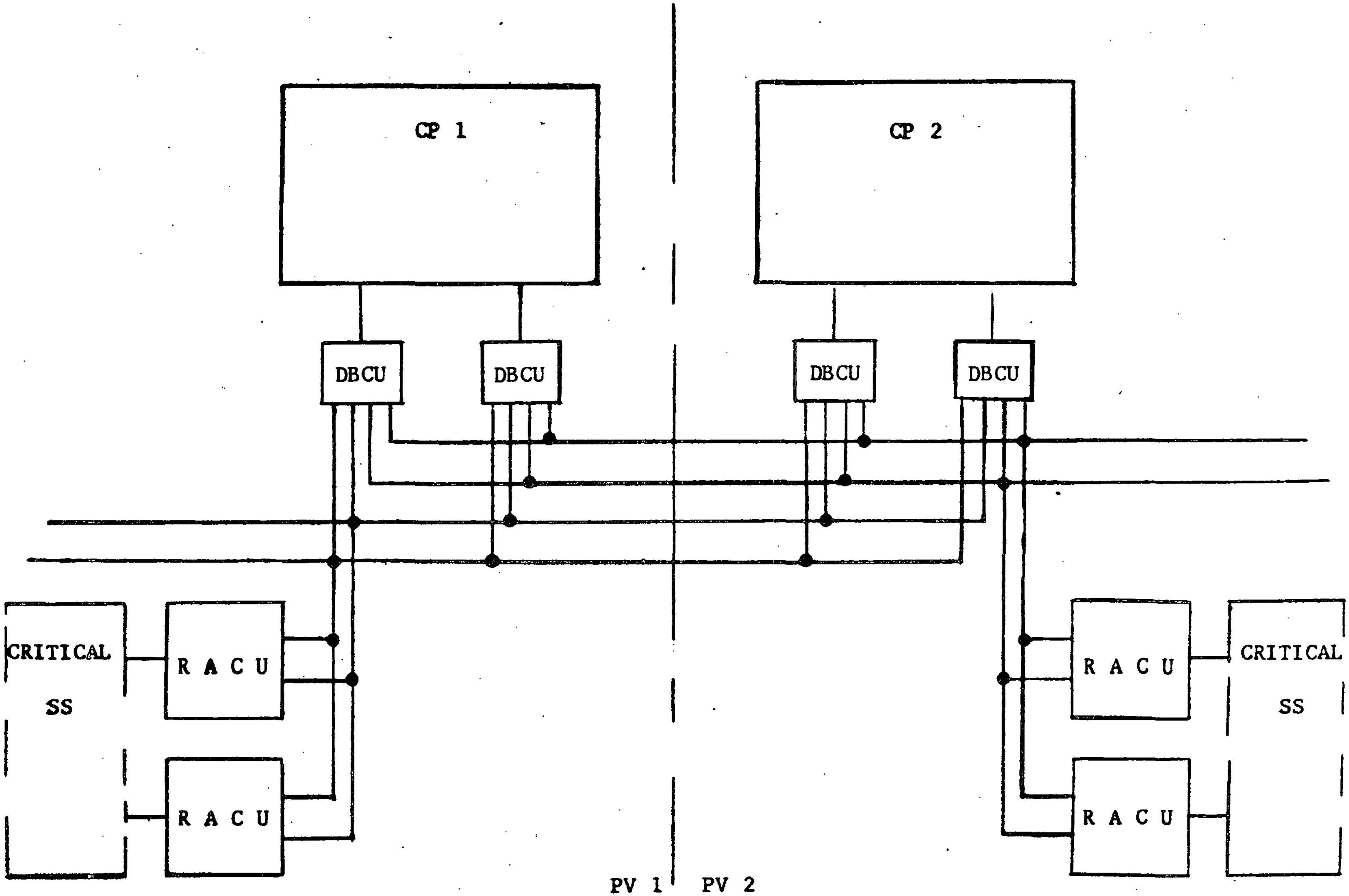

Figure 3-2. Recommended DACS Configuration

3.2 DACS BREADBOARD DESIGN

The DACS breadboard is an engineering model that is representative of the concepts for the data acquisition and control function for the data processing assembly of the modular space station. NASA defines a breadboard as a unit which performs the same functions according to the same characteristics as those defined by the hardware design.

A data acquisition and control subsystem is a semi-autonomous subsystem that provides controlled communication between a large number of remote locations and a control location. Insofar as possible, the DACS breadboard is an engineering model representative of the concepts for the data acquisition and control subassembly for the data processing assembly of the Modular Space Station. The DACS breadboard also provides a test bed for operational performance evaluation of numerous concepts for this type subsystem oriented toward the specific needs and requirements imposed by the Modular Space Station.

The overall breadboard concept for the DACS is a highly flexible, configuration-independent, building-block approach. This approach allows a large number of different DACS configurations to be assembled as an operating data acquisition and control subsystem breadboard. Each configuration concept can then be operated, tested, and evaluated for overall DACS concept and performance suitability.

Six basic types of units, plus additional test equipment comprise the DACS breadboard. These are the following:

a) Breadboard Modem Unit(s)
b) Core Bus Interface Unit(s)
c) Equipment Bus Interface Unit(s)
d) Interconnecting Cable(s)
e) Breadboard RACU(s)
f) Breadboard DBCU
g) Special Breadboard Test Equipment

The DACS breadboard was designed within the limits of the following constraints:

a) The DACS breadboard shall operate as a self-contained entity without the need for external intervention but under external command, control and influence.
b) Operation of the DACS breadboard will be internally controlled by the Data Bus Control Unit (DBCU).
c) All control interaction with the DACS breadboard from external sources will be through the DBCU.
d) All breadboard performance evaluation will be provided external to the RACU's, DBCU's, and the data bus breadboard units.
e) The breadboard shall operate with a fixed word length of 8 bits.
f) The breadboard shall operate with a variable size message structure in all modes, of from zero to 124 data words.
g) Hardware error detectionand encoding shall be provided.
h) The breadboard units will contain provisions for both fixed and variable coding and decoding of internal commands and data.

i) All hardware breadboard units shall have a standard disconnect/interconnect scheme for ease of assembly into various configurations.
j) A method (or methods) shall be provided for simulating faults within the breadboard units.
k) Provision for test equipment and/or panels, for determining breadboard performance, shall be made.
l) All breadboards will be non-redundant; redundant breadboard operation will be achieved through the use of multiple breadboard units in redundant configurations, and DBCU/Test Processor operational control programs and interaction.
m) RACU and DBCU breadboards shall have internal power supplies operating from the primary power source.

The DACS breadboard was designed with the following considerations for hardware error protection.

a) Hardware shall be provided in both RACU and DBCU breadboard units to perform error protective encoding and detecting on a word or message basis. Correction is not necessary for the DACS breadboard since this can be evaluated off-line if desired.
b) The encoding or non-encoding of the data shall be selectable by external control.
c) Provisions shall be made to allow other coding schemes generated and detected external to RACU or DBCU to be passed through the RACU or DBCU.
d) The data so encoded shall be passed through to external devices in either the encoded or decoded from, or both, for other evaluation, and vice versa.

The data bus breadboard shall be designed within the limits of the following constraints:

a) The data bus breadboard shall be a self-contained time-division multiplexed communication link utilizing pulse code modulation over a hardwired transmission path.
b) Bi-phase level (Manchester) data encoding will be utilized by the breadboard for transmitting data and control bits.
c) The nominal operating frequency is 10 megabits per second.
d) The longest data source to sink distance is 400 feet.
e) The longest non-interrupted line segment is 125 feet.
f) The number of equipments utilizing the data bus assembly in the operating system total less than 150.

The breadboard modem units was designed within the limits of the following constraints:

a) Breadboard modem units include all circuitry necessary for bi-phase level modulation and demodulation, clock recovery from the bi-phase level modulated signal, bit timing, preamble decoding, and bus usage by a RACU or DBCU.

b) Breadboard modem units shall operate in a half or full duplex mode.
c) Breadboard modem units shall have the capability whereby the output power delivered to the line can be externally adjusted through a limited range including the minimum for data bus operation.
d) The breadboard modem unit interface with other DACS breadboard elements consists of serial digital NRZ data, serial digital clock signals and various DC control signals.
e) Equipments utilizing the breadboard modem units will be assumed in close physical proximity, i.e., less than five feet from the modem.

The RACU breadboard was designed with the following constraints:

a) The RACU breadboard shall provide the standard interface between the digital data bus modem breadboard and a simulated subsystem functional loop.
b) The RACU breadboard shall contain the circuitry necessary to accept standard format serial digital data and clock signals from the breadboard modem, to convert the data to signals which are compatible with the subsystem requirements, to generate the required control signals for both the subsystem and for data bus usage, to provide buffer storage for subsystem data, and to provide subsystem data to the bus on command converted to a standard serial digital format.
c) The RACU breadboard shall be mechanized to respond to two types of messages as listed below:

   (1) Message A - Transmit Data to DBCU
   (2) Message B - Receive Data/Commands from DBCU

   Responses shall be of three types; no response, acknowledge response, and acknowledge and accept DBCU verification.
d) Each RACU breadboard shall have two input (receive) interfaces and two output (transmit) interfaces with the data bus breadboard modem(s).
e) The RACU/modem interfaces shall have independent address recognition circuitry but are not required to have independent control.
f) A provision shall be made for an external test interface in serial digital form consisting of the data received via the data bus (output) and accepting data for transmission via the data bus (input).
g) The external serial digital test interface shall have provision for parity generation of data at its input or not, and similarly parity checking the output data or not, externally selectable.
h) Internal data word buffer storage of 128 words minimum shall be provided for input and output messages.
i) Data transfer to and from the breadboard modem shall operate at a nominal frequency of ten megabits per second.
j) The RACU breadboard shall operate at appropriate time from three clock sources; either the receive clock from the modem, its own internal clock, or an external clock source via the test interface.
k) A subsystem functional loop simulator interface shall have provision for variable numbers of DC analog and discrete signals to be multiplexed at varying sample rates, converted to digital form, and formatted.

l) Special provision for local indication of responses to non-data commands from the DBCU should be considered.
m) Provision shall be made for an external preprocessor interface.
n) RACU addresses shall be externally pre-set.
o) All RACU operation will be under higher level control by the DBCU. Operation will be specified by the DBCU commands in each message. RACU operational sequences can be performed by hardware and/or software techniques.
p) A provision for variable decoding of DBCU commands shall be included to allow changing RACU operational modes and command responses.

The data bus control unit breadboard shall be designed within the limits of the following constraints:

a) The DBCU shall provide all command and control capabilities for fully exercising the DACS breadboard.
b) The DBCU breadboard shall contain the circuitry necessary to originate and control all messages for the DACS breadboard, to communicate with RACU breadboards via the breadboard modem units and data bus and to operate the DACS breadboard with or without test processor interaction.
c) Two types of messages shall be originated by the DBCU breadboard as listed below:

    (1) Message A - Request Data from an RACU
    (2) Message B - Transmit Data/command to an RACU

d) The breadboard DBCU shall have dual, switch selectable, interface capability for communicating with breadboard modem units.
e) Provision shall be included for an external test I/O interface consisting of serial digital data for transmission to RACU's and data received from RACU's.
f) The external serial digital test interface shall have provision for parity generation and detection of I/O data or not, externally selectable.
g) Internal data word storage shall be provided for message data sequences and buffering (minimum size of 128 words).
h) Data transfer to and from the breadboard modem units shall operate at a nominal frequency of ten megabits per second.
i) The DBCU breadboard shall operate at appropriate times from any of three clock sources; the receive clock from the modem, an internal clock source, or an external clock source via the test interface.
j) Message generation shall be under internal program control, including such message options and factors as message type, message size, RACU acknowledge, command verification, data retransmission, procedures for operation with errors detected and improper response conditions, and interaction with external equipments.
k) The internal DBCU breadboard operational program shall be both externally selectable and changeable via the test processor, test panel and breadboard user.
l) A test processor and test panel interface shall be provided for parallel and/or serial digital data transfer and DBCU (and therefore DACS breadboard) higher level control.

m) The DBCU breadboard shall be capable of providing internal operation status and DACS breadboard operational status data to the test panel and/or test processor. This status data will include that obtained from the RACU's, data bus breadboard status, the DBCU status, the errors detected, the operational DACS control modes being utilized (see item j), and improper DACS breadboard operation.

Figure 3-3 illustrates a laboratory configuration of the DACS breadboard. It will be possible with this breadboard, then, to evaluate wideband digital data bus operation (10 Mbps), automatic fault detection and isolation, automatic reconfiguration, techniques for executive control of data traffic, etc.

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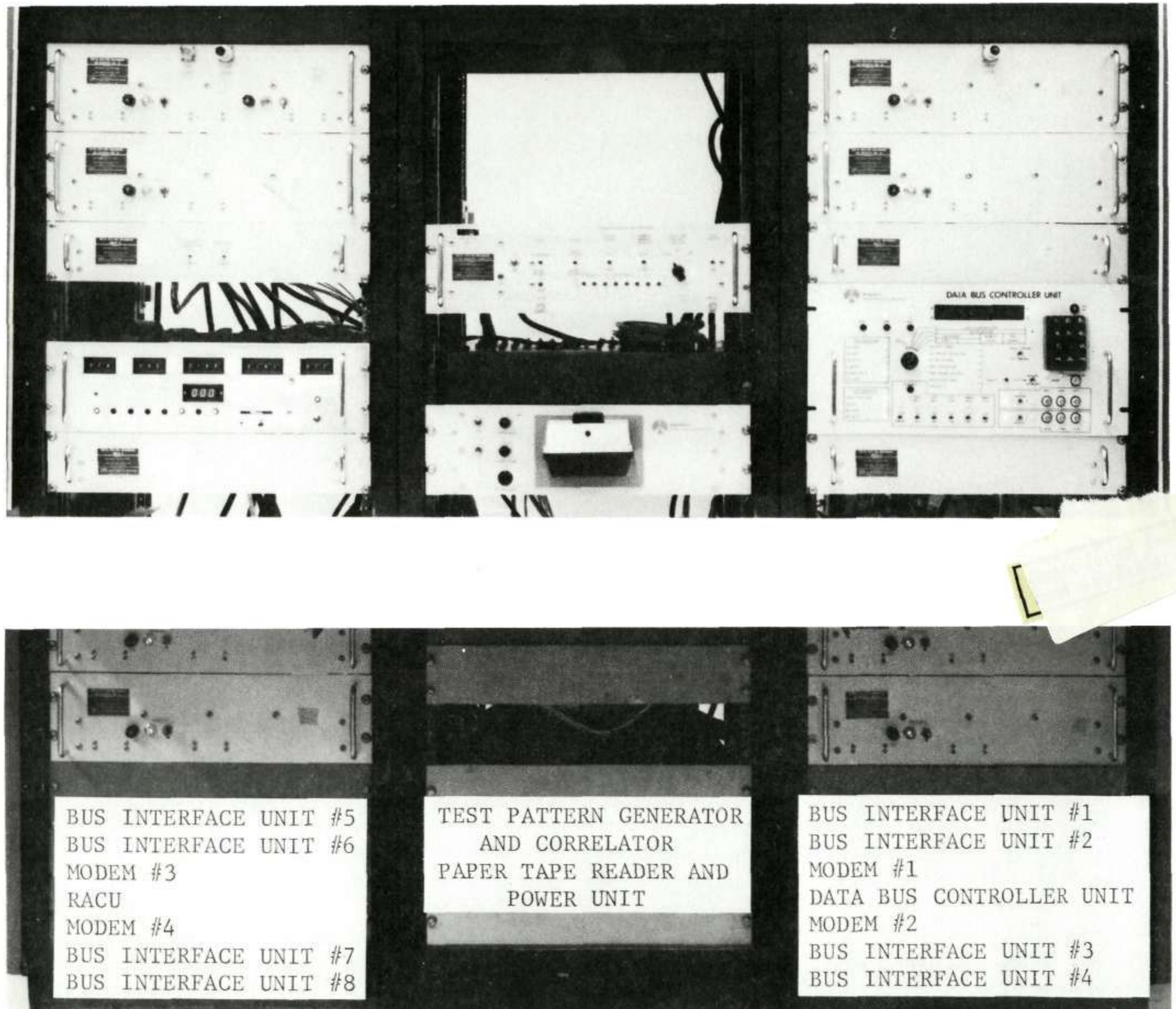


Figure 3-3 DACS Breadboard Configuration

4.0 DATA PROCESSING ASSEMBLY DEFINITION

4.1 SUMMARY

The requirements for a long duration manned space station include continuous maintenance of operational capability with minimum crew participation. This requirement can be achieved by automating operations of the subsystem functions with use of a computer system, referred to as the data processing assembly (DPA). Figure 4-1 represents the modular space station (MSS) DPA configuration. The computations required may be performed in a number of ways. The concepts, performance mechanization, reliability, and cost are sensitive to the amount of automation required.

Volume IV of this report summarizes the efforts directed to defining the DPA data input/output requirements and traffic flow patterns, allocating of logical and computational functions for the development of information flow diagrams, and defining a DPA configuration.

The approach taken was to (1) define the computation and logical functions which must be performed by the data processing assembly (DPA) for the orbital operations, (2) define in preliminary form the memory size and computer speed required to accomplish these functions, (3) allocate computations and logical operations to elements of the DPA, (4) develop preliminary flow diagrams which portray the information flow rates and functions performed by the DPA and its input/output interface with the MSS subsystems and (5) define a DPA configuration.

Figures 4-2 and 4-3 present the configuration selected for the data processing assembly. As noted, the station operations central processor is located in the primary control module (SM-1). Supervisory control of the equipment in the power and core modules is provided via a radio link during station buildup prior to SM-1 arrival. A special component (buildup data processor) is located in the core module for interfacing with the radio link and DPA. This component will be removed or disengaged when SM-1 arrives and supervisory control is exercised by the station operations control processor.

The baseline configuration is further shown to consist of remote processing units (RPU's) performing subsystem functions and failure detection. A redundant bus network connects these and the remote acquisition and control units (RACU's) to the central processor. A multiprocessor organization has been defined as the most suitable for the central processor. Redundancy at the central control level is further supplied by another central computer containing the critical operations functions and experiment support software. This second central processor is located in another pressure volume (SM-4) and is identical to the primary computer. The RPU's consist of uniprocessors with special input/output processing or signal processing as required to accommodate the subsystem functional requirements.

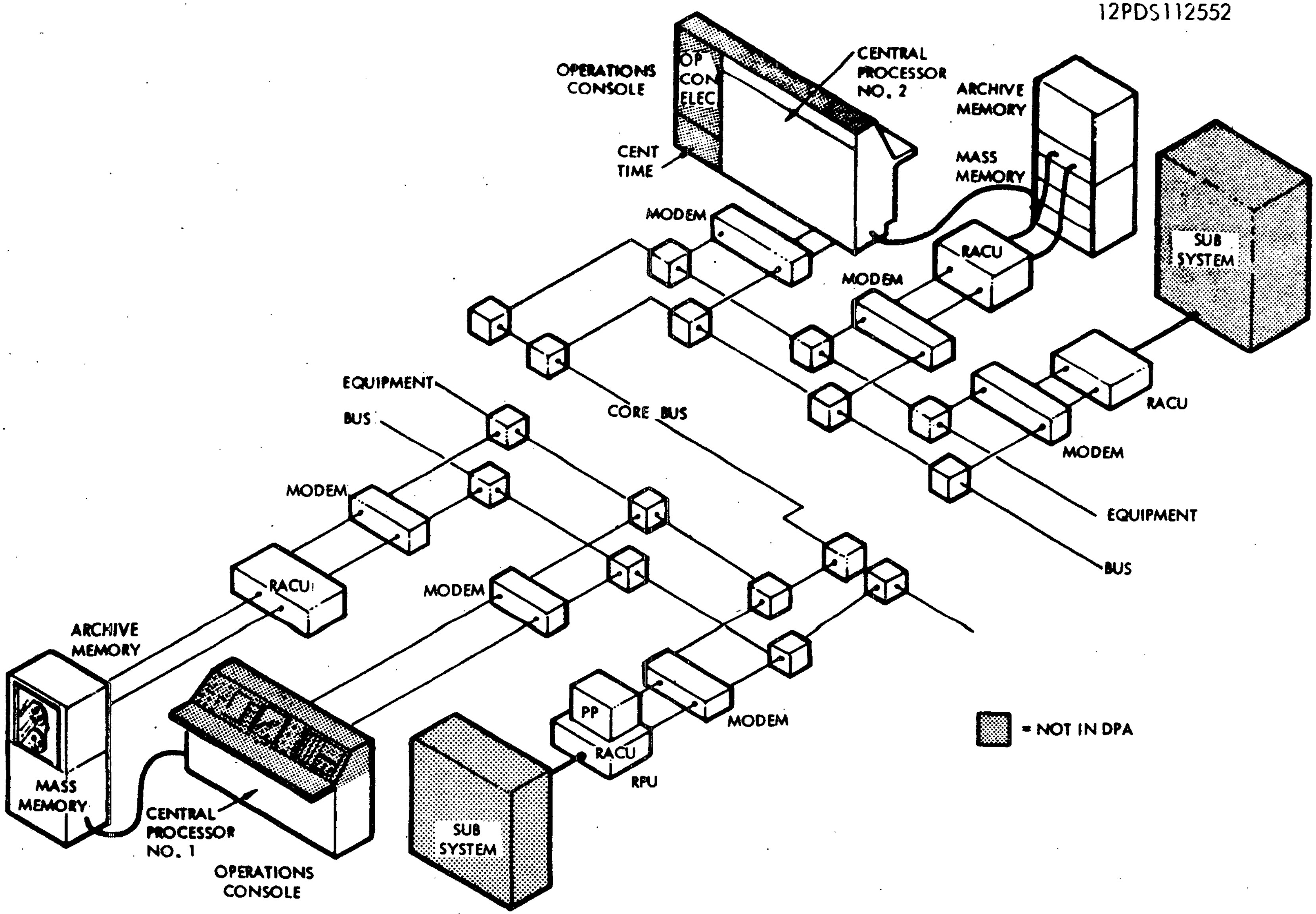
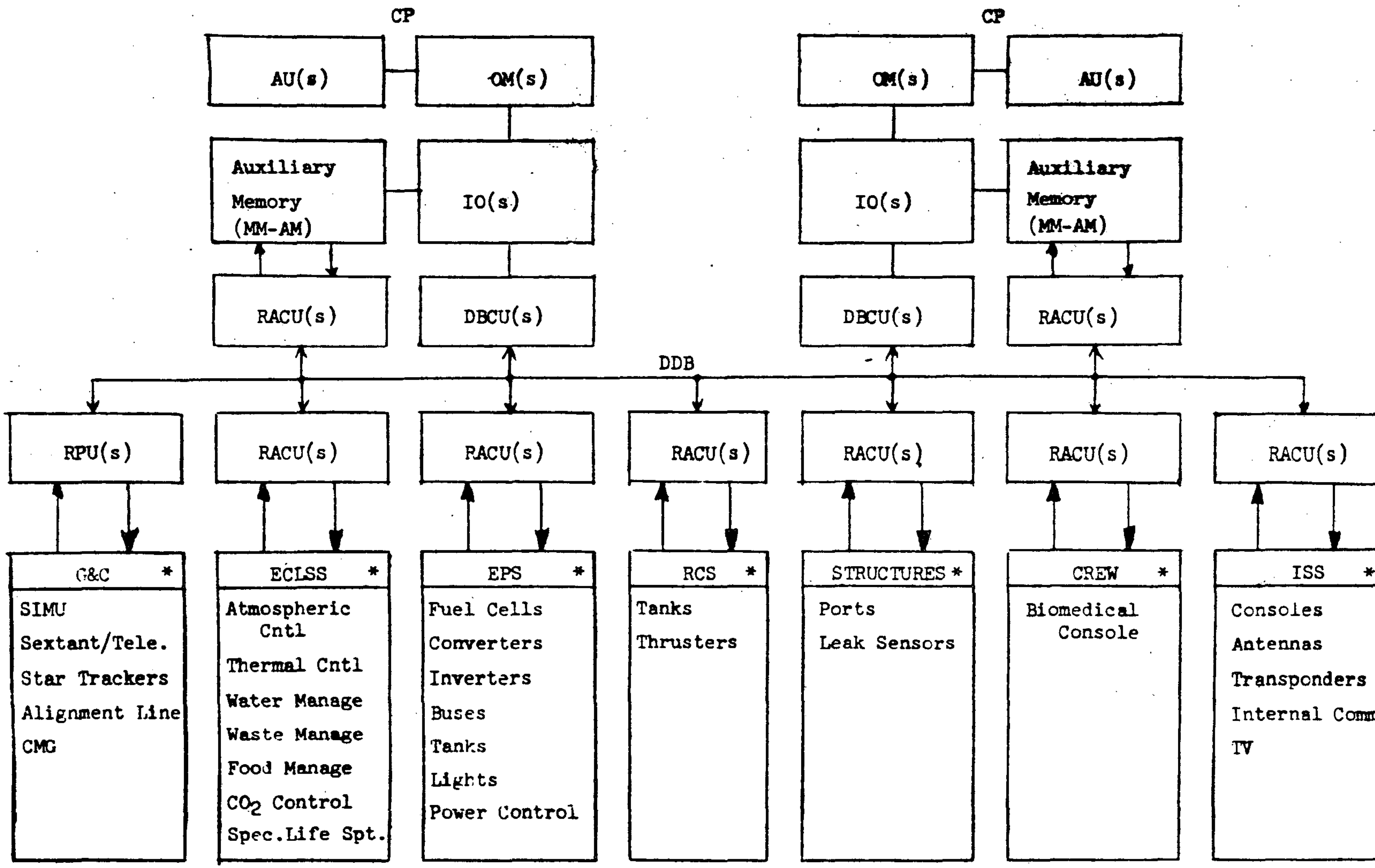


Figure 4-1. Data Processing Assembly (DPA)



*NOT PART OF DPA

Figure 4-2. DPA General Diagram

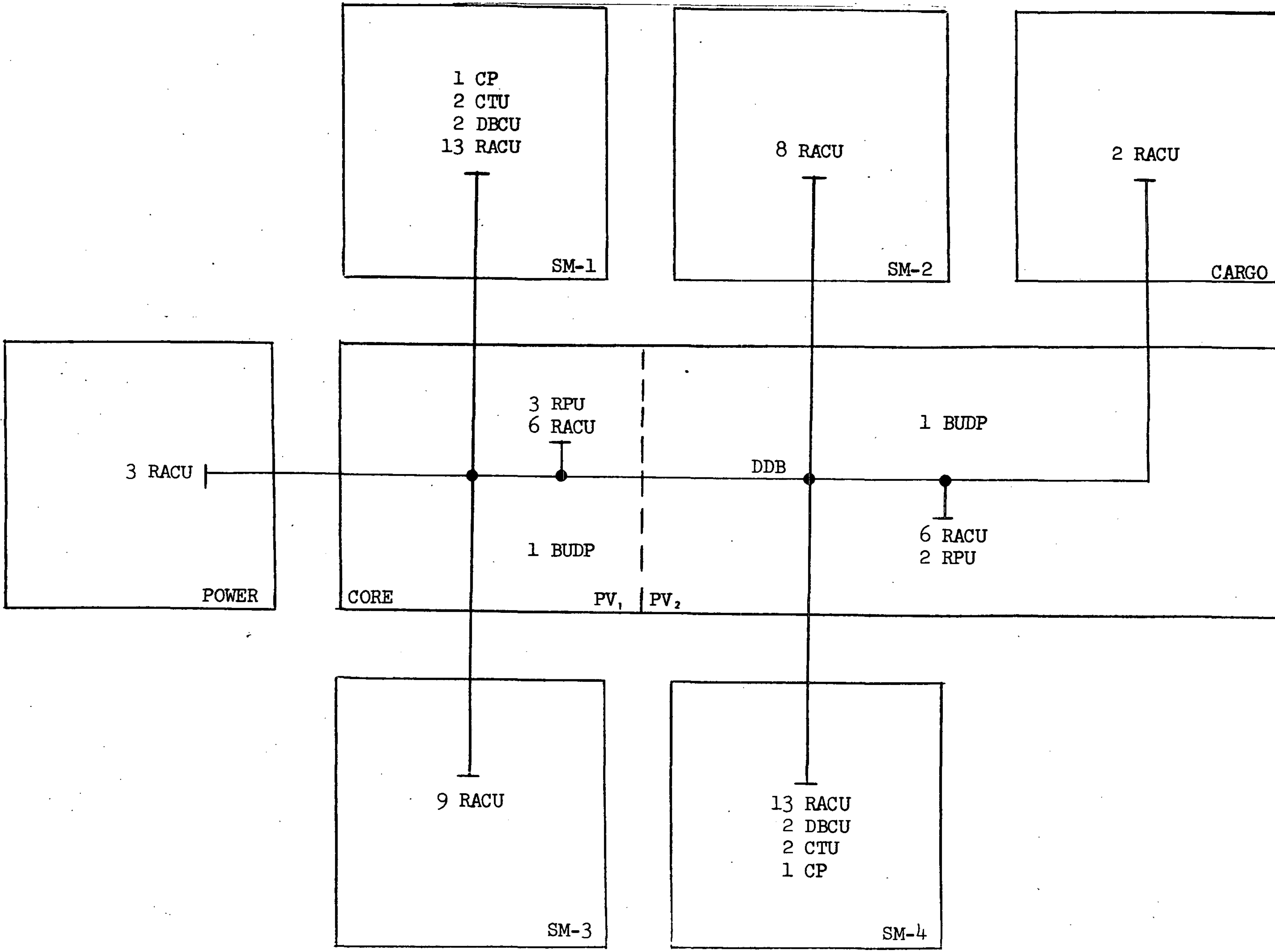


Figure 4-3. Data Processing Assembly Distribution

Figure 4-4 shows the tasks, their relationships, and the subcontractors who participated in each task. The impact of the simultaneous MSS Phase B study is also indicated. It will be noticed in reading this report (Volume IV) that many different values of memory size and operating speed are used. Basically, this is due to two factors: the DPA studies were impacted by the Phase B studies and the DPA studies were iterative (particularly as regards the selection of a DPA configuration). The most significant difference between two sets of DPA requirements is due to the ongoing requirements and subsystems analysis in the Phase B study. Once past the insertion of this large delta, the differences in assumed requirements is minor (not more than 10%) and does not significantly alter the DPA concept or the results of the study.

The study began with an analysis of the DPA requirements. This task defined the subsystems' functions which require data processing support; defined the mechanization required to provide data processing support for each identified function; estimated the memory, speed, and input/output data rates required for mechanization of each function; and integrated the subsystems' computation requirements to define a total set of MSS DPA requirements. Table 4-1 presents the performance requirements for station operations in parameters of processing speed, memory capacity, and data bus rate. Shown are the basic requirements, the design margin, the growth margin, the initial design requirements, and the maximum design requirements.

The next task was the definition of the baseline DPA configuration. The alternatives to be considered at each processing level were enumerated, and the distribution of the signals (subsystem interfaces) was tabulated on the basis of the physical distribution of the MSS subsystem. A tradeoff resulted in the selection of a central multiprocessor plus subsystem preprocessing as required. The multiprocessor-to-subsystem interfaces are to be implemented with RACU's which communicate with the central processor via a digital, time-serial data bus.

The purpose of the information flow study was to define the MSS DPA information flow so that the DPA could be simulated with NASA's IMSIM. A method of flow diagram and attendant tabulations presentation was carefully selected to provide a comprehensive data file of software and information characteristics that will prove beneficial in the continuation of the advanced development tasks and related studies. This data file consists of descriptions of each subsystem, baseline configuration data, buildup information, DPA computational loads and allocations, computer sizing information, message tabulations, signal interface lists, and DPA parametric data requirements.

The objective of the DPA throughput simulation was to provide information that would facilitate a selection of the final DPA configuration for the MSS; in particular, to provide information pertaining to DPA component performance that would yield a DPA configuration capable of accommodating imposed workloads within required response times.

The operational doctrine assumed to be in effect for the data bus is that of polling. Polling control is assumed to be a function of the I/O unit and the polling schedule is assumed to be on a fixed time basis per device. The

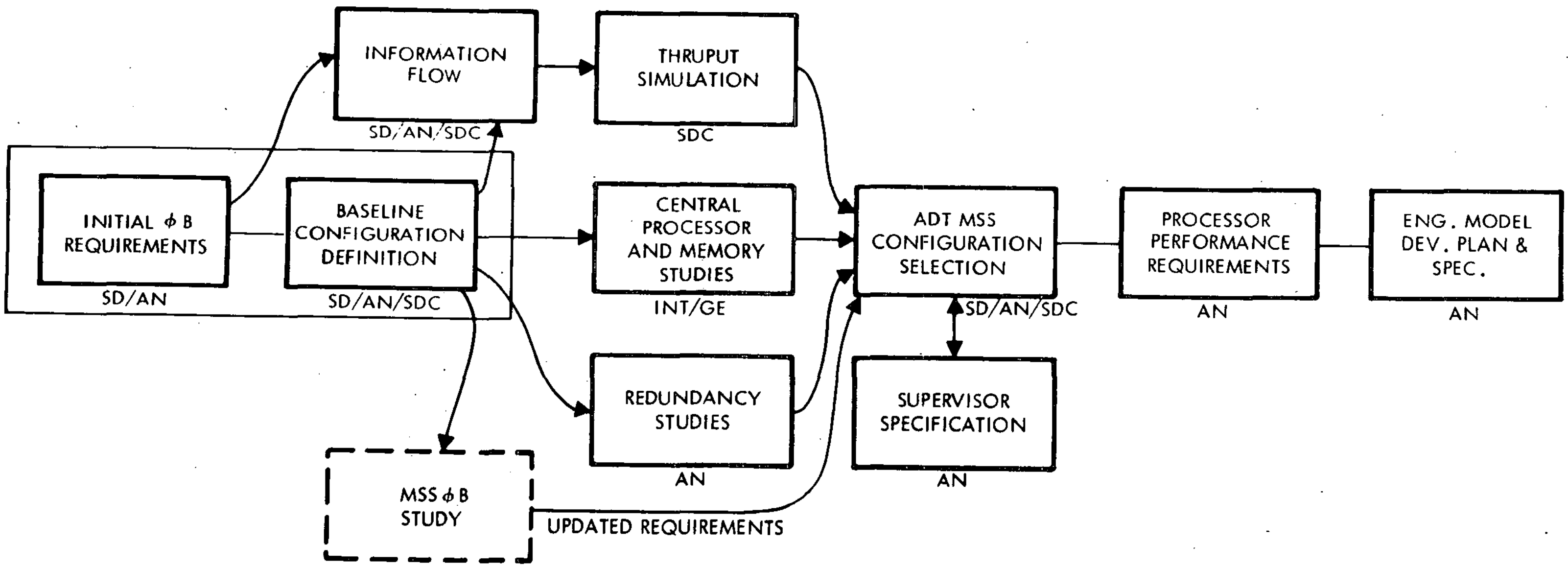


Figure 4-4. Data Processing Assembly Configuration Study

Table 4-1. Computation Requirements for Station Operations

Performance Requirements	Base Requirements		Maximum Requirements		Initial (6-Man) Requirements	
	Basic Requirements	Design Margin (100 percent)	Maximum Growth Margin (100 percent)	Maximum Design Requirements	Initial Growth Margin	Initial Design Requirements
Central processor Processing speed (Equivalent adds/sec)	631K	631K	631K	1893K	0	1262K
Operating memory (32 bit words)	67K	67K	67K	201K	0	134K
Mass memory (32 bit words)	341K	341K	341K	1023K	0	682K
Data bus rate (bits/sec) (1)	400K (Station Opn) 2000K (experiments)	400K	7.2M*	10M	7.2M	10M
Archive memory (32 bit words)	4.2M	4.2M	4.2M	12.6M	0	8.4M
Remote processingunit Processing speed (Equivalent adds/sec)	125K	125K	0**	250K	0	250K
Memory (32 bit words)	9K	9K	0**	18K	0	18K

* = Special allowance for experiments.
** = RPU growth will be accommodated by additional units.
(1) = IOC requirements is 2.8 Mbps

polling schedule assumed is predicated on dividing a second into 251 slots of 4 ms each.

Nine time slots (36 ms) were simulated; these were the initial nine slots of each one-second interval (250 slots) and were chosen for imposing the largest operational load on the DPA. Processor utilization during the execution of the simulation is shown in Figure 4-5. The simulations led to the following conclusions: the central processor can effectively process expected worloads; arithmetic unit speed of 750 KEAPS is adequate; the I/O processor is under-utilized at 750 KEAPS; a data bus commutation cycle of 250 slots per second is reasonable; the operating memory transfer rate of 2×10^6 words per second is adequate; and the mass memory transfer rate of 1×10^6 words per second is adequate.

The application of redundancy to the DPA stems from the failure criteria established for the MSS. The redundancy study was directed toward applying the criteria to the DPA concepts and recommending a satisfactory operational system. The recommended redundancy configuration is shown in Figure 4-6. The redundancy recommendations are shown in Table 4-2.

The objective of the central processor study was to determine the influence of the MSS central processor operational use and software organization on the design of the hardware aspects of the central processor. The architecture of the central processor was recommended to be as shown in Figure 4-7. The concept of a higher order language machine (HOLM) was studied as a basis for studying the central processor memory hierarchy and the internal bus design. Figure 4-8 shows the memory hierarchy which was studied for the MSS data processing assembly; Figure 4-9 presents the candidate internal bus configurations. Tables 4-3 and 4-4 summarize the conclusions reached during the study. Further analyses of fault tolerance for the central processor were conducted for the HOLM. The conclusions of those analyses are presented in Table 4-5.

Subsequent to the selection of a baseline DPA configuration, several of the influencing factors were changed as a result of the concurrent MSS Phase B definition studies. Most notable of these factors were the new buildup sequence for the MSS, the redefined DPA failure and error tolerance criteria, and the redefined computational requirements. The DPA configuration was redefined on the basis of these new factors and the studies that were completed (as shown in Figures 4-2 and 4-3). An analysis was also performed to determine the effects of a more efficient distribution of the processing tasks within the central processor between the arithmetic units and the input/output processors. Figure 4-10 presents a detailed allocation of the central processor functions which resulted from this analysis.

4.2 DPA DEFINITION

The data processing assembly (DPA) provides the computing functions needed for a high degree of reliable automation in the modular space station (MSS). The central processors and preprocessors are key elements of the DPA and must perform reliably and effectively over the life of the station. The processor performance requirements task covers the central processor and

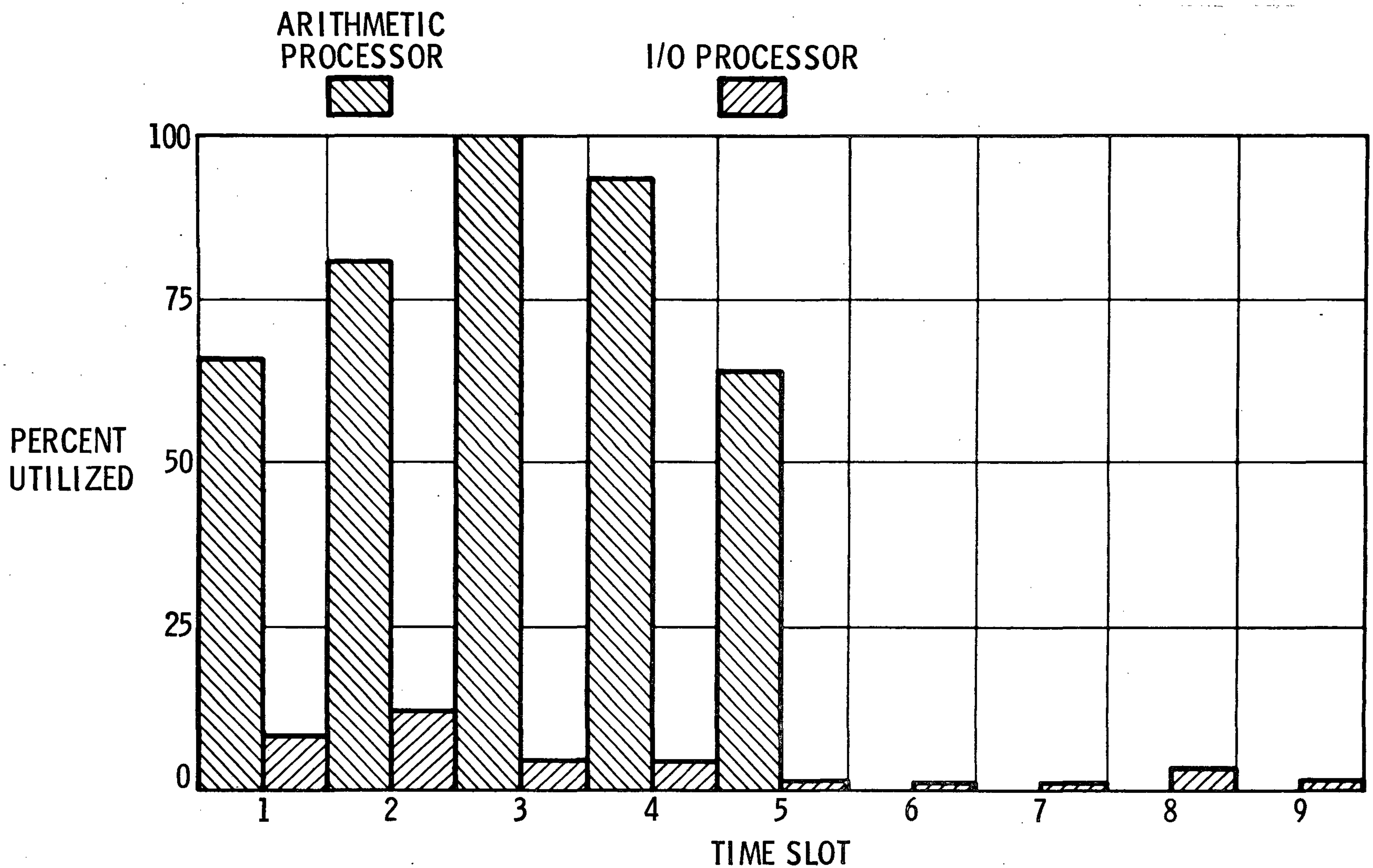


Figure 4-5. Processor Utilization

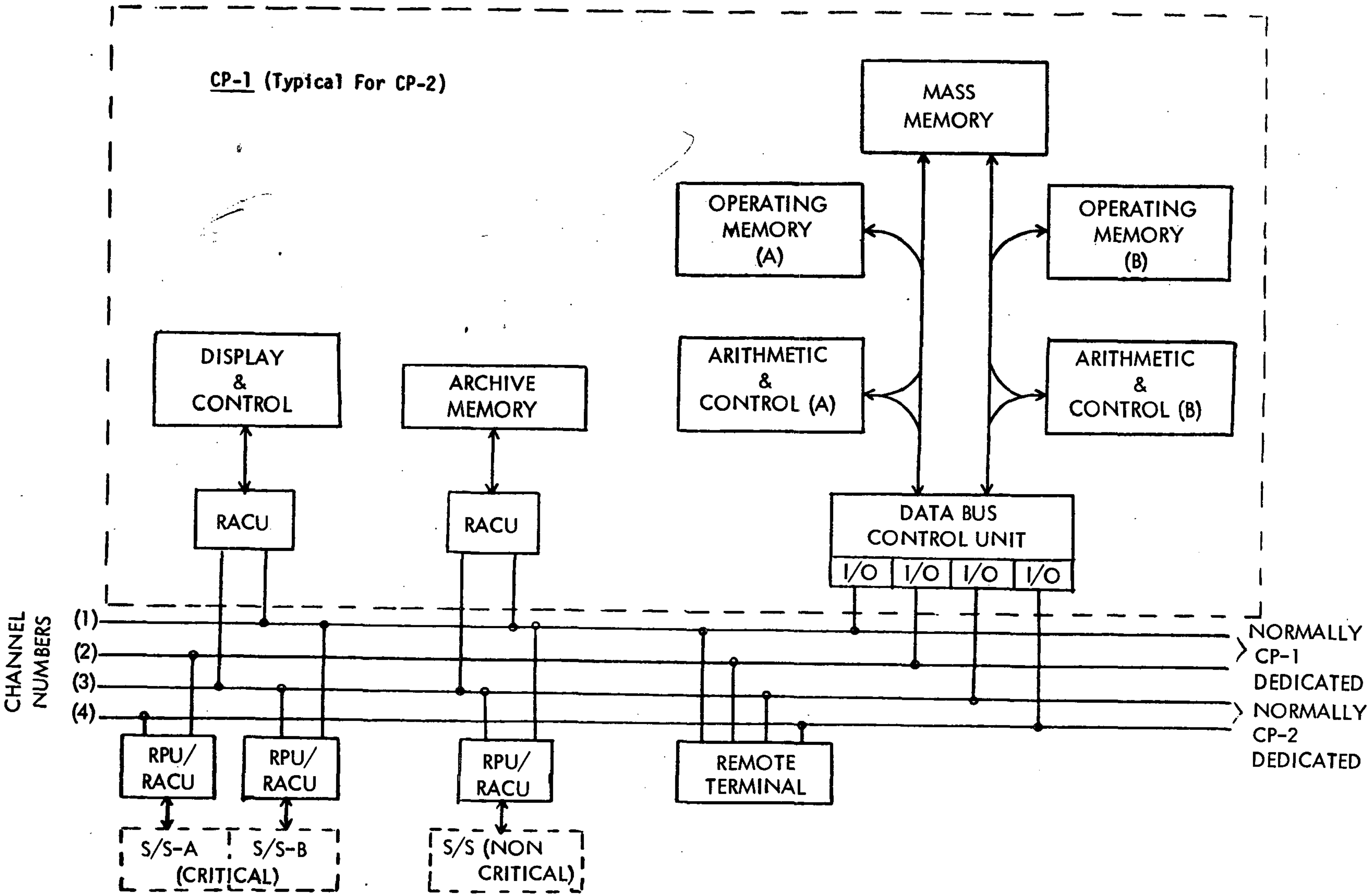


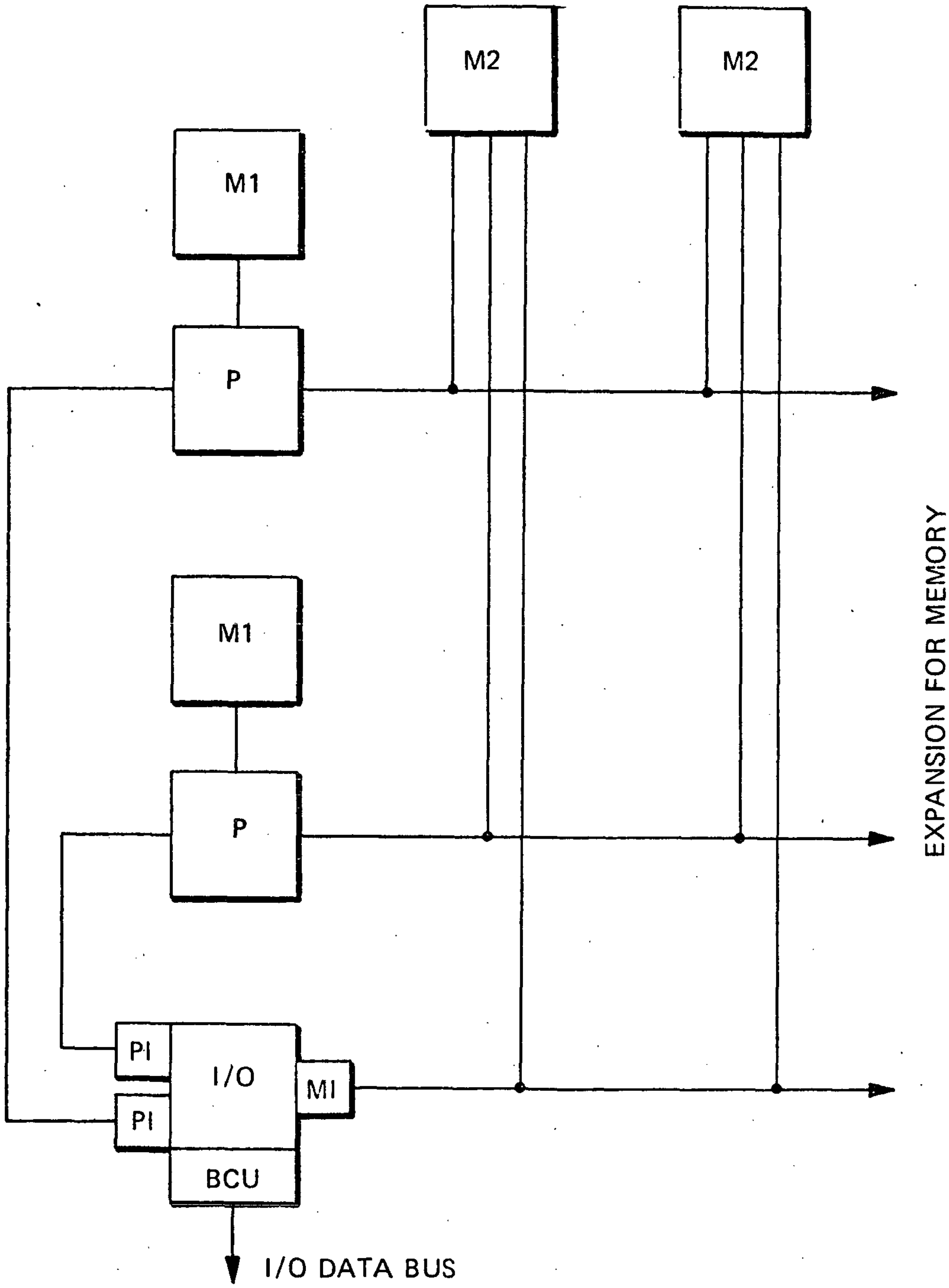
Figure 4-6. Basic Recommended Redundancy Configuration

SD 72-SA-0114-1

Space Division
North American Rockwell

Table 4-2. Redundancy Recommendations

Central Processor	• Two CP complexes • Each complex can tolerate one failure and detect another failure • Each complex can provide backup of critical functions
Data Bus	• Two plus two organizations • Error protection code for error detection • Retransmission for error correction
DBCU	• Controls all four buses
RACU	• Dual bus interface • Simplex subsystem interface



BCU - BUS CONTROL UNIT FOR DATA BUS
MI - I/O MEMORY INTERFACE
PI - PROCESSOR I/O INTERFACE

Figure 4-7. Simplex Multiprocessor Schematic

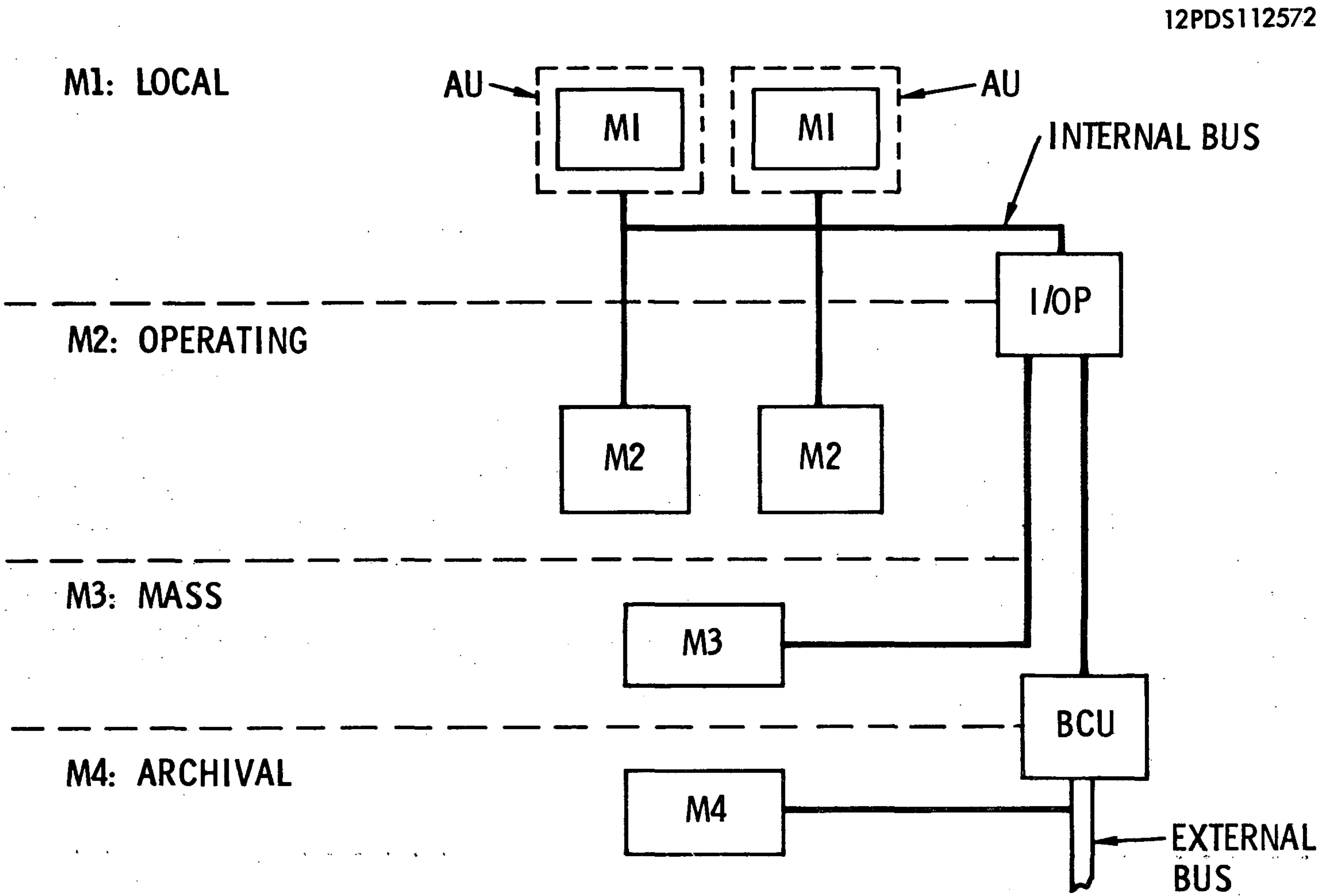


Figure 4-8. Memory Hierarchy

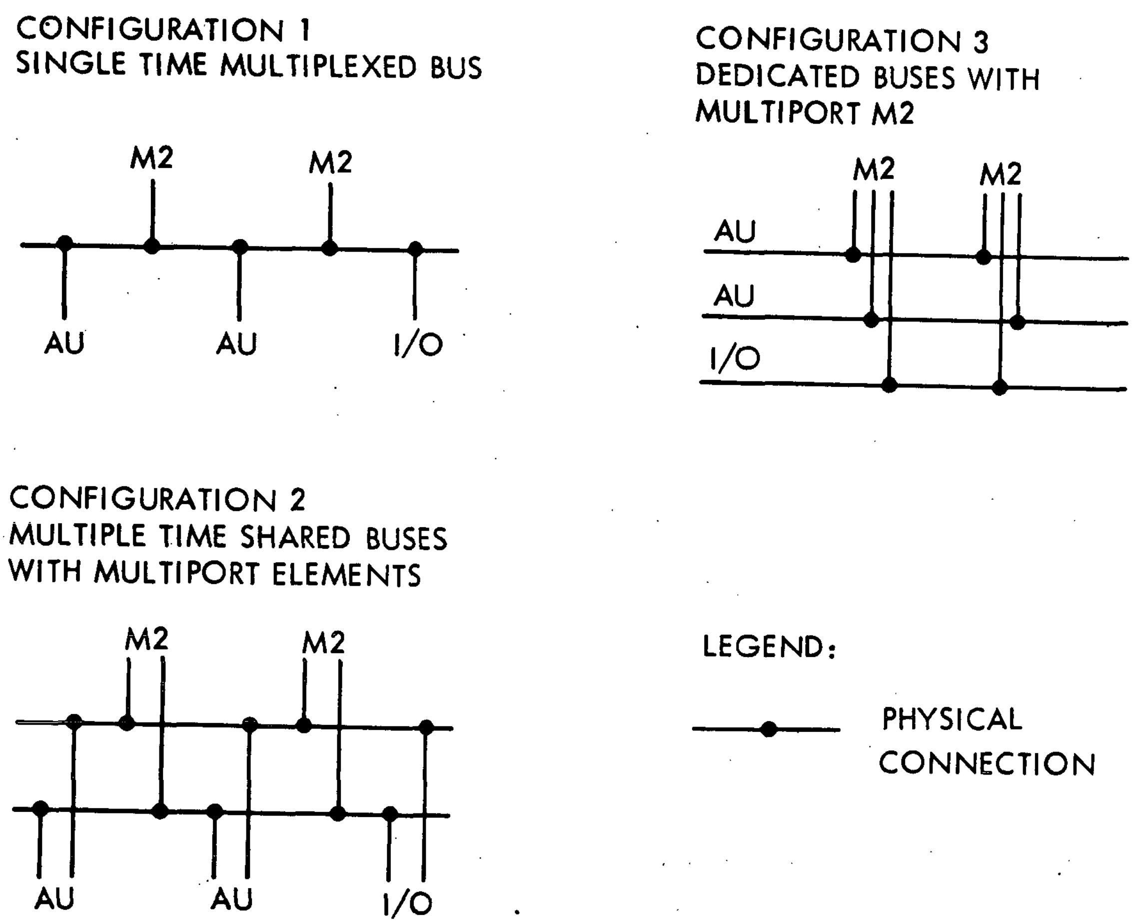


Figure 4-9. Internal Bus Configurations

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Table 4.3. Summary of Memory Hierarchy

M1 - Local Memory	
• Function	Stacks, descriptor, instruction buffer, data values
• Speed	200 - 500 ns
• Size	400 - 32 bit words
• Technology	CMOS LSI
M2 - Operating Memory	
• Function	Critical instructions, redundant critical data, overlay area
• Speed	Five-way interleaved 1 microsecond memory modules per M2 complex. Data rate 160 MPBS.
• Size	Two M2 complexes. Each complex 80K 32 bit words
• Technology	Plated wire
M3 - Mass Memory	
• Function	Non-critical instructions and data redundant copies of critical programs
• Speed	Five milliseconds latency 6 - 10 MPBS transfer rate
• Size	10^6 32 bit words
• Technology	Drum - low risk Plated wire - high risk

Table 4.4. Internal Bus Major Conclusions

- Internal bus is M2 switching network and packaged with M2
- Choice is dedicated bus structure
- Data path is 32 bits wide
- Maximum transfer rate per wire -5 MBPS
- Bus interfaces are synchronized

Table 4.5. Fault Tolerance Recommendations

- AU-M1

  Dual redundant AU's with comparator for error detection

  Generates M2 parity and checkword

  Indicates M2 errors by write echo check

  Reconfiguration via software restart at level of scheduled task

- M2

  Two independent M2 complexes containing critical programs, redundant critical data, and overlay area

  Block parity with imbedded address for error detection

  Software reconfiguration thru allocation of M2 space to critical tasks

- Internal Bus

  Not redundant

  Word parity error detection

- M3

  Recovery not required

  Failure detection similar to M2

- I/O

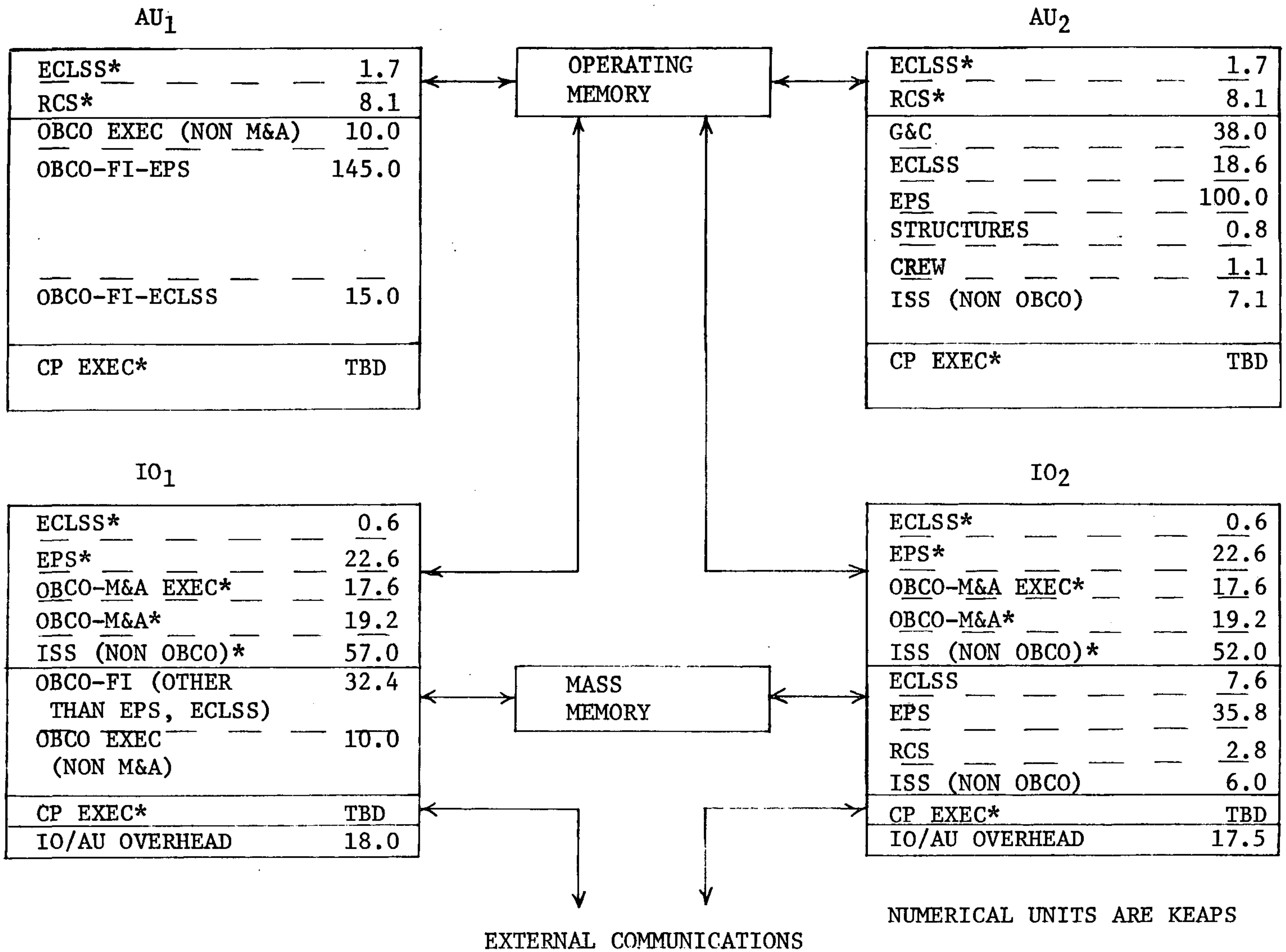
  Triple redundancy with voters

  M2 failure detection as per AU

- DBCU

  Generates F.S. communication

  Subsystems perform their own wind down in a F.S. situation



*critical functions
(a small portion of IO/AU overhead - that which services the critical 9.8 KEAPS of the AU - can be considered critical)

Figure 4-10. Detailed CP Subsystem Functional Allocations preprocessor in terms of their internal organization and required functional and performance characteristics.

The central processor is a multiprocessor which possesses the features shown in Table 4-6. As noted, a conventional organization is preferred. A memory hierarchy consisting of buffer memories in the processing elements and of modular operating and mass memories is provided. The requirements can be met with two arithmetic and input-output processing sets. Each set contains dual units with capability of comparing memory addressing, controls, and processed results.

The central processor utilizes two operating memories for the main storage functions. These memories are supplied by paging techniques with information from a mass memory. Additional offline storage is provided by an archive memory. The key features of these are shown in Table 4-6.

An arithmetic unit provides one million equivalent adds per second capability. An extensive repertoire, including floating point, is incorporated into the design. Modes of operation include the normal computational and the executive. Privileged instructions only executable in the latter are used. Linkage to the executive mode is by interrupts and special instructions.

All input-output functions are controlled by the AU's by means of I/O control words and commands from the AU's. Once initiated, I/O actions proceed independently of the AU's until completed.

Two transformer rectifier sets are used to convert the primary ac voltages to secondary dc voltages. A redundant power distribution capability is provided internal to the CP. Each set contains power circuitry in active redundancy capable of using either of the secondary sources.

It was noted earlier that the state of art of smaller aerospace computers is well advanced in preprocessing. The typical characteristics achievable from these is shown in Table 4-7.

The physical values shown in Table 4-6 and 4-7 are achievable with today's packaging capability. The processors are based upon the use of cased devices on multilayer boards. The mass memory utilizes 2 mil plated wire and power strobing and high density devices with beam leads, hybrid thin film and ceramic substrates.

4.3 DMS PROCESSOR EEM DEVELOPMENT PLAN

The development and test plan for the DMS EEM processor presents the schedule and identifies the major tasks. This plan is consistent with and requires inputs and support from the space station information management system (IMS) advanced development technology (ADT) program described in SD 71-240, Information Management Advanced Development Technology Extension Study Plan, North American Rockwell, Space Division, October 1, 1971.

Table 4.6. Technical Characteristics of the Central Processor

Type:

Multiprocessor, conventional organization, paralle, binary, 16/32 bit data and instruction words

Operating Memory, M2:

Two required, plated wire, NDRO, each consists of five memory modules of 13K x 33 bits maximum, one parity bit per memory word, one parity word exclusive OR-ed with block address for every five memory words, echo checking of write operations, one microsecond cycle time with interleaving of the five memory modules, maximum capacity of 18K x 33 bits per each module.

Auxiliary Memories:

Mass Memory - M3, Virtual memory using paging methods, error detection using one parity bit per word and one parity word with address exclusive ORed per every four data words; echo checking of write operations, 2 mil plated wire, NDRO, maximum capability of 1280K x 33 bits, modular design based upon 64K modules.

Archive Memory - Magnetic tape storage with $> 5 \times 10^6$ bits per cartridge.

Input-Output:

Two required, each contains dual IO units with comparator AU initiated with self-contained control, solid state buffer memory of nominal 2K x 33 words and 200 nanosecond cycle time, interface with data bus control unit, telemetry bus, and mass memory.

Arithmetic Set:

Two required, each contains dual arithmetic units with comparator, solid state buffer memory of nominal 2K x 33 words and 200 nanosecond cycle time 1 million equivalent adds per second per set, fixed and floating point with 100-200 instructions.

Physical Estimates:

	Mass Memory	Archive Memory	Multiprocessor Set
Size (cubic inches)	3900	1200	1000
Weight (pounds)	180	40	290
Power (watts)	15	45	400

Table 4-7. Technical Characteristics of the Preprocessor

Type: Uniprocessor, parallel-binary, 16 bits data, 16/32 bit instruction words
Memory: Capacity - 20K word, 17 bit plated wire storage One bit of parity per 16 bits Cycle time - 1 microsecond
Input/Output: One buffered 16 bit parallel input and output channel Eight external interrupts
Instruction Repertoire: Single and double word addressing Single word non-addressing Indexing Indirect addressing
Add Times (Fixed Point): Add - 4 microseconds Multiply - 20 microseconds Divide - 40 microseconds
Special Features: Internal and external interrupts General register file usable as index, base, or data register
Physical (20K x 17 Bits): Size - 400 cubic inches Weight - 15 pounds Power - 50 watts

The IMS ADT program is structured to include hardware and software studies leading to specifications and breadboard equipment for investigating key aspects of a spacecraft data handling system. These studies are necessary to support the procurement of the EEM processor. The breadboards and software defined in the ADT are required to enable concept evaluation and IMS integration testing.

The near-goal (1974) objective would be to assemble a prototype data management system to be used to develop automated subsystem's operations, orbiter payload interface requirements and payload data management operations. Figure 4-11 relates the present ADT BB equipments to this objective by a series of tasks. Figure 4-12 illustrates how these ADT extension (ADTX) tasks contribute to the definition and procurement schedule of an engineering evaluation model (EEM) of the DMS multiprocessor.

A development program consisting of three phases will provide the EEM processor. Further, dependent upon the level of available funding, various types of processor/breadboards may be procured.

Three possible breadboard processors are:

a. Simplex Model - 1 AU set; 1 IO set; 1 OM set and usable with the existing DACS breadboard

b. Multiprocessor Model - 2 AU sets; 2 IO sets; 2 OM sets and usable with the expanded DACS breadboard

c. Dual MP Model - Duplicate processors each consisting of 2 AU sets; 2 IO sets; 2 OM sets

The three phases and estimated durations are as follows:

Phase I: Requirements Analysis - 10 months

Phase II: Procurement

Simplex Model - 12 months
Multiprocessor Model - 15 months
Dual MP Model - 18 months

Phase III: Testing

Simplex Model - 8 months (acceptance)
Multiprocessor Model - 10 months
Dual MP Model - 12 months

Figure 4-12 showed the major milestones of the ADT extension study which will provide detailed definition of the central processor requirements and of the EEM processor requirements. This figure shows a requirement of 21 months to define the requirements and perform the EEM processor design analysis. This period would be followed by procurement and testing of the EEM processor - requiring between 20 and 30 months depending on the option chosen.

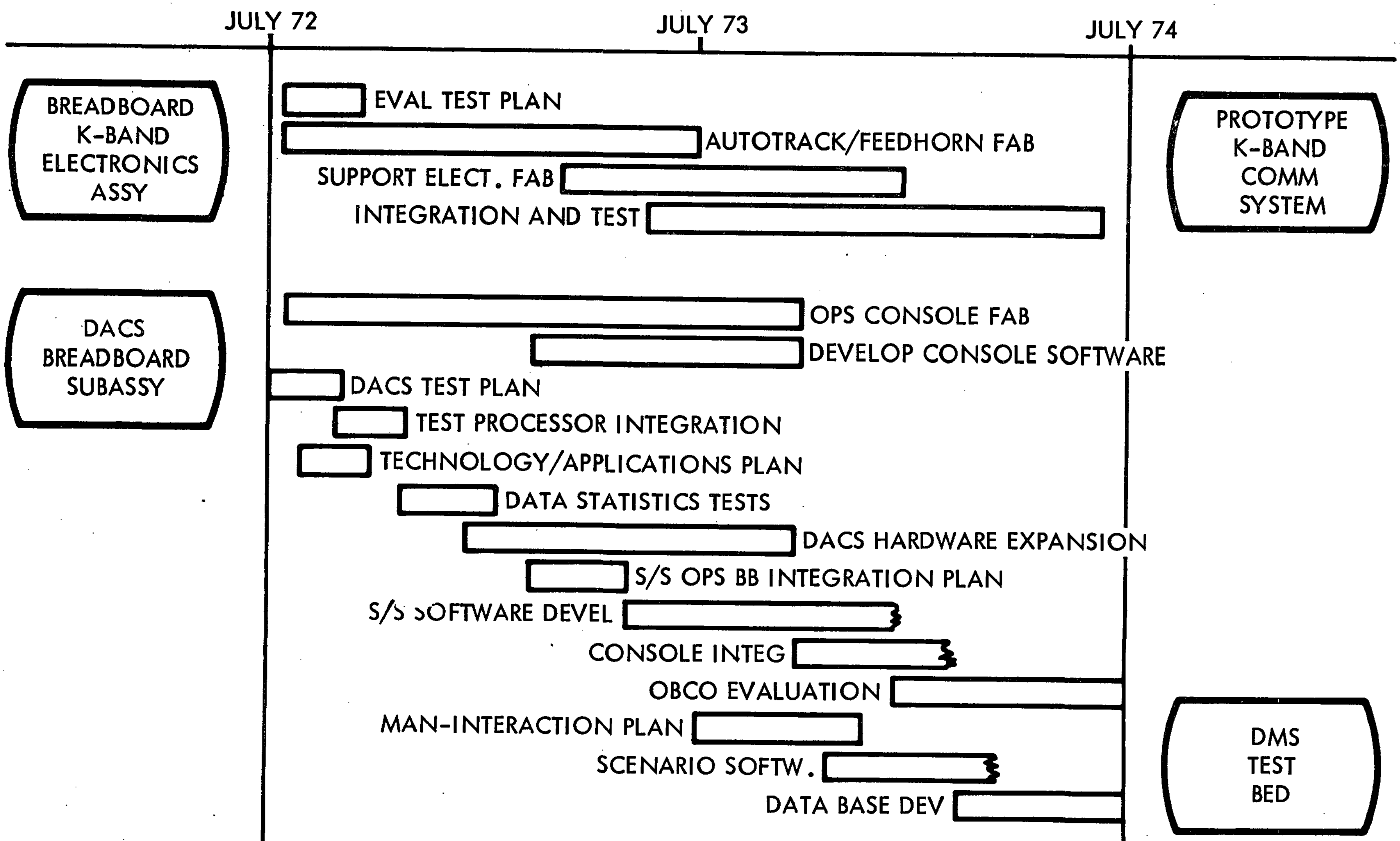


Figure 4-11. ADT Breadboards Related to ADT Plan

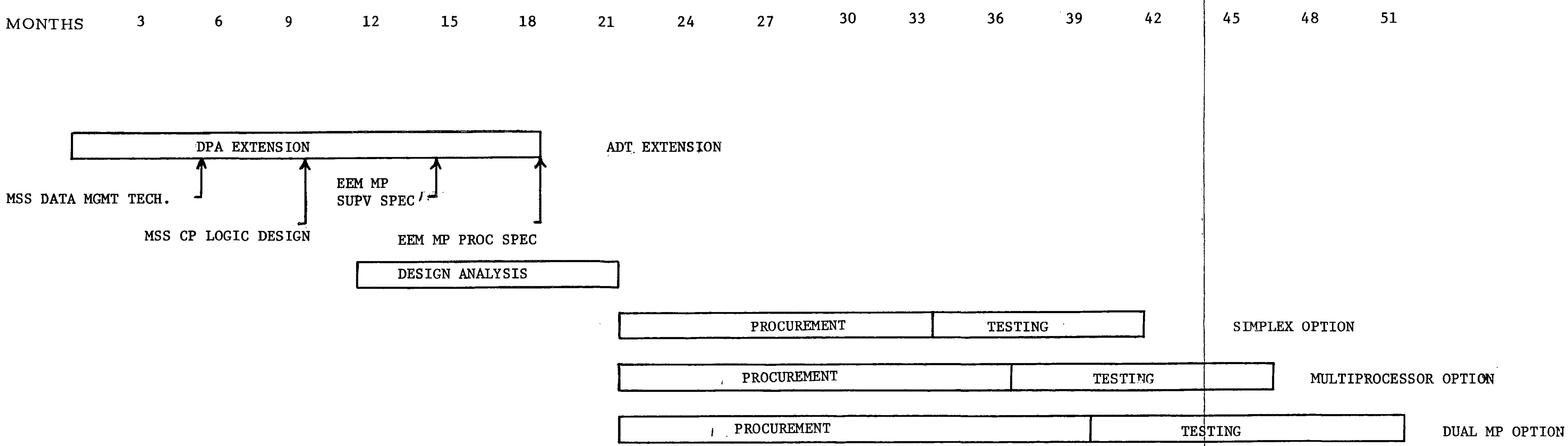


Figure 4-12. Relationship of EEM Processor Development to ADT Extension

In any event, it will be necessary to procure and evaluate a dual multiprocessor model prior to the procurement of the MSS central processors. There are a number of ways to accomplish this goal ranging all the way from sequential procurement of sufficiently many simplex models to all-out procurement of a dual multiprocessor in one effort.

To illustrate some of the effects of these possible procurement plans, we begin by assuming:

1. MSS IOC at the end of 1984
2. 18 months for MSS subsystems integration
3. 6 months for flight article dual multiprocessor acceptance and qualification testing
4. 18 months for procurement of the MSS flight article dual multiprocessor
5. At least 12 months of evaluation testing with the EEM dual multiprocessor prior to procurement of the flight article dual multiprocessor

Based on these, we can schedule IOC of the EEM dual multiprocessor for mid-1980. These assumptions and three procurement options are illustrated in Figure 4-13.

The first option represents sequential procurement of two simplex models (together forming a multiprocessor) followed by procurement of a second multiprocessor. This option will require the initiation of the requirements definition at the beginning of 1974. This option may also be characterized as having the least risk and by having the lowest peak of funding spread over 7.5 years.

The second option represents sequential procurement of two multiprocessors. Initiation of requirements definition could be delayed a year to the beginning of 1975, but this option would require higher funding peaks and higher risk.

The third option represents procurement of a dual multiprocessor saving another 15 months but requiring the highest funding peak and the highest risk of all the options.

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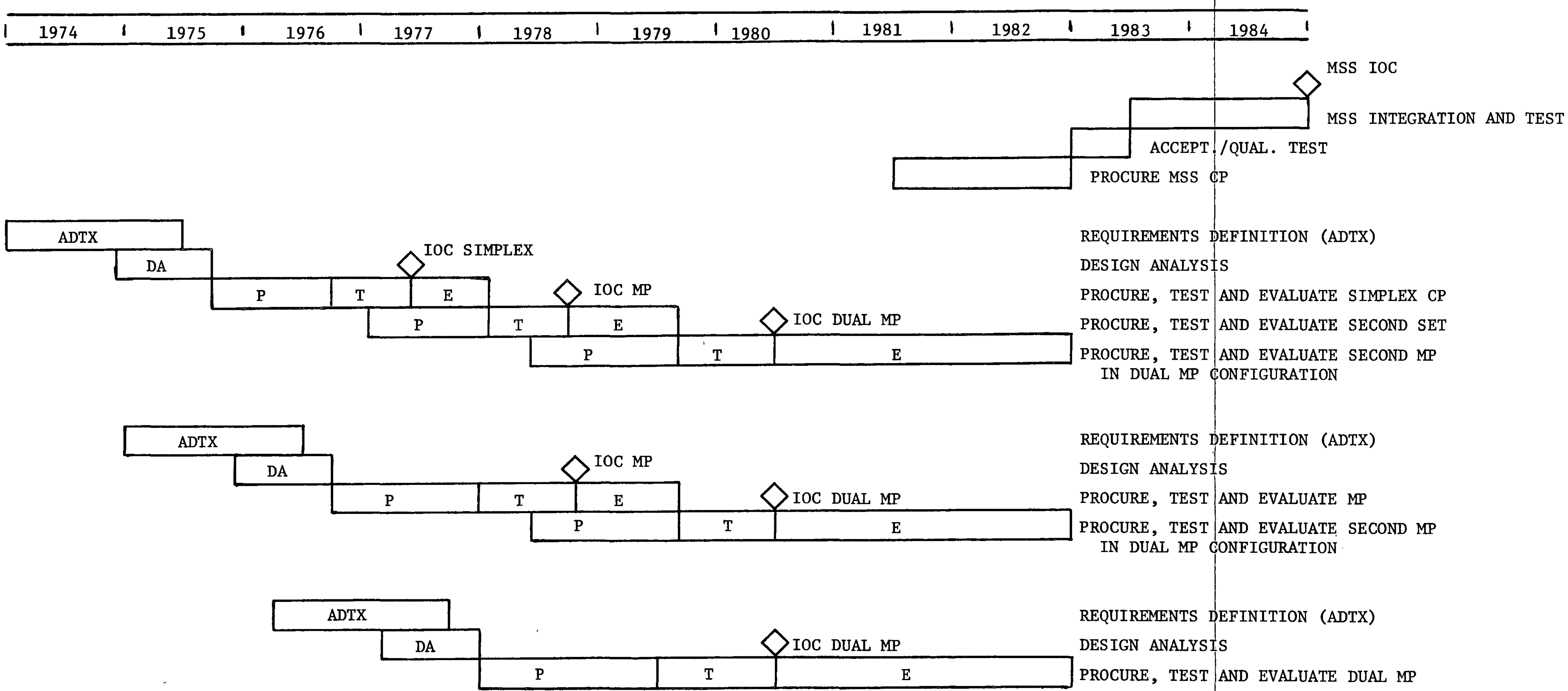

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Figure 4-13. Procurement Options for a Dual Multiprocessor

5.0 COMPUTER PROGRAM (SOFTWARE) ASSEMBLY DEFINITION

5.1 SUMMARY

The modular space station (MSS) incorporates a very large digital computer complex to assist the crew in accomplishing their assigned tasks. It was recognized from the inception of the Phase B study that the definition of the design requirements for the computer complex would be sensitive to the software (computer programs) that was to run it. To emphasize the importance of the software in the MSS program, it was defined to be an assembly, on the same level, but separate from the hardware assembly. It was also recognized that the assignment of functions to the several subassemblies (both hardware and software) would involve many tradeoffs to obtain a realistic configuration.

Therefore, the MSS software assembly was included within the advanced development task (ADT) as a series of interrelated studies in concert with similar data processing assembly (Volume IV) studies; these tasks were developed and conducted by representatives from System Development Corporation, Autonetics, and Space Division as a cooperative effort. The intent of these tasks was to develop uniform computer program standards and conventions for the space station program, develop a computer program specification hierarchy, define a computer program development plan, make recommendations for the effective utilization of all operating on-board space station program related data processing facilities, and develop a preliminary computer specification for the MSS CP executive program.

These five subtasks are by no means exhaustive of the necessary preliminary studies of the MSS software assembly that need to be completed before any actual computer programs are written; they are, perhaps, the very tip of the iceberg of software cost avoidance. Historically, the costs of developing software for extensive computer systems have been buried under other titles and have seldom indicated that the man-hours and other cost dollars attributable to hardware (the computer system) are usually exceeded by the costs for the programs that are to be run in the computer. Recognition of this situation caused NR-MSC to identify all the MSS software as a separate assembly of the on-board information management system - to further identify and device means to avoid the excessive cost buildup.

Identification of the components of software cost buildup strongly influenced the preliminary design of the MSS data processing assembly. Typically, the factors of limited computer speed and memory capacity were identified as a strong driver on software costs; the MSS DPA is, therefore, oversized in terms of identifiable station operations needs (Refer to Volume IV of this report). Another factor listed by many was the lack of experienced computer program designers; the MSS preliminary design was based upon the assumption that if the programs (routines) could be written in a higher-order language (HOL), in sufficiently small modules, this factor could be reduced considerably

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in influence. However, in order to accomplish this desirable objective, the total must be divided into very small work packages; governed by standardized terminology and procedures; planned to be effected during a progressive, unhurried time scale; and controlled with the same attention to quality and specificity as any of the hardware developments. It was to these points that the IMS ADT software assembly studies were addressed.

5.2 MSS SOFTWARE STANDARDS AND CONVENTIONS

The objective of this study was to define and rationalize an initial set of computer program standards and conventions for the information subsystem (ISS) of the modular space station (MSS) program.

For all large systems, software or hardware, the establishment and implementation of standards and good operating practices and conventions is an ongoing process which continues to be refined throughout the life of the system. In this respect, the material presented is not intended to be final or all inclusive. However, it is intended to identify those areas of profitable standardization and good practice which can serve as a base for uniform design, development, and implementation.

Basic Definitions

As used in this document, a standard is a definite rule or procedure which has been established by authority. A convention is a customary or agreed-upon rule or procedure. These standards and conventions will be of prime importance to computer programmers, system designers, and software system managers.

Software is defined as the computer programs and the programming aids and documentation required to produce and describe computer programs. This definition includes not only the operational programs but also support programs such as compilers, loaders, simulators, data reduction, analysis and documentation.

Software techniques are the methods used to produce computer programs. They include state-of-the-art knowledge and all tools which are and have been applied in computer programming activities.

Common and/or frequently used areas of software technique applications are termed information processing functions. These functions identify a group of actions and/or activities required to meet system software requirements. From a review of MSS operational and support elements, with possible software involvement, 14 basic information processing functions were identified. These are:

- Program production
- Program organization
- Documentation
- Program testing
- File management
- Symbol manipulation
- Calculations
- Decision making
- Bookkeeping
- Timing
- Message formatting
- Simulation
- Personnel
- Management

The standards and conventions presented are identified and discussed within a framework of 12 topic areas. Six of these are information processing functions, where a variety of software techniques are applicable and six are specific software techniques. This structure was selected as the most optimum to cover the subject of software standards and conventions for the MSS program.

- Languages
- Compilers
- Program production
- System organization
- Formats
- Technology and abbreviations
- Symbols
- Units of measurement and coversion
- Documentation
- Testing and validation
- Maintenance
- Management

Table 5-1 summarizes the suggested baseline standard and conventions. The intent of this section is to define an initial set of computer program standards and conventions that can serve as a beginning to the standards and conventions guidelines that will be required for the MSS program.

5.3 COMPUTER PROGRAM SPECIFICATION TREE

The objective of this study was to:

1. Develop a computer program specification hierarchy and describe in detail each component in the hierarchy
2. Prepare a preliminary top-level computer program system specification containing system performance and design requirements, system segment allocations and interfaces, identification of major contract end items, and requirements for system testing.

Figure 5-1 illustrates the logical sequence of contract end items to be produced and delivered and the responsible agency.

Figure 5-2 illustrates the detailed specification tree containing each specification as part of the DPA. For clarity, the computer program/modules listings have been indicated by symbol (A). Each symbol represents a number of listings corresponding to the number of subprograms or modules contained in the Part II specification.

Figure 5-3 illustrates the functional data processing requirements for MSS subsystem operations, extracted from the complete Preliminary Top-Level Computer Program System Specification of Volume V.

This specification establishes the top-level requirements for the performance, design, test and qualification of a computer program identified as the Modular Space Station Master Computer Program and defines in logical, and operational language the detail necessary to design, produce, and test this program. Data processing functions from all other subsystems are included in this specification.

Table 5-1. Baseline Standards and Conventions

Item	Standard
Computer Programming Language	
	A higher-order programming language (SPL or HAL) should be used as the standard higher-order programming language for all MSS on-board, ground, and supporting computer programs.
Compilers	
	Existing HOL compilers modified to meet any special MSS system requirements, if any, should be established as standard host developmental compilers to be used by all software contractors. New HOL compiler development should be limited to the production and organization of code for the on-board and ground based target computers.
Program Production	
Libraries	A computer program integrating contractor, or an equivalent organization, shall establish and maintain a computer program library of all accepted computer programs, subroutines, and algorithms. Standardized configuration control identification procedures shall be employed for each item contained in the MSS software system library. All MSS software system contractors shall have access to MSS software system library items for checkout and testing purposes. All library items shall be written in the selected HOL and shall be documented by: (1) a general non-technical description, (2) a capability description, (3) a test acceptance and condition report, and (4) a user's manual.

Table 5-1. Baseline Standards and Conventions (Cont)

Item	Standard
Program Production (Cont)	
Production monitoring and quality control	All MSS software contractors shall follow production status reporting procedures and schedules as defined by software configuration management requirements. All MSS software contractor-conducted assembly, subsystem, and system testing shall conform to establish MSS system test plans and the results documented in a standardized format as defined by software configuration management requirements.
Program segmentation	No specific MSS software production segmentation standards and conventions are recommended at this time.
Interpretive Simulations	All MSS software contractor conducted interpretive simulations shall conform to standardized MSS hardware and environmental characteristic equations. Contractor conducted interpretive simulations shall be operationally compatible with subsystem and system computer program integration simulations to be conducted by the same or a different software contractor.
FIX programs	Automated FIX computer programs for hardware and software errors are not recommended for MSS-ISS computer program production.
Machine independent programming	No standards and convention related to machine independent programming are required if a HOL is used.

Table 5-1. Baseline Standards and Conventions (Cont)

Item	Standard
Program Production (Cont)	
COMPOOL (data dictionaries)	The primary criterion for grouping data elements should be frequency of use. Whenever possible, the data should be structured by the following: (1) read-only data, (2) read/write data, (3) multiple-record data, and (4) single record data. Large blocks of related data should be structured as a single file with multiple records. Each record should have the same structure to allow a single COMPOOL definition to access the file one record at a time.
Allocation Programs	SPL table allocation, programmer allocation, and compiler allocation rules and recommended procedures shall constitute allocation standards and conventions and should be followed by all solftware contractors.
Flow Chart Generation	The IBM automatic flow chart generating program FLOWCHART, or an equivalent, should be established as a standard for the production of all MSS computer program flow charts.
Initialization	Computer program production testing and checkout shall be performed with standardized initial hardware and environmental conditions. Standardized system equations and initial parameter values for all MSS operational phases shall be defined for software system and subsystem testing.

Table 5-1. Baseline Standards and Conventions (Cont)

Item	Standard
Program Organization	
Modularization	See 2.5.1, Volume V
Executive and Monitor Programs	See 2.5.2, Volume V
Libraries	See 2.5.3, Volume V
Segmentation and Allocation	All HOL written computer programs shall be organized as follows to simplify maintenance documentation and checkout: • START • Description comments • Declarative statements • Imperative statements • Global closes • Procedures/functions • TERM
MACRO Programming	MACRO programming as a separate technique for computer program organization is not recommended.
Formats	
Documentation	See paragraph 2.6, Volume V
Messages	The selected HOL standards and conventions for INPUT and OUTPUT operations and the manipulation of TEXTUAL Communications shall be followed for all message formats. The general recommendations of paragraph 2.6.2, Volume V should be established as message format conventions.

Table 5-1. Baseline Standards and Conventions (Cont)

Item	Standard
Formats (Cont)	
Data Cards	Free-field formatting should be established as the standard for all symbolic data cards. Recommended conventions for data card formats consistent with the HOL usage should be followed.
Magnetic Tape	See paragraph 2.6, Volume V
Displays	See paragraph 2.6, Volume V
Terminology and Abbreviations	
	See paragraph 2.7, Volume V
Symbols	
	See paragraph 2.8, Volume V
Units of Measurement	
	See paragraph 2.9, Volume V

Table 5-1. Baseline Standards and Conventions (Cont)

Item	Standard
Documentation	
	See paragraph 2.10, Volume V Software documentation standards and conventions as defined and specified in MSS software configuration management procedures shall be followed by all software contractors. MSS software configuration management publications shall define the types of software documentation required for all computer programs. These publications shall also define a standard outline and a content description for each required document.
Testing and Validation	
	Standards and conventions for computer program testing and validation, at the assembly, subsystem and system levels shall be defined as test plan requirements by configuration management procedures. All computer program testing and validation shall be documented with: (1) Test Plan, (2) Test Procedures and (3) Test Result documentation.

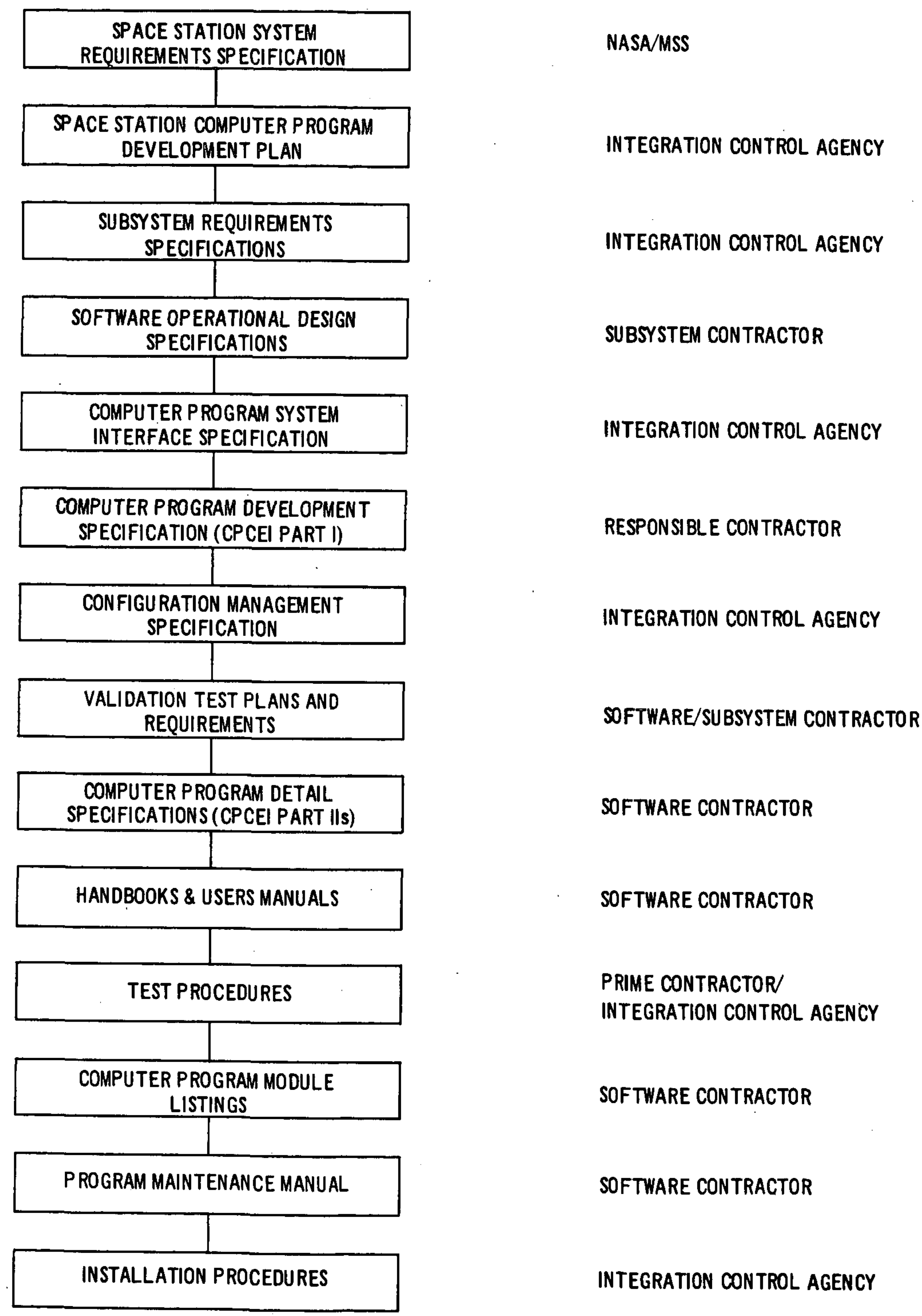

Figure 5-1. Hierarchy of Plans and Specifications

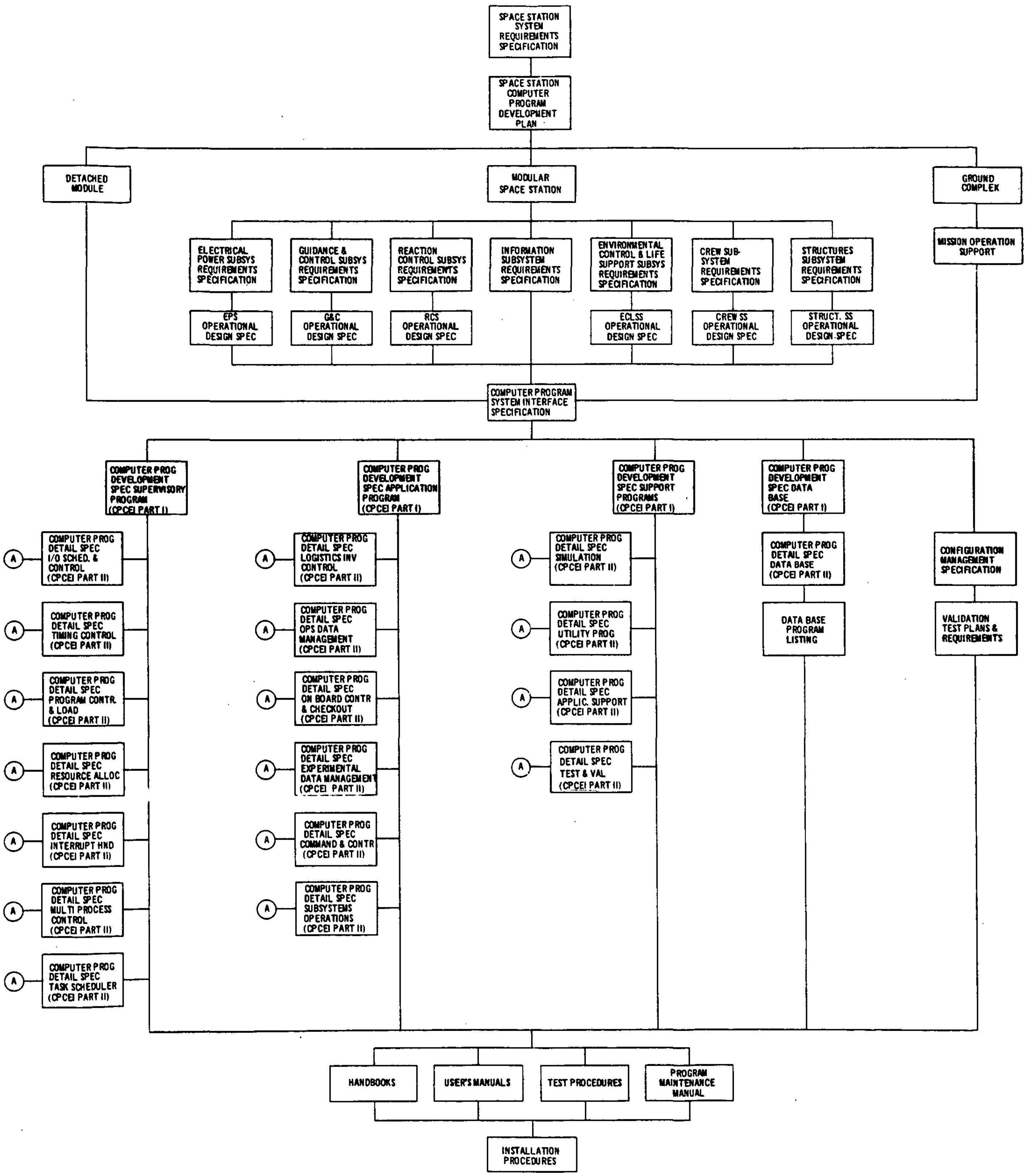

Figure 5-2. MSS Software Specification Tree

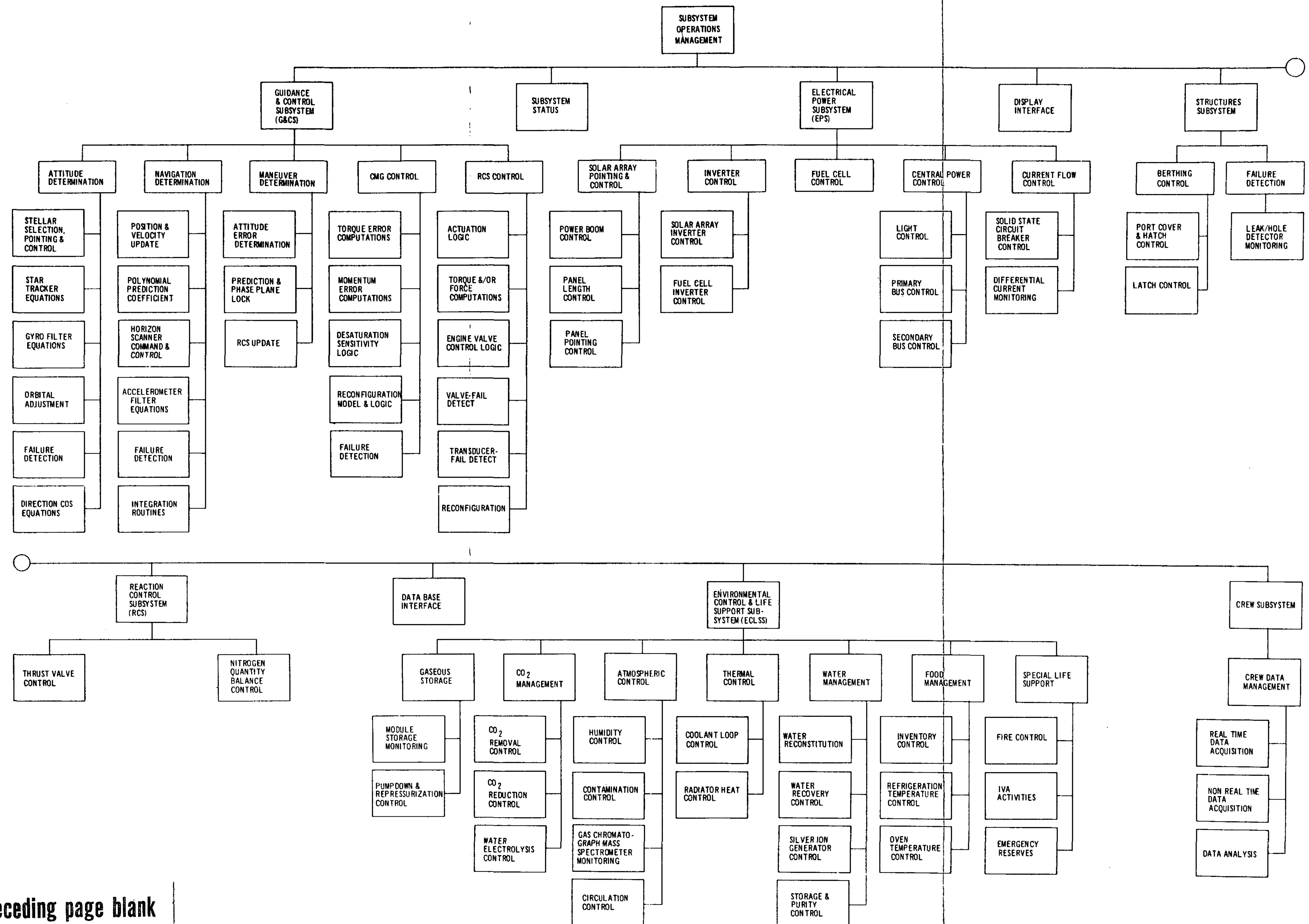

Figure 5-3. MSS Subsystems Operations

5.4 COMPUTER PROGRAM DEVELOPMENT PLAN

The computer programs required to perform all ISS functions and the software tools used to develop, test, and validate these computer programs constitute the MSS software assembly. Figure 5-4 identifies the five major subassemblies and illustrates an important aspect; namely, that the many modular routines are categorized by similarity.

Figure 5-5 lists the numerous software techniques that apply to the five subassemblies to indicate the type of activity controlled as implemented by the modular routines.

Figure 5-6 indicates how one subassembly (supervisory) would be assembled from small modules into routines, then into a master tape, and eventually into the total software system (ISS software assembly). Note that to avoid confusion, the terms assemblies, subsystems, etc., are not per the MSS hardware "tree," but are conventional software terminology (A.N.S.I. x3.12-1970). In this sense, a computer program module is a single program, a small group of computer programs that performs a single or basic operation.

To accomplish the development of the large order of computer programming for the MSS, it should be recognized that a strong, high-level authority structure is needed, particularly since there is a high degree of overlap and commonality with other space programs. Both Skylab and the earth orbital shuttle, as well as MSS and RAM, are integral parts of the whole space station program. Figure 5-7 suggests that one way to provide orderly management and to avoid needless duplication of effort would be to enforce, at the highest level, the same emphasis on interprogram coordination and commonality for software and hardware.

Figure 5-8 illustrates the recommended development flow for the MSS master tape and MSS subsystems operations tape; it is felt these software subassemblies must be flexible to follow the changes and modifications in requirements as the program develops. It is felt that three versions (V_1, V_2, V_3) will be adequate. The remaining software could utilize a single-version approach. Figure 5-9 shows the time-phased software development schedule and indicates that to achieve an MSS IOC in 1983 that the initial version of DPA software requirements should be available in 1977-78. Figure 5-10 continues the software development schedule milestones in greater detail. Note that the Version 3 software is used (per MSS program philosophy) to perform the vehicle subsystems installation, checkout, and acceptance and thus must be available about 1981-82.

5.5 COMPUTER-ASSISTED RESOURCE ALLOCATION AND UTILIZATION

Recommended data processing techniques and procedures for the planning, scheduling, and allocation aspects of an operational modular space station (MSS) total system are presented as conceptual and capability requirements in Volume V. Specific examples of recommended concepts and capabilities, in respect to MSS requirements, are discussed and illustrated with the recommendations. Following the recommendations, an implementation summary is presented.

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SOFTWARE ASSEMBLY

- **SUPERVISORY**
  - DPA OPERATIONS
    - Executive
  - CONT. OPERATIONS
    - Timing Control
    - Progr.Control & Load
    - Task Scheduling
    - Multiprocessing Control
  - INTERACTIVE OPERATIONS
    - I/O Scheduling & Control
    - Interrupt Handling
- **APPLICATION**
  - MONITOR & CONTROL
    - Subsystem Status
    - On Board Checkout & Control
  - VEHICLE INTEGRATION
    - Subsystems Management
    - Subsystems Interface
  - MISSION CONTROL
    - Mission Planning
    - Mission Scheduling
    - Mission Monitoring
    - Orbital Control
    - Message Generation Control
  - MISSION INTEGRATION
    - Logistics Inventory Control
    - Usage Prediction
    - Trend Detection
  - OPERATIONS CONTROL
    - Command Execution
    - Command Verification
    - Shuttle/Module Alignment
    - Communication Control
  - OPERATIONS INTEGRATION
    - Device Control
    - Data Analysis
    - Data Compression
    - Data Display
    - Experiment Data Management
    - Experiment Data Status
- **SUPPORT**
  - SERVICE
    - Simulation Program
    - Library Routines
    - Data Recording
    - Data Reduction
    - Real Time Evaluation
  - OUTPUT
    - Display Formatting
    - Telemetry Formatting
  - UTILITY
    - Compiler
    - Assembler
    - Start/Generator
    - Tape File Maintenance
  - APPLIC. SUPPORT
    - Data Storage
    - Information Retrieval
    - Catalog Maintenance
- **DATA BASE**
  - SUBSYSTEMS
    - Configuration Records
  - OPERATIONS
    - Ephemerides
    - Star Charts
    - Coordinate Origins
  - EXPERIMENTS
    - Reference Data Sets
  - PERSONNEL
    - Personnel Records
- **TEST/VERIFICATION**
  - STANDARD
    - Test Control
    - Flight Hardware Test Support
  - DIAGNOSTIC
    - Diagnostic & Debugging Pgms
    - Memory Dump
    - Symbolic Corrector

Figure 5-4. MSS Software Assembly Categonzation

Supervisory Programs	Application Programs	Support Programs	Data Base Programs	Test/Verification Programs
1. Initialization	1. Status Checkout	1. Program Generation	1. Allocation	1. Comparison
2. Decision Making	2. Status Reporting	2. Assembly	2. Address Transformation	2. Initialization
3. Time Control	3. Formatting	3. Compilation	3. Data Organization	3. Reformatting
4. Time Analysis	4. Symbol Manipulation	4. Formatting	4. Data Management	4. Time Analysis
5. Task Scheduling	5. Monitor and Control	5. Time Analysis	5. Sorting	5. Error Detection
6. Load Control	6. Bookkeeping	6. Code Improvement		6. Simulation
7. Task Allocation	7. File Manipulation	7. Simulation		
8. Configuration Control	8. Mathematical Calculations			
9. Execution Monitoring	9. Statistical Calculations			
	10. Time Sequencing			
	11. Initialization and Update			

Figure 5-5. Software Assembly Techniques

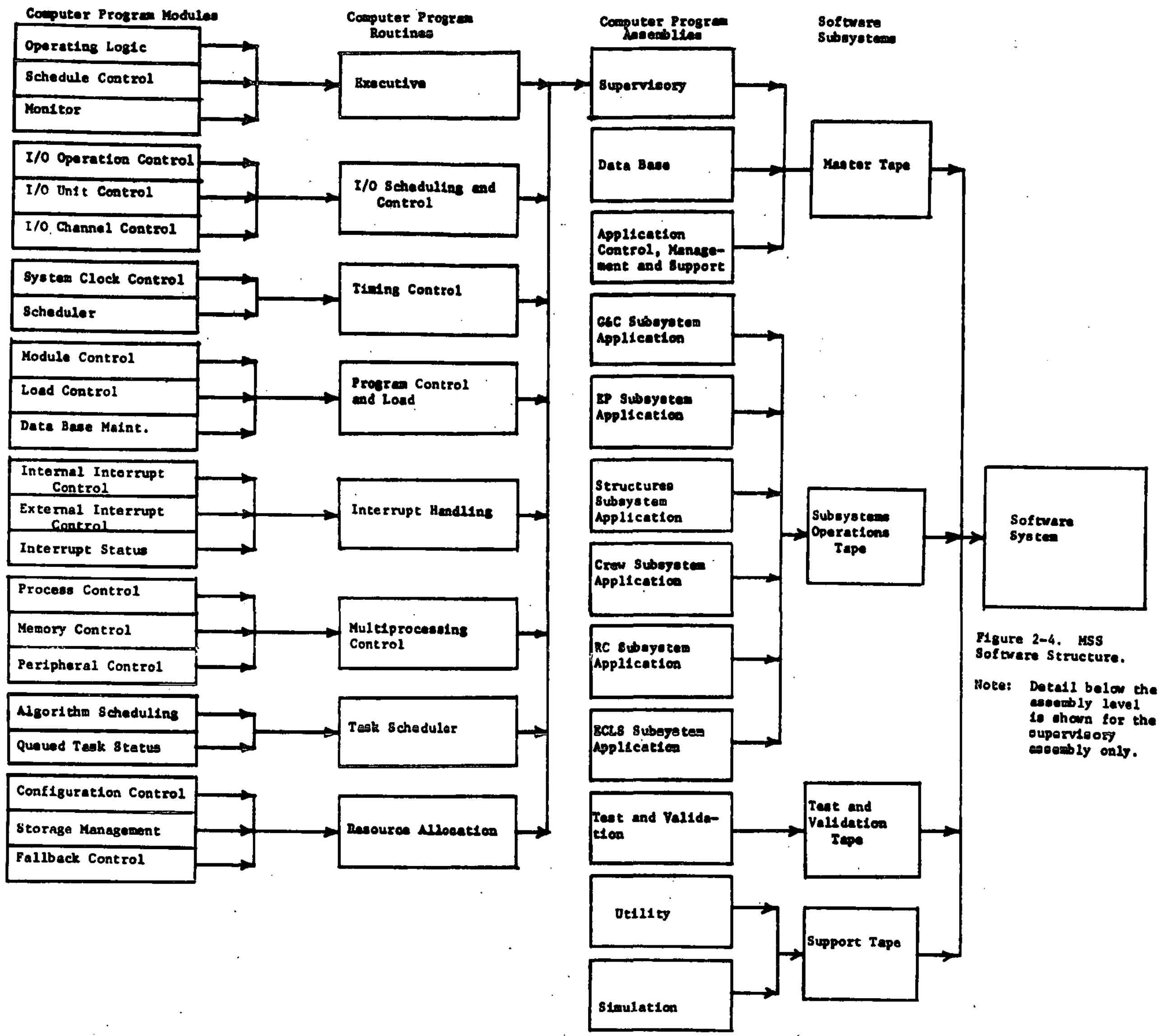

Figure 5-6. MSS Supervisory Program Structure

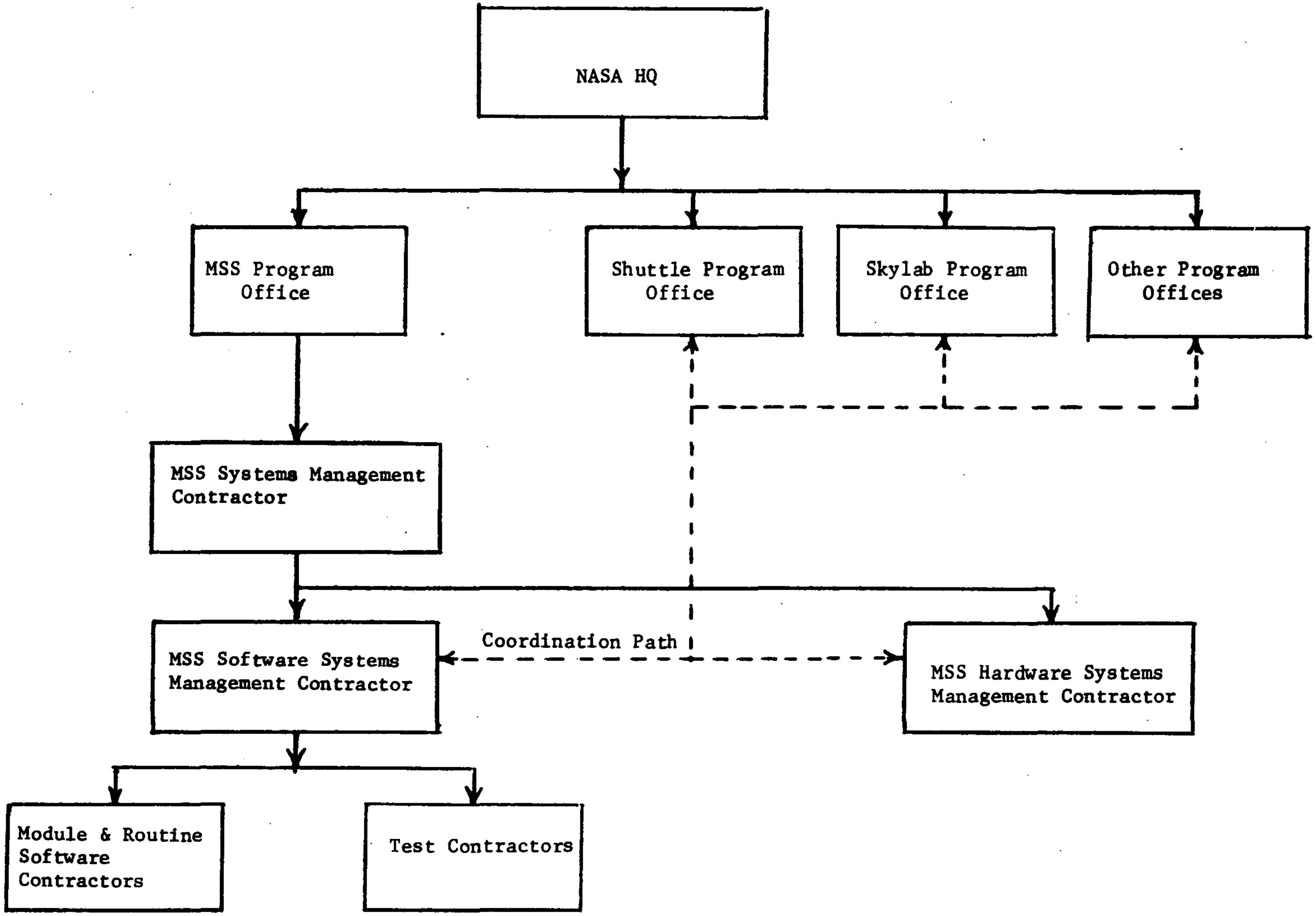

Figure 5-7. MSS Software System Authority and Coordination

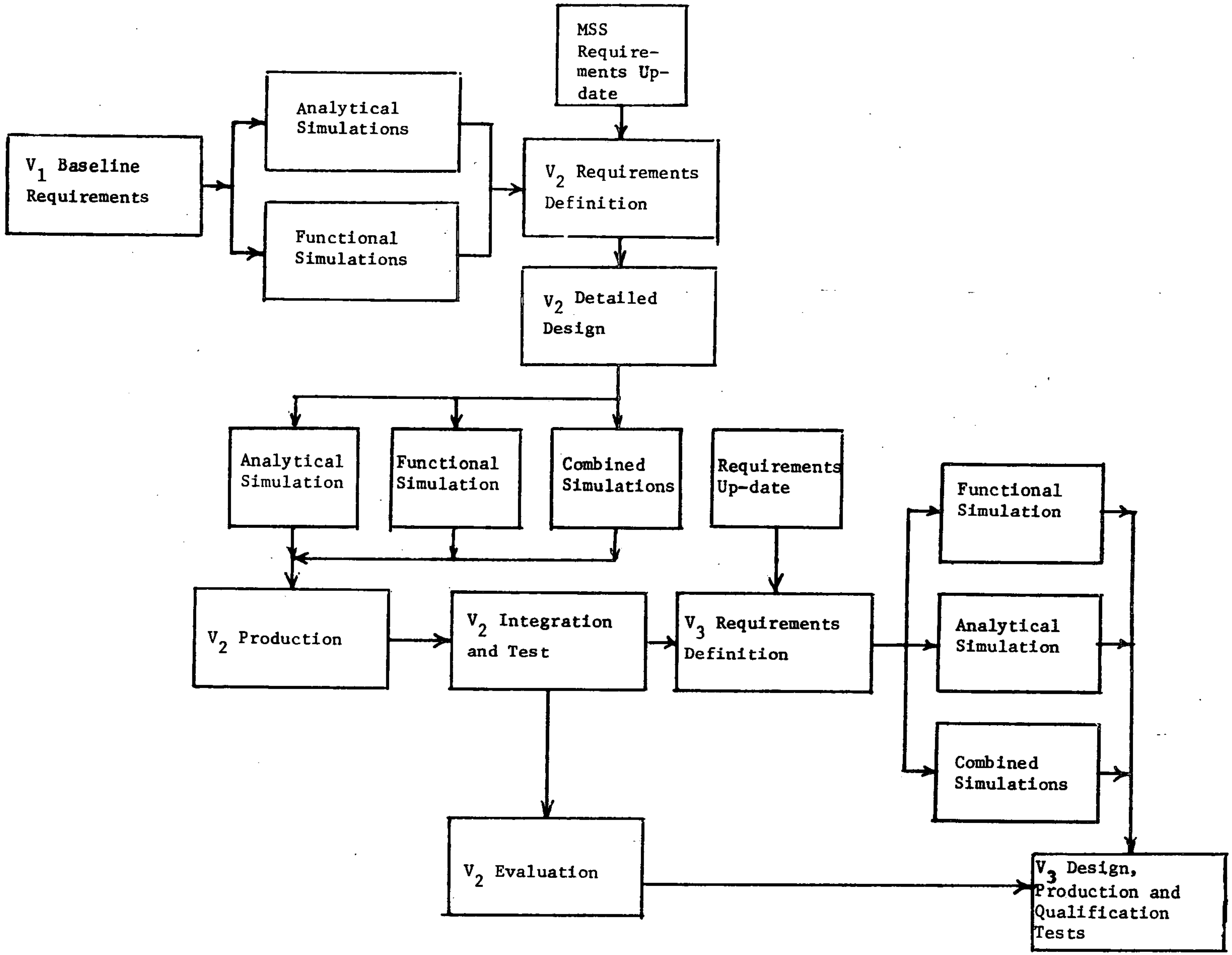

Figure 5-8. Multi-Model Development Flow

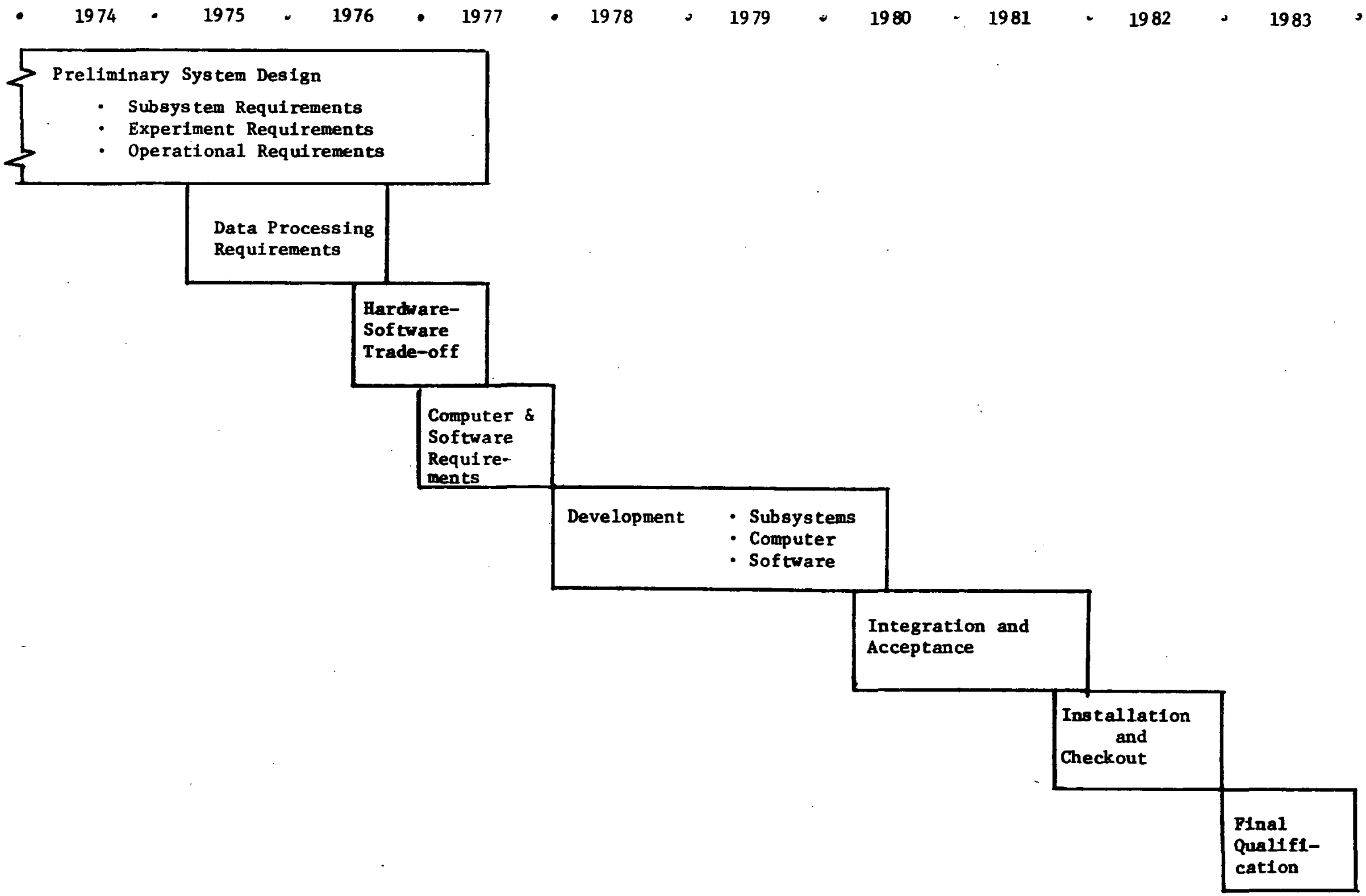

Figure 5-9. MSS Development Schedule

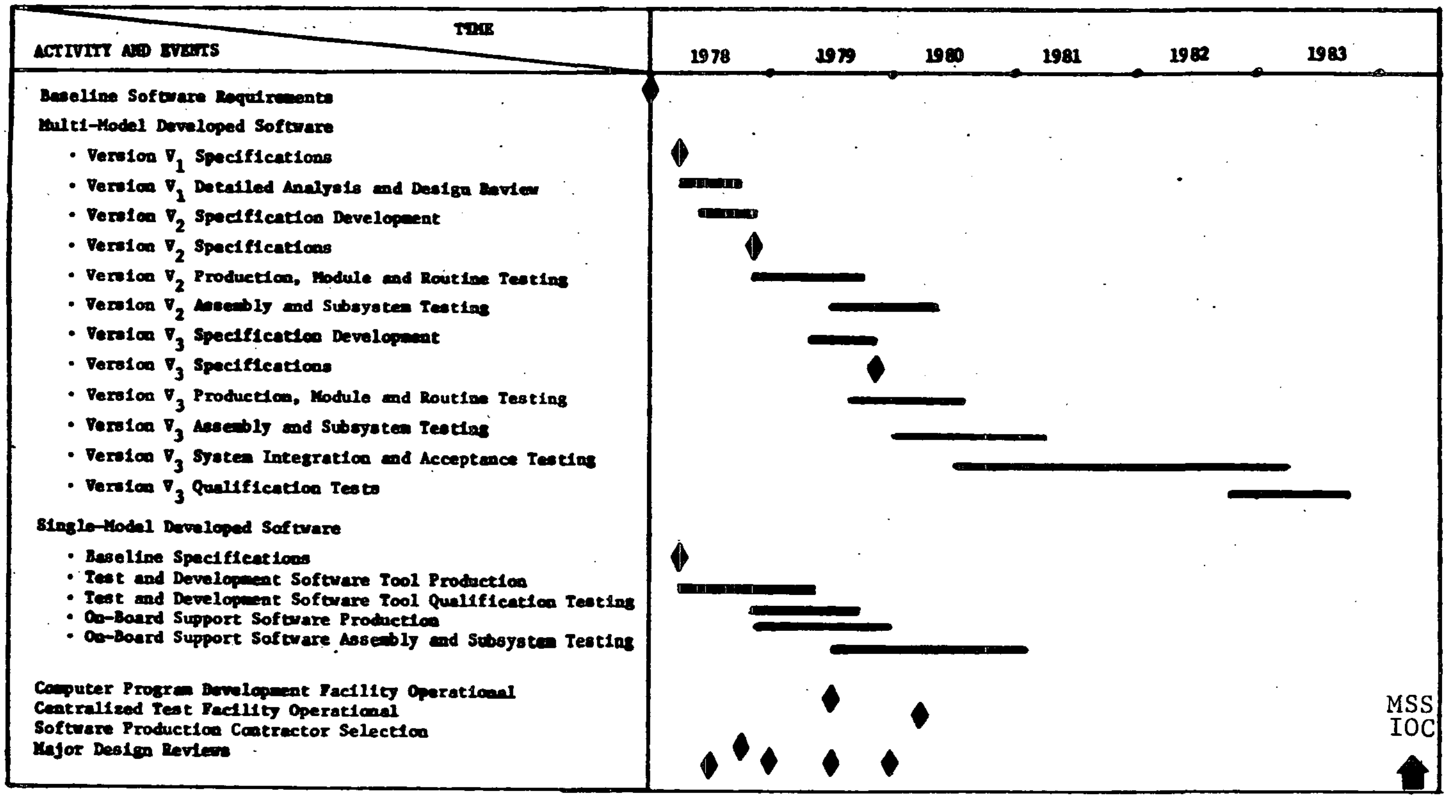

Figure 5-10. MSS Software Development Schedule

MSS system allocation, scheduling, and planning requirements include those necessary to perform mission and experiment operations both on-board the space station and all supporting ground-based facilities. These requirements are presented under the three subheadings of: (1) Users, (2) Processed Data, and (3) Resources.

Volume V also presents a condensed but comprehensive discussion of past and current computer-assisted allocation, scheduling, and planning technology. Past technology is discussed primarily in respect to problem areas and experience with implemented systems. Current technology is discussed in respect to the approaches being utilized and the basic operations performed.

The major resources that will require allocation and scheduling during space station missions are (1) data processing capabilities, (2) on-board consumables, (3) on-board and ground-based sensors, and (4) personnel skills. Discussions of utilization implications for these resources are presented in the following sections.

In discussing the data processing resources that must be employed for the space station program, it is important to note the distinction between the use of on-board computer-assisted methods to perform the scheduling function itself, as compared to the scheduled employment of these data processing resources to support station operations and experiments. Implications of these two areas are as follows:

1. Performance of scheduling function. It is envisioned that the on-board scheduling functions will be performed on the station operations central processor of the data processing assembly. There are two functions which involve resource allocation, both of which are noncritical information subsystem operations. Characteristics of these functions are as follows:

Function	Required Operating Memory	Required Mass Memory	Anticipated Operations
Planning and scheduling	2K words	21K words	Background
Logistics inventory control	2K words	8K words	2.3 KEAPS

It should be noted that these on-board estimates were predicated on a large proportion of the scheduling function being performed on the ground. Sizings were based upon the assumption that long-range and comprehensive weekly and monthly planning and scheduling activities will be performed on the ground with necessary data transmitted (data link or shuttle delivery) to the space station. The on-board planning and scheduling routines will provide for control, manipulation, and modification of the ground generated data.

It is quite possible that a heavier load of on-board scheduling requirements than those indicated above may be imposed on the space station, especially if it can be shown that interactive on-board scheduling is an efficient means for controlling the utilization of station resources. This would raise the storage and speed estimates, and thus impose increases in the overall memory and speed requirements for the central processors (CP's). The tradeoffs and implications of heavier on-board scheduling requirements will be discussed in subsequent sections of this report.

2. Employment of data processing resources for operations and experiments support. The emphasis throughout the ADT effort has been on the analysis and sizing of the station operations central processor. Since station operations have been comparatively well defined, specific estimates of the loads imposed on the DPA by the seven operational subsystems were compiled and used to size the speed requirements of the CP, as well as for sizing of operational, mass, and archival memory requirements. The assumption has been that experiment support will be performed by the second CP (the experiments central processor), but that the architecture and component parameters of this second CP will be identical to that of the operations CP.

Conceptually, the MSS system will differ from previous space projects in that major portions of the orbiting station's mission management functions will be performed on-board the station. The ground-based mission control and experiment control centers will monitor, back up, and supplement the on-board mission management, plus serve as points of coordination for system users. Recommendations for computer-assisted allocation, scheduling, and planning techniques presented in this section are based on the assumption that the above described operating philosophy will be implemented.

To meet the planning, scheduling, and allocation requirements of the total MSS operational system, a computer program system which provides a centralized source of scheduling information which may be changed or queried on demand is recommended. Significant features of this scheduling system should be:

- General applicability
- User-oriented
- Accommodation of constraints and priorities
- Conflict identification and resolution
- Generation and maintenance of current data buses

The total scheduling system should consist of compatible installations on-board the space station and at the ground-based mission control center. Input/output terminals will be located at each installation and consist of interactive display consoles equipped with functional keys, alphanumeric keyboards, light-pens, and channel selection keys to provide access to and control of the data base.

The data base should consist of the following basic categories of data:

1. Environment. Current condition information on all system parameters

2. Task. Information on requested scheduled activities and required resources

3. Event. Information on past and predicted future events; performance, execution times, resources utilized and relationships to other events

4. Display. Preformatted displays which can be requested by the system operators.

On-line access to the large data base is the basic operating concept of the system. As new data become available, or as changes in scheduling requirements and resource conditions occur, on-line access to the data base provides console operators on board the station and at mission control the most effective means of facilitating their decision-making responsibilities, while at the same time, increasing the span of control over the resource allocation and schedule implementation functions. Interaction with the operational data base is an integral part of this process. The system outputs "working" displays of operator selected data, providing computer-generated responses as the interactive console operator performs additions, deletions, and modifications to the data base being presented.

Major capabilities of the system will be as follows:

1. Data base formulation. Provides on-line input of system environment, scheduling requirements, selection and scheduling criteria, non-space station associated support requests, and batch input of space station information and post-event reports.

2. Data retrieval. Provides access to the data base through various media.

   a. TV displays: space station characteristics, ground-station capabilities, space station activity plot, ground-station activity plot, space station schedules, ground station schedules, priority lists, and parameter entry displays for data control functions

   b. Printed listings: space station schedules, ground-station schedules, space station characteristics, ground-station capabilities, priority lists, and printouts depicting results from data base editing functions

c. Teletype format paper tape: space station schedules for use by the operations control center, supporting stations, and other system users

3. Data base control. Provides control of the information in the data base by utilization of alphanumeric keyboards and light-pen device for interaction with TV displays, user-oriented data and control cards for batch input or requests or non-event associated activities, and magnetic tape and/or disc files for batch input of event summary data.

4. Scheduling. The scheduling capability provided by the system will allow a maximum of user control over the selection and scheduling of required support activities. There should be two basic modes of scheduling within the system - discrete and algorithmic.

   The discrete mode is defined here as the human process of selecting or scheduling one identifiable activity.

   Conversely, the algorithmic mode is defined as the computer program processing of selecting and/or scheduling one or more identifiable activities during one continuous operation.

   The discrete mode provides the capability of retrieving information on a particular event or activity, querying the system as to conflicts or constraints concerning that activity, and assigning a desired status.

   The algorithmic mode provides facilities for (1) scheduling an aggregate of activities which have previously been "requested" as a function of the discrete mode, and (2) scheduling of space station functions which are selected by the program on the basis of scheduling requirements defined in the system environment. The first method searches the data base for all activities satisfying operator-selected conditions (e.g., time span, ground-station, space station, support type, etc.) and whose schedule status is "requested." For each "requested" activity encountered, the function will change its status to "scheduled" if no resource conflict exists. If a conflict exists, a conflict summary printout will be generated Conflict resolution is performed as a function of the discrete mode of scheduling.

   The second method searches the data base for space station activities which satisfy the scheduling requirements defined in the system environment and which are not in conflict with activities already scheduled, and assigns a status of "scheduled" to each selected task. In addition, this method schedules "requested" tasks where possible. When requirements cannot be satisfied, a conflict summary printout is generated. Again, subsequent conflict resolution may be performed as a function of the discrete mode.

5. General file editing. Provides the console operator with general data base maintenance functions:

   a. Delete, add, or modify individual support activities

   b. Delete a series of support activities

   c. Slide the support times associated with a series of space station passes forward or backward in time

   d. Purge the data base, deleting support activities prior to a specified time

6. Display control. Provides the capability to assign any display appearing on an interactive console to any channel on the TV video drum for subsequent call-up by monitor positions.

7. Data base protection. Certain data base protection features are provided to reduce the possibility of both interactive console operators attempting to modify support activities that cover the same time span. Requests for certain functions in the system will be honored only when another console is quiescent, effectively locking out the other console for the duration of that function. Examples of functions falling under this restriction are purges of the data base, input of new pass summary information, slides of activities, and input of station post-pass reports. Generally, this restriction will apply to any function which would effect massive data file restructuring.

   Additionally, alarms will be displayed to the interactive console operator when he attempts to modify support activities whose start times are later than the beginning of the next daily schedule to be generated.

The same basic system capabilities should be provided for the on-board and ground-based portions of the total system. However, capability and capacity should be implemented to meet the following operational philosophy:

a. On-board space station planning, scheduling, and allocation functions should be confined to a specific operational time span. This time span should be of sufficient duration to meet all but long-range planning needs.

b. Ground-based planning, scheduling and allocation functions should consist of support and verification of those performed on the space station plus long-range planning with optimization study and analysis, i.e., the ground-based scheduling system should function operationally to support the space station, but should also be used to perform long-range studies of new and/or modified system requirements.

6.0 DPA SUPERVISOR PROGRAM

The supervisory function is essentially that of keeping a data processing system usefully occupied. This requires scheduling and activation of the various software tasks that perform all the system functions. This, in turn, involves monitoring events, allocating resources, and providing proper interfaces among separate software modules, among hardware modules, and between the software and hardware. The supervisor must also respond to anomalous events, or errors, and initiate procedures to correct errors, isolate failures and, when possible, reconfigure the system to keep operating in spite of failures. In addition, the supervisor should maintain records for later analysis to identify hardware and software deficiencies that produce errors or otherwise adversely affect system performance. Since the supervisor itself is an overhead item that does not directly perform system functions, its intrusions (time and facilities used) should be kept to a minimum.

6.1 MODULAR SPACE STATION OPERATIONS CONTROL CENTRAL PROCESSOR SUPERVISOR COMPUTER PROGRAM SPECIFICATION (PRELIMINARY)

6.1.1 Scope

This specification establishes the requirements for the supervisory software in the data processing assembly of the modular space station. In its present form, the specification is restricted to that part of the software that resides in the central processor dedicated to station operations.

6.1.2 Requirements

6.1.2.1 System Considerations

The supervisor will be controlling the activity and assignment of all hardware and software elements within a central processor and will monitor the status of all elements of the DPA. All software elements will be well tested and essentially debugged. The software will consist of application programs written to support MSS operations, the supervisor program being described, and various utility programs and subroutines available to all programs. All programs will be broken into independently executable modules, each of which will have a module control block (MCB) that will provide the supervisor with information needed to respond to and control each module. All internal application data will be either public or private, the public data being available in essentially fixed locations and the private data for use within a module or for communicating between modules being in blocks temporarily assigned to the given modules by the supervisor. Data for communication with elements of the DPA outside a central processor will be kept in buffers set up by the supervisor and maintained by the input/output processor programs.

Since the programs will all be cooperative and essentially debugged, it is not certain how much protection will be necessary for the information in memory. A certain amount of protection will be necessary for maintaining the integrity of critical programs and data, and checks may be necessary for some reading and many writing operations between M1 and M2 memories to prevent errors from propagating. The supervisor will be involved in such security, but the division of these functions between hardware (to save time) and software (for flexibility) is yet to be determined.

The module control blocks will have at least the following information for the supervisor:

(a) Code name of the program module. Indication of whether it is a subroutine.

(b) Activation indicator. A set of n bits to allow the conditional scheduling of this module by other modules or I/O operations.

(c) The number and identity of fixed-size data blocks required by this module for variable storage and intermodule communication.

(d) Which data blocks may be released on completion of this module.

(e) Code names of the program modules, each with a corresponding activation bit, which are to be successors of this module. If this module is a subroutine, the name (return module) will be provided by the module scheduling this subroutine. If a code name in (e) is that of a subroutine, another name <u>must</u> be provided for the subroutine's return.

(f) Delay times. If the module to be scheduled is not time-dependent, this delay may be zero, implying it can be scheduled without having to wait for the passage of time.

The input/output (I/O) section of the central processor will be executing I/O programs in parallel with the arithmetic units. It will communicate with the supervisor by means of I/O control blocks (I/OCB) which will contain at least the following information:

(a) Identification of the source (input) or destination (output) of the information being transmitted and the route (DDB).

(b) The location and size of the buffer in M2 containing the information.

(c) An indication of the last word communicated (either a counter or a pointer to the buffer).

(d) Indications of any errors in the transmission, the numbers and sources of the errors.

(e) The name of the program module to be scheduled on completion of the I/O operation and activity and completion indicators.

The I/OCB's will be initialized by the supervisor to start an I/O operation. The I/O processor will maintain them from then until the data transmission is completed or the supervisor terminates the operation. Certain I/OCB's will be permanently scheduled to receive inputs that are initiated by elements of the MSS outside the DPA. Any error indications detected by the I/O processor will initiate a recovery attempt which, if unsuccessful, will treat the error as a failure.

6.1.2.2 Performance Requirements

This section establishes the functions that must be performed by the supervisor. These are divided into the four general areas as shown in Figure 6-1. The performance requirements are detailed in Volume V, with only the important features discussed below.

Status Monitor. The supervisor must be aware of the current status of all DPA elements. A monitor program shall maintain status tables from which the resource allocation and scheduling programs can obtain the information necessary for their decisions. In addition, the monitor will alert the crew and/or other subsystems of the MSS of any significant status changes that will affect station operations. A portion of the monitor shall be permanently scheduled on a periodic basis. It will perform checks on the hardware that is not automatically tested (e.g., comparators, parity checkers and other testing circuits) or has just been entered into service (either a new module or one just repaired). Requests for particular responses will be sent to each element of the DPA (RPU's, RACU's, and the alternate central processor set) and the lack of the required response within a prescribed time will be treated as an error. In particular, the operation and experiment processors must monitor each other so that the experiment processor can take over station operation if the other processor fails. Note that some of this system testing might be done with hardware.

Status Tables. Every in-flight replaceable unit (IFRU) in the DPA shall have associated with it an entry that contains the following items to be maintained by the monitor:

(a) Activity status (active or standby)
(b) Functional status (functional, failed, under repair test)
(c) Number of transient errors in a given period
(d) Allowable transient errors in a given period
(e) Time period for above (but only if different for different IFRU's)

The supervisor shall respond to three kinds of requests for its services; direct requests from active program modules, indirect requests from I/O processor, and emergency requests through interrupts. The normal means for activation of the supervisor will be through a direct call by one of the active applications program modules. In the multiprocessing environment, there are three possibilities, and the processor receiving the supervisor call first must inhibit the other processor from also responding to a supervisor call until the active supervisor has determined the situation. Having determined the situation and performed the necessary checks, the supervisor will remove the calling module's

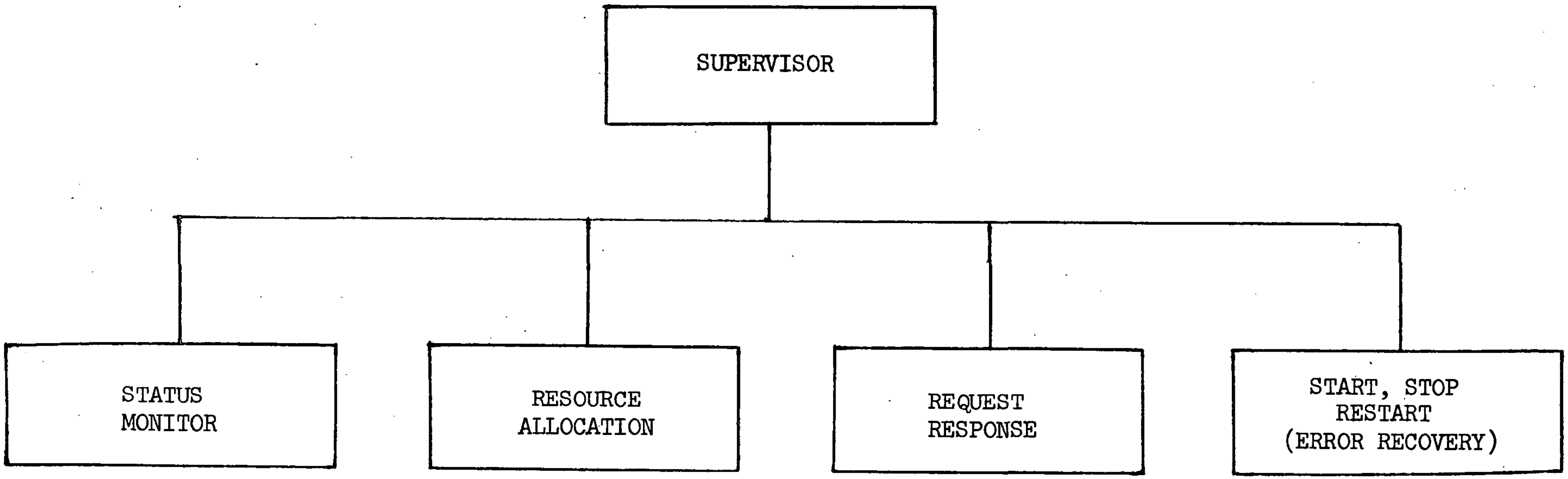

Figure 6-1. General Supervisory Functions

MCB from the waiting list, reset its activation indicators, and perform the memory management, I/O and scheduling functions specified in the supervisor call.

A program module releases a temporary data block when the information it contains is not needed by any of its successors. The memory space for this data block becomes available to other modules. The supervisor shall keep a list of these available blocks and add to this list any released by a module when it calls the supervisor. Those data blocks not released shall be retained for use by successor modules.

The major scheduling decisions will be built into the application programs. Each program module will call for its successor(s) to be activated, and the MCB for each program module will contain an activation indicator specifying how many (and which) modules will have to call for it before it is activated. Each subroutine module scheduled through the supervisor will have its successor (return) specified by the module that calls it. Input/output operations will be treated as other program modules except their data blocks will be called buffers and their successors will be determined indirectly. Periodic modules, will, in addition, have a time delay inherent in their MCB's or set by other modules.

The supervisor shall maintain an internal clock that will be periodically synchronized with an external clock (either part of the MSS or a time signal transmitted by a ground station). In addition to the master clock, the supervisor shall provide interval timers for the various time intervals required by the scheduler. These may be separate hardware countdown timers (noninterrupting) or timers maintained by the supervisor by reference to a single countdown timer. The supervisor shall also maintain countdown timers for the various testing functions required (e.g., program module timing, timing of responses from other DPS or MSS elements, etc.).

The supervisor shall maintain a list of available resources, including all elements of the DPA and time, and associate these resources with program modules to assure efficient use of these resources in the execution of the functional applications programs. The monitor shall indicate whether a particular DPA element is operational. The resource allocator shall keep track of which program modules on the waiting list require what resources and shall assign currently unassigned resources in such a manner as to make the most efficient use of these resources. The resources to be allocated consist of: time, processors, and data blocks for program modules; I/O processor, DDB channels, RPU's, RACU's for I/O programs; and M2 or M3 memory space for programs to be loaded or data to be saved.

The monitor and recorder functions shall maintain proper status history records to support the resource allocation algorithms in both system degradation and system recovery. Whenever there is a change in the operational resources (an element fails or a repair element added), the resource allocation algorithms must be aware of the event (through access to the monitor's status tables) and adapt accordingly. These algorithms will be sensitive to the sequence of events as well as the current status and must adapt in such a manner as to:

(a) Guarantee crew safety and MSS integrity
(b) Support critical MSS functions
(c) Guarantee proper operation of the DPA
(d) Support the experiment data processing

The supervisor shall keep track of available memory data blocks. If any of the program modules in the waiting list require the allocation of data blocks, the available data blocks shall be distributed among them in the most efficient manner. All program modules on the waiting list are automatically ready for execution if they need no additional data blocks. Those program modules on the highest priority waiting list shall be allocated data blocks first, if there are enough available to make them ready. The allocation algorithm shall avoid the deadlock problem of partial allocation to several programs from a limited availability list.

The supervisor shall allocate the I/O processor to a particular I/O operation by activating the associated IOCB. The I/O processor shall maintain its own scheduling and timing by reference to the active IOCB list. Buffers will already have been allocated for I/O by the modules which scheduled the I/O; the data blocks allocated to those modules become the buffers for the I/O processor. The I/O processor will take care of all the I/O error detection and recovery.

The supervisor shall provide for integrating all working elements of the DPA into a working system and to isolate all failed elements in a manner that will not adversely affect other subsystems of the MSS. This implies the ability to bring the system into operation from a cold start as well as accepting the replacement of a repaired IFRU that had previously failed, or a new IFRU to allow modular expansion of the system. The isolation of an element applied in the proper sequence to all elements allows safe shutdown of the entire system. These functions will require some assistance from the hardware and, in fact, the DPA is designed to take much of the burden from the supervisor software.

Data Base Requirements. The amount and format of the supervisor's data base is not yet determined, but the following items shall be included.

(a) Status tables. A table showing the status of each element in the DPA shall be maintained.

(b) Module control blocks. A table describing each software module in the program system shall be maintained. Each entry in this table shall consist of a module control block. Either copies of or points to MCB's shall be maintained in a waiting list in priority queues for all modules scheduled and waiting for execution.

(c) I/O control blocks. A table describing each I/O process shall be maintained. Each entry in this table shall consist of an I/O control block. Either copies of or pointers to IOCB's shall be maintained in an active I/O list for communication with the I/O processor.

(d) Data blocks and buffers. The data blocks and buffers (which may be interchangeable, the name applied implying use by a program module or an I/O program) are properly part of the applications programs; but the supervisor shall maintain a list of pointers to all data blocks/buffers with an indication for each whether or not it is allocated to a program module or I/O program.

The supervisor shall be coded in machine or assembly language. This will assure the maximum efficiency in the use of the data processor's features to attain speed of execution and completeness of error checking. The requirements for change in such a program are less extensive than those for applications programs, therefore a higher order language does not offer as much advantage. Also, many of the executive functions are highly machine dependent, which makes higher order languages, in general, unsuitable.

The supervisor is unique in that it can include features to aid in testing not only itself, but also all other program modules. Some of the error detection, status monitoring, data recording, and memory protection features included in the executive can be expanded to aid in program bug detection. These features can be useful in the development of the supervisor itself, but will be even more useful in the development of the application programs. The debugging features of the supervisor should therefore be developed early and designed in such a manner as to be easily removable or reducible. Thus, they will not use up time and memory overhead as the system becomes operational and the debugging and testing features can be left on the ground.

7.0 RECOMMENDATIONS FOR UTILIZATION OF ADT ACCOMPLISHMENTS

It was indicated in the introduction that the present ADT effort does not complete the definition of the MSS information subsystem, and that future studies and evaluations would be needed to define the equipment and software specifications. There is, however, much that can be learned by using the present breadboards and studies. Table 7-1 lists the current ADT accomplishments as reported in this document.

Table 7-1. Current ADT Accomplishments

Communications terminal	MSS - Representative K-band Electronics Communication System Specification
Digital data bus	MSS - Representative cabling configuration 10×10^6 bit/sec capability Integrated with RACU, RPU, DBCU, and test processor (DACS)
Data processor	DPA System Specification and DPA Supervisory Specification Bulk memory technology evaluation MSS subsystem support requirements definition Memory and internal traffic studies
Software	DPA throughput simulation Data organization studies Software standards and conventions Processing flow charts (subsystem support)

Table 7-2 indicates the possible utilization of the equipment breadboards for (1) stand-alone testing of the design concepts, and (2) combined testing for defining interface and integration requirements. Stand-alone testing would be accomplished using laboratory and simulated environments and situations to determine the strengths and/or shortcomings of these particular breadboard equipments for certain applications. It should be emphasized that these equipments, while developed to demonstrate MSS concepts, are by no means limited in application to that vehicle. The shuttle, sortie modules, RAM (and certain unmanned satellites) and ground-support installations can certainly be influenced and benefit from these evaluations.

A second point of emphasis is that the NR-MSC breadboards are functional and performance duals with the McDAC-MSFC breadboards, and that the implementation approach (mechanization) is different in both cases (DACS and CTB). There is an excellent opportunity to conduct parallel, comparative tests, using the same conditions and procedures on the similar equipments. The purpose would

Table 7-2. Utilization of Results

PERFORMANCE AND INTEGRATED EVALUATIONS USING CURRENT BREADBOARDS	
K-BAND ELECTRONICS DATA ACQUISITION/CONTROL	CURRENT HARDWARE BREADBOARDS
Design Concept and Performance Testing to Determine: Equipment and assembly performance Thermal and thermal/vacuum environment effects Fault detection and reconfiguration control operating limits Redundancy and error protection features	
Refinement of System Specification	
Development of OBCO Software Requirements	
Development of Integrated System Test Plan	
System Evaluations Using Augmented Breadboards	
Communications terminal plus DACS ECLSS subsystem breadboard plus DACS Solar panel prototype plus DACS Remote processor plus G&C	Integration tests to determine: OBCO parameters and procedures Automation algorithms Develop interface specifications
Experiment Technology Investigations	
DACS plus experiment sensors (simulated or prototype)	Experiment sensor monitoring, control, automation, data flow, data forms, rates, quantities
Man-Machine Technology Investigations	
DACS plus console plus subsystem breadboards	Subsystem fault isolation Communication scheduling/control Vehicle power management Subsystem configuration control
Payload Technology Development	
DACS plus console plus experimentor sensors	Experimentor data "quick-look" and editing Experimentor scheduling/control Sensor configuration/data quality

not be to "prove" which was best, but to determine which features are most applicable to given situations. From this additional knowledge the equipment and interface specifications for flight hardware (shuttle, sortie, RAM) can be developed with assurance.

Combined testing of these breadboards and other equipment developments would have even more beneficial results. No spacecraft subsystem is independent of other subsystems, and very certainly, it is the data and control system that links them together. Automation of many spacecraft functions require that certain parts of conventional subsystems must operate cooperatively and this will have considerable influence on the design requirements for these equipments. Again, it is the DACS/DMS capabilities that are needed to augment the interaction. Using the DACS breadboards as a "test bed" results in much useable knowledge being obtained to develop the vehicle system specifications.

Even more useful is the ability to use DACS or the DMS to investigate the role of the crew to manage the vehicle, its operations, and the related experiment operations. The present DACS, together with a console (not part of ADT) provides a flexible, efficient test bed by which to develop the software and display formats needed for a man-directed information system. It has been reiterated on numerous occasions that the DPA software, and the crew-interactive procedures, are the least well-defined and most difficult of all the ISS definition requirements. Figure 7-1 indicates that the next phase of the IMS ADT program should consider developing the man-machine interface (console and portable control unit), and continue the software development in terms of languages, algorithms (particularly for automation of other subsystems), and extend the studies to allocate functions to the different elements of the total information management system. Space Division Report, SD 71-240, "Information Management Advanced Development Technology Extension Plan," (1 October 1971) expands the details of the recommended actions.

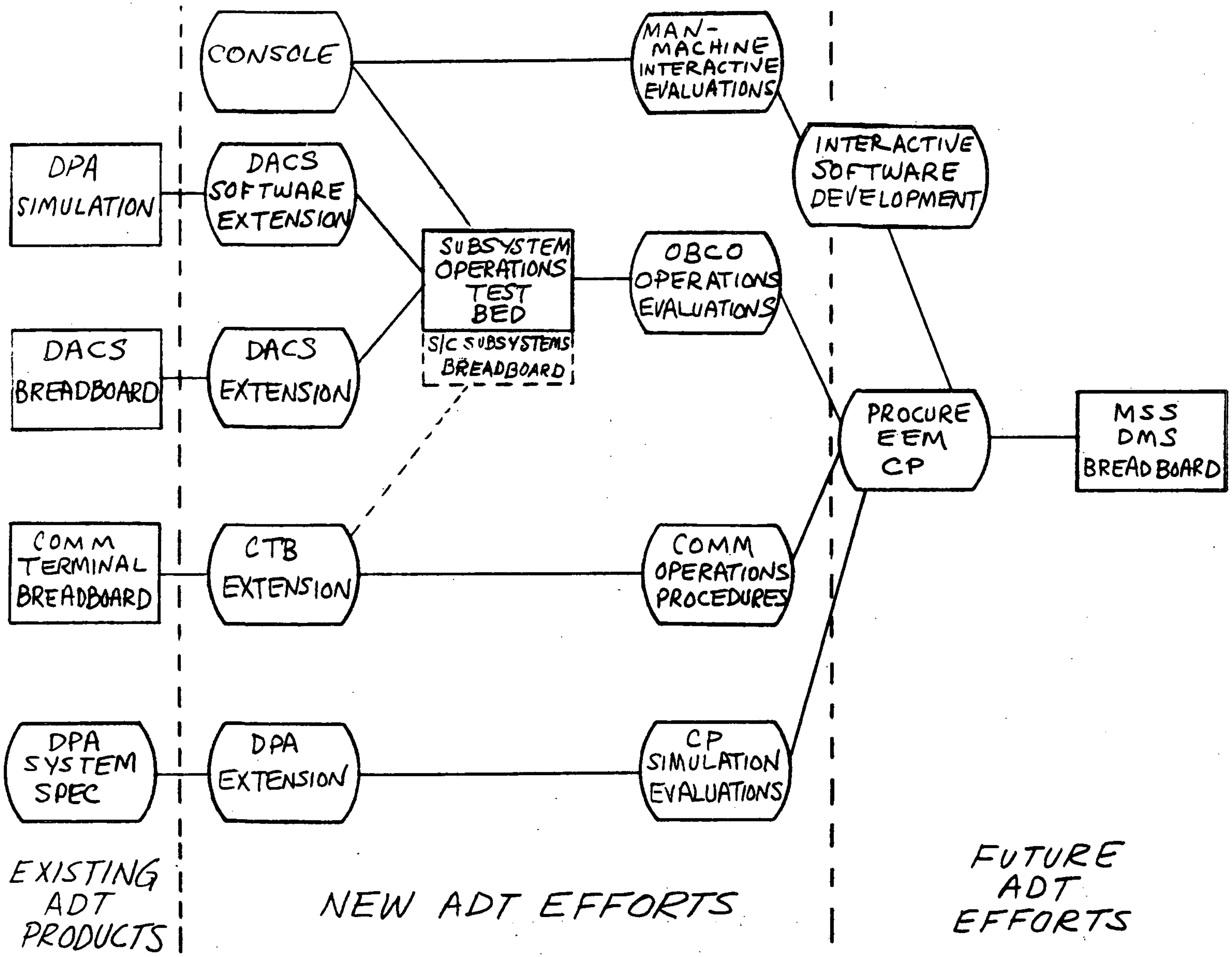

Figure 7-1. Advanced Development Task Extension (First-Level Flow)