February 1973

B73-10054

NASA TECH BRIEF

Marshall Space Flight Center

Glass Encapsulation Provides Extra Protection for IC Semiconductor Devices

The problem:

Semiconductor devices used in integrated circuits (IC's) are sensitive to surface contaminants such as moisture, ionic particles, and dust. Extreme cleanliness is required during the manufacture of these IC's, and the finished product must be hermetically sealed.

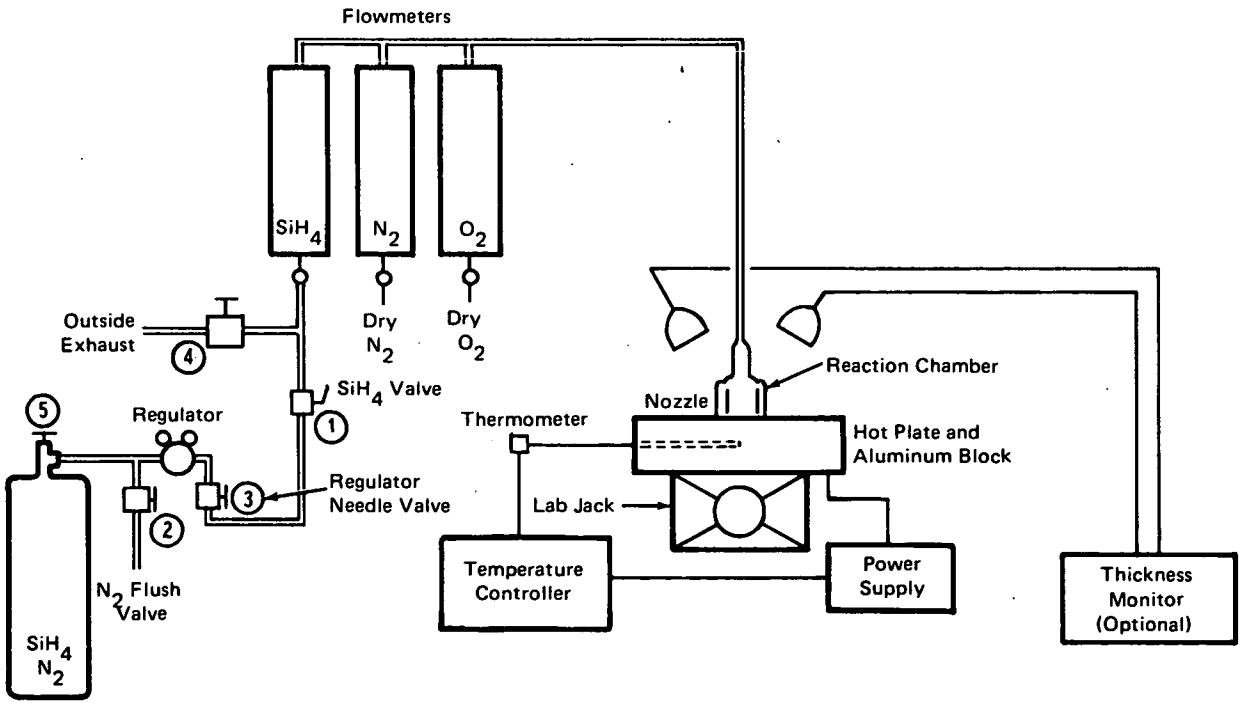
The solution:

An oxide-passivated semiconductor chip is given a protective glass coating by means of vapor deposition over the metallic substrate of the IC. This method provides more reliable protection for semiconductor elements than the combination of oxide-passivation and hermetic sealing in current use. Furthermore, chips and scratches incurred during dicing, testing, and assembly of the semiconductor are markedly reduced.

How it's done:

The semiconductor is coated with vitreous SiO_2 by what is essentially a molecular deposition process. Silane (SiH_4) reacts with oxygen to form SiO_2 as follows:

$$SiH_{4(g)} + 2O_{2(g)} = SiO_{2(s)} + 2H_2O_{(g)}$$



(continued overleaf)

This reaction occurs spontaneously at room temperature to form a powdery SiO_2 colloid. However, by diluting the SiH_4 with nitrogen (3 to 4% by volume), the conditions for the reaction are changed, and the rate may be controlled to allow deposition of a transparent, adherent film of SiO_2 on a semiconductor at temperatures ranging from 200 to 500° C.

The apparatus used for the deposition is shown in the figure. The reaction chamber produces a uniform flow of the mixed gases over the deposition area. This flow, the temperature, and the ratio of gases in the reaction mixture determine the quantity and rate of deposition. The materials to be coated are placed on an aluminum block under the reaction chamber and heated by the hot plate. The exhaust gases are removed through an exhaust valve in a second chamber that encloses the reaction chamber.

Testing has shown that the optimal processing stage at which to encapsulate the devices is while they are in wafer form, although they may be further encapsulated after assembly. Electrical connections to the encapsulated assembly are etched in the glass by use of photoresist masks.

The coating is stable under extreme conditions. Coated devices were tested and proven reliable under thermal shock (variations from −65 to 200° C); baking at 200° C for 16 hours; and subjection to 30 G vibration and constant acceleration.

The encapsulation itself is economical and is compatible with processing steps in the production of IC's. It provides a uniformly thick deposit over large areas and can coat the sides as well as the top of the device. Glass encapsulated devices have several desirable features in addition to the high level of mechanical protection. The coating provides high resistivity, low dielectric constant, and an adequate dielectric strength. The glass serves as the dielectric layer between various levels of metal interconnect and may be used to increase the dielectric thickness between metal overruns and the underlying silicon, thus reducing the fields which cause surface channeling. An increased dielectric thickness also reduces parasitic capacitive coupling.

Notes:

1. Information concerning this innovation may be of interest to manufacturers of semiconductor devices.
2. Requests for further information may be directed to:
   Technology Utilization Officer
   Marshall Space Flight Center
   Code A&PS-TU
   Marshall Space Flight Center, Alabama 35812
   Reference: B73-10054

Patent status:

NASA has decided not to apply for a patent.

Source: W. L. Doelp, Jr. of
Philco-Ford Corp.
under contract to
Marshall Space Flight Center
(MFS-21310)