June 1973

B73-10093

NASA TECH BRIEF

Lyndon B. Johnson Space Center

Four-Phase Differential Phase Shift Resolver

The problem:

Four-phase differential phase shift (DPSK) systems require a phase reference to resolve phase uncertainty during demodulation. Of the systems currently used, locally generated phase references introduce a phase uncertainty; references derived from a single received bit are noisy; and transmitted phase references use up a portion of the bandwidth and signal power, resulting in a reduction in the signal-to-noise ratio.

The solution:

Two similar systems have been developed, both of which resolve phase uncertainty without transmitting reference signals or compromising the signal in any way. In both methods the signal is impressed on the carrier as a differential, rather than an absolute, phase shift. A transmitter-encoder uses a two-bit accumulating adder to put a phase-shift code on a selected phase of the subcarrier. At the receiver, a four-phase demodulation and logic process unambiguously resolves the differential phase shift of the input carrier. Two receiving methods have been developed. In one method, a two-bit subtractor extracts the reference code and, in the second method, a decoder with a more general algorithm is used for the decoding.

How it's done:

In both systems, the signal is encoded upon transmission as shown in Figure 1. At the input to the encoder, the two synchronized bit streams are applied to the input of a two-bit adder. Also input to the adder are two bits representing the accumulated sum of all past inputs. The four outputs A, $\overline{A}$, B, and $\overline{B}$ are combined logically in the quadriphase modulator with the four outputs from the four-phase generator. It is the phase shift and not the absolute phase that is the important parameter. The four-phase output from the modulator passes through a bandpass filter to remove unwanted harmonics and can be transmitted directly over a telephone line or as a carrier (or subcarrier) in an RF transmission link.

At the reception point, the signal is demodulated as shown in Figure 2. The frequency of the incoming signal is doubled twice (multiplied by four), by squaring and filtering, to give a signal at four times the carrier frequency ($4f_o$). Since sine waves at the same frequency

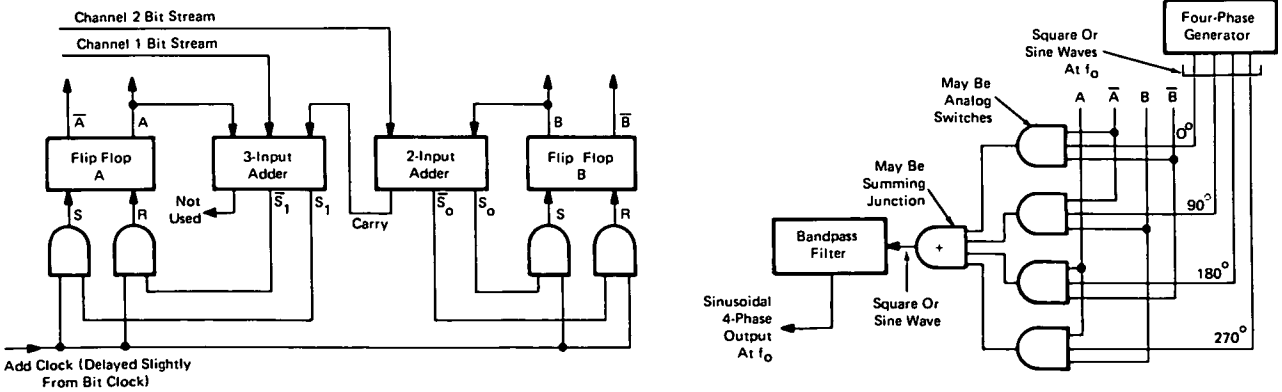

Figure 1. Adding Encoder/Modulator

(continued overleaf)

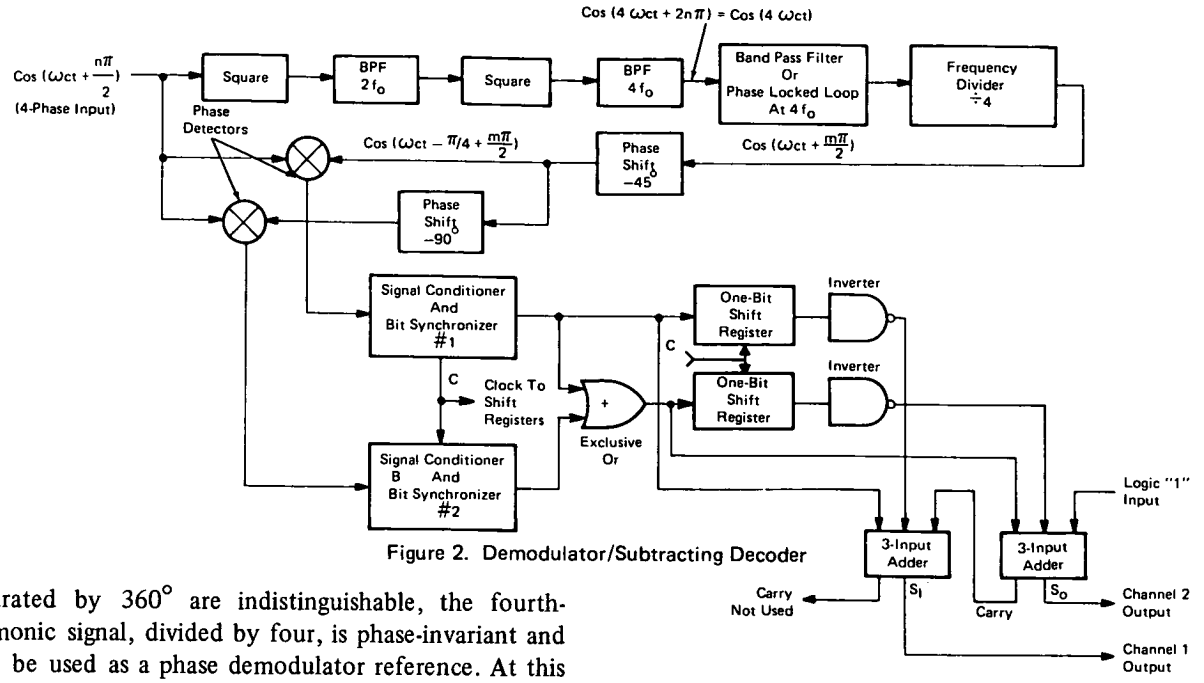

Figure 2. Demodulator/Subtracting Decoder

separated by 360° are indistinguishable, the fourth-harmonic signal, divided by four, is phase-invariant and may be used as a phase demodulator reference. At this point there is an unavoidable uncertainty in phase. However, the reference phase can be made to match the carrier phase within 90°. A 45° phase shift places the demodulator reference-phase equidistant between two of the received phases.

It is not necessary to determine the absolute phase of the reference signal; an unambiguous signal may be constructed by detecting the differential phase shift of the carrier between successive bit periods. One method of doing this is shown in Figure 2. A two bit accumulating subtractor is used to decode the signal. Signal conditioners and bit synchronizers are used to remove noise and produce two synchronized binary bit streams that are input to the subtracting decoder. In the decoder, the "exclusive-or" gate performs a count correction to produce an output identical to the output of the accumulating adder in the encoder.

The input data can be retrieved by taking successive differences between the bit pair output from the count corrector and the previous bit pair stored in the shift register. Subtraction is accomplished with a binary two-bit adder.

Another decoding technique (not shown) uses a phase resolver with a more general algorithm in place of the two-bit subtractor. As before, the two one-bit shift registers serve as a one-bit-period memory. The outputs of the bit synchronizers are compared with the outputs of the shift registers. A transition logic detects differences between the input phase status signals and the stored phase status signals and inputs a signal representing this change to the resolver logic.

The resolver logic forms phase shift indicator signals which are decoded into output data bits. The output data bits are assigned in accordance with the encoding performed at the transmitter

Both of these systems transmit and receive data without ambiguity and allow unique identification of two data channels without transmitting identification sequences.

Note:

Requests for further information may be directed to:

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Patent status:

This invention is owned by NASA, and a patent application has been filed. Inquiries concerning non-exclusive or exclusive license for its commercial development should be addressed to:

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W. M. Wallingford of
Lockheed Electronics Co.
under contract to
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