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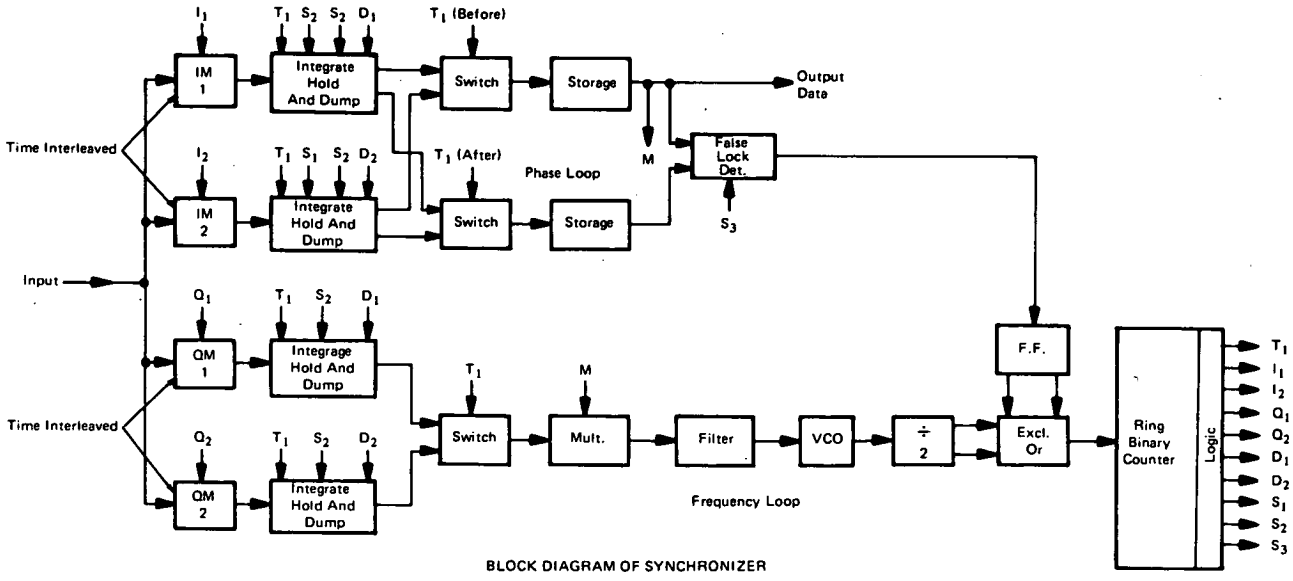
A Technique to Eliminate False Lock in PCM Demodulation



BLOCK DIAGRAM OF SYNCHRONIZER

The problem:

The transmission of data requires some medium and a code for the transmitted intelligence. The transmission medium may be an electrical or mechanical system. For long distances, radio (more generally, some form of electromagnetic radiation) is frequently used. One of the ways of incorporating data into an electromagnetic carrier wave is pulse code modulation (PCM). Here each pulse in the transmitted signal corresponds to a particular data bit. The information is transmitted in a frame (a cycle of data compilation) in which one or more words comprise a synchronizing code. At the receiver, where the information is extracted from the carrier by demodulation, the circuits determine the correct point to begin interpreting the data by matching the synchronizing code. To make sure that noise in the transmission does not cause an error in the synchronization, the synchronizer must contain a means of holding the frequency stable in the presence of noise. Even then, in split phase PCM, error may arise due to "false-lock", a condition in which the synchronized frequency is correct, but is actually 180° or 1/2 bit-time out of phase.

The solution:

The bit synchronizer uses one loop circuit, called the quadrature loop, to stabilize the frequency and another loop to detect the coherence of the input signal and the generated signal, called the in-phase loop. The first loop provides an error signal which adjusts the voltage controlled oscillator (VCO) to match the incoming signal. The other loop multiplies the input signal with the generated in-phase signal. The signals from both these loops are integrated over the bit period. The first loop detects a null which indicates a lockup, and the second loop emphasizes the input signal information.

(continued overleaf)

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How it's done:

The synchronizer circuit is shown in the figure. The synchronization frequency is generated by a voltage-controlled oscillator (VCO), a divide-by-two circuit, an "exclusive-or" for shifting bit synchronization 180° or 1/2 bit period and a binary counter and logic circuit. Parallel channels receive the transmitted PCM signal which is multiplied in the quadrature (Q) loop with the output from the logic circuit. When the multiplication indicates that the incoming and generated signals are not phase-locked, an error signal (at the end of each bit time) to the VCO adjusts the generated frequency until it matches the input.

At the end of each bit-time the polarity of the error signal is corrected by the detection of a "1" or a "0" in the in-phase loop. At this point the frequencies are matched, but the bit synchronizer may be locked correctly (true lock), or it may be locked off-phase by 180° or 1/2 bit-time (false-lock).

In the in-phase (I) loop, the multipliers combine the input signal with the generated signal from the logic circuit. The in-phase signals are time interleaved so the I signal can be integrated, held, and dumped over a complete bit period. The output of the I loop appears as an "up" ramp (for example a "1") and as a "down" ramp (for example a "0"). These ramps are sampled at the end of each bit-time and represent output data. This data is also used in the Q loop to correct the polarity of the error signal for the VCO.

For false lock detection, the I loop ramp is sampled twice each bit period: once before the end of bit-time and once after the end of bit-time. When the bit synchronizer is true locked, the integrated I signal will appear as a right trapezoid; thus, both samples will be the same; (that is, positive or negative). When the bit synchronizer is false-locked the integrated I signal will appear as an isosceles triangle. Both samples will be different, this difference is detected, and the bit synchronizer bit-time is shifted 180° or 1/2 bit-time by the "exclusive or" circuit. The bit synchronizer bit-time is shifted by shifting the I and Q generated signal 180°.

Notes:

1. A similar device is described in Tech Brief B73-10107
2. Request for further information may be directed to:
   Technology Utilization Officer
   Lyndon B. Johnson Space Center
   Code JM7
   Houston, TX 77058
   Reference: TSP73-10106

Patent status:

This invention is owned by NASA, and a patent application has been filed. Inquiries concerning non-exclusive and exclusive license for its commercial development should be addressed to:

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