NASA TECH BRIEF

Lyndon B. Johnson Space Center

Phase Shift Keyed, Pulse Code Modulated Signal Synchronizer

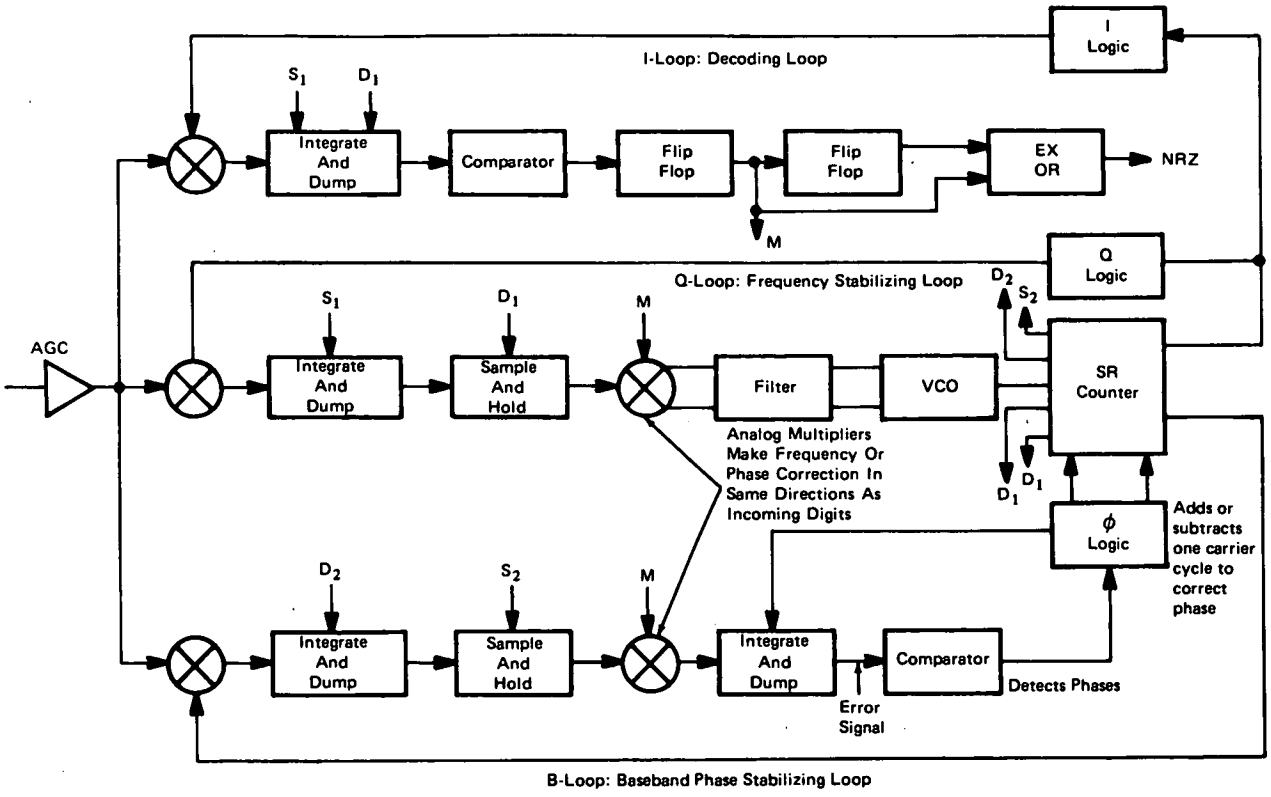

DIAGRAM OF SIGNAL SYNCHRONIZER

The problem:

Many data processing systems receive information impressed on an electromagnetic carrier (radio waves, for instance) in the form of pulses (pulse code modulation).

In one system the pulses represent a series of zeroes and ones (bits) which contain data coded by shifting the phase of a given subcarrier (phase shift keyed (PSK)). In cases where more than one subcarrier are used, the receiver may demodulate the higher subcarriers.

The solution:

A PSK split-phase, pulse code modulated (PCM) signal is demodulated and synchronized by three loop circuits: (1) a "Q" loop that uses a quadrature signal to stabilize the frequency, (2) a "B" loop that acts on a baseband signal (a continuous frequency signal) to stabilize the phase, and (3) a decoding "I" loop, which acts on an in-phase signal. In a system in which the receiver output is a PSK split-phase signal, this synchronizer may be used to eliminate false-lock. False

(continued overleaf)

lock occurs when the bit synchronizer bit-time differs from the incoming signal bit-time by 180° or 1/2 bit-time.

How it's done:

The circuit is shown in the block diagram. The incoming signal goes to an automatic gain control (AGC) amplifier circuit. Here a power divider splits the signal into three parts, each going to one of the three loops, "I", "Q", and "B".

In the frequency-stabilizing "Q" loop, a voltage-controlled oscillator (VCO) provides pulses to a logic circuit. This circuit generates PCM signals with a 90° subcarrier phase shift, to be multiplied with the incoming signal. The product is integrated and sampled to detect error signals that are used to adjust the VCO signal until it matches the incoming frequency. This loop contains another multiplier (M) that receives its input from the "I" circuit. It changes the polarity of the error signals so that the correction for frequency is in the same direction for either an "0" or "1" value of the incoming bits. The "Q" and "I" will lock up on many null points depending on the subcarrier-to-data ratio.

In the "B" loop a continuous VCO signal is multiplied with the incoming signals. During each bit period the "B" loop signal is integrated and sampled at the end of each bit-time. The second integrator accumulates each bit-time error in the proper polarity as determined by the "I" loop data until the threshold value of the comparator is reached. The comparator output goes to the logic circuit which advances or retracts the relative phase of the generated frequency one subcarrier cycle at a time. The "B" loop shifts out of all subcarrier cycle nulls except the true lock null and the false lock null.

The "I" loop is the decoding loop. Here the I-logic signal is multiplied with the incoming signal. During the sampling period, the value of the bit is determined, and the comparator operates the flip-flops and the "exclusive or" circuit to provide a bit indication that is the circuit output to a decommutator.

The false-lock in the PSK split-phase bit synchronizer is eliminated by the "Q" generated signal. The sensitivity or error signal is minimum for false-lock null while the error signal is maximum for the true lock null. By setting the "Q" loop sensitivity such that it will not lock on the minimum false-lock null, the bit synchronizer will always lock on the true-lock null.

Notes:

1. A similar device is described in Tech Brief B73-10106.
2. Requests for further information may be directed to:
   Technology Utilization Officer
   Lyndon B. Johnson Space Center
   Code JM7
   Houston, Texas 77058
   Reference: TSP73-10107

Patent status:

This invention is owned by NASA, and a patent application has been filed. Inquiries concerning non-exclusive or exclusive license for its commercial development should be addressed to:

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Source: Herbert S. Kobayashi
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