NASA TECH BRIEF

Lyndon B. Johnson Space Center

Complementary MOS Four-Phase Logic Circuits

The problem:

Logic circuits often use a four-phase clocking technique in conjunction with p-channel MOS (metal oxide semiconductor) devices to charge and discharge capacitors without providing a direct path from the power supply to ground. This arrangement saves considerable power compared to circuits having a load resistor between the power supply and ground. However, the p-channel, four-phase circuit has several disadvantages. Since it requires a four-phase clock, it cannot be used as a subassembly in a single-phase clock system without making prior provision for the clock generation. In addition, p-channel, four-phase circuits require two power supply voltages which makes it difficult to interface these circuits with other types.

The solution:

A complementary four-phase logic can provide a four-phase clock signal from a single-phase clock and requires only one power supply voltage.

How it's done:

The circuit uses complementary MOS devices as switches which charge and discharge capacitors in accordance with circuit requirements, but without a direct connection between the power supply and ground. Figure 1 shows the four-phase clock waveforms, and Figure 2 is a schematic of the four-phase circuits.

The Type 2 circuit described in detail as an example operates as follows: during clock time t_1 to t_2 (Figure 1), ϕ_1 turns transistor Q_3 (Figure 2 - Type 2) on and holds

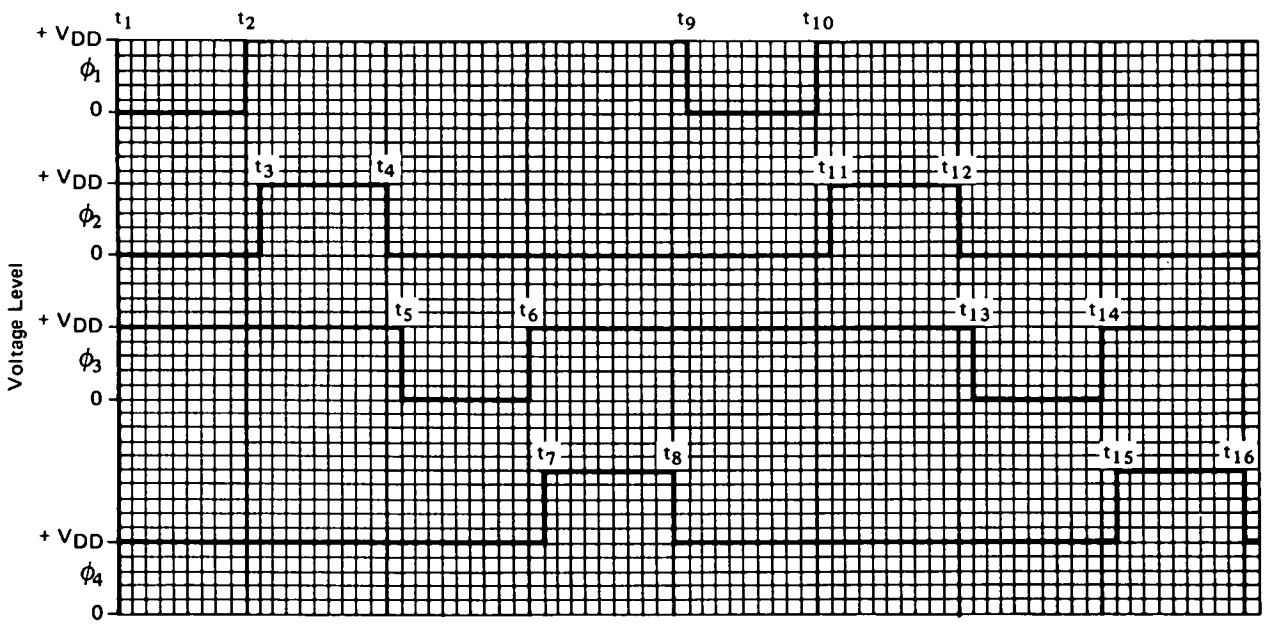

Figure 1. Complementary Four-Phase Clock Waveforms

(continued overleaf)

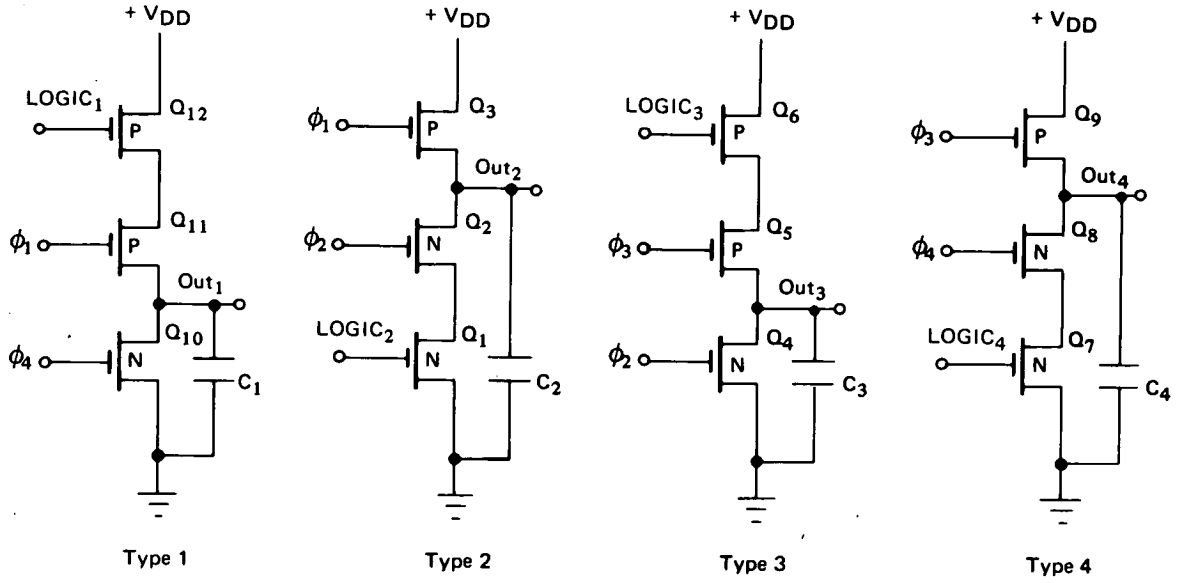

Figure 2. Complementary Four-Phase Circuits

transistor Q_2 off. This changes capacitor C_2 to $+V_{DD}$. From time t_3 to t_4, ϕ_1 turns Q_3 off and ϕ_2 turns Q_2 on. If at this time the input to Q_1 ($LOGIC_2$) is a logic "1" ($+V_{DD}$), Q_2 and Q_1 will form a conductive path which discharges C_2 to ground or logic "0". If, however, the input to Q_1 is a logic "0" (ground is zero volts), then C_2 remains charged to $+V_{DD}$ (logic "1"). The voltage on C_2 or the output of this circuit then remains unchanged and is valid during time t_4 to t_9. This circuit thus operates as an inverter which is precharged during t_1 to t_2, evaluated during t_3 to t_4, and valid during t_4 to t_9.

The Type 3 circuit operates in a similar manner and is also an inverter; it is precharged during t_3 to t_4, evaluated during t_5 to t_6, and valid during t_4 to t_9. Circuit Type 4 is similar to Type 2, and Type 1 similar to Type 3.

The four-phase clock waveform can be generated by the circuit from a single phase input. This can be done because the complementary inverter has a finite and predictable propagation delay. Thus, the output of the inverter is the inverse of the input, but is delayed by a small time. The output of a number of inverters can be joined in series and connected to logic gates to produce the required four-phase clock pulses shown in Figure 1.

Note:

Requests for further information may be directed to:
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Patent status:

This invention is owned by NASA, and a patent application has been filed. Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to:
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