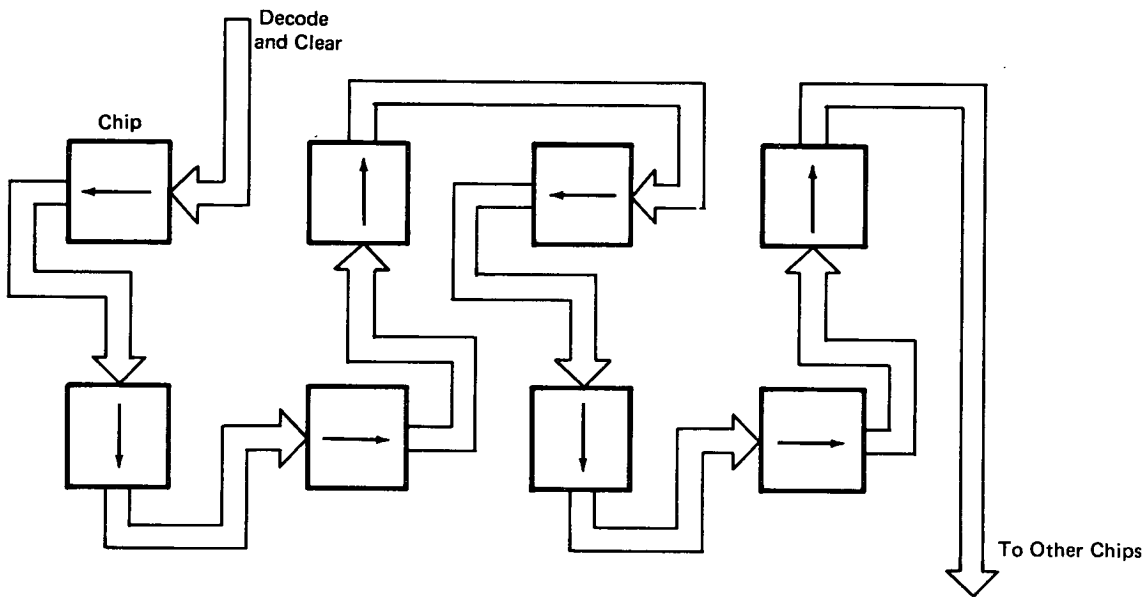
June 1973

B73-10202

NASA TECH BRIEF

Marshall Space Flight Center

Tetrad Bubble Domain Chip Arrangement for Multiplexing



Wiring Flow Diagram
for Tetrad Connection of Chips on Module

The problem:

It is difficult to provide a sufficiently large number of interconnections between the chips and modules of a large bubble domain memory to yield otherwise desirable chip and memory arrangements.

The solution:

The rotating magnetic field of a bubble domain memory is used to obtain time-division multiplexing of the bubble domain circuits into quadrants, thus allowing four-way multiplexing on sense and control lines.

How it's done:

A large (10^8-bit) bubble domain memory can be organized or partitioned in a number of ways. One simple, straightforward approach is to divide the total memory capacity by the number of data bits per memory word (say, 64) and let the resulting storage capacity define the basic memory module. If each bit of a memory word is assigned to a different module, then only one sense amplifier per module is required. The resulting bit-per-module system is simple and has a reasonable number of interconnections per chip, module, and page (see column A of the table).

The main problem with the bit-per-module approach is that all the bubbles must be circulated all the time, resulting in a large power dissipation. The power can be reduced by circulating only a portion of the bubbles at a time. It is convenient to assemble a module from 16 chips of 10^5 bits each. So if the memory bits were assigned on a bit-per-chip rather than a bit-per-module basis, only four modules at a time would need a rotating field supplied to them to provide access to the 64 data

(continued overleaf)

bits of 10^5 words. This approach requires 32 checkbits per word, versus 8 for the bit-per-module approach, but the power is still reduced to less than one-half the original. However, since each module now requires 16 write connections and 16 sense connections, the interconnections per module and page increase drastically (see column B of the table).

This problem can be overcome by realizing that the control currents as well as the sense signal are on for less than one quarter of the rotating field cycle. Hence, the chips can be arranged in groups of four (tetrads) at 90° to each other (see figure). The chips themselves are identical, so this space quadrature results in a time quadrature on the chips, i.e., when the first chip senses the field at 0°, the second senses it at 90°, the third senses it at 180°, and the fourth senses it at 270°. Thus at any given time only one of the four chips has a bubble opposite its sensor. This allows four-way multiplexing on the sense and control lines, which results in a significant reduction in the number of interconnections per module and page (see column C of the table) while preserving the feature of low operating power. The tetrad connection may be accomplished using no crossovers on the module, and the number of preamplifiers is reduced fourfold.

MEMORY INTERCONNECTION COUNTS

CONNECTIONS	BIT-PER-MODULE (A)	BIT-PER-CHIP, NON-TETRAD (B)	BIT-PER-CHIP, TETRAD (C)
Per Chip	28	20	20
Per Module	56	110	50
Per Page	68	411	123

Note:

Requests for further information may be directed to:

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Reference: B73-10202

Patent status:

Title to this invention has been waived under the provisions of the National Aeronautics and Space Act [42 U.S.C. 2457 (f)], to the IBM Corp., Huntsville, Alabama 35805.

Source: G. S. Almasi of
IBM Corp.
under contract to
Marshall Space Flight Center
(MFS-22296)