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Marshall Space Flight Center

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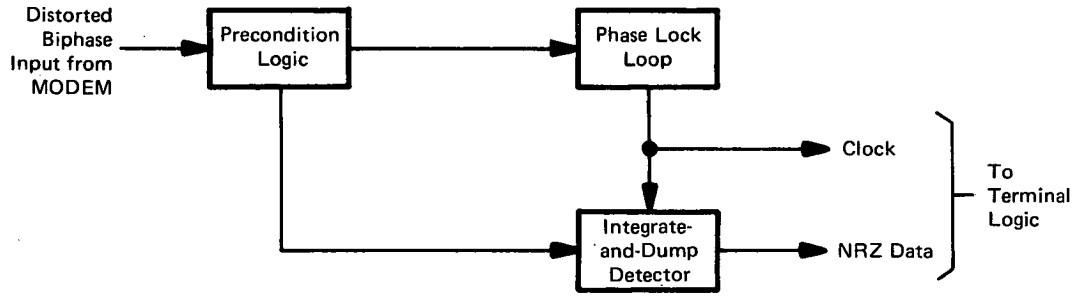
Synchronous Ten-Megabit Biphase Detector



Signal Conditioning Data Flow

The problem:

In the Space Station data-management system, ten megabit biphase data is frequency-division multiplexed (FDM) over a coaxial cable data bus. A model of the system is now under concept verification testing. The FDM process requires MODEMS (modulator/demodulators) that employ filters for channel selection. Distortion is caused by these filters as well as by couplers and imperfect cable and circuitry. The distorted data makes it impossible to generate a jitter-free clock directly from the data and correctly decode the biphase signal.

The solution:

A synchronous phase-lock-loop detector was designed to accept the distorted input and to generate a jitter-free clock. The data-detection circuitry takes advantage of this clock and employs an integrate-and-dump decision circuit to provide near-theoretically ideal data decoding.

How it's done:

The 10-MHz biphase data is accepted by the synchronous detector and is preconditioned by differentiation and rectification logic (see figure).

This logic generates a short pulse for each data transition and consequently produces a frequency spectrum to the phase-lock-loop that contains continuous-frequency components. The phase-lock-loop synchronizes to the 20-MHz component and accordingly locks to the phase of the incoming data. The phase-lock-loop provides filtering and does not follow the instantaneous transition variations of the distorted data. The 20-MHz output is "divided by two" to produce the required 10-MHz jitter-free clock output. Advantage is taken of the nearly ideal phase-lock-loop clock to implement an integrate-and-dump data detector.

Notes:

Requests for further information may be directed to:

Technology Utilization Officer
Marshall Space Flight Center
Code A&PS-TU
Marshall Space Flight Center, Alabama 35812
Reference: B73-10323

Patent status:

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Patent Counsel
Marshall Space Flight Center
Code A&PS-PAT
Marshall Space Flight Center, Alabama 35812

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