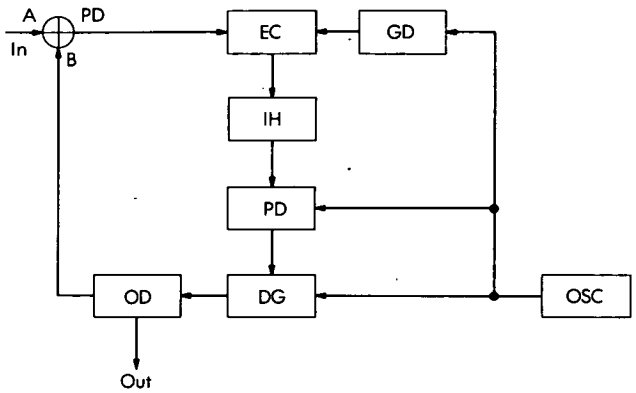
NASA TECH BRIEF

NASA Pasadena Office

All-Digital Phase-Lock Loops for Noise-Free Signals

Three newly designed bit-synchronizers for noiseless waveforms utilize all-digital phase-lock loops that are referenced to a high frequency digital clock (crystal oscillator). The loops include the usual phase



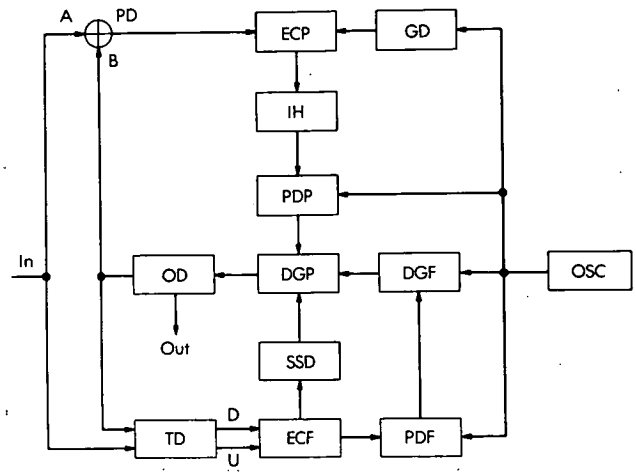
detector, filter or error signal processor, and frequency- or phase-correction mechanisms. The principle of the frequency-correction mechanism involves deletion of every nth pulse in the pulse train from the oscillator to an output divider for obtaining steady state indications and $(n-m)$ and $(n+m)$ corrections in either direction.

The phase-lock loop of the first design acquires the frequency within a nominal range and tracks the phase; it operates on symmetrical waveforms and is intended for uses such as truly digital frequency doubling, tripling, etc. Referring to the first diagram, the phase detector, PD, is a modulo-2 gate between the input (A) and the local waveform (B); the steady-state difference between the input and local waveform is 90°. The output from the phase detector is thus a pulse-duration-modulated error signal which acts as the enable control for error counter EC to count pulses from the fixed oscillator OSC. At the end of the sampling period, the result of the phase comparison in the error counter is transferred to an intermediate hold register, IH, where it is held over the next sampling period. The hold register controls a programmable divider, PD; at the PD output is deleted a pulse in the pulse train from the fixed oscillator through a delete gate, DG. The oscillator provides the clock for the programmable divider, the error counter, the error counter clock divider, GD, and the output divider, OD. The error counter clock divider provides loop gain control; the output divider controls the phase detector by controlling the transfer from the error counter to its hold register. When the loop is in lock, a bit time of the local waveform is symmetrical across a transition of the input signal. To reconstruct the actual phase, a flip-flop in the output divider is triggered by the complement term of a previous flip-flop.

The second design is similar to the first, except that it is modified for random binary data by the addition of a simple transition detector (TD), which consists of a shift register with two flip-flops and a modulo-2 gate between the outputs of the flip-flops. The loop is intended for use as an all-purpose digital bit synchronizer and will acquire the frequency and phase of the basic input signal over a nominal range.

The third design (second diagram) is similar to the first in that it operates on symmetrical signals only; however, because of additional elements, it acquires the frequency over a wide dynamic range. When the local waveform is grossly off frequency, the programmable divider, PDF, and delete gate, DGF, are the

(continued overleaf)



frequency-controlling elements, and programmable divider, PDP, and delete gate, DGP, are inhibited so as not to interfere while the frequency is being acquired. With a frequency discrepancy, the error counter, ECF, will count in one direction and change the local frequency via PDF and DGF so as to compensate for the discrepancy. When the local frequency equals the input frequency, ECF will not count in any direction; only its first bit will toggle. A steady-state detector, SSD, is connected to DGP; as long as ECF counts in either direction, the output of SSD will inhibit the effect of PDP and DGP, that is, as long as frequency acquisition is in progress, the phase-acquisition mechanism is inoperative. The steady-state detector is implemented through a copy flip-flop; the input to this flip-flop is the carry-out from the first bit of the ECF, and its clock is the OR-ed up and down input pulses (U and D).

Note:

Requests for further information may be directed to:

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NASA has decided not to apply for a patent.

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