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NASA TECH BRIEF

NASA Headquarters

Input-Output, Expandable-Parity Network

The problem:

Conventional expandable-parity circuits that generate bit sequences, with lengths that vary in eight-bit increments (e.g., 8, 16, 24, etc.), do not include a built-in parity check.

The solution:

A large-scale integrated (LSI) circuit generates and checks the parity of four eight-bit registers. In addition, the circuit will indicate by an output signal whether a parity error exists. The circuit can also generate or check

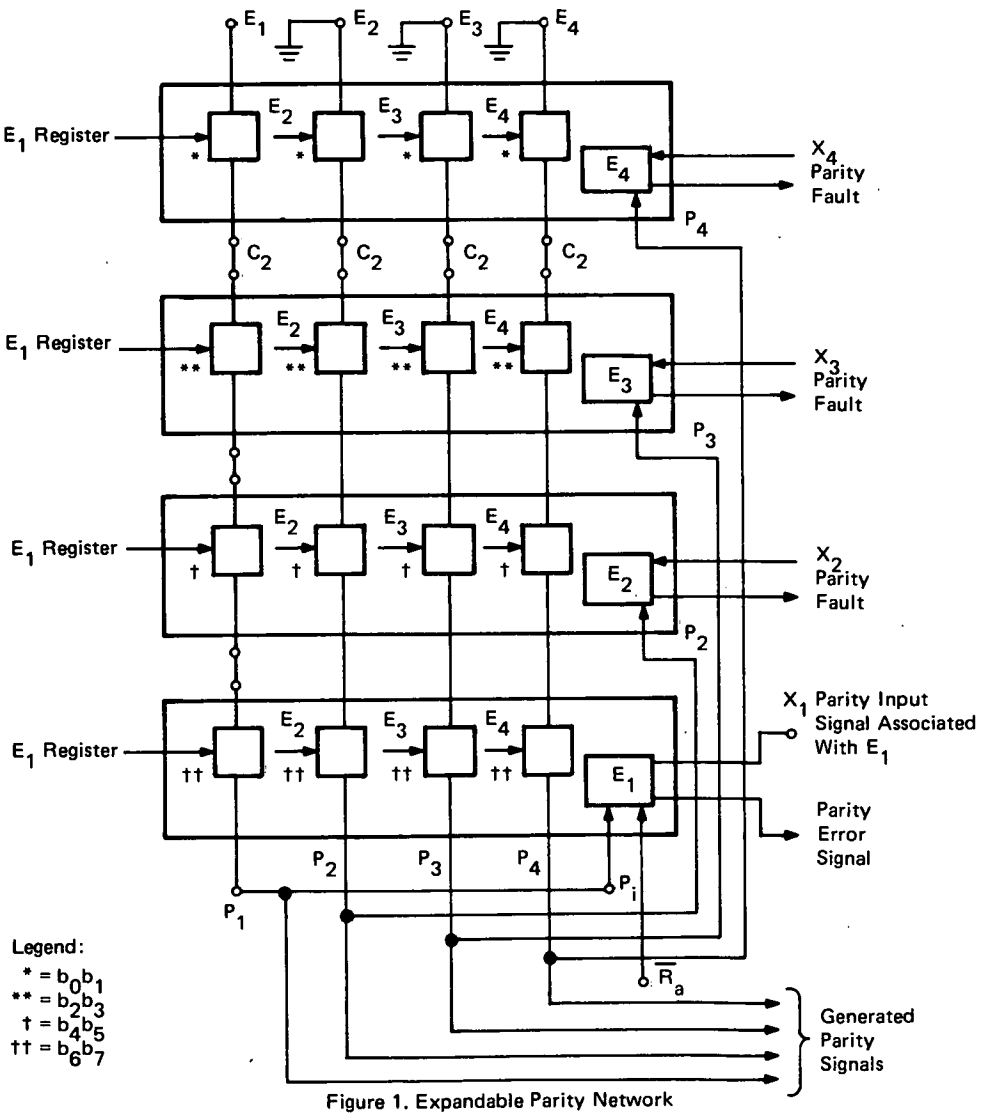

Figure 1. Expandable Parity Network

(continued overleaf)

the parity of words up to 32 bits. This is done by making the appropriate internal wiring connections on the LSI chip.

How it's done:

As shown in Figure 1, the parity-check circuit includes 16 identical circuits. Four of these circuits are associated with a specific eight-bit storage register. They are cascaded to allow the input of each subsequent stage to receive the output from the preceding stage. As shown in Figure 2, each of the logic groups receives, as its input, a unique two of the eight bits (b_0 through b_7) of all four storage registers (E_1 through E_4). Odd parity is defined as the state in which one or all of three bits (two of the data bits plus a carry bit) are true (logical "1"). A carry output signal (C_2, C_3, and C_4) is produced and coupled to the next stage. In essence, the circuit as shown in Figure 2 adds the two data bits and the carry-in bit (the carryout of the previous stage). The result is a carryout signal. After this process ripples down through the four logic states, the final carryout signal determines if the eight-bit register has an even or odd number of logical "1" bits.

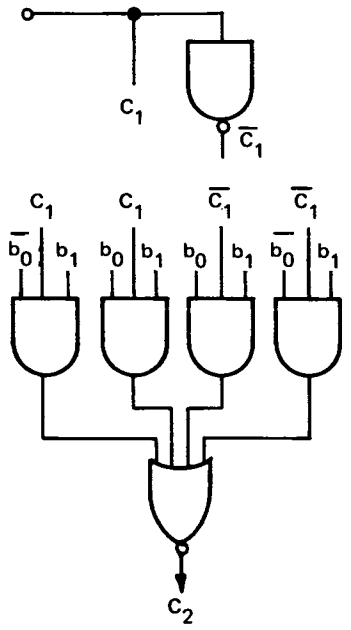

Figure 2. Parity-Check Comparison Circuit

If this final signal is a logical "0", the register contains an even number of "1" bits. If the signal is a "1", an odd number of "1" bits exists in the register. This signal is compared to known reference bits to check the parity of each of the four registers.

If the data are more than eight bits, the sequence is similar. For 16 bits, input/output stages are used to perform a parity check on the total bits. As shown in Figure 1, P_1 (carryout) of the first stage is connected to E_2 of the second stage. The E_2 point that is shown as grounded is lifted to allow this connection. The output P_2 is then used as a final carryout signal. This scheme may be extended to longer word lengths of 24 and 32 bits by making the appropriate internal wiring connections.

Note:

Requests for further information may be directed to:

Technology Utilization Officer
NASA Headquarters
Code KT
Washington, D. C. 20546
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Patent status:

NASA has decided not to apply for a patent.

Source: J. F. McKevitt III of
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