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NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Technical Memorandum 33-567

A Survey of and an Introduction to Fault Diagnosis Algorithms

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JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
PASADENA, CALIFORNIA

October 1, 1972

45

TECHNICAL REPORT STANDARD TITLE PAGE

1. Report No. 33-567	2. Government Accession No.	3. Recipient's Catalog No.
4. Title and Subtitle A SURVEY OF AND AN INTRODUCTION TO FAULT DIAGNOSIS ALGORITHMS		5. Report Date October 1, 1972 6. Performing Organization Code
7. Author(s) F. P. Mathur		8. Performing Organization Report No.
9. Performing Organization Name and Address JET PROPULSION LABORATORY California Institute of Technology 4800 Oak Grove Drive Pasadena, California 91103		10. Work Unit No. 11. Contract or Grant No. NAS 7-100 13. Type of Report and Period Covered Technical Memorandum
12. Sponsoring Agency Name and Address NATIONAL AERONAUTICS AND SPACE ADMINISTRATION Washington, D.C. 20546		14. Sponsoring Agency Code

15. Supplementary Notes

16. Abstract

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17. Key Words (Selected by Author(s))	18. Distribution Statement
Computer Applications and Equipment Electronic Components and Circuits	Unclassified -- Unlimited

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price
Unclassified	Unclassified	38	

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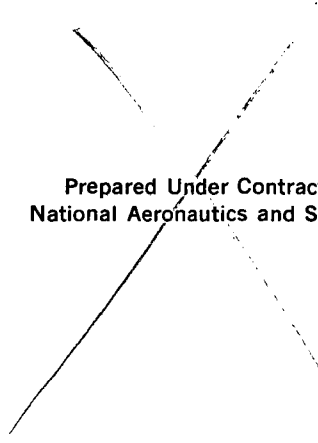


Prepared Under Contract No. NAS 7-100
National Aeronautics and Space Administration

PREFACE

The work described in this report was performed by the Astrionics Division of the Jet Propulsion Laboratory.

CONTENTS

FIGURES (contd)

ABSTRACT

This report surveys the field of fault diagnosis and introduces the reader to some of the key algorithms and heuristics currently in use. Fault diagnosis is an important and a rapidly growing discipline. This is important to the Jet Propulsion Laboratory's research efforts in the design of self-repairable computers because the present diagnosis resolution of its fault-tolerant computer is limited to a functional unit or processor. Better resolution is necessary before failed units can become partially reuseable. The approach that holds the greatest promise is that of resident microdiagnostics; however, that presupposes a microprogrammable architecture for the computer being self-diagnosed. The presentation here is tutorial and contains examples. An extensive bibliography of some 220 entries is included.

I. INTRODUCTION

The general field of system testing is an all-encompassing discipline ranging from fabrication processes, parts testing, and production techniques to the final system checkout. This report deals with the area of fault diagnosis as applied to digital computers and systems.

The term fault diagnosis includes both fault detection and fault location, where fault detection is the process of determining whether or not the system is fault-free, whereas fault location is the process of localizing the fault to specific components, sets of components, modules, or subsystems, depending on the diagnostic resolution desired.

Early methods of fault diagnosis in digital computers consisted of diagnostic programs designed to periodically check the major functions of the computer. Often this meant, at best, the testing of the instruction set of the machine using representative sets of data and known corresponding results.

The most commonly used fault model to represent system failures is the "line stuck at 1, line stuck at 0" model. This model assumes that failures are such that any line may become permanently stuck at logical 1 or logical 0 level. This is denoted by s-a-1 or s-a-0, respectively. This model thus includes "lines open" type of failures and also the "shorted lines" type of failures that are such as not to induce feedback as a result of the short.

In general, the problem of fault diagnosis may be succinctly stated thus: By applying signals to the inputs and observing the responses at the outputs, it is determined whether or not the network is operating properly; if not, it must be determined what changes from the norm have occurred.

Exhaustive methods very quickly become unmanageable. If a network consists of n edges, where each edge may be either fault-free, s-a-0, or s-a-1, then the total number of possible "stuck-at" faults amounts to $3^n - 1$ or 3^n faults, including the null fault. If only single faults are considered, then the total number of faults including the null fault is $2n + 1$. As an illustration, a NAND gate realization of an EXCLUSIVE-OR circuit consists of 9 edges; thus, the total number of possible faults that may arise are $3^9 = 19,663$. However, if the single fault assumption is made, the number of faults reduces to $2 \times 3 + 1 = 7$.

In order to make the problem of fault diagnosis more manageable, various simplifying assumptions are made, and algorithms are developed which are applicable to specific classes of digital networks or are more efficient under specific constraints than under others. Typical subclassifications of digital networks indicate whether the network is combinatorial or sequential, and in the latter case whether it is synchronous or asynchronous; whether the network has single or multiple outputs; whether single or multiple faults are considered; whether there is fan-out or no fan-out, and if there is fan-out, whether it is reconvergent or non-reconvergent; whether or not the network is redundant; and, finally, whether the particular technique developed is heuristic or algorithmic.

This report describes Gedanken experiments of faulty machine identification, diagnosing and homing experiments, Armstrong's equivalent normal form test generation method, the Boolean Difference techniques, Roth's D-Algorithms, and the newly evolving branch of microdiagnostics. Finally, an extensive bibliography of fault diagnosis has been compiled.

II. GEDANKEN EXPERIMENTS — SEQUENTIAL MACHINES

The material presented here is based on the work of E. F. Moore entitled "Gedanken — Experiments on Sequential Machines" and also that of A. Gill. In Gedanken experiments the finite-state sequential machine is considered to be a "black box" with inputs to which stimuli can be applied and outputs on which the responses may be observed. Only in this way can the behavior, characterization, and contents of the black box be determined.

III. MACHINE AND FAULT IDENTIFICATION EXPERIMENTS

In the problem of identifying the fault of a machine, the faulty version of the machine is simply regarded as another machine. Thus, the set of all possible failed machines under the class of known faults and the fault-free machine constitutes a class of machines. The experiment is to identify the particular unknown failed machine from this set of machines. A subproblem to the machine identification problem is that of state identification. In the latter case the complete state transition table of the finite-state sequential machine is known, and the problem is to determine its initial state, or, in the case of the homing experiment, to be able to drive it into a known state. In solving problems of fault identification both the machine identification and the state identification techniques are used.

The procedure is as follows. From the known machine M which may malfunction in a set of known ways, the possible faulty machines M_1, M_2, $\cdots$ are characterized by, e.g., specifying their transition tables. These faulty machines are then reduced to their minimal form and constitute an exclusive class of machines $\{M_1, M_2, \cdots, M_n\}$ such that no state in M_i is equivalent to any state in M_j $(j \neq i)$. The disjunction machine ΔM of M_1, M_2, $\cdots$, M_n is then formed. The fault identification problem in the original machine M is now reduced to that of identifying the final state, i.e., conducting a homing experiment on the machine ΔM.

IV. DIAGNOSING AND HOMING EXPERIMENTS

Figure 1 illustrates the theory underlying diagnosing and the allied problem of homing. The pertinent terms are ordered from the simple and obvious to the more complex and unobvious and are defined as follows:

Experiment. The process of applying input sequences to the input terminals of a machine, observing the resulting output sequences, and drawing conclusions based on these observations.

Preset Experiment. An experiment in which the applied input sequence is completely determined in advance.

Adaptive Experiment. An experiment in which the applied input sequence is composed of two or more subsequences, each subsequence (except the first) being determined on the basis of the previous response.

Copy. A machine is a copy of another machine if both have identical transition tables, and if both are at the same state before experiments commence.

Simple Experiments. Experiments in which only one copy of the machine is required.

Multiple Experiments. Experiments in which more than one copy of the machine is required.

Length of an Experiment. The total number of input symbols applied in the course of the experiment.

Order of an Experiment. The number of input sequences of which the experiment is composed.

Multiplicity of an Experiment. The number of copies required of the machine under investigation. (Note: a simple experiment is an experiment of multiplicity = 1; a multiple experiment is an experiment of multiplicity ≥ 2).

Diagnosing Problem. Machine M in one of the states $\{s_1, \cdots, s_m\}$, transition table known, to find this state.

Homing Problem. Machine M in one of the states $\{s_1, \cdots, s_m\}$, transition table known, to pass M into a known state.

Diagnosing Experiment. An experiment that solves the diagnosing problem.

Homing Experiment. An experiment that solves the homing problem. (Note: every diagnosing experiment is also a homing experiment; the converse is not true.)

Admissible Set A(M). Of machine M, the set of states $\{s_1, \cdots, s_m\}$ one of which is the initial state of M.

Admissible States. The states in the admissible set A(M).

m-Wise Diagnosing Problem. The problem of identifying the initial state of M where A(M) is arbitrarily m.

Pair-Wise Diagnosing Problem. The problem of identifying the initial state of M where m = 2.

Diagnosing Sequence. For $\{s_{i0}, s_{j0}\}$ is an input sequence of length n - 1 or less which, when applied to M in s_{i0} and M in s_{j0}, yields distinct output sequences.

Minimal Diagnosing Sequence. $E(s_{i0}, s_{j0})$ for the pair $\{s_{i0}, s_{j0}\}$ in a diagnosing sequence of length ℓ where s_{i0} are ℓ distinguishable and $(\ell - 1)$ equivalent $(1 \leq \ell \leq n - 1)$.

An Example

To find the minimal diagnosing sequence E(1, 2) for the pair of states $\{1, 2\}$ of the machine M whose state diagram is as shown in Fig. 2. First construct the P_k tables. P_k is the partition of S according to the k-equivalence of states in S. By observation of Fig. 2, the state transition table shown in Fig. 3a is derived. We apply the following algorithm:

Algorithm

To determine minimal diagnosing sequences for state pairs.

(1) Construct P_k tables.

Find ℓ such that s_{i0}, s_{j0} are adjoint rows in $P_{\ell-1}$ and disjoint in P_ℓ. Let k = 1.

(2) If $(\ell - k) > 0$ go to step 3.

If $(\ell - k) = 0$ E_k is given the heading of any column in the Z_v subtable of M such that rows s_{ik-1}, s_{jk-1} are distinct. $E_{u1}, E_{u2}, \cdots, E_{uk}$ is the minimal diagnosing sequence for $\{s_{i0}, s_{j0}\}$.

(3) E_{uk} is the heading of any column in $P_{\ell-k}$ such that rows s_{ik-1}, s_{jk-1} in this column have differently subscripted entries. These entries are s_{ik}, s_{jk}.

Increment k by 1 and return to step 2.

Now, having already constructed the P_k tables, we start from the P_3 that is the last table in which rows 1 and 2 are adjoint. Rows 1 and 2 in the P_3 table have distinct subscripts in entries 4c and 5d which appear in column β. β, then, is the first symbol in E(1, 2). In the P_2 table, rows 4 and 5 have

distinct subscripts in entries 3b and 2a which appear in column α. α, then, is the second symbol in E(1, 2). In the P_1 table, rows 3 and 2 have distinct subscripts in entries 5b and 1a, which appear in column α. α, then, is the third symbol in E(1, 2). Alternatively, β could have been chosen as the third symbol, since rows 3 and 2 have distinct subscripts in entries 1a and 5b, which appear in column β. In the Z_v subtable, rows 1 and 5 have distinct entries (0 and 1) in column α. α, then, is the fourth and last symbol in E(1, 2). Thus, (1, 2) is either $\beta\alpha\alpha\alpha$ or $\beta\alpha\beta\alpha$. From the P_0 table or Fig. 2 it can be readily verified that when $\beta\alpha\alpha\alpha$ is applied to M at state 1 and state 2 the last output symbol is 1 and 0, respectively. Consequently, if $\{1, 2\}$ is the admissible set of M, the distinguishing experiment may be conducted by applying $\beta\alpha\alpha\alpha$ and observing the last output symbol. If this symbol is 1, the initial state is 1; if this symbol is 0, the initial state is 2.

The minimal diagnosing sequences for all pairs of states $\{s_{i0}, s_{j0}\}$ in M are listed in Table 1. The last two columns in this table indicate the last output symbols Z_i and Z_j observed when the minimal diagnosing sequence is applied to s_{i0} and s_{j0}, respectively.

V. EQUIVALENT NORMAL FORM (ENF)

The ENF method is that of Armstrong (1966). The equivalent normal form is an equivalent two-level circuit representation that corresponds to a multi-level circuit. It is a test generation method well suited to the selection of efficient (near minimal) test sets. It is easily programmable on a computer; however, it becomes unmanageable for large circuits. The ENF method has not been proved to be algorithmic; however, a counter example has not been discovered.

A. ENF Method

To construct ENF of a combinational circuit with single output:

(1) Write the Boolean expression for the circuit. Corresponding to each gate G_j of the circuit, there shall be a pair of parentheses in the expression, the parentheses being labeled with the subscript j. The subexpression corresponding to G_j shall be en-

closed in parentheses. All literals in the Boolean expression will denote input variables.

(2) Expand to sum-of-products normal form. When a pair of parentheses is removed, its associated label is attached to each literal inside the parentheses as a subscript. No redundant terms are removed.

An example is shown in Fig. 4, where

$$
\begin{aligned}
f &= \left[\left((A \cdot B)_1 + (B \cdot C)_2\right)_3 \cdot D\right]'_4 \\
&= \left[(A_1 \cdot B_1 + B_2 \cdot C_2)_3 \cdot D\right]'_4 \\
&= \left((A_{13} \cdot B_{13} + B_{23} \cdot C_{23}) \cdot D\right)'_4 \\
&= (A_{13} \cdot B_{13} + B_{23} \cdot C_{23})'_4 + D'_4 \\
&= (A_{13} \cdot B_{13})'_4 \cdot (B_{23} \cdot C_{23})'_4 + D'_4 \\
&= (A_{134} + B'_{134}) \cdot (B'_{234} + C'_{234}) + D'_4 \\
&= A'_{134} \cdot B'_{234} + A'_{134} \cdot C'_{234} + B'_{134} \cdot B'_{234} + B'_{134} \cdot C'_{234} + D'_4 \\
&= A'_{\alpha} \cdot B'_{\beta} + A'_{\alpha} \cdot C'_{\beta} + B'_{\alpha} \cdot B'_{\beta} + B'_{\alpha} \cdot C'_{\beta} + D'_{\gamma}
\end{aligned}
$$

which is the ENF sum-of-products form where α, β, and γ are path from inputs to the circuit output. The ENF form is realized by the two-level AND-OR circuit shown in Fig. 5.

B. ENF Theorem

A test for a literal appearance in the ENF sensitizes the corresponding path in the circuit. Thus, if a set of literal appearances can be selected whose corresponding paths together contain every vertex of the circuit, and if a set of tests can be found which tests at least one appearance of each literal for the S-a-1 and S-a-0 faults, then the set of tests detects every fault of the circuit.

For example, in the above the test for a S-a-1 fault for the literal A'_{α} is $A' = 0$, $B' = 0$, $C' = 1$ and $D' = 0$. From the theorem this input vector (0,0,1,0) sensitizes the path α; i.e., G1G3G4 beginning at A.

VI. BOOLEAN DIFFERENCE ALGORITHMS

The Boolean difference method first applied to fault-diagnosis by Sellers et al. (1967) has been described by Akers (1959) and also by Amar and Condulmari (1967). Unlike the tabular or exhaustive search methods described earlier, Boolean difference approach is an elegant systematic equation-solving procedure. Algorithms have been implemented which can handle combinational networks with up to fifty primary input and output variables. Boolean difference techniques have also been extended to generate test patterns for asynchronous sequential circuits.

A. Basic Concept

If $f(x_1, \cdots, x_n)$ is a switching function of the n variables $x_1, \cdots, x_n$ then the Boolean difference is defined as:

$$df(x_1, \cdots, x_n)/dx_i = df(X)/dx_i$$

$$\triangleq f(x_1, \cdots, x_i, \cdots, x_n) \oplus f(x_1, \cdots, \overline{x}_i, \cdots, x_n)$$

which is also equivalent to

$$f(x_1, \cdots, 1, \cdots, x_n) \oplus f(x_1, \cdots, 0, \cdots, x_n)$$

This implies that Boolean difference $df(X)/dx_i$ is a function of (n - 1) variables $x_1, \cdots, x_{i-1}, x_{i+1}, \cdots, x_n$.

From the definition of EXCLUSIVE-OR function it follows that when $df(X)/dx_i = 1$

$$f(x_1, \cdots, 1, \cdots, x_n) \neq f(x_1, \cdots, 0, \cdots, x_n)$$

and when $df(X)/dx_i = 0$

$$f(x_1, \cdots, 1, \cdots, x_n) = f(x_1, \cdots, 0, \cdots, x_n)$$

Thus $df(X)/dx_i = 1$ is a condition for f(X) being dependent on the value of x_i. Which implies that a change at x_i always causes a change at f(X)

when $df(X)/dx_i = 1$, and x_i does not cause a change at f(X) when $df(X)/dx_i = 0$. Hence $df(X)/dx_i = 1$ is a sufficient condition for the path from x_i to F to be sensitized.

In general, $df(X)/dx_i$ is neither 1 nor 0 but some Boolean function not containing x_i; hence, input test patterns may be selected in order to satisfy the condition $df(X)/dx_i = 1$. Now, since $df(X)/dx_i$ is independent of x_i in general, two, i.e., a pair of test patterns, can be selected corresponding to in one case $x_i = 1$ and in the other $x_i = 0$.

The Boolean difference approach may be used to detect inversion-type faults ($1 \rightarrow 0$, $0 \rightarrow 1$) in addition to the conventional "stuck-at" faults.

An example of Boolean difference is shown in Fig. 6. We seek to find the conditions under which an error in x_1 causes an error at the output.

Solution

$$df(X)/dx_1 = d(x_1x_2 + x_3 + x_4)/dx_1$$

using the property

$$d(A + B)/dx_i = \overline{A}\, dB/dx_i \oplus B\, dA/dx_i \oplus dA/dx_i \cdot dB/dx_i$$

$$df(X)/dx_1 = (\overline{x_3 + x_4})\, d(x_1x_2)/dx_1$$

Now, using the property

$$d(A \cdot B)/dx_i = A\, dB/dx_i \oplus B\, dA/dx_i \oplus dA/dx_i \cdot dB/dx_i$$

$$df(X)/dx_1 = (\overline{x_3 + x_4}) \cdot x_2\, dx_1/dx_1$$

which, from the property ($dA/dx_i = 1$ if A depends only on x_i)

$$df(X)/dx_1 = (\overline{x_3 + x_4}) \cdot x_2$$

$$= \overline{x}_3 \cdot \overline{x}_4 \cdot x_2$$

$\overline{x}_3 \cdot \overline{x}_4 \cdot x_2 = 1$ when $x_2 = 1$, $x_3 = 0$ and $x_4 = 0$.

This is the condition when an error in x_1 causes an erroneous output.

The input test patterns for detecting failure at x_1 are (x_1, x_2, x_3, x_4) = (0,1,0,0) and (1,1,0,0).

B. Comments on the Boolean Difference

The astute reader will have observed that the Boolean difference concerns itself with only input variables, and the reader may well ask how does one generate test patterns for "internal" failures? The solution is to break the circuit at that point and consider it as an extra input to the circuit. Having obtained test patterns for this extra input one works backward to specify the test patterns, using only the original circuit inputs. Also, it is possible to form a two-level equivalent circuit of any multi-level circuit (see Subsection V, Equivalent Normal Form). Also, partial Boolean difference, Boolean difference chains, and Boolean difference of multiple variables have been defined. Application of Boolean difference to sequential circuit uses a similar approach to that of the D-algorithm of first modeling the circuit using the Moore model and cutting the feedback lines to reduce the model to an equivalent combinational circuit during delta time intervals. A summary of some basic properties of Boolean difference is found in Table 2.

References on the Boolean difference are found in Bibliography entries 2, 3, 10, 11, 44, 65, 91, 92, 93, 94, 134, 135, 152, 190, 191, and 192.

VII. D-ALGORITHM

The D-algorithm is the first method for generating tests for nonredundant combinational circuits that has been proved to be algorithmic; i.e., if a test exists for detecting a failure, then by the application of the D-algorithm one can find this test. The D-algorithm was formulated by J. P. Roth (see Bibliography entries 169, 170, 178, 180) and is precisely and elegantly expressed in terms of the calculus of cubical complexes. The D-algorithm is a systematic application and extension on the basic concept of path sensitization and is a logical culmination of Eldred's pioneering work. Besides algorithms for generating tests for specific faults Roth's program TESTDETECT solves the related problem of enumerating the set of all faults

that a particular test can detect. Finally the D-algorithm has been extended to apply to asynchronous sequential logic by transforming the problem of finding a single failure in the sequential circuit to that of finding multiple failures in an iterative combinational circuit constructed from the sequential model by the cutting of all its feedback lines. The D-algorithms DALG and DALG II, as well as their extensions: the sequential circuit heuristics, known as iterative test generator (ITG) and macroblock test generator (MTG) have been programmed in the APL language.

It should be noted that since the D-algorithm guarantees obtaining tests for non-redundant combinational networks then by implication the D-algorithm may also be used to detect redundancy of design in combinational circuits for which complete tests are not generatable.

A. D-Algorithm Definitions

Singular cover is a rearranged compact form representation of a truth-table (an x is used to denote that the corresponding variable may be a 1 or 0).

Singular cube rows of singular covers are termed singular cubes.

D-cubes represent the input-output behavior of the failing as well as the good circuit.

Primitive D-cubes of a logic block (element) is a subset of D-cubes defined as those D-cubes having a D or $\overline{D}$ on the output coordinate.

Primitive D-cube of failure is the particular primitive D-cube of a failing block. These are determined by both the logic function and the assumed failure of the block.

D-drive is the operation of constructing a D-path or set of D-paths (sensitized path) from the failed block to a primary output.

D-frontier consists of all the blocks in the circuit having D's or $\overline{D}$'s on some of their inputs and X's on their outputs.

Consistency operation is the justification of all 0, 1 values imposed during D-drive in terms of primary-input values.

D-signals are 5-valued logic $(0, 1, X, D, \overline{D})$ used to describe the behavior of a circuit with failures. The symbol D ($\overline{D}$) denotes a logical value which is 1 (0) in the good circuit and 0 (1) in the circuit with failure.

B. Algorithm to Form Primitive D-cubes From Singular Covers

Step 1. Intersect cubes (rows) of the singular cover, these cubes must have different output values.

Step 2. The intersection rules of the input values are:

$1 \cap 0 = \overline{D}$

$0 \cap 1 = D$

$X \cap X = X$

$0 \cap 0 = 0 \qquad X = X \cap 0 = 0$

$1 \cap 1 = 1 \qquad X = X \cap 1 = 1$

C. Algorithm to Form Primitive D-cubes of Failure

Step 1. Use cubes of the singular cover.

Step 2. Intersect pairs of cubes.

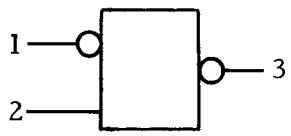
Step 3. Use same intersection rules as the algorithm to form primitive D-cubes.

Step 4. Select one cube of each pair from the singular cover, the other member is the corresponding cube from the singular cover of the failed gate.

Step 5. Assign bars by the following convention: A vertex of the intersection have value $\overline{D}$ if the vertex has value 0 in the cube of the failure-free block, and value 1 in the cube of the failed block. All other cases are assigned values D.

Example

Given the truth table for the INHIBIT-NOT logical block:



1	2	3
0	0	1
0	1	0
1	0	1
1	1	1

(1) To determine its singular cover:

Singular cover 1	2	3
0	1	0
X	0	1
1	X	1

(2) To determine the primitive D-cubes:

Primitive D-cube 1	2	3	its dual	1	2	3
D	1	D		$\overline{D}$	1	$\overline{D}$
0	D	$\overline{D}$		0	$\overline{D}$	D
D	$\overline{D}$	D		$\overline{D}$	D	$\overline{D}$

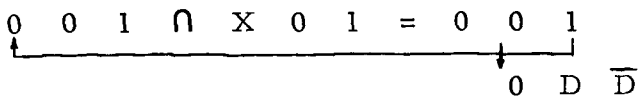
This is determined from the 0-cube 0 1 0 in the singular cover, which is used as the generator. Generators have the property that a change in a single input must force a change in the output. A change in either input or block inputs causes a change in the output.

A change in input 1:

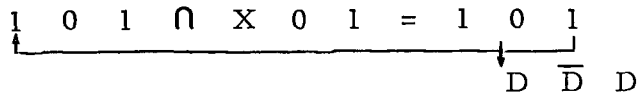
$$1\ 1\ 1 \cap 1\ X\ 1 = 1\ 1\ 1$$

$$D\ 1\ D$$

A change in input 2:



A change in inputs 1 and 2:



D. Circuit-Labeling Convention

(1) Assign an integer label to each vertex of the circuit.

(2) Designate gates (blocks) by the label of the vertex corresponding to its output. Note: each vertex corresponds to either a primary input signal or a gate output signal.

(3) Assign vertex number by using the "leveling rule" which is that the integer associated with a block shall be greater than the integers of all vertices which feed it.

E. D-Algorithm (DALG-II)

Start by applying a primitive D-cube of failure at the failing block (logic element), thus obtaining a D or $\overline{D}$ at its output.

(The goal is to construct a D-path (sensitized path) or set of D-paths, from the failed block to a primary output, an operation called D-drive.)

Initially the D-frontier (defined to consist of all the blocks in the circuit having D's or $\overline{D}$'s on some of their inputs and X's on their outputs) consist of the successors of the failed block. The D-frontier is then moved toward the primary outputs by applying suitable primitive D-cubes to the blocks in the D-frontier thus advancing the D-frontier itself, until a D or $\overline{D}$ has been imposed on a primary output. At this point, a connected D-path has been established from the failed block to the primary output, and the D-drive is terminated.

Now, all 0,1 values imposed during D-drive have to be justified in terms of the primary-input values. This is accomplished by the consistency operation; i.e., iteratively applying suitable singular cubes to all blocks having output values not justified by their inputs, if this is possible, until all 0,1 signals have been driven back to primary inputs. An example is shown in Fig. 8.

To construct a test for "line 7 s-a-0," first the primitive D-cube of failure 1 1 D is used to impose values 1 1 D on lines 1, 2 and 7. The primitive D-cube D 0 D is then applied, thus driving a D through block 9. As a consequence, a 0 must be imposed on line 3. The D on line 9 is now driven to the primary-output 12 by applying to lines 9, 10 and 12 the primitive D-cube D 0 $\overline{D}$. This completes the D-drive. The consistency operation now amounts to justifying the 0 value on line 10. This is done by imposing a 0 on line 4. The obtained test for "7 s-a-0" is 1100xx.

References on D-algorithms are found in Bibliography entries 18, 19, 20, 39, 43, 65, 67, 154, 161, 169, 170, 171, 173, 174, 175, 176, 177, 178, 180, and 186.

VIII. MICRODIAGNOSTICS

Microprogram routines stored in read-only memories, in contrast to the traditional control unit (CPU) of the classical computer, act as the master control governing at the gate level the data flow of the machine.

The traditional machine language diagnostics consisting of function tests, measurements tests, utility programs, and diagnostic monitors apply at the level of machine instructions and data words. However, microdiagnostics or diagnostic microprograms have a much finer resolution in that the data paths are controlled at the gate level thus enabling the application of diagnostic tests at the circuit level. Another advantage is that the amount of hard core (or unaccessible circuitry) is drastically reduced.

An example of the application of microdiagnostics is the IBM System 360 model 85. Its diagnostic routines are written in a microinstruction language and are executed out of a read-and-write form of control storage.

They claim that 85% of all failures in the model 30 CPU are fault-locatable to four or less SLT cards.

In the author's view, the approach that holds the greatest promise for the diagnosis of closed (inaccessible to human intervention) computer system is that of resident microdiagnostic; however, that presupposes a microprogrammable architecture of the computer being self-diagnosed.

References on microdiagnostics are found in Bibliography entries 8, 31, 79, and 96.

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Table 1. Minimal diagnosing sequences for state pairs in M

s_{i0}	s_{j0}	$E(s_{i0}, s_{j0})$	Z_i	Z_j
1	2	$\beta\alpha\alpha\alpha$	1	0
1	3	$\alpha\alpha$	0	1
1	4	α	0	1
1	5	α	0	1
2	3	$\alpha\alpha$	0	1
2	4	α	0	1
2	5	α	0	1
3	4	α	0	1
3	5	α	0	1
4	5	$\alpha\alpha\alpha$	1	0

Table 2. A summary of some basic properties of Boolean difference

$$df(X)/dx_i \triangleq f(x_1, \cdots, x_i, \cdots, x_n) \oplus f(x_1, \cdots, \overline{x}_i, \cdots, x_n)$$

$$df(X)/dx_i = f(x_1, \cdots, 1, \cdots, x_n) \oplus f(x_1, \cdots, 0, \cdots, x_n)$$

$$df(X)/dx_i = 0 \text{ if } f(X) \text{ is independent of } x_i$$

$$df(X)/dx_i = 1 \text{ if } f(X) \text{ depends only on } x_i$$

$$df(\overline{X})/dx_i = df(X)/dx_i$$

$$df(X)/dx_i = df(X)/d\overline{x}_i$$

$$\frac{d}{dx_i}(df(X)/dx_j) = \frac{d}{dx_j}(df(X)/dx_i)$$

$$d(f(X) \cdot G(X))/dx_i = f(X)\, dG(X)/dx_i \oplus G(X)\, df(X)/dx_i \oplus df(X)/dx_i \cdot dG(X)/dx_i$$

$$d(f(X) + G(X))/dx_i = \overline{f}(X)\, dG(X)/dx_i \oplus G(X)\, df(X)/dx_i \oplus df(X)/dx_i \cdot dG(X)/dx_i$$

$$d(f(X) \oplus G(X))/dx_i = df(X)/dx_i \oplus dG(X)/dx_i$$

$$d(f(X) \cdot G(X))/dx_i = f(X)\, dG(X)/dx_i \text{ if } f(X) \text{ is independent of } x_i$$

$$d(f(X) + G(X))/dx_i = \overline{f(X)}\, dG(X)/dx_i \text{ if } f(X) \text{ is independent of } x_i$$

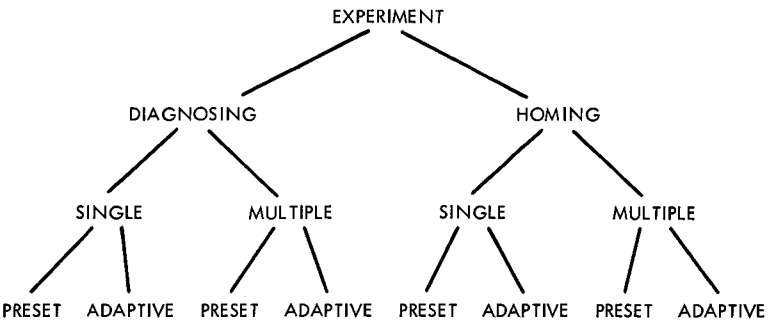


Fig. 1. Classification of identification experiments

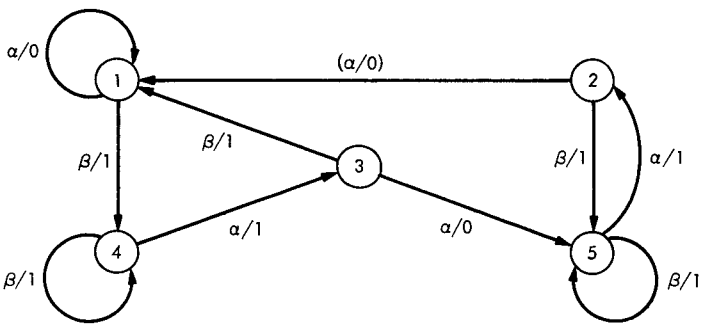


Fig. 2. Machine M transition diagram

(a) P_0

S_v \ X_v	Z_v		S_{v+1}	
	α	β	α	β
1	0	1	1	4
2	0	1	1	5
3	0	1	5	1
4	1	1	3	4
5	1	1	2	5

P_0 TABLE DETERMINED FROM FIGURE 2

(b) P_1

Σ_1	S_v \ S_{v+1}	α	β
a	1	1a	4b
	2	1a	5b
	3	5b	1a
b	4	3a	4b
	5	2a	5b

P_1 TABLE (DETERMINED FROM THE P_0 TABLE). THE RESPONSE SUBTABLE IS NOT SHOWN AGAIN. Σ_1, THE 1-EQUIVALENCE CLASSES ARE FORMED BY ADJOINING THOSE STATES IN THE TRANSITION TABLE HAVING IDENTICAL ROWS IN THE RESPONSE SUBTABLE i.e., STATES ARE ADJOINT IN P_1 IF AND ONLY IF, FOR EVERY INPUT SYMBOL, THEY YIELD IDENTICAL OUTPUT SYMBOLS

(c) P_2

Σ_2	S_v \ X_v	S_{v+1} α	S_{v+1} β
a	1	1a	4c
	2	1a	5c
b	3	5c	1c
c	4	3b	4c
	5	2a	5c

P_2 TABLE (DETERMINED FROM THE P_1 TABLE). Σ_2, THE TWO-EQUIVALENCE CLASSES ARE FORMED BY ADJOINING THOSE ADJOINT STATES IN THE P_1 TABLE THAT HAVE IDENTICAL SUBSCRIPT ROWS. DISJOINT ROWS IN P_1 REMAIN DISJOINT IN P_2

(d) P_3

Σ_3	S_v \ X_v	S_{v+1} α	S_{v+1} β
a	1	1a	4c
	2	1a	4d
b	3	5d	1a
c	4	3b	4c
d	5	2a	5d

(e) P_4

Σ_4	S_v \ X_v	S_{v+1} α	S_{v+1} β
a	1	1a	4d
b	2	1a	5e
c	3	5e	1a
d	4	3c	4d
e	5	2b	5e

P_4 TABLE CANNOT BE REFINED FURTHER, SINCE THE EQUIVALENCE CLASSES HAVE NO ADJOINT ROWS WITH DISTINGUISHABLE SUBSCRIPT ROWS. THE MOST REFINED PARTITION $\hat{P} = P_4$.

Fig. 3. P_k tables

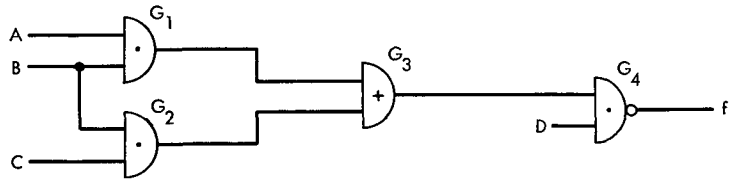


Fig. 4. Example of ENF of a combinational circuit with single output

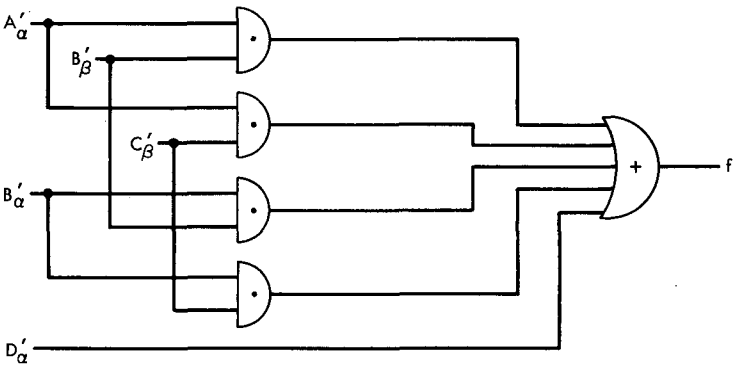


Fig. 5. Two-level AND-OR circuit

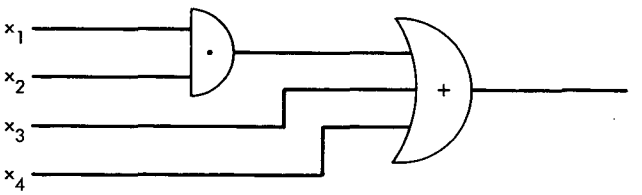


Fig. 6. An example of Boolean difference

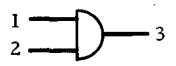
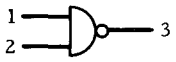
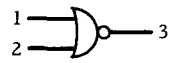
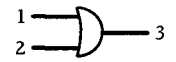
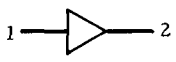
Block	Truth table	Singular cover	Primitive D-cubes
 AND	1 2 3 1 1 1 1 0 0 0 1 0 0 0 0	1 2 3 1 1 1 0 X 0 X 0 0	1 2 3 D 1 D 1 D D
 NAND	1 2 3 1 1 0 1 0 1 0 1 1 0 0 1	1 2 3 1 1 0 0 X 1 X 0 1	1 2 3 $\overline{D}$ 1 D 1 $\overline{D}$ D
 NOR	1 2 3 1 1 0 1 0 0 0 1 0 0 0 1	1 2 3 0 0 1 1 X 0 X 1 0	1 2 3 $\overline{D}$ 0 D 0 $\overline{D}$ D
 OR	1 2 3 1 1 1 1 0 1 0 1 1 0 0 0	1 2 3 0 0 0 1 X 1 X 1 1	1 2 3 D 0 D 0 D D
 NOT	1 2 0 1 1 0	1 2 X $\overline{X}$	

Fig. 7. Singular covers and primitive D-cubes of some common logic blocks

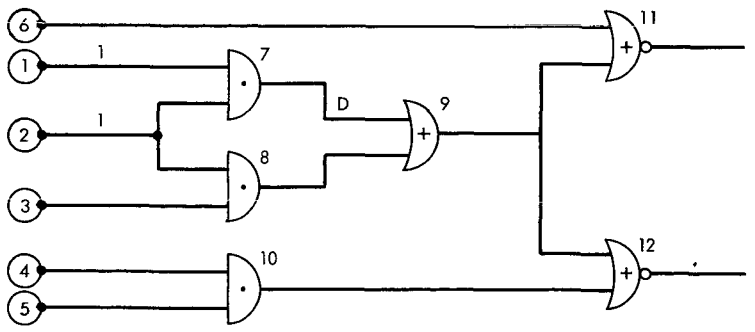


Fig. 8. Example of D-algorithm to construct test for "line 7 s-a-0"

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