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FINAL REPORT

DEVELOPMENT OF FERRITE LOGIC DEVICES FOR AN ARITHMETIC PROCESSOR

by C. H. Heckler, Jr.

Prepared under Contract No. NAS1-10816

by

Ampex Corporation
Redwood City, California

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ABSTRACT

A number of fundamentally ultra-reliable, all-magnetic logic circuits are developed using as a basis a single-element ferrite structure wired as a logic delay element. By making minor additions or changes to the basic wiring pattern of the delay element other logic functions such as OR, AND, NEGATION, MAJORITY, EXCLUSIVE-OR, and FAN-OUT are developed. These logic functions are then used in the design of a full-adder, a set/reset flip-flop, and an edge detector. As a demonstration of the utility of all the developed devices, an 8-bit, all-magnetic, logic arithmetic unit capable of controlled addition, subtraction, and multiplication is designed. A new basic ferrite logic element and associated complementary logic scheme with the potential of improved performance is also described. Finally, an improved batch process for fabricating joint-free power drive and logic interconnect conductors for this basic class of all-magnetic logic is presented.

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1.0 SUMMARY

In earlier work, a class of all-magnetic logic circuits was developed based on the use of a controlled threshold logic scheme and bi-material ferrite structures. One of the outstanding attributes of these logic devices is the absence of a failure mechanism which makes them fundamentally ultra-reliable. Also, these circuits provide increased power gain over that obtainable with other nonresistive magnetic logic schemes.

A basic delay circuit consisting of a multi-aperture ferrite logic structure driven by a two-phase clock is described. The input/output and bias windings of this basic logic structure are modified to obtain OR, AND, NEGATION, MAJORITY, and EXCLUSIVE-OR logic functions. Also described is a structural interconnection method of achieving logical fan-out. Each of the logical functions are then combined to form a full-adder device, a set/reset flip-flop, and an edge detector circuit.

A new structure form and a six-phase clock scheme is developed that has the advantage of less flux loss during transfer with an attendant increase in operating range over the above described circuits. Also, two new structures named the Theta and Mark II Theta are described. Both are more compact than the original single-stage structure. The Theta structure operates in a similar manner as the basic delay element, while the Mark II Theta operates in a potentially superior complementary mode.

The logic design of an all-magnetic arithmetic unit is presented based on using the elemental delay logic device and its derivatives. The arithmetic unit is designed to serially add or subtract two 8-bit or multiply two 4-bit positive or negative binary numbers. The unit's operation is

broken up into three descriptive subsections, the adder/subtracter, the decoder/control, and the timing section. The multiplication algorithm, the most complex operation of the three operations, is described in detail.

Problems with the old process of fabricating the magnetic logic circuits are discussed. This process has been abandoned because of the resulting low yield of less than 5 percent. A new process is described using printed circuit techniques on flexible Kapton printed circuit sheets.

2.0 INTRODUCTION

In earlier work a class of all-magnetic logic circuits was developed which was based on use of a controlled threshold logic scheme and bi-material ferrite structures. These circuits provided an increased power gain over that obtainable with other non-resistance schemes which, in turn increased operating margins. Single stage and multi-stage bi-material logic structures were developed in which the coercive force and threshold characteristics of the materials were especially tailored to maximize the power gain of the circuits.

One of the outstanding attributes of these magnetic logic devices is the absence of a failure mechanism which makes them fundamentally ultra-reliable. The requirement for only inductive coupling to a device to form an operating circuit indicated that a circuit reliability approaching this fundamental reliability of the device was possible. To realize such ultra-reliable circuits a fabrication process was developed in which circuits with joint-free conductors were formed by plating.

A polyimide varnish capable of surviving severe environments was used for the insulation between conductors. The use of this insulation, however, resulted in a low yield for the process.

The work covered by this report involved the development of additional logic circuits which are compatible with the circuits developed earlier, and which simplify the logic design of complex systems. An arithmetic unit was designed to demonstrate the capability of these all-magnetic circuits to implement complex logic systems. In addition, a new

logic structure, the theta structure, and a new logic scheme, the six clock logic scheme, were conceived. An alternate insulation process with a higher yield has been developed because the original insulation process had too low a yield to be used. The development of this process occurred too late to fabricate the new logic circuits for evaluation of their operating characteristics.

3.0 CIRCUITS FOR ALL-MAGNETIC LOGIC SYSTEMS

The all-magnetic logic circuits described in the following pages are of the steered flux class. In these circuits each stage is partially switched by a clock current; however, the flux state of the stage is controlled by the input signal(s) applied in coincidence with the clock. The flux state of a stage, in turn, controls the occurrence of an output signal when driven by a second clock current. The basic form of this circuit, the delay circuit, used to form shift registers and ring counters was developed in two earlier contracts[1,2]. The group of circuits described here build on the basic circuit and provide the capability for the design and implementation of complex digital systems. These circuits are compatible in that they will drive and be driven by any of the other circuits. They all use a basic four-phase clock cycle. Only the exclusive OR circuit requires two added phases and the circuit has been operated experimentally using four-clock phases. The more complex logic functions are formed from combinations of the basic circuits.

Two new structure designs were conceived during the investigations undertaken during this program and the basic circuits using these structures are described.

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1. Heckler, C.H., "Development of a Toroid Having Unique Partial Switching Characteristics and Fabrication of an Integrated Magnetic Logic Structure," Final Report Contract NAS1-5963, Stanford Research Institute, Menlo Park, Calif., October, 1967. Also available as NASA CR-66496.

2. Heckler, C.H., Jr. and Bhiwandker, N.C., "Development of Magnetic Logic Batch Fabrication Techniques," Final Report Contract NAS1-7878, Ampex Corp., Redwood City, Calif. Also available as NASA CR-66890.

3.1 Basic Circuits

The basic delay circuit consists of a multi-aperture logic structure driven by a two-phase clock. Alternate structures are driven at different clock times to provide temporary storage between transfers as a stage cannot simultaneously transmit and receive information. This requires four-clock phases -- two odd and two even -- for one unit of logic delay. The delay through the basic delay circuit being 1/2 unit of logic delay. The basic clock winding patterns for the delay circuit are shown in Figs. 1 through 4 and a timing diagram for the clock currents is shown in Fig. 5. The input and output winding patterns are shown in Fig. 6. A two-turns winding is used for the output winding providing a 2:1 turns ratio between the output and input windings. This provides the flux gain needed to overcome the losses associated with the clipper core and the resistance of the coupling loop so that a signal is not decreased during transfer. This "unity gain" condition is required so that the signal is not lost after any arbitrary number of transfers.

The operation of the basic circuit has been given elsewhere[2] and will only be summarized here. The reference state of a logic structure is the clear state in which the flux is saturated in a counter clockwise direction around the main aperture.*

The application of the set clock current through the "figure 8" winding on the drive apertures causes the flux to be half switched in a clockwise direction around the main aperture. This would normally result in both leg A and leg B being half switched. However, the bias clock current which is applied to leg A at the same clock phase prevents leg A

* Appendix B: Logic Structure Path Identification.

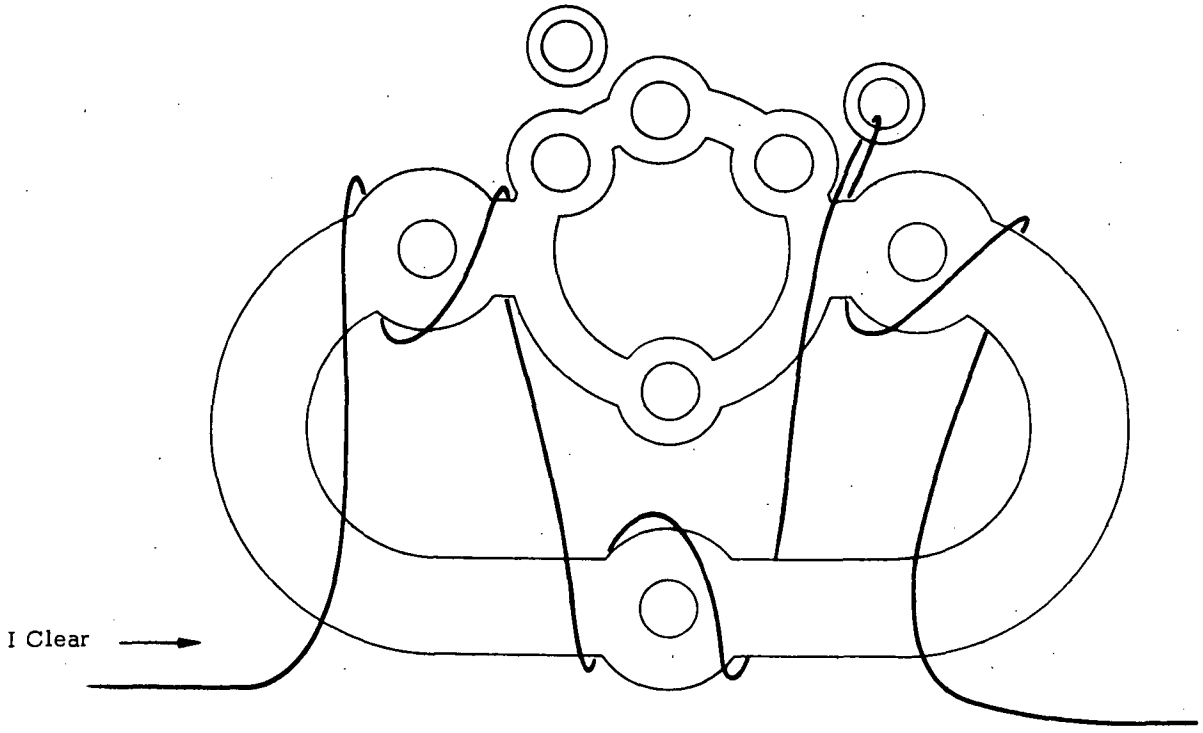


Fig. 1 Clear Winding Pattern: Basic Delay Circuit

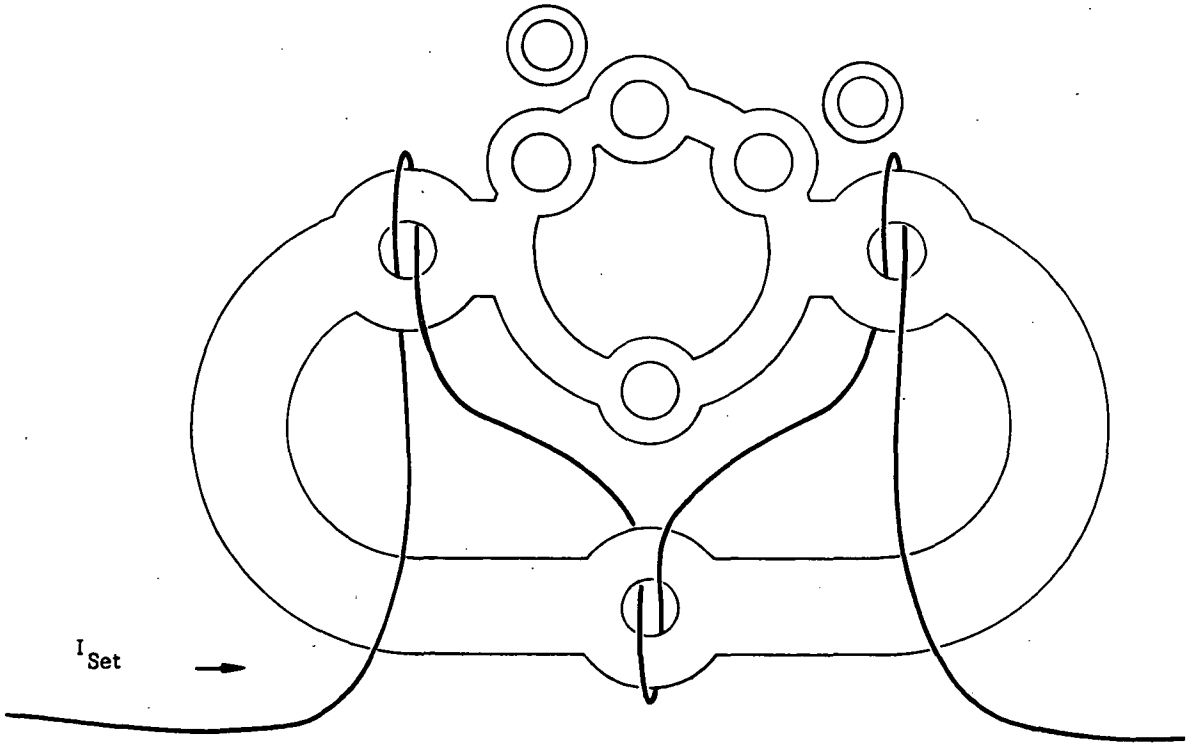


Fig. 2 Set Winding Pattern: Basic Delay Circuit

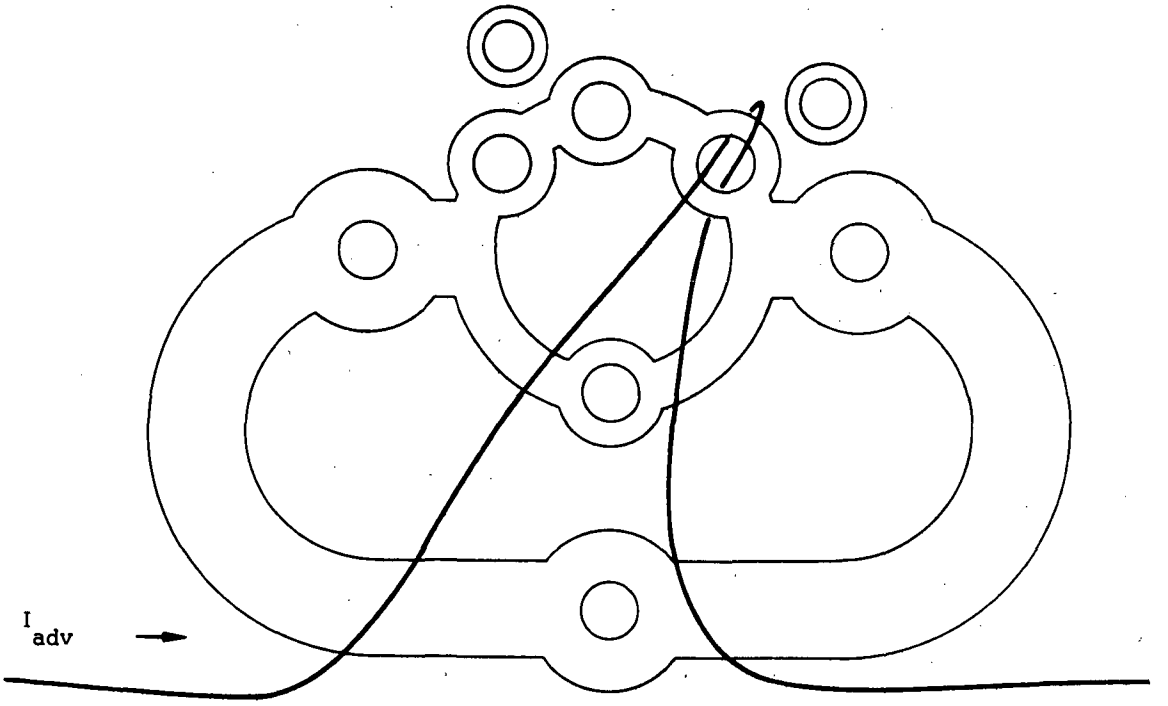


Fig. 3 Advance Winding Pattern: Basic Delay Circuit

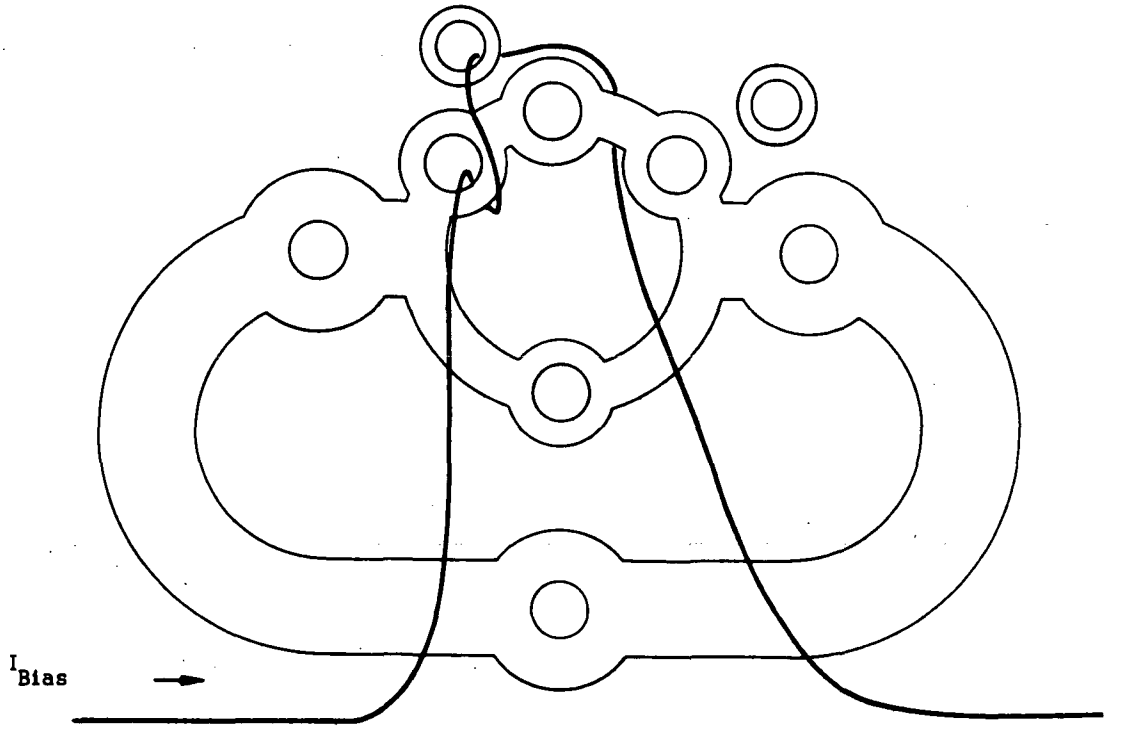


Fig. 4 Bias Winding Pattern: Basic Delay Circuit

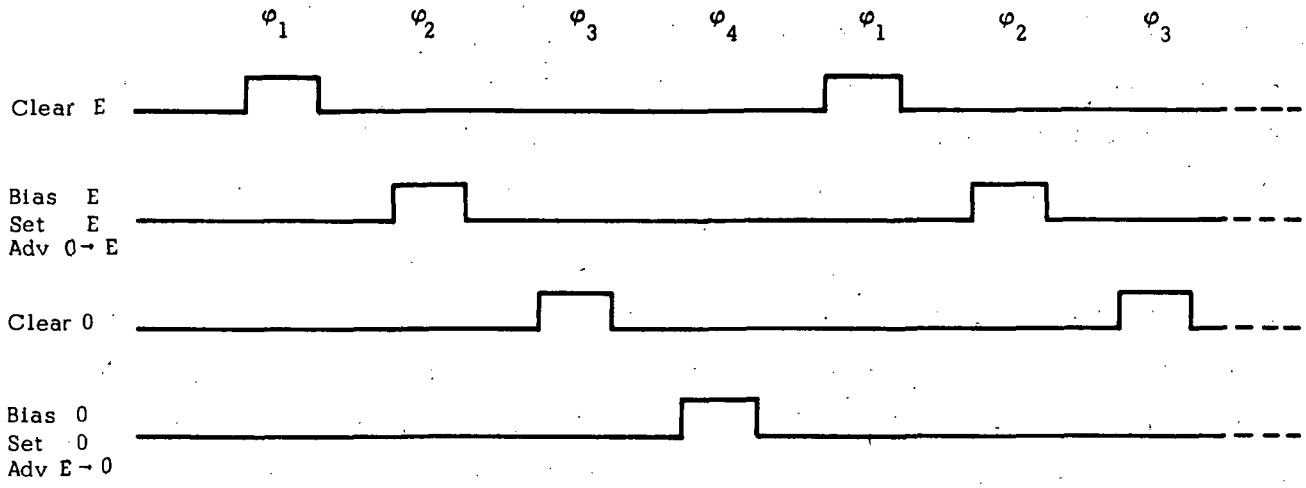
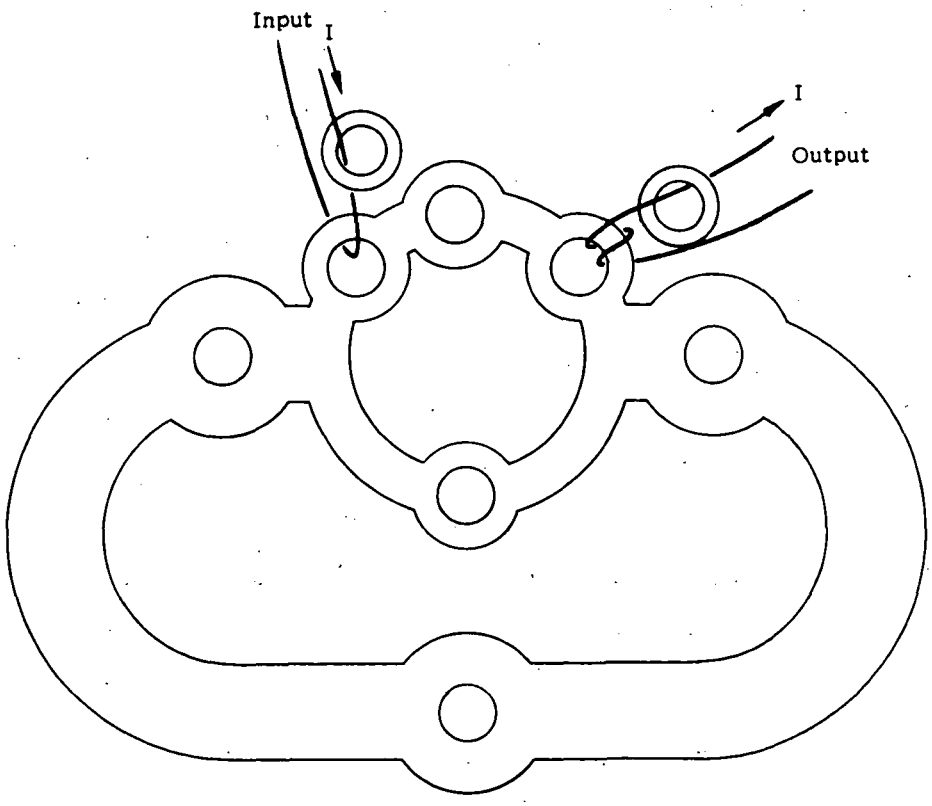


Fig. 5 Timing Diagram for Basic Delay Circuit



Note: Coupling loop current directions are shown for advance times φ_2 and φ_4

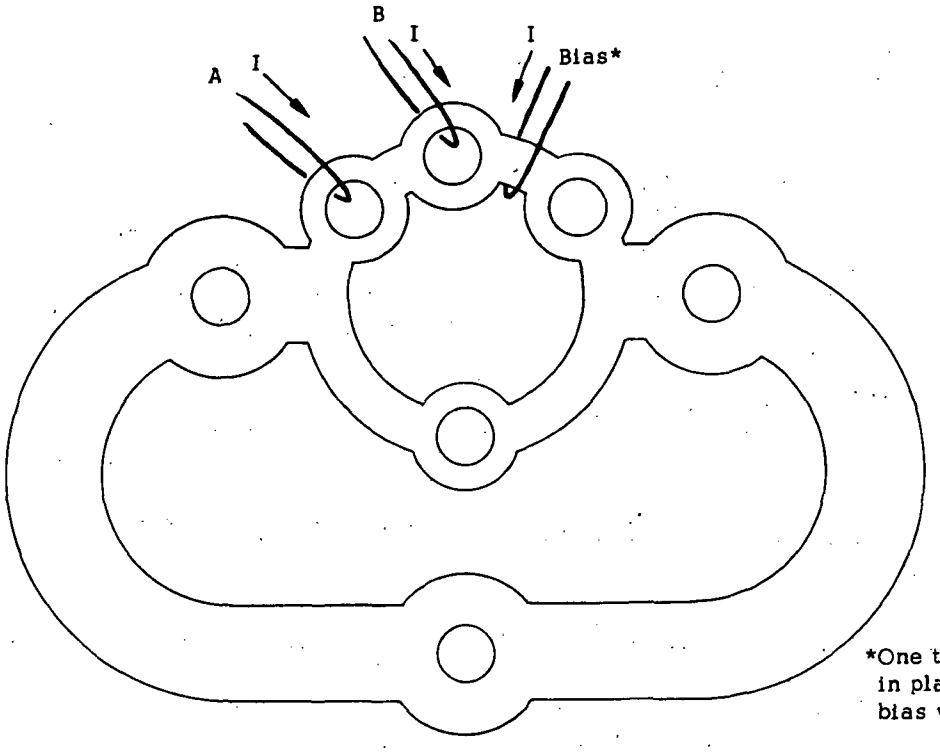
Fig. 6 Input/Output Winding Pattern: Basic Delay Circuit

from switching and this results in leg B being fully switched. This is the ZERO state of a structure and results when an input signal is not present during the phase the set clock is applied. With leg A in the clear state the application of the advance clock current through the "figure 8" winding on the output aperture can not switch through legs 1 and 2 around the output aperture and, therefore, no signal is induced in the output winding.

When an input signal is present during the phase the set clock is applied, the mmf produced by the input current is in a direction to oppose and of a magnitude to cancel the bias mmf. This results in leg A and leg B being half set. The application of the advance clock current when leg A is half set will cause legs 1 and 2 to switch around the output aperture inducing a signal in the output winding. As can be seen from the timing diagram of Fig. 5, the clock currents are so phased that an output from an odd structure provides an output signal at the time the even structure is set and vice versa. Information transfer is obtained by directly coupling the output windings from structures of one phase to the input windings of structures of the other phase.

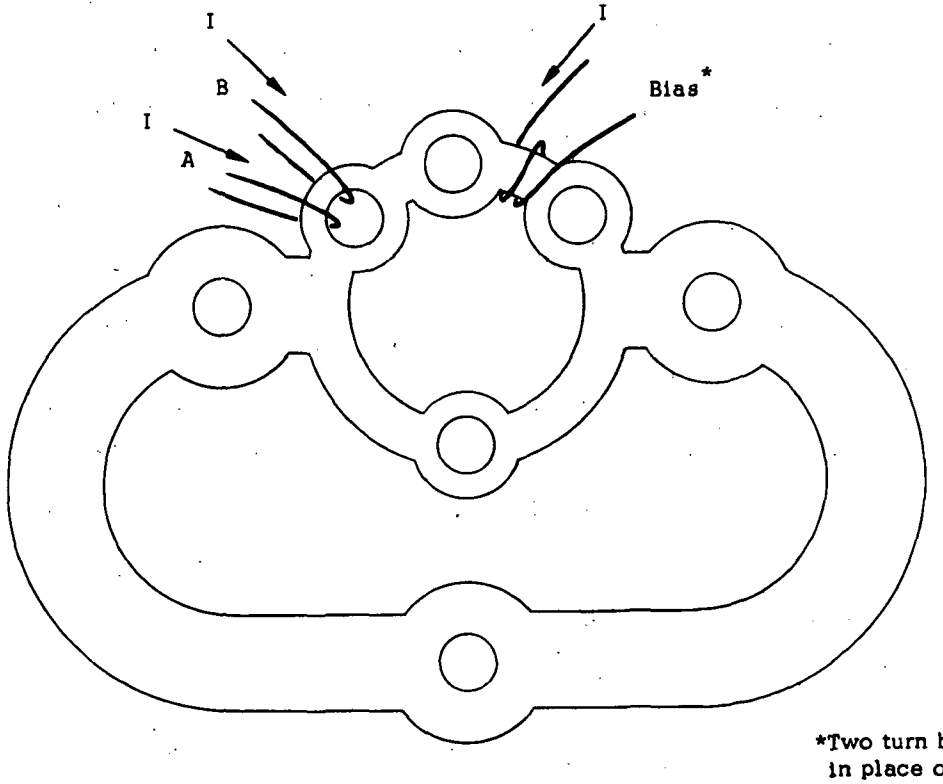
The OR function is obtained by adding an input winding to the second input aperture of a structure and simplifying the bias windings. The winding pattern for the OR function is shown in Fig. 7. Only those winding patterns which are not the same as for the basic delay circuit are shown . The two input apertures are used to provide the required decoupling when only one of the input signals is present. After a single input transfer the reversed coupling loop current induced by clearing of the transmitter causes switching in legs 1 and 2 around the input aperture without disturbing the ONE flux state of leg A.

The AND function is provided by modifying the OR circuit bias winding pattern. The winding pattern for the AND function is shown in Fig. 8. Only the winding patterns that differ from the basic delay circuit



*One turn bias winding in place of standard bias winding.

Fig. 7 Winding Pattern "OR" Function



*Two turn bias winding in place of standard bias winding.

Fig. 8 Winding Pattern "AND" Function

are shown. The bias winding is increased to two turns on leg A so that two input signals are required to cancel the bias mmf and set the structure into the ONE state. The occurrence of only one of the input signals is insufficient to steer flux into leg A. Since switching does not occur with only one input signal present, there is no need for decoupling the inputs separately as for the OR function.

The NEGATION function is obtained by replacing the clipper core of the basic delay circuit with a core of greater flux capacity and driving this core with the advance clock. The winding pattern for the NEGATION function is shown in Fig. 9. Only the winding patterns which differ from the basic delay circuit are shown. In this circuit the direction of the coupling loop current is reversed and, therefore, the connection to the input winding of the succeeding stage must also be reversed. When the NEGATION stage is in the ONE state the coupling loop current switches flux in legs 1 and 2 around the output aperture and thereby limits the coupling loop current below that which will set the receiver stage into a ONE state. When the NEGATION stage is in a ZERO state the coupling loop current will not cause switching in legs 1 and 2 around the output aperture and the coupling loop current is not limited. Thus a ONE is transferred into the receiver stage. The bias clock current is applied to the NEGATION stage at the time of the advance clock to prevent switching in leg A.

The NEGATION function may be combined with the other basic functions. Thus, the OR function and NEGATION function combined in one circuit to form the NOR function. Similarly the NAND function is formed in a single circuit by combining the AND and NEGATION functions.

The MAJORITY function is derived by an extension of the AND circuit. The only difference being that a third input is added.

The winding pattern for the MAJORITY function is shown in Fig. 10. Since the logic structure used has only two input apertures a means

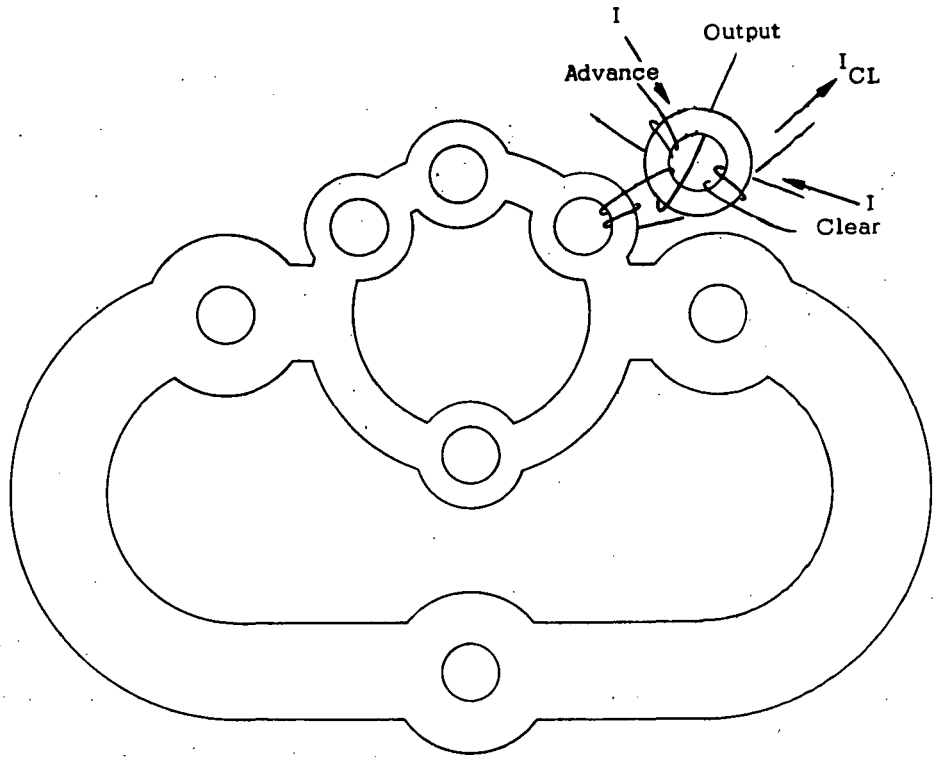


Fig. 9 Winding Pattern: Negation Function

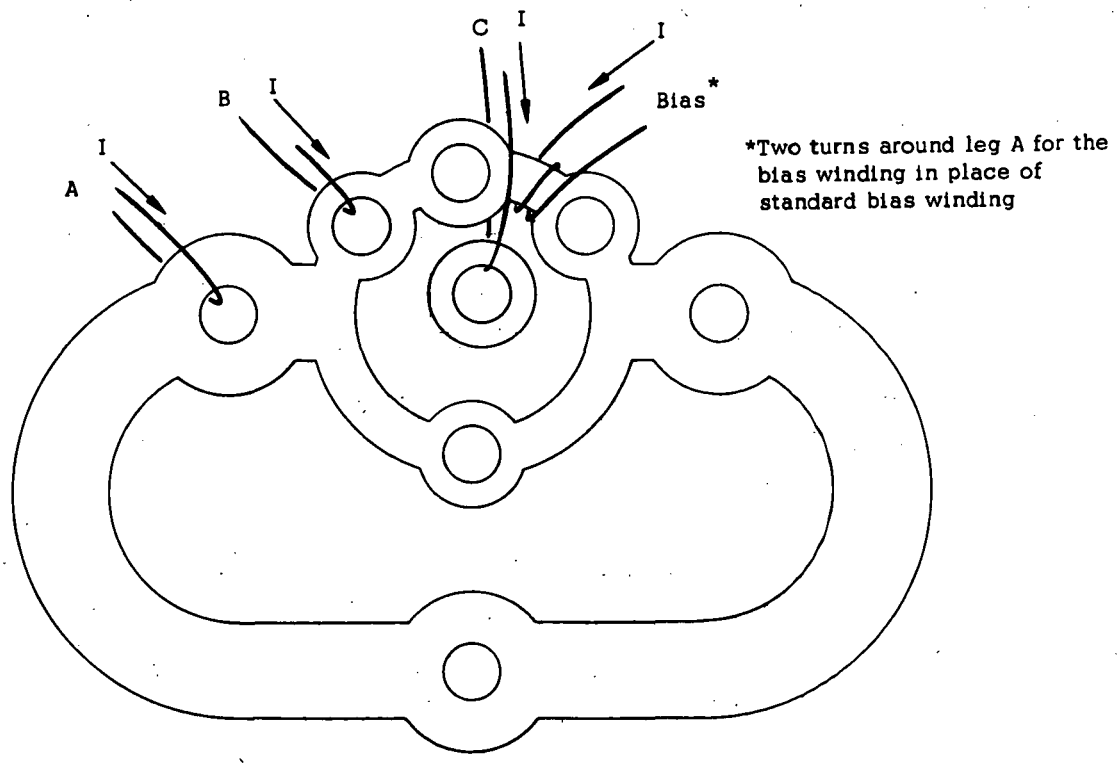


Fig. 10 Winding Pattern: Majority Function

must be provided to decouple the third input. Individual decoupling of the inputs is required in this circuit because a ONE transfer will occur with inputs signals on any two of the three inputs. Decoupling of this third input is accomplished with a synthetic aperture[3] which consists of a low threshold toroid also threaded by the input winding. This toroid is driven in the clear direction by the normal coupling loop current and so does not alter the circuit operation. When the transmitter is cleared and the coupling loop current reversed, this toroid switches and limits the coupling loop current below a value which would disturb the ONE state of leg A and provides the same decoupling as an input aperture.

Logic gain is provided by the FAN-OUT circuit shown in Fig. 11. The timing diagram showing the phases for the clock currents is shown in Fig. 12. In the FAN-OUT circuit the input winding links two receiver structures each of which are driven by the set and bias clock currents at different clock phases. One structure (receiver) is driven at the phases used for the basic delay circuit, i.e., φ_2 for even phase structures and φ_4 for odd phase structures. The input winding links the A leg of this structure in the normal sense but does not thread the input aperture. The second structure (receiver') is driven by the primed Set and Bias clocks. At the clock phase the transmitter is cleared, i.e., φ_3 for the even phase and φ_1 for the odd phase structures. The input winding through this struc- links leg 1 around the input aperture but in the opposite sense. The clock and output winding patterns are the same as for the basic delay circuit. A logical gain of 2 is provided by this circuit by transferring a ONE to the receiver structure at the normal transfer time and by transferring a ONE to the receiver' structure when the transmitter is cleared. There is no switching in the receiver' structure during the normal transfer as the

3 Englebart, D.C., "A New All-Magnetic Logic System Using Simple Cores," Dig. Tech. Papers, 1959, Solid State Circuits Conf., Philadelphia, Pa. pp. 66-67, Feb., 1959.

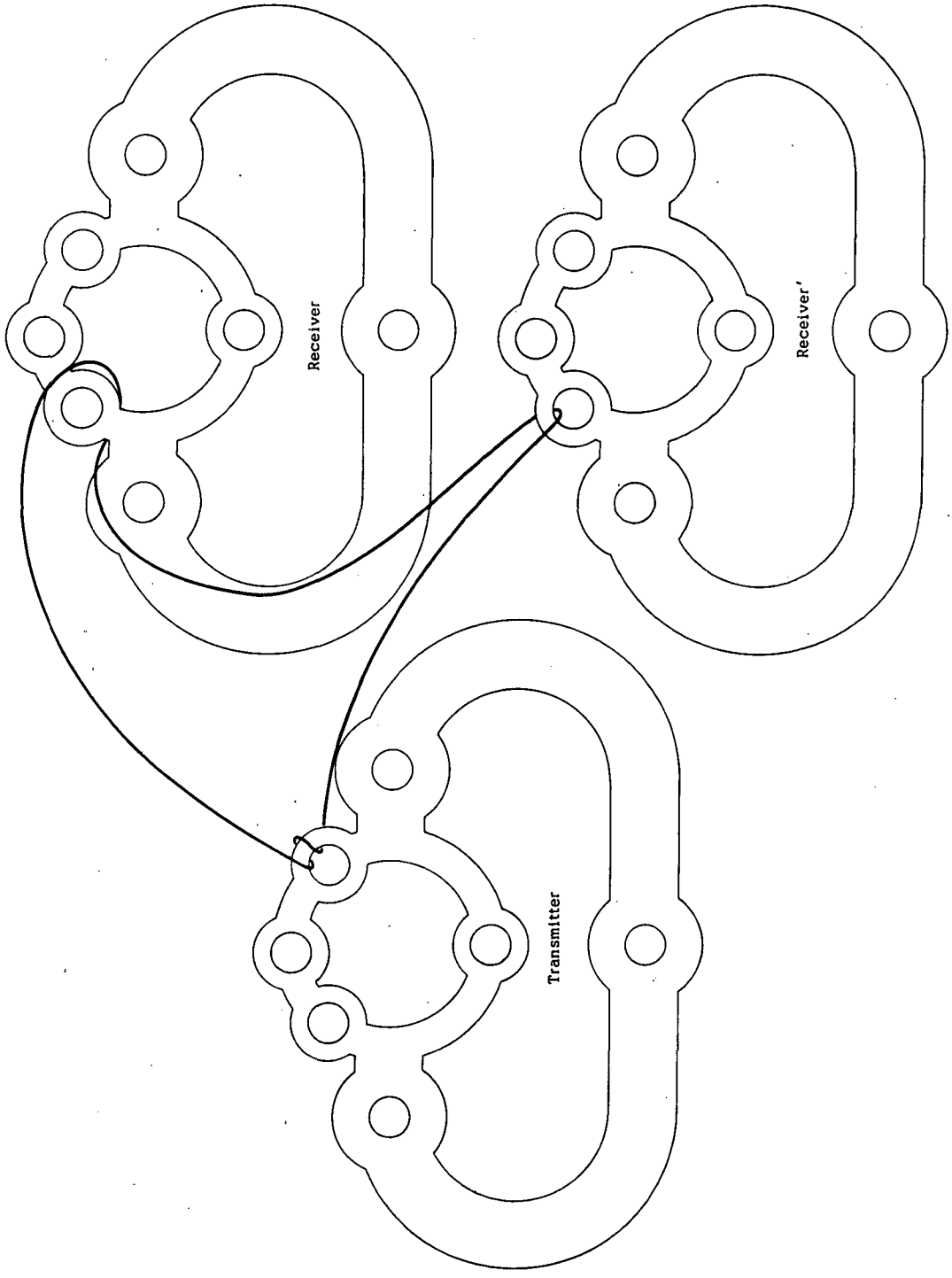


Fig. 11 Fan Out Winding Pattern

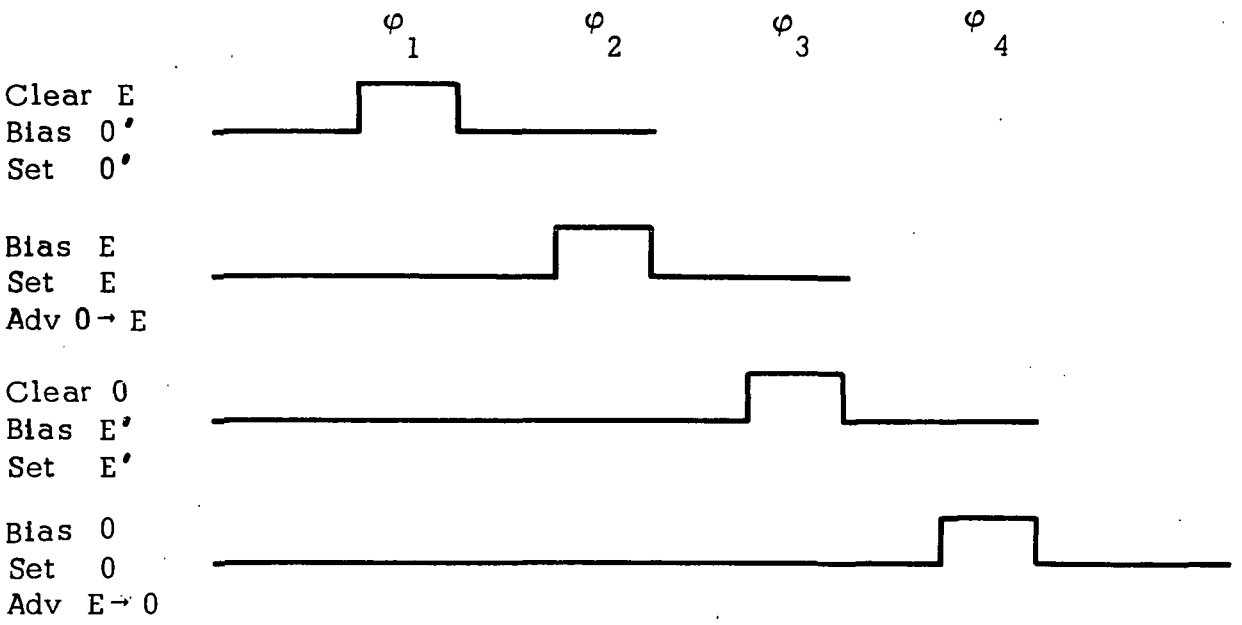


Fig. 12 Timing Diagram for Fan Out Circuit

coupling loop current drives leg 1 around the input aperture of this structure in the clear direction. There is no switching in the receiver structure during the second transfer, when the transmitter is cleared as the input winding does not thread the input aperture in this structure and legs 1 and 2 around the input aperture are not switched.

The EXCLUSIVE-OR function is obtained with the circuit shown in Fig. 13. The output windings of the transmitting stages are connected series opposing to form a bi-polar signal to drive the "C" structure. The input winding threads both input apertures of this structure so that either polarity signal will set the structure into a ONE state. The output windings of the "A" and "B" structure are "figure 8" windings to prevent signal loss which, with 2-turn windings on leg 1, would occur during a single ONE transfer. In this case, the coupling loop current through the output winding of the ZERO state structure would partially switch this structure and decrease the signal set into the "C" structure. For both "A" and "B" structures in a ONE state the output signals cancel and no coupling loop current

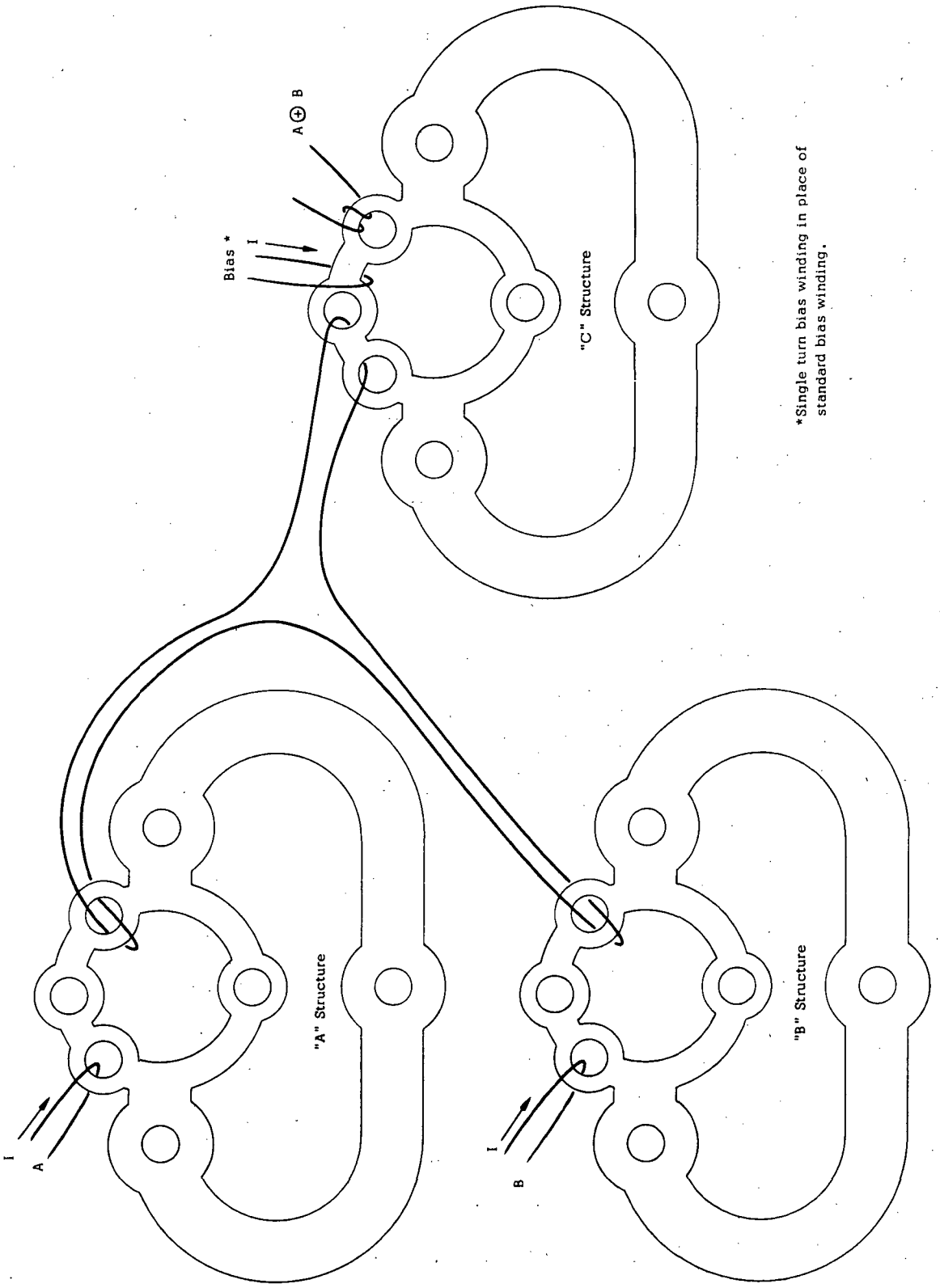


Fig. 13 Winding Pattern: "Exclusive OR" Function

flows allowing the "C" structure to switch into the ZERO state. The "figure 8" output winding does not have the flux gain of the normal 2 turn output winding. Therefore to increase the flux gain, a pre advance clock is added to obtain a larger output at the advance clock which switches legs 1 and 2 of the output aperture. With a "figure 8" output winding the flux set into a stage is divided equally into legs 1 and 2 as opposed to the standard 2 turn output winding where the flux is steered into leg 2 only.

The pre advance clock will switch flux, increasing flux in leg 1 and decreasing flux in leg 2 by an amount which is a function of the coupling loop current, the coupling loop resistance and the noise signal of the ZERO stage structure. However, the maximum flux which can be switched is equal to the flux set into the stage.

The flux switched by the advance clock is increased by an amount sufficient to provide unity gain transfer to the "C" structure. The pre advance and advance winding patterns are shown in Figs. 14 and 15. The timing diagram with the two additional phases which are required for the pre advance clocks is shown in Fig. 16. The gain curve for a hand wired exclusive - OR circuit wired as indicated in Figs. 13 through 15 is given in Fig. 17 together with the amplitude of the clock currents. The duration of all clock pulses was 3 μsec.

3.2 Derived Circuits

The full adder function is formed from two cascaded EXCLUSIVE-OR circuits, a MAJORITY circuit, and a FAN-OUT circuit. The logic diagram for the full adder is shown in Fig. 18. This is a serial adder for the addition of two numbers starting with the least significant bits. The sum of the two variables is produced by the first EXCLUSIVE-OR circuit. The carry generated by the preceding bits is added to the first sum in the second EXCLUSIVE-OR circuit to produce the final sum for that bit. The MAJORITY circuit produces a carry signal when two or more of the three inputs are

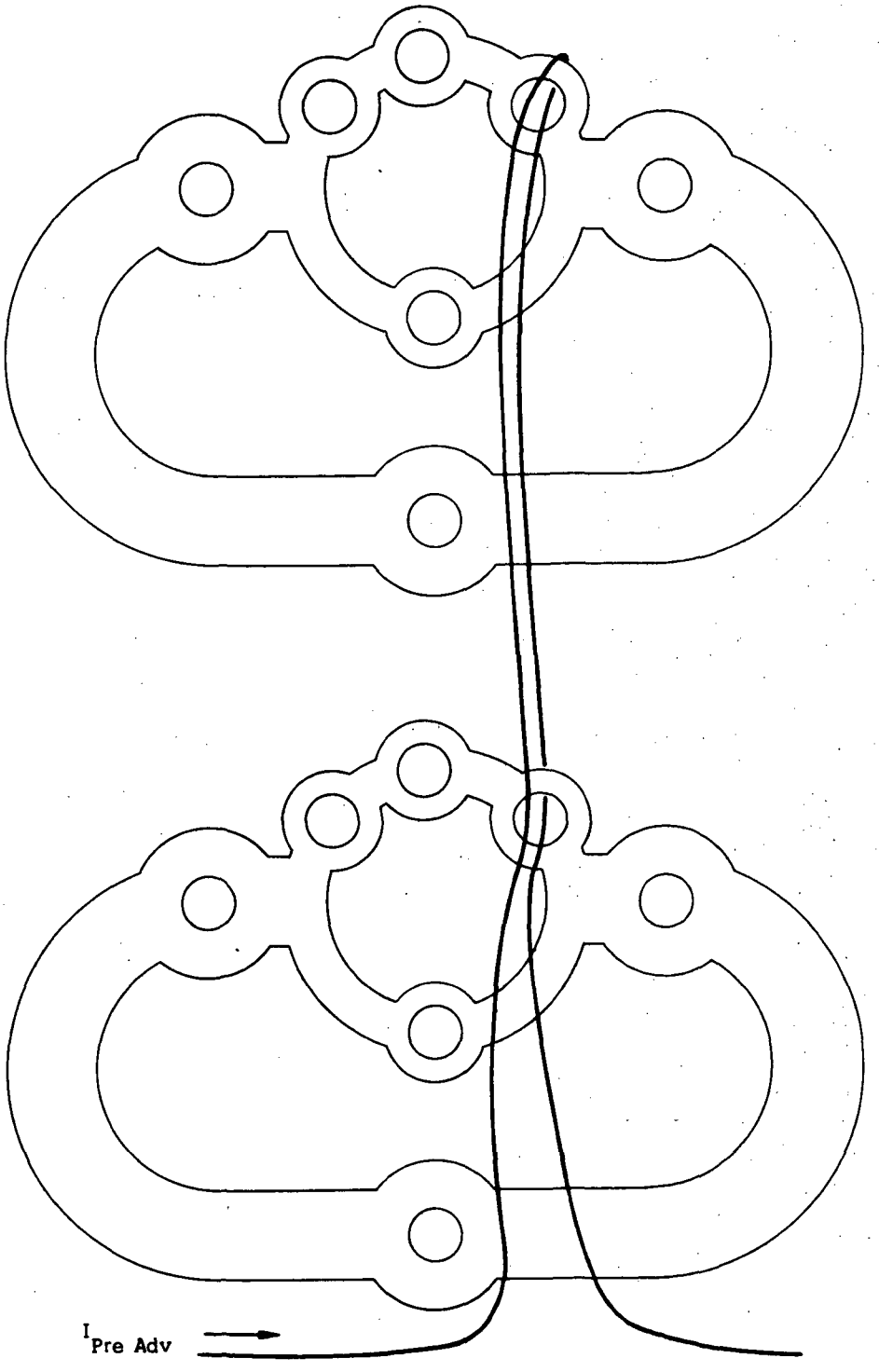


Fig. 14 Pre Advance Winding Pattern: Output Stages Driving Into Exclusive-OR

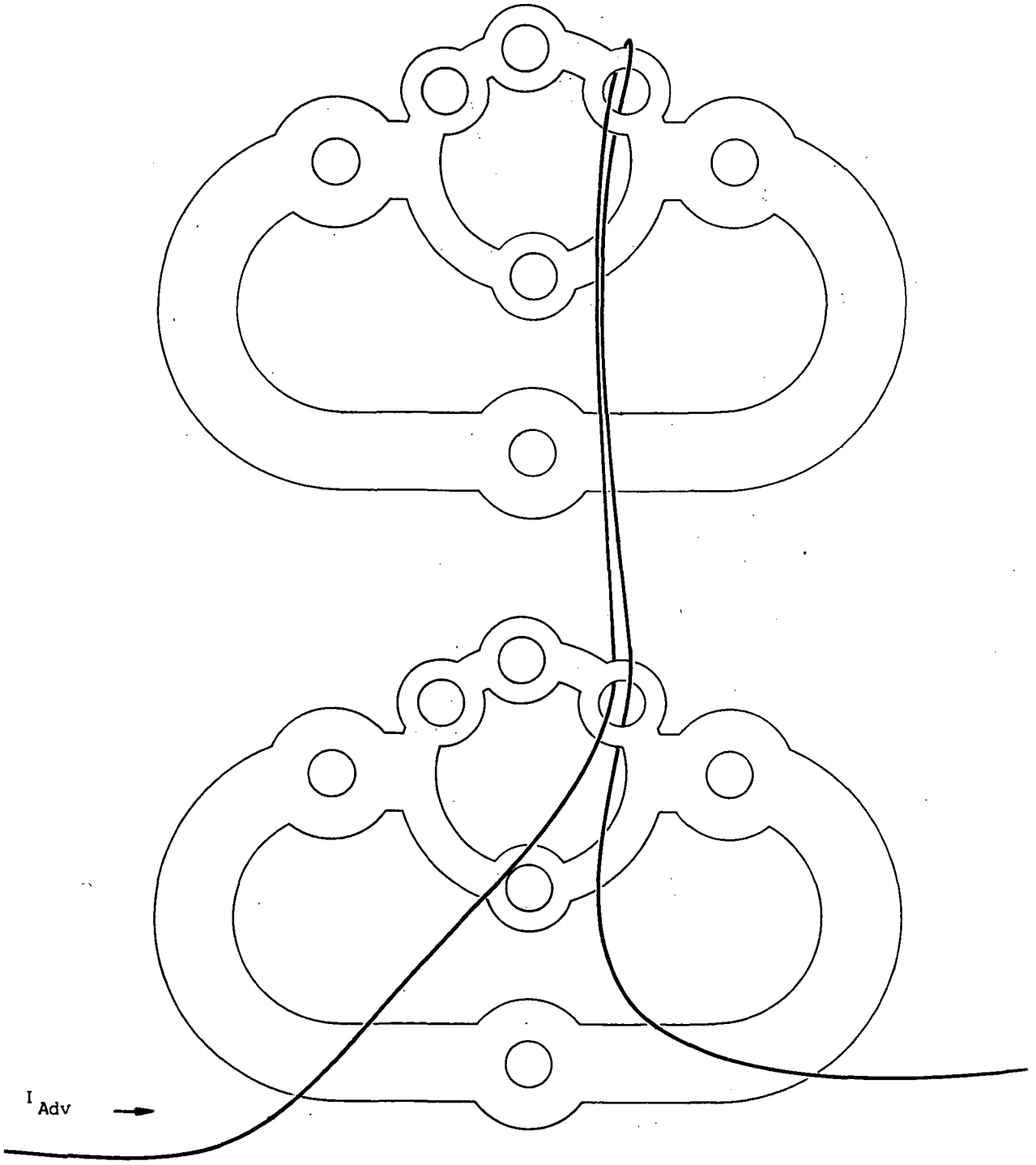


Fig. 15 Advance Winding Pattern: Output Stages Driving Exclusive -OR

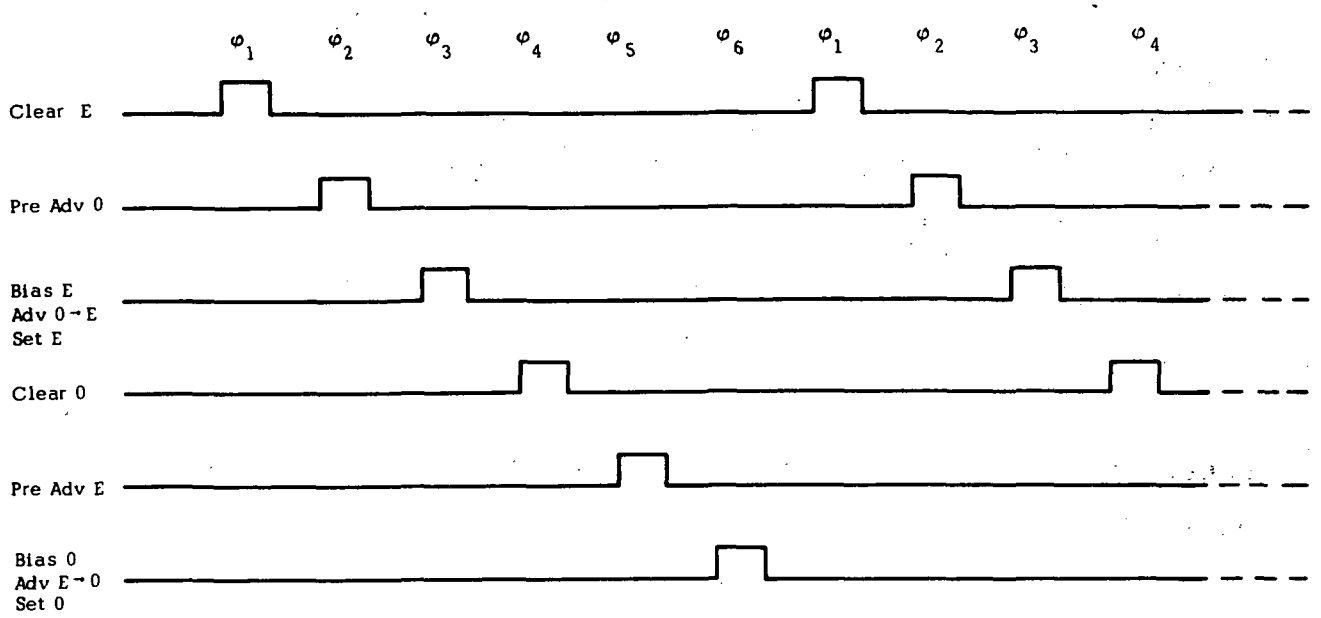


Fig. 16 Timing Diagram: Exclusive -OR

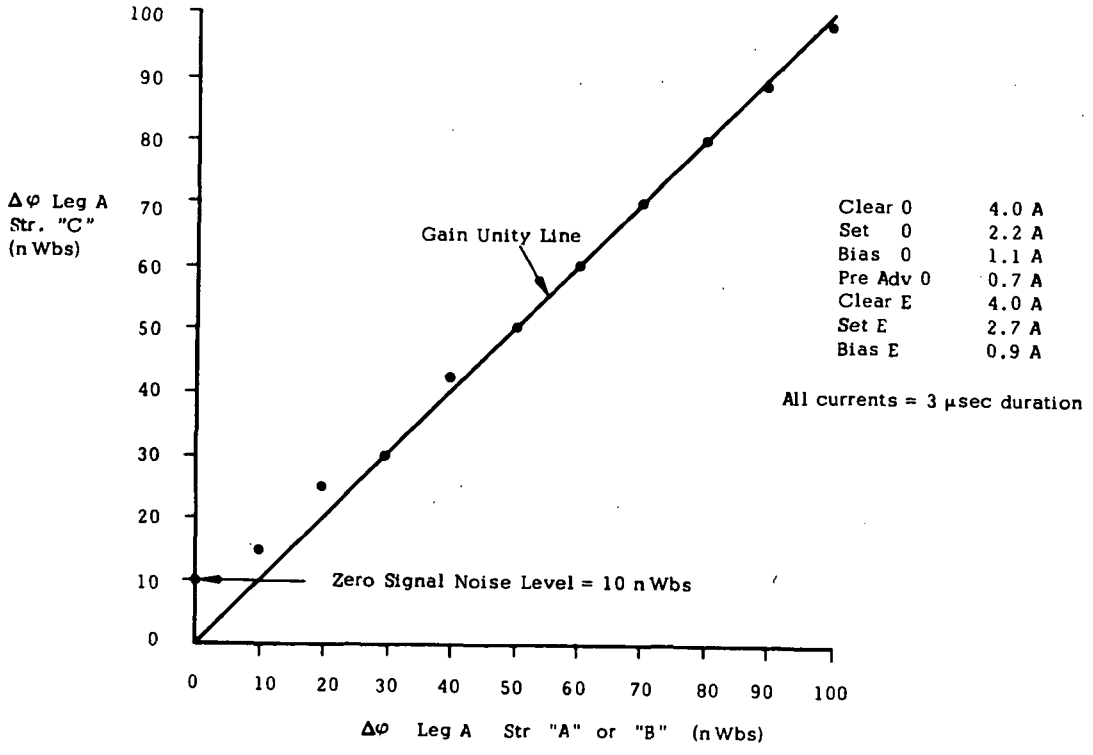


Fig. 17 Gain Curve: Exclusive-OR Circuit

present. The additional circuits provide a one unit and a one and one half unit logic delay to time the arrival of the carry bit to coincide with the next most significant bit at the MAJORITY circuit and the second EX-CLUSIVE-OR circuit. The truth table for the addition of two numbers is given in Table 1, and the truth tables for the sum and carry of the full adder circuit are given in Tables 2 and 3. Inspection shows the full adder circuit provides the outputs required for the addition of two binary numbers.

The flip flop circuit is formed from two NOR circuits, a FAN-OUT circuit and a NEGATION circuit. A logic diagram for the flip flop is shown in Fig. 19. The presence of a ONE on the set input causes the upper NOR to be set to the ONE state and therefore the lower NOR to the ZERO state. In this "set" state ONE's will be transmitted out of the output negation stage until the flip flop is reset. The presence of a ONE on the reset input sets the lower NOR circuit to the ONE state and therefore the upper NOR

Table I Truth Table for Serial Addition of Two Binary Numbers

A	B	Carry In	Sum	Carry Out
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

Table 2 Truth Table for Sum Output From Full Adder

A	B	Part. Sum 1st Ex-OR Output	Carry	Sum 2nd Ex-OR Output
0	0	0	0	0
1	0	1	0	1
0	1	1	0	1
1	1	0	1	0
0	0	0	0	1
1	0	1	1	0
0	1	1	1	0
1	1	0	1	1

Table 3 Truth Table for Carry Generation in Full Adder

A	B	Carry In	Carry Out
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	1

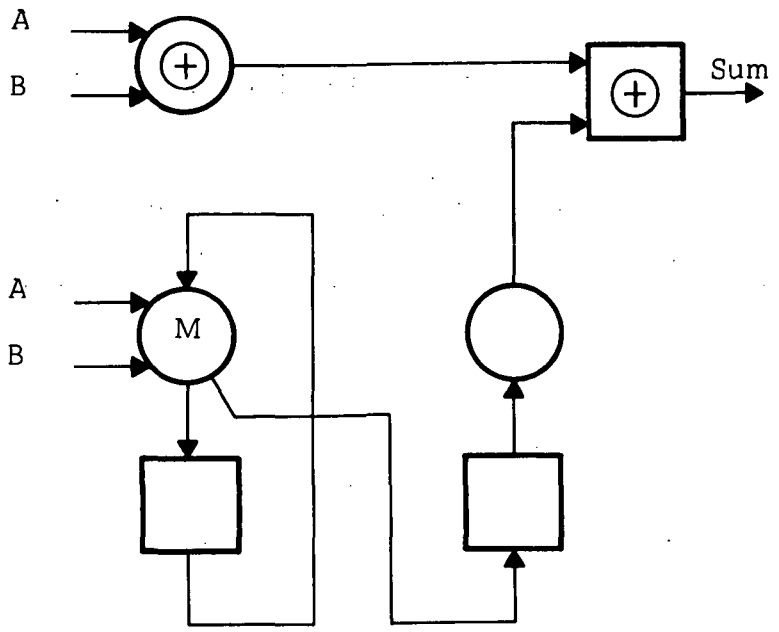


Fig. 18 Full Adder

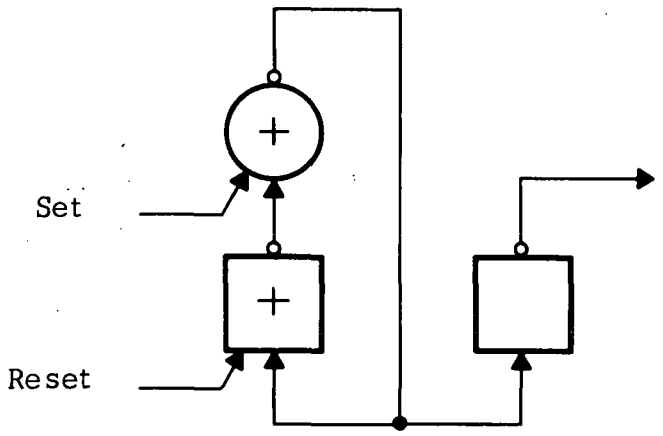


Fig. 19 Flip Flop

to the ZERO state. In this "reset" state ZERO's will be transmitted from the output negation stage until the flip flop is set.

The edge detector is a circuit for detecting the change in state of a flip flop and produces a single output at each such change. This circuit is implemented using a FAN-OUT circuit, an AND circuit and a NEGATION circuit. The logic diagram for realizing an edge detector is shown in Fig. 20. The AND circuit compares each bit with the NEGATION of the bit which preceded it. An output from the AND circuit is produced only for two ONE inputs which can occur only for a ZERO followed by a ONE. This is the condition when a flip flop changes from the reset to the set state.

3.3 New Circuits

A structure for use with a six phase clock cycle is shown with the basic winding patterns required for operation in Figs. 21 through 25. The timing diagram showing the phase of the clock currents is given in Fig. 26. The operation of this circuit is as follows: The clear clock places the structure in the reference state which is the ONE state, i.e., half switched clockwise around the stage apertures. At the advance phase, transfer of a ONE switches legs 1 and 2 around the input aperture placing leg 2 in the clear state. At the post advance phase the clock current is applied through legs 2 of the input and auxiliary apertures in a direction to clear the structure to a ZERO state. With leg 2 of the input aperture in the clear state there is insufficient mmf to switch flux around the stage aperture and the structure remains in the ONE state. The output is obtained as in the preceding circuits. When a ZERO is transferred, leg 2 of the input aperture is not set in the clear state and the post advance clock will switch the structure to the ZERO state and no output signal will be generated at the next advance phase.

A major advantage of this scheme is a lower flux loss during transfer as lower coupling loop currents are required. This in turn increases the operating range of the circuits. This circuit has been simulated with the present logic structures and shift register operation was obtained, without rewiring, in circuits that were too lossy to operate in the standard four clock phase scheme.

A new structure design was made with a redesigned return leg which is more compact than the present single stage structure. This structure, the Theta structure, is shown in Fig. 27. In operation, this structure uses the same winding patterns as the present single stage structure. The only difference is that the set clock is turned on with both advance clocks.

Consideration of the use of this structure design for complementary logic led to the Mark II Theta structure. The winding patterns for a complementary logic scheme using the Mark II Theta structure are shown in Figs. 28 through 31. Operation of this circuit is similar to the present circuits except that the function and its complement are generated in each circuit. A complete evaluation of the advantages and disadvantages of this circuit has not yet been made.

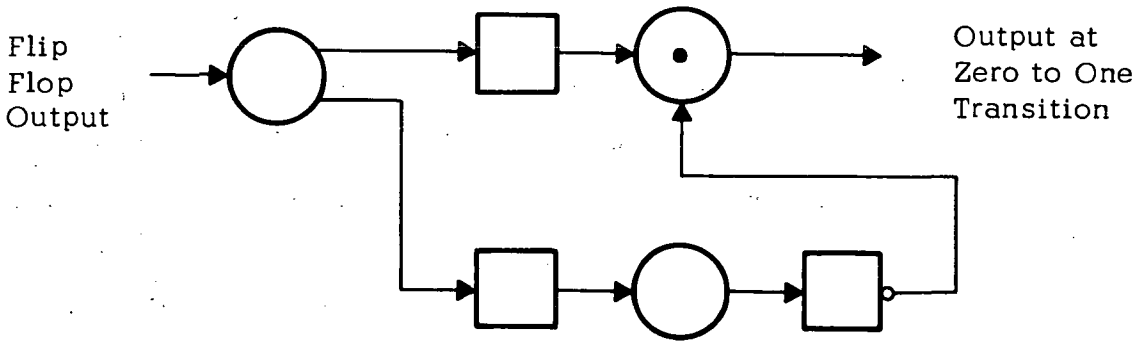


Fig. 20 Edge Detector

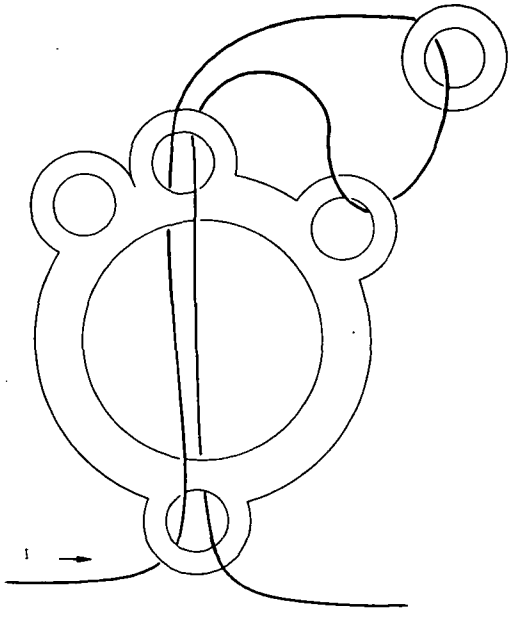


Fig. 21 Clear Winding Pattern: Six Clock Circuit

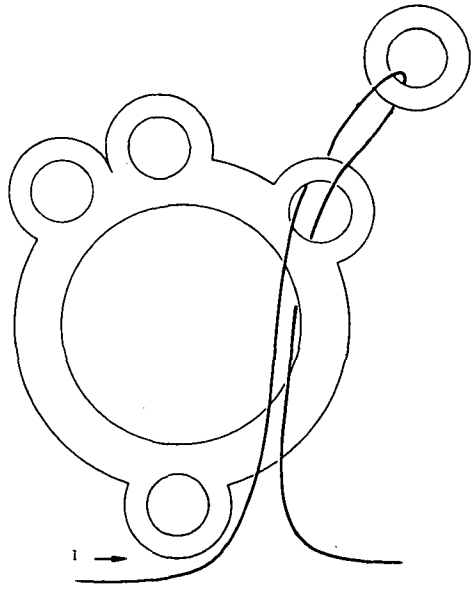


Fig. 22 Advance Winding Pattern: Six Clock Circuit

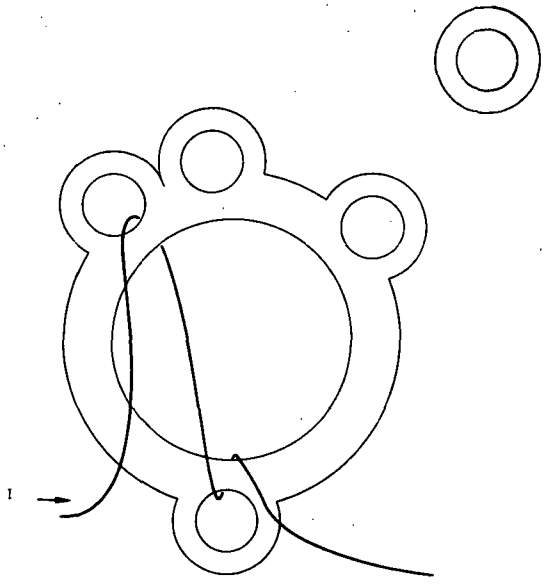


Fig. 23 Post Advance Winding Pattern: Six Clock Circuit

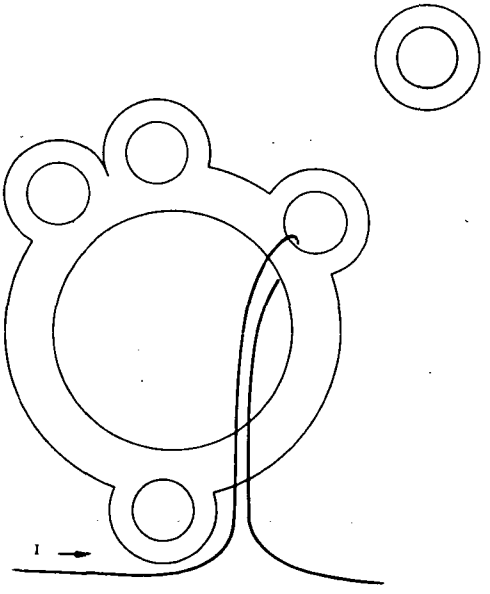


Fig. 24 Hold Winding Pattern: Six Clock Circuit

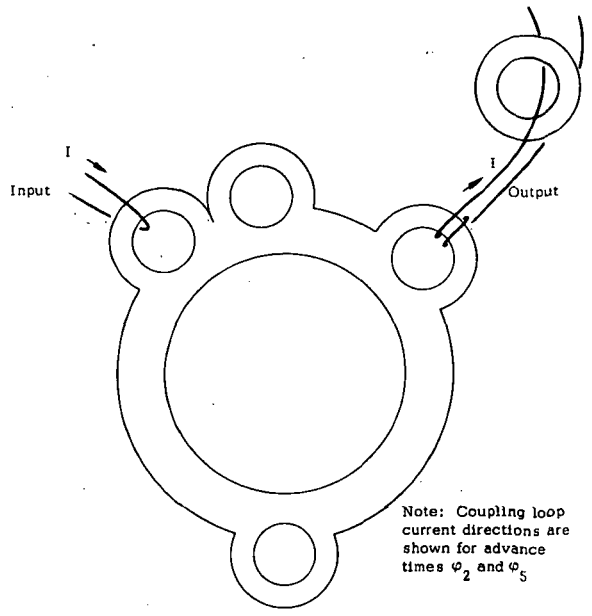


Fig. 25 Input Output Winding Patterns: Six Clock Circuit

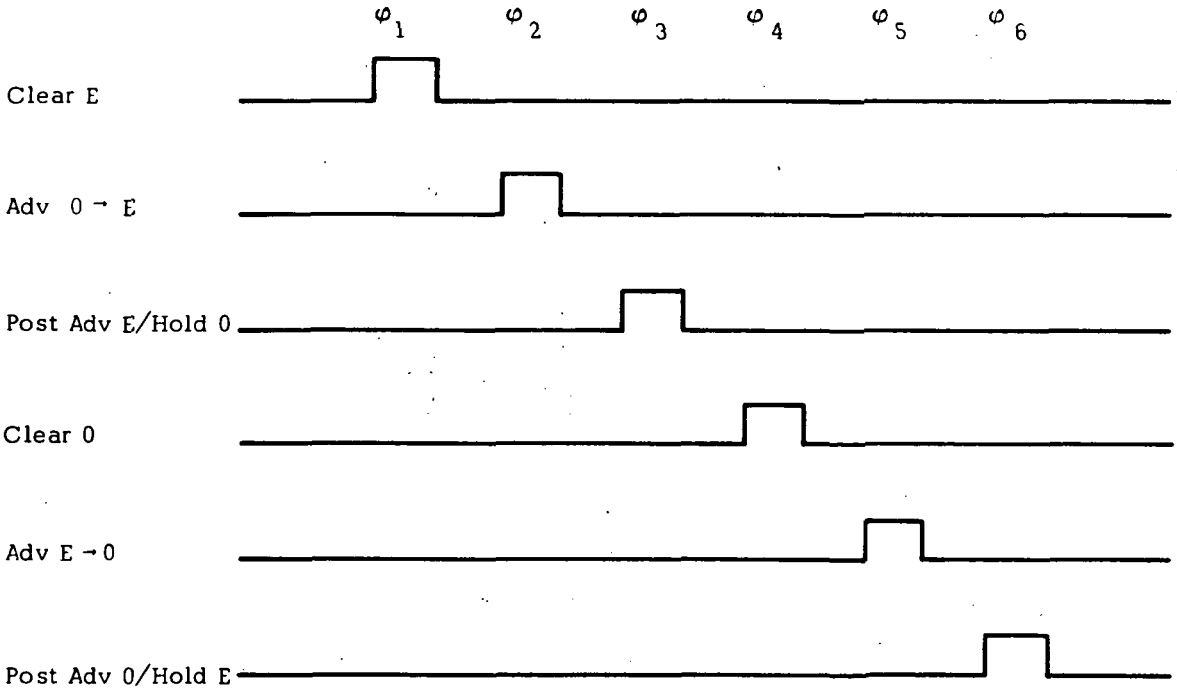


Fig. 26 Timing Diagram: Six Clock Circuit

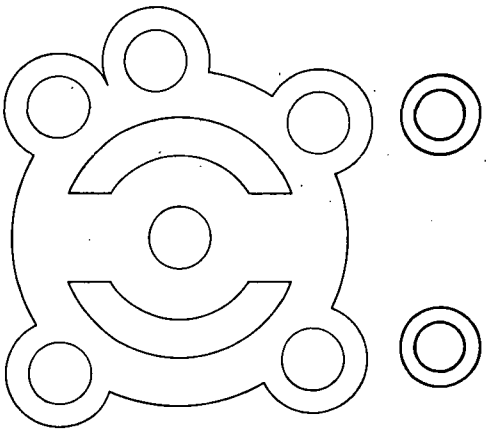


Fig. 27 The Theta Logic Structure

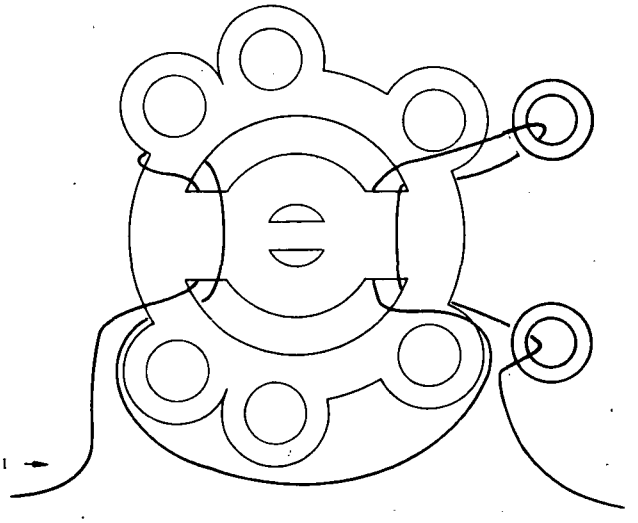


Fig. 28 Clear Winding Pattern: Complementary Logic Circuit

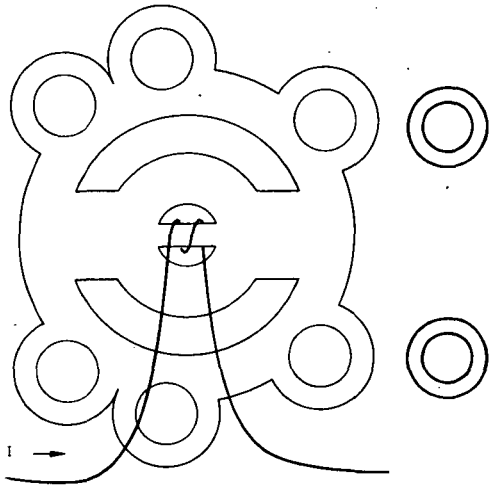


Fig. 29 Set Winding Pattern: Complimentary Logic Circuit

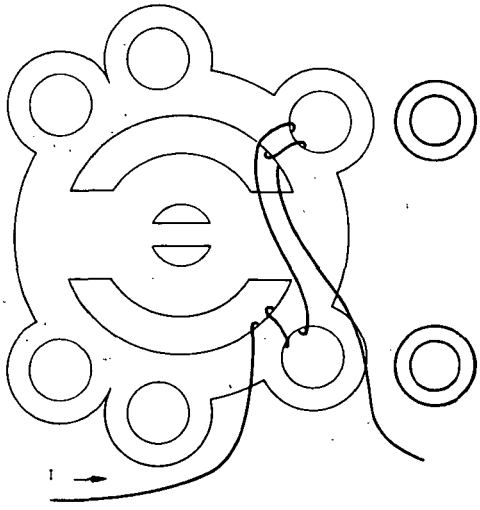


Fig. 30 Advance Winding Pattern: Complimentary Logic Circuit

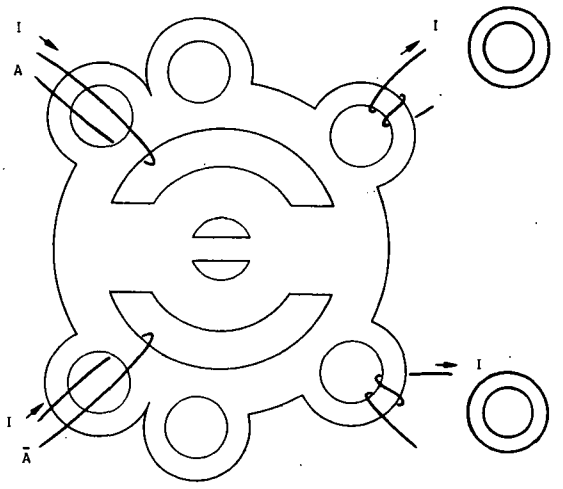


Fig. 31 Input/Output Winding Pattern
Complementary Logic Circuit

4.0 LOGIC DESIGN: ALL-MAGNETIC ARITHMETIC UNIT

The logic design for an All-Magnetic Arithmetic Unit has been made based on the basic logic circuit developed under Contracts NAS1-5963[1] and NAS1-7878[2] and the circuits described in Sections 3.1 and 3.2 The Arithmetic Unit is designed to serially add or subtract two 8-bit binary numbers or multiply two 4-bit binary numbers. The numbers may be positive or negative. The input and output numbers are represented by 8 bits plus a sign bit. Internal to the Arithmetic Unit negative numbers are transformed to be represented by the one's complement for addition and subtraction but remain represented by magnitude and sign for multiplication. Two function bits follow the sign bit and, a space bit is added to separate words to make a total of twelve bits for the word length. Words are input and output serially, least significant bit first.

The logic diagram for the All-Magnetic Arithmetic Unit is shown in Fig. 32. The logic circuits for the adder/subtracter sections are located at the upper half of the drawing, the circuits for the decoder/control section are at the lower right and the circuits for the timing section are at the lower left of the logic diagram.

Timing for synchronizing the input words is supplied by a sync pulse which occurs 1/2 logic cycle before the beginning of each word cycle. The number stored in the A register, which serves as the accumulator is read out on receipt of a clear command and all registers are cleared during the read-out cycle. The numbers stored in the A register are in the ONE's complement form except that the partial products generated during multiplication are stored as magnitude plus sign. However, upon completion of

the multiplication operations the product, when negative, is transformed to the ONE's complement form. On read out, negative numbers are converted to the magnitude plus sign representation by complementing the 8 least significant bits of the word. With this logic the operations of addition and subtraction may be intermixed, but where a series of operations includes multiplication only one multiplication can be included and that must occur as the first operation.

4.1 Adder/Subtracter Section

The adder/subtracter section is composed of the full adder circuit, the A register, the B register and the input register. Addition is performed by adding the contents of the B register (that is the 9 least significant word bits) serially to the contents of the A register. The sum is stored in the A register which also serves as an accumulator. Subtraction is performed by first complementing the subtrahend as it is transferred into the B register and then proceeding as for addition. Negative numbers are transformed into ONE's complement form by sensing the presence of the sign bit as the word is entered into the input register and complementing the number during transfer to the B register.

Complementing is performed with the exclusive OR circuit by connecting one input to a controllable source of ONE's such as the output of a control flip flop. When the control flip flop is in the reset state the output of the exclusive OR circuit is the same as the input. When the flip flop is in the set state the output of the exclusive OR circuit is the complement of the input.

There are two complementers in the connecting path between the input and B registers. One is under control of the sign flip flop, the other is under control of the subtraction complement flip flop, CCOM, which results in double complementing for a negative subtrahend.

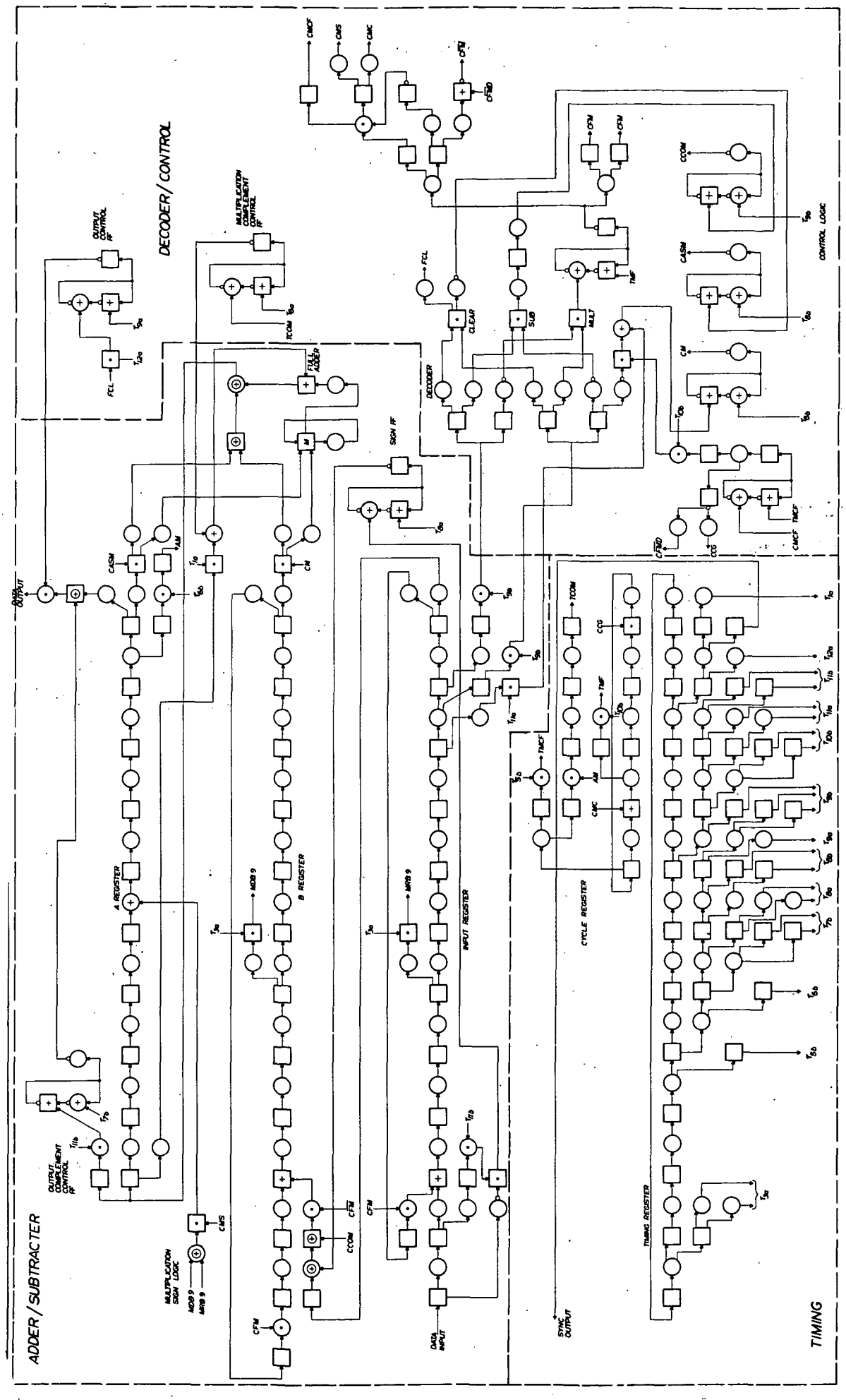


Fig. 32 Logic Diagram: All-Magnetic Arithmetic Unit

Because of the use of the ONE's complement a ONE is required to be added to the contents of the A register when an overflow bit occurs in the 10th word bit position. This is the end-around-carry requirement associated with the ONE's complement representation of negative numbers. The over flow bit is gated by τ_{1c} into the second exclusive OR of the full adder where it is added to the contents of the A register. This takes an extra word cycle so that a blank word is required to be input following each number added to or subtracted from the accumulator.

The length of the A register is ten stages long. The gate stage and the full adder stage provide the extra two stages required for storing a 12 bit word. The length of the B register and the transfer branch from the input register is 12 stages long so that proper alignment is preserved between corresponding bits of words in the A and B registers. In addition to the two complementers the transfer branch contains a gate circuit for control of word transfer into the B register which is inhibited during multiplication.

Because the form of negative numbers stored in the A register is the ONE's complement they must be converted to magnitude and sign for output. This is accomplished by an exclusive-OR complementer and the complement control flip flop which is set by gating the sign bit in the A register each word cycle. The output of the complementer is gated so that an output occurs only when the output control flip flop is set.

4.2 Decoder/Control Section

The decoder is used to decode the two function bits for control of the arithmetic operations according to the function codes listed in Table 4. The min terms required for decoding each function are also given. The complements for the two function bits are formed by negation circuits which together with three gates form the required min terms. The add function is not decoded as the control logic provides for execution of this function in

Table 4 Function Codes for All-Magnetic Arithmetic Unit

Function Code 2^{11}	Function Code 2^{10}	Function	Min Term
0	0	Add	$2^{\overline{11}} \cdot 2^{\overline{10}}$
0	1	Subtract	$2^{\overline{11}} \cdot 2^{10}$
1	0	Multiply	$2^{11} \cdot 2^{\overline{10}}$
1	1	Read/Clear	$2^{11} \cdot 2^{10}$

the absence of the other commands. Thus the absence of an input word results in adding ZERO's which leaves the number stored in the A register unchanged.

The function code associated with a word determines the operation to be performed on the next word entered. The two function bits are decoded at the end of the cycle in which a word is transferred into the B register. However, partial decoding of the most significant function bit occurs one cycle earlier so that complementing of negative numbers in the transfer branch between the input and B registers is inhibited during the multiplication and clear operations.

The operations required for execution of the arithmetic functions are controlled by the seven control flip flops and the decoder output signals which set the appropriate flip flops. These flip flops provide the following control signals: (1) Output Gate, (2) Multipliplication Complement, (3) CFM, for the recirculation gates of the input and B registers, (4) CCOM, for subtraction complement, (5) CASM, for the A register gate, (6) CM, for the B register gate and, (7) $\overline{\text{CFMD}}$, for the transfer gate into the B register.

With the exeption of the CFM and $\overline{\text{CFMD}}$ flip flops, all are reset late in each word cycle by a timing clock pulse. The CFM and $\overline{\text{CFMD}}$ flip flops are used for control of the multiplication operation which takes five word cycles and therefore are reset under control of the cycle counter. Two additional control flip flops, the sign flip flop and the output complement flip flop are set by the sign bit and reset by a timing clock each word cycle.

4.3 Timing

The timing for the all-magnetic arithmetic unit is provided by two ring counters. One 12 stages long, the timing register, divides each word cycle into 24 time slots. The clock signals required for control are formed using fan-out circuits appended to this register. A second ring counter, the cycle register, is 5 stages long and is used in conjunction with the timing register to provide the additional timing signals required for the multiplication cycle which is five-word cycles long. These signals are the TMCF, TMF, and TCOM signals formed by gating the output of the cycle register and the appropriate clock pulse from the timing register. The cycle register, unlike the timing register, does not operate continuously. It is activated by an output from the multiplication decoder gate which inserts a ONE into the cycle register via the CMC input, and enables the recirculation gate via the CCG signal to maintain circulation of the ONE for 5 cycles after which the gate is opened clearing the register.

4.4 Multiplication

Multiplication is the most complex of the three arithmetic operations implemented in this design. The multiplication is performed by adding the partial products formed by multiplying the multiplicand by the weighted value of each digit of the multiplier.[4] This is accomplished by first enter-

4 Physter, Montgomery, Jr., "Logical Design of Digital Computers," John Wiley & Sons, Inc., N.Y., 1958.

ing into the input register a word containing the multiplicand and the function code for multiply. The most significant bit of the function code inhibits the setting of the sign flip flop. This prevents complementing the multiplicand if it is negative. A second word is entered into the input register and the first is transferred into the B register during the next word cycle. The second word contains the multiplier and the function code for add. As the first word is transferred out of the input register the function code for multiply is decoded to form the control signals CFM, CMS, CMC and $\overline{\text{CFM}}$ and to set the CFM flip flop. These control signals disable the transfer gate $\overline{\text{CFM}}$ between the input register and the B register and the transfer gate CM between the B register and the full adder. The recirculation gates in the input and B registers, CFM, are enabled to recirculate the numbers set in these registers. The lengths of the recirculation path for the B register is 13 stages long to "shift left" which provides the weighting for each digit of the multiplier. The length of the recirculation path of the input register is 11 stages long providing a "shift right" of the multiplier which moves the next higher digit into the least significant digit position in the input register. It is the least significant bit position which controls the CM gate to add the (shifted) multiplicand to the A register. After three cycles of conditional adding and shifting, the recirculation gates are disabled by the resetting of the CM flip flop and the final conditional add is performed in the fourth cycle. Negative products are complemented in the fifth cycle under control of the multiplication control flip flop which is set by TCOM and supplies ONE's to the carry input of the second exclusive OR circuit of the full adder which serves as the complementer for the A register. At the end of the fifth cycle, the $\overline{\text{CFMD}}$ flip flop is reset by TMCF disabling the recirculation gate in the cycle register thereby clearing it.

The product sign is determined, using the exclusive OR and gate circuits forming the multiplication sign logic, in the first multiplication cycle by gating the sign bits of the multiplicand and multiplier - MDB9 and

MRB9 - into the exclusive OR circuit. As is seen from Table 5, in which the Truth Tables for the multiplication sign and the exclusive-OR are compared, the exclusive OR directly forms the product sign. The output from the exclusive-OR is gated into the sign bit position in the A register by CMS.

The multiplication complement control flip flop is controlled by the product sign bit. The sign bit is gated out of the A register each word cycle forming AM. For negative products the gate in the TCOM branch of the cycle register is enabled by AM for one clock phase. This gates the TCOM pulse, which occurs in coincidence with AM in the fourth cycle to set the multiplication complement control flip flop for the fifth cycle.

Table 5 Comparison of Multiplication Sign and Exclusive-OR Truth Tables

Multiplication Sign

Multiplicand		Multiplier		Product	
+	(0)	+	(0)	+	(0)
-	(1)	+	(0)	-	(1)
+	(0)	-	(1)	-	(1)
-	(1)	-	(1)	+	(0)

Exclusive -OR

X	Y	X⊕Y
0	0	0
1	0	1
0	1	1
1	1	0

5.0 FABRICATION OF CIRCUITS FOR ALL-MAGNETIC ARITHMETIC UNIT

The plated conductor process which was intended to be used for the fabrication of the magnetic logic circuits to be developed under this contract was the process developed under Contract NAS1-9836.[5] After a number of unsuccessful attempts to fabricate circuits, the insulation methods of this process had to be abandoned as unworkable. The insulation process was found to be too difficult to control with the result that the yield obtained was insufficient to permit fabrication of the required circuits. An alternate insulating process was finally developed that had a sufficiently high yield to permit fabrication of the required circuits. However, this development came too late in the contract to fabricate and evaluate all of the new circuits. This process utilized printed circuit technology to form the conductor patterns on insulated sheets which were bonded to both sides of the logic structures. Insulating tubes were bonded between these sheets where conductors were required to connect the top conductor pattern to the bottom conductor pattern.

5.1 Coated Insulation

The method of insulation which was used in the previously developed process was based on coating the magnetic logic structures, which are covered on three sides by an eddy current shield, with a layer of Pyre

5 Heckler, C.H., Jr. and Bhiwandker, N.C., "Batch Fabrication Process Development for Ferrite Logic Conductors," Final Report NAS1-9836, Ampex Corporation, Redwood City, CA, February, 1972. Also available as NASA CR-111983.

ML,* a polyimide insulating varnish. Due to a combination of the effects of surface tension and shrinkage of the insulation during curing, the edges of the structures were only partially covered by each coat of Pyre ML and the insulation over the edge areas covered was very thin. To fully cover the edges required 6 or more coatings with Pyre ML. However, even with less than 6 coats the insulation build-up on other parts of the structures was increased to a thickness where the surfaces became rough and were no longer flat.

A minimum thickness was required to prevent shorting between conductors, applied later in the process, and the eddy current shield. Because of the inability to control the coverage on the edges of the structures during each coating, the minimum thickness could not be determined by controlling the number of coats of insulation. A special test was used to insure that the thickness of the insulation was sufficient to prevent shorts in later processing since resistance measurements were only effective in detecting holes in the insulation. The test consisted of immersing each unit, after being insulated with six coatings of Pyre ML in a copper sulfate solution and testing for current conduction to the eddy current shield. Units which passed this test were processed further, those which failed the test were recoated and retested. The units which passed this test did not develop shorts in later processing. However, the excessive build-up of insulation caused other problems which adversely effected the writing of conductor patterns with the gold resonate. The roughness and lack of flatness of the insulated surface of the structures prevented the circuit sheets from being completely bonded to the structures. Gaps occurred between the circuit sheet and the structure in areas where conductors had to be written. The irregular surface caused variations in the width and thickness of the written gold resonate lines and the more severe surface irregularities produced

* Trademark E.I. duPont de Nemours & Co.

discontinuities in these lines. The gaps and the severe surface irregularities were able to be filled in using a Dow Corning high temperature epoxy, D.E.N. 438. The narrow conductor lines were able to be rewritten and a part of the over-width conductors were stopped off with a plating resist. All defects had to be detected and corrected prior to plating as repairs were possible only in a limited number of cases after an initial plating.

The combination of the problems associated with the insulation, the requirement that all defects be detected and repaired before initial plating of conductors, and the difficulty of detecting defects by optical inspection resulted in a yield of less than 5% after an extensive effort at improving the insulating process. Therefore, the insulating process involving coating with Pyre ML had to be abandoned.

5.2 Printed Circuit Insulation Process

The printed circuit process developed to replace the unsuccessful Pyre ML insulation process, uses 2 Mil Kapton* printed circuit sheets (with etched conductor patterns and etched holes) which are bonded to the top and bottom surfaces of a pair of single stage logic structures. The patterns for the drive conductor printed circuit sheets are shown in Figs. 33 and 34. The hole pattern for the drive conductor sheets is shown in Fig. 35. In Figs. 36 and 37 are shown the patterns for the coupling loop printed circuit sheets.

Insulated paths between the top and bottom printed circuit sheets are provided by Pyre ML tubes which pass through the etched holes in the sheets. The tubes are bonded, at their ends, to the Kapton sheets with the D.E.N. 438** high temperature epoxy. The conductor patterns of the two sheets are interconnected by conductor lines written through these tubes

* Trademark: E.I. duPont de Nemours & Co
** Trademark: Dow Corning Corp.

Fig. 33 Drive Conductor Pattern for Top Printed Circuit Sheets of 1-Stage All-Magnetic Logic Circuit

Fig. 34 Drive Conductor Pattern for Bottom Printed Circuit Sheets of 1-Stage All Magnetic Logic Circuit

Fig. 35 Hole Pattern for Printed Circuit Sheets of 1-Stage All Magnetic Logic Circuit

Fig. 36 Coupling Loop Pattern for Top Printed Circuit Sheet of 1-stage All-Magnetic Logic Circuit

Fig. 37 Coupling Loop Pattern for Bottom Printed Circuit Sheet of 1-Stage All-Magnetic Logic Circuit

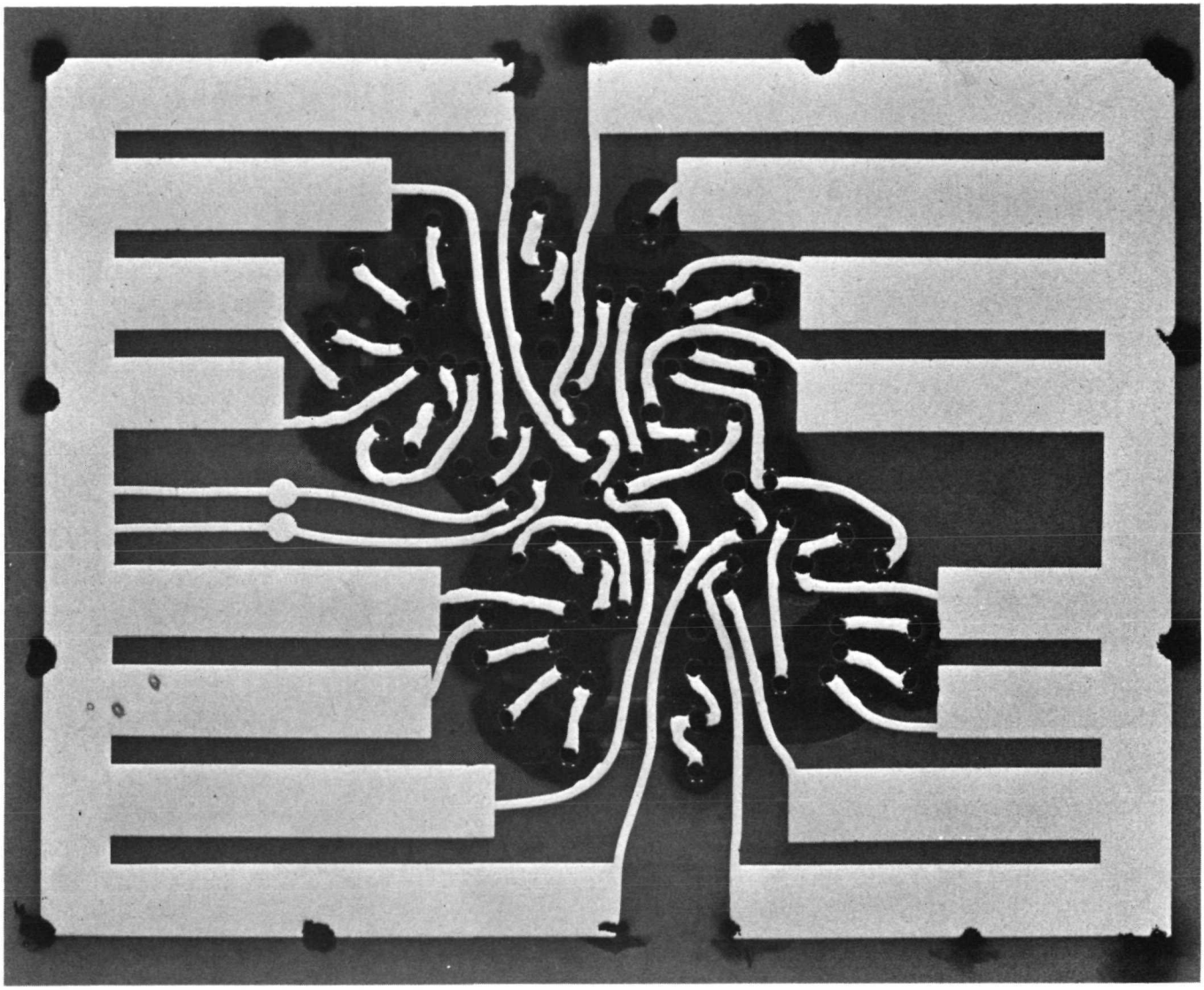


Fig. 38 Photograph of Single Stage Circuit With Plated Drive Conductors: Bottom View

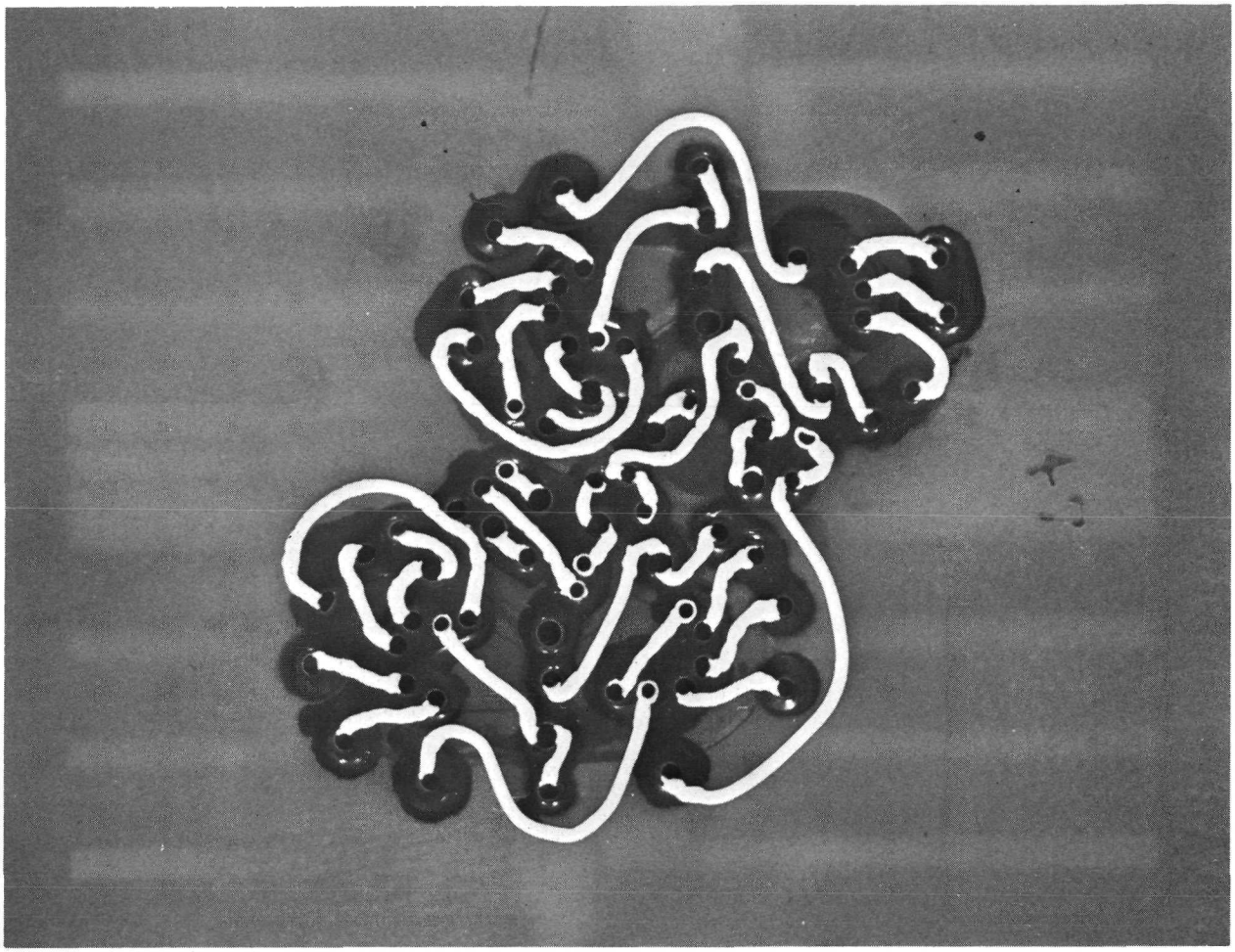


Fig. 39 Photograph of Single Stage Circuit With Plated Drive Conductors: Bottom View

with the mechanized writing head using gold resonate ink to form the completed drive conductor and coupling loop patterns. The joint-free conductors are formed, as before, by copper plating to a thickness of 0.002 to 0.004 inches. Figs. 38 and 39 are photographs of the top and bottom of a logic circuit with a completed drive conductor winding showing how the joint-free conductors are formed through the tubes.

The Kapton sheets and Pyre ML tubes epoxyed in place provide full insulation between the drive conductors and the eddy current shield and between the drive conductors and the coupling loops. The flat, smooth surfaces of the Kapton sheets and Pyre ML tubes are easily written on with the mechanized writing head and the patterns written are inspectable to insure that conductor lines are continuous. This has resulted in a minimum of opens in the conductor pattern after conversion of the gold resonate to gold in a 300°C firing. The low incidence of opens has significantly increased the yield of the overall process. The remaining cause for circuits not being successfully processed is poor adhesion of the initial gold metalization to the Kapton circuit sheets. This results in peeling of the conductor pattern during processing. A test to identify circuit sheets with poor adhesion before bonding to the structures has reduced the number of circuits failing from this cause to a tolerable level.

The number of circuits fabricated by this process has been too small to arrive at a reliable yield figure. However, the yield has steadily improved and is currently running about 80%.

6.0 CONCLUSIONS AND RECOMMENDATIONS

The basic logic functions, OR, AND and NEGATION required for general logic can be realized with the controlled threshold class of all-magnetic logic circuits. Additional logic functions, NOR, NAND and MAJORITY, are realizable in a single element which aides in the simplification of system logic designs. The more complex logic functions such as flip flops, full adders, decoders, etc. are formed by combining basic function circuits. A logic design for a serial arithmetic unit has been made demonstrating the capability of the all-magnetic logic circuits to provide the logic, timing and control functions for complex systems. The arithmetic unit provides for the addition and subtraction of 8-bit numbers and the multiplication of 2-4 bit numbers.

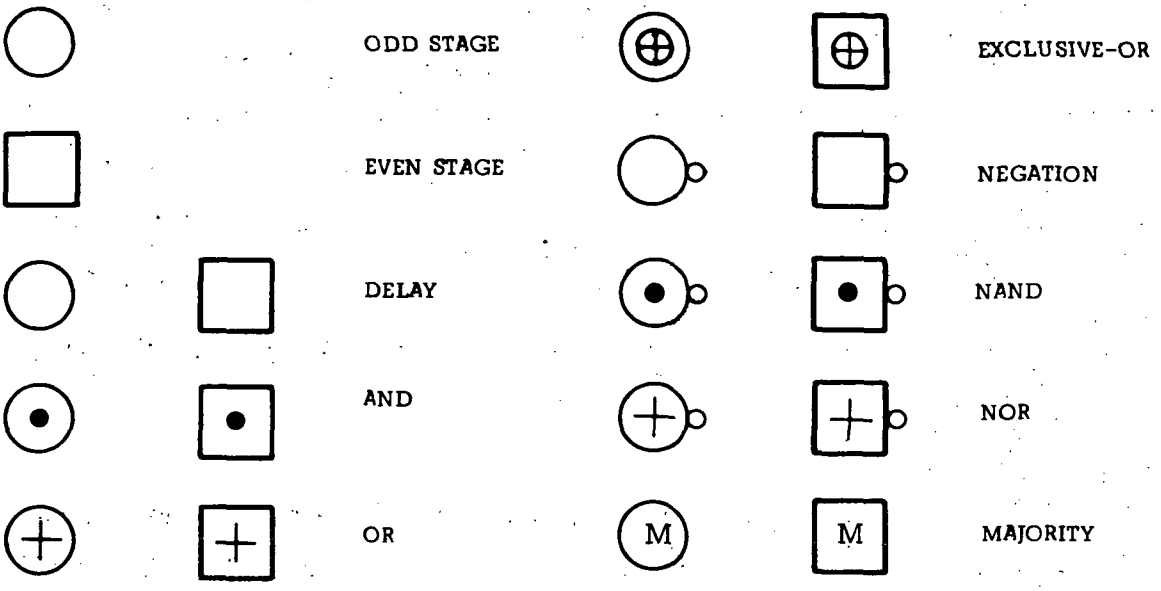
The change in the insulation process made during this contract has overcome the reproducibility and low yield problems associated with the earlier insulation process used in fabricating the all-magnetic logic circuits. This has been accomplished without reducing the ultra-high reliability of these circuits.

The problems associated with fabrication of circuits using single stage logic structures are significantly less than when using multi-stage logic structures, with a resultant increase in yield. In future work only single stage circuits should be used to take advantage of this higher yield. The logic blocks would then be formed by joining single stage circuits together prior to final plating of the drive conductors. Application of all of the coupling loops would be made after completion of the plating of the drive conductors.

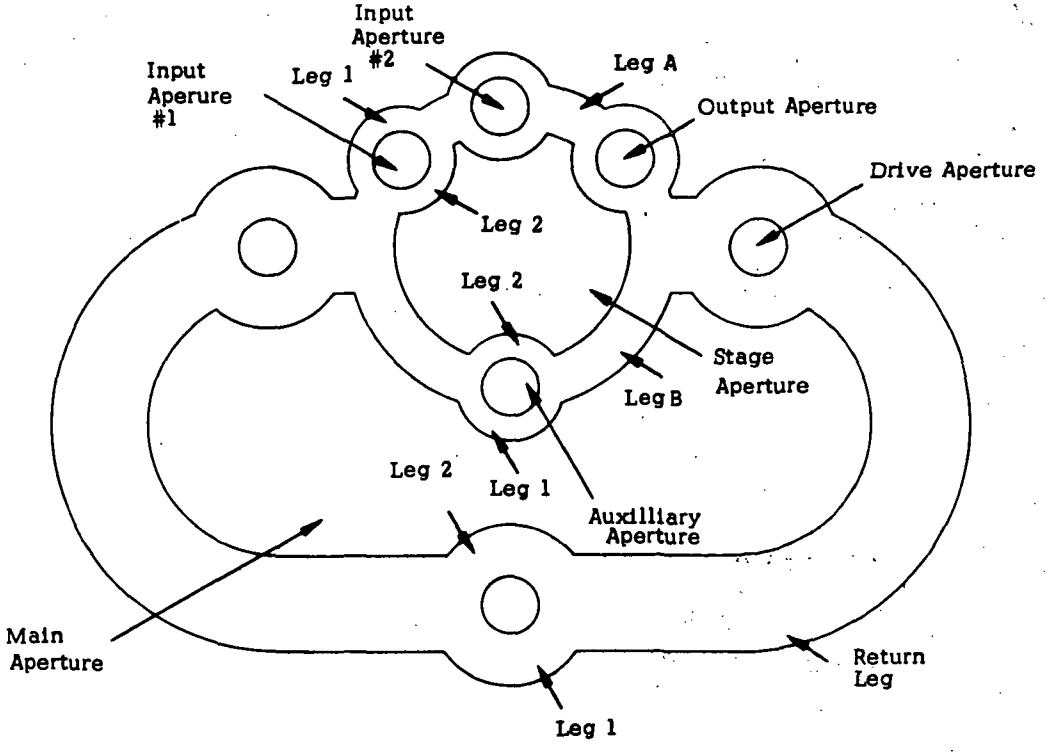
The new theta structure developed during this contract is much smaller than the present single stage structure and capable of being manufactured to closer tolerances. This structure should be evaluated further to determine its suitability for replacement of the present single stage structure. Circuits using the six-clock logic scheme have had improved operating performance over that obtained with the four-clock logic scheme. Additional circuits should be evaluated to determine the degree of improvement attainable for all of the basic logic functions using this scheme.

The process for the fabrication of all-magnetic logic circuits has been implemented only for making small numbers of circuits. Therefore it is a mixture of batch, semi-automatic and hand processing steps, even though many of these process steps are capable of being automated. Increased use of batch and automatic processing is needed to fabricate larger numbers of circuits and to reduce the cost of fabricating these circuits.

APPENDIX A: LOGIC SYMBOLS



APPENDIX B: LOGIC STRUCTURE PATH IDENTIFICATION



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