DESIGN, PROCESSING, AND TESTING OF LSI ARRAYS FOR SPACE STATION

BY

W. R. LILE AND R. J. HOLLINGSWORTH

QUARTERLY TECHNICAL REPORT NO. 8

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DESIGN, PROCESSING, AND TESTING OF LSI ARRAYS
FOR SPACE STATION

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SUMMARY

The object of this research effort is a low-power, high-performance, metal-oxide-semiconductor (MOS) 256-bit Random Access Memory (RAM). Technological achievements comprise computer simulations that accurately predict performance; aluminum-gate COS/MOS devices including a 256-bit RAM with current sensing; and a silicon-gate process that is being used in the construction of a 256-bit RAM with voltage sensing. The Si-gate process increases speed by reducing the overlap capacitance between gate and source-drain, thus reducing the crossover capacitance and allowing shorter interconnections. The design of a Si-gate RAM, which is pin-for-pin compatible with an RCA bulk silicon COS/MOS memory (type TA 5974), is discussed in full.

The evaluation of the fabricated devices is accomplished by using any of three test vehicles. The Integrated Circuit Tester (ICT) is limited to dc evaluation, but the diagnostics and data collecting are under computer control. The Silicon-on-Sapphire Memory Evaluator (SOS-ME, previously called SOS Memory Exerciser) measures power supply drain and performs a minimum number of tests to establish operation of the memory devices. The Macrodata MD-100 is a microprogrammable tester which has capabilities of extensive testing at speeds up to 5 MHz.

Beam-lead technology has been successfully integrated with SOS technology to make a simple device with beam leads. This device and the scribing are discussed.

I. INTRODUCTION

RCA has pioneered in the field of silicon-on-sapphire (SOS) integrated circuits for several years and has developed considerable background in this area, ranging from basic material studies and advanced bipolar and MOS device concepts to the realization of complex MOS integrated-circuit arrays of extremely high-performance capabilities. This unique approach to MOS arrays enables the realization of the full high-speed potential of the MOS device which is comparable to the npn bipolar transistor commonly employed in monolithic integrated circuits.

Silicon-on-sapphire is expected to compete with bipolar memory technologies in the area of static high-performance buffer and cache memories where fast access and cycle times are required. MOS/SOS memories, because of their inherent self-isolating micropower characteristics, can achieve higher packing densities, and therefore potentially lower cost, than present TTL bipolar memory arrays. The 256-word COS/SOS random-access memory described here was developed for use as a high-performance, micropower LSI memory array in space stations.

During this year's effort, the 256-word memory chip was used as the basic vehicle for applying Si-gate techniques to COS/SOS technology. Our emphasis was on high density, low power, high speed, and a process adaptable to low-cost mass production. In addition, we initiated a program to develop a beam-lead system for the basic COS/SOS technology. Our ultimate goal for this research is a Si-gate, sealed-junction, beam-lead COS/SOS technology that is compatible with the environmental conditions required for space and military applications.

In this report, the design of a Si-gate 256-word × 1-bit RAM is discussed. The particular memory design follows along lines of the original concept (ref. 1), with modifications to the decoder (ref. 2) and design changes from current to voltage sense as discussed in this report. The original memory design did not meet the requirements of speed and of proper interfacing using voltage sense. Simulation of the circuitry and expected performance of the modified design are described.

Beam-lead technology was applied to SOS circuits, and samples of beams were successfully fabricated. Attempts of laser scribing of the sapphire substrate were equally successful.

II. WAFER TESTING

A. Methods of Testing

The Integrated Circuit Facility here at RCA Laboratories has a dc test machine that operates under computer control. Since the 256-bit RAM has a dynamic address decoder, it could not be tested for storage integrity with this machine, but the protective diodes can be tested before dicing the wafer into chips.

A test device for evaluating the unit under actual operating conditions was built specifically for this 256-bit RAM. It cannot test the protective diodes, but can provide functional testing using simple patterns to evaluate the ability of the cell to retain information and to determine the cell's resistance to disturbs during both Read and Write. This test machine is referred to as the SOS Memory-Evaluator (SOS-ME).

A third test machine, the Macrodata MD-100, was placed in operation recently. This machine, like the SOS-ME, will not evaluate the dc parameters of the memory; however, it is an extremely flexible machine with an excellent repertoire of test subroutines. The MD-100 has a microprogrammable system that can test any type of memory device and includes a RAM that lets the operator create special programs for testing new devices.

B. SOS-ME Testing

The SOS-ME is capable of testing both wafers and packaged units. It can evaluate the memory by using three basic test patterns consisting of a uniform field and an alternating field, and a field with the diagonal information inverted. The inverse of the data used in these patterns includes additional test patterns used to ascertain the integrity of the memory devices.

The SOS-ME only runs at a 200-kHz clock rate; but the width and position of the sense strobe are variable, thus enabling a limit to be placed on access time.

Access time is measured directly with an oscilloscope. It is defined as the time between the 50% points of the leading edges of Chip Select (CS) and the sense amplifier output, minus the delay of the sense amplifier. A field of "1's" is written into the memory-under-test (MUT), and the memory is then continuously read while the signals are displayed on the oscilloscope. Access time is the time required for the slowest cell

in the memory to respond. Typical times are 70 to 90 nsec. Access time must be measured using only packaged devices in order to eliminate reflections on the long cable used for wafer probing. When wafers are probed, access time is unimportant in an absolute sense, as the established criterion is simply: — Will the memory work? The access time, however, must be less than 500 nsec, or the memory is considered to have some gross fault and is rejected.

To minimize the possibility of damaging a wafer and because the technology of fabricating the protective diodes has been largely perfected, the usual testing on the Integrated Circuit Tester is being omitted. The diodes are tested indirectly, however. When a leakage current measurement is made on the SOS-ME, excessive power supply drain can be attributed to the diodes if the current changes when the address lines are manually switched from "1" to "0".

Power supply drain is measured under static and dynamic operating conditions. In the static mode a uniform field of "1's" is written into the memory. All address lines are reset to "0". The leakage current (power supply drain) is Read under these uniform conditions. The same thing is repeated for a field of "0's". Dynamic power supply drain is measured for the same conditions except that the addresses cannot now be set to a given condition.

Typical dc supply current drains for the static measurements are in the 50-μA range. This indicates the memory device has a static dissipation of 2 μW per bit. When operating at 200 kHz, the typical supply current is 200 μA. This indicates a total power dissipation of 13 mW/MHz.

<div align="center">C. MD-100 Memory Testing</div>

As previously mentioned, the flexibility afforded by the microprogrammable MD-100 enables testing of any type of memory device. Cycle time is variable externally down to 200 nsec.

In addition to the test programs furnished with the MD-100, the operator can write programs and store them in the RAM. Although this storage is temporary, the operator can incorporate the simple patterns of the SOS-ME into the MD-100 routines. This testing mode further verifies basic testing results with the SOS-ME and makes it unnecessary to wafer probe with the SOS-ME.

Since the MD-100 is not equipped to measure the power supply current to a device, the SOS-ME must still be used to partially evaluate packaged units. However, the MD-100 is now testing wafers using an automatic index table and extremely rigorous patterns. Test time for a 60-chip wafer is about 4 minutes.

III. SILICON-GATE RAM DESIGN

The redesign of the 256-word $\times$ 1-bit static RAM utilizing the Si-gate SOS COS/MOS process has been undertaken. This memory chip is pin-for-pin compatible with the RCA COS/MOS (i.e., bulk silicon COS/MOS) 256-word $\times$ 1-bit RAM, developmental type TA 5974. This memory contains the following features:

(1). Eight addresses (A_0-A_7): All inputs are COS/MOS logic levels; i.e., high logic level $\cong$ V_{CC} (typically $\sim$ 10 V) and low logic level $\cong$ Ground (held at 0 V). All address inputs contain input protective devices to prevent static electrical discharges from damaging input gate oxides.

(2) V_{CC} supply: This is a COS/MOS voltage supply, typically 10 V above ground (V_{DD}).

(3) Ground (V_{DD}) supply: This is referenced at 0 V for the V_{CC} supply and for all inputs and outputs.

(4) Data In (D_{in}): This input is used to provide the 1-bit word that is to be written into a particular memory location during the Write operation. This input accepts a COS/MOS high or low logic level. It is protected against static electrical discharges by an input protective device.

(5) Data Out (D_{out}) and its logical complement ($\overline{D_{out}}$): These outputs are voltage level outputs, indicating a high or low COS/MOS 1-bit word at a particular memory address during the Read condition. It should be noted that the data output (and its logical complement) is a COS/MOS voltage output used to directly drive COS/MOS circuits. D_{out} and $\overline{D_{out}}$, are also designed to be OR-tied to other D_{out} and $\overline{D_{out}}$, respectively, of similar memory chips so as to expand a group of memory chips into a memory system.

(6) Write-Enable Input (WE): This WE input is used to choose between the Read or the Write operation. This input contains an input protective device as do all of the inputs. The WE input accepts a COS/MOS high or low logic level for operation designation.

(7) Chip Select Input (CS): The CS input is used to enable the chip for the Read or Write operation. This input accepts a COS/MOS high or low logic level such that a high level disables the memory in an uncharged static state. The low-level input enables the memory into a Read or Write operation (discussed later). This input is protected in the same manner as the others.

The Si-gate SOS/COS/MOS design will mirror the features of the RCA COS/MOS TA 5974. The memory will be packaged in a 16-pin DIP and will be designated as TA 6366.

The Si-gate design was chosen over the Al-gate process previously used for the following reasons:

(1) Higher performance because of reduced gate overlap capacitance, reduced crossover capacitance, and shorter interconnections.

(2) Self-alignment feature, improved mesa edge coverage, and smaller layout areas producing higher yields.

(3) A basically simpler device structure and cleaner processing yields lower device leakage currents.

The Si-gate process that is used on the SOS COS/MOS RAM incorporates a double epitaxial growth of p-type islands and n-type islands onto which the circuits are fabricated. The memory chip consists of both p- and n-type enhancement MOS transistors. The nominal threshold values for the devices are: p-type threshold = V_{TP} = 1.5 volts and the n-type threshold = V_{TN} = 2.0 volts. The polysilicon gates and interconnections are degenerately doped p^+ over the entire chip with a resulting sheet resistance of ~ 70 $\Omega/\square$. All metal lines are aluminum. The choice of the double epitaxial process with the particular doping levels and resultant threshold voltages was arrived at from a highly successful and reliable process evolution of SOS at RCA Laboratories.

The chip is organized as a 256-word X 1-bit memory which is conveniently reduced to a matrix of static memory cells: 16 rows by 16 columns. These rows and columns, in turn, are addressed by two distinct decoding circuits: one for the rows and one for the columns. The cells are accessed by two digit lines, which are oriented with the columns of the memory chip. These digit lines are used to read from and write into a particular cell which is chosen by the decoding circuitry. These digit lines are gated to the Read/Write circuitry by the column decoder. The Read/Write circuitry performs the particular operation upon the digit lines such that, through proper addressing, a memory cell can be written into or read from. The outputs from the Read/Write circuitry for the Read condition are inputted to a sense amplifier (on the chip), which produces a high or low COS/MOS logic level output for the word read from a chosen cell. This can be best observed in the block diagram of Fig. 1.

The basic static memory cell used in the memory chip design is a six-transistor flip-flop circuit as shown in Fig. 2. The P1 and N1 transistors comprise the flip-flop memory cell. The N2 transistors are used to access the memory cell to the two digit lines. Notice that the N2 devices are gated by the word line which is the output of
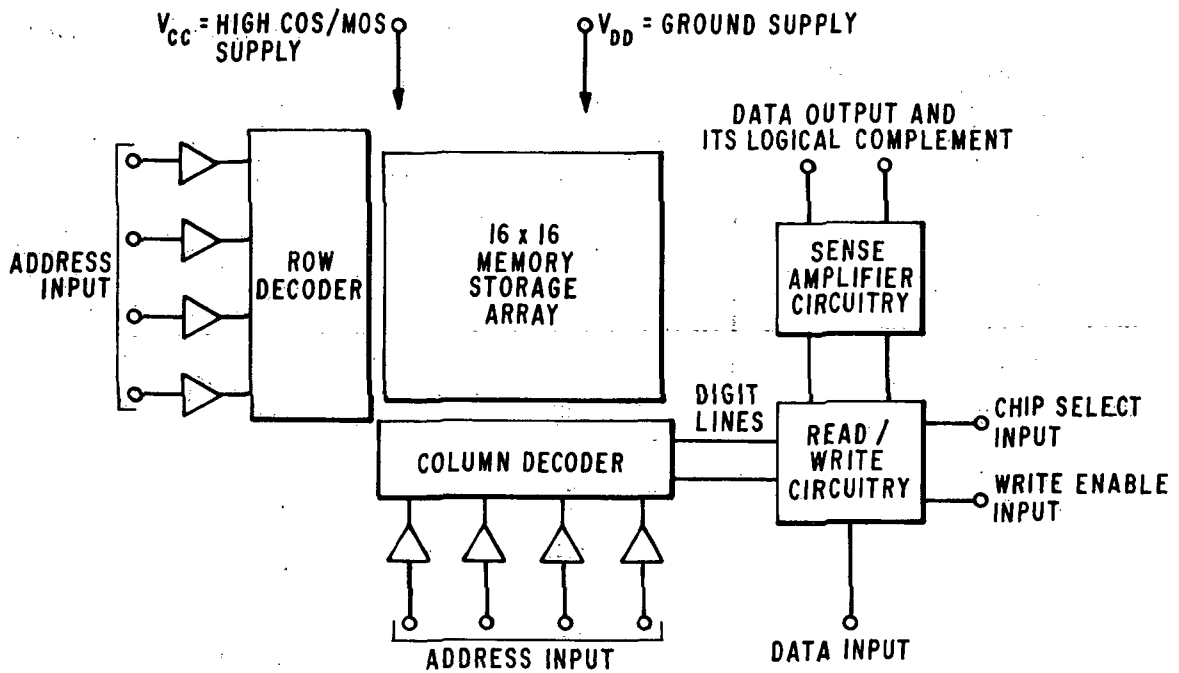
Figure 1. Silicon-gate 256-word × 1-bit SOS COS/MOS RAM block diagram.
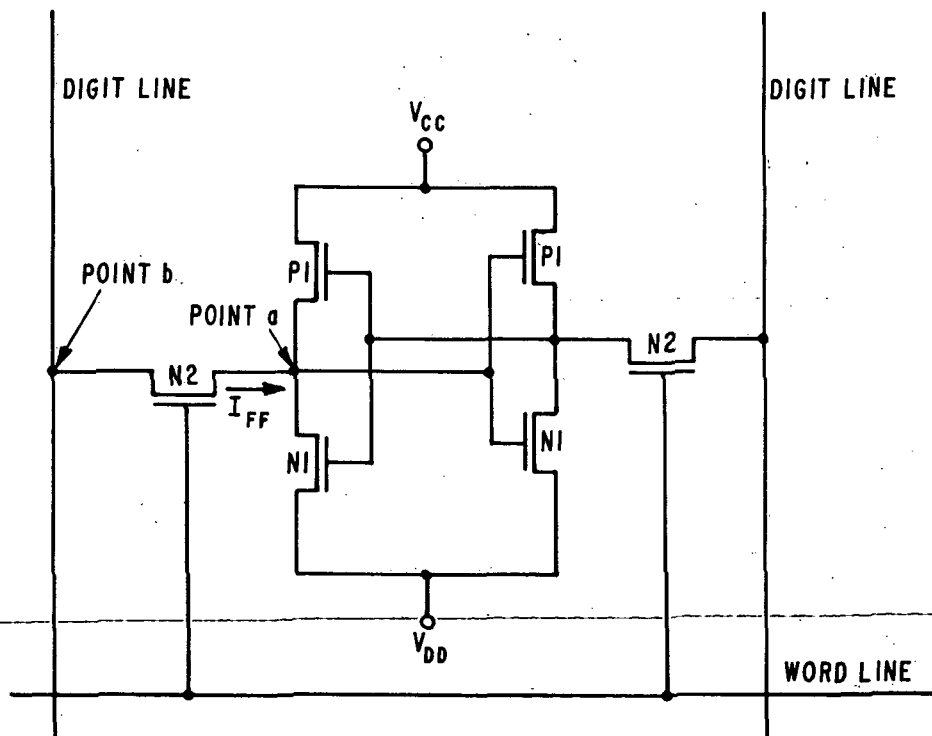
Figure 2. Basic 6-transistor memory cell.

the row decoding circuitry. The two-digit lines are thus gated to the cell by the appropriate high COS/MOS logic level on the word line.

The design considerations placed upon the memory cell require an analysis of each particular state of the cell during the memory-chip operation. The primary design criterion involves the insurance that the memory cell will statically perform its functions. To this end, the plot of Fig. 3 is referred to. This plot shows the transfer characteristic of the flip-flop memory cell of Fig. 2 at point a. The current is the current

Figure 3.   Memory cell operational characteristics.

into that node, and the voltage is the voltage at that node with reference to V_{DD}. It should be recognized that this transfer function only describes the P1 and N1 devices of Fig. 2. The various operations can be seen as follows:

(1) No operation: No operation requires that through the decoding circuitry there be no address selection. The net result is that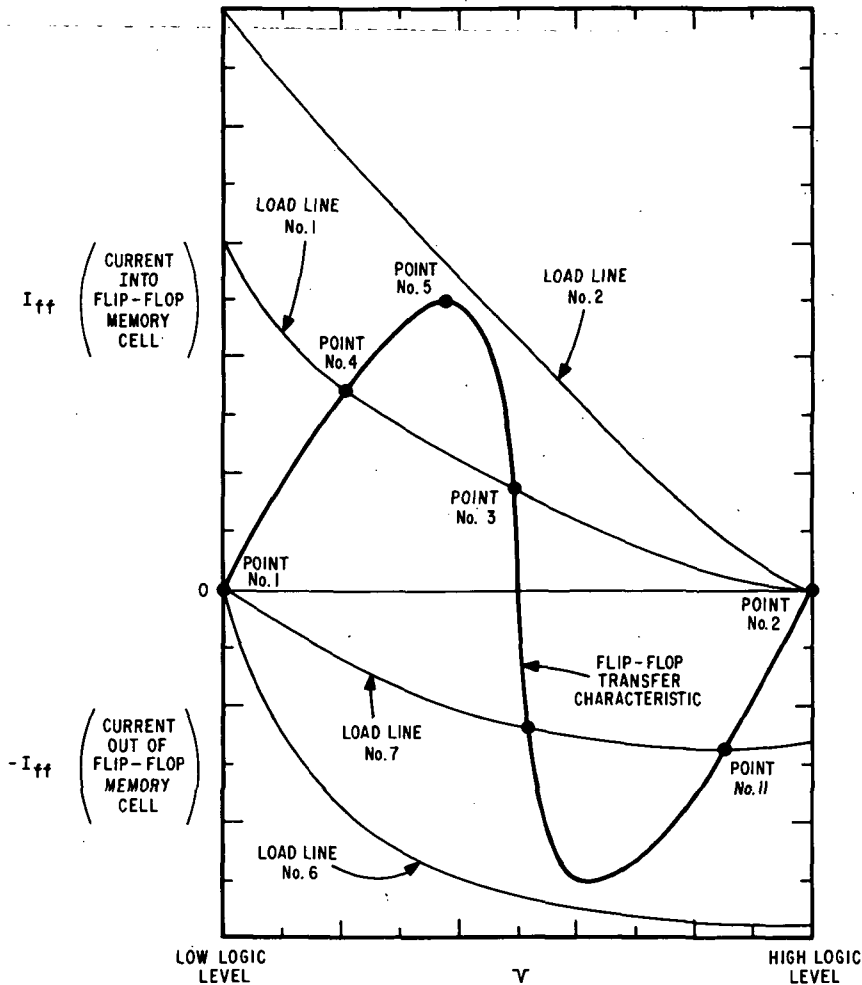 the word line is held at a low logic level and the N2 devices of Fig. 2 are held OFF, regardless of the state of the two digit lines. Thus, point a of Fig. 2 will remain at either V_{CC} or V_{DD}, depending upon the state of the flip-flop cell. From Fig. 3 it can be seen that there is no current flowing, and the cell is either at point 1 or point 2 of Fig. 3.

(2) Read: The Read state for a selected cell requires that the word line assume a high logic state. Thus, point a of Fig. 2 is accessed to point b through the N2 device. The state of the flip-flop can now be sensed by the digit lines. A requirement of the memory cell follows. The digit lines must be pre-charged to V_{CC} prior to a Read or Write operation. With this restriction, the design criteria for read operation are:

(a) A high logic level at point a of Fig. 2 results in the transfer character-istic of Fig. 3 being at point 2. The load line for the read state is simply the N2 device of Fig. 2 in series with a device of the column decode [see Fig. 4(c)] and an equivalent input capacitance associated with the Read/Write circuitry and sense amplifier. With the requirement that the digit lines be precharged to V_{CC} before the Read operation, the resulting load line for reading a high logic level on point a of Fig. 2 is simply the region near point 2 of Fig. 3. Thus, reading a high logic level at point a of Fig. 2 requires that the digit lines and Read/Write circuitry input be precharged to V_{CC}.

(b) A low logic level at point a of Fig. 2 will be analyzed by the load line 1 of Fig. 3. This load line includes the N2 device in series with the column decoder gate (see Fig. 4) and the input capacitance to the Read/Write circuitry. This transfer plot of load line 1 is for point a of Fig. 2. The design criterion thus requires an intersection of the flip-flop transfer curve with the Read load line 1. A nondestructive readout (NDRO) requires that load line 1 of Fig. 3 must intersect the the flip-flop transfer curve at points 2, 3, and 4. If this requirement is not realized, then a destructive Read will occur, as shown by load line 2 which displays the fact that point 1 will proceed along the flip-flop characteristic to point 5, "jump" to load line 2, and relax to point 2 of Fig. 3. This would yield a flipped cell and thus a destructive Read.
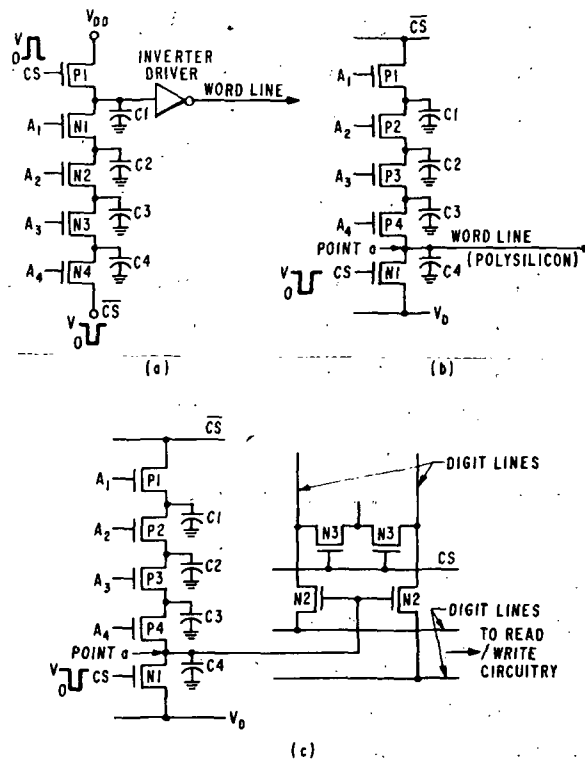
Figure 4. (a) Aluminum-gate RAM 2^N decoder; (b) silicon-gate RAM 2^N row decoder; (c) silicon-gate RAM 2^N column decoder.

In conclusion, the Read operation design criteria require that the devices and Read/Write and decoder circuitry be such that, with precharging of the digit lines, load line 1 be realized for nondestructive Read of a low logic level at point a of Fig. 2, and that precharging of digit lines and Read/Write circuitry yield relaxed stability of point a of Fig. 2 at a non-destructive Read of a high logic level.

(3) Write: Writing into a selected memory cell location requires that the word line assume a high logic state. This would turn the N2 devices of Fig. 2 ON and enable the digit lines to the two sides of the flip-flop. Therefore, point a is accessed to point b in Fig. 2. Writing is performed by proper selection of digit line states as follows:

(a) If we assume that point *a* contains a high logic level, then the Write operation will be determined by the level of point *b* of Fig. 2. If point *b* remains at the precharged high logic state, then the state of the selected cell remains the same. If a low logic state is placed upon point *b* (by the Read/Write circuitry), then the load line 6 of Fig. 3 will determine whether a proper Write operation will occur. This is the case if load line 6 does not intersect the negative portion of the flip-flop transfer characteristic. The cell (assumed at point 2) will flip by relaxing to point 1 by following the load line 6 of Fig. 3. If, however, the load line 7 results from the impedances of the decoder and Read/Write circuitry, then writing will not occur due to the intersection at point 11, which leaves the flip-flop in the high state.

(b) If we assume that point *a* contains a low logic level, then the write operation will be determined by the particular level at point *b* of Fig. 2. If point *b* is pulled down from its precharged high level to a low level, then point 1 of Fig. 3 will be maintained, and there is no switching of cell state. If, however, point *b* of Fig. 2 remains at a high logic level, then the load line 1 of Fig. 3 must be analyzed. This load line was that of the reading of a low state at point *a* of Fig. 2. This is due to the fact that the current-limiting properties of the load line that includes the N2 device of Fig. 2, the decoding gate, and the Read/Write circuitry are common to the reading of a low logic level at point *a* and to the writing of a high logic level into a previously low point *a* of Fig. 2. Thus, it can be seen that the constraints placed upon load line 1 of Fig. 2 during the Read operation have resulted in insufficient current for flipping the cell from a low logic level to a high logic level at point *a* of Fig. 2.

The Write operation is thus primarily determined by the ability of point *a* to be pulled "down" from a high level to a low level in Fig. 2. Due to constraints placed upon the read operation, a pulling "up" of point *a* from a low level to a high level is not sufficient for a proper Write operation. It should be noted at this point that the Read/Write circuitry during the Write condition will place opposite logic levels upon the two digit lines such that as the N2 devices turn ON for cell selection, the

Write operations outlined previously will act simultaneously to flip the cell of Fig. 2.

The cell layout can be seen in Fig. 5. The six-transistor flip-flop cell is 4.5 mils $\times$ 4.6 mils for an area of 20.7 mils^2. This is a significant reduction from the present Al-gate SOS COS/MOS 256-word $\times$ 1-bit RAM (i.e., TA 6266), which contains a six-transistor memory cell area of 30.5 mils^2. This 33% reduction in area is significant for the layout of 256 cells, namely, from the former 7808 mils^2 to the present 5299.2 mils^2. This decrease in memory cell area is not at the expense of viable Si-gate fabrication techniques. The design rules used in the layout have evolved from a reliable processing of large-scale integrated circuits using the Si-gate technology at RCA Laboratories.
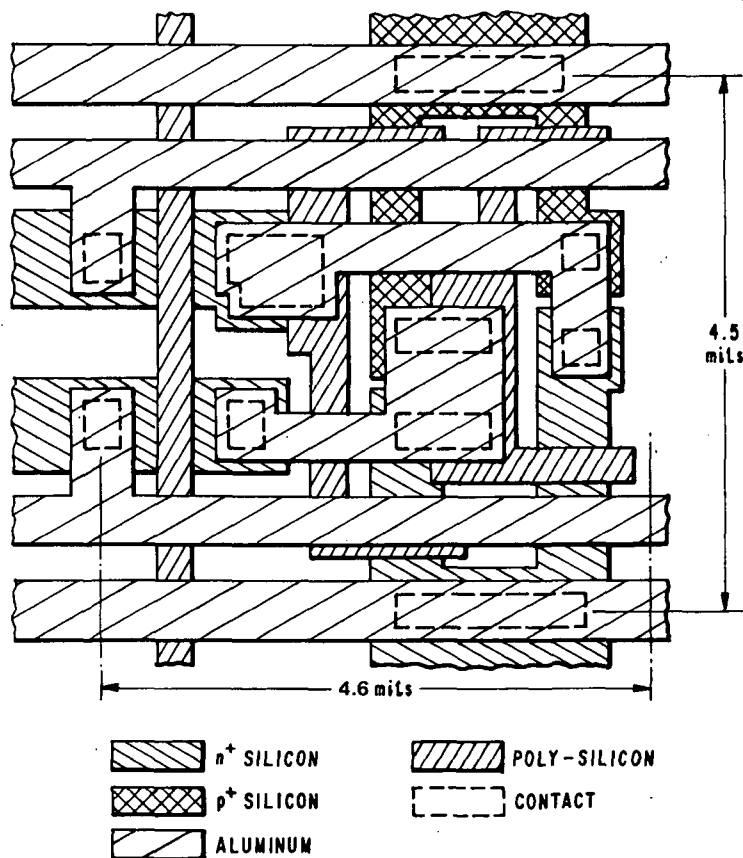

Figure 5. Silicon-gate SOS 6-transistor memory cell layout using standard layout design rules.

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The address decoding used in the Si-gate SOS COS/MOS RAM is that of a 2N string decoder. This decoder circuitry is the logical complement of the 2N decoder string used in the Al-gate 256-word × 1-bit SOS COS/MOS RAM (i.e., TA 6266). This can be seen in Fig. 4. The decoder circuitry of Fig. 4(a) has been well tested under stringent conditions in the Al-gate RAM and was chosen because of its successful implementation. The decoder shown in Fig. 4(b) is being used in the Si-gate RAM and is simply the logical complement of that shown in Fig. 4(a). The redesign was initiated primarily because of the elimination of the inverter driver of Fig. 4(a), which is used to drive the word line. This has resulted in a simpler layout with the exclusion of 32 inverter drivers from the chip. Notice that the row decoder drives the polysilicon word line directly and is shown in Figure 4(b). The column decoder drives the gates of the N2 devices of Figure 4(c). These gates enable the vertical digit lines to the Read/Write circuitry.

The decoder operation for the Si-gate RAM simply involves the simultaneous selection of the four address inputs to the decoder circuit in a low logic level with the enabled condition for the CS (Chip Select) input (i.e., CS = low logic level for ON condition). The output of the decoder string at point a of Figures 4(b) and 4(c) is pulled up to a high logic level such that the word line charges to turn on the input transistors to the flip-flop cells along a row (see Fig. 2), and the N2 transistors of Fig. 4(c) turn ON to enable the digit lines to the Read/Write circuitry. Particular cell selection occurs at the intersection of the chosen row and the particular digit lines which are enabled. The address inputs to the decoder string involve the eight address inputs to the chip and their internally created logical complements. The decoder layout results in a 2N configuration in which N = 8 (8 address inputs). The result is $2^8 = 256$, and any cell is selected through the proper input address combination to the chip.

The N1 devices of Figs. 4(b) and 4(c) are used as discharge devices for the decoder during the no operation condition. This ensures that during the OFF state the word line and the N2 transistors of Figs. 4(b) and 4(c), respectively, will be pulled down to the low logic level. This results in turning OFF the N2 transistors of Fig. 2 and the N2 transistors of Fig. 4(c). It should be noted that the N3 transistors of Fig. 4(c) represent the digit line precharge devices that are necessary for keeping the digit lines at a high logic level during the OFF condition. Digit line precharging is required in the memory chip operation and is the prime reason for the CS input being a pulse with certain timing criteria and not a level.

The inclusion of the Read/Write circuitry in the Si-gate 256-word × 1-bit COS COS/MOS RAM required the addition of circuitry that performs multiple operations such that reading or writing can be successfully implemented. The Read/Write circuitry is shown in Fig. 6. The inputs to this circuitry (i.e., $\overline{\text{CS} \cdot \text{WE}}$) (or, CS + $\overline{\overline{\text{WE}}}$), ($\overline{\text{CS} \cdot \text{WE}}$)

Figure 6. Read/Write circuitry.

are internally created by a simple SOS COS/MOS AND-NOT gate and an inverter. The operation of the Read/Write circuitry (Fig. 6) is as follows:

(1) No Operation: The N1 devices, which are gated by CS, turn ON and pre-charge the digit lines to a high logic level. The ($\overline{\text{CS} \cdot \text{WE}}$) input being high (due to $\overline{\text{CS}}$ being low during OFF condition) turns the P1 devices OFF. The ($\overline{\text{CS} \cdot \text{WE}}$) input being low (due to $\overline{\text{CS}}$ being low during OFF condition) turns the N2 devices OFF. The two digit lines are thus isolated from V_{CC} and V_{DD} because of the OFF N2 and P1 devices. This is independent of the state of the inputs to P2, P3, N3, and N4 devices.

(2) Write: A low-level CS requirement for a Write operation turns the N1 pre-charge devices OFF. The digit lines are now floating, and writing requires one digit line be pulled high as the other is pulled to a low logic level. The

($\overline{CS}\cdot WE$) input is at a high level for the Write operation, because $\overline{CS}$ and WE both must be high for a Write condition and the N2 devices to turn ON. The ($\overline{CS}\cdot WE$) input is thus at a low level and the P1 devices turn ON. With D_{in} at a high input level, for instance, $((\overline{CS}\cdot WE)\cdot D_{in})$ is at a low level. The net result is that P2 turns ON (with P3 turning OFF) and N4 turns ON (with N3 turning OFF). These simultaneous operations cause point a to be pulled up to a high level through the P1 and P2 transistors. The point b on the other digit line is therefore pulled down to a low state through N2 and N4 devices. The digit lines have assumed opposite logic states and coupled with a proper address selection, a word will be written into a particular cell location. The inverse condition in which a D_{in} is a low-level input will result in point a being pulled down to a low level through N2 and N3 and point b being pulled to a high level through P3 and P1. The digit lines will then be in opposite logic states and the inverse word is written into the memory.

(3) Read: The Read condition requires that the CS input fall to a low-level input. This will turn the precharge devices N1 OFF and leave the two digit lines floating at a high precharged level. The ($\overline{CS}\cdot WE$) is high and ($\overline{CS}\cdot WE$) is low due to the fact that WE is held at a low level for the read operation. The P1 and N2 devices are turned OFF, and the two digit lines are disconnected during this period from the V_{CC} and V_{DD} supplies. With P1 and N2 OFF, the possible conditions for N3, N4, P2, and P3 are of no consequence to the state of the two digit lines during the Read operation. Reading is performed by sensing the voltage levels on the two digit lines. This is accomplished by the sense amplifier circuitry and is discussed in the next section.

The most significant design of the Si-gate RAM has been the inclusion of voltage sense outputs described as D_{out} and $\overline{D_{out}}$. Before discussing the actual design used, it is instructive to analyze the requirements placed upon the word outputs (i.e., D_{out} and $\overline{D_{out}}$).

The implementation of the memory chip into any sort of memory system places some unique conditions upon the word outputs. In memory system organization, it is a frequent practice to "OR-tie" the word outputs of many memory chips, so as to realize an expanded memory storage capability. The "OR-tie" simply refers to the common wiring of the word outputs from a certain number of chips. Thus, the chip design must realize certain restrictions that the "OR-tie" condition places upon it. These requirements can be listed as follows:

(1) No Operation: During the no operation state, defined by CS being a high logic level, the D_{out} and $\overline{D_{out}}$ must show a high impedance to the circuitry external to the chip. The result is that in a system of memory chips, the word outputs of the chips that are not selected (i.e., no operation) will not load the D_{out} or $\overline{D_{out}}$ of the selected chip. This is a necessary condition for proper memory system operation as well as low power considerations. If the high-impedance input looking back into the word outputs for the nonselected chips is not realized, then possible sneak paths and spurious output levels would result.

(2) Write: The Write operation requires that on a particular chip the CS assume a low level and the WE be a high level. It is desired that the word outputs assume a high impedance looking back into the outputs from the external circuitry. Again, the "OR-tie" capability placed upon the memory chip outputs necessitates the exclusion of low-impedance paths into chips that are being written into.

(3) Read: The Read operation requires that the chip be selected (CS be a low level) and that the WE be a low level. The nature of the word outputs is such that they must assume a high- or a low-voltage level for a selected chip and a particular address location that is being read from. In the "OR-tie" of a memory system, the common word output (i.e., D_{out} or $\overline{D_{out}}$) of a group of memory chips will assume a high or low logic level, depending upon the state of a selected address location. The result is that the Read operation must sense the state of a selected memory cell location and transfer this as a high or low logic level to the common word output line (D_{out} or $\overline{D_{out}}$).

With the requirements placed upon the D_{out} and $\overline{D_{out}}$ outputs, a variety of methods for attaining these conditions can be utilized. The most common method is shown in Fig. 7(a). This figure shows the circuit schematic in which the digit lines are used as inputs to the sense amplifier circuit. From the analysis of the Read/Write circuitry, it was described that during the Read operation the digit lines are floating at the precharged high level and will assume the state (after some finite time, τ) of the selected memory cell. It was also shown that the digit lines are precharged to a high level in the no operation state, and they are set to high or low levels during the Write operation, depending upon the particular word being written into the selected cell. The circuit of Fig. 7(a) will realize all of the conditions placed upon the word
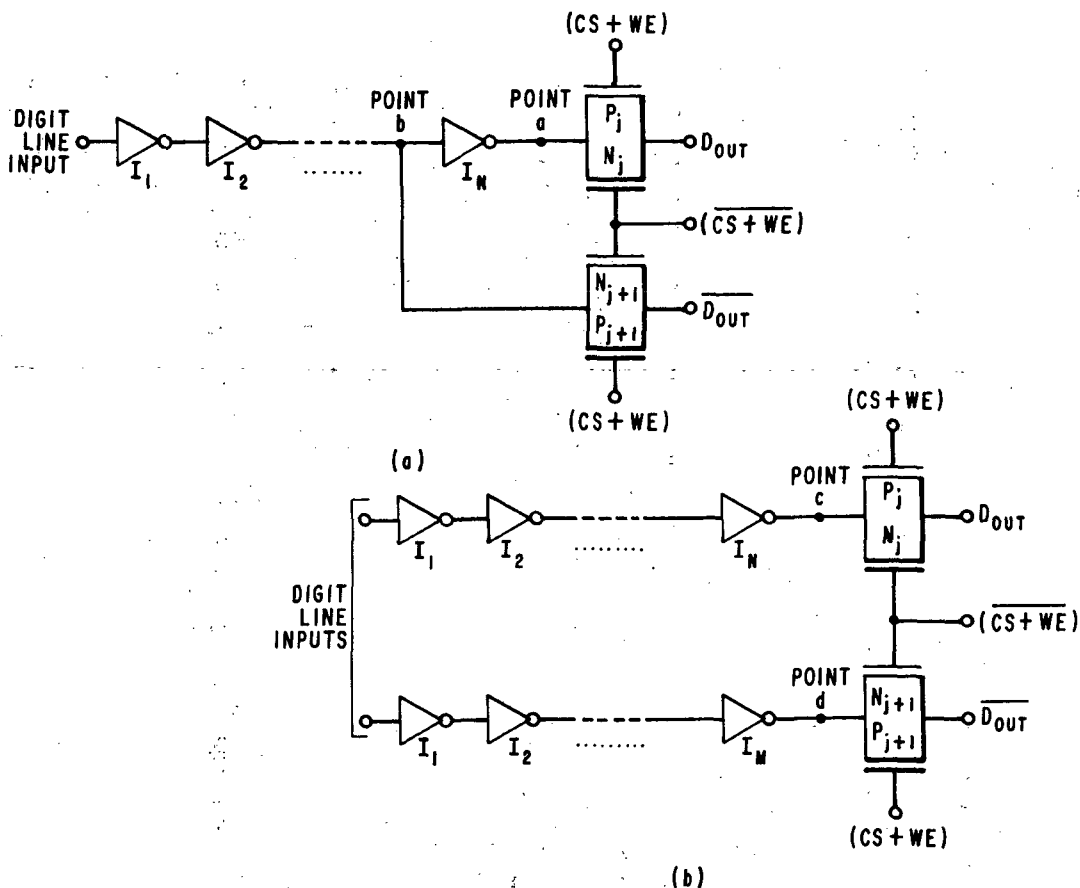
Figure 7. Standard sense amplifier circuitry.

outputs for Read, Write, and no operation states. It basically consists of a set of COS/MOS inverters in series which is inputted by one of the digit lines. The choice of the geometries and number of COS/MOS inverters used in this series depends upon the loading it places upon the internal cell and decoding circuitry, the loading of the P_j/N_j COS/MOS transmission gate, and system timing considerations. The P_j/N_j COS/MOS inverter of Fig. 7(a) represents the "switch" which determines the proper condition for the word outputs. This can be seen by the $(\overline{CS+WE})$ and $(CS+WE)$ signals which gate the N_j and P_j devices, respectively, in Fig. 7(a). These signals are created by a standard COS/MOS OR-NOT gate with an inverter on the chip. During Read the P_j/N_j transmission gate turns ON and transfers the information at point a to the D_{out} output. $\overline{D_{out}}$ is frequently obtained from the addition of a second separate transmission gate P_{j+1}/N_{j+1} which is tapped from point b of Fig. 7(a). An alternative method for $\overline{D_{out}}$ output is to use a second separate series of COS/MOS inverters attached to the other digit line and a corresponding transmission gate as shown in Fig. 7(b). In either case [Figs. 7(a) or (b)], the $(CS+WE)$ and $(\overline{CS+WE})$

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inputs to the transmission gate will turn the transmission gates (P_j/N_j and P_{j+1}/N_{j+1}) OFF during Write and no operation conditions, and access points a and b of Fig. 7(a) or points c and d of Fig. 7(b) to the respective D_{out} of $\overline{D_{out}}$ outputs. The prerequisites for proper memory chip operation in a memory system are therefore fulfilled. The circuit of Fig. 7(a) or 7(b) will suffice as a sense amplifier circuit.

The sense amplifier of Figs. 7(a) or 7(b) will not be used in the Si-gate RAM for the basic reason that it responds too slowly for a high-speed, low-power memory chip. Use of the circuit shown in Figs. 7(a) or 7(b) would defeat the purpose of the Si-gate SOS COS/MOS technology. This is due to the excessive load requirements placed upon the P_{n-1}/N_{n-1} and P_n/N_n inverter by the P_{j+1}/N_{j+1} and P_j/N_j transmission gates respectively in Fig. 7(a). The ability of the inverter that must drive through the impedance of the transmission gate is limited such that the response at the D_{out} or $\overline{D_{out}}$ output will be significantly degraded. This is coupled with the inherent delays associated with the series of N inverters that are used to amplify the digit line level so as to produce the correct voltage level at the input to the transmission gates. The same situation exists in Fig. 7(b) in which the P_n/N_n and P_m/P_m inverters must drive through the P_j/N_j and P_{j+1}/N_{j+1} transmission gates, respectively. The ON impedance of the transmission gates degrades the D_{out} and $\overline{D_{out}}$ response.

A sense amplifier circuitry vastly improved over the conventional circuit previously discussed has been designed and is used in the Si-gate SOS COS/MOS RAM. This circuit is shown schematically in Fig. 8. Notice that the input to the sense amplifier shows only one of the two digit lines. The other digit line contains the same circuitry, such that D_{out} and $\overline{D_{out}}$ are created.

The operation of the sense amplifier must adhere to the imposed constraints of the word outputs of a memory chip. It should be noted that the only inputs to the sense amplifier described in Fig. 8 are a digit line (one of the two) and a function ($\overline{CS+WE}$). This function is created internally on the chip using a standard COS/MOS OR-NOT gate. The various states of the sense amplifier (see Fig. 8) are described as follows:

(1) No Operation: The situation in which the chip is not selected is dictated by CS being at a high level. Thus, the ($\overline{CS+WE}$) input to the sense amplifier
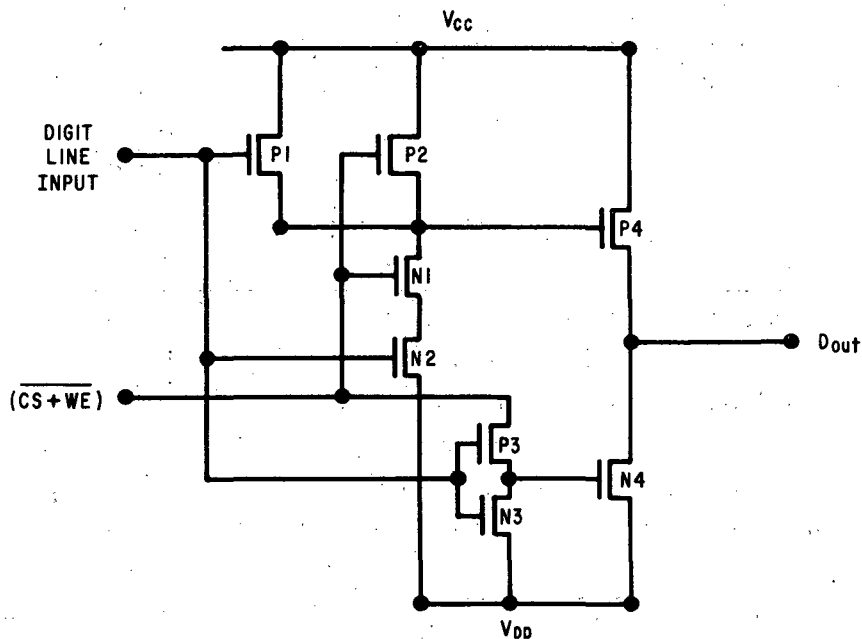
Figure 8. Improved sense amplifier.

is in a low logic level. The result is P2 turning on and the source of P3 being being pulled to a low logic level. Coupled with the fact that the digit lines (both of them) are precharged to a high level (during no operation), the P2 and N3 transistors are held on with the resulting P4 and N4 transistors being held OFF. Thus, the D_{out} (or $(\overline{D_{out}})$) "sees" a high impedance looking back into the sense amplifier, a necessary condition.

(2) Write: The Write operation requires that CS be in a low logic state and WE assumes a high logic level. The $(\overline{CS+WE})$ input is thus a low level and again the P2 device is held OFF and the source of P3 is strictly held low. The Write state of the digit line can be high or low such that the input to the P3/N3 inverter could assume either state. A high state will turn N3 ON and thus N4 would be held OFF. A low state will not turn on P3 because its

source is actively discharged and because the input capacitance of N4 must be discharged; the digit line input having been precharged for some finite time before a valid Write (i.e., N3 turns on; discharging the N4 gate capacitance during precharge). Thus, N4 must be OFF regardless of the state of the digit line input. The P4 device is held OFF by the P2 device being held ON. Thus, the P4 and N4 devices being held OFF is a necessary and sufficient condition for the memory chip word output during the Write operation.

(3) Read: The Read operation requires that CS and WE be held in a low level. This results in ($\overline{CS+WE}$) being a high logic level and thus P2 is OFF, N1 is enabled to turn ON, and the source of P3 is actively driven high. The two states of the digit line will determine the corresponding D_{out} (or $\overline{D_{out}}$). If the digit line is high, then N2 turns ON as does N3. The result is P4 turning ON and N4 turning OFF. Thus, D_{out} (or $\overline{D_{out}}$) is actively driven to a high level. If the digit line is in a low state, then P1 turns ON, N2 turns OFF, P3 turns ON, and N3 turns OFF. The result is P4 turning OFF and N4 turning ON. D_{out} (or $\overline{D_{out}}$) is therefore actively pulled to a low level. The Read operation is satisfied for proper word output behavior of a memory chip.

The analysis of the sense amplifier design has shown that there is a 20% improvement of the performance compared with the standard sense amplifier circuitry. This performance enhancement is reflected in faster memory chip access times and quicker rise times of the word outputs assuming equivalent conditions (e.g., temperature, external loading) for the standard and improved sense amplifier designs. The analyses have been performed using highly reliable in-house INPUT, MOSIM, and RCAP circuit simulation programs. It is firmly believed that the improved sense amplifier design of Fig. 8 will yield a performance that best utilizes the high-speed and low-power properties of Si-gate SOS technology.

All 11 logic inputs to the memory chip are protected against gate oxide damage from static electrical discharge at each input. The circuitry used for this purpose is shown in Fig. 9. It can be seen that the circuit is basically an n-type SOS enhancement type transistor in which the gate and source are tied together and a 100-Ω resistor is in series to the input pad. Excessive amounts of static electrical charge on the input pad will turn the large n-type transistor ON (either forward on characteristic or reverse transistor breakdown), providing a low-impedance path to the low level (assumed to be ground). This method of input protection to the

INPUT PAD o——/\/\/\——

100

N

V_{DD}

INPUT TO INTERNAL
SOS/COS/MOS CIRCUITRY
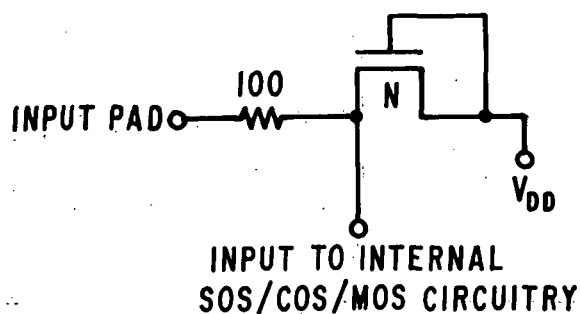
$V_{DD} = 0 \text{ V (GROUND SUPPLY)}$

Figure 9. Input protective device.

11 inputs is used as opposed to the diode protection utilized in the 256-word × 1-bit Al-gate SOS COS/MOS RAM. The reason is that the method of the self-gated n-type transistor does not require precise control of degenerate p^+ and n^+ doping levels as was the case with the diode input protection devices. The input protection that is being used is a proven Si-gate method that requires a small amount of layout area on the chip and uses a simpler process than the diode input protection used in the Al-gate RAM. The inputs using the input protection shown in Fig. 9 are A_0 - A_7, D_{in}, CS, and WE.

A summary of the Si-gate 256-word × 1-bit SOS COS/MOS RAM performance is shown in a typical timing diagram in Fig. 10. This timing was arrived at through the use of the circuit simulation programs: INPUT, MOSIM, and RCAP. These simulations have, in the past, been a highly reliable method of determining circuit performance. It is firmly believed that the timing diagram given in Fig. 10 is typical of the memory chip performance.

There are a few points that should be elaborated on. The access time t_{ac}, is a worst-case definition, chiefly because t_{ac} has been defined as the time from the address transition to the 50% point of the D_{out} (or $\overline{D_{out}}$). In memory system operation, this definition is the most realistic as far as performance evaluation is concerned. Thus, the choice of access time was given for a worst-case analysis. The Chip Select setup time, t_{su}, is defined for the proper precharging of the internal digit lines prior to memory chip operation. The Write Enable time, t_{we}, is delayed such that the selected memory cell is addressed prior to the Write operation. This prevents writing into an incorrect
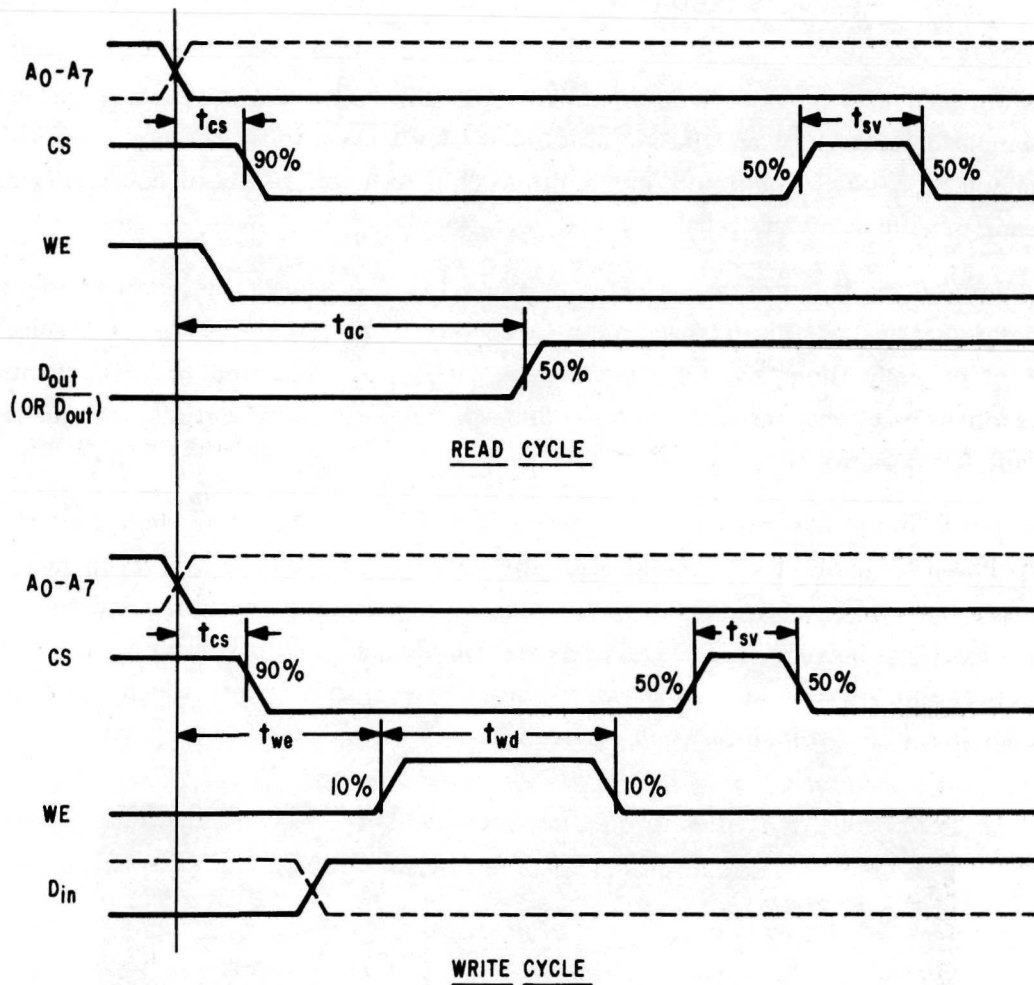
t_{cs}	5 NS
t_{ac}	70 NS
t_{we}	30 NS
t_{wd}	40 NS
t_{sv}	30 NS

CONDITIONS: TEMPERATURE = 55°C
CAPACITIVE LOADING TO OUTPUTS = 20 pF
P-TYPE THRESHOLD VOLTAGE = 1.5 V
N-TYPE THRESHOLD VOLTAGE = 2.0 V

Figure 10. Worst case timing diagram for silicon-gate
256-word × 1-bit SOS COS/MOS RAM.

cell location. The Write Delay time, t_{wd}, ensures an adequate period for Read/Write circuitry operation during the Write operation. The Chip Select time, t_{cs}, is used to guarantee that the address inputs to the decoder have settled to the proper selected states.

IV. BEAM-LEAD TECHNOLOGY

As outlined in a previous report (ref. 3) RCA has achieved extensive experience with beam-lead technology and its application in COS/MOS arrays. The application of this technology to SOS single-chip and multiple chip packages has been considered as one means of enhancing the reliability and performance of SOS memory arrays.

A simple SOS structure was selected as the vehicle to use in the initial phases of the process. Because of the extensive data taken on the RCA CD-4007, a bulk silicon package of basically three inverters, and because of the test data and process information available on its SOS counterpart, the TA 5388, this general configuration was chosen as the circuit for our program.

Beam-lead metal has replaced the aluminum metallization used in Phase I of the research. Phase II involved new masks with the beams. These masks have been made and circuits have been fabricated. A photograph of the beams interdigitated between an adjacent circuit is shown in Fig. 11. The beams appear to overlap other circuitry. This is not improper, however, as there is an oxide protecting the circuits which are protective diodes in the illustrated case.
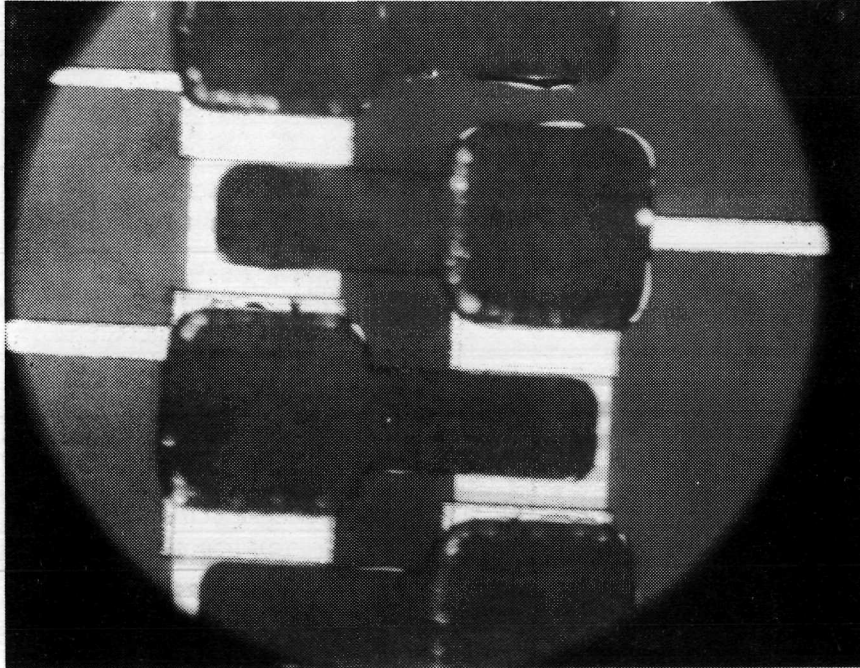

Figure 11. Interdigitated beam leads on a test sample.

The samples fabricated thus far have a mechanical problem due to an error in the mask-making. The error caused all transistors to be n-type, which, of course, makes it impossible to operate the devices as complementary-symmetry transistors.

Laser scribing has been successfully applied, in separating the samples into individual chips. This scribing is a part of the proposed Phase III program. The other part of Phase III remaining is the bonding of these chips to a ceramic substrate.

V. PERSONNEL AND EXPENDITURES

During this quarter the following personnel contributed to the contract:

W. R. Lile   Project Scientist
R. J. Hollingsworth
J. F. Kingsbury
N. K. Kudrajashev
L. C. Lucas
J. C. Sarace
W. C. Schneider

Total expenditures through August 31, 1972 have been $137,048. Problem areas that may create an overrun: none at this time.

VI. ACKNOWLEDGMENTS

REFERENCES

1. J. R. Burns, J. E. Meyer, and S. J. Connor, *Research and Development in Memory Arrays Using Complementary MOS*, Interim Technical Report, NASA Contract No. NAS12-2207, April 1970.

2. J. E. Meyer and W. R. Lile, et al., *Design, Processing, and Testing of LSI Arrays for Space Station*, Quarterly Technical Report No. 5, Contract NAS12-2207, December 1971.

3. W. R. Lile et al., *Design, Processing, and Testing of LSI Arrays for Space Station*, Quarterly Technical Report No. 6, Contract NAS12-2207, April 1972.

NEW TECHNOLOGY APPENDIX

It was concluded from the review of the work that one reportable item of New Technology has resulted from the contract effort during the period covered by this report.

A. READ/WRITE CIRCUITRY FOR THE SILICON-GATE RAM

Brief Description

All memories made previously in this contract effort have used current sensing. The redesign of the memory to use voltage sensing has been completed. Conventional methods of converting current-sensing devices to voltage-sensing devices are slow and have been abandoned. The approach described here preserves the speed of the device and provides for a tri-state output (open circuit, logic "1", logic "0").

Detailed Description

A sense amplifier circuitry vastly improved over the conventional circuit previously discussed has been designed and is used in the Si-gate SOS COS/MOS RAM. This circuit is shown schematically in Fig. 12. Notice that the input to the sense amplifier shows only one of the two digit lines. The other digit line contains the same circuitry, such that D_{out} and $\overline{D_{out}}$ are created.

The operation of the sense amplifier must adhere to the imposed constraints of the word outputs of a memory chip. It should be noted that the only inputs to the sense amplifier described in Fig. 12 are a digit line (one of the two) and a function $\overline{(CS + WE)}$. This function is created internally on the chip using a standard COS/MOS OR-NOT gate. The various states of the sense amplifier (see Fig. 12) are described as follows:

(1) <u>No Operation</u>: The situation in which the chip is not selected is dictated by CS being at a high level. Thus, the $\overline{(CS + WE)}$ input to the sense amplifier is in a low logic level. The result is P2 turning ON and the source of P3 being pulled to a low logic level. Coupled with the fact that the digit lines (both of them) are precharged to a high level (during no operation), the P2 and N3

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$$V_{CC}$$

DIGIT LINE INPUT

$(\overline{CS+WE})$

V_{DD}
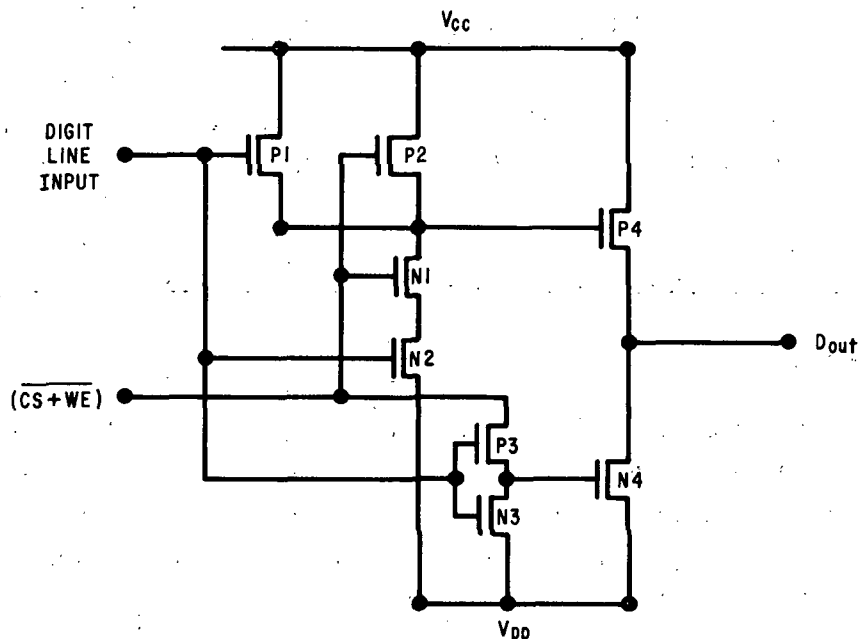
D_{out}

V_{CC}	V_{DD}
TYPICALLY:	
$V_{CC} = 10\,V$	
$V_{DD} = 0\,V$	

Figure 12. Improved sense amplifier.

transistors are held on with the resulting P4 and N4 transistors being held OFF. Thus, the D_{out} $\left(\text{or } \overline{(D_{out})}\right)$ "sees" a high impedance looking back into the sense amplifier, a necessary condition.

(2) Write: The Write operation requires that CS be in a low logic state and WE assumes a high logic level. The $\overline{(CS+WE)}$ input is thus a low level and again the P2 device is held OFF and the source of P3 is strictly held low. The Write state of the digit line can be high or low such that the input to the P3/N3 inverter could assume either state. A high state will turn N3 ON and thus N4 would be held OFF. A low state will not turn on P3 because its source is actively discharged and because the input capacitance of N4 must be discharged, the digit line input having been precharged for some finite time before a valid Write (i.e., N3 turns on; discharging the N4 gate capacitance

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during precharge). Thus, N4 must be off regardless of the state of the digit line input. The P4 device is held OFF by the P2 device being held ON. Thus, the P4 and N4 devices being held OFF is a necessary and sufficient condition for the memory chip word output during the Write operation.

(3) Read: The Read operation requires that CS and WE be held in a low level. This results in $\overline{(CS + WE)}$ being a high logic level and thus P2 is OFF, N_1 is enabled to turn ON, and the source of P3 is actively driven high. The two states of the digit line will determine the corresponding D_{out} (or $\overline{D_{out}}$). If the digit line is high then N2 turns ON as does N3. The result is P4 turning ON and N4 turning OFF. Thus, D_{out} (or $\overline{D_{out}}$) is actively driven to a high level. If the digit line is in a low state, then P1 turns ON, N2 turns OFF, P3 turns ON, and N3 turns OFF. The result is P_4 turning OFF and N_4 turning ON. D_{out} (or $\overline{D_{out}}$) is therefore actively pulled to a low level. The Read operation is satisfied for proper word output behavior of a memory chip.

The analysis of the sense amplifier design has shown that there is a 20% improvement of the performance compared with the standard sense amplifier circuitry. This performance enhancement is reflected in faster memory chip access times and quicker rise times of the word outputs, assuming equivalent conditions (e.g., temperature, external loading) for the standard and improved sense amplifier designs. The analyses have been performed using highly reliable in-house INPUT, MOSIM, and RCAP circuit simulation programs. It is firmly believed that the improved sense amplifier design of Fig. 12 will yield a performance that best utilizes the high-speed and low-power nature of Si-gate SOS technology.