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TWO-PHASE CHARGE-COUPLED DEVICE

by W. F. Kosonocky and J. E. Carnes

Prepared by
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Princeton, N.J. 08540
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16. Abstract

A charge-transfer efficiency of 99.99% per stage was achieved in the fat-zero mode of operation of 64- and 128-stage two-phase charge-coupled shift registers at 1.0-MHz clock frequency. The experimental two-phase charge-coupled shift registers were constructed in the form of polysilicon gates overlapped by aluminum gates. The unidirectional signal flow was accomplished by using n-type substrates with 0.5 to 1.0 ohm-cm resistivity in conjunction with a channel oxide thickness of 1000 Å for the polysilicon gates and 3000 Å for the aluminum gates. The operation of the tested shift registers with fat zero is in good agreement with the free-charge transfer characteristics expected for the tested structures. The charge-transfer losses observed when operating the experimental shift registers without the fat zero are attributed to fast interface state trapping. The analytical part of the report contains a review backed up by an extensive appendix of the free-charge transfer characteristics of CCD's in terms of thermal diffusion, self-induced drift, and fringing field drift. Also, a model was developed for the charge-transfer losses resulting from charge trapping by fast interface states. The proposed model was verified by the operation of the experimental two-phase charge-coupled shift registers.

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FOREWORD

This final report was prepared by RCA Laboratories, Princeton, New Jersey, for NASA's Langley Research Center under NASA Contract No. NAS 1-10983. It describes work performed from June 25, 1971, to December 24, 1971, in the Process and Materials Applied Research Laboratory, P. Rappaport, Director. The Project Supervisor is Dr. K. H. Zaininger, and the Project Scientist is Dr. W. F. Kosonocky. The following Members of the Technical Staff at RCA Laboratories participated in the research and the writing of this report: Dr. J. E. Carnes and Dr. W. F. Kosonocky. Mr. W. Romito was concerned with fabrication of the devices.

The Free Charge Transfer Analysis (contained in Section II-A and Appendix A) was carried out before the start of this contract. It is included in this report, as requested by NASA, in order to provide the necessary background information. In addition, it should be noted that about 50% of the effort described in this report has been funded by RCA Laboratories under its parallel research program, and the remaining 50% was supported by contract funds.

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SUMMARY

A charge-transfer efficiency of 99.99% was achieved in the fat-zero mode of operation of 64- and 128-stage two-phase charge-coupled shift registers at 1.0-MHz clock frequency. The experimental two-phase charge-coupled shift registers were constructed in the form of polysilicon gates overlapped by aluminum gates. The unidirectional signal flow was accomplished by using n-type substrates with 0.5 to 1.0 ohm-cm resistivity in conjunction with a channel oxide thickness of 1000 Å for the polysilicon gates and 3000 Å for the aluminum gates. The operation of the tested shift registers with fat zero is in good agreement with the free-charge transfer characteristics according to a model described in this report. The charge-transfer losses observed when operating the experimental shift registers without the fat zero are attributed to fast interface state trapping. The analytical part of the report contains a review backed up by an extensive appendix of the free-charge transfer characteristics of CCD's in terms of thermal diffusion, self-induced drift, and fringing field drift. Also, a model was developed for the charge-transfer losses resulting from charge trapping by fast interface states. The proposed model was verified by the operation of the experimental two-phase charge-coupled shift registers.

I. INTRODUCTION

Charge-coupled semiconductor devices (refs. 1-7) consist of closely spaced MOS capacitors pulsed into deep depletion by the clock phase voltages. For times much shorter than that required to form an inversion layer of minority carriers by thermal generation, potential wells will be formed at the silicon surface. The minority-carrier charge representing the information will be stored or confined in these potential wells. The propagation of the information is accomplished by clock pulses applied to the electrodes of the successive MOS capacitors (i.e., charge-coupled elements), resulting in a motion or spilling of charges from the potential wells that become shallower to the potential wells that become deeper. Such propagation of signal into the successive minima of the surface potential produces a shift register for analog signals having signal transfer efficiency approaching unity. Such analog shift registers may be used for various signal processing applications such as the electronically variable delays or self-scanning photosensor arrays. However, by adding simple charge-refreshing stages (refs. 2-4) a charge-coupled shift register for digital signals can be constructed.

If the charge-coupled structures are formed with symmetrical potential wells, at least three clock phases are required to determine the directionality of the signal flow. The use of more than three phases may be dictated by either the construction design symmetry, as in the case of a four-phase silicon gate overlapped by aluminum structures, or special signal coding schemes in which more than one bit may be propagated in one clock cycle. One important feature of the three-phase system is that it may be used for a bidirectional charge-coupled channel in which the flow of information may be reversed by reversing the timing of two of the three phase clocks.

Two-phase operation requires that the charge-coupled structures be formed so that the potential wells induced by the phase voltage pulses are deeper in the direction of the signal flow. In this case, as one phase voltage is lowered, the resulting potential barriers force a unidirectional signal flow. It should be noted that a one-clock operation can also be obtained in a two-phase charge-coupled shift register if a proper dc voltage is applied to one of the phases (ref. 2). Furthermore, a true single-phase or a uniphase charge-coupled structure (ref. 8) can be formed by replacing the dc-biased phase by a structure involving a fixed charge in the oxide. Such structures could be formed by the use of ion-implanted barriers (ref. 9) or by variation of the fixed oxide charge for the formation of the asymmetrical potential wells.

Charge-coupled devices can be constructed with any of the following three techniques:

(1) Single metallization using p-MOS or n-MOS processes for three phase CCD's.

(2) Polysilicon-aluminum structures for two-phase and multiphase CCD's.

(3) Single metallization with ion-implanted barriers for two-phase or uniphase CCD's.

The most conventional process and the one used to make our first charge-coupled circuits is the thick-oxide p-MOS process (refs. 2-4). The major limitation of this process is the etching of the separation between the gates which should be no larger than about 0.1 mil in order to control the surface potential in the resulting gap. The operation of n-MOS CCD's on the other hand, can be less sensitive in the interelectrode spacings because of the presence of positive charge usually present in thermally grown SiO_2 channel oxides.

The sealed-channel polysilicon-aluminum structures described in this report are the most compact structures that can be fabricated with more or less conventional layout rules. The self-aligning-gate construction of these devices allows fabrication of charge-coupled structures with gate separation comparable to the thickness of the channel oxides as well as having the channel oxide always covered by one of the metallizations. Another important advantage of the silicon-gate process is that it provides a very simple method for the construction of two-phase CCD's.

The two-phase CCD's described in Section III employ two thicknesses of channel oxide oxide for the formation of the asymmetrical potential wells needed for the unidirectional flow of signal. Another approach by which similar two-phase operation can be achieved is by introduction of ion-implanted barriers into regions of the substrate under the gates of the charge-coupled structure (ref. 9). The advantage of the two-phase CCD's with the ion-implanted barriers is a simpler processing requiring only one metallization. The other feature of these devices is that they normally operate in the so-called "bias-charge" mode described in Section III.

The analysis of charge-transfer characteristics of CCD's in terms of free-charge losses and losses due to the trapping by fast interface states are described in Section II. Section III deals with the construction and operation of two-phase charge-coupled shift registers made in the form of polysilicon gates overlapped by aluminum gates.

II. CHARGE TRANSFER ANALYSIS

A. Free Charge Transfer in CCD's

1. Introduction. — The utility of CCD's for various applications depends to a great extent upon the two interrelated questions of how fast and how completely can charge be transferred between adjacent potential wells. When interface state trapping is ignored, the answers to both of these questions are known if one knows how much charge remains in the transferring potential well as a function of time because this is essentially transfer efficiency vs. frequency information. An outline of the free charge transfer analysis which yields such information is given in this section; a more detailed discussion can be found in Appendix A.

There are three separate, conceptually identifiable mechanisms, or "driving forces," which cause charge to move from one potential well to an adjacent one of lower energy (see Figure 1). The first is thermal diffusion due to the random thermal motion of the carriers which causes charge to move from regions of higher concentration to regions of lower concentration. The

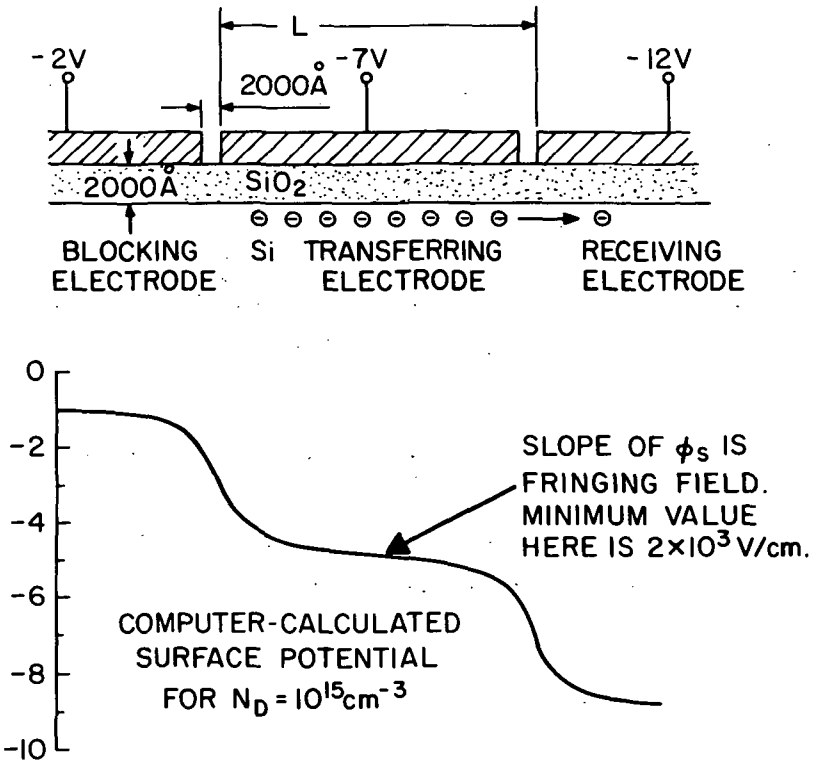


Figure 1. Cross section of three-phase CCD. Charge transfers from under center electrode to the right. The surface potential in the absence of signal charge as calculated by computer is shown in lower half.

second mechanism is due to the repulsion of the like-charged carriers which make up the signal and is referred to as "self-induced drift." It is basically a drift mechanism where the electric field is produced by the charged carriers themselves. The third mechanism is referred to as "fringing field drift." Here the electric field arises from the externally applied clock voltages. In the following discussion it will be shown that fringing field drift can appreciably speed up the charge-transfer process and, in appropriately designed CCD structures, can result in highly efficient transfer (η = 99.99%) at 10-MHz bit rates (neglecting interface state trapping).

2. Thermal Diffusion. — Strictly speaking, the time decay of charge remaining in the transferring potential well due to thermal diffusion alone depends upon the initial charge concentration profile. However, a Fourier analysis (ref. 10) of the problem indicates that the decay approaches an exponential one for long times with a decay constant τ_{th} given by

$$\tau_{th} = L^2/2.5D \tag{1}$$

where L is the center-to-center electrode spacing and D is the diffusion constant.In this problem it is assumed that a potential barrier prevents charge motion in the reverse direction while the receiving potential well serves as a perfect sink for carriers in the forward direction. Thus, if the carriers were not charged and thermal diffusion were the only transfer mechanism, the total number of carriers remaining in the transferring well as a function of time $N_{tot}(t)$ would be given by

$$N_{tot}(t) = N_{tot}(0)e^{-(2.5D/L^2)\,t} \tag{2}$$

The most important controllable parameter here is L, but even for reasonably small values of L thermal diffusion is rather slow. If we define t_4 as the time required to reach 99.99% transfer efficiency and f_4 as the corresponding clock frequency for two-phase operation, $f_4 = 1/(2t_4)$, then

$$t_4 = \frac{3.7L^2}{D} \tag{3}$$

or

$$f_4 = \frac{D}{7.4L^2} \tag{4}$$

Thus, for L = 10 μm and D = 6.25, f_4 is just 8.4 x 10^5 Hz.

3. Self-Induced Drift. — The drift of the carriers under the influence of the electric field produced by the signal charge itself is an important effect at carrier concentration levels above ~ $10^{10}cm^{-2}$. There are at least two different methods of approaching this problem (see Appendix A). Both lead to the same conclusion; i.e., the charge reamining decays hyperbolically in time according to the following equation:

$$N_{tot}(t) = N_{tot}(0) \frac{t_o}{t + t_o} \tag{5}$$

where

$$t_o \simeq \frac{L^2 C_{ox}}{1.57 \mu q n_o} \tag{6}$$

C_{ox} is the oxide capacitance per unit area (F/cm^2)
μ is the field effect mobility ($cm^2/(V\text{-}sec)$
q is the electronic charge (C)
n_o is the initial uniform carrier concentration (cm^{-2})

A hyperbolic time decay is very fast for short times ($t \leqslant 100\ t_o$), but becomes comparatively slow for long times. It can be shown that after $t = 1.6\ \tau_{th}$, the decay due to thermal diffusion proceeds faster than that caused by self-induced drift. Thus, self-induced drift is a very fast process effective in transferring the first 90-99% of charge. It becomes ineffective, however, in attaining transfer efficiencies of 99.99%.

4. Fringing Field Drift. — A third mechanism which can have a dominant effect on charge transfer, especially at low concentration levels, is fringing field drift. The fringing fields referred to are the electric fields at the Si-Sio_2 interface *along the direction of charge transfer* which arise from the externally applied clock voltages. In other words, the fringing field at any point along the interface is the slope of the surface potential there (see Figure 1).

Fringing field magnitudes have been calculated by an approximate analysis and computed numerically for the case of closely spaced electrodes. They depend upon the electrode length, the clock voltage magnitude, the oxide thickness, and the substrate doping density. The minimum value of the fringing field occurs at the center of the transferring electrode and is given by

$$E_{FMIN} = 6.5 \frac{X_{ox}}{L} \frac{V}{L} \left[\frac{5X_d/L}{5X_d/L + 1}\right]^4 \tag{7}$$

where X_{ox} is oxide thickness, V is ½ of the total clock pulse voltage, L is the gate length, and X_d is the depletion depth at the center of the transferring electrode. For the closely spaced electrode structures studied it was found that the average fringing field magnitude is twice the minimum value, so that the time required for a single carrier to transit across the length of the transferring gate, the single carrier transit time τ_t, is given by

$$\tau_t = \frac{L}{2\mu E_{FMIN}} = \frac{L^3}{13\,\mu X_{ox} V} \left[\frac{5X_d/L + 1}{5X_d/L}\right]^4 \tag{8}$$

However, our computer studies have shown that it takes longer than one τ_t to remove all of the charge from the transferring gate. Because of the combined effects of the nonuniform fringing field and the thermal diffusion which tends to oppose charge transfer, the total remaining charge decays exponentially in time with final decay constant τ_f. Further, it was found for the closely spaced gate structures studied that τ_f was equal to one-third τ_t, and since an analytical expression is available for τ_t, [Eq. (8)] the decay rate due to fringing field drift can be calculated. The time t_4 required to reach η = 99.99% is given by

$$t_4 = \frac{3L}{\mu E_{FMIN}} \tag{9}$$

For doping densities lower than ~ 10^{15} and gate lengths less than 1 mil, the fringing field drift mechanism significantly speeds up the transfer of the last few percent of charge.

5. Expected Performance. — The speed-efficiency performance expected for CCD's, neglecting interface state trapping, depends most strongly upon gate length and substrate doping. The importance of each is most clearly apparent when we plot the t_4 time (η = 99.99%) vs. gate length for various doping densities, as seen in Figure 2. The dotted line is the t_4 time given by Eq. (3) for thermal diffusion and represents the longest time required in any case. The solid lines are found from Eq. (9) while the data points represent computer simulation results of Appendix A. It is clear from Figure 2 that fringing field drift can ensure very

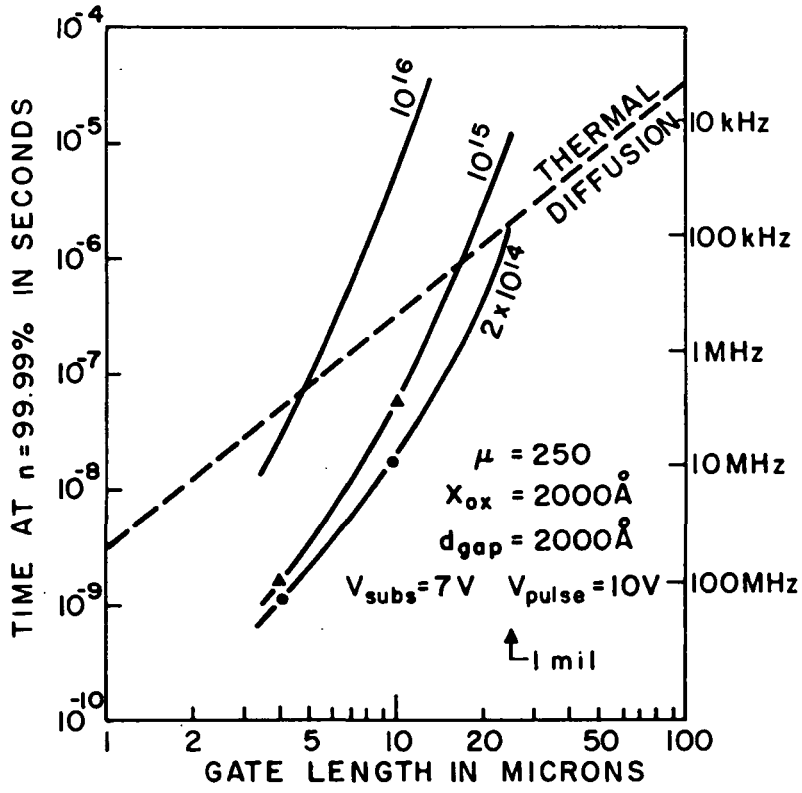


Figure 2. Time required to achive η = 99.99% vs. gate length for various doping levels. The thermal diffusion line is the maximum time required in any case.

complete free charge transfer for reasonable gate lengths ($\leqslant 10\,\mu$m) and doping levels ($\leqslant 10^{15}$cm^{-3}) at bit rates of 10 MHz or even higher. Thus, we must conclude that free charge transfer will not place any serious limitation on CCD performance. It is likely, however, that trapping of signal charge in fast interface states will limit operation. This subject is discussed in the next section.

B. Trapping Effects in Fast Interface States

1. Introduction. — Surface and interface states have influenced the development of solid state electron devices since the days of copper-copper oxide rectifiers in the late 1800's (ref. 11). For example, the bipolar transistor was probably developed only because surface states prevented the early realization of the field effect transistor, a much simpler transistor

concept first proposed by Heil (ref. 12) over ten years before Bardeen and Brattain's bipolar transistor (ref. 13). It was not until Atalla, et al. (ref. 14) demonstrated the passivation properties of SiO_2 layers on silicon surfaces in 1959 that interface states were reduced to a level which permitted fabrication of MOS field effect transistors. This marked the beginning of the MOS integrated circuit, which is only today beginning to exert a significant impact in the electronics industry. It is to be anticipated that once again in the area of charge-coupled devices, interface states will play a very important role.

In this section the effect of fast interface state (FIS) trapping upon CCD operation will be discussed. First the definition and characterization of FIS's will be outlined, followed by a formulation of the general problem and evaluation of the rate constants involved. A simplified, intuitive solution is then presented. Finally, a more exact expression for the fast state loss in the case of constant background charge (bias charge), varying background charge (fat zero), and small signal are presented in integral form.

2. Characterization of Fast Interface States. — Fast interface states exist in the silicon forbidden gap at the silicon-insulator interface and can exchange charge rapidly with the silicon conduction and valence bands. The time constant for charge exchange varies over many orders of magnitude depending upon the energy of the states; thus, some are faster than others. But the ability to communicate with bands defines them as "fast." Slow states, on the other hand, exist further into the insulator and change their occupation levels with time scales of hours and days (ref. 15).

As was shown by Tamm (ref. 16) and Shockley (ref. 17) fast states arise fundamentally from a quantum-mechanical point of view because of the abrupt termination of the silicon lattice periodicity. From a chemical viewpoint, the surface states can be thought of as caused by the dangling or unsaturated silicon bonds at the surface. Other factors which can cause fast states are chemical impurities, work damage, and stresses induced by thermal expansion mismatch between the insulator and silicon.

Fast states are characterized by two parameters:

(1) Their number per unit area per eV of energy, N_{ss}, in $(cm^2\text{-}eV)^{-1}$. This density may vary in energy.

(2) Their capture cross sections for electrons and holes, σ_n and σ_p, respectively, in cm^2. These quantities may also vary with energy, but are generally assumed to be constant.

Several different techniques have been devised for measuring fast state densities, all involving the MOS capacitor. They include capacitance-voltage (C-V) slope, C-V vs. temperature [Gray-Brown technique (ref. 18)] and conductance-voltage (G-V) technique (ref. 19). These methods are reviewed by Sze (ref. 20).

Measurements on the thermal SiO_2-Si system indicate that fast state densities range from 10^{10} to 10^{12} $(cm^2\text{-}eV)^{-1}$ depending upon oxide growth conditions, silicon orientation, and annealing procedures (refs. 20-21). Generally, the density is a minimum near the center of the gap gradually increasing to peaks about 0.1 eV above and below the two bands (ref. 19). (111) silicon surface orientation results in about one order of magnitude more fast states than (100) (ref. 18) while steam-grown oxides have lower fast state densities than dry oxides (ref. 19). A 500°C heat treatment step after aluminum deposition in hydrogen gas reduces fast state densities to the 10^{10} $(cm^2\text{-}eV)^{-1}$ level (ref. 22).

Capture cross sections for electrons have been measured to be between 10^{-15} and 10^{-16} cm^2, independent of energy and of most growth and annealing parameters. σ_p values range between 2 and 4 x 10^{-17} cm^2, (ref. 19).

3. General Formulation of Interface State Model. — The model which has been assumed consists of a uniform (or slowly varying) density in energy of interface states, denoted N_{ss}, which exist at the Si-SiO_2 interface. These states will trap free electrons or holes at a rate proportional to the number of free electrons or holes and the number of empty or filled states, respectively. The states will emit or de-trap electrons or holes at a rate proportional to the number of filled or empty states, respectively, and the Boltzmann factor appropriate for the energy of the states (ref. 20). Thus, the rate of change of occupation of the fast states at any given energy level ϵ below the conduction band is given by

$$\frac{dn_{ss}}{dt} = k_1(N_{ss} - n_{ss})\, n_s - k_2 n_{ss} e^{-\epsilon/kT} - k_3 n_{ss} P_s + k_4(N_{ss} - n_{ss})\, e^{-(\epsilon_g - \epsilon)/kT} \tag{10}$$

where n_{ss} is the number of occupied states in $(cm^2\text{-}eV)^{-1}$,

N_{ss} is the interface state density in $(cm^2\text{-}eV)^{-1}$,

n_s is the density of free electrons at the surface in cm^{-2},

p_s is the density of free holes at the surface in cm^{-2},

ϵ is the energy of the states below the conduction band edge,

ϵ_g is the energy width of the forbidden gap,

k is Boltzmann's constant,

T is absolute temperature, and

k_1, k_2, k_3, and k_4 are constants. Their values are discussed in a later section.

In principle, if we know how n_s varies with time, then by using Eq. (10) we can solve for n_{ss} as a function of time and energy. By integrating over energy, we find the total amount of trapped charge as a function of time. By comparing the total number trapped at the beginning of the transfer-in period with that trapped at the end of the transfer-out period we obtain the total number of carriers lost into interface states for each transfer. This procedure can be used to calculate the interface state loss vs. CCD clock frequency.

From a practical point-of-view, however, certain simplifying assumptions must be made. One simplification results from the nature of CCD operation. In normal operation CCD's are biased into deep depletion and remain there because any thermally generated charge is constantly being swept away by the CCD charge transfer action. Therefore the density of majority carriers at the interface is extremely low and for an n-channel device this means that p_s, the density of free holes at the surface, is negligible. Therefore, the third term of Eq. (10) may be neglected, yielding

$$\frac{dn_{ss}}{dt} = (N_{ss} - n_{ss}) \left[k_1 n_s + k_4 e^{-(\epsilon_g - \epsilon)/kT} \right] - k_2 n_{ss} e^{-\epsilon/kT} \tag{11}$$

In steady-state $dn_{ss}/dt = 0$ for all energies so that

$$\frac{n_{ss}}{N_{ss}} = \frac{1}{1 + \dfrac{k_2 e^{-\epsilon/kT}}{k_1 n_s + k_4 e^{-(\epsilon_g - \epsilon)/kT}}} \tag{12}$$

By setting $n_{ss}/N_{ss} = ½$, we can define a quasi-Fermi level, ϵ_Q:

$$k_1 n_s + k_4 e^{-(\epsilon_g - \epsilon_Q)/kT} = k_2 e^{-\epsilon_Q/kT} \tag{13}$$

When $k_1 n_{ss} >> k_4 e^{-(\epsilon_g - \epsilon_Q)/kT}$,

$$\epsilon_Q = kT \ln \frac{k_2}{k_1 n_s} \tag{14}$$

When $k_1 n_s << k_4 e^{-(\epsilon_g - \epsilon_Q)/kT}$

$$\epsilon_Q = \frac{\epsilon_g}{2} - \frac{1}{2} \ln \frac{k_4}{k_2} \approx \frac{\epsilon_g}{2}. \tag{15}$$

This means that when n_s is greater than $(k_4/k_1)\exp(-\epsilon_g/2kT)$, the quasi-Fermi level ϵ_Q will be in the upper half of the gap as given by Eq. (14), and emission of holes can be neglected. However, when n_s is lower than this value ϵ_Q will tend toward center gap, and hole emission is no longer negligible. As ϵ_Q tends below center gap, hole emission fills the states faster than electron emission can empty them. Since, as shown in a later section, $k_4/k_1 \approx 10^{12}$, $(k_4/k_1)\exp(-\epsilon_g/2kT) \approx 10^4 cm^2$. In the following analyses it is assumed that n_s is greater than this value and therefore ϵ_Q is determined by n_s [Eq. (14)].

If the number of occupied fast states at any energy is perturbed from its steady-state value, or if the value of n_s changes, thereby forcing a new ϵ_Q, n_{ss} will approach its new steady-state level at a rate given by

$$\frac{d\Delta n_{ss(t)}}{dt} = -\Delta n_{ss}(t) k_1 n_s - k_2 \Delta n_{ss}(t) e^{-\epsilon/kT} \tag{16}$$

where $\Delta n_{ss}(t)$ is the difference between the actual n_{ss} and the steady-state n_{ss} appropriate for the new value of n_s. Integrating Eq. (16), we have

$$\Delta n_{ss}(t) = \Delta n_{ss}(0) e^{-t/\tau} \tag{17}$$

where

$$\tau = \frac{1}{k_1 n_s + k_2 e^{-\epsilon/kT}} \tag{18}$$

If the change in n_s is an increase, then ϵ_Q moves higher in the gap, and essentially all the states between the old and new ϵ_Q's have to be filled. Since at the energies of interest $\epsilon > \epsilon_Q$, $k_1 n_s >> k_2 e^{-\epsilon/kT}$, and

$$\tau_{fill} = \frac{1}{k_1 n_s} \tag{19}$$

If the change in n_s is a decrease, then all states between the old and new ϵ_Q must be empty, and in this case $\epsilon < \epsilon_Q$; thus,

$$\tau_{empty} = \frac{1}{k_2} e^{\epsilon/kT} \tag{20}$$

Provided $n_s > k_4/k_1 \, e^{(-\epsilon_g/2kT)}$, the states will fill exponentially with time constant $1/k_1 n_s$. The empty time will vary an order of magnitude for every 0.06 eV change in energy (at room temperature) and since $k_2 \cong 10^{11}$, empty times vary from $\sim 10^{-11}$ sec near the band edge to $\sim 10^{-2}$ sec near midgap. Fundamentally speaking, it is this property that states can fill faster than they can empty which causes loss of charge into fast interface states.

4. Determination of Rate Constants. — The basic rate Eq. (10) includes constants k_1 through k_4. The following discussion estimates the values of these constants for the Si-SiO_2 case.

k_1 represents the probability per unit time that a given free electron will be trapped by any one trapping site. In the bulk trapping case k_1 is the volume swept out by a trap with cross section σ traveling at the thermal velocity v_{th}, or σv_{th} with units cm^3/sec. However, for the case of interface state trapping this expression is not valid. For one thing, the units are not correct. Actually, the interface trapping case is probably easier to visualize than the bulk case. Electrons confined in the inversion layer at the surface collide with the Si-SiO_2 interface with some average frequency ν. Each time an electron collides, it has the probability of being trapped by a particular interface state of σ, since the total area here is unity. Thus, the probability per unit time of one electron being captured by one empty interface state is $\sigma\nu$. Since σ has been measured for Si-SiO_2 fast states (ref. 19), it remains to estimate the value of ν.

In a given energy interval $d\epsilon$ located an energy ϵ above the conduction band, the time between surface collisions $\tau_c(\epsilon)$ is given by

$$\tau_c(\epsilon) = \frac{2W(\epsilon)}{v_x(\epsilon)} \tag{21}$$

where $W(\epsilon)$ is the width of the inversion layer at ϵ, and $v_x(\epsilon)$ is the x-directed velocity of electrons at ϵ. Assuming equipartition of energy, $v_x(\epsilon)$ can be written as

$$v_x(\epsilon) = \left(\frac{2q\epsilon}{3m^*}\right)^{1/2} \tag{22}$$

ϵ is given in electron-volts, and m^* is the effective mass. The inversion layer width can be estimated using the maximum field in the silicon E_s as

$$W(\epsilon) = \frac{\epsilon}{E_S} \tag{23}$$

The number of carriers at each energy, assuming nondegenerate conditions, is

$$n(\epsilon) = N(\epsilon)\, e^{-(\epsilon - \epsilon_f)/kT} = N_o\, \epsilon^{1/2}\, e^{-(\epsilon - \epsilon_f)/kT} \tag{24}$$

$N(\epsilon)$ is the three-dimensional density of states in the conduction band, ϵ_f is the Fermi level and kT is in units of eV.

The average frequency of collision with the interface is then obtained by integrating $1/\tau_c(\epsilon)$ weighted by $n(\epsilon)$ over energy and dividing by the total number of carriers:

$$\nu = \frac{\int_0^\infty \left(1/\tau_c\right) n(\epsilon)\, d\epsilon}{\int_0^\infty n(\epsilon)\, d\epsilon} \tag{25}$$

By making the substitution $u = \epsilon/kT$, we have

$$\nu = \frac{E_S \left(\frac{q}{6m^*kT}\right)^{1/2} \int_0^\infty e^{-u} du}{\int_0^\infty u^{1/2} e^{-u} du} \tag{26}$$

(26)

$$= E \left(\frac{q}{6m^*kT}\right)^{1/2} \frac{2}{\sqrt{\pi}} = \frac{2E}{\sqrt{\pi}} \left(\frac{q}{6m^*kT}\right)^{1/2}$$

At room temperature,

$$\nu = 10^{13} \left(E/10^5 \text{ V/cm}\right) \left(m/m^*\right)^{1/2} \text{ sec}^{-1} \tag{27}$$

Thus, carriers strike the interface approximately 10^{13} times a second for $m^* = m$ and peak silicon fields of 10^5 V/cm. Since $k_1 = \sigma\nu$, for cross sections of 10^{-15} cm^2, $k_1 = 10^{-2}$. k_3 will be of the same form except that the hole effective mass and cross section must be used.

The constants k_2 and k_4 are the attempt-to-escape frequencies of trapped electrons and holes, respectively, with the same meaning as for bulk traps. By using detailed balance arguments for the bulk case, it can be shown that (ref. 23)

$$k_2 = N_c v_{th} \sigma_n$$

and (28)

$$k_4 = N_v v_{th} \sigma_p$$

Using 10^{19} for N_c and N_v, 10^7 for v_{th}, and $\sigma_n = 10^{-15}$ and $\sigma_p = 10^{-17}$, $k_2 = 10^{11}$, and $k_4 = 10^9$ sec^{-1}.

In summary, the four constants in Eq. (10), k_1 through k_4, are given by

$$k_1 = 2E\left(\frac{q}{6\pi m_n^* kT}\right)^{1/2} \sigma_n \cong 10^{-2} \left(E/10^5\right) \left(m/m_n^*\right)^{1/2} \frac{\text{cm}^2}{\text{sec}}$$

$$k_2 = N_c v_{th} \sigma_n \cong 10^{11} \text{ sec}^{-1}$$

(29)

$$k_3 = 2E\left(\frac{q}{6\pi m_p^* kT}\right)^{1/2} \sigma_p \cong 10^{-4} \left(E/10^5\right) \left(m/m_p^*\right)^{1/2} \frac{\text{cm}^2}{\text{sec}}$$

$$k_4 = N_v v_{th} \sigma_p \cong 10^9 \text{ sec}^{-1}$$

5. Simplified Model. — In order to obtain an intuitive and straightforward solution to the question of the net charge remaining in traps after passage of a signal, certain simplifying assumptions have been made. First, it is assumed that a charge, $n_{s,o}$, is always present in the potential well. This establishes the occupation level before the signal charge arrives. Secondly, it is assumed that the signal charge is transferred into the well instantaneously at t = 0 and transferred out instantaneously at t = (1/2f) (two-phase operation). In addition, it is assumed that the magnitude of the signal is large enough to cause nearly all of the interface states to fill completely in times short compared with the period of operation. Since $\tau_{fill} = (1/k_1 n_s)$ and $k_1 = 10^{-2}$, this implies $n_s \geq 2 \times 10^8$ cm^{-2} for $\tau_{fill} = (1/2f)$ at 1 MHz, and for p-channel devices, $p_s \geq 2 \times 10^{10}$ at 1 MHz. At 10 MHz a somewhat larger signal level is required to satisfy this quick-filling assumption.

With these assumptions, it only remains to calculate the trap occupation at one-half a period after the free charge is transferred out, because virtually all charge released prior to this time will be able to rejoin the signal charge in the next potential well down the line. Since the excess trapped charge empties exponentially we can express the occupation at t = (1/2f) as

$$n_{ss}\left(t = \frac{1}{2f}\right) = \left[1 - f_{ss}(n_{s,o})\right] N_{ss}\, e^{-1/[2f\tau(\epsilon)]} \tag{30}$$

where $f_{ss}(n_{s,o})$ is the Fermi function appropriate for the zero level charge, $n_{s,o}$.

$$f_{ss}(n_{s,o} = \frac{1}{1 + \frac{k_2}{k_1 n_{s,o}} e^{-\epsilon/kT}} \tag{31}$$

and

$$\tau(\epsilon) = \frac{1}{k_2} e^{\epsilon/kT} \tag{32}$$

Since n_{ss} at the beginning of the transfer-in period ($t = -\frac{1}{2f}$) was determined by $n_{s,o}$, we have

$$n_{ss}\left(t = -\frac{1}{2f}\right) = f_{ss}(n_{s,o}) N_{ss} \tag{33}$$

The total number of carriers remaining behind in interface states is therefore

$$N_{LOSS} = \int_0^{\epsilon_g} \left[(1 - f_{ss})N_{ss}\, e^{-(1/2f\tau\epsilon)} - f_{ss}N_{ss} \right] d\epsilon \tag{34}$$

A further assumption which permits simple evaluation of this integral is that the quasi-Fermi levels define sharp cutoffs in occupation; i.e., all states above ϵ_Q are empty, all states below are full. Furthermore, in the emptying process, using Eq. (20) we define the energy where the states have emptied to 1/e of their initial level as the sharp-cutoff energy as follows

$$\epsilon_{1/e} = kT \ln (k_2 t) \tag{35}$$

With these assumptions and N_{ss} assumed constant in energy, we can simply write the number of carriers lost as

$$N_{LOSS} = N_{ss} \left[\epsilon_{1/e}\left(t = \frac{1}{2f}\right) - \epsilon_Q(n_{s,o}) \right] \tag{36}$$

$$N_{LOSS} = kTN_{ss} \ln \left(\frac{2f}{k_1 n_{s,o}} \right) \tag{37}$$

Figure 3 schematically follows the derivation of Eq. (37).

The loss per transfer is seen to increase with N_{ss} and f, but decrease as $n_{s,o}$ increases. The expression also predicts zero loss when

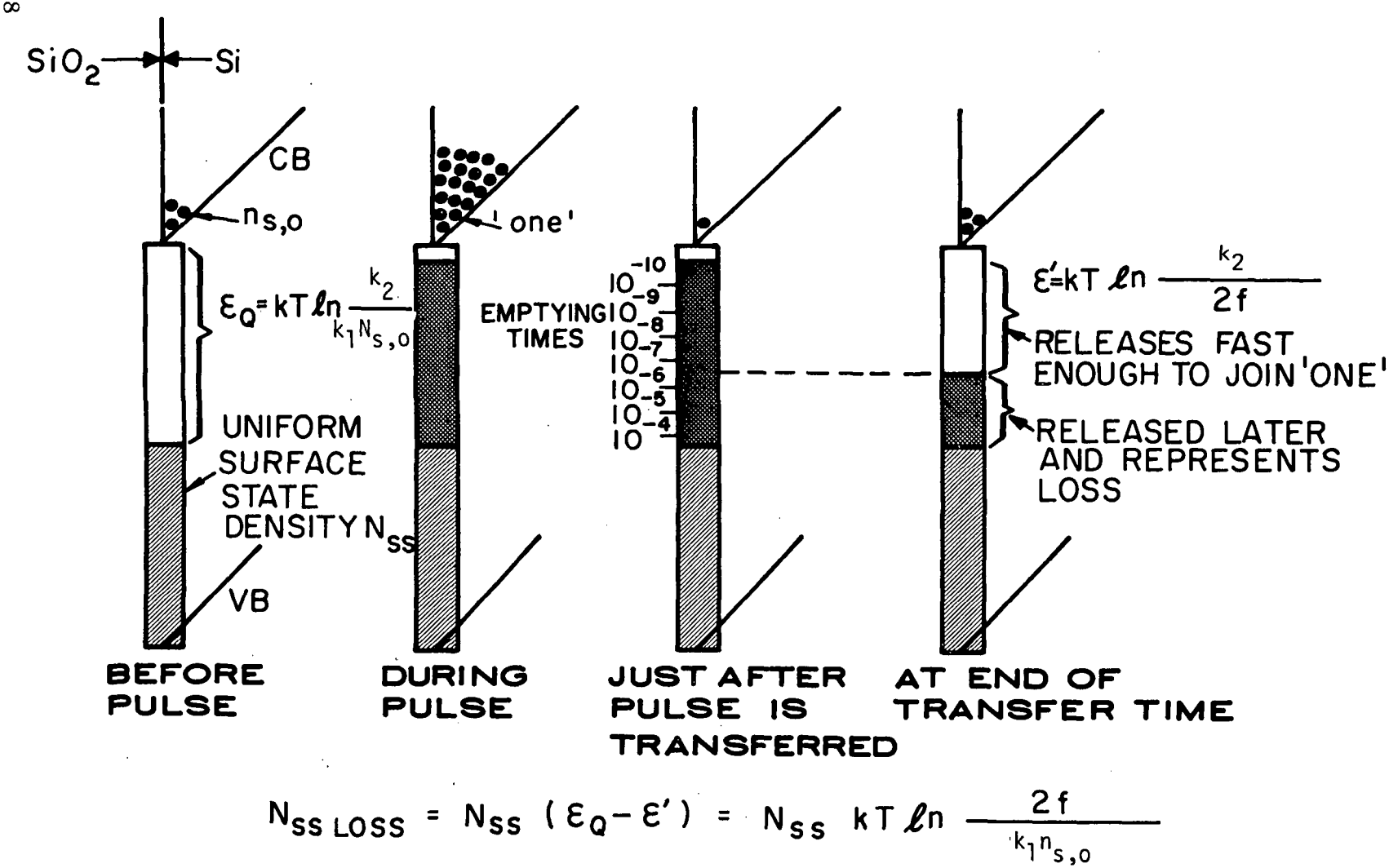
$$\frac{2f}{k_1 n_{s,o}} = 1 \tag{38}$$

which defines a cutoff frequency f_o as

$$f_o = \frac{k_1 n_{s,o}}{2} \tag{39}$$

When this condition is satisfied, the zero level charge is high enough so that the states are normally filled to an energy where the empty time is fast compared with the clock period; i.e., by $t = \frac{1}{2f}$ the states have emptied as much as they are going to.

This condition of absolutely zero loss is physically highly improbable and comes about mainly because of the unrealistic sharp-cutoff approximation used to aid in the evaulation of the integral of Eq. (34). When Eq. (34) is calculated numerically, the results indicate



$$N_{ss\,LOSS} = N_{ss}\,(\varepsilon_Q - \varepsilon') = N_{ss}\,kT\,\ell n\,\frac{2f}{k_1 n_{s,o}}$$

Figure 3. Schematic representation of the "before-after" sharp-cutoff interface state model.

that the losses do not go to zero quite so rapidly as suggested by Eq. (37). Rather, at frequencies below f_o, the number of carriers lost starts to depend linerarly upon f according to

$$N_{LOSS}\,(f < f_o) = kTN_{ss}\,\frac{f}{f_o} \tag{40}$$

Figure 4 shows a plot of N_{LOSS}/kTN_{ss} vs. f/f_o. The solid line is the sharp-cutoff approximation [Eq. (37)] while the dotted line joins the computer-calculated points.

The most important loss quantity for comparison purposes is the fractional loss ϵ_s, the fraction of the signal charge lost at each transfer.

$$\epsilon_s = \frac{N_{LOSS}}{N_{SIG}} \tag{41}$$

Since N_{LOSS} is independent of signal level provided N_{SIG} is large enough to cause rapid filling of all states, we expect interface state fractional losses to be inversely dependent upon signal level.

The expressions derived thus far have been for the loss experienced by a single signal pulse. However, if signal pulses arrive periodically so that sufficient time has not elapsed for the interface states to reach the occupation determined by the zero-level charge $n_{s,o}$, the occupation level at the beginning of the transfer-in period will be determined by the time since the last pulse, n_{zero}/f, where n_{zero} is the number of clock pulses since the last signal pulse, or the number of zeros. Then using Eq. (35) to express the energy to which the states have decayed, the number lost in the case of periodic pulses can be written:

$$N_{LOSS}^{PERIODIC\ PULSE} = kTN_{ss}\left(\ln\frac{k_2 n_{zero}}{f} - \ln\frac{k_2}{2f}\right) = kTN_{ss}\ln 2n_{zero} \tag{42}$$

using the sharp-cutoff approximation. This will only be valid provided

$$\epsilon_{1/e}\left(t = \frac{n_{zero}}{f}\right) < \epsilon_Q\ (n_{s,o})$$

or when

$$n_{zero} \leqslant \frac{f}{2f_o} \tag{43}$$

6. Fat Zero Operation. — So far, only a large signal model with a constant background charge has been considered. A constant background charge is unrealistic when complete emptying of the well occurs every cycle. To ascertain the occupation level of fast states in the presence of

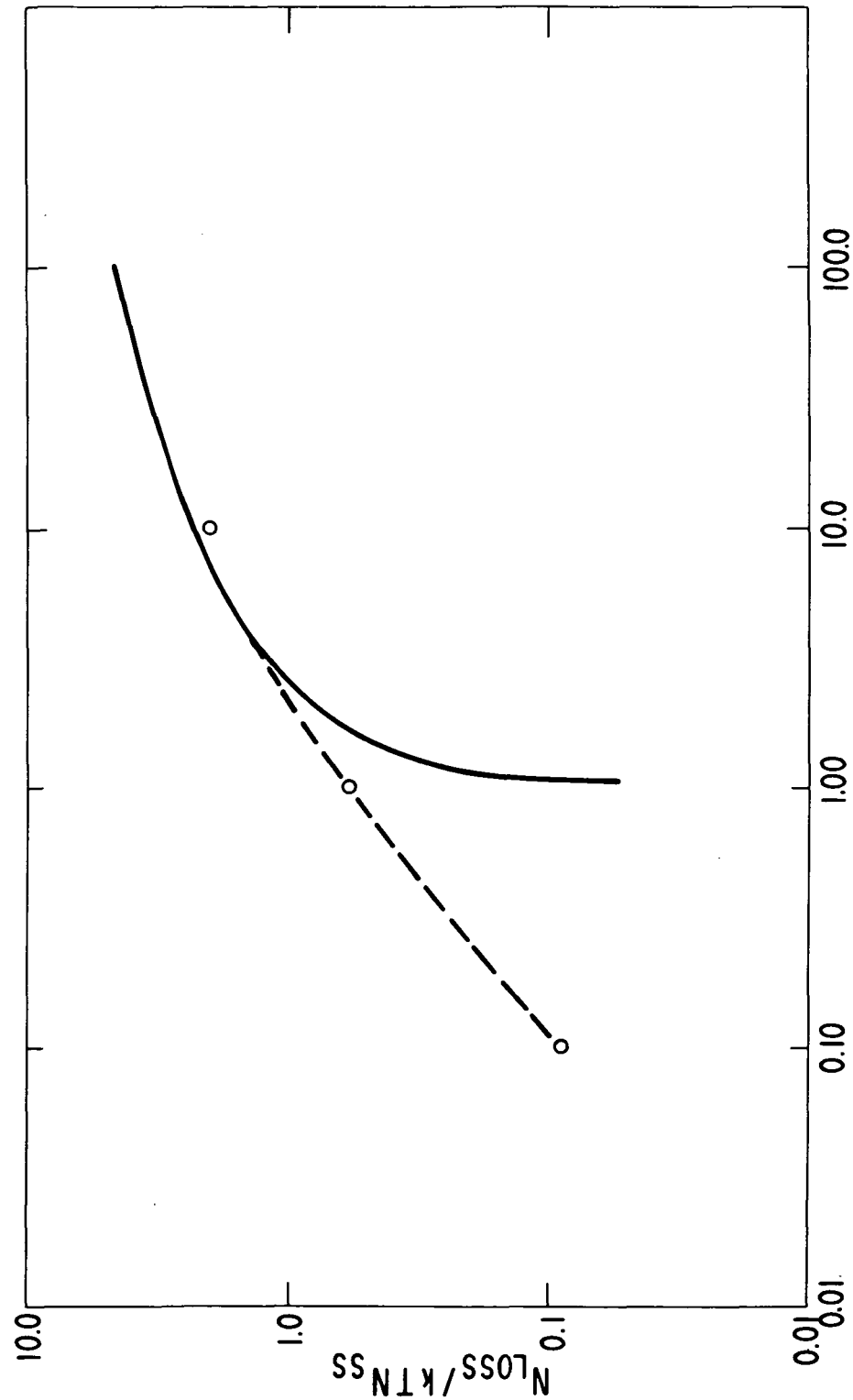


Figure 4. Normalized interface state losses vs. normalized frequency.

a "fat-zero" of concentration $n_{s,o}$ which is completely removed every half cycle one must find the occupation profile such that the total number of carriers trapped during one-half cycle is the same as the number released during the next half-cycle, or

$$\left(N_{ss} - n_{ss}(0)\right)\left(1 - e^{-f_o/f}\right) = \left[n_{ss}(0) + \left(N_{ss} - n_{ss}(0)\right)\left(1 - e^{-f_o/f}\right)\right]\left(1 - e^{-(1/2f\tau)}\right) \qquad (44)$$

trapped while fat zero present

released while fat zero absent

The occupation at the beginning of a transfer-in period is then

$$n_{ss}(0) = \frac{N_{ss}\left(1 - e^{-f_o/f}\right)}{e^{1/2f\tau} - e^{-f_o/f}} \qquad (45)$$

where

$$\tau = \frac{1}{k_2}\, e^{\epsilon/kT} \qquad (46)$$

Assuming the signal level is large enough to rapidly fill all states completely, the total loss from a signal pulse into all energy levels is then

$$N_{LOSS} = \int_0^{\epsilon_g} \left(N_{ss}\, e^{-(1/2f\tau)} - n_{ss}(0)\right) d\epsilon \qquad (47)$$

$$N_{LOSS} = N_{ss} \int_0^{\epsilon_g} \left[e^{-1/2f\tau} - \frac{\left(1 - e^{-f_o/f}\right)}{\left(e^{(1/2f\tau)} - e^{-f_o/f}\right)}\right] d\epsilon \qquad (48)$$

This integral has not yet been evaluated, and it appears that the losses for fat zero operation should have a different frequency dependence than those when a constant background charge exists.

7. Further Model Refinements. — All calculations made to this point assume that the signal is large enough to cause essentially complete filling of all fast states in a time short compared with period of operation. When this is not the case, i.e., for the small signal case, the states fill only partially while the signal charge resides in the well. Between $t = -\frac{1}{2f}$ and $t = 0$, the states fill exponentially from their initial value toward their new steady-state value according to

$$n_{ss}(t) = n_{ss}(-\tfrac{1}{2f}) \left[n_{ss}(\infty) - n_{ss}(-\tfrac{1}{2f}) \right] \left[1 - e^{-k_1 n_{s,o} (t + \frac{1}{2f})} \right] \tag{49}$$

where

$$n_{ss}(\infty) = f_{ss}(n_s)\ N_{ss} \tag{50}$$

and

$$n_{ss}\ (-1/2f) = f_{ss}(n_{s,o})\ N_{ss} \tag{51}$$

for constant background charge or Eq. (45) for fat zero operation. Note that transfer-in begins at $t = -\frac{1}{2f}$. At $t = 0$ the occupation will be

$$n_{ss}(0) = n_{ss}\left(-\frac{1}{2f}\right) + \left[n_{ss}(\infty) - n_{ss}\left(-\frac{1}{2f}\right) \right] \left(1 - e^{-f_o/f} \right) \tag{52}$$

After $t = 0$, when the signal charge is removed, this occupation will decay toward $N_{ss} f_{ss}(n_{s,o})$ for the case of constant background charge or toward zero for fat zero operation. The total loss for each case is thus

$$N_{LOSS} = \int_0^{\epsilon_g} \left[\left\{ n_{ss}\left(-\frac{1}{2f}\right) + \left[n_{ss}(\infty) - n_{ss}\left(-\frac{1}{2f}\right) \right] \left(1 - e^{-f_o/f} \right) - N_{ss} f_{ss}(n_{s,o}) \right\} e^{-t/\tau} - N_{ss} f_{ss}(n_{s,o}) \right] d\epsilon \tag{53}$$

constant background charge

$$N_{LOSS} = \int_{\substack{\text{fat zero} \\ 0}}^{\epsilon_g} \left[\left\{ n_{ss}\left(-\frac{1}{2f}\right) + \left[n_{ss}(\infty) - n_{ss}\left(-\frac{1}{2f}\right) \right] (1 - e^{-f_o/f}) \right\} e^{-t/\tau} - n_{ss}(-1/2f) \right] d\epsilon \quad (54)$$

Neither of these integrals has been evaluated at this time.

Another refinement which must be made to properly account for actual fast state losses in CCD's concerns the shape of the potential wells which are storing charge. The expressions for loss derived so far show strong dependences upon the background charge level. If the potential wells do not have a constant surface potential at all points, then the small amount of background charge or fat zero will accumulate in the regions of lowest potential leaving other areas devoid of charge. The larger packets of charge representing signal will see portions of the well which have had little or no background charge. A complete interface state loss model must take this effect into account.

III. TWO-PHASE CHARGE-COUPLED SHIFT REGISTERS

A. Two-Phase Charge Coupled Structures

1. Types of Two-Phase CCD's. — The charge-coupled devices initially described by Boyle and Smith (ref. 1) require three or more phase clocks to obtain the directionality of the signal flow. However, for most applications such as self-scanning photosensor arrays or digital shift registers, high packing density and better performance may be achieved with two-phase charge-coupled structures. As illustrated in Figure 5, the asymmetrical potential wells or

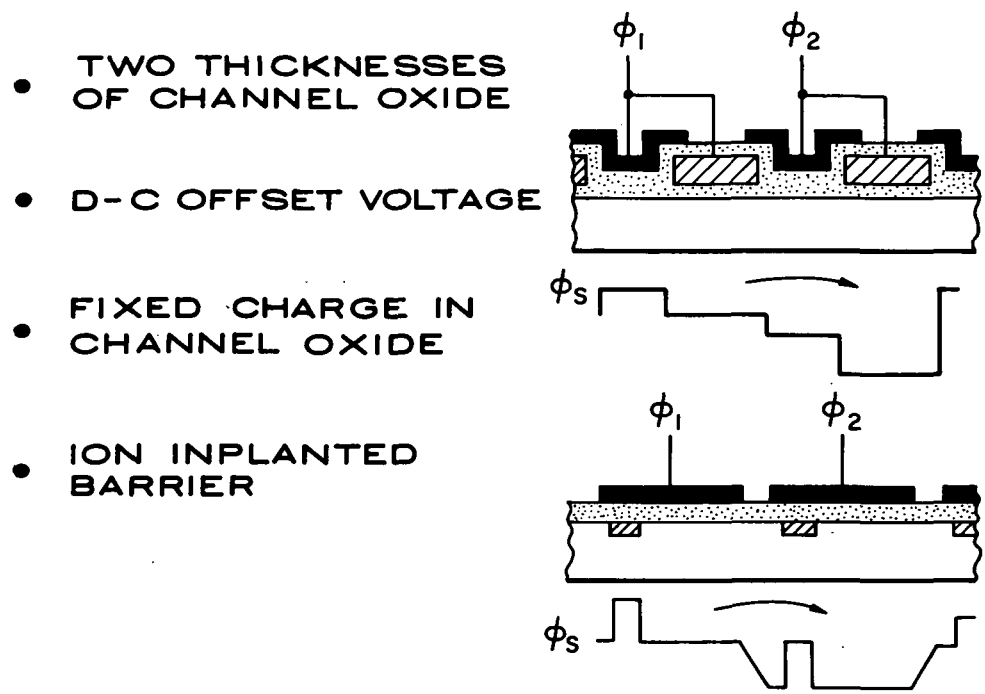


Figure 5. Types of two-phase charge-coupled structures.

barriers in the surface potential, needed to provide the directionality of the information flow for the two-phase operation, can be achieved by incorporating into the charge-coupled structures one of the following features:

(1) two thicknesses of the channel oxide,
(2) dc offset voltage between two adjacent gates powered by the same phase voltage,

(3) two levels of fixed charge in the channel oxide, or

(4) ion-implanted barriers (ref. 9).

The first three of the above two-phase charge-coupled shift registers can be conveniently implemented by self-aligned, closely spaced structures in the form of polysilicon gates overlapped by aluminum gates (refs. 2-4). In this section we will describe specifically the construction of two-phase CCD's with two different thicknesses of channel oxide for polysilicon and aluminum gates that were used as the test devices in the experimental part of this study. However, in view of the self-aligning characteristic of this structure and the available two-layer metallization, basically the same construction can be used to implement two-phase CCD's employing a dc offset voltage between the adjacent polysilicon and aluminum gates powered by the same phase voltage pulse train. The externally introduced dc offset voltage, however, can also be replaced by a difference in fixed charge in the channel oxide between the polysilicon and the aluminum gate. Such fixed charge can be introduced either by injection of charge under one set of gates or by fabricating the devices with different types of channel oxide under the two other sets of gates. The deposited Si_3N_4 and Al_2O_3 are examples of two other types of channel oxides that can be used for this purpose in addition to the thermally grown SiO_2.

2. Fabrication of Experimental Structures. — The fabrication of the test devices is illustrated in Figure 6. The substrate used was 1.0 to 0.5 ohm-cm n-type silicon with <111> orientation. As shown in (a) the p^+-diffusion and the field oxide for these devices were prepared following a standard thick-oxide p-MOS process. Boron nitride deposition at 1000°C was used as the doping source for the p^+-diffusions. The field oxide was made as a combination of 7000-Å steam SiO_2 grown at 1100°C followed by 5000-Å deposited SiO_2. The next sequence of the process step, as shown in (b), consisted of thermally growing approximately 1000-Å-thick channel oxide, depositing the polysilicon film, and defining it into the polysilicon gates. Then as shown in (c) a second layer of channel oxide is thermally grown for the aluminum gates to a total thickness of 3000 Å. This last step also results in the formation of an insulating layer over the polysilicon gates which is approximately 2500-Å thick. Finally as shown in (d), the device structure was completed by opening contacts to the p^+-diffusions and the polysilicon gates, depositing about 10,000-Å-thick aluminum, and defining it into the aluminum gates.

3. Description of Experimental Devices. — Three arrays of charge-coupled devices were made in this study. The first experimental device successfully operated with a two-phase 12-stage

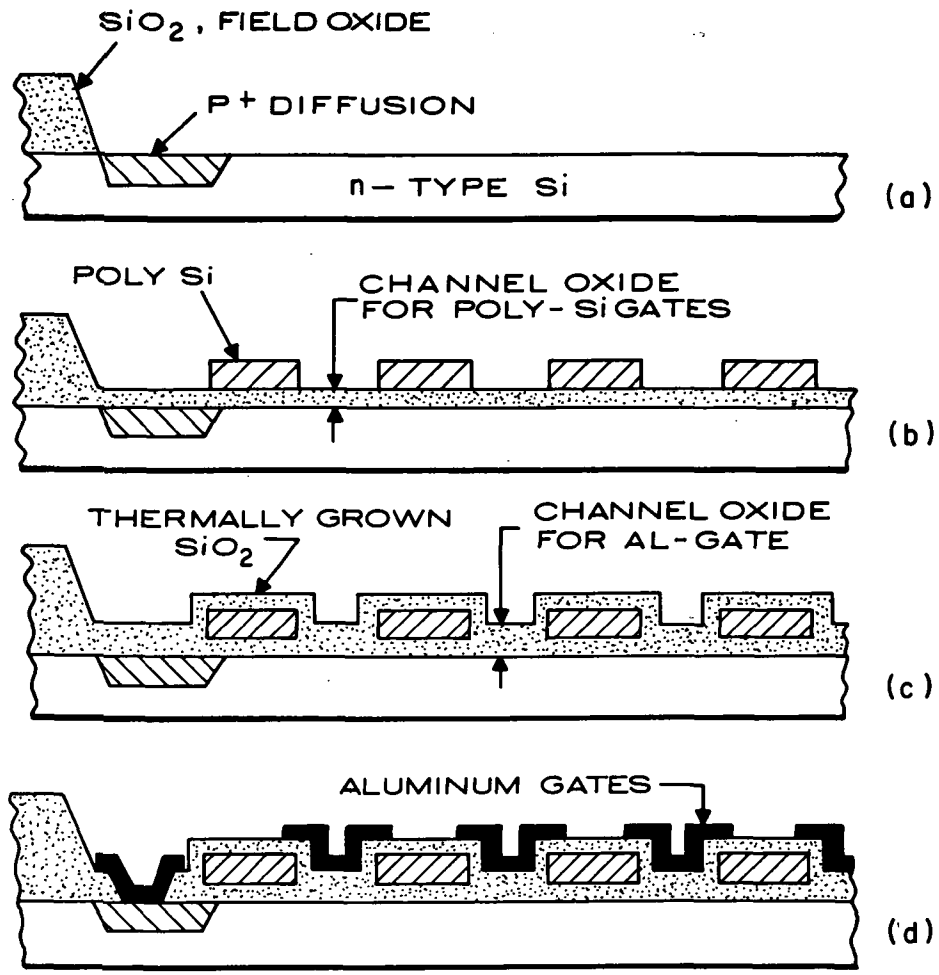


Figure 6. Construction of the experimental charge-coupled devices.

shift register, CCD-3. The construction of this device is illustrated by the photomicrograph in Figure 7 and the cross-sectional view in Figure 8. As shown, this device has nominally 0.7-mil-long polysilicon electrodes and 0.3-mil-long aluminum electrodes that add up to 2 mils per stage. The channel width for these devices is 10 mils.

The photomicrographs of CCD-6 and CCD-5 arrays are shown in Figures 9 and 10. The CCD-6 array contains 16- and 32-stage shift registers with 2.0-mil-long stages, and 32- and 64-stage shift registers with 1.2-mil-long stages. The CCD-5 array consists of 32- and 64-stage shifters with 2-mil-long stages, and 64- and 128-stage shift registers with 1.2-mil-long

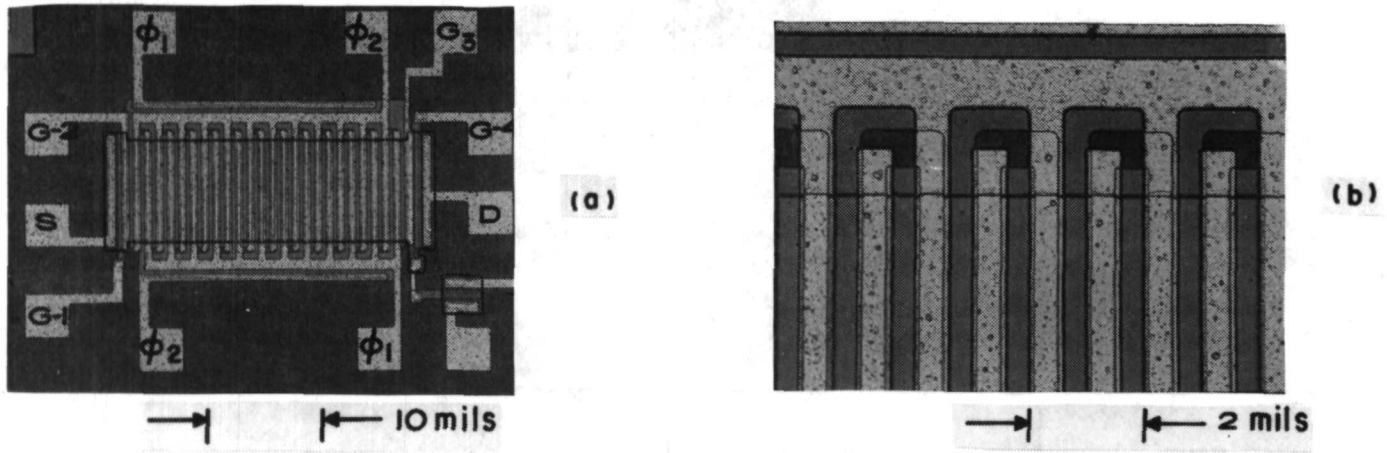


Figure 7. (a) Photomicrograph of the CCD-3 12-stage shift register. (b) Magnified section of the devices showing how the polysilicon and aluminum gates extend outside the channel oxide region. The dark areas represent the field oxide; the gray areas are the polysilicon gates; and the light areas are the aluminum gate.

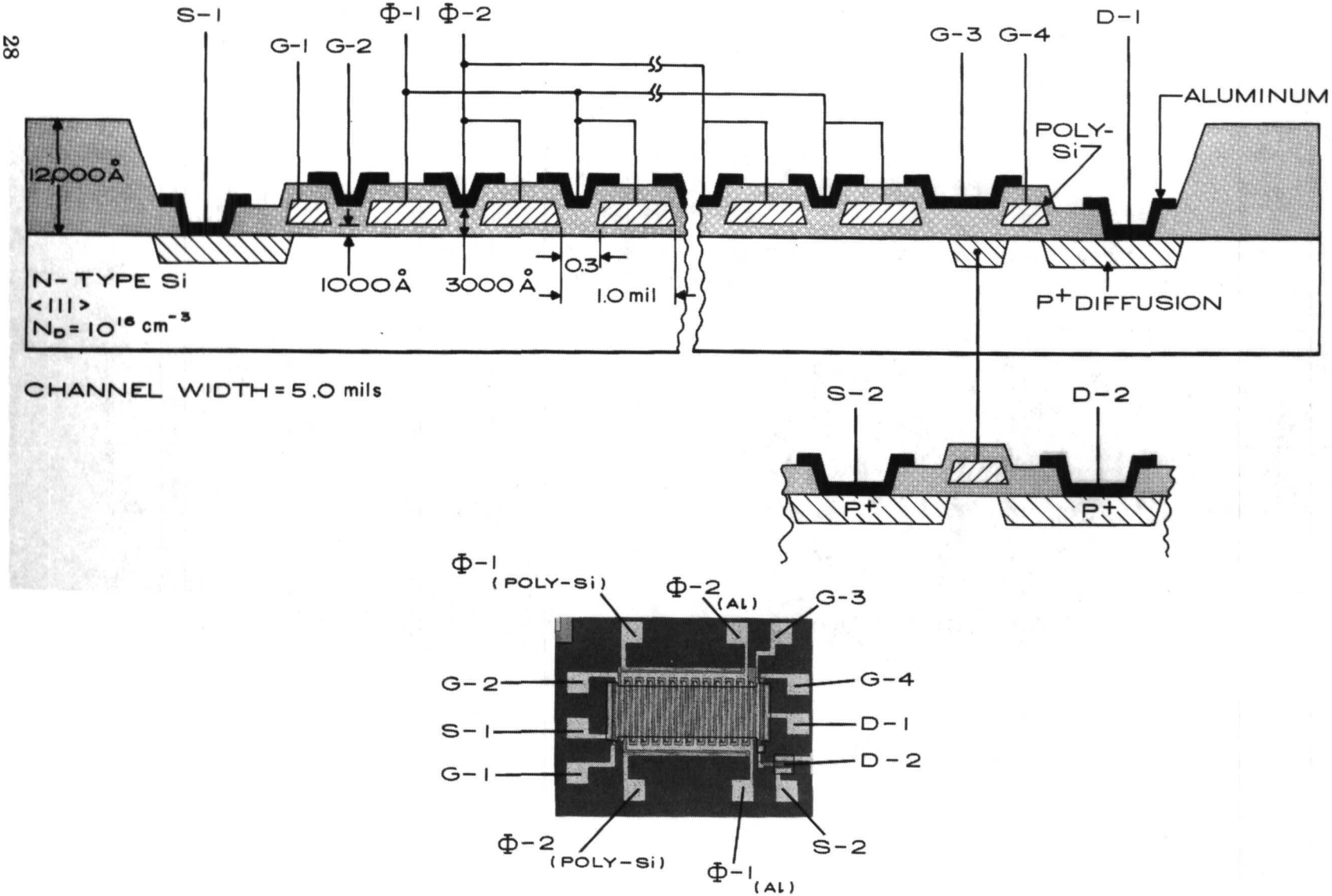


Figure 8. Cross-sectional view and a labeled photograph of the 12-stage shift-register CCD-3.

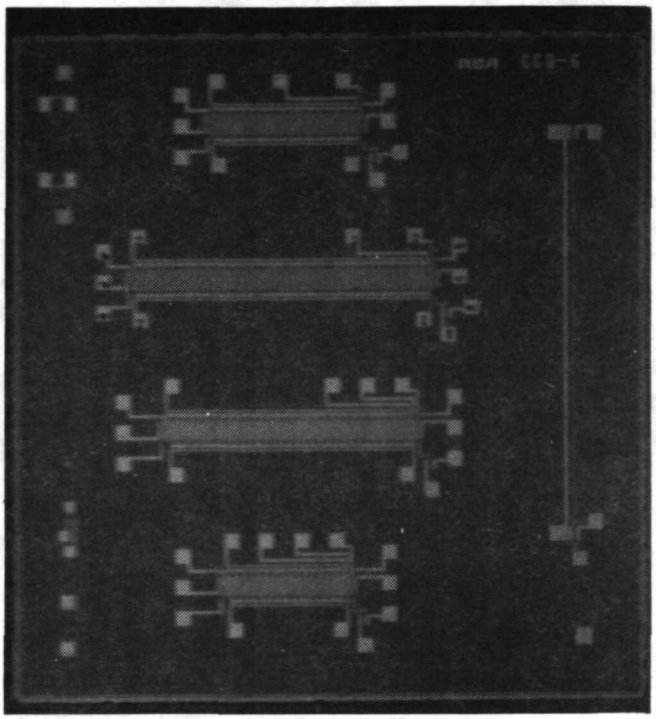


Figure 9. Photomicrograph of CCD-6.

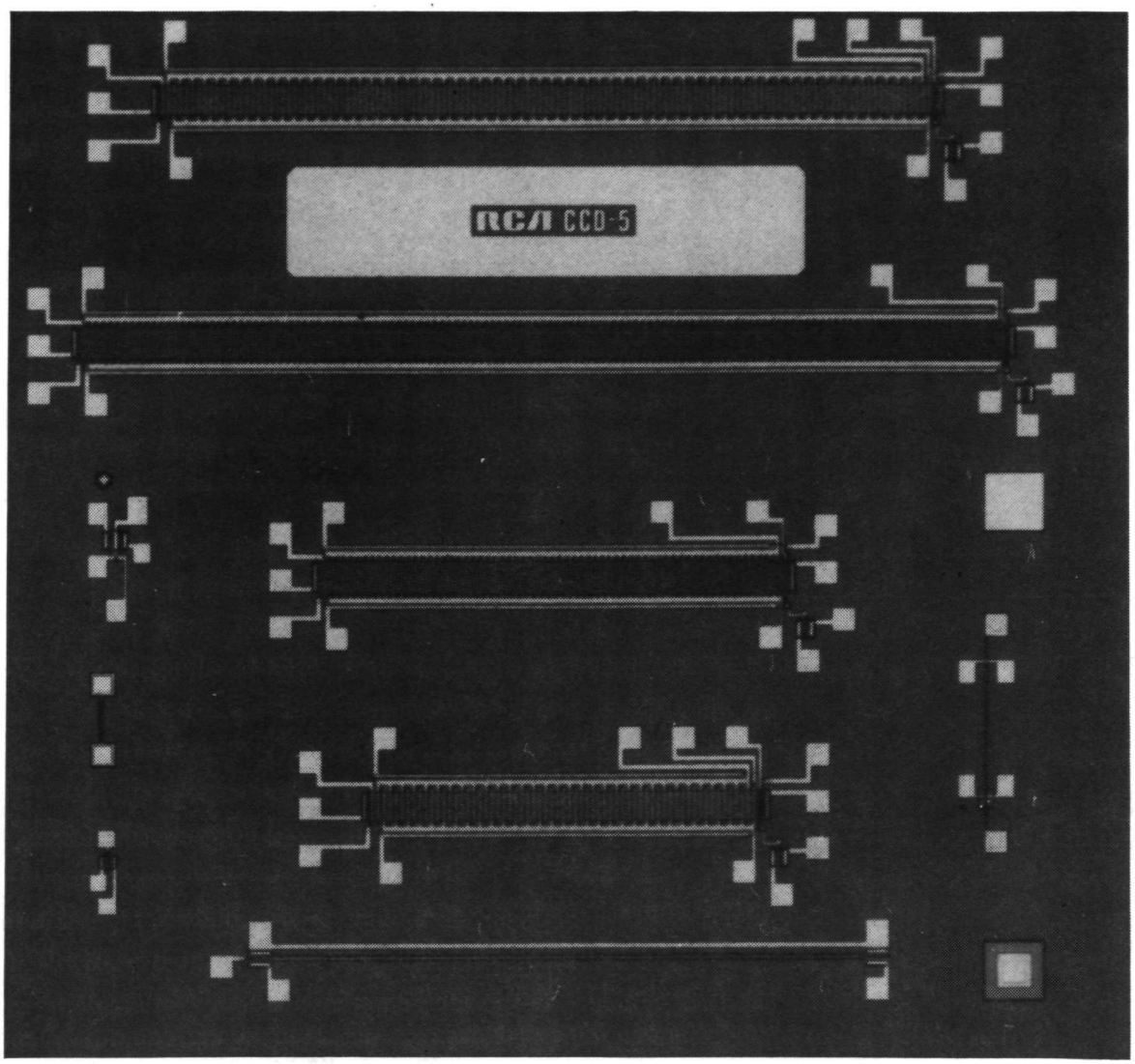


Figure 10. Photomicrograph of CCD-5.

stages. The construction of the two types of shift registers having 2.0- and 1.2-mil-long stages is illustrated in Figures 11 and 12, respectively. It should also be noted that the general layout of all experimental devices followed the same design patterns except for the variations in number of stages and the differences in the output circuits that are illustrated in Figures 8, 11, and 12. As shown in these figures, all of the devices have the same input stages consisting of a source diffusion S-1 and input gates G-1 and G-2. Separate electrical access has also been provided to the polysilicon and aluminum electrodes of each phase; i.e., ϕ-1(poly), ϕ-1(Al), ϕ-2(poly), and ϕ-2(Al). In addition to the variations in the width of the channels and length of the gates for the coarser and finer structures, the three different structures illustrated by Figures 8, 11, and 12 have variations in the design of the output stages. In each case the output can be detected as the current flow out of the drain diffusion D-1 or as a voltage change resulting from the charge signal introduced on the floating diffusion that, in turn, controls the gate voltage of a 3-mil-wide output MOS device with a source S-2 and drain D-2. In the case of the structure shown in Figure 11, three electrodes, G-3, G-4, and G-5, are externally available for controlling the signal flow in and out of the floating diffusion. However, only two electrodes, G-3 and G-4, are externally accessible in the case of the structures shown in Figures 8 and 12.

The test devices were mounted in 28-lead ceramic packages and the two types of bonding diagrams used for the experimental samples are illustrated in Figures 13 and 14.

4. Operation of Two-Phase CCD's. — Assuming essentially zero fixed charge in the channel oxide, substrates with relatively large doping concentrations are required to obtain a substantial difference between the surface potential under the polysilicon gates and the potential under the aluminum gates powered by the same phase voltage. The operation of such a device is illustrated in Figure 15, showing a computer solution for a two-phase structure with substrate doping concentration of $N_D = 10^{16} cm^{-3}$ and channel oxide thickness of 1000 Å and 3000 Å under the polysilicon and aluminum gates, respectively. Since in this case the potential barrier formed under the aluminum gate with respect to the surface potential under the polysilicon gate of the same phase is not constant as the phase voltage changes. The maximum amount of charge signal that can be stored and transferred will depend to some degree on the waveshapes of the phase voltages. These waveshapes may be symmetrical with equal rise time and fall time [see Figure 16(c)], nonoverlapping, or overlapping. In the overlapping case, illustrated in Figure 15, the transfer of charge is preceded by the condition in which both phase voltages are minimum. If we can assume that the signal charge will be originally contained in the potential well indicated by the phase-1 gate, then as the phase

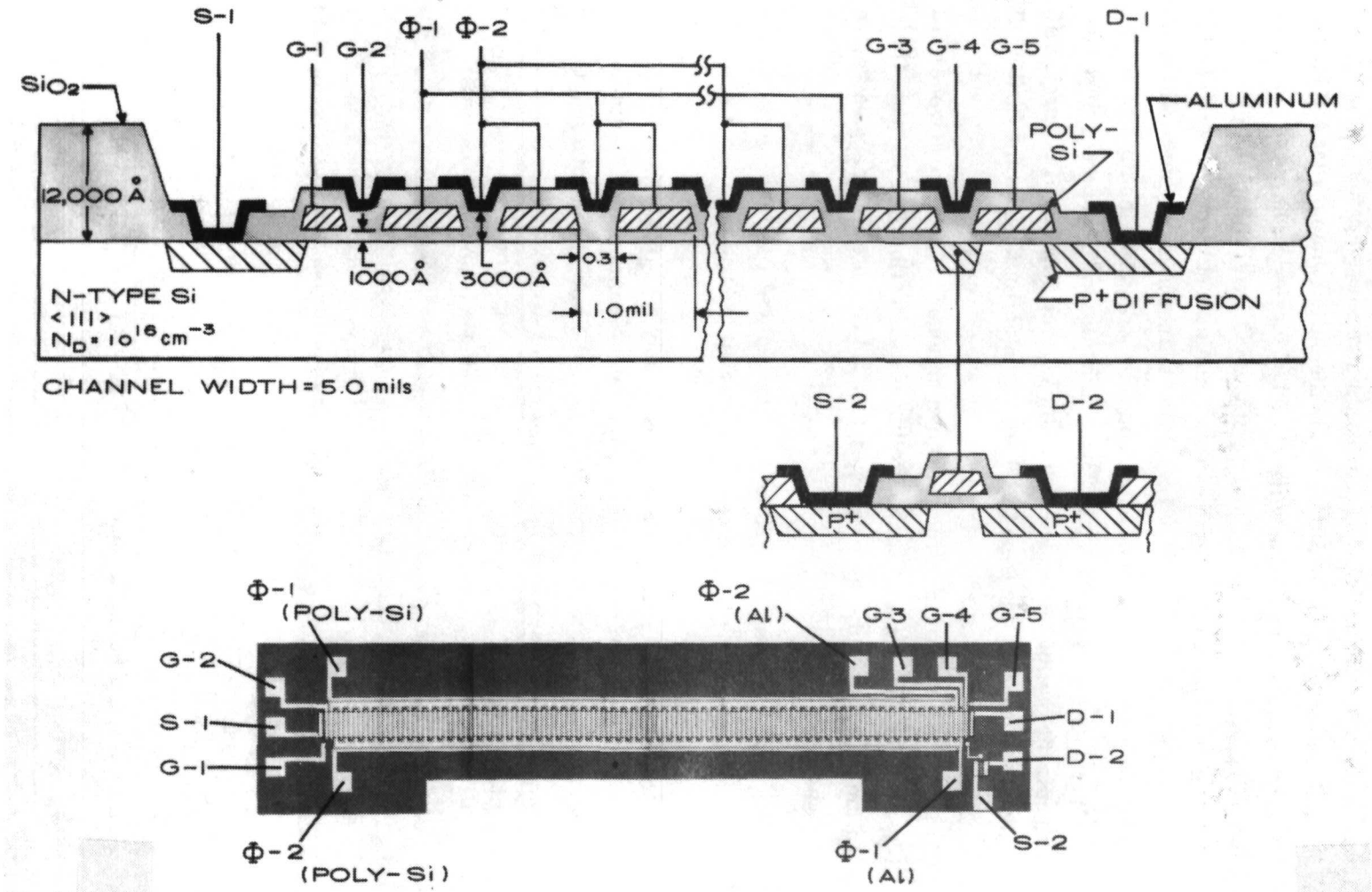


Figure 11. Cross-sectional view and a labeled photograph of CCD-5 64-stage shift register with 2-mil-long stages.

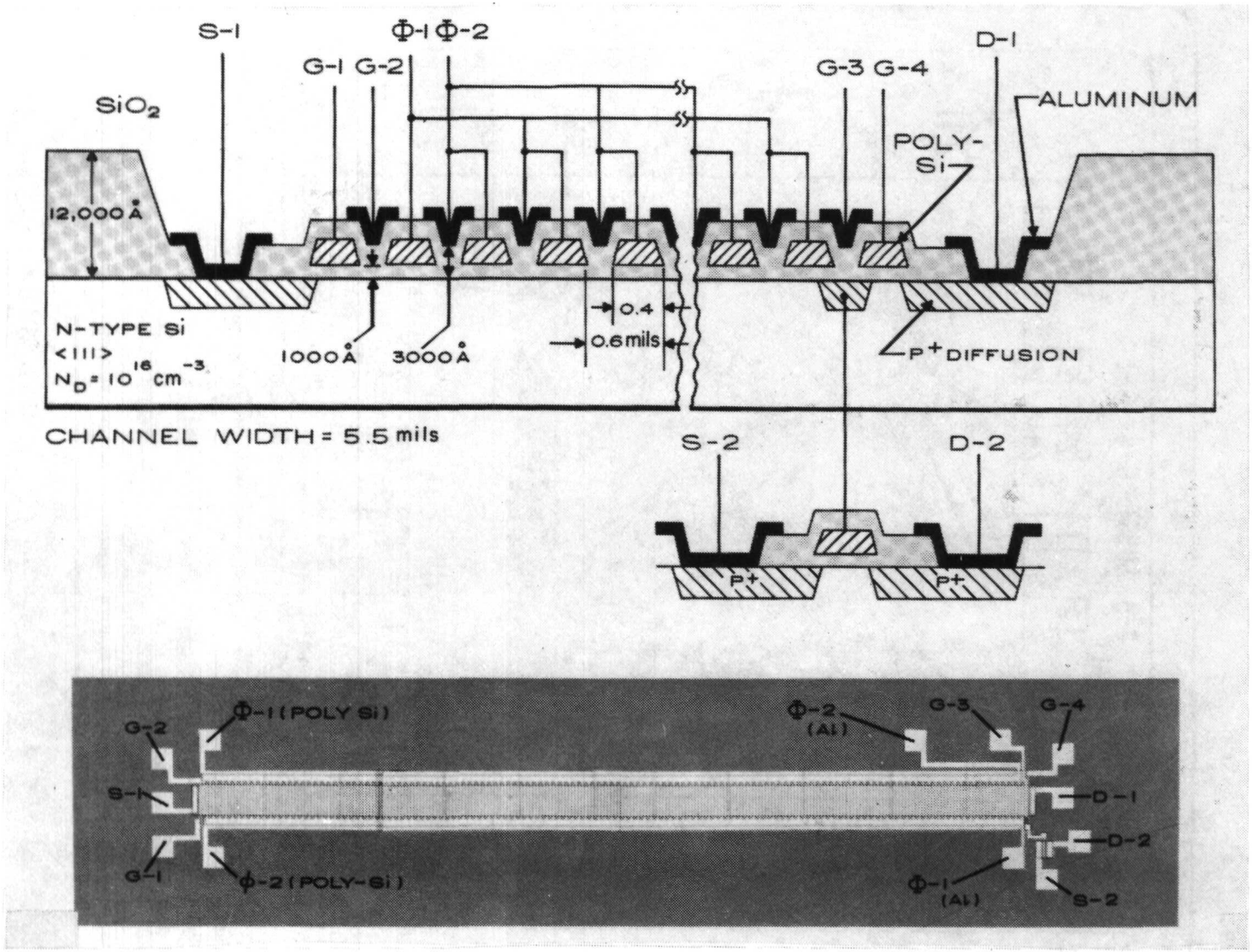


Figure 12. Cross-sectional view and a labeled photograph of CCD-T 128-stage shift register.

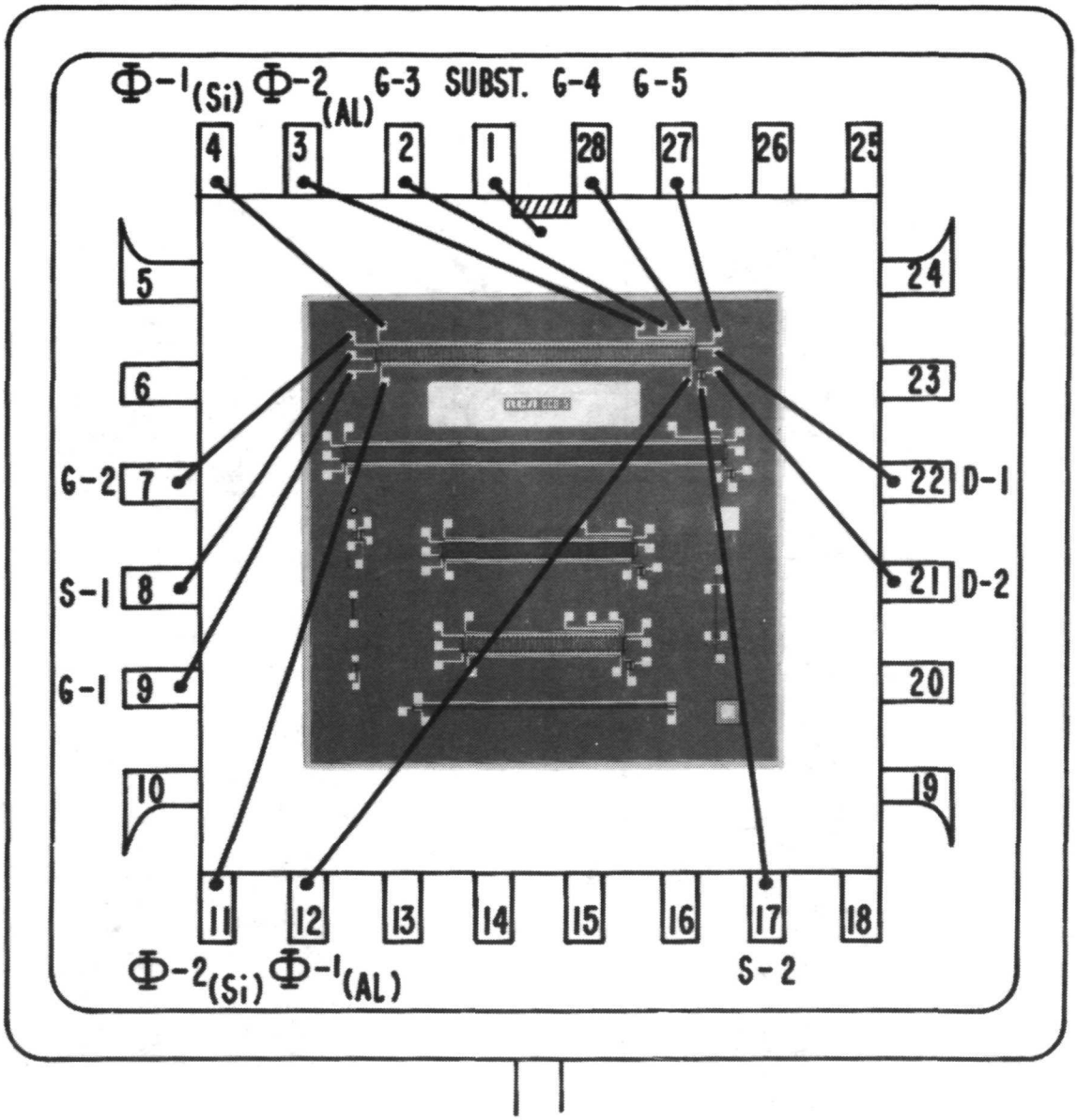


Figure 13. Bonding diagram for the CCD-5 64-stage shift register with 2-mil stages.

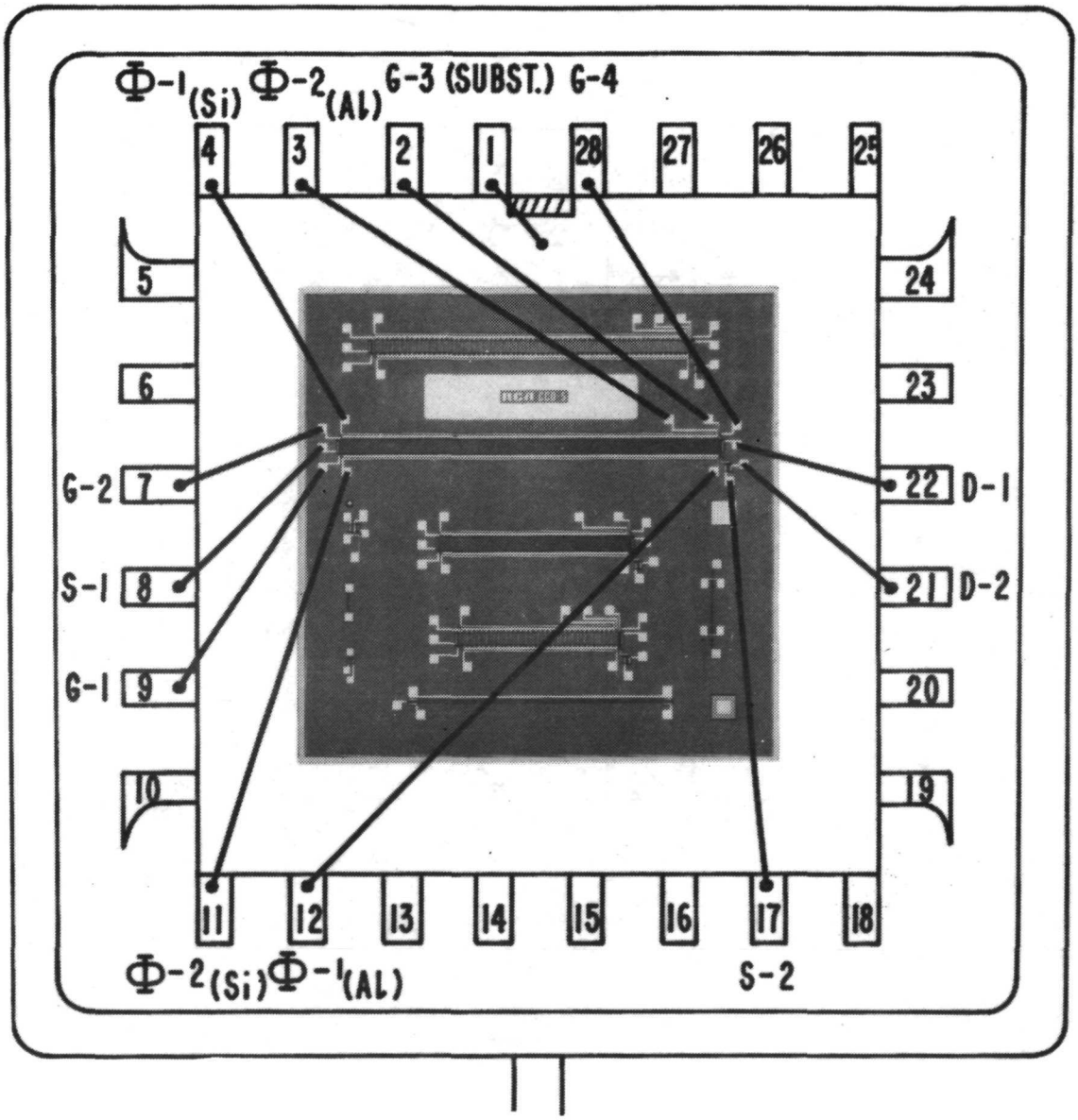


Figure 14. Bonding diagram for the CCD-5 128-stage shift register with 1.2-mil stages.

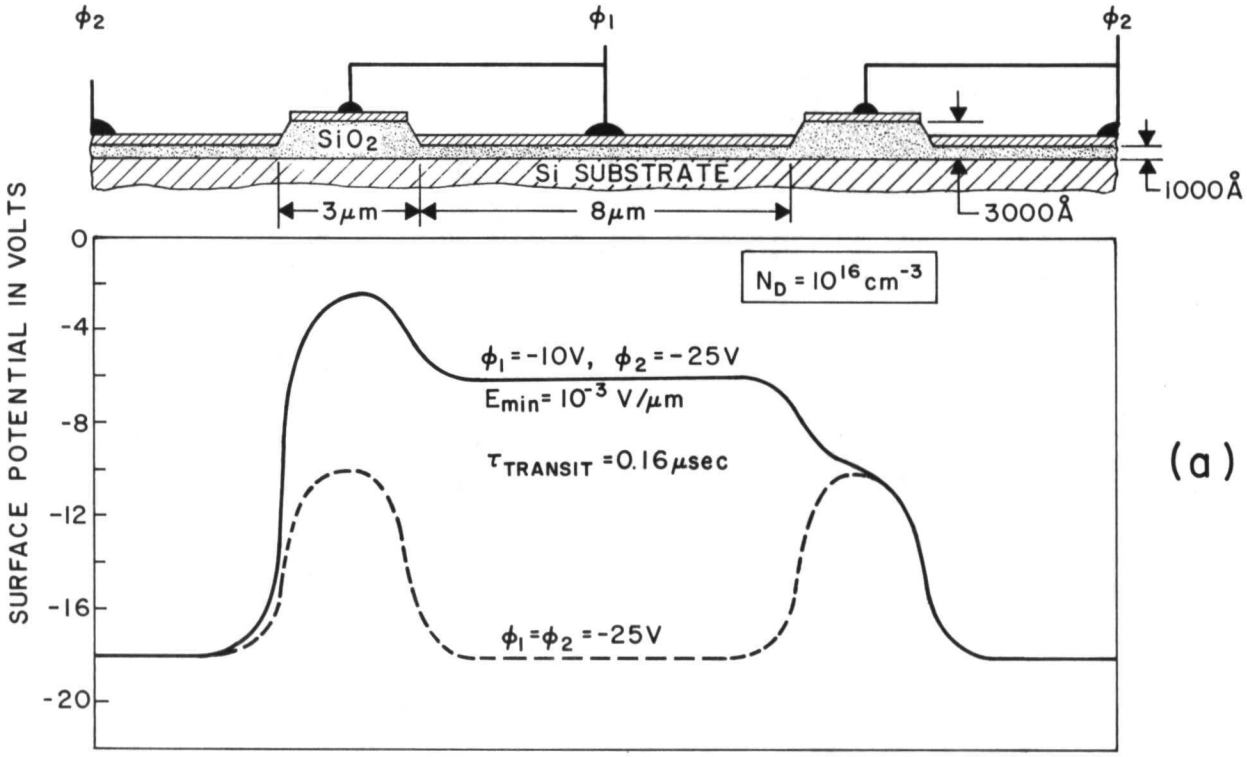


Figure 15. Computer solutions for the surface potential of two-phase CCD using 1000 Å channel oxides.

voltage ϕ_1 is changed from $\phi_1 = -25$ V to $\phi_1 = -10$ V, and the surface potential is raised from the dotted line to the solid line, the charge signal is transferred to a new potential well on the right side under the phase-2 gate. This mode of operation for two-phase charge-coupled devices will be referred to as the "complete charge-transfer" mode.

The complete charge-transfer mode operation is again illustrated in Figure 16 by two profiles of the surface potential. In this case at time t_1, the charge signal is accumulating in the potential wells under the phase-2 gates; and in the second half-cycle the charge signal will be transferred to the potential wells under the phase-1 gates.

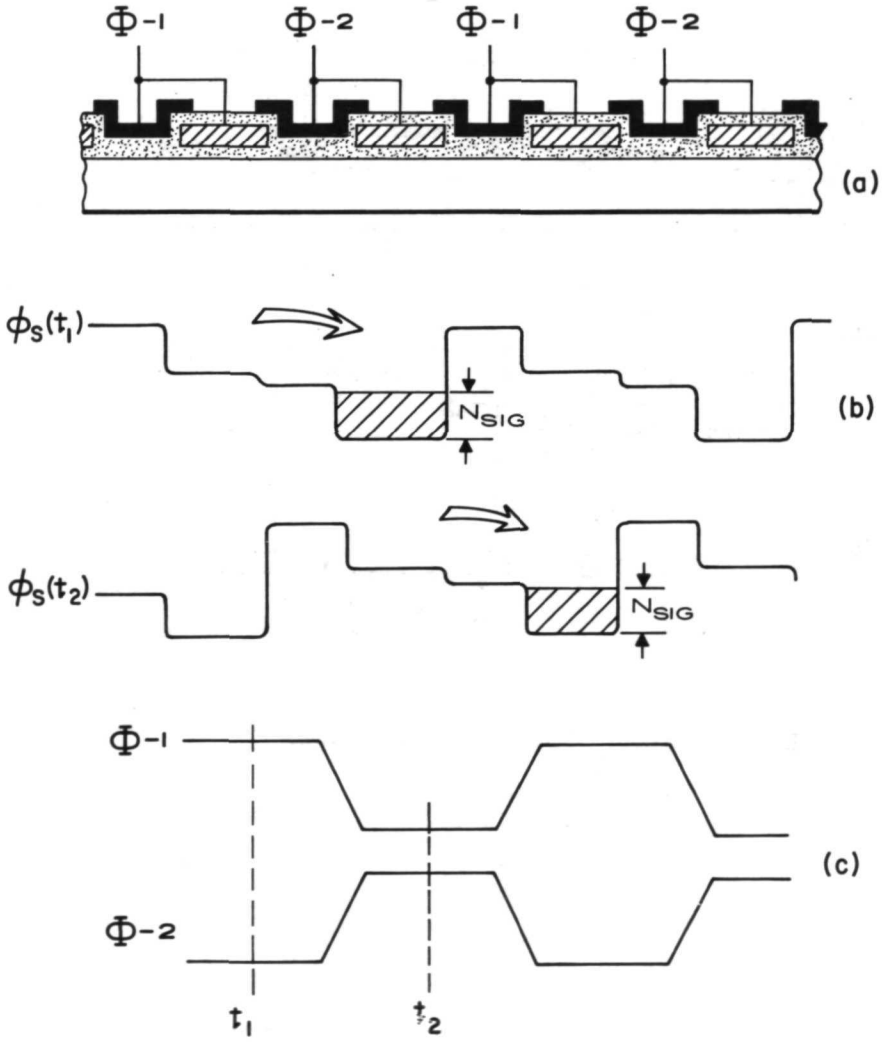


Figure 16. Complete charge-transfer operation of two-phase CCD.

Another mode of operation of two-phase charge-coupled devices is illustrated in Figure 17. In this case a barrier in the surface potential under the aluminum gates is so high that the potential wells under the polysilicon gates can never be completely emptied. In other words, the surface potential under the polysilicon gates powered by the minimum phase voltage is lower than the surface potential under the aluminum gates powered by the maximum phase voltage. This mode of operation will be referred to as the "bias-charge" or "bucket-brigade" mode. The bias charge N_{BIAS} illustrated in Figure 17(b) represents the background charge always present under the gates accumulating or storing the charge signal. In the steady-state operation of such charge-coupled shift registers, the bias charge will be maintained by thermal generation process.

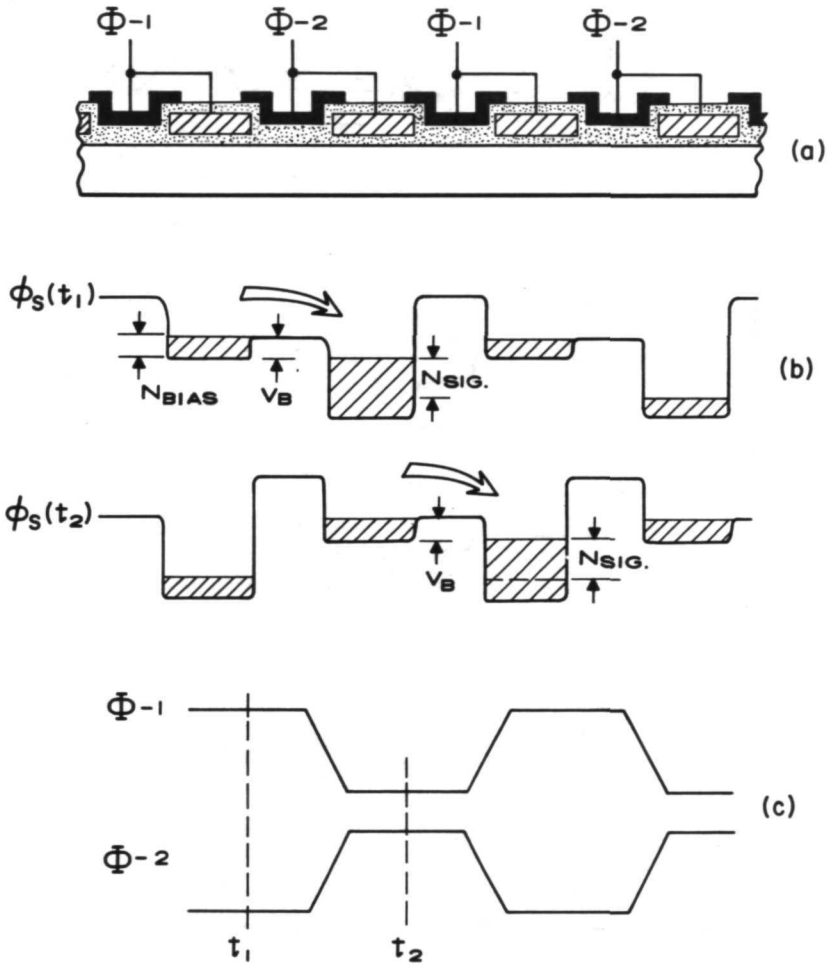


Figure 17. Bias-charge (bucket-brigade) mode of operation of two-phase CCD.

The transition from the complete charge-transfer mode to the bias-charge mode of operation can take place by increasing the dc bias level on the phase voltages. The presence of positive charge in the channel oxide in the case of n-channel devices will also increase the barrier under the aluminum gates above the values indicated for the example shown in Figure 15. The bias-charge mode of operation of two-phase charge-coupled shift registers is very similar to the operation of bucket-brigade (ref. 21) shift registers. In the bucket-brigade case the bias-charge regions are replaced by floating diffusions; otherwise, the operation of these two types of shift registers is very similar.*

As was generally known in connection with the operation of a bucket-brigade shift register (refs. 21, 22), a two-phase charge-coupled shift register can also be operated with one of the phases dc biased at a voltage halfway between the minimum and the maximum voltage applied to the other phase. This "one-phase" operation, or rather one-clock, is illustrated in Figure 18 and experimentally demonstrated by the waveforms in Figure 32. A uniphase charge-coupled structure (ref. 5) requiring only one set of externally controlled gates requires that the dc-biased phase shown in Figure 18 is replaced by a built-in bias in the structure which may be obtained by the presence of fixed charge in the channel oxide.

B. Experimental Testing of Two-Phase Devices

1. Test Setup. — The circuit used for the testing of the experimental two-phase shift registers is shown in Figure 19. The input signal is introduced into the shift register under the control of dc bias voltages E_S and $E_{G\text{-}S}$ and an input pulse V_{in}. The phase voltage clocks ϕ-1 and ϕ-2 are applied with dc bias E_ϕ. The output gate G-3 is connected to the phase voltage ϕ-1, and the output gate G-4 is biased at a voltage $E_{G\text{-}D}$ which is less negative than the drain bias voltage E_D. The output signal is sensed directly as current $I_{D\text{-}1}$ or as a current $I_{D\text{-}2}$. The value of $I_{D\text{-}2}$ is related to the potential of the floating diffusion that, in turn, controls the gate of the S-2—D-2 MOS device. Since the potential of the floating diffusion is inversely proportional to the charge signal (refs. 2-4), the $I_{D\text{-}2}$ current represents the charge signal. The detection of the output by means of the current $I_{D\text{-}2}$ provides a large output voltage at lower output impedance.

The substrate is grounded and a dc bias is applied to the phase electrodes. This simplifies the testing since all biases relative to substrate can be read directly. Typical values of the dc bias voltages are: $E_\phi = E_{G\text{-}D} = -10$ V and $E_D = -30$ V. Table I lists the equipment actually used in the reported tests.

*For more discussion of this subject see pp. 17-19 in Ref. 2.

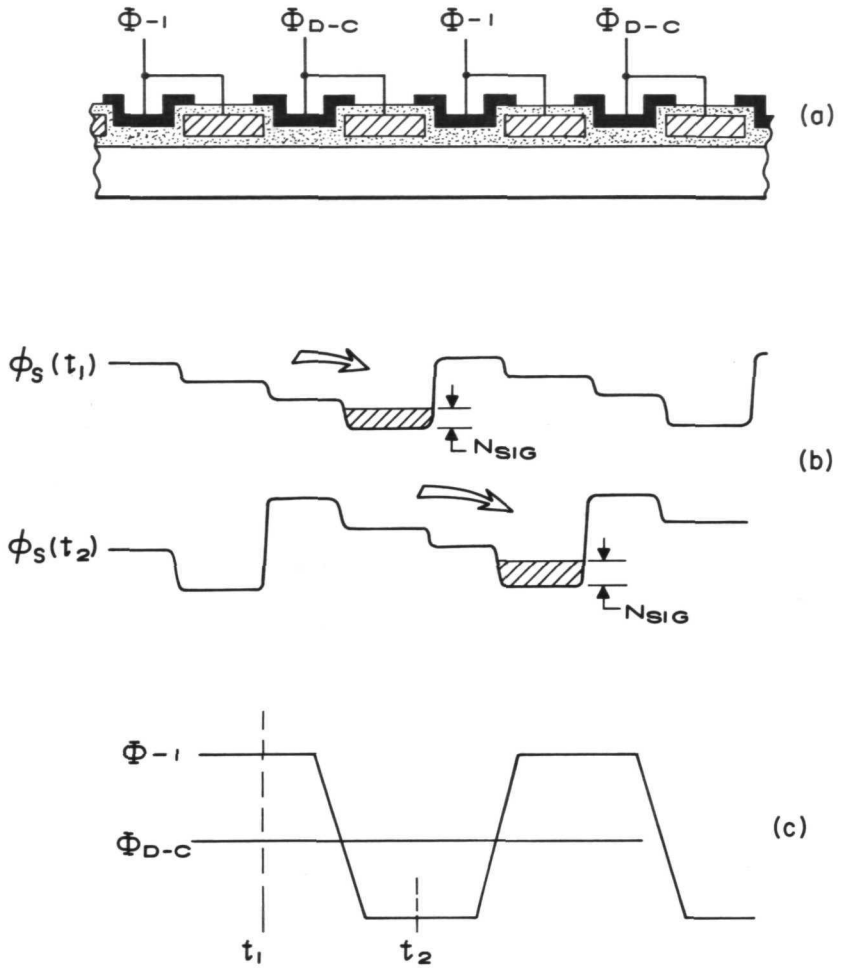


Figure 18. One clock operation of two-phase CCD.

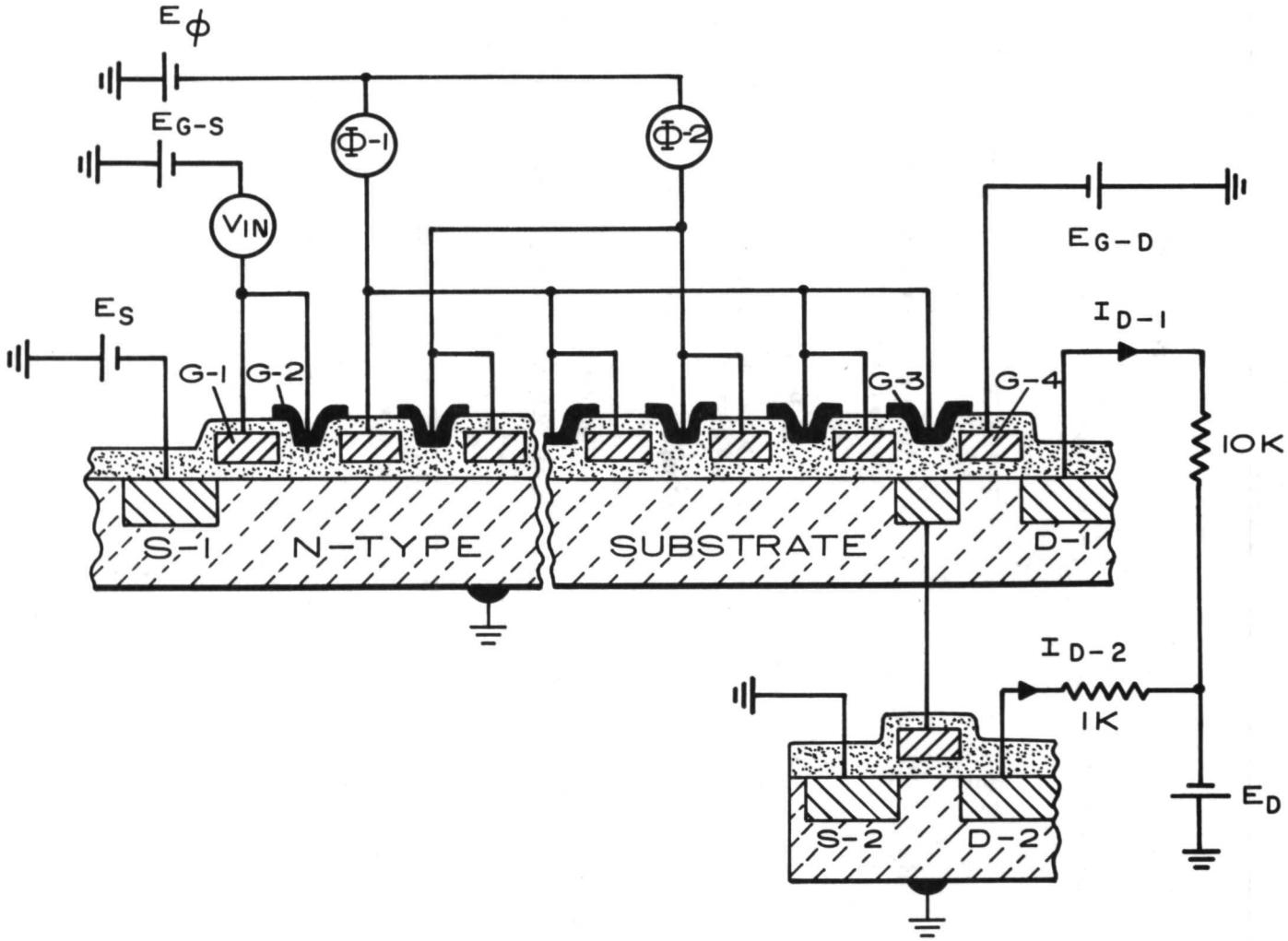


Figure 19. Circuit diagram for the tests of two-phase charge-coupled shift registers.

TABLE I

Test Equipment

Function	Equipment
1. ϕ-1, ϕ-2 (see Figure 18)	Textronix Pulse Generator, Type 115
2. V_{IN}	E-H Research Pulse Generator, Model 123
3. E_{ϕ}, $E_{G\text{-}S}$, E_s, $E_{G\text{-}D}$, E_D	Hewlett-Packard 721A Transistorized Power Supply
4. Miscellaneous triggering, counting, and gating	Textronix Pulse Generator, Type 115 Hewlett-Packard Pulse Generator, Model 214A Rutherford Pulse Generator, Model B16
5. Counter for spacing inputs	RCA CD4004AE 7 Stage COS/MOS Binary Counter

2. Loss Measurement Procedures. — In order to measure fractional loss per transfer, one must know: (a) how much charge is lost, (b) how much charge was originally in the signal pulse, and (c) how many transfers occurred. When only electrical inputs are possible, i.e., optical inputs are not available, the number of transfers is fixed by the length of the device, and the determination of the original amount of charge in the signal pulse is not always straightforward. For example, if a single "1" pulse of amplitude p_o is put in the input and the ϵN_g product (ϵ is the fractional loss per gate and N_g is the number of gates) approaches unity, by the time the pulse reaches the output it will be spread over many different pulses, all with reduced amplitude. It is then very difficult to determine the original signal amplitude. The procedure we have used to circumvent these difficulties consists of applying a string of consecutive "1s", to measure the step or pulse response of the shift register. Even in the face of sizable losses with ϵN_g products exceeding unity, provided the string of "1s" is long enough, the output signal amplitude will reach the original input value. This occurs because a pulse well removed from the leading one receives the losses from the preceding pulses which are just

enough to match the losses it suffers. Thus, as the number of "1s" in the string increases, the output amplitude increases until it saturates at the amplitude at the input. Then the sum of the trailing pulse amplitudes which follow the last "1" constitutes the total amount of charge lost by that last "1" as it passes through all the stages of the shift register. Since the last "1" is always maintained at full amplitude (by losses from previous pulses), the losses it suffers are easily analyzed in the case where the loss is a fixed fraction of the total charge, i.e., for free charge loss. This analysis is shown in Appendix B.

Thus, for free charge losses, provided the string of "1s" is long enough to provide full amplitude, the total loss $\epsilon N_g p_o$ is found by adding all the trailing pulse amplitudes. Alternately, the attenuation of the leading "1s" which will be symmetrical with the trailing edge can be totalled. Thus,

$$\epsilon = \frac{\Sigma p_i(N_g)}{N_g p_o} \tag{55}$$

See Appendix B for notation. Note here that since $\Sigma p_i(N_g)$ is proportional to p_o, ϵ does not depend upon p_o and the relative shape of the output pulse stays the same as the pulse amplitude is changed.

On the other hand, as discussed in a previous section, the fractional loss into fast interface states ϵ_s is inversely proportional to the signal amplitude. Another feature of fast state loss is that the attenuation of the leading edge of the pulse train is not symmetrical with the trailing pulse amplitude. Since the release times of the fast states vary over many orders of magnitude, the charge lost into fast states is released over a large number of trailing pulses with the amplitude of the j^{th} trailing pulse having an amplitude of

$$p_j = kTN_{ss}N_g \ln\left(\frac{2j+1}{2j-1}\right) \tag{56}$$

However, the leading edge is attenuated by an amount required to fill the states at each gate. Therefore, when measuring fast state loss, the attenuation of the leading edge is totalled and divided by $p_o N_g$ to find ϵ_s.

Figures 20 and 21 demonstrate the behavior of free charge loss and fast state loss, respectively, as signal amplitude is varied. Note symmetrical appearance of free charge loss

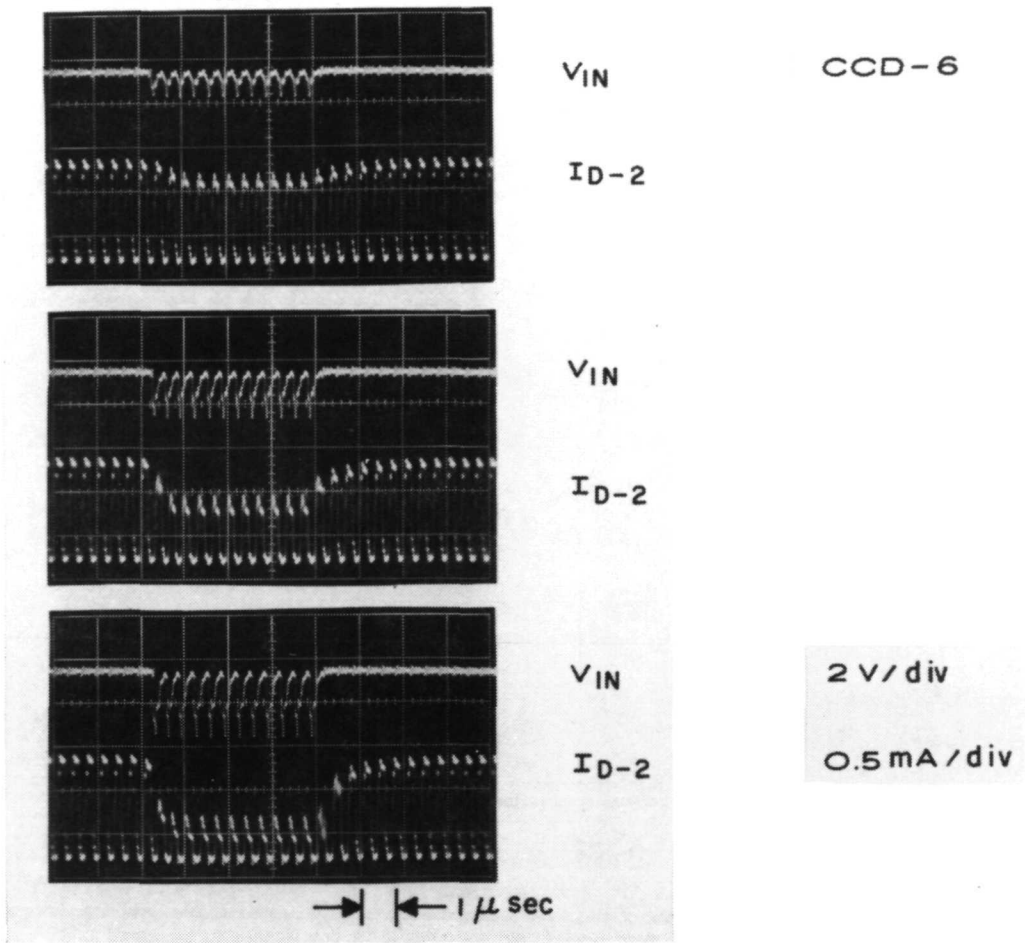


Figure 20. Oscilloscope photographs of input pulses and I_{D-2} current (traces are offset to align with one another) for 64-stage device at 3 MHz with fat zero operation. Three different photographs show how the free charge losses scale with signal amplitude.

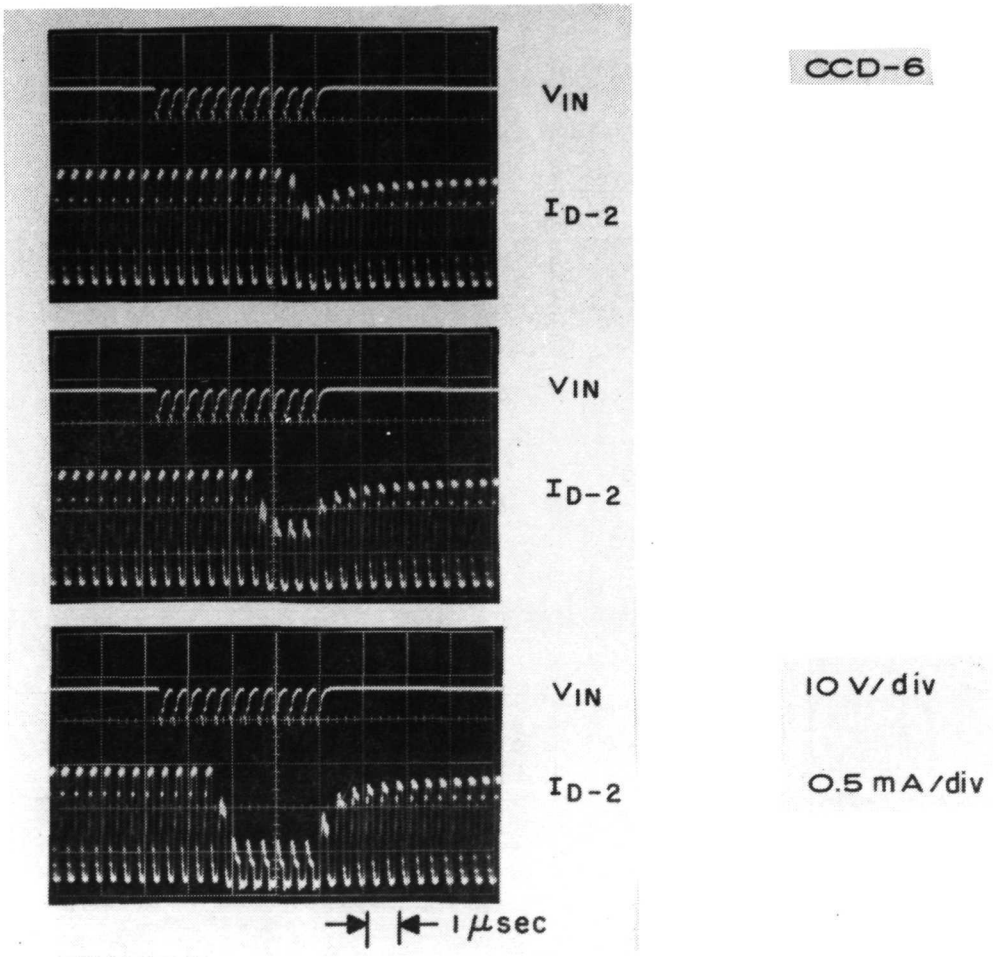


Figure 21. Oscilloscope photographs of input pulses and I_{D-2} current for 64-stage device at 3 MHz without fat zero. As signal level decreases more leading edge pulses are required to fill fast states.

and the manner in which it scales with signal amplitude. Fast state loss, however, is not symmetrical and has a total fixed loss independent of signal so that as signal is reduced the fractional loss increases considerably.

C. Loss Measurements

Figures 22 through 25 show typical waveforms for the four different length devices tested both with and without fat zero. The top oscilloscope photograph shows the two negative-going clocks along with the V_{IN} pulses. The negative V_{IN} pulses occur when ϕ-1 is "on" or negative. For tests shown in Figures 22 and 23 the output is shown as the detected current I_{D-1}. Both I_{D-1} and I_{D-2} are shown for the tests illustrated in Figures 24 and 25. Note the loss of the leading pulses in the case without fat zero with the absence of a build-up of the trailing zeros. This is due to fast state loss. The presence of charge signal results in reduction of the detected current. In Figures 24 and 25 note that the inversion of I_{D-2} pulse-current is less when signal charge is present.

Figure 26 presents the measured losses with and without fat zero as a function of frequency for a 128-stage, 1.2-mil/stage device. The dotted line through the "no fat zero" points represents a fit to Eq. (37) derived in a previous section with $N_{ss} = 8 \times 10^{10}$ $(cm^2\text{-}eV)^{-1}$ and $f_o = \frac{k_1 n_{s,o}}{2} = 10^3$ sec^{-1}. This implies $n_{s,o} \cong 2 \times 10^5$ cm^{-2}. Assuming a thermal generation rate of 10^{-9} A/cm^2, the average thermally generated background charge would be 4×10^5 cm^{-2}, remarkably close to the value inferred from Figure 26.

The dotted line through the "with fat zero" points represents exponential decay below $\epsilon = 10^{-2}$ with a thermal diffusion decay constant $L^2/2.5D = 64$ nsec, appropriate for $L = 10$ μm and $D = 6.25$ cm^2/sec. Above $\epsilon = 10^{-2}$ the dotted line represents the self-induced drift hyperbolic decay $t_o/(t + t_o)$ where $t_o = L^2 C_{ox}/1.57\ \mu q n_o$. The t_o of 0.85 nsec was determined by fitting the data and for an oxide thickness of 1000 Å implies a μn_o product of 1.6×10^{14} $(V\text{-}sec)^{-1}$. The μn_o product for a full well of $n_o = 10^{12}$ and $\mu = 250$ $cm^2/(V\text{-}sec)$ would be 2.5×10^{14} $(V\text{-}sec)^{-1}$. This excellent agreement with the free charge transfer analysis described in an earlier section indicates that we can use this analysis with confidence for CCD performance prediction and design.

Figure 27 is a similar loss vs. frequency plot for a 12-stage device. Here f_o is higher, probably due to inadequate shielding of ambient light which would increase $n_{s,o}$ and therefore f_o. Here the fast state density is $\sim 2 \times 10^{11}$ $(cm^2\text{-}eV)^{-1}$. Further confirmation of the

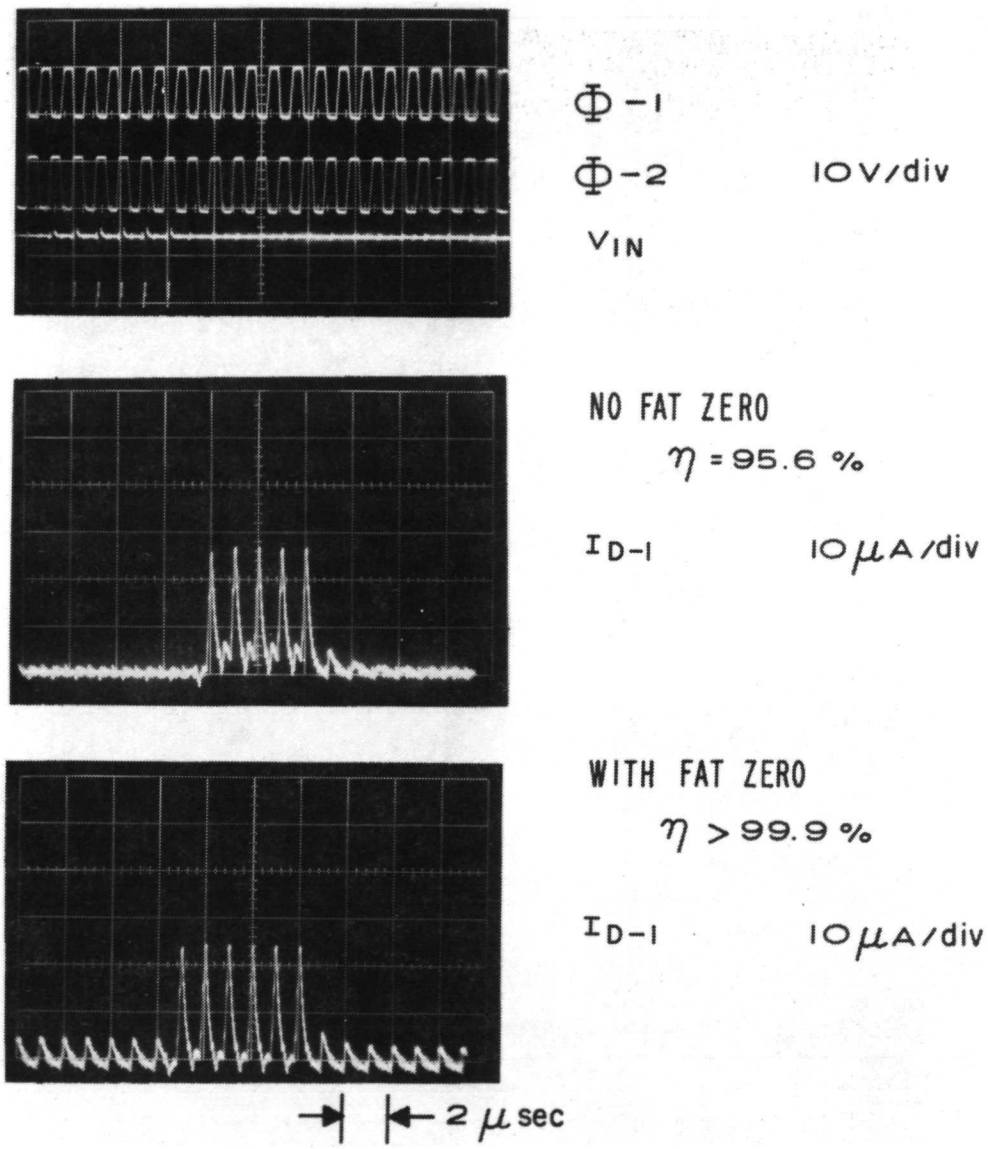


Figure 22. Typical waveforms for CCD-3 12-stage shift register at 1 MHz. Top photograph shows clocks and input pulses. Second photograph shows I_{D-1} without fat zero and the third with fat zero.

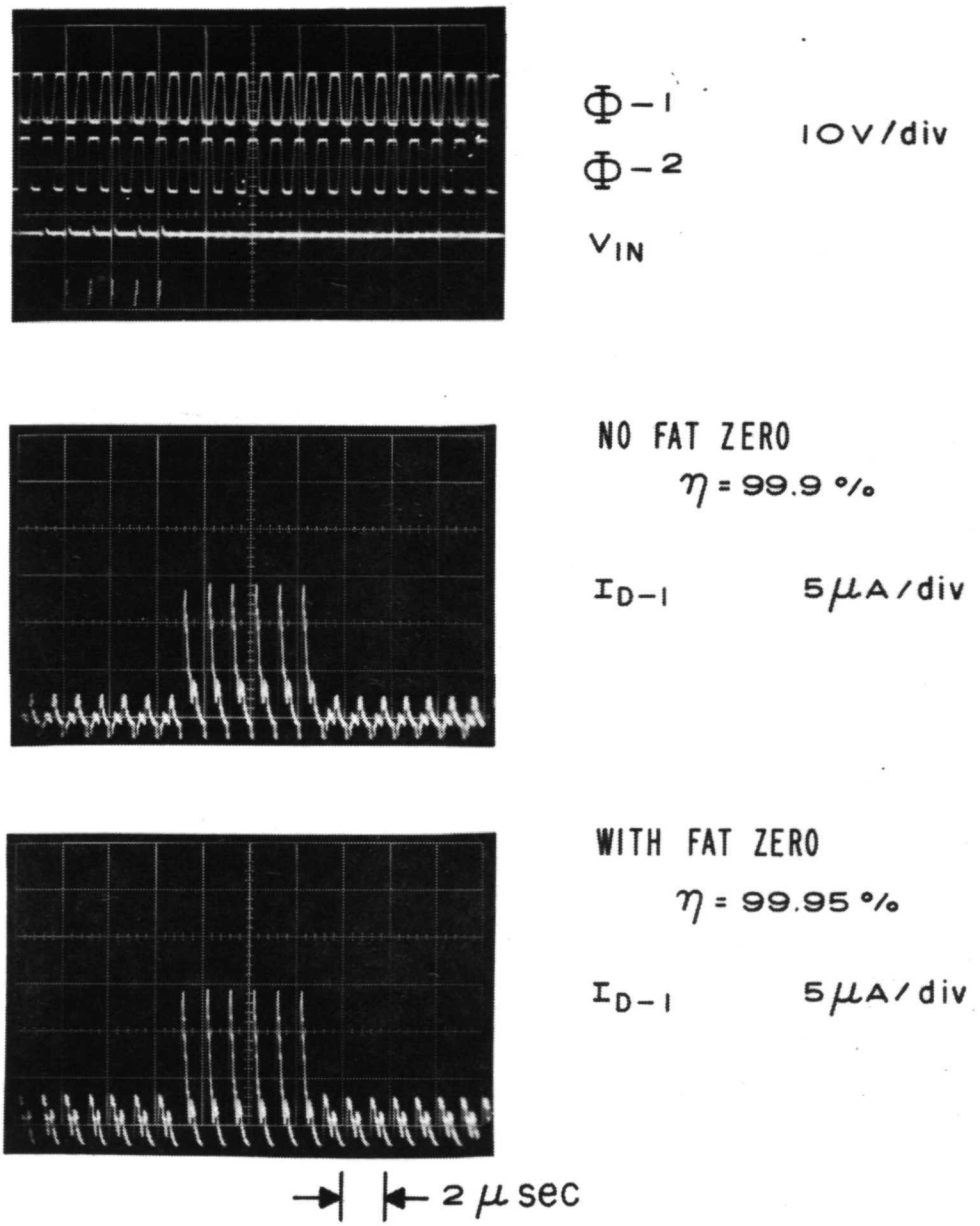
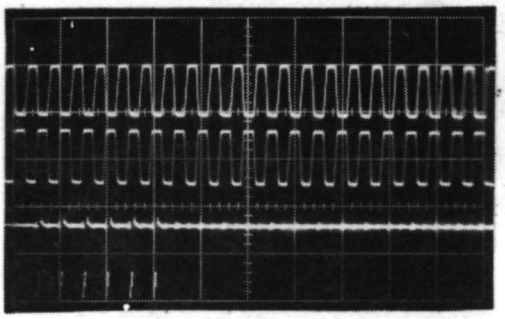


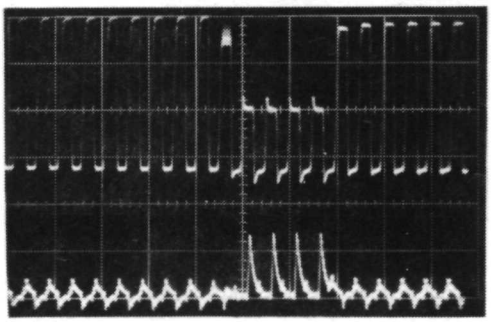
Figure 23. Typical waveforms for CCD-6 32-stage shift register at 1 MHz.



Φ-1

Φ-2 10 V/div

V_{IN}

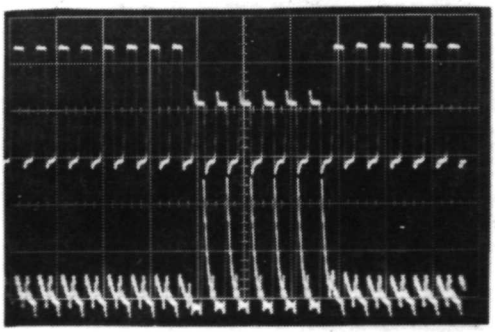


NO FAT ZERO

η = 98.65%

I_{D-2} 0.5 mA/div

I_{D-1} 10 μA/div



WITH FAT ZERO

η > 99.99%

I_{D-2} 0.5 mA/div

I_{D-1} 5 μA/div

2 μ sec

Figure 24. Typical waveforms for CCD-6 64-stage shift register at 1 MHz.

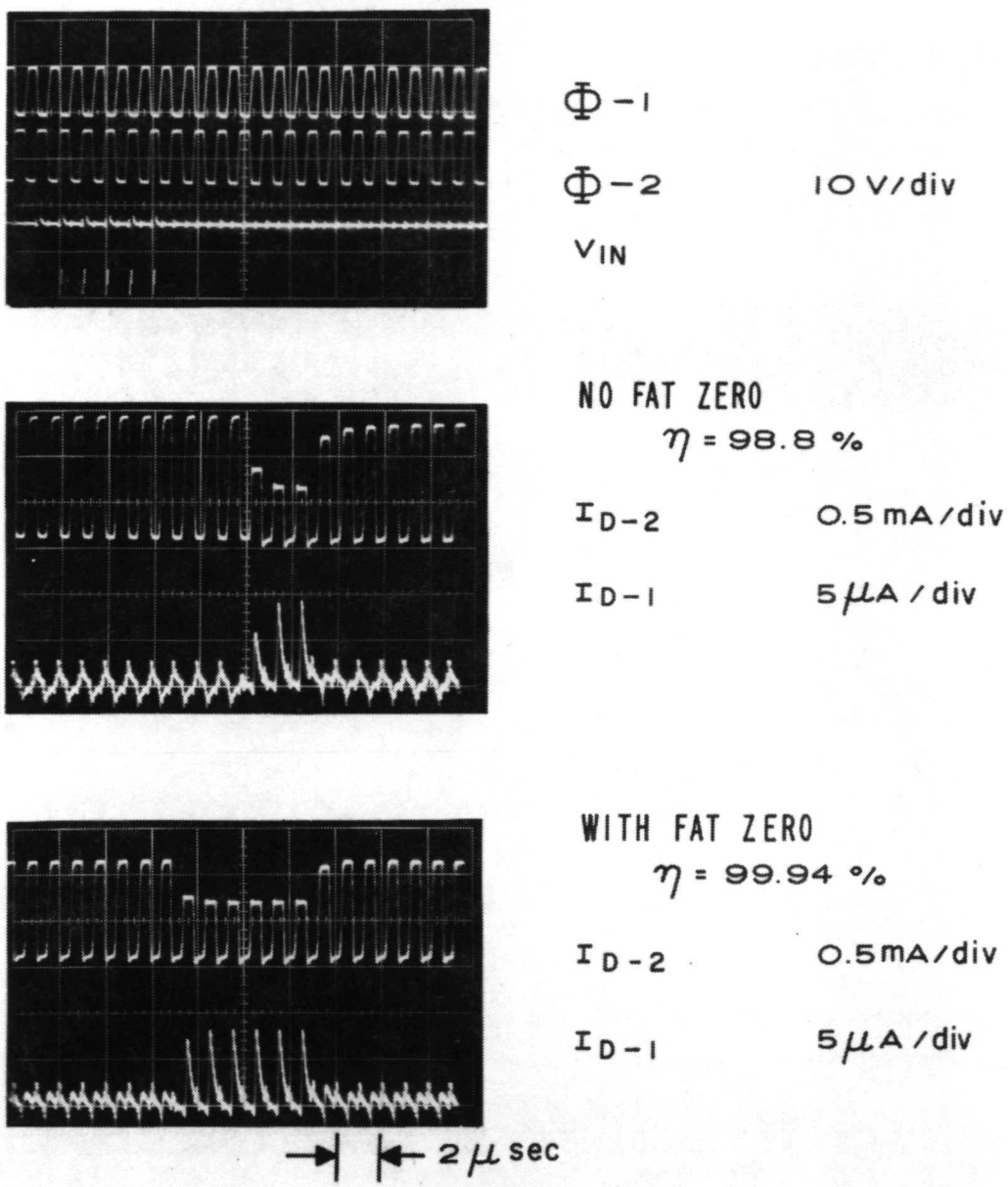


Figure 25. Typical waveforms for CCD-5 128-stage shift register at 1 MHz.

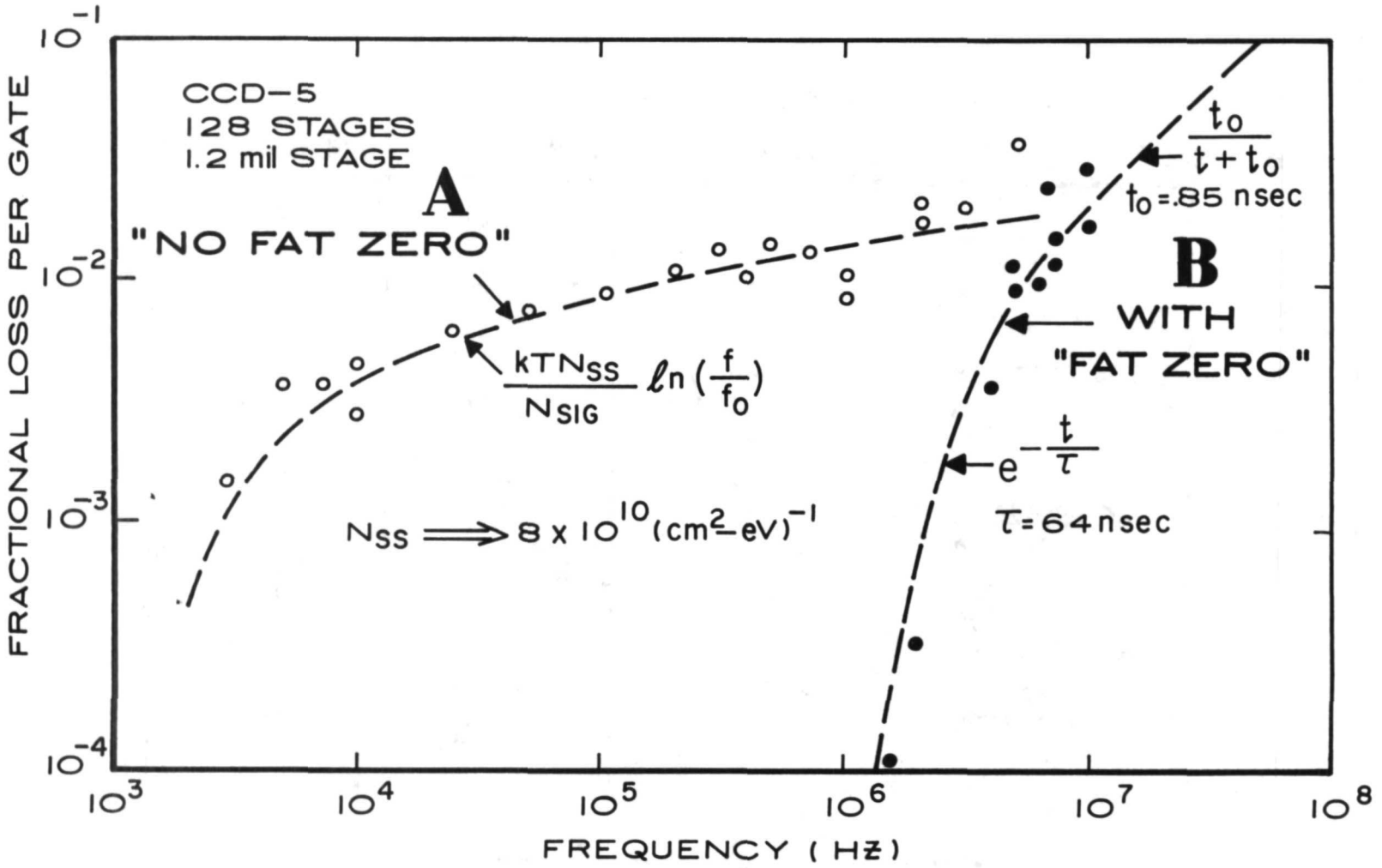


Figure 26. Fractional loss per transfer vs. frequency for 128-stage shift register with and without fat zero.

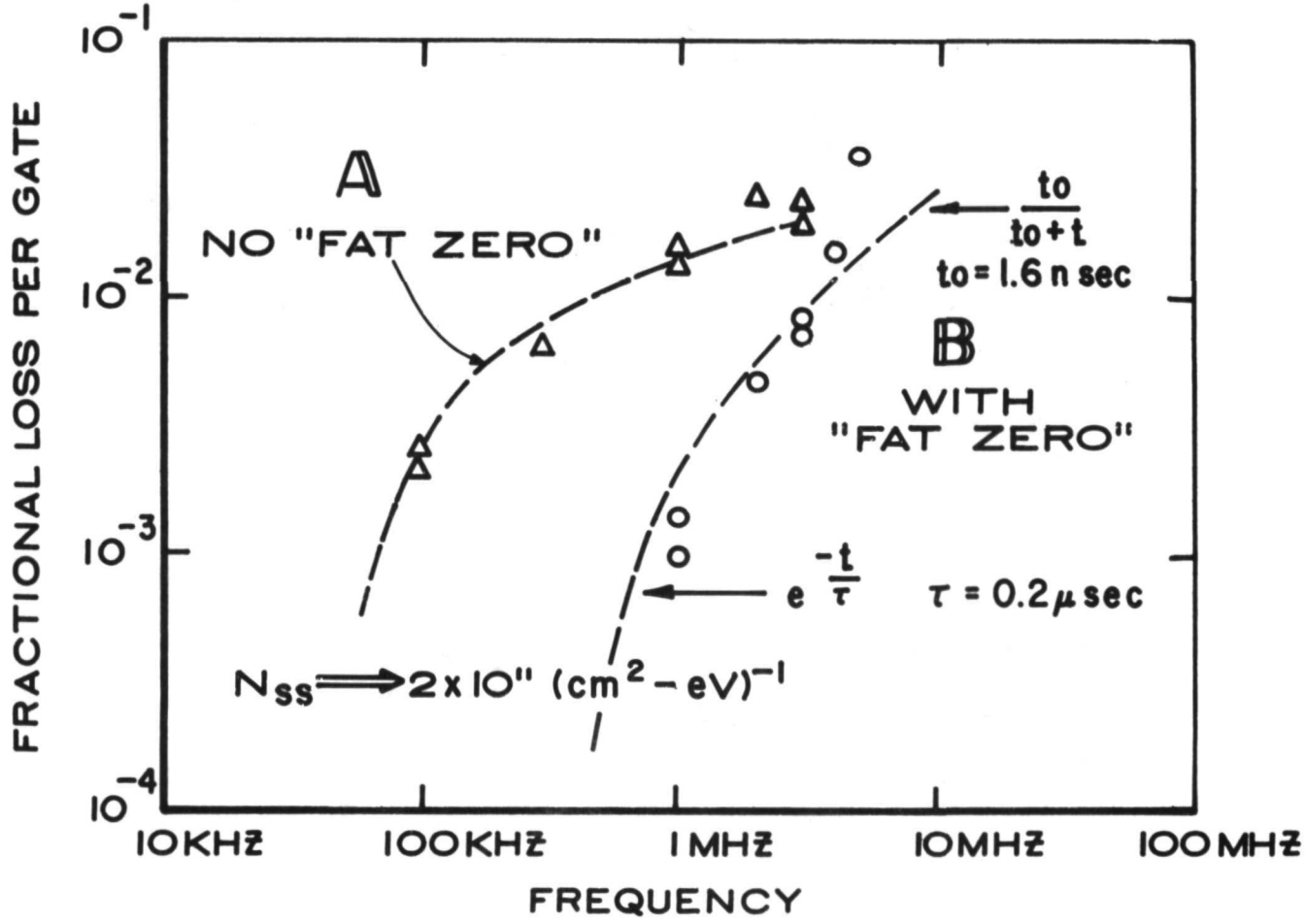


Figure 27. Fractional loss per transfer vs. frequency for 12-stage shift register, with and without fat zero.

basic assumptions in the interface state model is found in the next three figures. Figure 28 shows the inverse relationship between fractional loss and signal level which confirms the fixed loss independent of signal level predicted by the model. Figure 29 shows the fast state loss ϵ_s as a function of number of "0s" between the string of "1s". This curve follows the prediction of Eq. (42) and is a strong argument for the exponential dependence of empty times. The slope which is proportional to N_{ss} yields a value of 1.9×10^{11} $(cm^2\text{-}eV)^{-1}$ for the same device as in Figure 27. The straight line of the data indicates that the interface state density is uniform over the energy range represented; i.e., empty times from 4 to 100 μsec which correspond to energies above the valence band of 0.33 to 0.42 eV. This slope method is a very convenient way of measuring N_{ss} since the input signal repetition rate can be varied over a wide range without disturbing the basic operation of the CCD.

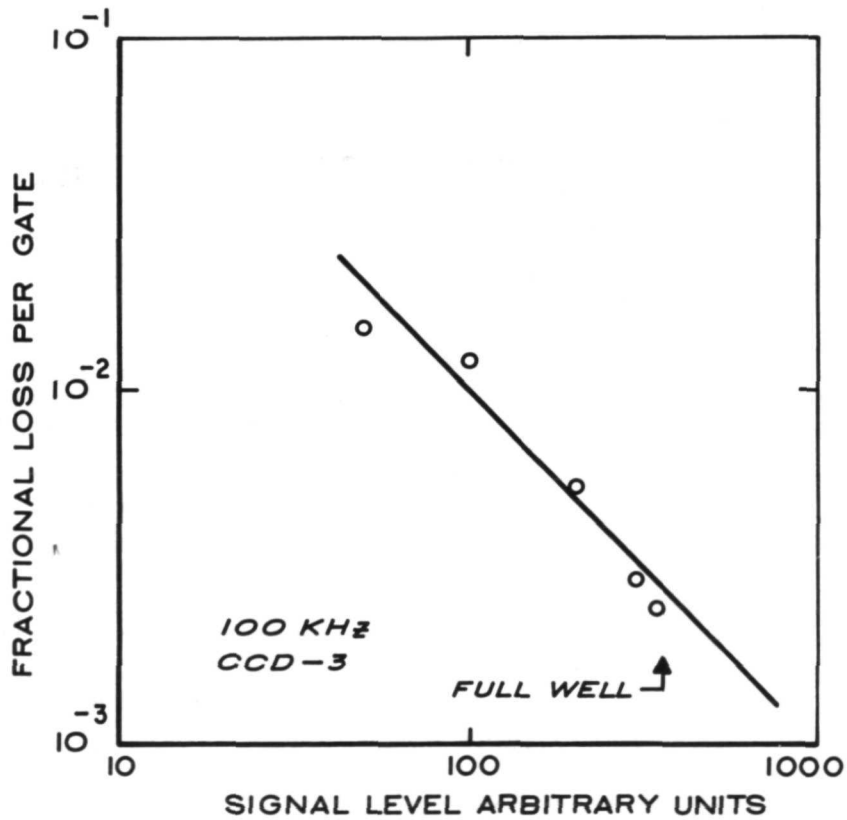


Figure 28. Fractional loss per transfer vs. signal level.

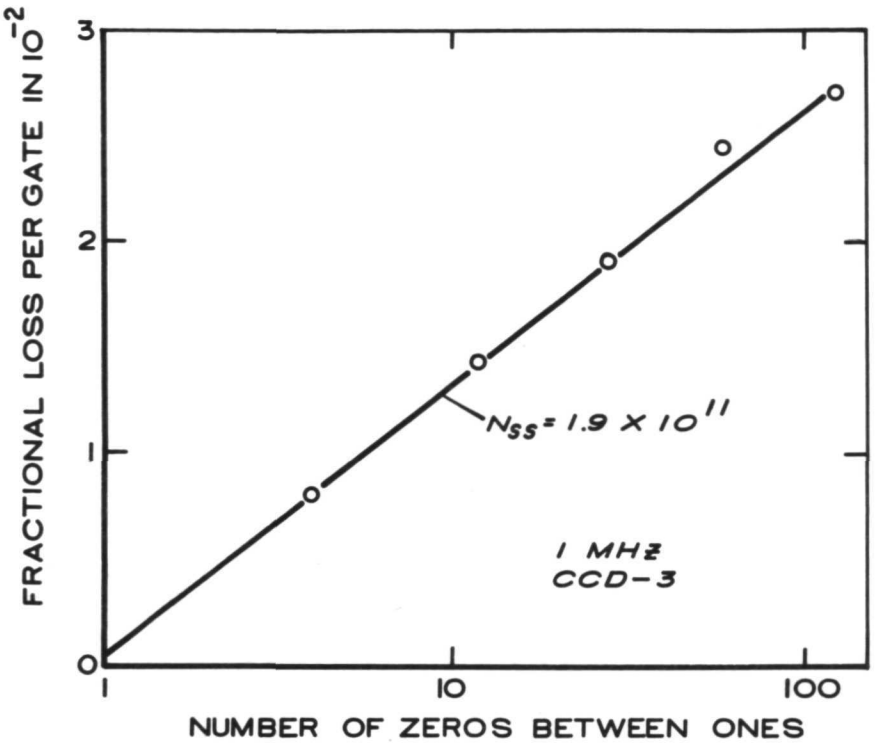


Figure 29. Fractional loss per transfer vs. log number of "0s" separating the string of "1s".

Figure 30 shows how the loss per transfer decreases over several orders of magnitude as the level of the fat zero is increased. The maximum loss at low fat zero levels seen in the figure was determined experimentally by introducing no fat zero. This also is predicted by the fast state loss model and is strong evidence of its validity.

Figure 31 illustrates the difference in transfer efficiency obtained for the two models of operation discussed earlier: complete charge transfer and bias charge operation. In both cases fat zero is present so that the losses observed are of a free charge transfer nature. As seen in the figure the amplitude of the first trailing pulse is reduced considerably when the bias on the aluminum gates is increased so as to obtain complete transfer operation.

Figure 32 shows oscilloscope photographs which compare normal, no fat zero operation (a) with the case of one-phase or one-clock operation (b). For one clock operation, ϕ-2 clock has been removed and the dc bias on ϕ-2 gates has been increased to midway between the ϕ-1 clock swings. ϕ-1 amplitude was not changed. Note that now about only one-half the

signal is seen because the potential wells are reduced in depth. The loss of additional leading edge pulses in the one-clock operation is due to the reduced signal and is symptomatic of fast state losses as discussed earlier.

Finally, Figure 33 illustrates the analog delay line operation of a 128-stage shift register. The potential of the input diffusion S-1 was modulated by a sine wave as shown in the top trace of each photograph. The output, delayed by 128 μsec, is shown as unfiltered I_{D-2} in the top photograph and after filtering with a 30-kHz low-pass filter in the lower photograph. The modulation frequency, 23 kHz, was such that, after delay of 128 μsec and when inverted by the output amplifier, the output signal is in phase with the input signal. This operation shows the linearity of the CCD shift register and demonstrates its potential application as an analog delay line.

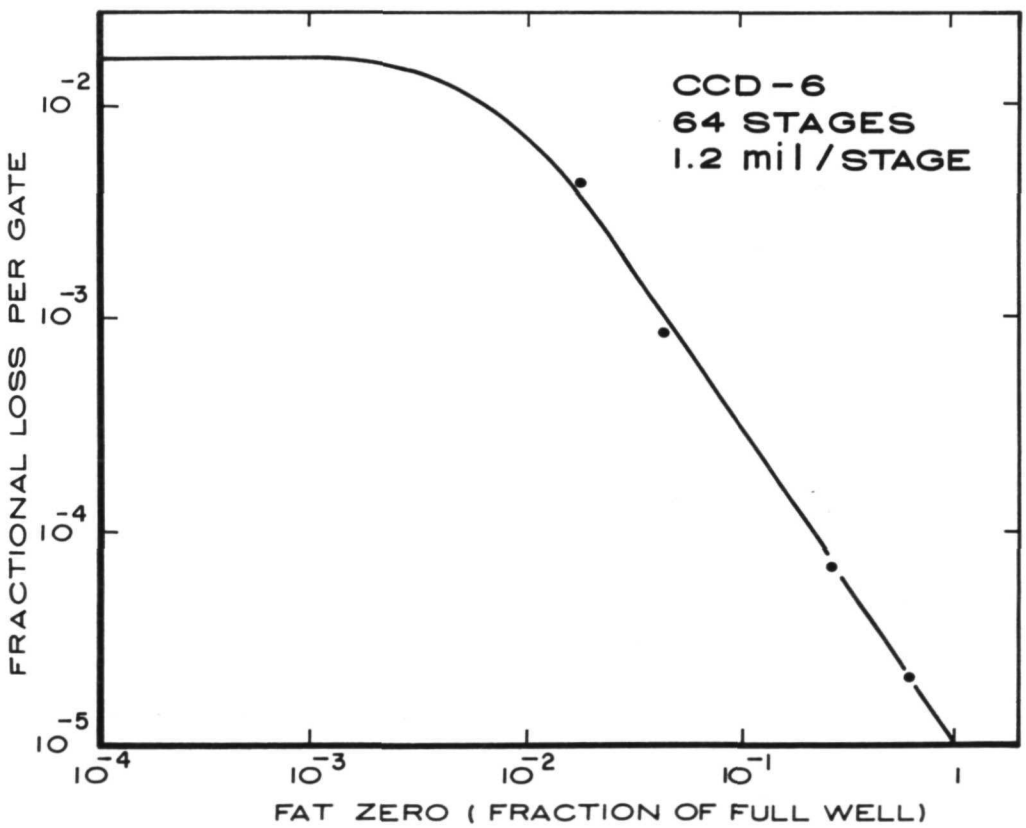


Figure 30. Fractional loss per transfer vs. amount of fat zero.

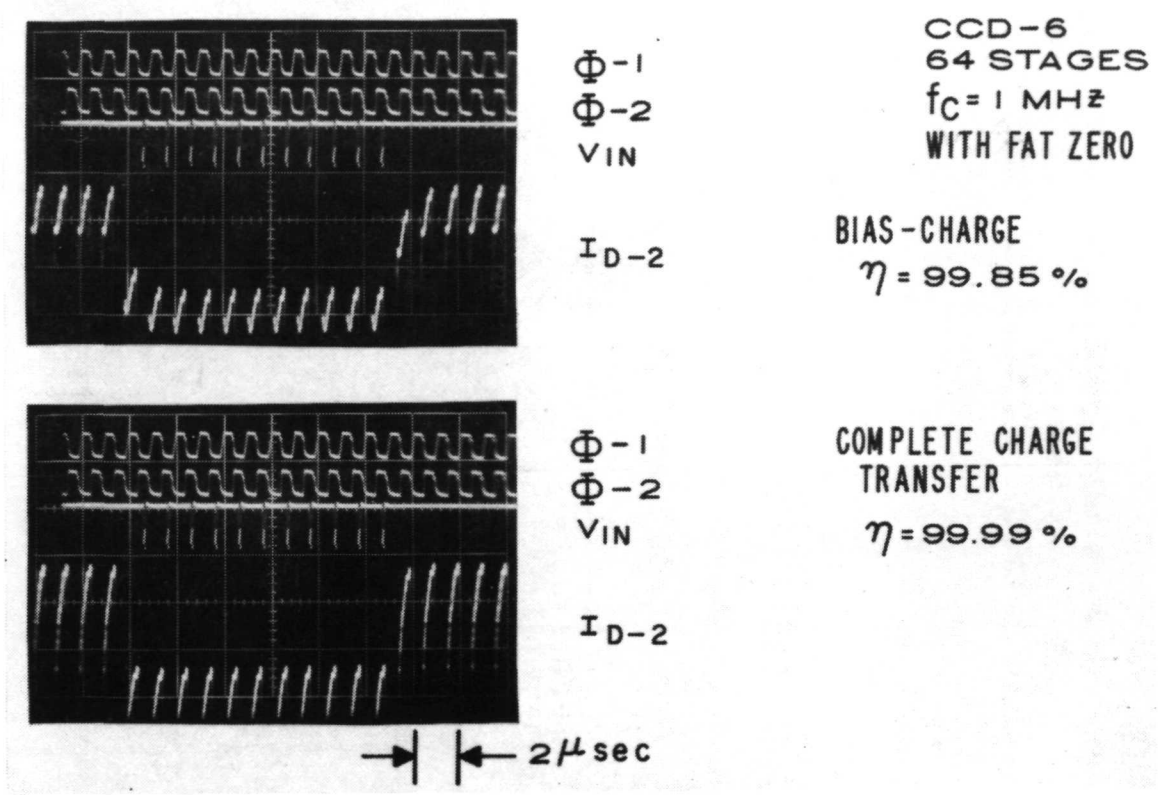


Figure 31. Oscilloscope photographs showing I_{D-2} current for bias charge mode of operation and complete transfer mode.

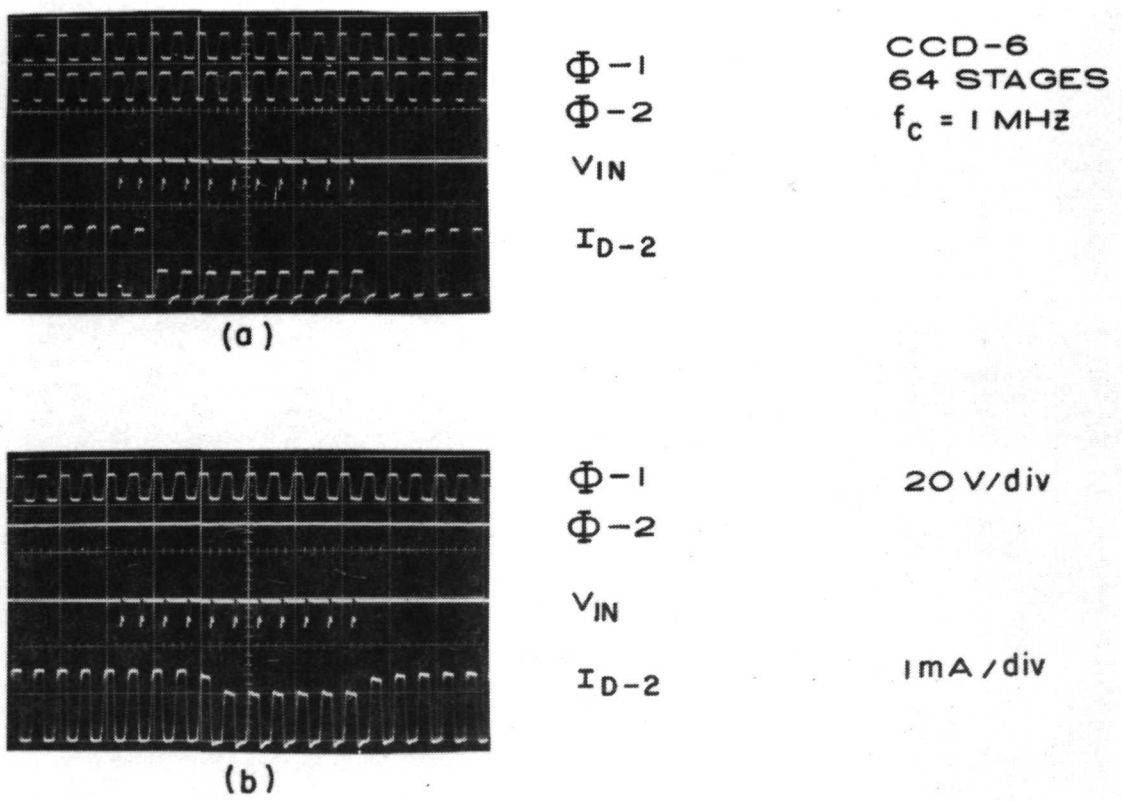


Figure 32. Oscilloscope photographs showing normal two-clock operation (top) and one-clock operation (bottom) with ϕ-2 returned to dc.

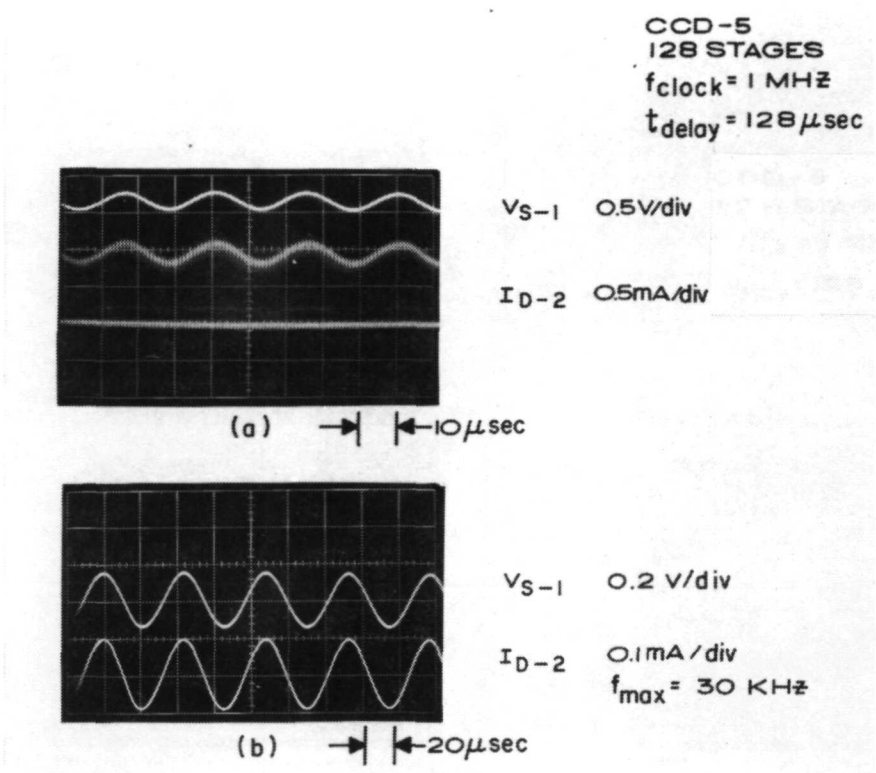


Figure 33. Analog delay line operation of 128-stage device. S-1 is sine-wave modulated at 23 kHz. Top photograph shows unfiltered I_{D-2} while bottom shows filtered I_{D-2}.

IV. CONCLUSIONS

The operation of two-phase charge-coupled shift registers in the form of polysilicon gates overlapped by aluminum gates has been demonstrated. Three test arrays were designed and fabricated that included shift registers up to 128 stages long (without signal refreshing stages). The unidirectional signal flow in the experimental shift registers was accomplished by using n-type substrates with resistivity of 0.5 to 1.0 ohm-cm in conjunction with channel oxide thicknesses of 1000 Å for the polysilicon gates and 3000 Å for the aluminum gates.

Charge-transfer efficiency of 99.99% per gate was achieved in the operation of the two-phase charge-coupled shift registers operating with a constant circulating charge — the fat zero. These results were found to be in good agreement with the expected charge-transfer efficiency resulting from incomplete free-charge transfer. The tests of the experimental charge-coupled shift registers showed that without fat zero, the charge-transfer losses are mainly due to the charge trapping by the fast interface states of the $Si\text{-}SiO_2$ interface.

A theoretical model was developed for the analysis of the interface state losses. A simplified solution of the interface state losses as a function of clock frequency was found to be consistent with the measured losses of the first "1" in the string of "1s" for no fat zero operation. The interface loss model also predicts that without fat zero the charge-transfer loss due to the fast states should be proportional to the logarithm of the number of "0s" between the strings of "1s". Such tests are proposed as a convenient method for measurement of the fast interface state density. The interface losses obtained in the operation of the tested charge-coupled shift registers correspond to a density of fast interface states of about 10^{11} $(eV\text{-}cm^2)^{-1}$, which is consistent with the silicon substrates with (111) orientation used for these devices.

A comparison of the complete charge-transfer mode and the bias-charge or bucket-brigade mode of operation of the experimental two-phase charge-coupled shift registers showed that at 1.0-MHz clock frequency the complete charge-transfer mode is about 10 times more efficient than the bias charge mode. At higher clock frequencies, such as 10 MHz, the two modes of operation were found to have about the same charge-transfer efficiency. Both of these results were obtained with fat zero operation.

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APPENDIX A

FREE CHARGE TRANSFER IN CHARGE COUPLED DEVICES*

by

J. E. Carnes, W. F. Kosonocky and E. G. Ramberg

ABSTRACT

The free charge transfer characteristics of charge-coupled devices are analyzed in terms of the charge motion due to *thermal diffusion, self-induced drift, and fringing field drift.* The charge-coupled structures considered have separations between the gates equal to the thickness of the channel oxide. The effect of each of the above mechanisms on charge transfer is first considered separately, and a new method is presented for the calculation of the self-induced field. Then the results of a computer simulation of the charge-transfer process which simultaneously considers all three charge motion mechanisms is presented for three-phase charge-coupled devices with gate lengths of 4 and 10 μm. The analysis shows that while the majority of the charge is transferred by means of the self-induced drift which follows a hyperbolic time dependence, the last few percent of the charge decays exponentially under the influence of the fringing field drift or thermal diffusion, depending on the design of the structure. The analysis shows that in charge-coupled devices made on relatively high resistivity substrates, the transfer by fringing field drift can be very fast, such that transfer efficiencies of 99.99% are expected at 5- to 10-MHz bit rates for 10-μm gate lengths and at up to 100 MHz for 4-μm gate lengths.

1. INTRODUCTION

Because charge-coupled devices (refs. A-1, A-2) are analog shift registers with no mechanism for gain, the attainable charge transfer efficiency, η, (the percent of charge transferred from one gate to the next) is extremely important. In order to achieve practical devices of several hundred stages, extremely low loss per gate is required; e.g., a one hundred stage three-phase device with an overall efficiency of 90% must have a single gate transfer efficiency of 99.97%.

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There are two basic mechanisms which degrade transfer efficiency. The first is the incomplete transfer of free charge because insufficient time is allowed for transfer. The second is the trapping of charge in fast interface states. This appendix is concerned only with the analysis of incomplete transfer of free charge.

In this study, the time required for free charge to transit from one potential well to the next has been determined by numerical solution of the continuity equation in which all the factors which cause charge motion have been simultaneously considered. This work was undertaken to determine the fundamental limitations on charge transfer efficiency imposed by the free charge transfer process and to determine the optimum device configuration for maximum transfer efficiency.

The three mechanisms which cause charge motion (thermal diffusion, self-induced drift, and fringing field drift) are discussed in Section 2, including a new method for calculating the self-induced electric fields. The results of the numerical solutions of charge transfer along with the associated charge and field profiles are presented in Section 3. The two methods for calculating the self-induced fields are compared in Section 4, and a discussion of the results and conclusions are presented in Section 5.

2. TRANSFER MECHANISMS

In the analysis of charge motion in a charge-coupled device (CCD) it is convenient to identify two sources of electric field at the interface along the directions of charge propagation: the fringing field $E_F(y,t)$ due to externally applied potentials on the gate electrodes and the field change due to the presence of the signal charges themselves, the self-induced field $E_S(y,t)$. Thus, if it is assumed that the field effect mobility μ is independent of electric field, the electron particle current density $j_n(y,t)$ may be written as the sum of three terms:

$$\begin{aligned} j_n(y,t) &= -n(y,t)\mu E_F(y,t) && \text{Fringing Field Drift} \\ &= -n(y,t)\mu E_S(y,t) && \text{Self-Induced Drift} \\ &= -n\frac{\partial n(y,t)}{\partial y} && \text{Thermal Diffusion} \end{aligned} \qquad (57)$$

where $n(y,t)$ is the carrier concentration of electrons (cm^{-2}) in the inversion layer, y is the direction of charge propagation along the interface, and D is the diffusion constant.

The continuity equation:

$$\frac{\partial n(y,t)}{\partial t} = -\frac{\partial j_n(y,t)}{\partial y} \tag{58}$$

describes the decay of charge, but an analytical solution including all of the terms in Eq. (57) is somewhat difficult. Consequently, in this section the three mechanisms will be considered separately in order to gain insight into their basic features. Numerical solutions considering all terms of Eq. (57) simultaneously will be presented in Section 3.

a. Thermal Diffusion

Kim (refs. A-2, A-3) has treated the transfer of free charge due to thermal diffusion. As derived in Supplement I, a Fourier analysis of the thermal diffusion process shows that for an initially uniform carrier concentration n_o, the carrier profile n(y,t) remaining under the transferring electrode approaches the following expression asymptotically in time

$$n(y,t) = \frac{4n_o}{\pi} \cos\frac{\pi y}{2L} \exp\left(-\frac{\pi^2 Dt}{4L^2}\right) \tag{59}$$

and the total number of carriers remaining at time t, $N_{tot}(t)$, by

$$N_{tot}(t) = \frac{8}{\pi^2} N_{tot}(0) \left(\exp -\frac{\pi^2 Dt}{4L^2}\right) \tag{60}$$

Aside from a small fraction of charge which decays very quickly, the decay of the total charge due to thermal diffusion is exponential with decay constant τ_{th} of $L^2/2.5D$.

b. Self-Induced Drift, Gradient Method

Self-induced drift occurs because of the electric fields induced by the signal charge itself. The magnitude of the self-induced fields directed along the Si-SiO_2 interface, E_s, was first described by Engeler, et al. (ref. A-4) by taking the gradient along the interface of the surface potential ϕ_s. In this approximation ϕ_s is calculated for the one-dimensional MOS capacitor and is assumed to be proportional to the signal carrier concentration n_s. Thus, if the oxide capacitance C_{ox} is much greater than the depletion layer capacitance, one can write

$$\phi_s(y,t) = \phi_{so} - \frac{q}{C_{ox}} n(y,t) \tag{61}$$

where ϕ_{so} is the surface potential of an empty well. Then

$$E_s(y,t) = \frac{q}{C_{ox}} \frac{\partial n}{\partial y} \quad (y,t) \tag{62}$$

The particle current is then given by

$$j_n(y,t) = -\frac{\mu q n(y,t)}{C_{ox}} \qquad \frac{\partial n(y,t)}{\partial y} \tag{63}$$

This is equivalent to a diffusion current with a concentration-dependent diffusion coefficient. The continuity equation is given by

$$\frac{\partial n(y,t)}{\partial t} = \frac{\mu q}{C_{ox}} \frac{\partial}{\partial y} \left(n(y,t) \frac{\partial n(y,t)}{\partial y} \right) = \frac{\mu q}{2C_{ox}} \frac{\partial^2}{\partial y^2} n^2(y,t) \tag{64}$$

If the carrier concentration n(y,t) is separable into a product function h(y)g(t), then as shown in Suppl. II, the total charge remaining will decay according to the following asymptotic expression

$$\frac{N_{tot}(t)}{N_{tot}(0)} = \frac{t_o}{t + t_o} \tag{65}$$

where

$$t_o = \frac{L^2 C_{ox}}{1.57 \mu q n_o} \tag{66}$$

Note that t_o depends inversely upon the initial carrier concentration n_o.

When the charge level drops to the point where the average carrier concentration n_{ave} is such that

$$\frac{\mu q}{C_{ox}} n_{ave} = D \tag{67}$$

the self-induced fields will be reduced to the level of thermal fields and further decay will be due to thermal diffusion. The time t_1 required to reach the condition of Eq. (67) can be expressed as

$$t_1 = t_o\left(\frac{n_o\mu q}{C_{ox}D} - 1\right) = 1.6\,\tau_{th}\left(1 - \frac{kT}{q}\,\frac{C_{ox}}{qn_o}\right) \tag{68}$$

Since in most cases, $\frac{kT}{q}\,\frac{C_{ox}}{qn_o} << 1$, the transition from self-induced drift to thermal diffusion occurs, in the absence of any fringing field drift, after a time approximately equal to the thermal diffusion time constant $L^2/2.5D$.

c. Self-Induced Drift, Integral Method

Another more exact method of calculating the self-induced fields along the Si-SiO_2 interface will be referred to as the integral method. In this approach, the electric field along the Si-SiO_2 interface due to an infinite line charge, also at the interface, is calculated by the method of images for the case where the Si is an infinite dielectric with no space charge region. (See Figure 34(a) and Suppl. III.) The contributions of each line charge-element which makes up any charge distribution (with spatial variations along the direction of the field and infinite extent perpendicular to it) are then summed by integration and the desired field is determined. Equation (69) gives the expression which for most cases must be evaluated numerically.

$$E_s(y) = \frac{1}{\pi\epsilon_2(1+\epsilon)}\left[\int_{y-L_1}^{L_2-y}\frac{\rho(y)ydy}{y^2} - \frac{2\epsilon}{1+\epsilon}\sum_{1}^{\infty}\left(\frac{1-\epsilon}{1+\epsilon}\right)^{n-1}\int_{y-L_1}^{L_2-y}\frac{\rho(y)ydy}{(2nx)^2+y^2}\right] \tag{69}$$

where $\epsilon = \epsilon_1/\epsilon_2$.

The case of a uniform charge concentration of length L can be evaluated analytically as shown in Suppl. III and the results provide useful insight into the question of self-induced field magnitudes. Equation (70) gives $E_s(y)$ for Si-SiO_2 for a uniform concentration n_o of length L.

$$E_s(y) = 1.8 \times 10^3\left(\frac{n_o}{10^{11}}\right)\ S\left(\frac{y}{L}, \frac{2X_o}{L}\right)\ \text{V/cm} \tag{70}$$

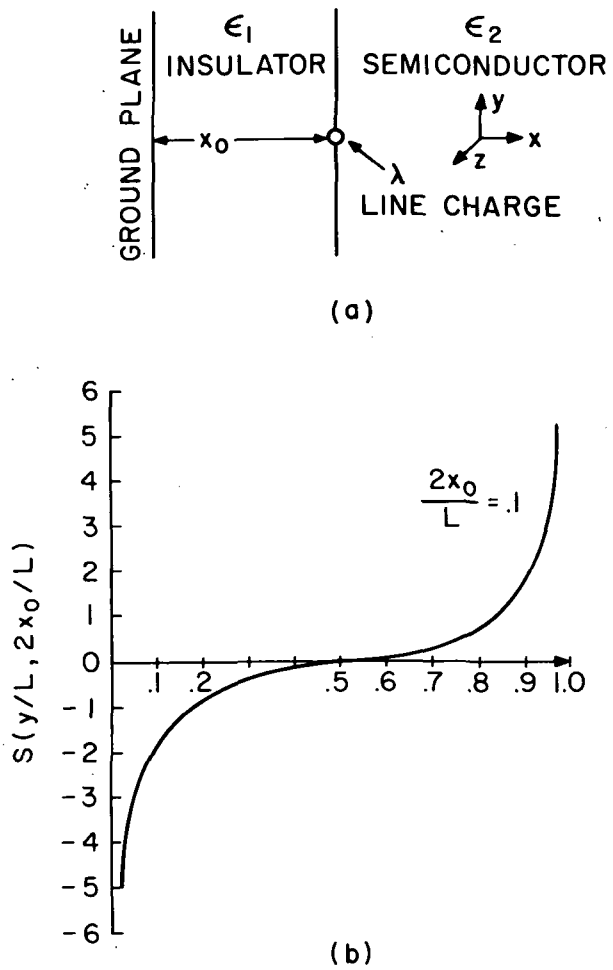

Figure 34. (a) Cross-sectional view of a line charge at a dielectric interface and near a ground plane. The total y-directed field at the dielectric interface is determined by integrating over all the line charge elements which make up the actual charge distribution.
(b) Shape function $S(y/L, 2X_o/L)$ for any uniform charge distribution of length L. The field magnitude for the Si-SiO_2 interface is $(n_o/10^{11})1.83 \times 10^3\ S(y/L, 2X_o/L)$ V/cm.

$E_s(y)$ is directly proportional to n_o, but the relative shape of $E_s(y)$ is independent of n_o. $S(y/L, 2X_o/L)$ is defined in Supplement III and is plotted in Figure 34(b). Strictly speaking, for a perfect step function charge profile, $S(0, 2X_o/L) \to \infty$. However, for most of the cases encountered in our charge transfer studies where the charge profile is rounded, a maximum value of S was four or five for a $2X_o/L$ ratio of 0.1. Using S = 4 in Eq. (70) provides a very simple expression for the maximum self-induced field magnitude for approximately uniform charge profiles given by

$$E_s \text{ max} \cong 7.2 \times 10^3 \left(\frac{n_o}{10^{11}} \right) \text{ V/cm} \qquad (71)$$

This expression provides a simple, approximate relationship between self-induced field magnitudes and the charge concentration.

The integral method also allows one to calculate how charge will arrange itself within a potential well. For example, charge placed in a square well with no externally induced electric fields in the interior will tend to crowd at the edges of the well due to the mutually repulsive properties of like charges similar to the arrangement of charge on a conducting disc in free space (ref. A-5). The results of a computer solution of this effect using the integral method [Eq. (69)] to calculate $E_s(y)$ is shown in Figure 35. The well is not exactly square — the walls have a finite slope — which accounts for the low charge concentration near the edges. However, the bottom of the well is flat over the majority of the region and the cusping of charge is due to the self-induced fields. The gradient method cannot be used to solve this type of problem.

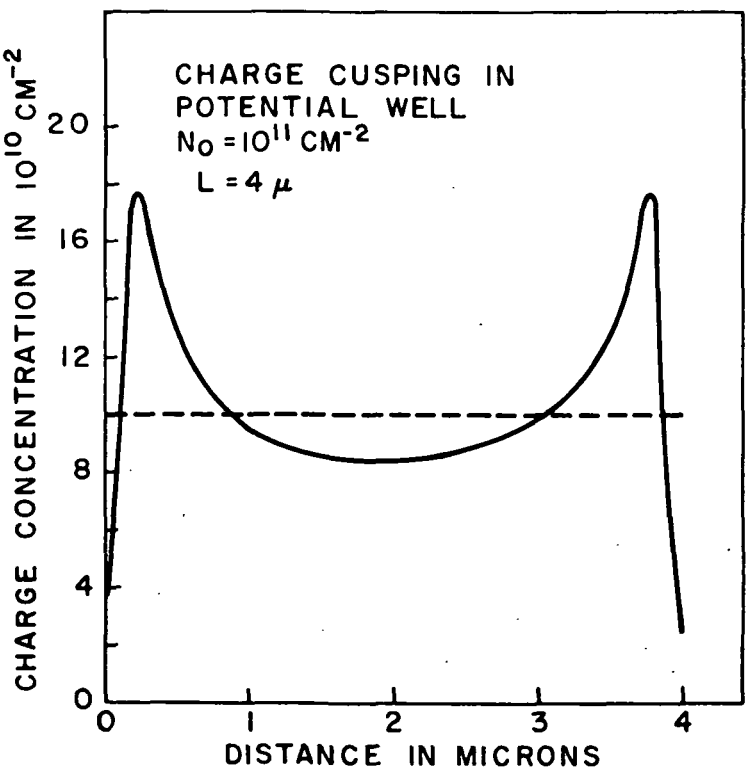

Figure 35. Cusping of charge stored in a square potential well due to self-induced fields calculated by the integral method.

d. Fringing Field Drift

The drift-aiding fringing field along the Si-SiO_2 interface arises because the surface potential at any point is determined not only by the electrode directly above but also by adjacent electrodes. An analytical expression for three-phase CCD fringing fields (ref. A-6) and computer solutions for both two and three phase fringing fields have previously been presented (refs. A-6, -7). These results indicate that in a certain range of gate lengths and substrate doping levels, the single carrier transit time (the time a single carrier would take to transit the length of the gate under influence of the drift-aiding fringing field) is small enough to indicate that fringing field drift may greatly aid the transfer process.

The numerical solutions to be discussed in Part 3 indicate that under the influence of fringing field drift and thermal diffusion, the relative charge profile becomes fixed or stationary and decays exponentially. When the spatial dependence of the charge profile becomes independent of time, n(y,t) can be expressed as a product solution, and for the exponentially decaying case can be written as

$$n(y,t) = h(y) \exp(-t/\tau_f) \tag{72}$$

where

$$N_{tot}(0) = \int_0^L h(y)dy \tag{73}$$

τ_f is the final decay constant of the total remaining charge. Neglecting self-induced effects, the continuity equation becomes

$$V_T \frac{d^2h(y)}{dy^2} + E_F(y) \frac{dh(y)}{dy} + \left(\frac{dE_F(y)}{dy} + \frac{1}{\mu\tau_f} \right) h(y) = 0 \tag{74}$$

where $V_T = kT/q$.
Solution of this equation subject to the boundary conditions

$$\mu h(0)E_F(0) + D \frac{dh(y)}{dy}\bigg|_0 = 0 \tag{75}$$

and

$$\mu h(L)E_F(L) + D \left.\frac{dh(y)}{dy}\right|_L = \frac{-1}{\tau_f} \int_0^L h(y)dy \tag{76}$$

allows one to determine h(y) and τ_f. Only a numerical solution for a general $E_F(y)$ appears possible.

From Eq. (74) it is clear that when $V_T = 0$, at the peak of charge where

$$\frac{dh(y)}{dy} = 0$$

$$\tau_f = -\frac{1}{\mu \left.\frac{dE}{dy}\right|_{peak}} \tag{77}$$

This has been substantiated by numerical solutions.

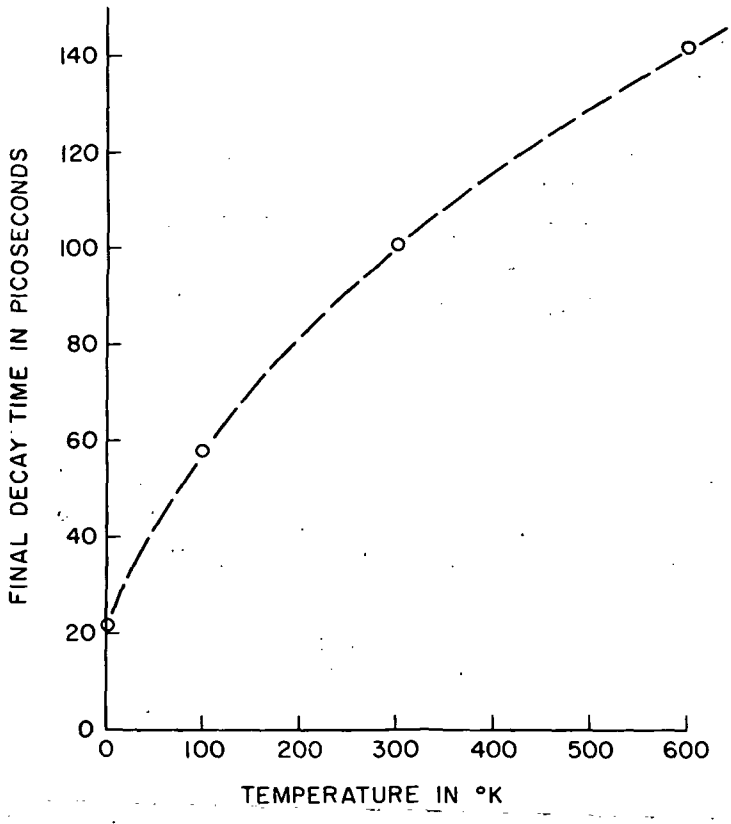

Figure 36. Final decay time of total remaining charge τ_f vs. temperature as determined by computer simulation for 4-μm gates and 10^{15} cm^{-3} doping.

Numerical solutions also show that the charge will decay exponentially even at zero temperature, but increasing temperature causes τ_f to increase. Thus thermal diffusion acts to hinder fringing field drift. Figure 36 shows τ_f vs. T for one particular fringing field configuration studied numerically.

3. COMPUTER SIMULATION RESULTS

In order to better understand the interaction of the various transfer mechanisms in typical charge-coupled device structures, the complete continuity equation has been solved numerically using both the integral method and the gradient method for calculating self-induced fields. Both 4-μm and 10-μm gate lengths were considered as well as doping levels of 2×10^{14} and 10^{15}cm^{-3}. Oxide thickness and electrode separations were 2000 Å in all cases (ref. A-7) (see Figure 37). Three-phase devices were assumed and the fringing field profile was determined numerically for the case where the transferring electrode potential was midway between the blocking and receiving electrode potentials. The voltages used were 2,7 and 12 V in all

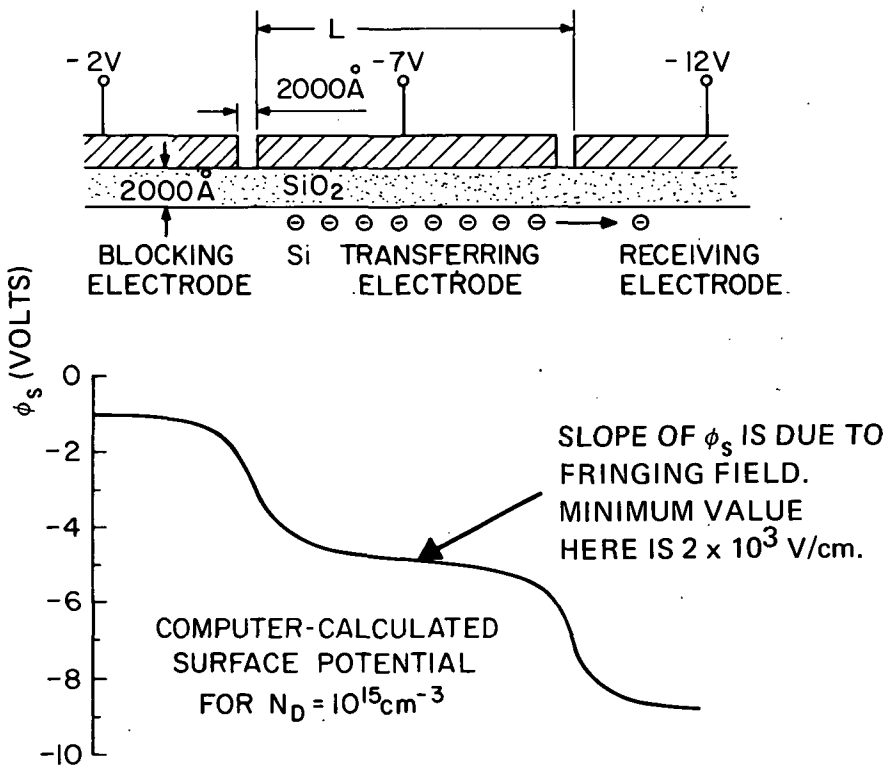

Figure 37. Cross-sectional schematic of basic configuration studied by computer simulation along with the surface potential for the 10^{15}cm^{-3} doping case.

cases. In actual practice, the transferring electrode potential will be changing from 12 to 2 V during the transfer process, but incorporating this into the solution unnecessarily complicates the problem. If anything, the electrode voltage configuration used probably underestimates the speed of transfer due to fringing field drift.

In the 4-μm gate studies, an initial uniform charge distribution of $4.6 \times 10^{11} cm^{-2}$ was used. No cusping occurred because fringing fields balanced the self-induced fields so that a uniform concentration was maintained. In all cases the mobility was assumed to be constant and equal to 250 cm^2/V-sec. All transfer times will scale inversely with mobility.

The configuration studied in most detail was the 4-μm gate, 10^{15} doping case. The overall charge decay versus time results using the integral method are shown in Figure 38. For times less than 500 psec the charge decay is dominated by self-induced drift. The dotted line shows how self-induced drift proceeds in the absence of any fringing field. This decay would eventually become exponential (after one thermal diffusion time of 10 nsec) with decay constant of 10 nsec. However, the fringing field drift causes the transfer to progress at a faster rate.

The single carrier transit time, τ_{tr}, given by

$$\tau_{tr} = \frac{1}{\mu} \int_0^L \frac{dy}{E_F(y)} \tag{78}$$

is 400 psec for this configuration. Clearly, the charge does not transit the sample in 400 psec. One of the main reasons for this is the retarding effect of the self-induced fields on the left half of the transferring region. The self-induced field profiles for various times are shown in Figure 39. Also shown is the drift-aiding fringing field. The self-induced fields remain as high as the minimum fringing field for up to 600 to 800 psec for this case and this tends to hold back the charge. Consequently, the charge remains well spread out over the entire gate region for times much longer than τ_{tr}.

The charge profiles are shown in Figure 40. After approximately 800 psec the fringing fields dominate and self-induced effects are negligible. The charge profile then tends to drift to the right under the influence of the drift-aiding fringing field and one might expect it to continue to drift entirely out of the region into the receiving potential well. However, this does not happen, but rather the charge profile becomes stationary at approximately 1400 psec and decays exponentially thereafter.

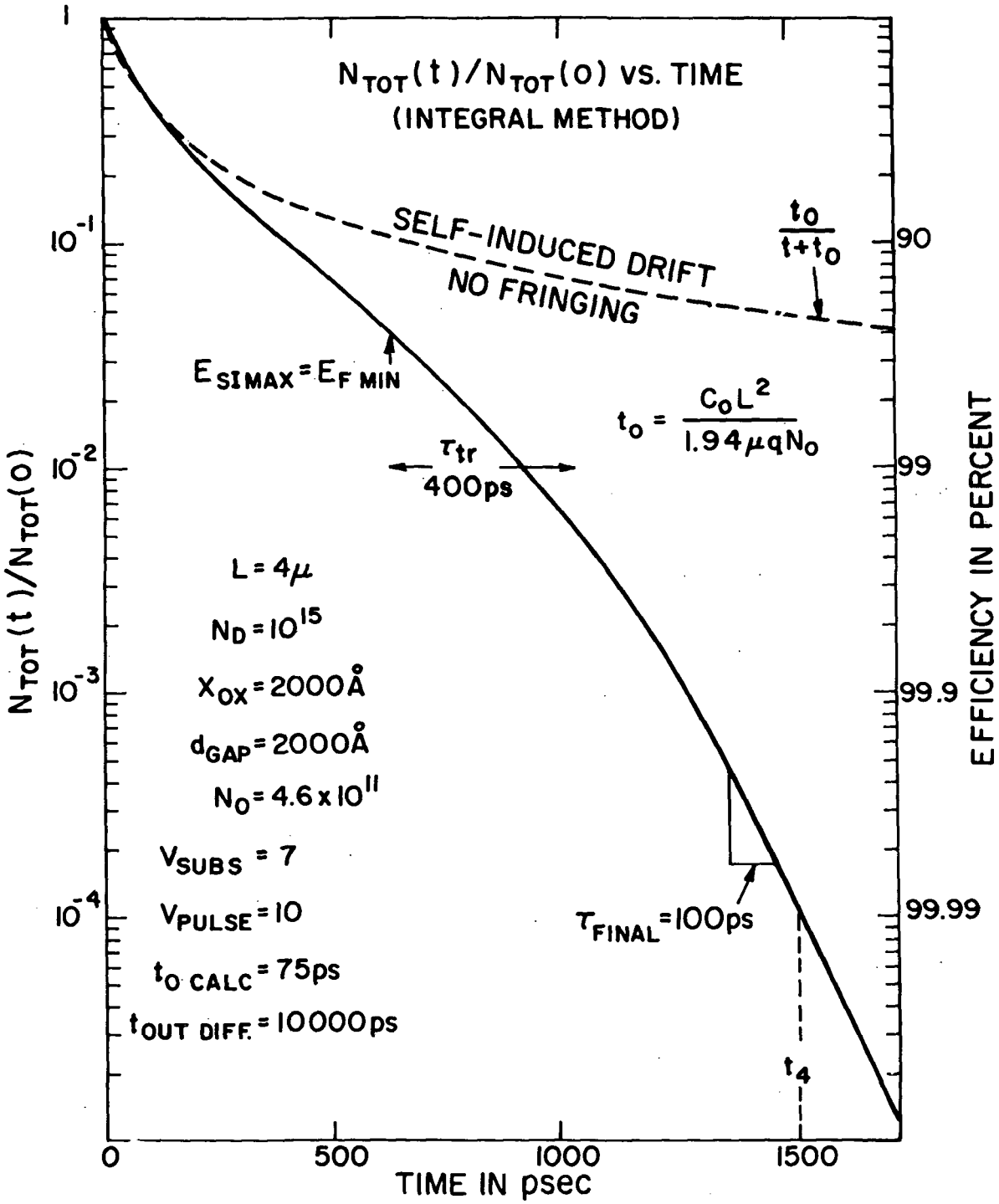

Figure 38. Normalized total remaining charge vs. time for 4-μm gate length and 10^{15}cm^{-3} doping. The dotted line indicates how the charge transfer would proceed in the absence of fringing fields.

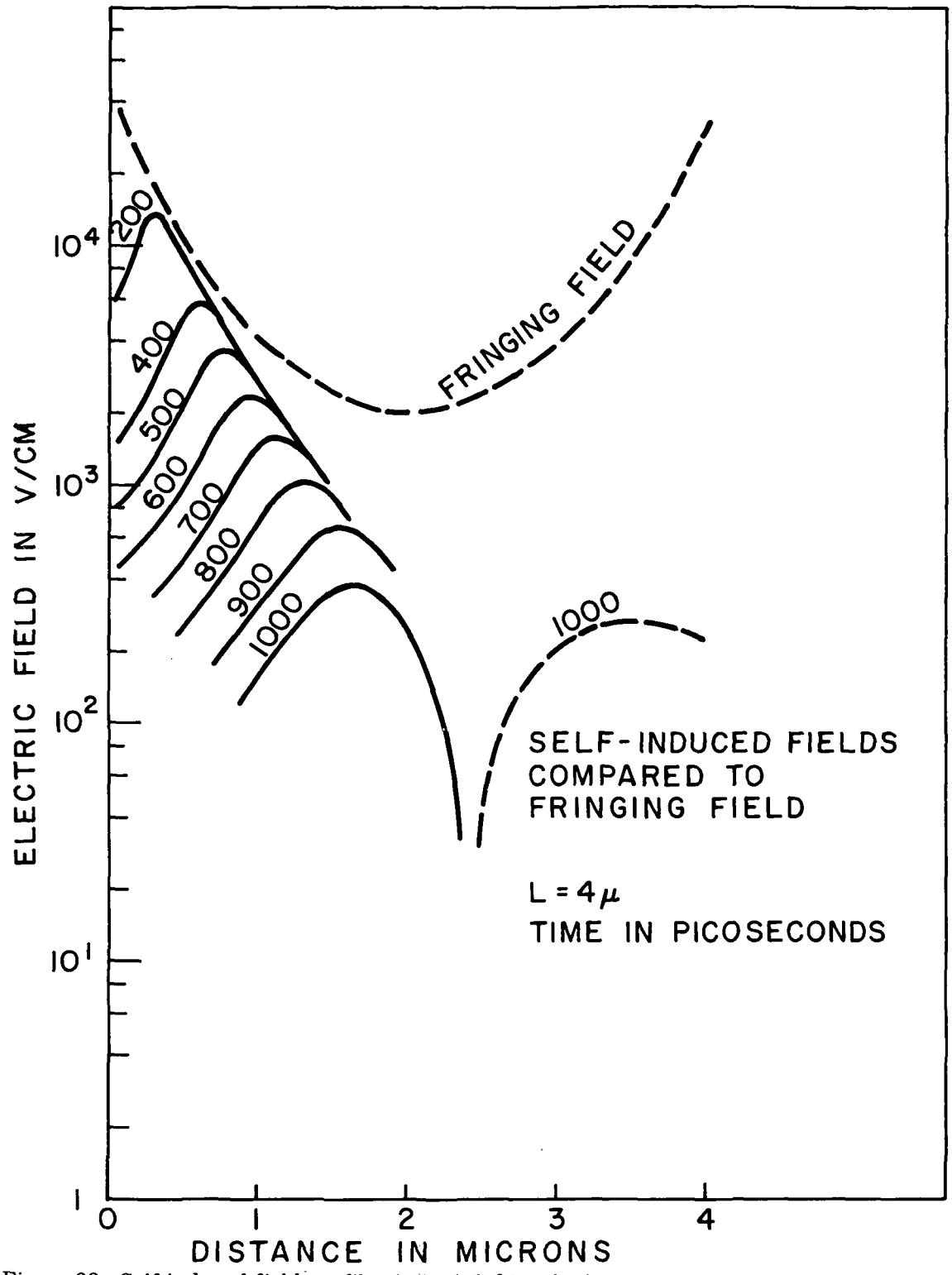

Figure 39. Self-induced field profiles (calculated by the integral method) at various times for the same problem shown in Figure 37. Solid line fields cause charge motion to left (hinder transfer), dotted line fields cause charge motion to the right (aid transfer).

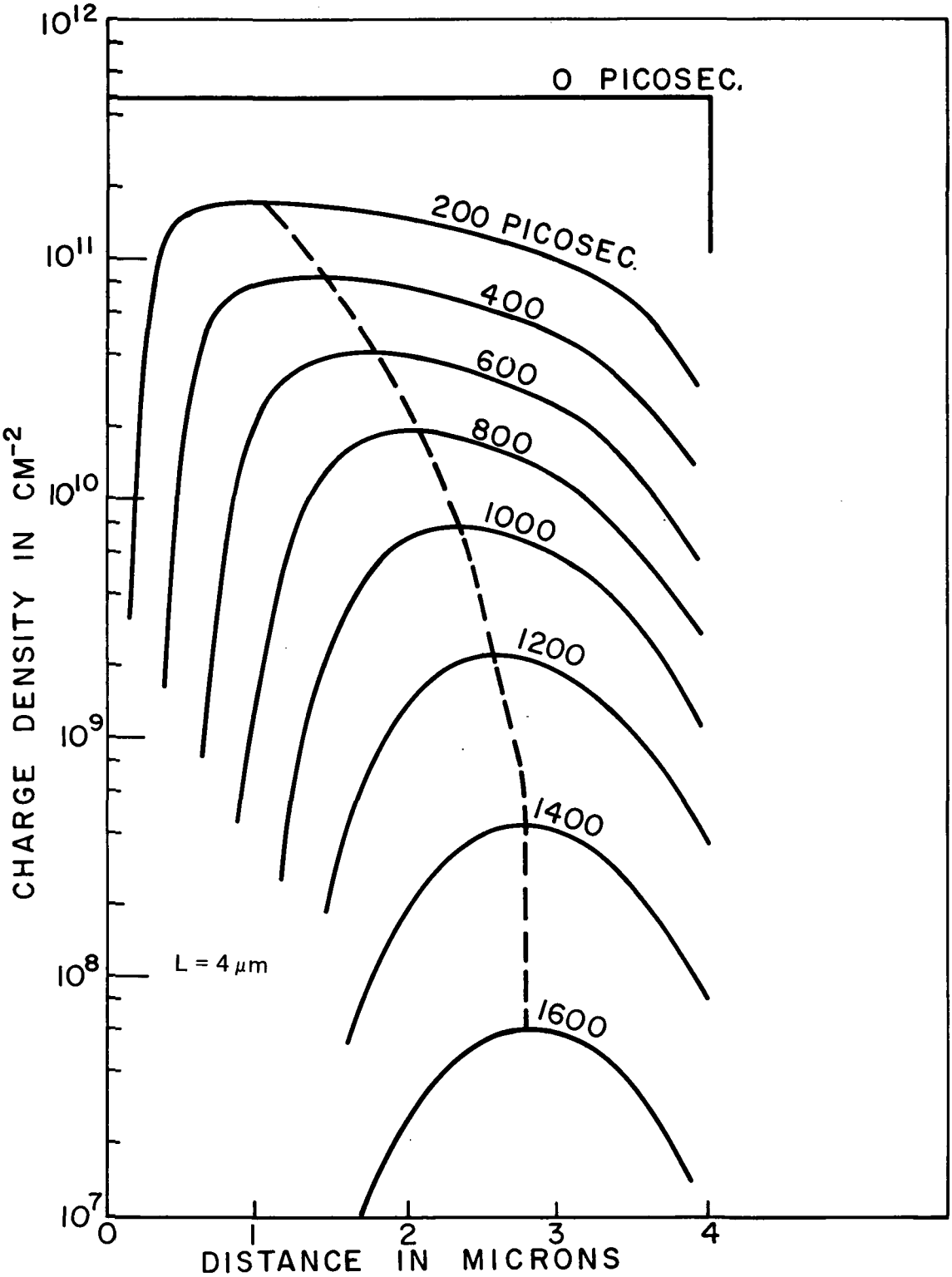

Figure 40. Charge profiles for various times during the same problem shown in Figure 37. The dotted line traces the charge peaks.

This occurs basically because the fringing field is not uniform but has large negative gradients on the right side of the region. The final decay time for this case is 100 psec. As noted in Part 2, the τ_f should be approximately

$$\tau_f = -\left(\mu \frac{dE_F(y)}{dy}\bigg|_{peak}\right)^{-1} \quad \text{for } V_T = 0 \tag{79}$$

In this case this quantity is 115 psec, which compares favorably with the actual τ_f of 100 psec.

As expected, decreasing doping density with the resultant increase in fringing field magnitude results in faster transfer. Figure 41 compares the charge decay curves for 10^{15} and $2 \times 10^{14} cm^{-3}$ doping. The higher fringing fields result in more complete transfer at all times and reduces the time t_4 required to achieve $\eta = 99.99\%$ from 1.46 nsec to 1.125 nsec. *In the absence of fringing fields, approximately 53 nsec would be required to achieve $\eta = 99.99\%$ by means of self-induced drift and thermal diffusion alone.*

Figure 42 shows charge decay results for the 10-μm gate case: both 2×10^{14} and 10^{15} doping. *Here the initial charge level was small, approximately $10^{10} cm^{-2}$, so that no self-induced effects are apparent.* Here again the final decay is exponential and transfer is materially aided by the higher fringing fields of the lower doped substrate.

The results for the four cases studied ($n_o = 10^{10} cm^{-2}$) are summarized in Figure 43 which shows the total charge remaining vs. time normalized by the single carrier transit time. All four cases with widely varying transit times generally follow the same curve with

$$\tau_f \cong 1/3 \ \tau_{tr} \tag{80}$$

and the time t_4 to achieve $\eta = 99.99\%$ of

$$t_4 \cong 4 \ \tau_{tr} \tag{81}$$

These relationships apply only at room temperature where fringing field drift dominates the final transfer of charge. When τ_{tr} is greater than τ_{th}, thermal diffusion dominates and τ_f will be τ_{th}. The time required to reach $\eta = 99.99\%$ when thermal diffusion dominates t_4^{th} is given by

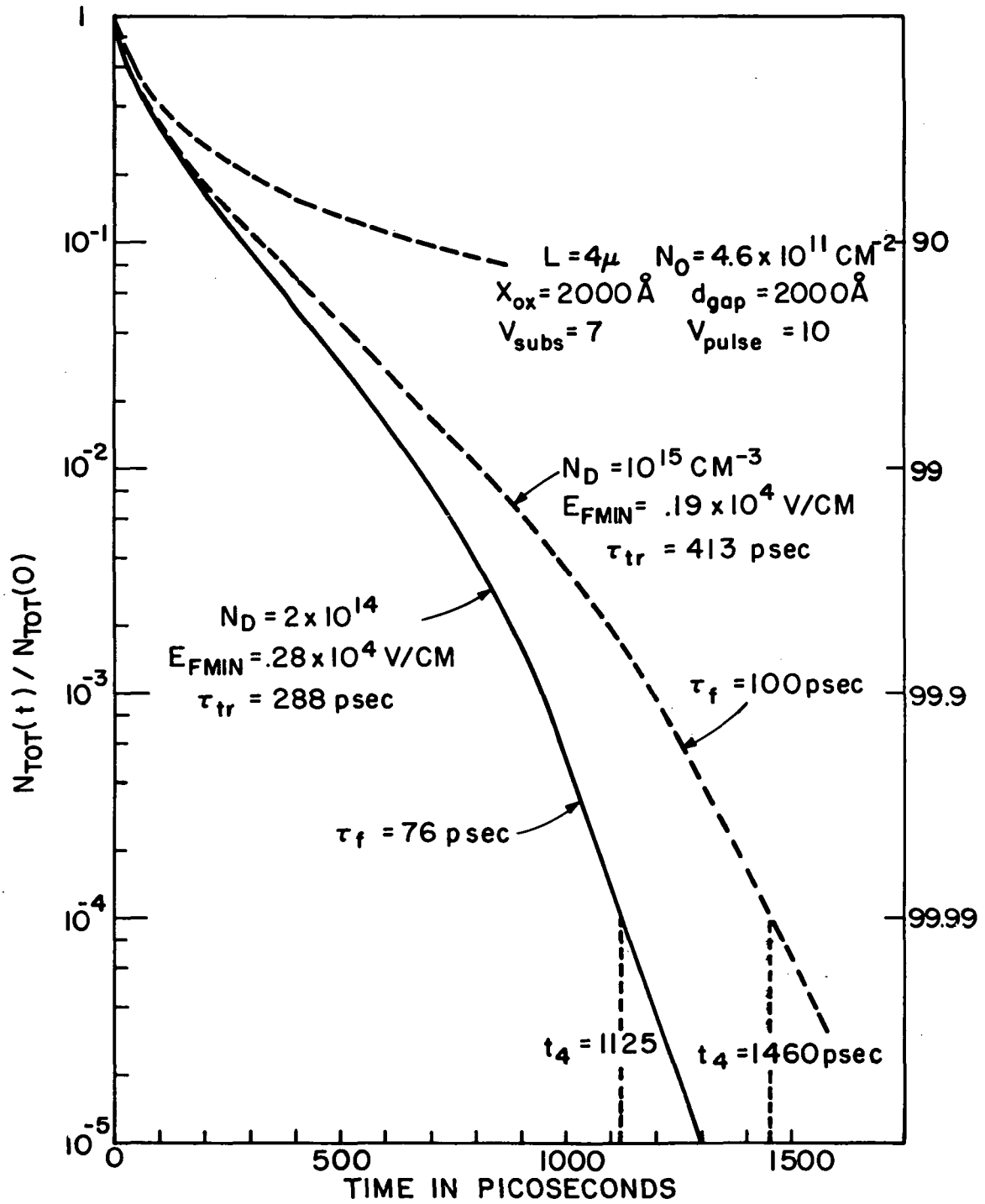

Figure 41. Normalized total charge remaining vs. time for the 10^{15} and 2×10^{14} cm^{-3} doping cases, L = 4 μm. The lower doping results in higher minimum, ringing field and faster charge transfer.

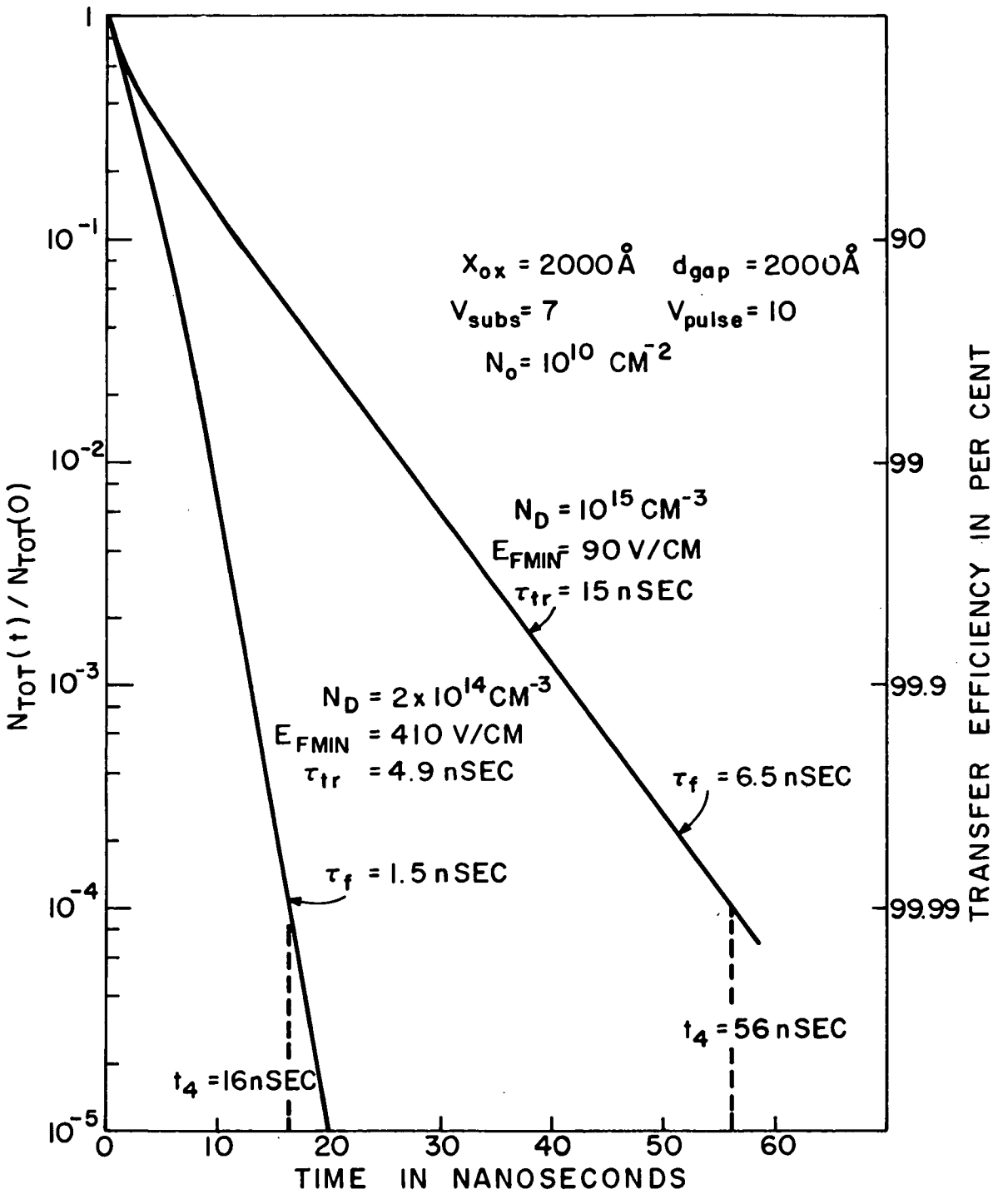

Figure 42. Normalized total charge remaining vs. time for 10-μm gate length, both 10^{15} and 2 x 10^{14}cm^{-3} doping. Initial charge concentration was low so that no self-induced drift effects are observed.

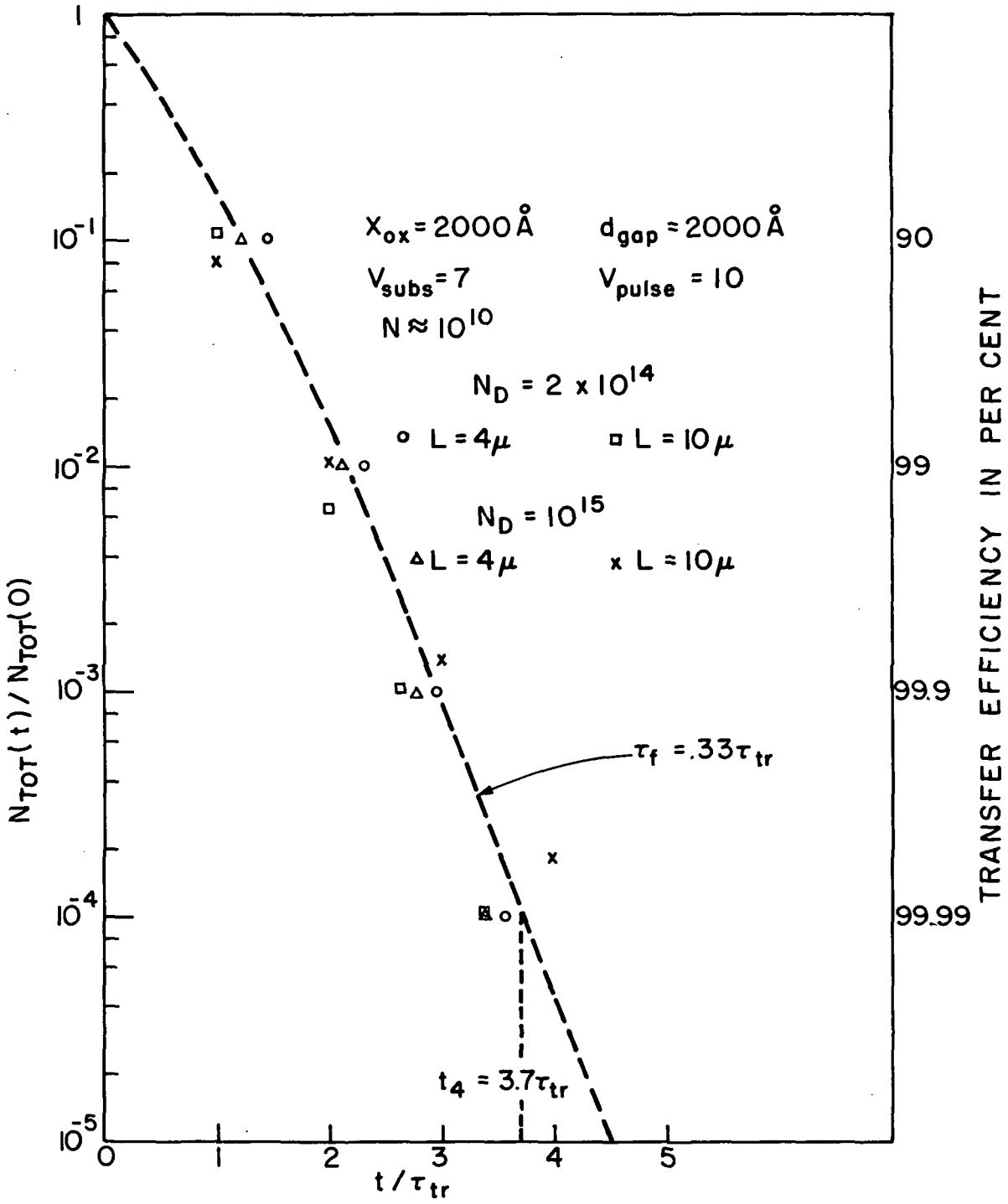

Figure 43. Normalized total charge remaining vs. time normalized by the single carrier transit time τ_{tr}.

$$t_4^{th} = \tau_{th}\left(6.7 - \log\frac{qn_o}{C_{ox}}\right) \cong 5.5\ \tau_{th} \tag{82}$$

4. GRADIENT METHOD VS. INTEGRAL METHOD FOR SELF-INDUCED FIELD CALCULATION

Since an alternative method of calculating the self-induced fields, the integral method (Part 2), has been introduced, the natural question of comparison with the gradient method arises. The most meaningful comparison involves the electric fields and overall charge transfer results for the two different methods. The degree of agreement between the gradient and integral methods for calculating self-induced field magnitudes depends upon the charge profile. Almost no agreement is obtained for the uniform charge concentration; the gradient method predicting zero field except at the edges, while the integral method prediction is given by Eq. (70) and Figure 34. Figure 44 shows a comparison for a charge profile which was picked at random during a computer simulation of charge transfer in a 4-μm gate case. To the left where the self-induced fields hinder charge transfer, the integral method predicts higher fields, while on the right, where self-induced fields aid charge transfer, the integral method fields are lower. Thus, the integral method should predict slower charge transfer than the gradient method and, in fact, comparison of the charge transfer rates using the two methods tends to bear this out. Figure 45 shows the overall charge decay vs. time for the 4-μm gate 10^{15}cm^{-3} doping case using the two methods. As expected, the integral method is slower with approximately twice the total charge remaining at any given time. However, because self-induced drift is important for only the first decade or so of charge transfer in what is essentially an exponentially decaying process, there are no significant time differences in the overall charge transfer characteristics for the two methods. In view of the fact that the integral method takes much more computer time, the gradient method is probably better suited for certain numerical solutions.

On the other hand, the integral method is required to accurately calculate charge profiles in storing potential wells and express the self-induced field magnitude as a function of the charge concentration rather than charge gradient.

5. DISCUSSION AND CONCLUSIONS

Equations (80) and (81) provide a rough estimate of the free charge transfer performance at room temperature for three phase charge-coupled structures which have strong drift-aiding

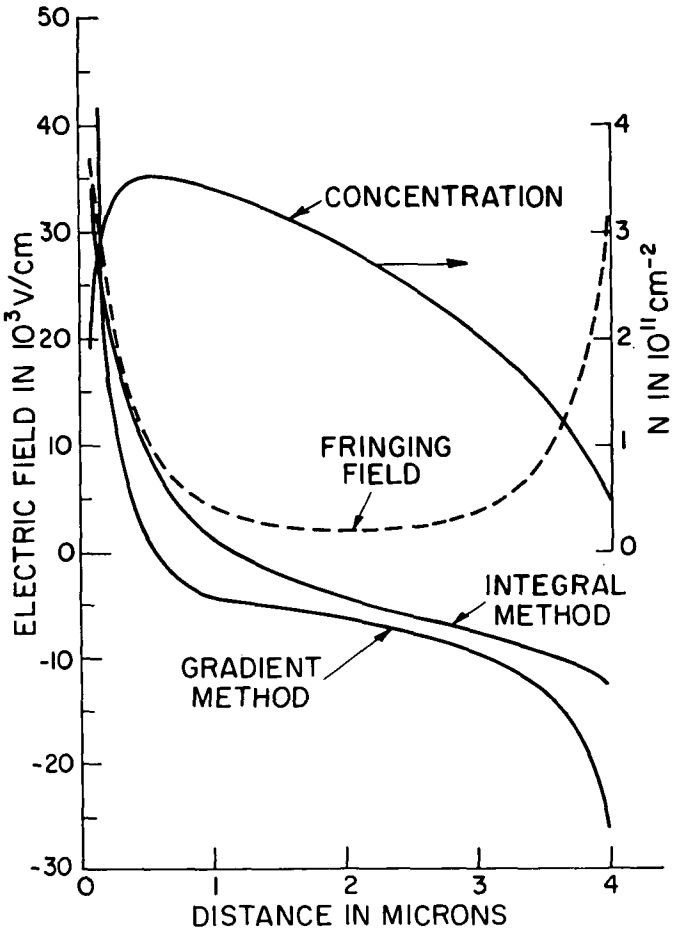

Figure 44. Comparison of the self-induced fields calculated by the integral and gradient methods for charge profile picked at random during computer simulation of charge transfer in 4-μm gate case. Charge concentration profile is shown at top. Negative of fringing field is also shown for comparison purposes.

fringing fields — at least for the closely-spaced electrode structures studied. Larger gaps between electrodes will change the fringing field profile and may lead to relationships which differ from Eqs. (80) and (81). Based upon Eqs. (80) and (81) the expected performance of closely-spaced, three-phase CCD's for various gate lengths and doping densities can be assessed based on knowledge of the fringing field profile alone, since this determines τ_{tr}. Reference A-6 describes an analytical solution for three-phase fringing field magnitudes and presents a relatively simple expression for the single carrier transit time (again probably valid only for closely spaced CCD structures) given by

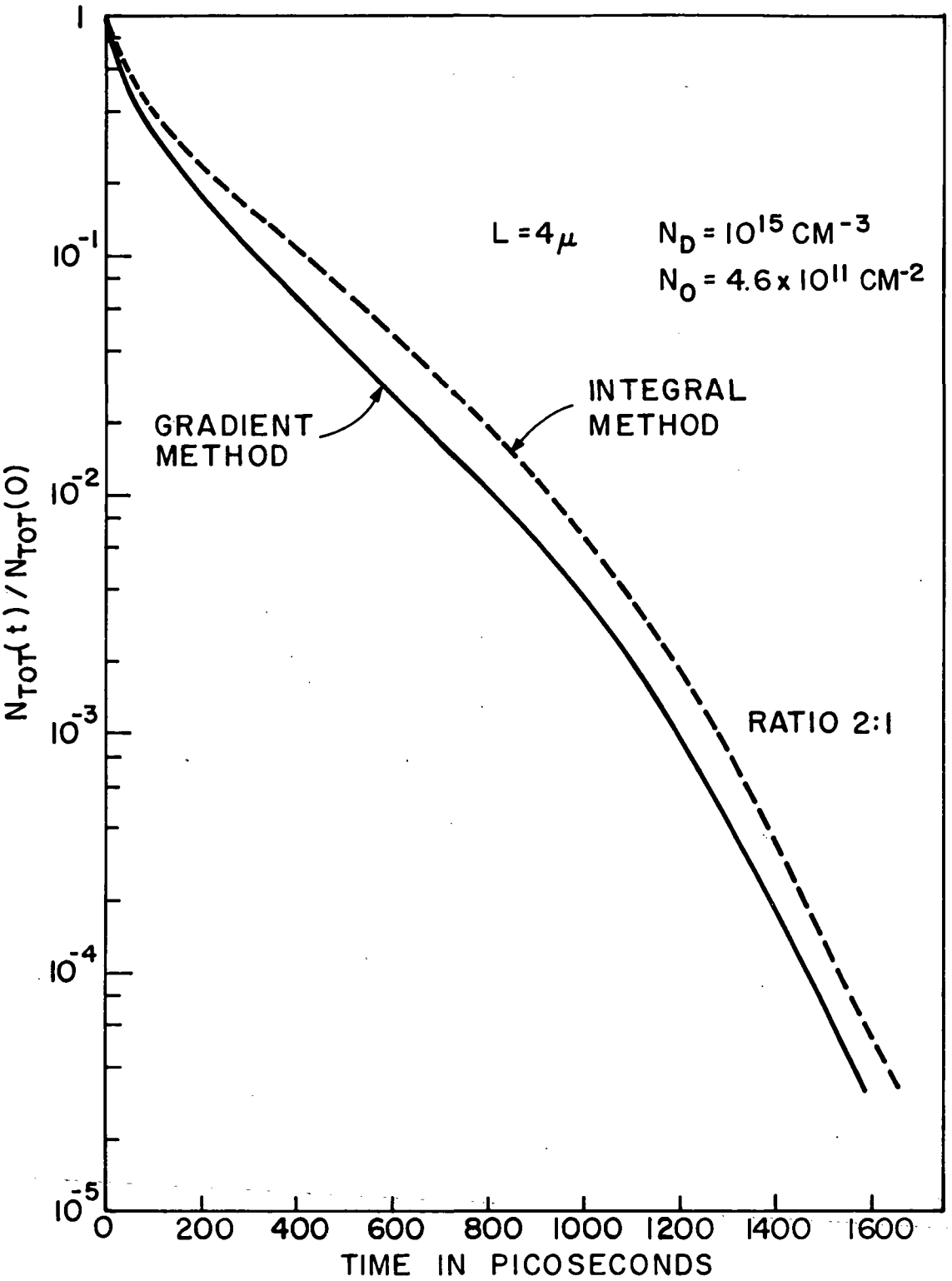

Figure 45. Comparison of the normalized total charge remaining vs. time for self-induced fields calculated by integral and gradient methods.

$$\tau_{tr} = \frac{L^3}{6.5\mu X_{ox} V} \left(\frac{5X_d/L + 1}{5X_d/L} \right)^4 \qquad (83)$$

where V is the pulse voltage, X_d is the depletion width at the center of the transferring electrode, and the other symbols have their usual meaning. The time to achieve $\eta = 99.99\%$ ($t_4 \cong 4\tau_{tr}$) is a reasonable figure of merit since this is consistent with devices with several hundred gates. Based upon Eqs. (81) and (83), Figure 46 shows t_4 vs. gate length for various doping levels. The points show the values predicted by computer simulation. Also shown by the dotted line is the t_4 predicted by thermal diffusion, Eq. (82), assuming $n_o = 5 \times 10^{11} cm^{-2}$. When the t_4 based upon fringing field considerations exceeds the thermal diffusion value, the latter time applies. In other words, the thermal diffusion t_4 is the longest time required for $\eta = 99.99\%$ for any configuration. Figure 46 clearly shows the advantage to be gained in speed by using low doped substrates to maximize the fringing field — especially below 15-μm gate lengths. Noteworthy is the 10-MHz operation predicted for 10-μm gates and 100-MHz

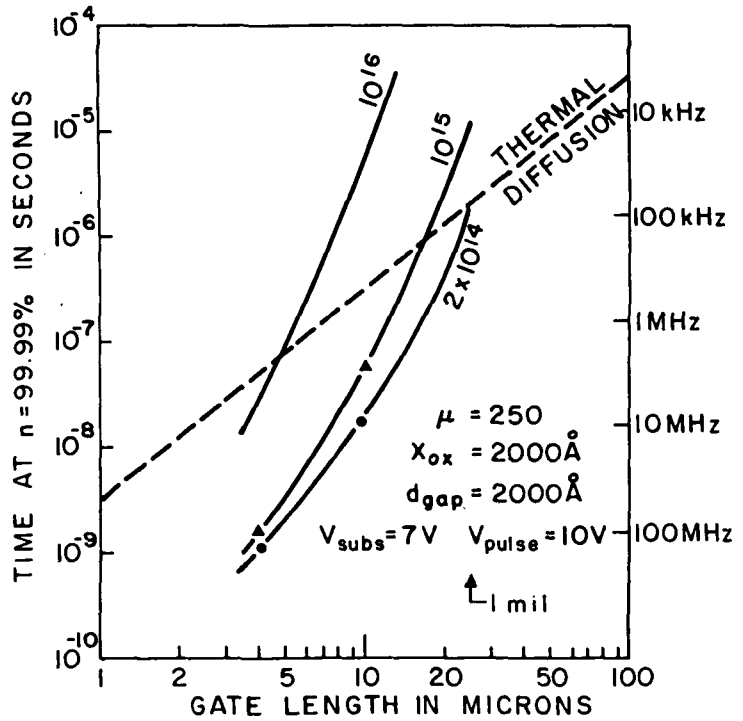

Figure 46. Time required to achieve $\eta = 99.99\%$ vs. gate length for various doping levels. The thermal diffusion line is the maximum time required in any case.

operation predicted for 4-μm gates. It must be kept in mind, however, that these predictions are based only upon the consideration of free charge transfer effects. No interface state trapping has been considered and this effect could possibly limit the transfer efficiency and frequency of operation to lower values than those predicted by Figure 46.

However, it is clear from these results that fringing field drift can be the most important transfer mechanism in appropriately designed CCD structures. Ironically, fringing field drift is also the most difficult mechanism to analyze, requiring numerical solutions to determine the charge decay characteristics. The relationships of Eqs. (80) and (81) were obtained for closely spaced electrodes and other configurations may give different results.

It is also clear from this study that in CCD structures which have strong drift-aiding fringing fields the transfer of free charge is sufficiently fast so that it should not be a factor in device design or operation. More specifically, incomplete transfer schemes such as "fat zero" operation (ref. A-8) do not appear necessary from a free charge transfer standpoint. However, such schemes may be useful in reducing surface state losses.

In conclusion, the three mechanisms causing free charge transfer in CCD's have been discussed. A new method for calculating self-induced fields as a function of charge concentration has been presented. A numerical solution of the charge transfer process shows that self-induced drift dominates during short times, but the majority of transfer is controlled by fringing field drift which is fast enough for 10-MHz operation with 10-μm gates and 100-MHz operation with 4-μm gates, provided interface state losses are negligible.

Supplement I: Charge Transfer by Thermal Diffusion. — The charge transfer due to thermal diffusion alone can be determined by means of Fourier analysis of the charge profile (ref. A-9). The diffusion equation which describes the decay of charge is obtained by substituting Eq.(57) of the text using only the thermal diffusion term, into Eq. (58) to obtain:

$$\frac{\partial n(y,t)}{\partial t} = D \frac{\partial^2 n(y,t)}{\partial y^2} \tag{84}$$

For the case of zero carrier gradient at y = 0 and zero carrier concentration at y = L, a Fourier expansion yields the following general solution where the coefficients are determined by the initial carrier profile n(y,0):

$$n(y,t) = \sum_{k=0}^{\infty} \alpha_k \cos(\lambda_k y) \exp(-\lambda_k^2 Dt) \tag{85}$$

where

$$\lambda_k = \frac{\pi}{2L}(2k+1)$$

and

$$\alpha_k = \frac{2}{L}\int_0^L n(y,0)\left[\cos\frac{\pi(2k+1)y}{2L}\right]dy$$

If the initial concentration is uniform; i.e., $n(y,0) = n_o$ for $0 \leq y \leq L$, then

$$\alpha_k = \frac{4n_o}{(2k+1)\pi}(-1)^k \qquad 0 < k < \infty \tag{86}$$

and

$$n(y,t) = \sum_{0}^{\infty} \frac{4n_o(-1)^k}{(2k+1)\pi} \cos\left(\frac{(2k+1)\pi y}{2L}\right) \exp\left[-\frac{(2k+1)^2\pi^2 Dt)}{4L^2}\right] \tag{87}$$

Each of the terms in the sum decay exponentially with a decay time τ_k given by

$$\tau_k = \frac{4L^2}{(2k+1)^2\pi^2 D} \tag{88}$$

The higher order terms decay faster and the charge profile quickly decays to a cosine shape after which the charge profile is given by

$$n(y,t) = \frac{4n_o}{\pi} \cos\frac{\pi y}{2L} \exp\left(-\frac{\pi^2 D}{4L^2} t\right) \tag{89}$$

with the total charge remaining after time t given by

$$N_{tot}(t) = \int_0^L n(y,t)dy = \frac{8}{\pi^2} N_{tot}(0) \exp\left(-\frac{\pi^2 D}{4L^2} t\right) \tag{90}$$

Aside from a small fraction of charge which decays very quickly, the decay of the total charge due to thermal diffusion can be considered to be exponential with decay constant $L^2/2.5D$.

Supplement II: Approximate Analysis of Self-Induced Drift. — Equation (64) of the text can be solved numerically but the results do not in themselves provide useful insight into the self-induced drift process. The numerical results do point out, however, that after a very short time the decaying carrier profile maintains the same relative shape with all points having the same time dependence. This implies that the carrier concentration at the surface is separable into a product solution:

$$n(y,t) = h(y)g(t) \tag{91}$$

This removes the partial differentials from Eq. (64) and permits the separation of variables with each side of the equation necessarily equal to a constant according to

$$\frac{1}{g^2(t)} \frac{dg(t)}{dt} = -A = \frac{\mu q}{2C_{ox}} \frac{1}{h(y)} \frac{d^2h^2(y)}{dy^2} \tag{92}$$

where A is a constant depending upon the initial conditions. The time dependence is then given by

$$g(t) = \frac{g(0)}{1 + Ag(0)t} \tag{93}$$

and the decay of charge is given by the ratio

$$\frac{g(t)}{g(0)} = \frac{t_o}{t + t_o}, \quad t_o = \frac{1}{Ag(0)} \tag{94}$$

In order to obtain an estimate for the constant t_o, we note that the continuity equation can be written formally as a diffusion equation:

$$j_n(y,t) = -\mu n(y,t) \frac{q}{C_{ox}} \frac{\partial n(y,t)}{\partial y} = -D_{eff} \frac{\partial n(y,t)}{\partial y} \tag{95}$$

with

$$D_{eff} = \frac{\mu q}{C_{ox}} \quad n(y,t) \tag{96}$$

Treating D_{eff} as a constant, we then write down a solution corresponding to Eq. (87), limiting ourselves, however, to the leading term of the Fourier series so as to satisfy the condition (91):

$$n(y,t) = h(y)g(t) = n_o \cos \frac{\pi y}{2L} \exp\left(-\frac{\pi^2 D_{eff} t}{4L^2}\right) \tag{97}$$

We then determine the average value of Ag(0) over the electrode length L to find $1/t_o$:

$$\frac{1}{t_o} = Ag(0) = -\frac{1}{L} \int_0^L \frac{1}{g^2(t)} \frac{dg(t)}{dt} g(0)dy$$

$$g(0) = 1$$

and using Eqs. (95) and (97)

$$\frac{1}{g^2(t)} \frac{dg(t)}{dt} = -\frac{\pi^2 \mu q}{4L^2 C_{ox}} n_o \cos \frac{\pi y}{2L} \tag{98}$$

$$\frac{1}{t_o} = \frac{\pi^2}{4L^3} \frac{\mu q n_o}{C_{ox}} \int_0^L \cos \frac{\pi y}{2L} dy = \frac{\mu q n_o \pi}{2L^2 C_{ox}}$$

Thus,

$$t_o = \frac{L^2 C_{ox}}{1.57 \mu q n_o} \tag{99}$$

This is only an approximate solution but provides insight into the decay process and the parameters which affect t_o.

Supplement III: Integral Method for Calculating Self-Induced Fields. — Consider an infinite line charge of λ coul/cm along the z-axis located at the interface between two dielectrics which forms the y-z plane [see Fig. 34(a)]. An infinite ground plane parallel to the dielectric is located a distance X_o from the line charge. It is desired to calculate the electric field at the dielectric interface directed perpendicular to the line charge axis. This will be the self-induced field due to a line charge element which will affect charge motion in the direction of transfer.

The desired field can be calculated using the method of images, but since charge is reflected by both the ground plane and the dielectric interface, an infinite series of image line charges is required to satisfy all of the boundary conditions. The reflection of a line charge λ_n through the ground plane results in an image charge $-\lambda_n$ located an equal distance on the other side of the ground plane. When reflecting a line charge λ_n at $-X_n$ through the dielectric interface the following rules apply:

An image line charge located at $+ X_n$

$$\lambda_n' = -\lambda_n \frac{1 - \epsilon}{1 + \epsilon} \quad \epsilon = \epsilon_1/\epsilon_2 \tag{100}$$

is used along with λ_n to calculate the potential for $x < 0$. This image charge must itself be reflected through the ground plane.

An image line charge located at $-X_n$

$$\lambda_n'' = \frac{2}{1 + \epsilon} \lambda_n \tag{101}$$

is used alone to calculate the potential for $x > 0$. The original "real" line charge λ located at $X = 0$ is reflected along with its λ' image through the ground plane to form a $\lambda_1 = -\lambda \frac{2\epsilon}{1+\epsilon}$ image at $x = 2X_0$. This charge contributes to the potential in both ϵ_1 and ϵ_2 regions, and is then reflected by the dielectric interface to form the λ_1' image at $+2X_o$ which is used along with λ_1 to calculate potential in ϵ_1 region. The λ_1'' image at $-2X_o$ contributes to the potential in ϵ_2 region. The λ_1' image is then reflected through the ground plane to form $-\lambda_1'$ image at $-3X_o$ and the process repeats *ad infinitum* to form two infinite series of image charges.

Using this procedure, the potential for the ϵ_1 region and ϵ_2 region are given by

$$\phi_1 = \frac{-\epsilon\lambda}{(1+\epsilon)\pi\epsilon_1} \sum_1^{\infty} \left(\frac{1-\epsilon}{1+\epsilon}\right)^{n-1} \ln \frac{\sqrt{[x - 2(n-1)X_o]^2 + y^2}}{\sqrt{(x + 2nX_o)^2 + y^2}} \tag{102}$$

$$\phi_2 = -\frac{\lambda}{(1+\epsilon)\pi\epsilon_2} \left[\ln \sqrt{x^2 + y^2} - \frac{2\epsilon}{1+\epsilon} \sum_1^{\infty} \left(\frac{1-\epsilon}{1+\epsilon}\right)^{n-1} \ln \sqrt{(x + 2nX_o)^2 + y^2}\right] \tag{103}$$

These potentials can be shown to satisfy the following boundary condition requirements:

1) $\phi_1(-X_o, y) = 0$ — Ground plane

2) $\phi_1(0,y) = \phi_2(0,y)$ — Continuous potential at dielectric interface

3) $\epsilon_1 \left.\frac{\partial\phi_1}{\partial x}\right|_{x=0} = \epsilon_2 \left.\frac{\partial\phi_2}{\partial x}\right|_{x=0}$ — Continuous normal D at dielectric interface

4) $\lim_{r \to 0} \left[\pi r\epsilon_1 \left(-\frac{\partial\phi_1}{\partial r}\right) + \pi r\epsilon_2 \left(-\frac{\partial\phi_2}{\partial r}\right)\right] = \lambda$ — Gauss' law at origin

The electric field in question is then given by

$$E_y(0,y) = -\frac{\partial \phi_2}{\partial y} = \frac{\lambda}{\pi \epsilon_2 (1+\epsilon)} \left[\frac{1}{y} - \frac{2\epsilon}{1+\epsilon} \sum_{1}^{\infty} \left(\frac{1-\epsilon}{1+\epsilon} \right)^{n-1} \frac{y}{(2nX_o)^2 + y^2} \right] \tag{104}$$

This is just the field due to a line charge element. By integrating the contributions of all the line charge elements which make up a surface charge distribution extending from L_1 to L_2 (with variations only along the y direction) the self-induced electric field is determined and is given by

$$E_s(y) = \frac{-1}{\pi \epsilon_2 (1+\epsilon)} \left[\int_{y-L_1}^{L_2-y} \frac{\sigma(y) y dy}{y^2} - \frac{2\epsilon}{1+\epsilon} \sum_{1}^{\infty} \left(\frac{1-\epsilon}{1+\epsilon} \right)^{n-1} \right. \tag{105}$$

$$\left. \int_{y-L_1}^{L_2-y} \frac{\sigma(y) y dy}{(2nX_o)^2 + y^2} \right]$$

For an arbitrary $\sigma(y)$ this calculation is best done by computer, but an analytical solution is possible for a uniform charge distribution σ_o which extends from y = 0 to y = L. If $\beta \equiv y/L$, then

$$E_s(y) = \frac{-\sigma_o}{2\pi(\epsilon_1 + \epsilon_2)} \sum_{1}^{\infty} \left(\frac{1-\epsilon}{1+\epsilon} \right)^{n-1} \ln \left\{ \frac{1 + \left[\frac{2(n-1)X_o}{(1-\beta)L} \right]^2}{1 + \left[\frac{2(n-1)X_o}{\beta L} \right]^2} \frac{1 + \left[\frac{2nX_o}{\beta L} \right]^2}{1 + \left[\frac{2nX_o}{(1-\beta)L} \right]^2} \right\} \tag{106}$$

By defining the sum, which does not depend upon σ_o, as the shape function, $S(y/L, 2X_o/L)$, we can write for $Si\text{-}SiO_2$

$$E_s(y) = \frac{\sigma_o}{2\pi(\epsilon_1 + \epsilon_2)} S\left(\frac{y}{L}, \frac{2X_o}{L}\right) = 1.8 \times 10^3 \left(\frac{n_o}{10^{11}}\right) S\left(\frac{y}{L}, \frac{2X_o}{L}\right) V/cm \qquad (107)$$

where $n_o = \sigma_o/q$

Typical S plots are shown in Figure 34(b).

List of Symbols

A	Constant
C_{ox}	Oxide capacitance per unit area (f/cm^2)
D	Diffusion constant
D_{eff}	Effective diffusion constant associated with self-induced drift. $D_{eff} = (\mu q/C_{ox})\, n(y,t)$
$E_{F(y,t)}$	Fringing field at interface along direction of charge motion (V/cm)
$E_{S(y,t)}$	Self-induced field at interface along direction of charge motion (V/cm)
$h(y)$	Function describing the y-dependence of $n(y,t)$ for all t
$g(t)$	Function describing time dependence of $n(y,t)$ for all y
$j_n(y,t)$	Electron particle current density
k	Boltzmann's constant
$n(y,t)$	Concentration of signal carriers in CCD inversion layer ($\#/cm^2$)
n_{ave}	Average value of signal carrier concentration; i.e. $n_{ave} = \frac{1}{L} \int_0^L n(y,t)dy$
n_o	Uniform concentration of signal carriers (cm^{-2})
$N_{tot}(t)$	Total number of carriers remaining under electrode at time t; i.e. $N_{tot}(t) \int_0^L n(y,t)dy$
$N_{tot}(0)$	Total number of carriers under electrode at beginning of transfer process
q	Electronic charge
t	Time from beginning of transfer process
t_o	Characteristic time associated with decay of charge via self-induced drift

t_1	Time required for charge to decay to point where self-induced fields are equal to thermal fields.
t_4	Time required to reach 99.99% transfer efficiency
t_4^{th}	Time required to reach 99.99% transfer efficiency in the absence of fringing fields; i.e., thermal diffusion dominates the transfer process
T	Absolute temperature (°K)
V	Clock voltage
V_T	Thermal voltage: kT/q
x	Direction normal to Si-SiO_2 interface
X_d	Depletion layer thickness at center of transferring electrode
X_o	Gate oxide thickness
y	Direction of charge motion
ϵ_1	Dielectric permittivity of insulator
ϵ_2	Dielectric permittivity of semiconductor
ϵ	ϵ_1/ϵ_2
$\phi_s(y,t)$	Surface potential (volts)
ϕ_{so}	Surface potential in the absence of signal carriers; i.e., when $n(y,t) = 0$
λ	Line charge density (C/cm)
η	Charge transfer efficiency
μ	Field effect mobility
$\sigma(y)$	Surface charge density
τ_f	Time constant of exponential decay of final remaining charge; i.e., final decay constant
τ_{th}	Exponential decay constant for thermal diffusion
τ_{tr}	Single carrier transit time. The time required for a single carrier to drift the length of the electrode under influence of the fringing field.

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APPENDIX B

TRAILING PULSE AMPLITUDE FOR CASE OF FREE CHARGE LOSSES

(ϵ independent of signal level)

It is desired to find the general expression from the amplitude of the j^{th} trailing pulse after the last "1" in a string of "1s", after being transferred to the i^{th} gate, $p_j(i)$, when the loss at each gate is a fixed fraction ϵ of the charge transferred. It is assumed that the string of "1s" is long enough for the pulses to reach the full input amplitude, p_o. Consider the first trailing pulse after the last "1", $p_1(i)$. When the last "1" transfers from gate 1 to gate 2, it leaves behind ϵp_o; therefore,

$$p_1(1) = \epsilon p_o \tag{108}$$

At gate 2, the last "1" leaves behind another ϵp_o, and $(1 - \epsilon)\, p_1(1)$ is transferred from gate 1 to gate 2 so that

$$p_1(2) = 2\epsilon p_o - \epsilon^2 p_o \tag{109}$$

Likewise,

$$p_1(3) = 3\epsilon^2 p_o + \epsilon^3 p_o \tag{110}$$

By proceeding in this manner, one can establish that the general expression for the first trailing pulse after i transfers is

$$p_1(i) = p_o \sum_{k=1}^{i} (-1)^{k+1} \binom{i}{k} \binom{k-1}{0} \epsilon^k \tag{111}$$

where $\binom{i}{k}$ is the binomial coefficient

$$\binom{i}{k} = \frac{i!}{(i-k)!\,k!} \tag{112}$$

The generalized expression for the amplitude of the j_{th} trailing pulse after i transfers is given by

$$p_j(i) = p_o \sum_{k=1}^{i} (-1)^{k+1} \epsilon^{k+j-1} \binom{i+j-1}{k+j-1} \binom{k+j-2}{j-1} \tag{113}$$

If this analysis is correct, then the sum of all trailing pulses at any instant in time should be equal to ϵp_o times the number of transfers made by the last "1".

$$\text{Total loss} = \epsilon N_g p_o = \sum_{j=1}^{N_g} p_j(N_g - j + 1) \tag{114}$$

Note that when the last "1" has made N_g transfers, the first trailer is at $i = N_g$, the second at $i = N_g - 1$, etc., so the index i is $N_g - j + 1$.

$$\text{Total Loss} = p_o \sum_{j=1}^{N_g} \sum_{k=1}^{N_g-j+1} (-1)^{k+1} \epsilon^{k+j-1} \binom{N_g}{k+j-1} \binom{k+j-2}{j-1} \tag{115}$$

This double sum is best evaluated by examining the sum of terms in like powers of ϵ, say ϵ^r. If $k + j - 1 = r$, then the second sum is removed and only the $k = r + 1 - j$ term used.

$$\text{Coefficient of } \epsilon^r \text{ term} = p_o \sum_{j=1}^{N_g} (-1)^{r-j} \epsilon^r \binom{N_g}{r} \binom{r-1}{j-1} \tag{116}$$

$$= p_o \binom{N_g}{r} \epsilon^r (-1)^r \sum_{j=1}^{N_g} (-1)^{j-1} \binom{r-1}{j-1}$$

However, provided $u \neq 0$, the sum:

$$\sum_{v=0}^{u} (-1)^{v} \binom{u}{v} = 0 \tag{117}$$

This is the same as the sum in Eq. (116) for all r except r = 1; therefore, the coefficients of all terms of ϵ^r for $r > 1$ are zero. Thus, as can be seen by evaluating Eq. (116) for r = 1 and j = 1, the total loss is given by $p_o \epsilon N_g$ as required.

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