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RELIABILITY OF HYBRID MICROCIRCUIT DISCRETE COMPONENTS

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16. ABSTRACT

Hybrid microcircuit technology has rapidly become a standard technique in development and fabrication of electronic hardware. The most obvious reasons for the rapid acceptance of hybrids are small size, reduced weight and higher reliability. The reliability of a hybrid microcircuit is determined by factors such as wire bonding, interconnection techniques, thick- and thin-film processing, discrete component mounting, and hermetic sealing. Most of these factors can be controlled during fabrication cycles with proper process controls. However, since the hybrid manufacturer has little or no control on the design and fabrication of discrete components, these devices have the most paramount effect on microcircuit reliability. Therefore, each hybrid manufacturer must establish criteria for selection, qualification, and screening of discrete devices.

This report details the data accumulated during 4 years of research and evaluation of ceramic chip capacitors, ceramic carrier mounted active devices, beam-lead transistors, and chip resistors. Life and temperature coefficient test data, and optical and scanning electron microscope photographs of device failures are presented and the failure modes are described. Particular interest is given to discrete component qualification, power burn-in, and procedures for testing and screening discrete components. Burn-in requirements and test data will be given in support of 100 percent burn-in policy on all NASA flight programs.

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RELIABILITY OF HYBRID MICROCIRCUIT DISCRETE COMPONENTS

INTRODUCTION

The rapid acceptance of hybrid microcircuits as a major contributor to electronic system integration has created many problems in defining and describing accurate reliability factors. The reliability of hybrid microcircuits is determined by factors such as wire bonding, interconnection techniques, thick- and thin-film processing, discrete component mounting, and hermetic sealing. These factors can be controlled and regulated during fabrication cycles with proper process controls. However, the discrete component, over which the hybrid manufacturer exercises little or no control, poses the most dominating effect on microcircuit reliability. With this consideration, each hybrid manufacturer must establish criteria for selection, qualification, and screening of discrete devices.

The Marshall Space Flight Center (MSFC) conducts inhouse research and development in hybrid technology and fabricates prototype microcircuits for feasibility studies. The hybrid facility performs inhouse evaluations of microcircuit discrete components. Results of these evaluations are distributed to hybrid manufacturers under NASA contract and NASA systems groups to use as guidelines in the design and specification of hybrid systems. Results of microcircuit discrete component evaluations accumulated over several years of study are summarized in this report.

HYBRID PROBLEMS

To list and discuss all the problems encountered in the fabrication and use of hybrid microcircuits would be difficult, but this does not imply that hybrids are less reliable than other assembly methods. On the contrary, when microcircuitry is required, hybrids are definitely more advantageous and reliable to use than most assembly methods. The trends at MSFC and in industry indicate that hybrids are gaining in popularity and usage. Generally, these microcircuits are produced in relatively small volume with a high degree

of sophistication. Only a few companies have experienced millions of manhours in reliability testing and volume production of hybrids. Because of this low volume production and circuit specialization, hybrid microcircuits are currently higher cost items than conventional electronics. However, this cost factor will improve as the technology develops and usage increases. Good quality control and product assurance, selection of proper fabrication and assembly techniques, and close surveillance will ensure a good reliable product; i.e., problems can be virtually eliminated in such areas as film defects, contamination, bond failure, parts mounting, and package sealing by using good production control methods with complete and practical documentation. However, one phase of hybrid microcircuit technology is causing the most concern and problems in relation to circuit reliability; i.e., the basic controlling factor in the reliability of hybrids is the quality of discrete parts used in the circuit. Because of this, our policy has been to recommend and apply screening procedures to every discrete component before assembly onto the substrate whenever long-life and high-reliability circuits are specified. Naturally, this can be a difficult and costly operation, especially when one considers the more complex integrated circuit chips being used today in hybrid assemblies.

DISCRETE COMPONENT QUALIFICATION AND SCREENING

Qualification and screening of discrete chip devices are necessary to assure maximum reliability of hybrid microcircuits. However, many problems arise when attempts are made to qualify and screen these devices. Among these problems are:

1. Determination of applicable specifications and standards.

2. Determination of meaningful test conditions.

3. Fabrication of handling, storage, and test fixtures.

Marshall Space Flight Center attempts to guarantee reliability of discrete chip devices through line certification. The method cannot be applied as a replacement for qualification and screening but is a valuable and necessary supplement.

Line Certification

In coordination with the Microelectronics Subcommittee of the NASA Parts Steering Committee, MSFC has developed a program called line certification to improve reliability of microcircuits. The main feature of the line certification program is based on the statistical control of key process steps. Work has been in progress for the past 7 years concerning monolithic microcircuits. Documentation and procedures have recently been developed for hybrid microcircuit processing and is currently being tested on a trial-run basis. The full monolithic-hybrid line certification program has been operational since June 1972.

The purpose of line certification is to raise the reliability level of microcircuits and, more important, to make this reliability more consistent to increase yield. For classification purposes, microcircuits are grouped into broad categories such as monolithic and hybrid (others are planned). Experience has been exclusively with monolithic manufacturing (semiconductor) facilities. First, upon the request of a supplier, an initial survey is conducted; then if sufficient microcircuits are being produced by a supplier in quantity and quality, an MSFC (or NASA-wide) team actually performs the line certification. The process usually requires three to four visits by the team and may take 1 to 2 years to complete, depending upon the suppliers' facilities and process controls. It is anticipated that line certification will be performed for hybrid microcircuits for pending procurement actions only. More details about the line certification program can be obtained from MSFC's Quality and Reliability Assurance Laboratory.

Qualification

At MSFC the following documents are used to reference most qualification tests conducted on discrete chip devices.

1. MIL-STD-202D, Test Methods for Electronic and Electrical Component Parts.

2. MIL-STD-883, Test Methods for Microelectronics.

3. MIL-STD-750A, Test Methods for Semiconductor Devices.

4. MSFC Specification 85M03927, Discrete Chip Devices for Hybrid Microcircuits.

However, these specifications have several shortcomings when applied to hybrid circuits. Among these are:

1. The specifications are often too general and frequently omit necessary test conditions.

2. Allowable percent changes and parameter variations are generally omitted from the specifications and are rarely given in the detailed component specification sheet.

3. Conditions such as shock and vibration levels are designed for large massive discrete components and are meaningless for small discrete chip devices.

Each discrete chip device required different qualification tests. Discrete chip devices are qualified by applying the tests and specifications given in Tables 1 through 4.

TABLE 1. QUALIFICATION TESTS FOR CERAMIC CAPACITORS

Test	Specification or Condition
Visual Examination	MSFC 85M03927
Capacitance	MSFC 85M03927
Dissipation Factor	MSFC 85M03927
Insulation Resistance	MSFC 85M03927
Dielectric Withstanding Voltage	MSFC 85M03927
Temperature Coefficient	MIL-STD-202D, Method 304
Operating Life	MIL-STD-202D, Method 108A Condition D

TABLE 2. QUALIFICATION TESTS FOR TANTALUM CAPACITORS

Test	Specification or Condition
Visual Examination	MSFC 85M03927
Capacitance	MSFC 85M03927
Dissipation Factor	MSFC 85M03927
Dc Leakage	MSFC 85M03927
Temperature Coefficient	MIL-STD-202D, Method 304
Operating Life	MIL-STD-202D, Method 108A, Condition D

TABLE 3. QUALIFICATION TESTS FOR RESISTORS

Test	Specification or Condition
Visual Examination	MSFC 85M03927
Dc Resistance	MIL-STD-202D, Method 303
Noise Index	MIL-STD-202D, Method 308
Temperature Coefficient	MIL-STD-202D, Method 304
Thermal Shock	MIL-STD-883, Method 1011
Operating Life	MIL-STD-202D, Method 108A, Condition D

TABLE 4. QUALIFICATION TESTS FOR TRANSISTORS

Test	Specification
Visual Examination	MSFC 85M03927 MIL-STD-883, Method 2010
Electrical Measurements	MSFC 85M03927 MIL-STD-750A
High Temperature and Impressed Voltage	MSFC 85M03927
Temperature Cycling	MIL-STD-883, Method 1010
Power Burn-in	MSFC 85M03927 1000 hours at maximum rated power

Screening

Screening, as applied to components for hybrid microcircuits, is the testing of a discrete device before assembly into a circuit. This screening may consist of reading only one parameter but, nevertheless, every discrete chip device is subjected to some type of pretesting.

At MSFC the most important factor controlling the reliability of hybrid microcircuits is the discrete chip devices in the assembly. As previously pointed out, problems with wire bonds, thin- and thick-film elements, contamination, and package sealing can be almost eliminated with good quality and process control procedures. However, most hybrid manufacturers purchase practically all discrete chip devices and therefore have little control over the manufacturing process. Regardless of the tight specification and screening requirements to which discrete devices are procured, a failure rate of 10 to 40 percent is very likely. A hybrid assembly with several discrete chip devices has a slight statistical chance of working properly without replacement of one or more parts. More than 50 percent of all custom hybrid assemblies are reworked or repaired at least once. The rework that is referred to and considered detrimental to reliability is the removal and replacement of discrete components.

Rework of hybrids is currently one of the most controversial problems facing the hybrid industry. Based on experience with inhouse programs and with hardware manufactured by contract, some degradation has been observed in the reliability of a circuit once it has been reworked. The only way to avoid rework is 100 percent screening and power burn-in of discrete chips before attachment on the substrate. This is the policy adopted by MSFC when requirements specify high reliability hybrid hardware. Since this policy requires special equipment and procedures, less critical circuit applications may not require 100 percent burn-in of all devices. The screening tests for discrete chip devices specified by the Hybrid Microcircuit Research Section are given in Tables 5 through 8. These tests are performed on every chip device before mounting into the hybrid assembly.

MSFC Approach. Screening can be done at various levels. For instance, screening can be performed where the device is manufactured or where the hybrid circuit is assembled. There are many different philosophies concerning the place where screening should be performed. However, Astrionics Laboratory recommends that screening tests be performed where the hybrid microcircuit is assembled because several problems have been traced to defective chip devices that were supposedly screened at the factory. This method substantially reduces the total cost of the discrete chip devices and creates an additional confidence that no defective part will be assembled into the hybrid microcircuit.

TABLE 5. SCREENING TESTS FOR CERAMIC CAPACITORS

Test	Specification
Visual Examination	MSFC 85M03927
Capacitance	MSFC 85M03927
Dissipation Factor	MSFC 85M03927
Insulation Resistance	MSFC 85M03927
Dielectric Withstanding Voltage	MSFC 85M03927
Power Burn-in	MSFC 85M03927

TABLE 6. SCREENING TESTS FOR TANTALUM CAPACITORS

Test	Specification
Visual Examination	MSFC 85M03927
Capacitance	MSFC 85M03927
Dissipation Factor	MSFC 85M03927
Power Burn-in	MSFC 85M03927

TABLE 7. SCREENING TESTS FOR RESISTORS

Test	Specification
Visual Examination	MSFC 85M03927
Dc Resistance	MIL-STD-202D, Method 303
Noise Index	MIL-STD-202D, Method 308
Low Temperature Operation	MIL-R-55342
Power Burn-in	MSFC 85M03927

TABLE 8. SCREENING TESTS FOR TRANSISTORS

Test	Specification
Visual Examination	MSFC 85M03927
Electrical Measurements	MSFC 85M03927
High Temperature and Impressed Voltage	MSFC 85M03927
Power Burn-in	MSFC 85M03927

Handling Problems. One of the problems with screening is the handling of the chip. Marshall Space Flight Center has developed and patented a spring-loaded test board for handling, shipping, storing, and testing chip devices. This includes chip resistors, chip capacitors, leadless inverted devices (LID), and beam-lead type transistors, diodes, and integrated circuits. With slight modifications, these test boards can be used for nearly all chip devices presently on the market. The basic test board, illustrated in Figure 1, is a single-sided rexolite printed wiring board. The chip devices are held in position with beryllium-copper springs soldered through the rexolite board to the gold-plated copper pattern. The use of these test boards in conjunction with simple fixturing for a multiburn-in station has greatly enhanced our ability to perform screening tests on discrete chip devices. At the present time, MSFC recommends that all semiconductor die requiring preassembly burn-in be procured mounted on ceramic carriers, such as LID or U-channel packages. This facilitates the screening processes and handling during assembly. Figures 2 and 3 illustrate chip devices in the test fixtures.

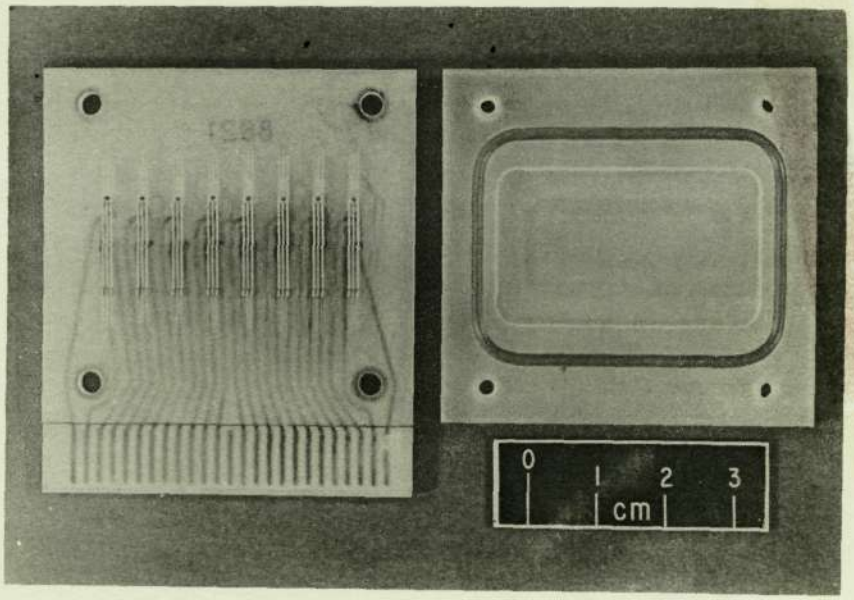

Figure 1. Spring-loaded test board for handling, shipping, storing, and testing chip devices.

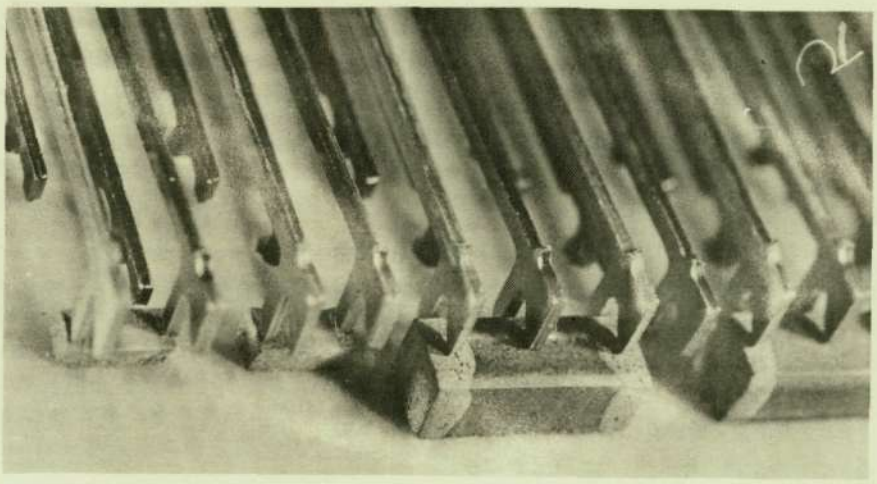

Figure 2. Chip capacitors mounted in spring-loaded test board.

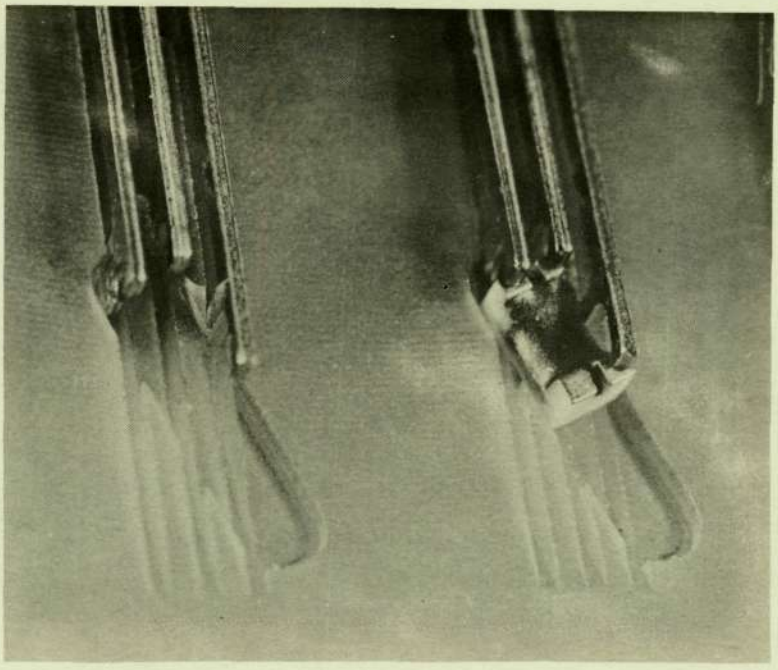

Figure 3. LID transistor mounted in spring-loaded test board.

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RESULTS OF FAILURE ANALYSIS STUDIES

Much test data on discrete chip devices have been accumulated over the past several years. A general survey of the discrete chip industry reveals that many of the chip devices fail to meet minimum MSFC screening and qualification specifications. Most of the chip devices sold today are designed for commercial application and lack sufficient process documentation and traceability. This section details results of visual examinations, scanning electron microscope examinations, and screening and qualification test results.

Incoming Receiving Visual Examination

Two specifications are used by MSFC to control visual examinations of microcircuit discrete devices: 85M03927, Discrete Chip Devices for Hybrid Microcircuits and 85M03924, Internal Visual Inspection of Semiconductor Devices. When tested to these specifications, discrete devices often encounter a fall-out rate of 10 to 30 percent. The primary causes of failure are misalignment, false cuts, cracks, nicks, scratches, metallization defects, and defective wedge and ball bonds. Figures 4, 5, 6, and 7 illustrate typical visual failures. The only way to control and possibly eliminate these types of failures is to impose the specifications stated. However, because this often reflects an individual discrete device price increase, MSFC usually purchases the parts without the specifications imposed and performs the testing after the parts are received.

Electrical and Environmental Evaluation

This section reveals data of tests performed on capacitors, resistors, and bipolar transistors. Each device was compared using different tests. Table 9 depicts the various tests used to illustrate the results.

Methods of Statistical Analysis

Discussion of ratio failure rate. The ratio failure rate is the ratio of the number of failures which occur during a unit interval of time to the original number of parts at the start of the reliability test. This is given by the formula $\lambda = \frac{f}{n}$, where λ = ratio failure rate, f = total failures during a given interval of time, and n = number of parts originally placed on test.

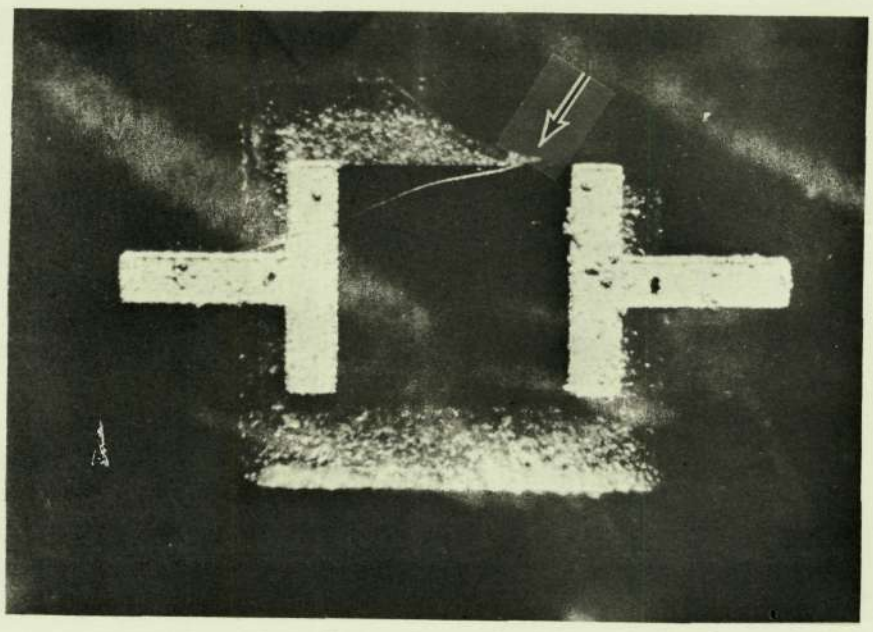

Figure 4. Cracked glass substrate of beam-lead resistor.

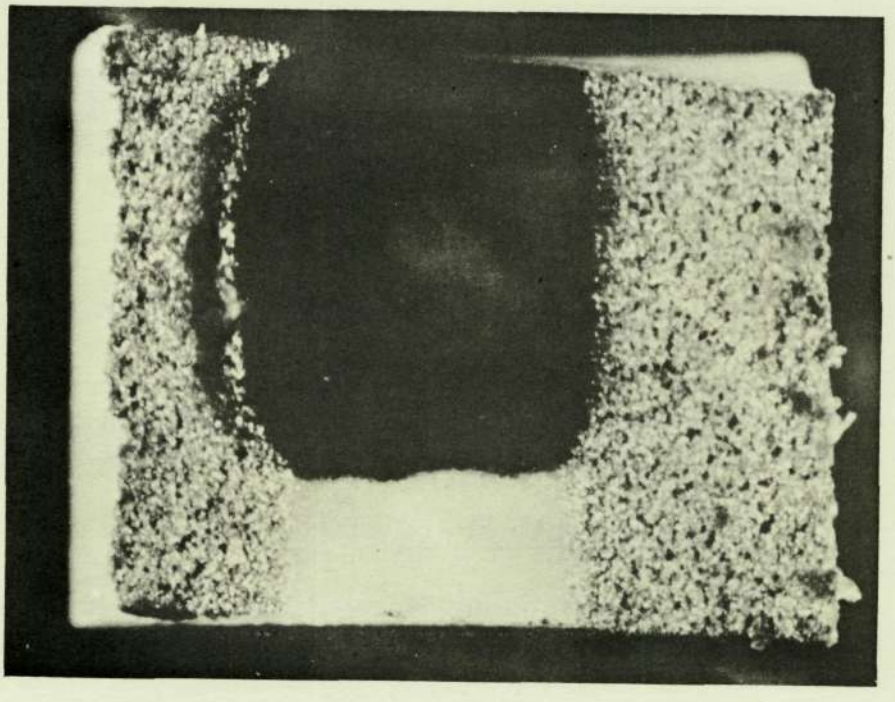

Figure 5. Misaligned metallization on chip resistor .

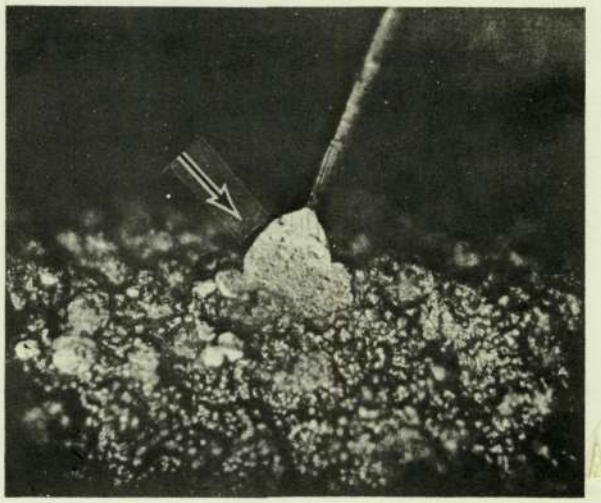

Figure 6. Pinched-off wedge bond on edge of LID step.

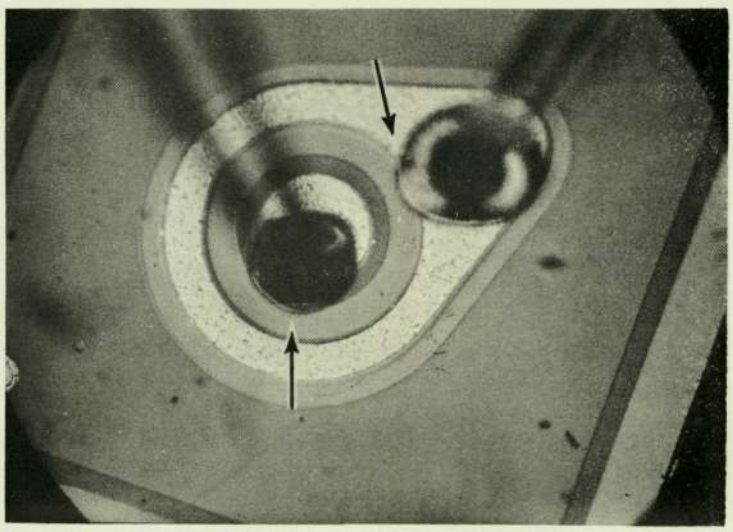

Figure 7. Ball bond on junction of die mounted in a LID carrier.

TABLE 9. RELIABILITY TESTS PERFORMED FOR FAILURE ANALYSIS STUDIES OF DISCRETE COMPONENTS

Component Type	Tests Performed
Capacitors	Temperature Coefficient (-55° C to 125° C) Life (1000 hours, 125° C, rated voltage)
Resistors	Temperature Coefficient (-65° C to 150° C) Life (1000 hours, 125° C, rated power)
Transistors	Life (emitter loading, 80 percent rated power)

The ratio failure rate is used to predict the probability of failure during a particular time interval and is especially useful in that it gives the fraction of original parts which are expected to survive during a particular time interval.

Discussion of failure rate. The failure rate, or hazard rate, is expressed in terms of failures per unit of time. It is computed as a simple ratio of the number of failures during a specified test interval to the aggregate survival test time of the devices undergoing test during the test interval. The equation for this relationship is $r = \frac{f}{T}$, where r = failure rate per hour, f = total number of failures for the test interval, and T = total test hours. This failure rate is used to predict the number of failures that will occur during a particular time interval.

Mean time between failures. The mean time between failures (MTBF) is probably the most commonly used term to describe component reliability. It is computed by taking the reciprocal of the failure rate and is expressed in units of time. As the term indicates, it is used to predict the mean time between failures for a component or circuit.

Capacitors. Three types of capacitors are generally used in hybrid microcircuits. These are barium-titanate ceramic chips, beam-lead tantalum chips, and solid-tantalum chips. The data given depict the test results of the barium-titanate ceramic chip capacitors only. Tests on the beam-lead and solid-tantalum types are in progress and will be reported at a later date. Tables 10 and 11 illustrate the data taken on these chip capacitors.

TABLE 10. RATIO FAILURE RATES FOR CAPACITORS SUBJECTED TO TEMPERATURE COEFFICIENT TESTS

Vendor	Number Tested	Number Failed	Ratio Failure Rate (percent)
A	56	44	78.6
B	90	2	2.2
C	128	22	17.2
D	66	56	84.8
E	180	41	22.8

TABLE 11. RELIABILITY DATA SUMMARY FOR CAPACITORS SUBJECTED TO OPERATING LIFE TESTS AT 125° C AND RATED VOLTAGE

Vendor	Number Tested	Number Failed	Total Test Hours	Failure Rate	MTBF	Ratio Failure Rate
				Per 10^6 Hours	Hours	Percent
A	56	17	46 448	366	2740	30.4
B	150	9	306 000	29	34 014	6.0
C	128	6	261 120	23	43 478	4.7
D	56	2	114 240	18	57 143	3.6

For the data given in Table 9, a failure was defined as any capacitor that failed to meet the specifications on the manufacturer's data sheets. Typically, this was ±15 percent capacitance change over the temperature range -55° C to +125° C for type K1200 and ±30 ppm/° C for type negative-positive-zero (NPO).

For the data presented in Table 10, a failure was defined as any capacitor that opened, shorted, had a capacitance change greater than ±10 percent, had a dissipation factor greater than 10 percent, or had an insulation resistance less than 10^4 MΩ or 100 MΩ - μF, whichever is less.

Resistors. Three types of resistors were examined: thick-film, cermet pellet, and tantalum nitride. Tables 12 and 13 illustrate the data taken for temperature coefficient and operating life tests, respectively.

TABLE 12. RATIO FAILURE RATES FOR RESISTORS SUBJECTED TO TEMPERATURE COEFFICIENT TESTS

Vendor	Number Tested	Number Failed	Ratio Failure Rate (percent)
A	32	1	3.1
B	60	2	3.3
C	160	16	10.0
D	96	23	24.0
E	100	2	2.0

In Table 12, vendors A and B represent thick-film resistors, vendor C is a cermet-pellet resistor, and vendors D and E are tantalum-nitride resistors. In this table, a failure was defined as any resistor that failed to meet the rated temperature coefficient of resistance specified on the manufacturer's data sheets. All resistors were tested over the temperature range of -55° C to 125° C. Obviously, some of the high failure rates are merely the reflection of manufacturers' exaggerated performance claims, and would appear as a more reliable resistor if the specification sheets reflected more realistic performance claims.

In Table 13, vendors A and B are thick-film chip resistors, vendor C is a cermet-pellet resistor, and vendor D is a tantalum-nitride resistor. For

TABLE 13. RELIABILITY DATA SUMMARY FOR RESISTORS SUBJECTED TO OPERATING LIFE TESTS AT 125° C AND RATED POWER

Vendor	Number Tested	Number Failed	Total Test Hours	Failure Rate	MTBF	Ratio Failure Rate
				Per 10^6 Hours	Hours	Percent
A	32	• 2	32 256	62	16 129	6.2
B	58	1	58 464	17	58 824	1.7
C	155	7	156 240	45	22 222	4.5
D	100	2	108 000	19	52 632	2.0

the calculations given in Table 13, a failure was defined as an open or a resistor that had a resistance change greater than ±10 percent. One of the primary factors was the rated power given by the resistor vendor. Some of the rated power values given by the manufacturers were much higher than expected and thus contributed to the high failure rates given in the table.

Transistors. The semiconductors evaluated for this report were premounted in a LID subcarrier. These LIDs are used to facilitate handling and screen testing of bare semiconductor devices. The subcarrier, or LID, is a small ceramic substrate, slightly larger than the die with metallized contact pads. Permanent wire bonds are made from the die to the base step of the carrier. Contact can be made to the terminal posts for screen testing before permanent assembly into the hybrid microcircuit. Table 14 illustrates the data taken for operating life tests at 25° C with emitter loading.

TABLE 14. RELIABILITY DATA SUMMARY FOR TRANSISTORS SUBJECTED TO OPERATING LIFE TESTS

Vendor	Number Tested	Number Failed	Total Test Hours	Failure Rate	MTBF	Ratio Failure Rate
				Per 10^6 Hours	Hours	Percent
A	215	29	55 220	5.25	1905	13.5
B	84	33	20 160	16.37	611	39.3

For this calculation, a failure was defined as any part that opened, shorted, or had an h_{FE} out of tolerance given by the manufacturer's rated specification. Each of the transistors tested was loaded to 100 milliwatts at 25° C ambient with emitter loading. A diagram of this loading circuit is shown in Figure 8.

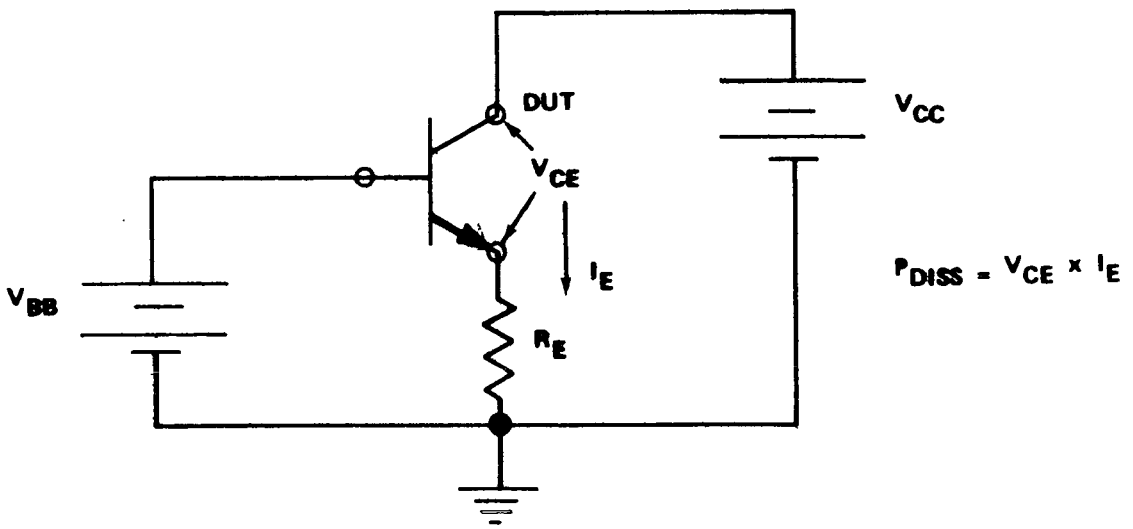

Figure 8. Circuit for Operating Life Test of LID Transistors.

The high failure rates for this device are characterized primarily by poor workmanship which the manufacturer conveniently hides with epoxy encapsulant. Wherever possible, NASA recommends the LID transistors be purchased without an epoxy encapsulant. Thus, the hybrid manufacturer can visually examine the transistor die before assembly. It is believed that this method of application will greatly enhance hybrid circuit reliability by eliminating many potential transistor failures.

Optical Examination of Failed Devices. The Hybrid Microcircuit Research Section endeavors to classify a mode of failure for each failed device. In this effort, the evaluations performed serve their greatest purpose to both the discrete chip device vendor and the hybrid manufacturer. Optical examinations can be used to identify most of the modes of failure. Typical failure modes described by optical examination are illustrated in Figures 9 and 10.

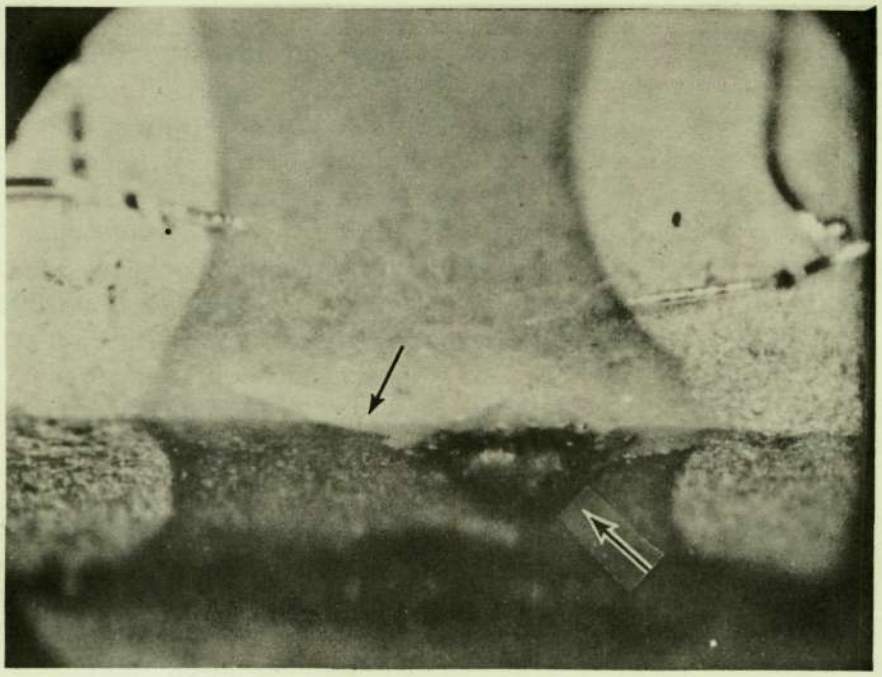

Figure 9. Fractured body of a K1200 ceramic chip capacitor.

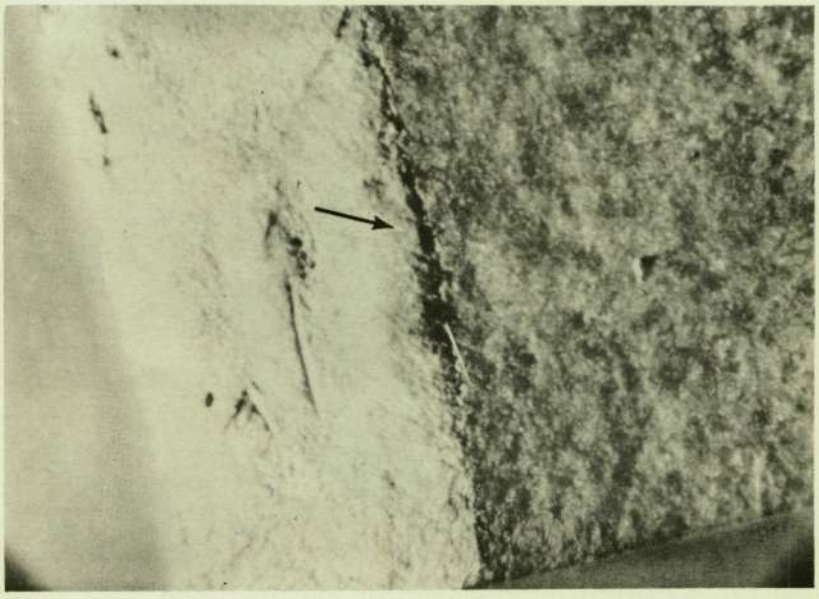

Figure 10. Delamination of capacitor termination metallization.

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Scanning Electron Microscope Examinations of Failed Devices. The scanning electron microscope (SEM) has been a principal investigative tool in the failure analysis of discrete chip devices. All types of chip devices have been investigated, including ceramic-chip capacitors, chip resistors, and semiconductors. The electron microscope is employed primarily because high magnification optics have a definite limited depth of field. The SEM employs an electron beam which is focused to a submicron sized spot on an inclined plane specimen. These include reflected electrons, secondary electrons, X-ray fluorescence, and cathode luminescence. Synchronized with the beam spot position of the substrate, these signals are put into a cathode-ray tube where they provide a high resolution image of that particular surface emission. Depth of field of the SEM permits formation of high quality images at 10 000× with excellent resolution.

The SEM examination process is characterized by mounting the specimen in thermal-setting plastic. The plastic is then lapped and polished to expose the area of failure. Once the area of failure is revealed, the specimen is placed in the SEM and SEMographs are prepared. Often large ceramic specimens require a 1 to 2 picometer (100 to 200 angstrom units) gold coating to prevent charge buildup while in the SEM. Figure 11 illustrates a specimen in the thermal-setting plastic.

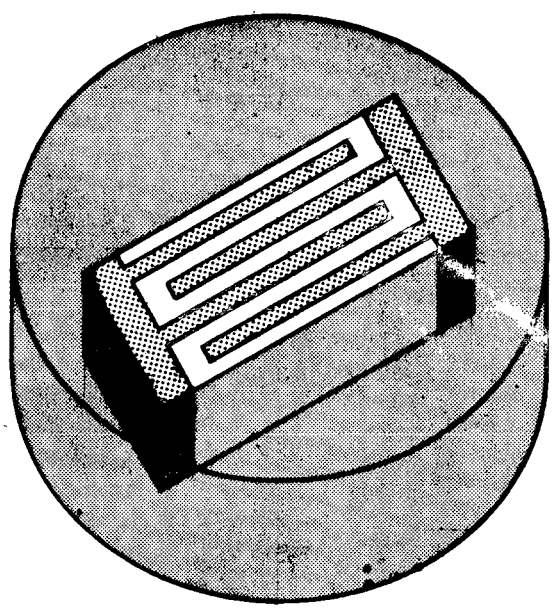

Figure 11. Ceramic-chip capacitor encapsulated in thermal-setting plastic disc.

The most significant findings using the SEM are (1) capacitor-plate structure (Figs. 12, 13, and 14); (2) peppered effect on abrasive trimmed chip resistors (Fig. 15); (3) microcracks in laser-trimmed chip resistors (Fig. 16); and (4) lifted ball bond on a chip transistor (Fig. 17). The capacitor with shorted plates, illustrated in Figures 12 and 13, had no physical external damage when observed optically at 100× and visually appeared to be in perfect operating condition. The short is caused by a porous dielectric and occurred at 168 hours of life test at 125° C.

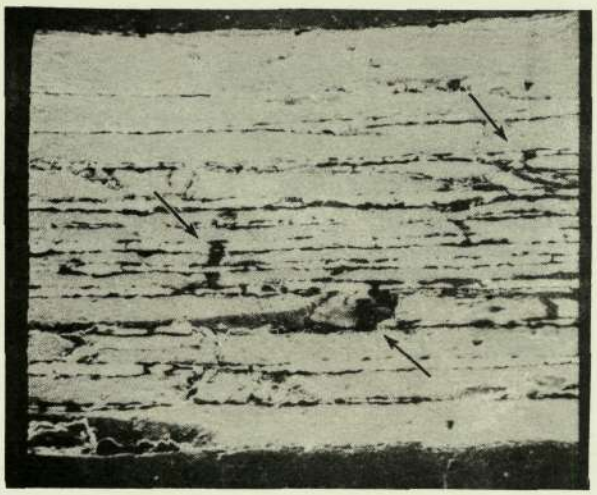

Figure 12. Ceramic-chip capacitor with many fractures in the dielectric and several shorted plates.

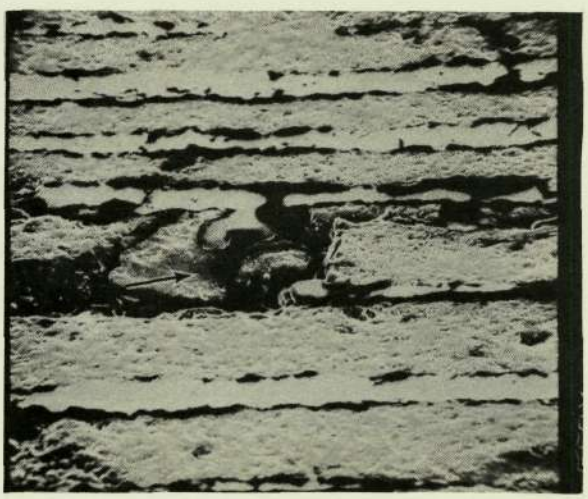

Figure 13. Expanded view of shorted plates depicted in Figure 12.

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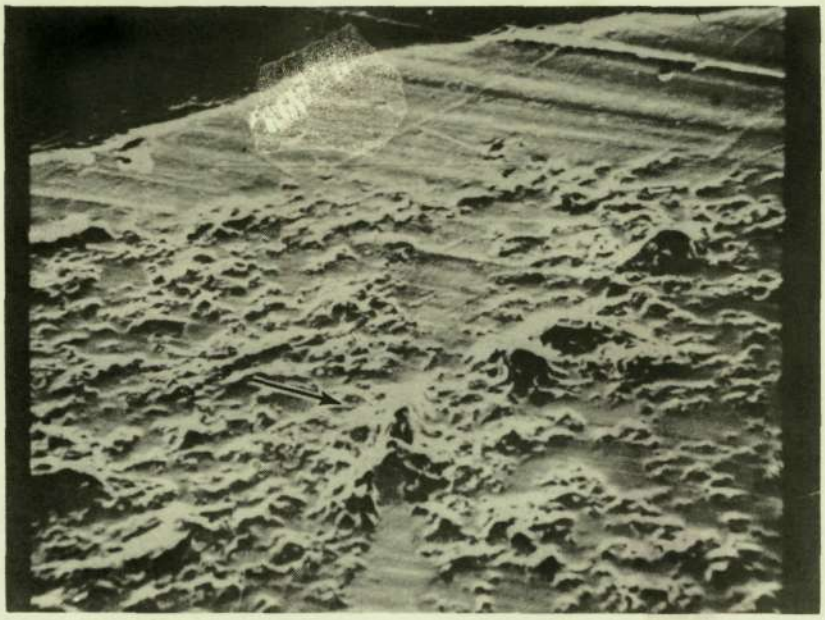

Figure 14. Ceramic-chip capacitor with plate failing to contact termination metallization.

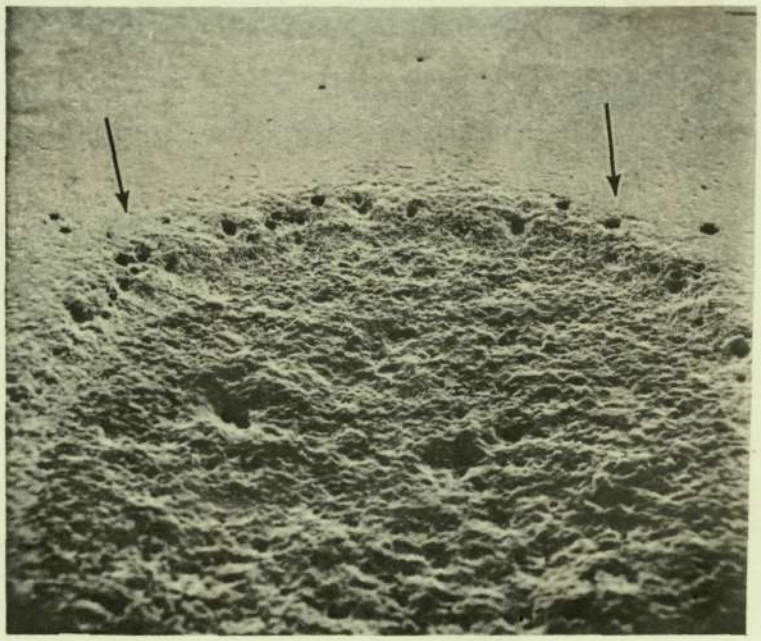

Figure 15. Peppered effect of abrasive trimmed chip resistors.

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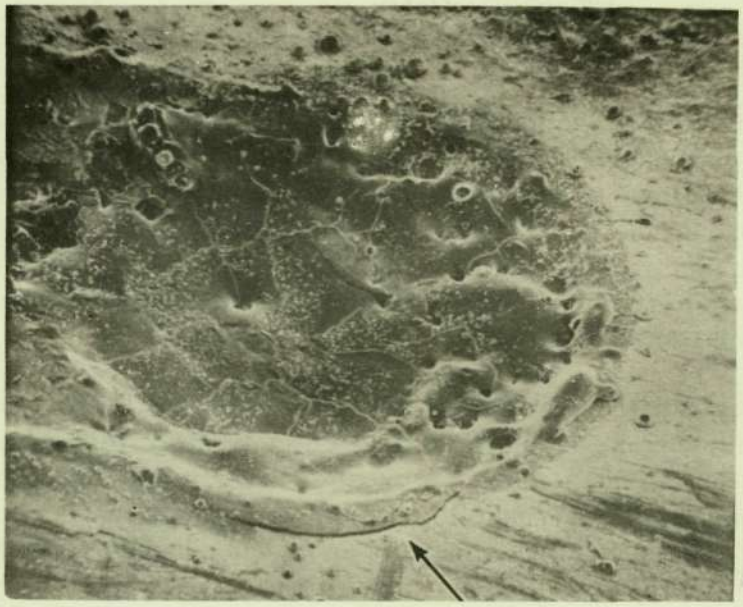

Figure 16. Microcracks in laser trimmed chip resistors.

Figure 17. Lifted bond on chip transistor.

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CONCLUSIONS

The test results clearly demonstrate that the discrete component is the most critical part in the hybrid microcircuit. Also, the data illustrate a varied difference in component vendor and type of component. To design the best quality component into the hybrid microcircuit at the most economical price, the hybrid manufacturer must have a thorough working knowledge of the application of his discrete components and he must understand their performance capability and limitations.

The data clearly illustrate that semiconductors have the highest rejection rate of all discrete components. All of the semiconductors tested were LIDs supplied with an epoxy encapsulant. A cross section of one of the failed semiconductors revealed multiple bond attempts on the LID base surface. Marshall Space Flight Center concludes that the epoxy encapsulant merely hides poor workmanship and thus believes a more reliable part can be supplied when no epoxy encapsulant is used. This affords the hybrid manufacturer the opportunity to visually inspect the die and the wire bonds. However, it must be noted that extra care in handling must be given to unencapsulated devices. Also, the unencapsulated devices do not dissipate as much power as those with the epoxy encapsulant.

Close analysis of the data verifies that all discrete components in aerospace high-reliability systems should undergo some screening and burn-in before assembly application. The screening requirements given in Tables 5, 6, 7, and 8 are recommended by MSFC. Also, MFSC recommends that all semiconductors, excluding beam-lead devices, requiring preassembly burn-in be procured mounted on some type of ceramic carrier.

A multiplexer system currently in assembly at MSFC is comprised of over 140 digital integrated circuits in the die form. These dies were ordered to the precap visual inspection of MIL-STD-883, Method 2010, Condition B. When assembled in the hybrid circuits, over 75 percent of all devices had some failures and required repair or replacement. Marshall Space Flight Center contends that procurement of these devices on a carrier would have facilitated power burn-in and greatly reduced the repair and rework required. Since repair and rework of hybrid circuits is discouraged and often not permitted by MSFC for high-reliability long term missions, it is believed that a cost savings is realized when the devices undergo preassembly power burn-in.

FUTURE PROGRAMS

The failure analysis studies presented are merely a segment of a continuous program. Future work will include evaluation of beam-lead components, microwave porcelain capacitors, and power devices. Also, new vendors will be evaluated along with reevaulation of vendors already tested.

Other programs will include improving the existing design of the burn-in test carriers, illustrated in Figure 1, and design of a burn-in test carrier for power devices. Furthermore, if the use of active chips in the die form is permitted, meaningful screening programs must be developed.

RELIABILITY OF HYBRID MICROCIRCUIT DISCRETE COMPONENTS

By Robert V. Allen and Salvadore V. Caruso

The information in this report has been reviewed for security classification. Review of any information concerning Department of Defense or Atomic Energy Commission programs has been made by the MSFC Security Classification Officer. This report, in its entirety, has been determined to be unclassified.

This document has also been reviewed and approved for technical accuracy.

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