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NASA CR-

IMPROVEMENT OF SCREENING METHODS FOR SILICON PLANAR SEMICONDUCTOR DEVICES

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FINAL TECHNICAL REPORT

By W. M. Berger

September 1972

Prepared under Contract No. NAS12-2197 by

THE PHILCO-FORD CORPORATION, WESTERN DEVELOPMENT LABORATORY DIVISION

Palo Alto, California 94303

for

THE NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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TECHNICAL MONITOR

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BBTP1	Bilayer Bipolar Test Pattern 1 - The metalization and oxide integrity test pattern evaluated in conjunction with the DCQ.
BBTP2	Bilayer Bipolar Test Pattern 2 - The bulk and surface effects test pattern evaluated in conjunction with the DCQ.
BV3A	The breakdown voltage of the large area diode structure of MOSPA.
CTI67	The Capacitor structure of BBTP1 formed by an interdigited bottom layer aluminum plate and a planar "P" diffusion separated from each other by thermal oxide.
CVI56	The Capacitor structure of BBTP1 formed by an interdigitated bottom layer and a solid top layer aluminum plate separated from each other by the vapor deposited phosphosilicate dielectric.
CTP47	The Capacitor structure of BBTP1 formed by a planar bottom layer aluminum plate separated from the planar "P" diffusion of the silicon chip by thermal oxide.
CVP34	The capacitor structure of BBTP1 formed by a planar bottom and top layer aluminum plate separated by vapor deposited phosphosilicate dielectric.
DCQ	Digital Crosspoint Quad - The bilayer metalized bipolar integrated circuit used as the functional bipolar test vehicle.
h_{FEL}	The Lateral Beta of the MOS transistor of MOSPA.
h_{FEM}	The forward Beta of the input transistor structure of BBTP2.
h_{FEMR}	The reverse Beta of the input transistor structure of BBTP2.
h_{FEO}	The forward Beta of the output transistor structure of BBTP2.
h_{FER}	The reverse Beta of the output transistor structure of BBTP2.
IR3A	The leakage current of the large area diode structure of MOSPA.
MOSPA	The MOS Test Pattern used in conjunction with the 5R100's and the P2000's for the evaluation of the bulk and surface properties of each individual wafer.
MOSPB	The MOS Test Pattern used in conjunction with the 5R100's and the P2000's for the evaluation of the metalization and oxide integrity of each individual wafer.
P2000	The Dual 50 Bit Shift Register, fabricated according the PHILCO-FORD's Regrown IIT Process, used in conjunction with the 5R100's as the MOS Integrated Circuit Functional Test Vehicle.
R_B	The resistance of the wide "p" type diffucion structure of BBTP2, or the designation of the structure.

LIST OF SYMBOLS (continued)

R_{BOND}	The resistance of the bond integrity evaluation structure of BBTP1 or the designation of the structure.
R_{BP}	The resistance of the Emitter-Base Pinch resistor structure of BBTP2, or the designation of the structure.
R_{EBPJ}	The resistance of the Epitaxial-Base Pinch resistor structure of BBTP2, or the designation of the structure.
R_{EK}	The resistance of the Epitaxial resistor structure of BBTP2, or the designation of the structure.
R_{EML}	The resistance of the n+ Emitter diffusion structure of BBTP2, or the designation of the structure.
R_{MBE}	The resistance of the 0.25 MIL wide bottom layer planar metalization strip of BBTP1, or the designation of the structure.
R_{MBPA}	Resistance of the bottom layer planar metalization stripe of BBTP1, or the designation of the structure.
R_{MBPS}	Resistance of the bottom layer planar metalization stripe of BBTP1, or the designation of the structure. This stripe has only 6 angle points as compared to the 18 angle points of R_{MBPA}.
R_{MBS}	Resistance of the BBTP1 bottom layer metalization stripe structure that crosses steps in the thermal oxide that result from etching the bottom layer metal, or the designation of the structure.
R_{MCC}	Resistance of the BBTP1 or the MOSPB structure formed by connecting in series a group of diffused resistors and bottom layer metalization stripes through thermal oxide contact cuts, or the designation of the structure.
R_{MP}	The resistance of the 0.35 MIL planar aluminum strip of MOSPB, or the designation of the structure.
R_{MS}	The resistance of the 0.35 MIL aluminum stripe, over oxide steps, of MOSPB, or the designation of the structure.
R_{MTB}	Resistance of the planar metalization stripe of BBTP1, formed by depositing top layer metalization over the bottom layer metalization after the insulating dielectric has been etched away, or the designation of the structure.
R_{MTE}	The resistance of the 0.25 MIL wide bottom layer planar metalization stripe of BBTP1, or the designation of the structure.
R_{MTP}	Resistance of the planar top layer metalization stripe of BBTP1, or the designation of the structure.

LIST OF SYMBOLS (continued)

R_{MTS}	Resistance of the BBTP1 top layer metalization stripe structure that crosses steps in the insulating dielectric that results from the underlying bottom layer metalization, or the designation of the structure.
R_{MVIA}	Resistance of the metalization path formed by connecting in series a group of bottom and top layer metalization stripes through vias in the insulating dielectric of BBTP1, or the designation of the structure.
R_{NE}	The resistance of the buried n+ diffusion structure of BBTP2, or the designation of the structure.
R_{25}	The resistance of the 0.15 MIL wide "p" type resistance structure of BBTP2, or the designation of the structure.
V_{CL}	The designation of the 100 MIL^2 gate oxide capacitor structure of MOSPB.
V_{CM}	The designation of the 10 MIL^2 gate oxide capacitor structure of MOSPB.
V_{CS}	The designation of the 1 MIL^2 gate oxide capacitor structure of MOSPB.
V_{FB1AN}	The Flat Band Voltage of the field oxide capacitor structure of MOSPA after negative voltage drift.
V_{FB1AO}	The Flat Band Voltage of the field oxide capacitor structure of MOSPA after zero bias drift.
V_{FB1AD}	The Flat Band Voltage of the field oxide capacitor structure of MOSPA after positive voltage drift.
V_{FB2AN}	The Flat Band Voltage of the gate oxide capacitor structure of MOSPA after zero bias drift.
V_{FB2AP}	The Flat Band Voltage of the gate oxide capacitor structure of MOSPA after positive voltage drift.
V_{OFBL}	Voltage of first breakdown for 100 MIL^2 capacitor structure of MOSPA.
V_{OFBM}	Voltage of first breakdown for 10 MIL^2 capacitor structure of MOSPA.
V_{OFBS}	Voltage of first breakdown for 1 MIL^2 capacitor structure of MOSPA.
V_{PT}	The punch through voltage of the lateral diffusion structure of MOSPA.
V_{6AN}	The inversion voltage of the field oxide MOS transistor of MOSPA after negative voltage drift.

LIST OF SYMBOLS (continued)

V_{6AO}	The inversion voltage of the field oxide MOS transistor of MOSPA after zero bias drift.
V_{7AN}	The inversion voltage of the Gate oxide MOS transistor of MOSPA after negative voltage drift.
V_{7AO}	The inversion voltage of the Gate oxide MOS transistor of MOSPA after zero bias drift.
5R100	The Dual 50 Bit Shift Register, fabricated according the PHILCO-FORD"S Regrown II Process, used in conjunction with the P2000's as the MOS Integrated Circuit Functional Test Vehicle.

IMPROVEMENT OF SCREENING METHODS FOR SILICON PLANAR SEMICONDUCTOR DEVICES

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SECTION I

1.1 SUMMARY

Silicon planar semiconductor devices occasionally fail during systems applications because of highly time dependent failure mechanisms that are not effectively removed by current high reliability screening techniques. These relatively infrequent failures, however, can jeopardize the successful completion of a mission, and result in the waste of large quantities of time and capital. The waste of time and capital is particularly annoying if the devices are utilized in space systems where maintenance is impossible and the failure of a device causes the malfunction of a space probe that cannot be repeated for a considerable length of time.

These highly time dependent failure mechanisms are generally recognized by the semiconductor industry, but they are usually quite difficult to accelerate and therefore, may not be detected and removed during the stringent screening to which high reliability devices are subjected throughout the manufacturing process. The objective of this program was the development of a more sensitive method of selecting silicon planar semiconductor devices for long life applications. The methods developed are applicable to integrated circuits at the highest level of integration as well as to discrete diodes and transistors. The methods developed also hold promise of economic as

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well as technical feasibility, and should aid the manufacturer of the devices in the improvement of his processing techniques so that both increased reliability and yields are achieved.

There are two basic manufacturing technologies for silicon planar semiconductor devices. These technologies are the MOS and the Bipolar approaches. Although there is some similarity in both approaches, the bonding and the encapsulation techniques for example, the predominant highly time dependent failure mechanisms for MOS and bipolar technologies are different. The reasons for the differences in the failure mechanisms are primarily due to the differences in the electrical characteristics and the physics of operation between MOS and bipolar devices.

The approach pursued therefore, was to utilize both MOS and bipolar test pattern vehicles, fabricated on the same wafers as MOS and bipolar functional devices to determine more sensitive screening methods for the detection of the highly time dependent failure mechanisms peculiar to each construction technique as well as the failure mechanisms common to both construction techniques.

The efforts on this program were broken into four phases for MOS vehicles and four phases for bipolar vehicles. The different phases are as summarized below:

Phase 1 Study and Evaluation of Effective Screening Procedures.

Phase 2 Generation of Test Method (Item 1 of Contract) based on the Phase 1 study and evaluation.

Phase 3 Generation of a detailed Evaluation Plan (Item 2 of Contract) and execution of detailed evaluation plan (Item 3 of Contract).

Phase 4 Review of the results obtained during the execution of the testing done in Phase 3 and the optimization of the screening method based on data obtained during the Phase 3 testing (Item 4 of Contract).

The test data taken during the course of this contract demonstrates that sensitive test pattern chips interdispersed on the same wafers as functional MOS or bipolar integrated circuits can be utilized to detect and screen in a relatively short period of time highly time dependent failure mechanisms which would ultimately cause the failure of the functional devices. The data also shows that failure mechanisms are not necessarially the same for all wafers from a given diffusion lot and that ultra high reliability selections must be based on a wafer by wafer evaluation.

During the work performed under this contract both visual and electrical correlations were observed between the measurements made on the functional and the test pattern structures that could be economically applied as standard screening techniques to enhance the reliability of the final functional product. Specifically the correlations between the measurements and the reliability of the DCQ device were:

a. The DCQ devices from the wafers with high functional test die sort yields performed more reliably during the environmental screening, burn-in testing and 2,000 hour life testing than the devices from low functional die sort yields.

b. The DCQ wafers with high functional test yields exhibited higher pre-seal visual yields for the good functional DCQ devices than did the wafers with low functional test yields.

c. The electrical test pattern data taken on wafers at electrical die sort correlated very well with the measurements made on the test patterns after encapsulation.

d. DCQ devices from wafers with low test pattern failure percentages at electrical wafer mapping performed more reliably through the screening, burn-in and 2,000 hour operating life test than DCQ devices from wafers with high test pattern failure percentages.

e. DCQ devices from wafers where the measurements on the test patterns indicated the thickness ratio (Bottom layer metal/vapox dielectric) was unity or greater performed in general more reliably than DCQ wafers where this ratio was less than unity. In the cases where this thickness ratio-reliability relationship did not hold, capacitor shorting tests performed on the BBTP1 vehicles indicated difficulties with the vapox dielectric integrity and BBTP2 data indicated difficulties with the bulk parameters.

f. Worst case determinations of the DCQ device parameters I_{OL}, V_{OH} and I_{SC} based on the characteristics of the individual structures of the DCQ cell as determined by measurement of the test structures of BBTP2 showed a good correlation between the calculated DCQ parameter values and the percentage of failures experienced by the DCQ devices on a wafer by wafer basis.

g. An abnormally high or low total V_{CC} leakage current for the DCQ devices correlated quite well with subsequent failure of the device.

The correlations observed between the measurement of the MOS test vehicles and the reliability of the MOS functional devices were:

a. The flat band voltage (FB1AN) and the threshold voltage (V6AN) determined with the use of the structures of MOSPA after negative voltage charge drifting at 300°C showed good correlation with the reliability of both the MOS 5R100 and P2000 functional devices.

b. Abnormally high MCF values were indications of functional device failure.

c. A high stress functional burn-in to stress the internal nodes of the MOS device was beneficial in reducing the percentage of failure of these devices during the operating life test.

Other correlations were observed such as the time to failure of metalization stripes was function of the cross sectional area of the stripe and the

measured resistance of the stripe, but these correlations had no relationship to the failure mechanisms of the MOS functional test vehicles. The fact that correlations such as indicated above were not useful in assessing the reliability of the functional devices used on this program does not negate the potential effectiveness of these types of structures on device designs where current densities are high or metalization cross sections are reduced at oxide steps because of inadequate processing. The test pattern data taken during this contract indicates that oxide steps do cause increased resistance in metalization stripes, but because of the low current densities imposed on the devices used in this contract no electromigration difficulties were experienced.

Evaluation of MDS chips from the inner portion of the wafers as opposed to MSD chips from the periphery of the wafers did not indicate any appreciable differences in reliability. Differences in reliability between the 5R100 devices and the P2000 devices; however, were observed. Both device types perform the same electrical functions, but differences in the manufacturing process exist (the gate metal of the 5R100 device is terminated over this gate oxide, whereas the gate metal of the P2000 device is terminated over thick oxide, and a two terminal input protection device is used on the 5R100 device as opposed to a three terminal input protection device on the P2000 devices). The improved reliability of the P2000 devices over the 5R100 devices is attributed to the construction of the gates and the improved input protection rather than diffusion and metalization processes, and this infers similar comparisons can be made with other MOS processes.

Poor correlation was observed between the stringency of the per-seal visual inspection of the MOS devices and the reliability of these devices, but this is attributed to the fact that the failure mechanisms that can be screened by a visual inspection were not present in the test vehicles utilized.

In general, the correlations observed during this portion (Phase 3) of the contract were consistent with the correlations observed during the Phase 1 portion of the evaluation. These studies were reported in detail in the

Interim Scientific Reports on the Phase 1 Bilayer Bipolar Evaluation and the Phase 1 MOS Evaluation.

The data collected during the Phase 1 Bilayer-Bipolar evaluation showed good correlation between:

a. The top-to-bottom layer metalization shorts experienced by the DCQ throughout the testing sequence and the percentage of vapor deposited oxide shorts observed on the test pattern capacitor structures.

b. The top-to-bottom layer metalization shorts experienced by the DCQ devices and the metalization and vapor deposited dielectric thicknesses measured on each wafer prior to wafer scribing.

c. The top-to-bottom layer metalization on shorts experienced by the DCQ device and exposure to thermal cycling stresses.

d. The stability of the electrical characteristics of the actual test structures of BBTP2 and the parametric stability of the DCQ device.

e. The detection of electrical failures with total V_{CC} current electrical screens applied subsequent to the 100% in-process screens and parametric failures detected at a subsequent D.C. test.

f. The stringency of the pre-seal visual inspection criteria and the quantity of failures incurred during subsequent electrical testing.

g. Test pattern transistor and resistor parameter mean values to the electrical yield of the DCQ devices.

The data collected during the Phase 1 MOS evaluation showed good correlation between:

a. 5R100 failures and the flat band voltage measured on test patterns.

b. 5R100 shorts during input stress testing and the average breakdown of the test pattern capacitor test structures.

c. The order in which electromigration failures occurred during the test pattern evaluation with the mean value of metal stripe resistance.

d. The higher percentage of 5R100 failures incurred from the Class "B" visual inspection group as compared to the Class "A" visual inspection group.

Based on the data obtained during the course of this contract, the utility of the test pattern approach to improved reliability has been demonstrated, the the approach will be particulary effective for small quantity procurements where the reliability inherent with high volume continious production of a high reliability product is not available, and for the procurement of LSI devices where elaborate evaluation of the finished LSI product is neither technically or economically feasible. The test pattern approach should improve both reliability and yield because it affords immediate feedback on deficiencies in a manufacturing process and enables rapid correction of these defects. The extent to which reliability and processing yields are improved will bear economic benefits not only to the user of the devices in term of the less maintenance and improved performance of the systems in which the devices are used but also to the manufacturer in terms of reduced material, testing, and labor costs.

SECTION II

INTRODUCTION

2.1 SCOPE OF REPORT

This report describes the results obtained during the Phase 3 evaluations performed according to the MOS and Bilayer Evaluation Plans which were generated based on the results of the Phase 1 Evaluations and previously submitted as part of the requirements of this contract. The report also defines the screening procedure developed as a result of the tests and evaluations performed on the functional and test pattern vehicles evaluated during both the Phase 1 and Phase 3 testing portions of this contract. The screening procedure details the electrical, thermal and mechanical tests and the rejection criteria that is to be applied to insure the procurement of reliable devices for long term aerospace applications.

2.2 PROGRAM OBJECTIVES

The purpose of the program was the development of a more sensitive method of selecting silicon planar semiconductor devices for long life applications. The methods developed are generally applicable to all types of semiconductor components. The program effort, however, was premarily concerned with the screening of highly time dependent failure mechanisms which are difficult to accelerate to a degree that renders them detectable in a reasonable period of time. The objective of the work was to improve the effectiveness of acceleration methods and/or the sensitivity of detection techniques for failure mechanisms that have been shown capable of escaping the best current practical screens, and ultimately contribute in a significant way, to system failure.

2.3 PROGRAM APPROACH

Our approach to attaining the objectives of the program was:

a. The development and evaluation of preseal visual and preseal electrical test procedures, supplementing normal in-process screens, which effectively screen failure mechanisms associated primarily with the semiconductor die.

b. The development and evaluation of feasible post seal electrical, mechanical, and thermal test methods which effectively screen failure mechanisms associated with packaging, thermal stress and packaged device ambient.

c. The development of sensitive test pattern structures and the correlation of short term test data from the test structures with long-term-difficult-to-accelerate failure mechanisms of functional devices. This established a set of practical short term acceptance criteria, based on measurements of test structures fabricated on the same wafer as the functional devices, to aid in the determination of the long term reliability of the functional devices.

The utilization of sensitive test patterns permits the acceleration of potential failure mechanisms which would be difficult or impossible to accomplish on complex functional devices within a reasonable period of time. This is because the metalization interconnections prevent the application of sufficiently large stresses to internal circuit nodes to accelerate degradation that can occur during long term applications of in-use stresses. Secondly utilization of a standard test pattern will monitor the basic failure mechanisms of any process and identify potential failure mechanisms regardless of device complexity. However, since test patterns occupy only a finite area on any wafer, they will determine potential failure mechanisms that are common to an entire wafer or lot, but will not detect localized defects that occur in an area that does not contain the test pattern. Therefore, to insure long term reliability, the test pattern screens developed as a result of this program are used to supplement the 100% pre- and post-seal visual, electrical, and thermal screens also developed during the course of this contract.

Based on the results of the testing performed during the Phase 1 and Phase 3 evaluations of both functional devices and test pattern structures, it was determined that the test pattern structures could be utilized as both a tool for the evaluation of highly time dependent, difficult to accelerate failure mechanisms, and as an evaluation vehicle from which realistic and practical wafer rejection criteria could be obtained.

The design of the test pattern structures was based on our experience in the ut utilization of test patterns during in-house evaluations and contract testing, combined with our experience in reliability evaluation and physics of failure determination made on integrated microcircuits.

The evaluation vehicles used during the course of this contract were the:

a. SP0199A, Digital Crosspoint Quad (DCQ) a bilayer metalized-bipolar intigrated circuit of intermediate complexity.

b. 5R100, MOS Dual 50 Bit Shift Register fabricated according to PHILCO-FORD RII Process.

c. P2000 MOS Dual 50 Bit Shift Register fabricated according to the PHILCO-FORD RIIT Process.

d. BBTP1, a test pattern designed for the evaluation of the metalization and oxide integrity of bilayer metalized devices.

e. BBTP2, a test pattern designed for the evaluation of bipolar bulk and surface effects.

f. MOSPA, a test pattern designed for the evaluation of bulk and surface phenomena primarily associated with MOS devices. Two versions of this test structure were used, one for the MOS RII process and one for the MOS RIIT process.

g. MOSPB, a test pattern designed for the evaluation of metalization and oxide integrity of MOS devices. An RII and an RIIT version of this pattern were used.

The devices evaluated during this contract were obtained from wafers fabricated according to standard production procedures. Each wafer fabricated contained both functional microcircuits and test patterns interdispersed within the normal grid spacing of the wafer. The functional microcircuit and test patterns combinations, fabricated on single wafers, and used during the course of this contract were:

a. DCQ, BBTP1 and BBTP2 Vehicles

b. 5R100, MOSPA (RII) and MOSPB (RII) Vehicles

c. P2000, MOSPA (RIIT) and MOSPB (RIIT) Vehicles.

Photomicrographs, circuit drawings, and descriptions of the individual test vehicles are contained in the Interim Scientific Reports and Evaluation Plans previously submitted as part of this contract.

2.4 EVALUATION EMPHASIS

During the Phase 1 and Phase 3 evaluations, primary consideration was given to the development of screening techniques that can be utilized to identify and subsequently remove semiconductor devices with highly time dependent, but difficult to accelerate failure mechanisms. The mechanisms that were given particular attention during the contract were:

a. Electromigration of metalization patterns

b. Inversion or channeling

c. Contact cut resistance, including via resistance in the bilayer metalized test vehicles.

d. Aluminum - SiO_2 interactions

e. Surface effects

f. Oxide Shorts

g. Surface contamination

h. Chip-to-header bonds

i. Wire bonds.

Many of the chemical and physical causes for device degradation and/or failure are introduced during the wafer processing operations and are of a nature that affects every device on the wafer.

During this program, we investigated the feasibility of incorporating a wafer screen to identify and remove wafers with inherent potential reliability hazards. We therefore, conducted sufficient testing and evaluation of the wafer screens to insure that the final screen rejects only wafers which contain devices which, in general, are not reliable.

The wafer screen evaluation consisted of microscopic examinations and electrical measurements made at the wafer level, and subsequent testing of both packaged test patterns and functional devices from the screened wafer to establish the relationship between the process induced potential failure mechanisms and actual failures incurred during testing.

The microscopic examination techniques for the screening of wafers that were evaluated included:

a. The measurement of metalization and resistor line widths to determine the deviation from the designed width.

b. The determination of the variation of alignment of the diffusion and metalization patterns.

c. The determination of the extent of overetching that occurs during the diffusion and metalization photolithographic operations, by comparing actual cut sizes to designed cut values, actual line widths to designed line widths and by observing metalization neck down at oxide steps.

In addition to the above microscopic observations, Talley Surf and interferometer measurements of the thicknesses of both metalization and oxide layers were made on each wafer.

The electrical wafer screening measurements made on the bilayer-bipolar test patterns included:

a. Resistance determinations on top and bottom layer aluminum stripes, some of these stripes were planar, others crossed oxide steps, and others contained vias between top and bottom metalization layers.

b. Resistance determinations on a series string consisting of diffused resistors interconnected by aluminum metalization.

c. Oxide breakdown determinations for both planar and interdigitated large area capacitors. The oxides evaluated were the thermal oxides and the vapor deposited oxides.

d. Resistance measurements of special diffused components incorporated into the test patterns for the evaluation of epitaxial resistivity, base and emitter sheet rho, and buried n+layer sheet rho.

e. Resistance measurements of pinch resistors for the evaluation of base widths, and base substrate spacings.

f. Reverse breakdown and reverse leakage of special collector-base diode structures, including a large area diode structure.

g. Resistance measurements on a 0.15 mil wide "p" type diffused resistor, the same dimensions used in the functional vehicles.

h. Beta, V_{SAT} , & I_{CEO} measurements on a NPN transistor of the same geometry as used for the output device in the functional circuit.

i. Beta, I_{CEO}, and Emitter to Emitter transverse beta measurements on a multiple emitter NPN transistor of the same geometry used for the input device in the functional circuit.

j. Isolation leakage current at three different reverse voltages.

k. V_{GST} measurements on a special "p" channel, enhancement mode, MOS transistor.

The DCQ devices from each wafer were subjected to an electrical die sort consisting of a functional test and the measurement of specified DC parameters.

The electrical wafer screening measurements made on the MOS test patterns included:

a. Flat band voltage determinations on large area MOS capacitors.

b. The measurement of reverse leakage current and reverse diode breakdown of a large area p-n junction diode.

c. The measurement of punch through on a specially designed test pattern to determine the extent of lateral diffusion.

d. The measurement of surface recombinations velocity with the use of a gate controlled p-n junction diode.

e. The determination of lateral h_{FE}.

f. The measurement of field inversion voltage on both thick and thin gate oxide MOS transistors.

g. The measurement of the resistance of aluminum stripes and p type diffusions.

h. The determination of oxide breakdown voltage on MOS capacitor structures.

The functional 5R100 and P2000 devices from each wafer were subjected to an electrical die sort consisting of a functional test and the measurement of the specified D.C. parameters.

2.5 PRESEAL VISUAL INSPECTION AND POST SEAL TESTING

A preseal visual inspection was performed after all processing operations except sealing were completed according to the requirements of the specification generated for use and evaluation during this program. The detailed

specification used is contained in Appendix "A" of this report.

The functional devices were segregated into Class "A", Class "B" and Class "R" visual categories according to the requirements of the preseal visual specification. Both functional devices and the test patterns were sealed, and were subjected to additional screening and testing as indicated in detail in the MOS and Bilayer Bipolar Evaluation Plans and Interim Scientific Reports.

2.6 EFFECTIVENESS OF CORRELATION OF TEST PATTERN DATA WITH LONG TERM FUNCTIONAL DEVICE FAILURE MODES

During both the Phase 1 and the Phase 3 testing, the evaluation of the short term data obtained from the test patterns was able to predict potential long term reliability hazzards that existed in the functional devices on a wafer by wafer basis. The good wafer by wafer correlation of test pattern data with functional device failures was utilized to develop wafer rejection criteria for functional devices based on both wafer mapping and post encapsulation measurements of the individual test structures. The wafer rejection criteria for bilayer-bipolar devices, based on test structure measurements is contained in Section IV. The criteria for functional MOS devices is contained in Section VI.

2.7 CORRELATION OF FUNCTIONAL DEVICE FAILURE WITH PRESEAL VISUAL INSPECTION

For the DCQ devices, correlation of the preseal visual inspection data with the subsequent failure of these device indicated:

a. DCQ devices from high visual yield wafers performed more reliability throughout the entire Phase 3 evaluation program than DCQ devices from low visual yield wafers.

b. The Class "A" and Class "B" visual devices performed more reliably than devices which did not meet the Class "A" or "B" visual criteria. The devices which did not meet the Class "A" or "B" criteria were designated Class "R" devices.

For the P2000 and the 5R100 devices there was no significant difference in reliability as a function of the preseal visual category into which the devices had been placed. The reason for the good correlation between the DCQ visual category and reliability, and the lack of correlation between the 5R100 and P2000 visual category and reliability is attributed to the fact that the failure mechanisms associated with MOS failures are related to charge densities in the oxide layer which is not a visual phenomena, but the mechanisms associated with DCQ failures are related to metalization and oxide integrity which is microscopically visible.

2.8 EFFECTIVENESS OF SCREENING PROCEDURE

The effectiveness of the screening procedure developed as a result of this program is quite high. Based on the data taken during the DCQ wafer inspection, all of the wafers that experienced high failure rates through the evaluation program could have been screened if the developed wafer rejection criteria has been applied. Based on the data taken for the 5R100 and P2000 devices during the test pattern evaluation, and on the results of the 340 hour burn-in the MOS devices which exhibited high failure rates during the 2,000 hour stress life test would also have been removed as high reliability risk devices.

SECTION III

BIPOLAR TEST RESULTS AND ANALYSIS

3.1 GENERAL

The arrangement of the factual data in this section is:

a. A summary of all of the Bilayer-Bipolar test vehicle data collected during the Phase 3 evaluation performed in accordance with Test Flow Diagrams of Figures 3.1, 3.2 and 3.3 and according to the requirements of the Evaluation Plan, Bilayer-Bipolar Vehicles, generated under the work on this contract and submitted in its final form during September 1971.

b. The correlation of the BBTP1 and BBTP2 test data obtained during the Phase 3 evaluations with the data obtained from the DCQ functional test vehicles.

Where required, explanations are given in the text to clarify the data summaries, or the interpretations of the significance of the data.

Throughout the entire bipolar test program, control devices were measured prior to the measurement of any of the test devices. The data obtained from the control devices is not specifically mentioned in the text, but maximum variation in the parameters of the controls throughout the program was less than 3 percent indicating that the measurement of the test vehicles was properly performed. Throughout the text of this report references to Class "A" or Class "B" visual devices means that the devices have been inspected and meet the visual criterial contained in Appendix A, reference to Class "R" visual devices means these devices marginally failed the lower (Class "B") visual inspection criterial of Appendix A.

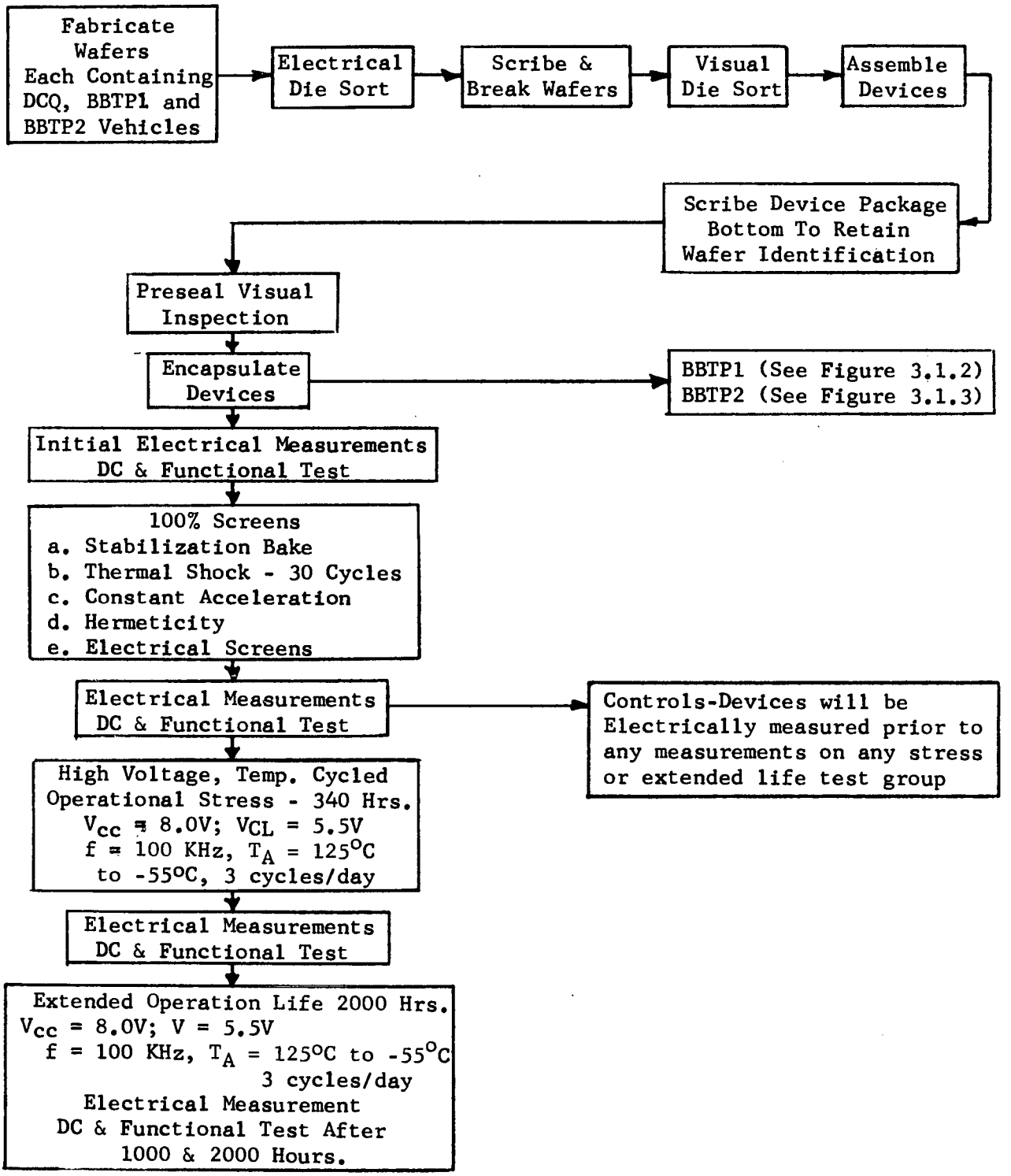
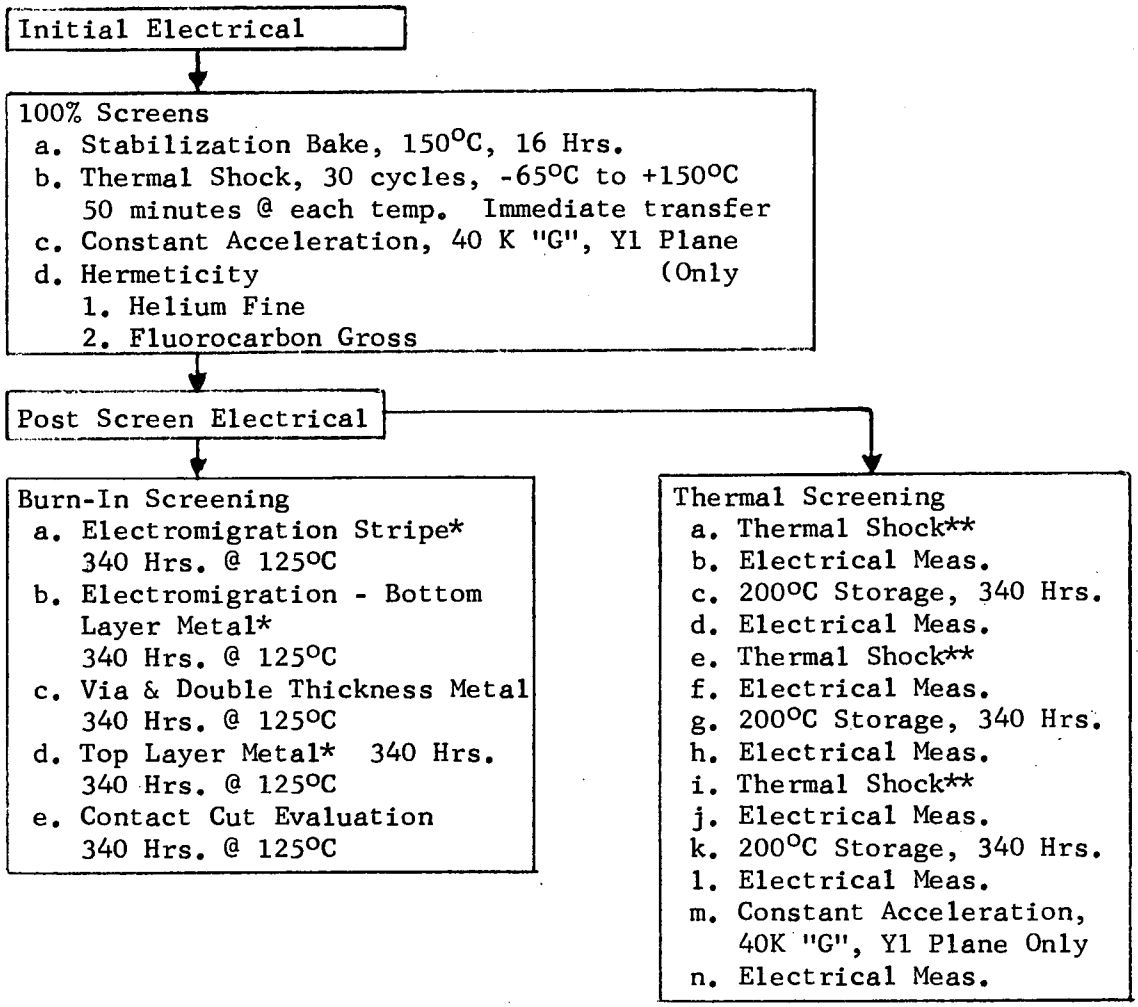


FIGURE 3.1 - EVALUATION PLAN FLOW DIAGRAM FOR BILAYER-BIPOLAR DCQ VEHICLES



* - Life rack shall be monitored with a recorder, the time of each life rack failure shall be recorded.

** - Thermal Shock, 10 cycles, -65°C to +150°C, 15 minutes at each temperature extreme, immediate transfer.

FIGURE 3.2 - EVALUATION PLAN FLOW DIAGRAM FOR BBTP1, METALLIZATION AND OXIDE TEST STRUCTURES.

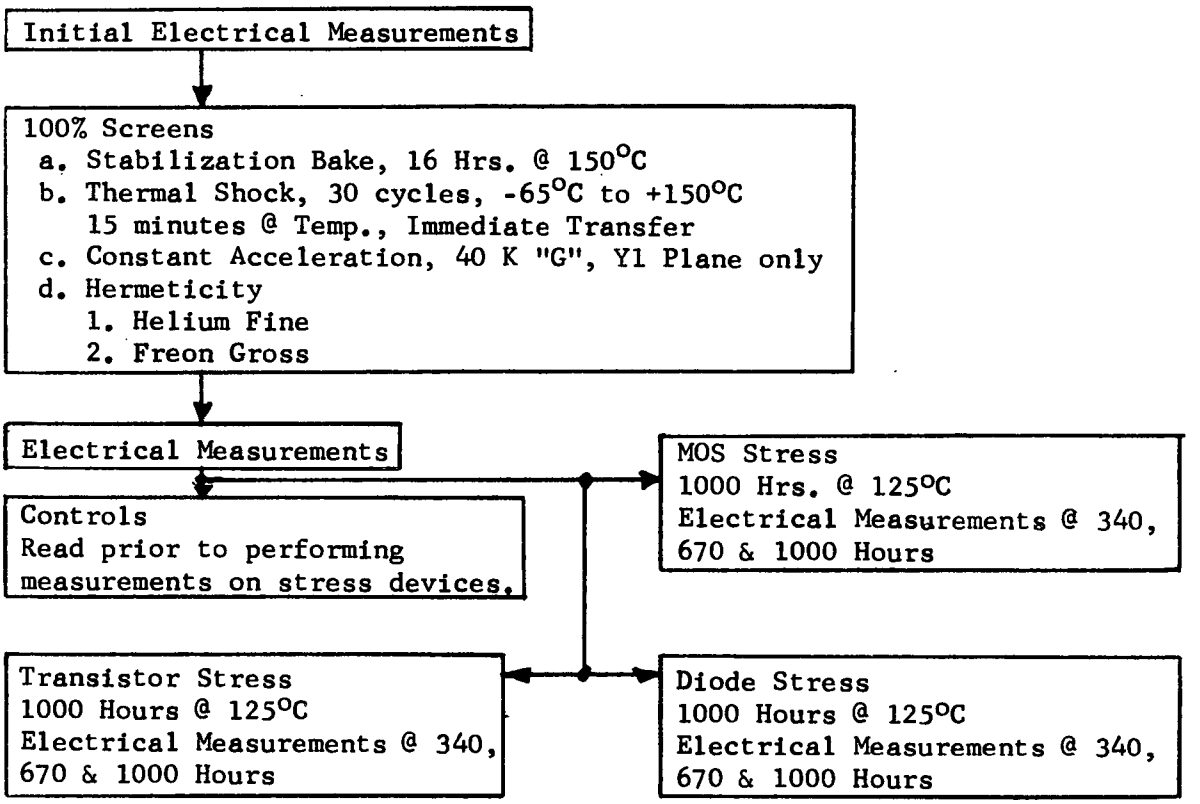


FIGURE 3.3 - TEST FLOW DIAGRAM FOR BBTP2

3.2 BILAYER BIPOLAR TEST VEHICLE DATA SUMMARY

The material contained in the following subsections summarizes, on a wafer by wafer basis, the results of the preseal visual inspection, and failures incurred during the Phase 3 evaluation of the DCQ, BBTP1, and the BBTP2 test vehicles. The results of the failure analysis performed on the test vehicles is also summarized. The correlation of the test pattern data with the functional device data is presented in Subsection 3.3.

3.2.1 DCQ Evaluation Data Summary

Table 3.1 summarizes the quantity of devices from each wafer that were placed into the different visual categories according to the preseal visual inspection criteria contained in Appendix "A". This table also summarizes the total functional yield of the DCQ devices, on a wafer by wafer basis, at the electrical die sort measurements, and the initial 25°C functional and D.C. test yield subsequent to bonding and encapsulation.

Table 3.2 summarizes the quantity of DCQ failures incurred through the entire evaluation program by wafer and visual category. The failure criteria is defined in the final draft of the Evaluation Plan for Bilayer Bipolar Devices submitted during September 1971; any device that did not meet the minimum and/or maximum values established for the D.C. measurements or the screening measurements, or which did not meet the GO/NO-GO functional test requirements, or which failed the hermeticity requirements was considered a failure. Additionally any device which became non functional during the burn-in or life test was also considered a failure.

A physics of failure determination was performed on all devices which failed during the evaluation sequence. The analysis included the opening and microprobing of all devices where meaningfull information could be obtained. The results of this portion of the evaluation are summarized in Table 3.3.

LOT/WAFER	LOT/WAFER CODE	DIE SORT-FUNCTIONAL TEST YIELD - %	ASSEMBLED	TOTAL CLASS "A" VISUAL	TOTAL CLASS "B" VISUAL	TOTAL CLASS "R" VISUAL	FINAL TEST YIELD % CLASS "A" DEVICES	FINAL TEST YIELD % CLASS "B" DEVICES	FINAL TEST YIELD % CLASS "R" DEVICES
33/15	A	16.0	36	12	14	10	83	100	0
35/9	I	11.0	9	2	5	2	50	80	50
35/12	H	14.5	10	1	3	6	0	100	83
38/3	E	3.7	16	5	5	6	50	20	17
38/7	F	5.5	24	2	16	6	60	25	17
38/8	G	7.5	32	10	13	9	40	31	22
39/12	J	11.9	39	7	24	8	86	58	38
39/13	B,C	11.0	43	3	24	14	67	77	57
39/14	D	3.5	16	2	7	7	0	29	0

TABLE 3.1

FUNCTIONAL DIE SORT YIELD, PRESEAL INSPECTION RESULTS
& POST SEAL 25°C FUNCTIONAL AND D.C. TEST YIELDS BY WAFER

LOT/WAFER	VISUAL CLASS	SAMPLE	INITIAL MEASUREMENTS	100% PHYSICAL SCREENS	ELECTRICAL SCREENS	HERMETICITY	POST SCREEN ELECT.	DURING BURN-IN	POST BURN-IN ELECT.	DURING LIFE TEST 1 - 1,000 HOURS	POST 1,000 HOUR LIFE	DURING LIFE TEST 1,000-2,000 HOURS	POST 2,000 HOUR LIFE	TOTAL
33/15	A	12	2	0	0	0	0	0	0	0	1	0	0	3
35/9	A	2	1	0	0	0	0	0	1	0	0	0	0	2
35/12	A	1	1	-	-	-	-	-	-	-	-	-	-	1
38/3	A	5	2	0	0	0	1	0	1	1	0	0	0	5
38/7	A	2	1	0	1	0	0	0	1*	-	-	-	-	3
38/8	A	10	6	0	0	0	1	0	0	0	1	0	0	8
39/12	A	7	1	0	1	0	1*	0	1	1	0	0	0	5
39/13A	A	1	0	0	0	0	0	0	0	0	0	0	0	0
39/13B	A	2	1	0	0	0	0	0	0	0	0	0	0	1
39/14	A	2	2	-	-	-	-	-	-	-	-	-	-	2
TOTAL	A	44	17	0	2	0	3	0	4	2	2	0	0	30
33/15	B	14	0	0	0	2	0	0	0	0	0	0	0	2
35/9	B	5	1	0	0	0	2	0	0	0	0	0	1	4
35/12	B	3	0	0	0	0	1	0	0	0	1	0	0	2
38/3	B	5	4	0	1	0	1*	0	0	0	0	0	0	6
38/7	B	16	12	0	1	0	0	0	0	0	0	0	1	14
38/8	B	13	9	0	0	0	0	0	0	0	0	0	0	9
39/12	B	24	10	0	2	0	2	0	0	0	0	0	1	15
39/13A	B	18	6	0	0	3	0	0	1	0	0	0	1	11
39/13B	B	8	0	0	1	1	0	0	0	0	0	0	0	2
39/14	B	7	5	0	0	0	0	0	0	0	1	0	0	6
TOTAL	B	113	47	0	5	6	6	0	1	0	2	0	4	71
33/15	R	10	10	-	-	-	-	-	-	-	-	-	-	10
35/9	R	2	1	0	1	0	1*	-	-	-	-	-	-	3
35/12	R	6	1	0	2	0	2*+2	0	1	0	0	0	0	8
38/3	R	6	5	0	0	0	0	0	0	0	0	0	0	5
38/7	R	6	5	0	0	0	0	0	0	0	0	0	0	5
38/8	R	9	7	0	0	0	0	0	0	0	0	0	0	7
39/12	R	8	5	0	0	0	0	0	1	0	0	0	0	6
39/13A	R	9	5	0	0	0	0	0	0	0	0	0	0	5
39/13B	R	5	1	0	0	0	0	0	0	0	0	0	0	1
39/14	R	7	7	-	-	-	-	-	-	-	-	-	-	7
TOTAL	R	68	47	0	3	0	3*+2	0	2	0	0	0	0	57

* Device previously failed electrical screening measurements.

TABLE 3.2

DCQ FAILURES THROUGH EVALUATION TEST SEQUENCE

WAFER	CLASS	S/N	POINT OF FAILURE DETECTION	FAILURE MODE	FAILURE MECHANISM
33/15	A	A3	Post 1,000 Hr. Life	High I_F, I_R & V_{OL}, Low V_{OH}	
35/9	A	I5	Post Burn-In	High I_{CCO}, V_{OL} - All Temp.	
38/3	A	E6	Post Burn-In	High I_F, I_R, V_{OL}, I_{CER}, High V_{OH}, All Temp.	
	A	E7	Post Screening	Marginal I_{SC} - High Temp.	
	A	E9	During Life Test	Open Device During L.T.	Poor Emitter Contact
38/7	A	F24	Elec. Screen, Post B.I.	High I_F, I_R, V_{OL}, Low V_{OH} All Temp.	Poor Emitter Contact, Poor Via Contact.
38/8	A	G25	Post Screening	High I_{CEX}, I_{CER} - All Temp.	Undetermined
	A	G3	Post 1,000 Hour	High I_{CEX}, I_{CER} - All Temp.	Undetermined
39/12	A	J32	Elec. Screen, Post Screen	High I_{CEX} - All Temp.	Undetermined
	A	J3	Post B.I.	High I_{CCO}- All Temp, High V_{OL}, Room Temp.	
	A	J6	During Life Test	Shorted Input.	
35/9	B	I1	Post Screening	Unstable V_{OL} - Low Temp.	V_{OLS} Recovered, Possible Contact Problem.
	B	I6	Post Screening	High V_{OL} - Low Temp.	Low Beta, 1st Temp. Test
35/12	B	H9	Post Screening	High V_{OL} - Low & High Temp.	
	B	H5	Post 1,000	High I_F, I_R, V_{OL}, I_{CCO} - All Temp.	
38/3	B	E3	Elec. Screen, Post Screen	High V_{OL}, I_{CEX}, Low V_{OH} - All Temp.	
39/12	B	J21	Elec. Screen	High I_{CV5}, I_{CV8}	Do Not Fail Functional or DC
	B	J36	Elec. Screen	High I_{LVCL}	Do Not Fail Functional or DC
	B	J2	Post Screen	Catastrophic	Chip Lifted From Header
	B	J17	Post Screen	Catastrophic	Chip Lifted From Header

TABLE 3.3

FAILURE ANALYSIS SUMMARY - DCQ DEVICES

WAFER	CLASS	S/N	POINT OF FAILURE DETECTION	FAILURE MODE	FAILURE MECHANISM
39/13A	B	B9	Post B.I.	High V_{OL}, HIGH I_{CCO} - All Temp.	
39/13B	B	C6	Elec. Screens	High I_{LVCL} - Room Temp.	No Standard Parameter Failures
39/14	B	D10	Post 1,000 Hour Life	High V_{OL}, High I_{CEX} - 70°C only.	
35/9	R	I8	Elec. Screen, Post Screen	High V_{OL}, Low Temp. only	Low Beta - 1st Temp. Test
35/12	R	H1	Elec. Screen, Post Screen	Catastrophic	Chip Lifted From Header
	R	H8	Elec. Screen, Post Screen	High V_{OL}, Low Temp. only	Low Beta - 1st Temp. Test
	R	H7	Post Screen	High V_{OL}, Low Temp. only	Low Beta - 1st Temp. Test
	R	H10	Post Screen	High V_{OL}, Low Temp. only	Low Beta - 1st Temp. Test
	R	H4	Post B.I.	High V_{OL}, Low Temp. only	Low Beta
39/12	R	J22	Post B.I.	Catastrophic	Cracked Chip, V_{CC} to Substrate Short, Burned Open Internal V_{CC} Lead.
39/13A	B	B24	Post 2000 Hr. Life	High I_{CEX}	
38/7	B	F22	Post 2000 Hr. Life	I_F, I_R, V_{OL}, I_{SC}	Metal to Metal Layer Short.
35/9	B	I7	Post 2000 Hr. Life	V_{OC}, V_{OH}, I_{SC}, I_{CCO}	Metal to Metal Layer Short.
39/12	B	J18	Post 2000 Hr. Life	Catastrophic	Metal to Metal Layer Short.

TABLE 3.3

FAILURE ANALYSIS SUMMARY - DCQ DEVICES

3.2.2 BBTP1 Data Summary

The failures observed on the metalization stripe structures of BBTP1 during the wafer measurements prior to chip scribing are summarized in Table 3.4. Subsequent to the electrical wafer measurements visual measurements of metalization widths and thicknesses, oxide thickness, and diffused resistor widths were performed, this data is summarized in Table 3.5. A total of 6 devices from each wafer were assembled, visually inspected, encapsulated and subjected to screening and high stress evaluation. The results of the post encapsulation measurements BBTP1 devices are summarized in Table 3.6. It should be noted that not all structures in the BBTP1 devices were visually acceptable, but the test program was arranged so that only those individual structures that were visually acceptable were utilized on the tests intended to evaluate that particular structure. The results of the screening and high stress testing of the BBTP1 devices are summarized in Table 3.7. Table 3.8 summarizes the hours to failure for each of the devices subjected to the electromigration stress testing.

The results of the failure analysis performed on these test vehicles are summarized in Table 3.9.

LOT	WAFER	SAMPLE SIZE FOR RESISTIVE STRUCTURES	RMBPA	RMVIA	RMBPS	RMTP	RMTS	RMCC	RMBS	SAMPLE SIZE FOR CAPACITIVE STRUCTURES.	CVP34	CVI56	CTP47	CTI67	
33/15	A	12	1_1	0	0	1_1	1_1	1_1	2_2	2_1	4	0	0	1	0
35/9	1	12	0	1_1	0	0	1	3_1	2_1	0	4	1	2	0	1
35/12	H	12	0	1_1	0	0	1	2_1	5_2	0	4	1	2	0	1
38/3	E	12	0	4_2	0	1	0	0	12_4	0	4	2	3	1	0
38/7	F	12	0	1_1	2_2	0	0	3_2	2_2	3	4	0	3	0	1
38/8	G	12	1_1	2^1	0^2	1_1	1_1	1_1^2	7_2	2_1	4	1	3	0	1
39/12	J	12	1	1	0	0	0	0	2	2	4	1	2	0	1
39/13	~~B+C~~	12	0	5_3	3_2	2_2	0	0	4_3	1	4	0	0	0	0
39/14	D	12	1_1	1_1	0^2	0^2	0	1	0^3	0	4	1	2	0	1
TOTAL -	ALL	108	4_3	16_9	5_4	5_4	4_2	11_6	36_{16}	10_2	36	7	17	2	6
% FAIL -	ALL	-	3.7	14.7	4.6	4.6	3.7	10.2	33.3	9.3	--	19.5	47.2	5.6	16.6

NOTE:

a. The subscripts attached to failures indicate the number of failures that were incurred in test patterns located at the edge of the wafer.

b. Failure Criteria - Resistive Element Failure are those structures which exhibit either abnormally high resistance or open structures, capacitive element failures are those structures which exhibit oxide breakdown voltages of less than 200 volts.

TABLE 3.4

SUMMARY OF BBTP1 FAILURES AT WAFER MAPPING

TABLE 3.5

SUMMARY OF AVERAGE WIDTHS, THICKNESS AND CROSS SECTIONS FOR METALIZATION PATTERNS, PHOSPHOSILICATE DIELECTRIC AND DIFFUSED RESISTORS.

LOT	WAFER	BOTTOM LAYER Al THICKNESS Å	BOTTOM LAYER Al WIDTH - MILS.	BOTTOM LAYER Al CROSS SECTION - cm^2 x 10^8	TOP LAYER Al THICKNESS Å	TOP LAYER Al WIDTH - MILS.	TOP LAYER Al CROSS SECTION - cm^2 x 10^8	PHOSPHOSILICATE DIELECTRIC THICKNESS Å	RATIO DIELECTRIC TKNS / BOTTOM Al TKNS	RESISTOR DIFFUSION WIDTH - MILS.
33/15	A	8.9K	0.47	10.6	25.0K	0.43	27.3	10.0K	1.13	0.14
35/9	I	13.7K	0.47	16.3	18.0K	0.39	17.8	6.1K	0.45	0.15
35/12	H	13.7K	0.47	16.3	17.0K	0.38	16.5	6.5K	0.47	0.16
38/3	E	10.3K	0.48	12.5	14.7K	0.4	15.0	10.3K	1.0	0.16
38/7	F	10.3K	0.51	13.4	20.6K	0.34	17.8	8.9K	0.86	0.17
38/8	G	9.2K	0.51	11.9	20.6K	0.34	17.8	6.3K	0.61	0.16
39/12	J	10.0K	0.50	12.7	17.0K	0.50	21.6	8.5K	0.85	0.17
39/13	B+C	8.9K	0.50	11.3	15.1K	0.39	15.0	9.2K	1.03	0.16
39/14	D	8.9K	0.50	11.3	14.7K	0.40	15.0	10.3K	1.15	0.18

FAILURES*

LOT	WAFER	SAMPLE	R_{MTB}	R_{MBS}	R_{MTP}	R_{MBPA}	R_{MTS}	R_{MVIA}	R_{MCC}	R_{MBE}	R_{MTE}	R_{BOND}	CVP34	CVI56	CTP47	CTI67
33/15	A	5	0	0	0	1/0	0	0	0	1/1	0	0	0	1/0	0	1/0
35/9	I	6	0	2/2	0	2/2	0	1/1	0	0	0	0	3/0	5/0	1/0	2/0
35/12	H	6	0	0	1/1	1/1	0	0	0	0	0	0	1/0	2/0	0	1/0
38/3	E	6	0	0	0	0	0	0	6/2	0	0	0	3/1	5/1	1/0	3/1
38/7	F	6	0	1/1	0	0	3/0	0	1/1	0	6/6	0	5/0	6/0	1/0	1/0
38/8	G	6	0	0	0	0	0	0	6/0	0	0	0	4/0	5/0	1/0	0
39/12	J	6	0	1/1	0	0	1/1	0	0	0	0	0	0	2/0	1/0	2/0
39/13A	B	6	0	2/0	0	0	0	1/1	1/1	0	0	0	4/0	4/1	2/0	4/1
39/13B	C	6	3/3	1/1	0	1/1	0	5/5	4/4	3/3	0	4/4	1/0	2/0	2/0	1/0
39/14	D	6	0	0	0	0	1/0	0	0	0	0	0	2/0	5/0	1/0	4/0
TOTALS		59	3/3	7/5	1/1	5/4	5/1	7/7	18/8	4/4	6/6	4/4	23/1	42/2	10/0	19/2
% FAIL			5.1	11.9	1.6	8.3	8.3	11.7	30.0	6.7	10.0	6.7	39.0	71.3	17.0	32.2

* FAILURE CRITERIA
RESISTIVE STRUCTURES - OPENS OR ABNORMALLY HIGH RESISTANCE
CAPACITIVE STRUCTURES - OXIDE BREAKDOWN OF LESS THAN 200 VOLTS.

NOTE: The Failure Symbolism (X/X) Indicates:

Total Failures/Failures Were Defect Was Microscopically Visible At Preseal Inspection (i.e., 3/2 indicates 3 failures occurred, but 2 of the failures were at locations where visual defects were observed during the preseal microscopic inspection.) Visual defects were used in this evaluation because each structure is an individual test element and a visual problem with RMTB for example would have no effect on the testing performed on RMBS.

TABLE 3.6 - BBTP1 FAILURES AT POST ENCAPSULATION ELECTRICAL MEASUREMENTS

TEST STRUCTURE	TEST CODE	TEST	SAMPLE ALL WAFERS COMBINED	R_{MTB}	R_{MBS}	R_{MTP}	R_{MBPA}	R_{MTS}	R_{MVIA}	R_{MCC}	R_{MBE}	R_{MTE}	R_{BOND}	CVP34	CVI56	CTP47	CTI67	COMMENTS
BBTP1	E1	INITIAL MEAS.	59	3	7	1	5	5	7	18	4	6	4	23	42	10	19	SEE TABLE 3.2.6
BBTP1	E2	POST SCREEN	59	0	0*	0	0	0	0*	0*	0	0	0	0	0	0	0	SEE NOTE a.
THERMAL STRESS SEQUENCE (DEVICES SELECTED FROM INITIAL SAMPLE OF 59 AFTER E2 MEASUREMENTS)																		
BBTP1	T1	POST 10 CYCLES THERM. SHOCK	28	0	0	0	0	0	0	0	0	0	0	--	--	--	--	
	T2	POST 340 HR. 200°C STORAGE	28	0	0	0	0	0	0	0	0	0	0	0	1	1	0	SEE NOTE b.
	T3	POST 10 CYCLES THERM. SHOCK	28	0	0	0	0	0	0	0	0	0	0	--	--	--	--	
	T4	POST 340 HR. 200°C STORAGE	28	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	T5	POST 10 CYCLES THERM. SHOCK	28	0	0	0	0	0	0	0	0	0	0	--	--	--	--	
	T6	POST 340 HR. 200°C STORAGE	28	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	T7	POST 40K "G" CONST. ACCEL.	28	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ELECTROMIGRATION STRESS SEQUENCE (DEVICES SELECTED FROM INITIAL SAMPLE OF 59 AFTER E2 MEASUREMENTS)																		
BBTP1	EM	POST R_{MTE} & R_{MBE} STRESS	19	14 OF 19 DEVICES EXPERIENCED OPENS IN R_{MTE} OR R_{MBE} STRUCTURES DURING 40 HRS. OF TEST.														SEE TABLE 3.2.8
	BL	POST R_{MBPA} & R_{MBS} STRESS	20	16 OF 20 DEVICES EXPERIENCED OPENS IN R_{MBPA} OR R_{MBS} STRUCTURES DURING 61 HRS. OF TEST.														SEE TABLE 3.2.8
	VA	POST R_{MVIA} & R_{MTB} STRESS	17	7 OF 17 DEVICES EXPERIENCED OPENS IN R_{MVIA} STRUCTURE DURING 340 HRS. OF TEST.														SEE TABLE 3.2.8
	TL	POST R_{MTP} & R_{MTS} STRESS	20															
	CC	POST R_{MCC} STRESS	20															

NOTES: a. FOUR DEVICES (S/N E2, F4, G1 & G5) SHOWED IMPROVED R_{MVIA} CHARACTERISTICS, 1 DEVICE (G2) WHICH INITIALLY FAILED R_{MCC} RECOVERED, 2 DEVICES (S/N G6 & I9) SHOWED IMPROVED R_{MBS}

b. DEVICE J6 FAILED CVI56 MEASUREMENT, DEVICE I5 FAILED CTP47 MEASUREMENT.

TABLE 3.7 - BBTP1 SCREENING & HIGH STRESS TESTING FAILURE SUMMARY

EM STRESS (STRUCTURES R_{MTE} AND R_{MBE})
I = 63.5 mA, TEMPERATURE = 125°C

SAMPLE	HOURS TO FAILURE	S/N OF FAILURE	STRUCTURE FAILED
19	5	A3	R_{MBE}
	16	A1	R_{MBE}
	47	E3	R_{MBE}
	76	H2	R_{MBE}
	121	A3	R_{MBE}
	168	I1	R_{MBE}
	169	C1	R_{MBE}
	170	H3	R_{MBE}
	170	I4	R_{MBE}
	171	D2	R_{MBE}
	172	G3	R_{MBE}
	173	J1	R_{MBE}
	175	C5	R_{MBE}
	176	B3	R_{MBE}

BL STRESS (STRUCTURES R_{MBPA} AND R_{MBS})
I = 200 mA, TEMPERATURE = 125°C

SAMPLE	HOURS TO FAILURE	S/N OF FAILURE	STRUCTURE FAILED
20	13	A1	R_{MBS}
	22	A3	R_{MBS} & R_{MBPA}
	25	G3	R_{MBS} & R_{MBPA}
	26	E1	R_{MBS}
	35	H2	R_{MBS}
	41	E3	R_{MBS}
	42	B2	R_{MBPA}
	44	G1	R_{MBPA}
	46	A2	R_{MBPA}
	49	H3	R_{MBS}
	50	I1	R_{MBPA}
	56	C1	R_{MBPA}
	57	I4	R_{MBPA}
	58	D4	R_{MBPA}
	61	C5	R_{MBS}

VA STRESS (STRUCTURES R_{MVIA} AND R_{MTB})
I = 200 mA, TEMPERATURE = 125°C

SAMPLE	HOURS TO FAILURE	S/N OF FAILURE	STRUCTURE FAILED
17	14	I4	R_{MVIA}
	141	A2	R_{MVIA}
	183	E1	R_{MVIA}
	203	D2	R_{MVIA}
	228	G1	R_{MVIA}
	273	C1	R_{MVIA}
	302	G3	R_{MVIA}

TL STRESS (STRUCTURES R_{MTP} AND R_{MTS})
I = 200 mA, TEMPERATURE = 125°C

SAMPLE	HOURS TO FAILURE	S/N OF FAILURE	STRUCTURE FAILED
19	4	D3	R_{MTS}
	11	D4	R_{MTS}
	21	I4	R_{MTS}

CC STRESS (STRUCTURES R_{MCC})
I = 5.7 mA, TEMPERATURE = 125°C

SAMPLE	HOURS TO FAILURE	S/N OF FAILURE	STRUCTURE FAILED
19	405	I4	R_{MCC}
	551	G1	R_{MCC}

TABLE 3.8 - BBTP1 ELECTROMIGRATION STRESS FAILURE SUMMARY

TEST FAILED, STRUCTURE FAILED AND FAILURE MECHANISM

DEVICE S/N	EM Stress, high current stress of the electromigration test structures R_{MTE} and R_{MBE}	BL Stress, high current stress of the bottom layer metal test structures R_{MBS} and R_{MPA}*	VA Stress, high current stress of test structures R_{MVIA} and R_{MTB}*	TL Stress, high current stress of the top layer metal structures R_{MTS} and R_{MTP}*	CC Stress, high current stress of the test structure R_{MCC}*
A1	Electromigration, R_{MBE}	Electromigration, R_{MBS}			
A2	Electromigration, R_{MBE}	Electromigration, R_{MBS}	Defect Cause Not Visible		
A3	Defect Cause Not Visible	Electromigration, R_{MBS}			
B2		Electromigration, R_{MBS}			
B3	Electromigration, R_{MBE}				
C1	Electromigration, R_{MBE}	Electromigration, R_{MPA}	Defect Cause Not Visible		
C5	Electromigration, R_{MBE}				
D2	Electromigration, R_{MTE} Scratch		R_{MVIA} Open At Scratch		
D3		Electromigration, R_{MBS}		Electromigration, R_{MTS}	
D4		Electromigration, R_{MPA}		Defect Cause Not Visible	
E1		Electromigration, R_{MBS}	Burned Contact R_{MVIA}		
E3	Defect Cause Not Visible	Electromigration, R_{MBS}			
G1		Electromigration, R_{MBS}	Defect Cause Not Visible		Defect Cause Not Visible
G3	Electromigration, R_{MBE}	Defect Cause Not Visible	Defect Cause Not Visible		
H2	Defect Cause Not Visible	Electromigration, R_{MBS}			
H3	Electromigration, R_{MBE}	Electromigration, R_{MBS}			
I1	Electromigration, R_{MBE}	Electromigration, R_{MBS}			
I4	Electromigration, R_{MBE}	Electromigration, R_{MBS}	Damaged R_{MVIA} Metal	Electromigration, R_{MTS}	Damaged R_{MCC} Metal
J1	Electromigration, R_{MBE}				

* See Table 3.2.8 For Specific Test Conditions.

TABLE 3.9 - FAILURE ANALYSIS SUMMARY - BBTP1

3.2.3 BBTP2 DATA SUMMARY

Table 3.10 summarizes the mean values of the pertenent BBTP2 parameters measured during wafer mapping. Table 3.11 summarizes the mean values of the pertenent device parameters measured subsequent to encapsulation of the test patterns. The test conditions for the post encapsulation measurements were made at slightly different test conditions than the wafer map measurements but there is good correlation between the two sets of measurements.

Subsequent to the post encapsulation measurements the BBTP2 devices were subjected to the same 100% in process screens as the DCQ devices and were then remeasured electrically and split into three different groups to perform high stress testing on:

a. The Transistor Structures,
b. The Diode Structures, and
c. The MOS Structure.

The results of the high stress testing on each of these structures is shown in Table 3.12. Table 3.13 shows the mean value of V_{GST} for each of the individual wafers. The V_{GST} value is proportional to the thermal oxide layer thickness.

No catastrophic failures were incurred during the high stress evaluation of this test pattern and therefore no failure analysis was required.

TABLE 3.10 - MEAN VALUES - WAFER MAP PARAMETERS OF BBTP2

LOT/WAFER	WAFER CODE	h_{FEM} MEAN INPUT TRANSISTOR		h_{FEO} MEAN OUTPUT TRANSISTOR		V_{SAT} (VOLTS) OUTPUT TRANSISTOR		R_{NE} (Ω/□) BURIED n^+ DIFFUSION		R_B (OHMS) WIDE P TYPE RESISTOR		R_{BP}(KΩ) WIDE EMITTER-BASE PINCH RESISTOR		R_B (Ω/□) BASE DIFFUSION SHEET P		R_{25} (Ω/□) 25K DIFFUSED RESISTOR		R_{EML} (Ω/□) n^+ EMITTER DIFFUSION		R_{EK} (KΩ) EPI RESISTOR		R_{EBPJ} (KΩ) EPI - BASE PINCH RESISTOR	
		n	MEAN	n	MEAN	n	MEAN	n	MEAN	n	MEAN	n	MEAN	n	MEAN	n	MEAN (NOMINAL)	n	MEAN	n	MEAN	n	MEAN
33/15	A	10	17.8	11	29.5	12	.126	12	13.8	4	377	4	3.7	4	123	4	29	11	2.38	10	5.8	10	12.5
35/9	I	9	9.2	9	18.2	9	.131	10	12.9	4	366	4	2.7	4	120	4	30	12	2.37	11	5.6	11	13.4
35/12	H	12	11.6	10	19.8	10	.118	12	12.8	4	360	4	2.4	4	118	4	28	12	2.45	12	5.0	12	11.5
38/3	E	10	10.5	10	19.4	10	.216	11	21.1	4	417	4	3.0	4	136	4	38	11	2.50	11	5.8	12	14.1
38/7	F	7	11.2	6	21.3	9	.142	12	18.6	4	393	4	2.8	4	129	4	35	11	2.42	11	6.2	12	20.0
38/8	G	10	12.3	11	21.7	10	.168	12	17.5	4	430	4	2.5	4	140	4	28	10	2.45	10	5.5	11	10.0
39/12	J	11	22.3	11	36.4	11	.146	12	18.4	4	442	4	3.5	4	145	4	36	12	2.60	11	7.5	12	18.0
39/13	B&C	10	18.9	9	34.6	9	.138	11	16.8	4	395	4	4.5	4	129	4	33	10	2.53	9	5.9	9	13.2
39/14	D	9	29.6	10	49.0	10	.109	11	17.5	4	500	4	4.7	4	164	4	41	10	2.56	12	5.5	12	14.1
NOMINAL DESIGN VALUES			30.0		40.0		.15		20.0		385		3.0		118		25		2.0		2.5		13.0

LOT/WAFER	WAFER CODE	h_{FEM}	h_{FEMR}	I_{E1} (LATERAL h_{FE}) INPUT TRANSISTOR	h_{FEO}	h_{FEOR}	V_{SAT} (VOLTS)	V_{BE}(VOLTS)	BV_{CEO}(VOLTS)	V_{GST1}(VOLTS)	BVR1 (VOLTS)	BVR2 (VOLTS)	BVR3 (VOLTS)
33/15	A	25	0.1	0.75	23	0.55	0.135	0.80	15.0	9.0	45.0	40.0	45.0
35/9	I	15.5	0.06	0.03	17	0.30	0.15	0.80	16.0	15.0	40.0	40.0	50.0
35/12	H	13.5	0.07	0.03	16.5	0.22	0.13	0.80	14.0	20.0	30.0	35.0	50.0
38/3	E	17	0.06	0.03	17	0.33	0.20	0.87	15.0	28.0	50.0	48.0	48.0
38/7	F	24	0.25	0.2	23	1.0	0.14	0.81	15.0	*	*	*	48.0
38/8	G	15	0.04	*	17	0.27	0.20	0.84	16.0	*	45.0	45.0	45.0
39/12	J	25	0.04	0.04	25	0.32	0.11	0.79	16.5	28.0	35.0	35.0	45.0
39/13A	B	24	0.12	0.04	24	0.40	0.14	0.80	16.0	28.0	45.0	45.0	45.0
39/13B	C	30	0.20	0.08	24	0.70	0.14	0.80	13.5	40.0	30.0	30.0	45.0
39/14	D	39	0.19	0.09	34	1.10	0.11	0.78	11.0	30.0	36.0	37.0	45.0

NOTE: TYPICAL SAMPLE FOR ALL DEVICES IS 6 UNITS.

* DATA TOO SCATTERED TO DETERMINE MEAN VALUE.

TABLE 3.11 - MEAN VALUES - POST ENCAPSULATION PARAMETERS OF BBTP2

TRANSISTOR STRESS - INPUT AND OUTPUT TRANSISTOR STRUCTURES

CATASTROPHIC FAILURES

SAMPLE	POST 340 HR. MEAS.	POST 670 HR. MEAS.	POST 1000 HR. MEAS.	COMMENTS
19	0	0	0	INPUT TRANSISTOR h_{FEM} SHOWS DEGRADATION AFTER 670 HOURS. (SEE BELOW)

MEAN PARAMETER VALUES

TEST PERIOD	h_{FEM}	h_{FEMR}	I_{E1}	I_{E2}	h_{FEO}	h_{FER}	V_{SAT} VOLTS	V_{BE} VOLTS
INITIAL	24.1	.084	.043	.045	25.5	0.38	.160	.805
POST 340 HR.	24.1	.084	.043	.045	25.5	0.38	.160	.804
POST 670 HR.	22.8*	.084	.043	.045	25.7	0.38	.161	.801
POST 1000 HR.	22.3*	.084	.043	.045	25.5	0.38	.160	.803

*THE ONLY SIGNIFICANT PARAMETER SHIFTS OCCURRED IN h_{FEM}. THESE SHIFTS WERE 5.4% AFTER 670 HRS. AND 7.5% AFTER 1000 HRS.

DIODE STRESS - DIODE STRUCTURES

CATASTROPHIC FAILURES

SAMPLE	POST 340 HR. MEAS.	POST 670 HR. MEAS.	POST 1000 HR. MEAS.	COMMENTS
15	0	0	0	STABILITY IS GOOD - ABSOLUTE DELTA'S FOR REVERSE LEAKAGE ARE TYPICALLY LESS THAN 10 nA & REVERSE BREAKDOWN VOLTAGE DELTAS ARE TYPICALLY LESS THAN 0.2 VOLTS.

MOS STRESS - MOS STRUCTURE

SAMPLE	POST 340 HR. MEAS.	POST 670 HR. MEAS.	POST 1000 HR. MEAS.	COMMENTS
19	0	0	0	V_{GST} STABILITY THROUGH TEST IS SHOWN BELOW.

MEAN VALUE AND % CHANGE IN V_{GST}

TEST PERIOD	V_{GST1} MEAN	V_{GST1} % CHANGE	V_{GST2} MEAN	V_{GST2} % CHANGE
INITIAL	17.47	----	20.31	----
POST 340 HR.	18.12	3.6	20.93	3.0
POST 670 HR.	18.20	4.0	21.01	3.4
POST 1000 HR.	18.22	4.1	20.98	3.4

TABLE 3.12 - SUMMARY - HIGH STRESS TESTING OF BBTP2 DEVICES

MEAN VALUE

TEST PATTERN	LOT	WAFER	MEAN VALUE V_{GST1} VOLTS	MEAN VALUE V_{GST2} VOLTS
BBTP2	33/15	A	12.5	15.0
BBTP2	35/9	I	18.0	22.0
BBTP2	35/12	H	18.0	22.5
BBTP2	38/3	E	26.0	28.5
BBTP2	38/7	F	11.0	14.0
BBTP2	38/8	G	6.4	8.7
BBTP2	39/12	J	28.5	33.0
BBTP2	39/13	B+C	21.2	23.0
BBTP2	39/14	D	28.0	32.5

TABLE 3.13 - MEAN VALUES, V_{GST1} AND V_{GST2}, BY WAFER FOR BBTP2

3.3 BILAYER BIPOLAR TEST VEHICLE CORRELATION

The following subsections show the degree of correlation observed between the results of preseal visual inspection and DCQ failures incurred during the Phase 3 Test Program as well as the degree of correlation observed between the measured test pattern parameters and the DCQ failures incurred during the performance of the Phase 3 Evaluation.

3.3.1 Correlation Of DCQ Failures With Visual Inspection Results

Figure 3.4 shows the final electrical test yield for the DCQ vehicles as a function of the visual class into which the devices were assigned and as a function of the wafer from which the devices were obtained. In general, the Class A Visual Devices exhibited a higher final test yield than the Class B Devices, which in turn generally exhibited a higher electrical yield than the Class R devices. Exceptions to these generalities occur, but they occur when small sample sizes are used to calculate the yield, and the degree of confidence in the calculated percentage is low.

Figure 3.5 shows the observed DCQ failure rate as a function of visual classification for both the initial electrical test and the entire Phase 3 Evaluation Program. This data shows that the devices from wafers 33/15 (A) and 39/13 (B+C) exhibit not only the lowest initial failure percentage, but after removal of the initial failures, the remaining devices from these same wafers exhibit the lowest failure percentage throughout the entire screening and life test sequence. In general, the Class A and B Devices, combined as a single group to preclude the utilization of small samples, exhibit lower failure percentages than the Class R Devices.

Figure 3.6 shows the initial test failure percentage plotted against the visual yield for each DCQ wafer. Since all Class A devices are also Class B devices, the data for both the Class A and the Class B devices was combined for the Class B device plot. The plots show that the first test electrical failure percentage is inversely proportional to the visual yield on a wafer by wafer basis. Figure 3.7

shows that on a wafer by wafer basis, after the first test failures have been removed, the failure percentage of the remaining good devices through the screens and life test is also inversely proportional to the visual wafer yield.

The correlation of this data revealed:

a. The preseal visual inspection aids in the screening of potentially unreliable devices but is not sufficient to remove all potential failures.

b. The DCQ devices from the high visual yield wafers experienced the lowest failure rate both initially and throughout the screening and life testing.

c. The Class A and Class B visual devices showed better initial test failure rates than the Class R devices.

That the high preseal visual yield wafers experienced the lowest failure rates indicates that some intangable benefits are derived from the performance of the preseal visual inspections, and it may be possible to develop criteria that specifies the minimum visual yield required to accept a wafer for high reliability utilization. The quantity of data taken during this work; however, is not sufficient to make this determination.

The overall electrical failure percentage of the DCQ devices at various points in the Phase 3 Evaluation is shown below by visual class.

VISUAL CLASS	AT INITIAL TEST			THROUGH 100% SCREENS			THROUGH LIFE TEST		
	n	f	Fail	n	f	Fail	n	f	Fail
A	44	17	38.6%	27	6	22.2%	21	4	19.0%
B	157	64	40.7%	68	13	19.4%	61	6	9.8%
R	68	47	69.0%	21	7	33.3%	14	0	0%

From the above data, it is noted that at the initial electrical measurements there is no significant difference between the Class A and the Class B failure percentages, and the the failure percentage for the Class R devices is approximately 150% greater than for the Class A and B devices. Through the 100% screens, the failure percentage for all visual classes dropped to about one half the percentage experienced at the initial measurements. However, through life test, the Class A devices experienced the highest percentage of failures and the Class R devices, the lowest percentage of failures. Because all visual classes were subjected to identical testing, and because the Class R devices experienced higher failure rates through the initial testing and 100% screens the data infers that the preseal visual inspection is effective in removing devices with relatively gross manufacturing defects. That there was no significant difference in the failure rates of the Class A and B devices through the initial test and the 100% screens indicates only the defects for which the Class A criteria is more stringent were not factors involved in the failure of these particular devices. That the Class A devices experienced higher life test failure rates than the Class B devices which in turn experienced higher life test failure rates than the Class R devices indicates that other than visual mechanisms contributed to the failures. The other than visual mechanisms include variations in the diffusion parameters, variations in oxide thicknesses, and variations in metalization thickness as well as unresolvable oxide defects.

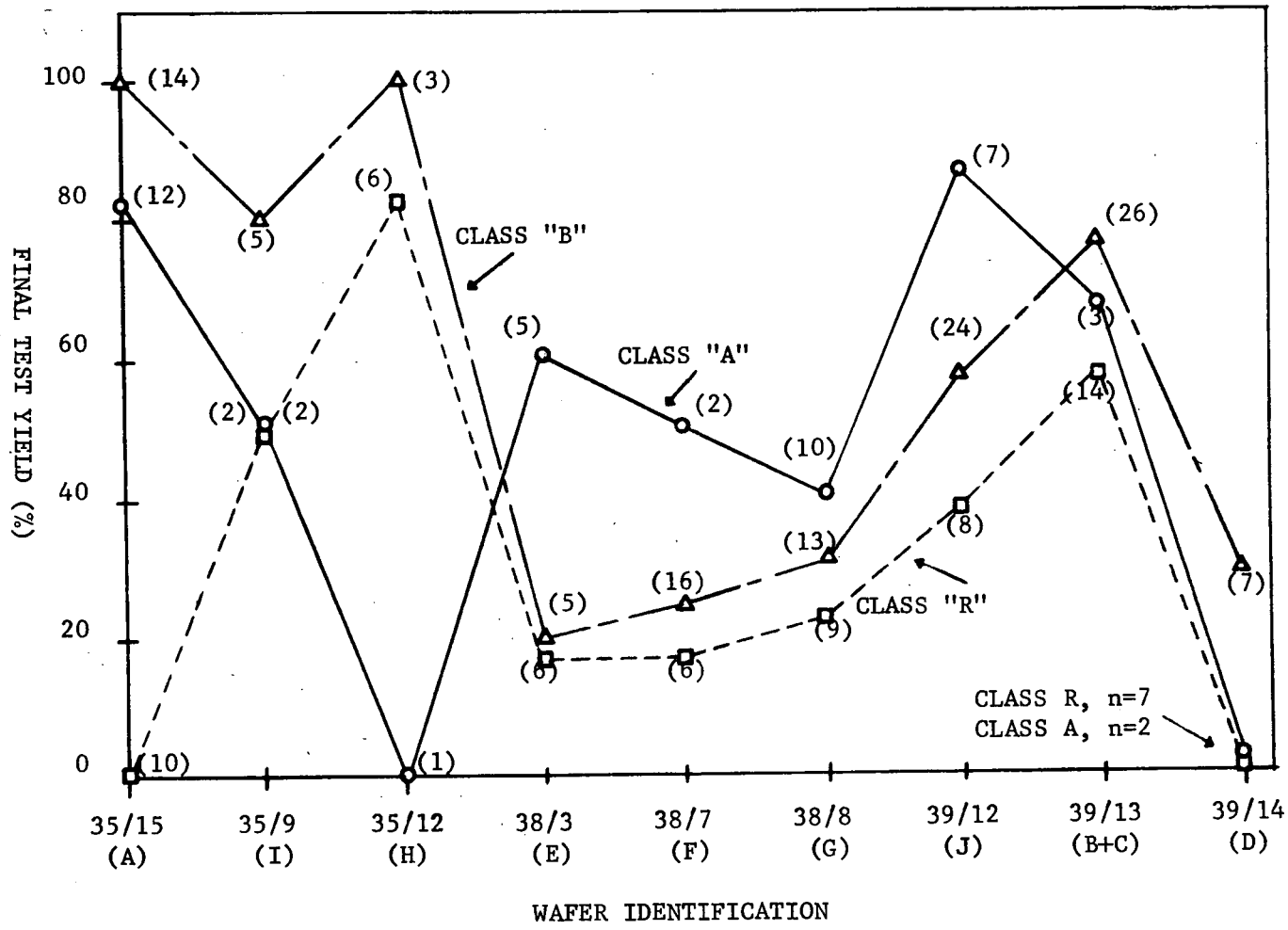


FIGURE 3.4 - FINAL TEST YIELD AS A FUNCTION OF PRESEAL VISUAL CLASSIFICATION.

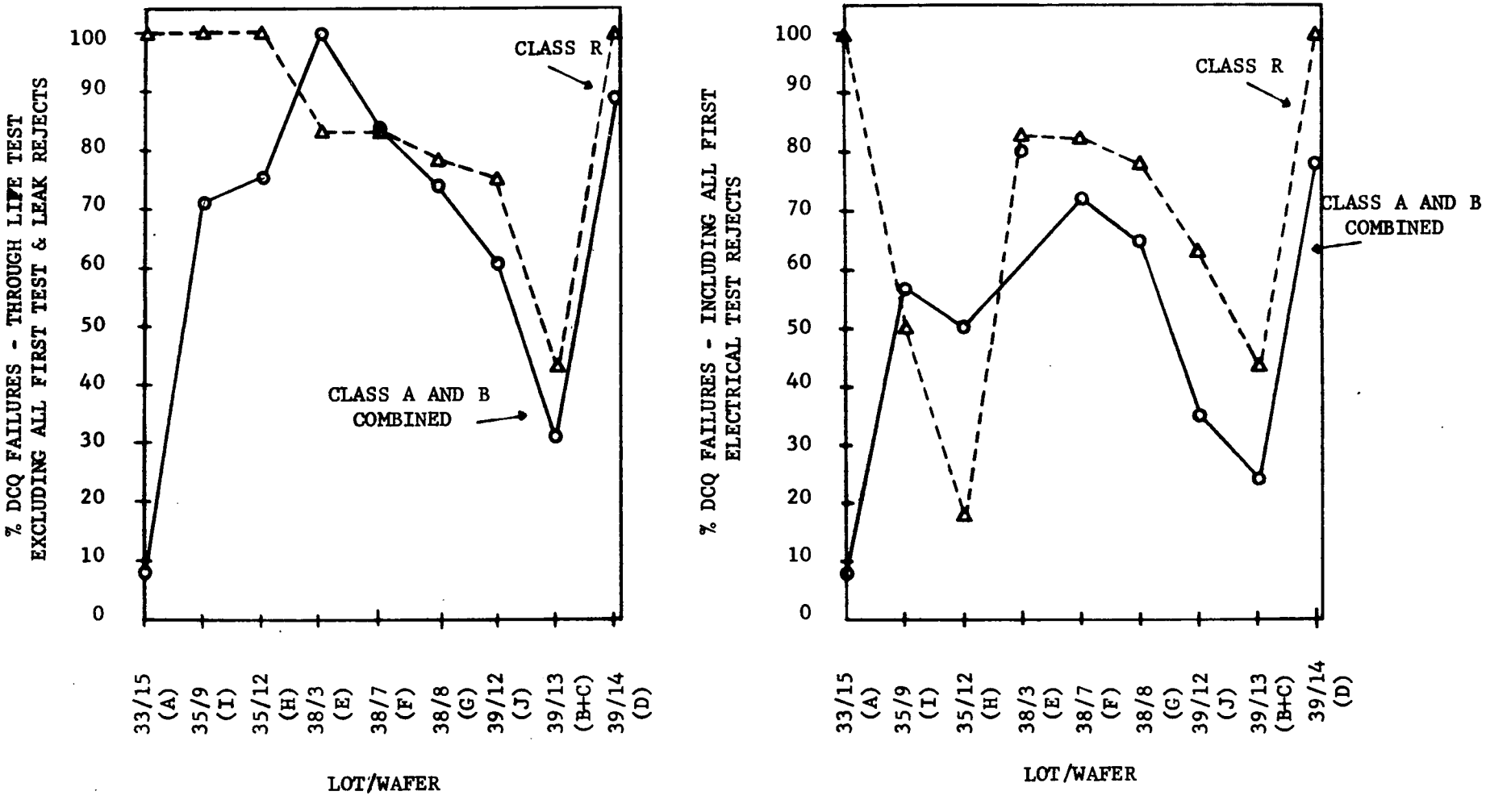
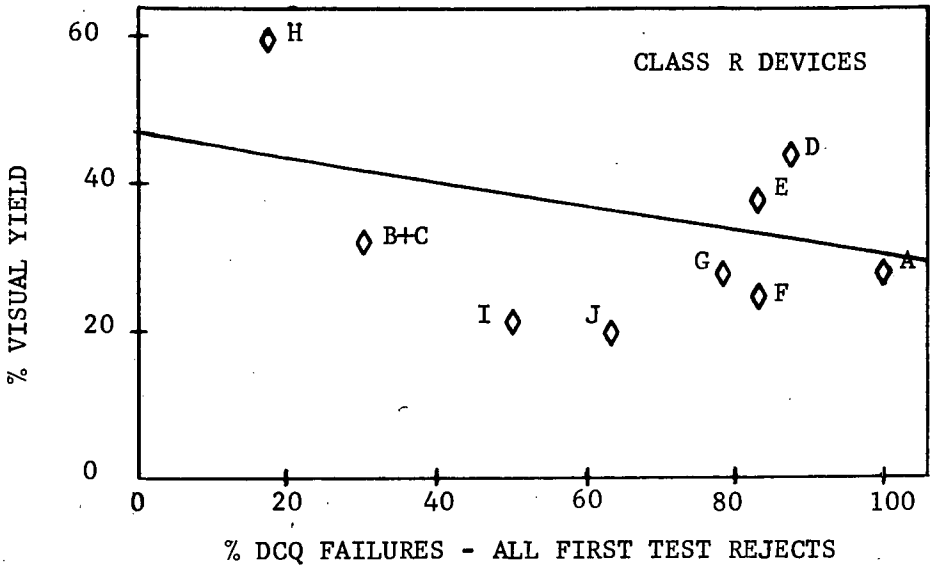
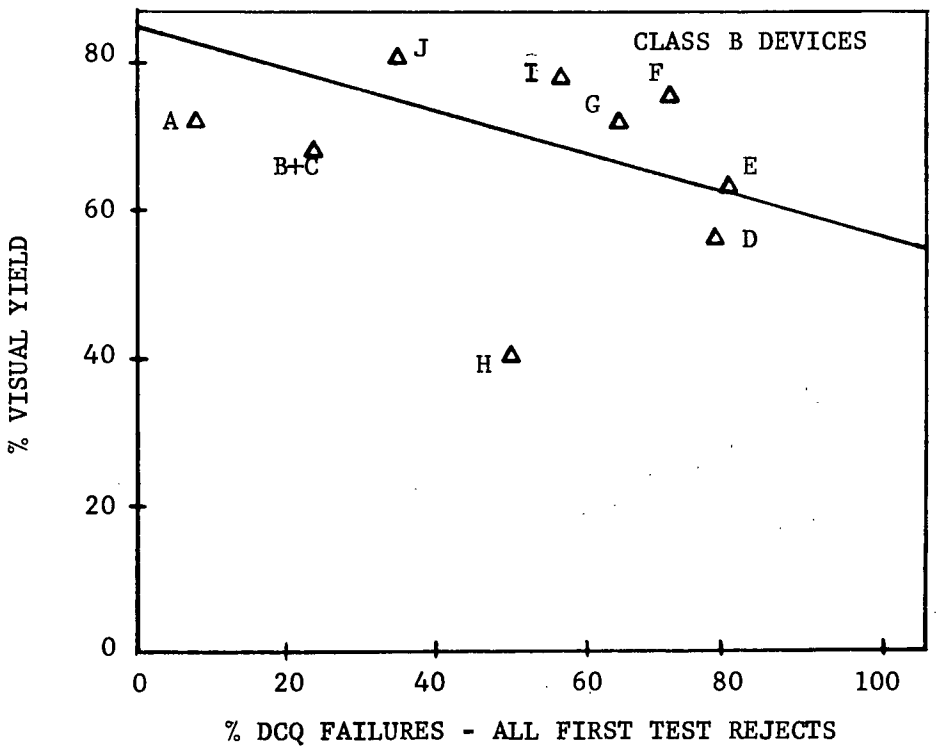


FIGURE 3.5 - OBSERVED FAILURE % OF DCQ VEHICLES AS A FUNCTION OF VISUAL CLASSIFICATION





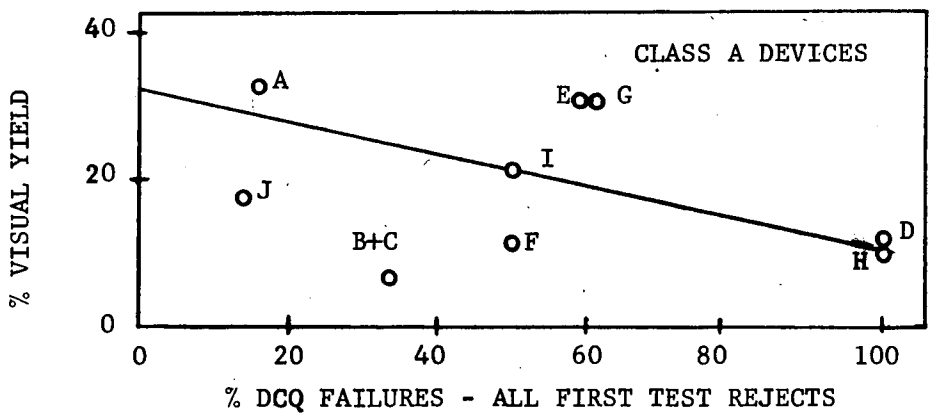


FIGURE 3.6 - VISUAL YIELD vs FIRST ELECTRICAL TEST FAILURE %

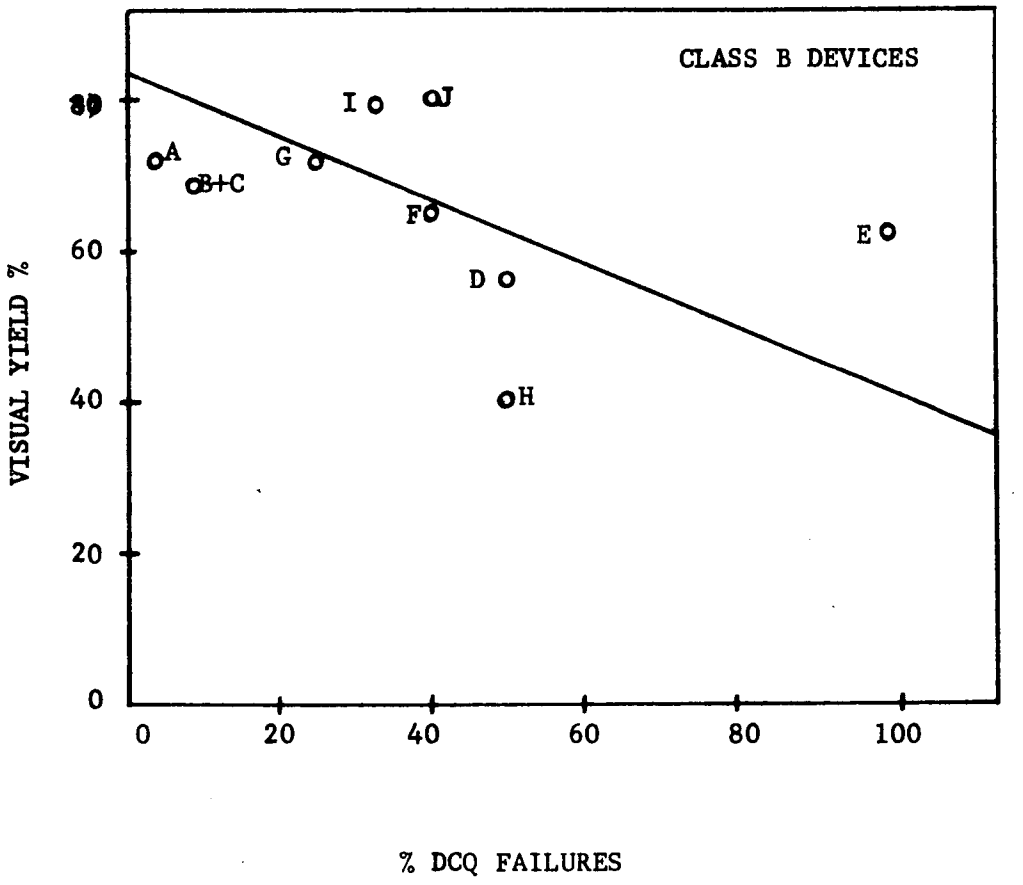


FIGURE 3.7 - % DCQ FAILURE % - THROUGH SCREENS AND LIFE TEST vs VISUAL YIELDS

3.3.2 Correlation of DCQ Failures With Electrical Parameter Measurements

Electrical parametric determinations were performed on the DCQ vehicles and the BBTP2 vehicles prior to wafer scribing and throughout the entire test program. The most significant correlations, obtained as a result of these measurements were:

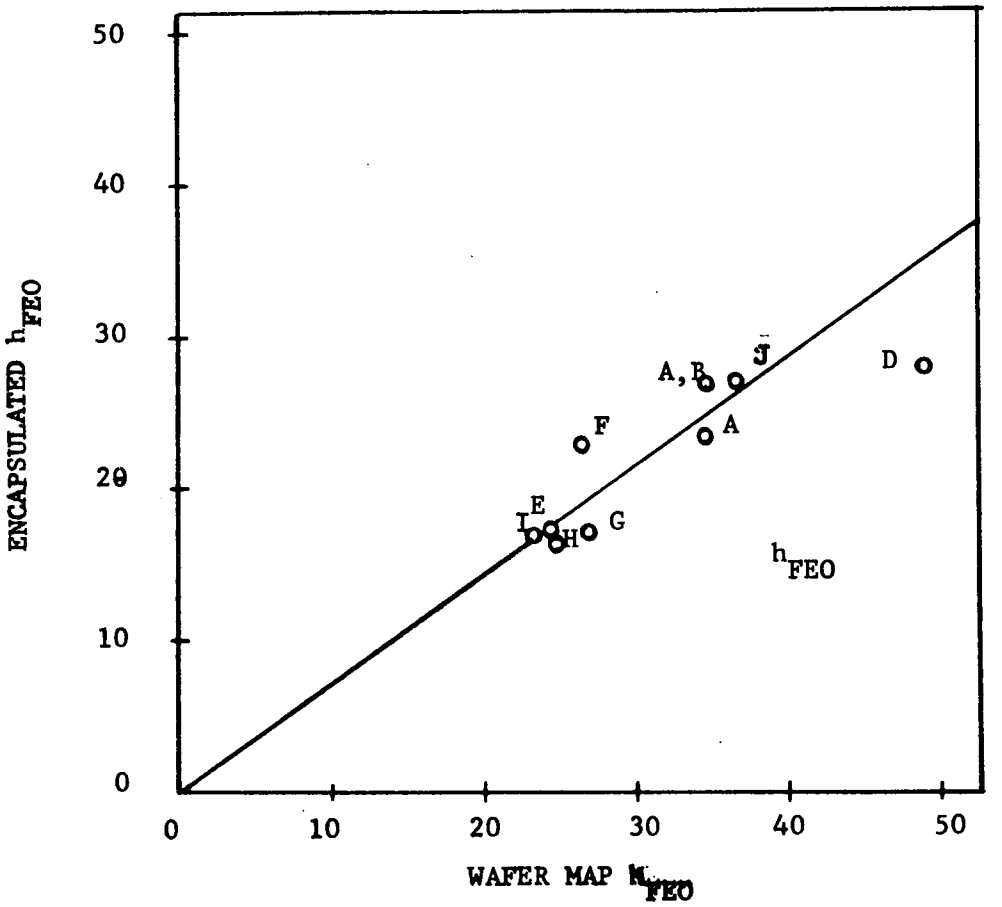
a. The bulk parameters measured on BBTP2 show a wafer to wafer correlation with the DCQ failure rate.

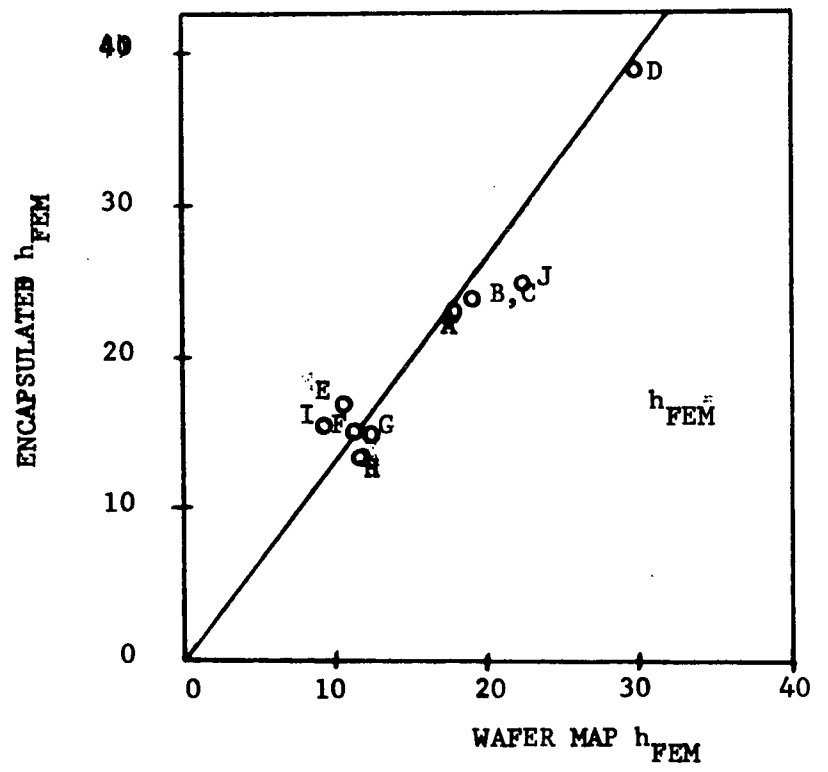
b. The oxide and metalization integrity parameters of BBTP1 show a wafer to wafer correlation with the DCQ failure rate.

c. The wafer mapping functional test data on the DCQ devices shows correlation with the initial D.C. test data, and with the failure rate through the 100% screening and life test.

3.3.3 Correlation of BBTP2 Parameters With The DCQ Failure Rate

The mean values obtained for the fundamental bulk parameters of BBTP2 measured during both wafer mapping and subsequent to encapsulation are summarized on a wafer by wafer basis in Tables 3.10 and 3.11 respectively. The evaluation of these parameters indicates that there is considerable variation in the bulk parameters between diffusion lots, and there is also variation in certain parameters in different wafers from the same diffusion lot. (The first two digits in the Lot/Wafer code indicate the diffusion lot number, the remaining digits indicate the wafer number from a given diffusion lot.) As shown in Figure 3.8, there is good correlation between the BBTP2 parameters measured during wafer mapping, and the parameters measured subsequent to encapsulation, which indicates that sufficient information can be derived from the wafer mapping to determine whether it is advisable to scribe and bond the functional and test pattern chips from any given wafer. If the evaluation of the bulk pattern data shows that yields will be low or that the circuit parameters will be marginal, then there is no point in assembly of any of the chips. However, if the bulk parameters indicate good yields, and well in specification functional circuit parameters, then both the





NOTE:
1:1 CORRELATION WAS NOT OBTAINED BECAUSE THE WAFER MAPPING MEASUREMENTS FOR BOTH h_{FEM} AND h_{FEO} WERE MEASURED AT DIFFERENT CONDITIONS THAN THE POST ENCAPSULATION MEASUREMENTS.

FIGURE 3.8 - CORRELATION OF BBTP2 WAFER MAP AND POST ENCAPSULATION PARAMETERS

test pattern chips and the functional chips should be assembled for further screening and stability evaluations.

The most significant deviations of the BBTP2 parameters from design values so far as proper circuit operation is concerned is the fact that in general the h_{FE} values were lower than nominal design and the resistance values were higher than nominal design values. Figure 3.9 shows the basic cell of the DCQ device with the nominal design values for the individual components. Table 3.14 shows the mean room temperature resistor and h_{FE} values for the individual components, as determined from the BBTP2 measurements on a wafer by wafer basis. Because we experienced difficulty with the proper operation of the DCQ life test circuit at -55°C and because we experienced low temperature DCQ parameter failures at a much greater rate than room or high temperature, the BBTP2 mean value parameters were corrected for temperature and their effect on proper circuit operation at -55°C was evaluated using the worst case design equations. The evaluation is covered in detail in Appendix B.

Figure 3.10 shows the -55°C calculated values for I_{OL}, V_{OH}, and I_{SC} plotted against the initial failure percentage of the DCQ devices on a wafer by wafer basis. With the exception of the devices from wafers D and F, the plots show a good correlation between the -55°C calculated values and the DCQ failure percentage (i.e., the devices from wafers well inside the parameter limits exhibited the lowest failure rates). Significantly, the devices from wafers A, B, and C, the wafers which exhibited the lowest initial failure percentage and for which the -55°C calculated values were well inside the parameter limits, exhibited the lowest failure percentages though the entire screening and life test sequence. The high initial failure rates for the devices from wafers D and F in spite of the fact they are well within the calculated -55°C limits can be explained by the fact that these wafers exhibited a high reliability risk based on the measurement of the capacitor structure of BBTP1 (see Table 3.16).

Wafer J experienced a relatively high failure percentage during the initial measurements as well as though the screening and life test sequence although the calculated -55°C parameters were well inside the established limits and the capacitor and resistor structures of BBTP1 showed only a moderate/reliability risk (Table 3.16). However, the analysis of 3 of the failures incurred on DCQ devices from wafer J showed they had failed because of chip to header bond failures, or cracked chips, mechanisms not sensitive to detection by the test pattern approach. The -55°C calculated parameters for wafer E certainly indicated that devices from this wafer would be reliability risks because the values determined for I_{OL}, V_{OH}, and I_{SC} all failed the specification limit and this wafer was also determined to be a metalization and oxide integrity risk (Table 3.16). The calculated -55°C values for I_{SC} for wafers H, I, and G showed that devices from these wafers were marginal to the minimum short circuit current parameter and wafers G and I were oxide integrity risks based on the capacitor data from BBTP1 (see Table 3.16).

The design equations of Appendix B indicate that the DCQ parameters are strong functions of both h_{FE} and the resistor values. Figure 3.11 shows the resistance of structure R_{25} plotted against the calculated base diffusion sheet rho determined from the measurement of R_B, and the calculated -55°C I_{SC} plotted against the quotient of h_{FEO} rho_{BASE} $\Omega/$. Both curves show good correlation, and demonstrate respectively the accuracy of the resistance measurements and the dependence of the calculated parameters on both h_{FEO} and the resistance values.

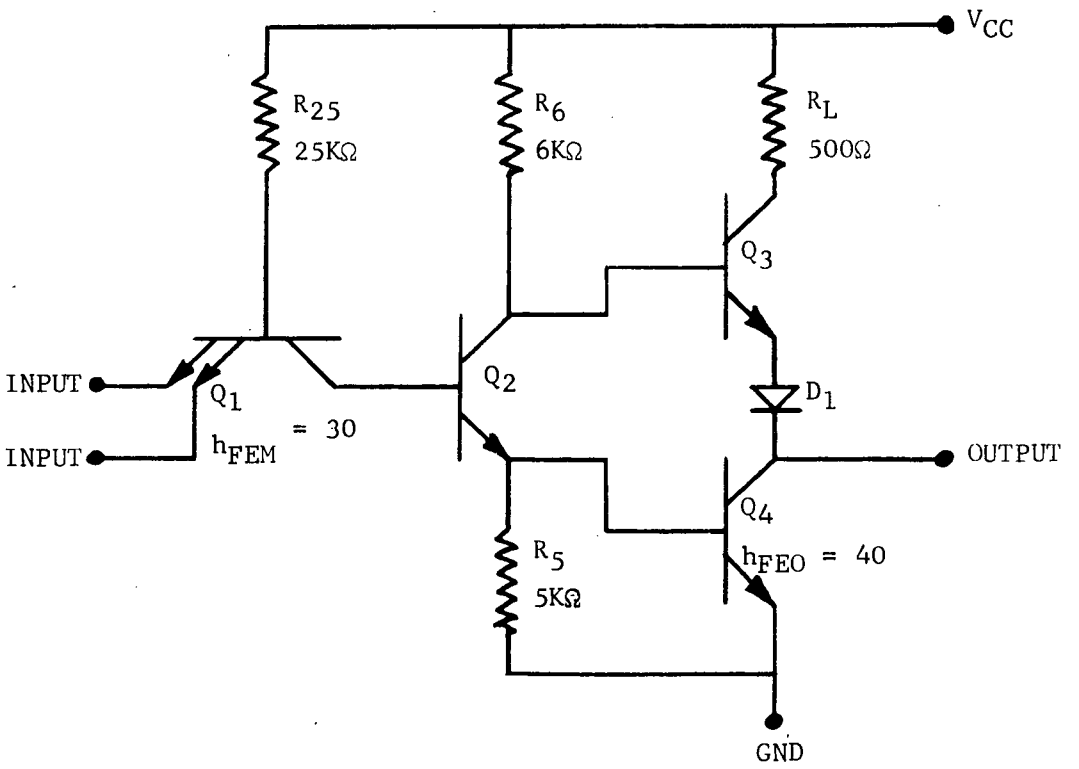
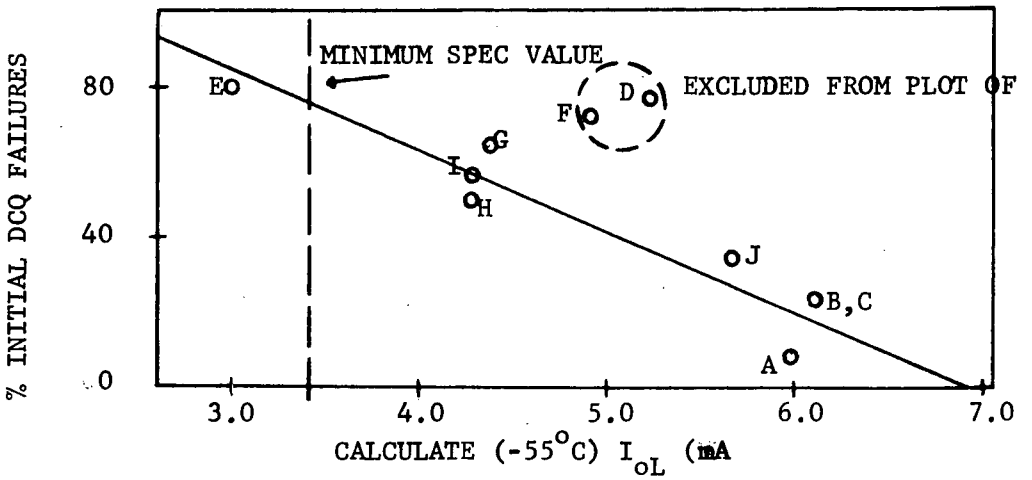


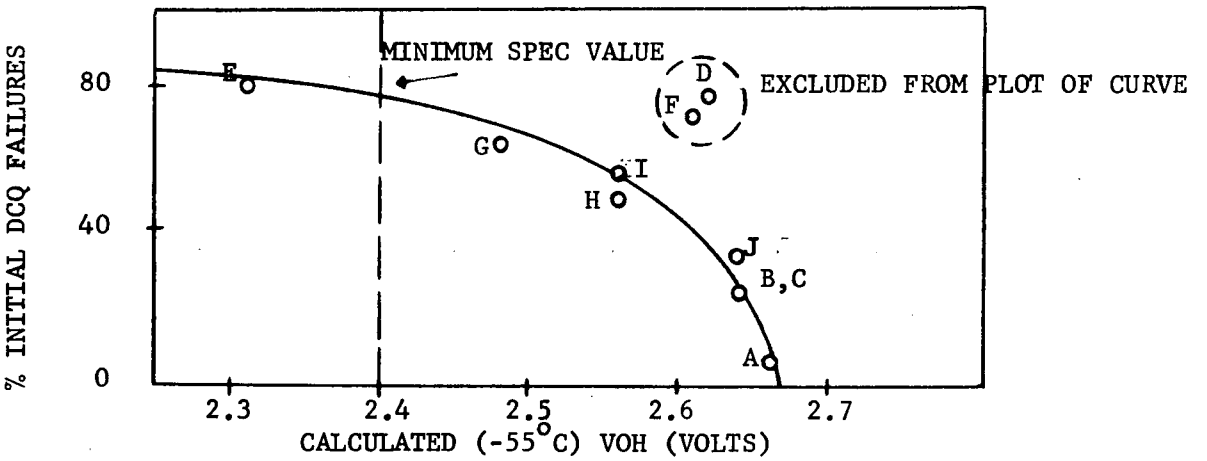
FIGURE 3.9 - BASIC DCQ CIRCUIT CELL, SHOWING NOMINAL DESIGN VALUES FOR THE INDIVIDUAL COMPONETS

MEASURED OR CALCULATED VALUES FROM BBTP2 DATA

LOT/WAFER	WAFER CODE	(MEAN) R_{25} (Ω)	R_6 (Ω)	R_5 (Ω)	R_L (Ω)	h_{FEM}	h_{FEO}	V_{SAT} (VOLTS)	V_{BE} (VOLTS)
33/15	A	29K	7.0K	5.8K	580	25	23	.135	.8
35/9	I	30K	7.2K	6.0K	600	16	17	.15	.8
35/12	H	28K	6.7K	5.6K	560	13	16	.13	.8
38/3	E	38K	9.1K	7.6K	760	17	17	.20	.87
38/7	F	35K	8.4K	7.0K	700	15	23	.14	.81
38/8	G	28K	6.7K	5.6K	560	15	17	.20	.84
39/12	J	36K	8.9K	7.2K	720	25	27	.11	.8
39/13	B+C	33K	7.9K	6.6K	660	24	27	.14	.8
39/14	D	41K	9.8K	8.2K	820	34	28	.11	.78

TABLE 3.14 -MEAN RESISTOR & TRANSISTOR PARAMETERS AS DETERMINED FROM BBTP2





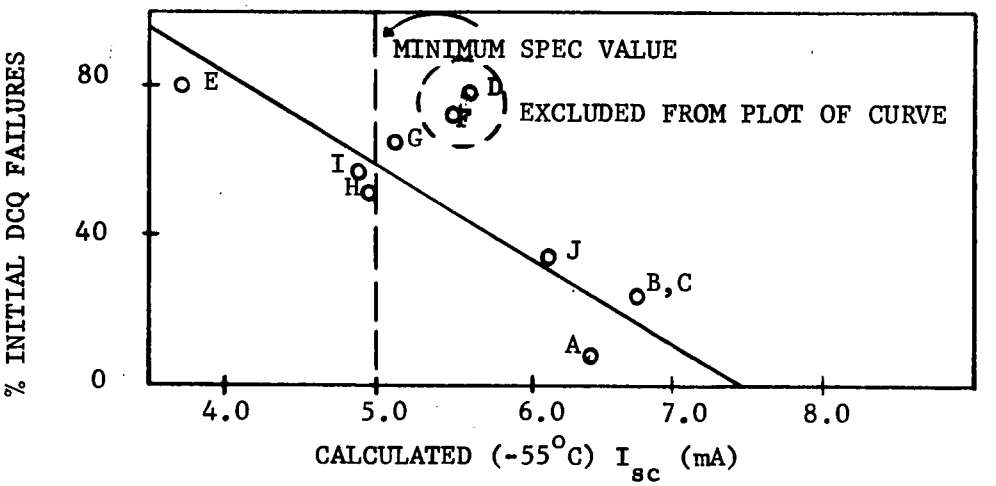
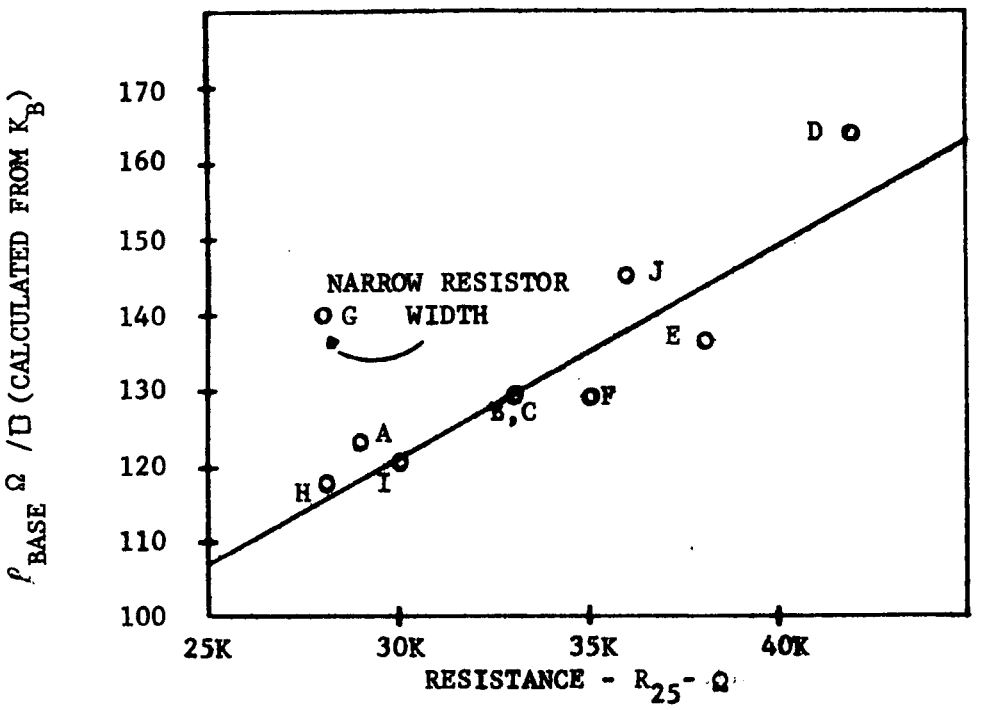


FIGURE 3.10 DCQ PARAMETER VALUES AT -55°C
(CALCULATED FROM BBTP2 DATA)



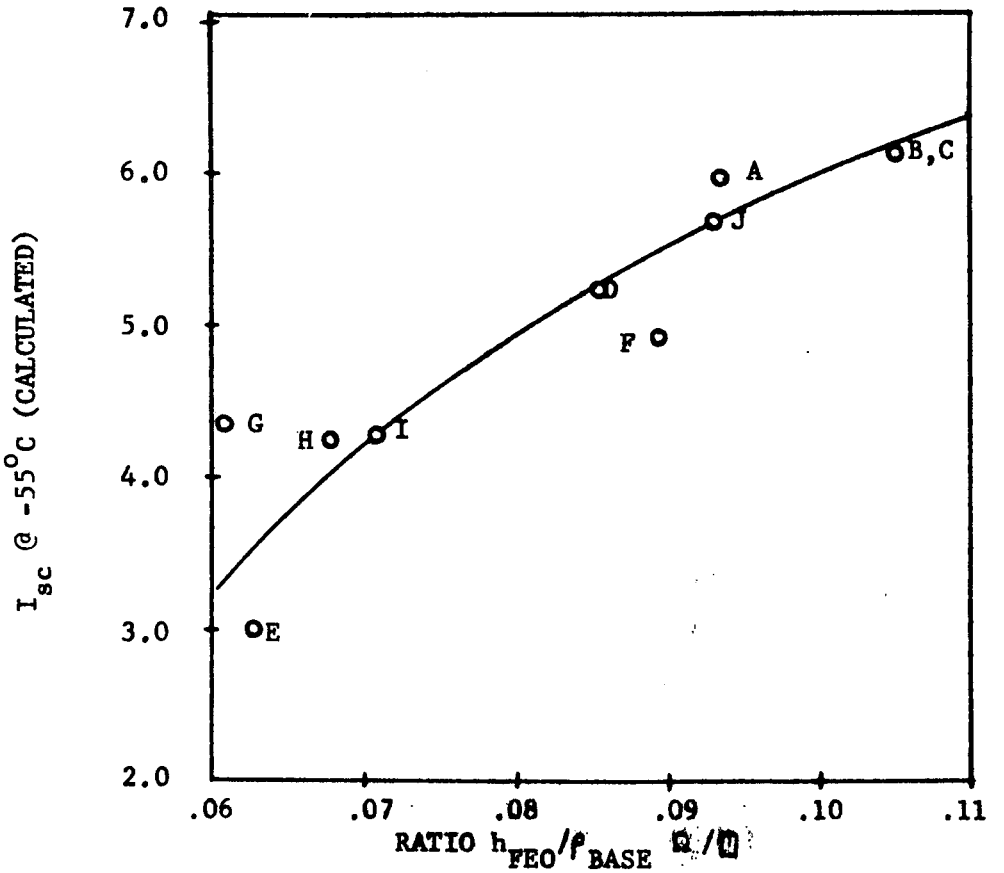


FIGURE 3.11 - BASE SNEET RHO vs R_{25} AND I_{sc} vs h_{FEO}/P_{BASE}

3.3.4 Correlation of BBTP1 Data With The DCQ Failure Rate

The mean thickness and width values obtained for the metalization and oxide integrity structures of BBTP1 are summarized in Table 3.5. Plots showing the relationship of this data are given in Figure 3.12, and from this plot certain factors are readily discernable:

a. The ratio of vapox dielectric thickness to bottom layer metalization thickness is greater than unity only for wafers A, B, C, and D.

b. A large variation in top layer metal thickness exists, ranging from 25K to 13.7K, but the metal thickness is in all cases thicker than the vapox dielectric.

c. The variation in vapox dielectric thickness is large, ranging from 10K to 6K.

Because the top layer metal is always thicker than the vapox dielectric, there should be no difficulty with open top layer metalization, and because the cross sectional area of the top layer metalization is in always greater than the bottom layer metal cross section any electromigration problems should be associated with the bottom layer metalization patterns.

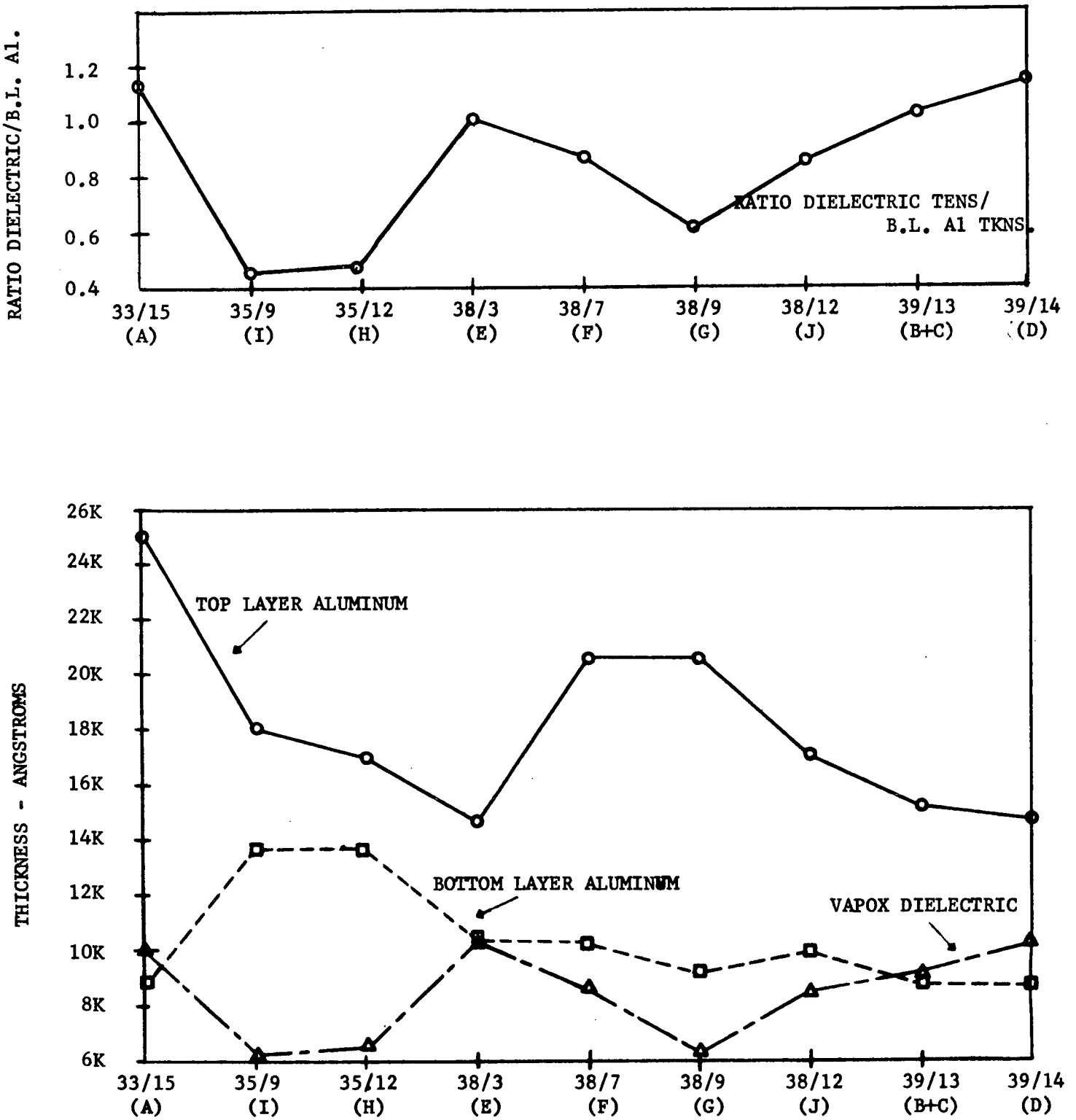


FIGURE 3.12 - RELATIONSHIP OF METALIZATION TO OXIDE LAYER THICKNESS

Problems can be expected at the points where the top layer metalization crosses the bottom layer metalization if the bottom layer metalization is thicker than the vapox dielectric layer and the bottom layer metalization does not have sufficient taper to insure good dielectric coverage. Significantly the devices which exhibited the highest yield and the best screening and life test reliability were devices from wafers A, B, and C, and these wafers all exhibit dielectric/bottom layer metal ratios greater than unity, and the best range for the -55°C values for I_{SC}, I_{OL} and V_{OH} based on the evaluation of the BBTP2 data. Wafer D also has a dielectric/bottom layer metalization thickness greater than unity, but the evaluation of the BBTP2 data indicated that low h_{FE} and high base sheet rho this device would limit reliable operation at low temperature.

Figures 3.13 and 3.14 shows the relationship of the resistance of the R_{MBS} and the R_{MBPA} structures to the cross sectional area of the metalization stripes, and the relationship of the resistance of planar metalization stripes and of stripes of the same length which cross over oxide steps. In general, the measured resistance value correlates well with the cross sectional area and the resistance of the planar metalization stripes correlates well with the resistance of the metalization stripe over oxide steps with the planar stripe exhibiting the anticipated smaller resistance value. The increase in resistance for the metalization stripes over oxide steps is attributed to the reduction in cross sectional thickness of the stripe at the oxide steps.

Figure 3.15 shows good correlation between the failures observed at wafer mapping and at the post encapsulation measurements for the test structures of BBTP1. This data indicates that problems can be expected at contact cuts because of the high percentage of failures observed for structure R_{MCC} during both the wafer mapping and the post encapsulation electrical testing.

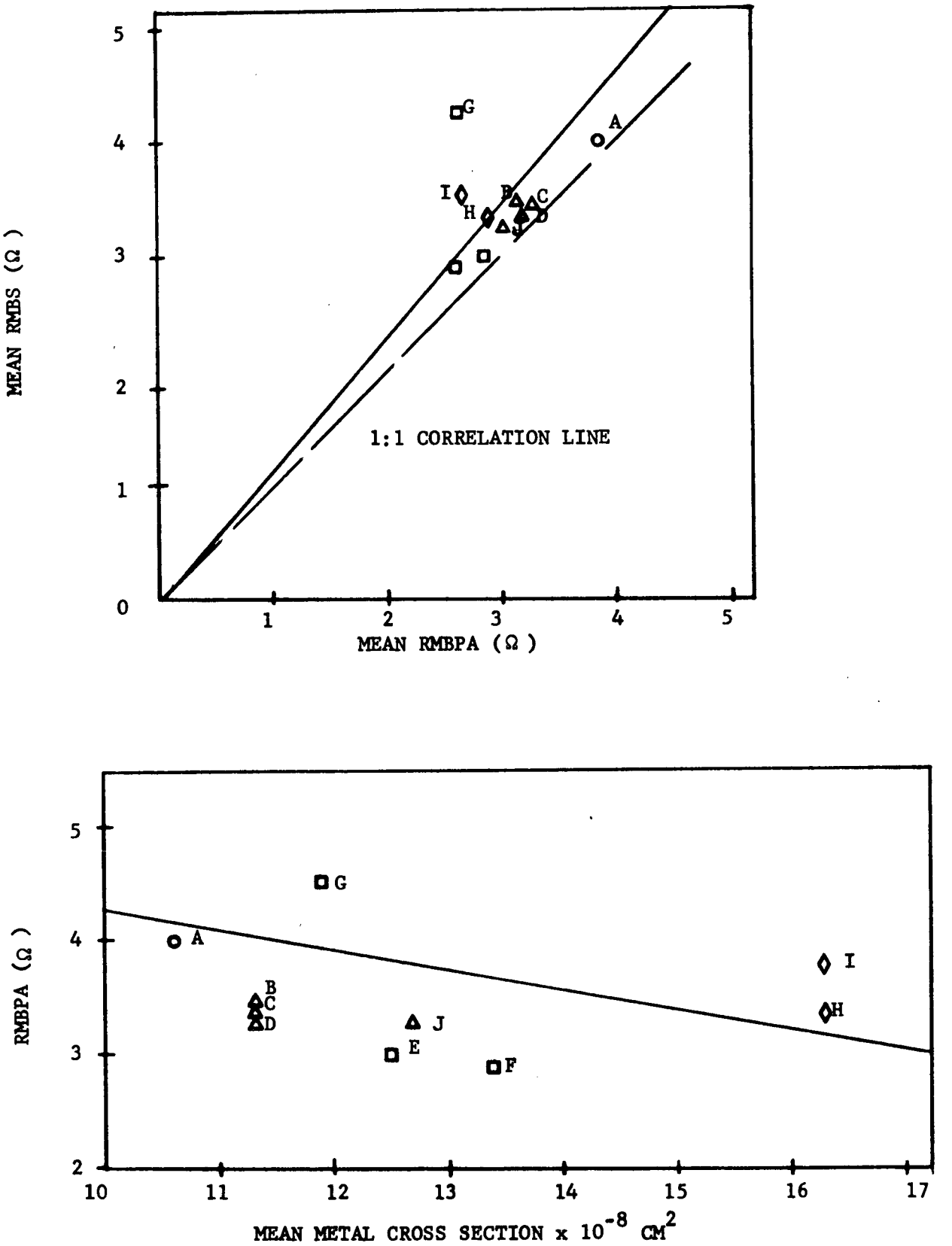


FIGURE 3.13 - METAL CROSS SECTION vs RESISTANCE FOR BOTTOM LAYER ALUMINIM STRIPES

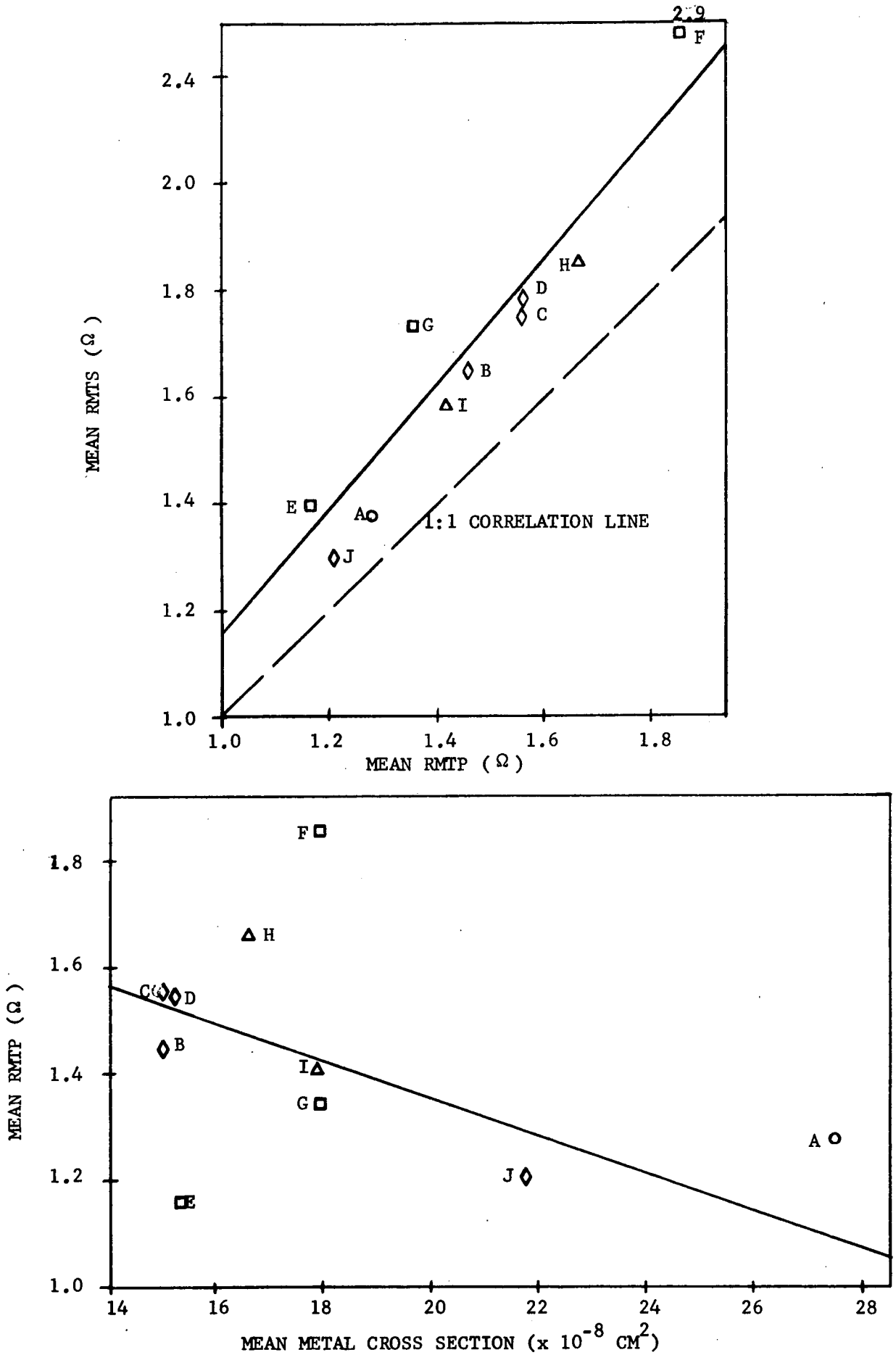


FIGURE 3.14 - METAL CROSS SECTION vs RESISTANCE FOR TOP LAYER ALUMINIM STRIPES

F

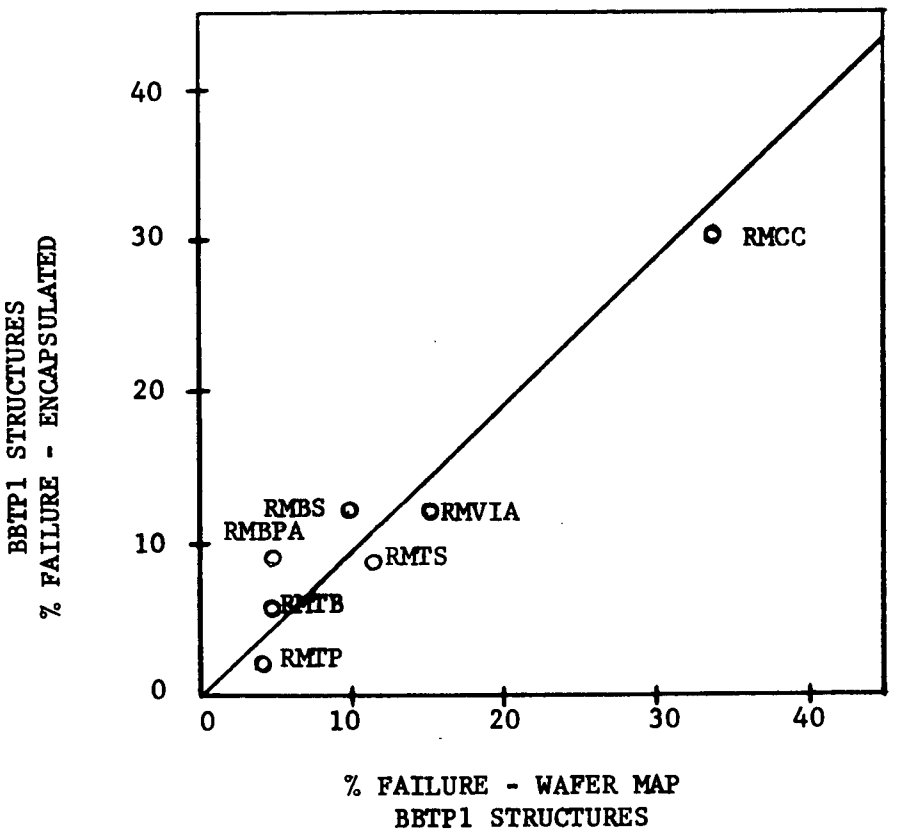


FIGURE 3.15 - CORRELATION OF WAFER MAP AND POST ENCAPSULATION FAILURE PERCENTAGES FOR BBTP1 STRUCTURES

Table 3.15 is a composite of Tables 3.4 and 3.6, but excludes from the failure count any failure of structures located near the edge of the wafer during the wafer map measurement because of high probability of damage during handling and the failure of any structure with microscopically visible damage. The quantity of failure by wafer, relative to the other wafers in this group is presented in Table 3.15.

From the relative quantity of failures, wafer A presents the fewest metalization and/or oxide integrity risks. Wafers B, C and H present moderate metalization and oxide integrity risks, but examinations of the data in Table 3.15 shows that the metalization failure quantities subsequent to encapsulation are quite small for wafers B and C. This could indicate that the wafer mapping measurements were improperly performed, but wafers B and C were originally a single wafer (39/13) which was broken approximately in half during processing. For the wafer map measurements, both pieces were matched together and treated as a single wafer; in all subsequent operations the original 39/13 wafer was treated as two seperate wafers (B and C). The high quantity of failures in wafer B+C at wafer mapping is therefore most probably due to increased damage of the peripheral chips because of handling of the broken wafer. The small quantity of failures subsequent to assembly infers that the damaged peripheral chips were not assembled and that the metalization patterns present low reliability risks.

Wafer D presents a low metalization reliability risk, but the oxide integrity risk is high. Wafer I presents a moderate metalization risk, but a high oxide integrity risk, and wafers E, F, and G present high metalization and oxide integrity risks. Additionally the analysis of the bulk pattern data from BBTP1 indicated that wafers D, E, F, G, H, I and J presented low temperature operation risks.

RESISTIVE STRUCTURES FAILURES

LOT/WAFER	WAFER CODE	N (APPROX.)	R_{MBPA}	R_{MVIA}	R_{MBPS}	R_{MTB}	R_{MTP}	R_{MTS}	R_{MCC}	R_{MBS}	TOTALS
33/15	A	12/6	0/1	-	-	-	-	-	-	1/0	1/1 = 2
35/9	I	12/6	-	-	-	-	1/0	2/0	1/0	-	4/0 = 4
35/12	H	12/6	-	-	-	-	1/0	1/0	3/0	-	5/0 = 5
38/3	E	12/6	-	2/0	-	1/0	-	-	8/4	-	11/4 = 15
38/7	F	12/6	-	-	-	-	-	1/3	-	2/0	3/3 = 6
38/8	G	12/6	-	2/0	-	-	-	-	5/6	1/0	8/6 = 14
39/12	J	12/6	1/0	1/0	-	-	-	-	2/0	2/0	6/0 = 6
39/13	B+C	12/12	-	2/0	1/2	1/0	-	-	1/0	1/0	6/2 = 8
39/14	D	12/6	-	-	-	-	-	1/1	-	-	1/1 = 2
TOTALS			1/1	7/0	1/2	2/0	2/0	5/4	10/10	7/0	45/17

CAPACITOR STRUCTURES FAILURES

LOT/WAFER	WAFER CODE	N (APPROX.)	CVP34	CVI56	CIP47	CTI67	TOTALS
33/15	A	4/6	-	0/1	1/0	0/1	1/2 = 3
35/9	I	4/6	1/3	2/5	0/1	1/2	4/11 = 15
35/12	H	4/6	1/1	2/2	0/0	1/1	4/4 = 8
38/3	E	4/6	2/2	3/4	1/1	0/2	6/9 = 15
38/7	F	4/6	0/5	3/6	0/1	1/1	4/13 = 17
38/8	G	4/6	1/4	3/5	0/1	1/0	5/10 = 15
39/12	J	4/6	1/0	2/2	0/1	1/2	4/5 = 9
39/13	B+C	4/12	0/5	0/5	0/4	0/4	0/18 = 18
39/14	D	4/6	1/2	2/5	0/1	1/4	4/12 = 16
TOTALS			7/22	17/35	2/10	6/17	32/84

NOTE: THE FAILURE SYMBOLISM X/X INDICATES:

FAILURES AT WAFER MAP/FAILURES AT FIRST POST ENCAPSULATION TEST

DEVICE FAILURES AT THE EDGE OF THE WAFER & VISUALLY DEFECTIVE DEVICES ARE NOT INCLUDED.

TABLE 3.15 - FAILURE SUMMARY BBTP1 - EXCLUDING PERIPHERAL DICE FAILURES

Based on the foregoing, the minimum risk metalization and oxide integrity wafers are A, B and C. Consideration of the oxide thickness data presented in Figure 3.12 and in Table 3.5, shows that the metalization patterns have reasonable thickness, and the dielectric thickness/bottom layer metal thickness ratio is greater than unity. The only other wafer for which the dielectric/bottom layer metal thickness ratio was greater than unity was wafer D. As previously pointed out, wafer D represented a high oxide integrity risk and exhibited poor low temperature characteristics based on the evaluation of the data from BBTP2. A summary of the metalization and oxide reliability risks on a wafer by wafer basis is presented in Table 3.16.

That wafer D exhibited a poor oxide integrity risk can be explained on the basis of test data taken during in-house evaluations of the bilayer metalization system during the early part of 1971 by the Process Development Laboratory of the Microelectronics Division. These evaluations were prompted by a high incidence of bottom to top layer metalization shorts and consisted of a Talysurf determination of the surface condition of the bottom layer metalization prior to dielectric deposition and a second Talysurf determination of surface conditions subsequent to dielectric deposition. A Talysurf scan of the bottom layer aluminum, across the entire BBTP1 chip at right angles to the interdigitated fingers of the capacitor structures was performed, these wafers were then coated with various thicknesses of vapor deposited phosposilicate glass according to the DCQ processing specifications and the second Talysurf/scan was made across the vapox dielectric in the same general area as the scan made across the bottom layer metalization. It was found that the hillocks present in the bottom layer aluminum subsequent to delinations were propagated in the vapor plated dielectric and that peaks in the glass could be from 10 to 20 times as high as the original hillock in the metalization, depending on the thickness of the glass layer.

WAFER	RELIABILITY RISK RESISTOR STRUCTURES LOW	MODERATE	HIGH	RELIABILITY RISK CAPACITIVE STRUCTURES LOW	MODERATE	HIGH	DIELECTRIC THICKNESS KÅ
A	X	-	-	X	-	-	10.0
I	-	X	-	-	-	X	6.1
H	-	X	-	-	X	-	6.5
E	-	-	X	-	-	X	10.3
F	-	-	X	-	-	X	8.9
G	-	-	X	-	-	X	6.3
J	-	X	-	-	X	-	8.5
B+C*	-	X	-	-	X	-	9.2
D	X	-	-	-	-	X	10.3

*NOTE:

THE SAMPLE SIZE OF B+C IS GENERALLY TWICE THE SAMPLE OF ANY OF THE REMAINING WAFERS BECAUSE THIS WAFER WAS BROKEN AND EACH HALF WAS TREATED AS AN INDIVIDUAL WAFER SUBSEQUENT TO ENCAPSULATION.

TABLE 3.16 - SUMMARY OF RELATIVE RELIABILITY RISKS FOR METALIZATION AND OXIDE LAYERS

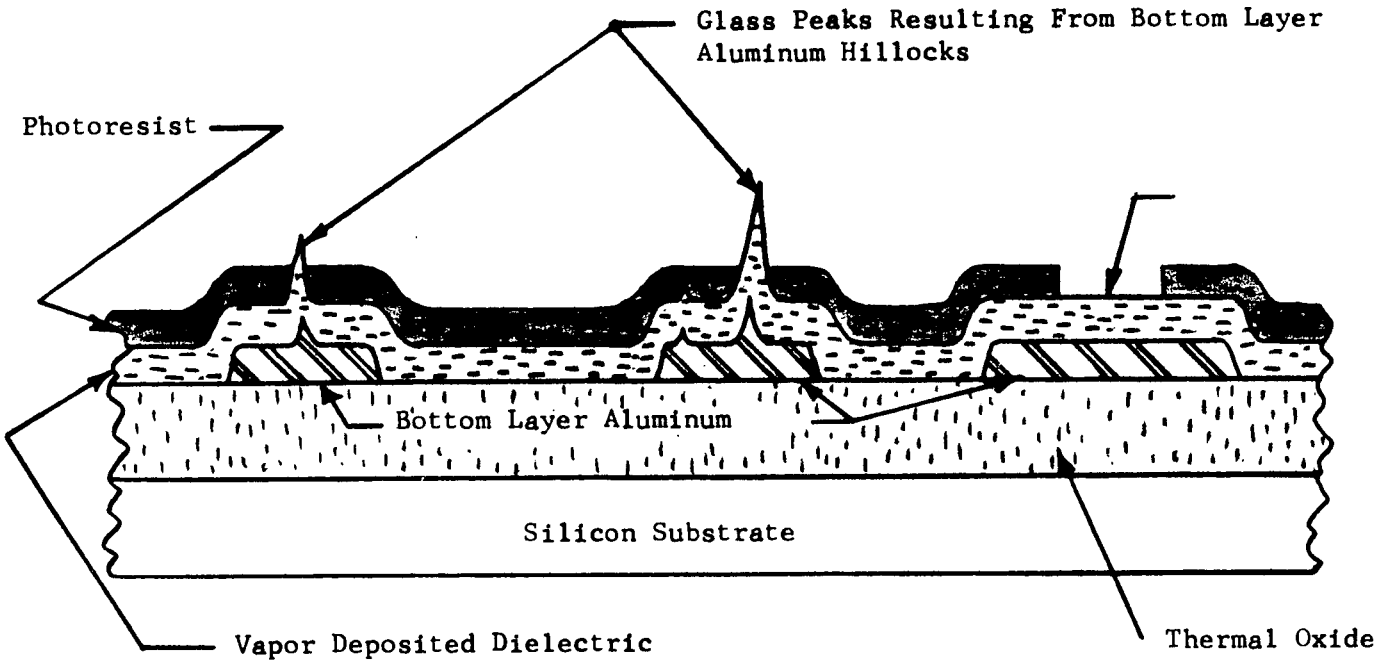
The high glass peaks are the result of the increased growth ratio of the glass at peaks and sharp corners. If the glass peaks are higher than the thickness of the photoresist layer used to delineate the via cuts, the via cut etch will also etch through the dielectric layer at these points and can result in top to bottom layer metalization shorts subsequent to top layer metalization. The mechanism involved is illustrated in Figure 3.16. Table 3.17 presents the data taken during the evaluation, and indicates that the density of peaks greater than a given height increases with vapor deposited glass thickness.

Referring to the summary of reliability risks of Table 3.16, it is observed with the exception of wafer F that the high oxide risks were associated with those wafers that had either relatively thin or relatively thick dielectric layers. The high incidence of shorts associated with the thick dielectric glass layers is attributed to the glass peak phenomena, the shorts associated with the thin dielectric layers are attributed to inadequate oxide coverage at the edge metalization stripes.

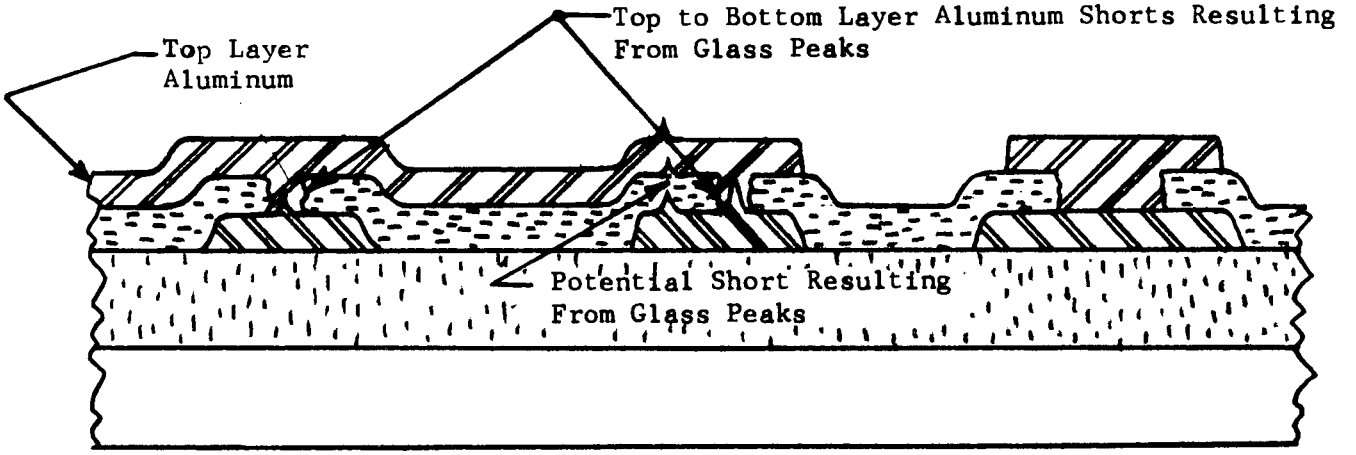
It should also be pointed out that subsequent to the initial testing of the capacitor structures only two additional failures were incurred on the BBTP1 vehicles subjected to the thermal stress screening. (See Table 3.7). This data infers that if the capacitor structures from a given wafer exhibit good initial test data, oxide integrity will not present a reliability problem.with the functional devices from that wafer.

As has been stated several times the DCQ devices from wafer A exhibited the best reliability throughout the Phase 3 evaluation. In addition to the data already discussed, the test patterns of wafer A also exhibited other good characteristics not evident to the same degree in the remaining wafers. They are:

a. Wafer "A" exhibited the best conformance to the emitter contact



CROSS SECTION SUBSEQUENT TO PHOTORESIST STEP SHOWING GLASS PEAKS NOT PROTECTED BY THE PHOTORESIST LAYER.



CROSS SECTION SUBSEQUENT TO TOP LAYER METALIZATION STEP SHOWING SHORTS RESULTING FROM VAPOR DEPOSITED GLASS PEAKS.

FIGURE 3.16 - ILLUSTRATION OF MECHANISM RESPONSIBLE FOR TOP TO BOTTOM LAYER ALUMINUM SHORTS AS A RESULT OF ALUMINUM HILLOCK PROPAGATION THROUGH VAPOR DEPOSITED DIELECTRIC LAYER

WAFER	BOTTOM LAYER METAL THICKNESS Å	NO. OF HILLOCK HIGHER THAN 5000Å	VAPOR DEPOSITED GLASS THICKNESS	NO. OF GLASS PEAKS HIGHER THAN 5000Å
1	10,500	0	6,500	2
2	10,100	0	8,200	12
3	9,300	0	10,600	15
4	9,200	0	12,700	20

TABLE 3.17 - SUMMARY OF DENSITY OF HILLOCK AND GLASS PEAK HIGHT AS A FUNCTION OF DIELECTRIC & BOTTOM LAYER METALIZATION THICKNESS

cut design. The design contact cut size is 0.25 X 0.25 mils, and they appeared reasonably square and of approximately the correct size on the multi-emitter transistor structure of BBTP2. The emitter contact cuts on the devices from most of the other wafers were generally small and considerably rounded rather than square as designed. It should also be stated that the 0.5 X 0.5 mil squares of the checker board alignment, a size monitor was not effective in determining whether good contact cut size had been achieved.

b. The bottom layer metalization taper on wafer A exhibited a greater degree of taper than the devices from the remaining wafers. The approximate horizontal distance from the edge of the metalization to the point where the taper intersected the tap surface of the bottom layer metalization pattern was approximately 0.15 mils for wafer A, approximately 0.12 mils for wafer E, approximately 0.10 mils for wafers H and I, approximately 0.08 mils for wafers J, B and C, and approximately 0.07 mils for wafers D and G.

3.3.5 Correlation of DCQ Failures With DCQ Test Data

Figure 3.17 shows the visual yield by visual category vs the functional die sort yield for each of the DCQ wafers. Regardless of the functional die sort yield, the visual yield by visual category is essentially constant. Figure 3.18 shows the final test electrical yield by visual category vs the functional die sort yield for each of the DCQ wafers. On a wafer by wafer basis, the high yield die sort wafers are also the wafers that exhibited a high final test yield (D.C. + Functional subsequent to encapsulation). Additionally there is no significant difference in the slope of this plot for the Class A or the Class B devices, but the Class R devices show a larger slope than the Class A and B devices indicating that the preseal visual inspection does remove some of the devices which present reliability risks. The calculated slopes for these plots are:

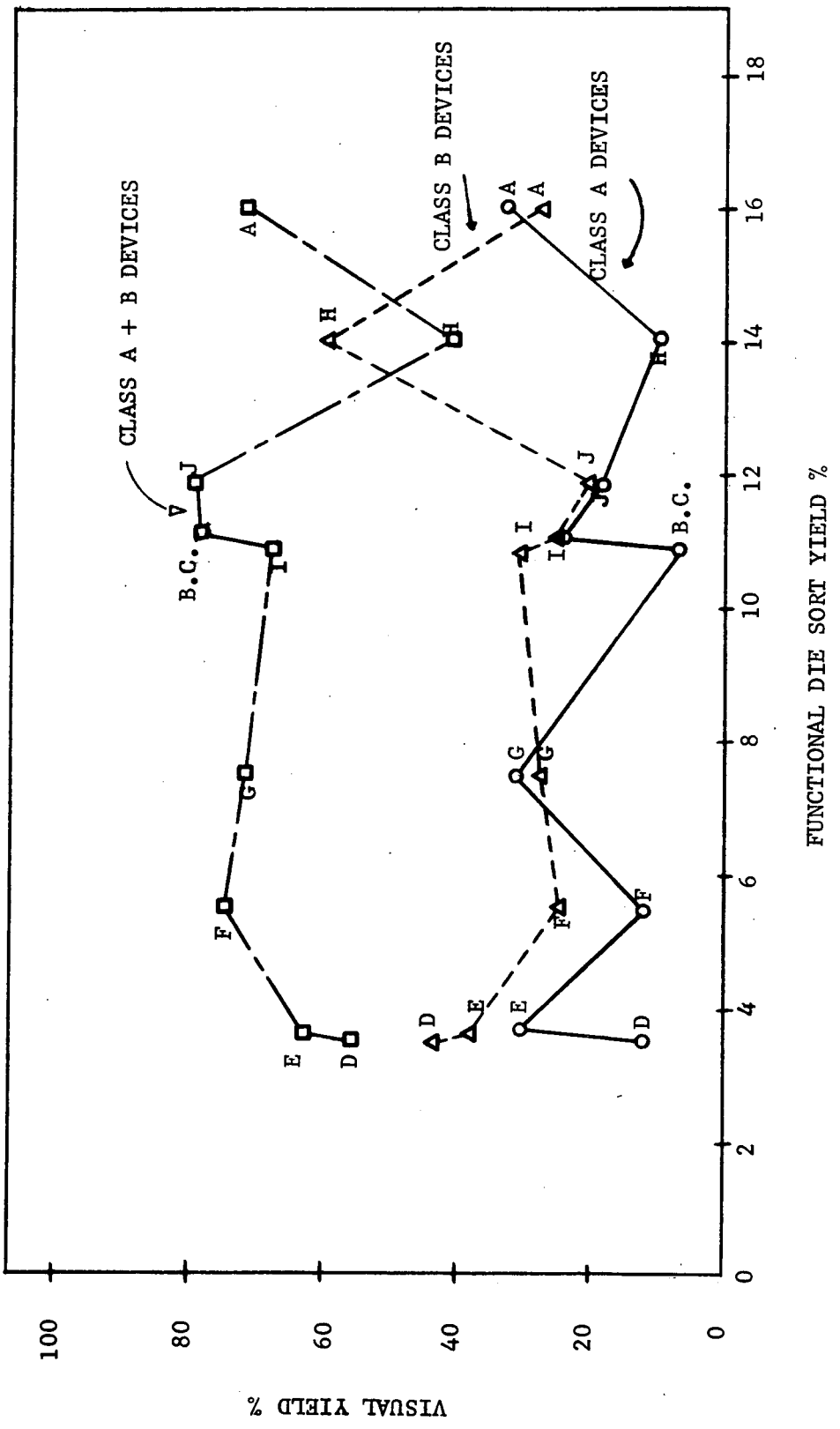


FIGURE 3.17 - VISUAL YIELD vs FUNCTIONAL DIE SORT YIELD

VISUAL CATEGORY	SLOPE $\frac{\%\ \text{FUNCTIONAL DIE SORT YIELD}}{\%\ \text{FINAL TEST YIELD}}$
A	0.16
B	0.16
R	0.24

Of significance in these plots is that Wafer A exhibited the best Class A and B yield during both the functional and the final electrical test, but the Class R devices from Wafer A had a zero final test yield.

Table 3.2 shows the quantity of devices which failed the arbitrarily established electrical screening parameter limits and indicates the quantity of devices which failed these limits that also failed during subsequent testing. These failures, by visual category are listed below:

	FAIL ELECTRICAL SCREENS		FAIL SUBSEQUENT TESTS	
VISUAL CLASS	n	S/N's	n	S/N's
A	2	F24, J32	2	F24, J32
B	5	C6, E3, F8, J21, J36	1	E3
R	3	H1, H8, I8	3	H1, H8, I8
TOTALS	10		6	

The electrical screens were at least partially effective in removing devices which were reliability risks, and moreover only one of the devices (S/N: J32, Class R) was a catastrophic failure.

Six Class B devices failed the hermeticity screen imposed but none of these devices failed during subsequent testing.

Table 3.18 shows the percentage of failures by visual class and wafer that failed initially (1st post encapsulation electrical test) and percentage of failure, of the devices which survived the initial test, by visual class and wafer through the screens and the life test. Figure 3.19 shows this data plotted for visual Class A and B combined and for all visual classes combined. Individual plots

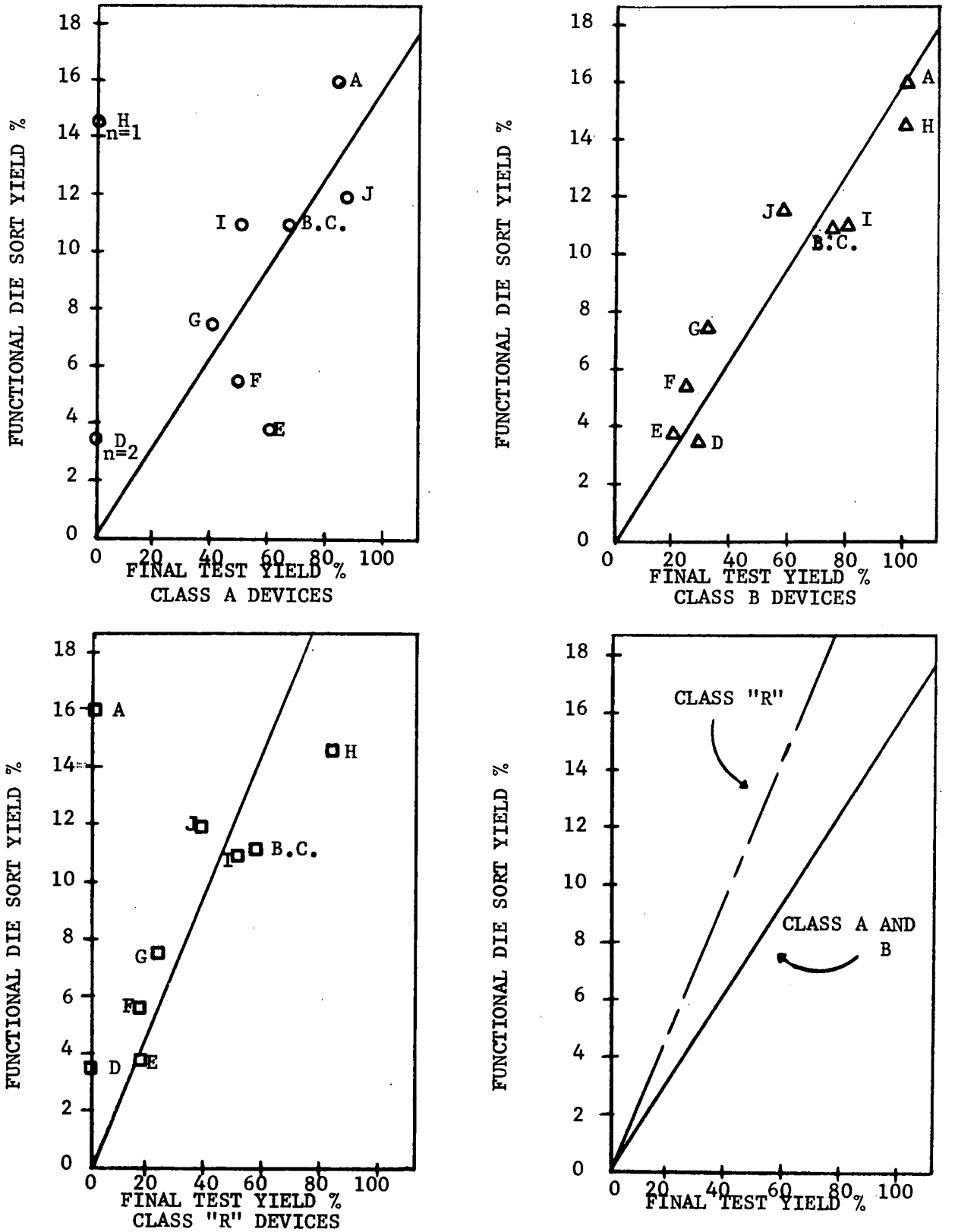


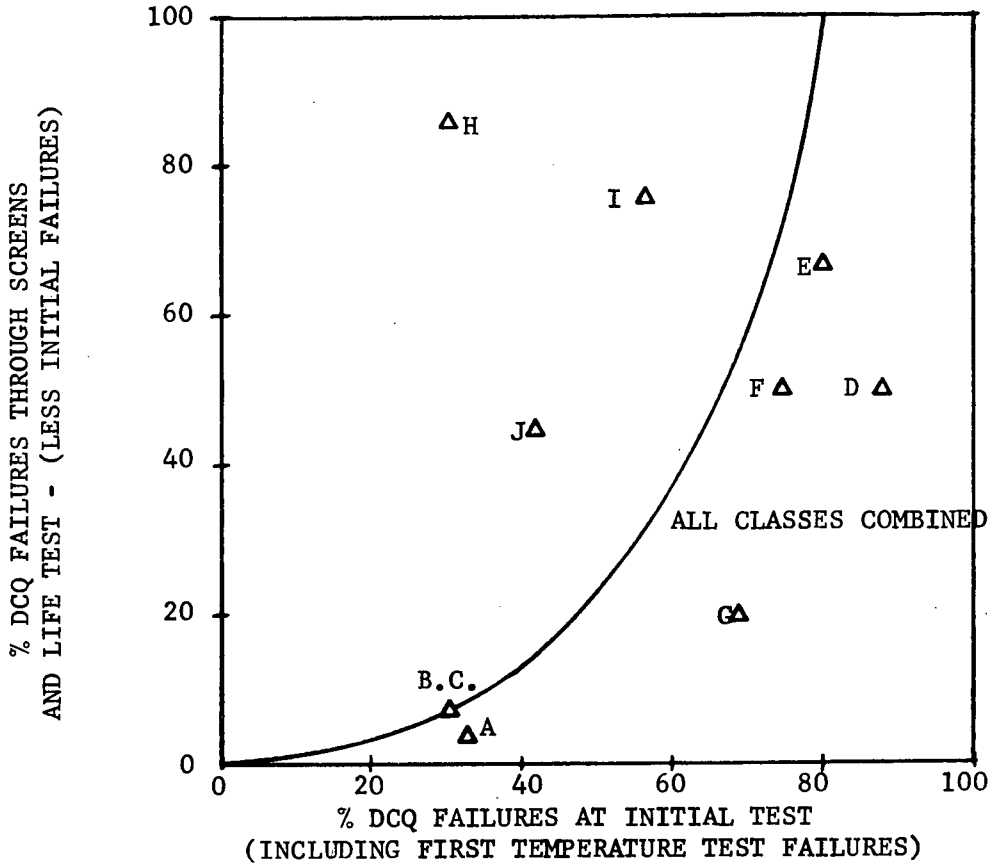
FIGURE 3.18 - FUNCTIONAL DIE SORT vs FINAL TEST YIELDS

INITIAL TEST

(LESS SUBSEQUENT HERMETICITY AND INCLUDING FIRST TEMPERATURE TEST FAILURES)

		CLASS A		CLASS B		CLASS R		CLASS A+B		TOTAL ALL CLASSES	
LOT/WAFER	WAFER CODE	FAILURE/SAMPLE	% FAILURE	FAILURE/SAMPLE	% FAILURE	FAILURE/SAMPLE	% FAILURE	FAILURE/SAMPLE	% FAILURE	FAILURE/SAMPLE	% FAILURE
33/15	A	2/12	16	0/14	0	10/10	100	2/26	8	12/36	33
35/9	I	1/2	50	3/5	60	1/2	50	4/7	57	5/9	56
35/12	H	1/1	100	1/3	33	1/6	17	2/4	50	3/10	30
38/3	E	3/5	60	5/5	100	5/6	83	8/10	80	13/16	80
38/7	F	1/2	50	12/16	75	5/6	83	13/18	72	18/24	75
38/8	G	6/10	60	9/13	69	7/9	78	15/23	65	22/32	69
39/12	J	1/7	14	10/24	58	5/8	63	11/31	35	16/39	41
39/13	B+C	1/3	33	6/26	23	6/14	43	7/19	24	13/43	30
39/14	D	2/2	100	5/7	71	7/7	100	7/9	78	14/16	88
		THROUGH SCREENING AND LIFE TEST									
33/15	A	1/10	10	0/14	0	-	-	1/24	4	1/24	4
35/9	I	1/1	100	1/2	50	1/1	100	2/3	67	3/4	75
35/12	H	-	-	1/2	50	5/5	100	1/2	50	6/7	86
38/3	E	2/2	100	-	-	0/1	0	2/2	100	2/3	67
38/7	F	1/1	100	2/4	50	0/1	0	3/5	60	3/6	50
38/8	G	2/4	50	0/4	0	0/2	0	2/8	25	2/10	20
39/12	J	4/6	67	5/14	36	1/3	33	9/20	45	10/23	44
39/13	B+C	0/2	0	2/12	17	0/8	0	3/12	9	2/30	7
39/14	D	-	-	1/2	50	-	-	1/2	50	1/2	50

TABLE 3.18 - PERCENTAGE OF DCQ FAILURES INCURRED AT INITIAL POST SEAL ELECTRICAL AND THROUGH SCREENS AND LIFE TEST



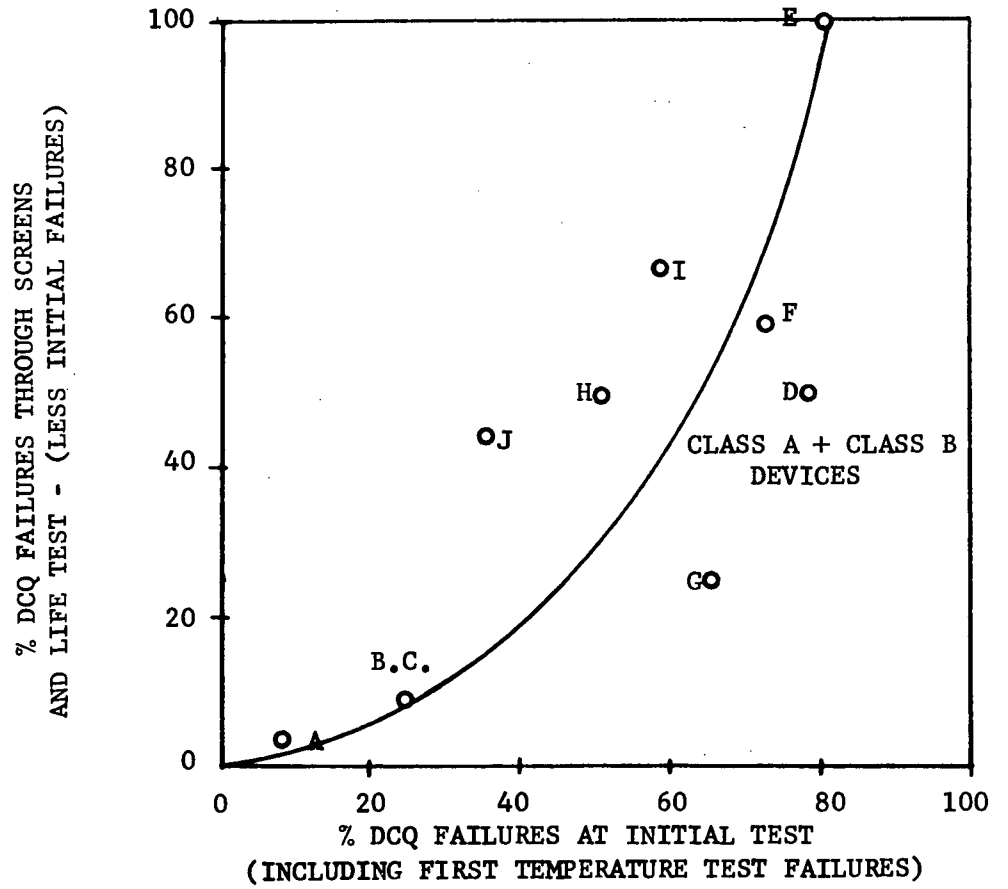
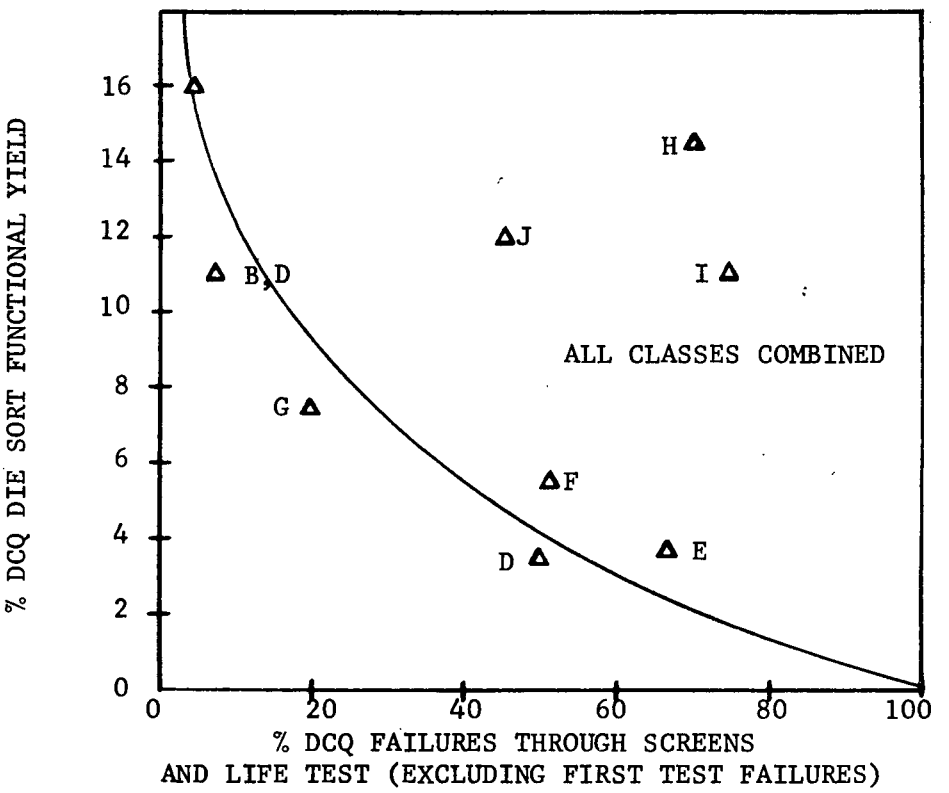


FIGURE 3.19 - INIDIAL vs SCREENING AND LIFE TEST FAILURE PERCENTAGE

for each visual class were not prepared because of the limited sample size of the Class A and Class R devices subsequent to the initial measurements. The significant feature of this plot is that it clearly depicts the relationship that exists between the percentage of initial failures and the percentage of failures, after the appropriate sample size reduction, of the devices which survived the initial test to fail during the subsequent screening and life testing. Based on the plots shown in Figure 3.19, wafers with a low final test yield can be expected to be less than reliable than devices with a high final test yield. Also comparison of the plot of the Class A and Class B devices with the plot for all visual classes shows that the slope $\frac{\%\text{FAILURES THROUGH SCREENS \& LIFE TEST}}{\%\text{ INITIAL FAILURES}}$ is greater for the plot of all classes combined which reflects the higher incidence of failure due to the Class R visual devices. This data infers that the visual reject devices, according to the preseal inspection criteria developed under this contract, are more susceptable to failure than the Class A and Class B devices. Figure 3.20 shows the percentage of failure through the screening tests and the life test plotted against the die sort functional yield for each wafer. The failure percentage for wafers H and J has been modified for these plots to exclude the three chip to header bond failure incurred on devices from wafer J and the cracked chip failure incurred on the device from wafer H, because these failures are mechanical and in no way related to the electrical measurements performed. Figure 3.20 shows a clear relationship on a wafer basis between the functional electrical yield at wafer mapping and the percentage of failures through screening and life test subsequent to the removal of the devices which fail the first post encapsulation measurements. The inference that can be made from the plots is that poor yield wafers represent poor reliability risks, and that the probability of good reliability increases asymptotically as the die sort yield approaches 20%.

The correlation exhibited between the wafer mapping measurement and



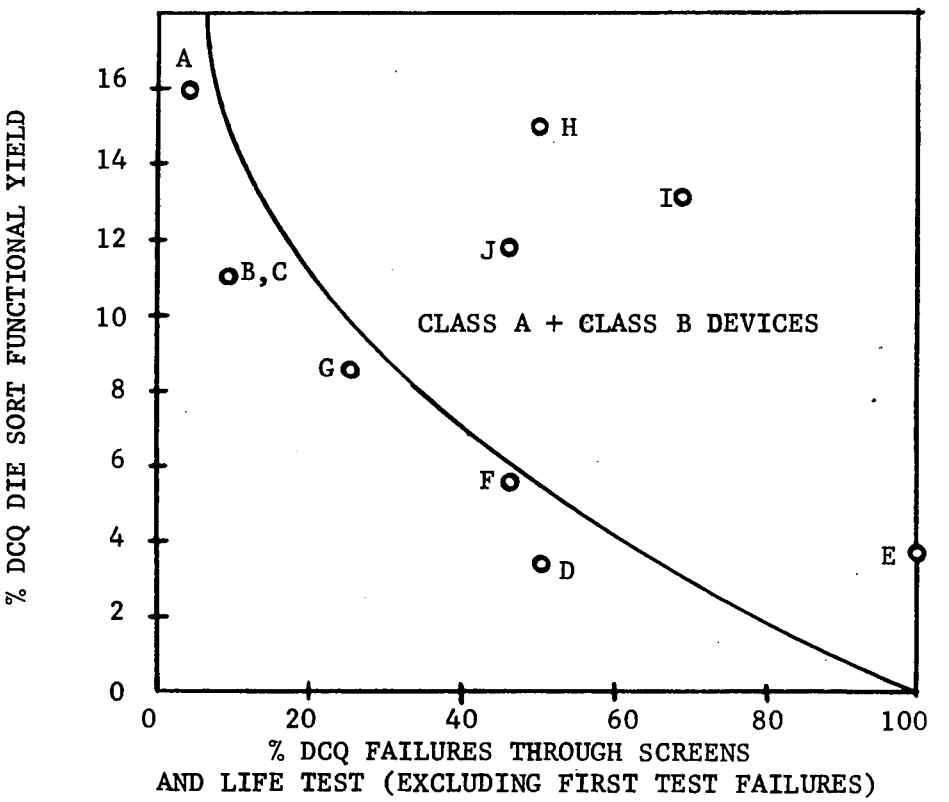


FIGURE 3.20 - DIE SORT YIELD vs SCREENING AND LIFE TEST FAILURE PERCENTAGE

the final test yield, and between the wafer mapping and/or final test yields and the screening and life reliability of the DCQ devices demonstrates that the ultimate reliability of a product is a stronger function of the processing variables than of the screens to which the product is subjected to remove potentially defective or reliability risk devices. The approach then to ultra high reliability then must be through stringent process control to insure that:

a. All individual component values fall within the limits defined by the worst case design equations,

b. Worst case metalization cross-sections are of sufficient area to insure they can conduct, without damage or degradation, the current it will be required to conduct in use,

c. The integrity of the thermal and vapor deposited oxides is such that it is free from pin holes or thin areas to the extent shorts through the oxide layer will not occur during use, and the oxide layers will not crack during ambient or electrical thermal excursions,

d. The contact cut and via cuts are of sufficient size to insure adequate contact and are capable of conducting the worst case currents they will be required to handle,

e. All die to header bonds are essentially void free and will not fail under the imposition of thermal and or mechanical stresses,

f. All wire bonds are of sufficient size to retain reliable contact throughout high mechanical and thermal stressing, and the internal lead wires are of sufficient size to preclude the possibility of thermal fatigue during operation. Also the internal lead lengths must be controled to the extent that the wires will not be mechanically stressed during bonding, but neither will they be capable of shorting to each other or to the package containing the device.

g. The package containing the device must be hermetic, capable of adequate heat transfer and be able to withstand the thermal and mechanical stresses to which it will be exposed.

All manufacturers utilize process controls to insure that each processing lot has a reasonable assurance of meeting the reliability and performance characteristics required. However, bulk parameters are normally monitored with the use of a single monitor wafer inserted into the processing lot containing up to 20 wafers. It has been documented that dopant flow patterns, depletion of dopant supply, and the orientation of wafers in the diffusion tube can result in bulk resistivity differences among the wafers in a single diffusion lot depending upon where and how each wafer is oriented in a given diffusion tube. Moreover, on the material utilized for the fabrication of the bilayer-bipolar test vehicles for this contract, bulk resistivity gradients were observed across the diameter of the individual wafers as well as variations in the bulk resistivities of the individual wafers from the same diffusion lots. The utilization of test patterns incorporated into each wafer will permit accurate characterization of each wafer intended for high reliability utilization and insure that each wafer meets the design equation requirements to preclude the possibility of long term failure because of slight degradation of initially marginal bulk parameters. Additionally, since the test patterns will permit measurement of the bulk characterics after the completion of all processing, information can be obtained to insure that the bulk characteristics monitored early in the diffusion process, (i.e., epitaxial restivity, resistor sheet resistivities, etc.) are not modified during subsequent diffusion or drive in operations. Test patterns provide a means for monitoring metalization and oxide integrity on a wafer basis rather than on a lot basis as is normally performed, and they also provide a means for monitoring contact cut, and via integrity across the diameter of a wafer.

If the test patterns are assembled into the same package at the same time and with the same process as the functional devices, they should provide a means for the detection of faulty chip to header bonds. However, during the course of this contract, we experienced three DCQ chip to header bond failures but no chip to header bond failures of any of the test patterns. It is significant that two of the three chip bond failures were from lot J, the same lot that also experienced a DCQ failure because of a cracked chip. The only acceptable explanation for these failures, although somewhat speculative, is that the test patterns were not bonded at the same time and the bonding process was somewhat out of control at the time the bonds were made.

It is difficult to attribute the cause of the low temperature VOL failures to a single mechanism. The factors involved include:

a. Small input transistor contact cuts,

b. High resistor values,

c. Low initial h_{FE} values and evidence of about a 10% h_{FE} degradation during the stress evaluation of the input transistor contained on BBTP2.

The small emitter contact cuts on the input transistors, based on the wafer mapping data obtained from BBTP2 appear to predominate at the edge of each wafer. This is due to inadequate photoresist delineation near the wafer periphery of these wafers and the small contact cuts can become resistive resulting in an inadequate voltage at the input to drive the output transistor into saturation. The high resistor values are a function of two variables; high "p" diffusion sheet rho and inadequate resistor width at the periphery of the wafer resulting from deficient photolith delineation. The low initial h_{FE} values apparently resulted from insufficient emitter drive in as indicated by the relationships between the h_{FE}, the base resistance sheet resistivity, and the value of the base-emitter pinch resistor

values. (See Table 3.10.) The combination of low beta, high resistance values, beta fall off with temperature, and beta degradation can minimize the base drive to the output transistor sufficiently so that it will not go into saturation, the conditions required for a good VOL value.

We did not experience any DCQ failures during the screening or life testing because of open metalization patterns or because of oxide shorts in spite of the variation in metalization and oxide thickness as monitored with the use of the structures of BBTP1. However, based on the worst case current densities the device will experience in use, and on the electromigration rate data available at the time the device was designed in 1969, the PHILCO-FORD Microelectronics Division Circuit Design Group extrapolated the MTF* to electromigration failure at 75°C to be of the order of 10^8 hours. This illustrates the conservative design limitations placed on the metalization system of this circuit, and indicates that electromigration failures should not have been anticipated. Because of the metalization and oxide thickness variations initial failures because of inadequate metalization coverage at oxide steps, particularly in those wafers where the ratio of the dielectric layer to the bottom layer metalization layer thickness was less than unity should be expected. Figure 3.21 illustrates that those wafers with a poor dielectric/bottom layer metalization thickness ratio did experience a high percentage of failures at the initial measurements. The data from wafers D, E, F and G does not fit this plot well, but these wafers also contained individual eomponents with very poor electrical characteristics which could also contribute to failure. The stresses likely to accelerate the failure of metalization patterns at oxide steps are thermal shock, and high current density testing. The BBTP1 devices subjected to the thermal stress sequence did not experience a single failure during the course of the test. Failures were experienced during the electromigration stressing of the structures of BBTP1. This testing was performed by applying a constant

*Mean Time First Failure.

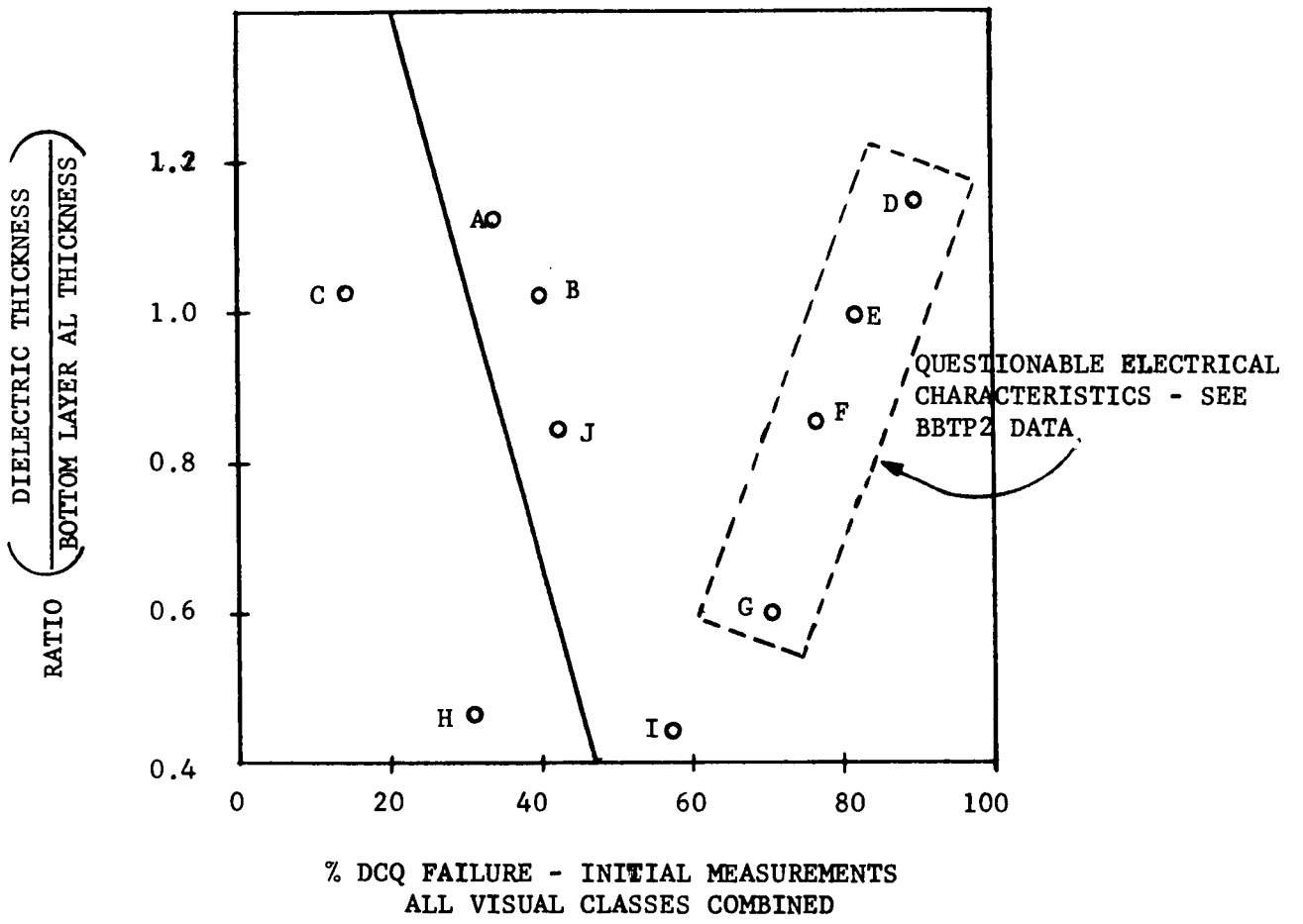


FIGURE 3.21 - INITIAL DCQ FAILURE PERCENTAGE vs DIELECTRIC/ALUMINUM RATIO

current to the metalization structure under test and the order in which failures were incurred was essentially according to cross sectional area as determined by the actual measurement of the structures, but the current density applied during these tests was substantially higher than experienced by the DCQ even under the stress operational test to which they were subjected.

Initial test capacitor structure failures were also incurred during the evaluation of BBTP1, but only two additional failures were incurred during the stress testing to which these vehicles were subjected. Concerning the initial capacitor structure failures, the highest percentage of failures were incurred on test structure CVI56, the interdigitated structure for the evaluation of the vapor plated dielectric. (See Table 3.6.) The high failure rate for this structure (71%) as compared to the planar structure CVP34 (39%) and the failure rate for the interdigitated thermal oxide structure CTI67, (32%) as compared to the planar thermal oxide structure CTP47 (17%) demonstrates that the periphery of the metalization is more susceptable to shorting than is the planar portion of the structure and the thermal oxide integrity is not as susceptable to failure as is a vapor deposited oxide layer. It must be remembered however, failure of the capacitor structures was defined as the inability of the structure to withstand an applied potential of 200 Volts, more than 20 times the maximum rated voltage of the DCQ devices. It should be reiterated however, that the capacitor structures of wafer A withstood the 200 V test quite well and the DCQ devices from wafer A experienced very few failures throughout the screening and life test sequence of the Phase 3 evaluation.

No DCQ internal bond wire failures were incurred during the Phase 3 evaluation, and the test structure of BBTP1 intended to evaluate bonding showed no degradation throughout the high stress screens to which they were exposed.

However, because each bond on an integrated circuit represents an individual assembly operation, each equally susceptable to operator error and failure, the wire and the chip bonds must be examined individually on each functional chip assembled. The test pattern structure will enable one to determine only if the bonding process is out of control, but will not detect individual processing defects.

A visual inspection must also be performed on each individual functional chip because localized defects can occur that would not be detected by test pattern data. During the course of this evaluation, the Class A visual devices did not perform any better than the Class B devices, but this is attributed to the fact that the types of defects for which the Class A visual inspection is more sensitive to did not occur. One of the areas in which the Class A visual specification was deficient however, was it accepted devices with contact cuts whose sides were no less than 0.75X the design size. This specification permits the designed 0.25 X 0.25 mil contact cut to be as small as 0.1875 X 0.1875 mils or a reduction in area from .0625 to 0.0352 square mils. Based on current technology the original specification is adequate for most contact cut sizes, but to insure the integrity of small emitter cuts, because we experienced problems in this area, the specification has been modified to set a lower limit on contact cut side lengths of 0.22 mils (minimum) for Class A devices. Also, because we experienced chip to header bond failures, the visual specification for chip bond acceptance has been tightened to reject all devices in which the resolidified eutetic is not visible along all four sides of the chip.

Package evaluations must obviously be performed on the package used for the device being qualified. All that is required in this area is that the packages tested be from the same lot material and they be assembled at with identical procedures, and be subjected to identical handling as the functional devices which they represent. Therefore, the packages used for the test patterns may be utilized

for this purpose, but since 100% environmental screening is required of the functional vehicles, the package evaluation might just as well be performed on the functional vehicles.

SECTION IV

BIPOLAR SCREENING PROCEDURE

4.1 GENERAL SCREENING PROCEDURE FOR BIPOLAR DEVICES

The recommended screening procedure for bipolar silicon semiconductor devices, based on the data collected during both the Phase 1 and the Phase 3 evaluations performed under this contract are contained in the following subsections. The procedure is intended to remove devices with highly time dependent failure mechanisms that are difficult to detect in a reasonable period of time. For this reason, the developed procedure incorporates the utilization of standard test pattern chips, containing individual test structures designed to be sensitive to potential failure mechanisms, that are interdispersed on the same wafer as the functional devices. The test structures are intended to improve the sensitivity of detection techniques for failure mechanisms that have been shown capable of escaping the best previously used practical screens. One of the advantages of the interdispersed test pattern approach is the individual test structures are exposed to the same diffusion, oxide growth and metalization processes as the functional devices and the data obtained from them permits an accurate assessment of potential failure mechanisms of any group of devices on a wafer basis. Additional advantages to the test pattern approach are:

a. Individual test structures can be subjected to stress levels not attainable in a functional integrated circuit because of the restrictions imposed by resistor values, interconnection configurations and thermal constraints. Stress testing of individual test structures can accelerate potential failure mechanism so that detection of the defect is possible in a reasonably short period as compared to the excessively long test periods that would be required if the functional integrated circuit device were operated at "in-use" conditions.

b. Test pattern chips can be designed to fit the grid pattern of all of the members of a integrated circuit family, and these test patterns can

be used to monitor these process on a step by step basis as well as providing the capability to minitor all processing parameters subsequent to the final processing operation. They therefore can be used to insure that the process is in control, and orginally "in-spec" diffusion parameters have not been inadvertently modified by subsequent processing operations to the extent that they can jeopardize reliability. Because utilization of a standard test pattern chip permits the characterization of the fundamental parameters of a family process, worst case design equations can be applied together with the test pattern data to insure that all individual functional family members, regardless of complexity, will meet their design requirements, on a wafer by wafer basis, as soon as the test pattern data is obtained.

The test pattern approach is generally applicable to all bipolar structures, although some modifications of the basic test structures may be required between the different families.

4.2 TEST PATTERNS

The utilization of standard test patterns however, supplements rather than precludes the 100% pre and post seal visual, electrical, mechanical, and thermal screen normally performed on integrated circuits because test patterns will not normally detect highly localized defects in areas not covered by the test structure. Examples of this type of defect includes:

a. Photolith defects,
b. Metalization scratches,
c. Diffusion defects, and
d. Oxide defects.

Test patterns may not detect individual processing step hazzards such as poor chip to header bonding, wire bonding, or package related defects. Therefore, 100% screening of the functional devices is also required to insure overall long term reliability.

Test pattern utilization should prove to be economical for both large and

small procurements. The additional costs involved include:

a. The design of a test pattern,

b. The step and repeat charges for interdispersing the test pattern into the master mask,

c. The generation of a test program for the individual structures,

d. The performance of the test program for the individual test structures,

d. The loss of some silicon wafer area that would normally be devoted to functional devices and

e. The cost of additional packages.

However items a. through c. are one time charges, the loss of silicon wafer area to test pattern is a small portion of the total wafer area, the performance of the test program can and the cost of additional packages will probably be offset by the savings incurred by rejecting wafers on the basis of the test pattern data prior to scribing thereby saving the assembly and test costs associated with functional devices that would subsequently be rejected.

When small procurements are involved, the one time charges can represent a significant portion of the overall cost of the devices, but the information obtained from the test patterns will offer insurance of adequate reliability that would cost a considerable amount if the reliability had been guaranteed with the use of additional functional test vehicles. When large procurements are involved the one time charges can be prorated over the entire procurement.

4.2.1 Bipolar Test Pattern Structures

The specified test pattern structures incorporated into each wafer, and tested as part of the Phase 1 and Phase 3 bilayer bipolar evaluation are described in detail in the Intermin Scientific Report on the Phase 1 - Bilayer Bipolar Evaluation Report and in the final draft of the Evaluation Plan, Bilayer Bipolar Devices. Both of

these documents were prepared under this contract and were dated September 1971. The structures described in these reports were adequate for the purpose of the functional devices studied under this contract, except the structure R_{MCC} contained 0.5 X 0.5 mil contact cuts instead of 0.25 X 0.25 mil cuts as used on the emitters of the multiple input transistors of the DCQ circuit and the evaluation of this structure yielded better results than were incurred on the small emitter contact cuts of the test transistor of BBTP2. The only other difficulty incurred with the test pattern structures was that structures R_{25}, R_B, and R_{BP} of BBTP2 were contained in a single isolation bucket and utilized a common ground buss. Because of this difficulty the ground buss had to be cut prior to the measurement of these structures to preclude the parallel measurement of these structures.

4.3 SPECIFIC SCREENING PROCEDURE FOR BIPOLAR DEVICES

The recommended screening procedure for bipolar devices is shown in Figure 4.1. The procedure is shown in the general form so that it is applicable to all types of bipolar circuits rangeing from high to lot resistivity substrate material. Specific recommendations are made for the rejection of devices and/or wafers based on their ability to meet the specified criteria at all test points throughout the screening procedure.

4.3.1 Test Pattern Design

The design of the test pattern chip must take into consideration the family for which the individual test structures are intended to evaluate. Digital type integrated circuits are normally diffused into low resistivity (0.5Ω-cm) substrates and do not normally experience inversion or channeling difficulties so surface parameters would not normally need to be monitored. Linear circuits however, are usually diffused into high resistivity substrates, are susceptable to inversion phenenomea, and should have sur-

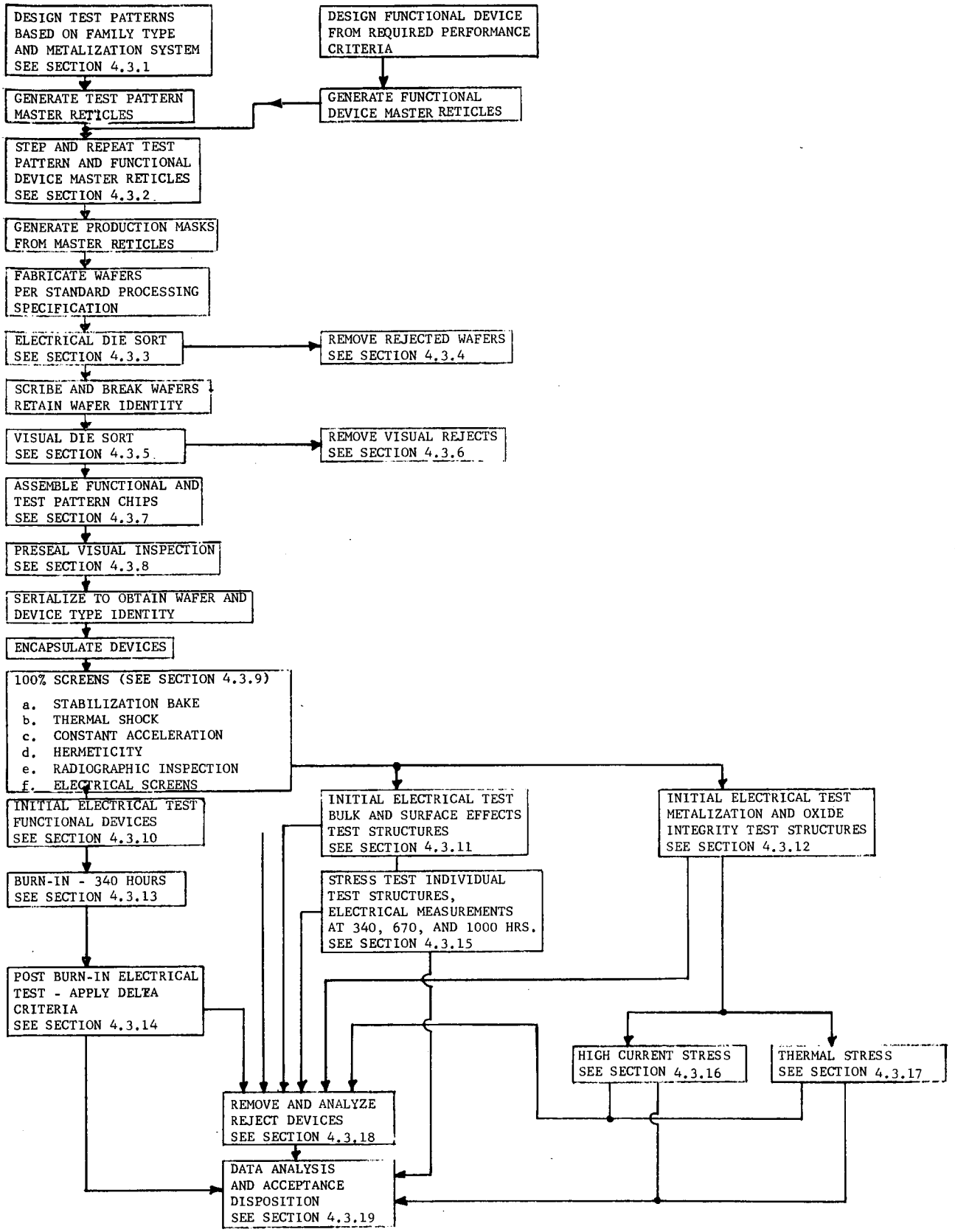


FIGURE 4.1 - SCREENING PROCEDURE FLOW DIAGRAM FOR BIPOLAR DEVICES

face parameter monitor structures included in the test pattern.

The following comprehensive list of test structures have been divided into the categories that the individual structures are intended to monitor.

a. Semiconductor Bulk Effect Structures:

1. N^+ insert sheet conductivity
2. Epitaxial layer sheet conductivity
3. Epitaxial layer sheet conductivity under base diffusion (no N^+ Buried layer)
4. Base diffusion sheet conductivity (wide resistor)
5. Resistance of diffused resistor-type pattern (narrow resistor)
6. Base sheet resistance under emitter diffusion
7. Emitter sheet conductivity
8. Double-diffused npn transistor parameters
9. Lateral bipolar pnp transistor parameters
10. Substrate collector pnp transistor parameters
11. Isolation diode parameters
12. Collector-base diode
13. Large area collector base diode
14. Schottky barrier device between Al and the collector region.

b. Surface Effect Structures:

1. A P-Channel MOS transistor between adjacent base diffusion regions
2. A N-Channel MOS transistor between adjacent emitter diffusion regions in a base diffused area
3. An MOS capacitor on a collector area
4. Surface ion migration structure
5. P-N junction with large periphery to area ratio

6. Test structures in the collector and in the base regions in which conductive paste can be used to form MOS capacitors, MOS transistors and structures for measuring the surface recombination velocity. These structures are to provide a means for characterizing regions not covered by metal-- regions in which leakage current and field inversion or leakage problems are most likely to occur.

c. Metallization, Oxide, and Ohmic Contact Integrity Structures:

1. Series of contacts to collector regions
2. Series of contacts to base regions
3. Series of contacts to emitter regions
4. Metal line over oxide steps
5. Metal line for sheet resistivity
6. Metal pattern for measurement of actual linewidth
7. Metal over base region
8. Metal over emitter region
9. Second level metal line for sheet resistance
10. Series of vias with contacts between first and second level metal
11. Second level metal area over planar first level metal
12. Second level metal area over delineated first level metal
13. Second level metal line crossing steps caused by delineated first level metal.

d. Bond Integrity Structures:

1. Adjacent pads connected by wide stripe, for measurement of bond resistance and stability

2. Bonding pad to measure breakdown strength of dielectric under wire bonds.

e. Alignment and Thickness Measurement Structures:

1. Pattern to measure the thickness of each layer in the structure directly by interference microscopy
2. Patterns to indicate alignment.

Structures for measurement of metal continuity over steps, (i.e., Items c.4, c.10, c.11, and c.13) should contain portions extending in mutually perpendicular directions to evaluate the possibility of discontinuities or weak areas because of shadowing in only one direction.

Structures b.1 through b.6 are applicable to high resistivity substrates, such as those used for linear integrated circuits, but not generally to digital integrated circuits.

4.3.2 Test Pattern Location

A possible method of location of the test pattern chips with respect to the functional devices on each high reliability wafer is shown in Figure 4.2. This method of location insures that a test pattern is adjacent to each functional device in the wafer and the ratio of chip area consumed by test pattern devices to the area consumed by the functional devices is only 0.16. An alternate approach to test pattern location with respect to the functional devices is shown in Figure 4.3. This approach insures that a typical cross section of the wafer is evaluated, and simplifies the electrical die sort measurement procedure. With the test patterns located in alternate positions, manual manipulation of the die sort station is necessary to preclude the possibility of damage to the test pattern because of the reject inker striking

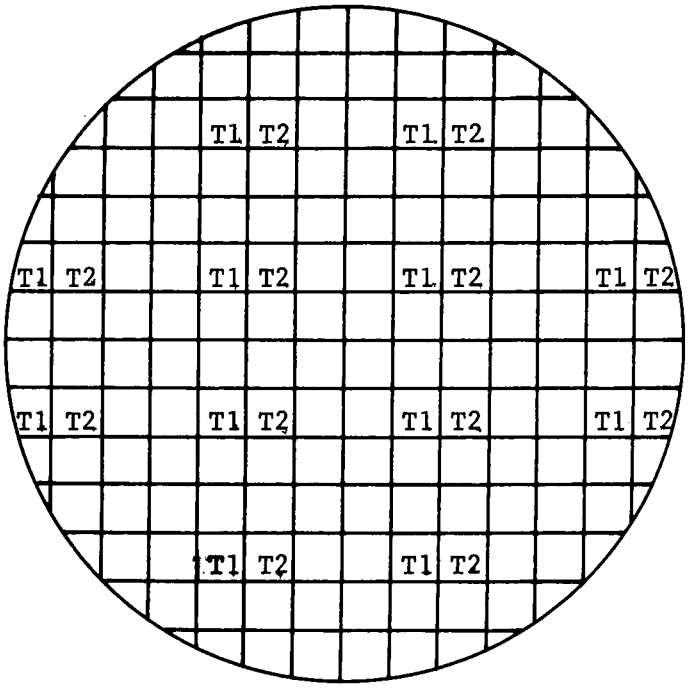


FIGURE 4.2 - POSSIBLE LOCATION OF TEST PATTERNS WITH RESPECT TO FUNCTIONAL TEST VEHICLES

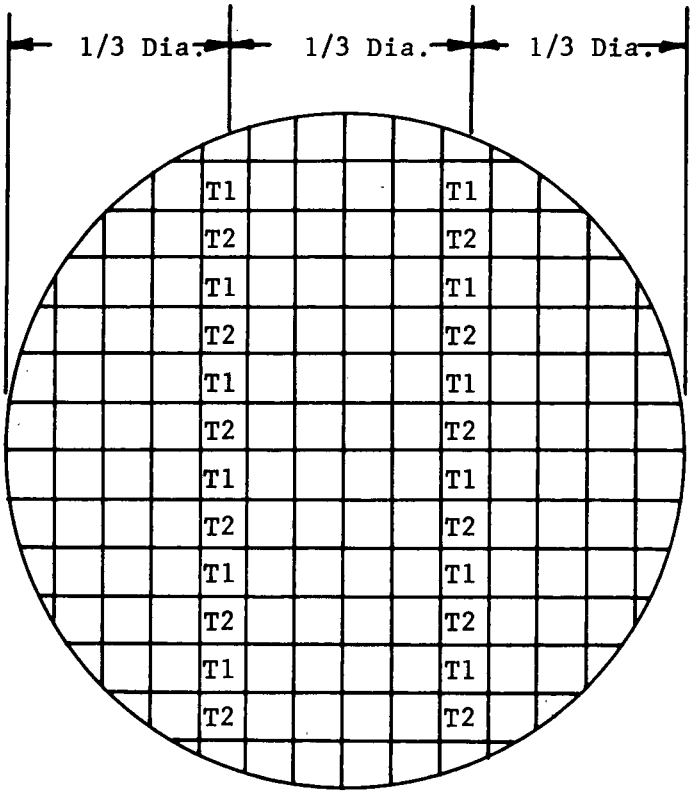


FIGURE 4.3 - PREFERRED LOCATION OF TEST PATTERNS WITH RESPECT TO FUNCTIONAL TEST VEHICLES

the test pattern when the test set is programed to test the functional device. Because the alternate approach can be utilized with fully automated die sort equipment with only a minimum of manual intervention, this approach is preferred. Additionally, this approach consumes only about 11% of the entire chip area, and will normally yield between 20 to 30 test patterns per wafer, a sufficient quantity for the evaluation of each wafer. Also this approach minimizes the problems inherent in stepping the test patterns into the functional device grid. Figures 4.2 and 4.3 show two test patterns because it is unlikely that all test patterns can be placed on one chip. The pattern shown in Figure 4.2 is the approach utilized during the work on this contract.

4.3.3 Electrical Die Sort and Visual Measurements:

The electrical die sort of each wafer should consist of a complete room temperature test of all of the functional, and all of the test pattern chips contained on the wafer. Care must be exercised so that the proper test conditions are applied to each type of chip on the wafer because inadvertant test of the functional device with the test pattern test program will cause the test equipment to sense a reject and will result in the imposition of an ink dot on the device in question. There is a strong possibility of damage to the device being tested if this should occur, either through the application of improper forcing functions or by mechanical damage due to improper adjustment of the inker. The test of the functional devices should include both D.C. and functional tests. The test of the test pattern structures should include Kelvin connection measurement of the aluminum stripe resistance structures, Kelvin connection measurements of the via and contact cut structures, oxide breakdown measurements of the contact

cut structures, measurements of the diffused resistor structures at a current low enough so ohmic heating does not influence the measured value, measurement of the transistor h_{FE}, V_{SAT}, V_{BE} and leakage currents at conditions under which they are intended to operate in the functional circuit. The special test structures intended for the evaluation of sheet and bulk resistivities should be measured at currents sufficiently high enough to insure accurate measurements, but the applied voltages should be kept sufficiently low so breakdown of the structure does not occur. The values determined for the test structures, (i.e., component values, sheet resistivities, bulk resistivities, oxide breakdown voltages, bulk breakdown voltages, etc.) should all be within the limits prescribed for the process and the design values for each component. The resistance values for the aluminum stripe, contact cut, and via cut structures must be within the values determined to be adequate to insure sufficient metalization cross section on the basis of electomigration studies. Metalization width and thickness measurements and oxide thickness measurements shall also be made at this point. All thickness and widths must be within the process specified limits.

4.3.4 Wafer Rejection At Die Sort

Based on the data obtained during this program, wafers with a low die sort yield had a very high probability of failure during the screening and life testing. (See Figure 3.20) Because of this data, any wafer that does not have a functional yield of 15% minimum for the functional device, should be rejected.

Based on the data obtained for BBTP1 during this evaluation (see Table 3.4) the wafers that exhibited a high incidence of test structure failures for metalization and oxide

integrity structures located on the interior of the wafer (this excludes the structures located at the periphery of the wafer) also exhibited a high function device failure percentage through screening and life test. For this reason, any wafer that exhibits greater than a 10% failure percentage for any given test structure should be rejected.

Excluding the bulk pattern structures at the periphery of the wafer, those wafers that exhibited deviations from the specified design values for the bulk parameters (such as sheet resistivity, resistance values, and betas) but which passed the initial measurements also exhibited a high failure percentage through screening and life test. Since the device design is based on a given tolerance on the process determined parameters (line widths, sheet resistivity, diffuction depth, metalization thickness) those wafers whose calculated mean values for processing determined parameters do not meet the specified worst case design limits, or whose calculated mean values do not meet the specified process resistivities, should be rejected. Also, neglecting the peripheral chips, the oxide and metalization widths and thicknesses must be within the process specified limits or the wafer shall be rejected.

The wafer rejection criteria based on the test pattern data, or based on the functional test of the functional devices are mutually independent. Failure for the criteria established for any one structure is sufficient for wafer rejection.

It is obvious that failure percentages must be kept for this testing.

4.3.5 Visual Die Sort

A visual die inspection, per the requirement of the visual inspection criteria of Appendix "A" may be performed by the manufacturer at this point so that die with obvious defects are not assembled. This inspection however, is at the manufacturer's discretion and is performed for reasons of economics because each device must be reinspected subsequent to assembly.

4.3.6 Removal of Visual Reject Die

If the manufacturer chooses the dice that does not meet the visual inspection criteria, or the dice which does not exhibit electrical reject ink dots, may be removed at this point.

4.3.7 Assembly

A sufficient quantity of each type of test pattern dice must be assembled to insure that a minimum of six of each test pattern dice from each wafer are available for subsequent testing after encapsulation. All of the available functional chips must be assembled. The assembly of both the test pattern and the functional dice must be accomplished at the same time to insure that the chip bonding conditions are identical, and wafer identity must be maintained. All assembled test patterns and functional devices must be bonded according to the individual bonding requirements for each chip design.

4.3.8 Preseal Visual Inspection

All devices which do not meet the requirements of the preseal visual inspection criteria of Appendix "A" are to be serialized to maintain wafer identity, and all assemblies are to be sealed according to the specified sealing procedure for the package.

4.3.9 In Process Screens

Both the functional test vehicles and the test patterns are to be subjected to the following in process screens:

a. Stabilization Bake per MIL-STD-883, Test Method 1008, 24 hours (minumum).

b. Thermal Shock, per MIL-STD-883, Test Method 1011, Test Condition C (minimum).

c. Constant Acceleration, per MIL-STD-883, Method 2001, 40,000 G (minimum) Y_1 plane only.

d. Hermeticity, fine and gross, per MIL-STD-883, Test Method 1014, Test Conditions A and C.

e. Radiographic Inspection, per MIL-STD-883, Method 2012.

The functional devices shall also be subjected to appropriate electrical screening tests designed to monitor the total device leakage at the maximum rated V_{CC} and input voltage conditions. Abnormally high leakage values will indicate internal shorts, and/or inadequate breakdown voltages which may not be detected during the normal electrical test of these devices. Devices exhibiting abnormal values should be rejected.

4.3.10 Initial Electrical Test, Functional Devices

All of the functional devices shall be D.C. and functional specification for the device under question. These measurements shall be made at -55°C, +25°C and +125°C. Any device which does not meet the requirements of detailed electrical specification of the device sha shall be rejected.

4.3.11 Initial Electrical Test, Bulk and Surface Effects Structures

The initial electrical measurements on the encapsulated bulk and surface effects structures should consist of the electrical determination of the fundamental component parameters. The encapsulated bulk and surface effects structures should include:

a. Transistors, both MOS and bipolar, of the same geometry as contained in the functional device. Several different transistor geometries may be required,

b. Diodes, of the same geometry as utilized by the functional device,

c. Metal-oxide-Silicon capacitor structures provided the functional device is fabriated in high resistivity substrate material (5 Ω-cm or greater).

As a minimum, except as otherwise noted, the fundemental component parameters should be measured at the conditions to which they will be exposed during nominal operation in the functional circuit. The following lists the parameters that should be measured on several types of structures.

OUTPUT TRANSISTORS

$V_{CE(SAT)}$ - Saturation Voltage
V_{BE} - Forward Emitter Voltage
h_{FE} - Forward Current Gain
h_{FER} - Inverse Current Gain
I_{CEO}, I_{CBO}, and I_{EBO} - Reverse Biased Leakage Currents.

INPUT TRANSISTORS

The same parameters as indicated for output transistors and laterial current gain between the emitters of multiple input transistors.

MOS TRANSISTORS

V_{GST} - Threshold Voltage
Voltage Gain
Leakage Currents.

DIODES

V_F - Forward Voltage

V_R - Reverse Voltage

I_R - Reverse Leakage Current.

METAL-OXIDE-SILICON CAPACITOR STRUCTURES

Flat Band Voltages

Charge densities, Q_{SS}, Q_O, and Q_{NEG}.

4.3.12 Initial Electrical Test, Metalization and Oxide Integrity Structures

The initial electrical measurements on the metalization and oxide integrity structures should consist of the determination of the resistances associated with each type of metalization structure utilized in the functional device, and of the oxide breakdown voltage of each type of oxide structure utilized in the functional device.

The metalization stripe structures for a monolayer metalization system should include as a minimum:

a. A planar metalization stripe,

b. A metalization stripe over oxide steps,

c. A structure consisting of short lengths of a metalization stripe in series with short lengths of "p" type resistor diffusions to evaluate the integrity of contact cuts.

The metalization stripe structures for multilayered metalization systems should include metalization stripes on each oxide layer similar to those described above, except rather than a series string of metalization stripes and diffused resistors interconnected through contact cuts, the upper layer metalization stripes should be interconnected

to bottom layer metalization stripes through vias.

The electrical measurements of the metalization stripe structures should be performed with Kelvin connections to preclude errors resulting from excessive contact resistance.

Capacitor structures should be included in the test pattern to evaluate the integrity of the thermal oxides and the dielectric layers between multilayer metalization planes. Since most oxide shorts occur at the periphery of the metalization stripes, the capacitor structures should be interdigitated to evaluate the possibility of peripheral shorts. Bipolar oxide systems should be capable, in the absence of defects, of supporting an applied potential of 200V.

4.3.13 Functional Device Burn-In

The Burn-In test circuit is dependent upon both the external pin configuration and the function the device is designed to perform. Digital bipolar circuits are normally fabricated into low resistivity substrate material and do not normally experience inversion difficulties. Linear bipolar circuits however, are fabricated in high resistivily material and are susceptable to inversion difficulties.

Burn-In is normally used to screen devices which have successfully passed all previous screening but would experience early failure in the subsystem application in which they will be used. Most early digital bipolar device failures are related to metalization and/or contact cuts and/or oxide shorting difficulties. For these reasons the burn-in operational circuits for digital bipolar devices should be one that applies the maximum voltages, the high-

est currents, utilizes the maximum number of internal components, and operates at the highest temperature possible. Since the circuit may be temperature cycled during use, it would also be advantageous to insure that temperature cycled operation would not cause metalization failures because of the application of thermally generated mechanical stress resulting from the difference in thermal coefficients between the metalization system, the oxide layers and the silicon substrate. Therefore, the burn-in circuit that would be most effective in screening potential digital bipolar device failures would be an open or closed ring circuit, depending on the individual device configuration, that is operated at the maximum rated voltage conditions consistent with the maximum rated operating temperature, and is cycled between the temperature extremes of +125°C and -55°C. Operation at the maximum rated voltages insures that the maximum amount of current is drawn through the device. High current operation is the most successful method for the removal of devices with metalization scratches or other defects such as thin metal at oxide steps, or metalization voids or smears. Temperature cycled ring circuit operation can be continously monitored, and provides a means of insuring that the device will function properly at the rated temperature extremes.

The recommended burn-in circuit for digital bipolar devices therefore, is a temperature cycled ring circuit, operated at the maximum rated voltages of the device. The temperature should be cycled between +125°C and -55°C three times daily. The test duration should be a minimum of 340 hours, but additional burn-in screening of devices intended for very high reliability operation would be desirable.

For linear bipolar circuits the first 340 hours of burn-in

should also be performed with the maximum rated supply and input voltages applied and the circuit should be temperature cycled between +125°C and -55°C three times daily. However, because of the possibility of inversion of these devices, a second step consisting of +125°C reverse bias testing should also be performed. The minimum duration of the reverse bias test should be 340 hours.

4.3.14 Post Burn-In Electrical Measurements - Functional Devices

The post burn-in electrical measurements of the functional devices shall consist of complete D.C. and functional testing per the individual device specification at -55°C, +25°C and +125°C. Transient measurements per the device specification shall also be performed at -55°C, +25°C and +125°C on a sampling basis. An LTPD of 10 with an acceptance number of 1 is to be applied to the transient measurements. If the devices fail this inspection, tightened inspection (LTPD = 7, acceptance number = 2) must be applied. Failure to the tightened inspection level will be cause for rejection of the devices from the wafer.

Failure of an individual device to meet the specified D.C. and/or functional test requirements shall be cause for rejection of the individual device. Failure of more than 10% of the devices from a given wafer during the burn-in test will be cause for the rejection of all devices from the wafer.

Delta limits shall also be applied to the pre and post burn-in test data. These limits shall be:

a. Measured voltages - $\pm$10%
b. Measured currents - $\pm$10%
c. Leakage Currents - $\pm$20 nA or $\pm$20% of the maximum specification limit, whichever is greater.

Individual devices which exceed the delta limit criteria shall be rejected. If more than 10% of the devices from a given wafer fail, in combination, the absolute and/or the delta limits, the entire wafer shall be rejected.

4.3.15 Stress Test - Individual Bulk and Surface Effects Test Structures

The stress tests on the individual bulk and surface effects structures should be designed such that, based on the worst case design analysis, these structures are subjected to stresses in excess of the stresses they will experience during actual circuit operation. The individual structures of this test pattern chip will be transistor structures and diode structures, structures of the same geometry as used in the functional device. Also for linear bipolar circuits Metal-Oxide-Silicon capacitor structures shall be used to identify possible inversion difficulties by applying the flat band voltage determination techniques described in a later section of this report. Flat band voltages shall be determined prior to and subsequent to charge drifting of the MOS capacitor structures.

The transistor and the diode structures of the bulk and surface effects pattern shall be generally subjected to back bias testing at +125^{o}C to determine whether these structures exhibit any instabilities. In the case of individual transistor structures that are copies of devices that operate in the active region in the functional circuit, power dissipation testing should be performed.

The individual structures shall be measured for the same D.C. parameters as measured initially after 340, 670 and 1,000 hours of operation. Both absolute and delta limit failure criteria shall be applied. The absolute limit criteria shall be based on the worst case design analysis

values of the parameters for each individual structure, and the delta criteria shall be:

a. Measured voltages - ±10%

b. Measured currents - ±10%

c. Leakage Currents - ±20 nA or ±20% of the maximum specified value, whichever is greater.

The minimum sample size from any one wafer for any test structure shall be 10. The test circuit shall be arranged so that all of the descrete structures can be tested simultaneously. Rejection of all of the devices, including the functional devices, from the wafer from which the test devices were obtained will be required if more than 20% of any individual test structure fails the absolute and/or delta criteria through 1,000 hours of test.

4.3.16 High Current Stress Testing

The metalization integrity patterns, consisting of the aluminum stripe structures, the contact cut structures and the via structures shall be subjected to high current stress testing to insure that there is no reliability problem associated with the contact cuts, the vias or the interconnecting aluminum metalization.

Effective utilization of the aluminum stripe patterns depends upon the generation of MTBF vs current density plots (for the worst case operating temperature the device will experience) for each metalization process involved in the functional device. Also the metalization stripes of the test structure should be of the same minimum cross section' that is utilized in the functional device.

The current to be applied during the stress testing shall be determined by calculating the current level required to

cause a current density of 1 X 10^6 Amps/cm^2 in the aluminium stripe of minimum cross section. The test temperature shall be the worst case operating temperature of the functional device and the test shall be continued for 340 hours or to the point of 50% failure. The mean time before failure shall be determined from the measured times to failure for the structures under test, and the data shall be extrapolated using the slopes of the previously determined data to insure that the mean time to failure, at the worst case temperature and current density experienced in the functional device, is in excess of the minimum reliability requirements of the device. The same current level as applied to the minimum cross section area stripe shall be applied to all other metalization stripe structures and to the via structure regardless of the current density to insure that the mean time to failure for these structures exceeds the mean time to failure of the minimum cross sectional area stripe.

In the case of the contact cut evaluation structure the maximum current level is limited by the resistor diffusion breakdown voltage. For this structure the current level to be applied shall be the maximum value that can be applied, without causing breakdown, to evaluate the integrity of the contact cuts.

The functional devices from any given wafer will be rejected if the test pattern data indicates that metalization, or via, or contact cut structures will not meet the minimum reliability requirements of the functional device.

4.3.17 Thermal Stress - Metalization and Oxide Integrity Structures

The metalization and oxide integrity structures shall be subjected to thermal stressing to accelerate potential

failure mechanisms associated with bonding, metalizations, and oxide layers. The test patterns should be capable of withstanding these stresses and failure of the test structures will indicate potential reliability problems. The thermal stress sequence shall consist of:

a. Electrical Measurements
b. Thermal Shock*
c. Electrical Measurements**
d. 200°C Storage, 340 Hours
e. Electrical Measurements**
f. Thermal Shock*
g. Electrical Measurements**
h. 200°C Storage, 340 Hours
i. Electrical Measurements**
j. Thermal Shock*
k. 200°C Storage, 340 Hours
l. Electrical Measurements**
m. Constant Acceleration***
n. Electrical Measurements**

* Per MIL-STD-883, Method 1011, Condition D.

** Measure all metalization, wire bond, via, and contact cut structures, to determine resistance value. Subject all capacitor structures to a 200 V stress.

*** Per MIL-STD-883, Method 2001, 40,000 G, Y_1 plane only.

A minimum of 10 structures from each wafer shall be subjected to the above test sequence. Failure shall be defined as the inability of the capacitor structures to withstand the application of the 200 Volt potential, the shorting or opening of the resistance structures, and/or greater than a $\pm$10% change in resistance values when compared with the initial measurement. The functional de-

vices from the wafer from which the test patterns were obtained shall be rejected if more than 10% of the test structures from that wafer fail to meet the thermal stress requirements.

4.3.18 Analysis of Failures

All functional and test structure vehicles which fail the post encapsulation requirements of the screening procedure shall be subjected to an analysis sufficient to determine the the mechanism responsible for failure. The results of the analyses shall be summarized, by wafer, according to the mechanism responsible for failure and this data shall be submitted for evaluation, concurrent with the statistical data derived during the course of the screening procedure prior to the final acceptance of the devices from any wafer.

4.3.19 Data Analysis and Acceptance Disposition

All of the data collected throughout the screening sequence shall be collected and the failure criteria specified for both the functional devices and the test structures shall be applied on a wafer by wafer basis. The functional devices from all wafers which do not meet the screening requirements previously specified, shall be removed.

A summary of the screening data shall be prepared which indicates by wafer, the serial numbers of the acceptable devices, and the serial numbers of the unacceptable devices and wafers together with the reasons for the rejection of the devices and/or wafers.

SECTION V

MOS TEST RESULTS AND ANALYSIS

5.1 GENERAL

The arrangement of the factual data in this section is:

a. A summary of all the MOS test vehicle data collected during the Phase 3 evaluation performed in accordance with the Test Flow Diagram of Figure 5.1 and Table 5.1, and according to the requirements of the MOS Evaluation Plan generated under the work on this contract.

b. The correlation of the MOSPA and the MOSPB data with the data obtained from the MOS functional vehicles.

Where required, explanations are given in the text to clarify the data summariers, or the interpretations of the significance of the data.

Throughout the entire MOS evaluation control devices were measured at each electrical test prior to subjecting any of the evaluation vehicles to the measurement. The control device data is not specifically mentioned in the text, but the maximum variation on the control device parameters was less than 5% for leakage currents and less than 3% for measured currents and voltages throughout the test program thus insuring adequate test set up and proper electrical measurements. The preseal visual categories referred to throughout this report as Class "A" or Class "B" devices are those devices which met the preseal visual criteria of Appendix A. Class "R" devices are devices which marginally failed the lower level (Class B) visual inspection criteria.

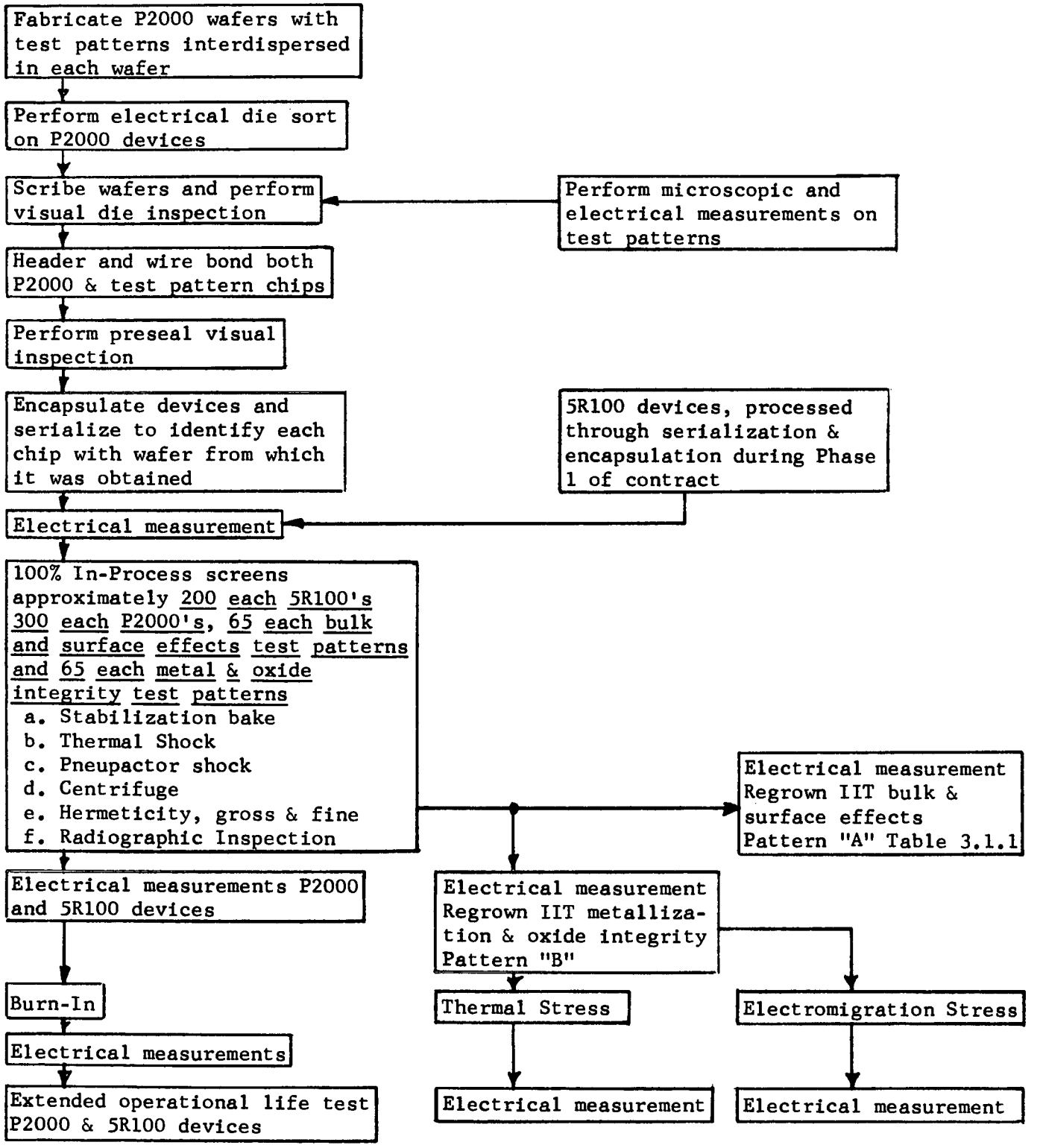


FIGURE 5.1 - EVALUATION PLAN FLOW DIAGRAM FOR MOS VEHICLES

TEST STRUCTURE	DESCRIPTION	MEASUREMENT
1	MOS Capacitor over field oxide	Flat band voltage a. After drifting mobile charge, under 0 Volt bias, for 12 minutes at 300°C. b. After drifting mobile charge, under -36 Volt bias, for 12 minutes at 300°C.
2	MOS Capacitor over gate oxide	Flat band voltage a. After drifting mobile charge, under 0 Volt bias, for 12 minutes at 300°C. b. After drifting mobile charge, under -12 Volt bias, for 12 minutes at 300°C.
3	Large area p-n junction Diode	a. Leakage current at -20 V. b. Breakdown voltage at 10 μA.
6	Field oxide MOS Transistor	Inversion voltage a. After drifting mobile charge, under 0 Volt bias, for 12 minutes at 300°C. b. After drifting mobile charge, under -36 Volt bias, for 12 minutes at 300°C.
7	Gate oxide MOS Transistor	Inversion voltage a. After drifting mobile charge, under 0 Volt bias, for 12 minutes at 300°C. b. After drifting mobile charge, under -12 Volt bias, for 12 minutes at 300°C.
8	Lateral Bipolar Transistor	h_{FE} at 5 V_{CE} & 50 μAI_C.

TABLE 5.1 - ELECTRICAL MEASUREMENTS ON TEST PATTERN A

5.2 MOS TEST VEHICLE DATA SUMMARY

The material contained in the following subsections summarizes, on a wafer by wafer basis, the results of the preseal visual inspection, and the failures incurred during the Phase 3 evaluation of the 5R100, P2000, MOSPA and MOSPB test vehicles. The results of the failure analysis performed on the test vehicles are also summarized. The correlation of the test pattern data with functional device failures is presented in Subsection 5.3.

5.2.1 P2000 and 5R100 Evaluation Data Summary

Table 5.2 summarizes the quantity of the P2000 and 5R100 devices from each wafer that were placed into the different visual categories according to the preseal visual inspection criteria contained in Appendix "A". The Table also summarizes the total yield of the P2000 and 5R100 devices on a wafer by wafer basis subsequent to the electrical die sort measurement and subsequent to the initial post encapsulation test.

During the Phase 3 evaluations, the P2000 devices were serialized in a manner so it would be known if the assembled device was fabricated from a chip located in the "inner" or the "outer" portion of each wafer. The "inner" chips consists of all chips within the circular area approximately 5/8" in radius, concentric with the center of the 1" radius wafer, the "outer" chips are those around the periphery of the wafer not included in the 5/8" radius circle. The purpose of this identification was to determine if reliability was effected by the portion of the wafer from which the chip was obtained. Table 5.3 summarizes the results of the initial post encapsulation testing of the P2000 devices according to lot, wafer, and wafer position of the chips used in the fabrication of these devices.

Table 5.4 summarizes the P2000 and the 5R100 failures incurred through the entire Phase 3 evaluation program by wafer and visual category. The failure criteria is defined in the final draft of the evaluation plan for MOS devices submitted during September 1971.

TYPE	LOT	LOT CODE	WAFER	DIE SORT YIELD (%)	ASSEMBLED (n)	CLASS "A" VISUAL (n)	CLASS "B" VISUAL (n)	CLASS "R" VISUAL (n)	FINAL TEST YIELD CLASS "A" (%)	FINAL TEST YIELD CLASS "B" (%)	FINAL TEST YIELD CLASS "R" (%)
5R100	12-9-47	2	1	19	25	5	14	6	60	35	*
5R100	12-9-47	2	2	25	28	9	9	10	78	56	*
5R100	12-9-47	2	3	45	30	18	2	10	83	0	40
5R100	12-9-47	2	4	35	28	10	2	16	20	50	*
5R100	12-9-47	2	5	25	29	12	4	13	25	0	*
5R100	12-9-47	2	6	35	30	15	6	9	60	17	55
5R100	12-9-47	2	7	39	23	9	4	10	78	100	60
5R100	12-9-47	2	8	38	28	10	8	10	40	75	*
5R100	12-9-47	2	9	27	30	21	1	8	67	100	*
5R100	13-9-47	3	1	32	28	11	7	10	54	57	50
5R100	13-9-47	3	2	55	28	17	5	6	47	60	50
5R100	13-9-47	3	3	51	28	19	5	4	42	40	*
5R100	13-9-47	3	4	49	30	10	8	12	70	38	*
5R100	13-9-47	3	5	55	29	9	6	14	78	83	64
5R100	13-9-47	3	6	34	25	9	9	7	33	33	43
5R100	13-9-47	3	7	40	27	7	8	12	29	62	*
5R100	13-9-47	3	8	52	29	15	4	10	47	50	*
5R100	13-9-47	3	9	59	27	5	2	20	80	100	*
5R100	13-9-47	3	10	47	30	18	6	6	39	50	*
P2000	12-0-32	A	1	43	44	9	19	16	78	90	87
P2000	12-0-32	A	2	50	45	4	19	22	100	90	86
P2000	12-0-32	A	3	54	46	7	22	17	57	86	59
P2000	12-0-32	A	4	50	42	6	17	19	100	70	84
P2000	12-0-32	A	5	33	47	7	28	12	71	68	75
P2000	13-0-32	B	1	39	42	13	11	18	62	82	61
P2000	13-0-32	B	2	42	47	6	19	22	67	74	68
P2000	13-0-32	B	3	39	43	0	27	16	---	74	94
P2000	13-0-32	B	4	32	47	6	19	22	100	74	59
P2000	13-0-32	B	5	41	44	3	22	19	100	82	94
P2000	14-0-32	C	1	50	41	11	10	20	82	80	85
P2000	14-0-32	C	2	51	40	8	12	20	75	92	90

* DATA INADEQUATE TO CALCULATE YIELDS

TABLE 5.2 - ELECTRICAL DIE SORT YIELD, PRESEAL VISUAL INSPECTION RESULTS, AND POST SEAL ELECTRICAL TEST YIELDS FOR THE 5R100 AND P2000 TEST VEHICLES.

				CLASS "A" VISUAL				CLASS "B" VISUAL				CLASS "R" VISUAL			
				INNER		OUTER		INNER		OUTER		INNER		OUTER	
TYPE	LOT	LOT CODE	WAFER	FAILURE/SAMPLE	% FAIL	FAILURE/SAMPLE	% FAIL	FAILURE/SAMPLE	% FAIL	FAILURE/SAMPLE	% FAIL	FAILURE/SAMPLE	% FAIL	FAILURE/SAMPLE	% FAIL
P2000	12-0-32	A	1	1/5	20	1/4	25	1/11	9	1/8	12	0/6	0	2/10	20
P2000	12-0-32	A	2	0/2	0	0/2	0	2/18	11	0/1	0	0/4	0	3/18	17
P2000	12-0-32	A	3	1/2	50	2/5	40	1/11	9	2/11	18	4/9	45	3/8	38
P2000	12-0-32	A	4	0/4	0	0/2	0	5/9	56	0/8	0	2/7	28	1/12	8
P2000	12-0-32	A	5	2/3	67	0/4	0	3/14	22	6/14	43	2/6	33	1/6	17
TOTALS - LOT A				4/16	25	3/17	18	12/63	19	9/42	22	8/32	25	10/54	18
P2000	13-0-32	B	1	4/10	40	1/3	33	1/4	25	6/7	86	2/8	25	5/10	50
P2000	13-0-32	B	2	1/4	25	1/2	50	3/13	23	2/6	33	3/6	50	4/16	25
P2000	13-0-32	B	3	0/0	--	0/0	--	5/16	31	2/11	18	1/8	13	0/8	0
P2000	13-0-32	B	4	0/2	0	0/4	0	4/12	33	1/7	14	7/9	78	2/13	15
P2000	13-0-32	B	5	0/3	0	0/0	--	0/8	0	4/14	28	1/13	8	0/6	0
TOTALS - LOT B				5/19	26	2/9	22	13/53	25	15/45	33	14/44	32	11/53	21
P2000	14-0-32	C	1	1/7	14	1/4	25	1/5	20	1/5	20	0/9	0	3/11	27
P2000	14-0-32	C	2	0/3	0	2/5	40	0/6	0	1/6	17	2/14	14	0/6	0
TOTALS - LOT C				1/10	10	3/9	33	1/11	9	2/11	18	2/23	9	3/17	18
TOTALS - ALL LOTS				10/45	22	8/35	23	26/127	20	26/98	26	24/99	24	24/124	19

TABLE 5.3 - INITIAL P2000 POST ENCAPSULATION FAILURES
BY LOT, WAFER, AND CHIP LOCATION ON THE WAFER

TYPE	LOT/WAFER CODE	VISUAL CLASS	WAFER LOCATION	SAMPLE	INITIAL D.C.	INITIAL MCF	HERMETICITY	POST SCREEN MCF	POST SCREEN FUNCTIONAL	POST SCREEN D.C.	POST SCREEN MCF	POST BURN-IN D.C.	POST BURN-IN MCF	POST 340 HR. LIFE D.C.	POST 340 HR. LIFE MCF	POST 670 HR. LIFE D.C.	POST 670 HR. LIFE MCF	POST 1000 HR. LIFE D.C.	POST 1000 HR. LIFE MCF	POST 2000 HR. LIFE D.C.	POST 2000 HR. LIFE MCF
5R100	2/1	A	- /	5	2	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
5R100	2/2	A	-	9	0	2	0	1	0	0	0	2	0	1	0	0	0	0	0	0	1
5R100	2/3	A	-	18	1	2	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0
5R100	2/4	A	-	10	4	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5R100	2/5	A	-	12	5	4	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
5R100	2/6	A	-	15	2	4	0	0	0	1	1	4	0	0	0	0	0	0	0	0	0
5R100	2/7	A	-	9	1	1	0	0	0	0	0	2	1	1	0	0	0	0	0	0	0
5R100	2/8	A	-	10	3	3	0	0	0	0	0	1	2	0	0	0	0	0	0	0	0
5R100	2/9	A	-	21	4	3	0	0	0	7	0	0	2	1	0	0	0	0	0	0	0
TOTALS				109	22	23	0	2	0	9	2	12	5	4	0	0	0	0	0	0	1
5R100	3/1	A	-	11	1	3	0	0	0	0	3	2	1	0	0	0	0	0	0	0	1
5R100	3/2	A	-	17	3	6	0	1	0	0	0	5	1	0	0	0	0	0	0	0	0
5R100	3/3	A	-	19	2	9	0	0	0	0	3	3	2	0	0	0	0	0	0	0	0
5R100	3/4	A	-	10	0	3	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
5R100	3/5	A	-	9	0	2	0	1	1	1	0	0	0	0	0	0	0	2	0	0	0
5R100	3/6	A	-	9	3	3	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
5R100	3/7	A	-	7	1	4	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0
5R100	3/8	A	-	15	1	7	0	0	0	1	0	3	1	0	0	0	0	0	0	0	0
5R100	3/9	A	-	5	0	1	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0
5R100	3/10	A	-	18	3	8	0	1	0	0	0	2	0	1	0	0	0	0	0	0	0
TOTALS				120	14	46	0	5	1	2	7	17	5	2	0	0	0	2	0	0	1
P2000	A/1	A	I	5	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
P2000	A/1	A	0	4	1	00	0	0	0	0	0	00	1	0	0	0	0	0	0	0	0
P2000	A/2	A	I	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
P2000	A/2	A	0	2	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
P2000	A/3	A	I	2	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
P2000	A/3	A	0	5	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
P2000	A/4	A	I	4	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
P2000	A/4	A	0	2	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
P2000	A/5	A	I	3	0	0	0	0	0	0	0	00	1	0	0	0	0	0	0	0	0
P2000	A/5	A	0	4	0	00	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
TOTALS				33	4	1	0	0	0	0	0	2	5	0	0	0	0	0	0	0	0
P2000	B/1	A	I	10	3	0	0	1	0	1	0	4	1	0	0	0	0	0	0	0	0
P2000	B/1	A	0	3	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0
P2000	B/2	A	I	4	1	0	0	1	0	0	0	2	0	0	0	0	0	0	0	0	0
P2000	B/2	A	0	2	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
P2000	B/3	A	I	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P2000	B/3	A	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P2000	B/4	A	I	2	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
P2000	B/4	A	0	4	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0
P2000	B/5	A	I	3	0	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0
P2000	B/5	A	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
TOTALS				28	6	0	0	3	0	1	1	10	2	1	1	0	1	0	1	0	0
P2000	C/1	A	I	7	0	0	0	0	0	3	0	0	0	0	0	0	0	0	0	0	1
P2000	C/1	A	0	4	1	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0
P2000	C/2	A	I	3	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0
P2000	C/2	A	0	5	2	0	0	0	0	2	0	0	1	0	0	0	0	0	0	0	0
TOTALS				19	3	0	0	0	0	7	0	00	2	0	0	0	0	2	0	0	1

TABLE 5.4 - P2000 AND 5R100 FAILURES THROUGH EVALUATION TEST SEQUENCE

TYPE	LOT/WAFER CODE	VISUAL CLASS	WAFER LOCATION	SAMPLE	INITIAL D.C.	INITIAL MCF	HERMETICITY	POST SCREEN MCF	POST SCREEN FUNCTIONAL	POST SCREEN D.C.	POST SCREEN MCF	POST BURN-IN D.C.	POST BURN-IN MCF	POST 340 HR. LIFE D.C.	POST 340 HR. LIFE MCF	POST 670 HR. LIFE D.C.	POST 670 HR. LIFE MCF	POST 1000 HR. LIFE D.C.	POST 1000 HR. LIFE MCF	POST 2000 HR. LIFE D.C.	POST 2000 HR. LIFE MCF
5R100	2/1	B	-	14	7	2	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0
5R100	2/2	B	-	9	2	2	0	3	0	1	0	0	0	0	0	0	0	0	0	0	0
5R100	2/3	B	-	2	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5R100	2/4	B	-	2	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
5R100	2/5	B	-	4	3	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5R100	2/6	B	-	6	0	5	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
5R100	2/7	B	-	4	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
5R100	2/8	B	-	8	0	2	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0
5R100	2/9	B	-	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
TOTALS				50	13	14	0	5	0	4	0	5	1	0	0	1	0	0	0	0	0
5R100	3/1	B	-	7	0	3	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
5R100	3/2	B	-	5	0	2	0	0	0	0	1	2	0	0	0	0	0	0	0	0	0
5R100	3/3	B	-	5	0	3	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
5R100	3/4	B	-	8	0	5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5R100	3/5	B	-	6	0	1	0	1	0	2	0	0	00	0	0	0	0	0	0	0	0
5R100	3/6	B	-	9	3	3	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0
5R100	3/7	B	-	8	3	0	0	1	0	0	0	2	0	0	0	0	0	0	0	0	0
5R100	3/8	B	-	4	1	1	0	0	0	0	0	2	0	0	0	0	0	0	0	0	0
5R100	3/9	B	-	2	0	0	0	0	0	0	0	2	0	0	0	0	0	0	0	0	0
5R100	3/10	B	-	6	2	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
TOTALS				60	9	19	0	5	0	3	2	9	0	1	0	0	0	0	0	0	0
P2000	A/1	B	I	11	1	0	0	0	0	0	0	2	2	0	0	0	0	0	0	0	0
P2000	A/1	B	O	8	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0	1	0
P2000	A/2	B	I	18	2	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0
P2000	A/2	B	O	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
P2000	A/3	B	I	11	1	0	0	0	0	0	0	00	1	0	0	0	0	0	0	0	0
P2000	A/3	B	O	11	1	0	0	0	0	0	0	0	2	1	0	0	0	0	0	0	0
P2000	A/4	B	I	9	4	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
P2000	A/4	B	O	8	0	0	0	0	0	0	0	2	2	0	0	0	0	0	0	0	0
P2000	A/5	B	II	14	1	0	0	0	0	2	4	1	3	0	0	0	0	0	0	0	0
P2000	A/5	B	O	14	4	1	0	0	0	1	2	0	0	0	0	0	0	0	0	0	0
TOTALS				105	15	2	0	1	0	3	7	7	13	1	0	0	0	0	0	1	0
P2000	B/1	B	I	4	1	0	0	0	0	0	0	3	0	0	0	0	0	0	0	0	0
P2000	B/1	B	O	7	5	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
P2000	B/2	B	I	13	3	0	0	0	0	7	0	2	0	0	0	0	1	0	0	0	0
P2000	B/2	B	O	6	2	0	0	0	0	0	0	4	0	0	0	0	0	0	0	0	0
P2000	B/3	B	I	16	3	2	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0
P2000	B/3	B	O	11	2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0
P2000	B/4	B	I	13	4	1	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0
P2000	B/4	B	O	7	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0
P2000	B/5	B	I	8	0	00	0	1	0	0	2	0	3	0	0	0	0	0	0	0	0
P2000	B/5	B	O	14	0	4	0	1	0	1	0	0	0	0	0	0	1	0	2	0	0
TOTALS				99	21	8	0	4	0	111	3	11	6	0	0	0	2	0	2	1	0
P2000	C/1	B	I	5	0	0	0	3	1	0	0	1	0	0	0	0	0	0	0	0	0
P2000	C/1	B	O	5	2	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0
P2000	C/2	B	I	6	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
P2000	C/2	B	O	6	1	0	0	1	1	0	0	2	0	0	0	0	0	0	0	0	0
TOTALS				22	3	0	0	5	4	0	1	3	0	0	0	0	0	0	0	0	0

TABLE 5.4 - P2000 AND 5R100 FAILURES THROUGH EVALUATION TEST SEQUENCE

TYPE	LOT/WAFER CODE	VISUAL CLASS	WAFER LOCATION	INITIAL SAMPLE/TEST SAMPLE	INITIAL		HERMETICITY	POST SCREEN MCF	POST SCREEN FUNCTIONAL	POST SCREEN		POST BURN-IN		POST 340 HR. LIFE		POST 670 HR. LIFE		POST 1000 HR. LIFE		POST 2000 HR. LIFE	
					D.C.	MCF				D.C.	MCF	D.C.	MCF	D.C.	MCF	D.C.	MCF	D.C.	MCF	D.C.	MCF
5R100	2/1	R	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
5R100	2/2	R	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
5R100	2/3	R	-	10/4	2	3	0	1	0	0	0	0	3	0	0	0	0	0	0	0	0
5R100	2/4	R	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
5R100	2/5	R	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
5R100	2/6	R	-	9/5	1	3	0	0	0	1	3	1	0	0	0	0	0	0	0	0	0
5R100	2/7	R	-	10/6	0	2	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
5R100	2/8	R	-	1/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5R100	2/9	R	-	1/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TOTALS				31/15	3	8	0	1	0	2	3	1	3	0	0	0	0	0	0	0	0
5R100	3/1	R	-	10/5	2	3	0	-	-	1	0	1	1	0	0	0	0	0	0	0	0
5R100	3/2	R	-	6/3	0	3	0	0	0	0	0	1	2	-	-	-	-	-	-	-	-
5R100	3/3	R	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
5R100	3/4	R	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
5R100	3/5	R	-	14/9	4	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
5R100	3/6	R	-	6/3	0	3	0	-	1	1	0	0	0	1	0	-	-	-	-	-	-
5R100	3/7	R	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
5R100	3/8	R	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
5R100	3/9	R	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
5R100	3/10	R	-	1/0	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
TOTALS				37/20	7	10	0	0	1	2	0	3	3	1	0	0	0	0	0	0	0
P2000	A/1	R	I	6/5	0	0	0	3	1	0	0	0	0	0	1	0	0	0	0	0	0
P2000	A/1	R	0	10/0	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
P2000	A/2	R	I	4/4	0	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0
P2000	A/2	R	0	18/1	3	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
P2000	A/3	R	I	9/4	2	2	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0
P2000	A/3	R	0	8/1	1	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
P2000	A/4	R	I	7/5	2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
P2000	A/4	R	0	12/0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
P2000	A/5	R	I	6/4	2	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
P2000	A/5	R	0	6/1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
TOTALS				86/25	14	4	0	7	2	0	1	0	1	0	2	1	0	0	0	0	0
P2000	B/1	R	I	8/5	2	0	0	4	1	0	0	0	0	0	0	0	0	0	0	0	0
P2000	B/1	R	0	12/0	4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
P2000	B/2	R	I	5/4	2	0	0	2	1	0	0	0	0	0	0	0	0	0	0	0	0
P2000	B/2	R	0	16/2	4	0	0	2	0	0	0	0	0	0	0	0	0	0	0	0	0
P2000	B/3	R	I	8/5	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0
P2000	B/3	R	0	8/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
P2000	B/4	R	I	9/2	5	2	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
P2000	B/4	R	0	13/3	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
P2000	B/5	R	I	13/5	0	1	0	0	0	0	2	0	0	0	0	0	0	0	0	0	0
P2000	B/5	R	0	6/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TOTALS				98/25	19	5	0	9	3	0	3	0	1	0	1	0	0	0	0	1	0
P2000	C/1	R	I	9/5	0	0	0	0	0	3	1	0	1	0	0	0	0	0	0	0	0
P2000	C/1	R	0	11/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
P2000	C/2	R	I	12/5	0	0	0	0	0	4	0	0	1	0	0	0	0	0	0	0	0
P2000	C/2	R	0	6/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TOTALS				38/10	0	0	0	0	0	7	1	0	2	0	0	0	0	0	0	0	0

* THE CLASS "R" DEVICE SAMPLE SIZE WAS REDUCED SUBSEQUENT TO THE INITIAL TEST. THE INITIAL SAMPLE/TEST SAMPLE COLUMN SHOWS THE QUANTITY OF DEVICES SUBJECTED TO INITIAL TEST OVER THE QUANTITY OF DEVICES THAT WERE SUBJECTED TO SUBSEQUENT TESTING.

TABLE 5.4 - P2000 AND 5R100 FAILURES THROUGH EVALUATION TEST SEQUENCE

A physics of failure determination was performed on all devices which failed during the evaluation program. The analysis included the opening and the microprobing of all devices where meaningful information could be obtained. The results of this portion of the evaluation are summarized in Table 5.5.

5.2.2 MOSPA Data Summary

The MOSPA test vehicles were incorporated into each P2000 wafer to determine the stability of the fundemental bulk and surface parameters of each MOS wafer. Because the Phase 1 evaluation showed that these parameters drift between wafer mapping and post encapsulation all of the Phase 3 measurements were performed subsequent to encapsulation. The parameters evaluated are summarized in Table 5.6, and the mean values obtained are summarized in Table 5.7. Similar data was obtained on the 5R100 wafers during the Phase 1 evaluation and is contained in the interim scientic report on the MOS Phase 1 evaluation.

5.2.3 MOSPB Data Summary

The MOSPB vehicles were incorporated into each P2000 wafer to determine if the metalization and oxide integrity was adequate to insure device reliability. Encapsulated devices from each wafer from each lot were subjected to electromigration and thermal stress testing in accordance with the MOS Evaluation Plan to evaluate both the aluminium stripe and capacitor structures of the test pattern. These test structures were also used to measure metalization and oxide thicknesses, metalization widths and diffusion widths. The data derived during the evaluation of the test structures is shown in the tables and figures on the following pages as indicated:

TABLE	DESCRIPTION
5.8	Metalization and diffusion line widths
5.9	Metalization and Oxide thicknesses
5.10	Summary-Oxide Breakdown voltage prior and subsequent to thermal screening

TYPE	LOT	VISUAL CLASS	SERIAL NUMBER	FAILED AT	FAILURE MODE	FAILURE MECHANISM
5R100	2	B	231	POST 100% SCREENS	NO OUTPUT - SIDE 1	INTERNAL GATE TO GND. SHORT
5R100	2	B	232	POST 100% SCREENS	HIGH LEAKAGE & MCF	CP1 TO GND. SHORT
5R100	2	B	234	POST 100% SCREENS	HIGH LEAKAGE & MCF	CP1 TO GND. SHORT
5R100	2	B	239	POST 100% SCREENS	HIGH LEAKAGE & MCF	CP1 TO GND. SHORT
5R100	3	A	950	POST 100% SCREENS	HIGH MCF	RECOVERED DURING 300°C BAKE
5R100	3	B	135	POST 100% SCREENS	HIGH MCF	RECOVERED DURING 300°C BAKE
5R100	3	B	556	POST 100% SCREENS	HIGH MCF	RECOVERED DURING 300°C BAKE
5R100	3	B	636	POST 100% SCREENS	HIGH MCF	RECOVERED DURING 300°C BAKE
5R100	3	B	737	POST 100% SCREENS	HIGH MCF	RECOVERED DURING 300°C BAKE
5R100	3	B	039	POST 100% SCREENS	HIGH LEAKAGE	INTERNAL GATE TO GND. SHORT
P2000	A	B	214	POST 100% SCREENS	HIGH MCF	CP2 TO VDD SHORT
P2000	A	R	119	POST 100% SCREENS	HIGH LEAKAGE	RECOVERED DURING 300°C BAKE
P2000	B	A	110	POST 100% SCREENS	NO OUTPUT - SIDE 1	OPEN BOND-INPUT TO SIDE 1
P2000	B	A	202	POST 100% SCREENS	HIGH LEAKAGE	INTERNAL GATE TO GND. SHORT
P2000	B	B	328	POST 100% SCREENS	HIGH LEAKAGE	OUTPUT BUFFER CAPACITOR SHORT
P2000	B	B	511	POST 100% SCREENS	HIGH MCF	RECOVERED DURING 300°C BAKE
P2000	B	B	534	POST 100% SCREENS	HIGH LEAKAGE MCF	OUTPUT BUFFER CAPACITOR SHORT
P2000	C	B	109	POST 100% SCREENS	FAILED FUNCTIONAL	OPEN VDD LINE
P2000	C	B	111	POST 100% SCREENS	HIGH MCF	RECOVERED DURING 300°C BAKE
P2000	C	B	131	POST 100% SCREENS	HIGH LEAKAGE	INTERNAL GATE TO GND. SHORT
P2000	C	B	235	POST 100% SCREENS	HIGH LEAKAGE	UNKNOWN.
5R100	2	A	344	340 HOUR BURN-IN	HIGH LEAKAGE & MCF	BIT 1 GATE TO GND. SHORT
5R100	2	A	345	340 HOUR BURN-IN	HIGH LEAKAGE & MCF	CP1 TO GND. SHORT
5R100	2	A	346	340 HOUR BURN-IN	HIGH LEAKAGE & MCF	BIT 1 GATE TO GND. SHORT
5R100	2	A	339	340 HOUR BURN-IN	HIGH LEAKAGE & MCF	BIT 1 GATE TO GND. SHORT
5R100	2	A	659	340 HOUR BURN-IN	HIGH LEAKAGE & MCF	BIT 1 GATE TO GND. SHORT
5R100	2	A	751	340 HOUR BURN-IN	FAIL MCF	BITS DROPPED - CAUSE UNKNOWN
5R100	2	B	134	340 HOUR BURN-IN	HIGH LEAKAGE & MCF	BIT 1 GATE TO GND. SHORT
5R100	2	R	333	340 HOUR BURN-IN	HIGH MCF	RECOVERED DURING 300°C BAKE
5R100	2	R	337	340 HOUR BURN-IN	NO OUTPUT	BIT 31, GATE TO GND. SHORT
5R100	2	R	342	340 HOUR BURN-IN	HIGH LEAKAGE	INPUT PROTECTION DEVICE SHORT
5R100	3	A	138	340 HOUR BURN-IN	HIGH LEAKAGE	INPUT PROTECTION DEVICE SHORT
5R100	3	A	549	340 HOUR BURN-IN	FAILED FUNCTIONAL	OPEN GROUND LINE
5R100	3	A	842	340 HOUR BURN-IN	HIGH LEAKAGE	CP1 TO GND. SHORT
5R100	3	R	140	340 HOUR BURN-IN	HIGH LEAKAGE	INPUT PROTECTION DEVICE SHORT
P2000	A	A	103	340 HOUR BURN-IN	FAILED FUNCTIONAL	PROBABLE SHORT IN OUTPUT BUFFER CIRCUIT
P2000	A	A	404	340 HOUR BURN-IN	HIGH LEAKAGE	INPUT PROTECTION DEVICE SHORT
P2000	A	A	501	340 HOUR BURN-IN	FAILED FUNCTIONAL	SHORT IN OUTPUT BUFFER CIRCUIT
P2000	A	A	505	340 HOUR BURN-IN	FAILED FUNCTIONAL	INTERNAL GATE TO GND. SHORT
P2000	A	A	527	340 HOUR BURN-IN	FAILED FUNCTIONAL	SHORT IN OUTPUT BUFFER CIRCUIT
P2000	A	B	114	340 HOUR BURN-IN	HIGH LEAKAGE & MCF	CP2 TO OUTPUT SHORT
P2000	A	B	217	340 HOUR BURN-IN	HIGH MCF	SHORT IN BUFFER CIRCUIT CAPACITOR
P2000	A	B	331	340 HOUR BURN-IN	HIGH MCF	SHORT IN BUFFER CIRCUIT CAPACITOR
P2000	A	B	337	340 HOUR BURN-IN	HIGH MCF	SHORT IN BUFFER CIRCUIT CAPACITOR
P2000	A	B	412	340 HOUR BURN-IN	HIGH MCF	SHORT IN BUFFER CIRCUIT CAPACITOR
P2000	A	B	431	340 HOUR BURN-IN	HIGH MCF	SHORT IN BUFFER CIRCUIT CAPACITOR
P2000	A	B	504	340 HOUR BURN-IN	HIGH LEAKAGE	INPUT PROTECTION DEVICE SHORT
P2000	A	B	507	340 HOUR BURN-IN	HIGH MCF	SHORT IN BUFFER CIRCUIT CAPACITOR
P2000	A	B	508	340 HOUR BURN-IN	HIGH MCF	SHORT IN BUFFER CIRCUIT CAPACITOR
P2000	A	B	515	340 HOUR BURN-IN	HIGH MCF	SHORT IN BUFFER CIRCUIT CAPACITOR
P2000	B	A	427	340 HOUR BURN-IN	HIGH MCF	SHORT IN BUFFER CIRCUIT CAPACITOR
P2000	B	A	502	340 HOUR BURN-IN	HIGH MCF	SHORT IN BUFFER CIRCUIT CAPACITOR
P2000	B	B	414	340 HOUR BURN-IN	HIGH LEAKAGE	INPUT PROTECTION DEVICE SHORT
P2000	B	B	433	340 HOUR BURN-IN	HIGH LEAKAGE & MCF	INTERNAL GATE TO GND. SHORT
P2000	B	B	207	340 HOUR BURN-IN	HIGH LEAKAGE	INPUT PROTECTION DEVICE SHORT
P2000	B	B	504	340 HOUR BURN-IN	HIGH MCF	SHORT IN BUFFER CIRCUIT CAPACITOR
P2000	B	B	505	340 HOUR BURN-IN	HIGH MCF	SHORT IN BUFFER CIRCUIT CAPACITOR
P2000	B	B	506	340 HOUR BURN-IN	HIGH MCF	SHORT IN BUFFER CIRCUIT CAPACITOR
P2000	C	A	107	340 HOUR BURN-IN	HIGH MCF	SHORT IN BUFFER CIRCUIT CAPACITOR
P2000	C	A	128	340 HOUR BURN-IN	HIGH LEAKAGE	INPUT PROTECTION DEVICE SHORT
P2000	C	A	230	340 HOUR BURN-IN	HIGH LEAKAGE	INPUT PROTECTION DEVICE SHORT
5R100	2	A	233	POST 2000 HR. LIFE	HIGH MCF	RECOVERED DURING 300°C BAKE
P2000	A	B	137	POST 2000 HR. LIFE	HIGH LEAKAGE	RECOVERED DURING 300°C BAKE
P2000	B	B	330	POST 2000 HR. LIFE	HIGH LEAKAGE	INPUT PROTECTION DEVICE SHORT
P2000	B	B	331	POST 2000 HR. LIFE	HIGH MCF	RECOVERED DURING 300°C BAKE
P2000	B	B	431	POST 2000 HR. LIFE	HIGH MCF	RECOVERED DURING 300°C BAKE

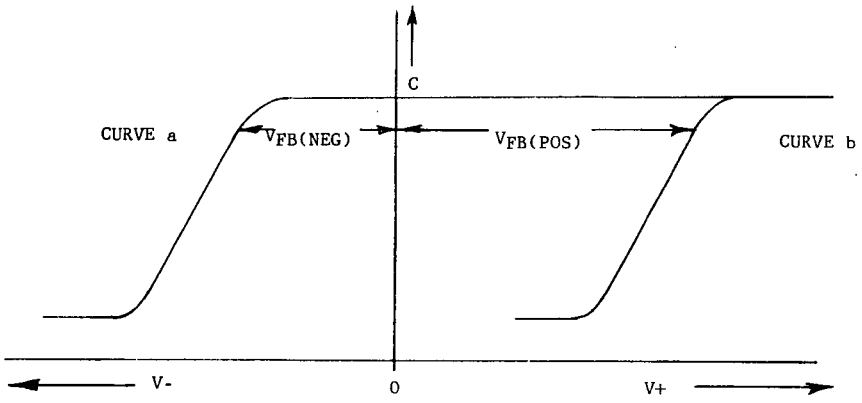
TABLE 5.5 - MOS 5R100 AND P2000 FAILURE ANALYSIS SUMMARY

TEST STRUCTURE	MEASUREMENT & PARAMETER SYMBOLS	DATA OBTAINED FROM MEASUREMENT
MOS CAPACITOR (FIELD OXIDE DIELECTRIC)	C-V CHARACTERISTICS a. After -36V, 300°C Drift (VFB1AN) b. After +36V, 300°C Drift (VFB1AP) c. After 0V, 300°C Drift (VFB1A0)	FLAT BAND VOLTAGE DOPING DENSITY OXIDE THICKNESS Q_{SS}, Q_O, AND Q_{NEG} DENSITIES
MOS CAPACITOR (GATE OXIDE DIELECTRIC)	C-V CHARACTERISTICS a. After -12V, 300°C Drift (VFB2AN) b. After +12V, 300°C Drife (VFB2AP) c. After 0V, 300°C Drift (VFB2A0)	FLAT BAND VOLTAGE DOPING DENSITY OXIDE THICKNESS Q_{SS}, Q_O, AND Q_{NEG} DENSITIES
LARGE AREA p-n JUNCTION DIODE	a. Reverse Current at -20V (IR3A) b. Breakdown Voltage at 10μA (BV3A)	MEASURE OF SURFACE CONDITIONS
LATERAL DIFFUSION	PUNCH THROUGH VOLTAGE AT 10μA. FOR EACH OF THE 5 DIFFERENT DESIGN SEPERATIONS. (VPT)	EXTENT OF LATERIAL DIFFUSION.
MOS TRANSISTOR (FIELD OXIDE GATE)	INVERSION VOLTAGE a. After -36V, 300°C Drift (V6AN) b. After 0V, 300°C Drift (V6A0)	EFFECT OF MOBILE CHARGE ON V_{GST} OF FIELD OXIDE TRANSISTOR
MOS TRANSISTOR (GATE OXIDE GATE)	INVERSION VOLTAGE a. After -12V, 300°C Drift (V7AN) b. After 0V, 300°C Drift (V7A0)	EFFECT OF MOBILE CHARGE ON V_{GST} OF GATE OXIDE TRANSISTOR
LATERIAL BIPOLAR TRANSISTOR	h_{FE} AT $5V_{CE}$ AND 50μA I_C (H_{FEL})	MEASURE OF FAST STATE DENSITY

TABLE 5.6 - MOSPA EVALUATIONS

LOT/WAFER	SAMPLE	MEAN DOPING DENSITY $X10^{15}$ ATOMS/CM^2	MEAN FIELD OXIDE THICKNESS - Å	MEAN Q_{SS} $X10^{11}$(CHARGES/CM^2)	MEAN Q_{NEG} $X10^{11}$ (CHARGES/CM^2)	MEAN Q_O X 10^{11} (CHARGES/CM^2)	MEAN V_{FB1AN} (VOLTS)	MEAN V_{FB1AO} (VOLTS)	MEAN V_{FB1AP} (VOLTS)	MEAN DOPING DENSITY $X10^{15}$ ATOMS/CM^2	MEAN GATE OXIDE THICKNESS - Å	MEAN Q_{SS} $X10^{11}$(CHARGES/CM^2)	V_{FB2AN}	V_{FB2AO}	V_{FB2AP}
A/1	4	1.5	13.8K	3.6	3.0	4.6	- 4.2	-22.8	- 5.1	1.8	1.30K	1.2	-1.4	-1.0	-1.0
A/2	4	1.6	13.7K	3.1	2.3	3.0	- 5.0	-19.3	-38.2	1.9	1.30K	1.1	-1.0	-0.9	-0.9
A/3	4	1.4	13.6K	3.4	2.4	1.9	- 6.3	-21.0	-32.6	1.8	1.34K	1.1	-1.2	-0.9	-1.0
A/4	4	1.3	13.6K	3.0	2.6	3.7	- 4.5	-20.2	-41.6	1.8	1.30K	1.0	-1.2	-0.9	-1.0
A/5	4	1.4	13.5K	2.7	1.7	3.0	- 6.1	-16.8	-35.6	1.8	1.30K	1.3	-1.2	-1.1	-1.0
B/1	4	1.6	13.9K	2.3	3.2	4.1	+ 4.7	-15.1	-41.0	1.9	1.30K	1.1	-1.1	-0.9	-0.8
B/2	4	1.5	13.7K	2.1	3.0	3.1	+ 5.5	-13.2	-32.0	1.7	1.30K	1.1	-1.1	-1.0	-1.0
B/3	4	1.6	14.0K	2.3	4.7	2.5	+15.2	-14.7	-30.3	1.6	1.35K	1.5	-1.2	-1.2	-1.2
B/4	4	1.7	13.9K	3.1	2.2	2.2	- 5.5	-19.8	-32.3	1.8	1.30K	1.3	-1.3	-1.1	-1.2
C/1	4	1.5	13.5K	3.4	4.4	3.2	+ 8.8	-18.5	-38.2	1.6	1.30K	7.3	-3.3	-4.6	-1.3
C/2	4	1.8	13.7K	2.0	1.7	2.6	- 3.1	-14.1	-29.6	1.7	1.30K	7.1	-4.5	-4.5	-1.3

LOT	SAMPLE	MEAN IR3A (nA)	SAMPLE	MEAN BV3A (VOLTS)	SAMPLE	MEAN V_{PT} (0.3 mil structure) (VOLTS)	SAMPLE	MEAN V6AO (VOLTS)	SAMPLE	MEAN V6AN (VOLTS)	SAMPLE	MEAN V7AO (VOLTS)	SAMPLE	MEAN V7AN (VOLTS)	SAMPLE	MEAN h_{FEL}
A	17	0.55	17	96.0	13	5.95	19	32.12	19	24.55	20	3.08	20	2.60	19	0.37
B	18	0.98	18	92.0	13	6.50	16	27.15	16	14.38	20	3.03	20	1.52	16	0.42
C	7	0.99	7	100.0	8	3.56	7	30.82	8	12.06	5	1.26	7	1.00	8	0.35



$V_{FB(NEG)}$ is a negative flat band voltage.
$V_{FB(POS)}$ is a positive flat band voltage.

SIGN CONVENTION USED FOR FLAT BAND VOLTAGE

TABLE 5.7 - SUMMARY OF MEAN VALUES OBTAINED FROM THE RIIT MOSPA VEHICLES DURING POST SCREEN EVALUATION

	LOT 12-0-32 (A)				LOT 13-0-32 (B)				LOT 14-0-32 (C)			
	LOCATION	METAL WIDTH	DIFFUSION WIDTH	VISUAL	LOCATION	METAL WIDTH	DIFFUSION WIDTH	VISUAL	LOCATION	METAL WIDTH	DIFFUSION WIDTH	VISUAL
WAFER 1	IN	0.27 MILS	1.02	NOTE A	IN	0.30	1.02	NOTE A	IN	0.30	1.02	NOTE A
WAFER 1	IN	0.30 MILS	1.00	NOTE A	IN	0.25	1.07	NOTE A	IN	0.27	1.06	NOTE A
WAFER 1	OUT	0.25 MILS	1.06	NOTE A	IN	0.25	1.02	NOTE A	OUT	0.30	1.06	NOTE A
WAFER 1	OUT	0.30 MILS	1.02	NOTE A	IN	0.25	1.02	NOTE A	OUT	0.25	1.01	NOTE A
WAFER 2	IN	0.29 MILS	1.02	NOTE A	IN	0.27	1.02	NOTE A	IN	0.25	1.06	NOTE A
WAFER 2	IN	0.35 MILS	1.02	NOTE A	OUT	0.29	1.06	NOTE A	IN	0.29	1.01	NOTE A
WAFER 2	OUT	0.35 MILS	0.97	NOTE A	OUT	0.30	1.06	NOTE A	OUT	0.29	1.08	NOTE A&B
WAFER 2	OUT	0.32 MILS	1.02	NOTE A	OUT	0.27	1.06	NOTE A	OUT	0.29	1.02	NOTE A&B
WAFER 3		----			--							
WAFER 3		----			--							
WAFER 3		----			--							
WAFER 3		----			--							
WAFER 4		----			IN	0.29	1.06	NOTE A				
WAFER 4		----			OUT	0.25	0.97	NOTE A				
WAFER 4		----			--							
WAFER 4		----			--							
WAFER 5	OUT	0.29	1.02	NOTE A	IN	0.27	1.06	GOOD				
WAFER 5	OUT	0.29	1.06	NOTE A	IN	0.27	1.06	GOOD				
WAFER 5	OUT	0.27	1.00	NOTE A	OUT	0.25	1.06	GOOD				
WAFER 5	OUT	0.25	1.08	NOTE A	OUT	0.25	1.07	GOOD				
MEAN VALUE		0.294	1.024			0.269	1.043			0.280	1.04	

NOTES: "A" - MARGINAL METALIZATION ALLIGNMENT IN ONE DIRECTION, SUCH THAT CONTACT CUTS ARE NOT COMPLETELY COVERED AND METAL STRIPE DOES NOT COMPLETELY CROSS OXIDE STEPS.

"B" - POOR CONTACT CUTS - CONTACT CUTS ARE SMALL AND NOT COMPLETE ETCHED.

TABLE 5.8 - METALIZATION AND DIFFUSION LINE WIDTH MEASUREMENTS - MOSPB

LOT	LOT CODE	SAMPLE	MEAN METALIZATION THICKNESS Å	MEAN GATE OXIDE THICKNESS Å	MEAN FIELD OXIDE THICKNESS Å	MEAN VAPOX THICKNESS Å
12-0-32	A	12	10,600	1500	14,700	5900
13-0-32	B	11	9,270	1500	14,800	4500
14-0-32	C	4	11,800	1500	14,700	5900
PROCESS SPECIFICATION RANGE			8,000 15,000	1475 1550	13,500 15,500	11000 13000

TABLE 5.9 - MEAN METALIZATION AND OXIDE THICKNESS MEASUREMENTS - MOSPB

LOT	LOT CODE	TEST	MEAN V_{OFBL} (VOLTS) CAPACITOR AREA = 100 MIL^2						MEAN V_{OFBM} (VOLTS) CAPACITOR AREA = 10 MIL^2						MEAN V_{OFBS} (VOLTS) CAPACITOR AREA = 1 MIL^2					
			n	INSIDE	n	OUTSIDE	n	COMBINED	n	INSIDE	n	OUTSIDE	n	COMBINED	n	INSIDE	n	OUTSIDE	n	COMBINED
12-0-32	A	POST SCREEN	-	-	-	-	17	76	-	-	-	-	17	85	-	-	-	-	17	89
		POST THERMAL STRESS	10	68	10	72	20	70	10	82	10	100	20	91	10	86	10	96	20	91
13-0-32	B	POST SCREEN	-	-	-	-	19	70	-	-	-	-	19	89	-	-	-	-	19	86
		POST THERMAL STRESS	9	75	9	88	18	82	9	78	9	108	18	93	9	98	9	109	18	103
14-0-32	C	POST SCREEN	-	-	-	-	8	90	-	-	-	-	8	90	-	-	-	-	8	98
		POST THERMAL STRESS	4	85	4	90	8	88	4	110	4	102	8	106	4	113	4	107	8	110

TABLE 5.10 - SUMMARY - OXIDE BREAKDOWN VOLTAGE, PRIOR AND SUBSEQUENT TO THE THERMAL SCREENING SEQUENCE PERFORMED ON THE MOSPB VEHICLES.

TABLE	DESCRIPTION
5.11	MOSPB Thermal Stress Sequence Failure Summary
5.12	MOSPB Electromigration Stress Failure Summary

FIGURE	DESCRIPTION
5.2	Mean Value Plot of Resistance of Test Structures R_{MCC}, R_{MS}, and R_{MP} versus Steps of Thermal Stress Sequence
5.3	Mean Value Plot of Leakage Current Across Capacitor Structures versus Steps of Thermal Stress Sequence

The physics of failure analysis of all MOSBB device from which meaningful information could be derived is shown in summary form in Table 5.13.

5.3 MOS TEST VEHICLES CORRELATION

The following subsections show the degree of correlcation observed between the results of the preseal visual inspection and the 5R100 and P2000 failures incurred during the Phase 3 test program, as well as the degree of correlation observed between the measured test pattern parameters and the 5R100 and P2000 failures incurred during the Phase 3 evaluation. All of the Regrown IIT MOS test pattern measurements were made during the Phase 3 evaluation because these patterns were incorporated into the Regrown IIT P2000 mask sets which were fabricated for use in the Phase 3 evaluation. The Regrown II MOS test pattern measurements however, since these patterns were incorporated into the Regrown II 5R100 masks fabricated for use in both the Phase 1 and Phase 3 evaluations, were all performed during the Phase 1 evaluation. The data obtained from the Regrown IIT MOS test patterns is contained in Sections 5.2.2 and 5.2.3 of this report. The data obtained from the Regrown II MOS test patterns is contained in the Interim Scientific Report on the Phase 1 - MOS Evaluations for this program.

5.3.1 Correlation of 5R100 and P2000 Failures With Visual Inspection Results

Figure 5.4 shows the final electrical test yield of the 5R100 and

LOT	LOT CODE	SAMPLE	POST THERMAL SHOCK 1*	POST 150°C STORAGE 1, 340 HRS.	POST THERMAL SHOCK 2*	POST 150°C STORAGE 2, 340 HRS.	POST THERMAL SHOCK 3*	POST 150°C STORAGE 3, 340 HRS.	TOTALS	COMMENTS
12-0-32	A	20	0	0	0	0	0	1	1	SHORTED V_{CM} CAPACITOR
13-0-32	B	20	0	0	0	0	0	0	0	
14-0-32	C	8	0	0	0	0	0	0	0	

TABLE 5.11 - MOSPB THERMAL STRESS SEQUENCE FAILURE SUMMARY

ELECTROMIGRATION STRESS

(STRUCTURES R_{MP} AND R_{MS})
I = 66 mA, TEMPERATURE = 125°C
J = 7.5 X 10^5 AMP/CM^2

SAMPLE	LOT	S/N OF FAILURE	HOURS TO FAILURE
15	A	35	55
	A	513	102
	B	50	104
	B	15	106
	B	113	122
	A	42	167
	B	317	188
	C	215	216
	A	114	282
	B	26	301
	A	214	345

ELECTROMIGRATION STRESS

(STRUCTURES R_{MP} AND R_{MS})
I = 89 mA, TEMPERATURE = 125°C
J = 1.0 X 10^6 AMP/CM^2 (NOMINAL)

SAMPLE	LOT	S/N OF FAILURE	HOURS TO FAILURE
14	B	36	27
	C	24	34
	A	313	41
	C	113	51
	B	16	63
	A	57	94
	B	414	96
	C	217	99
	A	210	125
	B	22	126
	A	15	127

ELECTROMIGRATION STRESS

(STRUCTURES R_{MP} AND R_{MS})
I = 158 mA, TEMPERATURE = 125°C
J = 2.0 X 10^6 AMP/CM^2

SAMPLE	LOT	S/N OF FAILURE	HOURS TO FAILURE
14	B	311	1
	B	419	10.5
	A	112	11.5
	B	41	12.5
	A	33	14.0
	A	58	15.5
	A	413	16.0
	B	112	18.5
	A	314	21.0
	C	113	21.5
	B	24	23.0
	B	59	27.0
	C	26	39.0
	A	213	45.0

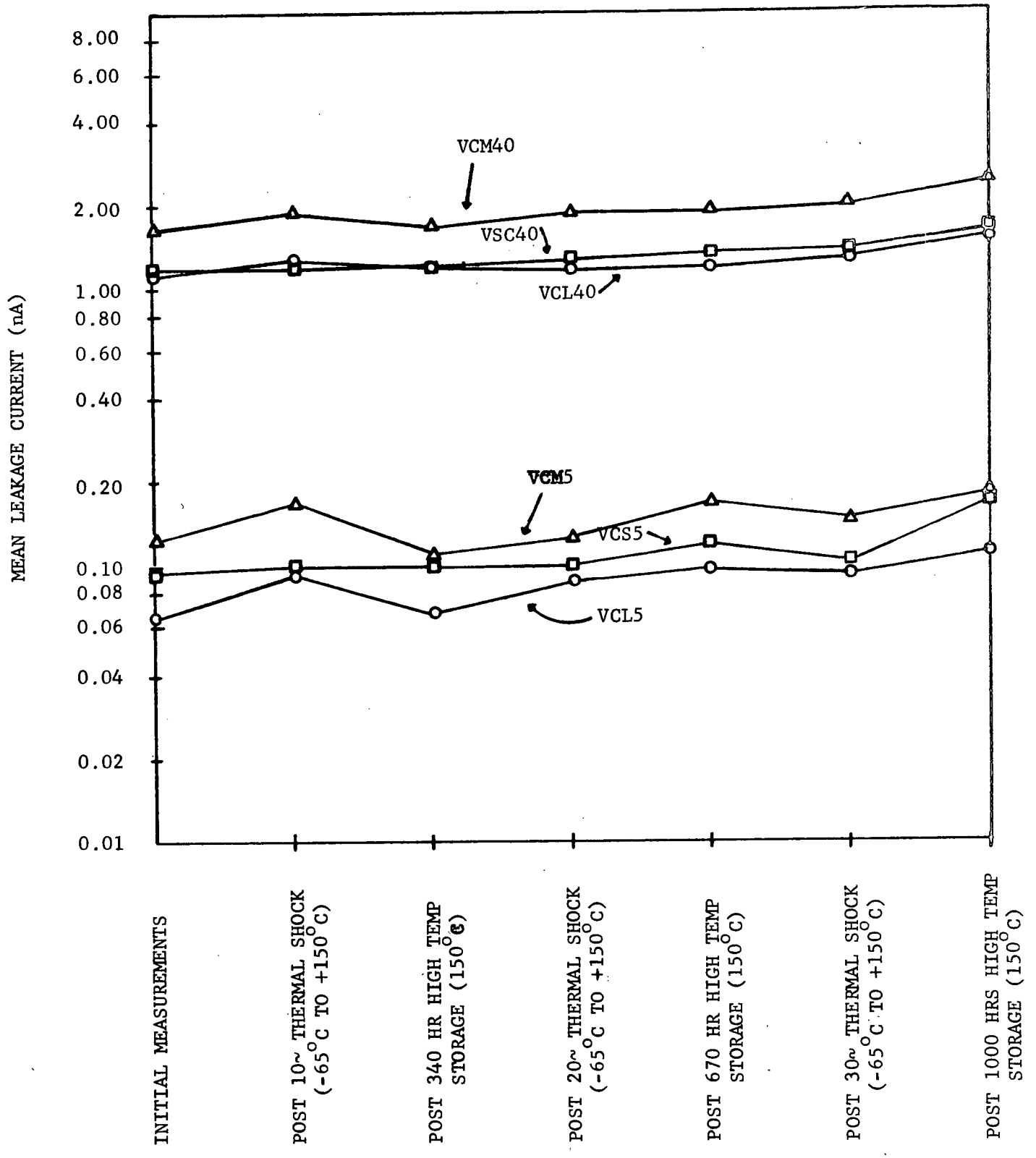
NOTE: Serial Number indicates wafer and portion of wafer from which each device was obtained according to the following code:

a. 2 digit serialization, the first digit is the wafer number, the second is the device number. All devices with two digit serial numbers came from the inner portion of the wafer.

b. 3 digit serialization, the first digit is the wafer number, the second and third digits are the device number. All devices with 3 digit serial numbers came from the outer portion of the wafer.

TABLE 5.12 - SUMMARY OF MOSPB ELECTROMIGRATION STRESS FAILURES

FIGURE 5.2 - MEAN RESISTANCE THROUGH THERMAL STRESS SEQUENCE



MEAN LEAKAGE CURRENT OF CAPACITOR STRUCTURES
CS, CM AND CL OF MOSPB
vs
STEPS OF THERMAL STRESS SEQUENCE

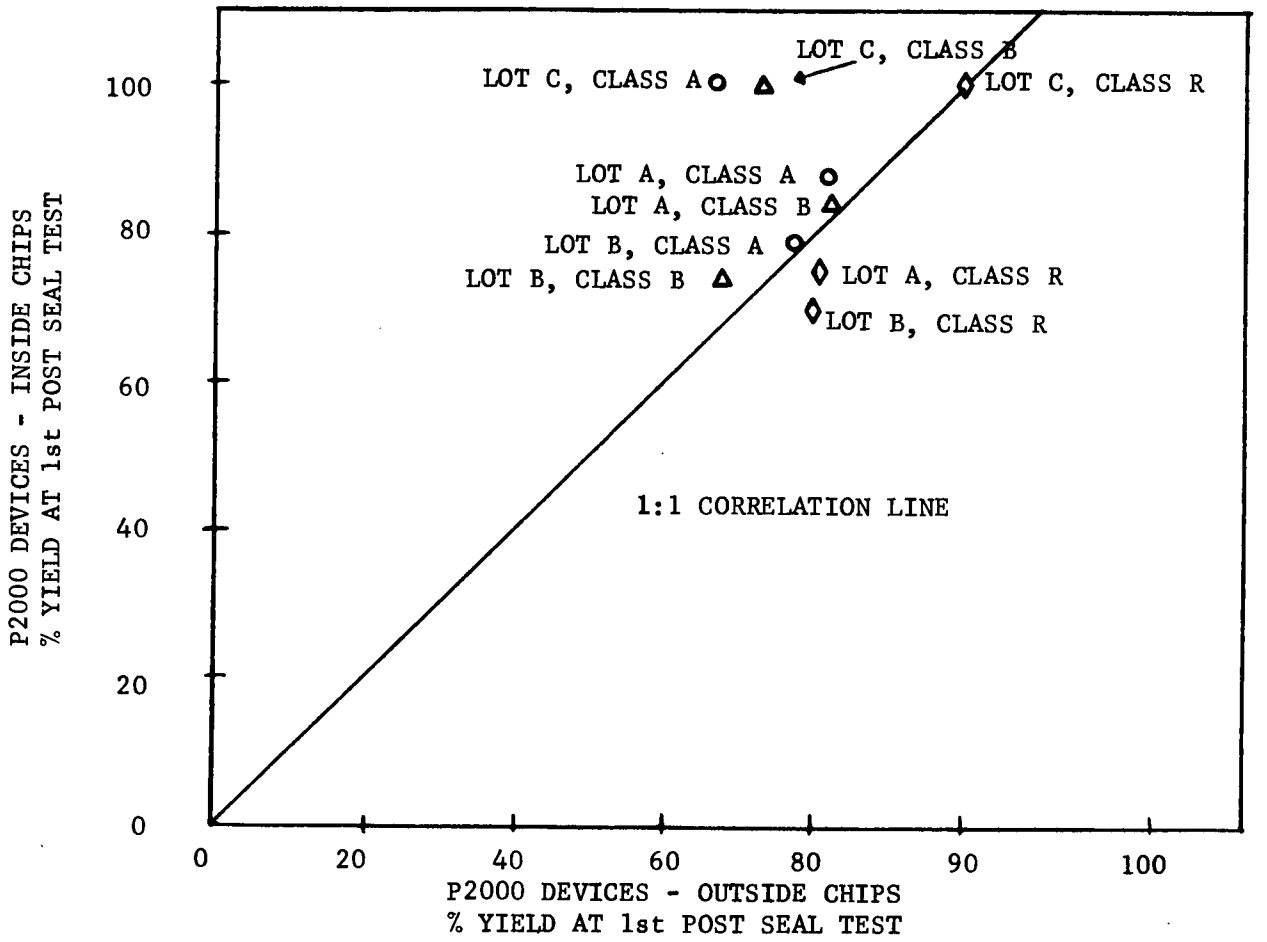
FIGURE 5.3 - CAPACITOR LEAKAGE THROUGH THERMAL STRESS

S/N	LOT CODE	ELECTROMIGRATION STRESS CURRENT DENSITY-AMP/cm^2	STRUCTURE FAILED	MECHANISM
58	A	$2X10^6$	R_{MS}	OPEN METAL AT OXIDE STEP
112	A	$2X10^6$	R_{MS}	OPEN METAL BETWEEN OXIDE STEPS
213	A	$2X10^6$	R_{MS}	OPEN METAL AT OXIDE STEP
24	B	$2X10^6$	R_{MS}	NO VISIBLE DEFECT
41	B	$2X10^6$	R_{MP}	OPEN METAL AT SCRATCH
59	B	$2X10^6$	R_{MP}	BURNED OPEN METAL, NO EVIDENCE OF DEFECT IN METAL PRIOR TO FAILURE
311	B	$2X10^6$	R_{MP}	BURNED OPEN METAL, NO EVIDENCE OF DEFECT IN METAL PRIOR TO FAILURE
15	A	$1X10^6$	R_{MS}	OPEN METAL NEAR BONDING PAD
57	A	$1X10^6$	R_{MS}	OPEN METAL AT OXIDE STEP
210	A	$1X10^6$	R_{MS}	NO VISIBLE DEFECT
215	A	$1X10^6$	R_{MS}	POSSIBLE OPEN AT OXIDE STEP
313	A	$1X10^6$	R_{MS}	NO VISIBLE DEFECT
16	B	$1X10^6$	R_{MP}	NO VISIBLE DEFECT
414	B	$1X10^6$	R_{MS}	OPEN METAL AT OXIDE STEP
15	C	$1X10^6$	R_{MS}	NO VISIBLE DEFECT
24	C	$1X10^6$	R_{MS}	NO VISIBLE DEFECT

TABLE 5.13 - FAILURE ANALYSIS SUMMARY - MOSPB

P2000 devices as a function of the visual category to which the devices were assigned during the preseal visual inspection. This figure also shows the correlation between the final test yields of the P2000 devices from the inner portion of the wafer as compared to the P2000 devices from the outer portions of the wafer. In general, there is no significant yield difference between the Class "A", Class "B", and the Class "R" visual devices. The correlation plot of Figure 5.4 does not show any significant difference between the yields of devices from the center of the wafer as opposed to devices from the periphery of the wafer. Figure 5.5 shows the percentage of failures at post seal electrical test and through screening and life test as a function of visual category and P2000 or 5R100 lot from which the devices were obtained. The plot for the percentage of failures at the first post seal electrical test does not show any general appreciable indication of improved yield as a result of the more stringent preseal visual inspection criteria applied to the Class "A" devices, although the Class "A" device failure percentages are in general lower than the failure percentages for the Class "B" devices. The failure percentages for the Class "R" however, because they are quite similar to the Class "A" devices negate any interpretation of the small differences between the Class "A" and Class "B" devices.

The plot of Figure 5.5 for the percentage of failures through screening and life testing yields some indication that the Class "A" visual criteria has some effect on the improvement of reliability, but even in this case the high failure percentage of the Lot B P2000 Class "A" devices, and the low failure percentage of the Lot 3, 5R100 Class "R" devices negate any general statements that the more stringent visual inspection criteria have improved reliability for these particular test vehicles. The only explanation for the fact that improved reliability was not in general observed for the devices subjected to the more stringent visual inspection criteria is that the criteria is not sensitive to the mechanisms that resulted in the



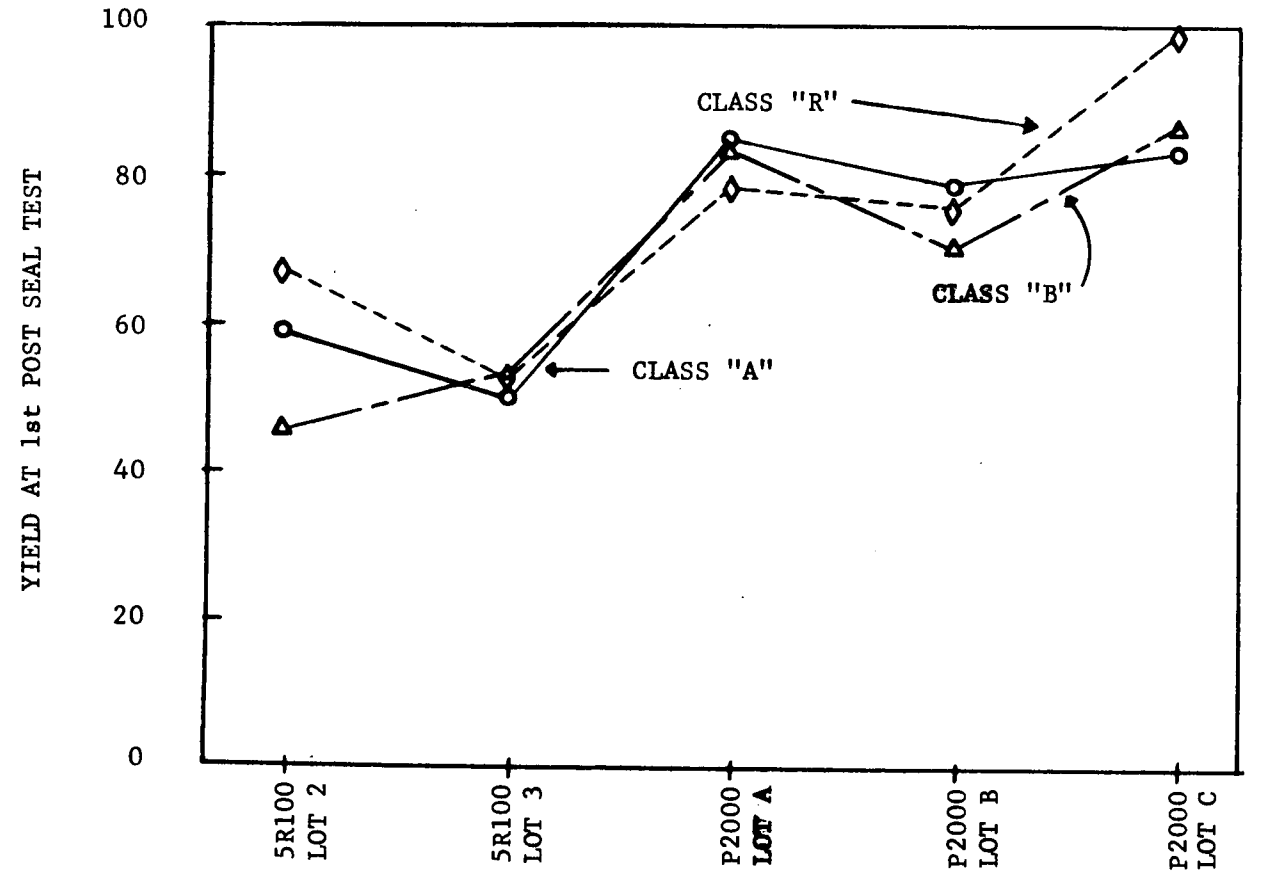


FIGURE 5.4 - FINAL TEST YIELDS AS FUNCTION OF VISUAL CLASSIFICATION AND WAFER LOCATION

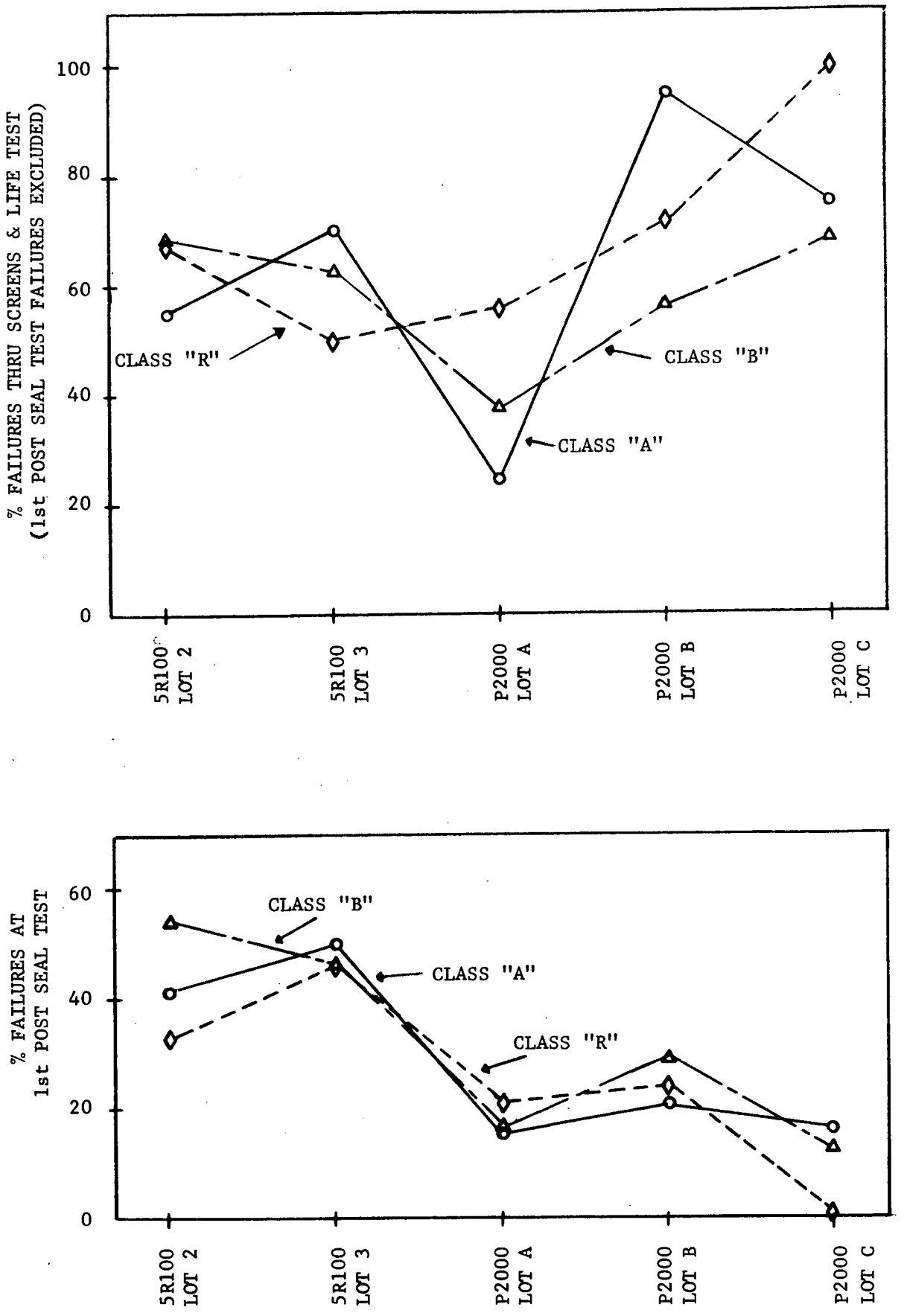


FIGURE 5.5 - FAILURE PERCENTAGE AS A FUNCTION OF PRE SEAL VISUAL CLASSIFICATION

failure of these MOS devices. Visual inspection criteria can be utilized to screen devices with visual metalization, diffusion, oxide or bonding defects, provided they are large enough to be resolved at the magnification utilized. The magnifications specified in the preseal visual inspection criteria of Appendix A are sufficient to screen any metalization or diffusion or bonding anomalies that can present reliability hazzards. Gate oxide shorts however, because of the thin oxide used over MOS gates, can occur at relatively small defects and may not be observed at a practical magnification for 100% preseal visual inspection.

It is our opinion that the highest practical magnification for preseal visual inspection is 200X. Magnifications in excess of 200X require multiple scanning techniques where chip areas are liable to be overlooked. Also the objectives used at higher than 200X magnification have short working distances with a very shallow depths of field. Because of these restrictions the possibility of chip or bonding wire damage due to inadvertent contact between the microscope objective and the device under inspection is quite high therefore, higher than 200X microscopic inspection should not be used for preseal inspection. Additionally, MOS devices are sensitive to inversion phenomena and the charge densities responsible for this difficulty can not be microscopically observed.

The fact that there is no definite correlation between the stringency of the preseal visual inspection criteria and the failures incurred during this program does not infer the criteria should be modified. It infers only that the failure mechanisms for which the inspection criteria is sensitive were not present in the vehicles used during this program. Had these types of defects been present the criteria would have been effective, and it is our opinion the criteria as now written is not only adequate but is also necessary to screen devices where visual failure mechanisms are present.

5.3.2 Correlation of 5R100 and P2000 Failures With MCF, MVVO, and MCVO Measurements, and With The Input Stress and Stress Functional Test Data.

Minimum Clock Frequency Measurements (MCF).

Minimum V_{DD} Voltage of operation measurements (MVVO), and Minimum Clock Voltage of operation measurements were made on all 5R100 and P2000 devices subjected to the Phase 3 evaluations. There was no significant difference in the MVVO and the MCVO measurements for any of the device types regardless of the visual category. The MCF measurements exhibited appreciable differences between the 5R100 and the P2000 device types, and also exhibited significant differences between individual wafers within a given lot. This data is summarized in Table 5.14, however, there was no correlation between the MCF values measured and the failure rate of either the 5R100 or the P2000 devices, except that devices which exhibited high MCF values (>2000 Hz at room temperature) subsequently failed during the test sequence.

Only 10 devices failed the stress functional test performed at 25°C subsequent to the 100% environmental screens. The intent of this test was to stress the internal nodes of the device and cause failure of those devices with internal node oxide weaknesses. The input stress test performed prior to the first post seal D.C. electrical measurements does not stress the internal nodes of the device because of the circuit configurations of both the 5R100 and the P2000 devices. Comparison of the stress functional and the burn-in circuit however, shows that burn-in test to which the devices were subjected was in effect a more severe extension of the stress functional test because the voltages applied in both cases were identical, but the burn-in was performed at 125°C for 340 hours as compared to the 25°C, several second duration stress functional test. The conditions are compared below:

TEST	V_{DD}	V_{CP1}	V_{CP2}	V_{IN}"0"	V_{IN}"1"	TEMP.	TEST DURATION
Stress Functional	-25V	-30V	-30V	-4V	-9V	25°C	<30 Seconds
340 Hr. Burn-In	-25V	-30V	-30V	>-3V	<-10V	125°C	340 Hrs.

MEAN MCF VALUE - Hz

			WAFER 1	WAFER 2	WAFER 3	WAFER 4	WAFER 5	WAFER 6	WAFER 7	WAFER 8	WAFER 9	WAFER 10
5R100	2	A	272	950	678	1874	745	1382	485	1429	662	-
5R100	2	B	949	261	-	5300	-	50	794	375	338	-
5R100	2	R	-	-	19	-	-	2249	63	-	-	-
5R100	2	ALL COMBINED	723	852	568	3016	745	1546	394	902	639	-
5R100	3	A	1930	54	1220	100	985	1480	2442	149	20	478
5R100	3	B	418	93	25	164	183	998	1158	208	115	375
5R100	3	R	1168	25	-	-	392	1494	-	-	-	-
5R100	3	ALL COMBINED	1404	59	955	119	517	1321	1586	162	67	452
P2000	A	A	22	21	20	13	2018					
P2000	A	B	21	20	26	25	931					
P2000	A	R	20	20	20	10	477					
P2000	A	ALL COMBINED	21	20	24	20	1088					
P2000	B	A	36	51	-	44	56					
P2000	B	B	27	41	31	69	58					
P2000	B	R	-	-	33	202	36					
P2000	B	ALL COMBINED	34	43	32	70	56					
P2000	C	A	19	12								
P2000	C	B	23	29								
P2000	C	R	22	10								
P2000	C	ALL COMBINED	20	18								

TABLE 5.14 - MEAN MCF VALUES BY DEVICE TYPE, LOT, WAFER AND VISUAL CLASSIFICATION

It is therefore not surprising that the burn-in test cause the failure of a considerable quantity of the devices that were subjected to this testing, nor is it surprising that the majority of the devices which failed this test failed as a result of internal node shorts. The results of the 340 hour burn-in are summarized below, the results of the failure analysis are summarized in Table 5.5.

		CLASS "A"			CLASS "B"			CLASS "R"		
TYPE	LOT	n	f	% FAIL	n	f	% FAIL	n	f	% FAIL
5R100	2	51	17	33%	14	6	43%	9	4	45%
5R100	3	45	22	49%	22	9	41%	17	6	35%
P2000	A	28	7	25%	77	20	28%	15	1	7%
P2000	B	17	12	70%	52	17	33%	10	1	10%
P2000	C	9	2	22%	9	3	33%	2	2	100%

In general, the 5R100 devices had a higher failure rate during this testing than the P2000 devices, which demonstrates a reliability improvement by terminating metalization over thick field rather than over gate oxide. The 5R100 devices terminate metalization over gate oxide, the P2000 devices do not.

5.3.3 Correlation of 5R100 and P2000 Failures With MOSPA Data

The mean values for the RIIT bulk and surface effect structures of MOSPA were summarized in Table 5.7 and the mean values for the similar RII structures were summarized in the MOS Interim Scientific Report. These values are shown on a lot by lot basis in Table 5.15 for easy comparison. The parameters which exhibit appreciable differences between lots and should be of significance so far as screening is concerned are FBIAN, and V6AN. Both of these parameters are associated with the drifting of charge in the field oxide under the influence of negative bias. Figure 5.6 shows the cumulative percentage of failure (for the Class "A" and Class "B" devices combined) as a function of burn-in and life test for each lot of devices used in the Phase 3 evaluation. It is evident from this plot that the P2000 devices from lots "B" and "C" continue to fail at a fairly

LOT CODE	PROCESS	FB1AN (VOLTS)	FB1AO (VOLTS)	FB1AP (VOLTS)	FB2AN (VOLTS)	FB2AO (VOLTS)	FB2AP (VOLTS)	IR3A (nA)	BV3A (VOLTS)	V6AO (VOLTS)	V6AN (VOLTS)	V7AO (VOLTS)	V7AN (VOLTS)	h_{FE}
2	RII	- 4.5	-18.3	-	-1.53	-1.40	-	250	78.2	28.8	20.3	3.82	3.73	0.39
3	RII	-10.2	-19.5	-	-1.32	-1.37	-	72	71.7	28.7	22.2	3.64	3.57	0.32
A	RIIT	- 5.2	-20.0	-30.6	-1.16	-0.96	-1.0	0.55	96.0	32.1	24.6	3.08	2.60	0.37
B	RIIT	+10.0	-15.6	-33.7	-1.16	-1.05	-1.05	0.98	92.0	27.2	14.4	3.03	1.52	0.42
C	RIIT	+ 2.8	-16.3	-33.6	-3.9	-4.5	-1.3	0.99	100.0	30.8	12.1	1.26	1.00	0.35

TABLE 5.15 - MEAN VALUES OF MOSPA TEST STRUCTURE PARAMETERS BY LOT

FIGURE 5.6 - CUMULATIVE % FAILURE THRU BURN-IN AND LIFE TEST

high rate throughout the entire burn-in and life test, the P2000 devices from Lot "A" experienced very few failures through both the burn-in and life test and the 5R100 devices from Lots 2 and 3 experienced a rather high failure percentage early in the testing, but failed less frequently subsequent to the post 340 hour measurement. Examination of the Phase 1 life test data for the 5R100 devices from Lots 2 and 3 shows that both lots experienced about a 30% failure percentage through the 2,000 hour life test that was performed under less severe operating conditions (V_{DD} = -15V, V_{CP} = -26V, T_A = 125°C). Figure 5.7 shows the percentage of failure through the 2,000 hour life test performed as part of the Phase 3 evaluation (V_{DD} = -25V, V_{CP} = -30V, T_A = 125°C). It is observed from this plot that the 5R100 devices from Lots 2 and 3 behave similarly, but exhibit an increasing failure percentage with time, and the P2000 devices from Lot "A" show a relatively low and constant failure percentage with time. Comparison of the failure percentage with time on life test with the mean values for FB1AN and V6AN shows correlation of the increasing failure percentage lots (P2000, Lot B and P2000 Lot C) with positive FB1AN values and abnormally low V6AN values. The similarity between the percentages for the 5R100 Lot 2 and 3 devices during the Phase 3 life testing and the similarity between the failure percentages during the Phase 1 life testing indicates that the Phase 1 and Phase 3 data is compatible. The lower failure rates during the Phase 3 life testing are attributed to the fact that the Phase 3 burn-in conducted at a more severe stress level than during the Phase 1 evaluation was more successful in screening potential 5R100 failures.

5.3.4 Correlation of MOSPB Data

The data obtained from the MOSPB vehicles during the Phase 3 evaluations are contained in subsection 5.2.3. The intent of the measure-

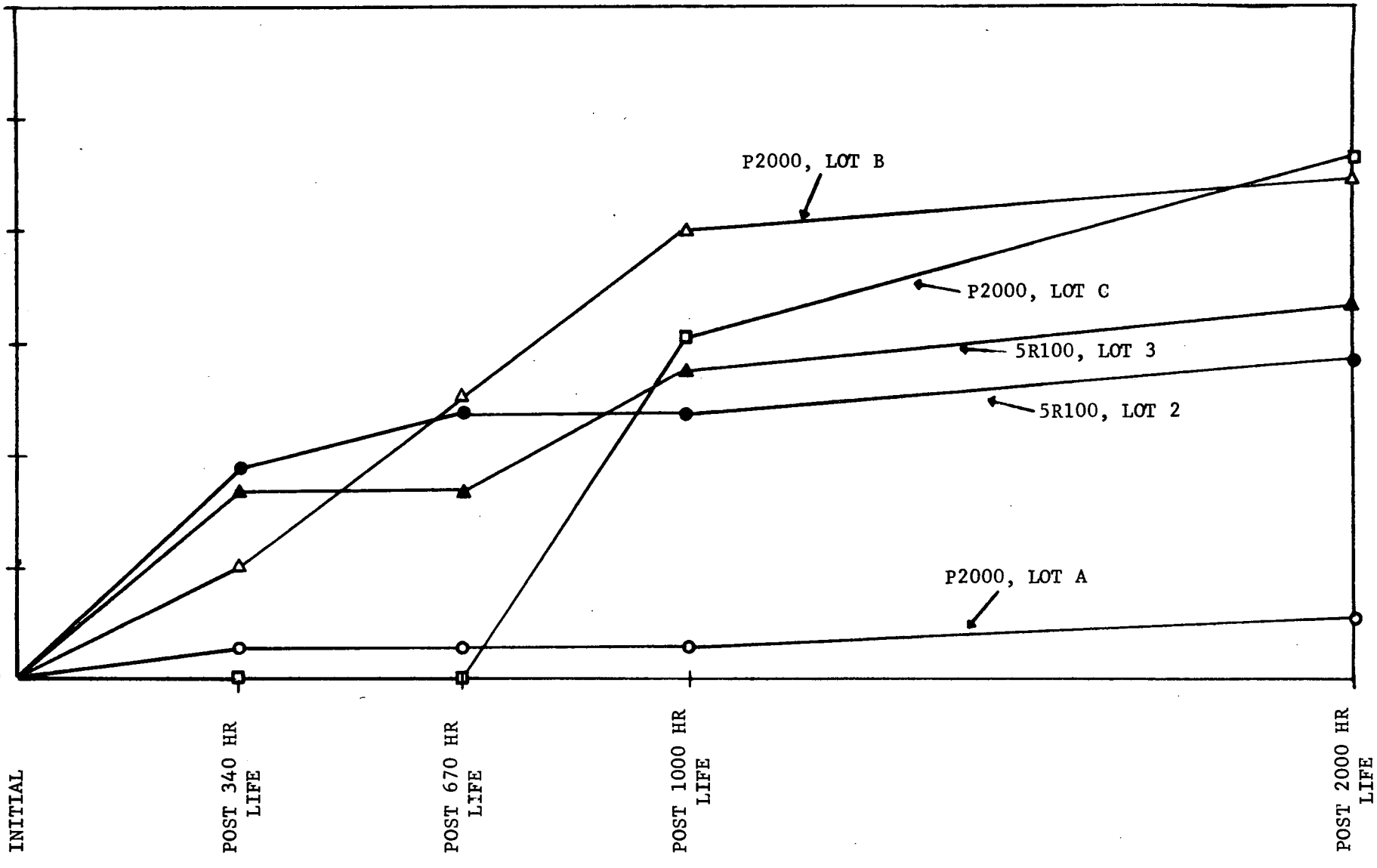


FIGURE 5.7 - CUMULATIVE % FAILURE THRU LIFE TEST

ments and testing of the individual structures of this pattern was to insure that the metalization and oxide layers of the functional device conformed to the processing specification and would not jeopardize the reliability of the functional vehicles.

The process specified thicknesses for the metalization and oxide thicknesses are:

GATE OXIDE	-	1,475Å - 1,550Å
FIELD OXIDE	-	13,500Å - 15,000Å
METALIZATION	-	9,000Å - 16,000Å
PHOSPHOSILICATE SURFACE PASSIVATION	-	11,000Å - 13,000Å

Comparision of the data from Table 5.9 with the indicated specified values shows that all but the passivating glass layer thicknesses were within the process specified tolerance and these thicknesses were quite well controlled. Table 5.8 shows the width measured data taken on metalization stripes, and "p" type resistor diffusion. The metalization line width was designed to be 0.3 mil and the resistor diffusion designed width was 1.0 mils. Comparison of the measured values of Table 5.8 with the design widths indicates that the diffusion widths were controlled to within 6-7% which is somewhat loose, but adequate, and the metalization widths were controlled to within 16% of the design width. The metalization widths were typically narrower than designed, but because these particular MOS devices do not operate at high currents, no difficulties should be experienced with metalization opens.

Table 5.10 shows the voltage required to cause shorting of the capacitor structures of the RIIT, MOSPB test pattern. The data taken on a sample of devices prior to thermal screening, and the data taken on a second sample of devices subsequent to thermal screening indicates that successive application of thermal shock (-65°C to +150°C) and 150°C storage does not degrade the insulating characteristics of the gate oxide utilized as the dielectric for these

capacitor structures. The data does indicate however, that the capacitor structures from the outer portion of the wafer, on the average, are capable of sustaining a higher voltage than the structures from the inside of the wafer. Table 5.11 summarizes the results of the thermal stress sequence testing of the MOSPB test patterns. The single failure incurred during the test sequence was a shorted 10 mil^2 capacitor after the completion of the final 340 hour 150°C storage step. The maximum potential that had been applied to the capacitor structures to this point was -40 Volts, and a single failure from a total of 48 patterns each containing 3 discrete capacitor structures does not indicate the existance of any potential oxide shorting problem with the P2000 test vehicles. The failure analysis summary for the P2000 devices (Table 5.5) indicates that the majority of failures incurred during the burn-in of these circuits was the result of shorts in the output buffer circuit capaci tor. The maximum applied voltages during the burn-in and life test of the P2000 devices were $-25V_{DD}$ and $-30V_{CP}$. Figure 5.8 shows the circuit configuration of the output stage of the P2000 device. Capacitor C1, (the output buffer stage capacitor which exhibited shorting problems during burn-in) and its associated circuitry is used in lieu of a V_{GG} power supply. During clock number 1 (CP1) "ON" time, a charge of approximately V_{DD} is placed on capacitor C_1. When capacitor C_1 is turned off and CP2 is turned on the voltage at node A is instantaneously $V_{DD} + V_{CP2}$. In this manner capacitor C_1 develops an additive voltage level higher than any externally impressed voltage, and under the conditions applied during the burn-in and life test this voltage is equal to approximately 55 Volts. That the burn-in was effective in screening devices with potential oxide weaknesses it is necessary to consider the theoretical voltage stress capability of thin silicon oxide films. The theoretical limit for thin oxide films is of the order of 1×10^7 volts/cm. The stress applied to C_1 during burn-in was:

$$\text{Voltage stress} = \frac{\text{Instantaneous } C_1 \text{ Voltage}}{C_1 \text{ Dielectric Thickness}}$$

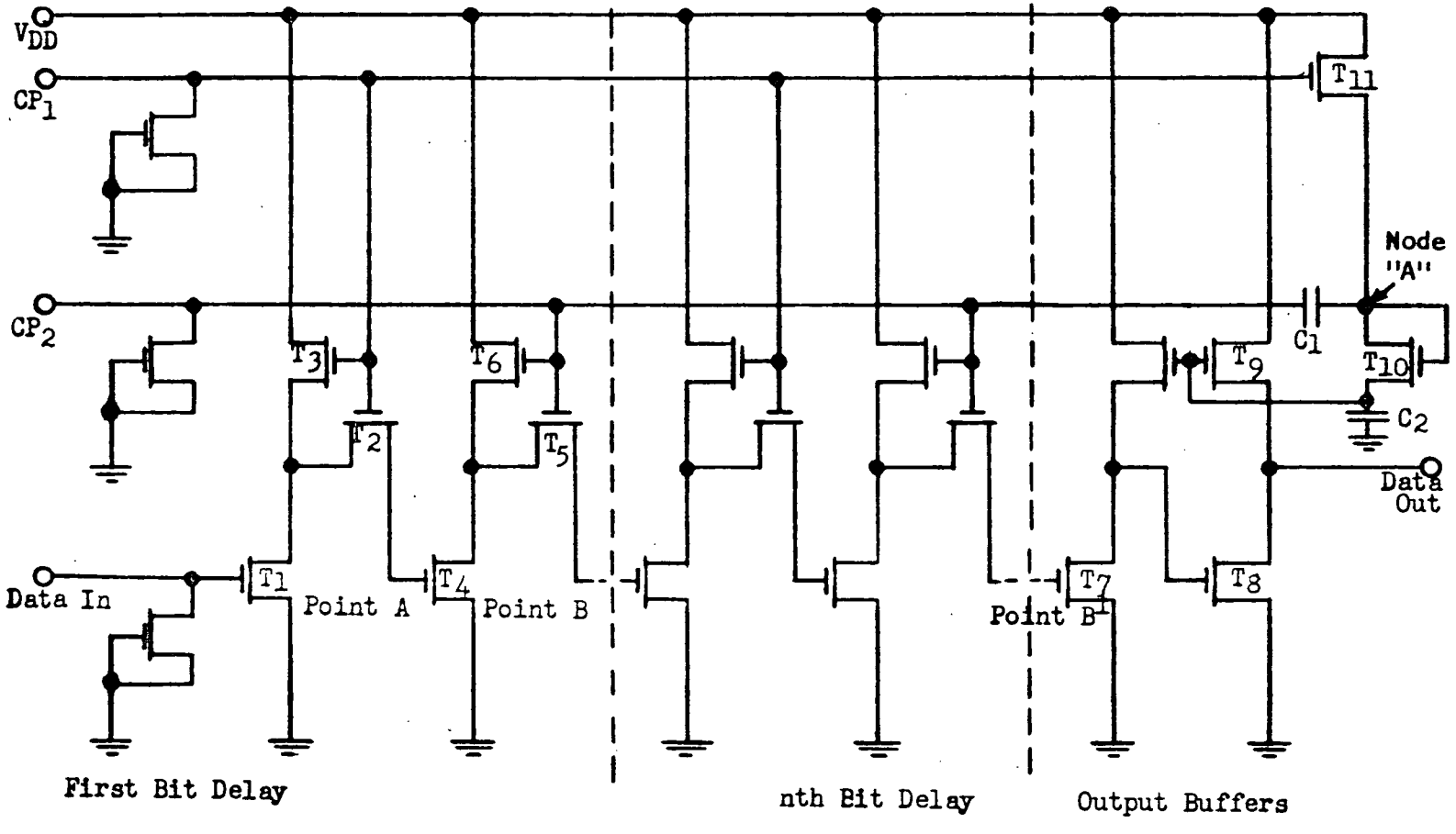


FIGURE 5.8 - SCHEMATIC OF pL5R100 (2000), SHOWING THE LOCATION OF THE OUTPUT BUFFER STAGE CAPACITOR C.

$$\text{Voltage Stress} = \frac{55 \text{ Volts}}{1500\text{Å (Dielectric Thickness)} \times 10^{-8}\text{cm/Å}}$$

$$\text{Voltage Stress} - 3.7 \times 10^{6} \text{ Volts/cm.}$$

This stress is not of sufficient magnitude to cause shorting provided the oxide layer does not contain any defects, but if defects exist that reduce the oxide thickness to 600-700Å at any point, the maximum theoretical sustaining voltage limit is approached and shorting will occur. Actually oxide defects will always limit the maximum voltage that can be applied to a dielectric layer. Figure 5.9 shows the mean voltage that the capacitor structures (gate oxide dielectric layers) of MOSPB were able to sustain before shorting as a function of the area of the capacitor. The decrease in sustaining voltage with increased capacitor area is attributed to the increased probability of a more serious oxide defect in the oxide area under the larger area metalization. Based on this data, and the area of the C_1, capacitor (6 mils X 3 mils), the C_1 structure should be able to withstand, on the average, a stress of 90 volts.

Figure 5.2 shows the stability of the metalization and contact cut structures of MOSPB and Figure 5.3 shows the stability of the capacitor structures of MOSPB through the thermal stress sequence. This data indicates that there is no degradation of these structures as a result of thermal stressing.

Table 5.12 shows the results of the electromigration testing performed on the metalization structures R_{MP} and R_{MS} of MOSPB. The data takes the same general shape as the data obtained during the Phase 1 evaluation on similar structures, but the mean time to failure for these structures at any given current level is less than was observed during the Phase 1 testing. The decrease in the mean time to failure for the Phase 3 structures is the result of the application of larger current densities because of the reduced cross section of the Phase 3 vehicles. (The line widths for the Phase 3

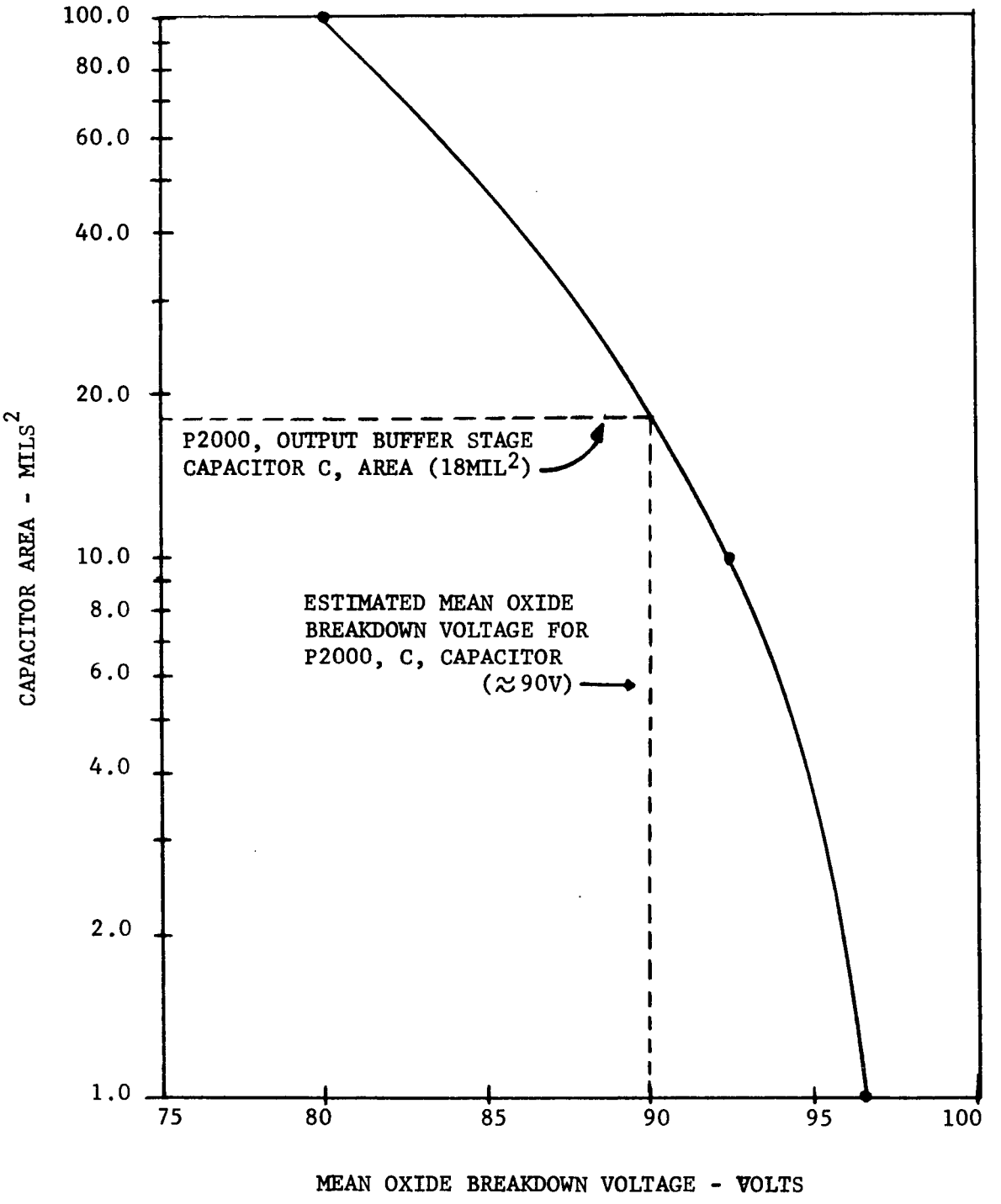


FIGURE 5.9 - OXIDE BREAKDOWN VOLTAGE VR CAPACITOR AREA

vehicles were narrower than the 0.3 mil design width, and the line width for the Phase 1 vehicles were wider than the 0.3 mil design width.) The length and the metalization thickness for the Phase 1 and the Phase 3 vehicles were essentially the same. The difference in metalization width was reflected in the measured resistance values:

	PLANAR METALIZATION STRIPE		METALIZATION STRIPE OVER OXIDE STEPS	
	Resistance	Structure Symbol	Resistance	Structure Symbol
PHASE 1	6.5Ω	R_{1B}	7.5Ω	R_{4B}
PHASE 3	8.9Ω	R_{MP}	9.8Ω	R_{MS}

The electromigration data indicates that no electromigration difficulties should have been observed during the Phase 3 testing and no functional failures occurred as a result of open metalization patterns. The design of these particular devices however, is such that they are not susceptable to electromigration difficulties. In order to achieve a current density of 5×10^5 Amp/cm^2 in the P2000 metalization pattern, almost 80% of the ground stripe would have to be removed by a scratch or void, and the preseal visual criteria precludes this occurrance by rejecting devices where less than one half of the metalization stripe has been disturbed.

SECTION VI

MOS SCREENING PROCEDURE

6.1 GENERAL SCREENING PROCEDURE FOR MOS DEVICES

The recommended general screening procedure for MOS devices is contained in the following subsections. As with the general screening procedure for bipolar devices, the utilization of test patterns fabricated into the same wafer as the MOS functional devices to aid in the removal of functional MOS devices with highly time dependent failure mechanisms is advocated. The arguements concerning the advantages of test patterns that were presented in Section 3.4 in conjunction with the justification for the use of test patterns with bipolar devices are equally valid for MOS devices. It was stated in Section 3.4 and must be re-emphasised here however, the utilization of test patterns as a screening tool supplements, but does not replace the normal screening techniques generally applied to high reliability procurements of MOS devices.

6.1.1 MOS Test Pattern Structures

The specific test pattern structures incorporated into each wafer and tested as part of the Phase 1 and Phase 3 MOS evaluations are described in detail in the Phase 1 - MOS Evaluation Interium Scientific Report and in the MOS Test Method and Evaluation Plan prepared and submitted as part of this contract during September 1971. The test pattern structures described in these reports were adequate for the evaluation of the functional vehicles evaluated under this contract. It should be pointed out however, that two different MOS processing procedures were used during this contract, the RII process for the fabrication of the 5R100 devices, and the RIIT process for the fabrication of the P2000 vehicles. Because of the change in processing, the test pattern masks had to be modified to obtain the required individual test structures for each process even though the final structures performed identical functions. Other processing

techniques will also require mask sets compatable with the processing by which the functional device is being fabricated. The comments of subsection 4.3.1 concerning test pattern design are pertainent to MOS test pattern design, and the comprehensive list of test structures given in that subsection are applicable to individual MOS test structures. The location of test patterns in each wafer was discussed in Section 4.3.2, for bipolar devices; the identical arguments for the location of test patterns can be applied to wafers containing MOS Vehicles.

6.2 SPECIFIC SCREENING PROCEDURE FOR MOS DEVICES

The recommended screening procedure for MOS devices is shown in Figure 6.1. The procedure is shown in the general form so that it is applicable to all types of MOS circuits. Specific recommendations are made for the rejection of devices and/or wafers based on their ability to meet the specified criteria at all test points throughout the screening sequence.

6.2.1 Test Pattern Design

The design of MOS test pattern structures must take into consideration the MOS family the structures are intended to monitor, the metalization system utilized, and the potential failure mechanisms inherent in the functional structures. Since MOS vehicles are normally diffused into high resistivity substrates, they are particulary susceptable to inversion phenomena and the test pattern should include structures capable of monitoring surface and oxide charge. Consideration should also be given to the incorporation of patterns to monitor oxide integrity because the construction of MOS devices causes them to be susceptable to oxide shorting. Because of the high packing density of MOS circuits and the relatively small size of the individual circuit components, alignment is critical so alignment monitoring structures should be provided. Electromigration may or may not present reliability risks depending upon the current densities that occur in metalization patterns, however, because construction in the metalization patterns because of inadequate processing may cause

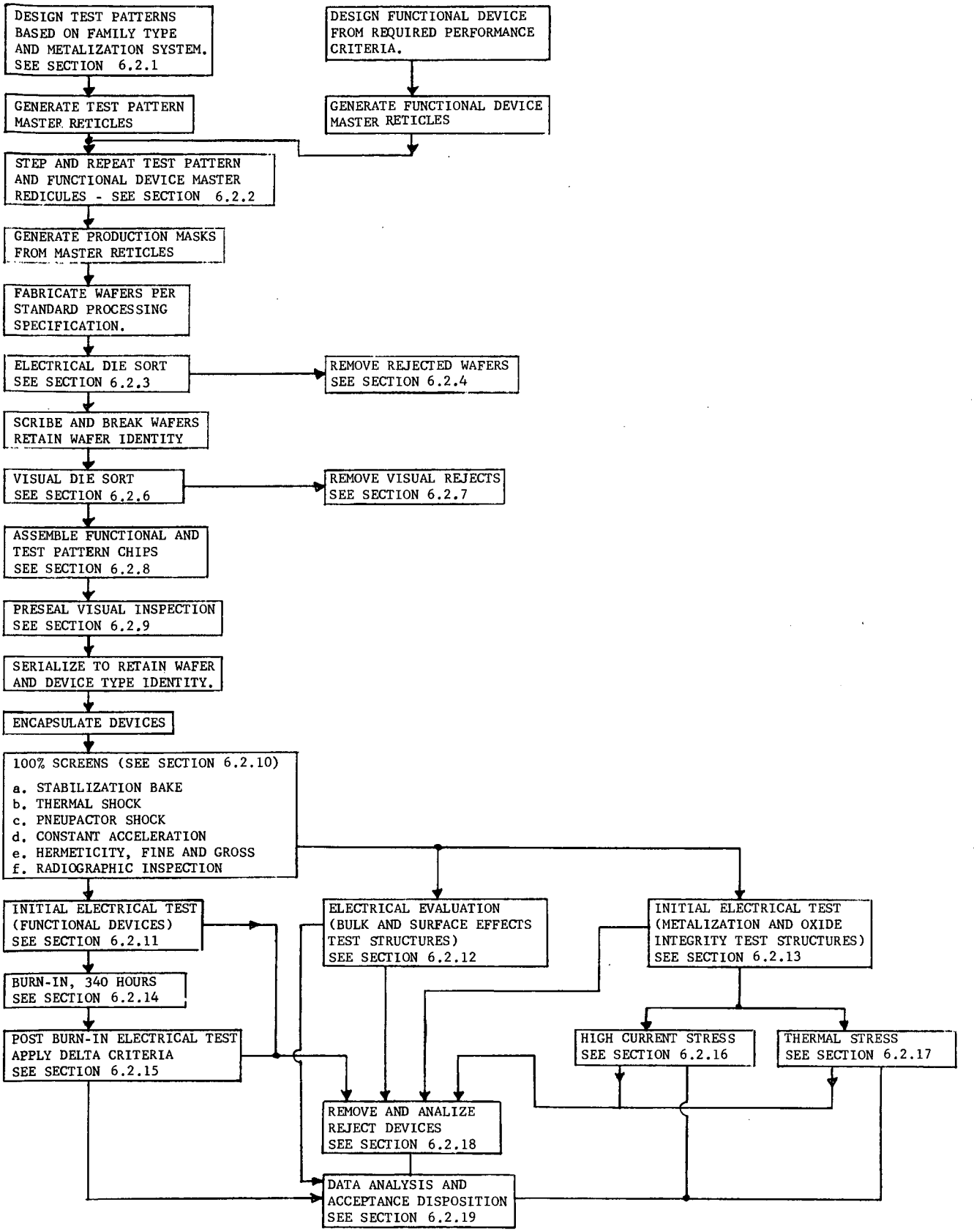


FIGURE 6.1 - SCREENING PROCEDURE FLOW DIAGRAM FOR MOS DEVICES

unanticipated problems, structures should be included to monitor the integrity of the interconnecting metalization. Provisions should also be made to monitor the integrity of contact cuts because MOS shift registers have been known to function properly for a short period of time by virtue of capacitive coupling through unopened contact cuts. This type of failure demonstrates that the many small contact cuts of MOS devices are a definite reliability risk and require evaluation. A comprehensive list of test structures was divided into the categories they are intended to monitor were presented in subsection 4.3.1, and the complete description of the MOS portion of this contract was presented in the Phase 1 Interim Scientific Report. As a minimum, the structures utilized during this program should be included into any test pattern chip, designated for the evaluation of MOS devices. The design of the structures however, may require modification so they are sensitive to parameter variations if other than oxide gate MOS vehicles are to be evaluated.

6.2.2 Test Pattern Location

The location of test patterns on the functional device chip was discussed in detail in subsection 4.3.2, and the arguments concerning the location of test patterns with respect to the functional devices are equally valid for MOS vehicles. The recommended location of test patterns on each wafer is shown in Figure 4.3

6.2.3 Electrical Die Sort

The electrical die sort of each MOS wafer should consist of a room temperature evaluation of all of the functional vehicles, of the metalization and oxide integrity test pattern structures, and of the diffusion evaluation test pattern structures contained on the wafer. The surface effects test structure evaluations however, because these measurements are time consuming, rather difficult to perform with probing techniques, require heat treatment of the wafer, are of a nature where wafer damage could occur and the values obtained are susceptable to change upon encapsulation, should be postponed until the individual structures are encapsulated. It is assumed that all MOS manufac-

tures have included in-process screens for the determination and control of Q_{SS}, and Q_O in the standard processing specification and wafers which do not meet their internal criterial are rejected. The die sort test of functional devices should include both D.C. and functional tests of sufficient quantity to insure that the devices will meet their specified performance specifications. The evaluation of the test pattern structures should include:

a. Kelvin connection measurements of the metalization and contact cut integrity structures, including metalization stripes on planar surfaces, metalization stripes over oxide steps, contact cut evaluation structures and via evaluation structures if required by the metalization system.

b. Kelvin contact evaluation of the diffused resistor structures at current levels sufficiently low so ohmic heating does not influence the measured values.

c. Leakage measurements of the oxide integrity structures at a voltage higher than will be applied to the functional device during operation but lower than the oxide breakdown voltage for good structure to preclude destruction of good structures.

d. The measurement of the fundemental parameters of dielectric MOS transistors at voltage and current levels to which they will be exposed during functional device operation. The MOS transistor parameters that should be measured include the gate threshold voltage (V_{GST}) the drain to source breakdown voltage (BV_{DSS}) and the gate to substrate leakage current (I_{DS}).

The values determined for the individual test structures should all be within the limits prescribed by the processing specification and the individual component values

should be with the tolerances specified in by device circuit design specification. The resistance values for the aluminum stripe, contact cut and via structures must be within the values determined to be adequate to insure sufficient metalization cross section on the basis of electromigration studies. Metalization thickness, and width measurements and diffusion width measurements shall be made at this time and must be within the tolerances specified in the processing specification.

6.2.4 Wafer Rejection at Die Sort

Figure 6.2 shows the electrical die sort yield plotted against the combined percentage of the Class "A" and Class "B" failures incurred through the entire Phase 3 evaluation plan test sequence on a wafer by wafer basis. The plot indicates that a low die sort yield results in a high percentage of failure of the encapsulated devices through the screening and the life testing portions of the evaluation. A high die sort yield however, does not insure a low failure rate of the encapsulated devices. Based on this data however, any wafer that does not have an electrical die sort yield of 40% for the functional devices should be rejected for use in high reliability application.

Excluding the test pattern chips located at the periphery of the wafer, any wafer that exhibits greater than a 10% failure rate for any given test pattern structure shall be rejected.

Because device design is based upon a given tolerance of the process determined parameters such as resistivities, line widths, oxide thickness, and metalization thickness, those wafers whose calculated mean values for the process determined parameters (as determined by the evaluation of the test pattern structures) do not meet the specified

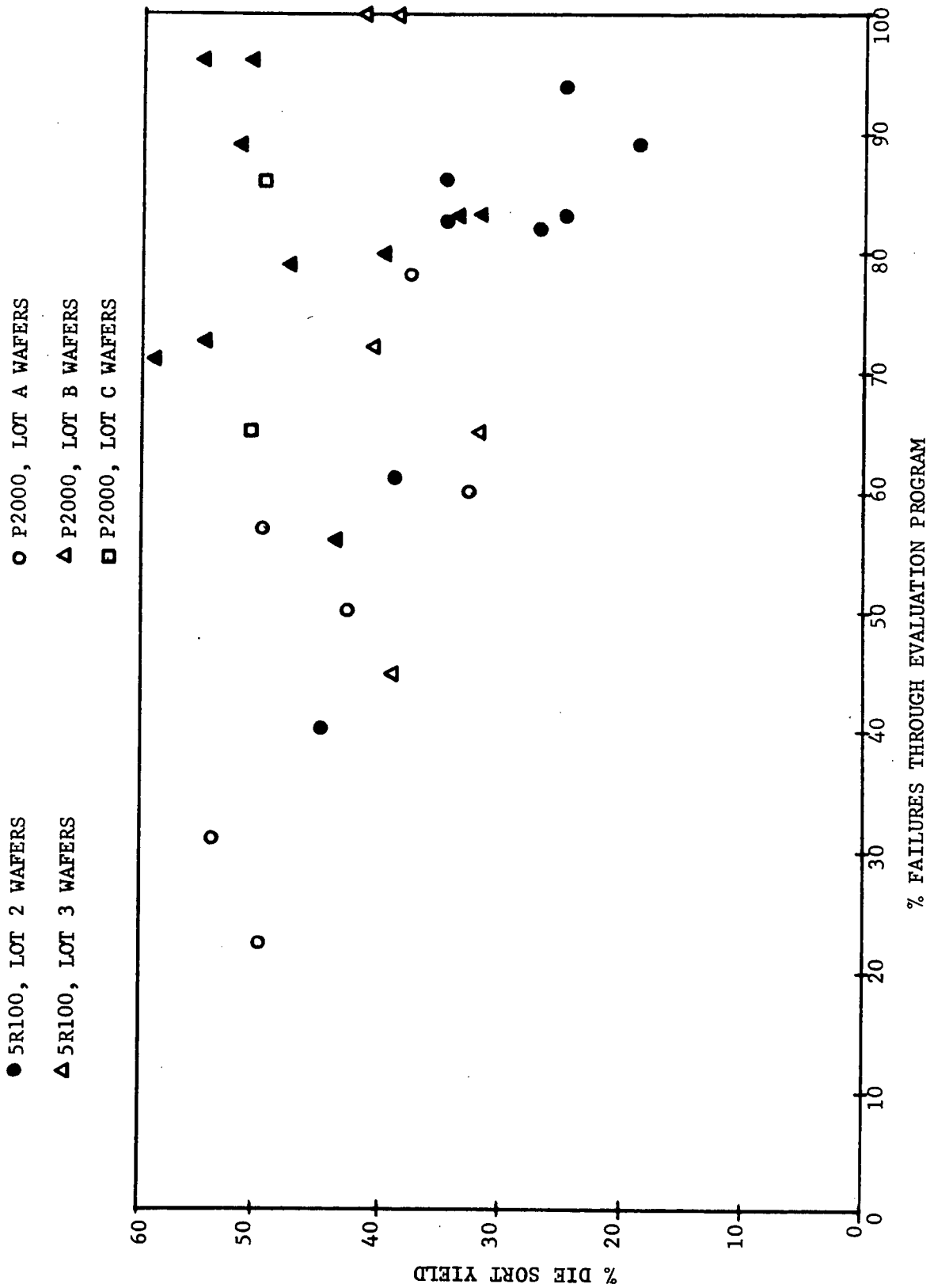


FIGURE 6.2 - DIE SORT YIELD vs EVALUATION PLAN PERCENTAGE

values for any given process shall be rejected. Peripheral chips shall not be included in the calculation of mean values.

The test pattern measurements made on test structures identical to structures used in the functional device shall be evaluated under forcing functions similar to those devices shall see in functional circuit operation. The mean values for these parameters shall be determined and any wafer for which the mean value does not meet the worst case design equation values shall be rejected.

6.2.5 Removal of Rejected Wafers

Those wafers which do not meet the electrical die requirements shall be removed from the process flow.

6.2.6 Visual Die Sort

A visual die inspection shall be performed according to the requirements of the visual inspection criteria of Appendix "A" may be performed at this point at the manufacture's discretion. Regardless of whether this inspection is performed, each device must be completely reinspected according to the preseal visual criteria of Appendix "A" subsequent to chip and wire bonding.

6.2.7 Removal of Visual Reject Dice

If the manufacturer chooses, dice that do not meet the requirements of the preseal visual inspection criteria of Appendix "A" can be removed from the process flow at this point. The removal of dice which exhibit detects is only for reasons of economics because all devices which fail the preseal visual criteria will be removed at a later point in the process flow.

6.2.8 Assembly

A sufficient quantity of each type of test pattern dice shall be assembled to insure that a minimum of six of each type of test patterns are available for testing subsequent to encapsulation. All of the available functional chips must be assembled. The assembly of both the functional and the test pattern chips must be performed simultaneously on the same equipment and according to the same processing specification. The assembly of these devices must be performed in such a manner that the identity of the wafer from which the devices were obtained is retained for subsequent identification during the evaluation of the reliability of devices on a wafer by wafer basis. All assembled test pattern chip and functional device chips must be bonded according to the individual bonding requirements for each chip design.

6.2.9 Preseal Visual Inspection

All devices are to be inspected according to the requirements of the preseal visual inspection specification contained in Appendix "A". Those devices which do not meet this criteria are to be removed from the processing flow. The surviving devices must be serialized to retain wafer identity and device type (i.e., test pattern or functional vehicle) and all assemblies are to be sealed in accordance with the specified sealing procedure for the family and package type.

6.2.10 In Process Screens

The functional and the test pattern vehicles are to be subjected to the following in-process screens:

a. Stabilization Bake, per MIL-STD-883, Test Method 1008, 24 hours (minimum).

b. Thermal Shock per MIL-STD-883, Test Method 1011, Test Condition C (minimum).

c. Mechanical Shock per MIL-STD-883, Test Method 2002, Test Condition G (minimum) Y_1 plane only.

d. Constant Acceleration per MIL-STD-883, Test Method 2001, 40,000 G (minimum).

e. Hermeticity, fine and gross, per MIL-STD-883, Test Method 1014, Test Conditions A and C.

f. Radiographic, per MIL-STD-883, Method 2012.

6.2.11 Initial Electrical Test, Functional Devices

All functional devices shall be subjected to an input voltage stress of sufficient magnitude and duration to insure that subsequent failures will not occur because of inadequate input protection. If the device is of a construction that gates of the internal nodes are not available at the external termination of the device, a high stress functional stress shall be applied to cause the failure of weak internal gates so these devices can be removed during subsequent testing. Examples of input voltage stress tests and stress functional tests for oxide gate "p" enhancement mode MOS shift registers are contained in the MOS Evaluation Plan. Upon completion of the stress testing the devices shall be subjected to a 100% D.C. and functional test at -55°C, 25°C, and +125°C according to the requirements of the individual device specification. Any device which does not meet the requirements of the specification shall be rejected.

F

6.2.12 Electrical Evaluation, Bulk and Surface Effects Patterns. As a minimum the test structures that shall be included in the bulk and surface effects pattern and the evaluations that should be performed on these test structures are shown below:

TEST STRUCTURE DESCRIPTION	MEASUREMENT
MOS Capacitor over field Oxide	Flat Band Voltage a. After drifting mobile charge, under 0 Volt bias, for 12 minutes at 300°C. b. After drifting mobile charge, under -36 Volt bias, for 12 minutes at 300°C.
MOS Capacitor over gate Oxide	Flat Band Voltage a. After drifting mobile charge, under 0 Volt bias, for 12 minutes at 300°C. b. After drifting mobile charge, under -12 Volt bias, for 12 minutes at 300°C.
Large area p-n junction Diode	a. Leakage current at -20 Volt. b. Breakdown voltage at 10 μA.
Field Oxide MOS Transistor	Inversion Voltage a. After drifting mobile charge, under 0 Volt bias, for 12 minutes at 300°C. b. After drifting mobile charge, under -36 Volt bias, for 12 minutes at 300°C.
Gate Oxide MOS Transistor	Inversion Voltage a. After drifting mobile charge, under 0 Volt bias, for 12 minutes at 300°C. b. After drifting mobile charge, under -12 Volt bias, for 12 minutes at 300°C.
Lateral Bipolar Transistor	h_{FE} at 5 V_{CE} & 50 μA I_C.

The detailed test procedures for these evaluations are contained in Appendix "C" of the MOS Evaluation Plan.

6.2.13 Initial Electrical Test, Metalization and Oxide Integrity Test Structures

As a minimum the metalization and oxide test structures that should be included in the test pattern are those that were utilized during the evaluations performed under this contract. The initial measurements performed on the metalization and oxide integrity pattern shall consist of the determination of the resistance of all metalization stripe structures, and the determination of the leakage current across all capacitor structures. The current levels applied to the metalization stripe structures will be sufficiently high to accurately determine the initial resistance, but low enough to insure that it will not cause damage to the stripe. An approximate current level is about 10 mA, but this may vary somewhat depending upon the actual geometry of the stripe. The voltage applied to perform the capacitor leakage tests shall be greater than the maximum voltage the oxide dielectric will experience during circuit operation, but lower than the voltage that will cause distructive shorting of oxide layers of reasonable integrity. An approximation of the voltage level for 1500Å thick gate oxide dielectric capacitors is 60 Volts, but this value will vary as a function of the thickness and material used for the capacitor dielectric.

6.2.14 Functional Device Burn-In

The decision concerning the most effective burn-in test for any given functional device is generally quite difficult, and is partially determined by the end use of the particular device type being evaluated. For MOS devices the fact they are susceptable to inversion phenomenea and that they do not generally draw sufficient current to present electromigration problems leads the reliability engineer to the serious consideration of high temperature

reverse bias testing. During the Phase 1 evaluation of the 5R100 devices under this contract, three different life test evaluations were performed on three different groups of devices from the same processing lots. The evaluations were:

a. High temperature reverse bias operation.

b. Temperature cycled clocked ring circuit operation.

c. High temperature clocked ring circuit operation.

The data reported in the Phase 1 Interium Scientific Report showed that the high temperature, clocked ring circuit life test was the most effective life test screen to which the devices were exposed. Based on this information, the Phase 3 340 hour burn-in and 2,000 hour life testing was performed in a 125°C clocked ring circuit, with the devices operating under the maximum rated V_{DD} and clock voltages. During the Phase 1 evaluation, the 168 hour clock ring circuit evaluation was performed at 125°C with the maximum rated V_{DD} and clock voltages applied to the devices under test, but the voltages were reduced to the nominal in use voltages during the 2,000 hour life test. The 340 hour burn-in performed during the Phase 3 evaluation proved quite effective for screening weak circuit elements, specifically the output buffer capacitor, from the devices evaluated, and with the exception of the P2000 devices from Lots B and C the remainder of the test vehicles from the P2000 lot and the 5R100 lots 2 and 3 experienced few failures through the 2,000 hour life test. The failures experienced by the 5R100 lots 2 and 3 and the P2000 lot A device occurred principally prior to the 340 hour measurement. The failures experienced by the P2000 Lot B and C devices occurred throughout the life test, and the flat

band voltages determined from the test structures of MOSPA indicated difficulties with the devices from these lots. Based on this data, the recommended burn-in for MOS devices should be performed in a functional circuit similar to the circuit the devices will be subjected to in subsystem usage. The functional circuit offers an advantage over a back bias circuit in that the functional circuit can be designed to exercise most of the individual components of the integrated circuit chip where as it is usually not possible to design a back bias circuit to evaluate more than half of the individual devices on a chip. The burn-in should also be performed at the maximum rated voltages of the device, and where power dissipation is a function of operating frequency the highest operating frequency should be applied. The question as to whether the circuit should be operated at 125°C or should be temperature cycled from -55°C to +125°C during the burn-in is a function of the current densities in the metalization patterns and the type of metalization systems used. If current densities are high of the order of 1×10^5 Amp/cm, and/or if multilayered metalization systems are used temperature cycled operation is more likely to detect dielectric oxide layer, via, and metalization defects. If the device uses a monolayer metalization system, and if current densities are relatively low, high temperature (125°C) operation is more likely to screen difficulties associated with current leakage. The duration of the burn-in should be a minimum of 340 hours and for the majority of MOS devices currently available, the devices should be operated at 125°C with the maximum rated voltages applied. The possibility of reliability risks because of inversion phenomenea can be evaluated with the use of the surface effect test structures.

6.2.15 Post Burn-In Electrical Test Functional Devices

The post burn-in electrical measurements of the functional MOS devices shall consist of complete D.C. and functional testing per the individual device specification at -55°C, 25°C and +125°C. Transient measurements shall also be performed ona sampling basis. An LTPD of 10 with an acceptance number of 1 is to be applied to the transient measurements. If the devices from a wafer fail the initial transient measurements, tightened inspection (LTPD = 7, acceptance number = 2) must be applied. Failure to the tightened inspection level will be cause for rejection of the devices from the wafer. The devices subjected to transient measurements are to be only those devices which meet the D.C. and functional test criteria described in the following paragraph.

Any device which fails to meet the specified D.C. and/or functional requirements shall be cause for rejection of the individual device. Devices which fail to meet the delta limit criteria outlined below shall also be rejected. The delta limits to be applied are:

a. Measured Voltages $\pm$10%

b. Measured Currents $\pm$10%

c. Leakage Currents $\pm$20 nA or $\pm$20% of the maximum specification limit, whichever is greater.

If more than 10% of the devices from a given wafer fail the post burn-in electrical criteria for absolute and/or delta limits combined, all devices from the wafer shall be rejected.

6.2.16 High Current Stress Testing

The metalization stripe structures of the test patterns

shall be subjected to high current density testing according to the discussion presented in Subsection 4.3.16. Rejection of the functional devices from any wafer whose metalization test pattern structures do not meet the minimum reliability requirements of the functional device will be required.

6.2.17 Thermal Stress Evaluation

The metalization and oxide integrity test patterns shall be subjected to the same thermal stress sequence as shown in Subsection 4.3.17. A minimum of 10 test patterns from each wafer will be subjected to this evaluation. The failure criteria shall be the same for the MOS test patterns as for the bipolar test patterns except that capacitor structures fabricated over gate oxide shall be required to withstand the application of a 60 volt potential difference rather than the 200 volt potential difference required for capacitor structures fabricated over field oxide regions. The functional devices from the wafer from which the test patterns were obtained will be rejected if more than 10% of the test structures fail to meet the thermal stress requirements.

6.2.18 Analysis of Failures

The functional and test pattern failures incurred during the screening evaluation shall be analized as indicated in Subsection 4.3.18.

6.2.19 Data Analysis and Acceptance Disposition

The data analysis and the acceptance disposition of all devices shall be performed as indicated in Subsection 4.3.19.

SECTION VII

CONCLUSIONS

7.1 GENERAL

Based on the data derived during the course of this contract, it has been demonstrated that the screening methods developed represent an improvement over previous high reliability screening techniques. Part of the success of the screening method is attributed to the utilization of test pattern structures which provided a means for the establishment of rejection criteria which would not have been possible if the criteria had been based entirely on functional integrated circuit device performance. Utilization of test pattern rejection criteria also provides a means for effective screening of very complex integrated circuits where normal high reliability screening techniques become ineffective because the complexity of these devices preclude a complete evaluation of the highly time dependent failure mechanisms which could result in long term reliability risks. Test pattern structure screening techniques also enable the standardization of screening methods so that comparison of the reliability of different devices from the same family or the comparison of the reliability of the same type of device fabricated at any period of time can easily be performed based on the fundamental characteristics of the family. As previously discussed however, to insure overall reliability, the test pattern screen techniques supplement, but do not replace the normal electrical, visual, and thermal screening of the functional devices themselves.

7.2 EFFECTIVENESS OF THE BILAYER BIPOLAR SCREENING PROCEDURE

A failure summary for the bilayer-bipolar DCQ devices by visual class and by wafer was presented in Table 3.2. The DCQ devices were assembled into the three test groups (Class "A", Class "B", and Class "R") according to the standard industry practice of initially assigning devices to different reliability categories based on the results of the preseal visual inspection.

The highest reliability category was Class "A", the lowest was Class "R". During the initial assignment to reliability categories the test pattern data taken during the wafer mapping step was not applied because data from the encapsulated test patterns was not yet available and it was necessary to insure that the wafer mapping test pattern data correlated with the post seal test pattern data prior to the application of this data to the functional devices. Subsequent testing showed that the correlation did exist, and evaluation of the test pattern data showed that only the devices from wafers A, B, and C should have been placed in a high reliability category. A failure summary of the data obtained from the devices from these wafers is shown in Table 7.1, and this data indicates that the effectiveness of the screening procedure was excellent, provided test pattern data is evaluated and applied on an individual wafer basis prior to the assignment of devices to a high reliability category. Two failures were incurred during the high stress 2,000 hour life test. Analysis of the devices showed that the Class "A" failure that occurred at the post 1,000 hour life measurement was the result of a top to bottom layer metalization short but the device contained visual defects that should have precluded its placement into this category. The Class "B" failure that occurred at the post 2,000 hour life measurement failed because leakage current had increased to the point where it exceeded the device specification, although it was still a good functional device. No mechanism for the cause of the increase in leakage was observed.

7.2.1 Areas Where Bilayer-Bipolar Screening Procedure Improves Previous Approaches

The most obvious improvement to previous screening approaches is that the application of test pattern data to devices from a given production run, on a wafer by wafer basis, permits the assessement of the fundamental mechanisms that can result in functional device failure that would not be possible if the screening procedure utilized only functional device data. Increased device complexity smaller individual component geometries and higher packing densities together with multilayered metalization systems will eventually make traditional screening procedures ineffective because preseal visual

Lot/Wafer	Lot Code	Visual Class	n	Initial Failures	n	Fail Screen	n	Fail Burn-In	n	Fail Post 1000 Hr. Life	Fail Post 2000 Hr. Life	Total Life Failures
33/15	A	A	12	1	11	0	11	0	11	1*	0	1
39/13A	B	A	1	0	1	0	1	0	1	0	0	0
39/13B	C	A	2	1	1	0	1	0	1	0	0	0
Totals			15	2	13	0	13	0	13	1	0	1
33/15	A	B	14	0	14	0	14	0	14	0	0	0
39/13A	B	B	18	6	12	0	12	1	11	0	1**	1
39/13B	C	B	8	0	8	1	7	0	7	0	0	0
Totals			30	6	24	1	23	1	22	0	1	1
33/15	A	R	10	10	-	-	-	-	-	-	-	-
39/13A	B	R	9	5	4	0	4	0	4	0	0	0
39/13B	C	R	5	1	4	0	4	0	4	0	0	0
Totals			24	16	8	0	8	0	8	0	0	0

* Top to bottom layer metal short, but device contained visual defects that should have precluded its placement into the class "A" visual category.

** Parametric failure to Icex specification, but device functions properly.

Table 7.1 Failure summary for devices from high reliability wafers as determined by test pattern data.

inspection will require magnifications too difficult to use on a 100% in-process basis, and lower layer visual defects will be obscurred by upper layer metalization layers. Although thermal, mechanical screens can still be applied complete electrical testing must be performed to insure that the failures induced by these screens are removed, and this testing will be expensive and time consuming to implement. The approach to high reliability must be to insure that the process is reliable and under control and the means to this end is through the use of test structures included on each wafer to monitor the fundemental processing parameters.

The utilization of test patterns on this program demonstrated that:

a. Reliability is a wafer to wafer rather than a lot to lot variable and must be controlled on an individual wafer basis.

b. The utilization of the data from the test patterns resulted in the reassignment of wafers classified as high reliability material by previous screening techniques into a high risk category and the data derived through the screening procedure justified this characterization.

The correlation of bipolar test pattern die sort measurements with the measurements subsequently made on encapsulated test patterns justifies wafer reliability classification at wafer mapping. This permits immediate feed back of information to the in-process control points and should result in a better controlled process. Additionally wafer characterization at die sort will result in economic benefits through the rejection of high risk wafers and thereby saving, scribing, assembly, in-process screening and electrical testing costs.

7.2.2 Effectiveness of the Bilayer Bipolar Test Patterns

The bilayer-bipolar test patterns utilized during the course of this contract were quite effective in determining processing defects that were ultimately responsible for unreliable operation of the DCQ devices from some of the wafers from which the test vehicles were obtained. Of particular significance are:

a. The bulk parameters measured on the transistor and resistor structures of BBTP2 showed that some of the DCQ wafers contained individual components which exhibited a considerable deviation from the nominal DCQ design values, and the solution of the DCQ design equations utilizing the bulk parameter values obtained from the BBTP1 devices indicated that the DCQ devices from certain wafers would have difficulty in meeting the D.C. specification. More importantly, the prediction of high reliability risk wafers based on the solution of the design equations exhibited a high degree of correlation with the percent of failures incurred by the DCQ devices during the evaluation.

b. The measurement of metalization and oxide thicknesses utilizing the special thickness evaluation structures of BBTP1 predicted possible oxide shorting problems that occurred on DCQ devices during the Phase 3 test sequence.

c. The evaluation of oxide integrity with the use of the MOS Capacitor structures predicted possible shorting problems on a wafer which had a bottom layer metalization to insulating dielectric ratio greater than unity. Shorting problems would not normally be anticipated based on the measured oxide and metalization thickness, and the greater than unity metal to oxide ratio. The devices from this wafer performed poorly during the Phase 3 evaluation.

Not all of the individual test structures indicated reliability problems, but in the cases where no problems were indicated by the test

patterns, none occurred with the functional devices during the course of the evaluation. An example of this type of correlation is that no DCQ electromigration problems were anticipated based on the BBTP1 test data, and none occurred. The fact that certain structures did not indicate problems and that none occurred in the DCQ devices is positive correlations, and that no problems were revealed does not negate the utility of the structures. Had the problem existed, the structure would have detected it.

7.2.3 Areas In Which The Bilayer-Bipolar Screening Procedure Is Deficient

Weaknesses in the bilayer-bipolar screening procedure are:

a. The evaluations performed as part of this contract were sufficient to demonstrate the feasibility of the test pattern approach to high reliability screening, but because of the limited scope of the contract there was not sufficient data generated to insure that the approach is effective for all bipolar families or for all metalization and dielectric layer processing techniques.

b. Individual wafer characterization presents handling and identification difficulties to manufacturers accustomed to accumulating many wafers into a large assembly lot, and wafer identification subsequent to scribing and prior to serialization after assembly is particulary difficult to control.

c. To be effective the preseal visual inspection criteria must be stringent, but this results in the specification of criteria that becomes subjective. Unfortunately there is no alternative at this time.

7.2.4 Further Investigation of Bipolar Screening Procedures

The data taken during this program demonstrated the feasibility of the screening approach, however, additional investigations should be performed with a larger variety of device families and processing techniques to increase confidence in the data and to insure the approach is generally applicable.

7.3 EFFECTIVENESS OF THE MOS SCREENING PROCEDURE

In general, the MOS screening procedure was effective in removing devices which were high reliability risks, and although the test pattern measurements were helpful in determining high risk MOS wafers, the test pattern data did not show the same degree of correlation with functional device failures as was observed for the bipolar vehicles. The 340 hour, 125°C, maximum rated voltage burn-in screen was effective in removing a considerable quantity of high reliability risk devices, but in spite of this screen failures were still incurred at a relatively high rate during the first 340 hours of life test. The solution to this difficulty is of course to extend the duration of the burn-in (see Figures 5.4 and 5.5) to insure that the high risk devices are removed during the burn-in phase. Correlations were observed between the flat band voltage (V_{FB1AN}) and the inversion voltage (V6AN) measured on test pattern structures and the failure of devices through the screening sequence. Some correlation was observed between the MCF measurements made on the MOS functional vehicles and the failure of these devices during the life test. This correlation indicated that very high MCF values were indicators of impending functional device failure, but devices with low MCF values also suffered subsequent failure.

7.3.1 Areas Where MOS Screening Approach Improves Previous Approaches

The same comments as advanced for the utilization of the bipolar test pattern approach to screening can be applied to the MOS test pattern approach. However, because MOS devices are surface sensitive, it was found during the Phase 1 evaluation that the surface sensitive test structures exhibited changes between the wafer measurement and the encapsulated device measurements and because of this phenomena and th the fact that high temperature drift measurements are difficult to perform with probing techniques the evaluation of these parameters should not be performed until the test patterns are encapsulated.

7.3.2 Effectiveness of the MOS Test Patterns

The MOS test patterns utilized during the course of this program were effective in determining those wafers which exhibited reliability

problems during the Phase 3 testing sequence because of high charge densities which resulted in the failure of the MOS functional test vehicles. These difficulties were predicted on a wafer by wafer basis by the flat band voltage determinations made on the capacitor structures of MOSPB and by the threshold voltage measurements made on the MOS transistor structures of MOSPA. The metalization and oxide integrity measurements, and the oxide and metalization thickness measurements made on the structures of MOSPB did not predict difficulties and none occurred with the MOS functional devices. This is a positive correlation, and as was stated in Section 7.2.2, that certain structures did not predict problems does not negate the utility of the structure for those situations where the defect to which the structure is sensitive occurs in the functional device.

7.3.3 Deficiencies in the MOS Screening Procedure

The same deficiencies as indicated for the bipolar screening procedure exist for the MOS screening procedure. In addition, the fact that the surface sensitive test pattern evaluations must be postponed until after encapsulation impedes the rapid characterization of individual wafers that was possible with bipolar devices. The results in additional storage problems for MOS manufacturers.

7.3.4 Further Evaluation of MOS Screening Procedures

Additional evaluation of the MOS screening procedures should be performed in increase confidence in the valicity of the approach and to insure it is generally applicable to all types of MOS devices.

7.4 OTHER OBSERVATIONS

The date collected on the 5R100, P2000, and DCQ vehicles indicated that those wafers with the highest electrical die sort yields were also the wafers which performed most reliabily through the evaluation test sequence. There has been considerable controversy concerning whether the good devices from a low yield wafer are as reliable as the good devices from a high yield wafer. Based on this data presented in the previous portions of this report, rejection criteria were assigned to reject wafers with low die sort yields.

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APPENDIX "A"

PRESEAL VISUAL ACCEPTANCE CRITERIA

The material contained in this appendix defines the preseal visual inspection criteria to be applied to MOS and Bipolar Semiconductor devices with mono or milti metalization layers, and ultrasonically bonded aluminum internal lead wires. If the devices are assembled with other than ultrasonically bonded aluminum internal lead wires, the bonding should be inspected according to the requirements of MIL-STD-883, Method 2010.1 Internal Visual (Precap). Two reliability categories are included in this specification. They are:

a. Class "A" - The ultra high reliability category to be applied to the inspection of semiconductor devices intended for use in aerospace systems where reliability is imperative and maintenance is not feasible.

b. Class "B" - The reliability category to be applied to the inspection of semiconductor devices intended for use in ground systems where reliability is not the prime consideration and maintenance can be economically performed.

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APPENDIX "A"

CLASS "A" DEVICE

VISUAL INSPECTION CRITERIA

ACCEPTANCE CRITERIA FOR CLASS "A" DEVICE CHIPS SUBSEQUENT TO CHIP & WIRE BONDING.

A1.0 DIE DEFECTS - (80X minimum magnification, binocular microscope, bright or dark field illumination).

A1.1 Scribing:

A1.1.1 Reject any die that shows evidence of scribe marks across an active or metalized area of the die.

* A1.1.2 Reject any die containing chip outs or misaligned scribe lines that reduce the width of oxide between any metalization pattern, or diffusion, and the scribed edge of the chip to less than ½ mil. This criteria does not apply where silicon dioxide is omitted by design. See Figure A1.

* A1.1.3 Reject any die which, because of imperfect die separation, has attached outside of the scribe line more than 10% of the adjacent die.

A1.1.4 Reject any die with a crack that exceeds 1 mil in length and occurs in the active area and/or points toward an active area, metalization, or bond. Reject any die with a crack greater than 1 mil in length that comes closer than ½ mil to any diffusion, regardless of the direction of the crack. See Figure A1.

A1.2 Bonding Pads:

A1.2.1 Reject any die which contains a bonding pad of insufficient size to contain all of the bond contact area. An insufficient bonding pad can be caused by:

a. Passivating oxide or photoresist material resulting in full or partial covering of the bonding pad.

* Indicates reduced criteria exists for Class "B" devices. See appropriate B.X.X.X. subsection.

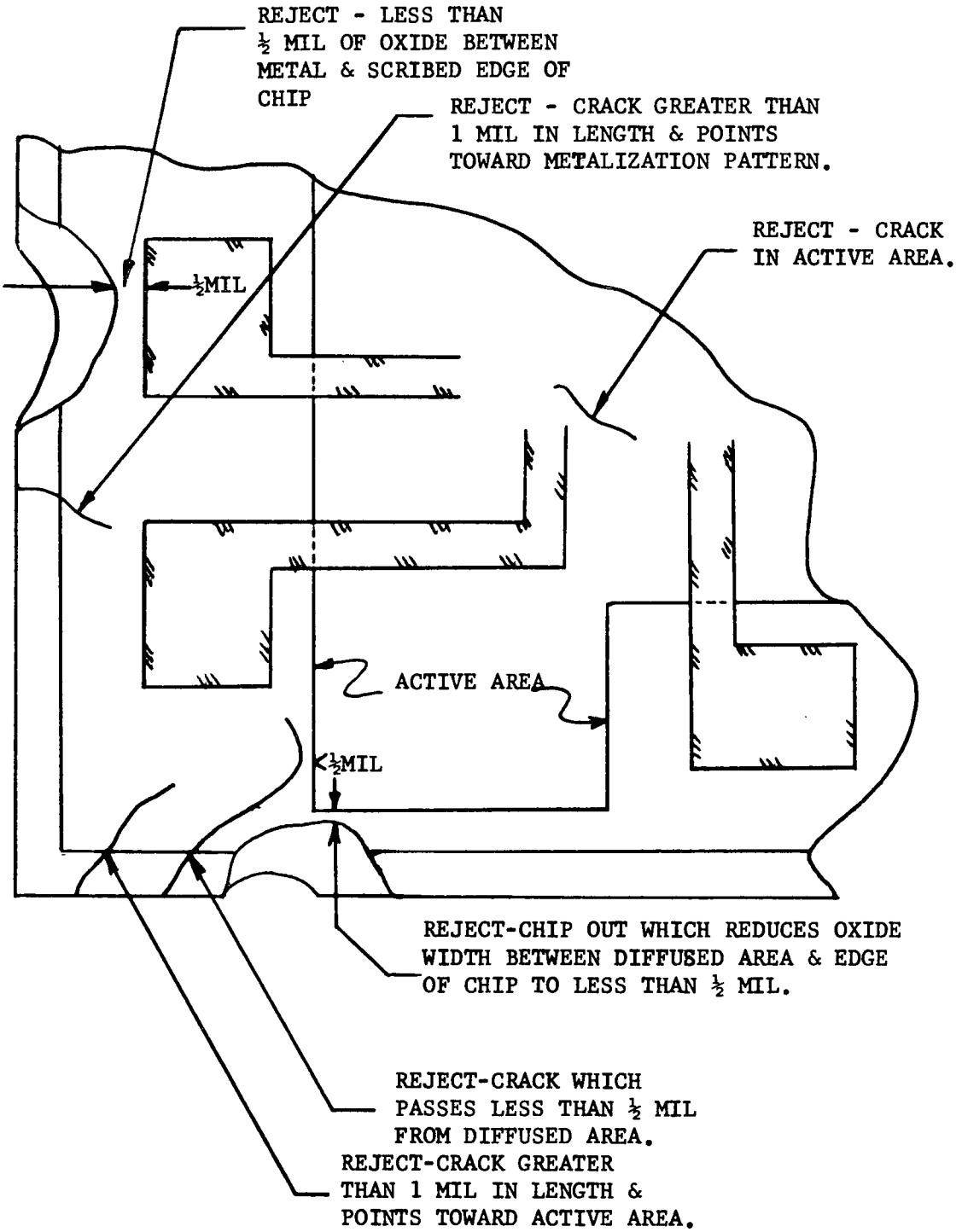


FIGURE A1 - CRACK AND CHIP OUT REJECT CRITERIA

b. Poor metal delineation resulting in missing bonding pad material.

c. Metalization scratches, that expose SiO_2, completely across bonding pad, thus reducing portion of pad attached to interconnect to insufficient size.

* A1.3 Foreign Material:

Reject any die which contains metallic or conductive foreign material under the passivating or insulating dielectric oxide layer if the material is located near metalized areas and the particle is greater than one half (1/2) of the designed space between the metalization patterns. Any visible particle will be considered conductive.

A1.4 Processing Material:

A1.4.1 Reject any die that exhibits an ink dot indicative of failure to the die sort electrical test.

A1.4.2 Reject any die that exhibits residual photo resist or other processing materials.

A1.4.3 Reject any die that exhibits evidence of corrosion or discoloration of the metalization pattern.

*A2.0 METALIZATION DEFECTS - (150X minimum magnification, binocular microscope, bright field illumination normal to chip surface).

A2.1 Scratches and Voids: (See Figures A2 and A3)

Reject any die which exhibits:

a. A scratch, void, or smear in the interconnecting metalization which reduces the width of the undisturbed metal to less than one-half (½) of the minimum designed width, provided the scratch exposes the underlying material at any point along its length. (Figure A2)

b. A scratch, void or smear in the interconnecting metalization over a contact cut, or a via, if the defect isolates more than one-half (½) of the designed contact from the interconnecting metalization. (Figure A2)

* Indicates reduced criteria exists for Class "B" devices. See appropriate B.X.X.X subsection.

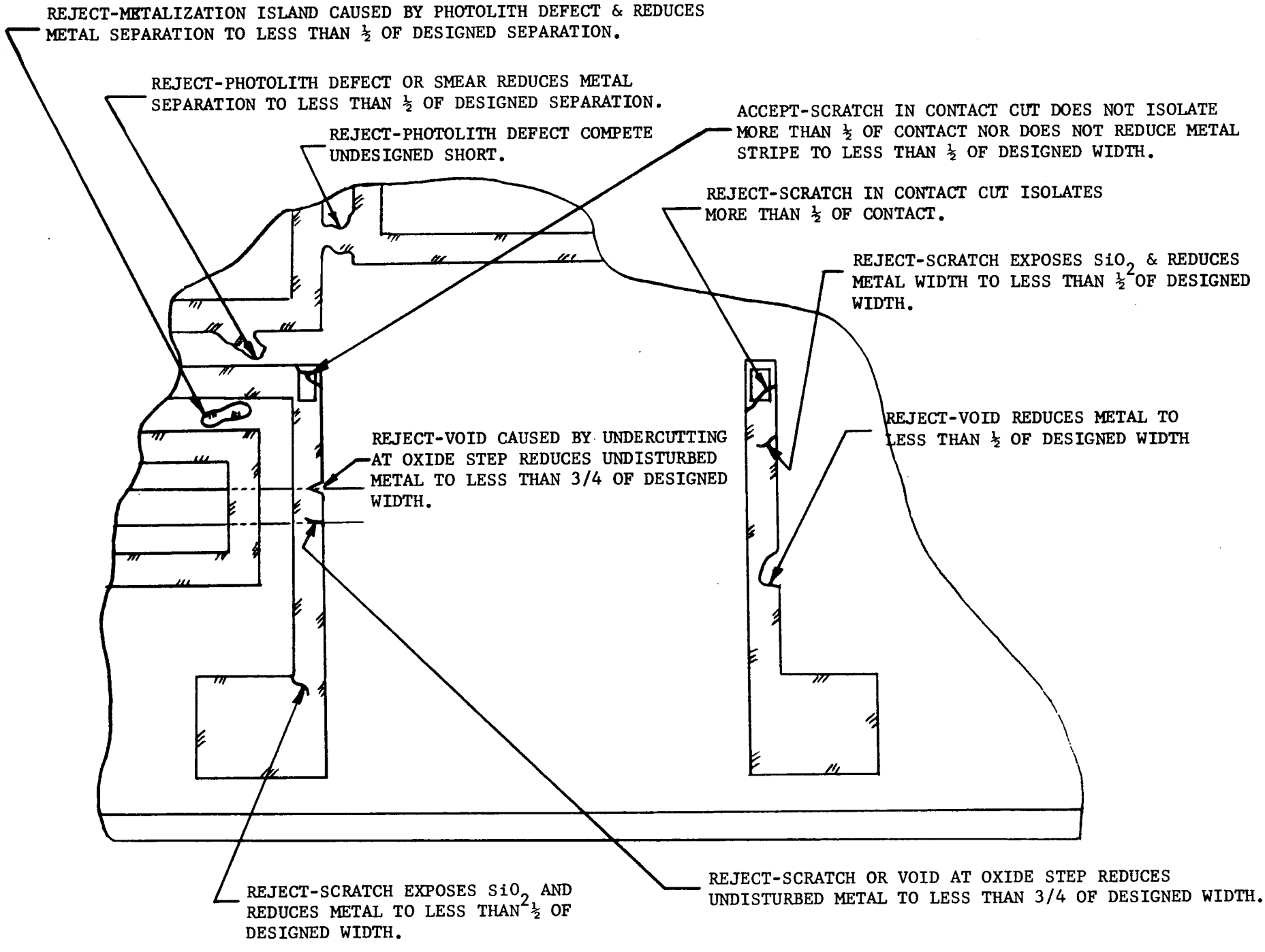


FIGURE A2 - METALIZATION DEFECTS
A4

* c. A scratch, void, or smear in the interconnecting metalization at any thermal or insulating dielectric oxide step which reduces the width of the undistrubed metal at the step to less than 3/4 of the minimum design width. (Figure A2)

d. A scratch, void, or smear in the gate metal which results in incomplete metal coverage of the age oxide. (MOS Structures only - Figure A3)

* A2.2 Bridged Metalization: (Figure A2)

Reject any die which exhibits bridged metalization defects to the extent that the distance between any two metalization stripes of the same metalization plane is reduced to less than one-half (½) of the designated separation width. The bridging may be caused by smears or defective metal delineation.

A3.0 ALIGNMENT - (80X minimum magnification, binocular microscope, bright field illumination normal to chip surface).

* A3.1 Gate Metal:

Reject any die which exhibits a misalignment of the gate metal such that the gate metal does not overlap the edge of the source and drain diffusions along the length of the channel, or is not, at least, coincident with the edge of the gate oxide along the width of the channel. Inspect two gates on diagonally opposite corners of each chip. (MOS Structures only - Figure A3)

* A3.2 Contact Cut:

Reject any die which exhibits a misalignment of contact cuts such that the minimum spacing between the cut and edge of the diffusion to which contact is made is less than 0.1 mils. Inspect two contact cuts on diagonally opposite corners of each chip. (Figure A3)

* A3.3 Gate Oxide:

Reject any die in which the gate oxide does not overlap the edges of the source and drain diffusions. Examine two gates on diagonally opposite corners of each chip. (MOS Structures only - Figure A3)

A4.0 OXIDE DEFECTS AND DIFFUSION FAULTS - (80X minimum magnification, binocular microscope, bright field illumination normal to surface of chip).

* Indicates reduced criteria exists for Class "B" devices. See appropriate B.X.X.X. subsection.

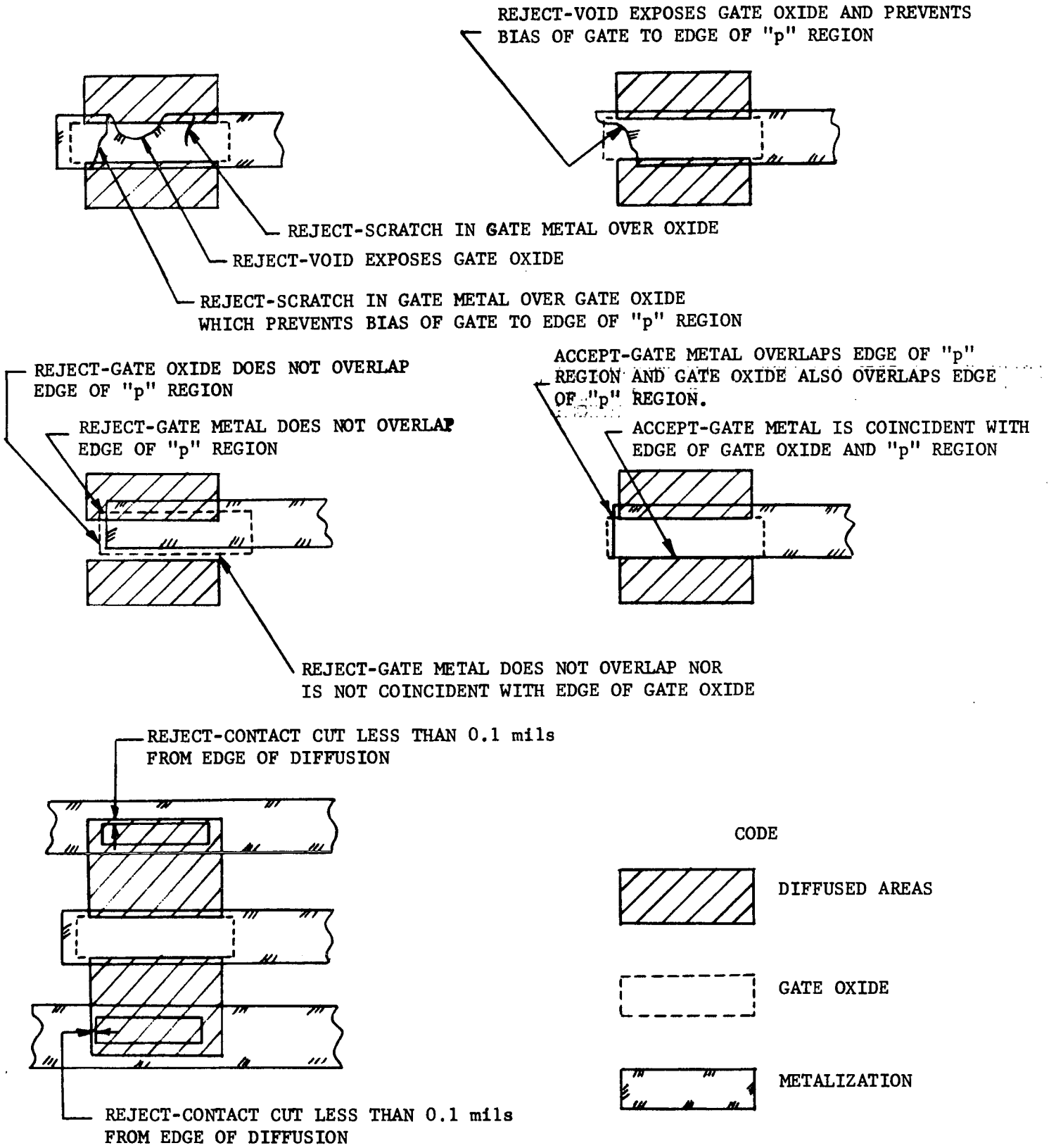


FIGURE A3 - GATE METAL DEFECT REJECTION CRITERIA

A4.1 Oxide Defects:

Reject any device in which a thermal or a deposited oxide defect:

a. Exceeds 40 square mils (approximately the size of two bonding pads.),

b. Exceeds 15 mils in its longest dimension,

c. Occurs under a metalized area and appears to be a short to the silicon chip or to underlying metalization. Newton fringes around periphery of defect indicates defect has depth,

d. Occurs under a metalized area between two "p" regions and appears capable of acting as a parasitic MOS transistor,

e. Connects a metal stripe to a diffused area not already connected to the stripe,

f. Connects two metal stripes,

g. Results from variations in the underlying crystalline structure and occurs across diffusion junctions, or occurs under or partially under metalization patterns.

A4.2 Spurious Diffusion Defects:

Reject any die in which a diffusion defect:

a. Shorts any two diffused areas,

b. Causes any diffusion to appear to be discontinuous,

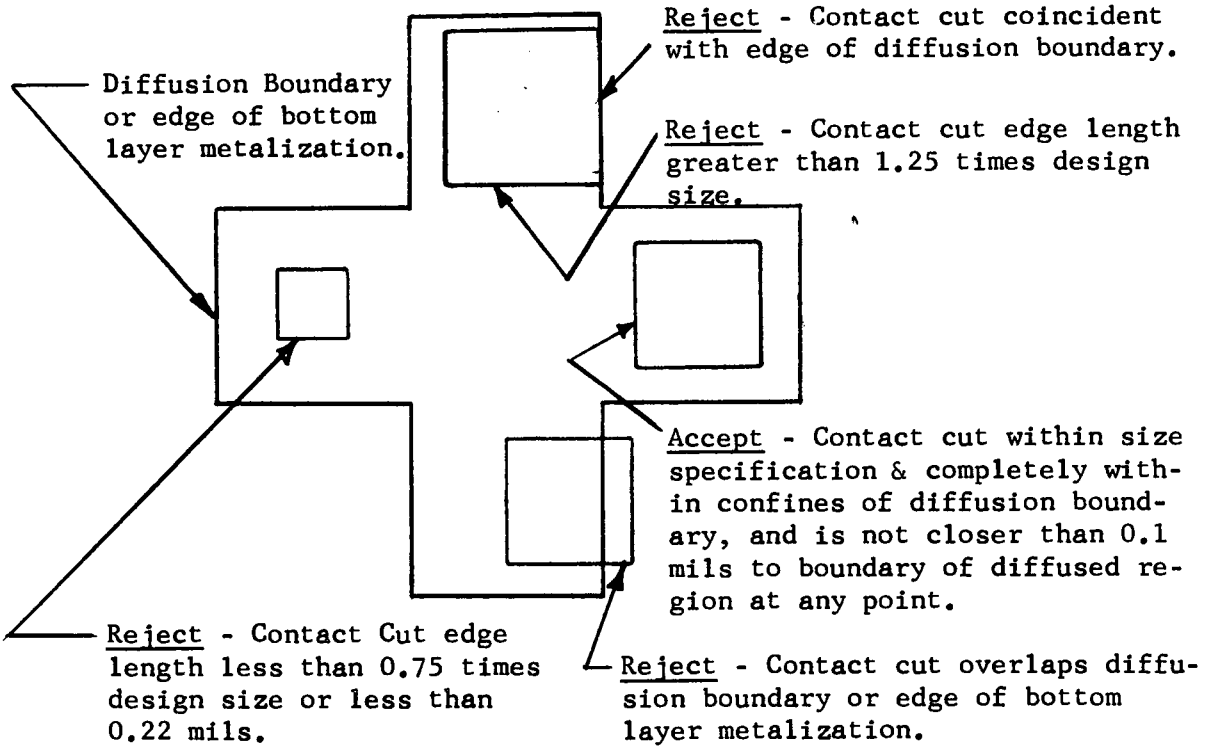
* c. Reduces the separation between any two diffusions to less than 0.2 mils, or to less than the minimum design spacing, when the diffusions are adjacent to or under any metal stripes except ground stripes.

* d. Reduces the diffusion width to less than one-half (½) the design width.

A5.0 CONTACT AND VIA CUTS - (80X minimum magnification, binocular microscope, bright field illumination normal to surface of chip).

* Indicates reduced criteria exists for Class "B" devices. See appropriate B.X.X.X. subsection.

* A5.1 Reject any die that exhibits contact cuts in which the lengths of edges of the cuts are less than 3/4 or more than 1-¼ times the design sizes. Contact cuts that are within the size limitation, but overlap or are coincident with a diffusion boundary, shall be rejected. Contact cuts whose edges are 0.1 mils inside of a diffusion boundary are acceptable. Via cuts that are within the size limitation but overlap the edge of the bottom layer metal shall be rejected. Regardless of the above minimum edge criteria, reject any device that contains contact cuts whose edges are less than 0.22 mils.



* Indicates reduced criteria exists for Class "B" devices. See appropriate B.X.X.X. subsection.

PRESEAL VISUAL WIRE & CHIP BONDING INSPECTION CRITERIA FOR CLASS "A" DEVICES

A6.0 CHIP BONDS - (30X minimum magnification, binocular microscope, oblique illumination).

* A6.1 Reject any device in which the die is rotated by more than $\pm 15^{o}C$ from the designed orientation and/or is misplaced by more than one-half ($\frac{1}{2}$) its smallest dimension (width) from its design location.

* A6.2 Reject any device in which the resolidified eutetic is not visible along all four sides of the die.

* A6.3 Reject any device in which the resolidified eutetic fillet is higher than one-half ($\frac{1}{2}$) of the die thickness.

A6.4 Reject any device in which the resolidified eutetic shows evidence of cracking, chipping, aggolmerating or flaking.

A7.0 BONDING WIRES - (30X minimum magnification, binocular microscope, bright field illumination normal to surface of die).

A7.1 Bond Location:

A7.1.1 Reject any device in which the compressed portion of any wire bond is:

a. Less than 75% within the confines of the chip bonding pad.

b. Less than 100% within the confines of the flat on the package bonding area.

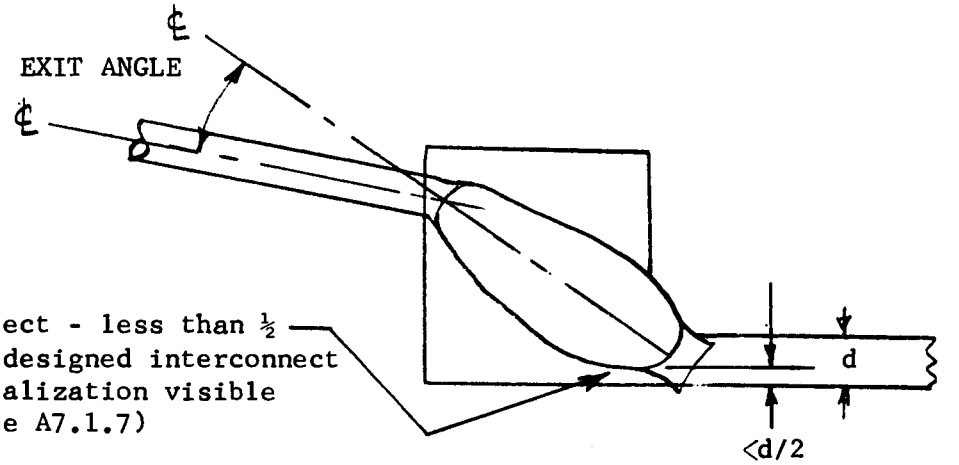
A7.1.2 Reject any device in which the compressed portion of any chip wire bond is not separated from the edge of the chip by 0.5 mils of oxide, unless there is no oxide by design.

A7.1.3 Reject any device in which the compressed portion or the tail of any wire bond is closer than 1 mil to an adjacent bond, or to a metalization pattern other than that to which it is bonded.

* Indicate reduced criteria exists for Class "B" devices. See appropriate B.X.X.X. subsection.

A7.1.4 Reject any device in which any bond is placed such that the wire leading from any bond crosses a wire from any other bond.

* A7.1.5 Reject any device in which any bond is located such that the wire exit angle (measured from the logitudinal ℄ of the wire to the logitudinal ℄ of the compressed portion of the bond) is greater than 15°.



A7.1.6 Reject any device in which the bonds are so placed that the wire from any bond is closer than 2.0 mils to the wire from any other bond at any point along their length except for the first 10 mils of length adjacent to the chip bond.

A7.1.7 Reject any device in which the bond is so placed that the metal width visible between the bond and the aluminum interconnect from the bonding pad is less than 50% of the narrowest design width of the interconnect.

A7.1.8 Reject any device in which the bonding pad shows evidence of smearing from sliding of the bond across the pad during placement.

A7.1.9 Reject any device containing a rebond over a preciously bonded area, or over a previous bond.

A7.2 Bond Size:

Reject any device containing any bond which does not meet the following size criteria:

a. Chip bonds:
   1. Bond compression length 3 to 5 mils.

* Indicates reduced criteria exists for Class "B" devices. See appropriate B.X.X.X. subsection.

* 2. Bond compression width 1.3 to 2.4 mils, and the compressed width does not vary between the heel and toe by more than one-half (½) the wire diameter.

b. Package bonds:
1. Bond compression length 3 to 5 mils.

2. Bond compression width 1.5 to 2.5 mils and the compressed width between the heel to toe does not vary by more than one-half (½) the wire diameter.

c. Chip and package bonds:
1. Bond tails shall not exceed two (2) wire diameters in length.

A7.3 Rebonds:

Reject any device which exhibits evidence of any rebonds on the chip bonding pad or on any package bonding pad.

A7.4 Wire Condition:

A7.4.1 Reject any device in which any bonding wire shows:

a. Nicks, cuts, crimps, neck down, or scoring of the wire which reduces the wire diameter by 25%.

b. The horizontal displacement of a wire run shall not exceed 3 wire diameters from the imaginary straight line between its terminal points (pad and post bond).

c. Excessive loop or sag in any bonding wire such that it could short to another wire, another package post to the die, or to any portion of the package.

A7.4.2 Reject any device in which there are any missing, broken, or incorrectly connected wires.

A8.0 PACKAGE CONDITION - (30X minimum magnification, binocular microscope, oblique illumination).

A8.1 Reject any device whose package exhibits:

a. Foreign material imbedded or attached in the package that would affect package quality or insulation resistance. Foreign material firmly attached to the package whose major dimension is less than 2 mils are acceptable, provided they do not interfer with the seal. Particles will be considered firmly attached if they cannot be removed with a nitrogen blow at a pressure of 20 psig.

* Indicates reduced criteria exists for Class "B" devices. See appropriate B.X.X.X. subsection.

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b. Evidence of corrosion in any area of the package.

c. Evidence of flaking or abnormal coloration of the plating utilized on the header or package leads.

A9.0 FINAL CHIP INSPECTION - (80X minimum magnification, binocular microscope, bright field illumination normal to the die surface).

A9.1 Reject any device whose die exhibits:

a. Unattached particles, silicon chips, or other foreign materials on the surface of the die. "Unattached" is defined as those particles which can be removed by blowing by a jet of nitrogen under a pressure of not more than 20 psig. Particles may be removed by this procedure to avoid rejection. Foreign material shall not be removed with tweezers or other mechanical instruments.

b. Attached foreign material, silicon chips, or groups of particles on the die surface which bridge more than half the space between two exposed metalization patterns, or which bridge more than half the space between exposed metalization and the boundary of the passivating oxide at the edge of the die. Unattached particles may be removed as indicated in "a" above.

c. Foreign material, silicon chips, or groups of particles under the passivating top oxide of a die which bridge more than half the space between two metalization patterns, or which bridge more than half the space between metalization pattern and the boundary of the passivating oxide at the edge of the die.

d. Evidence of corrosion at any area on the die.

CLASS "B" DEVICE

VISUAL INSPECTION CRITERIA

ACCEPTANCE CRITERIA FOR CLASS "B" DEVICE CHIPS SUBSEQUENT TO CHIP & WIRE BONDING.

B1.0 DIE DEFECTS - (80X minimum magnification, binocular microscope, bright or dark field illumination).

B1.1 Scribing:

B1.1.1 Reject any die that shows evidence of scribe marks across an active or metalized area of the die.

* B1.1.2 Reject any die containing chip outs or misaligned scribe lines such that oxide is not visible between any metalization pattern, or diffusion and the scribed edge of the chip. This criteria does not apply where silicon dioxide is omitted by design. See Figure B1.

* B1.1.3 Reject any die which, because of imperfect die separation, has attached outside of the scribe line more than 25% of the adjacent die.

B1.1.4 Reject any die with a crack that exceeds 1 mil in length and occurs in the active area and/or points toward an active area, metalization, or bond. Reject any die with a crack greater than 1 mil in length, that comes closer than ½ mil to any diffusion, regardless of the direction of the crack. See Figure B1.

B1.2 Bonding Pads:

B1.2.1 Reject any die which contains a conding pad of insufficient size to contain all of the bond contact area. An insufficient bonding pad can be caused by:

a. Passivating oxide or photo resist material resulting in full or partial covering of the bonding pad.

* Indicates the Class "B" criteria are reduced from the criteria specified for Class "A" devices.

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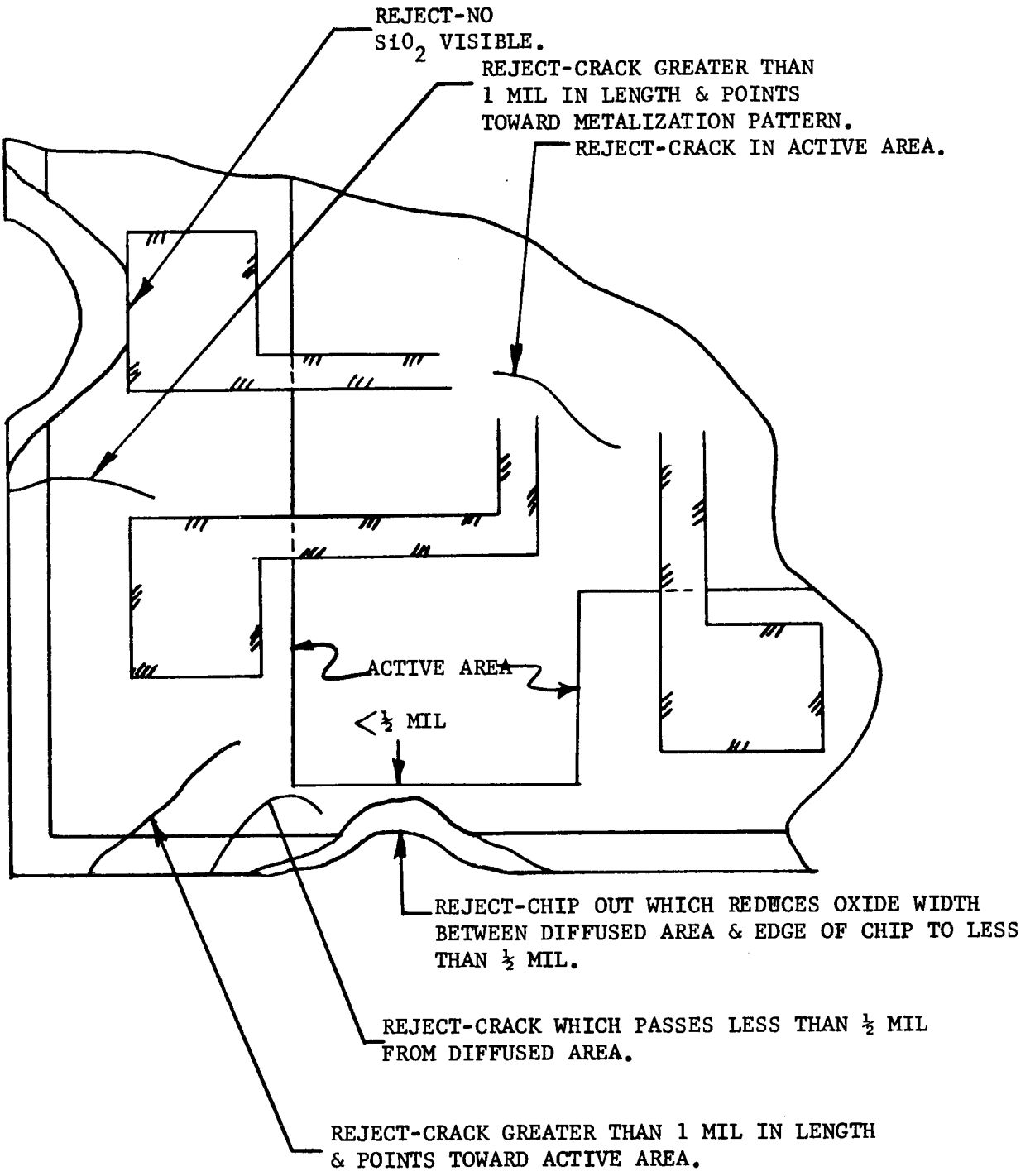


FIGURE B1 - CRACK AND CHIP OUT REJECT CRITERIA

b. Poor metal delineation resulting in missing bonding pad meterial.

c. Metalization scratches completely across bonding pad, thus reducint portion of pad attached to interconnect to insufficient size.

* B1.3 Foreign Material:

Reject any die which contains metallic or conductive foreign material under the passivating or insulating dielectric oxide layer if the material bridges the space between the metalization patterns. Any visible particle will be considered conductive.

B1.4 Processing Materials:

B1.4.1 Reject any die that exhibits an ink dot indicative of failure to the die sort electrical test.

B1.4.2 Reject any die that exhibits residual photoresist or other processing materials.

B1.4.3 Reject any die that exhibits evidence of corrosion or discoloration of the metalization pattern.

*B2.0 METALIZATION DEFECT - (80 - 100X minimum magnification, binocular microscope, bright field illumination normal to chip surface).

B2.1 Scratches and Voids: (See Figure B2 and Figure B3)

Reject any die which exhibits:

* a. A scratch, void, or smear in the interconnecting metalization which reduces the width of the undisturbed metal by three-quarters (3/4) of the minimum designed width, provided the scratch exposes the underlying material along its length. (Figure B2)

b. A scratch, void, or smear in the interconnecting metalization over a contact cut or a via, if the defect isolates more than one-half (½) of the designed contact from the interconnecting metalization. (See Figure B2)

* c. A scratch, void, or smear in the interconnecting metalization at any thermal or insulating dielectric oxide step which reduces the width of the undisturbed metal at the step by three-quarters (3/4) of the minimum design width, provided the scratch exposes silicon dioxide along its length. (See Figure B2)

* Indicates the Class "B" criteria are reduced from the criteria specified for Class "A" devices.

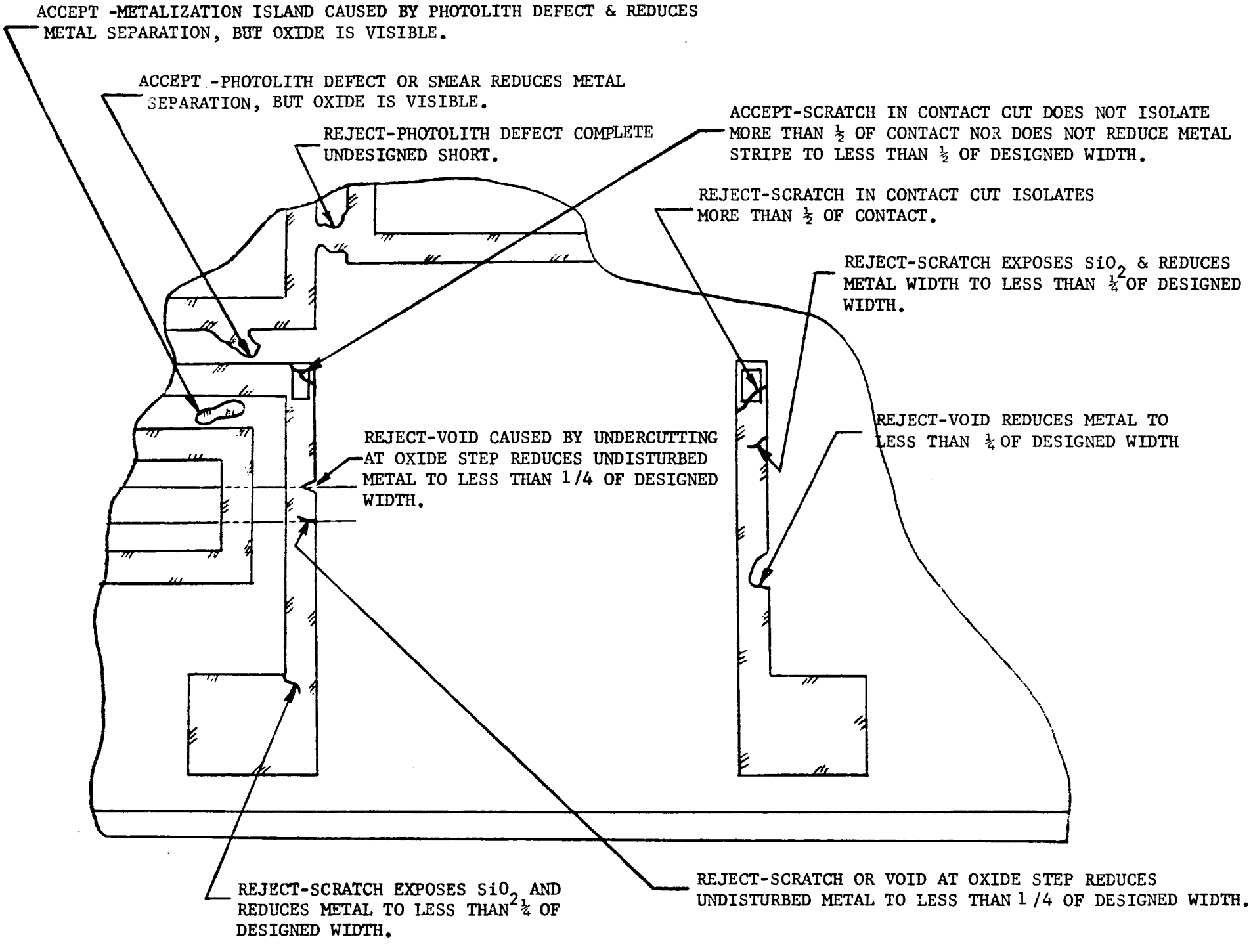


FIGURE B2 - METALIZATION DEFECTS
A16

* d. A scratch, void, or smear in the gate metal which results in incomplete metal coverage of the gate oxide. (MOS Structures only - Figure B3)

* B2.2 Bridged Metalization:

Reject any die which exhibits bridged metalization defects to the extent that oxide is not visible between any two metalization stripes of the same metalization plane. The bridging may be caused by smears or defective metal delineation. (Figure B2)

B3.0 ALIGNMENT - (80X minimum magnification, binocular microscope, bright field illumination normal to chip surface).

* B3.1 Gate Metal:

Reject any die which exhibits a misalignment of the gate metal such that the gate metal does not overlap the edge of the source and drain diffusion. Inspect two gates on diagonally opposite corners of each chip. (MOS Structures only - Figure B3)

* B3.2 Contact Cut:

Reject any die which exhibits a misalignment of contact cuts such that the edge of the cut and the edge of the diffusion are coincident. Inspect two contact cuts on diagonally opposite corners of each chip.

* B3.3 Gate Oxide:

No Class "B" criteria. (MOS Structures only)

B4.0 OXIDE DEFECTS AND DIFFUSION FAULTS - (80X minimum magnification, binocular microscope, bright field illumination normal to surface of chip).

B4.1 Oxide Defects:

Reject any device in which a thermal or a vapor deposited oxide defect:

a. Exceeds 40 square mils (approximately the size of two bonding pads).

b. Exceeds 15 mils in its longest dimension.

* Indicates the Class "B" criteria are reduced from the criteria specified for Class "A" devices.

A17

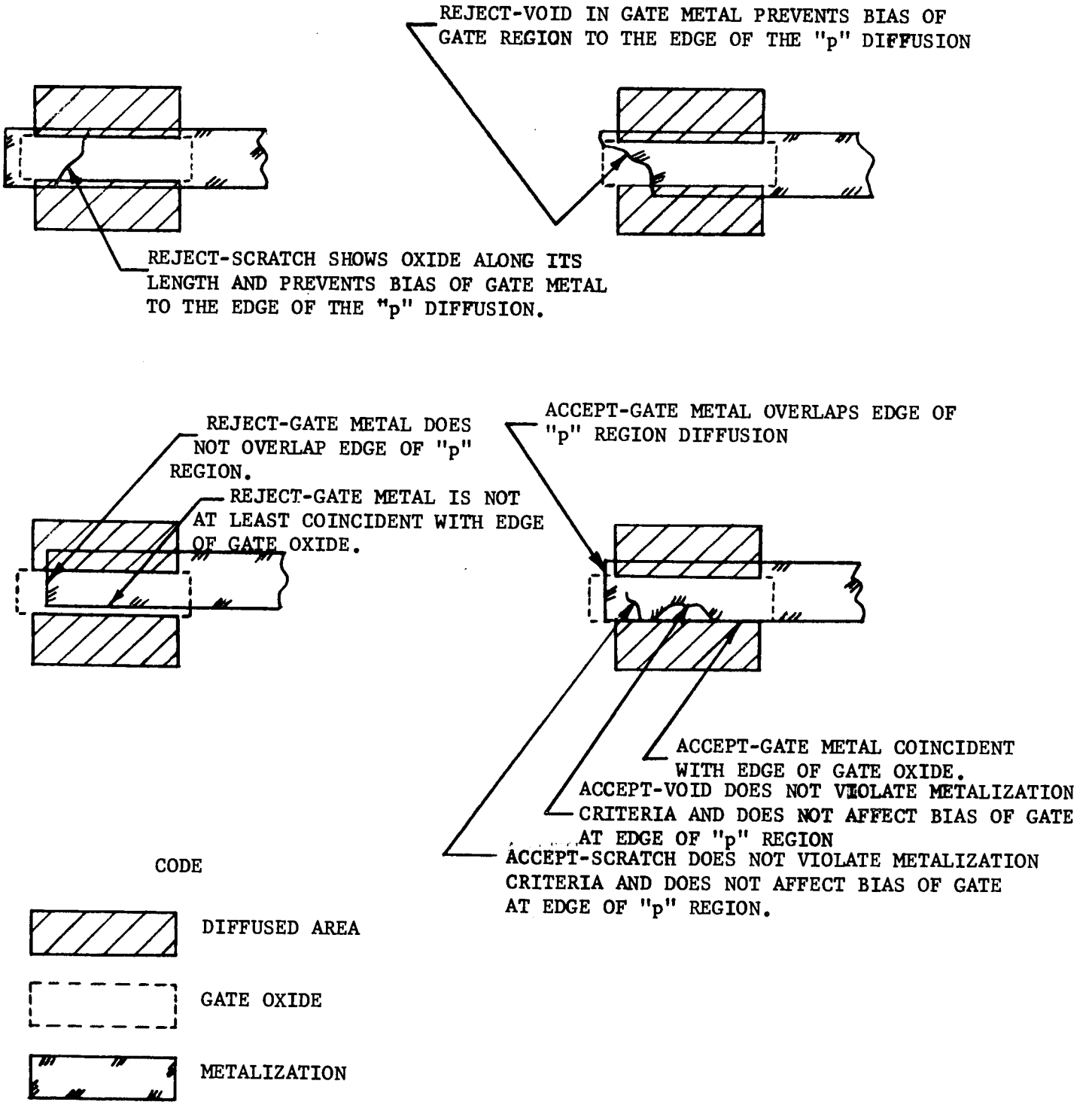


FIGURE B-3 GATE METAL REJECTION CRITERIA

c. Occurs under a metalized area and appears to be a short to the silicon chip or to underlying metalization. Newton fringes around periphery of defect indicates defect has depth.

d. Occurs under a metalized area between two "p" regions and appears capable of acting as a parasitic MOS Transistor.

e. Connects a metal stripe to a diffused area not already connected to the stripe.

f. Connects two metal stripes.

g. Results from variations in the underlying crystalline structure and occurs across diffusion junction, or occurs under or partially under metalization patterns.

B4.2 Spurious Diffusion Defects:

Reject any die in which a diffusion defect:

a. Shorts any two diffused areas.

b. Causes any diffusion to appear to be discontinuous.

* c. No Class "B" criteria.

* d. No Class "B" criteria.

B5.0 CONTACT AND VIA CUTS - (90X minimum magnification, binocular microscope, bright field illumination normal to surface of chip).

* B5.1 Reject any die that exhibits contact cuts in which the lengths of the edges of the cut are less than one-half ($\frac{1}{2}$) times the design sizes, or are 1.25 times larger than the design size. Contact cuts that are within the size limitations but overlap a diffusion boundary shall be rejected; accept overetched cuts that are coincident with a diffusion boundary. Reject any die that exhibits via cuts that overlap the edge of the bottom layer metal to which contact is to be made.

* Indicates the Class "B" criteria are reduced from the criteria specified for Class "A" devices.

B6.0 CHIP BONDS - (30X minimum magnification, binocular microscope, oblique illumination).

* B6.1 No Class "B" criteria.

B6.2 Reject any device in which the resolidified eutetic is not visible along a major portion of three sides of the die and at least 25% of the fourth side.

* B6.3 Reject any device in which the resolidified eutetic fillet is higher than the die thickness.

B6.4 Reject any device in which the resolidified eutetic shows evidence of cracking, chipping, agglomerating or flaking.

B7.0 BONDING WIRES - (30X minimum magnification, binocular microscope, bright field illumination normal to surface of die).

B7.1 Bond Location:

B7.1.1 Reject any device in which the compressed portion of any wire bond is:

a. Less than 75% within the confines of the chip bonding pad.

b. Less than 100% within the confimes of the flat on the package bonding area.

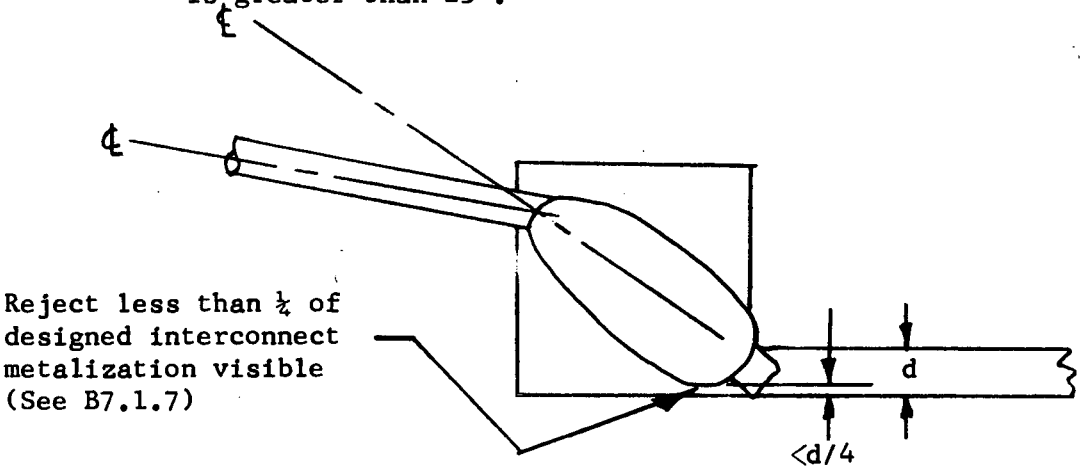
B7.1.2 Reject any device in which the compressed portion of any chip wire bond is not separated from the edge of the chip by 0.5 mils of oxide, unless there is no oxide by design.

B7.1.3 Reject any device in which the compressed portion or the tail of any wire bond is closer than 1 mil to an adjacent bond, or to a metalization pattern other than that to which it is bonded.

B7.1.4 Reject any device in which any bond is placed such that the wire leading from any bond crosses a wire from any other bond.

* Indicates the Class "B" criteria are reduced from the criteria specified for Class "A" devices.

B7.1.5 Reject any device in which any bond is located such that the wire exit angle (measured from the logitudinal ℄ of the wire to the logitudinal ℄ of the compressed portion of the bond) is greater than 25°.



B7.1.6 Reject any device in which the bonds are so placed that the wire from any bond is closer than 2.0 mils to the wire from any other bond at any point along their length except for the first 10 mils of length adjacent to the chip bond.

* B7.1.7 Reject any device in which the bond is so placed that the metal width visible between the bond and the aluminum interconnect from the bonding pad is less than 25% of the narrowest design width of the interconnect.

* B7.1.8 Reject any device in which the bonding pad shows evidence of smearing from sliding of the bond across the pad during placement, provided the smear exposes SiO_2.

B7.1.9 Reject any device containing a rebond over a previously bonded area, or over a previous bond.

B7.2 Bond Size:

Reject any device containing any bond which does not meet the following size criteria:

a. Chip bond:
   1. Bond compression length 3 to 5 mils.

   2. Bond compression width 1.2 to 2.4 mils.

* Indicates the Class "B" criteria are reduced from the criteria specified for Class "A" devices.

b. Package bonds:
   1. Bond compression length 3 to 5 mils.

   2. Bond compression width 1.4 to 2.5 mils and the compressed width does not vary by more than 0.25 mils along its entire length.

c. Chip and Package Bonds:
   1. Bond tails shall not exceed two wire diameters in length.

* B7.3 Rebonds:

Reject any device which exhibits evidence of more than one rebond on the chip bonding pad and more than one rebond on any package bonding pad.

B7.4 Wire Condition:

B7.4.1 Reject any device in which any bonding wire shows:

a. Nicks, cuts, crimps, neck down, or scoring of the wire which reduces the wire diameter by 25%.

b. The horizontal replacement of a wire run shall not exceed 6 wire diameters from the imaginary straight line between its terminal points (pad and post bond).

c. Excessive loop or sag in any bonding wire such that it could short to another wire, another package post to the die, or to any portion of the package.

B7.4.2 Reject any device in which there are any missing, broken, or incorrectly connected wires.

B8.0 PACKAGE CONDITION - (30X minimum magnification, binocular microscope, oblique illumination).

B8.1 Reject any device whose package exhibits:

a. Foreign material imbedded or attached in the package that would affect package quality or insulation resistance. Foreign material firmly attached to the package whose major dimension is less than 2 mils are acceptable, provided they do not interfere with the seal. Particles will be considered firmly attached if they cannot be removed with a nitrogen blow at a pressure of 20 psig.

* Indicates the Class "B" criteria are reduced from the criteria specified for Class "A" devices.

b. Evidence of corrosion in any area of the package.

c. Evidence of flaking or abnormal coloration of the plating utilized on the header or package leads.

B9.0 FINAL CHIP INSPECTION - (80X minimum magnification, binocular microscope, bright field illumination normal to the die surface).

B9.1 Reject any device whose die exhibits:

a. Unattached particles, silicon chips, or other foreign material on the surface of the die. "Unattached" is defined as those particles which can be removed by blowing a jet of nitrogen under a pressure of not more than 20 psig. Particles may be removed by this procedure to avoid rejection. Foreign material shall not be removed with tweezers or other mechanical instruments.

b. Attached foreign material, silicon chips, or groups of particles on the die surface which bridge more than half the space between two exposed metalization patterns, or which bridge more than half the space between exposed metalization and the boundary of the passivating oxide at the edge of the die. Unattached particles may be removed as indicated in "a" above.

c. Foreign material, silicon chips, or groups of particles under the passivating top oxide of a die which bridge more than half the space between two metalization patterns, or which bridge more than half the space between a metalization pattern and the boundary of the passivating oxide at the edge of the die.

d. Evidence of corrosion at any area on the die.

APPENDIX B

WORST CASE DESIGN ANALYSIS OF THE DCQ BASIC CELL AT -55°C BASED ON BBTP1 TEST DATA

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APPENDIX "B"

WORST CASE DESIGN ANALYSIS OF THE DCQ BASIC CELL AT -55°C BASED ON BBTP1 TEST DATA

B1.0 INTRODUCTION

The data presented in this appendix consists of:

a. The temperature correction factors applied to the room temperature BBTP1 parameter data.

b. The worst case equations for the basic DCQ cell parameters V_{OH}, I_{OL} and I_{SC}.

c. Examples of the calculations performed and a summary of the calculated values on a wafer by wafer basis.

B2.0 TEMPERATURE CORRECTION FACTORS

The individual structures of a diffused silicon integrated circuit all exhibit temperature coefficients which are function of the impurity density used for their fabrication. Resistors exhibit a positive temperature coefficient. Transistors exhibit a positive temperature coefficient for current gain and saturations voltage, and a negative temperature coefficient for forward biased diode. Diodes like transistors show a negative temperature coefficient for the forward voltage parameter.

B2.1 Temperature Coefficient of Resistance

Figure B1 shows a family of curves for the temperature coefficients of silicon diffused resistors. The mean sheet resistance for each of the wafers was shown in figure 3.2.10. The temperature coefficient for the resistors from each of the wafers was determined by fitting this value to the curves of figure B1 and extrapolating the curve to -55°C. The typical coefficient for all of the wafers was approximately 1700 parts per million per °C. The values obtained are shown by wafer in table B1.

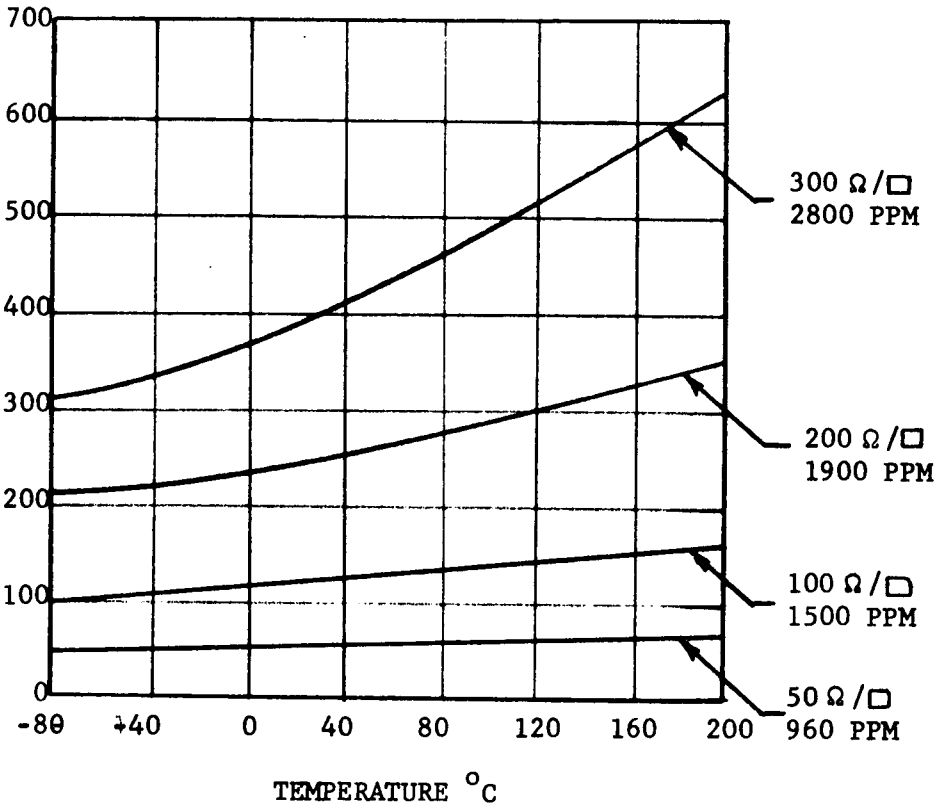

FIGURE B1 - RESISTOR VARIATIONS AS A FUNCTION OF TEMPERATURE FOR DIFFERENT SHEET RESTIVITIES (FROM PHILCO FORD MICROELECTRONICS TRAINING MANUAL - 12 MAY 1964)

WAFER	R_{25} K	R_6 K	R_5 K	R_L	h_{FEM} ----	h_{FEO} ----	V_{BEM} volts	V_{BEO} volts	$V_{CE(SAT)}$ volts
A	25.0	6.0	5.0	500	12.5	11.5	0.89	0.91	0.11
I	26.0	6.2	5.2	520	8.0	8.0	0.89	0.91	0.11
H	24.2	5.8	4.8	484	6.5	6.5	0.89	0.91	0.11
E	32.8	7.85	6.5	655	8.5	8.5	0.96	0.98	0.11
F	30.0	7.25	6.1	610	7.5	11.5	0.90	0.92	0.11
G	24.2	5.80	4.8	484	7.5	8.5	0.93	0.95	0.11
J	31.1	7.50	6.2	620	12.5	13.5	0.89	0.91	0.11
B,C	28.5	6.85	5.7	570	12.0	13.5	0.89	0.91	0.11
D	35.4	8.50	7.1	705	17.0	14.0	0.89	0.89	0.11

TABLE B1 - INDIVIDUAL PARAMETER VALUES AT -55°C

B2.2 Transistor Parameters

The temperature coefficients for the transistor parameters was determined directly by measuring a sample of the devices at room temperature and then at -55°C. The mean values obtained for the parameters h_{FEM}, h_{FEO}, V_{SAT}, amd V_{BE} are shown by wafer in table B1.

B3.0 WORST CASE EQUATIONS

The equations shown in the following subsections were derived from the electrical configuration of the basic DCQ cell, shown in figure B2, and were used together with the parameter values shown in table B1 for the determination of the short circuit current, (Isc), the high level output voltage (Voh) and the low level output current (Iol). The forcing functions used in the calculations were the voltages and currents defined in the DCQ specification.

B3.1 Short Circuit Current

The short circuit current is that current measured with the output grounded and the output transistor in the "off" state. It represents the worst case current the device will be required to supply, and is approximately the sum of the current which flows through the resistors R_6 and R_L. The exact equation is:

$$I_{SC} = I_6 + I_L - I_{LEAKAGE(Q2\ AND\ Q4)}$$

but since the typical leakage currents measured on the DCQ at 0°C were essentially zero then

$$I_{SC} \cong I_6 + I_L$$

$$I_{SC} = \left(\frac{V_{CC} - V_{BE(Q3)} - V_{BE(D1)}}{R_6}\right) + \left(h_{FEO}\cdot(Q3)\cdot I_6\right)$$

$$I_{SC} = \left(\frac{V_{CC} - 2V_{BE}}{R_6}\right)\left(1 + h_{FEO(Q3)}\right)$$

provided the second term of the equations does not result in a voltage drop between V_{CC} voltage. i.e.

$$I_L R_L + V_{CE(Q3)} + V_{BE(D1)} \quad V_{CC}$$

in all of the cases evaluated the h_{FE} of the transistor Q3 was sufficiently low that I_L did not cause a large enough voltage drop to

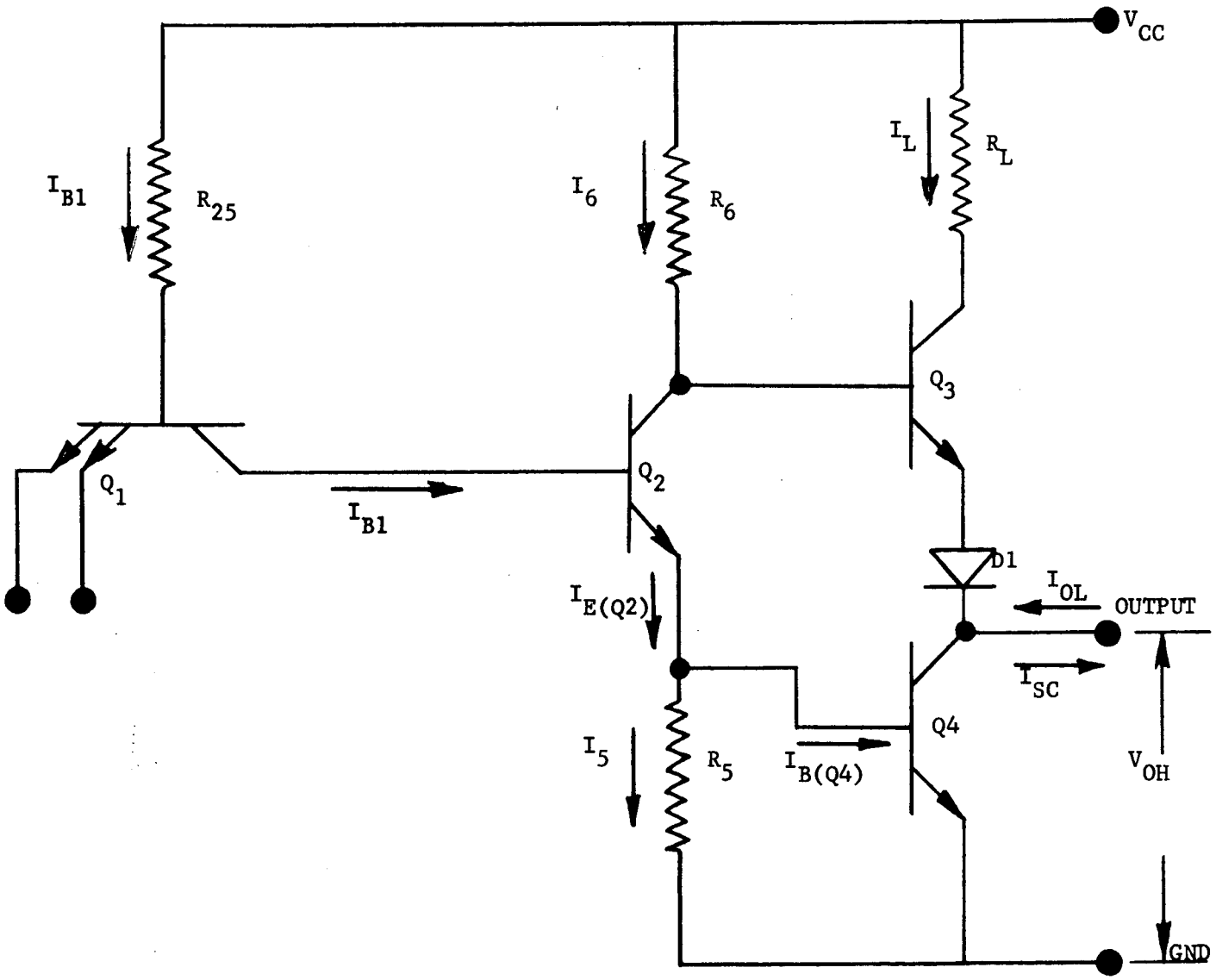

FIGURE B2 - CIRCUIT DIAGRAM - DCQ BASIC CELL

invalidate the equations shown for I_{SC}.

For wafer A

$$I_{SC} = \left(\frac{5.00 - 1.8}{6000}\right)\left(1 + 11.5\right) = 6.47 \text{ mA}$$

The values determined for all wafers are shown in table B2.

B3.2 High Level Output Voltage

The defining equation for the high level output voltage is:

$$V_{OH} = V_{CC} - V_{BE(Q3)} - V_{BE(D1)} - I_6 R_6$$

But I_6 must be of a value such that, I_{OH}, the current required at the output pins is equal to the specified value.

$$I_{OH} = I_{E(Q3)} = I_L + I_6$$

It must also be determined whether the transistor Q3 is in the active or the saturated condition to determine the magnitude of I_L. The conditions determining the state of the transistor are if:

$$h_{FEO(Q3)}(I_6) \geq I_L \longrightarrow \text{satuation}$$

$$h_{FEO(Q3)}(I_6) < I_L \longrightarrow \textbf{Active}$$

In all cases the transistor Q3 was operating in the active region.

Since

$$I_{OH} = I_L + I_6$$

Then

$$I_{OH} - I_6 = I_L$$

and

$$h_{FEO}(I_6) = I_L = I_{OH} - I_6$$

$$I_6 = \frac{I_{OH}}{1 + h_{FEO}}$$

then

$$V_{OH} = V_{CC} - V_{BE(Q3)} - V_{BE(D1)} - \frac{I_{OH}}{1 + h_{FEO(Q3)}}$$

solving the above equations for wafer A.

$$V_{OH} = 4.70 - 0.9 - \frac{0.465}{1 + 11.5} = 2.66 \text{ volts}$$

The calculated values for all wafers based on the parameters data shown in table B1 are given in table B2.

B3.3 Low Level Output Current

The DCQ specification sheet shows that the output low level voltage must be lower than 0.3 volts when the output low level current is at 3.4 mA. The V_{OL} of the DCQ basic cell can be described as:

$$V_{OL} = V_{CE(SAT)Q4}$$

Although the $V_{CE(SAT)}$ of the output transistor can be calculated based on measured parameters and sheet and bulk resistances through the use of the equation

$$V_{CE(SAT)} = \frac{-KT}{Q} \ln \alpha_i \frac{(1 - I_C/h_{FE} I_B)}{1 + (I_C/I_B)(1 - \alpha_i)} + I_C r_{SC}$$

where:

α_i = The inverse alpha of the transistor

Q = electronic charge

T = absolute temperature

K = Boltzman constant

r_{SC} = the collector saturation resistance which is determined by the geometry of the device and the collector resistivity

The difficulty in the application of this equations is there is no assurance that the output transistor is fully into saturation, however, application of the equations yields results that agree quite well with the measured $V_{CE(SAT)}$ of the output transistor of the BBTP1 vehicle (The measured -55°C $V_{CE(SAT)}$ value is 0.11 volts and the calculated value is 0.095 volts.) To avoid the difficulty imposed by inadequate knowledge of whether Q4 is completely into saturation. I_{OL} was calculated with the assumptions that V_{OL} was at its maximum specified limit of 0.3 volts.

The defining equation for I_{OL} is:

$$I_{OL} = h_{FEO}\left(I_{E(Q2)} - I_{BQ4}\right)$$

$$I_{OL} = h_{FEO}\left(I_{E(Q2)} - \frac{V_{BEO}}{R_5}\right)$$

where $I_{E(Q2)}$ is the minimum value obtained from either of the following two equations:

$$I_{E(Q2)} = (1 + h_{FEO})\ I_{B1}$$

or

$$I_{E(Q2)} = \frac{V_{CC} - V_{BEO(Q4)} - V_{CE(SAT)Q2}}{R_6} + I_{B1}$$

where I_{B1} is the base current into the multiple emitter input transistor and is:

$$I_{B1} = \frac{V_{CC} - V_{BEO(Q2)} - V_{BEO(Q4)} - V_{SAT(Q1)} - V_{BEM(Q1)}}{R_{25}}$$

The reason for taking the minimum value of $I_{E(Q2)}$ is if the resistor R_6 is too high in value to permit the current required by the I_{B1} (h_{FEO}) product, the transistor Q2 will go into saturations the current drawn will be that current defined by the equations containing the $V_{CE(SAT)Q2}$ terms. If the $I_{E(Q2)}$ value is not resistor limited and transistors Q2 does not go into saturations the $I_{E(Q2)}$ current will be defined by the equations containing the $(1 + h_{FEO})$ terms. Examinations of the equations show that the proper $I_{E(Q2)}$ current will be the minimum value obtained from the solutions of both of the $I_{E(Q2)}$ equations. In the evaluations of each of the wafers, the non saturated transistor equations was used only for the evaluations of wafers H and E. In all of the remaining wafers the base drive was sufficient to force Q2 into saturations. The solutions of the I_{OL} equations for wafer A is:

$$I_{OL} = h_{FEO}\left[\left(\frac{V_{CC} - V_{BEO(Q4)} - V_{CE(SAT)Q2}}{R_6} + \frac{V_{CC} - V_{BEO(Q2)} - V_{BEO(Q4)} - V_{CE(SAT)Q1} - V_{BEM(Q1)}}{R_{25}}\right) - \frac{V_{BEO(Q4)}}{R_5}\right]$$

$$I_{OL} = 11.5\left[\left(\frac{4.75-0.91-0.11}{6} + \frac{4.75-0.91-0.11-0.89}{25}\right) - \frac{0.91}{5}\right] = 5.97\ \text{mA}$$

and the solutions of the I_{OL} equations for wafer H is:

$$I_{OL} = h_{FEO}\left[(1 + h_{FEO})\left(\frac{V_{CC}-V_{BEO(Q2)}-V_{BEO(Q4)}-V_{SAT(Q1)}-V_{BEM(Q1)}}{R_{25}}\right) - \frac{V_{BEO(Q4)}}{R_5}\right]$$

$$I_{OL} = 8.0\left[(1 + 8)\left(\frac{4.75-0.91-0.91-0.11-0.89}{25}\right) - \frac{0.91}{4.8}\right] = 4.27 \text{ mA}$$

The calculated values for all wafers are shown in table B2.

LOT	WAFER	I_{SC} mA	V_{OH} VOLTS	I_{OL} mA
33/15	A	6.47	2.66	5.97
35/9	I	4.89	2.56	4.28
35/12	H	4.95	2.56	4/27
38/3	E	3.72	2.31	2.97
38/7	F	5.50	2.61	4.91
38/8	G	5.14	2/48	4.38
38/12	J	6.18	2.64	5.67
39/13	B,C	6.77	2.64	6.13
39/14	D	5.63	2.62	5.23

TABLE B2 - CALCULATED (-55°C) VALUES FOR I_{SC}, V_{OH} AND I_{OL} BASED ON BBTP1 TEST DATA.