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NASA CR- 130163

NTIS HC #27.50

AED R-3318F
April 23, 1970

ITOS
Meteorological Satellite System

TIROS M Spacecraft (ITOS 1)
Final Engineering Report

Volume I

(NASA-CR-130163) ITOS METEOROLOGICAL SATELLITE SYSTEM: TIROS M SPACECRAFT (ITOS 1), VOLUME 1 Final Engineering Report (Radio Corp. of America) 510 p HC $27.50 CSCL 22B G3/31

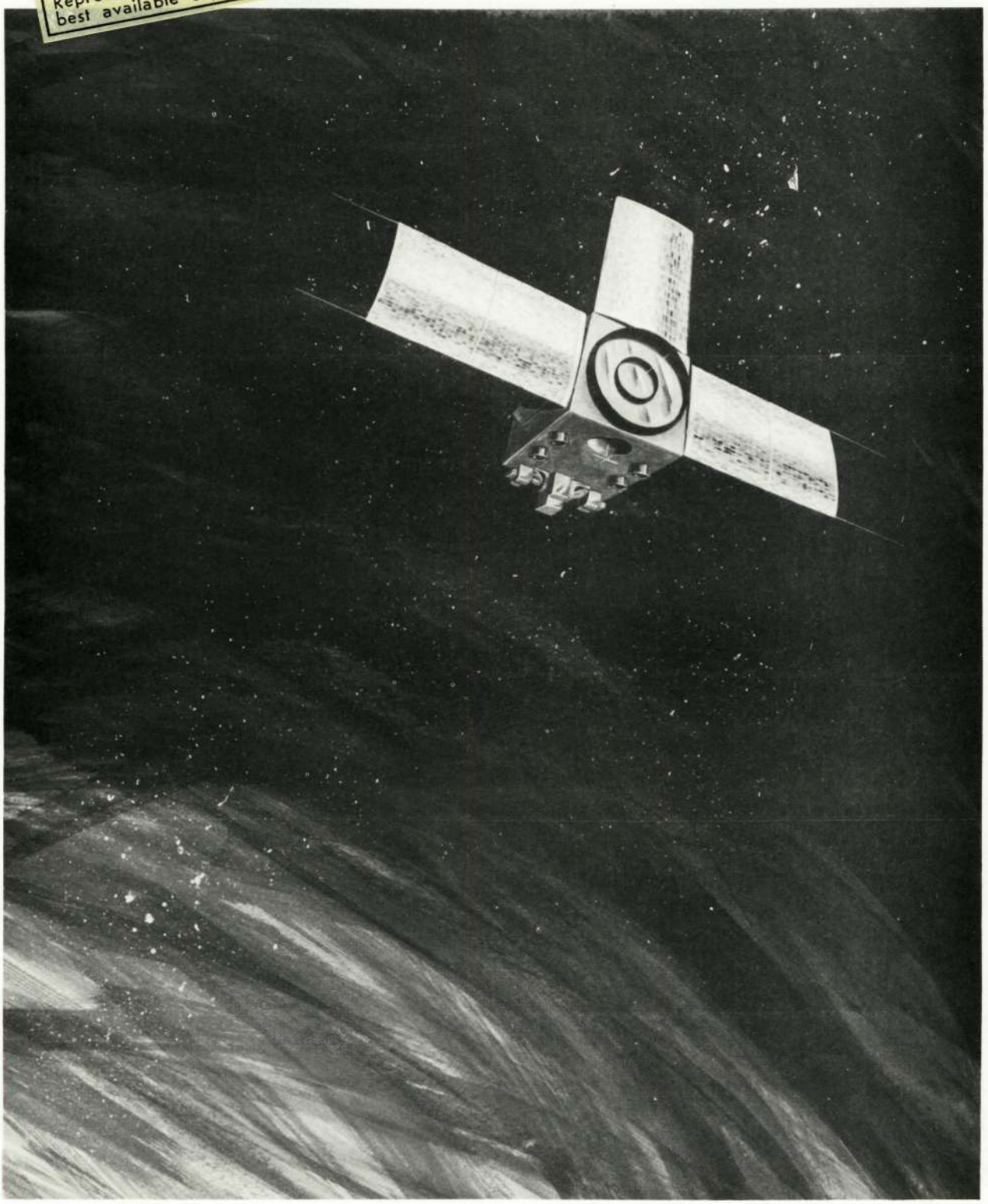
N73-16880

Unclas 54428

Prepared for
Goddard Space Flight Center
National Aeronautics and Space Administration
Washington, D.C.
Contract No. NAS5-10306

RCA

RCA | Defense Electronic Products
Astro Electronics Division | Princeton, New Jersey



Artist's Concept of the ITOS Spacecraft

PREFACE

The TIROS M (ITOS 1) spacecraft was developed and built by the Astro-Electronics Division of RCA Corporation for the Goddard Space Flight Center of the National Aeronautics and Space Administration, under NASA Contract NAS5-10306. The TIROS M (ITOS 1) spacecraft was developed to meet the requirements of an Improved TIROS Operational System (ITOS) mission, and became, upon attaining successful operation in orbit, the first of the second-generation operational meteorological satellites.

This document provides system, subsystem, and component descriptions for the spacecraft and ground support equipment, and documents the design, development, testing, and integration phases of the program. It also describes the prelaunch and launch activities in which RCA personnel participated.

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PART 1. INTRODUCTION

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SECTION I. THE ITOS SYSTEM AND MISSION

The TIROS M spacecraft was successfully launched from the Western Test Range at 1131 hours GMT on January 23, 1970. With this launching and the successful operation of the satellite in orbit (designated as ITOS 1), the Improved TIROS Operational System (ITOS) was inaugurated as the second generation operational meteorological satellite system. This report describes the ITOS program of design engineering, construction, and testing from its inception to the launching of TIROS M.

TIROS M is the first flight model spacecraft of the ITOS series, which, at this writing, includes five additional flight-model spacecraft designated ITOS A through E. The ITOS system represents an expansion of operational capabilities over its predecessor, the TOS system, as well as the implementation of advancements in the use of satellite sensory devices and techniques for meteorological data-gathering. A single satellite of the ITOS system exceeds the mission capabilities of both of the complementary ESSA satellites of the TOS system (TOS APT and TOS AVCS) by furnishing complete global observations of Earth's cloud cover every 12 hours, compared with the 24-hour period required by the two first generation TOS satellites.

In addition to providing both types of television picture coverage provided by the TOS system, the ITOS system provides, for the first time, operational, day and night, infrared and visible spectra radiometric data. The ITOS system is also designed as a baseline system that will accommodate further growth and enhancement of the existing mission capabilities.

Both the local television data (APT pictures) and local radiometric data (continuous scanning radiometer picture data) from the satellite are available to local users around Earth each day during their individual contact periods, affording daytime and nighttime service to all local stations. The global television (AVCS) and radiometric coverage is available to the National Environmental Satellite Center in every 12-hour period via the system ground stations and microwave links to the processing centers. Two types of secondary data provided by the satellite for evaluating solar proton flux density and Earth heat balance are also supplied to NESC by the ITOS system.

The ITOS mission takes advantage of the capabilities of a two-stage DSV-3N-6 launch vehicle to place the ITOS spacecraft into a circular, near-polar, sun-synchronous orbit at 790 nautical miles altitude to obtain the described television picture and scanning radiometer coverage of Earth's cloud cover.

Specifically, in fulfilling its mission, the ITOS system provides the following primary data for use by meteorologists and other scientists:

- Daytime observations of cloud cover, as detected in the visible spectrum, for direct transmission to users located around the world.
- Nighttime observations of cloud cover, as detected from radiance in the infrared spectrum, for direct transmission to users located around the world.
- Daily observations of global cloud cover, in the visible spectrum, for processing at the National Environmental Satellite Center (NESC) of the Environmental Science Services Administration (ESSA).
- Daily observations of global cloud cover, as detected from radiance in the infrared spectrum, for processing at NESC of ESSA.

In addition, the system provides the following secondary data:

- Measurements of solar-proton density obtained during the orbit for processing at NESC and the ESSA Research Institute.
- Heat balance measurements obtained throughout the orbit for processing at NESC of ESSA.

The ITOS system accomplishes the aforementioned objectives of providing primary and secondary data under the control of the ITOS ground complex. The ground complex provides for command program formulation and command encoding and transmission to the satellite, as well as data readout from the satellite, and data handling, processing, and storage.

SECTION II

PROGRAM SUMMARY

In 1966, design studies were initiated by the Goddard Space Flight Center of the National Aeronautics and Space Administration, in consultation with the Environmental Science Services Administration, for a second generation meteorological satellite system, to be designated Improved TOS (ITOS). The first in the series of the new generation of spacecraft was to be designated TIROS M, a research and development flight model spacecraft. A design study for TIROS M was begun immediately by RCA, concurrent with the ongoing TOS spacecraft program; the official hardware program, which culminated in the launching and successful operation in orbit of the TIROS M spacecraft (ITOS 1 satellite), was begun by RCA on April 25, 1967.

A guiding principle of the program from its inception was the adaptation of space-proven technology and hardware from the earlier TOS meteorological satellite program as well as the use from other programs of satellite sensor devices that offered potential as advanced meteorological sensors.

The implementation of the new program by RCA was planned and carried out as an orderly development and transition from the existing first generation program. Design and installation of ground support equipment was phased into the TOS ground station equipment as compatible modifications and additions that made possible the control and programming of both types of satellites. Thus, regular TOS operations were continued in order to obtain data from the ESSA 2, ESSA 8, and ESSA 9 satellites, all of which continued to supply operational meteorological data after the launching of TIROS M.

The ITOS program had as contractual requirements the design, construction and testing of four test model spacecraft, to prove the validity of the structural and thermal design of the spacecraft (mechanical test model and thermal test model), to test system and subsystem electrical performance (electrical test model), and to test performance of the spacecraft antennas on a full-scale model (antenna test model). The testing of the spacecraft models preceded the integration and testing of the TIROS M flight model spacecraft, and the histories of this testing are included in this report. The electrical test model (ETM) spacecraft was also used at the launch site in preparation for the TIROS M launching to check performance of communication links in the presence of site RFI. It will be modified, as necessary, and used in preparation for future ITOS launches, also.

Engineering support personnel were supplied for launch site and other ground support activities during the period of the TIROS M launching as they will be for the future ITOS launchings.

Engineering documentation and supporting publications were delivered under the contract to support each phase of design, assembly, testing, and launching of the spacecraft. Publications included design study reports, periodic and final engineering reports, alignment and calibration data, programming and control instructions and data, and operating and maintenance instructions for ground support equipment, as well as special reports and analyses.

In summary, the responsibilities of RCA Corporation during this portion of the program have been as follows:

(1) Implement the ITOS system design.

(2) Perform an analysis of the anticipated radiation environment for the ITOS configuration.

(3) Perform analyses of the dynamics control requirements of the ITOS spacecraft.

(4) Construct an MTM, an ATM, and a TTM, and conduct appropriate tests to verify the integrity of the spacecraft design.

(5) Construct an ETM and a flight model (TIROS M) spacecraft. The efforts on both spacecraft included:

- Qualification of the subsystem elements, including space units.
- Installation of the qualified subsystem elements on the spacecraft structure, integration of the elements into a complete spacecraft system, and determination that the integrated spacecraft met the respective established specifications.
- Performance of environmental tests on the integrated spacecraft.
- Alignment and calibration of the spacecraft sensing elements.

(6) Upon satisfactory completion of the environmental testing and calibration of the flight-model spacecraft, deliver the spacecraft to the Western Test Range (WTR) for launching, and provide engineering support for the launch effort.

(7) Design, fabricate, and install ITOS-TOS compatible ground equipment for the CDA stations, TOC, and TEC/TCC.

(8) Perform prelaunch analyses of the launch and orbit requirements.

(9) Prepare instructions for establishing and maintaining the required satellite attitude.

(10) Prepare instructions for checkout of the satellite functions and evaluation of the performance of the satellite during the initial orbits.

(11) Prepare instructions for commanding the satellite for the performance of specific attitude-control, momentum control, and data-gathering functions.

(12) Prepare instructions for receiving and processing data from the satellite and maintaining the ground equipment in good operating condition.

(13) Provide direct engineering support to the CDA stations and to TOC and TEC/TCC during the launch and immediate post-launch periods.

The proposal and study leading to the spacecraft program were initiated under NASA contract NAS5-9034 early in 1966. A proposal for a TIROS M spacecraft was submitted to NASA on August 22, 1966 and meetings were conducted during the following weeks with the purpose of achieving further definition of the spacecraft configuration. The initial configuration included two APT television cameras, two AVCS television cameras, and two high resolution infrared radiometers (HRIR's) as primary sensors. The radiometers were later replaced by scanning radiometers (SR's). Negotiation of the proposal was begun on November 16, 1966 and completed on December 16, 1966.

During January of 1967, the design study program for the TIROS M spacecraft was completed. Contract NAS5-10306 was received for signature during the same month. A draft of the design study report was submitted to NASA for review during March.

A design review of the structure was held on March 23, with representatives of NASA attending. A meeting between RCA and Douglas Aircraft Company (now MacDonnell Douglas) representatives was held on March 17 to define the interface between the launch vehicle and the spacecraft.

A design review of the vehicle dynamics subsystem was concluded at the end of March.

On April 25, 1967, a signed ITOS contract was received from Goddard Space Flight Center for a flight prototype (TIROS M) and three flight model spacecraft (initially designated ITOS I, J and K; later redesignated ITOS A, B and C). During April, several changes were made in the original equipment complement. The original high resolution IR radiometers (HRIR's) were replaced in the system design with two-channel (IR and visible light) scanning radiometers (SR's). A hybrid vidicon (electrostatic focusing and electromagnetic deflection) was incorporated in an improved version of the AVCS camera. Improved recorders for both the AVCS and SR subsystems were included in the spacecraft equipment complement.

In July 1967, the contract was modified to include two additional spacecraft, designated ITOS D and E.

During July and August, work proceeded on the mechanical and electrical design of spacecraft components and on the fabrication and testing of breadboards of the components. Drawings for the mechanical test model (MTM) and the thermal test model (TTM) were completed. A meeting was held on August 24 between RCA, NASA, and the Douglas Aircraft Company to observe and discuss the fit of the TIROS M separation ring and the DAC attach fitting.

On September 7, 1967, NASA formally directed RCA to incorporate the new line scanning radiometer, manufactured by the Santa Barbara Research Center, in the TIROS M design, replacing the HRIR radiometers of the original design. Additionally, the APT camera scan was changed from an 800-line scan to a 600-line scan. During September, the design of the pitch control loop was modified to provide for two modes of open-loop operation. The preliminary plan and schedule for installation of the ITOS-unique ground equipment at the CDA stations were included in a presentation made to representatives of ESSA and NASA on September 26, 1967. It was requested that work at the Gilmore, Alaska station be deferred until November, in order to take advantage of the transfer of responsibility for more spacecraft contacts to the Wallops Island, Virginia, station.

During October 1967, the TIROS M Stress Analysis Report was completed and submitted to NASA. Progress continued with drafting of layout drawings, schematics, and printed wiring masters and on fabrication and testing of breadboards for spacecraft components.

All electronics assembly drawings for the AVCS camera and camera electronics were completed during November. The mechanical test model (MTM) structure was completed and prepared for environmental testing in December.

In December the MTM spacecraft vibration test cycle was performed and the initial solar panel deployment tests, post-vibration alignment and balance check, moment-of-inertia measurements, and fixed-axis despin test were performed. Assembly of the thermal test model (TTM) was completed and TTM testing was initiated, also during December.

As a result of TTM testing, additional insulation was incorporated on the equipment panels to compensate for distributed leaks, bringing spacecraft temperatures into the desired range. The N-body analytical model was revised to obtain correlation with the results of the first phase of TTM testing.

Separation and shock tests using the launch vehicle third-stage attach fitting and the MTM were conducted during February 1968. In March, the report on MTM testing was delivered to NASA. The TIROS M structure was completed on March 22, 1968, and thermal testing of the TTM was completed on March 24.

In April, the contract was modified to change the launch vehicle from a three-stage Delta 3M vehicle to a two-stage Delta N vehicle. The antenna test model (ATM) was completed and the passive phase of ATM testing was performed during April. ATM active phase tests were completed during May.

The launch sequence for the TIROS M/Delta N launch was modified on June 12 to include a second-stage roll maneuver in order to obtain the required spacecraft orbital momentum. The launch sequence material in the Programming and Control Handbook was changed accordingly. A spacecraft breakaway connector was designed for the spacecraft and the spacecraft harness design was altered to accommodate the two-stage launch vehicle. Progress on the electrical integration of the electrical test model (ETM) continued during June and July.

The final report on ATM testing was completed on July 23, 1968.

The ETM spacecraft was modified to include the changes required for compatibility with the two-stage launch vehicle. Integration of the ETM and of the TIROS M spacecraft continued during August and September of 1968.

A number of failures, which had occurred during extended prototype vibration testing of DC-to-DC converters used in various subsystems of the spacecraft, led to an investigation of transistor types used in these units. The failures occurred at vibration levels and durations that exceeded prototype requirements, and would, therefore, not be expected to occur during normal testing at specified levels, or during any flight vibration exposure. An improved mechanical assembly of the transistor was instituted by the manufacturer.

An additional requirement for two one-quarter scale models of the spacecraft was negotiated during October 1968 and the contract was modified in November to include these models.

The TIROS M/ITOS Thermal Design Report, describing testing of the thermal test model and giving flight temperature predictions, was completed in October. Dynamic suspension testing of the ETM spacecraft was performed during October. Following this testing, a SEPET was performed with satisfactory results in all areas.

During November 1968, the momentum wheel assembly design was modified to add strain gages to the brush holder springs for the purpose of monitoring motor brush wear during life testing of the assembly.

The Instruction and Operating Handbook for the Improved TIROS Operational System was submitted to NASA during December of 1968. The ETM spacecraft was balanced during December and balance weights were installed to

simulate the final mass distribution of the TIROS M spacecraft. The measurements of moment of inertia, weight, and center of gravity were then performed on the ETM spacecraft.

A two-part review, consisting of a review of the test histories of all component boxes and a system review, was conducted during January for the NASA Project Office. ETM testing continued and the ETM spacecraft was used to verify procedures for thermal-vacuum testing, launch checkout, and detailed electrical testing of the pitch control subsystem.

Excessive wear of the MWA motor brushes caused persistent difficulties and intensive study of this problem was undertaken. Development tests and thermal analysis of the MWA indicated that brush performance could be improved by changes in configuration and material and these changes were incorporated in the design.

A preliminary system checkout of the TIROS M spacecraft was performed during March, using flight model units for all components except one SR recorder, one AVCS recorder, and the pitch control subsystem; prototype units were used for the latter components. All detailed electrical testing was completed and the Standard Electrical Performance Evaluation Test was performed with satisfactory results, using the configuration described above.

In April, the TIROS M Programming and Control Handbook and the ITOS-TOS Instruction and Operating Handbook were published. These documents furnished instructions and information for use in training programs for operators and other ground support personnel, as well as providing the primary publications sources for ground support of the satellites. Also in April, a confidence test cycle was initiated for TIROS M subsystems and components. This cycle consisted of an operational test of 168 hours duration for most components and a 240-hour test for dual units. Components already installed on the spacecraft were removed for this purpose.

Following the completion of confidence testing of the TIROS M units, the units were installed on the spacecraft. Those units that had not been installed previously were subjected to detailed electrical tests followed by an abbreviated SEPET. The spacecraft was closed to the flight configuration, with all thermal blankets, the solar panels, and the antenna arrays in place. RF interference testing was performed with excellent results, and with the exception of collimation of the cameras and sensitivity testing of the scanning radiometers, all calibration procedures were completed on the AVCS and APT cameras, the scanning radiometers, the solar proton monitor, and the flat plate radiometer. The remaining calibration tests were performed during the full SEPET and thermal-vacuum testing. APT camera 2 and AVCS camera 1 were replaced on the spacecraft because of a shift in sensitivity in the case of the APT camera and an undesirable warmup characteristic of the AVCS camera. A battery capacity test was also successfully completed during May.

The dynamic suspension test was performed on the TIROS M spacecraft in June. Seven successful capture sequences were performed. In addition, a prequalification SEPET was performed during June. Spacecraft temperature predictions for the thermal-vacuum environment were computed, including definition of the limits of temperature exposure for cameras, recorders, batteries, and the momentum wheel assembly.

In July, the design review report for MWA brush wear was completed. Also a stability analysis of the pitch control loop was completed during July, showing that good performance could be expected for momentum values within the expected ranges. Spacecraft testing during July included a SEPET, an RF interference test, a solar-panel deployment test, a solar-panel electrical checkout, a spacecraft shock and separation test, prototype level vibration testing, a vacuum firing of the solar panel pin pullers, and the thermal-vacuum survey in preparation for thermal-vacuum acceptance testing.

The flight level thermal-vacuum acceptance testing was begun late in July and completed on August 26 with satisfactory results. Problems encountered with the MWA, flat plate radiometer, and SR recorder led to the replacement of all three of these units with other flight qualified units. All replacements were tested and satisfactory results were obtained. One of the APT cameras also was replaced following thermal-vacuum testing when a failure occurred during electrical testing. Vibration testing was completed with satisfactory results and the final report on vibration testing was published during August. The strain gage amplifier unit for TIROS M was completed during August.

The TIROS M Flight Readiness Review Data Package was published in September, documenting the TIROS M flight configuration and summarizing the component and spacecraft testing for the TIROS M and ETM spacecraft. A preliminary review of TIROS M flight readiness was held by RCA for NASA on September 11 and 12. Revisions to the TIROS M Programming and Control Data Handbook, updated to include the revised open-loop MWA wheel speed, were also published in September. The Alignment and Calibration Data Handbook for TIROS M was published on October 10, 1969.

A study of regulator fusing was completed in October and a report of the study was published on October 15. During October a study and tests were performed to verify that the spacecraft thermal blankets and their fastenings could withstand the ascent depressurization of the two-stage launch. Results showed that an ample safety margin existed. Flight acceptance testing of the TIROS M spacecraft was completed on October 4. Following acceptance, launch checks were performed. The battery capacity tests were repeated and an abbreviated SEPET was performed, all with satisfactory results. The spacecraft was then placed in storage to await shipment to the Western Test Range.

The spacecraft remained in storage until December 7, 1969, when it was shipped, together with the ETM spacecraft and associated checkout equipment, to the Western Test Range. The shipment left AED on December 7 and arrived at the NASA Spacecraft Laboratory assembly building at the Western Test Range on December 8. During the following 10 days, fit checks, electrical tests, and launch procedure checks of the Phase 1 launch operations were performed. A joint review of the Phase 1 SEPET results was held by RCA and NASA on December 18, and the flight model spacecraft was pronounced ready for launch.

With Phase 1 operations completed, TIROS M and the ETM spacecraft were both reinstalled in their shipping containers to await the commencement of Phase 2 operations on January 5, 1970. During the storage period, a special battery charge cycle was applied to the TIROS M spacecraft on December 22 and on January 2, 1970.

Phase 2 of the launch support operation was started on January 5, 1970. On this date, the TIROS M spacecraft was removed from its shipping container and installed in the SEPET test fixture. An abbreviated SEPET was performed on January 5 and 6. The spacecraft pyrotechnic arming connectors, for solar panel deployment, were installed on January 6. On January 7, the three solar panels were preloaded for flight, the beacon and command antenna was installed, and the access-port blanket was installed.

On January 8, "on stand" launch checks were performed on the TIROS M spacecraft at the spacecraft laboratory, and the spacecraft was transported to the launch pad and mated with the launch vehicle. Spacecraft launch checks were performed and spacecraft test support was provided during the all-systems checkout on January 9. Daily spacecraft launch checks were performed from January 12 through January 22. The TIROS M spacecraft was launched at 1131 hours GMT (0331 PST) on January 23, 1970.

SECTION III

ITOS MISSION PROFILE

The ITOS mission is divided into four phases, the last of which is the mission mode operational phase, in which the satellite performs its normal primary and secondary sensing functions. Preceding the operational phase are the launch sequence phase, the acquisition phase (under expected conditions, the first five orbits) and the spacecraft system checkout phase. These three phases are depicted in Figure 1-III-1.

The objective of the launch and acquisition events is to achieve mission mode attitude for the spacecraft. Mission mode attitude is defined as the conditions which exist when the spacecraft:

- Solar panels are deployed,
- Momentum vector is aligned to within ±1 degree of the positive orbit normal,
- Cone half-angle of nutation is less than 0.3 degree,
- Momentum wheel is spinning at a rate of 150 ±2 rpm, and
- Pitch control electronics is in closed loop mode, and the pitch attitude is within ±1 degree of Earth reference peculiar to its altitude (local vertical) if the spacecraft is at nominal altitude.

A programmed series of launch vehicle and spacecraft events occurs in the interval between liftoff and the achievement of mission mode attitude. The launch vehicle, a Delta N booster, besides providing the thrust necessary to achieve the desired orbit, orients the spacecraft into an approximate mission

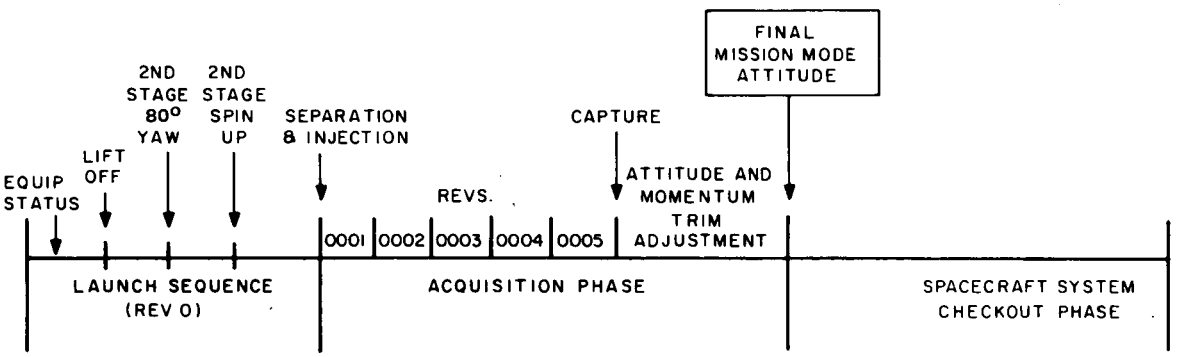

Figure 1-III-1. Launch to Mission Mode Events

mode attitude by the execution of a 80-degree yaw maneuver; it also imparts to the spacecraft the required angular momentum by means of a programmed spinup.

The objective of the programmed operations following the separation event is to establish the spacecraft in Earth-lock, with the solar panels deployed, by the time of completion of the CDA contact on revolution 0005. Certain conditions may make it necessary to use alternative commanding operations to achieve this same end. Some of these alternatives require that the lock-on attempt be delayed until a CDA contact later than that of revolution 0005. The constraints requiring alternative commanding operations are related to "moon interference" with proper operation of the pitch loop during the period of establishing lock-on and to variations from nominal performance of the second stage launch vehicle in the performance of spinup, resulting in variations from desired system momentum values. Constraints in both of the categories cited can be foreseen, and the required alternative operations predicted, prior to the time of their execution.

The sequence of events and the changes in spacecraft status that are undergone from liftoff to Earth lock-on are listed below.

- Establishment of equipment launch status,
- Liftoff,
- Delta-N pitch program,
- Burn No. 2 cutoff of second stage,
- 80-degree yaw maneuver,
- Spinup to desired roll rate,
- Separation event:
  - power applied to pitch loop motors,
  - momentum wheel accelerated to nominal rate,
  - spacecraft module decelerated to expected body rate,
  - telemetered accelerometer data removed and replaced by spacecraft roll data, and sun-angle data.

The subsequent operations on the spacecraft are initiated by ground command and are directed toward trimming the attitude, deploying the solar array panels, and achieving Earth lock via the pitch control system. Operations are based on a 3 PM ascending node orbit with the ascending node of the first revolution at approximately 35 degrees East longitude. While a satisfactory power and thermal condition exists with the spacecraft in this post separation orientation, since the three solar panels are still folded back along the sides

of the spacecraft body, a reduced amount of power is available for the spacecraft. It is, therefore, desirable to achieve the mission mode orientation as soon as possible. Revolution 0005 is the "target" revolution for these operations, because it provides for "long" contacts at both the Wallops Island and the Gilmore Creek CDA ground stations and is preceded by a satisfactory number of orbits during which the attitude trimming operations can be performed.

Following the achievement of the required mission mode attitude and Earth-lock, the spacecraft is subjected to a performance verification program, referred to as the "system checkout phase". The purpose of this program is to establish that all of the spacecraft equipment has satisfactorily survived the launch and that the spacecraft is capable and ready to perform the mission. During this phase, attention is centered on the functional performance of the equipment by checking operating parameters. Once satisfactory operation of a unit of equipment has been established, it is not exercised for further evaluation until all of the spacecraft equipment has been operated.

The mission of the spacecraft is such that simultaneous operation of the various data-gathering and control equipment is required. The end objective of the system checkout phase is to demonstrate that the basic operational combinations of the spacecraft equipment perform together in a satisfactory manner.

The first equipment to be checked is that which establishes the status of the telemetry, command, power, and stabilization equipment and permits subsequent parameter measurements. The secondary and primary data systems are next checked individually to verify satisfactory operation. Next, the equipment combinations are selected. To ensure that spacecraft operation will meet the mission requirements with the combinations of redundant equipment, several of these operational combinations are exercised in parallel during the operational mode checkout.

When spacecraft system checkout has been completed, demonstrating the operational capability of the spacecraft, mission mode operations may begin. These operations are performed on a routine basis subsequent to the attainment of mission mode attitude and pitch lock-on; they are continued throughout the operational life of the satellite.

Mission mode operations include the programming of the primary data sensors, attitude control operations, power supply monitoring, telemetry processing, secondary sensors data processing, and the exercising of redundant satellite equipment.

SECTION IV

DESIGN PHILOSOPHY AND CONSTRAINTS

The fundamental design philosophy for the ITOS program, as a continuation of the design philosophy for the TOS series of first generation operational satellites, embodied the same principles as its predecessors. These are:

- A sound system concept, with a baseline design that permits growth and accommodation for improved sensors.
- An engineering reliability and quality program to assure the adequacy of the space hardware.
- Detailed development test and prototype and flight acceptance tests at component, black box, and spacecraft levels to demonstrate the capability of meeting the expected launch and mission environment and life.
- A detailed spacecraft calibration and measurement program to enable evaluation of the satellite's performance in orbit and to provide key data to the operational centers.
- A spacecraft launch and post-launch support team to assure proper spacecraft handling, testing, and post-launch evaluation.
- The reliable Delta launch vehicle.
- A Project Team effort by government and industry personnel.

In addition to using space-proven TOS designs wherever these designs were compatible with existing program mission requirements, the ITOS spacecraft incorporates improved and new designs built around the established designs of the TOS program. This is evident in the APT and AVCS camera subsystem designs which are improved versions of the TOS television camera subsystems; in the command subsystem; in the power supply subsystem; in the beacon and telemetry subsystem; and in the communications subsystem, all of which are adaptations of the proven TOS designs, modified to meet the requirements of the ITOS spacecraft. The ITOS stabilization scheme is a further extension of the existing spin stabilization technology developed and proven on the earlier TIROS and ESSA satellites, providing a large, Earth-oriented platform for the sensors to view Earth's atmosphere.

The primary purpose of the program is to develop a second generation of meteorological satellites which will routinely provide operational data that can be readily translated and processed with Earth-bound conventional data for use by scientists, research organizations, and weather forecasters in this country and in nations abroad. In observing Earth's cloud cover by means

of two slow-scan TV camera systems aboard the Earth-orbiting satellite, the main design objective of the program is two-fold: (1) to upgrade the operational meteorological data in both quantity and quality and (2) to continue a baseline that can accommodate further growth and enhancement of the overall system.

The design techniques employed on previous TIROS/TOS programs afforded the means for translating sophisticated system concepts into the design and development of reliable, long-life, and flexible spacecraft components. In order to assure long operating life, subsystem redundancy is used throughout the spacecraft. As on the TOS programs, this feature ensures that spacecraft subsystem performance will be maintained, preventing any single malfunction from causing the loss of a spacecraft function. In addition, this design permits cross-coupling of units so that elements from one redundant chain can be brought on line with other selected elements of the second redundant chain. This feature enables the spacecraft to fulfill the mission objective using the optimum signal and data paths through the system.

The design for long life is further assured by the application of design techniques that facilitate spacecraft testing, calibration, and handling, which ensure that both design and workmanship are fully adequate for achieving mission success. The test program permits the screening of any early life failures and provides a record of spacecraft calibration which is utilized as a baseline to evaluate performance in orbit. The test program starts at the component level and continues through all levels of assembly including board level, box level, subsystem level, and finally, spacecraft level. For each "black box" component, a series of tests is performed to validate the breadboard design, the mechanical design, the prototype unit performance, and finally, the flight unit performance. At the spacecraft level, validating tests are performed on a mechanical test model, a thermal test model, an antenna test model, an electrical test model, and finally, the flight spacecraft.

The spacecraft is designed in a box-like structure that can be readily disassembled or assembled for various phases of the test program tasks. The large flat equipment panels permit flexibility in configuring and mounting new mission equipment, and the side walls can be easily raised to "button up" the spacecraft for final tests. The two side panels are configured to carry the primary television sensors, their associated electronics, and data storage recorders. The baseplate houses the equipment for the bus functions, such as power, telemetry, communications, command, and control. The "bus" concept looks forward to growth and alternate mission application with minimum redesign.

TOS-type QOMAC* coils are used to correct roll and yaw errors. MBC** coils are used to correct for the residual magnetic dipole and to provide a

* Quarter orbit magnetic attitude control
**Magnetic bias control

one-degree-per-day precession rate required to track the orbit regression of a sun-synchronous orbit. A magnetic spin-control coil provides for the adjustment of momentum about the pitch axis, and liquid dampers are used to reduce satellite nutation.

The combination of satellite magnetic attitude control of the body, and momentum control and stabilization, provides a very reliable, low power, long-life attitude and momentum control system. With no consumable products to be dissipated, the satellite can be kept under three-axis control for extremely long-term operation. This performance matches or exceeds that of systems which require greater power and utilize life-limiting stored-gas control jets.

In component design, all circuits and boxes were analyzed for potential failure modes. Fuse protection of key circuits for each chain was included in the design to assure isolation of a unit or subsystem in the event of a high current drain or a short, thus permitting safe operation of the balance of the system.

Although there is some loss of power due to radiation damage or degradation of solar cells, the array was sized with sufficient reserve to provide ample end-of-life power for the mission. The rechargeable nickel-cadmium batteries are operated with a shallow depth of discharge of 5 to 15 percent to assure long life.

During the spacecraft system and subsystem and black box design, design reviews were held. The first review was at the conceptual level; the second was a major design review at the time of design release; and the third, a follow-up review after the prototype tests were completed. The designers were required to utilize components listed in RCA's established spacecraft standards. These standards reflect data available from NASA and other government agencies. All nonstandard parts were given special tests to be certified as acceptable for space use.

A parts application program was established at the beginning of the design and was one of the items studied during the design review. Particular emphasis was placed on the derating of components and the actual application of each component in the circuit. Components were radiation tested to assure an understanding of radiation effects. Each circuit designer reviewed his design for beginning- and end-of-life conditions, taking into account the possible radiation degradation effects and temperature variations.

SECTION V

THE TIROS M SPACECRAFT

A. SYSTEM DESIGN

The TIROS M spacecraft (ITOS 1 satellite) acquires Earth cloud-cover data for meteorological analysis in both the visible and the infrared spectra, and transmits data to stations on Earth. Local data is transmitted in real time to individual APT ground stations, located around Earth, and stored global data (total Earth coverage) is transmitted to the Command and Data Acquisition (CDA) stations of the ITOS ground network. The destination of the global data is the National Environmental Satellite Center (NESC) of the Environmental Science Services Administration (ESSA), where satellite meteorological data is processed and analysed for use in weather predictions and in meteorological studies. The satellite is required to produce total Earth coverage in both the visible and the infrared spectra on a daily basis. Secondary data, consisting of Earth heat-balance data and solar proton and electron flux data in the orbit environment, is also provided by the satellite to the CDA stations on a daily basis.

The satellite performs its primary and secondary missions through the functioning of eight electrical subsystems, as follows:

- Primary sensor subsystems
  - AVCS television subsystem
  - APT television subsystem
  - Scanning radiometer (SR) subsystem
- Secondary sensors subsystem (including solar proton monitor and flat plate radiometer sensors)
- Command and control subsystem
- Communications subsystem
- Vehicle dynamics subsystem
- Power supply subsystem

In addition to the electrical subsystems, the spacecraft structure and the active and passive thermal control of the spacecraft are described in detail in Part 2 of this report.

Redundancy, at both the component and the subsystem levels, is used extensively in the spacecraft design to ensure a high level of performance of spacecraft

functions and to avoid the loss of any function as the result of single unit failure. Cross-coupling of components within a subsystem permits the selection of optimum signal-handling paths and may be used to circumvent multiple unit failures.

B. SUBSYSTEM DESCRIPTION

1. General

The functions of the ITOS satellite are divided into the command, vehicle dynamics, primary sensor, secondary sensor, communications, and power subsystems. The communications equipment includes telemetry components as well as all transmitters, antennas, and associated circuits.

2. Command Reception and Processing

The dual command receiver and the enable tone detectors of the dual decoder are powered continuously. The command receivers amplify and detect the received signals. The outputs of the receivers are applied to their respective associated decoders. Decoder selection is implemented by transmission of the appropriate "enable" tone from the ground station. Detection of the correct enable tone energizes the remainder of the selected decoder. Receipt and detection of the correct command sequence applies power to the circuitry of the selected decoder, permitting subsequent command reception and decoding. As the commands are received, verification data is retransmitted to the CDA station via the beacon transmitter to confirm correct reception.

Outputs of the decoder are used to select a programmer and a time base unit. The dual programmer provides the signals for all remote sequencing of spacecraft subsystems such as the cameras, radiometers, recorders, and attitude correction. The dual time base unit provides all the timing signals and frequencies required to operate the satellite subsystems. The programmer can be considered as providing the major timing events such as a picture sequence; the time base unit can be considered as providing detailed timing components such as time bases, synchronizing signals, and subcarrier frequencies.

The detected command signals are routed to a command distribution unit (CDU) where they are converted to the appropriate action. In addition to inputs from the decoder, the CDU also receives inputs from the programmers.

3. Dynamics Control

The dynamics subsystem enables the satellite to align the vehicle axes into the proper attitude for viewing the surface of Earth. Motion about the pitch

axis is controlled by a flywheel and torque motor, utilizing error signals from the selected pitch horizon sensor and shaft encoder. Redundant pitch sensors are provided. The magnetic bias control (MBC) coil is used to control the spin axis component of the satellite residual dipole by providing torque to precess the spin axis at the orbital regression rate of 1 degree per day. The quarter-orbit magnetic attitude control (QOMAC) coil provides controlled precession of the spin axis through quarter-orbit polarity reversal of its spin axis dipole moment to adjust spin axis orientation and to compensate for solar induced torques. Spin axis nutation is reduced by liquid dampers. Sensors provide attitude information. Attitude information will be obtained from a digital solar aspect sensor (DSAS) during initial orientation.

4. Primary Sensors

a. REAL-TIME DATA

The APT subsystem is redundant, either of the two cameras being selectable by ground command. Each camera consists of two assemblies, a camera housing which includes the lens, vidicon, and video preamplifiers, and a camera electronics unit which houses the scanning, amplitude modulator, and associated circuitry. Each camera provides two outputs for implementation of cross-strapping of the redundant systems, one output going to real-time transmitter 1 and the other to real-time transmitter 2. Each transmitter receives inputs from either APT camera, or either scanning radiometer via the SR processor. Cross-strapping and isolation are accomplished by resistance coupling, with unit selection being made by power programming. Thus, the selection of a camera or a radiometer and a transmitter is all that is required, and no switching of inputs is necessary.

The camera electronics output is an amplitude-modulated subcarrier, which frequency-modulates the real-time transmitter. The APT subsystem operates only during the subpoint daytime. Pictures are taken once every 260 seconds, with readout of one frame taking 158 seconds. This direct transmission is received by local APT ground stations (APTGS) around the world. The long frame time permits the signal to be transmitted on a narrow-band system. This simplifies the equipment used in the APTGS.

The nighttime signals for direct transmission are provided by the scanning radiometer. This subsystem is also redundant. The radiometer consists of a scanning unit and an electronics package. It has two data channels, one which responds to energy in the infrared region of the spectrum (10.5 to 12.5 microns) and the other to energy in the visible region of the spectrum (0.52 to 0.73 microns). One of the two outputs is selected in the dual SR processor by ground command; the selected signal amplitude-modulates a 2.4-kHz subcarrier in the

IR processor. This signal is one of the inputs to the real-time transmitter. The normal mode of operation is for scanning radiometer operation at night in the IR region of the spectrum. This visible channel can be used in the daytime with SR data interleaved between APT readouts.

One of the two scanning radiometers and one-half of the dual SR processor make up one-half of the redundant real-time SR subsystem.

b. STORED DATA

The stored data includes both SR and AVCS data. The IR and visible outputs from each SR are connected to the associated half of the dual SR processor. When the SR data is to be recorded, radiometer telemetry, calibration, and time code signals are commutated into the portions of the radiometer signals that do not include Earth scan data. The outputs of each half of the dual SR processor are cross-strapped to the redundant SR recorders so that either of the radiometer signals may be recorded on either recorder. Thus, the selection of the combination of radiometer (with associated processor) and recorder is accomplished by powering the selected units. No external switching is required. A second input to the recorders is a constant tone (for flutter-and-wow modulation), which is used during ground data processing to correct for tape recorder speed variations.

The AVCS cameras and tape recorders are also redundant. The AVCS camera has a camera housing and an electronics unit. The camera is programmed to provide daytime data coverage from terminator to terminator, with pictures taken at 260-second intervals. The camera outputs are cross-strapped to the AVCS tape recorders to permit the use of either camera with either tape recorder. A constant tone input is recorded. This tone, modulated by flutter-and-wow, is used during ground processing to correct for tape recorder speed variations.

5. Secondary Sensors

The secondary data subsystem consists of the flat plate radiometer, solar proton monitor, data format converter, and incremental tape recorder. The flat plate radiometer (FPR) contains four sensors to provide data for terrestrial heat-balance measurements. The control of the radiometer and the formatting of the digital data output for recording are performed in the data format converter.

The solar proton monitor (SPM) consists of an array of solid-state detectors and an electronics unit to encode the data in digital form. The subsystem detects solar protons in several energy ranges. An electron detector is included to

monitor the electron fluxes to provide an indicator of the boundary of the "polar cap" region within which solar proton fluxes can be accurately recorded. The control of the monitor and timing is accomplished in the data format converter. In addition to recorded data, SPM data can be transmitted in real time over the beacon and telemetry link.

The analog-to-digital converter accepts selected satellite analog telemetry and telemetry from the secondary data subsystem and converts it to digital data to provide telemetry throughtout the orbit.

The data format converter (DFC) is the interface and control unit for the SPM, FPR, incremental tape recorder, and analog-to-digital converter. Timing signals from the dual time base unit are routed through the DFC to the appropriate subsystems. The data readouts of the SPM, FPR, and analog-to-digital converter are synchronized by the DFC. The SPM data is recorded on one track of the recorder. The FPR data is combined with the digital telemetry data and time code and recorded on a second track of the recorder. The third track of the recorder contains synchronizing or clock pulses for the synchronization and timing of the data during ground processing. The recorder is played back on ground command, and the three outputs frequency-modulate three VCO's. The three VCO signals are combined in the DFC and sent to the dual multiplexer for eventual transmission over the S-band link.

6. Communications

a. S-BAND LINK

The dual multiplexer contains redundant multiplexers which can accept simultaneous inputs from one or two SR recorders (two SR data signals and two SR flutter-and-wow signals), an AVCS recorder (one AVCS data signal and one AVCS flutter-and-wow signal), and the combined output of the DFC. The signals are translated to appropriate channels and combined. The outputs of the redundant multiplexers are connected to the redundant S-band (1.7 GHz) transmitters. Selection of the redundant subsystem is made by powering the selected unit rather than by external signal switching. The outputs of the redundant transmitters are coupled to the S-band antenna.

b. REAL-TIME LINK

The real-time transmitter handles the SR real-time data as well as the APT data. The transmitter frequency for TIROS M is nominally 137.5 MHz. One of the redundant transmitters is selected by ground command. Two dipoles are configured to provide a linear polarized directive pattern in a 110-degree cone centered on the local vertical.

c. BEACON AND COMMAND LINK

The command RF carrier, in the 148-MHz band, is received on the beacon and command antenna, which accepts signals over a "look" angle of 4π steradians. The command signal is coupled to the receiver from the antenna via a TEE, a series of filters and a hybrid coupling network which splits the received power into both receivers. A coaxial switch controls the signal flow from the selected beacon transmitter through filters to the TEE and antenna.

Telemetry data is transmitted to the CDA ground stations by the beacon transmitter. The telemetry units consist of a signal conditioner and redundant telemetry commutators. The signal conditioner accepts all satellite telemetry points and conditions the signal levels and impedance levels as required. The telemetry signals are then connected to the redundant 120-channel commutators. Commutator selection is by ground command; it is possible to step the commutator manually on command to any 1 of the 120 points for continuous monitoring of any telemetry signal. Telemetry point No. 6 accepts the output of the digital telemetry from the DFC so that digital telemetry can be monitored in real time. The commutator output is also supplied as one input to the DFC analog-to-digital converter so that a selected telemetry point can be monitored throughout the orbit by recording the data on the incremental recorder.

The commutator outputs are routed through the CDU where the selected commutator signal is switched to the SCO/beacon transmitter pair which was also selected by ground command. Beacon transmitter 1 and set 1 of the dual SCO are associated permanently as a unit as are beacon transmitter 2 and set 2 of the dual SCO. The two SCO frequencies are IRIG channel 9 and IRIG channel 7 (modified). These channels are used to transmit telemetry, real-time SPM data, attitude data, command verification, accelerometer data (during launch) and digital solar aspect sensor signals.

7. Power Supply

The power supply subsystem comprises a solar array, power supply electronics, batteries, and external shunt dissipators. The solar array consists of three panels. Each panel has five circuits with nine parallel strings of 76 2 x 2 cm solar cells. A total of 10,260 cells comprise the complete solar array. The cells are wired in series-parallel combinations to provide component redundancy. The array output is supporting an average spacecraft load of 3 amperes, exclusive of power subsystem requirements. The electronics unit has a control amplifier which, in conjunction with the shunt dissipator, dissipates the array power in excess of the satellite requirements. A tapered charge controller regulates the charge rate of the batteries as a function of battery discharge condition and temperature. The series regulator provides the regulated -24.5-volt power, which most of the satellite subsystems use. The pitch control motors,

shutter drives, and the dual decoder/dual command receiver operate from the unregulated output of the power subsystem. The batteries are used to supply power during the "night" portion of the orbit and when satellite demands exceed the power available from the solar array during the daytime.

8. Subsystem Redundancy

a. OPERATING GOALS

The ITOS satellite has been designed to satisfy the requirements of the operational system. It will be in use full-time, providing complete data capability from AVCS, APT, SR, and secondary sensors every orbit. The minimum design mission lifetime of the satellite is 6 months with a one-year goal. To meet this requirement, design factors have been incorporated to allow for degradation of both solar array output and transistor characteristics due to aging and radiation bombardment. Premature termination of the mission because of subsystem failures has been minimized by the use of cross-strapped redundant units. Generally, redundant units have been included for those subsystems which are primary to the mission. Where it has not been feasible to provide a redundant unit in a primary subsystem, as in the command distribution unit, the unit has self-contained redundant circuits or functions.

As a further aid to improved reliability, the redundant units are generally cross-strapped by resistive coupling. Thus, it is not necessary to provide signal switching; the selection and powering of the desired redundant units automatically produce the desired subsystem combinations.

b. ALTERNATE MODES OF SYSTEM OPERATION

Since the scanning radiometers have daylight as well as nighttime capability, they can be used as a substitute for either APT or AVCS coverage, or both, with reduced ground resolution (4.1 nautical miles for SR versus 2 nautical miles for APT and AVCS) and some loss of data when successive ground station contacts are missed.

SECTION VI

ITOS GROUND COMPLEX

A. GENERAL

The ITOS system operations are monitored and controlled by a ground complex comprising three major groups of facilities:

- Command, programming, and analysis centers,
- Command and data acquisition (CDA) stations, and
- Spacecraft checkout facilities.

In addition to the above, the ITOS system utilizes the facilities of the NASA Space Tracking and Data Acquisition Network (STADAN). Automatic picture transmission (APT) field stations throughout the world also participate in the program as APT and SR (scanning radiometer) data users.

B. COMMAND, PROGRAMMING, AND ANALYSIS CENTERS

The command, programming, and analysis centers comprise three facilities; the name, location, and primary functions of each are given below:

(1) TOS Evaluation Center and TOS Checkout Center (TEC/TCC), Goddard Space Flight Center (GSFC), Greenbelt, Maryland. TEC/TCC functions as the control point for all operations concerned with the prelaunch checkout and launch operations of new or replacement spacecraft, and operates as the control center for orbital operations of the spacecraft during the checkout operations performed following the launch.

(2) TOS Operations Center (TOC), National Environmental Satellite Center (NESC), Suitland, Maryland. TOC is the central control point for the ITOS system and is responsible for overall system operations. It receives requests for weather data from NESC and formulates programs of commands for the satellite instrumentation, which are teletyped to the CDA stations and transmitted from the CDA stations to the satellite. TOC monitors all significant CDA events and provides instructions pertaining to courses of action CDA personnel should take. The facility receives, in real time, all attitude and other engineering data telemetered from the satellite to the CDA station via the beacon

link, evaluates this data, and, where applicable, formulates corrective command programs for transmission to the satellite(s).

(3) Data Processing and Analysis Facility (DAPAF), NESC, Suitland, Maryland. DAPAF is the installation that processes satellite meteorological data for presentation to the utilizing agencies. Video data, SR, and secondary sensor information received at the CDA station are transmitted to DAPAF where computer equipment is used to locate, format, and digitize the input data, and produce scale-rectified maps and other summaries of meteorological data. Photographs of the AVCS pictures, complete with longitude and latitude gridding, are produced on AVCS video processing equipment located at this facility. DAPAF also processes telemetered data in support of TEC/TCC and TOC. (Real-time SR and APT pictures are also processed by the APT ground stations.)

C. COMMAND AND DATA ACQUISITION (CDA) STATIONS

The CDA stations are located at Gilmore Creek, Alaska, and Wallops Island, Virginia. The CDA stations and the command, programming, and analysis centers are interconnected by a microwave communications system, which has characteristics suited to the transmission of the required data. (A backup ground station is located at the RCA Space Center in Princeton, New Jersey.)

Each of the two CDA stations functions primarily as a relay station between TOC and the satellites. The CDA stations receive the command programs teletyped to them by TOC, and, when the satellite comes within communications range on the orbit specified in the program, transmit the commands in the form of FSK audio-frequency tones modulating an RF command carrier frequency. In all operations, the stations receive and record on magnetic tape the video and telemetered data transmitted by the satellite, relaying the telemetered data in real time (as it is received at the station) to TOC for evaluation. The recorded data is played back after the satellite pass and transmitted to DAPAF over the communications network for processing by that facility.

D. SPACECRAFT CHECKOUT FACILITIES

The spacecraft checkout facilities include two complete sets of ground equipment that permit the functioning of the spacecraft to be fully checked out, as well as test equipment required during fabrication and assembly of the spacecraft.

One of these sets of ground equipment is the factory set located at RCA Astro-Electronics Division, Princeton, New Jersey, while the other set is installed

in a transportable air-conditioned van, for use at the factory or at the launch site as required for checkout of the spacecraft before launch.

In addition to providing most of the facilities included in the CDA station, each checkout facility includes equipment for RF signal handling (converting transmitted signals from the spacecraft into the frequency bands and to the proper interface signal levels and transmitting command data to the spacecraft); for simulating the operation of the DAF station for display of APT video and for both direct and recorded SR information; and for processing and displaying secondary sensor data.

E. SCOPE OF GROUND EQUIPMENT COVERAGE

Much of the ground equipment that is used for the ITOS system was installed as part of the TOS ground complex. A brief description of the ITOS ground complex equipment is presented in Part 5 report. Further information concerning that equipment is presented in the Instruction and Operating Handbook for the ITOS and TOS ground equipment, Volumes 1 through 5, prepared for the Environmental Science Services Administration under NASA contracts No. NAS5-10306 and No. NAS5-9034, dated April 3, 1969, revised December 3, 1969.

SECTION VII

SYSTEM PERFORMANCE

A. GENERAL

The performance criteria for the ITOS system are predicated on how well the system meets specified program mission requirements as defined by:

- Launch conditions, including spinup rate and orbit injection angle;
- Mission life and attitude; and
- Data coverage, including primary sensor (APT, AVCS, and SR) data and secondary sensor (solar proton monitor and flat plate radiometer) data in the respective visible and infrared portions of the radiation spectrum.

A series of launch vehicle and spacecraft operations occurs in the interval between liftoff and the acquisition of mission mode attitude. The launch vehicle, a Delta N booster, besides providing the thrust necessary to achieve the desired orbit, places the spacecraft into an approximate mission mode attitude by the execution of an 80-degree yaw maneuver; it also imparts to the spacecraft the required angular momentum by means of a programmed spinup. Once injected into the nominal orbit and oriented to the mission mode, the object of all subsequent operations is to establish the spacecraft in Earth-lock for providing primary and secondary subsystem data to the ground system. The operations described in this section are only a summary of events and operation sequences that occur atuomatically as well as those resulting from ground-commanded sequences for global, daylight, cloud-cover data and nighttime, infrared radiance data.

B. LAUNCH AND ORBIT INJECTION CONDITIONS

Launching of the ITOS spacecraft takes place from the Western Test Range (WTR). The launch vehicle, a Delta N booster, places the spacecraft into a sun-synchronous circular orbit with a nominal altitude of 790 nautical miles. A successful launch and orbit injection is dependent on the following sequence of events and conditions:

- Equipment launch status (established by ground command);
- Liftoff;

- Delta-N pitch program;
- Burn No. 2 cutoff of second stage;
- 80-degree yaw maneuver - momentum vector pointing error, ϕmax, after second stage yaw maneuver is no more than 10 degrees;
- Cone half angle of nutation, θ, is no more than 13 degrees after separation;
- Spinup to desired rate - spacecraft spin rate following separation is within the limits required for the initiation of the capture sequence.

NOTE

The exact values for the nominal spin rate and the limits on this parameter depend on actual inertia values of the spacecraft. The appropriate values for wheel speed and body rotation rate to be used in the calculations are supplied with the Flight Timetable. The inertia measurements are included in the Alignment and Calibration Data Book.

- Separation event:

  power applied to pitch loop motors,

  momentum wheel accelerated to 115 ±5 rpm,

  spacecraft module decelerated to expected body rate,

  accelerometer data on 2.3-kHz SCO removed (roll data telemetered from roll sensor 1), and

  accelerometer data on 3.9-kHz SCO removed (DSAS data telemetered).

- The time of injection into orbit and the accuracy of the sun-synchronous orbit are such that the orbit angle, the angle between a normal to the orbit plane and the Earth-sun line, is not greater than 60 degrees or less than 30 degrees.

In addition to matching orbit inclination angle to altitude in order to achieve sun synchronism, it is necessary to select the proper launch time to obtain the desired orbit o'clock angle. The launch time for a particular orbit fixed to the mean sun will always fall at the same hour regardless of calendar date. However,

the date of launch will determine where in the cyclic variation of sun angle the spacecraft is at the beginning of mission mode. For the sun synchronous orbit under discussion, an early July launch would result in a mission mode sun angle of 57 degrees, whereas an early November launch would result in an initial sun angle of 39 degrees.

C. MISSION LIFE AND ATTITUDE

1. Mission Life

The specified spacecraft mission life in orbit is at least 6 months, with a design goal of one year.

To achieve the desired mission life, subsystems and circuits successfully used on TOS are used as designed, and the primary sensor complements are essentially identical to those used on Nimbus and TOS. In components or circuits in which there are changes, the designs provide for a one-year design goal, except in the case of the solar array because of size and weight constraints.

To help achieve this goal, the spacecraft structure is designed to provide the subsystems with adequate protection from the environmental conditions at nominal altitude; namely, vacuum, solar radiation, ultra-violet deterioration, disassociated gases, X-rays, ionization, solid particles, magnetic field, electrons, protons, cosmic rays, and temperature. The spacecraft degradation design computations are based upon the projected 1965 data (based on the 1962 model) of the radiation environment for the TOS orbit with a 50-percent increase in solar proton population for the 1969-70 solar flare prediction.

As a function of design operation for achieving mission life, the following are basic performance requirements of the ITOS spacecraft:

- The spacecraft is designed to operate within the gamma angle range of 30 to 60 degrees at a nominal altitude of 790 nautical miles. It is desirable that the spacecraft provide performance as near satisfactory as possible with gamma angles between 15 and 75 degrees.
- The spacecraft is capable of operating at between 600 and 900 nautical miles; however, its performance capabilities may be less than at the nominal altitude.
- Nominal orbit radiation levels are as estimated for 1965.

2. Mission Attitude

At mission attitude, the spacecraft provides adequate power, a suitable environment, and proper orientation of the sensor subsystems so that, upon command from the ground, the sensor subsystems can provide data on Earth's environment.

In mission attitude the spacecraft is a three-axis stabilized body, and the sensor subsystems provide global storage of data and direct readout of the data. In the mission attitude, the sensor viewing surface is perpendicular to the local vertical throughout the orbit. The spacecraft attitude control system is designed to keep attitude errors in roll and yaw at less than $\pm$ 1.0 degree for the nominal orbit design altitude.

The pitch error at mission attitude varies as a function of the spacecraft altitude at a rate of approximately 1 degee for each 50-nautical-mile altitude error. The spacecraft attitude control system maintains the pitch error within limits when at mission altitude and at nominal momentum. Roll and yaw corrections of spacecraft attitude are controlled by ground command. Provision is also made for maintaining nominal angular momentum about the spacecraft pitch axis by ground command.

D. DATA COVERAGE

1. System Operation

The spacecraft sensor subsystems provide cloud-cover data in the visible and temperature data in the infrared portions of the radiation spectrum. Data is provided for direct readout to existing automatic picture transmission (APT) ground stations as well as stored on the spacecraft for playback and transmission to the command and data acquisition (CDA) stations for final processing at the National Environmental Satellite Center (NESC) of the Environmental Science Services Administration (ESSA).

To meet the data coverage requirements, the spacecraft carries redundant APT, advanced vidicon camera subsystem (AVCS), and scanning radiometer (SR) subsystems as the primary data sensors and a solar proton monitor (SPM) device and flat plate radiometer (FPR) as secondary data sensors. In the case of the primary sensors, the data storage requirements are achieved by means of redundant AVCS and SR tape recorders. An incremental tape recorder is used for storing secondary sensor data.

2. Visible Spectrum

a. PICTURE COVERAGE

Once injected into the nominal orbit and oriented to the mission mode, the spacecraft system provides global, daylight, visible cloud-cover data (APT camera data) every 24 hours. The spacecraft is capable of transmitting APT data while the subsatellite point is in the daylight portion of each orbit and of collecting and storing AVCS data during this period on each orbit up to a maximum of three orbits. Adjacent APT TV pictures taken in any one orbit have a minimum overlap of 20 percent; adjacent AVCS pictures along the orbit track have a minimum overlap of 50 percent. Pictures adjacent to those of the previous orbit overlap so that, as a minimum, they are contiguous at the equator. On each orbit, the spacecraft provides coverage of the illuminated area on both sides of the satellite subtrack by means of an 11-picture sequence from each of the camera subsystems (APT and AVCS).

b. PICTURE SEQUENCE

When the spacecraft is in mission attitude and photo coverage is desired, the spacecraft is capable of being commanded from the ground to initiate a sequence of 11 APT pictures, 11 AVCS pictures, or 11 APT pictures and 11 AVCS pictures and to repeat the sequence on each orbit. In addition, upon ground command, the spacecraft is capable of transmitting selected pictures from the APT sequence of 1 to 11 pictures.

Each camera exposure in an APT or an AVCS sequence occurs 260 seconds after the previous exposure in the sequence. The APT and AVCS prepare, expose, and readout cycles are synchronized so that the first AVCS cycle starts at T_0. An APT warmup cycle precedes T_0 by approximately 6.5 seconds, and a readout of the warmup is transmitted. The first useful transmitted APT cycle starts at the conclusion of the first AVCS cycle. The APT and AVCS cameras do not read out simultaneously. The timing is the same whether both APT and AVCS cameras or only one of the cameras has been selected.

In response to a ground command, the spacecraft programmer is capable of delaying the start of the picture sequence (T_0) in increments of 6.5 seconds from 182 seconds to 13,312 seconds (approximately 3 minutes to 3 hours and 40 minutes).

The picture sequence repeats each orbit until commanded to stop or until a new program is commanded. The orbit repeat time is programmable by ground command in increments of 6.5 seconds from 4166.5 seconds to 10,816 seconds (approximately 1 hour and 10 minutes to 3 hours). The orbit period is approximately 114.5 minutes.

2

3. Scanning Radiometer Subsystem

a. DATA COVERAGE

The scanning radiometer subsystem provides global, nighttime, infrared radiance data every 24 hours. The subsystem has both a visible and an infrared channel, and is capable of transmitting real-time data throughout the orbit. However, the subsystem normally transmits real-time infrared data while the subsatellite point is in the nighttime portion of each orbit. At no time does the spacecraft transmit the real-time scanning radiometer data and the APT data simultaneously.

The scanning radiometer subsystem is also capable of collecting and storing (on magnetic tape) radiance data throughout the orbit. All coverage is provided by a line scan radiometer, with scan essentially normal to the orbit plane.

The total storage capacity is approximately 290 minutes of data, when both scanning radiometer recorders are used in a single remote sequence. During one orbit, the subsystem is capable of storing all the data obtained during the orbit.

b. DATA SEQUENCE

Normally, the scanning radiometer subsystem is operated during the nighttime portion of the orbit. The period of operation depends upon the orbit period and the storage capacity of the recorders. Normally, the radiometers are off while the subsatellite point is in the illuminated portion of the orbit. In a backup mode, the subsystem is capable of transmitting data continuously and of storing data until the storage limit is reached.

The infrared subsystem is capable of collecting and storing data simultaneously with operation of the AVCS camera subsystem. Playback of stored scanning radiometer data on the primary data link does not inhibit transmission of scanning radiometer data on the direct data link.

4. Data Time Codes

The spacecraft system provides a 24-bit time-code reference associated with all data stored on spacecraft data recorders and a means of resetting the time-code reference to zero by ground command.

5. Data Acquisition

Data is retrieved by the ground system within the constraints of the orbital contact times for the design altitude. The data storage and transmission system is implemented so that: (a) three orbits of stored AVCS picture and time-code data on one AVCS recorder can be retrieved by the ground system in one ground contact that is above the minimum CDA antenna elevation angle for 6 minutes, (b) orbits with 128 minutes or 64 minutes of stored scanning radiometer and time-code data on one scanning radiometer recorder can be retrieved by the ground system in one ground contact that is above the minimum CDA antenna elevation angle for 10 minutes, and (c) the 300 minutes of the stored secondary sensor data can be retrieved by the ground system in one ground contact that is above the minimum CDA antenna elevation angle for at least 5 minutes.

The redundant storage capacity of 290 minutes of scanning radiometer data requires the minimum CDA antenna elevation angle to be exceeded for complete retrieval of the data by the ground system in one ground contact.

The data storage and transmission system is implemented so that simultaneous or sequential transmission of the AVCS, scanning radiometer, or secondary sensor data is possible.

SECTION VIII

ORBIT CHARACTERISTICS

A. THE ITOS ORBIT

The ITOS spacecraft is launched from the Western Test Range (WTR), Vandenberg AFB, California, by a two-stage Delta N launch vehicle. The nominal orbit is sun synchronous,* with an altitude of 790 nautical miles and an inclination of 101.7 degrees. Mission mode orientation of the spacecraft as well as its injection into orbit is accomplished by the launch vehicle. The final attitude of the spacecraft, in which the pitch axis is aligned with the positive orbit normal, is attained after injection by a programmed yaw maneuver of the second-stage launch vehicle. (See Figure 1-VIII-1 for details of the spacecraft orientation during mission mode.) To provide for the least delay in relaying daylight pictures to the National Environmental Satellite Center (NESC), launch time is chosen to put the ascending crossing** at 1500 hours local mean time (LMT). This permits picture playback during ground contacts immediately following picture recording.

The initial orbit, which begins with the powered flight at launch and ends at the first ascending node, is designated revolution 0000. Successive orbits thereafter start at the ascending node and are numbered serially, revolution 0001, 0002, 0003, etc. A day in the lifetime of the spacecraft is denoted by a Julian Day count, Julian Day 000 being launch day. Julian Day 001 begins at the following midnight, Greenwich Mean Time (GMT). Other orbital particulars are given in Table 1-VIII-1.

The sun-synchronous orbit provides the least annual variation in spacecraft sun angle for mission mode operation. (The term "sun angle" is used here to designate the angle between the pitch axis and the direction to the sun.) In such an orbit the annual fluctuations in picture illumination, spacecraft temperature, solar energy conversion, and duration of eclipse time are kept to a minimum. The orbit o'clock angle, which, among other things, determines the level of picture illumination encountered, is

*In a sun-synchronous orbit, the orbital plane precesses about Earth's polar axis in the same direction and at the same rate as Earth's average annual revolution about the sun.

**The point at which the orbit track intersects the equatorial plane, while traveling from south to north, is shown in Figure 1-VIII-2.

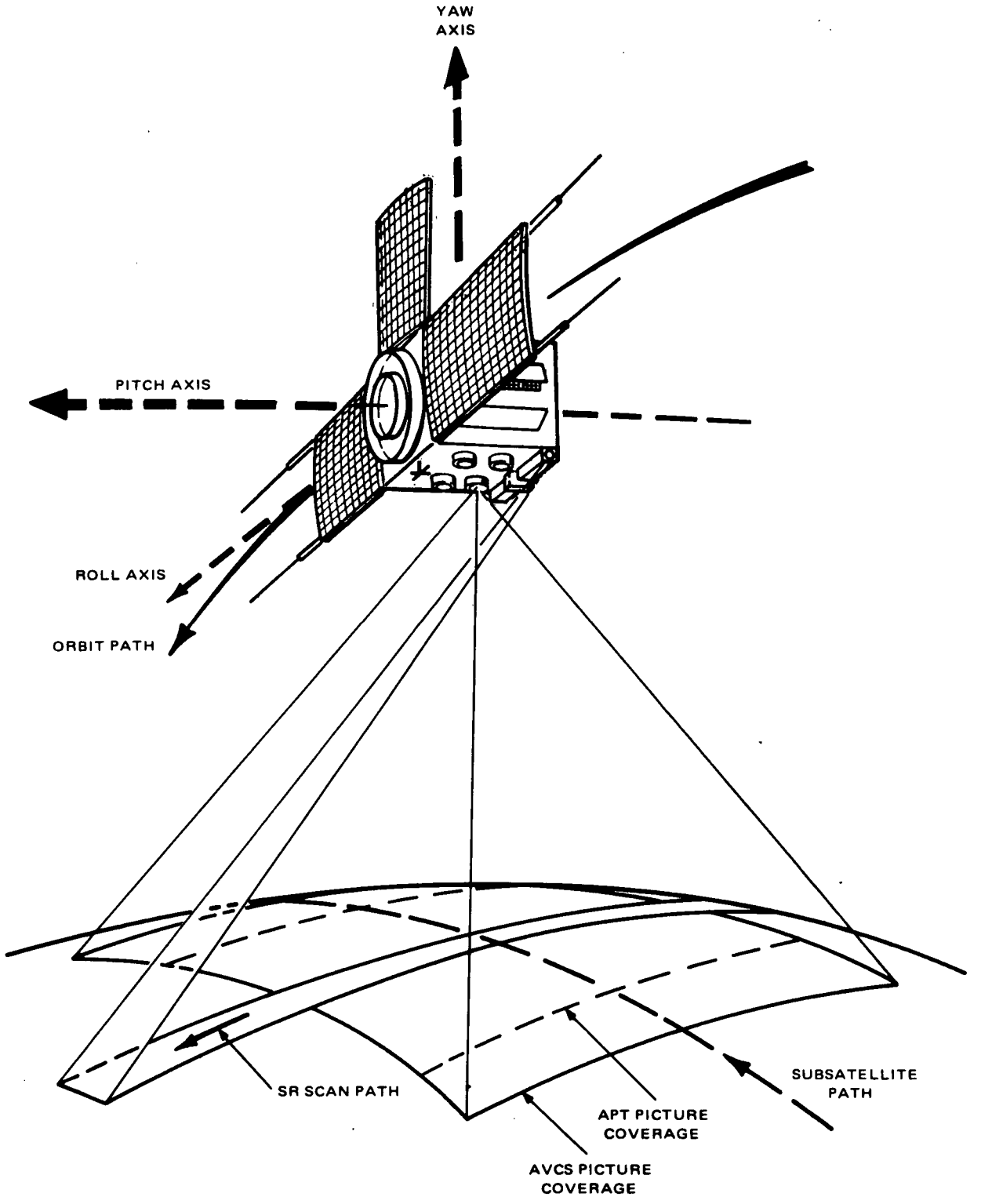

Figure 1-VIII-1. ITOS Mission Mode, Showing Primary Sensor Coverage

TABLE 1-VIII-1. PARTICULARS OF THE ITOS NOMINAL ORBIT

Parameter	Design Value
Altitude	790 nautical miles (circular)
Inclination	101.7 degrees
Nodal period	115.2 minutes
Nodal regression	28.8 degrees in longitude/orbit
Time of ascending node	1500 LMT (approx)
Orbital precession rate	0.9857 degree per day (eastward)
Orbits per day	12.5
Injection coordinates	Latitude 0.71 degrees S (nominal)
(Geographic)	Longitude 36.1 degrees E (nominal)

usually referenced as the "mean sun",* because of the variability in the apparent motion of the true sun; see Figure 1-VIII-2 for geometric particulars. In essence, the o'clock angle of the orbit gives the local mean time of the nodal crossing of reference. For example, a 1500 ascending node (AN) orbit (or what is commonly referred to as a 3 PM ascending node orbit) is a sun-synchronous orbit for which the time of the ascending node crossing is 3PM, LMT. The orbit o'clock angle may also be defined as the difference in right ascensions of the ascending node and sun.

The orbital precession is caused by the oblateness of the earth. The bulge of the earth's equator will cause the orbit plane to rotate at a fixed rate with respect to inertial space. For a circular orbit, the precession rate depends on altitude and inclination. The line of nodes moves westward if the orbit inclination angle is less than 90 degrees and eastward if it is more than 90 degrees, regardless of the altitude.

*To afford a uniform reference, a fictitious sun was invented, referred to as the "mean sun", which moves eastward around the celestial equator at a perfectly uniform rate, completing its circuit in one year. The apparent motion of the true sun about the equator is not precisely uniform.

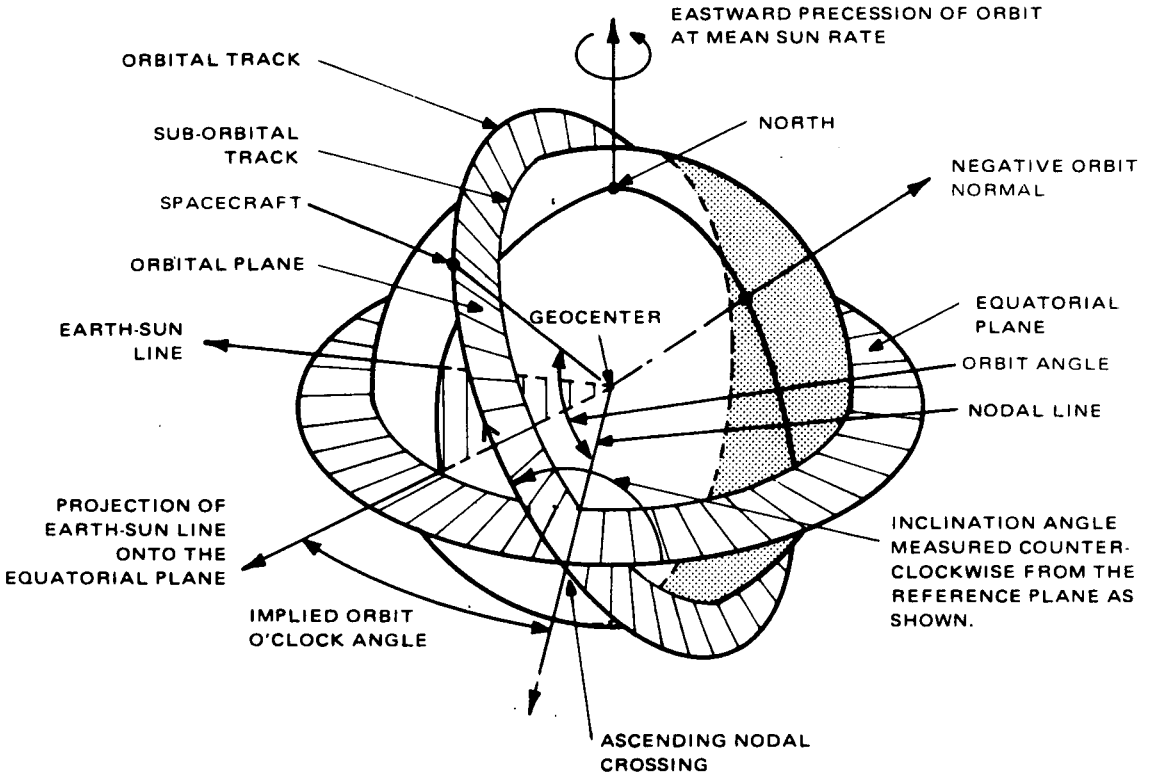

Figure 1-VIII-2. Geometry of the Sun-Synchronous Orbit

For a given altitude, the desired rate of orbital precession is obtained by the proper choice of orbital inclination angle. For the nominal altitude of 790 nautical miles of the ITOS spacecraft, an orbit inclination angle of 101.7 degrees is required for sun synchronism. For these conditions, the orbit plane rotates in an easterly direction at a rate of 360/365.24 or 0.9857 degree per day, which is the value required to maintain a constant angle between the orbit plane and the direction to the mean sun (i.e., to offset the average angular motion of the earth in orbiting the sun). In geographic coordinates, this corresponds to a westward drift in longitude at about 0.25 degree per minute, which causes successive ascending nodal crossings to occur some 28.8 degrees further westward.

B. OPERATIONAL EFFECTS OF ORBIT CHARACTERISTICS

As has been indicated, the sun-synchronous orbit has the property of maintaining a nearly constant orientation with the Earth-sun direction, thereby preventing large fluctuations in the solar-radiation-dependent phenomena, such as picture illumination and solar array power. However, even with an orbit strictly synchronous to the mean sun, orbital and seasonal variations in these properties occur that influence the operation of the spacecraft.

1. Ground Illumination

The illumination level of the picture area is subject to both orbital and seasonal variation as can be seen from the pictorial representation of Figure 1-VIII-3 and the graphical plot of Figure 1-VIII-4. As the spacecraft orbits the earth, the illumination angle at the subsatellite point cyclicly changes from negative values, for which the earth below the spacecraft is in darkness, to a positive peak value of more than 50 degrees. It is only when this angle has a value of about 14 degrees or greater that the illumination level is adequate for nephanalysis. Moreover, it can be seen from Figure 1-VIII-4 that there is a seasonal shift in the illumination level, which is caused by the eccentricity and inclination of Earth's orbit. In essence, this brings about a latitude shift of the terminator, which calls for an occasional resetting of the programmed picture-start time to maintain the proper illumination level. In practice, advance information of illumination for a given latitude is obtainable from the spacecraft Ephemeris* under the heading of sun angle.

Other factors, such as orbit o'clock angle** and launch errors, influence picture illumination. The number of adequately illuminated pictures also depends upon sun angle. The picture-taking capability for sun angles varying from 15 to 90 degrees, including the range of expected mission mode conditions, is given in Table 1-VIII-2. Two standards of illumination, corresponding to a 14- and a 10-degree solar-elevation angle, were used in compiling the results. Both of these illumination standards were applied to two different regions of the pictures. In one case, the region of interest was the center of the picture and in the other the midpoint of the most dimly illuminated side of the picture. The former tends to yield optimistic results and the latter, pessimistic. It can be seen that below a sun angle of 30 degrees, the picture-taking capability, judged by the 14-degree criterion, decreases rapidly with decreasing sun angle. With sun angles larger than 60 degrees, on the other hand, the number of pictures exceeds the picture-taking capability of 11 frames per sequence set for the programmer.

2. Spacecraft Sun Angle and Eclipse Time

Unlike picture-illumination angle, which exhibits an orbital as well as a seasonal variation, the sun angle of the spacecraft shows only a seasonal variation. This is indicated in Figure 1-VIII-5, which also shows the effect of orbit

*The (spacecraft) Ephemeris is released by NESC after the spacecraft becomes operational; it contains spacecraft subpoint and related data.

**O'clock angle is the angle measured from the mean sun to the ascending note (eastward positive). The angle is expressed in time units (degree/15 degrees hr-1 plus 12 hours) and is the local mean sun time at the ascending node.

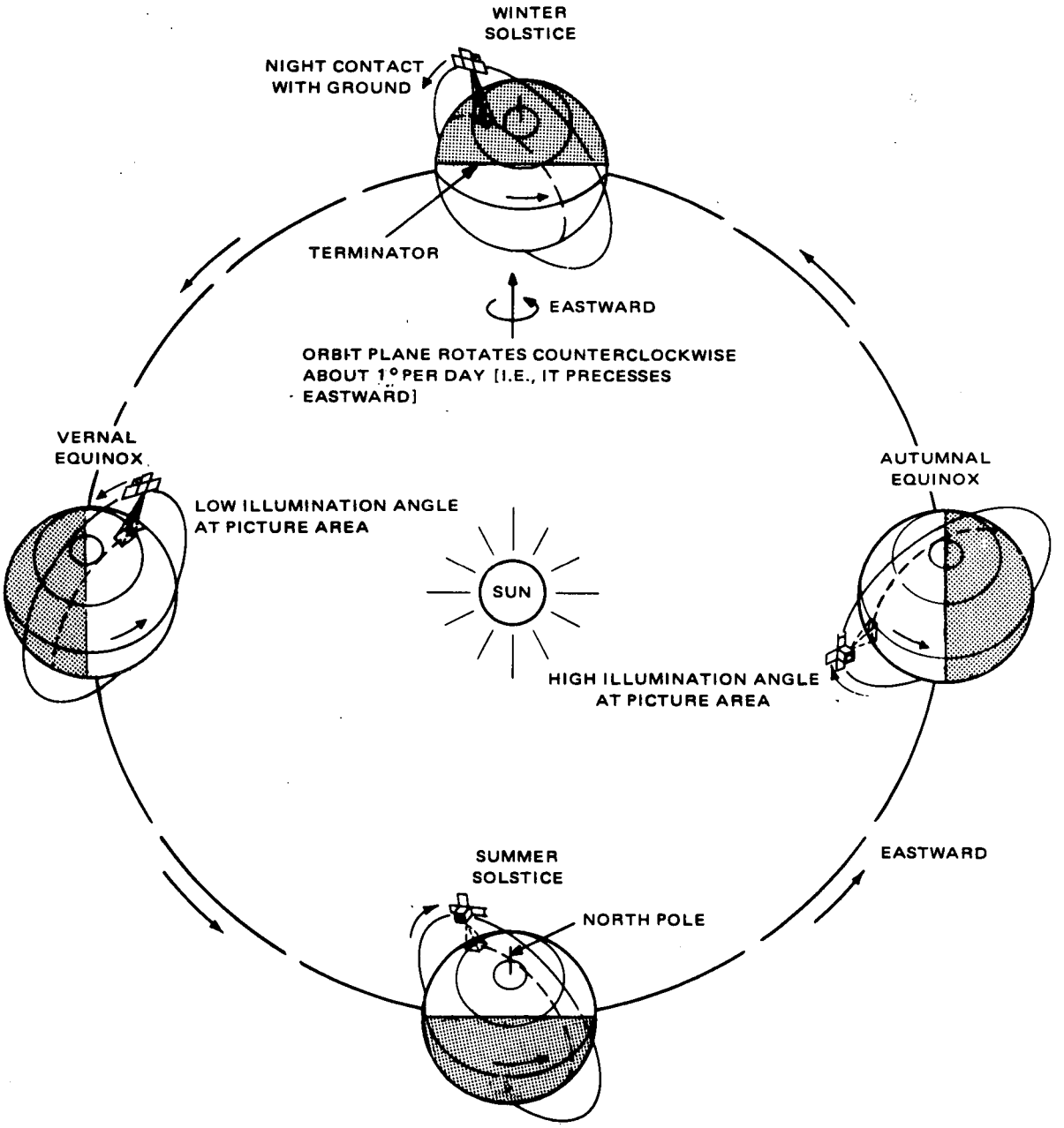

Figure 1-VIII-3. Seasonal Variations in Illumination for an Afternoon Sun-Synchronous Orbit

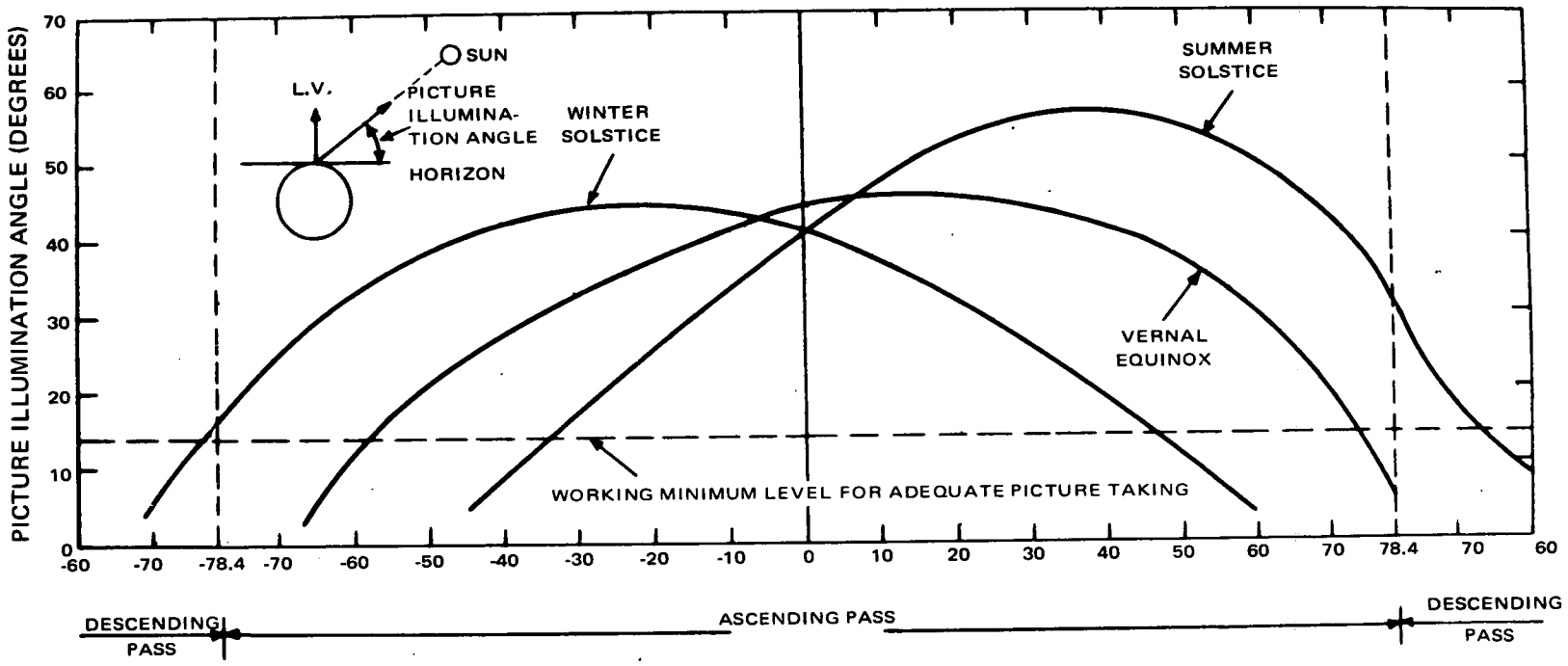

Figure 1-VIII-4. Picture Illumination Angle vs Geographic Latitude; 1500 Hour AN Orbit, 1968 Sun Data

TABLE 1-VIII-2. EFFECT OF SUN ANGLE ON PICTURE-TAKING CAPABILITY

Spacecraft Sun Angle (Mission Mode) (Degrees)	Pictures per Sequence with 14-Degree Sun Elevation*		Pictures per Sequence with 10-Degree Sun Elevation*	
	Picture Center Criterion	Picture Edge Criterion	Picture Center Criterion	Picture Edge Criterion
15	4	3	8	7
20	7	7	9	9
25	9	8	10	10
30**	10	9	11	10
60**	11	11	12	11
75	12	11	14	13
90	12	11	14	13

*Calculated results that were not whole numbers have been rounded off to the next smaller integer.

**Limits on expected mission mode sun angles.

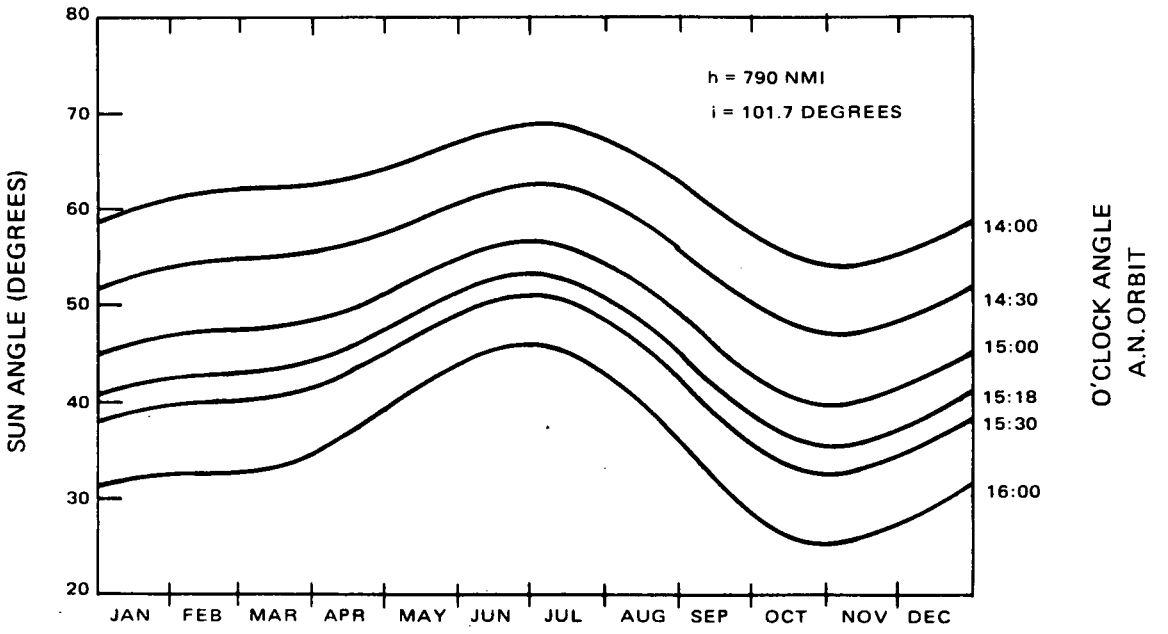

Figure 1-VIII-5. Seasonal Variation of Spacecraft Sun Angle for Afternoon AN Orbits

o'clock angle. It can be seen that, for afternoon AN orbits, the earlier the local mean time of the ascending node, the higher the sun angle for a given date.

The percent of time the spacecraft spends in the sun on each orbit also varies with calendar date orbit o'clock angle. Figure 1-VIII-6 shows that for those orbits in which the ascending node occurs earlier than 1522 LMT, the spacecraft will not experience 100-percent sun time at any time during the course of a year. The mission mode constraint on sun angle (30 to 60 degrees) and the date selected for launch set the time of launch and the duration of the launch window.

3. Ground Station Contact Time

The approximate contact times of the Alaska and Wallops Island CDA stations with the satellite are shown in Figures 1-VIII-7 and 1-VIII-8. Figure 1-VIII-7 shows the contact in minutes after the ascending node as a function of the longitude of the ascending node. The contact starts and ends 5 degrees above the horizon at the Wallops Island station and 5 degrees above the terrain at the Alaska station. The position of the terminator for the winter and summer extremes is also indicated. Figure 1-VIII-8 is a plot of net contact time as a function of the longitude of the ascending node.

Minimum ground station contact time of 10 minutes has been established as the total time required to perform satellite acquisition, playback-command transmission, and SR-data playback (9 minutes is required for data playback and 1 minute for the remaining functions).

For ascending-node longitudes in the range from 170 degrees West to 140 degrees East, neither the Wallops Island nor the Alaska station will be in contact with the satellite for the specified minimum time. Thus, the ITOS orbit, with 28.7 degrees between successive ascending nodes, could have two successive orbits with marginal ground station contact. Normally, one orbit with ground station contact less than the assumed minimum will occur every 12 to 13 orbits. When this "missed orbit" condition exists, data playback will be performed during the next orbit when adequate ground station contact time is available.

C. EFFECT OF DATE AND TIME OF LAUNCH

In addition to matching orbit inclination angle to altitude in order to achieve sun synchronism, it is necessary to select the proper launch time to obtain the desired orbit o'clock angle. The launch time for a particular orbit fixed to the mean sun will always fall at the same hour, regardless of calendar date. However, the date of launch will determine where in the cyclic variation

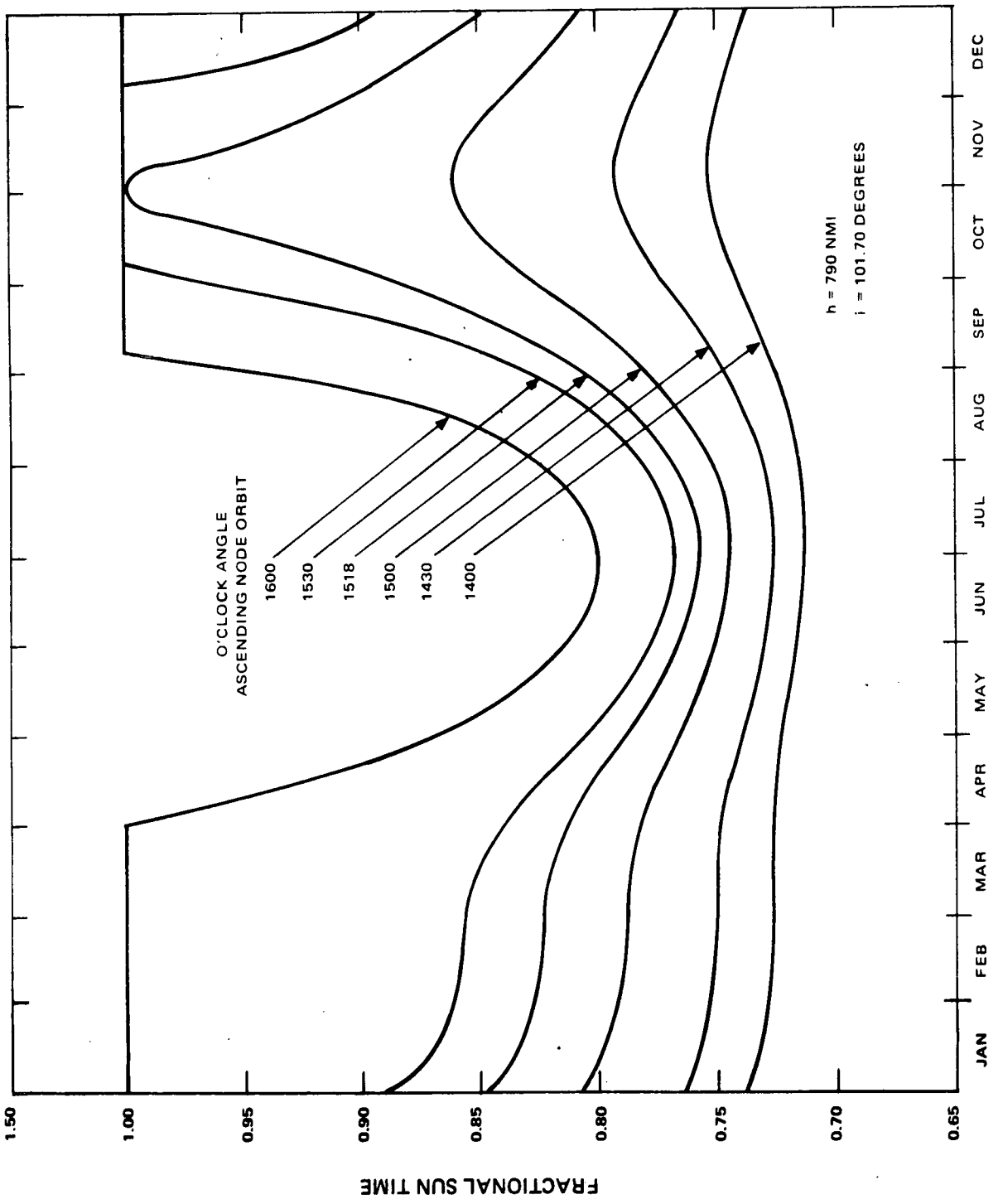

Figure 1-VIII-6. Satellite Time in Sunlight

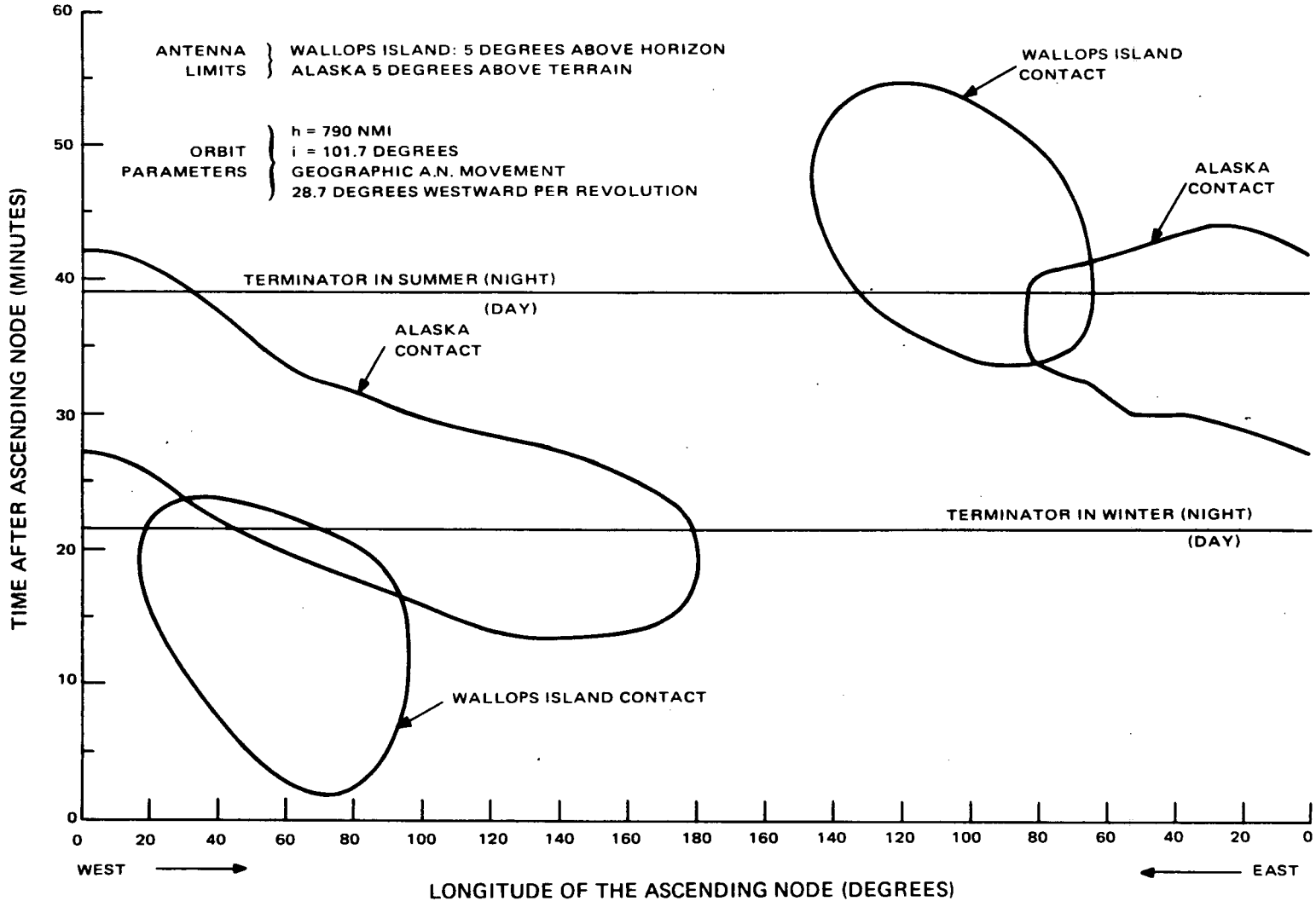

Figure 1-VIII-7. Typical Ground-Contact Boundaries for Wallops Island and Alaska CDA Stations

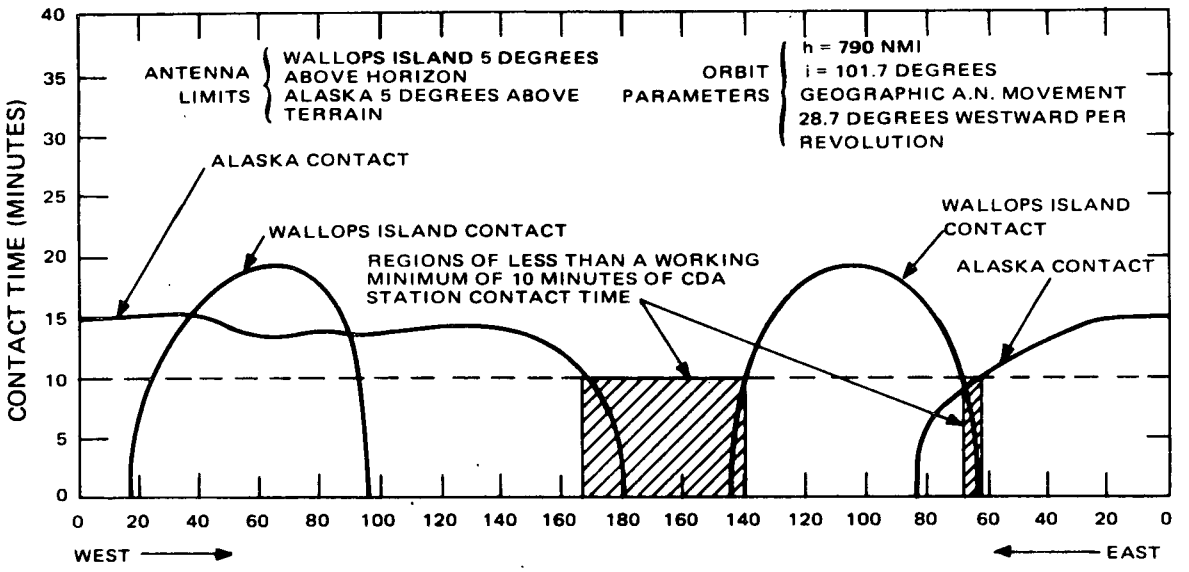

Figure 1-VIII-8. Typical CDA Station Contact Time

of sun angle the spacecraft will find itself at the beginning of mission mode. For the sun synchronous orbit under discussion, an early July launch will result in a mission mode sun angle of 57 degrees, whereas for an early November launch the sun angle will be only 39 degrees at the outset (see Figure 1-VIII-5).

The Greenwich Mean Time of the launch (GMT_L) is given by the expression:

$$GMT_L = LMT_N - \left[L_I \pm \mathrm{Sin}^{-1}\left(\tan \rho / \tan i\right)\right] /15 - t_{PF}/60^*$$

where

LMT_N is the local mean time of the node nearest to the final injection point (designated in hours from 0 to 24),

L_I is the geographic longitude of the injection point in degrees (eastward positive),

ρ is the latitude of injection (north positive),

i is orbit inclination angle in degrees, and

t_F is time of flight from liftoff to final injection in minutes.

*Within the brackets, use: + for descending nodes; - for ascending nodes.

D. EFFECTS OF INJECTION ERRORS

In general, there are two types of injection errors that affect mission operation. These are errors in orbital inclination angle and in spacecraft altitude, each of which affects sun synchronism. The individual effects may be separately evaluated and algebraically combined to determine the overall departure from synchronous condition.

The effects on the nodal drift rate of variations in inclination angle and in altitude are shown in Figures 1-VIII-9 and 1-VIII-10, respectively. The drift rates given are departures from the synchronous rate for the stated nominal values. Also listed are the 1σ values of the expected errors.

A number of different quantities change with injection errors. Orbital period, which is important in setting picture-repeat sequences and in unipolar torquing to correct for solar pressure torque, depends upon spacecraft altitude. The value of the orbital period can be obtained either from the Orbital Elements* or from nodal crossings printed in the (spacecraft) Ephemeris. An altitude error will also give rise to a pitch-axis angular offset as shown in Figure 1-VIII-11. This offset, which is given in terms of geographical degrees between picture center and subsatellite point, is also influenced by departures of the earth radiance level** and system temperature from nominal values. The combined effect of the two for the operating region defined by the tolerance extremes is shown in Figure 1-VIII-11.

Altitude and inclination angle, by controlling nodal drift, combine to affect sun angle history. Figure 1-VIII-12 shows the effect on sun angle history over a calendar year of an asynchronous nodal drift rate of 0.02 degree per day. Also shown is the effect of a 20-minute launch window, which has been centered about the launch time of a 1500 AN orbit. It can be seen that an extended launch window and an asynchronous nodal drift may combine to cause the sun angle to diverge beyond the mission extremes of 30 and 60 degrees.

E. SENSORS AND SENSOR COVERAGE

1. Primary Sensor Subsystems

The three primary environmental sensor subsystems and the principal equipment in each follow.

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*Computed at the NASA Computing Center from minitrack observations and issued periodically by the Goddard Space Flight Center.

**Heat energy radiated at temperatures between 200° and 280°K.

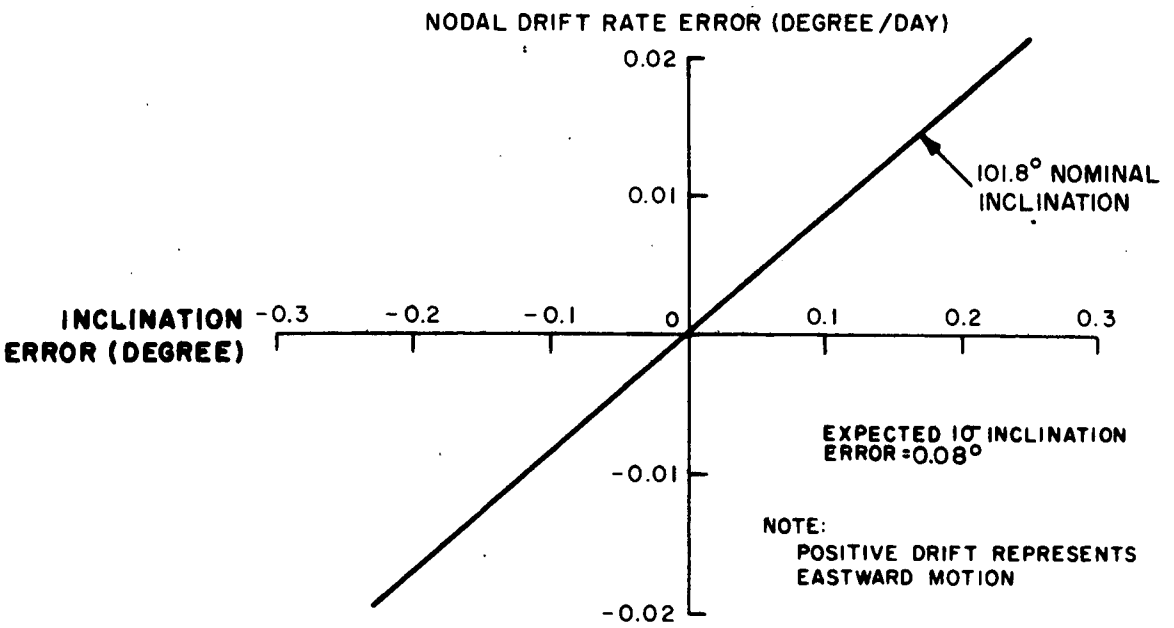


Figure 1-VIII-9. Nodal Drift Rate Error vs Inclination Error

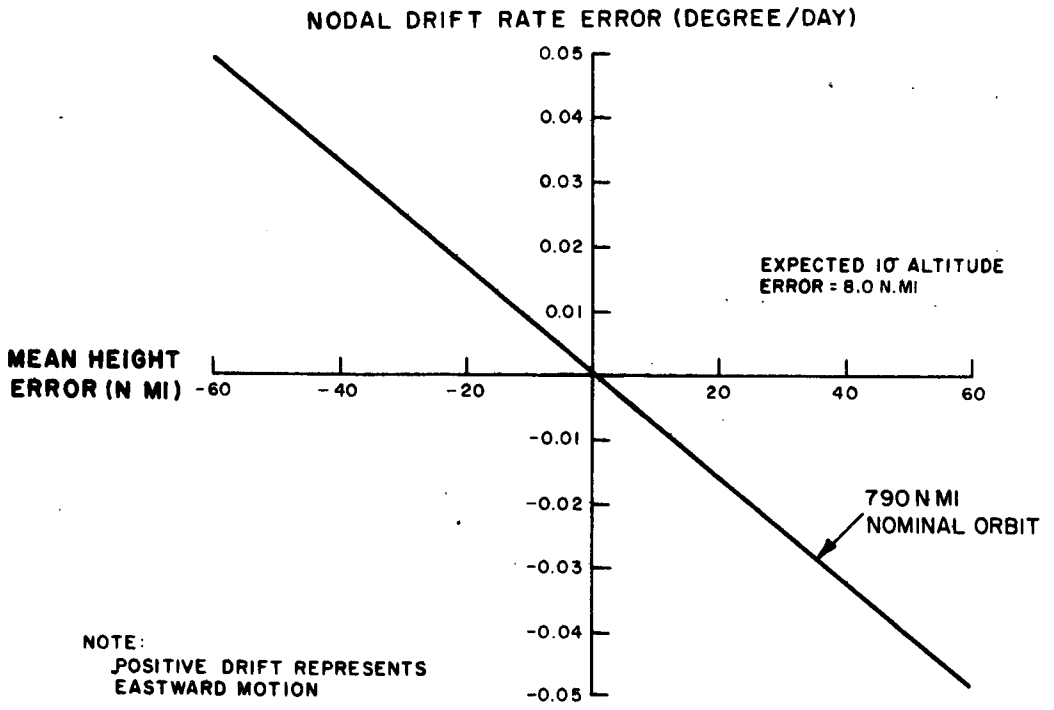


Figure 1-VIII-10. Nodal Drift Rate Error vs Mean Height Error

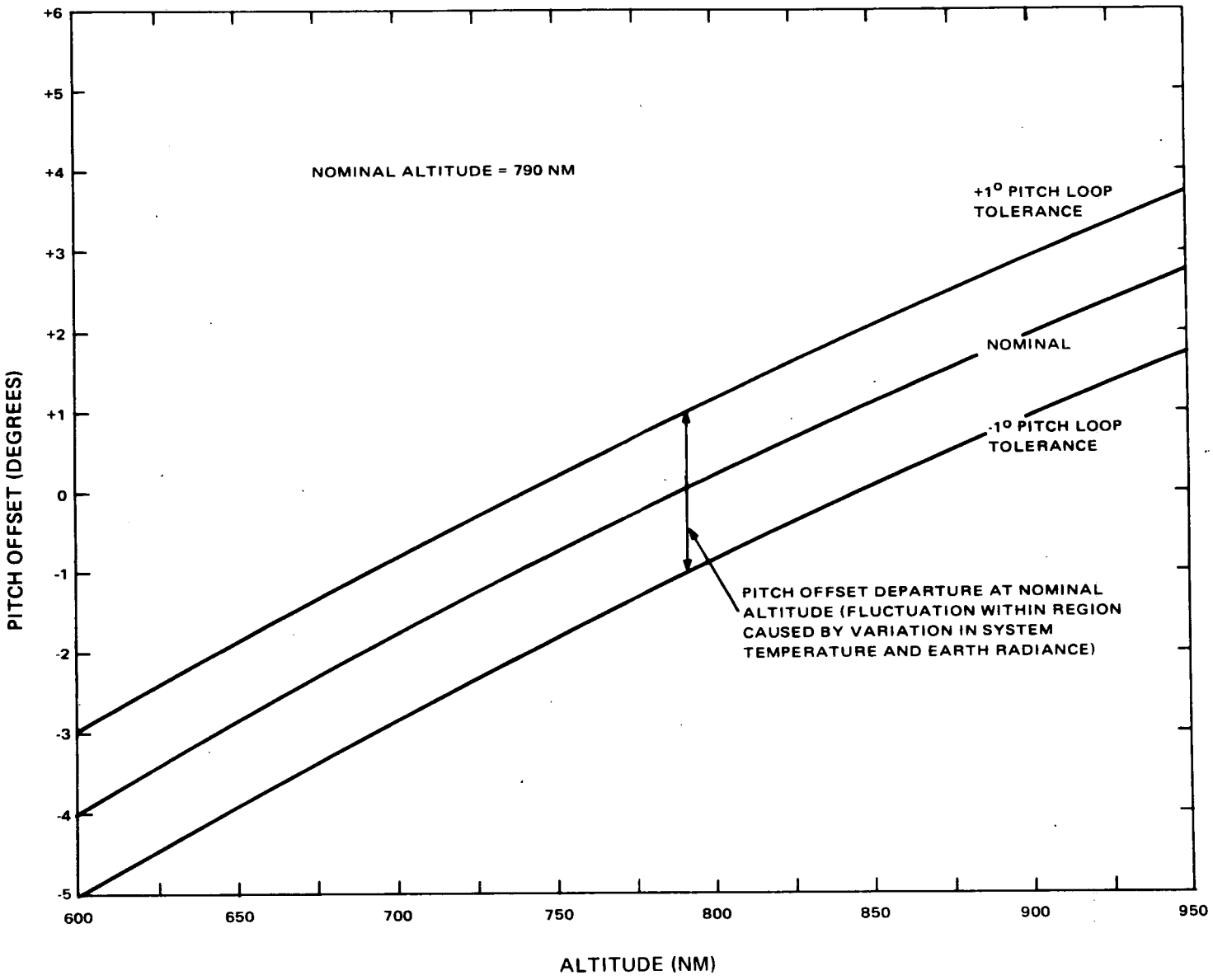


Figure 1-VIII-11. Spacecraft Pitch Attitude Offset vs Altitude

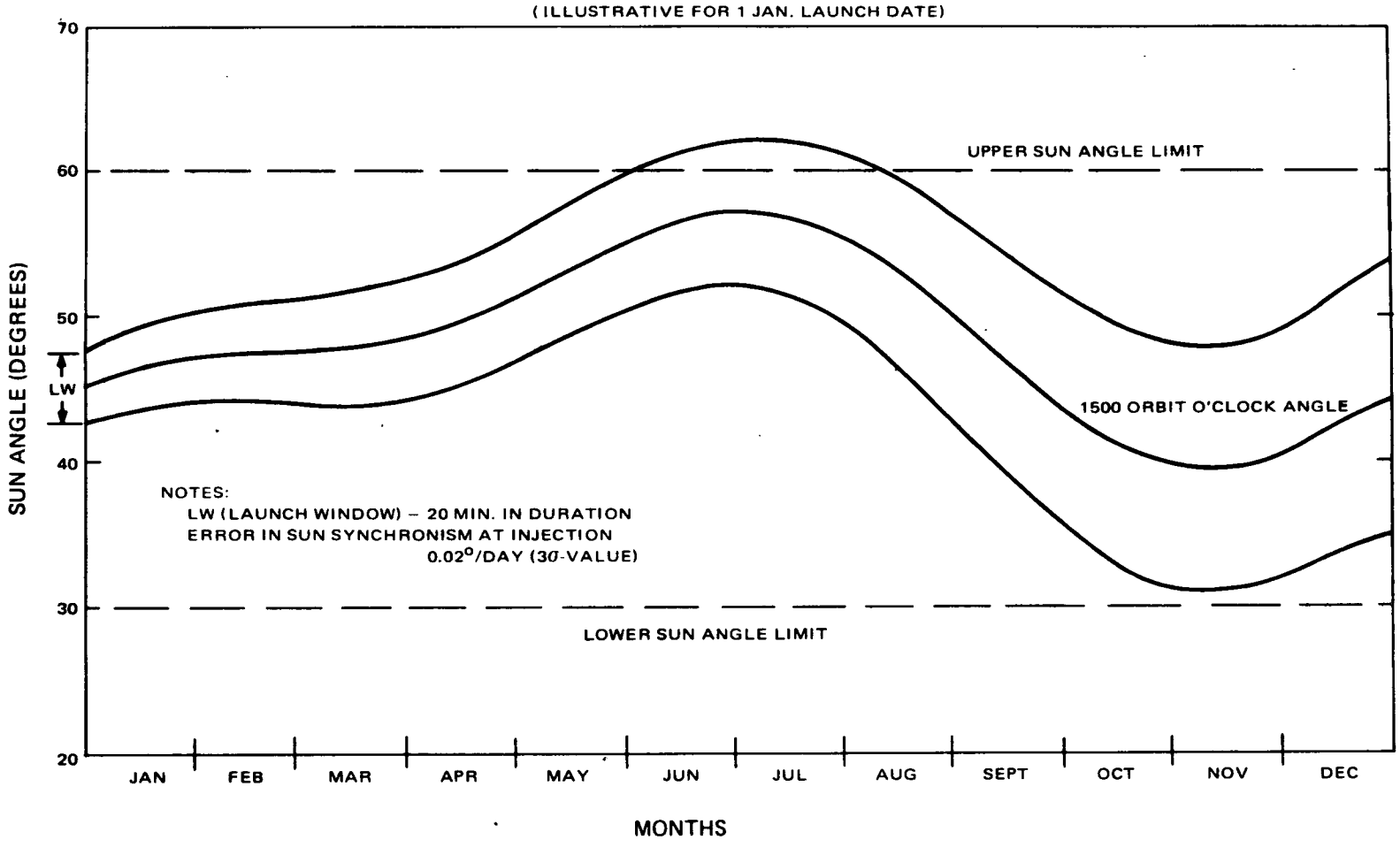


Figure 1-VIII-12. Effect of Launch Window and Injection Error on Mission Mode Sun Angle (Worst Case)

- Two advanced vidicon camera subsystems (AVCS), each having a camera sensor, an electronics unit, and a three-channel magnetic tape recorder.
- Two automatic picture transmission (APT) subystems, each having a camera sensor and an electronics unit.
- Two scanning radiometer (SR) subsystems, each composed of a scanning radiometer and control electronics, a processor, and a three-channel tape recorder.

Power- and signal-switching circuits, which are controlled by ground command, enable the selection of either AVCS camera in conjunction with either of the two tape recorders for operation. The same flexibility is provided for the selection of radiometer and tape-recorder combination for SR operation.

To fulfill primary mission requirements, one AVCS camera and one AVCS tape recorder will be used to obtain and record cloud-cover pictures from the daylight portion of the orbit. Concurrently, one of the two APT subsystems will provide daytime cloud-cover pictures for real-time transmission to local users. In general, during the nighttime portion of the orbit, one scanning radiometer (SR and one SR recorder) will be selected to measure and record data in both the visible* and infrared regions; in addition, there will be transmission in real time of the infrared data to provide cloud-cover pictures to APT stations. Daytime options for the operation of SR may also be used.

The AVCS cameras on the ITOS spacecraft have a field of view of 89 degrees on a side and 104 degrees across a diagonal. As shown in Figure 1-VIII-13, the area covered when the spacecraft is at a nominal altitude is approximately 1830 nautical miles on a side and about 2850 nautical miles along a diagonal. The APT format is about three-quarters the length of the AVCS along the spacecraft subtract.

The cameras have been designed to take TV pictures of Earth and its cloud cover during subpoint daylight. The picture-taking operations of each subsystem are controlled by ground-initiated commands, which are transmitted to the spacecraft from the CDA stations and subsequently processed and stored by the on-board command subsystem. In general, each subsystem may be commanded to take a continuously repeated sequence of 11 pictures, starting at some predetermined point in the orbit. Once initiated, the pictures in the sequence are taken automatically at 260-second intervals until all 11 have been completed. Shortly after the last picture in the sequence has been completed, the command subsystem turns the power to the cameras OFF until just before the

*Visible data imaged during nighttime will not produce usable information.

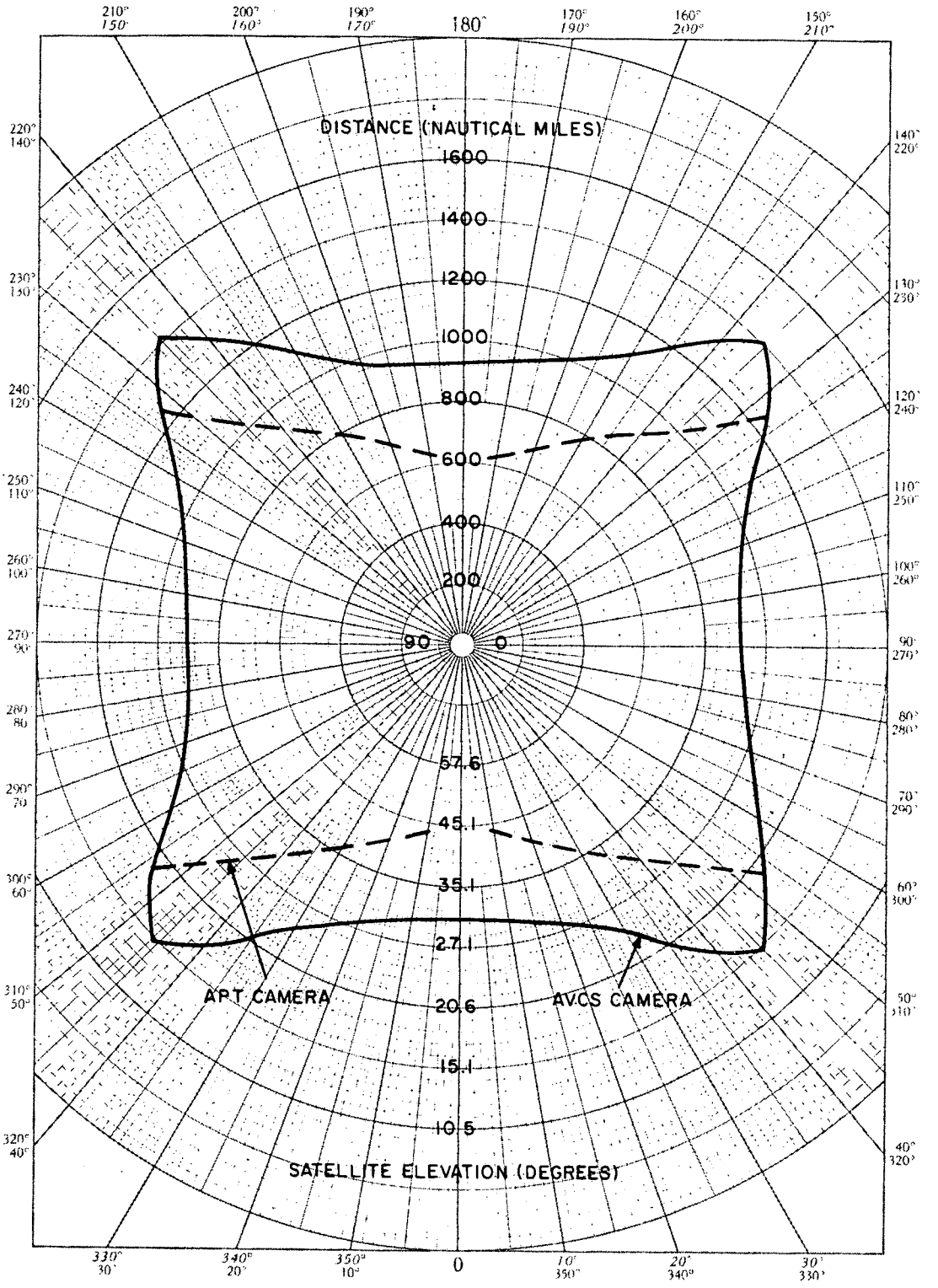


Figure 1-VIII-13. Camera Field of View for Orbit at 790-Nautical-Mile Altitude

sequence repeat time has expired; a "power on" signal generated by the programmer then restores power and the picture-taking sequence is repeated. The repeat time is determined by the data loaded into the programmer and generally is made as nearly equal to the orbital period as possible. When this is the case, subsequent picture sequences will start at very nearly the same latitude but at a longitude different from that of the previous orbit by the excess of Earth's rotation over the orbital precession; during one orbit, this excess is 18.8 degrees westward at the equator. The wide-angle nature of the pictures is sufficient to produce a slight lateral overlap in coverage at the equator with the prescribed longitude displacement. The amount of lateral overlap will increase, of course, with latitude. The 260-second picture-taking rate gives rise to a 50-percent overlap in successive AVCS pictures and about 20 percent in successive APT pictures along the orbital track (see Figure 1-VIII-14). The ground resolution of the pictures is about 2 miles per TV line pair at the spacecraft subpoint.

2. Secondary Sensors Subsystem

The secondary environmental sensors are part of the GFE* on the ITOS spacecraft. The secondary sensors subsystem and the principal components used in conjunction with its operation are as follows:

- A flat plate radiometer (FPR), which consists of two pairs of solid-state detectors, electronics, and a means of calibrating one pair of sensors;
- A solar proton monitor (SPM), which consists of six solid-state detectors and an electronics unit,
- An incremental tape recorder (ITR), and
- A data format converter (DFC).

The FPR is designed to gather Earth heat-balance data. From its output, which, after on-board processing by the FPR electronics, consists of 8-bit digital words, the amount of heat being radiated from Earth into space may be determined. By comparing this with the solar influx, the amount of heat absorbed by Earth may be ascertained.

The FPR consists of four detectors: one pair of radiative equilibrium (RE) detectors and one pair of thermal feedback (TF) detectors. Each pair consists of one "white" and one "black" sensor (the difference being in surface finish and, therefore, spectral response). The RE sensors are of the same type as those

*Government Furnished Equipment

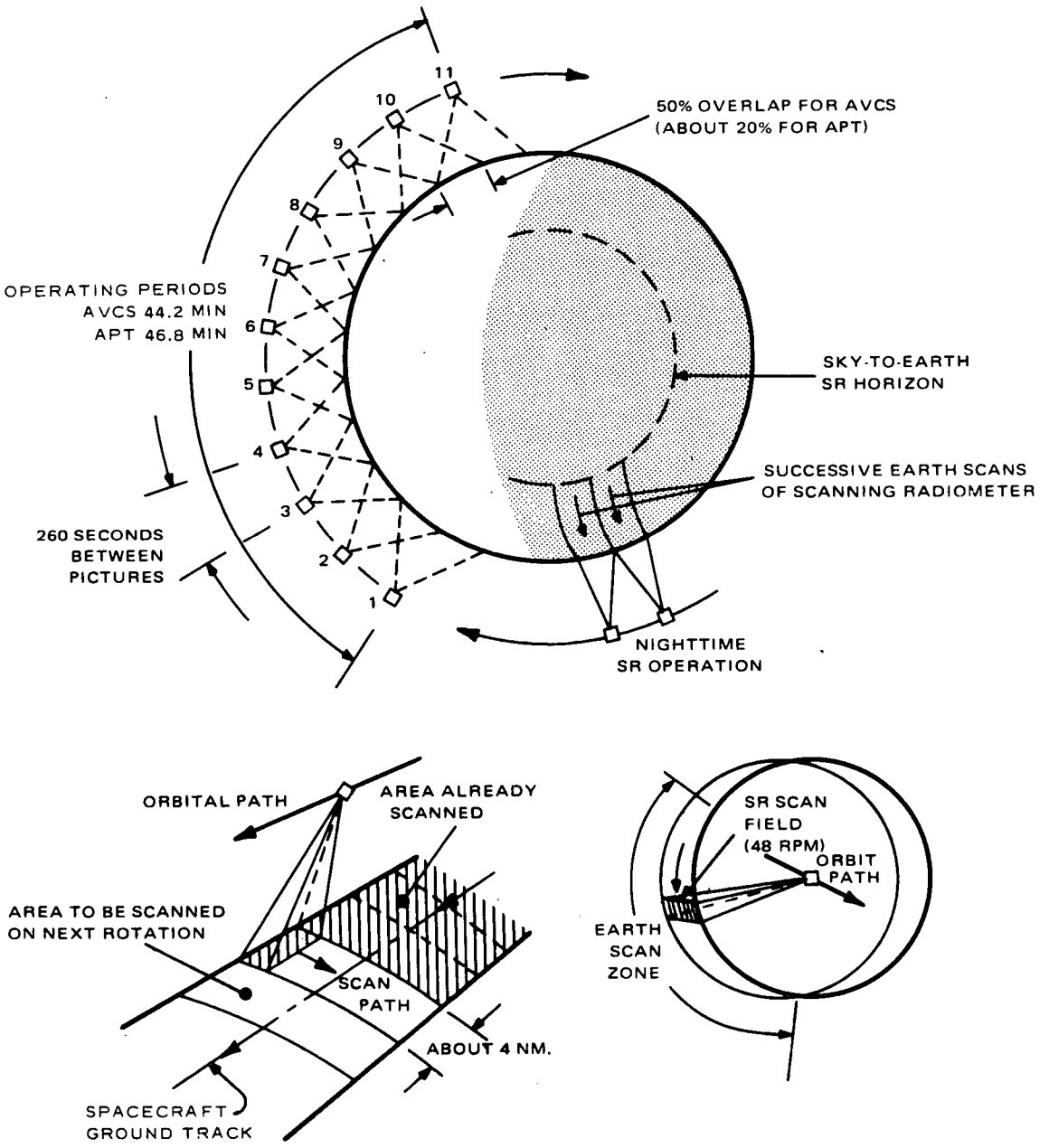


Figure 1-VIII-14. Orbit Coverage of Primary Sensors

used on the TOS AVCS spacecraft. The TF sensors employ a thermal detector and a heater strip. The sum of the thermal inputs from Earth, space, and heater maintain a constant detector output. The TF sensors may be calibrated in orbit. The detector outputs result in a pulse count which is assembled into the FPR digital bit-stream. The detectors, which are mounted on the Earth-facing side of the spacecraft, have a field of view equivalent to a hemisphere or 2π steradians. The state of the FPR and its signal output are controlled and processed by the data format converter.

The SPM is used to determine the proton fluxes encountered at the altitude of the orbit. SPM data is expected to provide a better means of measuring and predicting solar-flare activities, which exert detrimental effects on radio communication and impose a hostile environment for manned space exploration.

The SPM monitors the environment with six solid-state detectors. Five of these are proton detectors, whose design permits commutation to provide sequential readout of six energy levels. The sixth detector, which is designed to detect and measure electron activity, will be used to ascertain the degree to which proton flux measurements have been contaminated by high-speed electrons.

Three of the four detectors are mounted on the "anti-earth" face of the spacecraft and have fields of view of a full hemisphere; the fourth has a field of view of about 1/20th of this. All of these detectors have their view axes parallel to Earth's magnetic field in the vicinity of the poles. The remaining two detectors face along the spacecraft pitch axis and away from the sun, with their view axes very nearly perpendicular to Earth's magnetic field throughout the orbit. These units have fields of view of approximately 1/20th and 1/200th of a hemisphere, respectively. The outputs of the detectors are processed by the solar proton monitor electronics unit.

PART 2. SPACECRAFT DESIGN

SECTION I. INTRODUCTION

An overall exterior view of the ITOS spacecraft is shown in the frontispiece. (The TIROS M spacecraft is the flight model prototype of the ITOS spacecraft.) The general shape of the spacecraft is that of a rectangular prism with three hinged solar panels that are folded along the sides of the spacecraft at launch and deployed, as shown in the frontispiece, for operation in orbit. Approximately 10,000 solar cells are mounted on the solar panels to provide the electrical power required for subsystem operation. The primary sensory equipment, consisting of four television cameras and two scanning radiometers, is oriented to view the earth from one side of the spacecraft. Other external features of the "earth side" of the spacecraft are a flat plate radiometer, which is one of the secondary sensors, an S-band antenna, and a solar aspect sensor. The two solar panels hinged at opposite sides of the spacecraft support the elements of real-time antenna arrays at their outer corners.

On two sides of the spacecraft are hinged flaps, operated by thermal sensor-actuators, which provide active temperature control to maintain favorable temperatures in the interior component compartment. Passive thermal control is provided by concentric thermal "fences" and mirrored surfaces mounted at one "end" of the spacecraft box, and fixed radiator surfaces on the equipment panels and the baseplate. A single-element command and beacon antenna is mounted at the end with the thermal fences, and the antenna projects perpendicularly from the surface.

The baseplate is at the end opposite the thermal fences. A separation ring is attached to the baseplate and a momentum flywheel device used for spacecraft pitch control and attitude stabilization is located within the separation ring. On the hub of the flywheel is a mirror array which is part of the roll and yaw attitude sensing equipment.

Solar proton sensors of the secondary sensors subsystem are located at one corner of the spacecraft box.

The basic structure of the spacecraft consists of a central equipment module, including the baseplate and two equipment side panels, a cross-bracing structure at the end opposite the baseplate, and two side access panels. All of these structural components are of skin-and-stringer design and are fabricated from riveted sheet aluminum. The electronic components which make up the functional subsystems of the spacecraft are mounted on the baseplate and two equipment side panels. The thermal "flaps" are located in the equipment side panels and the

access panels are on the "earth" and "anti-earth" sides of the spacecraft. The solar panels are fabricated from bonded honeycomb material with three sheet metal reinforcing channels bonded to the concave sides.

The satellite components are grouped functionally into separate but coordinated subsystems which control spacecraft operation, maintain proper spacecraft attitude, and gather and transmit data to the ground stations. The subsystem groupings and their functional relationships are shown in Figure 2-I-1. The vehicle dynamics subsystem makes use of TOS-proven techniques of magnetic bias control and quarter-orbit magnetic attitude torquing. A speed-controlled momentum flywheel is employed to achieve the pitch control required for earth orientation of the primary environmental sensors. Attitude sensing is accomplished by a digital solar aspect sensor, two pitch horizon sensors, and two roll horizon sensors. Liquid dampers are used to reduce spacecraft nutation. The power supply subsystem is similar to the TOS power supply subsystem, but has greater capacity to handle the increased demands of the three primary data subsystems. A greater solar cell area is created by the array of cells mounted on the three deployable panels.

The APT and AVCS primary environmental sensor subsystems are very similar individually to the TOS APT and TOS AVCS subsystems, with revised timing to provide 11 pictures from one of the APT cameras and 11 pictures from one of AVCS cameras during the daylight portion of the orbit. Continuous infrared mapping is obtained during the nighttime portion of the orbit by the scanning radiometer (SR) subsystem. The APT and SR data are transmitted in real time for reception by APT ground stations around the world. SR data is also recorded in the satellite and transmitted with recorded AVCS data to CDA ground stations. The SR subsystem also produces a visible output, and either the visible or infrared output can be substituted for the APT output during subpoint daylight operations.

The secondary environmental sensors include a flat plate radiometer for obtaining earth heat balance data and a solar proton monitor for sensing proton and electron flux levels at the satellite altitude. Secondary sensor data is recorded on an incremental tape recorder and played back for transmission to the CDA ground stations.

The command subsystem for ITOS is similar in many respects to the TOS subsystem; however, it has an increased command capacity since the ITOS spacecraft has a greater number of functions.

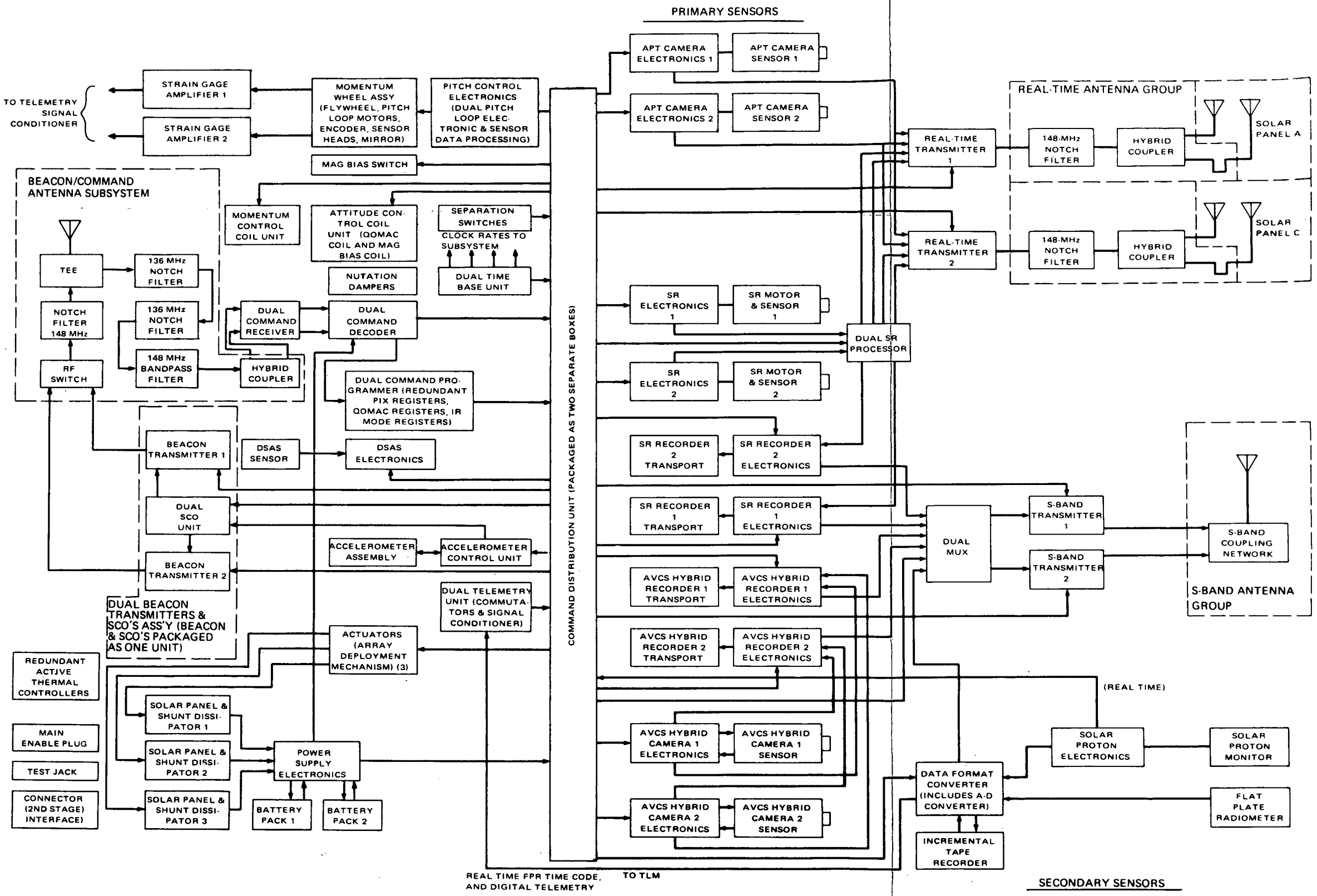


Figure 2-I-1. The ITOS Spacecraft, Functional Block Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

The communications subsystem consists of four data links which handle (1) commands transmitted to the satellite, (2) real-time environmental data transmitted from the satellite, (3) remote environmental data transmitted from the satellite, and (4) beacon and telemetry data transmitted from the satellite. The command, real-time, S-band, and beacon and telemetry links have their counterparts in the TOS communications links. The command and beacon antenna, remote data link antenna, and the real-time data link antenna designs were developed for ITOS.

SECTION II

SPACECRAFT STRUCTURE

A. GENERAL

The ITOS spacecraft configuration is illustrated in Figure 2-II-1; the panels comprising the main body, the three deployable solar panels, the passive thermal control fence, and the active thermal control louvers are identified in the illustration. The main body of the spacecraft measures 40 by 40 by 48.5 inches, the thermal control fence is 4.5 inches high and 36 inches in diameter, and each of the three curved solar panels is approximately 36.4 inches wide and 65.2 inches long. When folded, the solar panels extend 11 inches beyond the separation plane.

The spacecraft is designed to be dynamically and statically compatible with the launch vehicle and the improved Delta fairing. In the launch configuration, the spacecraft is mounted to an attach fitting and coupled to the fitting with a Marmon clamp. Four separation spring pads, two separation switches, a breakaway connector, and a separation ring keyway on the spacecraft interface with elements on the attach fitting. The spacecraft main body consists of externally reinforced aluminum panels bolted together to form a rectangular prism. The sensors and most of the electronic equipment are located on three of these panels; i.e., panels 2, 4, and the baseplate. Panels 2 and 4 are hinged to the baseplate and, as shown in Figure 2-II-2, can be laid flat for integration and electrical checkout of spacecraft components.

Large openings in the access panels, shown in Figure 2-II-3, permit component repair or replacement after the main body of the spacecraft is assembled. Panel 5 serves as the mounting surface for the passive thermal control fence, and the command and beacon antenna. Crossbracing is provided beneath this panel. The three curved solar panels are independently hinged to panels 2, 3, and 4 of the spacecraft.

The solar panels are of bonded-honeycomb construction, with sheet metal reinforcing channels bonded to the backside skin. All the other structural members are of skinstringer construction and are fabricated of riveted sheet metal.

B. DESIGN APPROACH

1. Requirements and Constraints

The primary influence on the size and configuration of the spacecraft structure was the accommodation of the electronic and sensor equipment for the spacecraft mission. The sensors (four cameras, three radiometers, and a solar

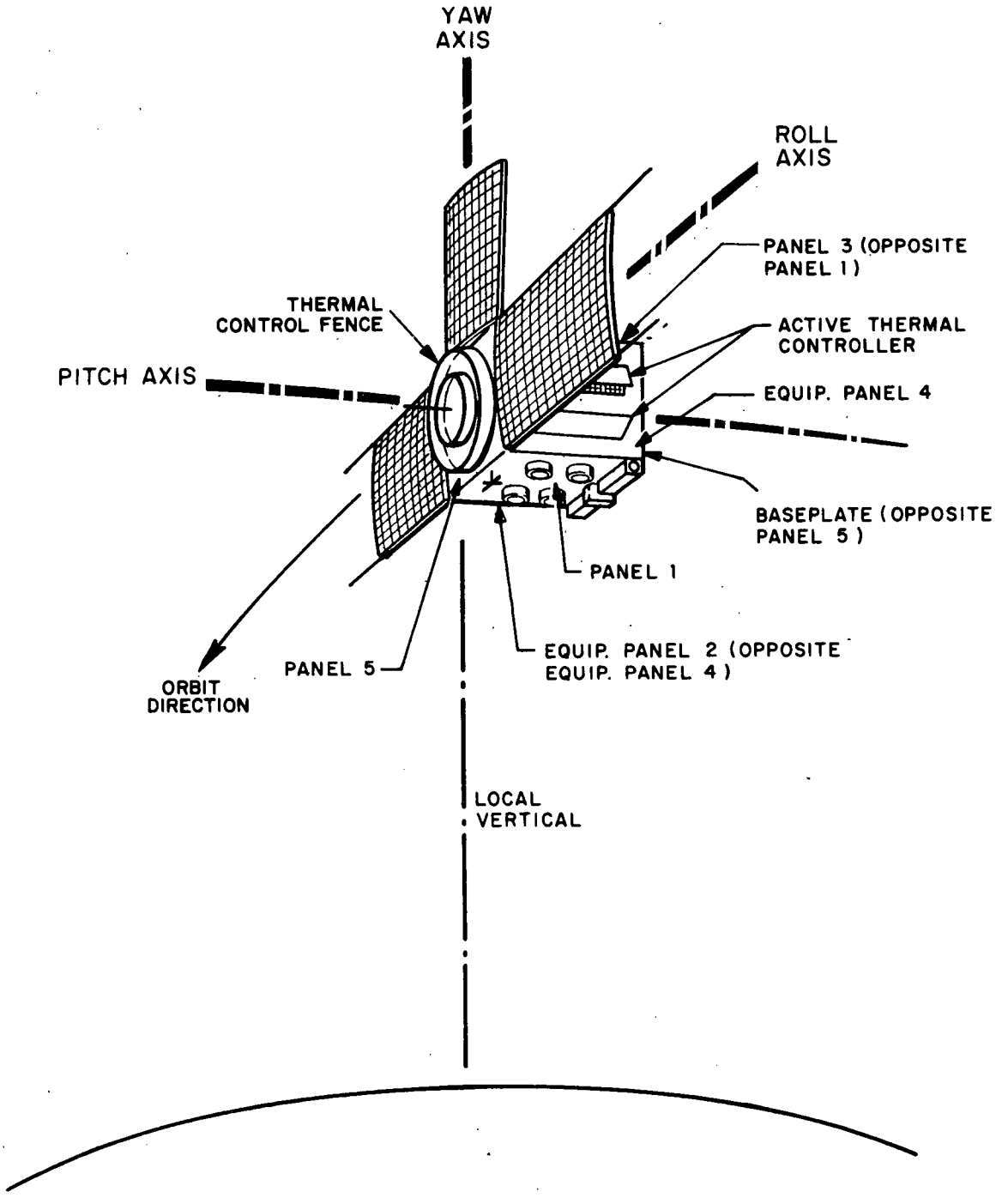


Figure 2-II-1. ITOS Spacecraft Orientation

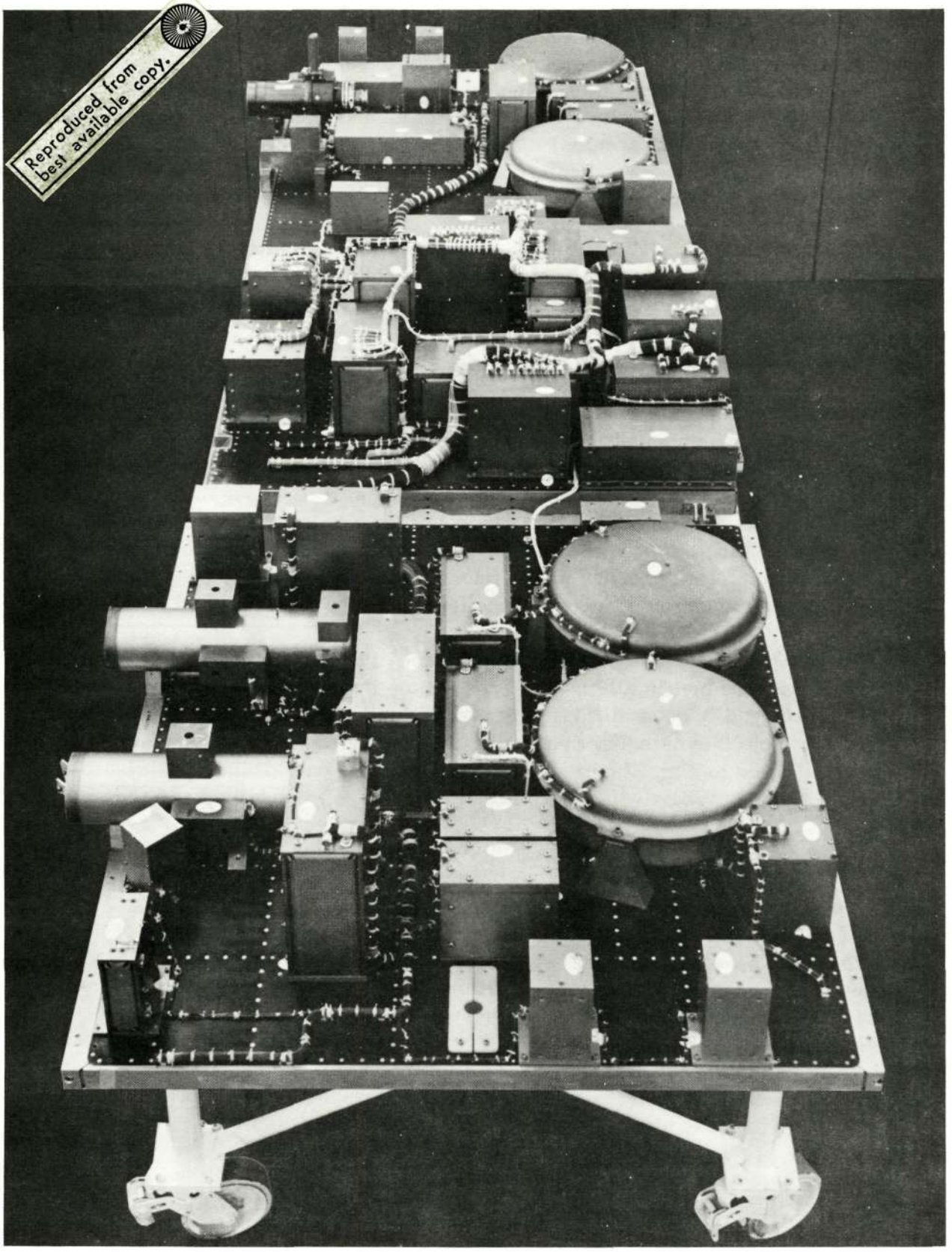


Figure 2-II-2. Spacecraft Component Integration Configuration

proton monitor) require a clear field of view, unobstructed by any part of the spacecraft structure, by other sensors, or by the antennas. Positioning of the antennas on the spacecraft was influenced by radiation pattern requirements. Various areas of the structure were required to accommodate power command and control, sensor electronics, dynamics and recording equipment. The design of the thermal control fence, active thermal controls, and solar panels was also influenced by and had an effect upon the design of the spacecraft structure.

The stabilization system, because of its configuration, function, and locational requirement, the fairing envelope and launch vehicle interface, accessibility, balance, interchangeability, manufacturability, alignment, grouping of subsystems, and environmental test constraints were other factors that influenced the configuration of the structure.

An order of importance was established for all requirements, to resolve conflicts between requirements or constraints and to optimize tradeoffs. The requirements were grouped into three categories: (1) those that demanded total compliance to avoid impairing the function of the spacecraft or of certain spacecraft equipment, (2) those that could be changed to a limited extent without impairing the function of spacecraft or equipment, and (3) those that could be modified within much broader limits than could the second category without impairing equipment or spacecraft function.

The first two categories of requirements were given top priority and the requirements were met in all parameters. In the third category, requirements could more readily be traded off with one another, and the order of importance selected within this category eventually determined the final configuration of the spacecraft, led to simplifications of design and fabrication, and established the degree of compatibility with future missions.

2. Design Synthesis

One of the first steps in the spacecraft design was the synthesis of requirements, constraints, and a structure concept into a compatible, balanced spacecraft design. The subsystem equipment was investigated to determine the various shapes and sizes that would be required for optimum performance. Where conflicts existed between subsystems, they were resolved in favor of program objectives. Certain of the system features were subjected to extensive review to determine exact requirements and interrelationships between components. The process of tradeoff study was begun at this point.

The baseplate area of the spacecraft was reserved for bus functions such as power, attitude control, and command distribution, while the equipment panels were used for the mounting of sensors and associated control and recording equipment. To facilitate installation of the electronic equipment and to provide maximum accessibility for testing, the panels were hinged, allowing the

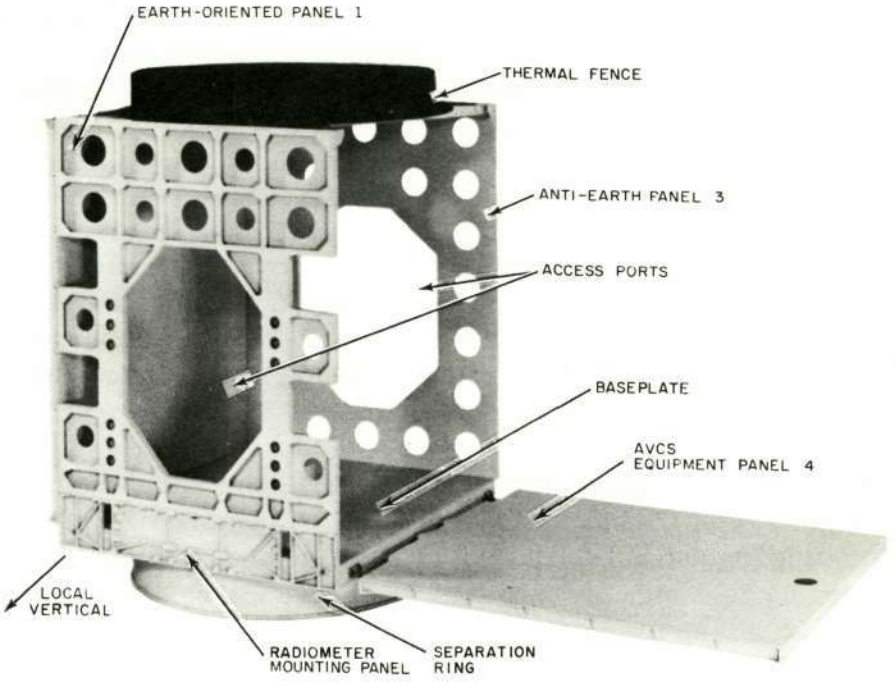


Figure 2-II-3. ITOS Basic Structure, Showing Panel Access Ports (Cutouts) and Hinged AVCS Equipment Panel Opened

structure to be opened. Access openings were included in the structure to permit repair or replacement of equipment inside the integrated spacecraft.

As the design progressed from the baseline configuration to the final hardware configuration, options were established and traded off and interrelationships and conflicting requirements were assessed and resolved. The design process started with the major structural configuration of the spacecraft, proceeded to the major component level (type of construction), to the minor component level (e.g., number and size of ribs), and finally to the detail level (e.g., type of bolts). Some options were restudied because of new information received during the design stage; in some cases, an alternate option was selected on the basis of the new information. Certain approaches were eliminated because of excessive cost and unavailability of materials.

3. Spacecraft Structure

The structure was broken down into simple elements; i.e., tension members, compression members (columns), beams, plates or shells, and torque tubes; these elements were then aligned with the expected loads. An established design goal was load sharing of members; accordingly, certain elements of the structure were designed to withstand multiple types of loading.

Simplicity and uniformity of elements were the design goals for the structure component configuration. The initial structure configuration was studied with the objectives of obtaining as many continuous notchless members as possible and of aligning these members with the highest loadings. The number of elements (ribs) was traded off against weight, cost, and complexity. Approximate calculations were made of the natural frequencies of the major components with the aim of attaining frequency separation. A 50-percent spread between frequencies of the major components was desirable to provide the necessary frequency isolation. To attain this separation, approximate calculations of the natural frequencies of these components were made. However, since the calculated values of natural frequency may differ from actual values (because values of parameters such as end fixity or joint compliance must be assumed), methods for detuning the system or changing its damping characteristics were introduced.

A feature of this type was incorporated into the solar panel design, to allow the natural frequency of the panels to be changed as required.* Information required for calculating the natural frequency of the launch vehicle attach fitting was incomplete, since design of the fitting was begun after design of the spacecraft. This information was essential to the calculation of spacecraft frequency, because the vibration input is applied to the bottom of this fitting. On the basis of the best information available, it appeared that the natural frequency of the solar panel would be between that of the equipment panel and that of the spacecraft, without sufficient separation. The use of a thicker solar panel would have raised the natural frequency and provided sufficient separation, but this was unacceptable because of weight and volume considerations.

To overcome this problem, two intermediate supports were added approximately halfway between the two main supports of the panel: the panel was preloaded so that it would remain in contact with the intermediate supports. The addition of the intermediate supports increased the natural frequency of the solar panel; the supports could be removed to lower the frequency if it should prove to be aligned with the natural frequency of another component.

4. Mechanisms

Two major goals of the mechanical design were (1) to minimize the number of moving parts and (2) to reduce the complexity of the moving parts without jeopardizing their functions. Wherever possible, existing space-qualified hardware was incorporated in the design to reduce the cost of qualification testing. Redundancy to reduce the possibility of system failure was also considered where applicable.

The hinge alignment problems usually encountered with rigid units and bored holes were avoided by using spherical, self-aligning, reinforced Teflon bearings

*This flexibility also permits the solar panel to be modified for other missions.

in all hinge members. The screws used in the bearings were coated with dry-film lubricant to provide redundant bearing surfaces. Most of the linkage joints were provided with the same type of spherical bearings to eliminate binding and misalignment. Spherical joints were designed into bumper pad assemblies and solar panel restraining elements to ensure complete seating of these items. Threaded members in these assemblies afforded sufficient adjustment so that tolerances of the major assemblies could be relaxed without jeopardizing their functions. The components were designed so that differential thermal expansion between major elements of the spacecraft would not result in jamming or increased friction in the mechanisms.

Moving parts between metal to metal contacting surfaces and butting metal surfaces which separate away in space were either interferred with dielectric spacers, or adjacent metal surfaces were treated with dry film lubricants. These surface treatments were primarily to prevent the possibility of vacuum cold-welding, a phenomenon which has been researched by industry and government without any conclusive results. Contact forces, surface roughness and similarity of contacting metals are parameters contributing to possibility of vacuum cold-welding to forego any possibility of metal seizing; therefore, all interfacing metal surfaces on the spacecraft were treated with dielecttic surface treatments or dielectric spacers.

5. Stress Analysis

The purpose of the stress and vibration analysis was to verify mathematically the integrity of the structure. The target weight of the spacecraft was approximately 670 pounds, but the design must be able to accommodate future mission flexibility and growth that could increase the total weight to 720 pounds. The analysis was accordingly conducted for the heavier model.

All stress analyses of the structure assumed an input G-level, applied to the lower end of the attach fitting, at 3.0 G's in the resonance range of the thrust direction and 2.3 G's in the resonance range of the lateral (transverse) direction, with no G-level notching.

Further evaluation by cognizant NASA agencies (at a later date) resolved that the Delta launch vehicle was not capable of developing the aforementioned dynamic forces to the spacecraft, particularly in the range of structure resonance. The qualification thrust G-levels were therefore reduced from 3.0 to 2.3 G's (peak-to-peak) and the lateral levels were reduced from 2.3 to 1.5 G's. An even larger reduction in the levels of applied power spectral density in the lower frequency range was invoked for the random spacecraft qualification tests. Furthermore, a notching criterion was introduced into the sinusoidal vibration tests whereby the dynamic forces in the thrust direction were being limited to 12,000 pounds and the lateral bending moments, at the spacecraft/attach fitting separation plane, were being limited to 75,000 inch-pound maximum. The

mechanical test model (MTM) contained solid dummy boxes and was tested to the higher G-levels; accordingly, the analysis was conducted using the higher vibration-amplification factors associated with the MTM. These factors have resulted in a structure conservatively designed for the actual 720-pound spacecraft, with an approximate 25-percent margin in weight carrying capacity based upon the latest vibration specifications.

Since the sizes and locations of the dummy boxes were not established at the start of the analysis, it was assumed that the 1-G dummy component loads were uniformly distributed on the equipment panels and baseplate. Because of the concentrated weight of the momentum flywheel at the center of the baseplate, an exception was made to the assumption of uniform distribution of static weight for this item. This approach resulted in an analysis that is also valid for the bus concept. The actual distribution of the dummy boxes was reviewed when the placements were determined. Local reinforcements were added to the structure to distribute local concentrated loadings from the box mounts to the main members of the structure.

The spacecraft was designed to comply with the following criteria:

- The sinusoidal sweep and random noise environment required by the NASA/GSFC Document S-320-D-2, dated June 1, 1965, and entitled "The Environmental Test Specification for the Spacecraft and Components Using the Launch Environments Dictated by the Improved Delta Launch Vehicle".*
- The solar panel actuator static load induced by Adel deployment actuator, which is equal to 160 pounds between the solar panel and the equipment or the anti-earth panels.
- The solar panel preloads required to keep the midspan of the solar panel in contact with its snubbers during the environmental tests.
- The handling loads induced into the pickup points of the spacecraft during moment-of-inertia tests and other movements of the spacecraft.
- The thermal stress induced into the solar panels and thermal supporting structure by the thermal environment.

A summary of the analysis results is given in Section 4.0 of the TIROS M Engineering Stress Analysis Report for the Spacecraft Structure, AED-R-3244.

*Latest Revision: S-320-G-1.

C. DESIGN PHILOSOPHY

1. General

A box with its sides fastened to each other along their edges is an efficient structure since each side supports the adjacent sides. The load sharing provided affords a rigid and lightweight structure. Lightweight components (antenna couplers, switches, filters, sensors, etc.) can be mounted on the access panels, freeing more area on the equipment panels for heavier components. The access panels also serve as mounting surfaces for the solar panel actuating mechanism and the S-band antenna. The earth-oriented access panel (panel 1, Figure 2-II-3) must be specially designed for each mission, depending upon the requirements for location of the sensors on the equipment panels. A more universal design could have been achieved for the earth access panel, but at the expense of additional weight.

The structure is designed for flexibility of application and will accommodate various arrays of electronic and sensor equipment without major modification. As shown in Figure 2-II-2, the equipment panels are hinged to the baseplate and can be folded down in line with the baseplate, thus facilitating testing and integration of the various components. When the structure is in the final assembled configuration, large holes in the access panels (Figure 2-II-3) facilitate component replacement or repair without disassembly of the structure.

One of the principal goals of the design effort was to achieve a sheet metal structure of minimum weight. Therefore, fabrication methods were selected on the basis of reduced structural weight, and studies were conducted on the main structural members to determine the design concept affording the least weight while maintaining the desired function. Where possible, flexibility of the design was increased and tradeoff studies were made for the major fixed components (i.e., momentum flywheel, nutation damper) and the structural elements to achieve the lightest possible system weight. Other design goals were simplicity of structure, maximum accessibility of interior parts, minimum number of parts, and use of proven fabrication methods. Wherever possible, one member was to serve several functions.

The structure analysis assumes a universal bus design to support a total spacecraft weight of 720 pounds with uniformly distributed static loads applied to the equipment panels and the baseplate. Each equipment panel carries approximately 30 percent of the component weight and the baseplate carries 40 percent of the component weight. Analysis was made of the primary loads induced by the critical sinusoidal and random vibrations encountered during the launch phase; secondary or local loads caused by the loading of the actual "black box" configuration during vibration testing was investigated when the configuration was finalized. Where high local stresses were induced by the loading of the black boxes, reinforcing brackets were added to the underside of the basic structure. The number of brackets, the locations, and the sizes must, of course, be unique for each mission.

Dynamic coupling between structural elements was minimized wherever possible by incorporation of frequency separation in the design. A separation of 50 percent is desirable for satisfactory isolation. Details of frequency isolation considerations are given in TIROS M Engineering Stress Analysis Report, Volume 1.

2. Mechanical Alignment

The major structural components, such as the baseplate, equipment panels, and access panels, are designed to achieve and maintain squareness and parallelism of the structure. Accurate jigs and fixtures accomplish positioning of the machined edge members, and the use of body-bound bolts maintains the alignment. No weight penalty is imposed for this alignment control feature.

Final machining of the baseplate and the use of close-tolerance bolts at the interface of the baseplate ring and the separation ring achieve and maintain control of the alignment of the spacecraft with the launch vehicle. The mating surface of the baseplate ring is perpendicular to the spin (pitch) axis within 0.01 degree, and flat to 0.005 inch TIR*. The upper and lower mating surfaces of the separation ring are parallel and flat within 0.005 inch TIR.

The mounting plate for the momentum wheel assembly is machined perpendicular to the pitch axis within 0.05 degree and flat to 0.005 inch TIR. This maintains the total nonperpendicularity from the separation ring mating surface to the mounting surface of the momentum wheel assembly within the 0.1 degree of the system requirement for alignment. The lower mating surface of the separation ring could therefore be used as a reference for momentum wheel assembly and camera sensor alignment procedures when the separation ring was bolted to the baseplate ring.

Close control of the camera and sensor mounting surfaces (to 0.03 inch TIR) minimizes the number of shims required for the final alignment of the cameras and sensors. The use of body-bound bolts, to join the major assemblies of the structure, maintains alignment during environmental tests and in the launch environments.

3. Component Accessibility

The integration of the electronic components into the spacecraft structure was accomplished as described earlier and as illustrated in Figure 2-II-2. The equipment panels are equipped with removable hinges for attachment to the baseplate and are coplanar with the baseplate in the folded-down position. With the structure in this open configuration, all integration and initial testing of the

*TIR - Total indicator runout.

subsystems were accomplished with excellent accessibility to all subsystem elements. With the structure assembled to its final box configuration, with the access panels in place and hinges removed access to the interior of the spacecraft is provided through the large cutouts in the earth-oriented and anti-earth access panels. These access holes, approximately 25-1/2 by 20-3/4 inches in the anti-earth panel and 18-1/2 by 25-1/2 inches in the earth panel, are large enough to admit a man's shoulders so that the electronic equipment could be repaired or removed from the spacecraft without disassembly of the structure. Two men could reach into the assembled spacecraft at the same time through the two access panels. Since no subsystem component is more than 20 inches from the access holes, inspection could be made without disturbing the spacecraft structure.

The nutation dampers, momentum control coil and active thermal controllers are mounted on the exterior of the equipment panels, and accessibility to these elements is not a problem; however, in the completely assembled spacecraft, the solar panels would have to be deployed and the thermal blanket removed if inspection of the elements were required.

4. Weight

The total estimated launch weight of the spacecraft is 682.0 pounds.

5. Fabrication and Assembly

Fabrication and assembly procedures were analyzed to provide assurance of structural alignment and interchangeability. To ensure the maintenance of tolerances on dimensions, squareness, parallelism, and the flatness of mating or mounting surfaces, the controlling surfaces were machined so that they could be held accurately in jigs and fixtures during riveting. The base of the spacecraft structure has a short, permanently attached ring (the baseplate ring) that mates with the separation ring. After fabrication of the baseplate, the baseplate ring was final-machined, using the skin of the baseplate as a reference surface. This eliminated distortions in riveting the ring to the baseplate and ensured parallelism between the baseplate skin and the mounting surface for the baseplate ring. During this operation, the mounting plate for the momentum wheel assembly was final-machined, ensuring the maintenance of an accurate reference between the baseplate ring and the momentum flywheel assembly. After machining, the baseplate-ring-to-separation-ring mating holes were jig-drilled. Close-tolerance, high strength bolts were used to provide alignment and concentricity control and to carry shear loads. The separation ring is interchangeable and easily replaced if damaged.

The radiometer mounting plate makes up the lower portion of the earth-oriented access panel (panel 1, Figures 2-II-1 and 2-II-3) and must be of the same width. To ensure that the surfaces of the radiometer mounting plate and the panel presented a continuous smooth mating surface for the equipment panels, the parts were assembled with accurately made fixtures and joined with close-tolerance bolts. The bolt holes were jig-drilled and reamed to ensure accurate realignment of the structural parts in the event of disassembly, as well as to provide adequate shear strength at the joint between the panel and the mounting plate.

Since the mounting surfaces for the equipment panels are the edges of the baseplate and the two access panels, these three parts (the radiometer mounting plate being considered a part of the earth-oriented access panel) must present a flat, smooth, continuous surface for the equipment panels. If the baseplate and one or both of the access panels differed in width within normal tolerances, the equipment panels could be stressed locally when these panels were bolted to the baseplate and access panels. To maintain tolerances on the width of the parts close enough to prevent such damage to the equipment panels would be difficult, expensive, and unnecessary. It was more advantageous to assemble the baseplate and access panels in accurately made fixtures of a matched dimension than to specify a close tolerance in width between the access panels and the baseplate.

The baseplate and access panels were assembled first, with the earth-oriented access panel and baseplate jig-drilled from a single jig. The drilled holes were then reamed to final size for shoulder bolts and the access panel was joined to the baseplate. The anti-earth access panel was joined to the baseplate similarly, but because of a different pattern of mounting holes, a different drill jig was used.

After the access panels were jointed to the baseplate, the bolt holes for the equipment mounting panels were drilled. The baseplate and access panel subassembly was clamped in a square configuration and a drill jig used to drill holes in the edges of the baseplate and access panels. Using the other side of the same drill jig, matching holes were drilled in the equipment panel. The same procedure was then followed for the second equipment panel, again using the same jig. Following this, the holes were all reamed to final size and precision bolts installed, thus completing the major assembly of the structure. Body-bound bolts were used for two reasons: they provide control for satisfactory alignment and also perform a shear function at the joint between adjacent panels. The crossbrace of panel 5 (opposite the baseplate) was the last structural assembly to be integrated into the structure. All the members except the four corner pieces were assembled in a fixture, then the corner pieces were joined to the main structure. The crossbrace or X-frame was then fitted, drilled, and riveted to the corner pieces. The thermal fence was attached to the X-frame at this time, with the holes in the thermal fence spotted from the X-frame. Standard hardware was used to join the crossbrace fittings to the panels and to attach the thermal fence. In addition, the thermal fence is conductively isolated from the crossbrace by means of fiberglass standoffs.

6. Integration of Electronic Equipment

Several conditions had to be satisfied in integrating the electronic equipment into the spacecraft. Due to their functions, certain components such as sensors, cameras, and the momentum flywheel are required to be placed in specific areas of the spacecraft. The remaining equipment could be placed anywhere on the structure, providing the static and dynamic balance of the spacecraft was satisfied. The location of a particular unit was also influenced by other considerations such as thermal requirements, proximity of like or related units, space, geometry, and harnessing.

It was desirable to locate the mounting feet of the "black boxes" over the flanges of main structural ribs. Where this was not possible, brackets were added to the underside of the structure to support the heavier components. These brackets, consisting of intercostal beams or angle clips, are located under the mounting holes of the black boxes and the box fastened to the brackets through the skin of the structure. The rivets are thus placed in shear during vibration.

After assembly of the structure, hinges were attached to the lower edges of the equipment panels. One half of a hinge was attached to each side of each equipment panel; the other halves of the hinges were attached to the baseplate. These hinges enabled the equipment panels to be lowered from their assembled position to a horizontal position (as shown in Figure 2-II-3) for testing or replacement of components mounted on the panels without complete disassembly of the structure.

The three solar panels were finally joined to the structure. A fixture and drill jig provided location of the hinges on the solar panels and the structure. The fixture controlled the position of the interface between the halves of the hinges rather than the mounting holes for the hinges.

7. Interchangeability

Two approaches were considered for the application of interchangeability to the TIROS M structure. One approach was to make all major subassemblies of the structure interchangeable with the same subassemblies from another structure or with spare subassemblies. A second approach was to make none of the subassemblies interchangeable. A compromise philosophy of interchangeability was adopted based on considerations of cost, design and fabrication, possibilities of electronic failures, and possibility of extensive physical damage to major structural assemblies.

The equipment panels are interchangeable to facilitate replacement. For the same reason, each solar panel is made identical and, therefore, interchangeable. The separation ring is also interchangeable since its holes were located from a common drill jig.

None of the other subassemblies (baseplate, access panels, thermal fence, or crossbrace assembly) is considered interchangeable. If necessary, however, these components can be replaced by assembling the replacement part in the same assembly fixture as that used for the original part; however, the mounting holes are not drilled. The part is then mounted in (or on) the structure and the mounting holes are drilled from the holes in the mating parts of the structure.

D. STRUCTURAL COMPONENTS

1. Separation Ring

The separation ring serves as the means of connection between the spacecraft baseplate and the launch vehicle attach fitting. The ring was purchased as a forged ring of type 7075-T73 aluminum alloy and machined to the final dimensions of approximately 38 inches outside diameter, 35.5 inches inside diameter, and 5.6 inches high. Type 7075-T73 alloy was chosen to provide minimum weight since this material is 50-percent stronger in tensile yield strength than type 6061-T6 and, therefore, permits the use of a thinner cross section. The present design has no pilot diameter on the baseplate ring flange. Analysis showed that the pilot diameter section would not withstand the shear loads imposed by the launch environment. More weight would have been needed to increase the section strength; therefore, from a weight economy standpoint, another means of carrying the shear load was necessary. This load is now carried by high strength, close-tolerance bolts joining the base ring and the separation ring. Control of the alignment and concentricity of the separation ring is maintained by these bolts.

The outer wall of the cylindrical portion of the separation ring has a double taper. (See Figure 2-II-4.) The wall is thickest at the flanges and thinnest at the midpoint between the flanges. The taper is a compromise between the weight and the stiffness necessary in the flange areas. The straight inner wall of the cylinder provides a convenient mounting for the separation spring pads, spring pad brackets, and separation switches. When attached to the baseplate, the separation ring allowed removal of the momentum wheel if the separation switch brackets and spring pad brackets were removed. The breakaway connector, which contacts a mating half of the connector pair on the launch vehicle attach fitting, was attached to a separate mounting bracket exterior to the separation ring. The breakaway connector bracket was jig drilled and aligned to the underside of the baseplate.

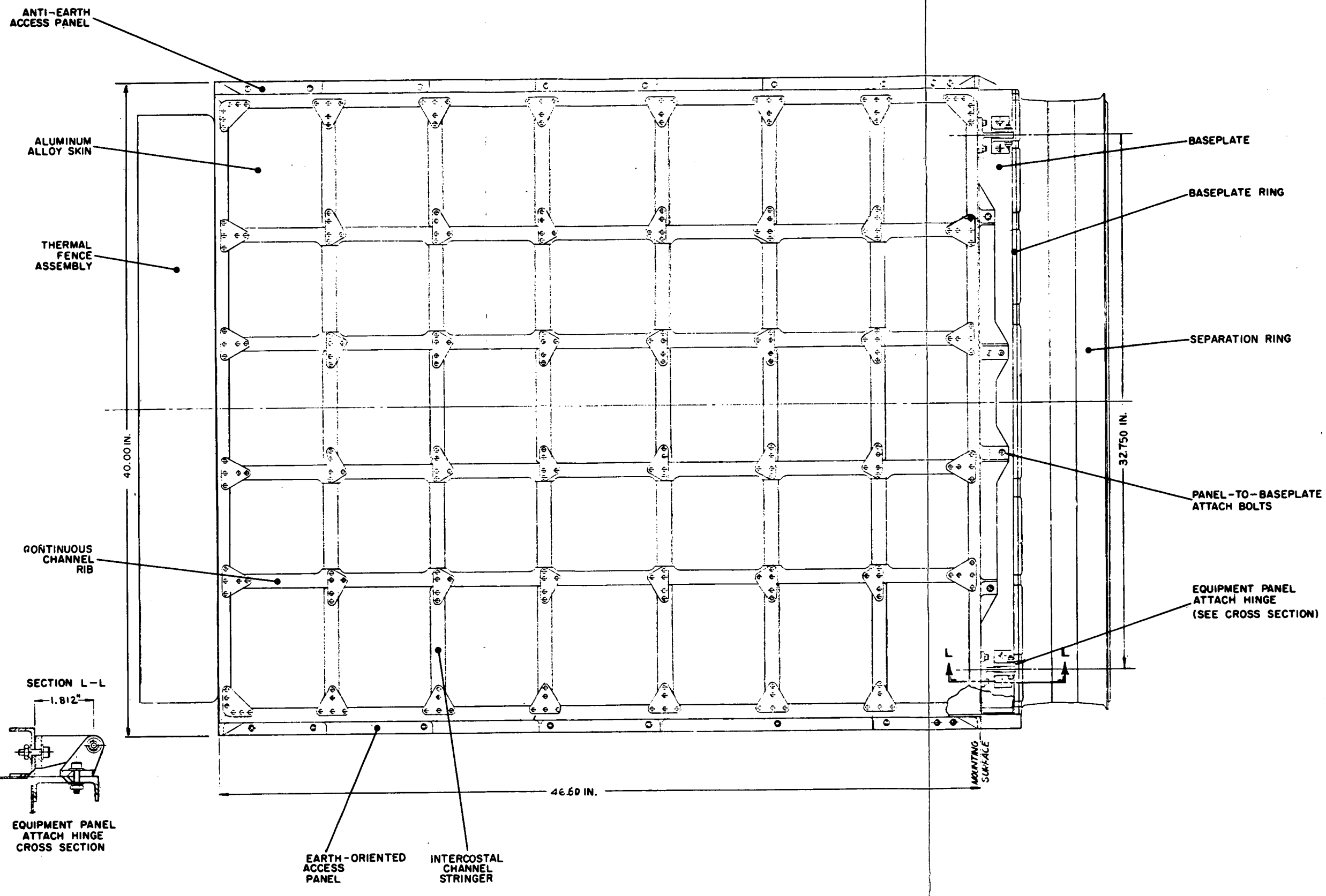


Figure 2-II-4. AVCS Equipment Panel

FOLDOUT FRAME 1

FOLDOUT FRAME 2

2. Baseplate

The baseplate assembly (Figure 2-II-5) was fabricated from sheet metal and machined components. The edge members of the baseplate are four machined 2024-T4 aluminum channels, with 0.09-inch-thick web and flanges. Bosses are located in the bolt-clamping areas and machined webs are used to join continuous channel ribs and intercostal channel stringers. The edge channels are joined together at the corners with type 6061-T6 aluminum angle clips. The mounting plate for the momentum wheel assembly was machined from 0.19-inch-thick 2024-T4 aluminum plate and was riveted to the continuous channel ribs and intercostal channel stringers.

All the continuous channel ribs and intercostal stringers were fabricated from 0.05-inch-thick, type 2024-0 aluminum and then heat-treated to the T4 or T6 condition. This procedure allowed these parts to be fabricated while the material was easily workable; maximum-strength capabilities would then be achieved through solution heat treatment and aging. The skin is 0.05-inch-thick type 2024-T4 aluminum alloy; all gussets are of the same material, but are 0.08-inch thick. During the early design phases, the skin thickness was 0.06 inch, to maintain thermal gradients between electronics equipment and thermal controllers within allowable limits. From a structural standpoint, a thinner skin would survive the imposed environmental conditions. Since a thermal analysis indicated that the 0.06-inch skin was not required, the skin thickness was reduced to 0.05 inch. The skin is finished with a blue epoxy paint on the equipment-mounting side and with 3M Black Velvet paint on the underside (radiator side). The nonradiating area of the underside of the baseplate was left in the Iridite finish state which undersurfaces all paint finishes. The equipment-mounting surface was appropriately masked off for the electronic equipment so that metal-to-metal grounding exists.

In the design of the baseplate, the continuous channel ribs were oriented in one direction and are continuous between the equipment panel mounting (edge) channels of the baseplate. This design aids thermal conductivity from the baseplate to the equipment panels since it reduces the number of joints between the electronic equipment located on the baseplate and the active thermal controllers located on the equipment panels. The continuous ribs also provide more efficient support for the equipment panels and momentum wheel assembly, which is the heaviest unit on the baseplate. The intercostal channel stringers were riveted between the continuous channel ribs and run perpendicular to them. Angle clips of the same material were used at the joints between ribs and intercostals to prevent distortion due to overall tolerance buildup.

The baseplate skin was riveted to the edge channels, ribs, and intercostal stringers. The skin and intercostal stringers are dimpled to accept the flathead rivets and provide a flat (within 0.03 inch TIR) surface for mounting electronic equipment. Gussets were riveted at all intersections of structural

members of the baseplate on the lower side. A ring which joins the separation ring to the baseplate was riveted to the ribs, intercostals, and edge members.

3. Equipment Mounting Panels

The equipment mounting panels (panels 2 and 4), like the baseplate, were fabricated from sheet metal and machined components. Continuous ribs and intercostal stringers make up an "egg-crate" structure within the edge members and the skin served as the mounting surface for the electronic equipment. The edge members were machined, with 0.09-inch-thick web and flange, from type 2024-T4 aluminum alloy. These members have a cross section that may be described as an "I" beam with part of one flange removed to form a "J" section. The open portion has gussets to provide stiffness to the outer flange for joining to the access panels.

The continuous ribs and the clips that tie the intercostal stringers to the ribs were formed of 0.04-inch type 2024-0 aluminum alloy and subsequently solution heat-treated then precipitation-hardened to the T4 condition. The intercostal stringers were formed of 0.04-inch type 7075-0 aluminum alloy and solution heat-treated to the T6 condition. The ribs are continuous, oriented vertically, and are riveted to the upper and lower edge channels. This orientation provides a better strength-to-weight ratio than an arrangement of the ribs in a horizontal direction. The ribs on these panels are located to join the baseplate at the same location as the baseplate ribs, to provide continuous stress-load paths to the separation ring. Intercostal members are located between the ribs and are perpendicular to them. The intercostal members are riveted directly to the ribs at one end and are tied to the adjacent ribs at the other end by angle clips to reduce the possibility of rib distortion during riveting. The pitch of the ribs and intercostal members on the equipment panels and baseplate was selected to provide the strongest structure for the least weight within the space and equipment constraints and still allow reasonable accessibility to attach component reinforcing brackets.

The skin of the equipment mounting panels is 0.04-inch-thick type 2024-T4 aluminum, riveted to the ribs, intercostal members, and edge channels with flathead rivets. The skin and structural members are either countersunk or dimpled, depending upon the section thickness, to recess the rivet heads below the surface of the skin to provide a flat (within 0.03 TIR) surface for mounting equipment. The skin thickness favors structural rather than thermal requirements; a thermal analysis indicated the adequacy of a thinner skin.

Gussets of 0.06- and 0.08-inch-thick type 7075-T6 aluminum are riveted to each intersection of ribs, intercostal members, and edge members to provide section continuity on the rib side of the panels.

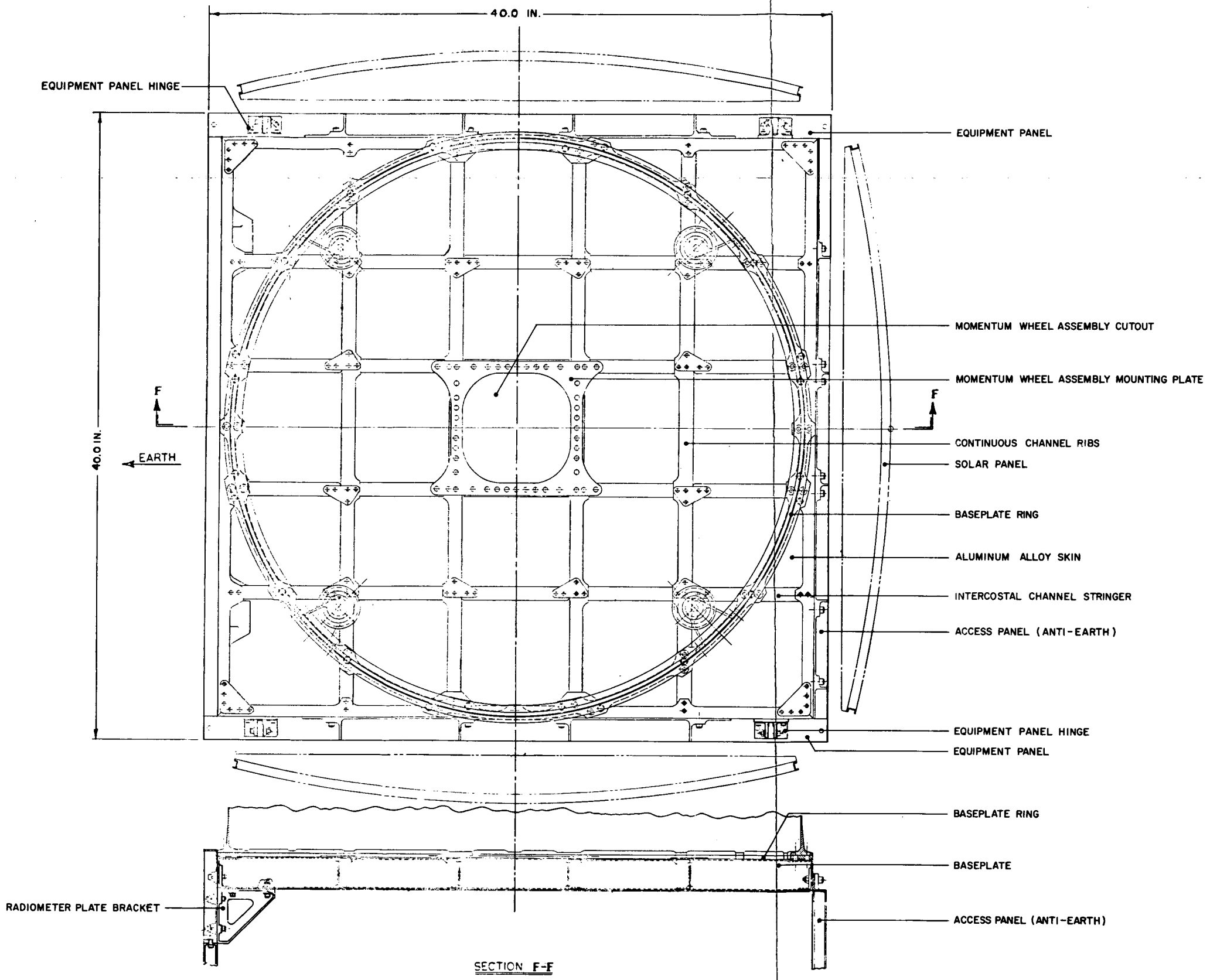


Figure 2-II-5. Baseplate Assembly

FOLDOUT FRAME 1

FOLDOUT FRAME 2

The equipment mounting surfaces of the equipment panels are finished with a blue epoxy paint, areas of which are masked to provide metal-to-metal contact with the electronic equipment, where required. The radiation surfaces, under the active-thermal-control (ATC) louvers, are finished with 3M Black Velvet Paint. The rest of the exterior surfaces of the equipment panels are left in their Iridite finish.

4. Access Panels

a. EARTH-ORIENTED PANEL

The earth-oriented access panel or front panel (Figure 2-II-6) has the same construction as the baseplate and equipment panels. It is formed of machined channels around the perimeter with a system of sheet metal ribs and intercostal stringer members within the area bounded by the edge channels. A metal skin covers the interior structural area.

The edge channels are machined from type 2024-T4 aluminum bar stock. The web of the channels is 0.09 inch thick and the flanges are 0.06 inch thick. The bottom channel interfaces with the radiometer mounting plate using close-tolerance bolts.

The ribs and the intercostal stringers were formed from type 2024-0 aluminum, and then solution-heat-treated, quenches, and age-hardened to the T4 condition. Rib and intercostal stringers are 0.03, 0.04, or 0.06 inch thick, depending upon local strength requirements. Unlike the baseplate and equipment panels, the ribs of the earth-oriented access panel are not consistent in the direction of orientation due to sensor view requirements and a large access cutout. These ribs are tied together by a system of intercostal stringers and edge members perpendicular to the ribs. Clips were again used at one end of each intercostal stringer to reduce the possibility of distortion during fabrication.

The skin was fabricated from 0.03-inch-thick, type 2024-T3 aluminum with a blue epoxy surface on the side opposite the ribs. The earth-oriented access panel is not designed to support equipment but rather is designed for minimum weight and maximum access to the interior of the spacecraft. Roundhead rivets, used to join the skin to the edge channel rib assembly, discouraged the mounting of equipment on the panel. Gussets of type 2024-T3 aluminum, 0.05 and 0.8 inch thick, are placed at most of the intersections of ribs, edge members, and intercostal stringers; intersections that do not have gussets are along each vertical side of the access cutout. These areas are supported by large shear plates riveted to the ribs to compensate for the loss of strength due to the camera cutouts. These plates were fabricated from 0.05-inch-thick, type 2024-T4 aluminum. The plates have lightening holes where strength is not necessary.

Large aircraft-type lightening holes with formed lips were used in the skin. These holes are centrally located between rib and intercostal intersections to reduce the panel weight without jeopardizing panel strength.

The access cutout is basically a rectangle with gusseted corners. The gussets were formed by the skin and a rib-type member at each corner. Small standard gussets carry the stress load from the corner rib to the main structural ribs. The camera sensor slots in the access panel were specifically located for the ITOS mission. The configuration can change as the number and location of the cameras and sensors change for different missions. The basic design concept of this member for the TIROS M mission was primarily a shear tie between the equipment carrying panels and baseplate. Added stiffening can be provided in a redesign of the earth-oriented panel for primarily load support in shear and bending.

b. ANTI-EARTH SIDE PANEL

The anti-earth access panel (Figure 2-II-7) construction closely resembles that of the earth-oriented access panel. The access cutout centrally located in the panel is larger than the cutout in the earth-oriented panel, but the panel has no cutouts for camera sensors along the vertical edges.

The channels that form the panel edges are the same as those for the earth-oriented panel, with the exception of the bottom channel whose cross section is a "J" section. This extra flange provides a surface for bolts to join the panel to the baseplate.

The ribs and intercostal stringers were fabricated by the same methods and from the same material as used on the earth-oriented panel. Material thickness of these members is 0.03 or 0.06 inch, depending on local strength requirements.

Again, this access panel is not designed to support electronic equipment but for minimum weight and maximum weight and maximum access to the interior of the spacecraft. Round-head rivets join the skin to the edge channel assembly.

The skin consists of two separate sheets of type 2024-T4 aluminum, with an overlap joint between the two pieces. The lower and upper pieces are 0.04 and 0.03 inch thick, respectively. The two-piece skin provides maximum shear strength on the lower portion where it is required and preserves the minimum weight concept in the upper area. Both areas have blue epoxy paint on the side opposite the ribs.

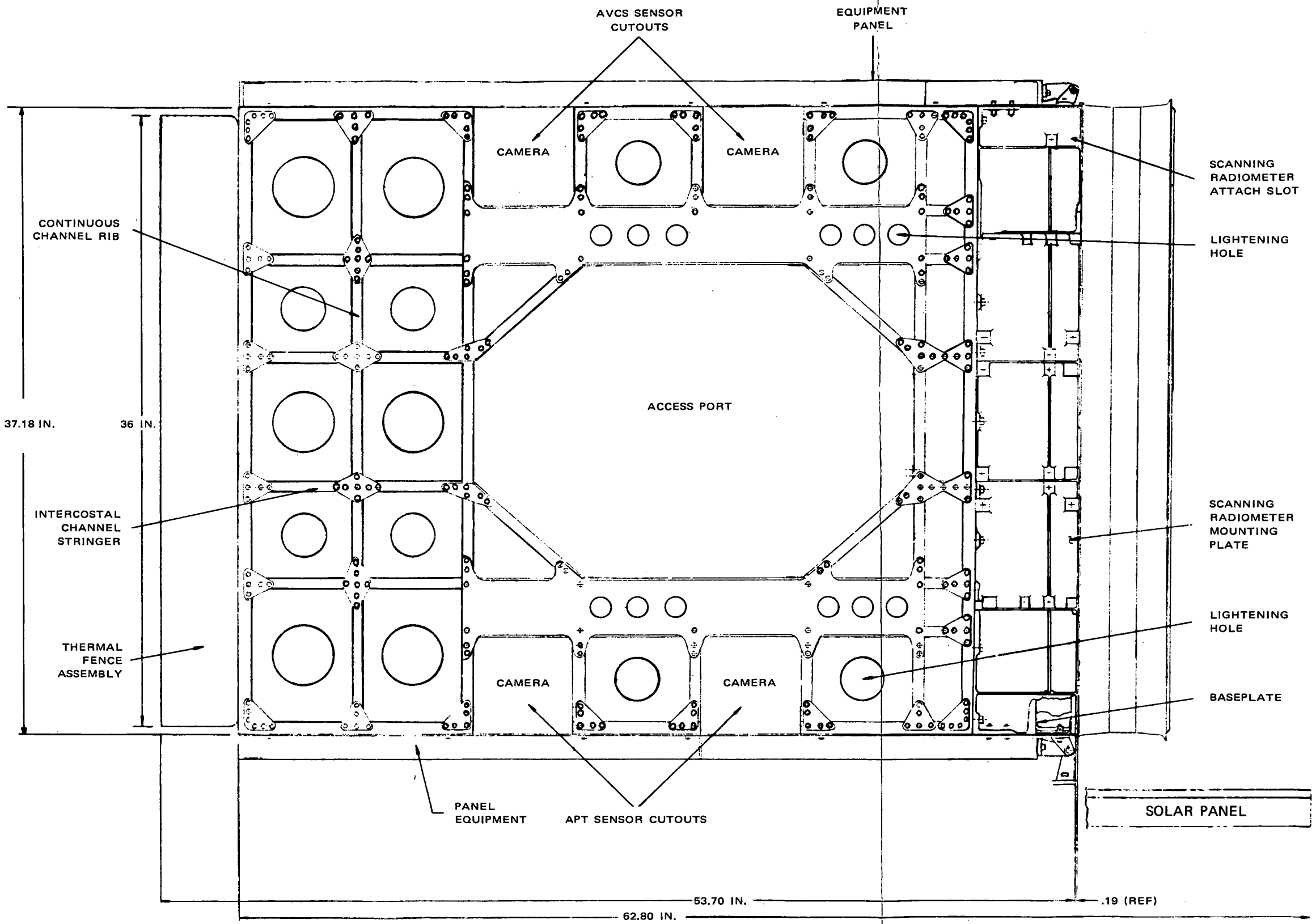


Figure 2-II-6. Earth-Oriented Access Panel

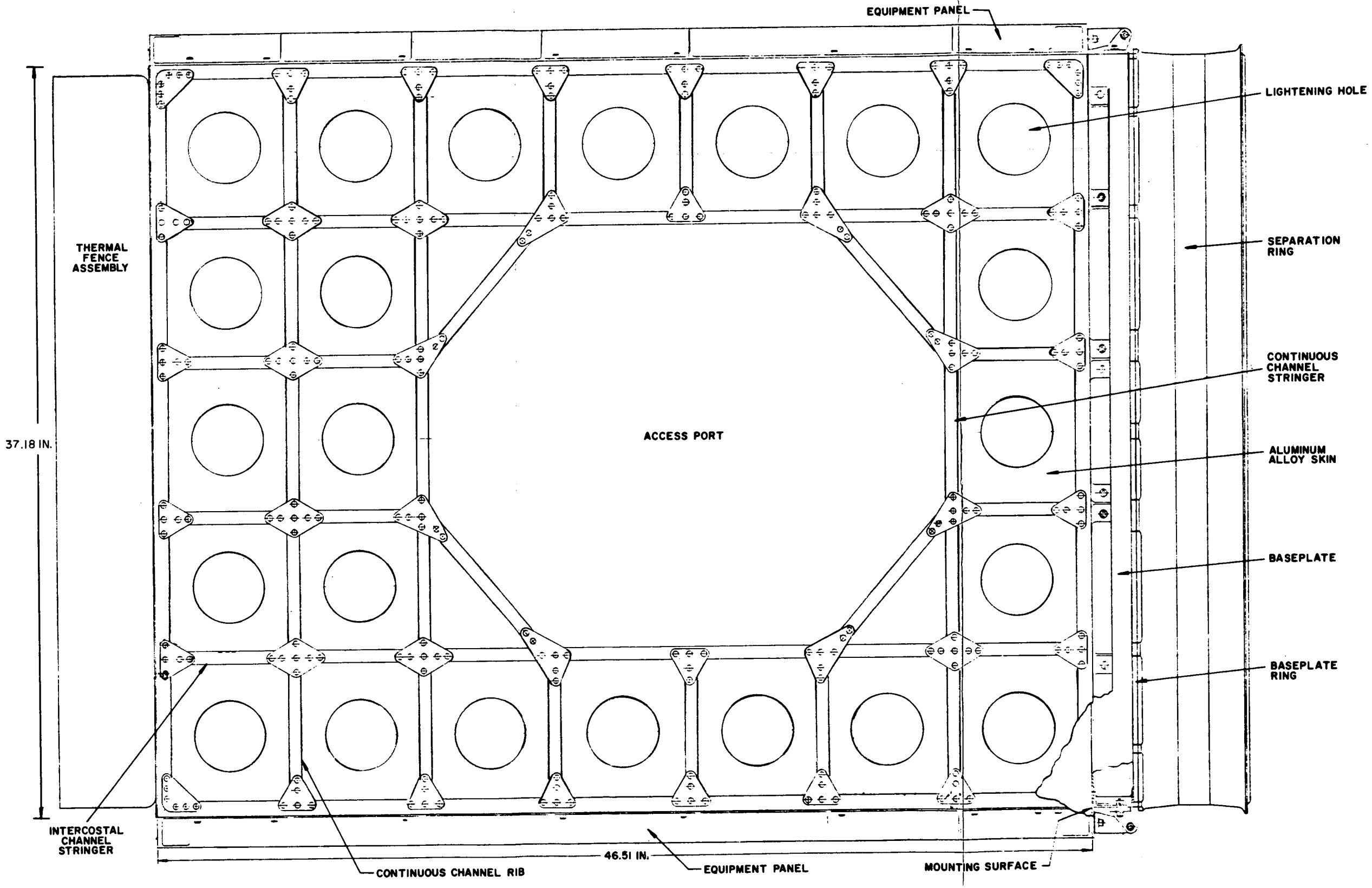


Figure 2-II-7. Anti-Earth Access Panel

Gussets of type 2024-T3 aluminum, either 0.04 or 0.08 inch thick, are used to provide maximum strength, were necessary, and minimum weight, where possible. As in the earth-oriented panel, lightening holes are provided in the skin where possible, to provide a maximum strength, minimum weight panel.

5. Scanning Radiometer Mounting Plate

The radiometer plate, shown in Figure 2-II-6, is different in form from the other assemblies of the structure. This plate, which is the mounting and support structure for the two scanning radiometers and the flat plate radiometer, was machined from type ZK60A-T5 magnesium. The plate is designed to have maximum strength and minimum weight, which are accomplished through the liberal use of machined ribs of minimum cross section.

6. Crossbrace Assembly

The crossbrace assembly (see Figure 2-II-8) is located at the top of the structure (panel 5). This assembly stabilizes the top of the spacecraft structure and supports the thermal fence.

The X-frame portion of the crossbrace was fabricated from 0.04-inch-thick type 7075-0 aluminum sheet, which was formed into a channel, then heat-treated to the T-6 condition. The shape of the beam is designed for uniform strength.

The corner fittings were machined from type 2024-T4 aluminum, with flanges to join them to the X-frame beams. The center of the X-frame, where the two channels intersect, is strengthened on the top and bottom with 0.08-inch-thick type 2024-T4 aluminum gussets, which are riveted to the channels. The upper plate has studs to fasten a shaft for checking runout of the spacecraft from the separation plane.

7. Thermal Fence

The configuration of the thermal fence was determined by the thermal requirements. The device consists basically of two concentric cups spun of 0.050-inch-thick type 6061-0 aluminum alloy, as illustrated in Figures 2-II-8 and 2-II-9. The outer cup is 36 inches in diameter and 4.81 inches high, while the inner cup is 14.7 inches in diameter and 1.94 inches high. The outer flat mounting ring is made from 0.050-inch-thick type 6061-T4 aluminum alloy with an inner diameter of 34 inches and an outer diameter of 40 inches. These three main members are riveted together with indium foil in the joints to provide thermal conduction between the members. The walls of the cups are finished in black to absorb heat; mirrors are supported above the flat surfaces

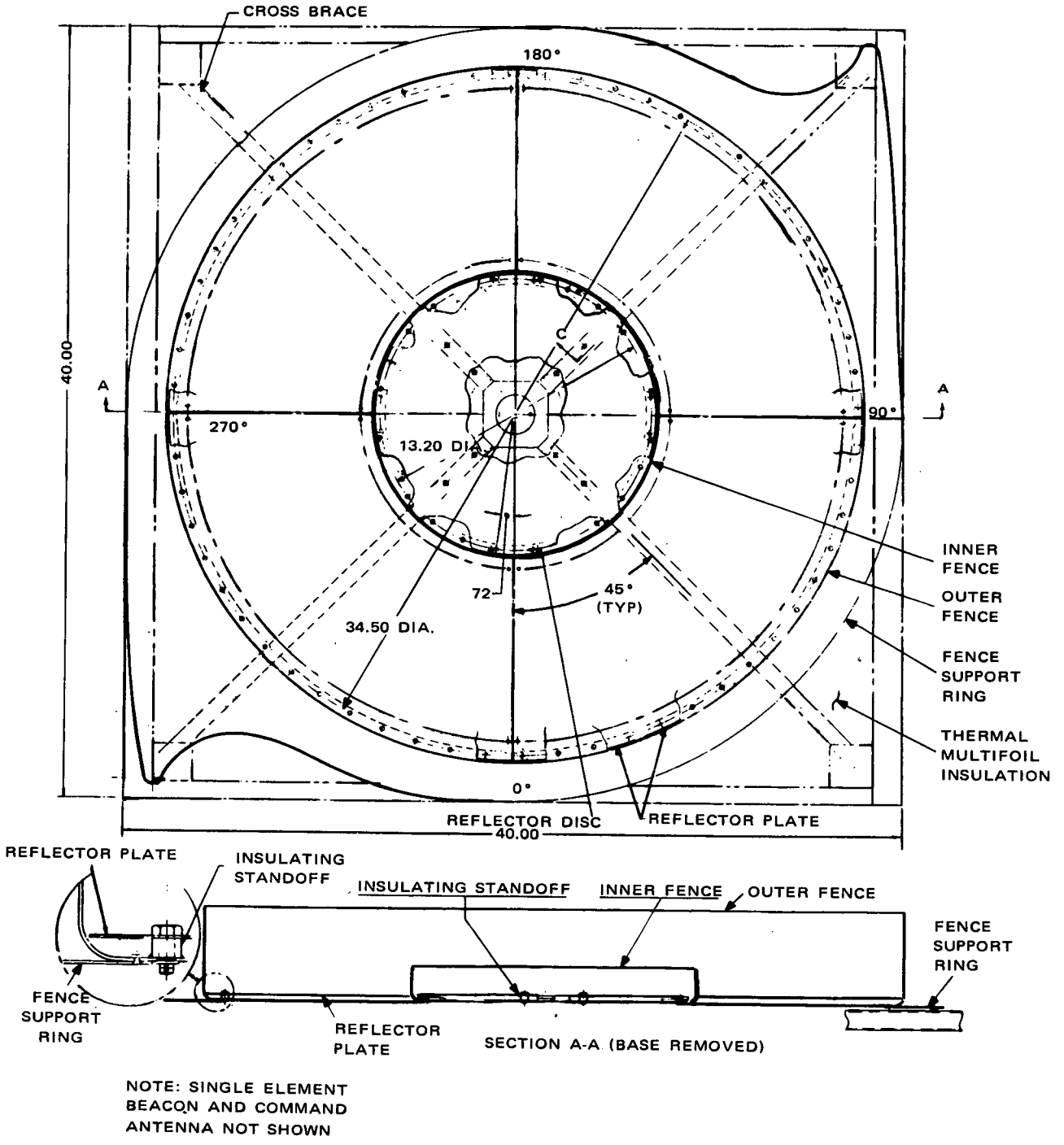


Figure 2-II-8. Top Assembly (Panel 5)

of the cups by epoxy glass standoff insulators. The mirrors, fabricated of 0.025-inch-thick Alcoa Alzak lighting sheet, Type I, with specular finish and H18 temper, are also insulated from the cups by thermal blankets. The assembled thermal fence is mounted to the crossbrace assembly by 24 standoff insulators. Details of this mounting are shown in Figure 2-II-9B.

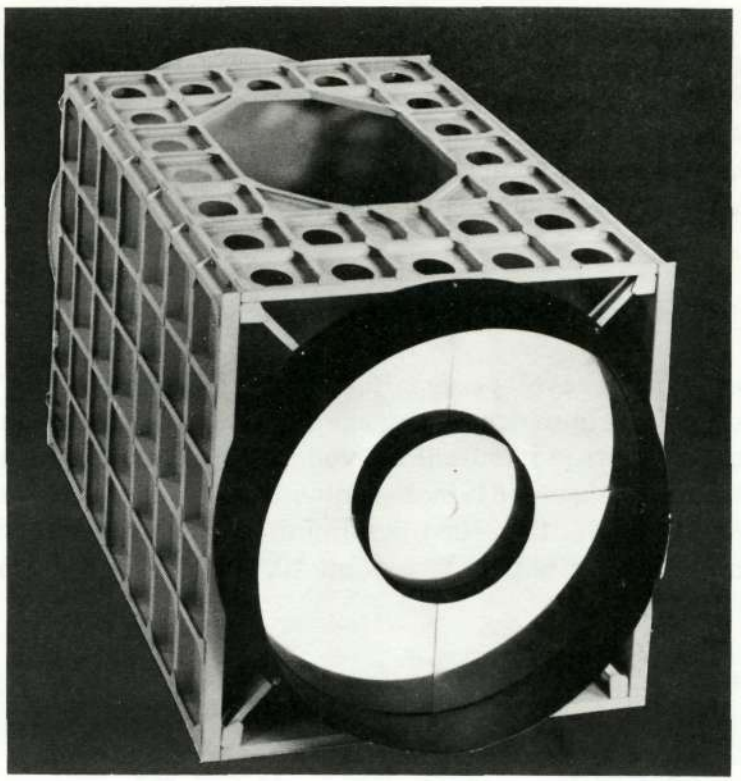
8. Solar Array Structure and Deployment Mechanism

The booster shroud envelope supplied by the McDonnell Douglas Aircraft Company afforded the basic overall measurements for the solar panels. The solar array consists of three identical curved solar panels 36.38 inches wide (measured on a chord of the 75.61-inch-radius circle described by the outer surface of the panel) and 65.15 inches maximum length from the upper machined channels of the structure to a point 10.9 inches below the separation plane (Figure 2-II-10).

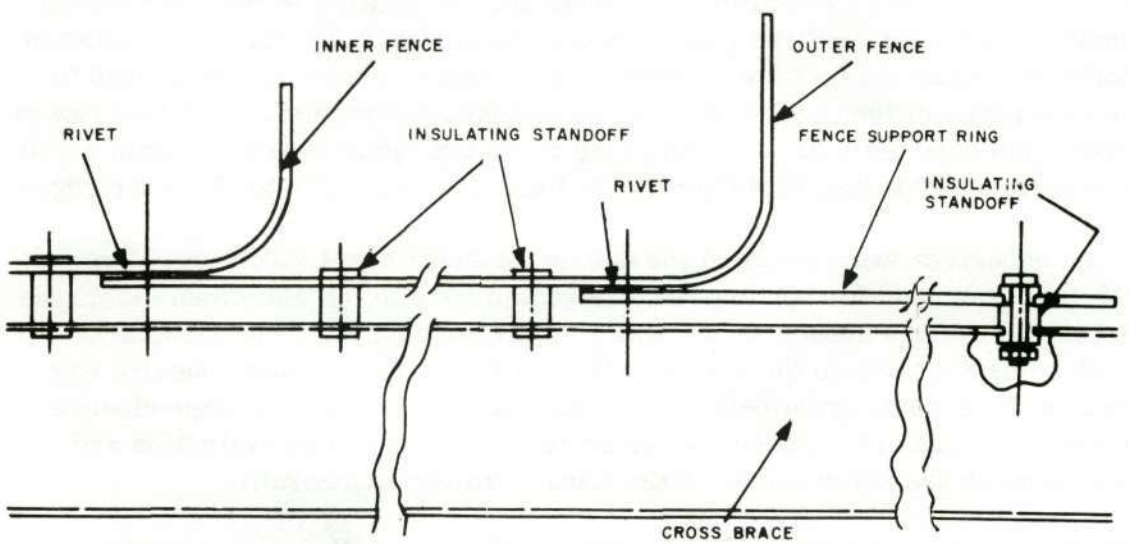
The solar panels are of a sandwich construction consisting of an aluminun honeycomb core 0.50 inch- by 0.001-inch thick (type 5052-H19), with 0.0047-inch-thick aluminum skins (type 5056-H-191). The panels have high torsional stiffness and high natural frequency combined with low inertia and low weight. The curved design provides a high section modulus plus the necessary clearance during separation. The convex side of each panel has one continuous surface for the mounting of solar cells. Bonded to the concave face are three reinforcing channels (hat sections) fabricated from 0.032-inch-thick type 2024-0 aluminum alloy, which is heat-treated to T4 condition after forming. In addition to their structural function, these hat sections provide mounting surfaces for the array isolation diodes and shunt dissipators. Formed "C"-channel members are bonded to the long edges of the panel and serve as a closeout structure. The last row of honeycomb core cells at each end of the panel are compressed to obtain a suitable surface for filling with type HT424 foam-type adhesive to close the edges.

Three adhesives were selected for use on the solar panel structure. Type FM-1000 was used for bonding the honeycomb core to the aluminum skin; type M-688/CH-16 was chosen as the adhesive for bonding the three structural reinforcing channels to the honeycomb skin; type HT-424 foam adhesive was used as the bonding agent between the honeycomb core and the edge-closure structural members. These adhesives received a thorough evaluation and were used on the solar panels of the Lunar Orbiter spacecraft.

The three solar panels are attached to the spacecraft by a set of hinges at the top reinforcing channel of the rear (anti-earth) access panel and the two equipment mounting panels. This permits the solar panels to be stowed, in the launch configuration. A spring actuator, hydraulically damped (Figure 2-II-11), is attached to this same channel of each mounting panel to deploy the solar array from the stowed position to the operating position.

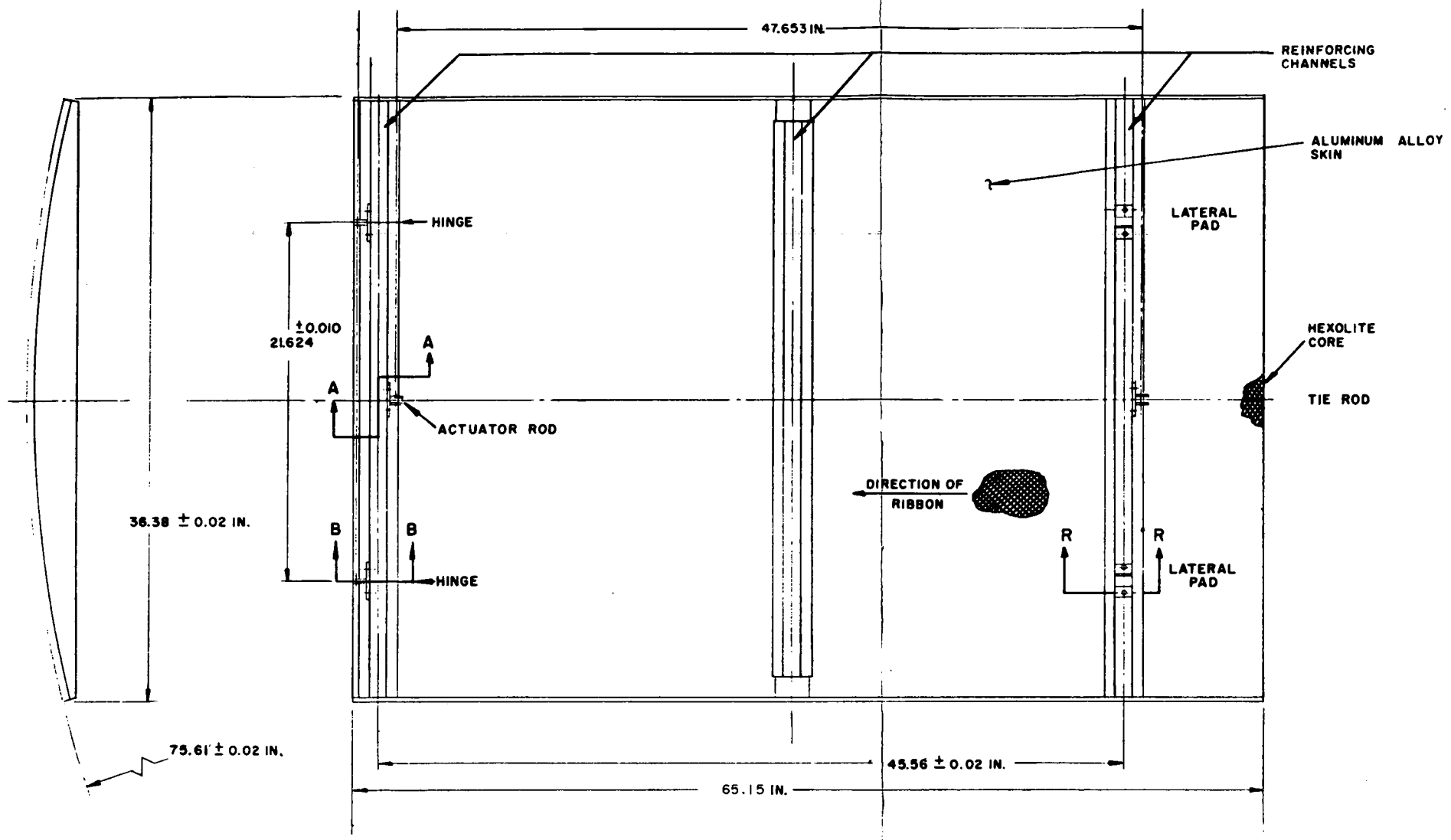


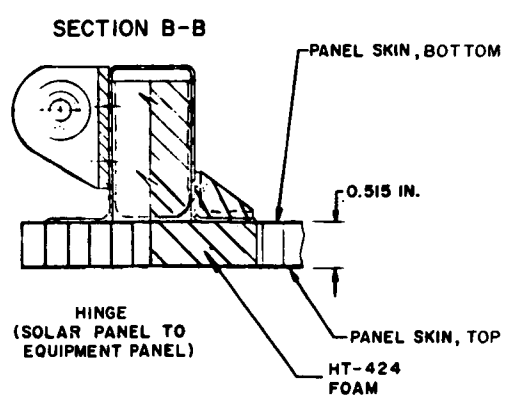
A. ITOS Structure Top View, Showing Thermal Fence Assembly

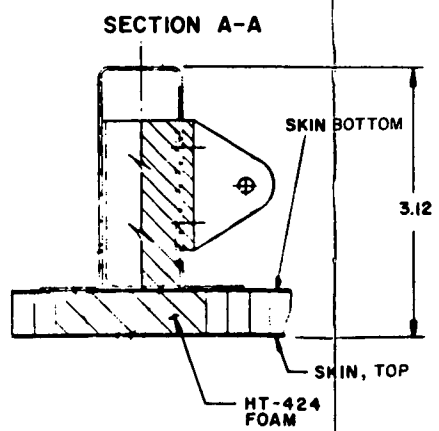


B. Thermal Fence Assembly Mounting Technique, Detailed

Figure 2-II-9. Thermal Fence Assembly Configuration







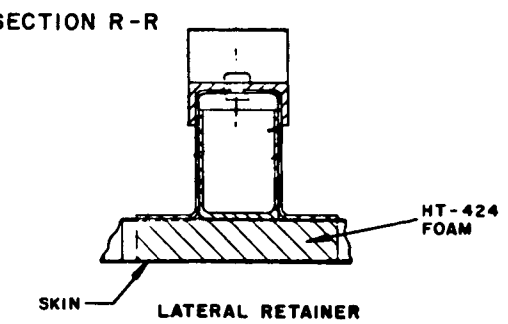


Figure 2-II-10. Solar Panel, Mechanical Configuration

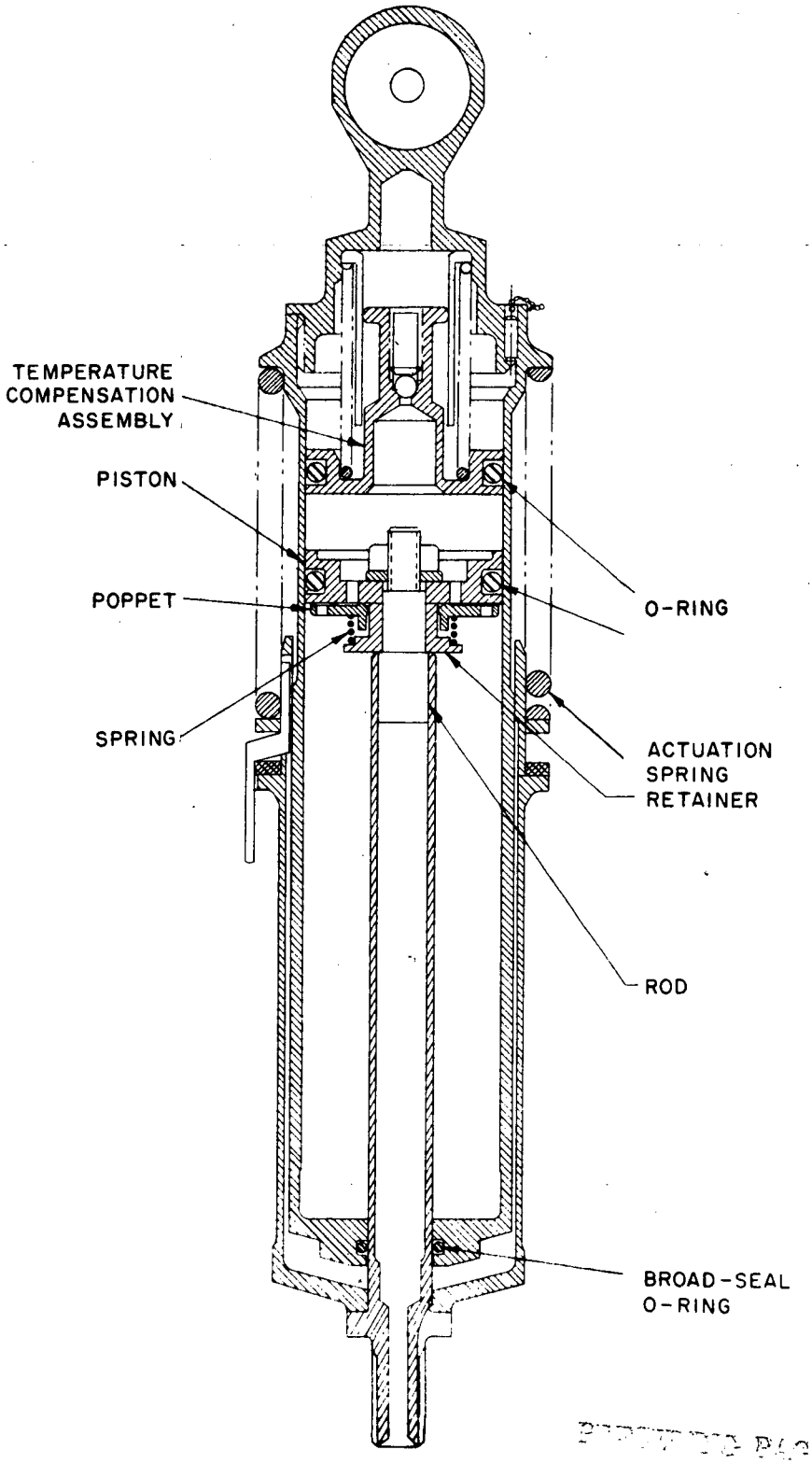


Figure 2-II-11. Solar Panel Hydraulic Actuator

Two secondary restraints are also employed. A pair of vibration snubbers located on the outer edges of the center reinforcing channel of each solar panel interface with screw jacks on the spacecraft structure. A set of pads on the outboard (bottom) reinforcing channel of the solar panels restrain the lateral movement of the solar panels and also interface with the spacecraft structure through jacks. One of the pads has the jacks so angled from a line normal to the panel-reinforcing channel and the spacecraft structure that the intersections of the lines of force of the two jacks meet at a point within the structure. The other pad has a jack normal to the rib to provide restraint to inward motion of the panel. This produces a two-directional stabilizing effect upon the panels; the panels are stabilized in the third direction by the hinges and hinge pins.

Two additional interfaces, associated with the actuating mechanism, exist between the solar panels and the spacecraft structure. A clevis fitting to accept the deployment actuator is located in the center of the top reinforcing channel of the structure. A restraining link is attached to a clevis fitting on the lower reinforcing channel through a pin-puller mechanism. This link consists of a turnbuckle link fastened by a bolt at one end to the solar panel and at the other to two pyrotechnic pin pullers on the spacecraft structure.

In operation, either pin puller (See Figure 2-II-12) releases the lower edge of the solar panel on ground command and the deployment actuator rotates the solar panel 90 degrees upward to its deployed position (see Figure 2-II-13). An end-of-stroke shouldered piston stop provides the 90-degree positioning.

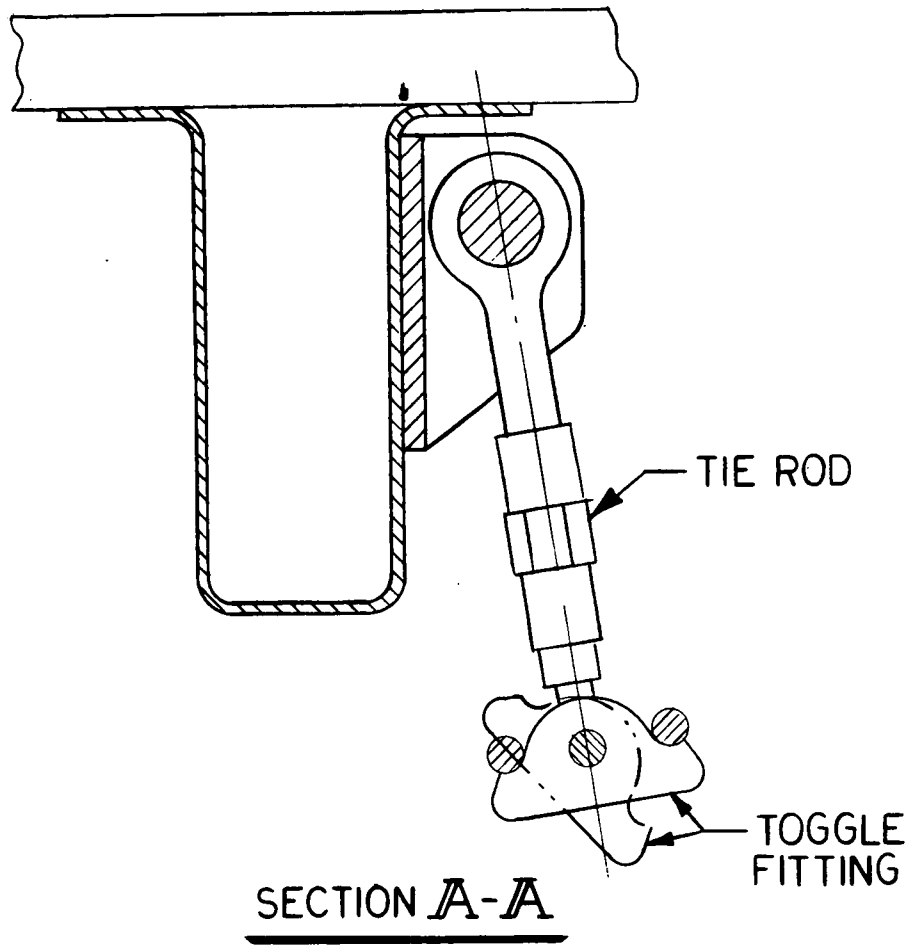
A hydraulically dampered actuator develops 158 pounds of axial force at the beginning of the panel deployment and 30 pounds at the end of the stroke.

All rotating interfaces between the solar panels, spacecraft structure panels, and deployment mechanisms are through Teflon-lined spherical bearings, permitting up to 10 degrees of misalignment between the solar panel and its interfaces.

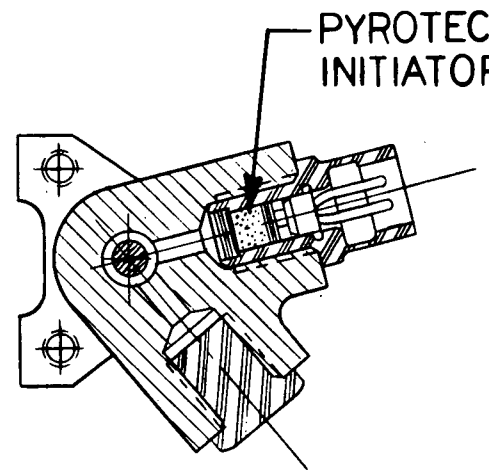
9. Momentum and Attitude Control Coils

The momentum coil was fastened to the ribs of one of the equipment panels beneath the thermal blanket and the attitude control coil was mounted on the separation ring attached to the baseplate. The concepts used in mechanical design of the coils are identical, although the finished sizes and shapes differed due to specific size, position, and electrical requirements.

Each coil was wound within a preformed, epoxy-impregnated, glass-cloth channel having the specified coil dimensions. As each layer of wire was completed, a coating of epoxy resin was brushed over the layer; this process continues until the entire winding operation was completed. The resulting assembly is a coil (or coils) embedded in a continuous epoxy matrix, with the glass channel forming an integral protective shell on three sides of the coil.



SECTION A-A



SECTION B-B

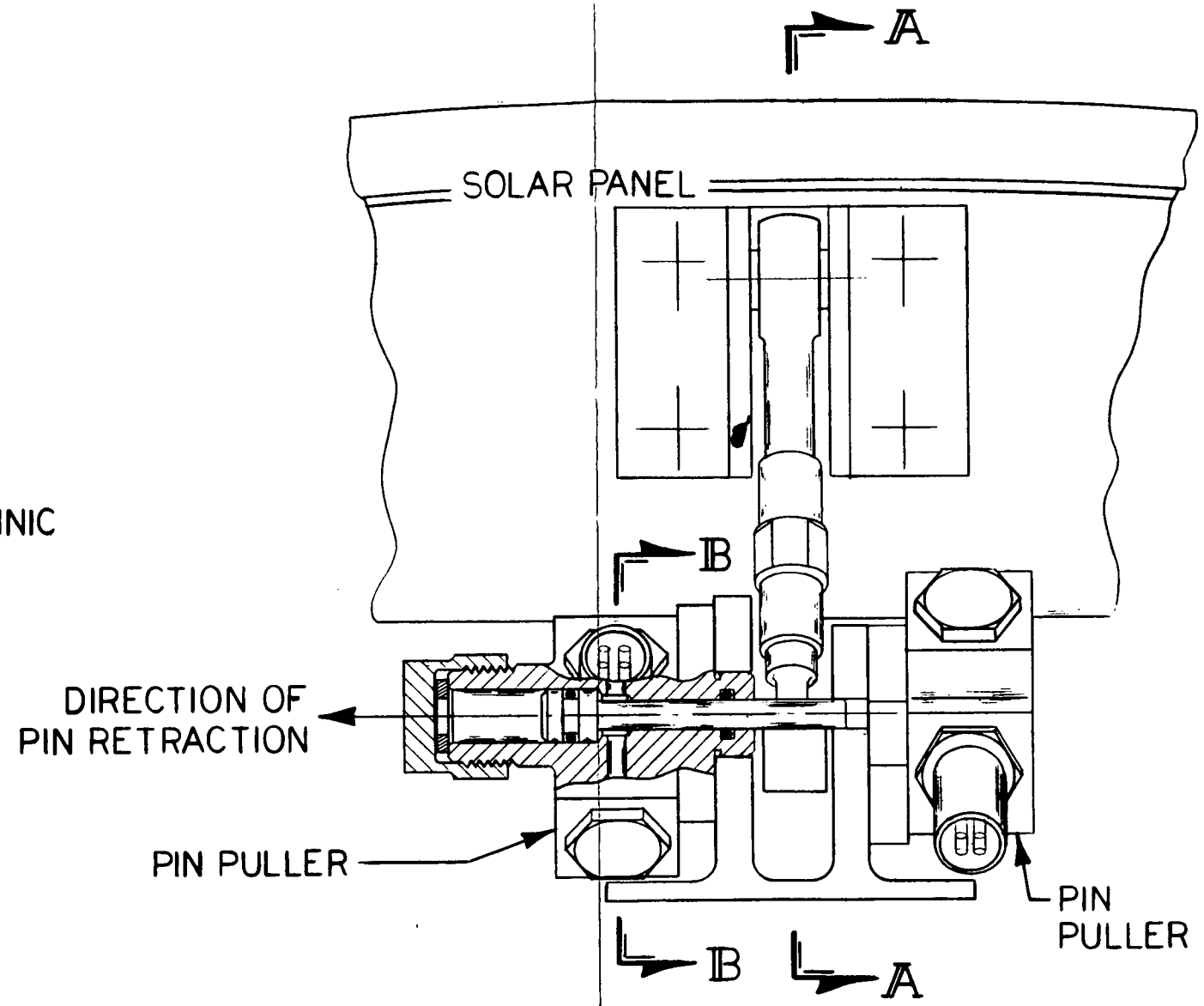


Figure 2-II-12. Solar Panel Retention and Release Mechanism

FOLDOUT FRAME 1

FOLDOUT FRAME 2

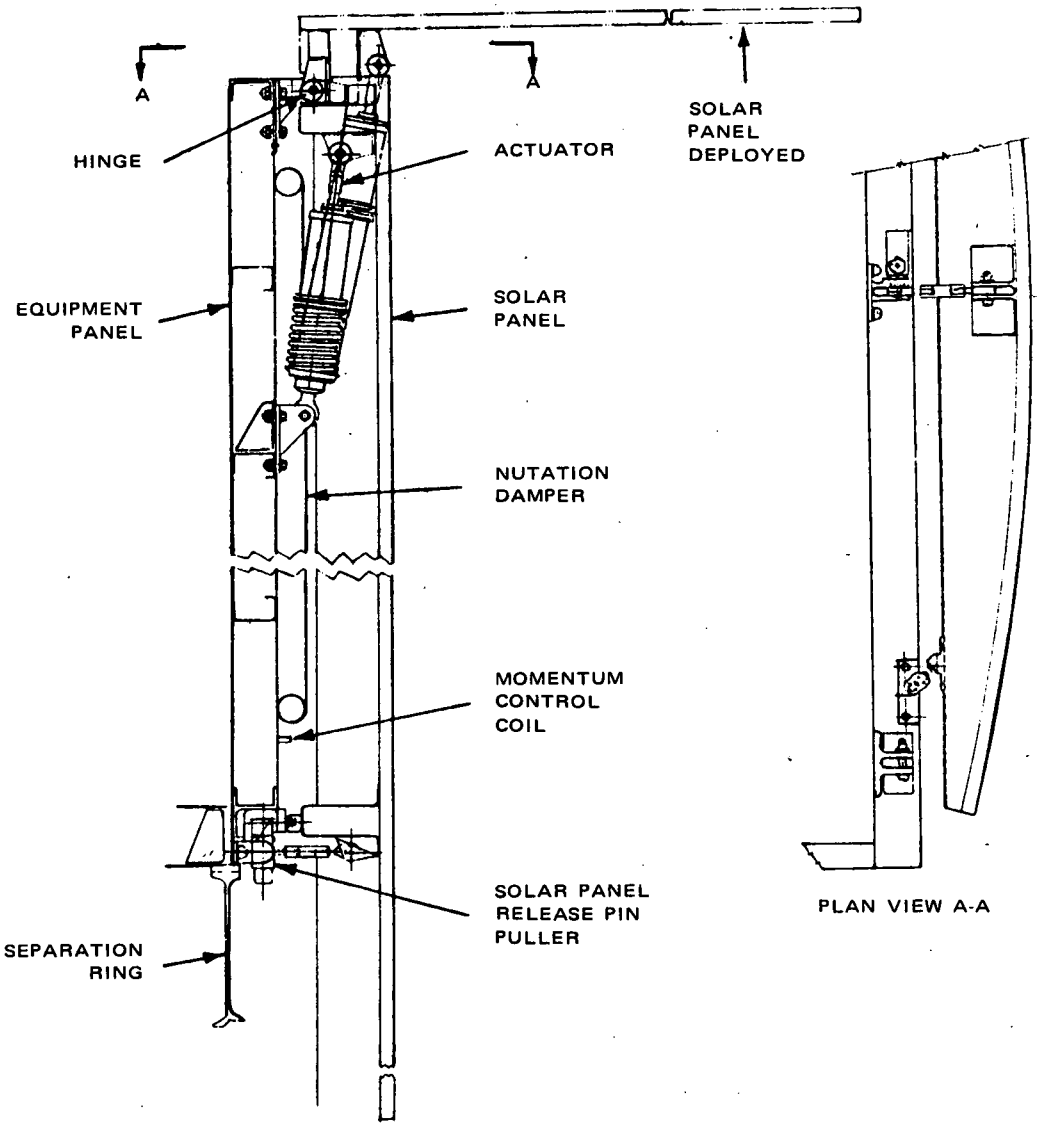


Figure 2-II-13. Deployment of Solar Panel

The free ends of the coil windings were soldered to connections on an epoxy terminal board which is bonded to the coil assembly. All such exposed connections were epoxy-coated to prevent subsequent damage to the coil wires. A second set of terminals was provided for external spacecraft connection.

10. Nutation Dampers

The two nutation dampers are fastened to the outside of each equipment panel, beneath the thermal blanket. The dampers were fabricated from type 5052-0 aluminum alloy drawn tubing having a 1.00-inch outside diameter and 0.035-inch wall thickness. The assembly approximates a rectangle with rounded corners, and has a cross fitting located in the center of one of the shorter sides. A bellows mechanism at one end of the fitting maintains fluid pressure within the tubing to prevent formation of vapor bubbles. At the opposite end of the fitting is a filling post. Prior to filling the assembled tubing with silicone fluid, all joints were leak tested using helium and a mass spectrometer.

11. Active Thermal Controller (ATC)

The ATC provides thermal control by varying the effective area of the radiative surface on the equipment panels. Two louvers are located on each equipment panel. Each louver is driven by a thermal actuator sensor that responds to the spacecraft temperature to maintain the equipment panels within given temperature limits.

a. ACTUATOR SENSOR UNIT

This unit is the sensing and actuating device that opens or closes the louver over the radiative surface of the equipment panel. The actuator sensor operates on the principle of controlled thermal expansion of a confined fluid. Its output is a linear motion as a function of the sensed temperature. Figure 2-II-14 is a cross section of the assembly. The actuator sensor characteristics are listed in Table 2-II-1.

The unit comprises two parts, the drive system and the adjust-relief system. The two systems are hydraulically coupled to each reservoir.

The drive system consists of a drive bellows, drive spring, and drive piston. The piston has two Teflon piston rings, which also act as bearings. The piston is not keyed to the housing, but can rotate, allowing its threaded end to be adjusted in the linkage without disassembly. The drive bellows is an accurate, electrodeposited, nickel element with a precise spring rate, stroke, and pressure capability. To package the device in the minimum space, the

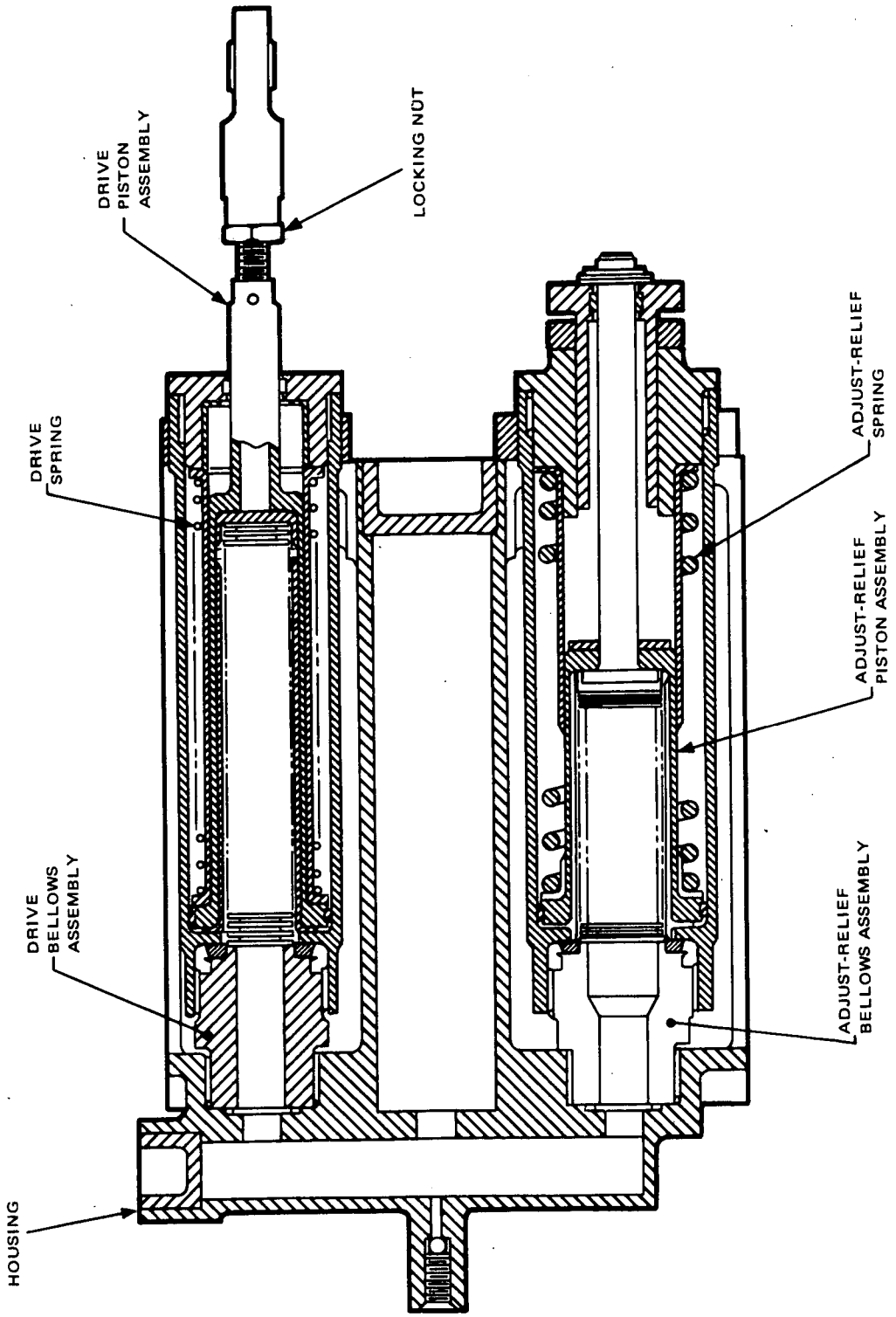


Figure 2-II-14. ATC Actuator Sensor Unit

TABLE 2-II-1. ACTUATOR SENSOR CHARACTERISTICS

Item	Characteristic
Operating Range	20° C
Range Selection	Any 20° C range between -10° and +55° C
Range Setting: (a) 6° C	Louver closed
(b) 26° C	Louver open
Overtemperature Relief (regardless of selected range)	+60° C
Period of Reliable Operation	1-year space life (equiv. to 5×10^3 cycles)
Stroke	0.6 inch
Force Output	4 to 7 pounds
Linearity	±2 percent of full stroke
Sensitivity	0.03 linear inch per° C
Weight	2 pounds

bellows is used in both the compressed and extended modes. The drive spring is sized so that it can completely compress the bellows and also supply force to the external linkage. As the temperature increases, the fluid expands, forces the bellows outward against the drive spring, and moves the piston outward. As the temperature decreases, the fluid contracts and the drive spring forces the bellows to contract; the excess force of the drive spring supplies the external driving force. The preload in the drive spring is such that the minimum external drive force of the drive spring and bellows combination is never less than 4 pounds, available when the piston is full in. As the fluid expands, the available force increases until it reaches 7 pounds at the maximum outward position of the piston. Since the drive necessary for the louver is approximately 1 pound, an adequate force margin is maintained throughout the stroke of the piston.

The adjust-relief system includes a bellows, spring, and piston, quite similar to the drive system. In this case, the piston rod is attached to the bellows and an adjusting nut that positions it relative to the housing. This arrangement fulfills two functions: the adjustment of the operating range and the provision of overtemperature relief. The combined spring rate is sized for compatibility with that of the drive system. The relief system is so designed that the minimum pressure required to move it is greater than the maximum pressure developed in the drive system. Incorporated in the adjust-relief system is an adjustment with a 20°C nominal range that can be adjusted anywhere between -10° to +55°C. This adjustment is made by turning the adjusting nut to increase or decrease the internal volume for the fluid. The adjusted range setting for the ITOS mission is such that the louvers are fully closed at 6°C and open fully at 26°C.

The unit is sealed and the absolute volume of a fluid is constant at a given temperature. The fluid will not exert any force until it is expanded by an increase in temperature to fill the selected volume. Additional incremental increases in temperature cause the expanding fluid to impart force (and motion) to the drive piston. This continues until the drive piston reaches the end of its stroke. At this point, increases in temperature beyond the selected range cause the adjust-relief shaft to move outward so that the internal pressure caused by the overtemperature does not cause failure of the bellows.

b. LOUVER AND HINGE ASSEMBLY

The louver is a honeycomb structure 34-1/4 by 4-3/8 inches with hinges bonded at each end of its long edges. The assembly is illustrated in Figure 2-II-15, together with the drive linkage and the actuator sensor unit.

The thermal requirements of the spacecraft dictated that the radiation surfaces of the equipment panels be exposed during the injection mode. It was also required that the ATC louver system must function normally when the spacecraft is in the operating mode.

For the first condition, the louvers must be rotated 180 degrees from the completely closed position to a folded back condition when the solar panels are folded. Two nylon hold-downs on the solar panel hold the louver open and release it during the solar panel deployment. The released louver should then assume a position required by the particular temperature of the spacecraft as determined by the position of the output shaft of the actuator sensor unit. This is accomplished by a spring-linkage system.

The actuator sensor is connected through a linkage system to the lower hinge. The linkage, which transforms the linear motion of the actuator unit to a rotary motion, consists of a drag link, a bell crank, a shaft, and two collars with fingers to engage a torsion spring. The shaft provides a bearing surface for

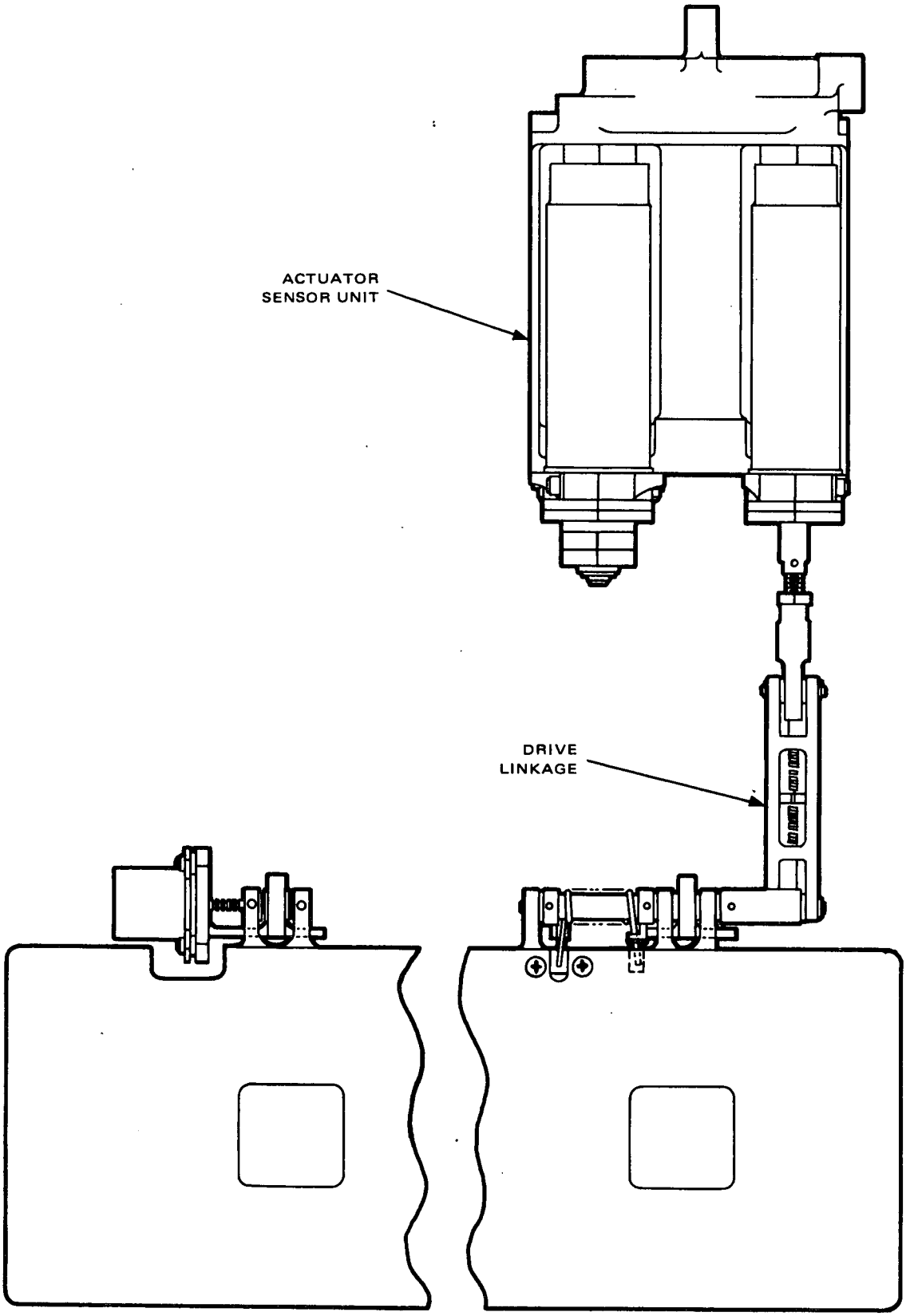


Figure 2-II-15. ATC Louver and Hinge Assembly

the louver hinge and acts as a drive member for the torsion spring, which has protruding ends. The bell crank and the two collars are pinned to the shaft, which is driven by the drag link connected to the output shaft of the actuator sensor unit. The fingers of the collars engage the protruding ends of the torsion spring. The spring is so positioned that the force output of the actuator is transmitted to the louver through the torsion force of the spring, which is limited by the collar fingers. When the louver if folded back to the launch position, the spring tends to return it to a position against the finger of the collar, so that it will then assume a position compatible with the temperature of the actuator sensor unit. A fast decaying vibration of the louver takes place but the final position of the louver is determined by the position of the actuator sensor output shaft. The pin of the second hinge is connected to a bellows, which is a coupler to a potentiometer. The louver is so connected to the hinge pin that the position of the louver is sensed by the potentiometer for use in telemetering this information. An anti-backlash spring is incorporated into the louver drive linkage which eliminates buildup of mechanical clearance tolerances and inaccuracies of louver position versus temperature.

The louver is 1/4 inch thick, constructed of 3/8-by 0.0016-inch type 5052-H39 honeycomb aluminum alloy core, with skins of 0.0037-inch-thick aluminum alloy. The same adhesive system was used for the louvers as for the solar panels. FM-1000 was used to bond the skins to the core; the edges were closed off with HT424 foamed adhesive; bumper areas were reinforced internally by filling with HT424 foamed adhesive; bumper plates of 0.14-inch-thick 5052-H34 aluminum alloy were bonded on the skin over the bumper areas with M688 A and B adhesive.

A system of hinge clearance was devised to provide for the temperature-differential expansion between the louvers and the equipment panels; this same system was used on the solar panel hinges. The clearance between the tangs on one set of hinges was kept close so that free rotational motion was provided but lateral motion was inhibited; this hinge assembly was designed to sustain the total lateral load of the louver. The clearance between the tangs of the other hinge was large enough so that contact would not occur at the extremes of differential temperature between the two structures, allowing for the expansion and contraction of the louver without impeding its rotational capability. As in the solar panels, all rotating interfaces are through Teflon-lined spherical bearings, allowing for misalignment of up to 10 degrees without any appreciable binding.

12. Accelerometer Assembly

Modification No. 16 to Contract NAS 5-10306 added an accelerometer assembly to the ITOS series of spacecraft, with the TIROS M spacecraft configured to read out the lateral (x-x and y-y) G-level of vibration response, during the early portions of the launch phase, while telemetry contact is maintained at the Western Test Range.

The complete accelerometer assembly consists of an accelerometer control unit (ACU) in addition to the accelerometer assembly. The mounting bracket of the accelerometer assembly has provision for mounting three mutually perpendicular accelerometers to read out the launch vibration environment in all three axes. Because of the limitation of only two beacon SCO's, the first three of the ITOS series are configured to read out in the following orthogonal spacecraft axes:

TIROS M	x-x and y-y
ITOS A	x-x and z-z
ITOS B	y-y and z-z

The same pattern is repeated on follow-on flight spacecraft. The functional and electrical operation of the accelerometer control unit and the interconnections with the telemetry link are given in paragraph C.3.b of Section VII.

E. INTERIOR ELECTRONICS ARRANGEMENT

1. General

The spacecraft structure is divided into six panels or planes as illustrated in Figure 2-II-1. The four sides of the structure attached to the baseplate are identified as follows. The earth-viewing panels, consisting of an access panel and a radiometer mounting panel, is designated as panel 1. The next panel clockwise is panel 2, the APT equipment panel. The next or anti-earth access panel is panel 3, and the remaining equipment panel is the AVCS panel, panel 4. The plane of the crossbrace and thermal fence at the top of the structure is designated as panel 5.

The equipment is laid out to maintain the module concept of the APT and AVCS subsystems. The APT system and the two SR recorders are mounted on panel 2, while the AVCS is mounted on panel 4. With the exception of the SR and solar proton sensors, which must be on the baseplate for functional reasons, it has been possible to reserve the baseplate area for bus functions such as power, attitude control, and command distribution functions. Since the equipment is on three panels, the harness wiring for the spacecraft is required to cross only two hinge lines.

The detailed layout of the equipment necessitated investigation of various factors so that appropriate placements could be accomplished. Harness runs had to be assigned to appropriate areas. Certain components, because of their thermal requirements, were isolated from each other to avoid thermal overload of a specific area of the structure; because of high thermal output, other components were located over a radiating area of the structure.

The positions of some RF components were restricted by lengths of RF cables, while other electronic components had to be close to associated sensors. Placement of the components was adjusted so that the mounting holes were not located in certain areas of the structure (jogs, dimples, and rib edges). Finally, it was required to minimize the number and types of underside brackets to support equipment. All of these adjustments had to be accomplished in such a manner that the spacecraft was dynamically and statically balanced.

2. Interior Electronics Arrangement of the Mechanical Test Model (MTM)

Configuration, weight, and placement of the mock-ups of the electronic boxes for the MTM was based on the component data as it existed on May 5, 1967. Since the data on the electronics was constantly being updated, it was decided to freeze the data and hopefully freeze the changes on the "blue boxes" at the start of the MTM placement study. Changes in the electronics boxes and in the system eventually caused the MTM balance data to differ slightly from the flight data. Since no layouts or detailed concepts of the harness existed at the time of the original calculations, estimates of the shapes, locations, and weights of the harness elements differed from those in the MTM spacecraft. Table 2-II-2 gives the balance weight and inertia data for the MTM spacecraft.

3. Interior Electronics Arrangement of the Flight Model Spacecraft

The interior electronics arrangement for the flight model spacecraft was performed and finalized later in the program when the electronic equipment data was more fully defined. The weight, balance, and inertia data for the TIROS M flight model spacecraft is given in Table 2-II-3.

F. DESIGN HISTORY TIMETABLE

The following history of the mechanical design of the spacecraft is a summary of the major events that occurred during the spacecraft design and fabrication program. The dates reported are, in many cases, the dates of the reporting periods in which the events occurred, covering a time period of approximately one week. This history begins at the conclusion of the major tradeoff studies, after the basic sheet metal structure with shear panels had been decided upon.

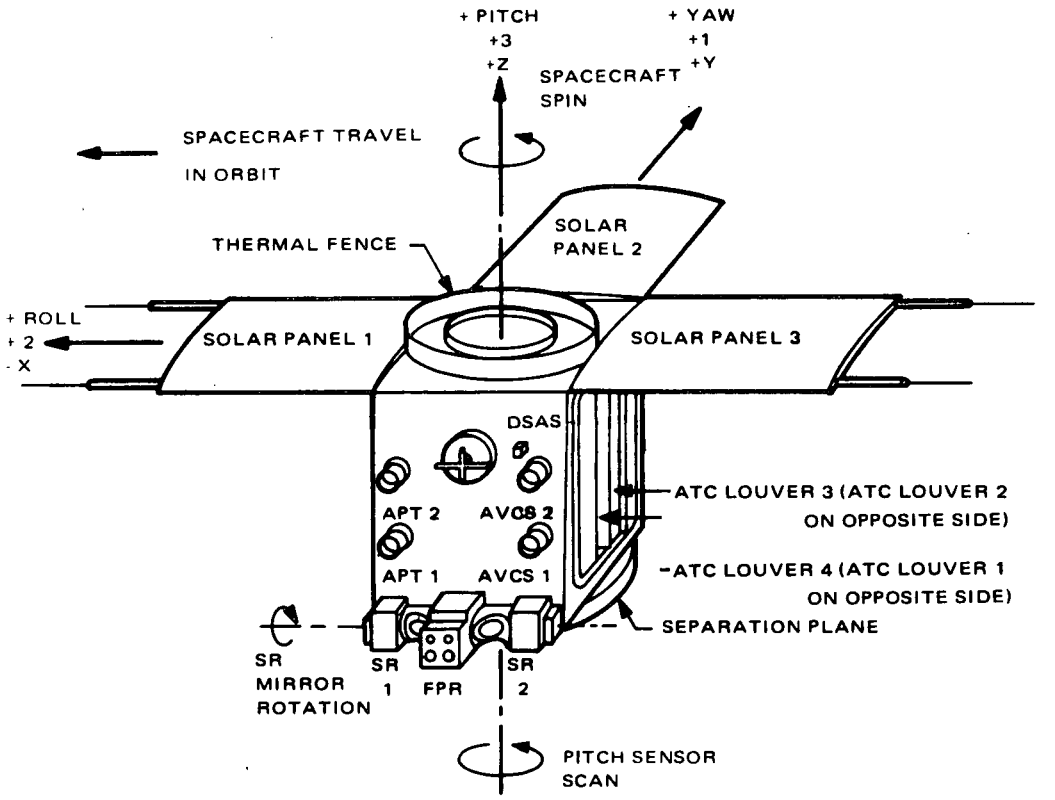


Figure 2-II-16. Spacecraft Alignment Reference Axes

The detail design of the basic sheet metal structure was begun on November 1, 1966. On November 9, 1966, a curved or segmented solar panel concept was first discussed when interference between the Douglas Aircraft Company* (DAC) adapter and the extended flat solar panels was discovered. On November 15, 1966, information was received on the new, improved Delta fairing, which resulted in moving the closure and deployment mechanism from the forward end of the fairing to the aft end. More information was requested on the FW-4 and TE-364 launch vehicle third stage attach fitting, constraints envelope, and radiometer configurations. Additional interface information about the DAC adapter envelope was received on November 21, 1966, and more information was requested about the DAC separation spring pads.

Tradeoff studies on the thermal fence fabrication technique were concluded on November 23, 1966; spun cups were selected for the construction. All FW-4 compatibility work was terminated.

The curved solar panels were approved on December 2, 1966. Preliminary design layout drawings of the major structural components were submitted to NASA for their information on December 15, 1966.

*Now McDonnell Douglas Astronautics Corporation (MDAC).

TABLE 2-II-2. BALANCE WEIGHT AND INERTIA DATA FOR MTM

	Measured Data		
	Launch	Orbit	Units
Weight*	656.37	652.41	lb
I zz	639.57	982.81	lb-in-sec^2
I xx	754.24	967.91	lb-in-sec^2
I yy	829.44	1129.32	lb-in-sec^2
I max	829.92	1129.54	lb-in-sec^2
P xy	5.95	5.96	lb-in-sec^2
xy**	4.5	2.2	Degrees
I Ratio	1.30	1.15	
Z Bar‡	22.26	22.34	Inches

* Dummy growth boxes removed before this test.
** Counterclockwise from Y axis viewing aft.
‡ Above separation plane.

On December 19, 1966, interference was discovered between the momentum flywheel mirror and the arming clearance on the TE-364 engine. This minor discrepancy was later resolved by reducing the clearance envelope. Due to the difficulty of satisfying the thermal, dynamic, and stress requirements, concepts other than that of mounting the despin mechanism on the thermal fence were investigated on December 27, 1966. An investigation of a 4-, 8-, and 12-support-post design was initiated. On December 29, 1966, a 4-post support for the despin mechanism was proposed as the design for the spacecraft.

On January 12, 1967, preliminary layouts of the active thermal control (ATC) and the nutation dampers were completed. On January 19, 1967, the second phase of the spacecraft structure was begun; the weight was to be reduced (from a reported weight of 672.3 pounds on January 9, 1967), the thermal requirements were to be given greater consideration, and the design was to be simplified.

TABLE 2-II-3. MECHANICAL AND PHYSICAL PARAMETERS

Parameter	Launch Configuration (Panels Folded)	Operational Configuration (Panels Deployed)
Spacecraft Weight	682.02 lb	682.02 lb
Moment-of-Inertia		
(a) About Yaw Axis I_{11}	849.46 lb-in-sec^2	1295.04 lb-in-sec^2
(b) About Roll Axis I_{22}	783.42 lb-in-sec^2	1020.65 lb-in-sec^2
(c) About Spin (Pitch) Axis I_{33}	682.09 lb-in-sec^2	1145.54 lb-in-sec^2
(d) About Roll-Yaw Plane		
I_{max}	849.64 lb-in-sec^2	--
I_{min}	783.24 lb-in-sec^2	--
(e) Location of I_{max} (Positive angles measured clockwise from earth side (-1) when viewed from above the baseplate)	183 degrees	--
(f) Inertia Ratio I_{max}/I_{33}	1.25	--
Product-of-Inertia		
(a) In Yaw-Roll Plane I_{12}	+3.46 lb-in-sec^2	+3.74 lb-in-sec^2
(b) In Yaw-Pitch Plane I_{13}	I_{13} and I_{23} assumed equal to zero for dynamically balanced spacecraft	+79.88 lb-in-sec^2
(c) In Roll-Pitch Plane I_{23}		-10.92 lb-in-sec^2
NOTE: Orbital moments-and-products-of-inertia are values about a set of coordinate axes which have been shifted parallel from the initial launch coordinates.		
Center of Gravity $\bar{z}$ (Above Separation Plane)	21.94 inches	24.85 inches
Dynamic Balance Residual Dynamic Imbalance (Maximum)	192 lb-in^2	See I_{12}, I_{13}, and I_{23} above.
Static Balance Residual Static Imbalance (Maximum)	15.5 lb-in	$\Delta\bar{y}$ = +0.859 inch $\Delta\bar{x}$ = -0.063 inch
NOTE: Dynamic balance test was performed on October 2, 1969. Moment-of-inertia test was performed on October 4, 1969.		

A meeting was held with personnel of the Applied Physics Laboratory (APL) of the Johns Hopkins University on January 31, 1967, to explore the configuration of the solar proton monitor.

On February 2, 1967, the DAC revised interface drawings were studied and a number of areas of conflict were discovered. Detailed layouts of the redesigned structure were completed on February 10, 1967 and a bidders' conference was held with several vendors on the spacecraft structure on February 15, 1967.

The drawings and specification for the solar panels were completed on February 16, 1967. Information was not available at that time on the mounting of the APT antenna. Feasibility studies were started on the ATC, including two sets of bifold louvers on each equipment panel. The specification was completed for the procurement of the solar panel deployment actuator.

On February 17, 1967, inconsistencies between the strength of the DAC "V"-clamp on the attach fitting and the requirements imposed on the structure were reported to NASA. On February 23, 1967, the solar panel drawings were submitted to several vendors for bids. On March 10, 1967, five vendors submitted quotes on the structure.

On March 17, 1967, a compatibility meeting was held at DAC to discuss interface problems; new information was exchanged. The major structure design review was held on March 23, 1967. A decision was made to again locate the despin mechanism on the thermal fence.

On March 30, 1967, the detail drawings for the breadboard ATC were released for fabrication. New quotes were received from vendors on the revised structure on April 3, 1967. Revised data was received from the antenna skill group on April 6, 1967 on the APT antenna; redesign of the solar panel was started.

On April 11, 1967, a preliminary procurement specification was completed for the pin puller and was submitted to vendors for bids. A vendor was selected for the structure on April 13, 1967. Work on the ATC louvers was delayed until the new thermal requirements were ascertained. On April 17, 1967, the specification for the solar panel actuator was released for flight procurement. A meeting was held with APL personnel about the solar proton monitor and information was exchanged.

Preliminary studies of the placement of the components on the MTM were completed on May 11, 1967. Also completed was the solar panel design. Conceptual design reviews were conducted for the despin mechanism and ATC actuator sensor designs.

On May 12, 1967, new data was received from the thermal engineering group concerning the area required under the ATC louvers. A new louver design

was initiated, the scanning radiometer selection was changed, and an investigation on the structure was started to assess the changes required for the new configuration.

On May 16, 1967, the solar proton monitor outline drawing was completed and submitted to APL for approval. The "black box" information for the MTM was frozen on May 18, 1967, and the placement studies were continued using this information. On May 25, 1967, a major design review was conducted on the solar panel, pin puller, deployment actuator, and separation ring. New information was received from the manufacturer about the scanning radiometer. The spacecraft weight was reported as 673.5 pounds.

The layout drawings of the ATC louvers were completed on June 1, 1967 and submitted to vendors for quotes. The redesign of the radiometer plate was completed. On June 6, 1967, the vendor was selected for the solar panel structure.

The vendor was selected for the nutation damper valve on June 14, 1967, and the vendor was selected for the ATC louvers on June 28, 1967. On July 5, 1967, parts were received from the vendor for the breadboard ATC actuator sensor and assembly was begun.

On July 12, 1967, the balance and placement study of the MTM spacecraft was completed. A major design review of the attitude control system hardware was held on July 13, 1967. The final stress report on the bus structure was held on July 18, 1967. On July 20, 1967, a meeting was held with personnel of the University of Wisconsin concerning the flat plate radiometer.

On July 26, 1967, the drawings for the underside brackets for the MTM and thermal test model (TTM) were completed. The "debugged" breadboard ATC actuator sensor test cycle was started on August 6, 1967.

On August 11, 1967, the design of the ATC actuator sensor was completed. The basic structure for the MTM was completed without the underside brackets. On August 16, 1967, the first destructive test model of the solar panel was completed. The design of the ATC actuator sensor was completed and released for fabrication.

A fit-check meeting was held on August 24, 1967 to check the compatibility of the spacecraft separation ring with the DAC attach fitting. No problems were encountered.

The pin puller vendor started design verification tests on August 25, 1967. The major design review of the ATC was also conducted.

On September 19, 1967, the MTM structure was delivered to AED from the vendor. On September 20, 1967, the MTM and TTM drawings, including placement of all electronic mockups, were completed.

On September 28, 1967, tests of the ATC breadboard model actuator sensor were completed satisfactorily. Fabrication of the first MTM unit was completed. The TTM structure was delivered on October 7, 1967.

The vendor for the pin puller completed design verification tests on October 11, 1967. The MTM louver panels were received from the vendor on October 18, 1967.

The studies for locations of the flight model boxes were started on October 25, 1967. On November 22, 1967, the assembly and instrumentation of the MTM spacecraft were completed. The MTM structure alignment measurements, solar panel deployment tests, and antenna deployment test were completed on November 29, 1967.

The MTM spacecraft vibration tests were started on November 30, 1967. On December 5, 1967, the flight placement study and balance calculation were completed. The MTM spacecraft vibration tests were completed on December 8, 1967.

On December 12, 1967, the post-vibration MTM structure alignment measurements, solar panel deployment tests, and antenna deployment tests were completed. The location drawing for the underside brackets and mounting holes for the flight model spacecraft was also completed.

On December 20, 1967, the spacecraft balance, moment of inertia measurements, and fixed-axis despin tests of the MTM were completed. The thermal fence was removed from the MTM and put onto the gimbal despin test fixture. The mechanical assembly of the TTM spacecraft was completed. On January 5, 1968, the gimbal despin tests were completed.

The separation and shock tests were conducted on the MTM spacecraft on February 29, 1968. All flight model drawings were completed and released for manufacturing on March 15, 1968.

On April 19, 1968, the drawings for the thermal blankets were completed, thus completing the mechanical design of the spacecraft.

On April 23, 1968, at NASA's direction, changes were initiated in the spacecraft design to accommodate the use of a two-stage launch vehicle rather than the three-stage vehicle originally intended. Because of this change, several spacecraft functions were no longer required. Since the two-stage vehicle is capable of placing the spacecraft into mission mode attitude before separation, the need for an initial acquisition and orientation maneuver of the spacecraft no

longer existed. Accordingly, the acquisition attitude sensor was no longer required and was removed. A high initial spin rate of the spacecraft was no longer required and the despin mechanism was deleted from the spacecraft design. A breakaway connector was added at the interface between spacecraft and launch vehicle attach fitting for the purpose of battery charging on the gantry, and to disconnect the accelerometer data through the beacon link at separation. Also deleted was the caging mechanism for the liquid nutation damper.

On June 15, 1968, the design drawing for the modified nutation damper was released. The modification deleted the pyrotechnic operated valve and substituted a bellows mechanism for oil pressurization.

On July 15, 1968, the nutation damper vacuum filling apparatus, used for oil-filling of the modified damper design, was completed.

On August 28, 1968, the first 1/4- and 1/2-scale models were delivered to NASA GSFC. Four additional 1/4-scale scale models were delivered over subsequent 5-month period.

On September 6, 1968 the procurement specification for the nutation damper bellows mechanism was released.

On April 4, 1969, the TIROS M spacecraft was rough balanced, and on April 5, 1969, the first of two moment of inertia tests were performed on the spacecraft.

On July 15, 1969, the TIROS M spacecraft was subjected to the separation shock test which consisted of cutting the Marmon damp bolts with pyrotechnic bolt cutters and allowing the attach fitting to fall away from the spacecraft.

On July 16 and 17, 1969, the TIROS M spacecraft was subjected to vibration tests and satisfactorily passed the sine and random test exposure.

On September 20 and 21, 1969, the magnetic dipole moments for the various spacecraft operating modes were measured and the required trimming magnets were installed.

On September 27, 1969, final alignment measurements were taken on the spacecraft sensory equipment.

On October 2, 1969, the spacecraft was fine balanced and on October 3, 1969, the final moment of inertia tests were performed on the spacecraft.

On October 4, 1969, all spacecraft tests were completed and the spacecraft was placed into temporary storage.

On December 8, 1969, the spacecraft was shipped to the Western Test Range.

The TIROS M spacecraft was launched on January 23, 1970.

SECTION III
THERMAL DESIGN

A. GENERAL

The final thermal design of the spacecraft is the result of modifications made to the intermediate design delineated in the Preliminary Draft of the Final Engineering Report, dated August 30, 1968. These modifications were based upon data derived from the thermal and electrical testing of the fully integrated flight spacecraft. Figure 2-III-1 shows the components used for thermal control.

Thermal control of the spacecraft is achieved by using passive thermal control surfaces in conjunction with active control surfaces. The passive thermal control of the spacecraft is accomplished by means of a variable solar absorptance thermal fence in conjunction with fixed radiators. See Figures 2-III-2 and 2-III-3. All radiator surfaces and thermal fence fins are finished with 3M 400 Series Black Velvet Coating to prevent degradation of the optical properties of the radiators due to space radiation.

The active control is accomplished with temperature controlled adjustable louvers, two per equipment side, which cover or expose radiator surface as required. Radiator and louver sizes are shown in Figure 2-III-2. General location with respect to the overall spacecraft configuration is illustrated in Figure 2-III-4.

Internal temperature distribution is controlled by a balance of conductive and radiative coupling to the thermal control surfaces of the fence and radiators. By proper location of the baseplate radiator area, high thermal dissipation units are controlled within specifications. Distribution of the radiator area controls the internal gradients. Figure 2-III-2 illustrates this distribution.

The spacecraft surface not used for temperature control is blanketed with insulation to limit the radiative heat transfer from these areas. The effective emissivity has been empirically determined to be 0.02 for the insulated area.

The design specifications have been met for both the acquisition and operational modes of the mission plan for the limited thermal conditions anticipated (i.e., an orbit sun angle range of 29 to 64 degrees during the first year of life, predicated on the ±0.03 degree per day tolerance on orbit sun synchronism associated with two-stage orbital insertion and a 20-minute launch window).

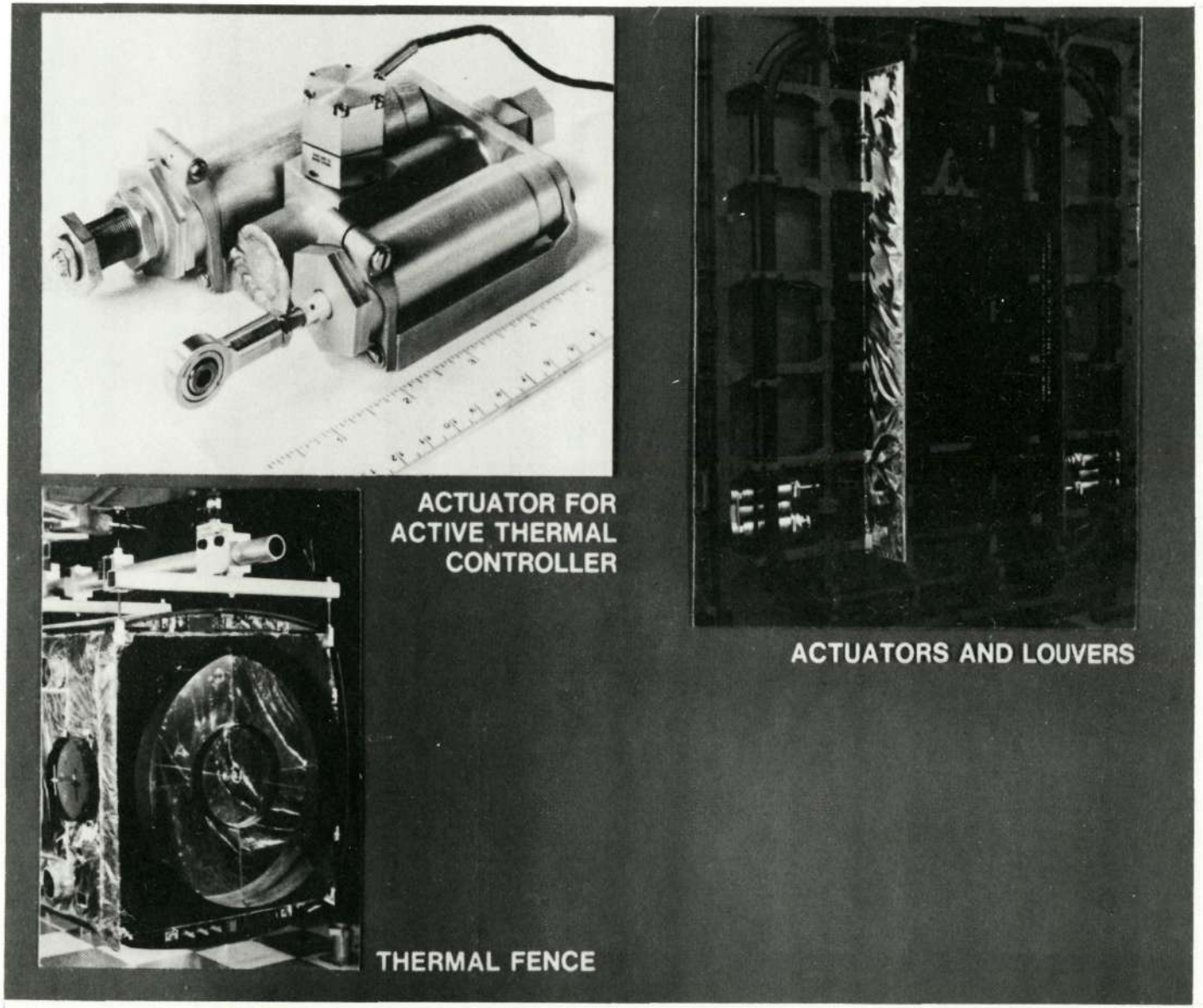


Figure 2-III-1. Thermal Control Components

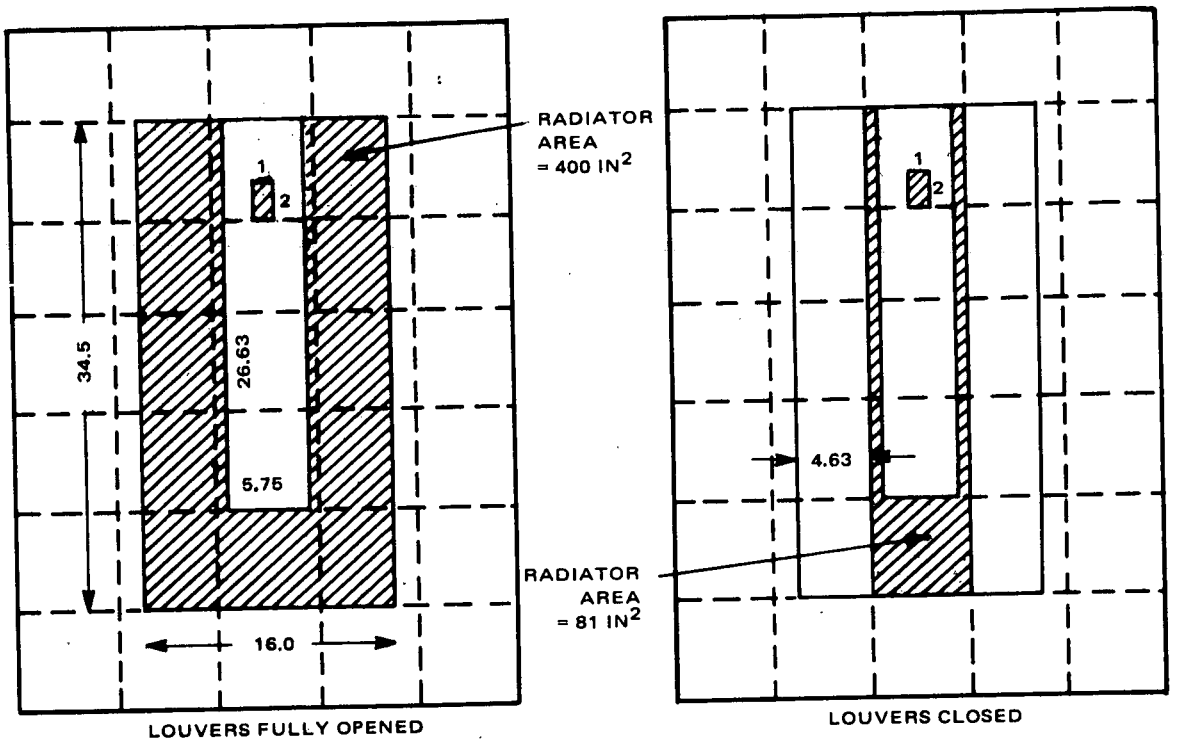


Figure 2-III-2. Thermal Radiators

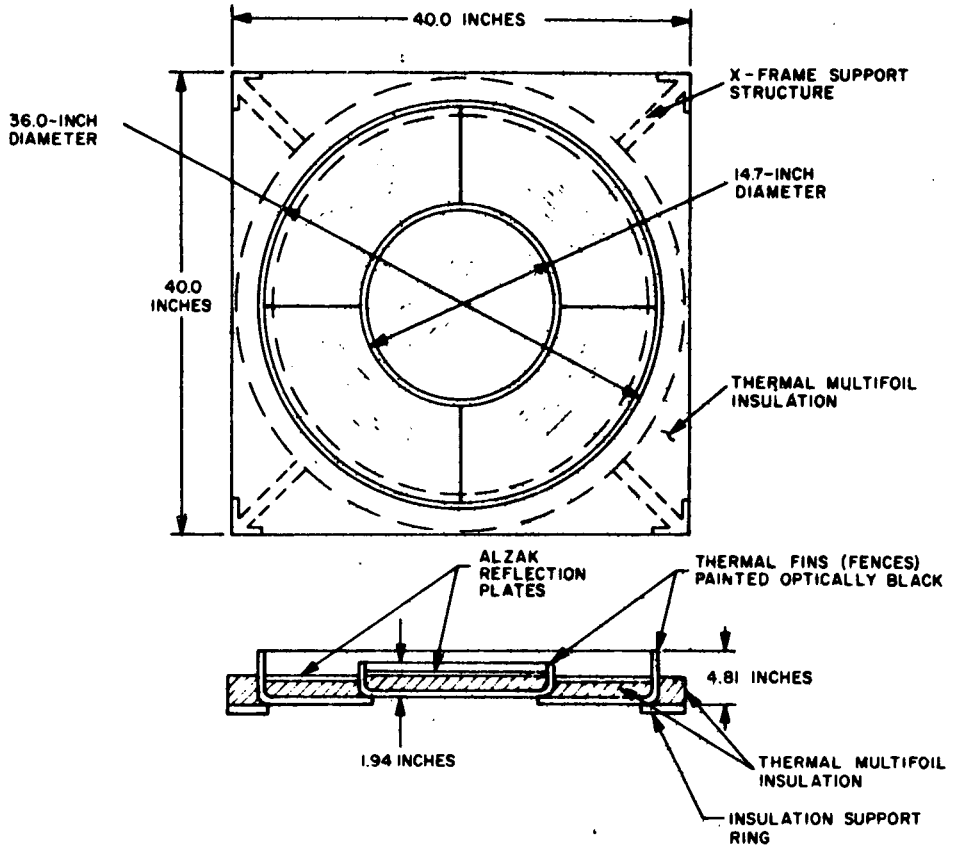


Figure 2-III-3. Thermal Control Fence

B. FUNCTIONAL DESCRIPTION

1. Thermal Fence

The thermal fence is composed of two spun sheet metal cylinders concentrically riveted to form a common sheet metal plate as illustrated in Figure 2-III-3. The horizontal surface of the assembly, called the fence plate, is covered with a multilayer insulation blanket at the outer (space viewing) surface. A thin, flat, metal reflector is placed over the insulation blanket in the area enclosed by the vertical portions of the two cylinders. The vertical portions of the cylinders, called fence fins, project through the insulation and are exposed to space. The surface finish on the fins and plate is optically black, while the solar reflectors are Alzak aluminum (a high emissivity, high specular solar reflectance material).

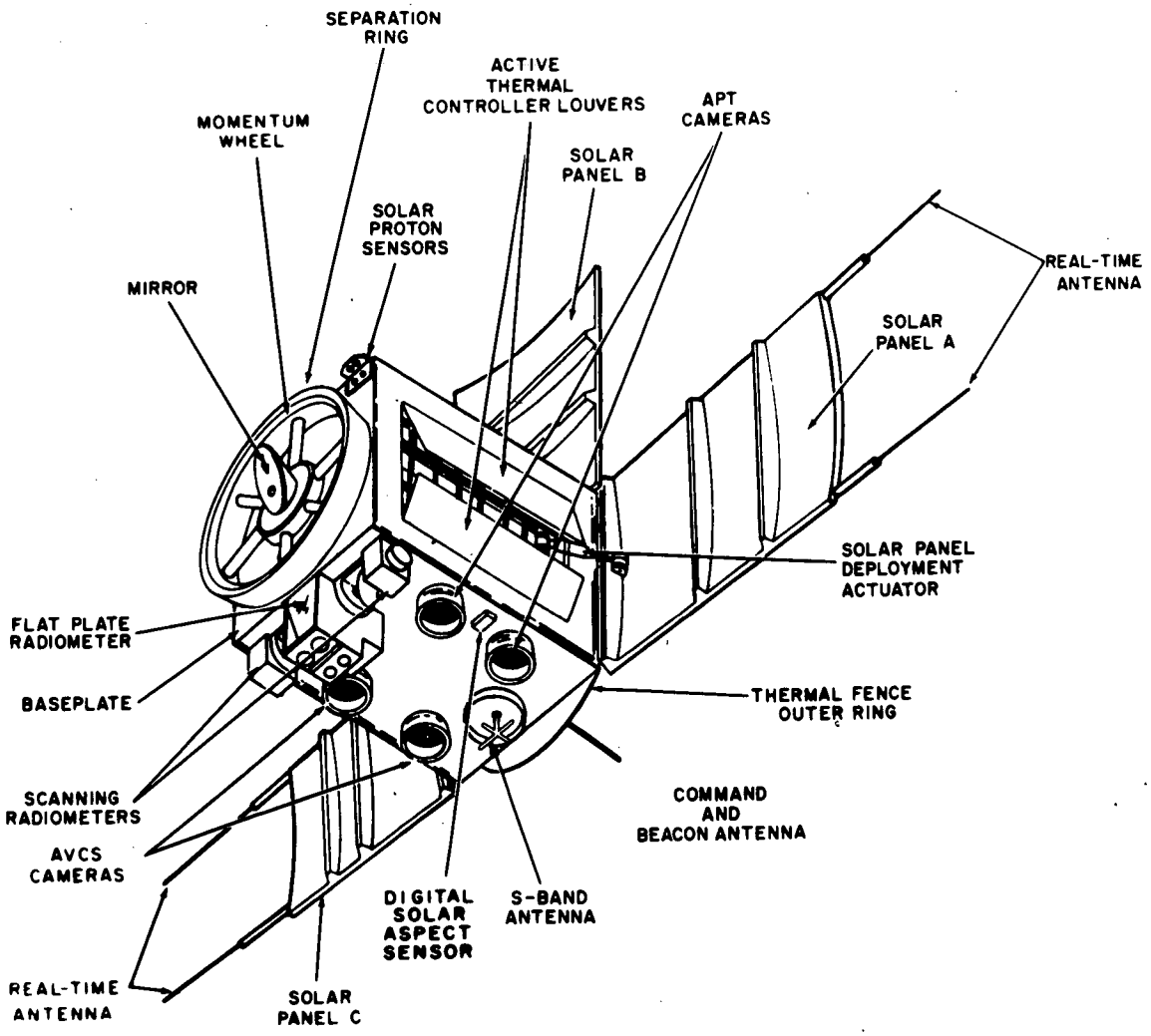


Figure 2-III-4. Spacecraft Configuration

The thermal fence is attaced to an X-frame support member by thermal insulation spacers. The X-frame attaches to the spacecraft at four diagonal corners and is not insulated for structural reasons. Conductive heat losses from the fence to the spacecraft structure are minimal. Exchange of radiant energy between the thermal control fence and the interior of the spacecraft occurs at the inner surface of the fence plate. Areas on the top endplate beyond the periphery of the circular fence plate are covered with a multilayer insulation blanket (see Figure 2-III-3) to shield the view to space from the interior of the spacecraft.

The desired thermal performance is achieved as follows. At a given solar angle of incidence, (γ), solar energy is absorbed by the exposed black fins from two sources; namely, by direct illumination and by specular reflection from illuminated portions of the reflector plate. As the solar angle of incidence increases from 0 to 60 degrees, more fin absorption results due to the combined effects of the increasing direct projected area and the increasing indirect specular reflections. The resulting fence plate temperatures are used to control the spacecraft temperatures by means of radiation heat exchange. Incorporating theoretically predicted and experimentally derived values, the net heat exchange between the thermal fence plate and a representative 20°C spacecraft is portrayed graphically as a function of sun angle in Figure 2-III-5.

Confirmation of the validity of the thermal control fence design theory was obtained by tests of a model of the device, performed at Jet Propulsion Laboratory (JPL), Pasadena, California.*

The purpose of the test program was to evaluate the behavior of the thermal fence in a simulated (Earth orbit) solar-space environment and to compare the results with analytical predictions. The JPL 10-foot space simulator was selected by RCA for this program because of the solar douser capability, and the conformance of solar intensity, uniformity, and spectrum to RCA requirements. The following test objectives were established:

- Determine effective solar absorption of the fence as a function of solar incidence angle.
- Determine effective thermal emittance of the fence as a function of solar incidence angle.
- Determine performance data on fences with nondegraded reflector surface finish and with severely degraded reflector surface finish in order to establish worst-case tolerances for solar absorptance and thermal emittance.

*TIROS M Thermal Control Fence Space Simulator Test 10-18, August 1967, Jet Propulsion Laboratory, California Institute of Technology, Pasadena, California.

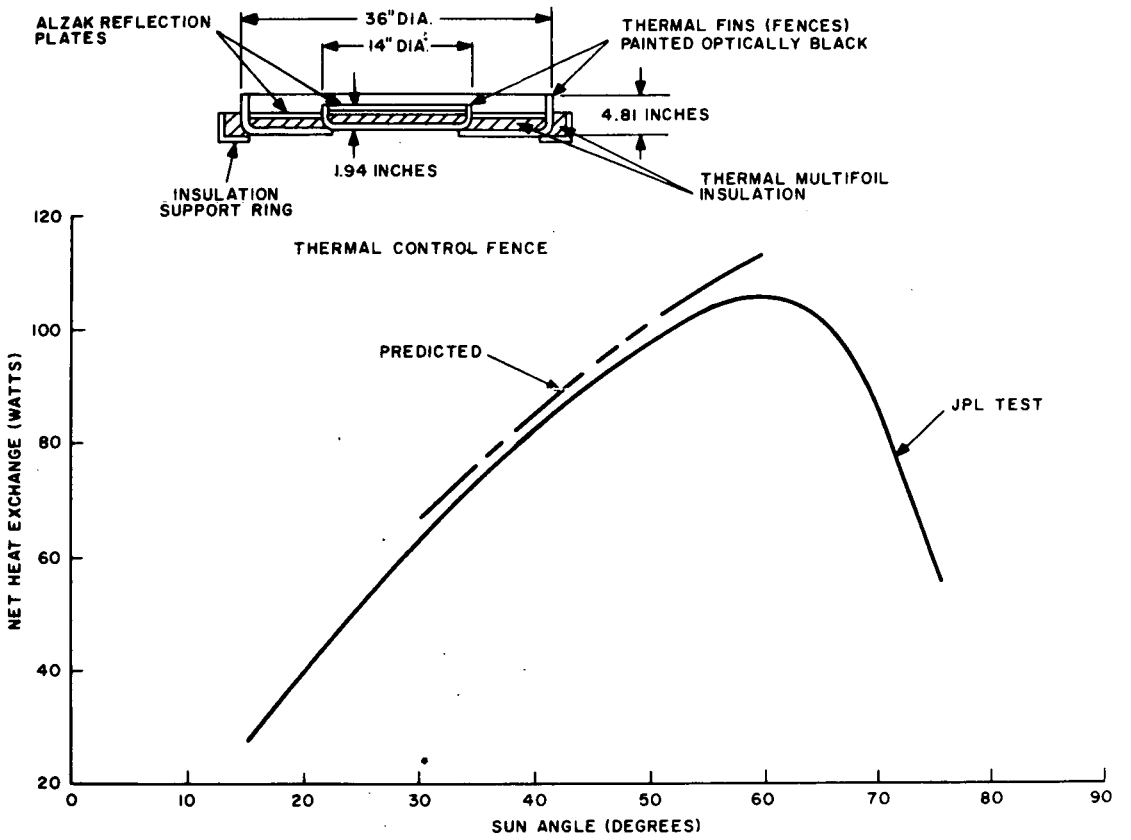


Figure 2-III-5. Net Heat Exchange Between Thermal Fence Plate and 20°C Spacecraft

The solar-space environment achieved during the test was as follows:

- Heat sink conditions of outer space were simulated by use of a black wall shroud held at a mean wall surface temperature of approximately -300°F.
- Chamber vacuum was in the 10^{-6} torr range.
- Solar flux level was 129.6 w/ft^2.

Testing of the thermal control fence was accomplished in the 10-foot space simulator. The test data results closely approximated the data calculated from a computer model at RCA.

2. Active Thermal Controller (ATC)

The active portion of the control system consists of four independent ATC units (two per equipment side), each consisting of a fluid expansion actuator/sensor mechanically linked to a single, vertically-hinged louver.

The actuator/sensor responds to local temperature changes at its mounting surface and develops motion through the controlled volumetric expansion of a confined fluid. The unit includes both safety and temperature adjustment features; it is located on, but external to, the equipment panel between the panel and the insulation blanket, and adjacent to the lower end of its associated louver. Each ATC is designed to provide a 90-degree louver rotation (fully closed to 90 degrees open) for an actuator/sensor box temperature change of 20°C. It is further designed to provide an adjustment feature which allows the 20°C temperature differential to be selected anywhere in the -10° to +55°C range. Survival under a qualification soak temperature range of -15° to +60°C is a design requirement.

The ATC's are operable only when the solar panels are deployed. Injection temperature requirements must be satisfied when the louvers are fixed in a forced open condition (i.e., rotated 180 degrees from the closed position). Return of the louvers from the forced open condition is accomplished by means of spring-loading.

3. Thermal Insulation

The insulation material provides an effective emissivity of approximately 0.01 in areas of the spacecraft not acting as thermal control surfaces. In theory the effective emissivity of a multilayered aluminized film insulation can be expressed as:

$$\frac{1}{\epsilon_e} = \frac{1}{\epsilon} + \frac{1}{\epsilon_1} + \frac{1}{\epsilon_2} + \frac{1}{\epsilon_3} + \cdots + \frac{1}{\epsilon_{2n}} - n$$

where

ϵ_e is effective emissivity,

ϵ is emissivity spacecraft structure,

$\epsilon_1, \epsilon_2, \epsilon_3 \cdots$ is emissivity of subsequent film surface, and

n is number of film layers.

The theoretical value is elusive in actual practice since other factors become prominent. Conduction from layer to layer, where contact between subsequent surfaces occurs, will reduce the insulating qualities of the material. Edge losses by radiation and face-to-face conduction by bonding, stitching, or fastening devices are also factors which increase the effective emissivity of the insulation, thereby reducing the insulating quality.

The insulation used consists of ten layers of aluminized film, each separated with nylon netting. As determined empirically in laboratory tests and substantiated on the TTM and flight spacecraft (i.e., All-Up Thermal) tests, the effective emissivity meets the 0.01 to 0.02 requirement deriving from the capabilities of the passive and active thermal control elements.

4. Thermal Painting

The paint used on the radiators and thermal fence is the 3M 400 Series Black Velvet Coating, selected for high emissivity and absorptivity at values which will be stable over the full orbit life of the spacecraft.

A detailed investigation of this series of 3M paint was performed by the AED Materials Engineering Activity, and a report, dated July 1967, was submitted. The specifications, pertinent to the final design, which were generated in conjunction with the report are listed in Table 2-III-1.

TABLE 2-III-1. THERMAL PAINT SPECIFICATIONS

RCA Specification	Subject
2021064 Manufacturing Specification	Thermal control coatings
1960416 Materials Specification	3M 400 Series Black Velvet Coating
1960706 Materials Procedure	Thermal control coatings
1960707 Materials Procedure	Protective peelable coating for polished aluminum

5. Temperature Sensors

The temperature sensors measure the flight temperatures at various locations within the spacecraft. This is done in analog fashion by resistance thermometry voltage divider action, where an output voltage is developed as a

function of temperature at the output of a sensor and applied, via an electronic commutator which time-shares the sensor signal with those signals from other sensors and functions, to the input of the analog telemetry subsystems.

To achieve uniform temperature resolution over the various estimated temperature ranges, predetermined for the selected locations of the sensors, there is, ideally, a linear relationship between output voltage and sensor temperature.

A three-terminal passive element using ceramic thermistors and fixed resistors has been developed, which provides an output voltage that is nearly a linear function of temperature when supplied with a low impedance, regulated voltage of -24.5 volts DC. This is accomplished by a unique combination of semi-conductor and metallic resistance materials having different temperature coefficients of resistance. The circuits and assemblies were qualified on the TOS program and have demonstrated reliability.

The sensors have a linear repeatibility and intercept temperature insensitivity better than 10 percent, but to achieve a readout accuracy of 1°C, individual calibration is required.

C. DESIGN HISTORY

1. Final Design Requirements

To ensure best performance in orbit and to provide margins over test levels, design requirements for the acquisition and operational phases of the mission plan were imposed on the thermal control system which were more stringent than those specified for both qualification and flight acceptance procedures. These requirements are listed in Table 2-III-2.

As stated earlier, thermal control of the spacecraft is achieved by using fixed thermal control surfaces in conjunction with active control surfaces. This approach ensures a favorable temperature environment for the electronic equipment as planned, and also provides a capacity to accommodate spacecraft growth in terms of higher power and more precise temperature control. Surface areas of the spacecraft not functioning as thermal control surfaces are covered with multilayer aluminized film insulation.

The passive thermal control of the spacecraft is accomplished by a variable solar absorptance design in conjunction with fixed radiators. This variable solar absorptance design consists of concentric rings or fences, as illustrated in Figure 2-III-3, whose solar absorptance varies as a function of solar incidence

TABLE 2-III-2. SPACECRAFT THERMAL CONTROL SYSTEM FINAL DESIGN REQUIREMENTS

Mode	Parameter	Temperature (°C)*	
		Max	Min
Acquisition	Internal components (except MWA)	+45	-5
	Momentum wheel assembly	+45	-5
	Scanning radiometers	+45	-5
	Flat plate radiometer	+45	-10
	Solar proton monitor	+55	-50
	Shunt limiter		
	a) transistors (junction)	+115	-55
	b) resistors	+175	-100
Operational	Internal components (except MWA, PSE, batteries and cameras)	+35	+5
	Batteries	+30	+10
	Cameras	+30	+5
	PSE	+40	+5
	Momentum wheel assembly	+30	0
	Scanning radiometers	+45	-5
	Flate plate radiometer	+35	-10
	Solar proton monitor	+15	-40

*All temperatures listed apply to structure mounting points with the following exceptions:

- Momentum wheel assembly — flange temperature
- Scanning radiometer — box temperature
- Flate plate radiometer — box temperature

angle. As the solar incidence angle, γ, (the angle between the fence plate normal and the sun vector) increases, the solar absorptance of the fence increases, resulting in the desired heat balance for the spacecraft. (See Figure 2-III-5.)

The active temperature controller (ATC) further limits the operating temperature of the subsystems. The ATC consists of a hydraulic reservoir, which is the temperature sensor, coupled to a bellows. A change in the temperature at the hydraulic reservoir causes a related change in the volume of the liquid; the volumetric differential is manifest in the bellows as a rectilinear expansion or contraction which is translated to the mechanism used to open or close a louver on the side of the spacecraft, as shown in Figure 2-III-6. The range of operation of the ATC is set, but can be changed by variations in one or a combination of the following:

- Mechanisms,
- Fluid material,
- Fluid volume, and
- Bellows geometry.

Both the passive thermal fence design and the ATC were designed particularly for the ITOS spacecraft program. The composition of the aluminized film insulation was also newly developed, this being the first AED project to have a major portion of the surface blanketed with insulation.

2. Definition of Preliminary Design

To establish a preliminary thermal design, steady-state analysis of a 22-body parametric model was performed. The analytical results for the preliminary thermal design are described below, followed by results of the intermediate and final design analyses.

a. ACQUISITION MODE

The 22-body model was utilized to predict the average temperatures of the baseplate, the equipment panels (comprising the AVCS and APT sides), the thermal fence, and the solar panels for maximum and minimum suntime orbits (i.e., 88- and 73-percent suntimes consistent with orbit sun angles of 38 and 60 degrees in a circular orbit of 775-nautical-mile altitude) and a range of spacecraft sun angles encompassing 30 and 150 degrees, commensurate with the then prevalent assumption of three-stage injection. The results indicated that the temperatures of

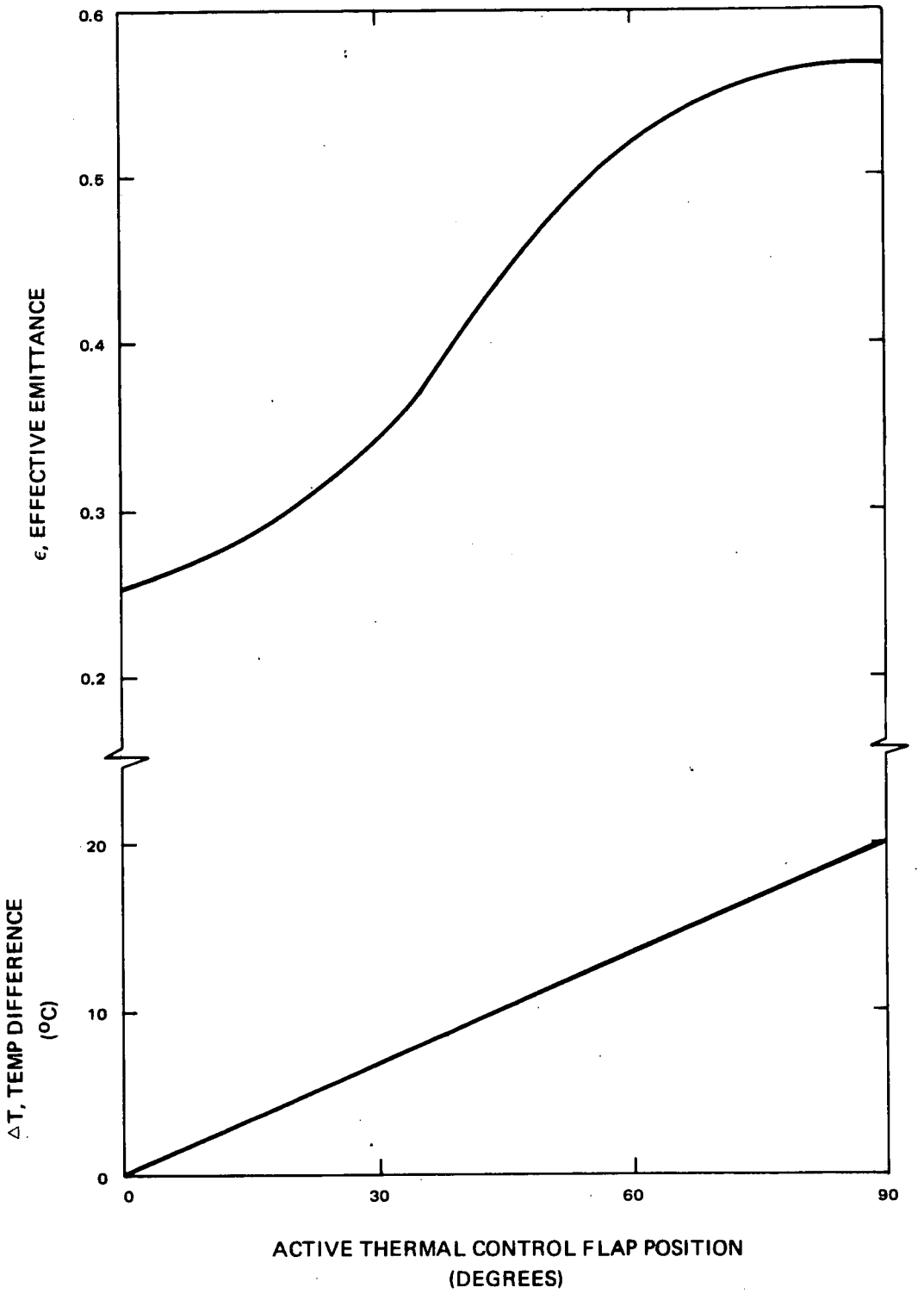


Figure 2-III-6. Active Thermal Control, Functional Characteristics

the internal component mounting points could be maintained well within the -5°C and +45°C limits by postulating a 610-square-inch baseplate radiator area located inside the adapter ring with effective solar absorptivity of 0.45 and an effective emissivity of 0.87.

Pursuant to the determination of a suitable surface finish for the complex waffle-type construction of the baseplate to obtain the desired values of α_{eff} and ϵ_{eff}, an analysis was initiated. The results of this analysis indicated that 3M White Velvet paint would provide acceptable values of α_{eff} and ϵ_{eff} of 0.44 and 0.93, respectively.

b. OPERATIONAL MODE

Operational mode temperature predictions were made, again utilizing the 22-body model, for a range of orbit sun angles bounded by 30 and 60 degrees, based on the assumption of black side radiators with the surface properties α_{eff} = 0.97 and ϵ_{eff} = 0.89, each 463 square inches in area, and an operational range for the ATC units, controlling each of the four rectangular louvers, of from 2° to 22°C. The results indicated that the mounting point temperatures for the internal components could be readily maintained within the 5°C and 35°C limits and, further, that such a design could accommodate an additional 10 watts of electrical dissipation per panel. Moreover, there was a clear indication that a louver failure requirement of maintaining mounting point temperatures in the 0° to 40°C range should any two ATC units becomes inoperative, in either a closed or open position, could also be satisfied by judicious sizing of the side radiator bias areas. A study was made to effect a tradeoff between providing sufficient heat dissipation during a hot orbit (i.e., 30-degree orbit sun angle) where a closed louver failure was postulated, and holding to a minimum heat leakage from the spacecraft where an end-of-life power failure was combined with an open louver failure, at an orbit sun angle productive of a worst-case cold condition. In conjunction with other thermal considerations, the results indicated that a bias area 5 inches in width would be ideal, capable of maintaining mounting point temperatures above the 0°C limit in the presence of an end-of-life failure power level as low as 20 watts at an orbit sun angle of 30 degrees, the condition which proved to be the coldest failure case. The foregoing dimensional requirements for bias and total side radiator area dictated that louvers 4.63 inches in width (158 square inches in area) be used, in conformance with the 14.25-inch spacing between the hinge lines of pairs common to the same side panel.

c. CRITICAL PARAMETER VARIATION

To fully justify the spacecraft preliminary thermal design, it was necessary to investigate the effects of variation in certain critical parameters. Since both the hot and cold acquisition mode conditions attending the three-stage launch were found

to occur with the sun on the baseplate, the most critical parameter during acquisition became the effective baseplate solar absorptivity. The results of a parametric study initiated to assess the sensitivity of mounting point temperatues to the α_{eff} of the baseplate radiator indicated that values in the range of 0.38 to 0.53 would suffice to ensure satisfaction of the -5°C to 45°C design requirement. Consequently, an α_{eff} of 0.45, midway between the indicated limits, was chosen as the design value.

The spacecraft temperatures during the operational mode are essentially a balance between the thermal loading and the radiative coupling to space. To evaluate the cumulative effects on mounting point temperatures of deviations of both these parameters from nominal values, further parametric study was undertaken. Results indicated that an 8-percent reduction in thermal loading concurrent with an identical increase in radiative coupling was tolerable, as was a 4-percent variation of opposite sense. In both cases, the mounting point temperatures were found to conform to the 5° to 35°C design requirement.

3. Modifications of Thermal Design Due to Detailed Analysis and Fabrication

The design modifications described below are attributable to the results of analytical studies of a more detailed nature conducted subsequent to the initial definition effort, and to the physical problems encountered during fabrication of the preliminary design.

a. RELOCATION OF THE ATC FLAPS

To force the ATC units to operate nearer the center of their operating range than indicated by the 22-body analysis, the spacing between louver hinge lines was increased from 14.25 to 16.25 inches. Retaining the 158-square-inch louvers, this change results in an increase in available radiator area from 463 to 532 square inches.

b. INSULATION CHANGE

Initial fabrication of the multifoil insulation blankets indicated that application of black paint to the insulation covering the top endplate beyond the periphery of the circular fence plate, as specified in the preliminary design, was ill-advised as the coating was found to be extremely susceptible to chipping. To overcome this problem, the outer surface specification has been changed from 3M Black Velvet paint ($\alpha = 0.971$, $\epsilon = 0.895$) to aluminum-backed H-film ($\alpha = 0.354$, $\epsilon = 0.525$). This change resulted in an increased, but acceptable, heat loss from the spacecraft through the insulation.

c. REDISTRIBUTION OF BASEPLATE RADIATOR

Baseplate gradient studies indicated that the battery packs and the power supply electronics must be located immediately above the radiator area. Since the preliminary design did not satisfy this requirement, the baseplate radiator distribution was modified from a configuration with the entire radiator inside the adapter ring to one of the same total radiator area where, in addition to that within the adapter ring, bays at three of the four corners of the baseplate were denuded of insulation, painted black and utilized as radiative surfaces.

d. REDUCTION OF TOTAL RADIATOR AREA

The 22-body analysis indicated that the tops of the equipment panels and the baseplate regions near the battery packs and the power supply electronics were the hottest component mounting regions in the spacecraft.

The widening of the side radiators (Paragraph 3.a) and the redistribution of the base radiator (Paragraph 3.c) had the effect of reducing temperatures in the hot regions. The insulation change (Paragraph 3.b) resulted in a general reduction in spacecraft temperature level. It was possible, therefore, to reduce the temperature gradients in the equipment panels by selectively reducing the radiator areas in the colder regions of the spacecraft. Reducing the side radiator area by insulating 142 square inches of the bottom portion resulted in a design side radiator area of 390 square inches. Selective insulation of the available base radiator area resulted in a design base radiator area of 476 square inches.

4. Transient Thermal Analysis

To verify the adequacy of the modified thermal design, transient thermal studies were performed for representative worst-case orbital conditions utilizing a 127-body analytical model devised expressly for the task. The results of the transient analyses are summarized below.

a. ACQUISITION MODE

The 127-body model was used to generate transient temperature predictions for one of the cold acquisition mode cases identified during the preliminary design study, defined by an orbit sun angle of 60 degrees and a spacecraft sun angle of 150 degrees, consistent with the assumption of a three-stage launch. The results of this study indicated that the modified design would indeed ensure satisfaction of the $-5^{\circ}C$ minimum mounting point temperature requirement. More significantly, the

results generated with the aid of the 127-body model exhibited a high degree of correlation with those derived from the 22-body model. By virtue of this correlation, the temperature predictions made for the balance of the injection mode cases examined during the preliminary design study were considered representative of the modified design, obviating further investigation of acquisition mode thermal performance. The acquisition mode thermal transient results indicated that, for an initial spacecraft temperature of 20°C, a condition of dynamic thermal equilibrium, amenable to characterization by steady-state, orbit-average temperatures, would be achieved approximately 38 hours (i.e., ~20 orbits) after launch.

b. OPERATIONAL MODE

Transient temperature predictions for both the worst-case hot and worst-case cold operational mode conditions were generated, again using the 127-body model. The results so derived reinforced the previous findings, confirming the adequacy of the modified design.

(1) The total range of operational temperatures for all components, excluding the power supply electronics, was found to be 10.8° to 29.2°C which is within the design specification of 5° to 35°C. The maximum power supply electronics temperature predicted was 36.2°C which is well within the operational temperature range of previously flown power supply electronics components.

(2) The total range of operational temperatures for the battery pack was found to be 10.8° to 25.8°C which is within the design specification of 10° to 30°C.

(3) The total range of operational temperatures for all the cameras was found to be 17.1° to 21.7°C which is well within the design specification of 5° to 30°C.

(4) As previously, the results generated with the aid of the 127-body model exhibited a high degree of correlation with those derived from the 22-body model. Accordingly, the temperature predictions made for the failure and non-nominal operational cases during the preliminary design study were considered representative of the modified design.

5. Modification of Thermal Design Due to Analytical Evaluation, TTM Testing and Launch Vehicle Reconfiguration

a. REDISTRIBUTION OF THE RADIATOR AREA

Evaluation of the temperature predictions generated in the course of the foregoing analysis revealed significant thermal gradients between the equipment panels and the baseplate, dictating a redistribution of radiator surface area. The low spacecraft temperatures which prevailed during the initial phase of TTM testing compelled an even more comprehensive redistribution of radiative surface. The redistribution entailed a reduction in baseplate area of 193 square inches, eliminating radiator surface at the baseplate corners and some radiator surface inside the adapter ring, bringing about an intermediate design value of 283 square inches. Also, the side radiator areas were increased by 51 square inches each, bringing about an intermediate design value of 441 square inches. The revised design incorporated bias radiator areas for the side panels of 125 square inches, tailored by the utilization of 116-square-inch "islands" of insulation.

b. ALTERATION OF BASEPLATE RADIATOR SURFACE FINISH

The reconfiguration of the launch vehicle from a three- to a two-stage assembly suggested the resurfacing of the baseplate radiator area with the preferrable 3M Black Velvet finish. The alteration in surface finish from the degenerative white to the relatively impervious black finish was made possible by the fact that the spacecraft orbital insertion maneuver for which the two-stage assembly was programmed precluded illumination of the baseplate radiator by the sun. The alteration was accomplished prior to TTM testing.

c. REDESIGN OF INSULATION

During the initial phase of the TTM testing, it was determined that the effective emissivity of the insulation blanket was far in excess of the design value utilized in the analytical evaluation. As a result, a redesign of the insulation was initiated with regard to the basic blanket composition, the quantity of through-sewing, and the amount and integrity of blanket overlap. The blanket was changed from a 20-layer, unseparated, embossed, aluminized Mylar composition to a 10-layer aluminized Mylar composition, intersticed with nylon netting separators. After installation of the redesigned blanket, the TTM was submitted for retesting. The results of the retest indicated a redesign induced reduction in effective insulation emissivity from 0.05 to the prescribed design value of 0.02.

6. Predicted Flight Temperatures for Small-to-Large Sun Angles at an Orbit Altitude of 775 Nautical Miles

The 127-body model mentioned previously was used to generate, in a modified format, orbit-average, steady-state predictions of component mounting point temperatures for the conditions of normal and extended mission mode operation (i.e., for orbit sun angles of 15 to 75 degrees) in an orbit of 775 nautical miles altitude. Including the 3°C uncertainty deriving from orbital transient variations, revealed through repeated attempts at analytical correlation of TTM test results, the predictions for conditions of normal mission mode operation (i.e., that attending an orbit sun angle range of 30 to 60 degrees), with a single exception, conformed to the prescribed temperature specifications. The exception was the predicted battery mounting point temperature, which exceeded the maximum specification value of 30°C. Resolution of this potential conflict was effected upon disclosure that actual cell-to-mounting gradient was significantly lower than that postulated in the derivation of the 30°C specification (i.e., 3°C as compared to 5°C), to the extent that the maximum cell temperature, realized in operation, would prove acceptable.

7. Predicted Flight Temperatures for Normal Operating Sun Angles at Orbiting Altitudes of 600 and 900 Nautical Miles

The analysis was extended to evaluate subsystem performance under the extremes of mission mode thermal conditions for both 600- and 900-nautical-mile altitude orbits. The predictions derived indicated that, in practice, component mounting point temperatures would differ by no more than 1°C from those attending corresponding thermal conditions where a 775-nautical-mile altitude was assumed.

8. Modifications of Thermal Design Due to Thermal and Electrical Testing of the Fully Integrated Flight Spacecraft

The necessity of compensating for the reduced power dissipation levels disclosed during the electrical testing of the integrated spacecraft and the unexpectedly large heat leakage through the scanning radiometer units revealed during the initial abortive "All-Up Thermal Test" (i.e., an order-of-magnitude greater than that postulated in the analytical model) dictated a substantial reduction of the radiator areas on the baseplate and both equipment panels. The baseplate area underwent a reduction of 227 square inches to a final design value of 56 square inches, located within the adapter ring to provide a means of heat dissipation for the PSE (power supply electronics). Additionally, the equipment panel radiator areas were reconfigured by expansion of the "islands" of insulation mounted thereon to a final design providing a total of 400 square inches of available radiative surface on each panel with 81-square-inch bias areas. The precise distribution of radiator surface

area is displayed in Figure 2-III-2. Apart from the reconfiguration of radiator area, the SR mountings were revised; the steel spacers and alignment shims used previously were replaced by copper spacers with an RTV interface, where the bonding agent is applied as a liquid and allowed to vulcanize.

9. Predicted Flight Temperatures for Mission Mode Sun Angles at an Orbit Altitude of 790 Nautical Miles

In the interim between the issuance of the Thermal Design Report and the authorization of the "All-Up Thermal Test", the operational orbital altitude for the spacecraft was revised upward from 775 to 790 nautical miles in order to provide sufficient scan path overlap to ensure contiguous camera coverage in the earth's equatorial region. For the summary analysis, the 127-body model utilized previously was modified. These modifications entailed an expansion of the model to encompass 131 bodies including the scanning and flat plate radiometers and the revision of a number of radiative and conductive coupling coefficients as warranted by the results of the "All-Up Thermal Test". The test-correlated 131-body thermal model employed in the summary exercise is delineated in Figures 2-III-7 and 2-III-8, showing the structural model and the component model, respectively. Orbit-average, steady-state temperature predictions were generated for the full range of mission mode orbit sun angles (30 to 60 degrees) for conditions of maximum and minimum internal power dissipation to define operational temperature envelopes for the many components. The maximum power dissipation level is predicted upon realization in-orbit of the maximum electrical loading specified for the individual components and a maximum beginning-of-life array output, with the added stipulation of a normal battery charging rate. The minimum level is representative of an in-orbit component loading approximating that measured in test (a derating factor of 10 percent was utilized) and an array output characteristic of an end-of-life, degraded condition. Displays of predicted box and mounting point flight temperatures for certain critical system components as functions of orbit sun angle are presented in Figures 2-III-9 through 2-III-17. The flight temperature predictions for the balance of the nodes incorporated in the thermal model are summarized in Table 2-III-3. The predictions indicate that, of the many components on-board, only the batteries would violate the design temperature specifications, should the full 3°C tolerance (deriving from imprecise correlation of analytical and experimental results and the diurnal variations associated with in-orbit operation) apply in a positive sense under conditions of maximum power dissipation and a 30-degree orbit sun angle. In fact this potential violation does not merit concern, as the option for trickle-charge operation can be exercised resulting in a reduction in battery temperature approximating 10°C.

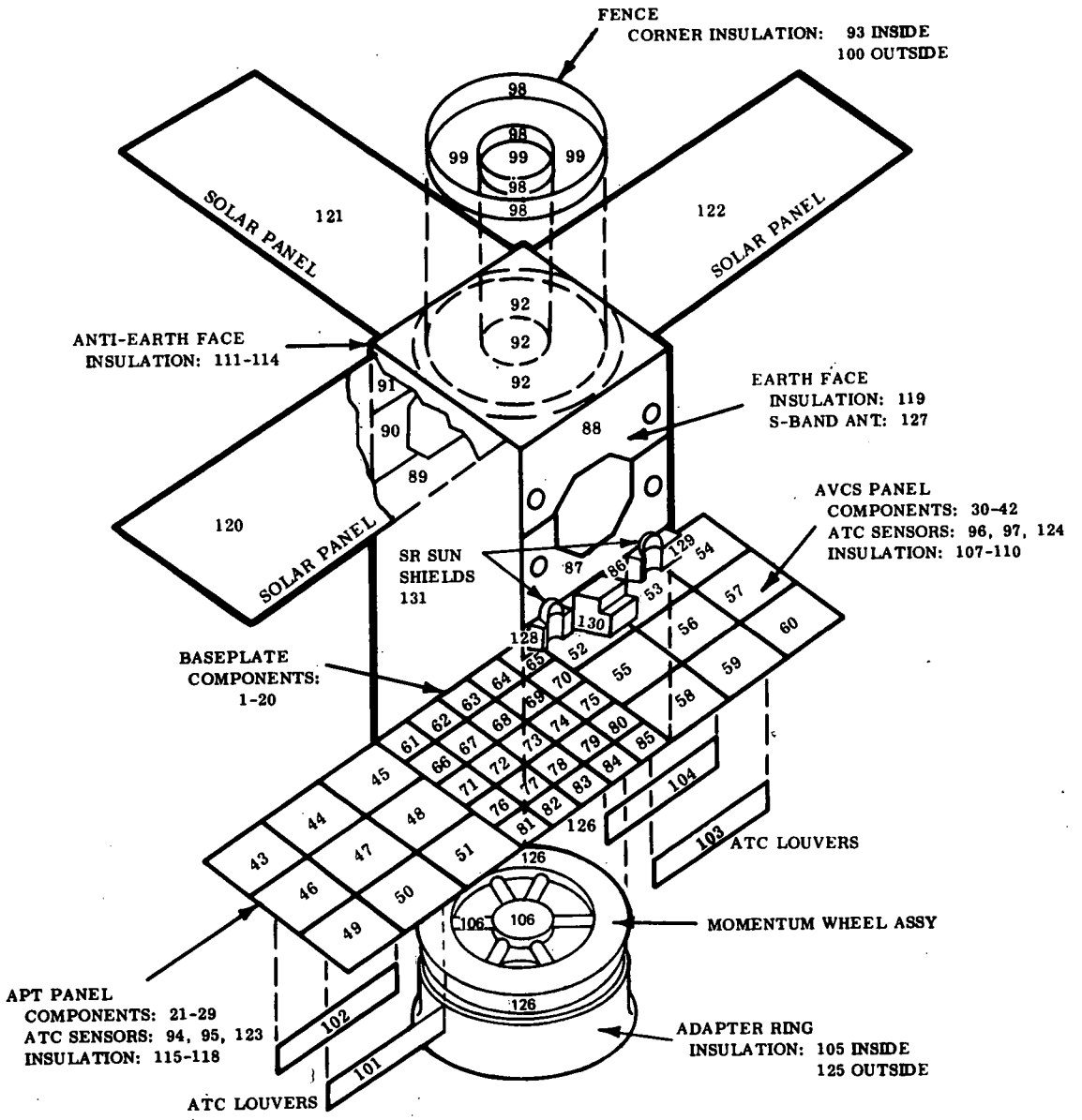
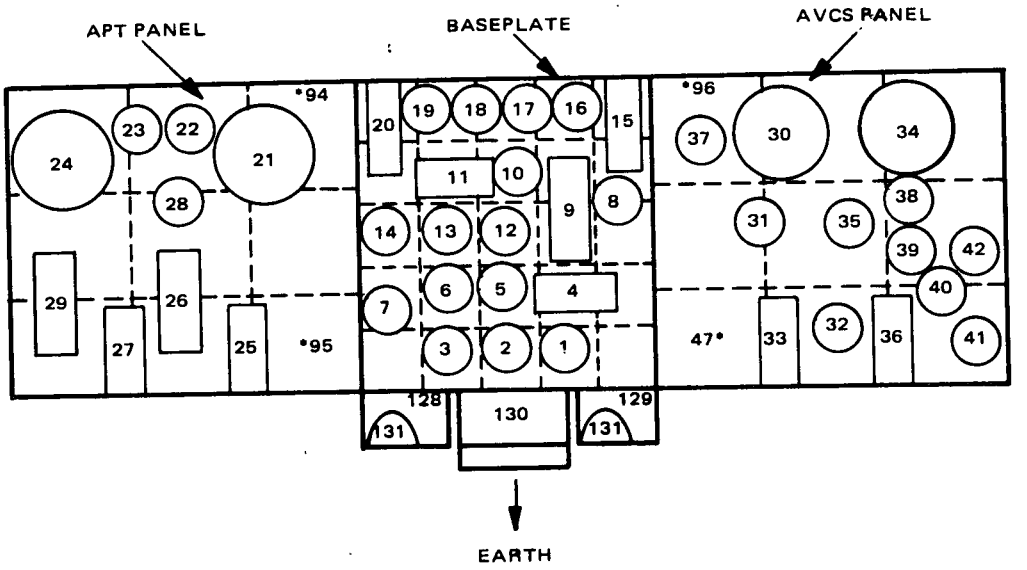


Figure 2-III-7. Structure Thermal Model for 131-Body Analysis



BASEPLATE COMPONENTS

1: S.R. ELECTRONICS #2
2: DUAL I.R. PROCESSOR
3: S.R. ELECTRONICS #1
4: POWER SUPPLY ELECT.
5: PITCH CONTROL ELECT.
6: INCREMENTAL RECORDER
7: MAGNETIC BIAS SWITCH
8: COMMAND DIST. UNIT B
9: DUAL MULTIPLEXER
10: DUAL COMMAND RECEIVER
11: DUAL PROGRAMMER
12: MOMENTUM WHEEL HOUSING
13: DATA FORMAT CONVERTER
14: COMMAND DIST UNIT A
15: BATTERY PACK #2
16: SIGNAL COND. & TELEMETRY
17: TIME BASE GENERATOR
18: DUAL DECODER
19: SOLAR PROTON ELECT
20: BATTERY PACK #1

APT PANEL COMPONENTS

21: S.R. RECORDER #1
22: S.R. RECORDER ELECT. #1
23: S.R. RECORDER ELECT. #2
24: S.R. RECORDER #2
25: APT CAMERA #1
26: APT CAMERA ELECT. #1
27: APT CAMERA #2
28: REAL TIME XMTR
29: APT CAMERA ELECT. #2

AVCS PANEL COMPONENTS

30: AVCS RECORDER #1
31: AVCS RECORDER ELECT. #1
32: AVCS CAMERA ELECT. #1
33: AVCS CAMERA #1
34: AVCS RECORDER #2
35: AVCS RECORDER ELECT. #2
36: AVCS CAMERA #2
37: BEACON XMTR & SCO ASSY
38: S-BAND XMTR #1
39: S-BAND XMTR #2
40: AVCS CAMERA ELECT. #2
41: ACQUISITION ATTITUDE SENSOR
42: DIGITAL SOLAR ASPECT SENSOR

ACTIVE THERMAL CONTROLLERS

94: APT ATC #2 (*ON BACK OF PANEL)
95: APT ATC #1 (*ON BACK OF PANEL)
96: AVCS ATC #3 (*ON BACK OF PANEL)
97: AVCS ATC #4 (*ON BACK OF PANEL)

EXTERNAL COMPONENTS

127: S-BAND ANTENNA
128: SCANNING RADIOMETER #1
129: SCANNING RADIOMETER #2
130: FLAT PLATE RADIOMETER
131: SCANNING RADIOMETER SUN SHIELD

Figure 2-III-8. Component Thermal Model for 131-Body Analysis

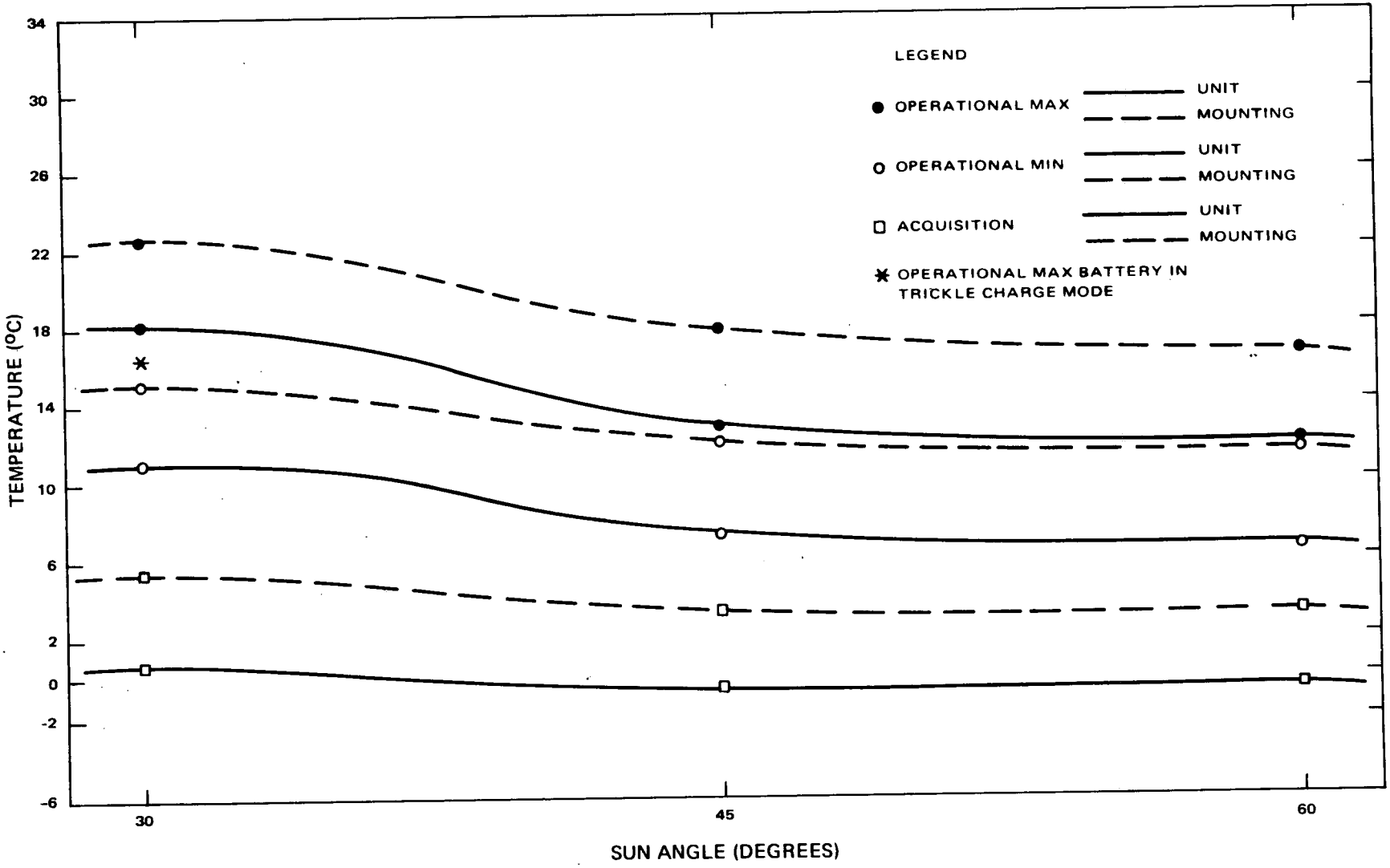


Figure 2-III-9. Flight Predictions Temperatures Versus Sun Angles for Scanning Radiometer

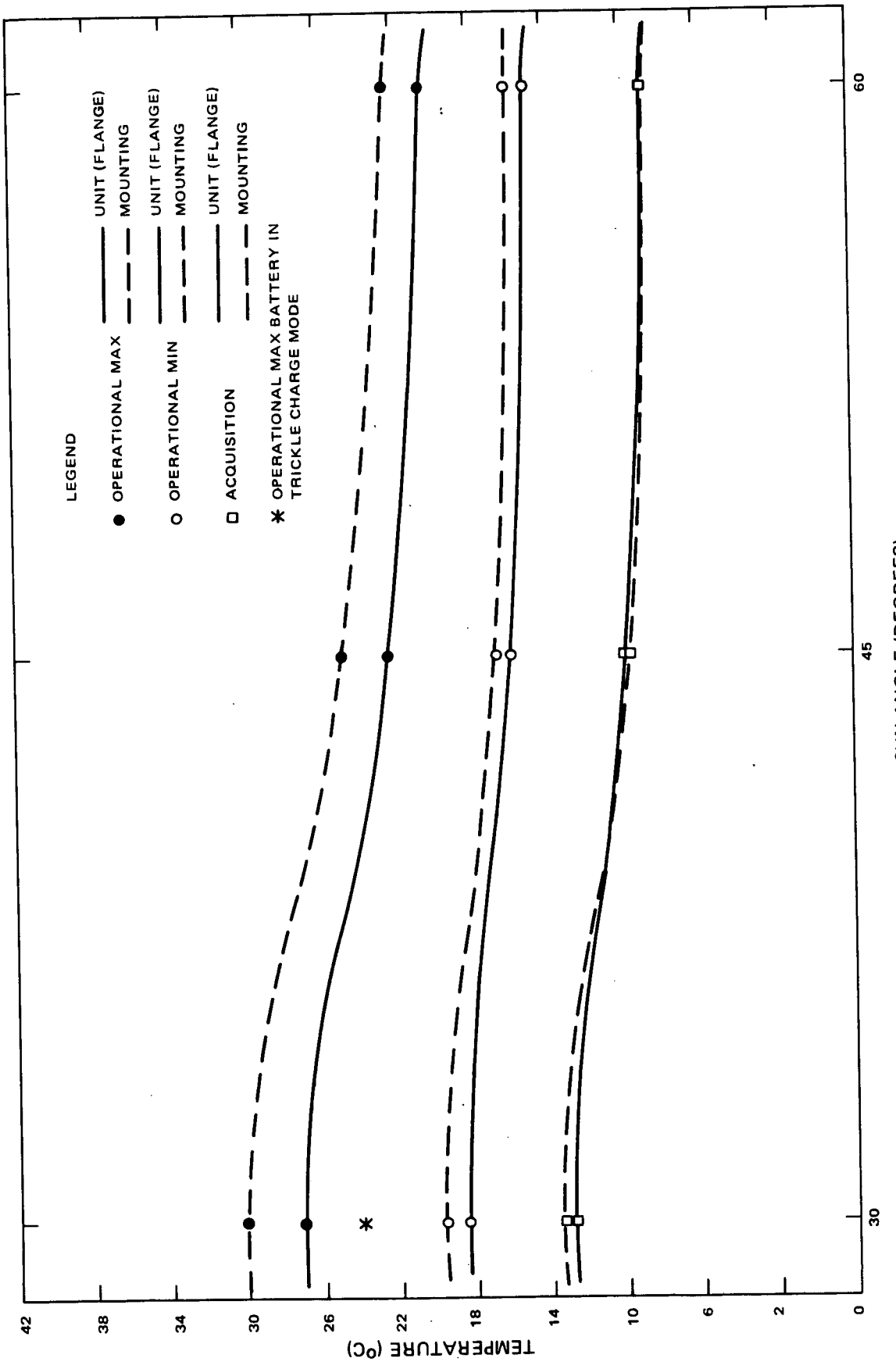


Figure 2-III-10. Flight Predictions Temperatures Versus Sun Angles for Momentum Wheel Assembly

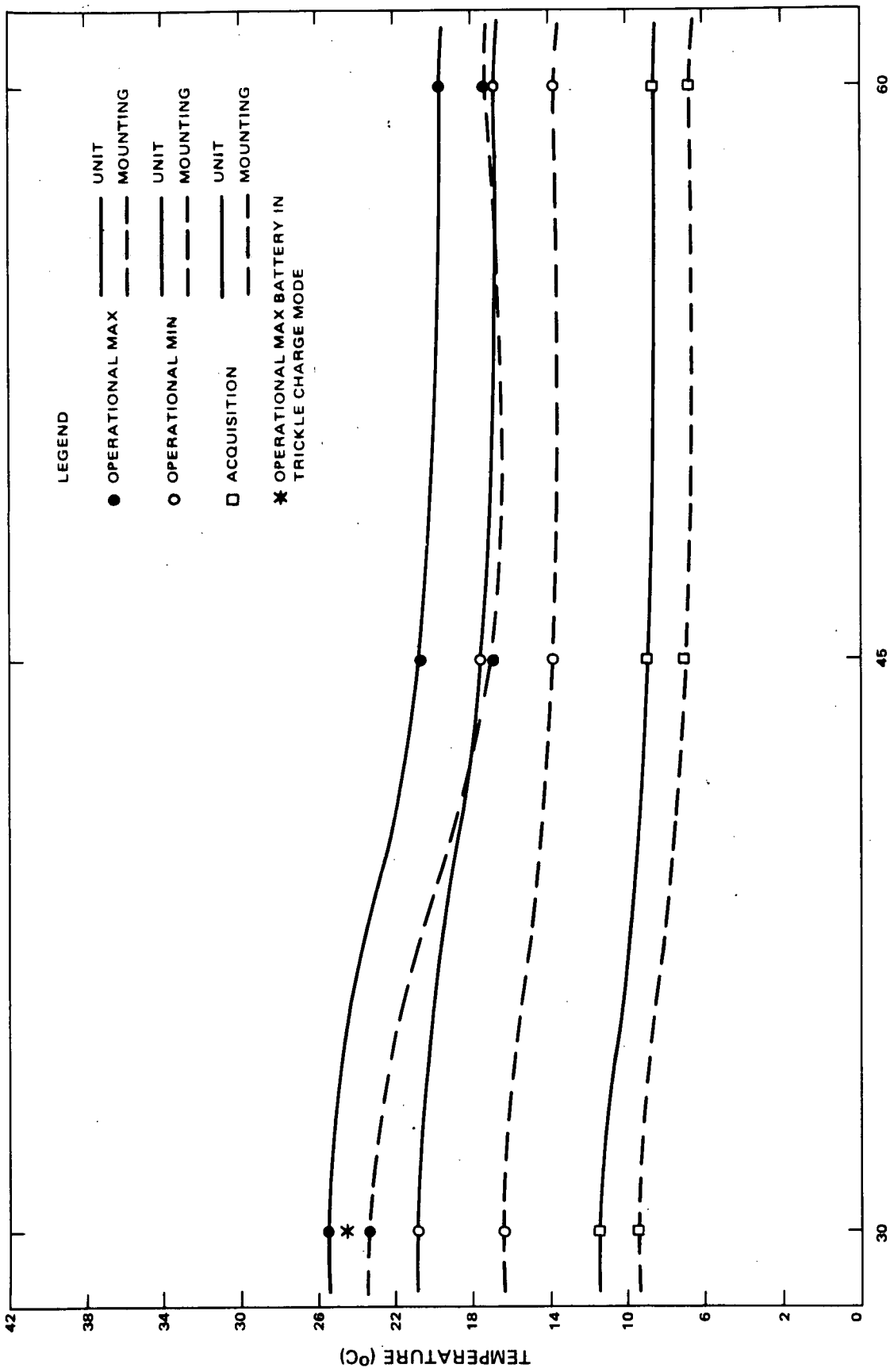


Figure 2-III-11. Flight Predictions Temperatures Versus Sun Angles for APT Camera

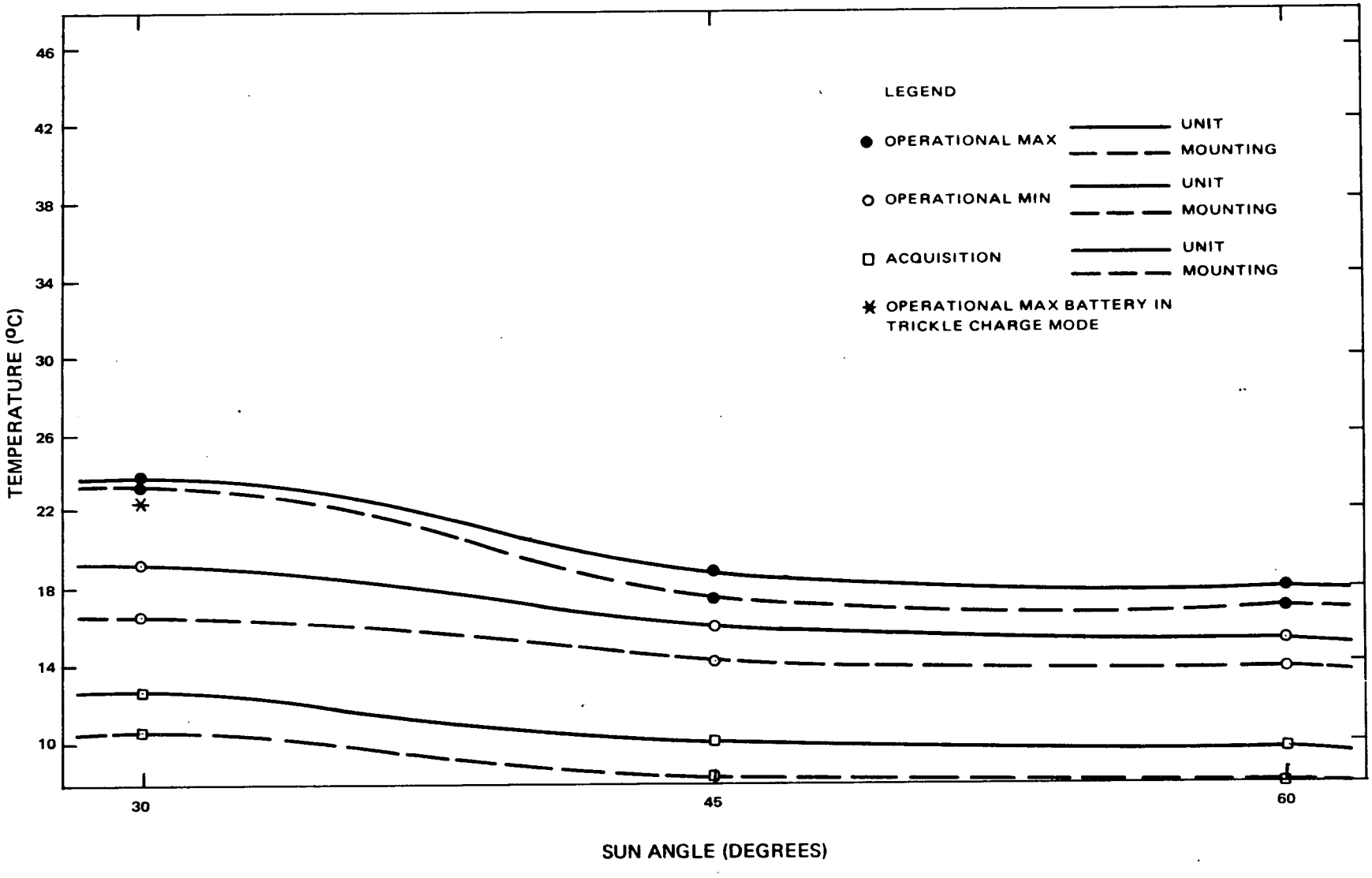


Figure 2-III-12. Flight Predictions Temperatures Versus Sun Angles for AVCS Camera

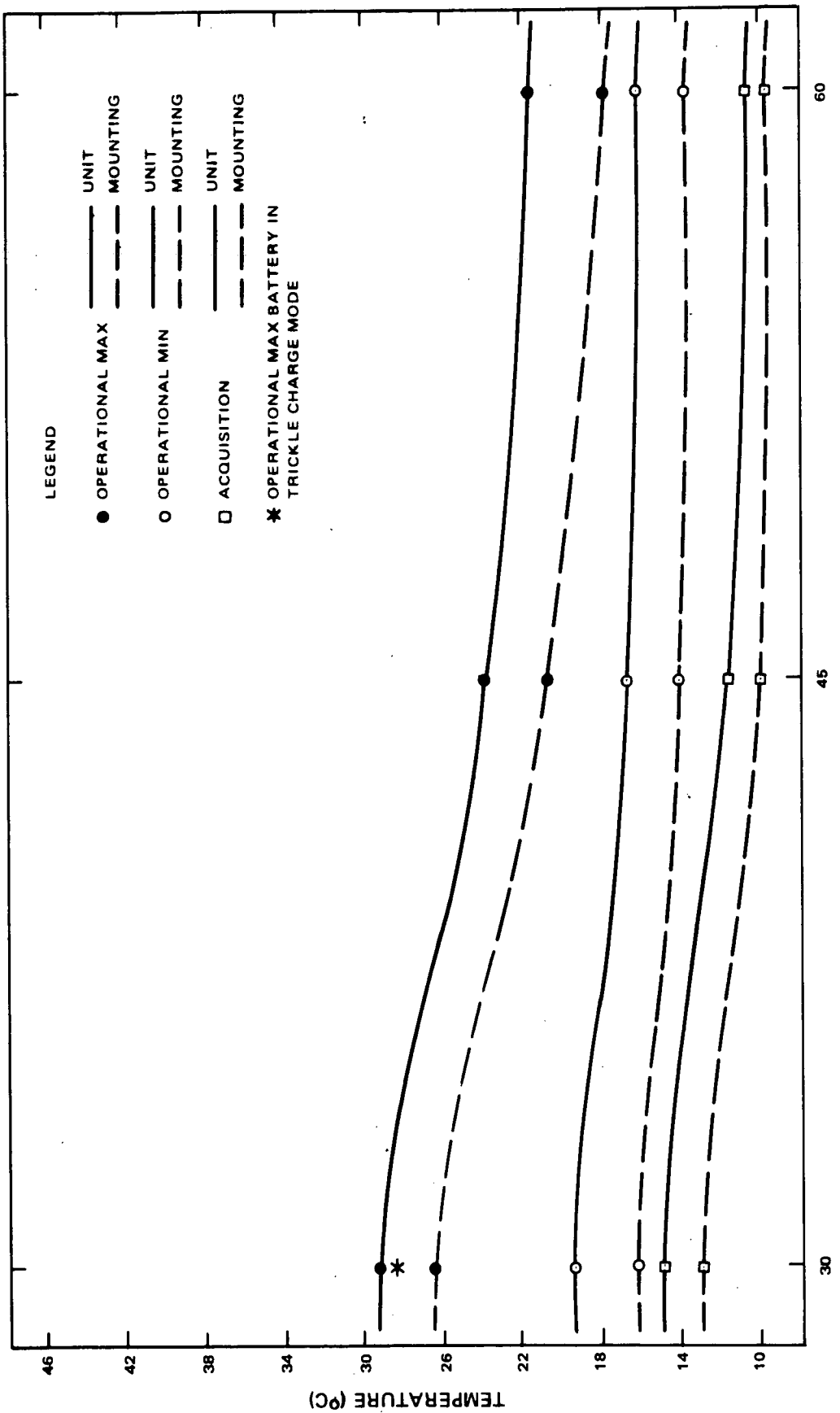


Figure 2-III-13. Flight Predictions Temperatures Versus Sun Angles for SR Recorder

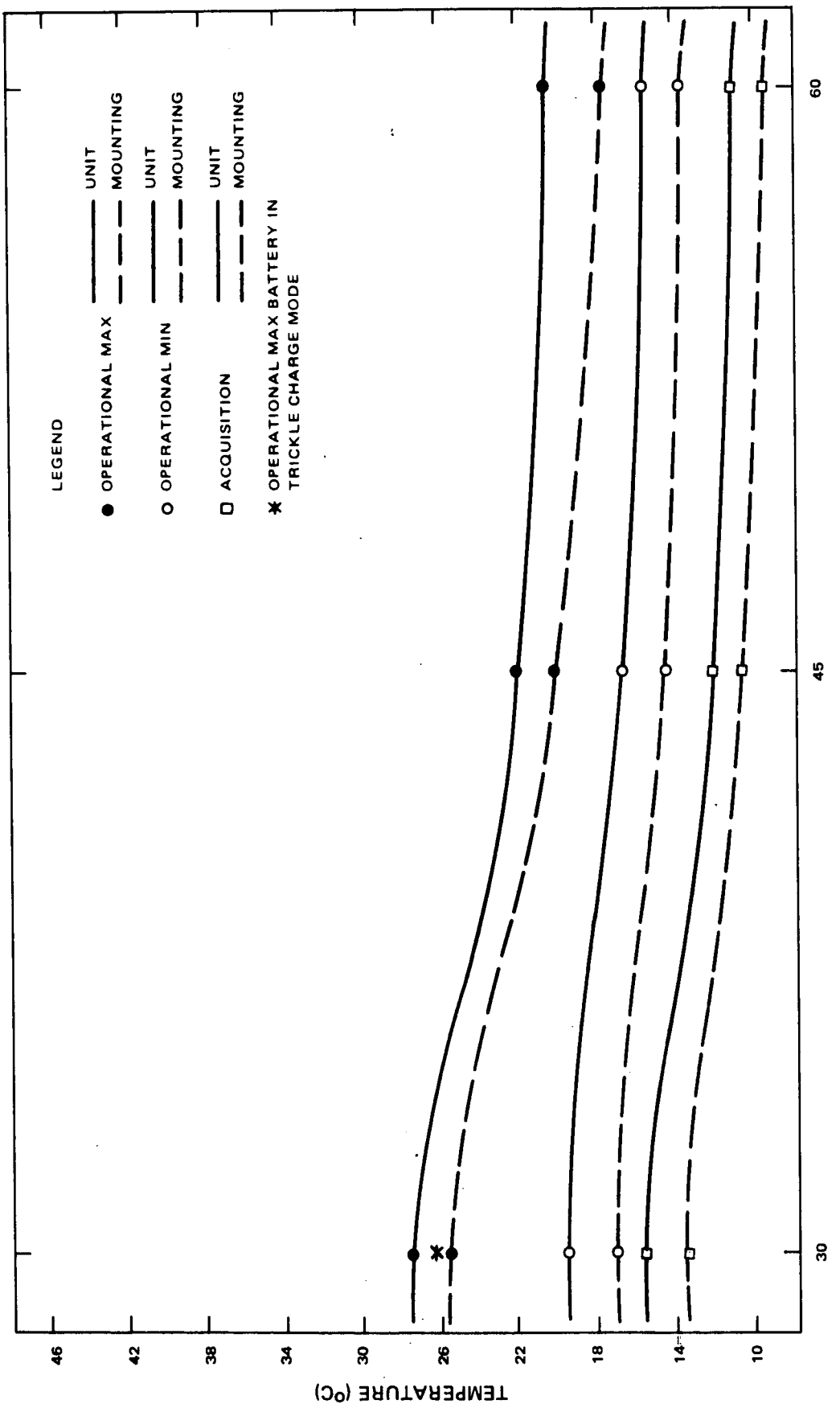


Figure 2-III-14. Flight Predictions Temperatures Versus Sun Angles for AVCS Recorder

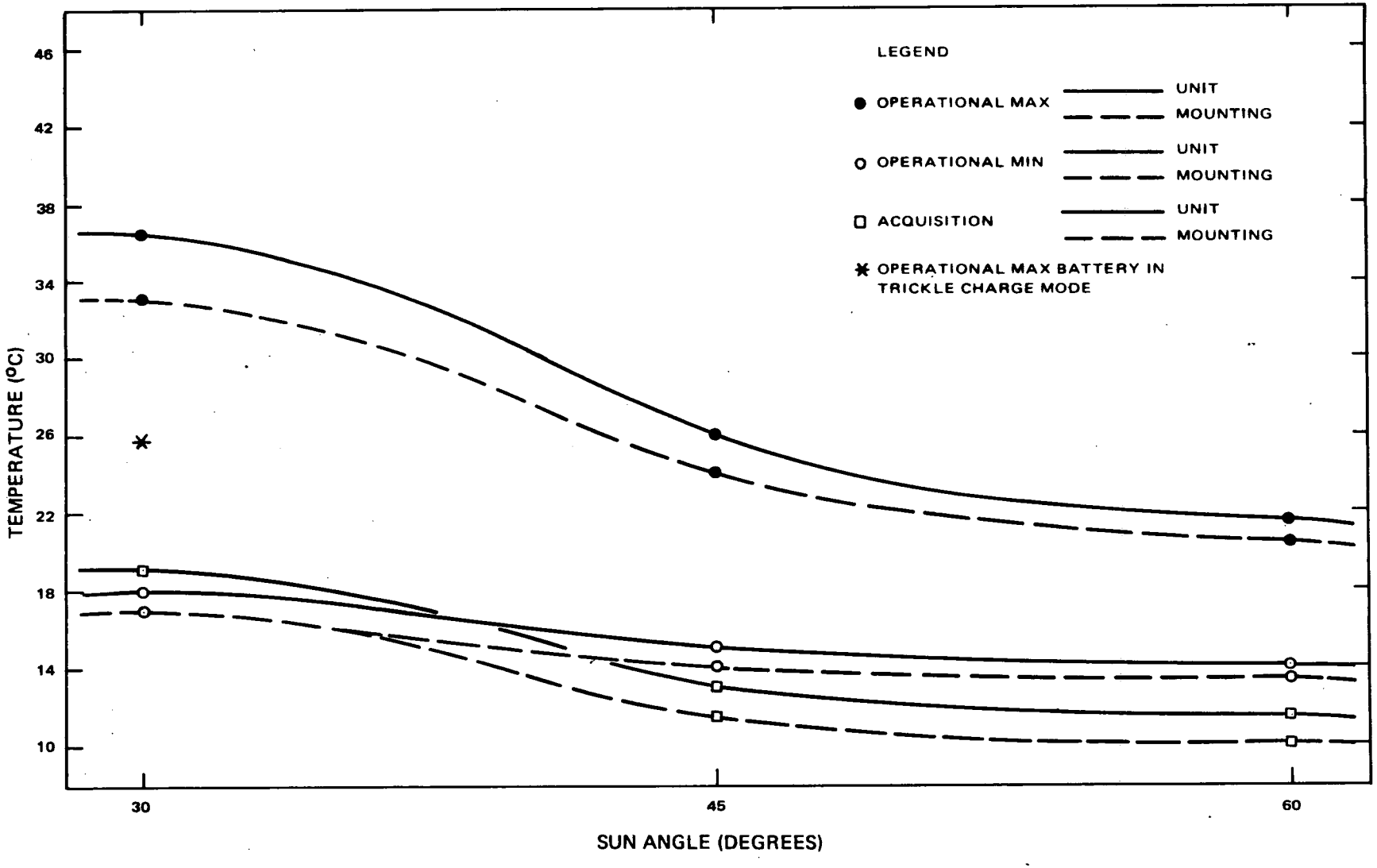


Figure 2-III-15. Flight Predictions Temperatures Versus Sun Angles for Battery

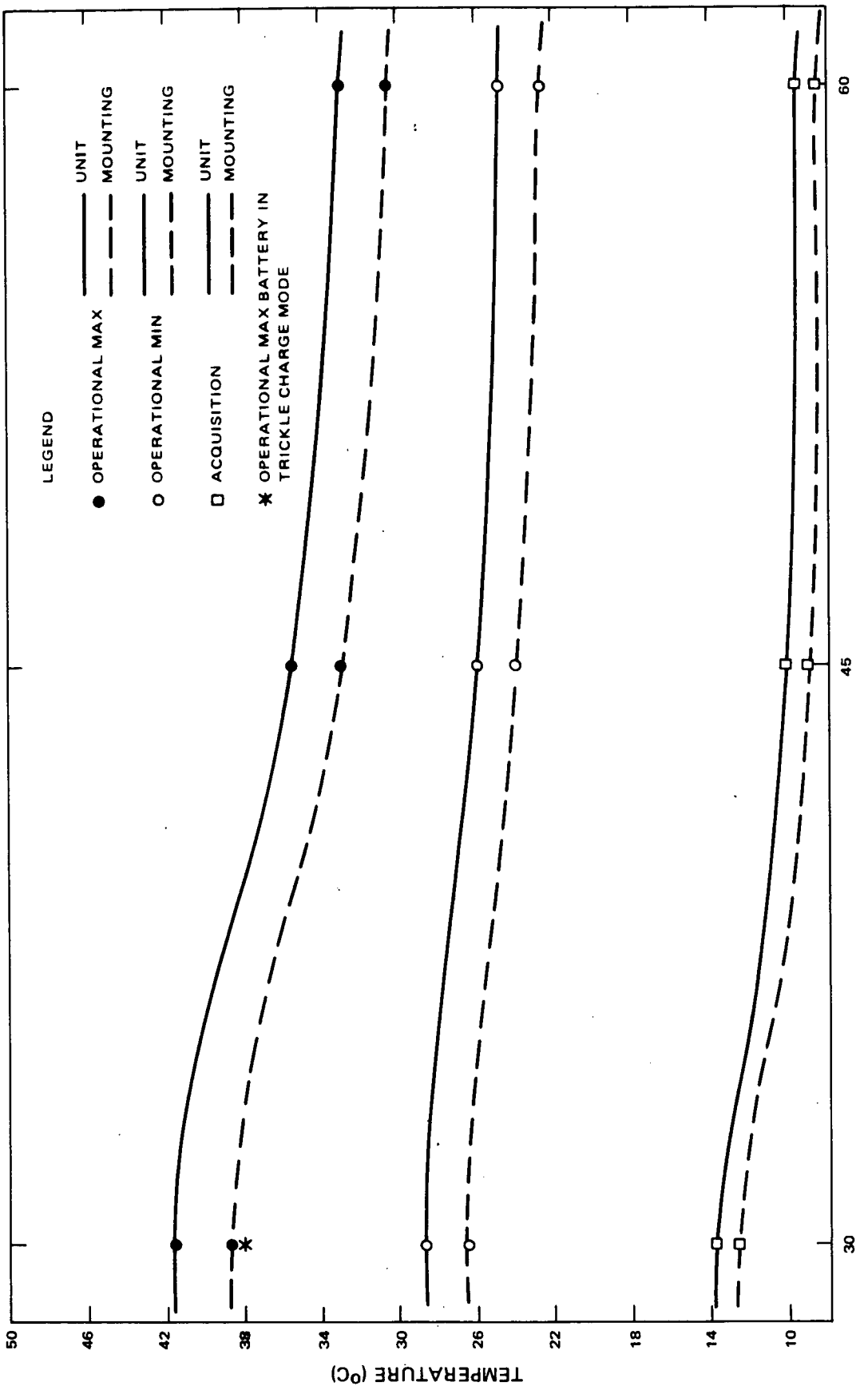


Figure 2-III-16. Flight Predictions Temperatures Versus Sun Angles for Power Supply Electronics

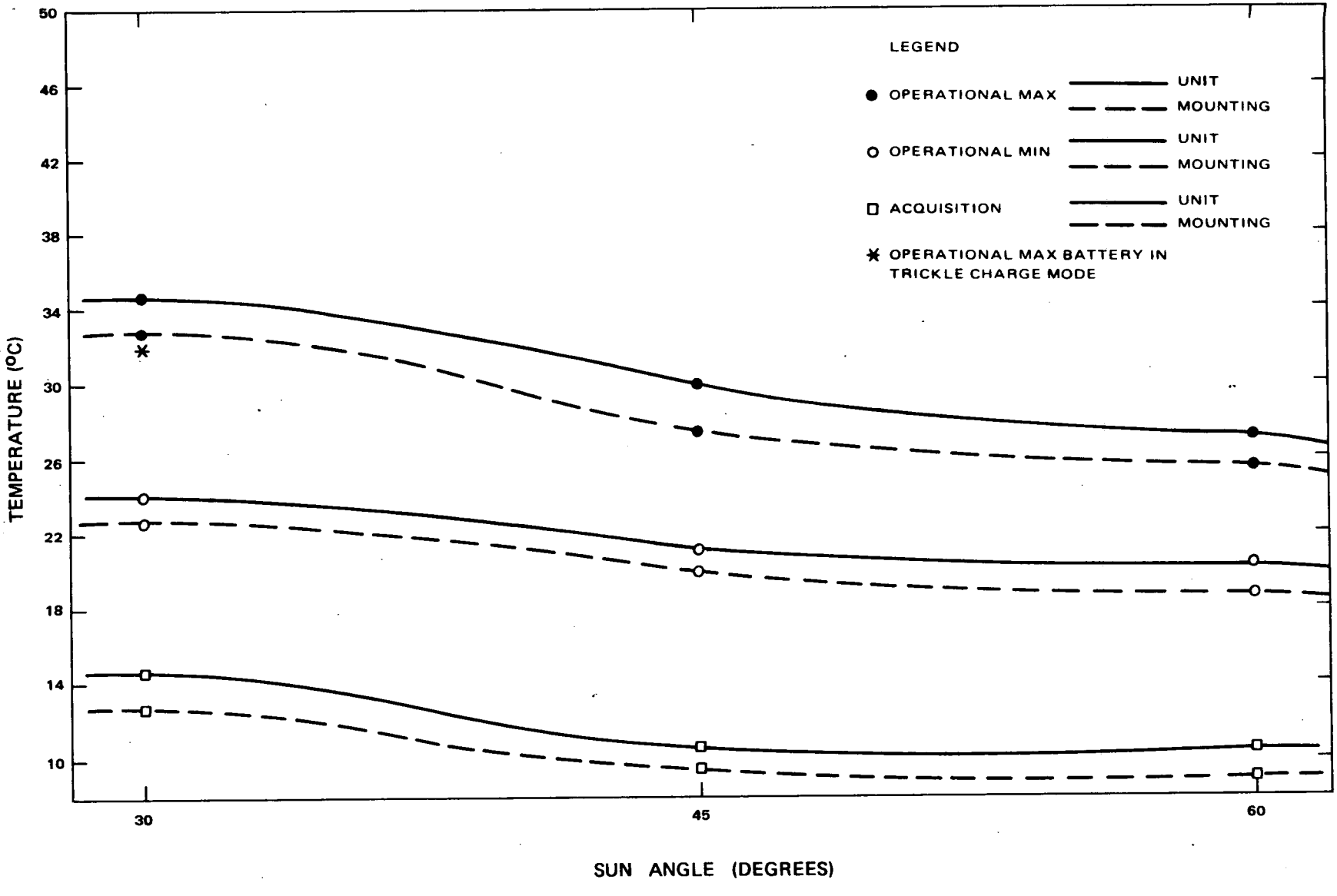


Figure 2-III-17. Flight Predictions Temperatures Versus Sun Angles for Pitch Control Electronics

TABLE 2-III-3. OPERATIONAL AND ACQUISITION MODE FLIGHT TEMPERATURE PREDICTIONS

Node \ Sun Angle (degrees) →	Operational Mode							Acquisition Mode		
	Maximum with Normal Battery Charge (°C)			Max with Trickle Charge (°C)	Minimum with Normal Battery Charge (°C)			Nominal Power Panels Deployed, Spinning (°C)		
	30	45	60	30	30	45	60	30	45	60
1	28.0	23.0	21.5	25.7	19.4	16.5	15.7	9.2	6.4	6.1
2	27.7	22.8	21.4	25.5	18.9	15.9	15.2	8.9	6.2	5.9
3	29.3	24.6	23.4	27.2	19.6	16.7	16.1	8.3	5.8	5.5
4	41.6	35.6	33.0	38.2	28.7	26.0	24.8	13.8	10.1	9.4
5	34.6	29.0	26.8	31.8	24.4	21.3	20.3	14.7	11.4	10.7
6	28.7	23.8	22.4	26.0	19.9	17.2	16.6	10.4	7.6	7.2
7	23.2	18.7	17.8	20.6	15.8	13.3	13.1	8.9	6.3	6.1
8	27.3	22.3	20.1	23.1	17.0	14.7	14.3	12.4	8.6	8.0
9	30.4	25.5	22.3	26.2	19.5	16.8	16.0	13.9	9.1	8.3
10	31.3	25.2	22.5	26.6	20.1	17.2	16.3	16.1	11.6	10.5
11	31.8	25.5	23.2	27.2	20.8	17.9	17.0	16.8	12.6	11.5
12	27.5	23.4	21.9	25.3	16.6	14.0	13.3	13.9	10.7	10.0
13	29.6	24.4	22.8	26.3	20.3	17.6	17.1	13.1	9.8	9.1
14	27.1	20.7	18.9	21.7	16.1	13.7	13.5	13.2	9.5	8.7
15	36.6	26.2	21.7	26.2	18.4	15.2	14.1	19.8	13.4	11.7
16	31.5	24.0	20.7	25.3	18.8	15.6	14.3	17.1	11.9	10.3
17	32.4	25.1	21.8	26.6	19.9	16.6	15.3	18.0	12.9	11.3
18	31.9	24.6	21.4	26.5	20.1	16.7	15.2	17.9	12.8	11.0
19	32.0	24.4	21.4	25.8	19.5	16.2	15.1	16.1	11.1	9.6
20	36.3	25.5	21.3	25.4	18.1	15.0	14.1	19.3	13.1	11.4
21	27.8	22.3	20.8	24.2	19.5	16.8	16.1	15.2	11.6	10.6
22	29.3	25.3	24.4	28.0	21.6	18.8	17.9	13.8	10.5	9.6
23	27.1	23.1	22.2	25.9	21.0	18.1	17.1	14.2	10.8	9.8
24	29.4	23.9	21.6	28.7	26.6	22.0	19.8	22.5	17.8	15.8

TABLE 2-III-3. OPERATIONAL AND ACQUISITION MODE FLIGHT TEMPERATURE PREDICTIONS (Continued)

Node \ Sun Angle (degrees) →	Operational Mode							Acquisition Mode		
	Maximum with Normal Battery Charge (°C)			Max with Trickle Charge (°C)	Minimum with Normal Battery Charge (°C)			Nominal Power Panels Deployed, Spinning (°C)		
	30	45	60	30	30	45	60	30	45	60
25	25.2	20.6	20.1	24.0	20.9	17.4	16.9	11.5	8.9	8.7
26	29.2	25.3	25.5	28.2	25.1	22.3	22.0	13.6	10.2	9.6
27	25.6	20.6	19.8	24.7	22.5	18.5	17.6	15.1	11.9	11.3
28	36.0	32.0	32.0	34.9	32.0	29.1	28.7	14.7	11.2	10.4
29	28.1	22.4	19.9	27.5	25.9	21.1	18.6	22.0	16.9	14.8
30	25.8	20.6	19.1	23.2	19.5	16.4	15.4	15.7	12.1	11.0
31	21.1	18.6	19.8	18.8	15.0	14.5	16.1	11.0	10.2	11.2
32	23.7	19.2	18.6	22.5	19.5	16.2	15.6	13.0	9.9	9.4
33	23.5	18.8	18.3	22.3	19.4	15.9	15.3	12.8	10.1	9.8
34	27.5	22.2	20.4	26.4	24.1	20.0	18.3	20.1	16.0	14.3
35	24.7	20.2	20.0	23.6	21.0	17.9	17.3	15.6	12.2	11.5
36	23.8	18.8	18.0	22.7	20.3	16.4	15.6	14.3	11.2	10.7
37	27.6	22.1	20.4	23.3	16.3	13.9	13.4	16.2	12.9	12.0
38	26.0	21.5	21.1	25.0	22.3	19.1	18.5	15.7	12.2	11.6
39	25.0	20.5	20.3	23.9	21.6	18.3	17.8	16.3	12.8	12.1
40	27.3	21.5	19.1	26.6	24.9	20.1	17.8	21.5	16.6	14.6
41	24.6	19.0	16.6	23.9	22.3	17.6	15.3	18.9	14.2	12.3
42	28.0	21.9	19.2	27.4	25.7	20.6	18.0	22.5	17.9	15.9
43	26.5	20.8	17.8	26.2	24.6	19.5	16.5	21.1	15.8	13.1
44	26.3	22.5	21.7	25.1	20.3	17.6	16.7	13.4	10.2	9.2
45	24.7	19.4	18.4	20.6	16.2	14.0	13.8	13.1	10.0	9.3
46	27.1	20.6	17.3	26.8	25.3	19.6	16.4	21.7	15.7	13.2
47	28.3	24.5	24.8	27.3	24.4	21.7	21.4	13.3	10.0	9.3
48	18.4	16.5	18.5	16.1	12.9	13.0	15.2	9.7	9.6	10.9

TABLE 2-III-3. OPERATIONAL AND ACQUISITION MODE FLIGHT TEMPERATURE PREDICTIONS (Continued)

Node \ Sun Angle (degrees) →	Operational Mode							Acquisition Mode		
	Maximum with Normal Battery Charge (°C)			Max with Trickle Charge (°C)	Minimum with Normal Battery Charge (°C)			Nominal Power Panels Deployed, Spinning (°C)		
	30	45	60	30	30	45	60	30	45	60
49	25.6	19.8	16.8	25.3	23.9	18.8	16.0	20.2	14.8	12.4
50	21.4	17.5	17.2	20.6	18.7	15.7	15.1	11.4	8.3	7.7
51	19.2	15.9	16.0	17.4	13.7	12.0	12.3	7.5	5.7	5.9
52	24.6	19.4	18.2	20.5	15.2	13.1	12.8	13.9	10.9	10.3
53	21.0	16.7	15.7	19.4	17.2	14.3	13.4	13.4	10.4	9.5
54	25.7	20.1	17.5	25.2	23.6	18.8	16.3	20.2	15.6	13.2
55	19.8	17.6	19.2	17.5	13.9	13.7	15.6	10.5	10.1	11.2
56	24.1	19.7	19.7	23.0	20.6	17.5	17.1	15.2	11.8	11.2
57	26.7	20.4	17.5	26.2	24.7	19.3	16.6	21.8	16.5	14.3
58	20.8	17.3	17.3	18.9	14.7	13.0	13.1	8.4	6.3	6.5
59	22.1	17.8	17.3	21.1	18.6	15.3	14.7	12.8	9.7	9.2
60	25.8	19.9	17.2	25.2	23.7	18.7	16.1	20.6	15.5	13.3
61	32.7	23.4	20.0	23.8	17.1	14.2	13.3	16.8	11.4	9.9
62	30.9	23.3	20.2	24.6	18.2	15.1	14.0	15.7	10.7	9.2
63	30.5	23.3	20.2	24.9	18.5	15.3	14.0	16.3	11.3	9.6
64	31.4	23.9	20.5	25.1	18.5	15.3	14.1	16.8	11.6	10.1
65	33.1	24.3	20.4	24.7	17.5	14.5	13.4	17.4	11.8	10.2
66	27.2	20.5	18.5	21.4	15.7	13.2	12.9	13.1	9.1	8.3
67	30.6	24.2	21.9	25.7	19.5	16.6	15.8	15.5	11.3	10.2
68	30.5	24.3	21.6	25.7	19.2	16.3	15.4	15.3	10.9	9.7
69	29.3	23.4	20.3	24.2	17.7	14.9	14.1	13.9	9.2	8.2
70	28.7	22.2	19.3	22.9	16.5	13.8	13.1	13.7	9.1	8.1

TABLE 2-III-3. OPERATIONAL AND ACQUISITION MODE FLIGHT TEMPERATURE PREDICTIONS (Continued)

Sun Angle (degrees) / Node	Operational Mode							Acquisition Mode		
	Maximum with Normal Battery Charge (°C)			Max with Trickle Charge (°C)	Minimum with Normal Battery Charge (°C)			Nominal Power Panels Deployed, Spinning (°C)		
	30	45	60	30	30	45	60	30	45	60
71	23.8	18.4	17.1	19.4	14.3	12.1	12.0	10.2	7.1	6.7
72	29.2	23.8	22.2	25.7	19.7	17.0	16.4	12.8	9.4	8.7
73	30.2	24.9	22.6	26.5	19.7	16.9	16.2	13.6	9.7	8.9
74	30.1	25.4	22.0	25.9	19.1	16.5	15.8	13.5	8.7	7.9
75	27.2	22.1	19.7	22.9	16.7	14.4	13.9	12.0	8.1	7.4
76	22.2	17.6	16.7	19.5	14.5	12.1	11.9	7.5	5.1	4.9
77	27.8	22.8	21.4	25.0	18.9	16.2	15.6	10.0	7.1	6.7
78	32.8	27.4	25.3	30.0	22.7	19.8	18.8	12.7	9.5	8.9
79	38.7	33.0	30.5	35.4	26.4	23.8	22.7	12.7	9.1	8.4
80	29.4	24.4	22.6	26.4	19.5	17.1	16.4	9.5	6.4	6.0
81	21.6	17.0	16.0	19.3	14.2	11.5	11.1	5.9	3.6	3.4
82	24.3	19.5	18.2	22.0	16.2	13.3	12.6	6.7	4.2	4.0
83	25.2	20.2	18.8	22.9	16.9	13.9	13.2	7.0	4.5	4.2
84	26.8	21.8	20.2	24.4	18.0	15.1	14.3	7.4	4.8	4.5
85	24.5	19.7	18.3	22.0	16.2	13.5	12.9	6.7	4.2	3.9
86	22.8	17.9	16.6	20.7	15.2	12.1	11.4	5.6	3.3	3.2
87	25.4	20.5	19.4	23.5	19.1	15.9	15.2	11.0	8.2	7.9
88	28.9	23.3	21.6	27.8	25.6	21.1	19.5	20.4	16.8	15.8
89	30.3	22.2	18.3	25.9	20.8	16.0	13.4	18.7	12.7	9.7
90	28.2	23.0	21.5	26.2	22.5	19.0	17.9	17.7	13.8	12.7
91	30.0	24.7	22.9	29.0	26.7	22.4	20.8	22.7	18.3	16.8
92	42.8	38.0	36.6	42.1	40.5	36.5	35.2	38.1	34.0	32.9
93	28.0	22.5	20.2	27.2	25.3	20.7	18.6	21.4	16.9	15.1
94	24.4	19.2	18.1	20.4	15.9	13.8	13.6	12.9	9.9	9.2

TABLE 2-III-3. OPERATIONAL AND ACQUISITION MODE FLIGHT TEMPERATURE PREDICTIONS (Continued)

Sun Angle (degrees) / Node	Operational Mode							Acquisition Mode		
	Maximum with Normal Battery Charge (°C)			Max with Trickle Charge (°C)	Minimum with Normal Battery Charge (°C)			Nominal Power Panels Deployed, Spinning (°C)		
	30	45	60	30	30	45	60	30	45	60
95	19.0	15.7	15.8	17.1	13.5	11.8	12.1	7.4	5.6	5.8
96	24.3	19.2	17.9	20.3	15.0	12.9	12.6	13.7	10.8	10.1
97	20.6	17.1	17.1	18.6	14.5	12.8	12.9	8.2	6.1	6.4
98	50.4	45.8	44.8	49.9	48.9	44.8	43.9	47.3	43.2	42.4
99	32.9	11.3	-5.7	32.7	32.3	10.9	-6.2	31.8	10.2	-7.0
100	126.7	89.1	60.8	126.5	126.3	88.8	60.4	125.9	88.3	59.8
101	-4.9	0.8	3.9	0.1	4.8	5.1	5.8	4.4	4.1	4.7
102	8.1	9.2	9.2	9.7	11.4	10.2	10.0	6.1	5.9	6.4
103	-7.3	-1.0	3.2	-2.2	3.8	4.2	5.1	4.7	4.4	5.0
104	5.1	6.1	6.1	6.7	9.2	7.8	7.5	6.1	6.1	6.8
105	-68.0	-71.3	-72.2	-70.7	-74.4	-75.7	-75.7	-77.7	-79.5	-79.6
106	-76.0	-77.7	-77.9	-77.7	-80.6	-80.9	-80.4	-83.8	-84.4	-83.8
107	-14.0	-28.5	-38.8	-13.7	-15.2	-29.3	-38.9	-10.7	-24.8	-33.9
108	-32.0	-38.2	-40.8	-31.8	-33.0	-38.7	-40.9	-28.0	-32.3	-27.5
109	-47.8	-46.9	-41.4	-46.4	-45.2	-45.5	-40.4	-39.1	-34.6	-24.2
110	-51.0	-39.0	-12.1	-51.2	-52.0	-39.5	-12.4	-40.5	-29.3	-8.7
111	-22.1	-37.9	-47.7	-29.9	-23.7	-38.9	-47.9	-12.6	-27.3	-36.8
112	-42.0	-45.7	-37.4	-42.0	-43.5	-46.5	-37.6	-32.1	-38.1	-35.3
113	-57.7	-47.3	-27.6	-57.8	-59.1	-48.0	-27.8	-44.0	-40.3	-28.9
114	-60.1	-42.3	-10.5	-60.3	-61.4	-42.8	-10.7	-37.6	-29.3	-10.7
115	-13.9	-28.5	-38.8	-13.7	-15.2	-29.3	-38.9	-10.7	-24.9	-33.9
116	-31.9	-38.1	-40.7	-31.7	-32.9	-38.6	-40.8	-28.1	-32.3	-27.6
117	-47.1	-46.1	-40.8	-45.6	-44.7	-45.0	-40.0	-39.2	-34.7	-24.3
118	-51.1	-39.0	-12.2	-51.2	-52.0	-39.5	-12.4	-40.5	-29.3	-8.8

TABLE 2-III-3. OPERATIONAL AND ACQUISITION MODE FLIGHT TEMPERATURE PREDICTIONS (*Continued*)

Sun Angle (degrees) / Node	Operational Mode							Acquisition Mode		
	Maximum with Normal Battery Charge (°C)			Max with Trickle Charge (°C)	Minimum with Normal Battery Charge (°C)			Nominal Power Panels Deployed, Spinning (°C)		
	30	45	60	30	30	45	60	30	45	60
119	5.3	-5.1	-7.8	5.3	5.1	-5.3	-8.0	-20.6	-14.0	-8.6
120	47.9	20.5	-4.4	48.4	46.1	19.3	-4.4	49.0	21.6	-2.6
121	46.5	18.2	-7.5	46.9	44.4	16.9	-7.5	48.7	21.2	-3.0
122	47.9	20.5	-4.4	48.4	46.1	19.3	-4.4	49.0	21.7	-2.5
123	21.7	17.4	17.0	18.7	14.7	12.8	12.9	10.2	7.7	7.5
124	22.4	18.2	17.5	19.5	14.7	12.8	12.8	11.0	8.5	8.2
125	-115.3	-116.1	-115.5	-116.9	-118.9	-118.4	-117.3	-122.4	-122.3	-121.2
126	-48.7	-50.0	-49.7	-50.4	-52.9	-52.8	-51.9	-55.1	-55.3	-54.4
127	24.3	12.3	9.4	24.1	23.8	11.9	9.1	4.0	9.8	15.6
128	18.2	12.9	11.7	16.4	11.4	7.5	6.8	0.7	-0.7	-0.5
129	17.6	12.3	11.1	15.8	11.1	7.3	6.5	0.7	-0.7	-0.5
130	4.5	3.9	-1.1	3.2	-0.9	-0.4	-5.1	-15.3	-16.0	-15.2
131	23.9	9.0	1.9	23.7	23.0	8.3	1.1	15.0	10.2	10.4

10. Acquisition Mode Flight Temperature Predictions

Included in Figures 2-III-9 through 2-III-17 and Table 2-III-3 are acquisition mode temperature predictions. The acquisition mode is that period of the mission between solar panel deployment, executed during the fifth orbit at which time the spacecraft pitch axis is essentially aligned with the orbit normal, and the initiation of pitch lock during a subsequent orbit. A spacecraft spin rate of no less than 0.1 rpm and a level of electrical power dissipation significantly lower than that for the operational case distinguish the acquisition mode. In the operational mode, by definition, the spacecraft rotates at an angular rate of 1 revolution per orbit, precluding the averaging of external heat inputs attending acquisition mode operation. The results presented comprise orbit-average, steady-state predictions derived with the aid of the test-correlated 131-body spacecraft thermal model and conform, without exception, to the design temperature requirements, indicating that the spacecraft could accommodate acquisition mode operation for an indefinite period.

11. Solar Panel Flight Temperature Predictions

A 101-body analytical model was devised for the spacecraft solar panels to predict the transient thermal behavior of these items during the multiple phases of the mission. The model is shown in Figure 2-III-18. The results derived with the aid of this model are presented in Figures 2-III-19 through 2-III-24. Figure 2-III-19 shows thermal envelopes defining the anticipated temperature extremes to which the shunt dissipator elements (i.e., the transistors and resistors) and the solar cells would be subjected during the initial phase of the mission, from launch to spacecraft separation. These results were predicated on realization of the mission profile published in Douglas Report DAC-61864, "Detailed Test Objectives for Long Tank Delta (Six-Solids Retrofit) Launch Vehicle, Spacecraft: TIROS M", dated May 1969, and were relevent for a launch in the time period Oct. 1 to Nov. 1, 1969, resulting in a 1500-hour ascending node orbit. The thermal envelopes presented in Figures 2-III-20, 2-III-21, and 2-III-22 are extensions of those displayed in Figure 2-III-19; the time frame for Figures 2-III-20 through 2-III-22 is from spacecraft separation to solar panel deployment. The low temperature boundaries define the thermal behavior of AVCS solar panel elements attending an October 1 launch, whereas the high temperature boundaries characterize the thermal behavior of anti-earth solar panel elements attending a November 1 launch. In both cases, the spacecraft spin axis was assumed to be aligned at all times with the orbit normal so that unique values of spacecraft sun angle could be utilized throughout the individual analyses. This expedient had the effect of suppressing the short term transients associated with spin axis erection which were appraised as being of little consequence over a time span approximating five orbits. The operational mode transient temperature predictions for solar panel elements recorded in

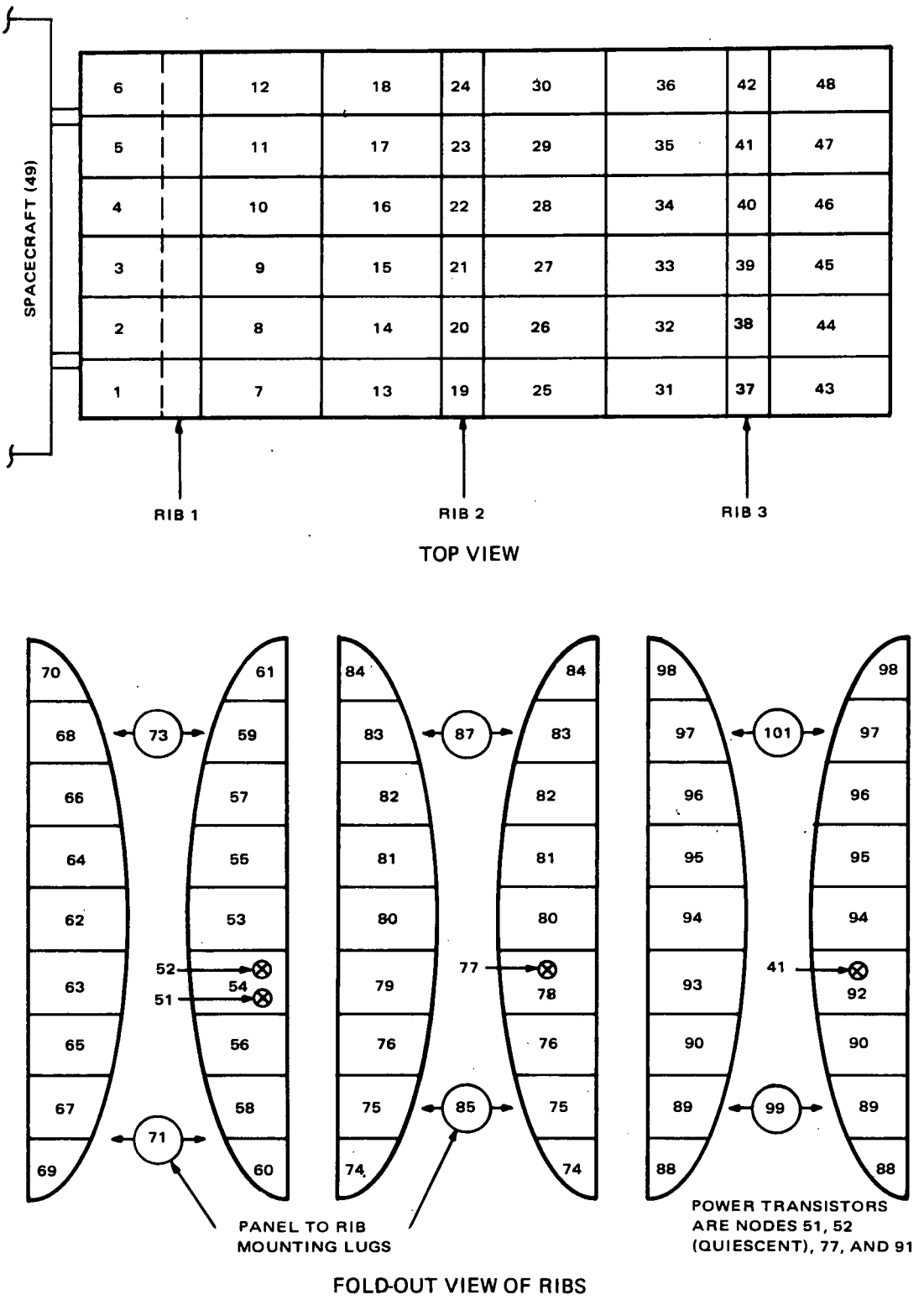


Figure 2-III-18. Solar Panel Thermal Analysis Model

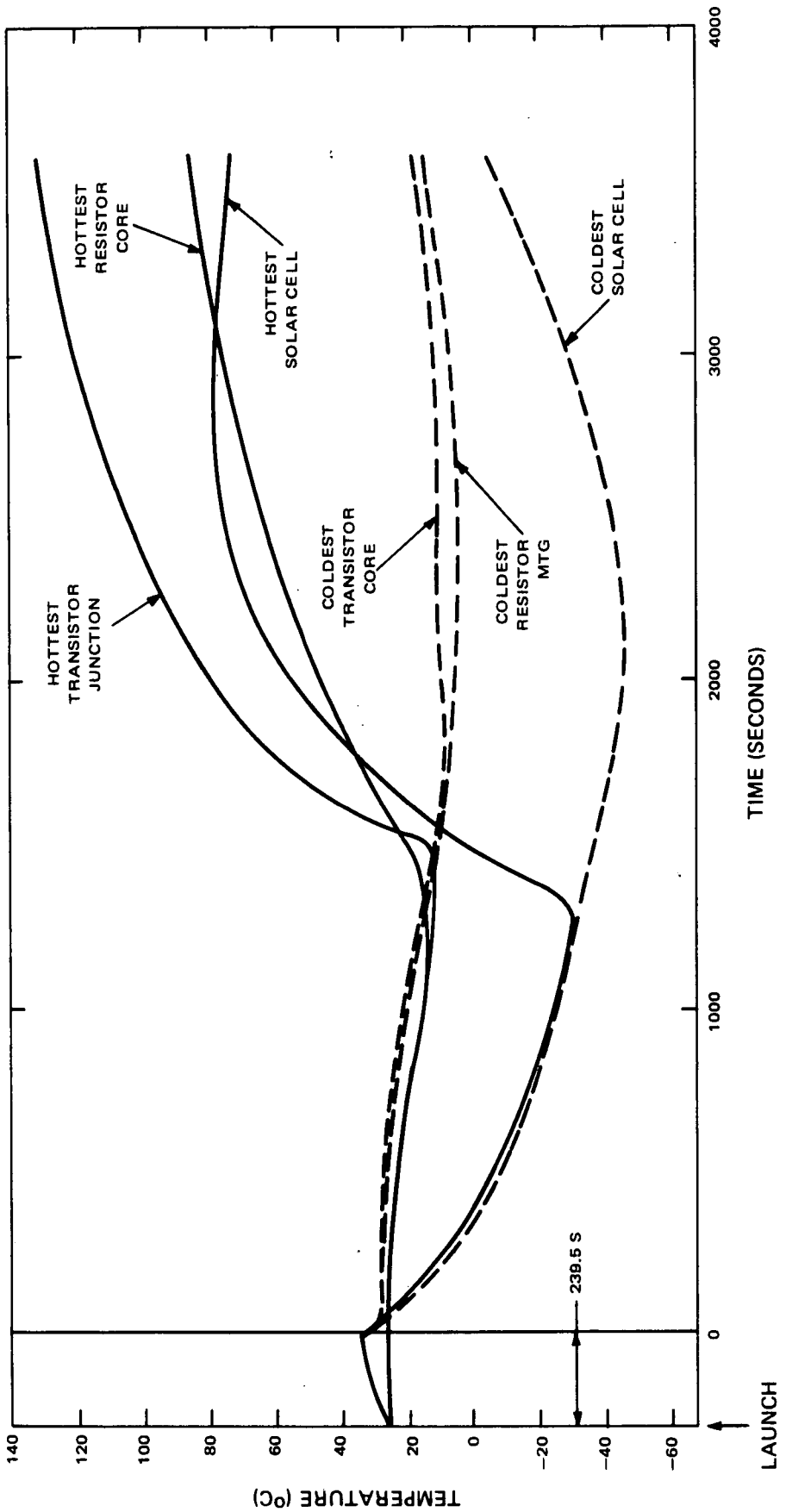


Figure 2-III-19. Solar Panel Temperatures, Launch to Separation

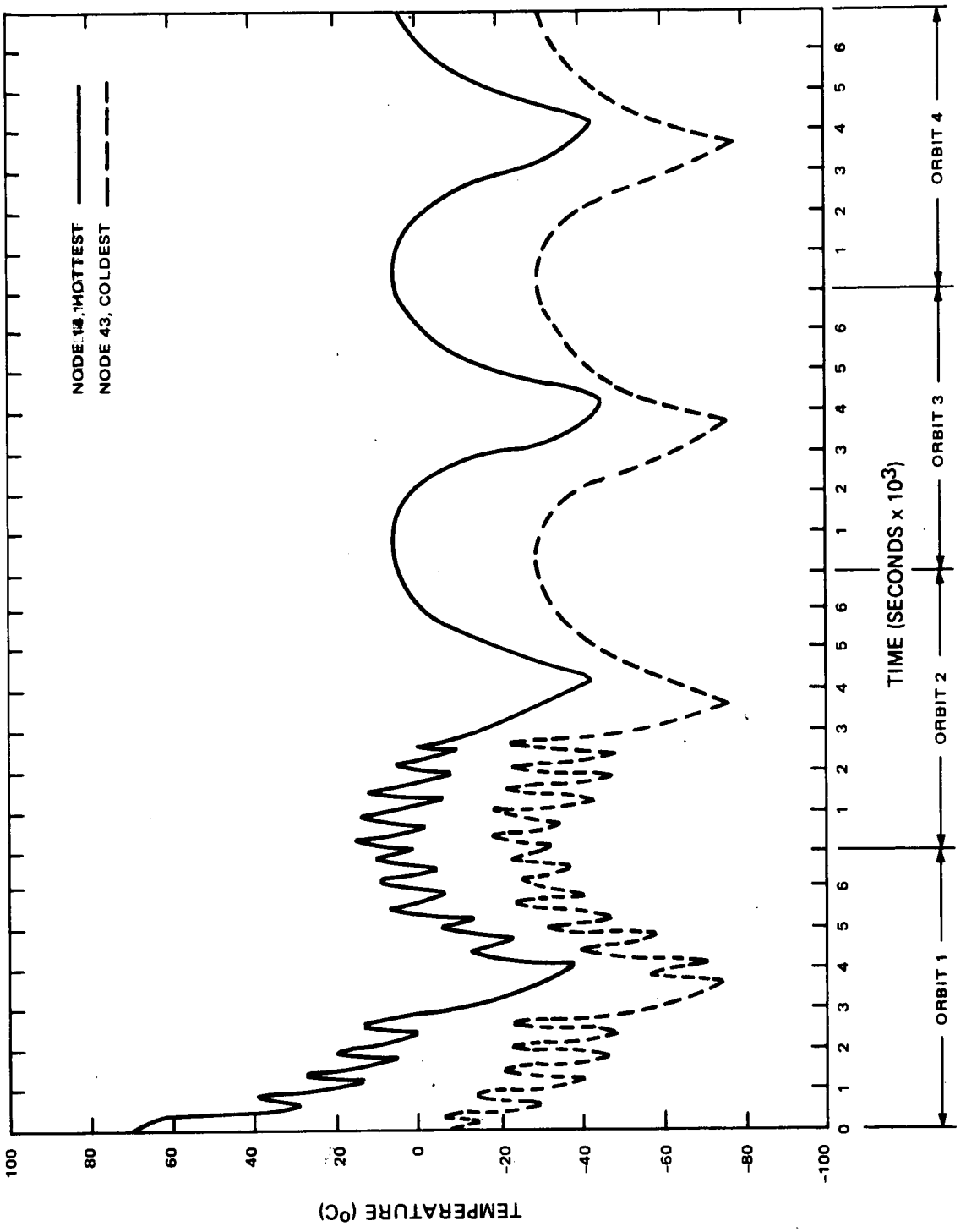


Figure 2-III-20. Solar Cell Temperature Prior to Solar Panel Deployment

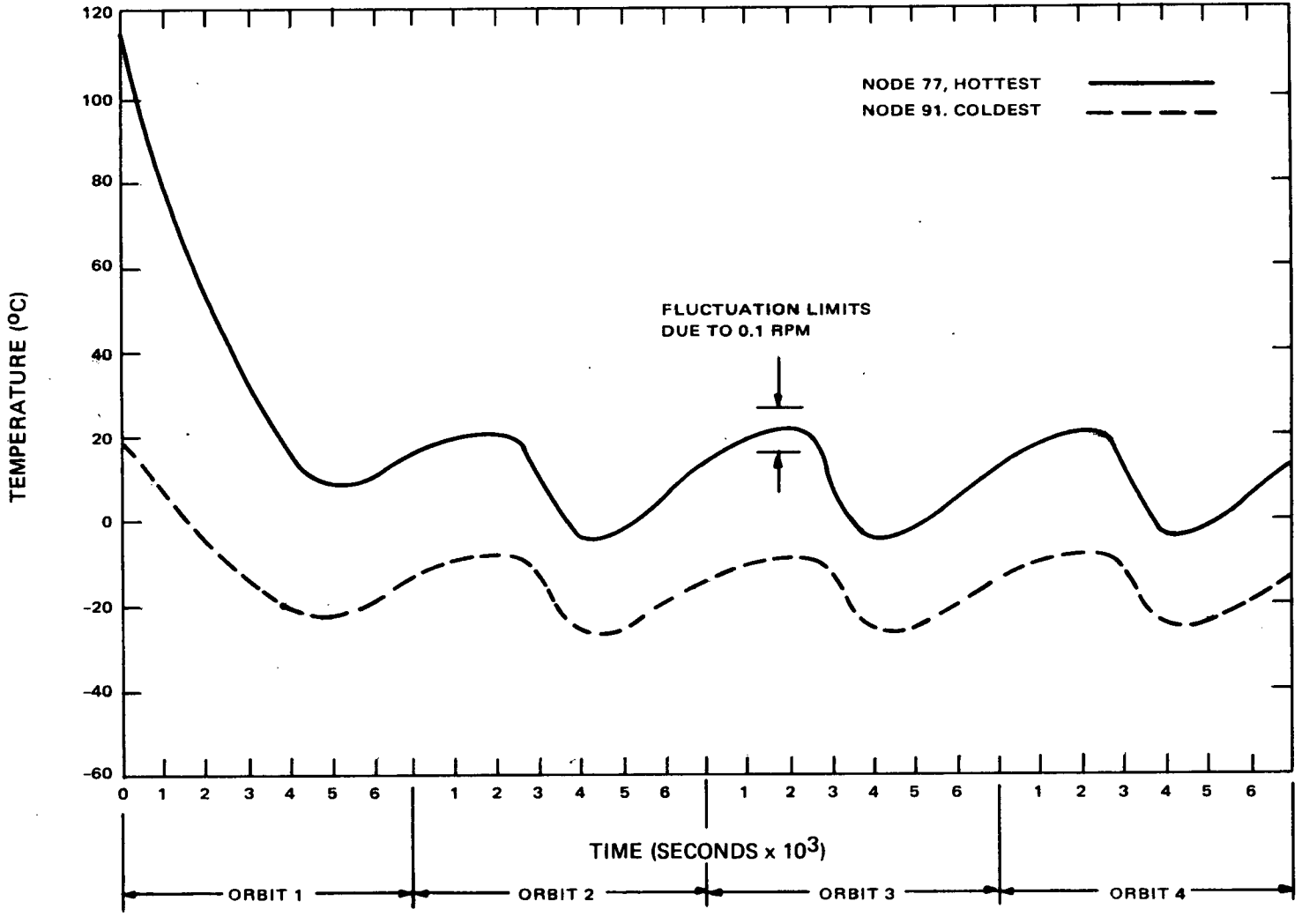


Figure 2-III-21. Power Transistor Case Temperature Prior to Solar Panel Deployment

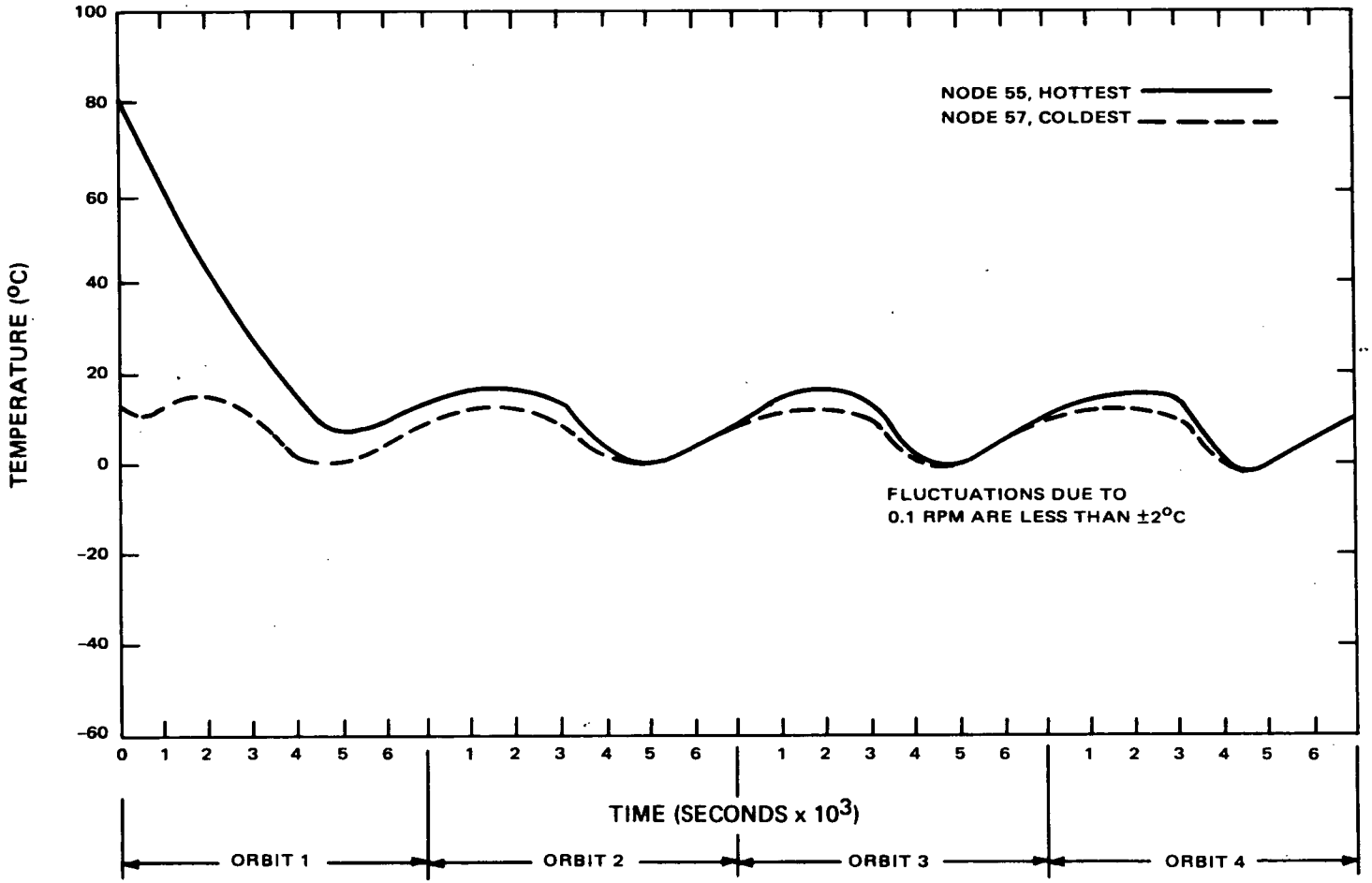


Figure 2-III-22. Resistor Mounting Temperature Prior to Solar Panel Deployment

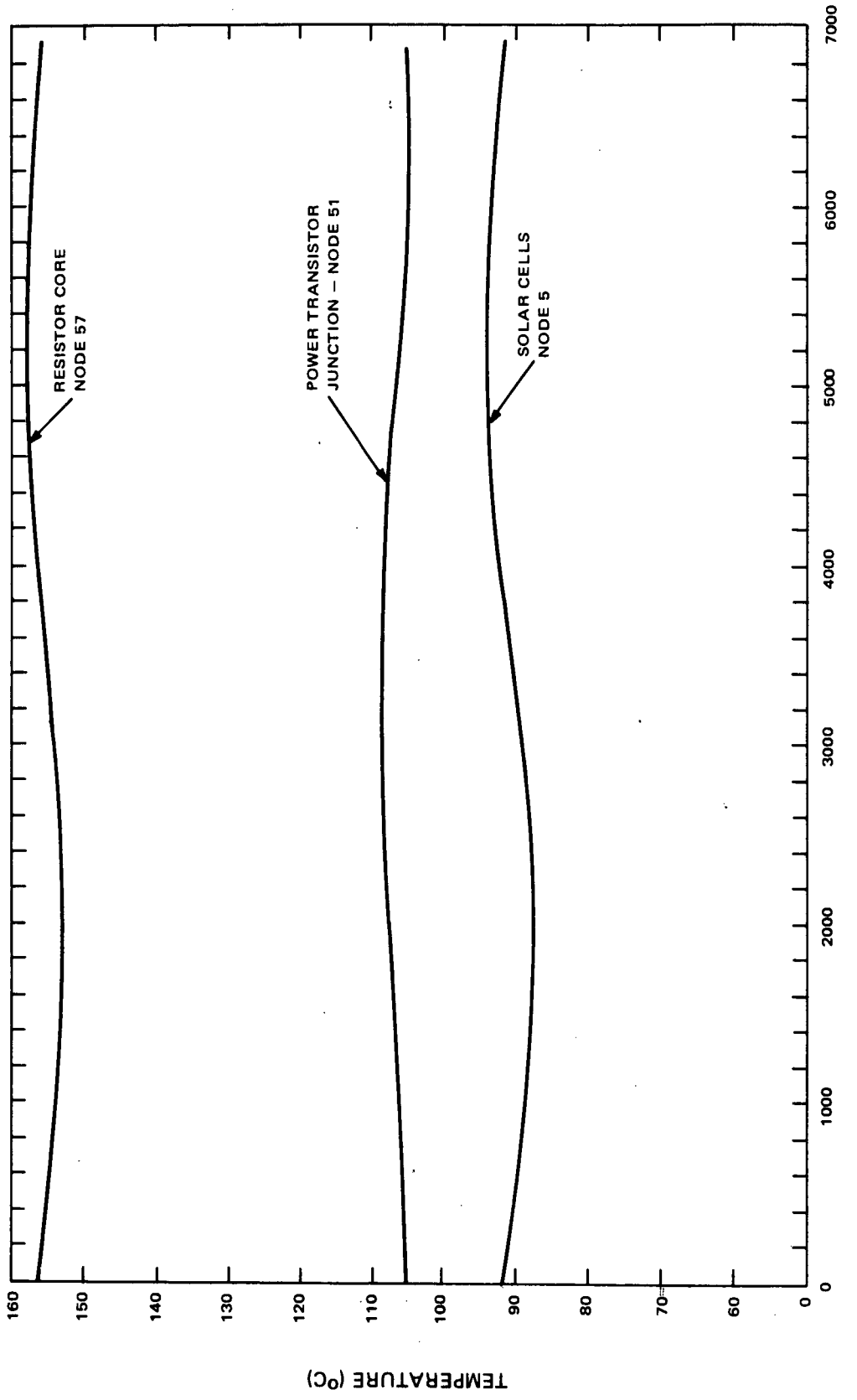


Figure 2-III-23. Solar Panel Temperatures Worst-Case-Hot Operational Mode (30-Degree Orbit BOL)

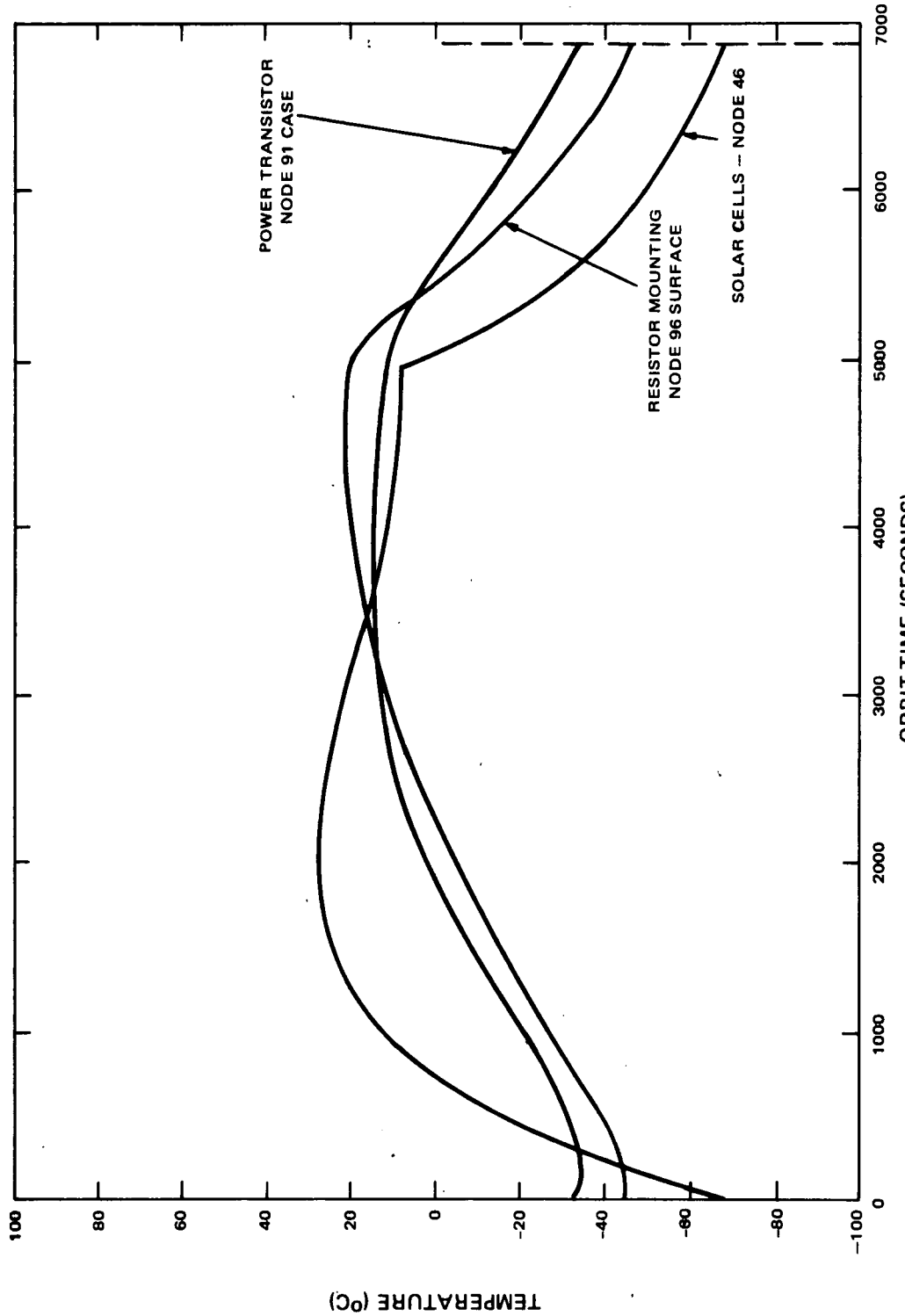


Figure 2-III-24. Solar Panel Temperatures Worst-Case-Cold Operational Mode (60-Degree Orbit EOL)

Figures 2-III-23 and 2-III-24 comprise worst case orbit histories, deriving from the combination of the extremes of mission mode sun angle and spacecraft condition of life. With the exception of an anti-earth panel mounted, shunt dissipator transistor, during the initial phase of a November 1 launch (see Figure 2-III-19), the results indicate that the design temperature requirements imposed upon the solar panel elements could be readily satisfied throughout the mission profile. The violation of the 115°C design limit (the indicated design limit represents a 42.5-percent derating of the manufacturer's 200°C specification) by the errant transistor is mitigated by the fact that the condition would persist for no more than 17 minutes, since the junction temperature would decrease rapidly after spacecraft separation.

SECTION IV
COMMAND SUBSYSTEM

A. GENERAL

The satellite command subsystem receives commands transmitted from the CDA ground stations, recognizes and rejects spurious commands, accepts and decodes valid commands, and distributes the appropriate control signals and voltages, with the proper timing, throughout the satellite to effect the command operations. The command functions include those that respond immediately to ground station command and those that take place in programmed sequences of variable duration and begin at programmed orbit times. Remote camera functions, scanning radiometer functions, and attitude control functions are in the latter category. The command subsystem also performs ancillary timing and telemetry functions.

The command subsystem performs the following specific functions:

- Provides for selective commanding of an individual satellite in a multiple-satellite system and for the selection of one of the satellite's redundant command channels for receiving the commands.
- Provides immunity from spurious commands, including commands intended for other satellites in the same system.
- Decodes received commands and, depending on the commanded function, either processes and distributes them for real-time response or stores the command program for remote operations.
- Regenerates the commands, as detected in the satellite, for retransmission to the ground station for use in command verification.
- Routes commands and internally sequenced signals to the various subsystems of the satellite where they are required for initiation or control of operations.
- Generates timing signals from which all required satellite timing and synchronizing signals are derived and from which a coded time identification signal is generated to accompany camera, radiometer, and secondary sensor data.

- Provides for satellite response to telemetry request by certain specially equipped stations other than CDA stations.
- Provides storage and delayed initiation for remote picture-taking radiometry, and attitude correction commands.

B. FUNCTIONAL DESCRIPTION

The ITOS command subsystem is functionally similar to its counterpart on the TOS spacecraft. However, the TOS decoder programmer unit, which contains two decoders, two programmers, and one time code generator, has undergone mechanical redesign to place these circuits into three units in the ITOS design. The three units are a dual decoder, a dual programmer, and a dual time base unit. This repackaging reduces the complexity of the individual units and facilitates handling during debugging and electrical testing. Because ITOS is more complex than the TOS spacecraft, more commands are required to control its operation. To handle the increased number of commands, the size of the command distribution units (CDU's) has been increased, and the CDU circuits are housed in two boxes.

As a result of comparative analysis between the resistor-capacitor transistor logic (RCTL) series integrated circuits previously used in the TOS program and the diode transistor logic (DTL) series integrated circuits previously used in a classified program at AED, the DTL series logic was selected for use in the ITOS command subsystem units. This selection was based on such factors as lower cost and power requirements, and greater flexibility, reliability, and noise immunity of the DTL circuits.

As shown in Figure 2-IV-1, the command subsystem comprises five major units: (1) a dual decoder unit consisting of two similar command decoders, each of which receives an input from one of two identical command receivers in the communications subsystem, (2) a dual programmer unit, comprising two identical programmers, (3) two command distribution units, and (4) a dual time base generator unit, comprising two identical time base generators and two identical time code generators.

The command receivers and decoders form two separate command channels and either channel can be commanded from a ground station. Only the elements associated with one command channel (No. 1 or No. 2) are used by the satellite at one time to process all transmitted commands. Cross-coupling withing the subsystem provides for selecting individual components to make up the command receiving channel in order to prevent a single component failure from

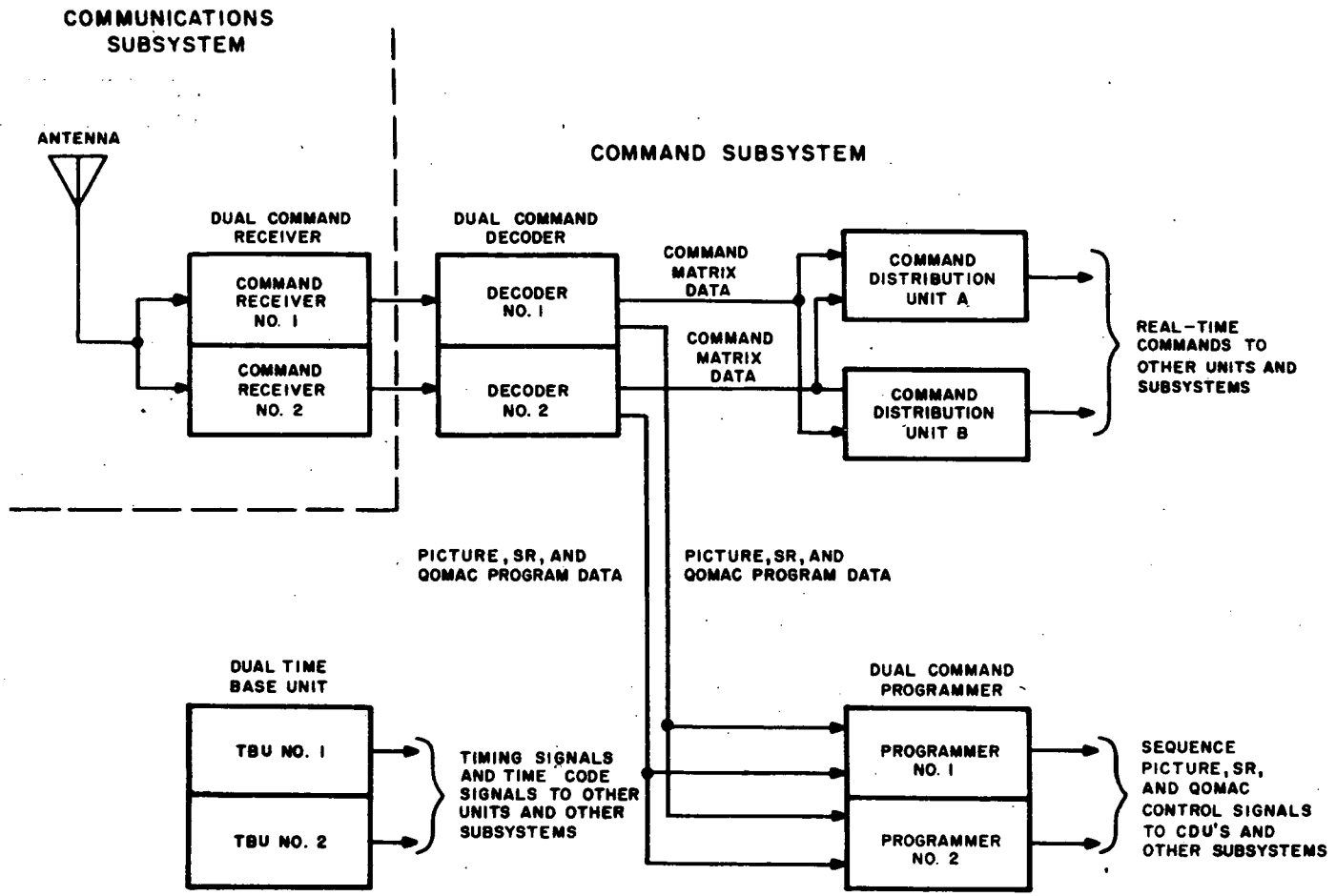


Figure 2-IV-1. Command Subsystem, Functional Block Diagram

disabling the subsystem or degrading its performance. The command distribution units provide real-time commands, and the dual time base unit provides timing signals and time codes, to other units and subsystems.

1. Command Data Format

A command transmitted to the satellite by a ground station contains, in sequence, two audio frequency tones, a fixed frequency "enable" tone and a frequency-shift-keyed (FSK) tone both as amplitude modulation on the radio frequency carrier. The enable and FSK tones, each at a different frequency, constitute a tone pair. The digital command message data is provided as modulation for a specified FSK tone. The frequency of the enable tone determines which FSK tone detector becomes enabled, and hence, which of the redundant decoders is to be used. The frequency and duration of the ensuing unmodulated portion of the FSK tone are then checked. If the frequency and duration of the FSK tone are correct, power is applied to the FSK decoding circuits so that the modulated portion of the FSK tone, containing the command message, can be detected.

2. Command Data Reception and Verification

The command receivers and the front end of the decoders in the satellite are continuously powered and maintained in a standby condition ready to accept command transmissions. Upon receipt of the RF carrier, the receivers demodulate the signal and apply the resultant enable and FSK tones to their respective decoder. One of the two decoders detects the pair of tones with filters, extracts the digital command data from the FSK tone, and supplies it to either the command distribution units or programmers, dependent upon the command format.

During processing by the satellite, all of the command data is retransmitted, bit-by-bit, to the ground station for verification. If the data received from the satellite does not coincide with the data transmitted by the station, the command may be retransmitted automatically or manually to correct the error or the error may be ignored. Command verification is performed in real-time via the telemetry subsystem.

3. Command and Control Functions

The first portion of the binary, FSK-coded command message contains a satellite address, which is one of two 12-bit binary words, each containing 2 data

"1's" and 10 data "0's". The satellite address is decoded, and, if the address and the format of the address (two data "1's" properly located in the 12-bit word) are both correct, decoder power is latched on, thus opening the circuits for continued command decoding and for command execution. Each command that follows must be preceded by a correct satellite address and must contain a correct (2-out-of-12) format. If these conditions are met, the ensuing commands are decoded and routed either to the command distribution units (CDU's) for real-time operations or to the programmers for storage and control of remote operations.

If remote operations are programmed, the programmer produces sequenced signals for control of attitude correction or camera and scanning radiometer operations at programmed intervals. These signals are distributed to the appropriate camera or attitude control circuits.

The ITOS command format has a capacity of 132 commands, compared with 66 for TOS. The 66-command limitation of the TOS command subsystem is imposed by the 2-out-of-12 command code format. Although the ITOS command format also uses a 2-out-of-12 code, the total number of available ITOS command functions has been approximately doubled. Each command belongs to one of two "sets". Each 2-out-of-12 coding is used twice, once in each set. The set to which a particular command belongs is determined by the spacecraft address that precedes it. The normal address coding is used to select Set I. Set II is selected by shifting each of the coded address bits by one bit position in the 12-bit format. The command distribution units contain a decoding circuit for each of the 2-out-of-12 codings in each set which is used in the spacecraft (other than the load programmer commands, which are decoded in the decoders).

This method of extending command capacity was selected to double the command capacity with minimal modification of the basic logic used in the TOS decoder and with no change in command format, thus simplifying the ground station compatibility requirements.

A list of the commands used for the ITOS spacecraft is given in Table 2-IV-1. The "Set" column indicates which of the two satellite address codes (Set I or Set II) precedes the 2-out-of-12 command word, and the "Bits" column indicates the position of the two "1" bits in the command word format.

TABLE 2-IV-1. ITOS COMMANDS

Command Names	Set	Bits
SR Motors 1 and 2 ON	I	2, 4
SR Motor 1 OFF	I	5, 11
SR Motor 2 OFF	II	5, 11
Select Scanning Radiometer 1, Not 2	I	1, 8
Select Scanning Radiometer 2, Not 1	II	1, 8
Select Neither Scanning Radiometer	II	3, 12
Select Scanning Radiometer Recorder 1	I	7, 12
Select Scanning Radiometer Recorder 2	II	7, 12
Select Neither Scanning Radiometer Recorder	II	2, 4
Play Back Single Scanning Radiometer Recorder	I	1, 2
Play Back Both Scanning Radiometer Recorders in Parallel	I	4, 8
Select Visible Real-Time Day SR Modulation	II	1, 10
Select IR Real-Time Day SR Modulation	I	1, 10
Disable SR Real-Time Day Operation	I	4, 5
SR Visible Calibration ON	I	6, 10
Use Real-Time Transmitter 1, Not 2	I	1, 9
Use Real-Time Transmitter 2, Not 1	II	1, 9
Use Neither Real-Time Transmitter	I	8, 11
Real-Time Transmitter During Day Only	I	2, 3

TABLE 2-IV-1. ITOS COMMANDS (Continued)

Command Names	Set	Bits
Select APT Camera 1, Not 2	I	9, 12
Select APT Camera 2, Not 1	II	9, 12
Select Neither APT Camera	I	4, 11
Use Beacon Transmitter 1, Not 2	I	2, 8
Use Beacon Transmitter 2, Not 1	II	2, 8
Use Neither Beacon Transmitter	II	8, 11
Housekeeping Telemetry Commutator 1 ON	I	9, 11
Housekeeping Telemetry Commutator 2 ON	II	9, 11
Telemetry Commutators in Manual Advance Mode	II	3, 8
Telemetry Commutators in Automatic Advance Mode	I	4, 9
Disable Digital Telemetry Power	I	2, 9
Telemetry in Acquisition Mode	II	5, 9
Telemetry in Operation Mode	I	5, 9
Telemeter Pitch Sensor 1	I	1, 12
Telemeter Pitch Sensor 2	II	1, 12
Telemeter Roll Sensor 1	I	3, 4
Telemeter Roll Sensor 2	II	3, 4
Telemeter Time Code	II	1, 2
Telemeter Roll Sensor 1 and Selected Pitch Index	I	2, 12
Telemeter Roll Sensor 2 and Selected Pitch Index	II	2, 12

TABLE 2-IV-1. ITOS COMMANDS (Continued)

Command Names	Set	Bits
Flat Plate Radiometer ON	I	11, 12
Flat Plate Radiometer OFF	II	11, 12
Calibrate Flat Plate Radiometer	II	4, 8
Solar Proton Monitor ON	I	3, 11
Solar Proton Monitor OFF	II	3, 11
Data Format Converter, Digital TLM Power, and Incremental Tape Recorder ON	I	3, 5
Data Format Converter, Digital TLM Power, and Incremental Tape Recorder OFF	II	3, 5
Play Back Incremental Tape Recorder	I	2, 5
Time Base Unit 1 ON, Not 2	I	10, 12
Time Base Unit 2 ON, Not 1	II	10, 12
Select Programmer 1, Not 2	I	1, 11
Select Programmer 2, Not 1	II	8, 10
Select Neither Programmer	II	4, 6
Select AVCS Camera 1, Not 2	I	5, 10
Select AVCS Camera 2, Not 1	II	5, 10
Select Neither AVCS Camera	II	4, 11
Select AVCS Tape Recorder 1, Not 2	I	1, 6
Select AVCS Tape Recorder 2, Not 1	II	1, 6
Select Neither AVCS Tape Recorder	II	7, 10

TABLE 2-IV-1. ITOS COMMANDS (Continued)

Command Names	Set	Bits
Play Back AVCS Tape Recorder	I	6, 8
Stop AVCS Tape Recorder	II	6, 8
Advance AVCS Tape Recorder	I	7, 10
Select S-Band Transmitter 1, Not 2	I	1, 4
Select S-Band Transmitter 2, Not 1	II	1, 4
S-Band Transmitter ON	I	2, 11
S-Band Transmitter OFF	II	2, 11
Select Multiplexer 1, Not 2	I	5, 12
Select Multiplexer 2, Not 1	II	5, 12
Use -24.5V Regulator 1, Not 2	I	3, 7
Use -24.5V Regulator 2, Not 1	II	3, 7
Shunt Control Amplifier 1 ON	I	1, 7
Shunt Control Amplifier 2 ON	II	1, 7
Shunt Control Amplifier Mode 1	I	5, 8
Shunt Control Amplifier Mode 2	II	5, 8
Charge Control Trickle Charge	I	1, 3
Charge Control Normal Charge	II	2, 5
Use Pitch Loop 1, Not 2	I	3, 6
Use Pitch Loop 2, Not 1	II	3, 6
Pitch Loop Open Loop Mode	I	2, 7

TABLE 2-IV-1. ITOS COMMANDS (Continued)

Command Names	Set	Bits
Pitch Loop Closed Loop Mode	II	2, 9
Pitch Sensors Crossed	I	7, 9
Pitch Sensors Normal	II	7, 9
Enable Dual Motor Mode	I	2, 6
Disable Dual Motor Mode	II	1, 3
Dual Motor Mode ON	II	2, 7
Pitch Loop Gain Coarse	I	5, 7
Pitch Loop Gain Normal	II	5, 7
Enable QOMAC Power	II	6, 10
Disable QOMAC Power	I	2, 10
Magnetic Bias System Positive	I	3, 10
Magnetic Bias System Negative	II	3, 10
Disable Magnetic Bias System	II	6, 7
Step Magnetic Bias Switch	I	6, 7
Momentum Coil 1 ON	I	3, 9
Momentum Coil 2 ON	II	3, 9
Disable Momentum Coil System	II	2, 10
Momentum Coil System Positive	I	4, 10
Momentum Coil System Negative	II	4, 10

TABLE 2-IV-1. ITOS COMMANDS (Continued)

Command Names	Set	Bits
Deploy Solar Panels	II	4, 7
Load Picture Program	I	1, 5
Load QOMAC Program	I	3, 8
Total number of commands: 100		

C. DUAL COMMAND DECODER

1. General Description

Each of the redundant channels of the dual command decoder, Figure 2-IV-2, consists of tone detection and FSK demodulator sections (composed of discrete analog circuitry), command format decoding logic (composed of digital integrated circuits), and output interface buffers (composed of discrete circuitry). In the standby state, power is applied in the decoder to portions of the tone detector circuits only. Only one channel is active while the satellite is in contact with a ground station. This channel, rendered operative by a tone sequence transmitted from the ground station, processes subsequent commands for all satellite functions. Each channel receives its inputs from an associated command receiver in the communications subsystem.

The ITOS decoder is basically the same as that used on the TOS spacecraft. However, two major changes were made:

(1) The decoder is now capable of processing 132 commands (compared to 66 for the TOS decoder), and

(2) DTL integrated circuit logic is now used rather than the RCTL type used for TOS.

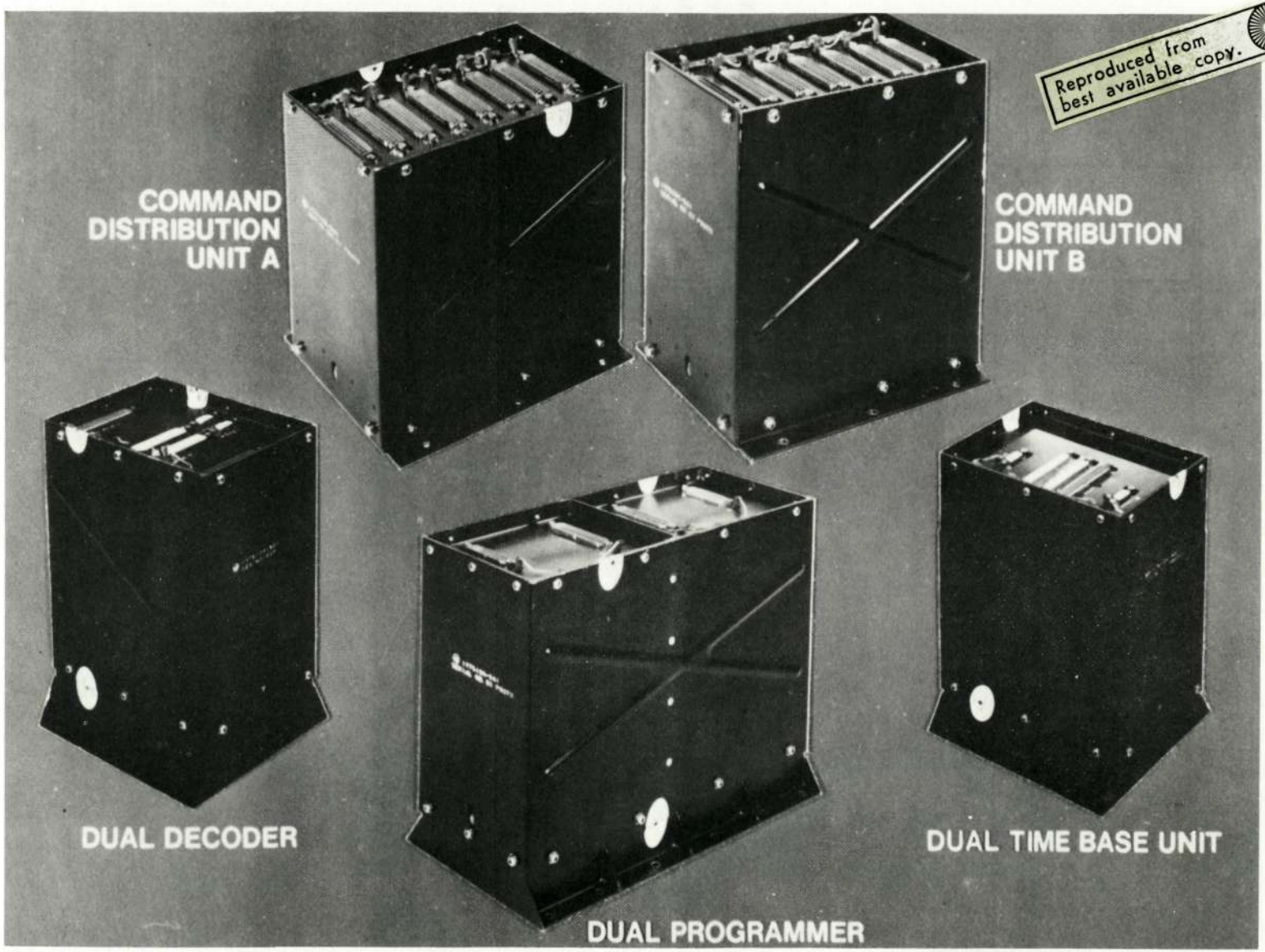


Figure 2-IV-2. Command Subsystem Components

a. POWER AND SIGNAL INTERFACES

The power converter section of each decoder channel consists of a DC-to-DC converter which receives power from the spacecraft's unregulated bus and provides four outputs. The converter supplies regulated -23 volts to the decoder analog circuits, to circuits in command distribution units (CDU's) A and B, and to the command receiver with which it is associated. The command receiver and portions of the decoder analog circuitry are powered continuously; the -23-volt power to the remaining analog circuits and the appropriate circuitry in CDU's A and B is switched as described below. The converter also supplies regulated +5 volts and +5.35 volts to the decoder digital and output interface buffer circuits, respectively. Both of these power outputs are switched, except for two digital integrated circuits that are powered continuously from the +5-volt output. Finally, the converter provides a square wave clock at the conversion frequency, specified as higher than 11 kHz.

The signal input to each decoder is routed directly from its associated command receiver. The audio input signal to each channel of the decoder consists of two tones, an enable tone and an FSK tone. The receipt of a valid enable tone and FSK tone, for the required durations, causes -23-volt power to be switched to CDU's A and B and to the FSK detector in the decoder, and also causes +5-volt and +5.35-volt power to be switched to the decoder digital and buffer circuits, respectively, thus permitting the spacecraft to be addressed. The digital address, as well as the digital command data, modulates the FSK tone. The FSK tone is characterized by a center frequency tone, f_c, which is shifted to f_c +7.5 percent to represent a data "1" and to f_c -7.5 percent to represent a data "0".

Two unique tone pairs, consisting of an enable tone and an FSK tone, are available for commanding a spacecraft. Each of the four tones has a different frequency. Each set of tone pairs is recognized by only one receiver-decoder channel. If a failure occurs in one decoder channel, the second pair of tones may be used to address the second channel. The use of distinct enable and FSK tones increases the security of the system from spurious commands, without greatly increasing the number of components in the spacecraft. The arrangement described also provides maximum isolation between channels and guarantees that the opposite channel will not be enabled during commanding, which would be the case if a common enable tone were used. Since the tones are transmitted by amplitude modulation, a carrier frequency higher than those of the commercial broadcast band has been selected. The receiver bandwidth limits the upper end of the baseband spectrum to about 12 kHz.

A diagram of the decoder input and output interfaces is shown in Figure 2-IV-3. Brief descriptions of the signals which comprise the output interface are contained in Table 2-IV-2.

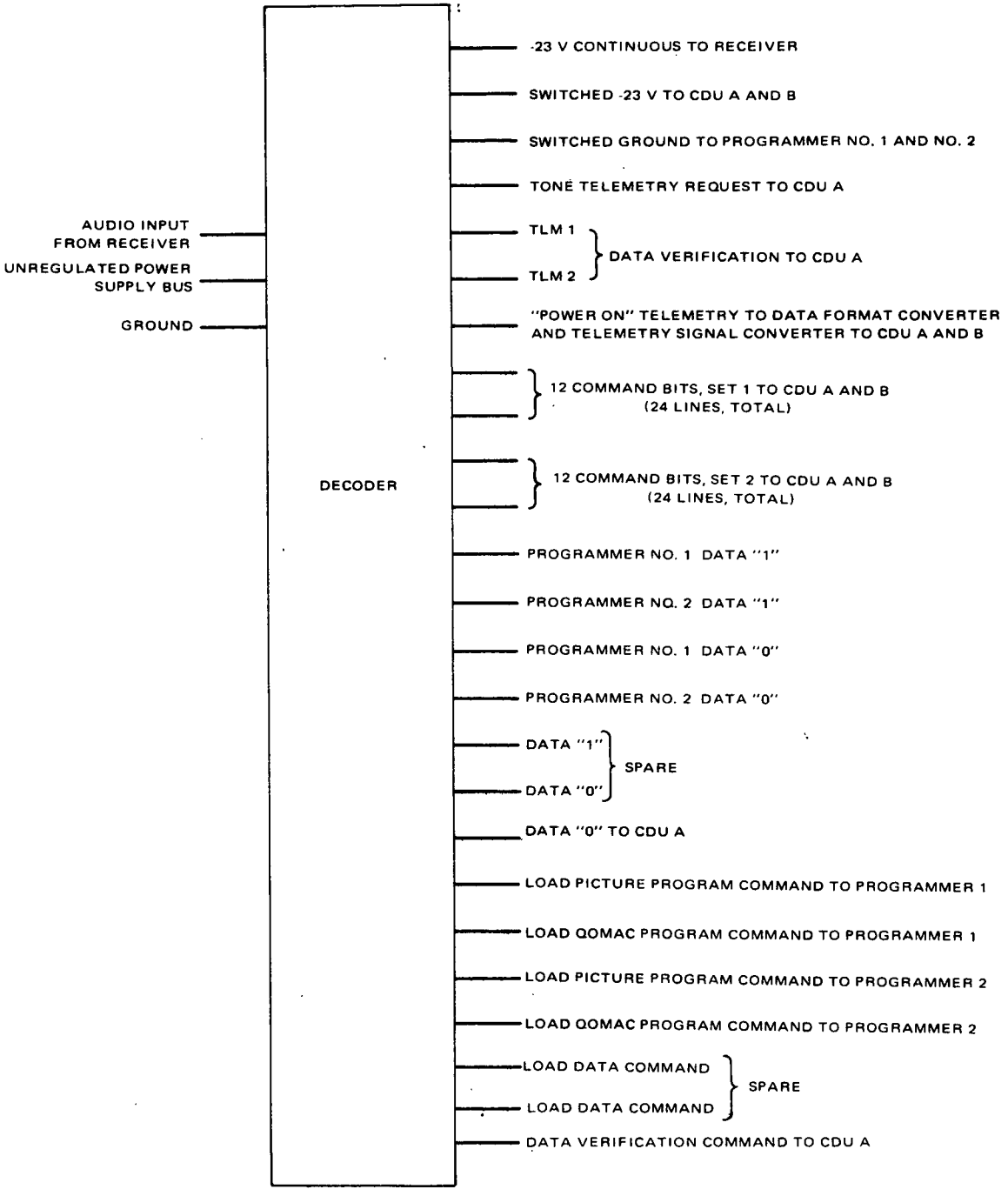


Figure 2-IV-3. Decoder Input and Output Interfaces

TABLE 2-IV-2. DECODER OUTPUT INTERFACE SIGNALS

Signals	Description
Continuous -23-Volt Power	Each decoder supplies -23-volt power continuously to portions of its analog circuitry and to the command receiver associated with the decoder.
Switched -23-Volt Power	When a decoder has been "enabled" and is in its operational state, -23-volt power is switched to both CDU's and the remainder of the decoder analog circuitry.
Switched Ground	The switched ground output consists of a hard ground made through a set of relay contacts. When the decoder is in the standby state, the output is at ground; when the decoder is enabled and is in the operational state, activation of the relay causes the ground to become an open circuit. Two lines from each decoder are used to deliver this output to both programmers.
Tone Telemetry Request	If the enable tone is received continuously for the appropriate length of time, this output is generated and sent to CDU A, where it initiates the readout of one frame of telemetry from a telemetry commutator provided the appropriate beacon transmitter is operating at the time.
Data Verification	All command and data bits are retransmitted to the ground station in real time. The decoder output is a three-level signal in which the different voltage levels represent the reception of data "1", data "0", or FSK center frequency. These levels, when coupled into the beacon telemetry channel of the spacecraft, are used to modulate an SCO.
Data Verification Command	This signal is used to energize a nonlatching relay in CDU A while command transmission is taking place. The closure of this

TABLE 2-IV-2. DECODER OUTPUT INTERFACE SIGNALS (Continued)

Signals	Description
Data Verification Command (cont)	relay permits the decoder data verification signal to be coupled into the spacecraft telemetry link.
Power ON Telemetry	This output is held at -4.5 volts when the switched -23-volt power is activated. If this power is not switched on, this output is at ground potential.
Two Sets of 12-Command-Bit Outputs to Each CDU	Each validly received command causes two outputs belonging to one of these sets to become activated. The decoding of these outputs takes place in one of the CDU's, depending on which particular command has been received.
Digital Data Outputs to Programmers	Two separate data "1" output lines and two separate data "0" output lines from each decoder are used to supply digital data to both programmers.
Data "0" to CDU	This output is pulsed on whenever a data "0" input is being received by the decoder. It is used to provide the clock for the telemetry commutators in the manual mode.
Load Picture Program Command	Two distinct command outputs of this type are provided by each decoder, one for each programmer. This signal must preceed picture program data which is to be loaded into the programmer.
Load QOMAC Program Command	Two distinct command outputs of this type are provided by each decoder, one for each programmer. This signal must precede QOMAC program data which is to be loaded into the programmer.

TABLE 2-IV-2. DECODER OUTPUT INTERFACE SIGNALS (Continued)

Signals	Description
Spare Outputs	A dual load data output, of the Load Picture (or QOMAC) Program variety described above is provided for possible future use. Similarly, one data "1" line and one data "0" line of the type described above (Digital Data Output to the Programmers) is also provided.

b. DECODER DATA FORMAT

The data format for the decoder is shown in Table 2-IV-3. Each data bit is denoted by a shift in the FSK tone to the data "1" frequency or to the data "0" frequency for 50 milliseconds. Sync is denoted by a shift to the data "1" frequency for 350 milliseconds. In both cases, these transitions are followed by a 50-millisecond return to center frequency, which is to be considered as an integral part of all data bits and sync.

TABLE 2-IV-3. DECODER DATA FORMAT

Function	Code
Address Sync	Data "1" frequency continuously for 350 milliseconds
Address Word	2 data "1" bits and 10 data "0" bits
Command Sync	Data "1" frequency continuously for 350 milliseconds
Command Word*	2 data "1" bits and 10 data "0" bits
Command Termination*	1 bit
Programmer Data	28 bits (follows Load Programmer commands only)

* For initial command entry into the spacecraft, a dummy command word consisting of 12 data "0" bits and a 13th "0" execute or dummy command termination bit immediately follows the first command sync pulse, in order to complete the format of the first command in a command sequence.

2. Functional Operation

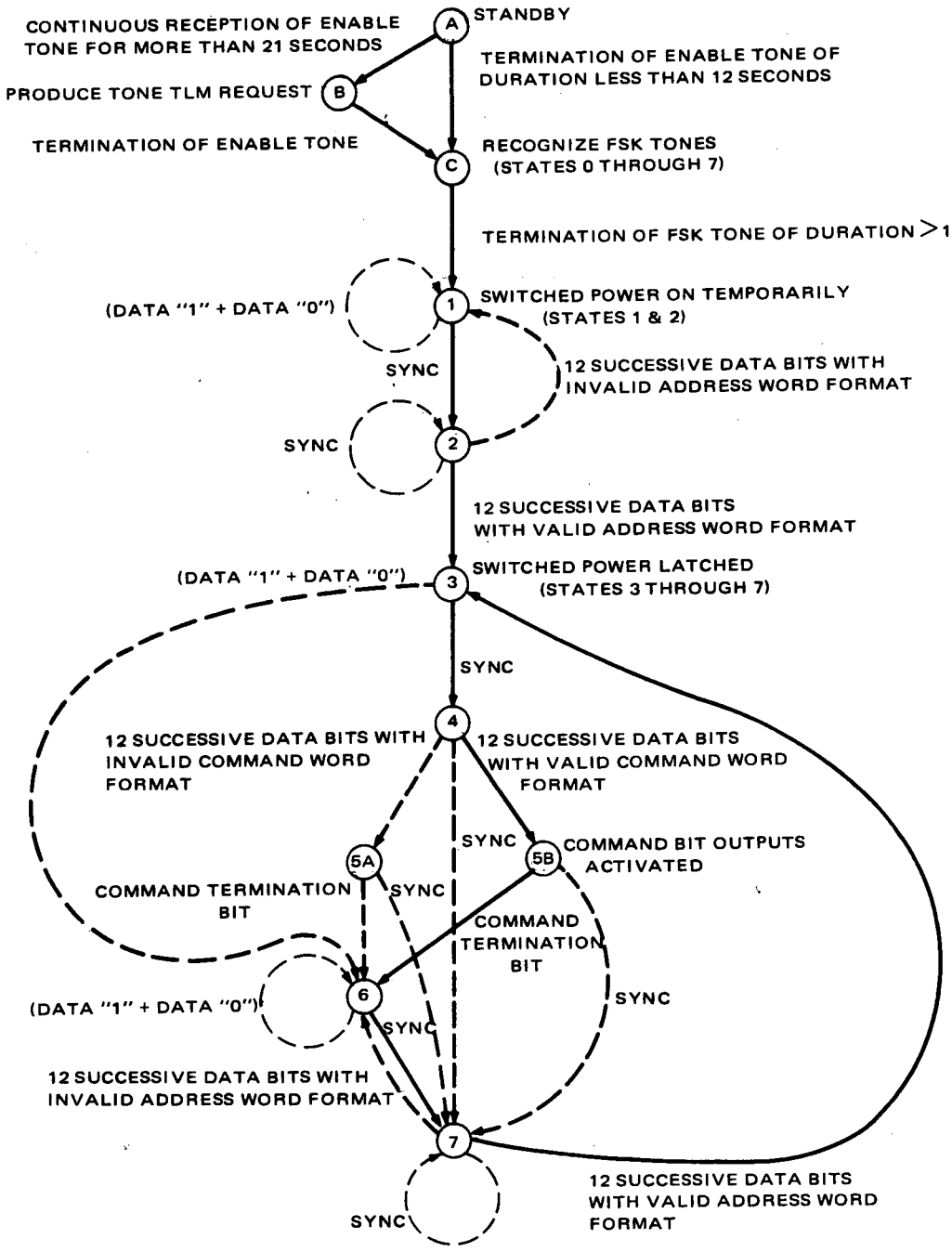
a. GENERAL DECODING PROCESSES

Typically, when the spacecraft is not in the process of receiving commands, both decoder channels reside in the standby state. In this condition, the only power supplied by a channel is that required for its associated command receiver and portions of its tone detector circuitry. To activate one of the decoder channels, a CDA station transmits the correct tone pair, which permits that channel to verify the data format of subsequent addresses and commands. The sequence and timing requirements for valid input signals as well as the decoder's response to certain invalid command sequences is discussed below. A simplified logic flow diagram of the decoder is shown in Figure 2-IV-4.

Activation of a decoder residing in the standby state is accomplished by a latching sequence in the following way. That channel's enable tone is received for a minimum of 5 seconds and is followed, within 3 seconds after the termination of the enable tone, by that channel's FSK center frequency tone which lasts for a minimum of 1 second. The response of the decoder to this tone sequence is to supply power temporarily to the CDU's and all the decoder circuits, which permits FSK data to be processed. If a properly formatted spacecraft command address for the temporarily activated decoder is not received within a 3-second period following the termination of the enable tone, the switched power will drop out at the end of that time; in such a case, activation of the decoder channel can be achieved only by retransmitting the described sequence, starting again with the enable tone. However, if a valid address is received within the allowed time period, the temporarily switched power will become permanently latched, and it will not be necessary to utilize the enable tone to process further data unless the FSK tones are absent for a period greater than 250 milliseconds.

Incorrect sequences of enable and FSK center frequency tones, time durations which are too short, or frequencies and/or amplitudes which do not meet specification will result in the decoder remaining in the standby state. Only if a decoder has been successfully activated through the receipt of a valid tone pair, will it demodulate the FSK signal and thereby provide logical true levels to its then enabled digital circuitry. These levels are generated by the decoder on separate data "1", data "0", and f_c (center frequency) lines at times corresponding to the receipt of the appropriate tone at the audio input to the decoder.

An auxiliary function is performed by the decoder if the enable tone provided to it is present for a period greater than 21 seconds. Such an input, in addition to satisfying the requirements for the first step in activating the decoder, also causes it to generate a "tone telemetry request" signal which is used to initiate the readout of a frame of telemetry data.



NOTES:

1. THE TRANSITION FROM STATE 0 TO STATE 3 MUST BE ACCOMPLISHED WITHIN THREE SECONDS OR LESS. FAILURE TO MEET THIS TIMING REQUIREMENT WILL RESULT IN A REVERSION TO STATE A.

2. FOR STATES 3 THROUGH 7, FSK TONE DROPOUT FOR A PERIOD GREATER THAN 250 MILLISECONDS WILL CAUSE A REVERSION TO STATE A.

3. THE TRANSITIONS SHOWN IN SOLID LINES INDICATE THE LOGICAL FLOW FOR NORMAL, PROPERLY FORMATTED COMMANDING OF THE DECODER, THOSE TRANSITIONS INDICATED BY DASHED LINES ARE ANOMALOUS, AND DO NOT OCCUR WHEN THE PROPER DATA FORMAT IS USED.

Figure 2-IV-4. Decoder Simplified Logic Flow Diagram

As shown in Table 2-IV-3, a valid address consists of a sync signal followed by 12 data bits, and only 2 of which must be data "1" bits. The decoder verifies that the address contains exactly 2 data "1" bits in a field totaling 12, and also checks that these 2 bits lie in the proper positions within the address word. Each decoder channel will accept as valid either of two such addresses; on any one spacecraft both decoder channels respond to the same two addresses, but the addresses for different spacecraft are unique. In a particular decoder channel, one address enables a set of gates used to decode a group of 66 command words; the other address enables a different set of gates which decode the same group of 66 command words. However, the outputs of all the gates are physically connected to perform separate functions. Thus, through the use of two distinct addresses, 132 real-time spacecraft commands may be executed using only 66 command words.

When the spacecraft is being commanded initially, the first validated address is followed by a dummy command word, as indicated in Table 2-IV-3, which completes the latching sequence. The decoder is now set up to receive and decode the command sequence consisting of the spacecraft address followed by the command word (and a 28-bit data word if QOMAC, SR, or AVCS is being commanded). During the command sequence, and following the receipt and validation of the spacecraft address as previously explained, the decoder is prepared to verify a command word.

A valid command word, as shown in Table 2-IV-3, has a format similar to a valid address: a sync signal followed by 12 data bits, 2 of which must be data "1" bits; however, in addition, proper format calls for a single command termination bit to follow the 12-bit command word. This 13th bit is a data "1" for command words in the command sequence (but a data "0" for the dummy command which occurs in the latching sequence). The decoder checks that a received command word contains only 2 data "1" bits in a field totaling 12 bits. If this is the case, two decoder outputs corresponding to the positions of the 2 data "1" bits in the command word are provided from among that set of 12 gates which has been enabled by the particular address word which preceded the command word. The activated outputs are presented to both CDU's, in one of which the actual command decoding and execution takes place, depending upon which particular command has been sent. Receipt of the 13th, or command termination bit, causes the deactivation of these decoder outputs.

If the received command word was a Load Picture Program or Load QOMAC Program command, 28 bits of digital data are then provided through the decoder to the programmers. These data bits are identical in character to those in the decoder address and command words, and are presented immediately following the command termination bit of Load Programmer commands.

All of the data in the received address and command, as recognized by the decoder, is transmitted back from the spacecraft to the CDA station via the data verification link, with the following two exceptions:

(1) The address sync is not transmitted on the verification link. During the period when address sync occurs, solor proton monitor data appears on the beacon link when the telemetry subsystem is in the operational mode; DSAS data will appear on the beacon link when the telemetry subsystem is in the acquisition mode.

(2) The data "1" command termination bit following the command word is not retransmitted as a data "1" if the decoder has verified a valid command word. Instead, when the decoder has verified a valid command word, it provides a marker on the data verification link in the form of a lengthened data "0". This marker indicates the reception of the frequency representing data "0" during the period corresponding to actual reception of the center frequency portion of the 12th bit of the command word (in addition to the period corresponding to the frequency shifted portion of this data bit, but only if it is indeed a data "0") as well as during the entire period corresponding to the reception of the command termination bit, no matter which type of data bit is actually sent. However, if a received command is not a valid command, all address data (excluding address sync) and command data (including the command termination bit) will be returned via the data verification link exactly as interpreted by the decoder.

Once the decoder switched power has been latched on by an acceptable sequence of enable tone, FSK center frequency tone, and initial address as described above, it remains latched until all FSK signals drop out for a period greater than 250 milliseconds. At that time, the decoder enters the standby mode and the entire sequence of enable tone, FSK tone, address and dummy command must be repeated to regain access to the decoding circuits. This operation is analogous to a "push-to-talk" system and has the advantage that, when the spacecraft is beyond communications range of a CDA station, the command decoding system is turned off and is thus inaccessible to spurious command. In addition, the decoder automatically reverts to standby power requirements for the greater part of the spacecraft orbit.

In the normal operation of the decoder, the initial address is followed by command sync and a command word as described above. Subsequent commands, even when properly formatted, can be verified by the decoder and decoded by a CDU only if each command word is preceded by a valid, properly formatted address. Therefore, the normal commanding sequence following the initial command word after acquisition is: valid address, valid command, valid address,

valid command, etc. Once latched, the decoder switched power may be held on while the spacecraft is in range of a CDA station, without the necessity of continuously transmitting this address-command sequence. This can be done by simply transmitting a continuous FSK center frequency tone, which starts, typically, immediately after the transmission of a command termination bit. The result of receiving various incorrect data formats on the decoder operation may be deduced from an examination of Figure 2-IV-4, the simplified logic flow diagram of the decoder.

B. DETAILED CIRCUIT DESCRIPTION

A block diagram of each decoder channel is shown in Figure 2-IV-5, and a timing diagram in Figure 2-IV-6. The detailed logic diagram for the dual command decoder is RCA Dwg. No. 1976087, which may be found in a separate manual.*

(1) ANALOG CIRCUITS

The input amplifier of the decoder provides a nominal voltage gain of 4 to increase the level of the audio tones from the receiver to a usable level for the detection and demodulator circuits and to provide drive capability for the tone filters. The enable tone is coupled through a ±7.5-percent bandpass filter, centered at the enable tone frequency, to a detector circuit where it is rectified. The rectified pulses are then integrated by an RC network. After 6 seconds (nominal), the integrated signal is of sufficient magnitude to arm a transistor switch, so that at the termination of the enable tone, an RC differentiator is presented with a negative step voltage. The resultant negative going output of the differentiator is used to turn on another transistor gate for a period of 3 seconds; this period is determined by the differentiator time constant. Additionally, at the time the switch is armed by an enable tone of 6 seconds (nominal) duration, another RC integrator begins to time a 16-second (nominal) interval. Only if the enable tone is maintained for a total time of 21 seconds, the output of the second RC integrator will achieve a level sufficient to turn on a transistor switch which provides the "tone telemetry request" signal directly to CDU A.

As indicated in Figure 2-IV-5, during the 3 seconds that the transistor gate is on, the decoder is capable of processing an FSK signal to be used to pull in its relay. This must be accomplished before any other processing of input signals can take

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*RCA Corporation, Astro-Electronics Division, TIROS M/ITOS Spacecraft Logic Diagrams, AED M-2175, Contract NAS5-10306, Princeton, N.J., June 15, 1969.

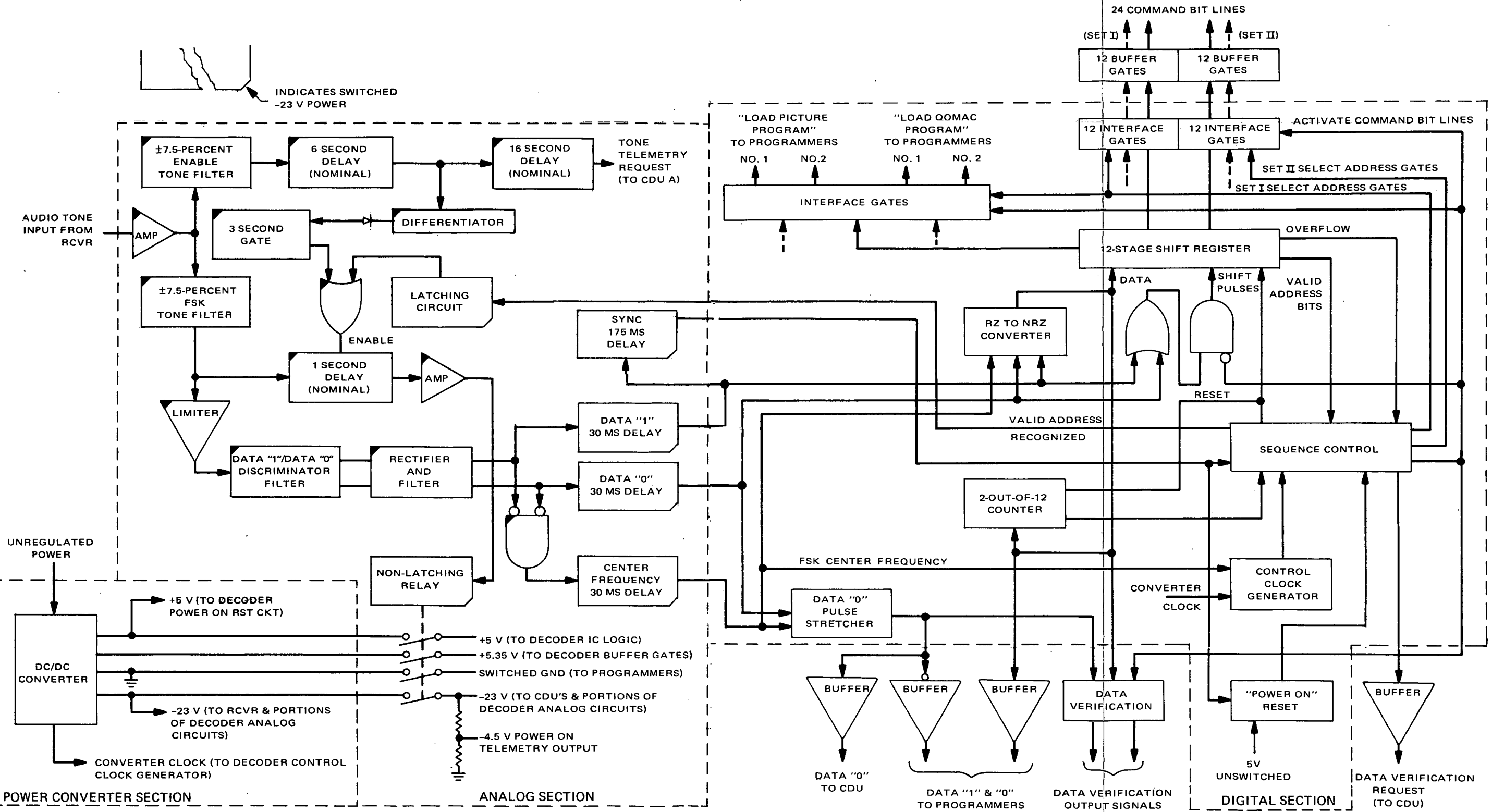

Figure 2-IV-5. ITOS Decoders, Block Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

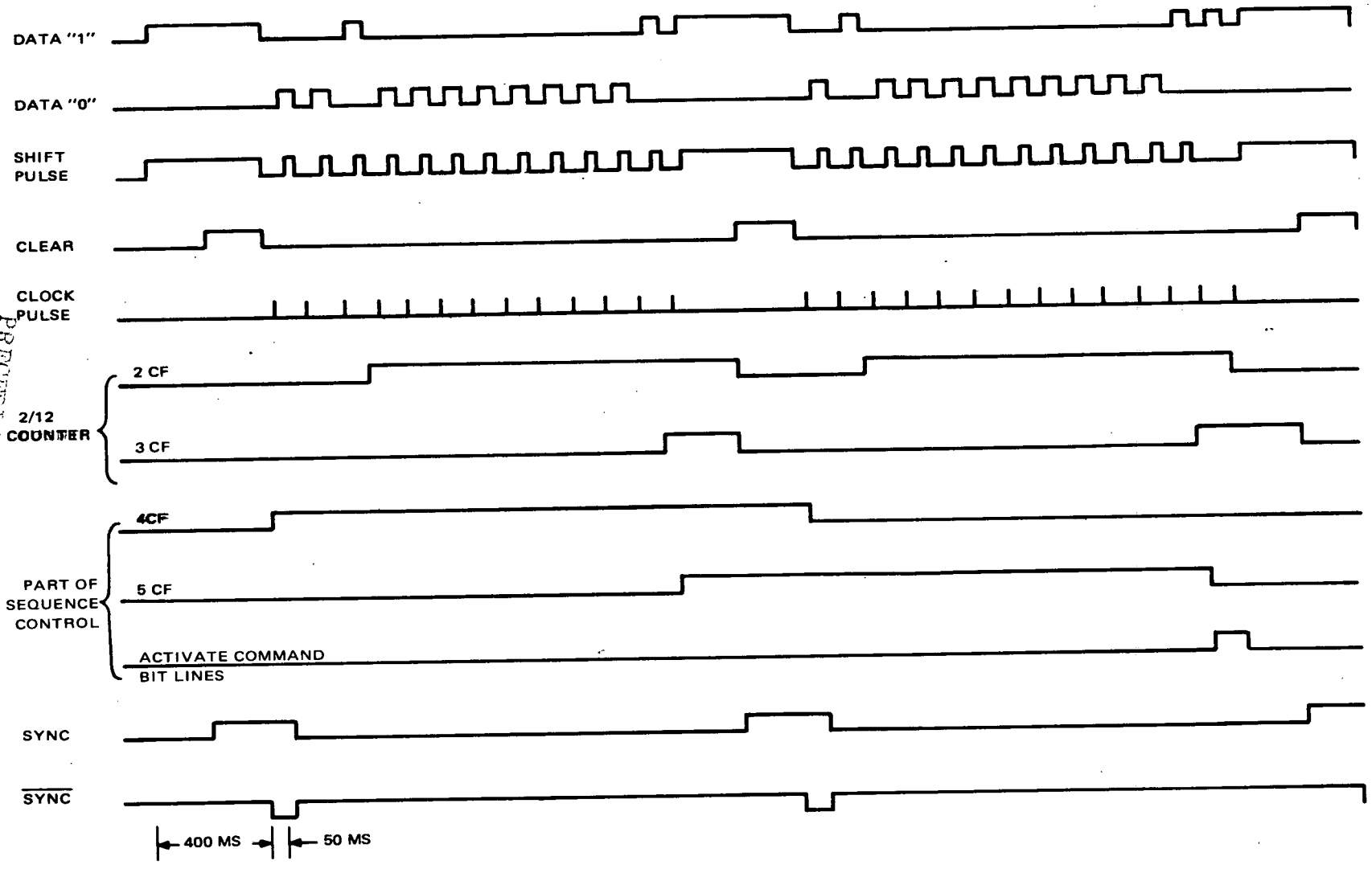

Figure 2-IV-6. Decoder Timing Diagram

place. Thus, an FSK tone provided during the 3-second "enabled interval" is passed through a ±7.5-percent bandpass filter, centered at the FSK center frequency, to a detector circuit where it is rectified. The filter input comes from the same amplifier used to boost the received enable tone level. The rectified pulses are then applied to an RC integrator. After 1 second (nominal), the integrated signal is large enough to close a transistor switch; two more such switches immediately raise the current level to that required to operate the relay.

The closure of the relay causes -23-volt power to be applied to the CDU's, in anticipation of command decoding to take place there, and in addition applies this power to previously unpowered portions of the decoder analog circuitry. Simultaneously, +5-volt power is applied to all of the decoder IC logic circuitry, while +5.35-volt power is applied to its output buffers. The Power On Telemetry output goes to -4.5-volts at this time. It is at this point that the decoder is first capable of recognizing data bits which modulate the FSK tone.

The output of the ±7.5-percent bandpass filter centered at the FSK center frequency, f_c, is also coupled to a limiter amplifier which drives a discriminator-filter. The signal at the "1" output of the discriminator-filter peaks with a shift in the FSK frequency to f_c +7.5 percent. The signal at the "0" output of the discriminator-filter peaks at a frequency of f_c -7.5 percent. The signal levels at the "1" and "0" outputs are at least 9 dB down from the peaks when the FSK tone is at center frequency, and are at least 15 dB down from their maximum level when the opposite output achieves its peak. The relative difference in the magnitudes of these outputs, at the pertinent frequencies, is sufficiently great to permit the decoder to determine which frequency, if any, is being received.

The discriminator-filter outputs are rectified and filtered, and then each applied to two respective series of transistor switches. Certain key stages within each series have had power applied due to the relay closure. As shown in Figure 2-IV-5, each signal is RC integrated for a period of 30 milliseconds before being delivered, in the form of a pulse, to the decoder digital circuitry. In addition, after rectification and filtering, the discriminator-filter outputs are effectively inverted and applied to an AND gate which drives its own series of transistor switches, also powered in part by the relay closure. The output is delivered to the digital circuitry (delayed 30 milliseconds as in the data "1" and data "0" cases) in the form of a pulse occurring once each time the simultaneous absence of signals from both discriminator-filter outputs is detected; this condition is recognizd as FSK center frequency, f_c. Finally, the data "1" output, after being delayed for 30 milliseconds, is applied to another RC integrator followed by a transistor switch powered by the relay closure. This integrator introduces a further delay of 175 milliseconds, before this final switch is allowed to turn on.

By this means, a sync pulse, whose shifted frequency is the same value as a data "1" pulse but whose shifted frequency duration is seven times longer, is recognized. The output of the sync delay circuit is delivered to the digital circuitry in the form of a pulse after a total delay of 205 milliseconds; the width of this pulse as well as the data "1", data "0", and f_c pulses provided to the digital logic circuitry is determined by the duration of the reception of the respective audio tones by the decoder; pulse termination is coincident with tone termination.

The latching circuit contained in the decoder analog section is a transistor switch (powered only after relay closure). When this switch is on, it provides an alternate path to maintain the enable to the 1-second FSK delay circuit. Thus, the latching circuit, if provided with an input signal from the decoder logic circuitry, will permit the relay to remain closed even after the enabling signal provided by the 3-second gate terminates. (The circuit operation responsible for providing the input signal to the latching circuit is discussed below). It is clear from Figure 2-IV-5 and the above discussion that the presence of an FSK tone is required to maintain relay closure. Stored energy in the 1-second delay circuit will maintain relay closure for only 250 milliseconds following the termination of all FSK tones.

(2) DIGITAL (INTEGRATED) CIRCUITS

The data, f_c, and sync pulses received from the analog section are pulses whose widths have been shortened by their respective delay circuits. Thus, a data "1" pulse, having a nominal width of 50 milliseconds, has been reduced to a 20-millisecond pulse because of the 30-millisecond delay time. Following the trailing edge of this pulse, a 30-millisecond interval (the f_c delay time) elapses before a 20-millisecond f_c pulse is provided (assuming a nominal 50-millisecond f_c duration between data pulses). The data "1" and data "0" pulses are buffered by IC gates and are then OR'ed to obtain decoder shift pulses. The return-to-bias (RB) format of the data pulses is converted to nonreturn-to-zero (NRZ) format before being presented to the first stage in the decoder shift register, the 2-out-of-12 counter, the data "1" output buffer to the programmer, and the data "1" input to the data verification buffer. The data "0" inputs to the latter two buffers are provided by separate pulse stretching circuitry, to provide the waveforms required.

When power is initially applied to the digital logic, the power-on reset circuit, a DC flip-flop, locks the sequence control logic (SCL) in state 1 (see Figure 2-IV-4). Reception by the decoder of a sync pulse is required to toggle this flip-flop, which releases the lock on the SCL and only then permits validation of data. Thus, the first sync pulse following initial relay closure releases the SCL; in addition, the termination of this sync pulse places the SCL in state 2, wherein

it is prepared to validate an address. This and all transitions of the SCL are synchronous with the clock produced by the control clock generator. The clock is a series of pulses approximately 80 microseconds in width, one of which is produced at the leading edge of every f_c pulse presented to the decoder digital section. The decoder digital section provides information, for all data which it recognizes, to the data verification buffer; however, the SCL, which controls the generation of the data verification request signal, provides such a signal only in states 2 through 5, and state 7.

The 12-stage shift register, which is asynchronously cleared by the sync pulse, shifts in the data bits which the decoder normally receives following a sync pulse. When 12 successive data bits (any combination of "1" and "0" bits) has been received, the overflow of the shift register is detected by the SCL. While the data is being shifted into the register, the 2-out-of-12 counter is simultaneously keeping track of whether none, one, two, or more than two data "1" bits are contained in the data stream. At the time of register overflow, the SCL performs a logical check on the data which has been received. The SCL does this to ensure that, of the 12 bits received, only 2 are data "1" bits, and, also, that this pair of bits has been received in one of the two preassigned positions which correspond to a valid address. Only if this logical AND condition is true will the SCL provide a valid address recognized signal, enable the command bit gates which are controlled by the particular address received, and advance itself to state 3. The valid address recognized signal, which remains present until switched power is removed from the decoder, provides a continuing enable signal to hold the relay on for as long as FSK tones continue to be received. Of course, if the last described conditions have not occurred within 3 seconds of the termination of the enable tone, switched power is already lost and the decoder has reverted to state A in Figure 2-IV-4. Furthermore, if the logical AND condition described above is false, the SCL will reset to state 1 at the time of overflow.

Assuming that a valid address has been received within the required time, and that therefore the SCL has reached state 3, the decoder awaits further data input. If an (abnormal) 13th data bit follows the valid address, the SCL will advance to state 6, where it will require that another valid address be received before any command decoding can take place. However, a (normal) sync pulse will cause the SCL to advance to state 4, where it is ready to validate a command word; the sync pulse also causes an asynchronous clear signal to be applied to the shift register and the 2-out-of-12 counter, thus readying them for the command word which normally follows.

While the command word data is being shifted in, the shift register and the 2-out-of-12 counter operate exactly as before. When register overflow is detected by the SCL, it simultaneously checks the state of the 2-out-of-12 counter. Only if the 12 data bits in the register contain exactly 2 data "1" bits (in any position whatever) will the SCL advance to state 5B; otherwise, it will go to state 5A.

Typically, while the SCL is in state 5B, the command bit lines to the CDU's, which correspond to the two stages of the shift register which contain data "1" bits, are activated; then, signals on these lines are provided from the outputs of two gates contained in the set previously enabled by the particular address received. In state 5A, no output lines from the decoder are activated.

An additional action is performed by the decoder in state 5B, but only if the command word bits in the shift register are those which produce any of the Load Programmer commands. These commands are decoded in the digital section of the decoder by means of an IC AND gate, and the commands themselves (in addition to the command bit outputs provided to the CDU's, which do no decoding in this case) are provided directly to the programmers.

In any case, any command outputs activated by the decoder while in state 5B will remain activated until inputs are received which cause it to leave this state. Normally, a command termination bit, which may be either a data "1" or a data "0", is used for this purpose. Reception of this bit will advance the SCL into state 6, where the decoder command outputs are deactivated. To prevent the shifting of the command bits in the register while they are being used to activate the proper decoder command outputs, the SCL inhibits the shift register clock during the time of the command termination bit if the command has been recognized as valid. This prevents the 13th bit from being shifted into the register. If the decoder had detected an invalid command and the SCL had entered state 5A, the command termination bit would have nevertheless returned the SCL to state 6.

Another signal from the SCL is generated during the time that the decoder command output lines are activated. This signal is used to force the data verification output buffer to indicate the presence of a data "0" level throughout that time. When the command word is found to be invalid by the decoder, the output buffer is allowed to indicate the presence of the actual input at that time, which corresponds to the time of reception of the command execution bit.

Having achieved state 6 via the route(s) described, the decoder digital circuitry is in a rest state similar to state 1. The only essential difference is that power is latched in the former state and it is not in state 1. That is, the decoder digital logic has returned to the same condition as in state 1, and will respond to inputs exactly as described above; except for the differing power conditions, states 6 and 7 (which is reached from state 6 in response to a sync pulse) correspond to states 1 and 2, respectively; the operation of the decoder logic circuitry in the corresponding states is identical and is described above.

One remaining unique response of the decoder to a command word which produces a Load Programmer command, results from the fact that a word of programmer data follows these commands. This data word is conveyed through the decoder to

the programmer while the SCL resides in state 6. As indicated in Figure 2-IV-4, the SCL will continue to reside in state 6 while the decoder processes this stream of data bits. The circuitry which handles the processing is described at the beginning of this section.

(3) BUFFER CIRCUITS

The decoder makes use of two standard buffer circuits to provide signal outputs. The first circuit, a transistor switch with emitter tied through a diode to the +5.35-volt supply, is used for all command data bit outputs and the data "0" output to CDU A. The output is delivered from the transistor collector through a series resistance of 30 ohms. The data verification request output is also provided by this type of circuit, but without the diode. The second standard output is through a simple RC integrator which is used for the Load Programmer commands as well as the data outputs which are supplied to the programmers. The spare outputs are also provided by this type of buffer.

The three-level data verification signal to CDU A is formatted and buffered in a resistor summing network. The switched power telemetry signal and tone telemetry request to CDU A are provided directly from the decoder analog section by a resistor divider and transistor switch (output from collector through 1 kilohm series resistance), respectively. Power and ground outputs from the decoder come from the self-contained DC-to-DC converter; switched outputs of this type are delivered through relay contacts.

D. COMMAND DISTRIBUTION UNITS (CDU'S) A AND B

1. General Description

Two CDU's, Figure 2-IV-2, designated CDU A and CDU B, perform the decoding and command distribution functions for all but two of the realtime commands. The CDU's are located on opposite sides of the baseplate for mechanical balance considerations. Hereafter, both boxes will be referred to as "the CDU" unless one or the other is specifically designated.

The two boxes are not redundant; that is, CDU A could not be replaced by CDU B or vice-versa. Each CDU box controls a different set of functions, and, correspondingly, each decodes a unique group of commands. The CDU internal circuitry is designed so that redundancy is provided internally rather than between identical units.

All circuits in the CDU are composed of discrete components; no integrated circuits are used. The components used are as follows:

- Relays (latching and nonlatching);
- Transistorized circuitry (command decoding gates, level shifters, buffers, and ground switches for status indications);
- Frame pulse generators and circuitry (to produce a pulse when the telemetry commutator has completed a frame, which controls the removal of power from the commutator);
- Magnetic bias stepping switch driver and circuitry (to provide power drive to step the magnetic bias switch). The circuit has built-in timing which terminates the output after 150 milliseconds, thus preventing component damage if an abnormally long command pulse should occur accidentally;
- Push-to-talk (PTT) generators and circuitry (to provide an automatic turn-off pulse for various spacecraft functions). The cirucit includes nonlatching relays and timed drivers; and
- QOMAC coil drivers and circuitry (to provide current for the QOMAC coils).

As shown in Figure 2-IV-2, the CDU's are physically similar. Each CDU is housed in a box approximately 4 inches wide and 8 inches high; at approximately 8 inches long, the box for CDU A is approximately 1 inch longer than that for CDU B. Maximum weight for either CDU is approximately 6 pounds. CDU A contains eight component boards and a harness board; CDU B contains seven component boards and a harness board. In each CDU one "spare" board is provided so that additional decoding circuits or relays can be added and hard wired to perform additional functions without disrupting the existing circuits.

Wherever possible, functions associated with a subsystem are confined to one board to minimize interboard connections. Connections between the CDU boxes are also kept to a minimum. The CDU is designed to meet all applicable requirements of the reliability program plan. All parts have been selected, derated, and preconditioned in accordance with the standard parts list for ITOS.

2. Functional Operation

a. GENERAL

The CDU performs the following functions:

- Transform command bits received from either command decoder into command functions which are used to change the internal status of the CDU or are sent as control signals to other spacecraft subsystems;

- Acts as a switching device to connect power, as commanded, to redundant spacecraft subsystems;
- Controls the operation of various spacecraft subsystems and functions;
- Serves as a memory by storing commands;
- Interconnects and/or level-shifts spacecraft signals and routes them to appropriate subsystems;
- Performs automatic turn-off of various subsystems and functions whenever switched -23-volt decoder voltage to the CDU is removed; and
- Provides test points and telemetry outputs to permit monitoring of internal status.

The CDU receives the following inputs:

- 24 command bit lines from each decoder (12 Set I lines and 12 Set II lines);
- Switched -23-volt power from each decoder, which is used to power the decode gates associated with the respective decoder;
- Separate fused lines for each unit of each subsystem whose power is switched by relays located in the CDU;
- Control or status indication signals (these signals are used either to change the internal state of the CDU or they are level-shifted and routed to the appropriate subsystem);
- Telemetry signals to be processed;
- Emergency telemetry requests from each decoder; and
- Ground.

The following outputs are provided by the CDU to accomplish functional tasks:

- Decoded commands used to drive relays or other circuitry located within the subsystem concerned;
- Power switched through relay contacts located in the CDU;
- Transistorized buffer driver outputs where level-shifted control signals or power switching functions are accomplished with transistors;
- Telemetry signals which have been "processed" within the CDU;

- Housekeeping and digital telemetry power; and
- Internal telemetry and test points.

b. COMMAND DECODING

The ITOS commands (see Table 2-IV-1) are presented in a matrix format in Figures 2-IV-7 and 2-IV-8. These figures show which commands are under lock (LK) or toggle switch (TS) control in the CDA. Note that, in general, the command to choose side 1 of a redundant subsystem is in Set I and the corresponding command to choose side 2 is in Set II, with the same bits assigned. Thus a command transmitted in the wrong set will not effect another subsystem. Commands which would have a disruptive affect if inadvertently received, such as II - 4, 6 (Select Neither Programmer), have no counterpart in the opposite set (I-4, 6 is blank in Figure 2-IV-7).

Commands are decoded in series transistor AND gates, as shown in Figure 2-IV-9. Each decoder supplies 12 Set I bit lines, 12 Set II bit lines and a -23-volt (switched) line to each CDU as shown in Figure 2-IV-10. The -23-volt line is switched on to power the decoding gates in the CDU whenever the decoder is enabled to receive commands. Redundancy is maintained internally in the CDU in that any command can be actuated from either decoder.

The only difference between the TOS and ITOS decoding gate design is that the base hold-off resistor of the top transistor is returned to its own emitter rather than to the emitter of the bottom transistor as was the case in TOS. This modification results in less current drain on the bit lines without sacrificing reliability. Despite this change, care must be exercised in assigning additional commands in the future to avoid overloading any bit lines. The decode transistors for ITOS were changed to 2N2222A types, which have a lower V_{ce}, and the OR diodes were changed to 1N3600 types, which have better structural rigidity.

Bit lines originate from the collectors of PNP output buffer transistors located in the decoder. Bit lines corresponding to received bits are activated by pulses at approximately +4 volts for 100 milliseconds. The decoded output is used internally in the CDU to activate relays, is used as an input to other buffer circuits, or is sent out from the CDU as a control signal to a spacecraft subsystem.

c. DECODED COMMANDS AND THEIR FUNCTIONS

All commands decoded in the CDU are listed below, grouped by CDU and controlled subsystem. Brief descriptions of the actions caused by the commands

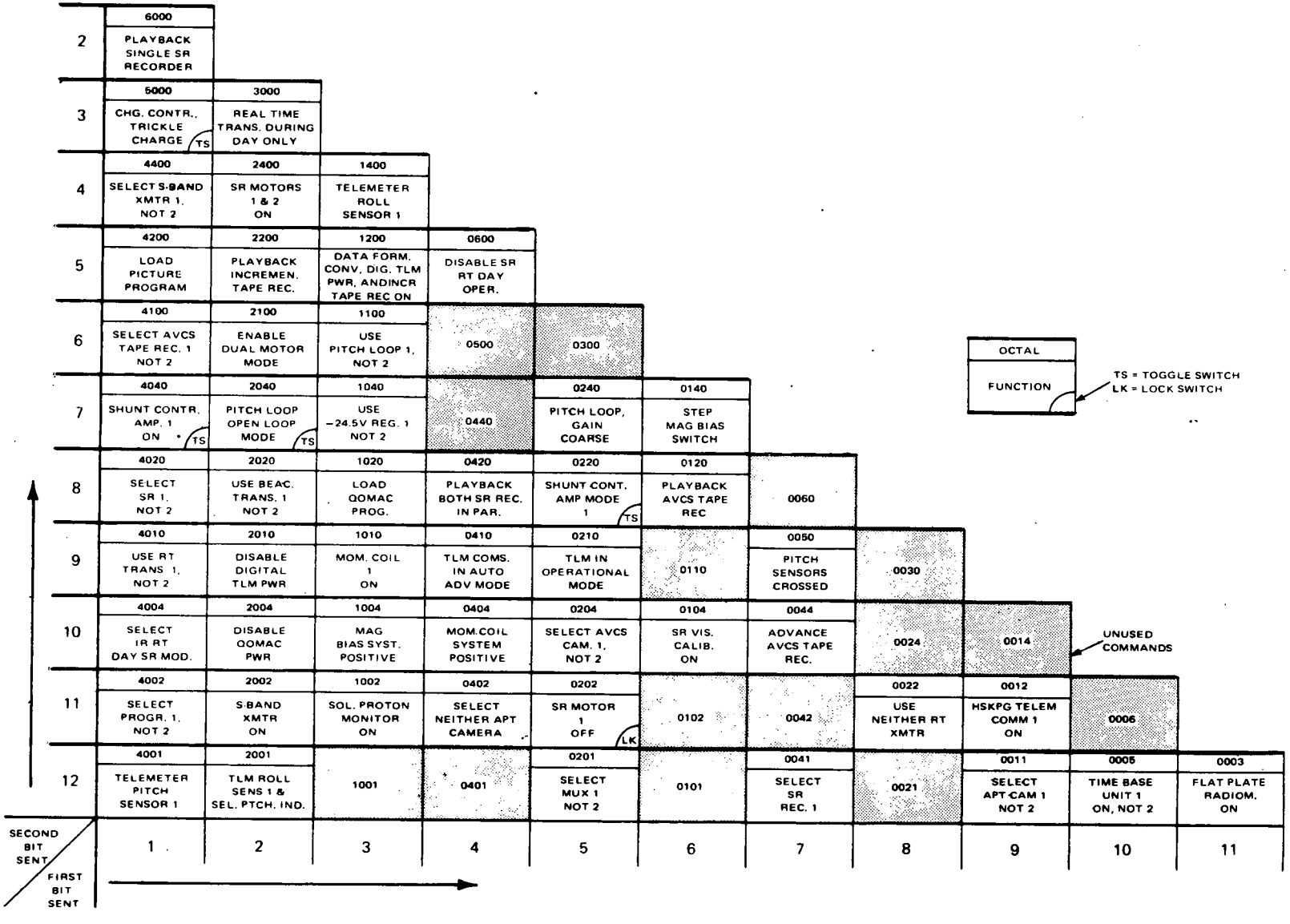

Figure 2-IV-7. Direct Command Matrix, Set I - Digital and Octal Codes

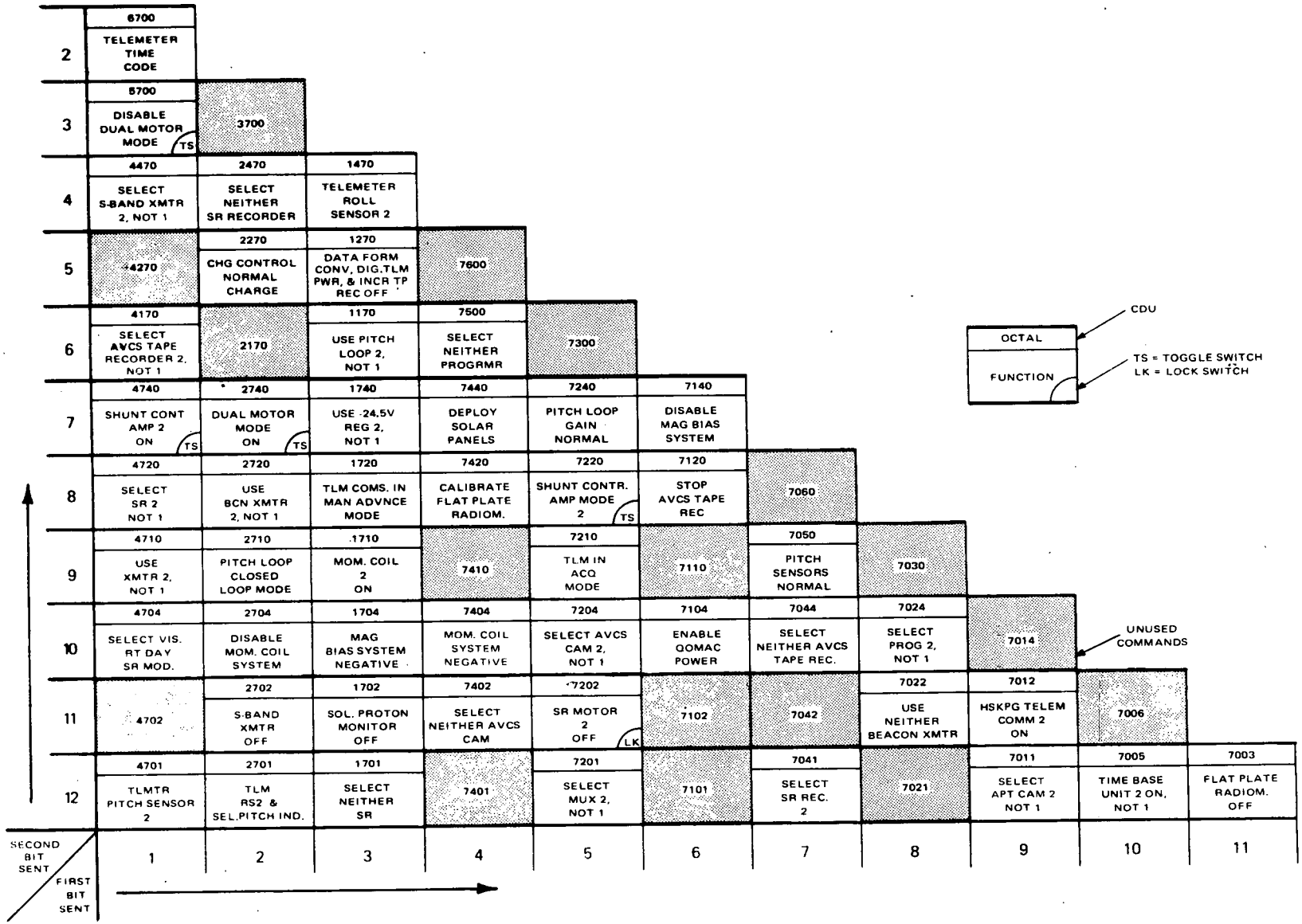

Figure 2-IV-8. Direct Command Matrix, Set II—Digital and Octal Codes

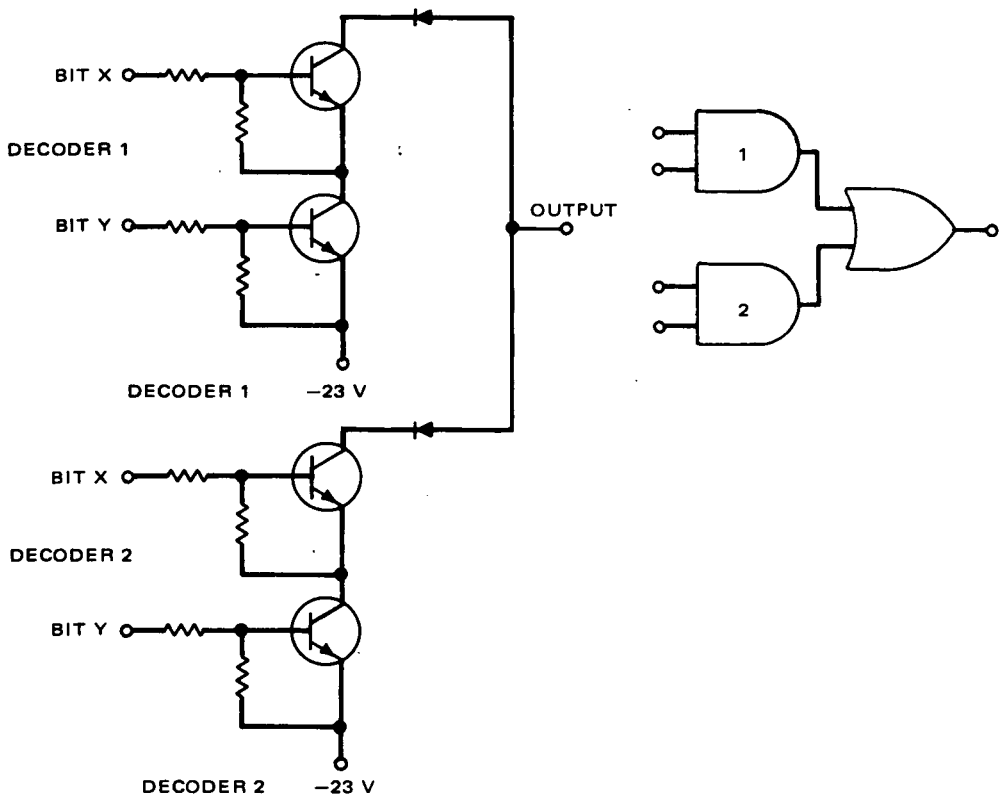

Figure 2-IV-9. Typical CDU Decoding Gate, Schematic Diagram

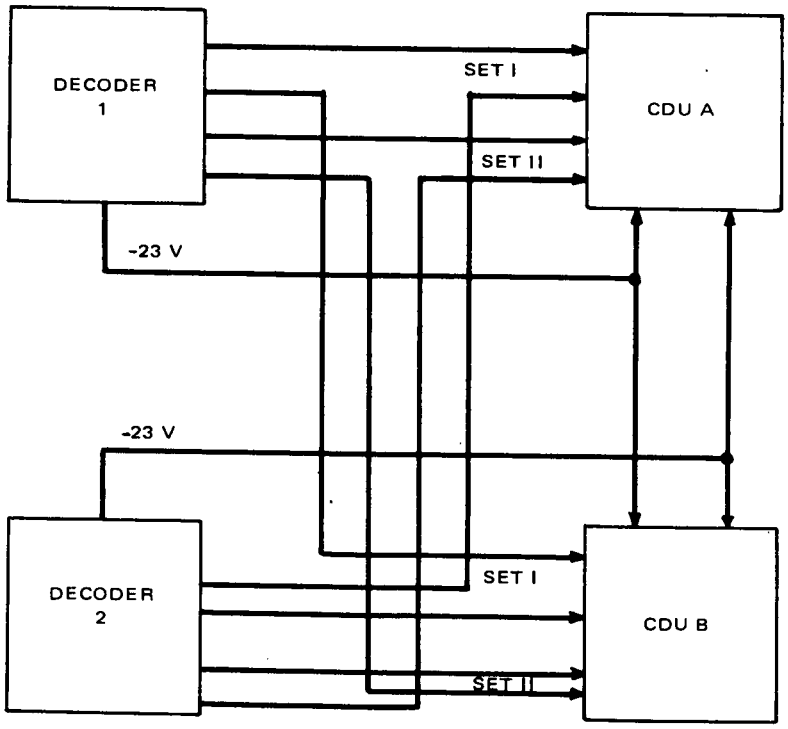

Figure 2-IV-10. Decoder and CDU Interconnections, Simplified Block Diagram

are given. The detailed logic diagrams for the CDU's are RCA Dwg. Nos. 1976085 and 1976086, respectively. These drawings are provided in a separate manual.*

Commands for controlled subsystems listed under subparagraphs (1) through (11) are decoded by CDU A and those under subparagraphs (12) through (21) by CDU B. The commands applicable to a controlled subsystem immediately follow that subsystem's listing. Each command is preceded by the number of the command set (Set I or II) of which the command is a part and the 2 data "1" bit positions in the 2-out-of-12 command word.

(1) SCANNING RADIOMETER (SR) SUBSYSTEM MOTOR CONTROLS

I - 2,4 SR Motors 1 and 2 ON

I - 5,11 SR Motor 1 OFF

II - 5,11 SR Motor 2 OFF

These commands are decoded and sent as command pulses to the SR subsystem where power is switched to the SR motors as indicated.

(2) SR ELECTRONICS

I - 1,8 Select SR 1, Not 2

II - 1,8 Select SR 2, Not 1

II - 3,12 Select Neither SR

These commands latch relays in the CDU, enabling level-shifting buffer drivers according to which side of the subsystem is chosen for operation. These buffer circuits are controlled by programmer signals which turn the selected SR electronics on according to program requirements. A special feature of the circuit causes a turn-off pulse to be sent to the SR whenever the command II-4,6 (Select Neither Programmer) is received.

I - 6,10 SR Visible Calibration ON

This command is decoded and sent out as a command pulse. The opposite function, SR visible calibrate off, is generated automatically by command I - 1,8 or II - 1,8 (Select SR Commands) or by a PTT pulse.

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*RCA Corporation, Astro-Electronics Division, TIROS M/ITOS Spacecraft Logic Diagrams, AED M-2175, Contract NAS5-10306, Princeton, N.J., June 15, 1969.

I - 1,10 Select IR Real-Time Day SR Modulation

II - 1,10 Select Visible Real-Time Day SR Modulation

I - 4,5 Disable SR Real-Time Day Operation

These commands are used to activate latching relays in the CDU which store the last command sent. Status indications of these relays are then sent to the SR processor and the programmer as control signals. Selecting either IR or visible modulation also sets the relays in the proper position to enable SR real-time day operation.

(3) SR RECORDER

I - 7,12 Select SR Recorder 1

II - 7,12 Select SR Recorder 2

II - 2,4 Select Neither SR Recorder

I - 1,2 Play Back Single SR Recorder

I - 4,8 Play Back Both SR Recorders in Parallel

Either, neither, or both SR recorders may be chosen by ground command. Recorder playback commands are implemented immediately, provided that the enabling condition of an S-band transmitter in operation is established. The record mode is not under ground station control via direct command. Two playback commands are provided; one for playback of a single recorder and one for both recorders simultaneously. When both recorders are commanded to play back, power is removed from the visible channel playback to both recorders and only IR and flutter-and-wow channels are powered. Logical interlocking prevents a playback command from being executed and a playback function from being maintained unless an S-band transmitter is on and a playback end-of-tape indication is not present.

Signals are sent to the programmer to indicate the status of the SR recorder (SRR) selection relays. These signals are fed to a flip-flop in the programmer whose outputs are returned to the CDU for use in the control logic of the playback controls. If both SR recorders have been selected and a Play Back Single SR Recorder command is given, the programmer will determine which recorder will play back. These programmer signals are disregarded for all other SRR logic combinations. If only one SRR has been selected and a Play Back Single SR Recorder or a Play Back Both SR Recorders in Parallel command is given, the recorder which has been selected will be enabled to play back if an S-band transmitter is on and if its playback end-of-tape signal is not present. If both SR recorders are playing back in parallel and either recorder reaches playback end-of-tape, the recorder not yet at end-of-tape will revert to the "playback single" mode of operation.

(4) REAL-TIME TRANSMITTER SUBSYSTEM CONTROLS

I - 1,9 Use Real-Time Transmitter 1, Not 2

II - 1,9 Use Real-Time Transmitter 2, Not 1

I - 8,11 Use Neither Real-Time Transmitter

I - 2,3 Real-Time Transmitter During Day Only

Either real-time transmitter, or neither, may be selected, but both cannot be selected at the same time. Selecting either transmitter resets the mode control relay so that the transmitter will remain turned on continuously. Command I - 2, 3 sets the mode control relay so that power to the chosen transmitter is toggled on by the day pulse and off by the night pulse as received from the programmer.

Every 48.5 days, the time base unit (TBU) will send a signal to the CDU which is used to turn off either transmitter that is operating, provided that the time code generator in use has not been reset. (Reset is accomplished by the transmission of either TBU selection command.) One of the selection commands must then be sent to reestablish transmission.

(5) APT CAMERA SUBSYSTEM CONTROL

I - 9,12 Select APT Camera 1, Not 2

II - 9,12 Select APT Camera 2, Not 1

I - 4,11 Select Neither APT Camera

Regulated power and shutter bus power are switched through selection relays in the CDU to the APT cameras. Either or neither camera may be selected but both cameras cannot be selected at the same time. Camera operation is controlled directly by the programmer without interfacing through the CDU. However, a signal is sent to the programmer indicating the status of the camera selection relays. This control signal is used to determine whether SR real-time data (if enabled) is to be sent full time on the real-time data link, which would be the case if neither APT camera were selected, or whether SR data is to be interleaved between APT pictures, which would be the case if either APT camera were selected.

(6) BEACON TRANSMITTER CONTROL

I - 2,8 Use Beacon Transmitter 1, Not 2

II - 2,8 Use Beacon Transmitter 2, Not 1

II - 8,11 Use Neither Beacon Transmitter

Power is switched to the beacon transmitter through relays in the CDU. Either or neither beacon may be selected but not both at the same time. Each beacon transmitter is modulated by two SCO's designed as SCO 1-1 or 2-1 (2.3 kHz), and SCO 1-2 or 2-2 (3.9 kHz). The first number in the SCO identification denotes the beacon transmitter with which the SCO is associated; the second number indicates its frequency. There is no cross-strapping between SCO's and beacon transmitters. When a beacon transmitter is selected, power is also supplied to both of the associated SCO's. The selection command also controls the output switching relay, thus coupling the selected beacon transmitter to the antenna.

(7) HOUSEKEEPING TELEMETRY SUBSYSTEM CONTROL

Relay switching within the CDU determines which of the available telemetry signals will be used to modulate the SCO. In the acquisition telemetry mode, the 3.9-kHz SCO's receive either housekeeping data, DSAS data, or command verification data; in the operational telemetry mode, SPM real-time data replaces DSAS data. In the acquisition mode, the 2.3-kHz SCO's receive either roll sensor data, summed roll sensor and pitch index pulse data, or time code data; the same data is received in the operational mode, with the addition of pitch sensor data.

Relay chains establish priorities for each telemetered function; the "priority trees" are shown in Table 2-IV-4.

(8) 3.9-kHz TELEMETRY SUBSYSTEM

I - 9, 11	Housekeeping Telemetry Commutator 1 ON
II - 9, 11	Housekeeping Telemetry Commutator 2 ON
I - 4, 9	Telemetry Commutators in Automatic Advance Mode
II - 3, 8	Telemetry Commutators in Manual Advance Mode
I - 5, 9	Telemetry in Operational Mode
II - 5, 9	Telemetry in Acquisition Mode

Both commutators (No. 1 and No. 2), either commutator, or neither may be chosen by ground station command. A mode selection command will program the selected commutator to read out a frame of housekeeping telemetry at the rate of 15 channels per second or to advance one step for each data "0" received from the decoder if no data verification or signal is present in CDU A. A commutator will also be selected when the "emergency tone TLM request" is received from decoder No. 1 or No. 2, and will advance in the automatic mode. Selection of either commutator also enables the housekeeping telemetry power bus. In the manual advance mode, the outputs of both commutators are sent to the SR processor and data format converter for recording on the SR recorder and incremental tape recorder, respectively.

TABLE 2-IV-4. TELEMETRY PRIORITIES

	3.9-kHz SCO's	
	SCO 1-2	SCO 2-2
Top Priority	Commutator No. 1 Commutator No. 2 Decoder No. 1 (data verification) Decoder No. 2 (data verification)	Commutator No. 2 Commutator No. 1 Decoder No. 2 (data verification) Decoder No. 2 (data verification)
(Acquisition Mode) (Operational Mode)	DSAS SPM	DSAS SPM
	2.3-kHz SCO's	
	SCO 1-1	SCO 2-1
Top Priority	Roll Sensor No. 1 Roll Sensor No. 2 Time Code Time Code Roll Sensor No. 1 and Pitch Index Roll Sensor No. 2 and Pitch Index	Roll Sensor No. 2 Roll Sensor No. 1 Time Code Roll Sensor No. 2 and Pitch Index Roll Sensor No. 1 and Pitch Index
(Acquisition Mode) (Operational Mode)*	Open Channel Pitch Sensor No. 1 or 2	Open Channel Pitch Sensor No. 1 or 2

*When pitch sensor data is selected, all other telemetry is removed from the 2.3-kHz SCO's, thus giving pitch data a form of top priority. However, pitch sensor data may subsequently be interrupted on ground command by any of the other data on that priority tree.

An "emergency tone telemetry request" signal from a particular decoder will result in the turn-on of an associated telemetry commutator and set the commutator in the automatic advance mode, provided the correct beacon transmitter is selected. The tone requests are complementary to the standard digital telemetry commands.

The "emergency tone TLM request" signals are interlocked with beacon transmitter power so that an emergency tone TLM request from decoder No. 1 (which turns on commutator No. 1 only) is recognized only when beacon transmitter No. 1 is on. A similar arrangement enables an "emergency tone TLM request" from decoder No. 2 (which turns on commutator No. 2 only) to be recognized only if beacon transmitter No. 2 is on. If the tone is maintained during the complete frame, automatic turn-off of the commutator is overridden.

A push-to-talk (PTT) signal removes the commutator outputs from the priority trees but does not remove power from the commutators or from the housekeeping telemetry power bus.

A frame pulse from either commutator, or the command to use neither beacon transmitter, will turn off both commutators and remove power from the housekeeping telemetry power bus.

A "data verification" signal may be received from either a decoder or a programmer. When present, it causes the data bit stream, as received from the decoder, to be switched onto the telemetry tree according to its priority, as given above.

In the acquisition telemetry mode, power is switched to the digital solar aspect sensor (DSAS). In the operational telemetry mode, this sensor is not powered.

(9) 2.3-kHz TELEMETRY SUBSYSTEM

I - 1, 12	Telemeter Pitch Sensor 1
II - 1, 12	Telemeter Pitch Sensor 2
I - 2, 12	Telemeter Roll Sensor 1 and Selected Pitch Index
II - 2, 12	Telemeter Roll Sensor 2 and Selected Pitch Index
II - 1, 2	Telemeter Time Code
I - 3, 4	Telemeter Roll Sensor 1
II - 3, 4	Telemeter Roll Sensor 2

These commands are used to switch telemetry to the SCO's in accordance with the priority tree, Table 2-IV-4. A passive summing network in the CDU adds the roll sensor inputs to the selected pitch index pulse input. These summed signals are provided as outputs to the SR processor, as well as being available internally for switching onto the telemetry tree.

(10) DIGITAL TELEMETRY SUBSYSTEM CONTROL

I - 3, 5	Data Format Converter, Digital TLM Power and Incremental Tape Recorder ON
II - 3, 5	Data Format Converter, Digital TLM Power and Incremental Tape Recorder OFF
I - 2.9	Disable Digital Telemetry Power

Power on the digital telemetry power bus is controlled by relay switching in the CDU. The command to turn on the data format converter (DFC) causes regulated power to be applied to the digital telemetry power bus. A command to turn off the DFC, or to disable digital telemetry, will connect the digital telemetry power bus in parallel with the housekeeping telemetry power bus. Thus, when power is applied to the latter, the digital telemetry bus will also be powered.

(11) DATA FORMAT CONVERTER AND ASSOCIATED SENSORS

I - 3, 5	Data Format Converter, Digital TLM Power and Incremental Tape Recorder ON
II - 3, 5	Data Format Converter, Digital TLM Power and Incremental Tape Recorder OFF
I - 11, 12	Flat Plate Radiometer ON
II - 11, 12	Flat Plate Radiometer OFF
II - 4, 8	Calibrate Flat Plate Radiometer
I - 3, 11	Solar Proton Monitor ON
II - 3, 11	Solar Proton Monitor OFF
I - 2, 5	Play Back Incremental Tape Recorder

These commands are decoded and sent as command pulses to the subsystem involved. Power to the incremental tape recorder (ITR) is also toggled by the data format converter ON and OFF commands, as is power to the digital telemetry power bus. Logical interlocking assures that the flat plate radiometer (FPR) will not be ON unless the DFC is also ON; i.e., the Data Format Converter, Digital TLM Power and Incremental Tape Recorder OFF command (II - 3, 5) also turns OFF the FPR (II - 11, 12) and the Flat Plate Radiometer ON command (I - 11, 12) also turns ON the DFC (I - 3, 5).

FPR calibration is turned ON by command II - 4, 8 but turned OFF by command I - 11, 12, Flat Plate Radiometer ON.

(12) TIME BASE UNIT

I - 10, 12 Time Base Unit 1 ON, Not 2

II - 10, 12 Time Base Unit 2 ON, Not 1

These commands are decoded and sent as command pulses to the dual time base unit (TBU). There are interlocking arrangements which assure that one side of the redundant TBU will always be powered, but that both will never be powered simultaneously. These commands also reset the time code generators.

(13) PROGRAMMER

I - 1, 11 Select Programmer 1, Not 2

II - 8, 10 Select Programmer 2, Not 1

II - 4, 6 Select Neither Programmer

These commands are decoded and sent as command pulses to the dual programmer. An interlocking function ensures that both programmers will not be on at the same time. The command to select neither programmer (II - 4, 6) is also used in CDU A to send a turn-off pulse to the selected scanning radiometer electronics.

(14) AVCS CAMERAS

I - 5, 10 Select AVCS Camera 1, Not 2

II - 5, 10 Select AVCS Camera 2, Not 1

II - 4, 11 Select Neither AVCS Camera

These commands toggle relays in the CDU, latching regulated-bus voltage and shutter-bus voltage to the selected camera. They are interlocked so that both cameras cannot be powered simultaneously.

(15) AVCS TAPE RECORDERS

I - 1, 6 Select AVCS Tape Recorder 1, Not 2

II - 1, 6 Select AVCS Tape Recorder 2, Not 1

II - 7, 10 Select Neither AVCS Tape Recorder

I - 6, 8 Play Back AVCS Tape Recorder

I - 7, 10 Advance AVCS Tape Recorder

II - 6, 8 Stop AVCS Tape Recorder

The selection commands toggle relays in the CDU, latching regulated-bus voltage to the selected tape recorder electronics and motor.

Playback of a recorder can occur only if an AVCS recorder has been selected, if an S-band transmitter is ON, and if a recorder end-of-tape signal is playback is not present. If any of these conditions is not satisfied, playback operation is disabled. Playback operation also terminates on the receipt of command II - 6, 8 (Stop AVCS Tape Recorder), a "PTT" signal, or an end-of-tape indication.

The AVCS camera selected, at the time a playback command is given, determines which track of the AVCS tape recorder will be played back. Therefore, playback of an empty channel results if camera selection at playback is different than that when the data was recorded.

Changing recorders during a playback operation causes the operation to cease at the point to which the tape has already advanced. Changing cameras causes the new channel to be played back without interrupting playback operation. The command to advance the recorder latches a relay in the CDU supplying a control signal to the AVCS recorders. Tape advance, except that commanded by the spacecraft programmer, is terminated by command II - 6, 8 (Stop AVCS Tape Recorder), or by a "PTT" signal.

The AVCS direct picture mode is not controlled by a unique set of commands. An enabling signal for this mode is generated whenever an AVCS camera and recorder have been selected and an S-band transmitter is ON. Data will be available for transmission only when the recorder is commanded into the record mode, by either the programmer or by the advance tape command.

(16) S-BAND TRANSMITTER AND MUX

I - 1, 4	Select S-Band Transmitter 1, Not 2
II - 1, 4	Select S-Band Transmitter 2, Not 1
I - 2, 11	S-Band Transmitter ON
II - 2, 11	S-Band Transmitter OFF
I - 5, 12	Select Multiplexer 1, Not 2
II - 5, 12	Select Multiplexer 2, Not 1

Unregulated bus voltage is switched through latching relays in the CDU to either of the S-band transmitters, but not to both simultaneously. Commands choose the transmitter to be used, and separate commands turn the selected transmitter ON or OFF. Application of power to either transmitter also supplies power to the multiplexer that has been selected, and supplies a signal to the DFC, the SR, and the AVCS tape recorder, thus enabling playback and the AVCS direct picture mode.

A "PTT" signal will turn OFF the chosen transmitter and multiplexer, thereby removing the playback and direct picture enable signal.

(17) POWER SUPPLY ELECTRONICS CONTROL

I - 3, 7	Use -24-Volt Regulator 1, Not 2
II - 3, 7	Use -24-Volt Regulator 2, Not 1
I - 5, 8	Shunt Control Amplifier Mode 1
II - 5, 8	Shunt Control Amplifier Mode 2
I - 1, 7	Shunt Control Amplifier 1 ON
II - 1, 7	Shunt Control Amplifier 2 ON
I - 1, 3	Charge Control Trickle Charge
II - 2, 5	Charge Control Normal Charge

These commands are decoded and sent to the power supply electronics (PSE) where they are used to perform switching functions as indicated by the command names. The four shunt control amplifier commands are necessary for prelaunch checkout of the shunt limiter operation; in no circumstances is it expected that these commands will be transmitted during the life of the spacecraft.

(18) PITCH CONTROL SUBSYSTEM

I - 3, 6	Use Pitch Loop 1, Not 2
II - 3, 6	Use Pitch Loop 2, Not 1
I - 2, 7	Pitch Loop Open Loop Mode
II - 2, 9	Pitch Loop Closed Loop Mode
I - 7, 9	Pitch Sensors Crossed
II - 7, 9	Pitch Sensors Normal
I - 5, 7	Pitch Loop Gain Coarse
II - 5, 7	Pitch Loop Gain Normal
I - 2, 6	Enable Dual Motor Mode
II - 1, 3	Disable Dual Motor Mode
II - 2, 7	Dual Motor Mode ON

These commands are decoded and sent to the pitch control electronics as command pulses. The commands to use either pitch loop No. 1 or pitch loop No. 2 also result in a command pulse to turn off the dual motor mode.

(19) ATTITUDE CONTROL COILS

(a) QOMAC and Magnetic Bias Coils

II - 6, 10	Enable QOMAC Power
I - 2, 10	Disable QOMAC Power
I - 3, 10	Magnetic Bias System Positive
II - 3, 10	Magnetic Bias System Negative
II - 6, 7	Disable Magnetic Bias System
I - 6, 7	Step Magnetic Bias Switch

Magnetic bias and QOMAC operations are controlled by commands and by programmer signals. The magnetic bias coil current is controlled by a stepping switch, advanced by command; however, QOMAC coil current is a fixed value. Magnetic bias polarity is controlled by command but QOMAC polarity and duty cycle are determined by the programmer. Selecting a polarity for the magnetic bias current power to be applied to the magnetic bias coil through the stepping switch also enables the switch to be stepped. When the stepping switch is in position 11 (high torque mode), the magnetic bias coil is operated by the same programmer signal as the QOMAC coil. However, power to the QOMAC and magnetic bias coils may be enabled or disabled independently by the enable or disable commands, respectively. In the high torque mode, the output of position 11 of the magnetic bias stepping switch is applied directly to the magnetic bias coil when the appropriate programmer signals are present, unless the QOMAC coil has been disabled. In that case, an 821-ohm resistor is connected in series with the output of position 11 of the stepping switch, and the current thus limited is applied to the magnetic bias coil. In all other positions of the stepping switch, the output of the switch is applied directly to the magnetic bias coil, independt of any QOMAC coil function.

In the high torque mode, a "QOMAC even" signal from the programmer sets the magnetic bias polarity relays to the negative torque position and a "QOMAC odd" signal sets them to the positive torque position.

(b) Momentum Coils

I - 3, 9	Momentum Coil 1 ON
II - 3, 9	Momentum Coil 2 ON
II - 2, 10	Disable Momentum Coil System
I - 4, 10	Momentum Coil System Positive
II - 4, 10	Momentum Coil System Negative

Power to the momentum coils is switched through enable/disable and polarity relays in the CDU. Either, neither or both coils may be selected for operation at the same time. The momentum coils are controlled by direct command only, and not by programmer signals as are the QOMAC coils. A polarity command operates on both coils so that they will always operate in parallel. A "PTT" signal turns off both coils but does not change the polarity selection.

(20) SOLAR PANEL SQUIB FIRING

II - 4, 7 Deploy Solar Panel

This command, from either of the two decoders, results in the operation of one of two redundant nonlatching relays for the duration of the command pulse period. The relays connect squib bus No. 1 (if decoder No. 1 is used) or squib bus No. 2 (if decoder No. 2 is used) to the solar panel squibs.

(21) NUTATION DAMPERS AND YO-YO'S

II - 4, 12 Uncage Nutation Dampers

I - 4, 12 Deploy Yo-Yo's

Circuitry to accomplish these two functions remains in the CDU although the functions are no longer required.

d. COMMAND SEQUENCING

There are a limited number of cases in which a specific sequence of commands must be sent in order to obtain the desired result. The following list includes those sequences concerned with relay switching within the CDU and does not include sequencing requirements in other subsystems receiving only command pulses from the CDU. The tabulation does not include the obvious sequences, such as the requirement that a recorder must be selected before a playback command can be actuated.

The magnetic bias coil must be enabled (which is accomplished by selecting a polarity for the coil) before the magnetic bias stepping switch can be advanced. To obtain high torque mode QOMAC (available for either normal or unipolar QOMAC) the magnetic bias stepping switch must be in position 11 and both the magnetic bias and QOMAC coils enabled.

The desired S-band transmitter must be selected before the turn-on command is given. Also a transmitter must be on before playback of an SR, AVCS, or incremental tape recorder can be accomplished.

The desired combination of AVCS camera and recorder should be chosen before a Recorder Playback command is given. Playback will be terminated if recorder selection is changed during a playback operation.

Similarly, SR recorder selection must be made before a playback command is sent. Enabling the second recorder while the first is in playback will not result in playback of the two recorders in parallel. The command to play back both recorders in parallel may be sent even if only one SR recorder is selected but only the selected one will respond, and then as if a playback command for only a single recorder had been received.

Telemetry outputs to the beacon SCO's is determined by the sequencing of commands given under telemetry command functions.

e. INTERLOCKED COMMANDS AND FUNCTIONS

Certain commands perform more than one functional operation. Also, certain resetting functions are the OR combinations of two commands to avoid unnecessary command allocations. These are as follows:

Command I - 3, 5 (Data Format Converter, Digital TLM Power and Incremental Tape Recorder ON) applies power to the DFC, the digital telemetry power bus, and the ITR.

Command II - 3, 5 (Data Format Converter, Digital TLM Power and Incremental Tape Recorder OFF) also switches the digital telemetry power bus in parallel with the housekeeping telemetry power bus and produces a command pulse to turn off the flat plate radiometer (FPR).

Command I - 11, 12 (Flat Plate Radiometer ON) also produces command pulses to turn on the data format converter and turn off FPR calibration.

Command II - 8, 11 (Use Neither Beacon Transmitter) also turns off both housekeeping telemetry commutators and removes power from the housekeeping telemetry power bus.

Command II - 4, 6 (Select Neither Programmer) also produces a command pulse to turn off the selected scanning radiometer.

Command I - 3, 6 (Use Pitch Loop 1, Not 2) or II - 3, 6 (Use Pitch Loop 2, Not 1) also produces a command pulse to reset the "pitch loop dual motor mode" of operation.

Command I - 1, 9 (Use Real-Time Transmitter 1, Not 2) or II - 1, 9 (Use Real-Time Transmitter 2, Not 1) also resets the mode of operation of the transmitters to full-time operation.

Command I - 1,10 (Select IR Real-Time Day SR Modulation) or II - 1,10, (Select Visible Real-Time Day SR Modulation) will also act to enable SR real-time day operation.

f. SPECIAL OPERATIONAL FEATURES

The CDU performs various functions automatically, or in response to input signals other than commands. The following is a list of these functions and operations.

(1) PUSH-TO-TALK OPERATION

Whenever the -23-volt power from a decoder is unlatched from the CDU, the push-to-talk (PTT) circuit generates a pulse which is used internally to terminate various functions; it is also sent as a command pulse to other subsystems. When a PTT pulse is generated, the following actions occur:

- AVCS, SR and incremental tape recorder playbacks are terminated,
- AVCS direct picture mode is terminated,
- S-band transmitter is turned off,
- Momentum coils are turned off,
- SR visible calibration OFF pulse is generated,
- AVCS recorder manual advance function is reset, and
- Housekeeping telemetry commutator outputs are removed from the beacon transmitter SCO's; however, power is not removed from the housekeeping telemetry power bus, and the commutators continue to function as commanded.

(2) EMERGENCY TONE TELEMETRY REQUEST

When the FSK enable tone is maintained for approximately 20 seconds, the decoder sends a signal to CDU A to turn on a telemetry commutator in the automatic advance mode. A signal from a particular decoder is interlocked with beacon transmitter power and a commutator such that a signal from decoder No.1 will turn on commutator No.1 if beacon No.1 is on, and a signal from decoder No. 2 will turn on commutator No. 2 if beacon No. 2 is on. However, either decoder will activate the automatic advance mode and apply power to the housekeeping telemetry power bus. If the tone is maintained through a whole readout frame of data, the automatic turn-off of the commutator will be overridden and consecutive frames obtained.

(3) TBU OVERFLOW

Every 48.5 days, a signal will be sent from the time code generator in use to the CDU, where it will be used to select neither real-time transmitter. This signal is used as a backup in case total capability to turn off the transmitter by command has been lost.

(4) QOMAC HIGH TORQUE MODE

When the magnetic bias stepping switch is in position 11, the magnetic bias coil will be operated by the same signals as the QOMAC coil, so that the coils will operate in parallel with their magnetic moments adding. Under normal operation, when the stepping switch is in position 11, full regulated-bus voltage is applied across the magnetic bias coil. However, if the QOMAC coil is disabled, a series resistor is inserted in the magnetic bias coil output lines. This limits current through the magnetic bias coil to a value which gives the same dipole moment obtainable from the QOMAC coil. In this mode, the magnetic bias coil is then capable of performing the QOMAC function.

(5) AVCS DIRECT PICTURE MODE

A direct picture output is available from the AVCS camera whenever the following three conditions are met: an AVCS camera is selected, a recorder has been selected, and an S-band transmitter is ON.

(6) TELEMETRY COMMUTATOR OUTPUTS

When the telemetry subsystem is in the manual advance mode, the outputs of the housekeeping telemetry commutators are supplied to the SR processor and data format converter for processing and recording on the SR and incremental tape recorders, respectively.

E. DUAL COMMAND PROGRAMMER

1. General Description

The dual command programmer (DCP), Figure 2-IV-2, includes two completely redundant circuits which are housed within a single unit. The term "programmer" is used hereafter to describe either of these redundant circuits; the term "dual programmer" (or DCP) is reserved to describe the unit containing both programmers. Each programmer receives real-time commands and data

from either of the spacecraft's two redundant decoders. Timing signals for the synchronous operation of the DCP digital logic are received from the time base unit (TBU). Either programmer, but not both, may be commanded ON at any time. The active programmer stores the decoder-supplied data, which contains the information necessary for the remote operation of the APT camera subsystem, the AVCS, the SR subsystem, and the QOMAC coil. The execution of the stored program may be modified by the real-time commands. Programmer outputs are distributed to appropriate spacecraft destinations either directly or via the command distribution units.

The basic technique of controlling event sequencing by counting the time elapsed from the start of an orbit is retained from previous TOS spacecraft. However, ITOS requirements demanded extensive modification to the TOS programmer with respect to the number of outputs provided, their destinations, and their timing. These changes have been necessitated mainly by:

- The presence of both AVCS and APT cameras on the same spacecraft for the first time,
- The addition of a scanning radiometer (SR) subsystem, requiring nighttime operation, and
- A TIROS M spin rate of one rotation per orbit, obviating the need for spin synchronization of the sensor subsystems.

The required programmer changes have been implemented by extending proven techniques used in the TOS equipment. These changes involved, mainly, the addition of new logic circuitry and the modification of previously existing circuitry to meet the new requirement outlined above. Some of the major sections of logic which are either new or have undergone extensive revision are:

- Rephasing word and APT picture inhibition circuitry,
- Unipolar torquing control circuitry,
- SR sequence control logic, and
- Numerous changes in the decoding circuitry to provide properly timed and sequenced outputs.

During the design phase, the DCP was the subject of a reliability analysis and a failure mode, effects, and criticality analysis. The former analysis estimates the failure rate for an individual ITOS programmer (one half of the DCP) to be 2.9077 percent per 1000 hours. The latter analysis uncovered a failure mode which was categorized as catastrophic at the DCP-CDU interface. This situation was remedied by making appropriate changes in the CDU buffer circuits.

a. PHYSICAL DESCRIPTION

The integrated circuits of each redundant unit within the DCP are mounted on 6 four-layer printed circuit boards (a total of 12 boards). In addition, 2 more printed circuit boards have mounted on them the discrete component mini-mod buffer circuits which serve both units of the DCP. The interconnections between these 15 boards are made by another four-layer printed circuit board (the harness board) into which the boards containing the integrated circuits and mini-mods are plugged. The harness board is wired from its underside through connectors to the power switching relays and the self-contained DC-to-DC converters.

All the above circuitry is packaged in a container which measures approximately 11-1/4 inches long by 4-3/4 inches wide by 8-3/4 inches high. The weight of the DCP is approximately 8.8 pounds.

b. FUNCTIONAL DESCRIPTION

An overall block diagram of the DCP is shown in Figure 2-IV-11. The detail logic diagram for the DCP is RCA Dwg. No. 1976084, which is provided in a separate manual.*

The two identical programmer circuits, each with its own DC-to-DC converter, are housed in a single dual programmer container and provide full redundancy of the programmer function. Either programmer can control remote operations (i.e., remote from CDA station contact) of the APT camera subsystem, the AVCS, the SR subsystem, and the QOMAC coil. During a CDA station contact, command data programs transmitted from the ground are routed to the programmer from one of the satellite decoders and are loaded into and stored in the selected programmer registers. The programmer then generates, at properly timed intervals, the signals required to control remote operation of the sensor subsystems and the QOMAC coil, in accordance with the command program. The programmer receives timing reference signals from the TBU which establish the counting rates for interval timing.

(1) PROGRAMMER INPUT AND OUTPUT INTERFACES

The dual command programmer receives the following inputs:

- Power (-24.5 volts regulated and ground).

*RCA Corporation, Astro-Electronics Division, TIROS M/ITOS Spacecraft Logic Diagrams, AED M-2175, Contract NAS5-10306, Princeton, N.J., June 15, 1969.

- A Programmer No. 1 ON command from CDU, which causes a latch-latching relay to apply power to programmer No. 1.
- A Programmer No. 1 OFF command from the CDU, which causes a latching relay to remove power from programmer No. 1.
- A Programmer No. 2 ON command from the DCU, which causes a latching relay to apply power to programmer No. 2.
- A Programmer No. 2 OFF command from the CDU, which causes a latching relay to remove power from programmer No. 2.
- A switched ground from either decoder, indicating that the associated decoder has its power turned off and the receipt of spurious data from that decoder is inhibited.
- A Load Picture Program command from either decoder, which resets the appropriate sections of the programmer and enables it to be loaded with a 28-bit T_0 word or rephasing word.
- A Load QOMAC Program command from the decoder which enables the programmer to accept 28 bits of QOMAC program digital data.
- Binary data in a 28-bit digital format from either decoder. This data may serve as a T_0 word, a rephasing word, or a QOMAC word.
- An "SR recorder 1 only selected" signal and an "SR recorder 2 only selected" signal from the CDU, which cause the timed control signals for SR recorder operation to be directed to the designated recorder.
- An "enable SR real-time day coverage" signal from the CDU, which causes the programmer to generate "SR modulator day enable" signals during parts of the day portion of each orbit. Real-time operation of the SR subsystem then takes place during the day portion of the orbit as described in Paragraph 2.IV.E.2.a.
- An "APT camera selected" signal from the CDU, which limits the amount of SR real-time day coverage as described in Paragraph 2.IV.E.2.a.
- An "AVCS playback end-of-tape 1" signal and an "AVCS playback end-of-tape 2" signal from the CDU which causes the programmer to generate a lengthened "AVCS run tape" output whenever the selected recorder has just completed playback.
- A 480-pps clock pulse from the time base unit, which is used throughout the programmer as a strobing pulse for many shifting functions.
- A 4-pps clock pulse from the time base generator, from which are derived a clock pulse with a 6.5-second period for timing all camera and SR remote operations and a clock pulse with a 4-second period for timing QOMAC remote operations.

The dual command programmer outputs are as follows:

- A "picture power on" level to the APT camera.
- A "prepare" pulse to the APT camera.
- A "filament power on" level to the AVCS camera.
- A "high voltage" signal to the AVCS camera.
- A "run tape" signal to the AVCS recorder.
- A "shutter start" pulse to the AVCS camera.
- A "shutter stop" pulse to the AVCS camera.
- A "vertical sync" pulse to the AVCS camera.
- A "clamp prepare" pulse to the AVCS camera.
- A "clamp hold" pulse to the AVCS camera.
- A "time code gate" to the AVCS camera.
- An "SR power ON" pulse to the CDU.
- An "SR power OFF" pulse to the CDU.
- A "modulator night enable" level to the SR processor.
- A "modulator day enable" level to the SR processor.
- An "SR recorder 1 record" level to the SR recorder.
- An "SR recorder 2 record" level to the SR recorder.
- A "use SR recorder 1" level to the CDU.
- A "use SR recorder 2" level to the CDU.
- A "day" pulse to the CDU.
- A "real-time night" pulse to the CDU.
- A "QOMAC ODD" signal to the CDU.
- A "QOMAC EVEN" signal to the CDU.
- A "data verification hold-on" signal to the CDU.
- A "programmer status telemetry" signal to the telemetry signal conditioner.
- A "QOMAC status" telemetry signal to the telemetry signal conditioner.
- An "SR status" telemetry signal to the telemetry signal conditioner.

- An "orbit counter clock" test point.
- A "QOMAC counter clock" test point.

(2) PROGRAM DATA LOADING

When a Select Programmer 1, Not 2 (or 2, Not 1) command is received by the spacecraft, a latching relay in the programmer becomes energized; this allows power to be applied to the DC-to-DC converter in the designated programmer, which, in turn, supplies voltages to the integrated circuits and to the interface circuits. At power turn-on, the programmer becomes completely reset and then enters a standby mode. The programmer remains in the standby mode until a load command is received; this command may be a Load Picture Program or a Load QOMAC Program command. If the command is a Load Picture Program command, the 28 bits of digital data which follow contain instructions pertaining to remote operation of the AVCS and APT camera subsystems, and the SR subsystem.

The 28 bits of data which follow a Load Picture Program command constitute either a "T_0 word" or a "rephasing word". Word identification is given by the first 2 of the 28 bits. These 2 bits are decoded and an enabling signal is sent to either the T_0 word control logic, or to the rephasing word control logic, to permit the loading of the remaining bits of the program data into the appropriate register. The T_0 word data (see Table 2-IV-5) includes the T_0 delay time (i.e., time from loading of the programmer until T_0, the defined night-to-day transition of the orbit) and the orbit correction factor, which establishes the exact duration of the orbit in the orbit counter. The rephasing word data (see Table 2-IV-6) includes the number of phasing correction counts, the polarity of the phasing correction, and the mode of recorded SR operation (day and night or night only); it also controls the amount of APT and/or SR real-time day coverage per orbit.

The data verification level is generated at the trailing edge of a 100-millisecond Load Picture Program command pulse, and the 3-stage picture program word identification counter and decoder are enabled. The first 2 bits of the word are decoded to determine if the remaining 26 bits contain a T_0 word or a rephasing word. If the data is a T_0 word, the T_0 control logic enables the 12-stage orbit correction shift register, and 12 bits of data are shifted into the register. The first bit to enter the register is not used. The other 11 bits form the 2's complement of the T_0 delay time. After loading, these bits are parallel-transferred to the 11-stage counter and the next 12 bits of the program (bits 15 through 26) are then shifted into the register. Of these, only bits 17 through 26 are used. These bits represent the true orbit time minus 640 counts and are called the orbit correction factor. Bits 27 and 28 are not used by the programmer. The

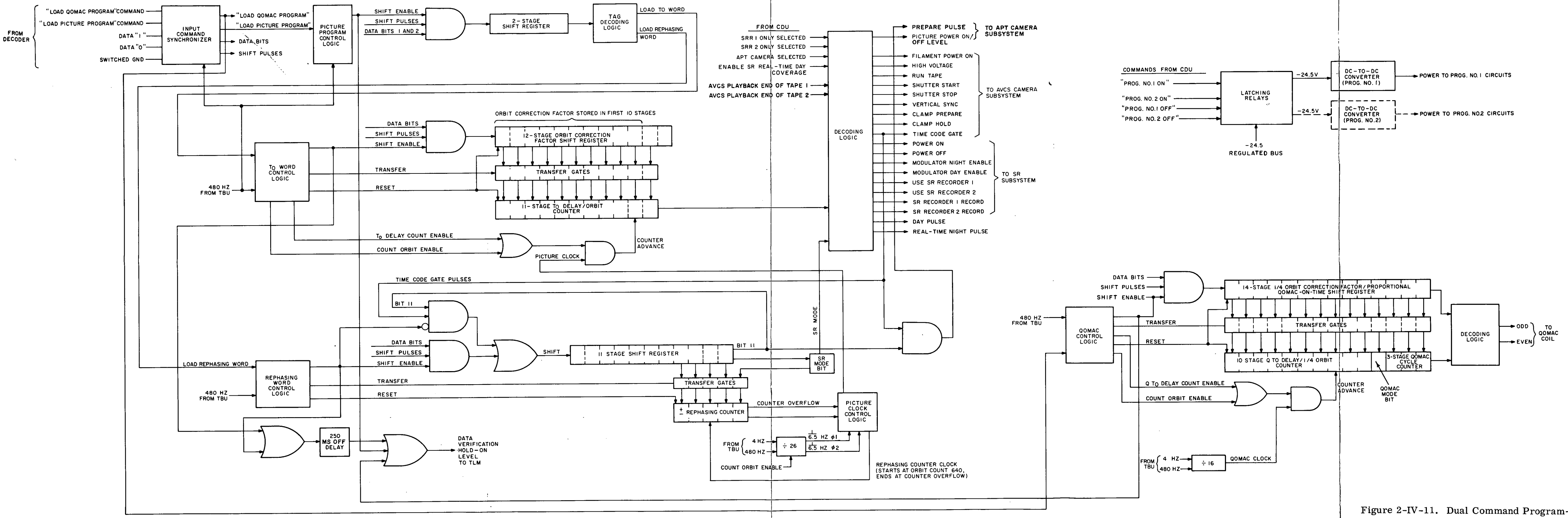


Figure 2-IV-11. Dual Command Programmer, Block Diagram

TABLE 2-IV-5. FORMAT OF T_0 WORD*

Bit No.	Function
1, 2	Bit 1 is a data "1", bit 2 is a data "0" in the T_0 word
3	Not used by programmer
4 through 14	2's complement of the number of 6.5-second intervals from the end of loading the programmer until the first transition of the spacecraft from orbit night to orbit day (T_0) - called "T_0 delay time"
15, 16	Not used by programmer
17 through 26	2's complement of the number of 6.5-second intervals in the true orbit time minus 640 counts - called "orbit correction factor"
27, 28	Not used by programmer
* The T_0 word must be preceded by Load Picture Program command.	

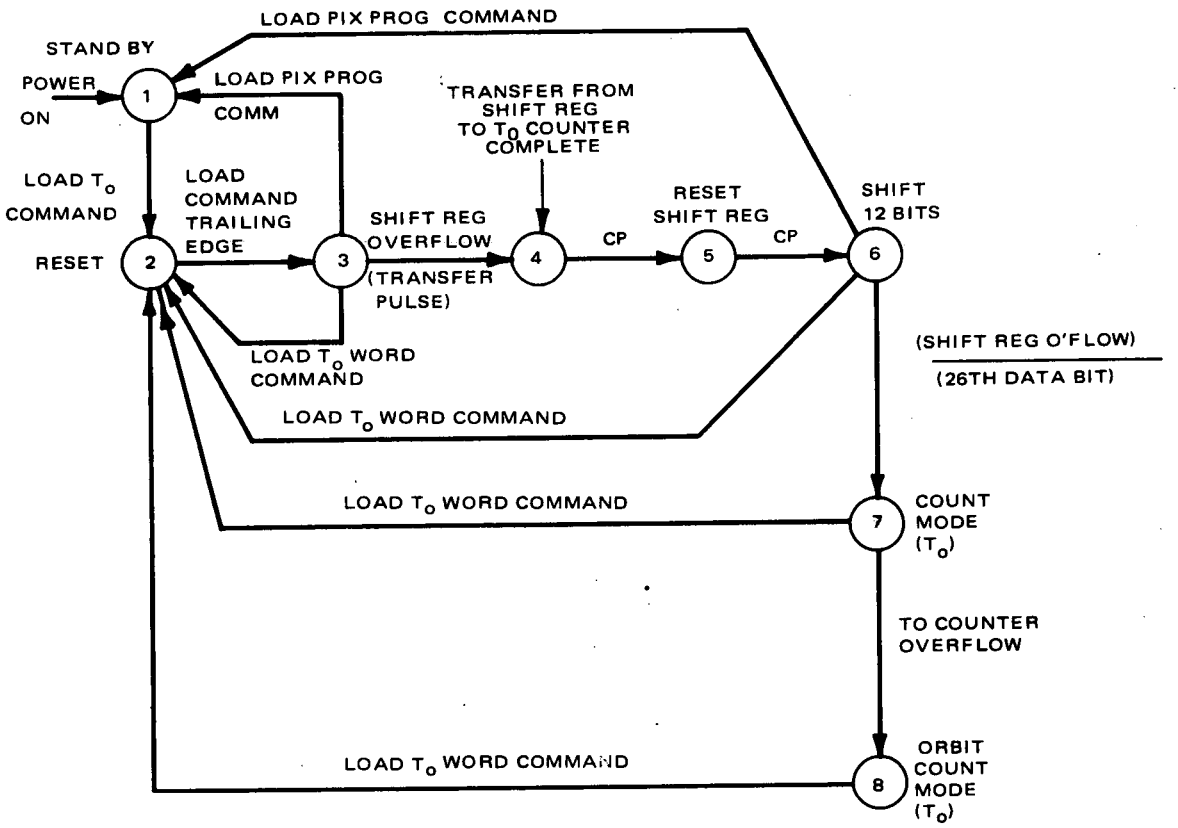
data verification signal is terminated 250 to 500 milliseconds after the end of bit 26. After loading has been completed, the 11-stage counter commences counting the T_0 delay time with counts occurring at 6.5-second intervals. The orbit correction factor continues to be stored in the register until after the T_0 has been counted out. At count T_0 plus 640, the factor is parallel-transferred (without destruction in the register) to the counter, which continues to the next T_0 (counter overflow) to establish the corrected orbit duration. The orbit correction factor remains stored in the register and corrects the duration of succeeding orbits until the programmer is turned off, or the register is reloaded. The flow diagram describing the operation of the T_0 word sequencer, which controls the handling of T_0 data, is shown in Figure 2-IV-12.

If the data following a Load Picture Program command is a rephasing word, the 5 data bits following the 2-word identification bits are shifted into the rephasing shift register and transferred to the rephasing counter. Bits 8 through 14 are not used by the programmer. Bits 15 through 26 are shifted into the register and stored to control remote APT and SR operation. Bits 27 and 28 are not used by the programmer. The data verification signal is terminated 250 to 500 milliseconds after the end of bit 26. Bit 15 is stored in the SR mode stage of the register and its value controls the outputs of the orbit counter decoding logic to the SR recorders. If a data "1" is stored in this stage, the output signals are provided to permit SR recorder operation during both the day and night portions of the orbit. If a data "0" is stored, the SR recorder output signals are generated

TABLE 2-IV-6. FORMAT OF REPHASING WORD*

Bit No.	Function
1, 2	Bit 1 is a data "0", bit 2 is a data "1" in the rephasing word
3 through 6	2's complement of the selected number of phasing correction counts; from 1 to 15 counts can be programmed
7	Polarity of the phasing correction. A data "1" causes the selected number of phasing counts to be subtracted from the orbit count; a data "0" causes the selected number of phasing counts to be added to the orbit count.
8 through 14	Not used by programmer
15	A data "1" causes SR data to be recorded during both day and night portions of the orbit. A data "0" causes SR data to be recorded during orbit night only.
16 through 26	These 11 bits represent the 11-pictures in the full APT camera sequence. Any combination of the 11 APT pictures may be omitted or included in the sequence by programming a data "0" for each picture to be included and a data "1" for each picture to be omitted. This data also affects the extent of real-time SR day coverage in certain operational mode.
27, 28	Not used by programmer
* The rephasing word must be preceded by Load Picture Program command.	

only during the night portion of the orbit. The 11 bits stored in the remaining stages of the shift register control the APT and SR sequencing. They accomplish this by controlling the generation of the APT prepare pulse for each individual APT picture, and by controlling the generation of the SR modulator day enable level. Bit 16 controls the prepare pulse immediately following programmer loading. The shift register recirculates the 11 bits once each orbit to permit their effect to be repeated on successive orbits. During the first night portion of the orbit following loading of a rephasing word, the counter in which rephasing word bits 3 through 6 are stored commences counting (at T_0 plus 640). This causes the programmed number of counts to be added to or subtracted from (depending on the value of bit 7) the number of picture clock pulses generated in the picture clock control logic and supplied to the orbit counter. Thus, time T_0 may be shifted in either direction with respect to the actual night-to-day transition point in the orbit. The flow diagram which describes the rephasing of the orbit counter clock is shown in Figure 2-IV-13.



SHIFT MODE – STATES 3, 4, 5, AND 6
COUNT MODE – STATES 7 AND 8
RESET – STATES 1 AND 2
SHIFT REG RST – STATES 1, 2, AND 5
DATA TRANSFER = (STATE 3) * (REGISTER OVERFLOW)

Figure 2-IV-12. T_0 Word Sequencer Flow Diagram

The identification of the picture program data as either a T_0 or rephasing word is performed by a separate sequencer, within the programmer, which decodes the first 2 bits in the data word. Figure 2-IV-14 is a flow diagram which describes the decoding operation. Also shown in this figure is the generation of the data verification level for this data.

If the command is a Load QOMAC Program command, the 28 bits of data which follow contain instructions for remote operation of the QOMAC coil (See Table 2-IV-7 for the format of the QOMAC Program Word). The trailing edge of the 100-millisecond command pulse enables the 14-stage shift register, and the 28-bit digital data word begins to shift into the register. At the same time, the data

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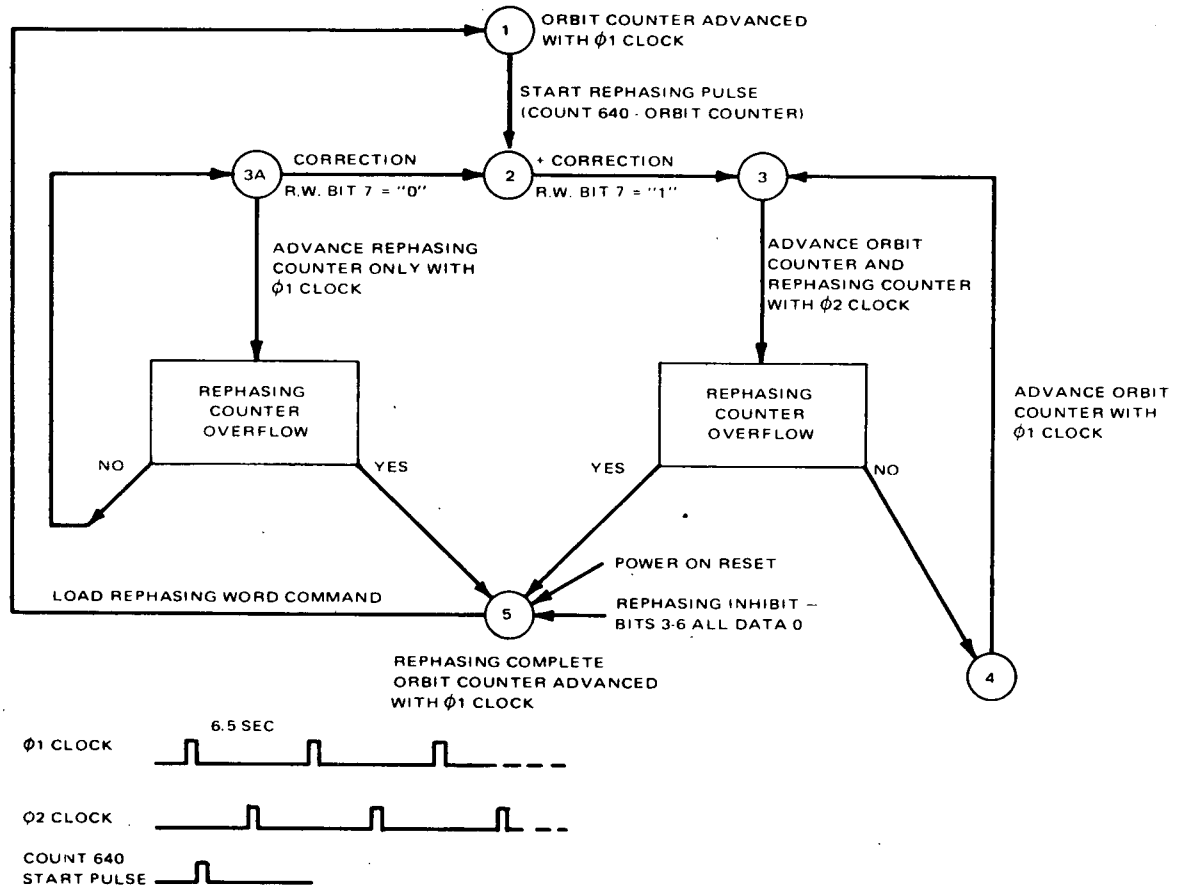


Figure 2-IV-13. Orbit Counter Clock Rephasing, Flow Diagram

verification hold-on level is generated. When the first 14 bits of data have been shifted into the register, an overflow signal causes the parallel transfer of these bits into the "count" registers. The first 3 bits, representing the number of QOMAC cycles to be performed, are transferred into a 3-stage counter. If the program is a unipolar torquing program, these bits are not used. The 4th is the QOMAC mode bit, denoting whether normal QOMAC or unipolar torquing operation is to be performed. The remaining 10 bits are transferred into a 10-stage counter which counts the delay until QT_0, the time at which remote QOMAC operation begins. When these bits have been transferred, the shift register resets and the remaining 14 bits of the program enter the shift register. These bits are used after QT_0 to control the actual QOMAC operations. When this second group of 14 bits is stored as indicated by an overflow signal, no further data bits can be accepted (without a new Load QOMAC Program command) and the programmer enters a count mode. The data verification level is then terminated.

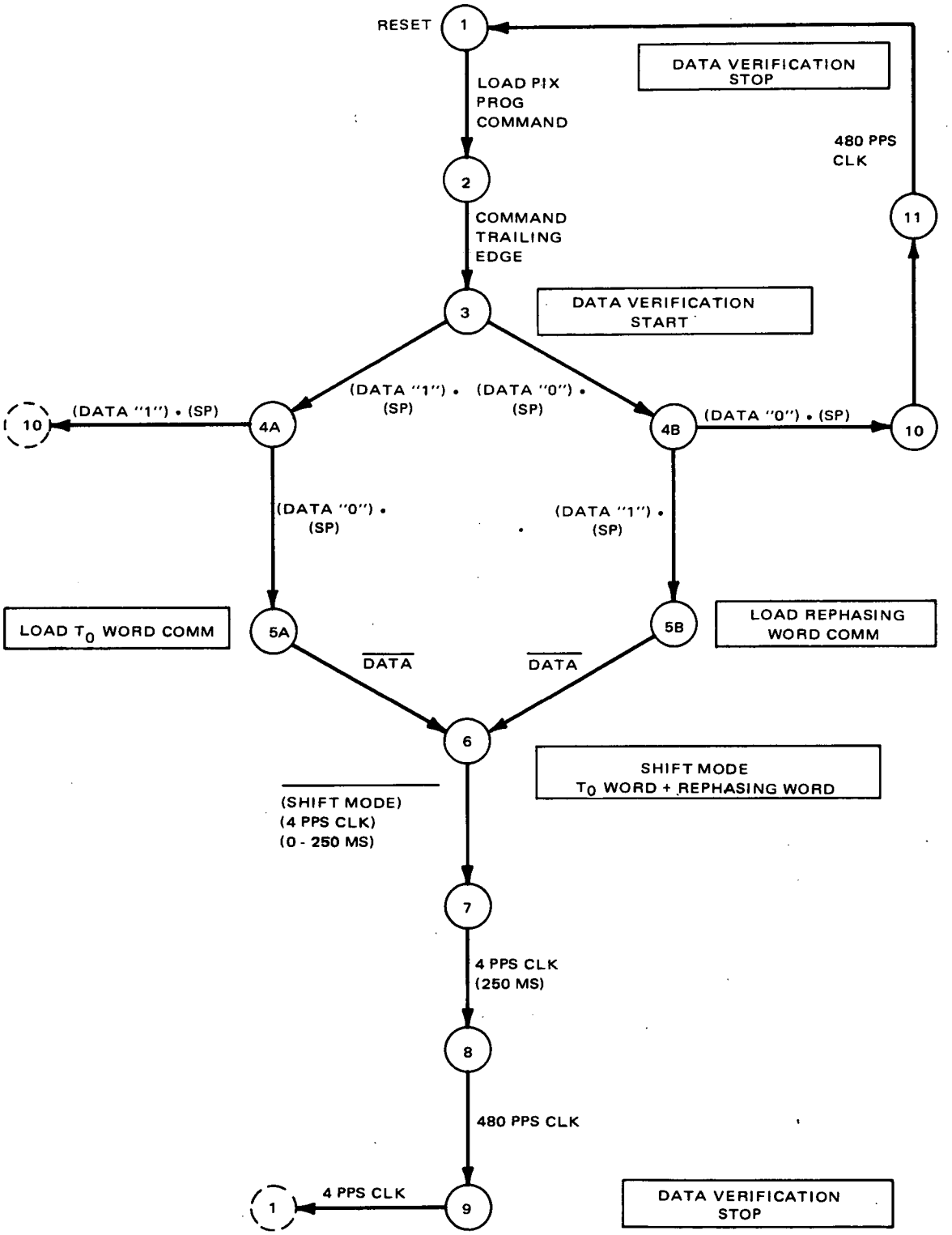


Figure 2-IV-14. Load Picture Program Command Tag Sequencer and Data Verification Extender, Flow Diagram

TABLE 2-IV-7. FORMAT OF QOMAC PROGRAM WORD*

Bit Number	QOMAC (Bit 4 must be a data "0")	Unipolar Torquing (Bit 4 must be a data "1")
** 1 through 3	2's complement of the number of QOMAC cycles to be performed (from 1 to 8)	Not used
** 4	Data "0"	Data "1"
5 through 14	2's complement of the delay time until the first quarter-orbit timing begins. Delays of 1 to 1024 counts in 4-second increments may be programmed.	Same as for QOMAC
15 through 21	Not used	2's complement of the actual portion of each quarter orbit, in 16-second increments, during which the QOMAC coil will be energized when proportional QOMAC operation is being used
22 through 28	2's complement of the true quarter-orbit time minus 256 counts, in 4-second increments; corrects the quarter-orbit counter to the exact quarter-orbit time	Same as for QOMAC

* The QOMAC program word must be preceded by a Load QOMAC Program command.

** If bits 1 through 4 are all data "1's", QOMAC operation stops and the QOMAC logic returns to the standby condition.

2. Operating Modes

a. AVCS, APT, AND SR CONTROL

During the day portion of the orbit, the AVCS and APT camera subsystems will normally perform 11 picture-taking cycles each, the APT picture data being transmitted in real time to local stations and the AVCS data being recorded for later playback to a CDA station. SR sequencing will be normally performed during both the day and night portions of each orbit.

(1) MODE 1

When the normal mode of SR operation; i.e., Mode 1, has been selected by coding bit 15 of the rephasing word as a data "1" and by supplying the "enable real-time day coverage" signal from the CDU, the detailed sensor sequencing program, after data reception and storage, proceeds as described below. The picture program counter is advanced in 6.5-second increments (the times referred to in this discussion are counts of 6.5 seconds each). Typical timing of sensor sequencing is shown in Figure 2-IV-15. Detailed timing of the APT and AVCS camera signals are shown in Figure 2-IV-16. In the step by step program outlined here, the "APT camera selected" signal from the CDU is assumed to be present.

1. T_0 is defined as the time of transition from nighttime to daytime operations, the time at which the programmer orbit counter overflows (or resets). The loading of T_0 word data may occur during any portion of the orbit. After the reception of data, the time to the next night-to-day transition of the spacecraft is counted out; following this, the orbit counter begins to count the time required for successive complete orbits.

2. When the T_0 word data is loaded, the "SR power on" pulse is generated. The pulse width at this time is 40 milliseconds. Also at this time, the "SRR 1 record" level is generated unless the SRR 2 Selected command from the CDU is present; if this command is present, the "SRR 2 record" level is generated instead. The "SRR record" level (1 or 2) will remain as originally generated throughout the T_0 delay time unless the opposite SRR Selected command is received from the CDU. Alternating the CDU commands will cause continual switching of the SRR chosen for recording.

3. During the time of the T_0 delay, the "use SRR 1" level is generated whenever the "SRR 1 record" level is generated; the "use SRR 2" level is generated whenever the "SRR 2 record" level is generated during this time.

4. At the time the T_0 word data is loaded, the "SR modulator night enable" level is generated.

5. At count T_0 minus 1 (i.e., 6.5 seconds before T_0), the "APT picture power on" level is generated.

6. At count T_0 minus 1, the 6.5-second "day" pulse is initiated.

7. At count T_0 minus 1, the "AVCS filament power" level is generated.

8. At count T_0 minus 1, the "SR modulator night enable" level is terminated.

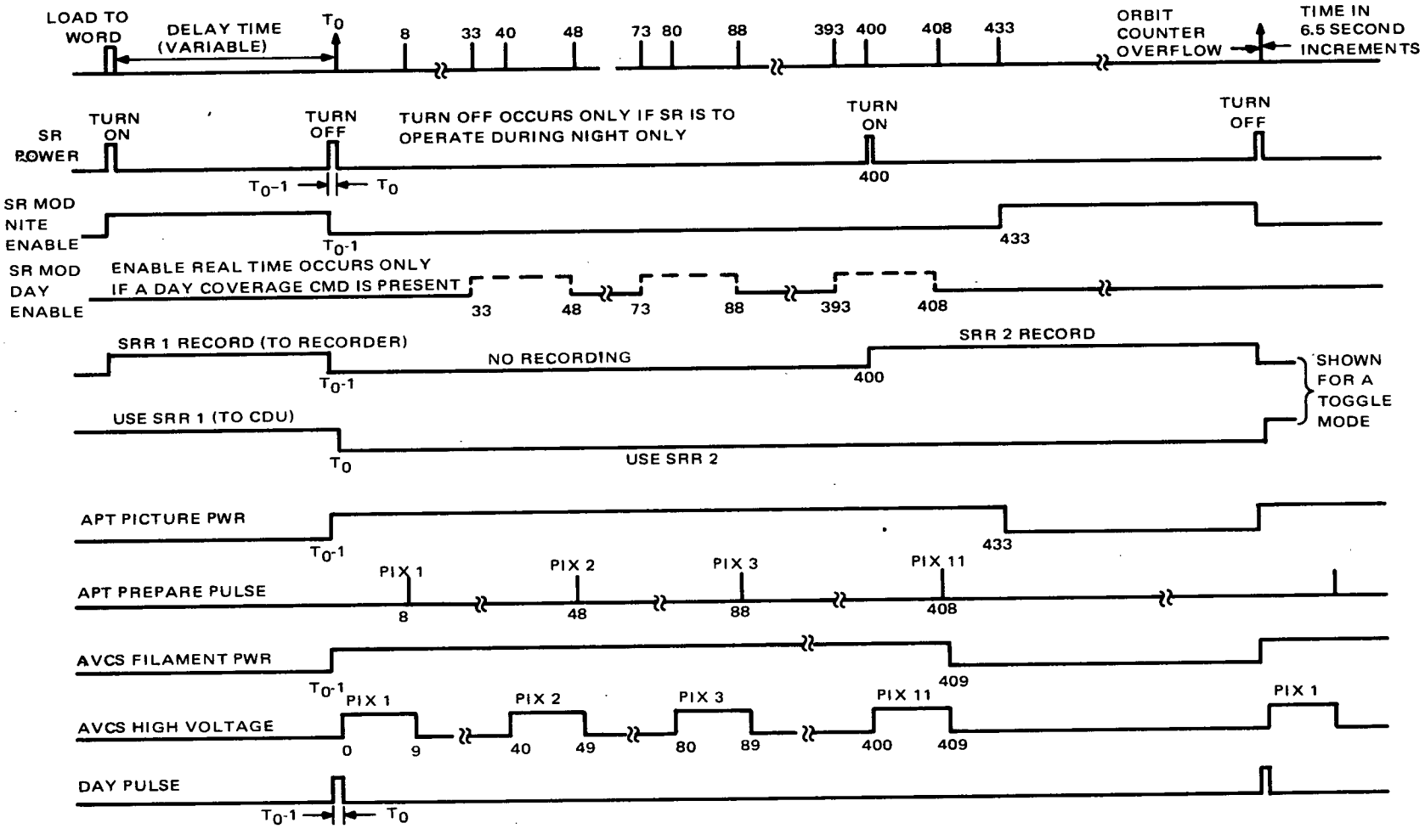
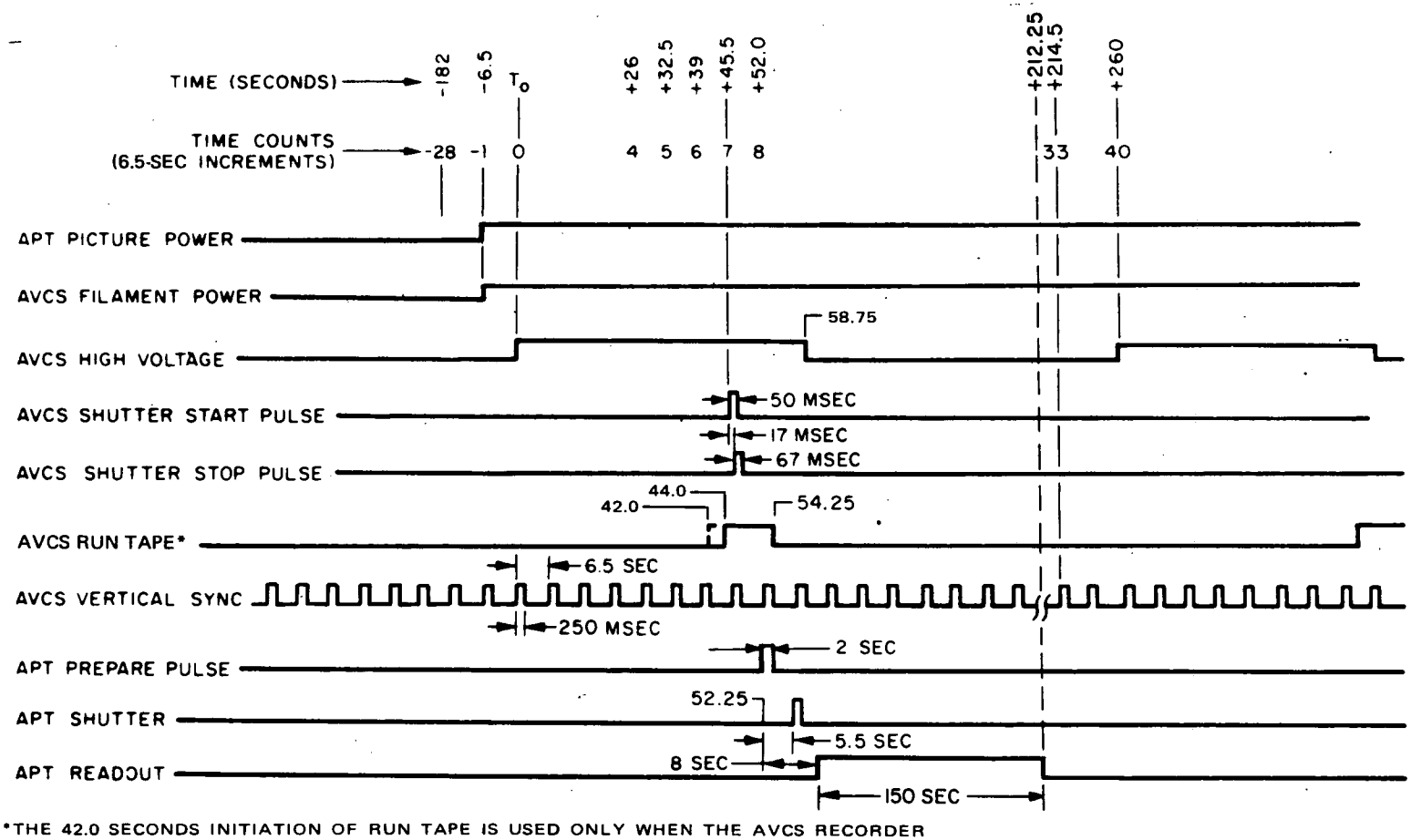


Figure 2-IV-15. Sensor Sequencing, Typical Gross Orbital Timing



*THE 42.0 SECONDS INITIATION OF RUN TAPE IS USED ONLY WHEN THE AVCS RECORDER IS SENSED TO BE IN PB END-OF-TAPE.

Figure 2-IV-16. AVCS and APT Camera Control, Timing Diagram

9. At count T_0, if neither SRR Selected command is being provided by the CDU, the "SRR record" and "use SRR" levels toggle and are, therefore, generated for the SRR (1 or 2) which was unused immediately prior to time T_0. If an SRR Selected command is being provided by the CDU, no toggling of these signals takes place. These signals (1 or 2) will remain as originally established at T_0 for the duration of the orbit unless the opposite SRR Selected command is received from the CDU. Alternating the CDU commands will cause continual switching of the SRR chosen for recording.

10. At T_0, and every 6.5 seconds thereafter as long as the AVCS filament power is on, a vertical sync pulse, having a pulse width of 250 milliseconds, is generated.

11. At count T_0, AVCS high voltage level is generated.

12. At T_0 plus 6 counts, the "AVCS clamp prepare" pulse is generated; the pulse width is 250 milliseconds.

13. At T_0 plus 6 counts plus 3.0 seconds, the "AVCS run tape" signal is generated, if and only if both "playback end-of-tape" signals from the CDU are absent. If either of the CDU signals are present, the "AVCS run tape" signal is generated beginning at T_0 plus 6 counts plus 5.0 seconds.

14. At T_0 plus 7 counts, the "AVCS clamp hold" pulse and the "AVCS shutter start" pulse are generated. The clamp hold pulse has a 6.5 second width. Seventeen milliseconds after the "AVCS shutter start" pulse is generated, the "AVCS shutter stop" pulse is generated. The former pulse has a duration of 50 milliseconds; the latter has a duration of 67 milliseconds.

15. At T_0 plus 8 counts plus 0.25 second, the "APT prepare" pulse is generated. The time of the prepare pulse is chosen so that any transients due to the APT shutter (which is activated by the camera 5.5 seconds after the prepare pulse) will not affect the quality of the AVCS picture. Likewise, during APT camera readout, which lasts until approximately T_0 plus 33 counts, no AVCS camera transients occur that might affect APT picture quality. Note that the APT pulse may be inhibited by stored rephasing word data as described in paragraph 2.IV.E.1.b.(2). Also at T_0 plus 8 counts plus 0.25 second, the "AVCS time code gate" plus is generated.

16. At T_0 plus 8 counts plus 2.25 seconds, the "APT prepare" pulse, and the AVCS "run tape" and "time code gate" signals are terminated.

17. At T_0 plus 9 counts plus 0.25 second, the "AVCS high voltage" signal is terminated.

18. At T_0 plus 33 counts, the "SR modulator day enable" signal is generated, but only if the succeeding "APT prepare" pulse, which occurs at T_0

plus 48 counts plus 0.25 second, is not inhibited by stored rephasing word data as described in paragraph 2.IV.E.1.b.(2).

19. At T_0 plus 40 counts, the AVCS high voltage is again turned on and the operations described in steps 11 through 18 are repeated; this process is repeated at 40-count intervals.

20. At T_0 plus 48 counts plus 0.25 second, the "SR modulator day enable" signal, if present, is terminated; this event is repeated at 40-count intervals.

21. At T_0 plus 400 counts, an "SR power on" pulse is generated. The pulse width at this time is 250 milliseconds. Note that in the mode of SR operation being described (Mode 1) the SR subsystem is already on at this time.

22. At T_0 plus 408 counts plus 2.25 seconds, the "SR modulator day enable" signal, if present at this time, is terminated for the remainder of the orbit.

23. At T_0 plus 409 counts plus 0.25 second, the "AVCS filament power" level is turned off to terminate AVCS picture-taking for the remainder of the orbit.

24. When T_0 plus 433 counts is reached, the "APT picture power on" level is terminated to end APT picture-taking for the remainder of the orbit. Also at this time, a pulse which signals the transition from the daytime to the nighttime portion of the orbit is generated and is designated the "real-time" pulse. This pulse is 250 milliseconds wide. Finally, at this time the "SR modulator night enable" level is generated.

25. At T_0 plus 640 counts, the 11th stage of the orbit counter is set and the contents of the first 10 stages of the orbit correction shift register (programmer data bits 17 through 26) are transferred into the first 10 stages of the orbit counter. The counter then counts in normal binary fashion until the next T_0 or overflow of the counter. An overflow from the first 11 stages of the counter occurs at the next night-to-day transition of the spacecraft. This event is a cyclical one-orbit displacement from the original T_0 and is also labeled T_0. One count before this T_0, the "APT picture power on" level is again generated, the "day" pulse is generated, the "SR modulator night enable" signal is terminated, and the "AVCS filament power" level is again turned on. Succeeding events recur as described above in steps 9 through 25.

26. The programmer continues to repeat the same picture-taking and scanning radiometer operations until either the active programmer is turned off, or the real-time commands supplied to it are changed, or a new Load Picture Program command is received from a CDA station. Note that a rephasing word may be loaded without disturbing the

continuity of an orbit count in progress. Of course, any change in pertinent rephasing word bits will be reflected by their effect on the generation of certain sensor signals and their timing.

The normal orbit sequencing of the camera subsystems and the scanning radiometer subsystem may be altered to achieve additional operational modes. The difference between the normal mode described above and the other modes involves the periods during which signals are generated for the SR system.

(2) MODE 2

As described above, in the normal mode, the SR subsystem operates during both orbit day and orbit night. In the first alternative (Mode 2) to the normal mode, the SR subsystem is commanded (by continuing to supply the "enable real-time day coverage" signal from the CDU and inserting a data "0" in bit position 15 of the rephasing word) to provide real-time coverage during both the day and the night portions of the orbit but to record data only during orbit night. The real-time data may be received by any properly equipped (passive) local stations as the satellite transmits within contact range of these stations; the data transmitted during the day is interleaved with the APT data as in the normal mode described above. The timing of programmer outputs is the same as in Mode 1, except for the following:

1. At count T_0 minus 1, all "SRR record" levels become absent.
2. At count T_0, if neither SSR Selected command is being provided by the CDU, the "use SRR" levels toggle and are therefore generated for the SRR (1 or 2) which was unused immediately prior to time T_0. If an SRR Selected command is being provided by the CDU, no toggling of the "use SRR" levels takes place. These "use SRR" levels (1 or 2) remain as originally established at T_0 for the duration of the orbit unless the opposite SRR Selected command is received from the CDU. Alternating the CDU commands will cause continual switching of the "use SRR" signal between side 1 and side 2.
3. At T_0 plus 400 counts, an "SR power on" pulse (remote-night pulse) is generated. Also at this time, the programmer generates the "SRR record" level (1 or 2) corresponding to the "use SRR" signal which is present.

(3) MODES 1 OR 2 WITH ALTERED TIMING

If the APT camera selected signal from the CDU is <u>not</u> present, alterations in the timing of the SR real-time day coverage will occur in Modes 1 and 2. Operation in these modes, as described above, assumes this signal to be present.

It if is not present, the timing of sensor outputs in Mode 1 or Mode 2 will be as described above, respectively, except for the following:

1. If no "APT prepare" pulses are inhibited by stored rephasing word data, as described in paragraph 2.IV.E.1.b.(2), then the "SR modulator day enable" signal will be present throughout the day portion of the orbit. That is, the signal will be initiated at count T_0 minus 1 and terminated at count T_0 plus 433.

2. If "APT prepare" pulses are inhibited by stored rephasing word data as described in paragraph 2.IV.E.1.b.(2), the "SR modulator day enable" signal will be absent from particular segments of the day portion of the orbit corresponding to the particular "APT prepare" pulse which is inhibited. In particular, if the "APT prepare" pulse occurring at 8 counts plus 0.25 second is inhibited, then the "SR modulator day enable" signal will not be generated from count T_0 minus 1 to 8 counts plus 0.25 second nor from 408 counts plus 0.25 second to count 433. If any of the other "APT prepare" pulses occurring 40N plus 8 counts plus 0.25 second (with N = 1, 2, ... 10) are inhibited, then the "SR modulator day enable" signal will not be generated from 40(N-1) plus 8 counts plus 0.25 second to 40N plus 8 counts plus 0.25 second.

Figure 2-IV-17 is a timing diagram showing the sequencing of the "SR modulator day enable" output under arbitrary conditions of APT picture deletion and time of loading. Timing is shown for both the case of the APT camera selected signal being present, and the case of its being absent.

(4) MODE 3

In the next alternative mode of operation, Mode 3, the SR subsystem is commanded (by not supplying the "enable real-time day coverage" signal from the CDU and inserting a data "1" in bit position 15 of the rephasing word) to provide real-time coverage during orbit night only, and to record the data during both the day and night portions of the orbit. The timing of sensor outputs are the same as in Mode 1 except that no "SR modulator day enable" signals are generated at any time.

(5) MODE 4

In another alternative mode of operation, Mode 4, the SR subsystem is commanded (by not supplying the "enable real-time day coverage" signal from the

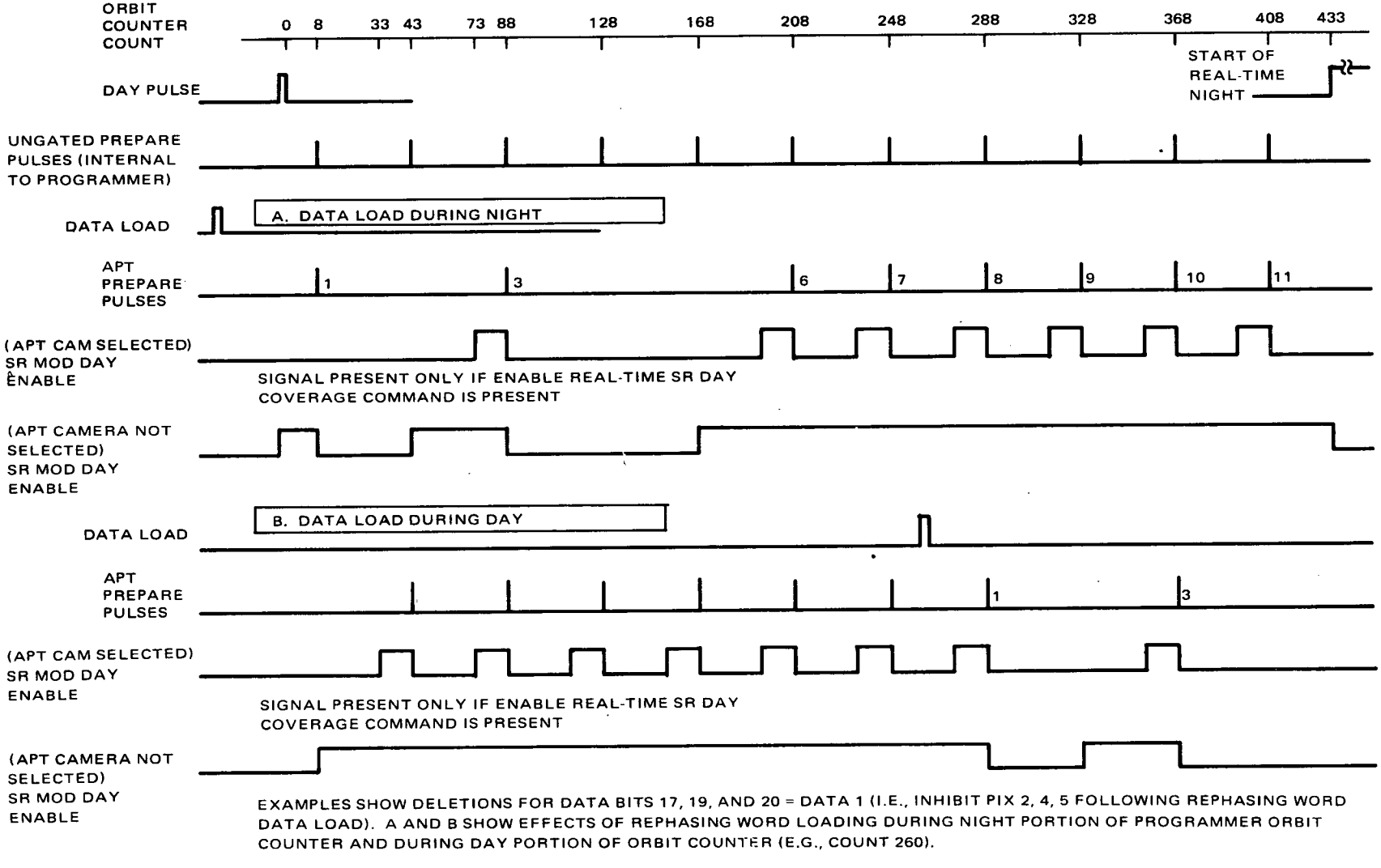


Figure 2-IV-17. APT Picture/SR Modulator Day Enable Signal Delections Via Bits 16 through 26 of Picture Program Rephasing Word, Timing Diagram

CDU and inserting a data "0" in bit position 15 of the rephasing word) to provide real-time coverage, and to record the data during the night portion of the orbit only. The timing of sensor outputs are the same as in Mode 1, except for the following:

1. No "SR modulator day enable" signals are generated at any time.
2. At count T_0 minus 1, the "SR power off" pulse is generated; the pulse width is 6.5 seconds. In addition, at this time, all "SRR record" levels become absent.
3. At time T_0, if neither Selected command is being provided by the CDU, the "use SRR" levels toggle and are therefore generated for the SRR Selected command is being provided by the CDU, no toggling of the "use SRR" levels takes place. These "use SRR" levels (1 or 2) will remain, as originally established at T_0, for the duration of the orbit unless the opposite SRR Selected command is received from the CDU. Alternating the CDU commands will cause continual switching of the SRR chosen for recording.
4. At T_0 plus 400 counts, an "SR power on" pulse (remote-night pulse) is generated. Also at this time, the programmer generates the "SRR record" level (1 or 2) corresponding to the "use SRR" signal which is present.

b. QOMAC CONTROL

After a Load QOMAC Program command has been received and the associated 28 bits of program data have been stored, the QOMAC sequence logic enters a count mode. Clock pulses, which the programmer derives by dividing a 4-Hz TBU signal by four, drive the QOMAC quarter-orbit counter which, initially, contains data bits 5 through 14 of the program. The first clock pulse to be counted occurs from 4 to 4.3 seconds after the trailing edge of the 28th data bit. When a number of clock pulses equal to the 2's complement of bits 5 through 14 has been counted, the counter overflows. The time of overflow is referred to as QT_0. The delay time until QT_0 can be from 1 to 1024 counts (in 4-second increments). At QT_0 the counter resets and begins to count the quarter-orbit time in 4-second increments.

If data bit 4 in the program is a data "0", the program is a normal QOMAC program. At QT_0, the QOMAC "ODD" output is initiated. Counting then continues until count QT_0 plus 256; at that time, data bits 22 through 28 are transferred from the storage register into the first 7 stages of the counter. These bits represent a correction factor and cause the first 9 stages of the counter to overflow after the programmed time interval of the corrected quarter orbit. Quarter-orbit times, from 385 to 512 counts (in 4-second increments), may be programmed. When overflow occurs, the QOMAC "ODD" signal is terminated and the QOMAC "EVEN" signal is initiated. Counting continues until count 256 is again reached, at which time the correction factor is again transferred to the counter.

When the next overflow of the first 9 counter stages occurs, signifying completion of the second quarter orbit, stage 10 of the counter overflows again. At this time the QOMAC "EVEN" signal is terminated, completing one QOMAC cycle. A 3-stage counter, initially containing the programmed number of QOMAC cycles in 2's complement form, is advanced each time one cycle is completed. The QOMAC cycle is repeated, as described above, until the cycle counter overflows (a maximum of eight cycles may be performed), indicating the completion of the programmed number of cycles. At this time, the QOMAC sequencer enters a standby mode and no further QOMAC output signals are generated until another QOMAC program is received.

c. PROPORTIONAL QOMAC CONTROL

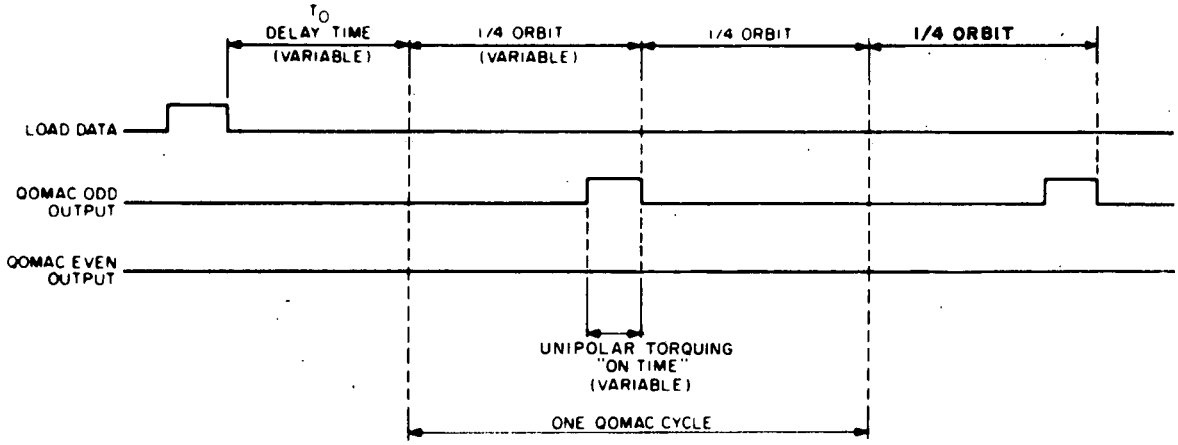
If data bit 4 in the load QOMAC program ia a data "1", the program is a proportional QOMAC program. Counting operations proceed as for a normal QOMAC program, except that no output signal is initiated until a programmed time after T_0 plus 256. Immediately after the QT_0 plus 256 transfer of data bits 22 through 28 into the first 7 stages of the quarter-orbit counter, the contents of stages 3 through 9 of the counter are compared with bits 15 through 21, which are stored in a separate register. When these numbers are equal, the QOMAC "ODD" output is initiated. Counting and quarter-orbit correction continues as in a normal program until a quarter orbit is completed. At that time, the QOMAC "ODD" output is terminated. Counting continues until a second quarter orbit is completed, but no QOMAC outputs are generated during this interval. The proportional QOMAC cycle, like the normal QOMAC cycle, is complete at the end of the second quarter orbit, even though no QOMAC outputs occur during the second quarter orbit. The same sequence of events as described above is reinitiated at each quarter-orbit overflow of the counter.

The QOMAC cycle counter is inhibited in the proportional QOMAC mode of operation, functioning only as a storage register for bits 1, 2, and 3. If bits 1, 2, and 3 are all data "1's" (in addition to bit 4), the QOMAC sequencer assumes a standby mode and does not generate QOMAC output signals. In the proportional QOMAC mode, the "on" time for the QOMAC "ODD" output is programmable in 16-second increments; however, it is limited to a maximum time equal to the true quarter-orbit time minus 1024 seconds. The proportional QOMAC cycle is illustrated in Figure 2-IV-18.

F. DUAL TIME BASE UNIT (TBU)

1. General Description

The dual time base unit (TBU), Figure 2-IV-22, consists of two identical redundant sections (TBU No. 1 and TBU No. 2), each section containing two subunits (a time base generator and a time code generator) which provide the



OPERATIONAL LIMITS

VARIABLE	TIME DURATION	COUNTS	TIME INCREMENT (SECONDS)
T_0 DELAY	4 SECONDS TO 68 MIN 16 SECONDS	1 TO 1024	4
1/4 ORBIT TIME	25 MIN 40 SECONDS TO 34 MIN 8 SECONDS	385 TO 512	4
"ON TIME"	16 SECONDS TO 1/4 ORBIT TIME MINUS 1024 SECONDS	1 TO ~ 41	16

Figure 2-IV-18. Unipolar Torquing Cycle

synchronizing and timekeeping functions for all other spacecraft subsystem operations. Two ground commands are provided which turn on one TBU section while turning off the other by power switching.

The time base generator section of each TBU generates the timing signals for synchronizing and coordinating all timing function aboard the spacecraft. All of the timing signals required by the various sensors, programmers, secondary equipment, and telemetry circuits originate within the time base generator section of the TBU. Each time base generator consists of a high-stability crystal oscillator, a DC-to-DC converter, digital integrated circuits, and input/output interface circuits. The crystal oscillator provides a stable-frequency signal which, in turn, is used as the basic clock pulse. The clock pulse is then counted down by means of an appropriate number of counters, using integrated circuit flip-flops, to obtain the desired frequency signals. The signals are then sent through output buffers (output interface circuits) to the corresponding spacecraft subsystems.

The time code generator section of the TBU generates and updates a serial stream, resettable, 24-bit time code every 0.25 second, yielding a total time capacity of 48 days, 13, hours, 5 minutes, and 4 seconds. The time code generator consists of a 24-bit shift register and an "add 1" feedback circuit. For every readout cycle, the serial data (consisting of 24 binary bits) is shifted out of the register, processed through the "add 1" feedback circuit, and shifted back again into the register; a binary "1" is thus added to the previous count during each readout cycle. When a power turn-on command is received, the time code generator is reset to provide the time code data for count "0". After one readout cycle, the count advances to "1", then "2", and so forth. Updating of the stored count continues to the maximum count condition; following this condition, the count in the shift register is reset to "0" and the entire operation is repeated.

a. TBU CIRCUITS

High-reliability integrated flip-flops and gates were chosen for the digital logic circuits because of their high reliability, low power consumption, and low volume and weight. The types of integrated circuits used are flip-flops and NAND gates. Integrated circuits were chosen for maximum fan-out capability and high noise immunity.

Two Fairchild μL 930 integrated circuit modules, with high fan-out capability, are used directly following the crystal oscillator in the time base generator. Each module drives a countdown branch consisting of several Johnson counters, using Fairchild μL 9040 DTL clocked flip-flops; those counters which operate at frequencies higher than 300 kHz use high speed DTL clocked flip-flops (Fairchild μL 931). NAND gates are employed to invert waveforms or to form different duty cycle signals. The following 90-series logic gates are used throughout the time base unit: 9041, 9044, 9046, 9047 and 930 DTL gates. Choices of specific gates were made after considering fan-in and fan-out requirements.

The choice of the Fairchild 90-series gates and flip-flops was based on comparisons of (1) logic capability, (2) fan-out capability, (3) noise immunity, (4) power consumption, (5) speed, (6) reliability data available, (7) cost, and (8) signal transition times. The decision to use the Johnson counter circuit also influenced the choice of the Fairchild flip-flop, since it is suitable for synchronous operation.

b. COUNTING TECHNIQUE

Single-change counters (called Johnson counters) are used in the time base unit for the countdown circuits; each counter uses high reliability Fairchild clocked DTL flip-flops. Each stage of the Johnson counter is triggered by a common clock pulse which synchronizes the circuit timing. The Johnson counter, with only one

flip-flop changing state at a time, provides a more stable output frequency and a less variable output waveform than other circuits in which more than one flip-flop changes state at a time.

The waveforms of each stage of the Johnson counter are, in general, of the same wave shape but of different phase. With this characteristic, the Johnson counter offers an easy and economical means of forming signals with different duty cycles by gating several waveforms derived from different stages of the counters.

c. REDUNDANCY

Two identical TBU sections are packaged in the time base unit. The output buffer gate circuits are redundantly OR'ed so that the failure of a single buffer gate will not cause the loss of a timing signal. With a standard buffer circuit, each OR gate combines the signals from both sections of the time base unit and provides two output signals, one to each side of the redundant spacecraft subsystems.

d. SPECIAL REQUIREMENTS

A high-stability oscillator was required for the time base unit to generate a stable clock pulse for use in the time base generator. A 2.4-MHz crystal oscillator with a 24-hour short term stability of ±0.0002 percent and a 1-year long term stability of ±0.0006 percent was selected for this function.

A special 300-kHz MUX signal is generated to meet the requirements of the dual multiplexer. This signal is a square wave with a second harmonic content 10 dB or greater below the fundamental, and a 2.5 ±0.5 volt (peak-to-peak) fundamental component measured across the nominal 620-ohm load resistance. To minimize distortion of this output signal, due to capacitance of the shielded lines, the source impedance of the unit was designed to be nominally 50 ohms.

The power reset circuit gemerates a reset signal to clear the time code generator, assuring an all "0" time code each time the command input signal is applied to this circuit. The "real-time transmitter off" signal is normally generated 48.5 days after the TBG section of the unit has been turned on. However, by applying the "time code lock" signal to the TBU before power is commanded on, the "real-time transmitter off" signal can be obtained for test purposes.

2. Functional Operation

a. INPUT SIGNALS

Operation of the TBU sections is controlled by two command signals from the command distribution unit (CDU). There signals cause power to be applied to one section and, simultaneously, to be removed from the other. The command signal input terminal voltage is -21 ±3 volts, capable of supplying a minimum of 66 milliamperes, to turn on one of the two TBU sections. The two input signals (see Figure 2-IV-19) which command the power operation of the time base unit are listed below.

1. The TBU No. 1 ON, TBU No. 2 OFF command signal causes power to be applied to TBU section No. 1 and to be removed from TBU section No. 2. This input also generates a RESET signal to reset time code generator No. 1, whether or not power has been previously applied.
2. Conversely, the TBU No. 2 ON, TBU No. 1 OFF command signal causes power to be applied to TBU section No. 2 and to be removed from TBU section No. 1. This input also generates a RESET signal to reset time code generator No. 2, whether or not power has been previously applied.

A third input to the TBU is a "lock time code generator" signal. This input, a -24 ±1-volt signal level, is used only during diagnostic testing of the time code generator before launch. Application of this input signal produces a special time-code output for test purposes.

b. OUTPUT SIGNALS

The time base unit generates and supplies the timing signals shown in the signal interface and timing diagrams, Figures 2-IV-19 and 2-IV-20, respectively. Except for those signals used in the data format converter (DFC) subsystem, out put signals are buffered by mini-module output buffers connected in a "standard" manner. From each output signal supplied by an activated time base section to a "standard" buffer, two identical output signals are provided, one signal for each of the redundant circuits of the subsystem being supplied. The only signals provided from nonstandard mini-module output buffers are the 300-kHz MUX and the time code data outputs. These signals are provided as single outputs through separate nonstandard buffers in each of the redundant time base sections.

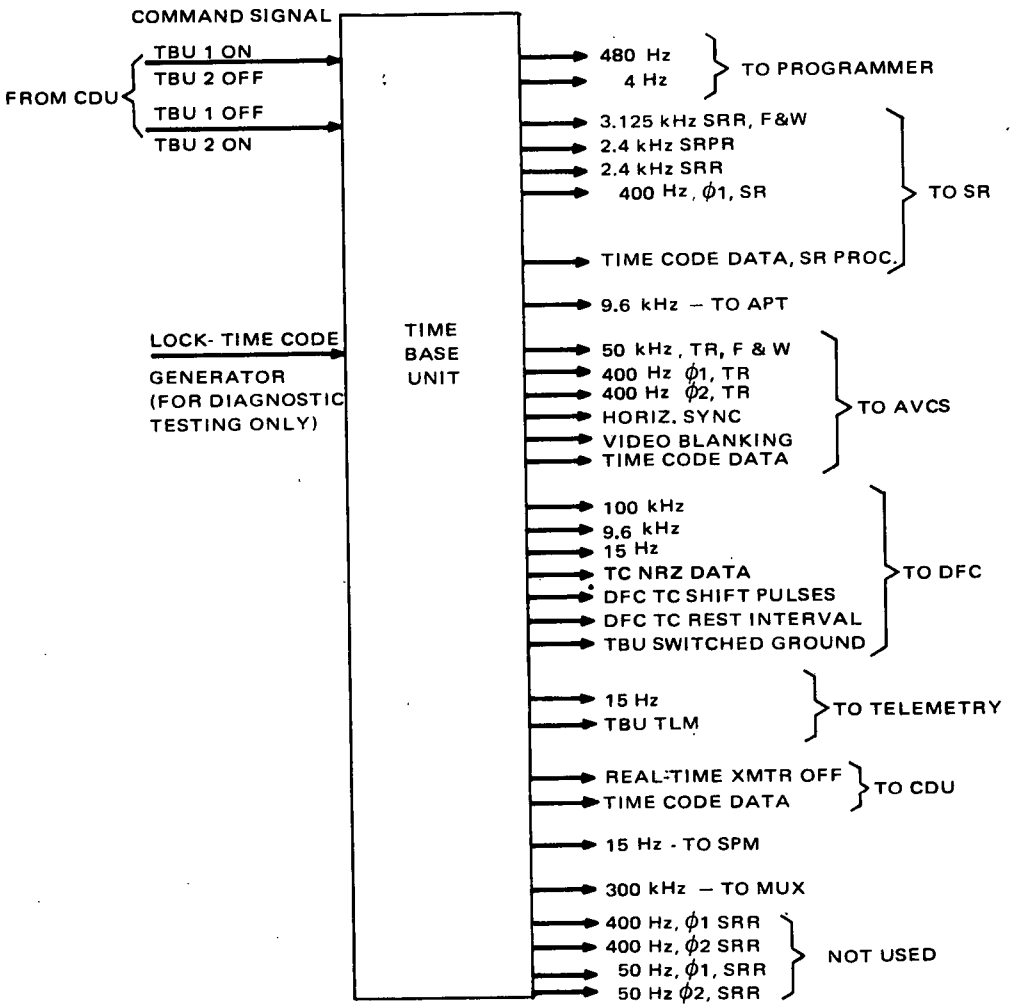
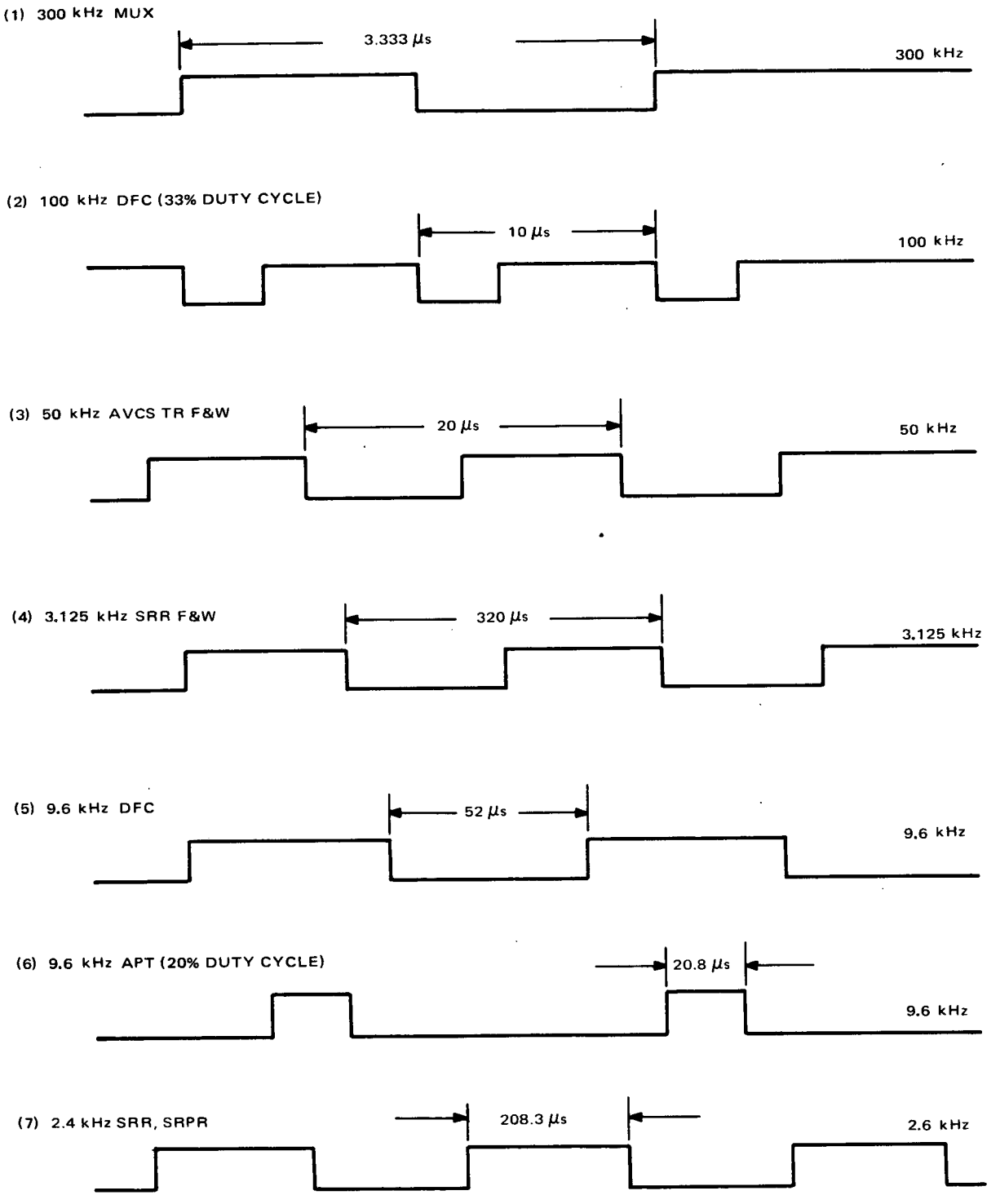


Figure 2-IV-19. Time Base Unit Signal Interface Diagram

c. POWER CONTROL AND CONVERSION

Refer to Figure 2-IV-21, the block diagram of each redundant TBU. The detail logic diagram for the dual TBU is RCA Dwg. No. 1976083, which is provided in a separate manual.*

* RCA Corporation, Astro-Electronics Division, TIROS M/ITOS Spacecraft Logic Diagrams, AED M-2175, Contract NAS5-10306, Princeton, N.J., June 15, 1969.



NOTES:
1. THE TIMING RELATIONSHIPS AMONG THE VARIOUS WAVEFORMS ARE NOT SHOWN, EXCEPT WITHIN BRACES.
2. UNLESS OTHERWISE INDICATED, ALL SIGNAL OUTPUTS ARE SQUARE WAVES.

Figure 2-IV-20. TBU Output Signals Timing Diagram (Sheet 1 of 2)

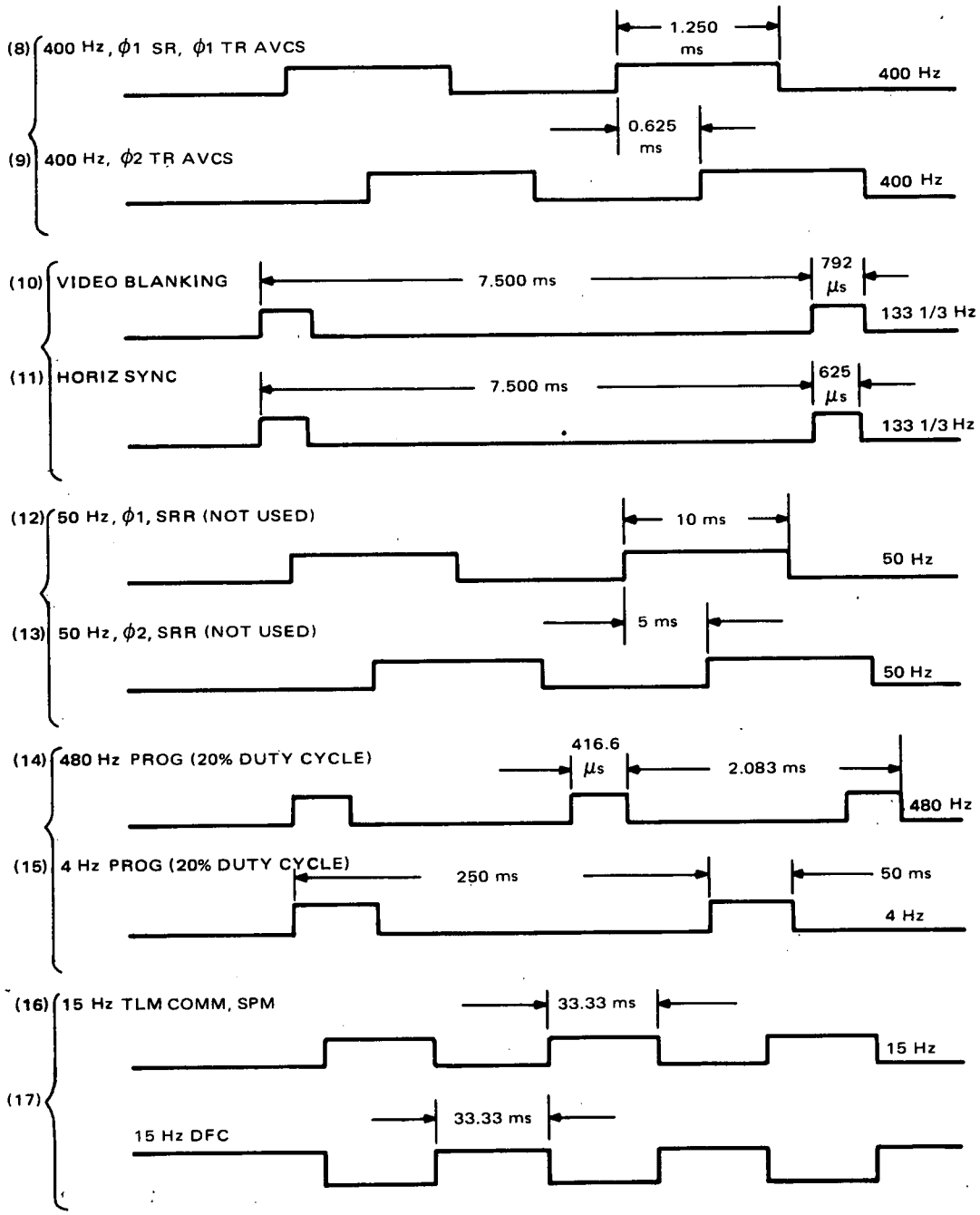


Figure 2-IV-20. TBU Output Signals Timing Diagram (Sheet 2 of 2)

Each section of the TBU derives its power from a DC-to-DC converter which supplies +5 volts for operation of the internal digital logic integrated circuits and +5.35 volts for the buffer interface circuits. Power is derived from the -24.5-volt DC regulated bus and is selected by the command input signal. Power switching is accomplished by two latching relays. These relays control the input power to one of the DC-to-DC converters, in response to the command signal being applied to the particular section. The TBU section which is commanded "OFF" has the input to its DC-to-DC converter disconnected from the input power bus.

d. TIME BASE GENERATOR (TBG)

The time base generator consists of a 2.4-MHz crystal oscillator and a number of countdown circuits (Johnson counters) as required to obtain the desired output frequencies. For example, the 2.4-MHz signal is counted down by a "divide by 4" counter and then by a "divide by 2" counter to obtain the 300-kHz signal required by the dual multiplexer (MUX) subsystem. Other output signals are derived similarly. Different phases with the same frequency are obtained, in general, by choosing outputs from different stages of a counter; a different duty cycle is achieved by gating several waveforms of the same or different counters. Output signals, except those which are used by the data format converter (DFC), are buffered by standardized mini-module output buffers. The standard buffers also OR the signals derived from both TBU sections.

e. TIME CODE GENERATOR (TCG)

The time code generator consists of a 24-bit time code shift register, an "add 1" feedback circuit, a reset circuit, an NRZ/RZ converter, a "real-time transmitter off" decoder, a time code lock input buffer, and several countdown circuits. Reception of the Time Base Unit 1 ON, Not 2 (or 2 ON, Not 1) command will cause a reset circuit to force the appropriate time code shift register to an all "0" time code. The time code is an NRZ 24-bit serial data stream; it is provided by a 24-bit shift register, and an "add 1" feedback circuit consisting of a flip-flop and three logic gates. Both the shift register and the "add 1" feedback circuit flip-flop are clocked by the same pulse train (time code shift pulses) to assure synchronous operation. Each shift pulse causes the information in a stage to be shifted to the succeeding stage. As the data is shifted out, it is recirculated through the "add 1" circuit and fed back into the shift register. Each time this occurs, a 24-bit output is presented serially in NRZ form at the last stage of the shift register.

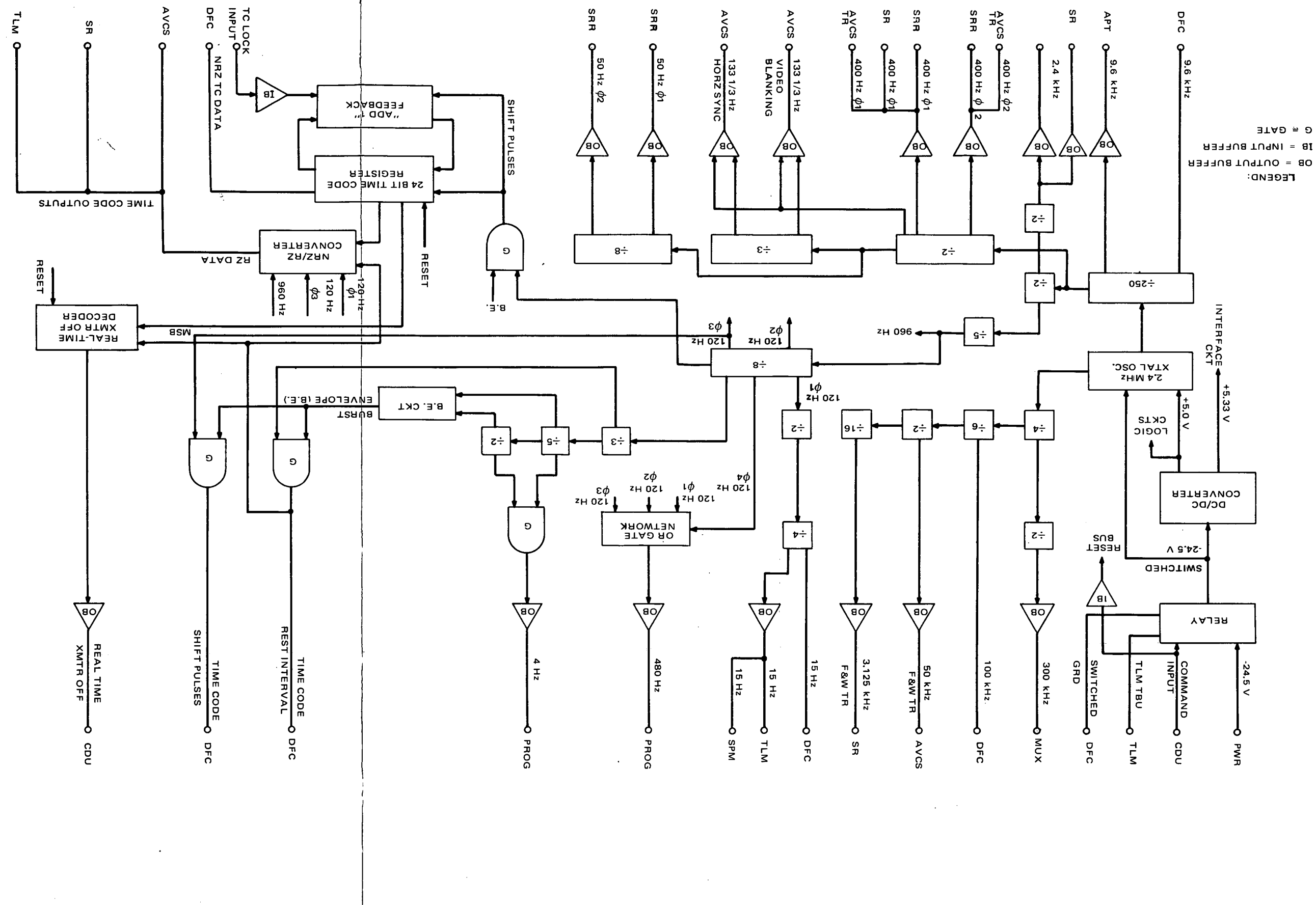


Figure 2-IV-21. TBU Block Diagram

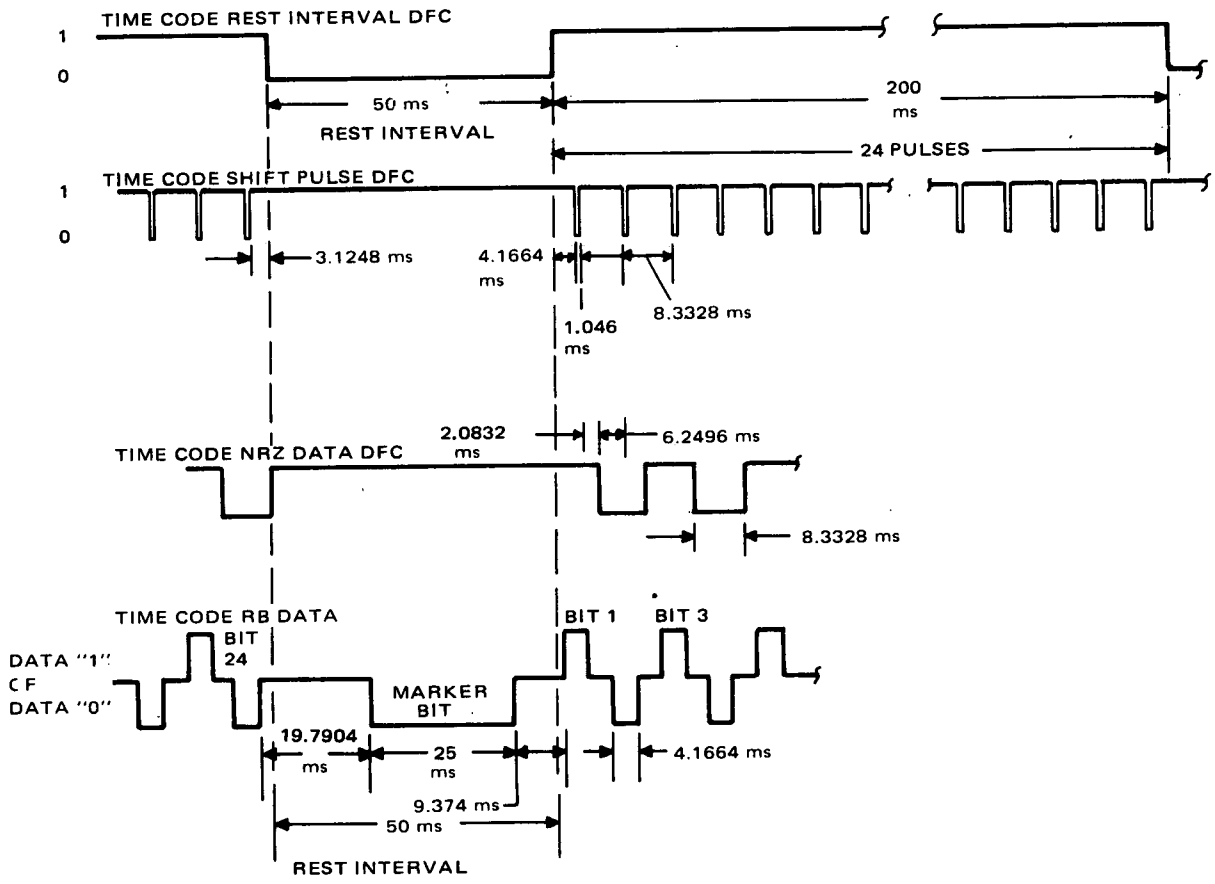


Figure 2-IV-22. TCG Signal Characteristics

The NRZ/RZ buffer-converter, changes the nonreturn-to-zero (NRZ) data from the shift register to the return-to-bias (RB) output format. In this format, -0.5 volt denotes data "1", -2.5 ± 0.8 volts denotes "absense of data", and -4.5 ± 0.8 volts denotes data "0". This RB data is provided to the SR, AVCS, and TLM subsystems; the DFC is provided with time code data in NRZ format.

The "real-time transmitter off" decoder consists of two flip-flops which are strobed once after each updating of the time code data. The decoder senses the state of the most significant bit (MSB) contained in the time code shift register. After approximately 48.5 days of continuously applied power to a time base unit, both the flip-flops will be in the data "1" state. This causes an output pulse with 0.25-second duration to be generated; this pulse is used to turn off the real-time transmitter if one is on at this time.

The time code lock input buffer provides a time code lock signal when it receives a -24.5-volt input. This signal is applied only during diagnostic testing of the time code generator prior to spacecraft launch. It causes the "add 1" circuit to alternately fill the time code shift register with all data "1" and all data "0" counts.

The waveforms of some TCG signals are shown in Figure 2-IV-22. The time code rest interval is generated every 0.25 second, for a duration of 50 milliseconds. The remaining 200 milliseconds of this signal's period defines the burst envelope time. The burst envelope is used as a gate to enable only 24 clock pulses from a 120-pps train to be provided to the time code shift register, once every quarter second. A similar burst of 24 pulses is also provided to the DFC during the burst envelope time. These clock pulses are used by the DFC to clock the NRZ data, which is also provided by the TBU. The characteristics of the RZ data from the TBU are also shown in Figure 2-IV-22. The 120-Hz phase 2 and phase 3 signals are used in the NRZ/RZ converter to establish the pulse width of the RZ data.

SECTION V

PRIMARY ENVIRONMENTAL SENSOR SUBSYSTEMS

A. INTRODUCTION

The primary environmental sensing functions of the spacecraft are performed by three sensor subsystems, which provide full orbital coverage (both day and night) of earth cloud cover, including real-time readout of local weather pictures to APT ground stations. The subsystems and the equipment in each subsystem are as follows:

- A redundant advanced vidicon camera subsystem (AVCS), each side of which is composed of a camera sensor assembly, a camera electronics unit, and a three-channel magnetic tape recorder. Each tape recorder includes a tape transport assembly and recorder electronics for recording and playing back the television data generated by the camera sensors.
- A redundant automatic picture transmission (APT) subsystem, each side of which is composed of a camera sensor assembly and a camera electronics unit.
- A redundant scanning radiometer (SR) subsystem, each side of which is composed of scanning radiometer and electronics, an SR processor, and a three-channel tape recorder and electronics. The two SR processors are packaged as a single unit.

Power and signal switching circuits, controlled by ground command, provide the means for selecting one of the redundant sides of a sensor subsystem for operation. For AVCS, the switching arrangement is such that it is possible to select either of the two cameras for operation with either of the two tape recorders. A similar switching arrangement provides comparable flexibility in the selection of a radiometer and tape recorder for operation in the SR subsystem.

To meet the mission requirements, one AVCS camera and one AVCS tape recorder obtain and store cloud cover pictures from the daylight portion of the orbit. Concurrently, in the primary mission mode, one of the two APT subsystems provides daytime cloud cover pictures for real-time transmission to local users. During the nighttime portion of the orbit, one scanning radiometer and one tape recorder are in operation to measure and record infrared data for subsequent playback. The SR subsystem also transmits infrared data in real time to provide nighttime radiance data to APT stations. Secondary modes of operation permit either visible or infrared SR data transmission to be substituted

for APT subsystem operations and also provide for continuous (day and night) recording of the SR signals for subsequent playback.

SR data and AVCS pictures stored on the spacecraft tape recorders are played back and transmitted to the ground upon command by a CDA station, from which they are relayed over a microwave link to ESSA facilities for meteorological analysis.

B. ADVANCED VIDICON CAMERA SUBSYSTEM (AVCS)

1. General Description

The AVCS (Figure 2-V-1) is used to take a series of wide-angle, high resolution television pictures of the earth and its cloud cover, to store these pictures on one of two satellite-borne tape recorders, and, on command, to play them back for transmission to a CDA station. Picture-taking operations of the AVCS are controlled by a program of instructions that is prepared by TOC and transmitted to the satellite by a CDA station. This program is stored and processed by the active programmer in the satellite's command subsystem. Before each picture-taking operation, commands transmitted to the satellite select the AVCS camera and the tape recorder to be used.

In the record mode, the active programmer controls the AVCS camera for a sequence of pictures starting just after the satellite track crosses the earth's terminator into the subpoint daylight portion of the orbit. A complete picture sequence lasts approximately 48 minutes, during which 11 pictures, or frames, are taken at intervals of 260 seconds and stored on the selected tape recorder. When the last picture in the sequence is taken and recorded, the command subsystem provides a "power off" signal for the AVCS. A "power on" command and the picture-taking sequence are repeated during succeeding orbits until the active programmer is either reloaded or turned off. The repeat time is determined by the data loaded into the programmer and normally is the time of one orbital revolution. Consequently, successive picture sequences start at approximately the same latitude as the first, but are displaced in longitude by approximately 28.5 degrees at the equator; this displacement produces a slight lateral overlap at the equator in coverage. The amount of lateral overlap increases with increasing latitude. The overlap of successive pictures along the orbital track is a function of the fixed picture-taking rate and is about 50 percent.

In the playback mode, which is initiated by CDA station command, the pictures stored by the satellite's AVCS tape recorder are played back and transmitted to the CDA station.

In the direct AVCS readout mode, picture data is transmitted as it is read out of the AVCS camera to the tape recorder. This operation is terminated when

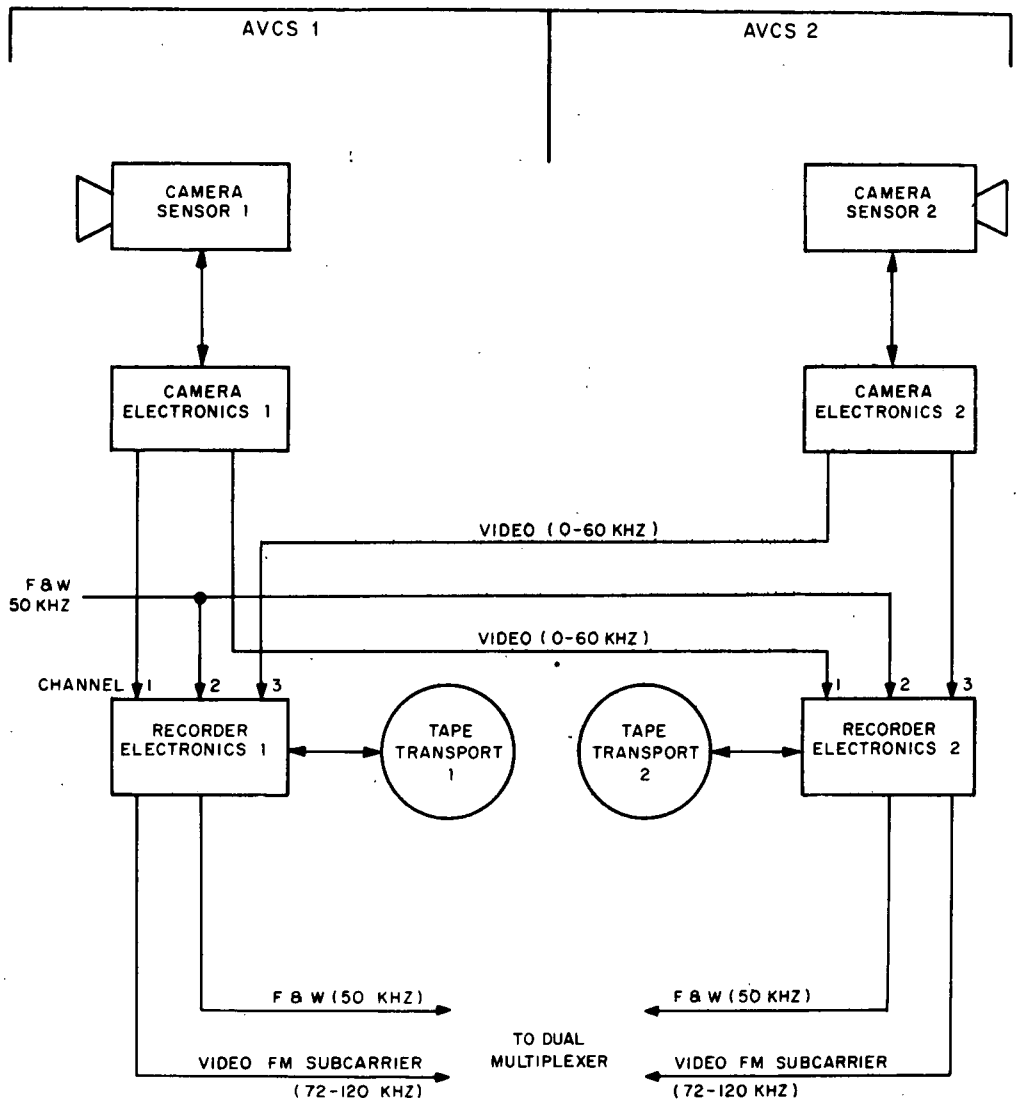


Figure 2-V-1. AVCS Subsystem, Block Diagram

the S-band transmitter is turned off (although the programmed picture sequence is not interrupted) before the satellite travels out of station communication range. The real-time picture data may be used for evaluation of camera performance and later compared with the played back picture data for assessment of tape recorder and AVCS performance.

The AVCS consists of two advanced vidicon camera chains, each composed of a camera sensor assembly, a camera electronics unit, and a three-channel magnetic tape recorder. The subsystem components are shown in Figure 2-V-2. The tape recorder comprises a tape transport assembly and recorder electronics for recording and playing back the data generated by the camera sensor.

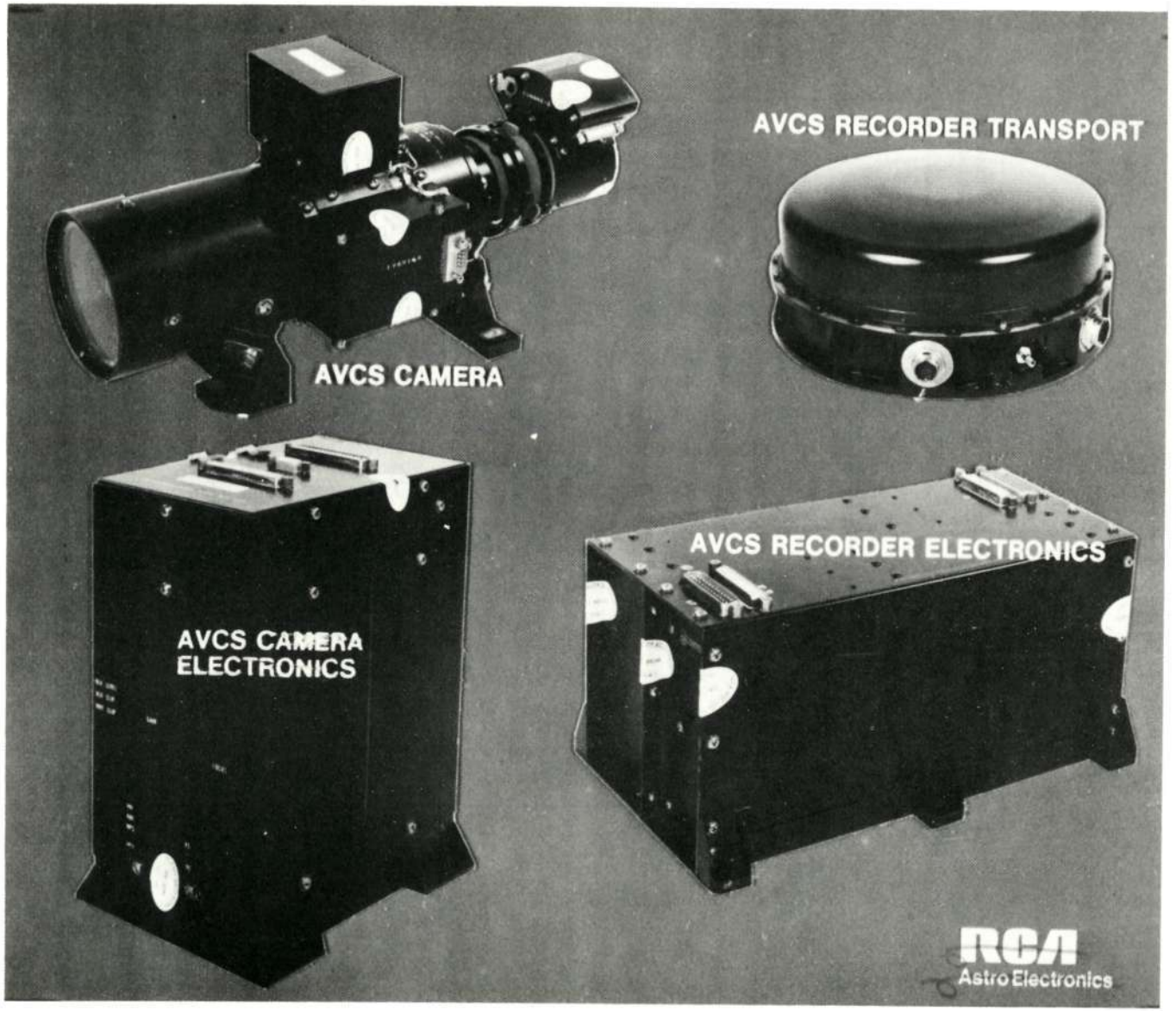


Figure 2-V-2. AVCS Components

Power and signal switching circuits, which are controlled by ground command, provide a means for selecting an AVCS camera* and tape recorder for operation. The switching arrangement is such that it is possible to select either of the two cameras for operation with either of the two tape recorders.

2. Functional Description

This portion of the discussion offers a more detailed, time-oriented, functional description of AVCS subsystem operation in the two principal modes: record and playback. During this discussion, refer to the timing diagram for AVCS operation, shown in Figure 2-V-3.

a. RECORD MODE

The first picture in a sequence is taken 45.5 seconds after the programmer alarms (overflows) at time T_0, where T_0 is the subpoint night-to-day transition-time reference in the programmer counter. For the 6.5-second interval before T_0 and for 45.5 seconds after T_0, the AVCS camera is prepared for picture-taking. At T_0 minus 6.5 seconds (refer to Figure 2-V-3), the command subsystem delivers a "standby power" signal to the camera electronics unit. This signal activates a solid-state switch that applies -24.5 volts DC to a low voltage power supply that supplies +6.3 volts DC to the vidicon filament. At T_0 the command subsystem applies a "main power" signal that activates a solid-state switch to energize the high voltage power supply and other camera circuits.

The vertical sync pulses, video blanking, and horizontal sync pulses (the latter two are not shown in Figure 2-V-3) are present whenever the time base unit is "ON". The video blanking and horizontal sync pulses recur at intervals of 7.5 milliseconds, a repetition rate of 133-1/3 pps.

The horizontal sync pulses and the 250-millisecond vertical sync pulses are used to initiate the horizontal and vertical sweeps and the vidicon blanking pulses. The use of the video blanking pulses is explained later.

With the application of high voltage, the vidicon beam is turned on and scanned completely across the image area seven consecutive times (T_0 to T_0 plus 45.5 seconds) before exposure. This scanning operation deposits a uniform charge (black level) on the vidicon photoconductor, preparatory to exposure. At the

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*In this particular context and for simplicity of expression, the term "camera" signifies the camera sensor assembly and camera electronics unit of one AVCS chain, excluding the tape recorder.

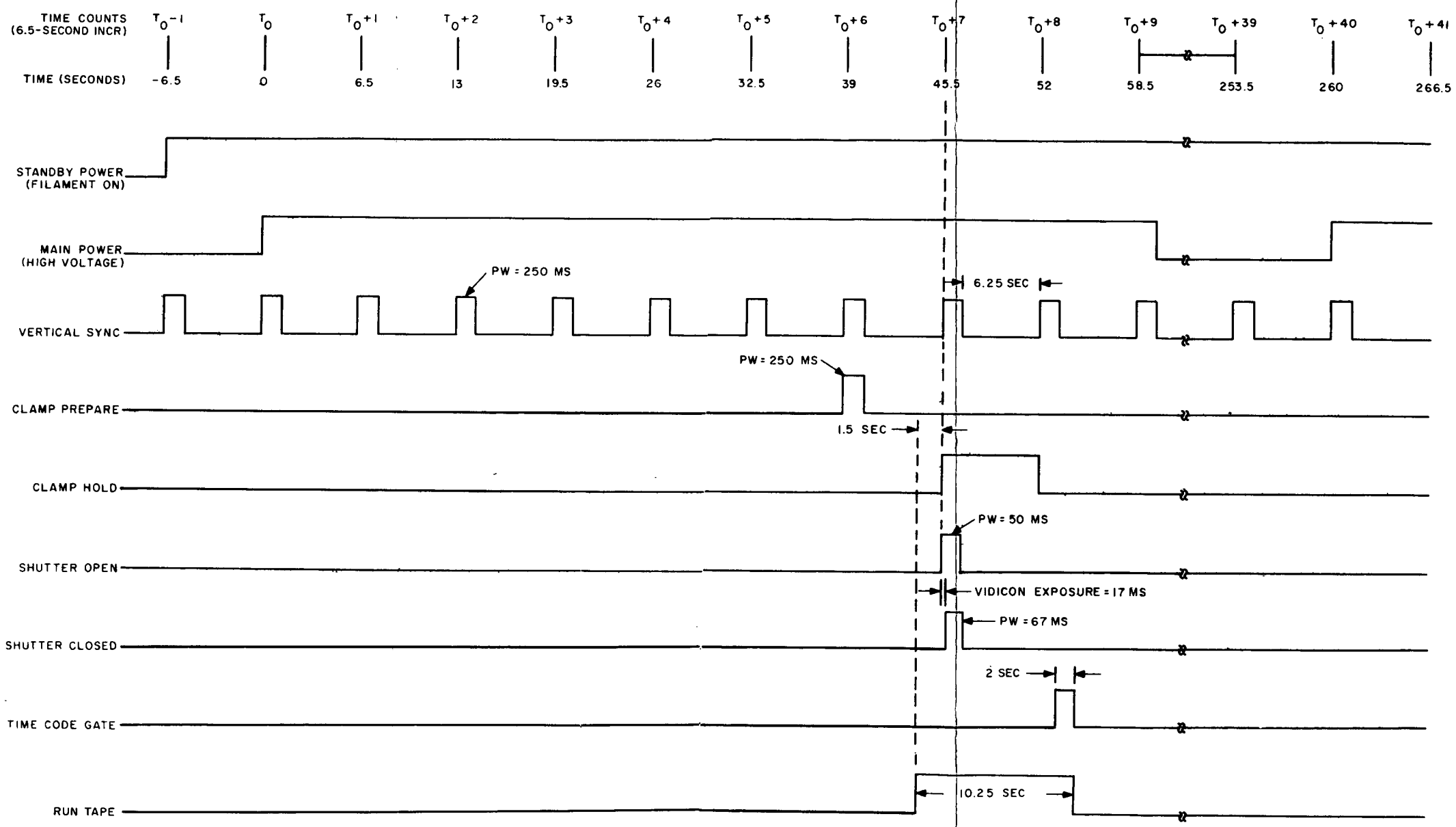
beginning of the seventh 6.5-second interval, or one frame before exposure, a "clamp prepare" pulse, coincident with the vertical sync pulse, conditions a video clamp circuit for operation. During the 6.25 seconds following the clamp prepare pulse, samples of the vidicon dark current are applied to the video clamp, which subtracts the vidicon dark current signal and establishes a DC reference for the video signal.

Optical exposure occurs at T_0 plus 45.5 seconds with the sequential application of "shutter open" and "shutter close" pulses. The delay between the leading edges of these pulses determines the exposure time, about 17 milliseconds. The shutter pulses operate a solenoid-actuated, double-bladed focal plane shutter. The shutter blades move sequentially from one side of the lens to the other as shown in Figure 2-V-4. Exposure alters the uniform charge pattern of the photoconductor by causing each resolution element to discharge in proportion to the amount of incident light.

Coincident with optical exposure, an incandescent lamp is energized and its light output is directed through a 15-step gray scale transparency (by means of a lens and prism arrangement) onto the vidicon photoconductor alongside the TV image area to serve as a reference when the TV pictures are processed at the ground facility.

Shutter actuation occurs during vertical retrace time, at the conclusion of which the horizontal and vertical scan pattern is resumed to read out the data imaged on the vidicon. As the electron beam traverses the photoconductor, it deposits a charge on the resolution elements that have been discharged by exposure to varying intensities of light. The charging currents developed during the deposition process constitute the video signal which, after preamplification in the camera sensor assembly, is delivered to the camera electronics unit. There the video signal is further amplified, the video sync and blanking pulse are inserted at the beginning of each scan line to provide a sync and back porch, and the picture time code data is added after the 250-millisecond vertical sync period following the end of video readout. (See Figure 2-V-5.) Video readout lasts 6.25 seconds. The inclusion of the time code takes an additional 2 seconds. During the interval of vertical sync the video output is at black level. No horizontal pulses appear during this interval. This signal has been changed to simplify the data processing at DAPAF.

The composite video signal and time code are applied to an FM modulator in the tape recorder electronics. The frequency deviation of the FM modulator is a linear function of the video amplitude and ranges from 72 to 120 kHz. This



FOLDOUT FRAME 1

FOLDOUT FRAME 2

Figure 2-V-3. AVCS Subsystem, Timing Diagram

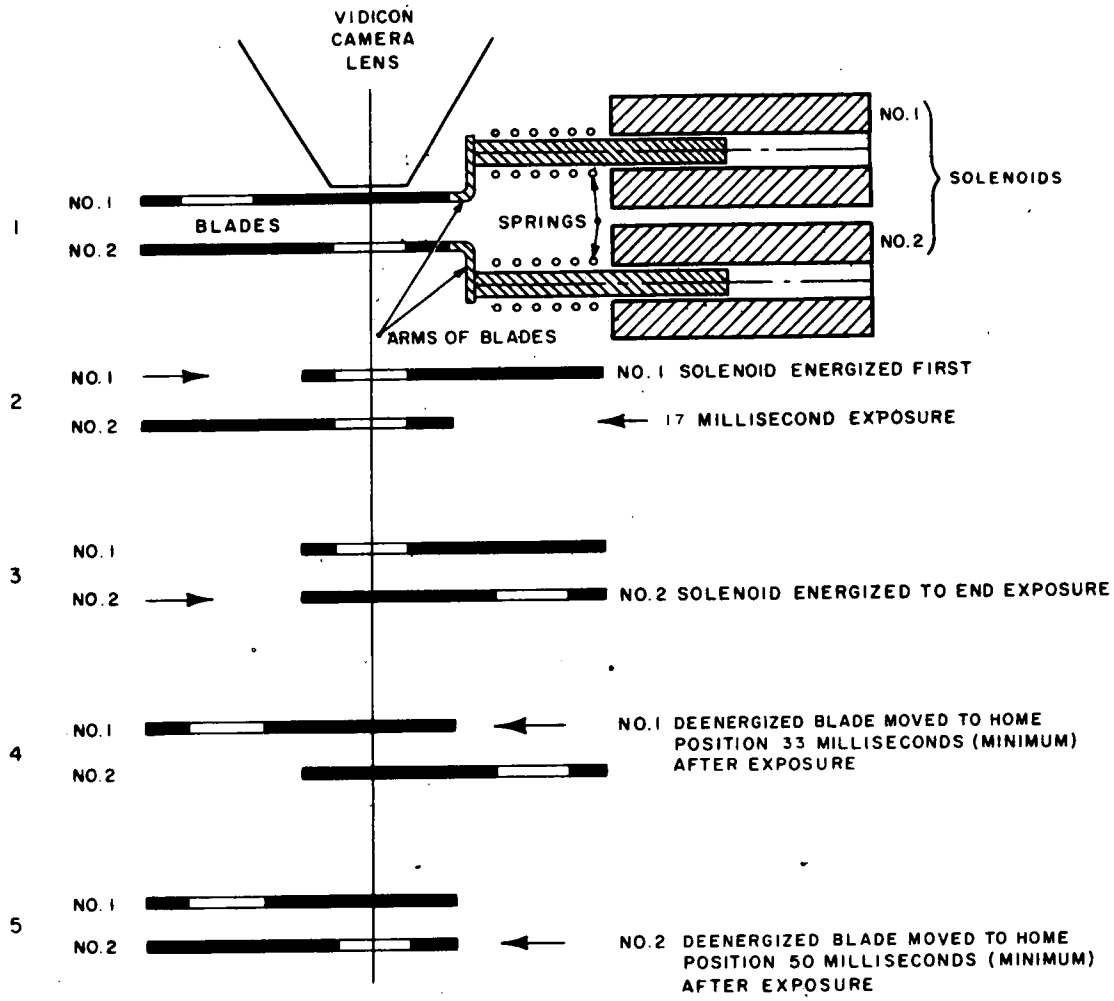


Figure 2-V-4. Operation of the Double-Bladed Focal Plane Shutter

subcarrier is applied to the record head* through an amplifier. The tape recorder drive motor is turned on 1.5 seconds before vidicon exposure to permit the motor to attain synchronous speed before data readout begins. Accordingly, at T_0 plus 44 seconds, a programmer-generated "run tape" signal is applied to a power switch that applies -24.5 volts to the record electronics and to a power amplifier whose output drives the tape recorder motor. The power amplifier is driven by a 400-Hz signal that is applied continuously from the active time base generator.

A 50-kHz signal, continuously available from the time base generator, is applied to channel 2 of the tape recorder. This signal is used by the ground data processor to correct for flutter-and-wow products of tape recorder speed variations.

*Video signals from camera 1 are applied to channel 1 of both tape recorders, and those from camera 2 are applied to channel 3 of both recorders, but only one recorder and one camera are active at any given time.

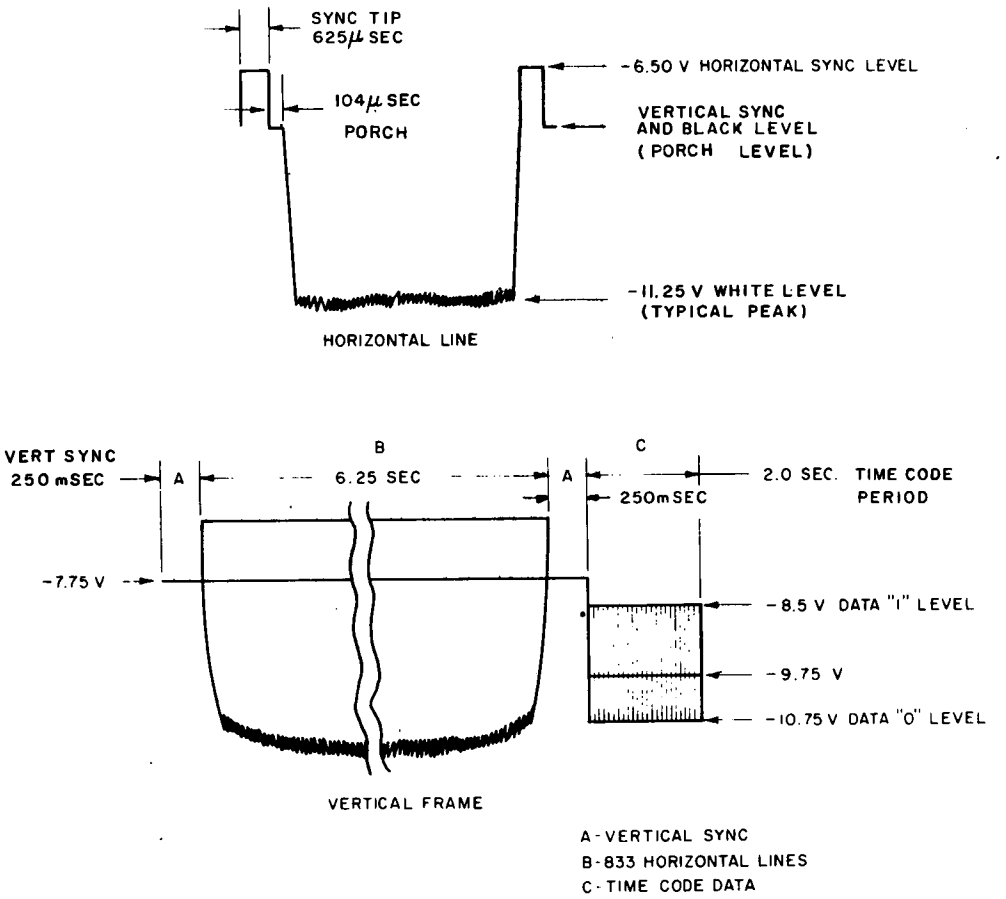


Figure 2-V-5. Composite Video Signal

The first picture-taking and recording cycle is terminated at T_0 plus 58.75 seconds by terminating the "main power" signal, but is repeated at 260-second intervals until all 11 pictures in the sequence are taken. At the end of the sequence, "standby power" is removed. The entire sequence is repeated once during each orbital revolution of the satellite, until the programmer is reloaded or turned off by ground command.

b. PLAYBACK MODE

When the satellite comes within communications range of a CDA station, playback is initiated by the transmission of a "recorder playback" command to the satellite.* In response to this command, the command subsystem delivers a signal which causes the selected recorder to perform the following functions:

- Connects operating power to the appropriate video and flutter-and-wow playback electronics of the recorder and

*A "transmitter ON" command to turn on an S-band transmitter in the playback video link is also required.

- Connects a drive voltage that causes the tape recorder motor to run in the playback direction.

During playback, the 72- to 120-kHz video signal (from channel 1 or channel 3) is preamplified and limited and applied through an output amplifier to the multiplexer. The amplified and limited 50-kHz flutter-and-wow signal from channel 2 is also fed to the multiplexer through a separate output amplifier.

When the playback end-of-tape sensor is reached, a momentary -24.5-volt "end-of-playback" signal is generated, recorder playback power is removed and the AVCS is returned to the record mode, ready for another picture-taking and recording sequence.

To play back the 11 pictures taken during a single orbit takes slightly less than 2 minutes. A minimum of three complete picture sequences can be stored on the tape recorder before commanding playback.

c. DIRECT MODE

The direct mode is activated whenever the recorder receives a Record command and a S-Band Transmitter ON command is sent to the satellite while a picture-taking sequence is in progress. Besides turning on a transmitter in the playback video link, this command introduces a "direct command" to the active tape recorder. This signal connects power to the appropriate playback electronics (but not to the playback motor drive circuits or the preamplifier) at the same time that power is being applied to the record electronics. Because of a permanent connection between the output of the record amplifier and input to the playback limiter in each channel of the tape recorder, the TV pictures and flutter-and-wow data are transmitted to the CDA station, in real time, as they are being recorded on tape.

3. AVCS Components

a. CAMERA SENSOR AND CAMERA ELECTRONICS

(1) GENERAL DESCRIPTION

The elements of the camera are shown in the block diagram in Figure 2-V-6 and in the composite photograph (Figure 2-V-7). The camera sensor contains a lens, shutter, gray scale calibrator, hybrid vidicon, deflection yoke, and preamplifier. The camera electronics assembly contains the video processing, vidicon shading correction, deflection, shutter drive, and power supply circuitry.

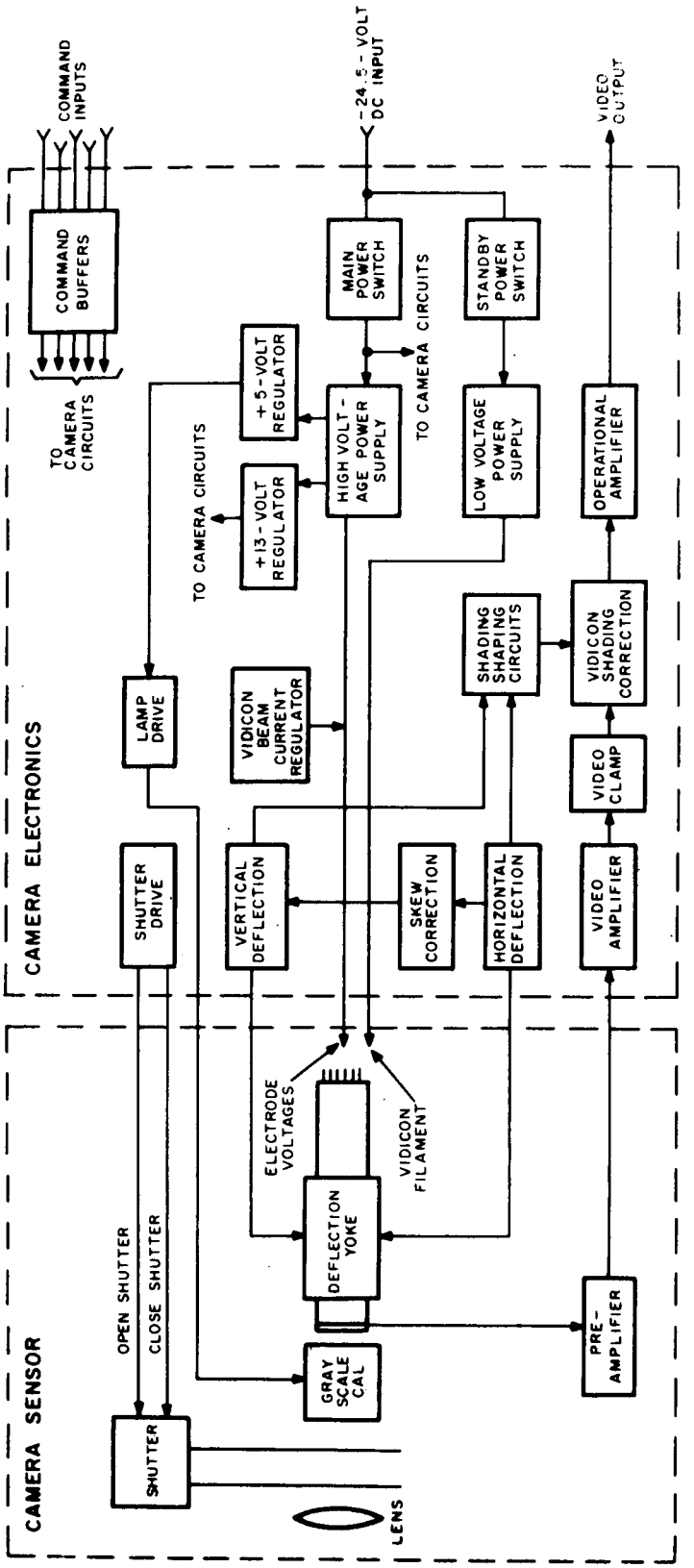


Figure 2-V-6. AVCS Camera Sensor and Electronics, Block Diagram

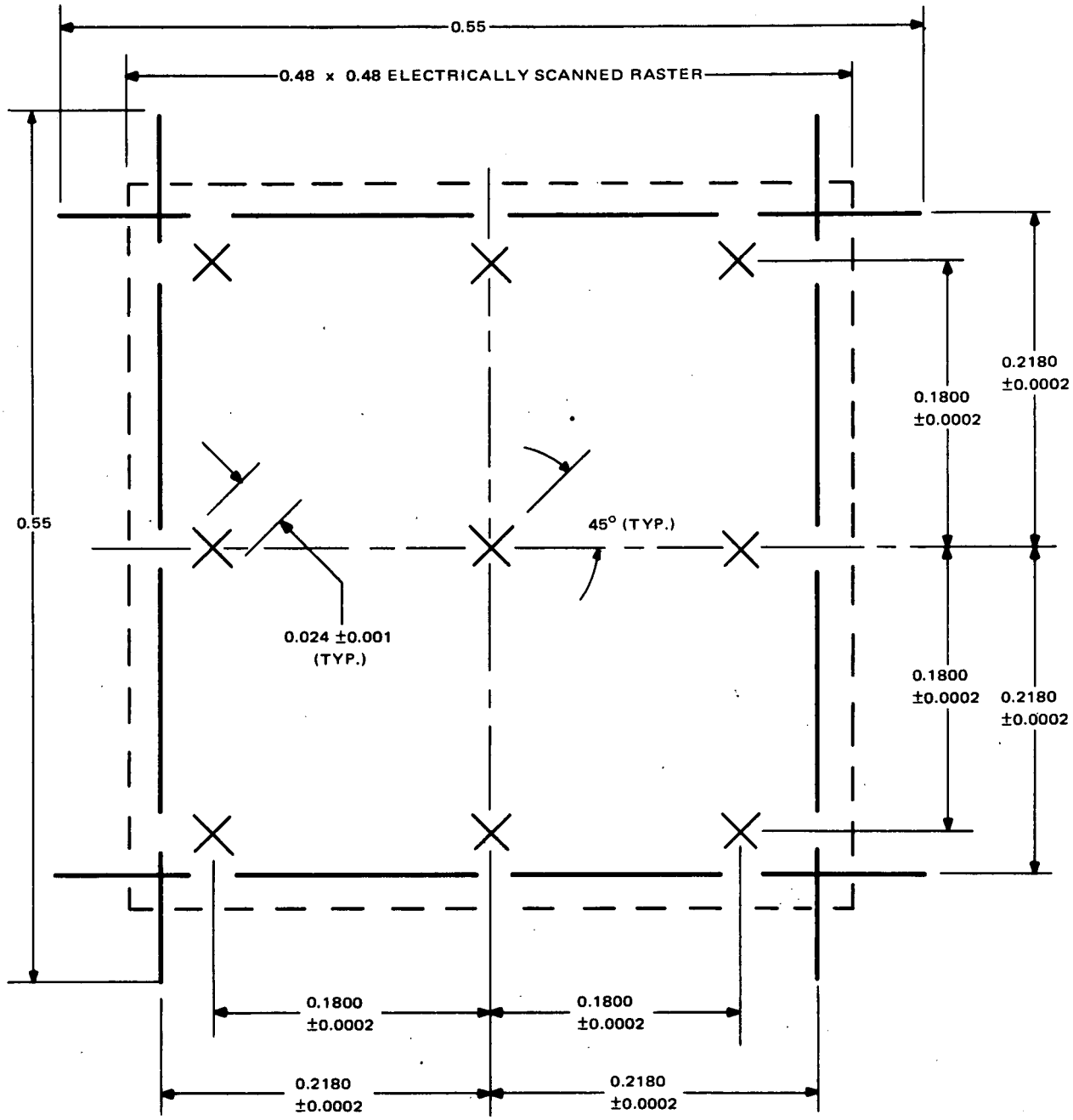


Figure 2-V-7. Vidicon Reticle Pattern

The video preamplifier within the sensor housing preamplifies and buffers the vidicon signal to ensure an adequate signal-to-noise ratio at the input to the following video amplifier stages.

Several stages of equalization are used in the video amplifier, including high frequency peaking and aperture correction, to linearly advance the phase of the video signal with increasing frequency. Low frequency video equalization and gain control are also included in the video amplifier, as well as a low pass filter that attenuates frequencies beyond the required passband.

The output of the video amplifier is applied to a video clamp that restores the DC video component and removes the video dark current signal.

A complementary emitter follower is used to buffer the video clamp and drive the vidicon shading correction circuits. The shading correction circuit is essentially a high-level balanced modulator that can vary the video gain over a 3-to-1 range without imposing the modulating signal on the video. By varying the video gain inversely as a function of the shaded video signal, vidicon and/or lens shading components are reduced.

Following the shading correction modulator, an operational amplifier combines and processes the camera output video signal. Inputs to this amplifier include vertical and horizontal base line correction (part of the shading correction signals), porch and synchronization timing signals, and time code data. This amplifier also performs both black and white level clipping. The composite video signal is then applied to an FM modulator in the tape recorder electronics.

Vertical and horizontal deflection generators supply the sawtooth signals for the vidicon deflection yoke. These signals are also applied to the shading correction circuit signal generators and to a skew correction circuit.

The shutter drive circuit provides the required drive for the mechanical double-bladed focal plane shutter. The exposure time is controlled by the application of two timing signals that are digitally derived from the spacecraft clock and delivered by the programmer. The configuration of the shutter drive circuit permits simultaneous or random sequential application of the regulated and unregulated bus voltages without any degradation to components or performance.

A vidicon beam current regulator maintains a constant vidicon cathode current, regardless of variations in vidicon parameters such as temperature, filament voltage, and filament aging.

The gray scale calibrator assembly, utilizing an incandescent lamp as a light source, provides 15 linear density steps (0.13 neutral density). The light output from the lamp source is directed through the gray scale transparency, by

a lens and prism arrangement and impressed on the vidicon photoconductor. The gray scale serves as a reference when the TV pictures are processed at the ground facility.

Minus 24.5-volt DC power is applied to a high voltage DC-to-DC converter that supplies all the vidicon electrode voltages as well as an output to a +13-volt regulator and a +5-volt regulator used by the camera electronics circuits. A low voltage DC-to-DC converter provides +6.3 volts for the vidicon filament.

The principal characteristics of the AVCS camera sensor and electronics are given in Table 2-V-1. All subsystem interface signals, with the exception of telemetry output voltages are listed and described in Table 2-V-2.

(a) AVCS Camera Sensor

As shown in Figure 2-V-5, the camera sensor assembly contains a lens assembly, a hybrid vidicon, a shutter assembly, a gray scale calibrator, and a video preamplifier. This assembly is 15.5 inches long, 7.1 inches high, 7.5 inches wide, and weighs 8.75 pounds. The form of the unit is essentially cylindrical, with a set of mounting feet attached and isolated from the main structure by means of urethane pads. The mountings and isolators are constructed so that the dynafocal principle is utilized. (The central normals pass through the center of mass of the camera assembly.) In general, high strength magnesium alloy, chemically treated with Dow 23, was used for construction. All external surfaces were sprayed with blue epoxy polymide paint.

1. AVCS Hybrid Vidicon

The vidicon converts the optical image, formed by the lens and timed by the shutter, into an electrical signal. The vidicon is a 1-inch "hybrid vidicon" which is electrostatically focused and magnetically deflected as compared to the "all magnetic" vidicon which utilizes magnetic fields for both focus and deflection. Because focusing in the hybrid vidicon is achieved by electrostatic fields, a focus coil is not required and consequently there is a considerable saving of weight and power. The vidicon photoconductor (ASOS) is capable of storing an image for 9 seconds with little degradation.

The vidicon used is capable of withstanding a maximum of 36 G's and its major resonant frequency lies between 800 and 1100 Hz. System environmental requirements call for a sine input of 10 G's from 5 to 2000 Hz. This limits the permissible Q (magnification factor) at the vidicon to 3.6 with a desired resonance below 300 Hz. The dynafocal mounting of the assembly fulfills this condition.

TABLE 2-V-1. AVCS CAMERA AND ELECTRONICS CHARACTERISTICS

Characteristic	Value
Pictures per orbit	11
Time for an 11-picture sequence	Approximately 48 minutes
Time between picture	260 seconds
Vidicon	1-inch hybrid (electrostatically focused)
Lens	f/1.8, 5.7 mm focal length
Field of view	Approximately 108 degrees across the picture diagonals; effectively 89 ±1 degrees across the picture flats.
Ground resolution	Approximately 2 nmi per scan line at picture center
Line resolution (vertical and horizontal)	Approximately 800 TV lines
Aspect ratio	1:1
Shutter	Double-bladed, focal plane
Preparation, picture-taking, and recording cycle duration	58.75 seconds
Vidicon exposure time	17 milliseconds
Vidicon readout time	6.25 seconds
Vertical sweep period	6.5 seconds
Vertical blanking and retrace	250 milliseconds
Horizontal sweep period	7.5 milliseconds per line
Horizontal lines per frame	833 (noninterlaced)
Video signal	See Figure 2-V-4
Time code:	
Number of bits in complete burst	24 return to bias
Bit rate	120 kilobits per second
Amplitude	See Figure 2-V-4

TABLE 2-V-2. AVCS CAMERA ELECTRONICS AND SPACECRAFT INTERFACE SIGNALS

Interface Signal	Description
Spacecraft Power	
-28 VDC	Unregulated. Powers the solenoids in the shutter drive circuit when the shutter drive signals described in this tabulation are present.
-24.5 VDC	This is the main power source for the AVCS. It is switched on and off by the standby-power and main-power signals described later in this tabulation.
Timing	
Standby Power	Applied one 6.5-second period before T_0. It activates a solid-state switch that applies -24.5 volts to the low voltage DC-to-DC converter whose +6.3-volt output provides the vidicon filament power. It is on for the entire 11-picture sequence.
Main Power	Applied at T_0 for 58.75 seconds and cycled on/off every 260 seconds. It activates a solid state switch which applies -24.5 volts to the high voltage DC-to-DC converter and to the remaining camera circuits.
Vertical Sync	There are 8 vertical frames during the main power interval, the next to the last frame being the video readout. The vertical sync is utilized to initiate vertical deflection sweep and retrace. This signal is also used to inhibit vidicon dark current sampling during vertical deflection retrace and provides the blanking signal for the beam current regulator.
Clamp Prepare	One vertical frame prior to the video readout, the clamp prepare pulse initiates discharge of the dark current storage capacitor. This allows the clamp circuit to resample the vidicon dark current just before the picture-taking frame.

TABLE 2-V-2. AVCS CAMERA ELECTRONICS AND SPACECRAFT INTERFACE SIGNALS (Continued)

Interface Signal	Description
	Timing (Continued)
Clamp Hold	This signal lasts for the entire vertical frame during video readout and is used to inhibit the vidicon dark current sampling circuit. The dark current storage capacitor will then maintain its reference voltage during this entire interval.
Video Blanking	This signal gates off the video operational amplifier during horizontal retrace and establishes the rear porch on a horizontal line of the composite video signal.
Horizontal Sync	Applied to the horizontal deflection circuit to initiate horizontal sweep and retrace. It is also used as follows: (1) Provides the blanking signal for the beam current regulator. (2) Gates the switches in the clamp sampling circuitry. (3) Gates the camera video information on/off to provide the video sync tip.
Shutter Open, Shutter Close	Shutter operation is controlled by these two pulses; the delay between their leading edges determines the shutter exposure time.
Time Code Gate	This signal is used to gate the time code data into the video output amplifier.

In order to provide specific geometric information, a set of reticle marks is deposited on the vidicon target. The reticle pattern is shown on Figure 2-V-7. When the vidicon target is scanned, the reticle pattern appears superimposed on the image.

2. Gray Scale Calibrator Assembly

The objective of this unit to provide a gray scale (neutral density steps) capable of covering the dynamic range of the camera in discrete steps. Once the camera system has been set up, the gray scale may be calibrated and a curve of faceplate illuminance versus output level could be constructed. In addition, it will also reveal shifts or changes of vidicon sensitivity as a function of operating temperature and time. The calibrator assembly is 1.6 inches long, 1.3 inches wide, 0.14 inch high, and weighs 0.03 pound. This assembly is attached to the vidicon yoke assembly.

As shown in schematic diagram (Figure 2-V-8), the calibrator assembly consists of an incandescent light source, an aperture plate, filters, a positive lens, and a right angle prism. The light from the incandescent source that passes through the aperture is collected by the lens and beamed in parallel rays to one of the faces of a prism. The prism deflects the light rays through an angle of 90 degrees and illuminates the gray steps which have been deposited on the other prism face. The calibrator assembly is mounted in the camera housing so that the surface of the prism with the gray steps is parallel to, and very close to, the vidicon faceplate. The gray scale is projected onto the photosensitive surface of the vidicon.

The gray scale consists of 15 steps, each increasing in density by 0.13, to a maximum value of 1.83. The scale extends over a width of 0.375 inch, with each step being 0.025 inch wide.

Neutral density filters are mounted at either side of the gray scale aperture to obtain the desired light level from the gray scale lamp.

3. Deflection Yoke

The yoke is 5.84 inches long, 2.150 inches in diameter, and weighs a maximum of 1.15 pounds.

The deflection yoke consists of horizontal and vertical deflection windings and a corresponding pair of alignment coils. Electrostatic shields are provided on the inside of the yoke to shield the vidicon from the electrostatic effects of the deflection signals, as well as noise that may be introduced into the video via the deflection windings. Another electrostatic shield is placed between the windings

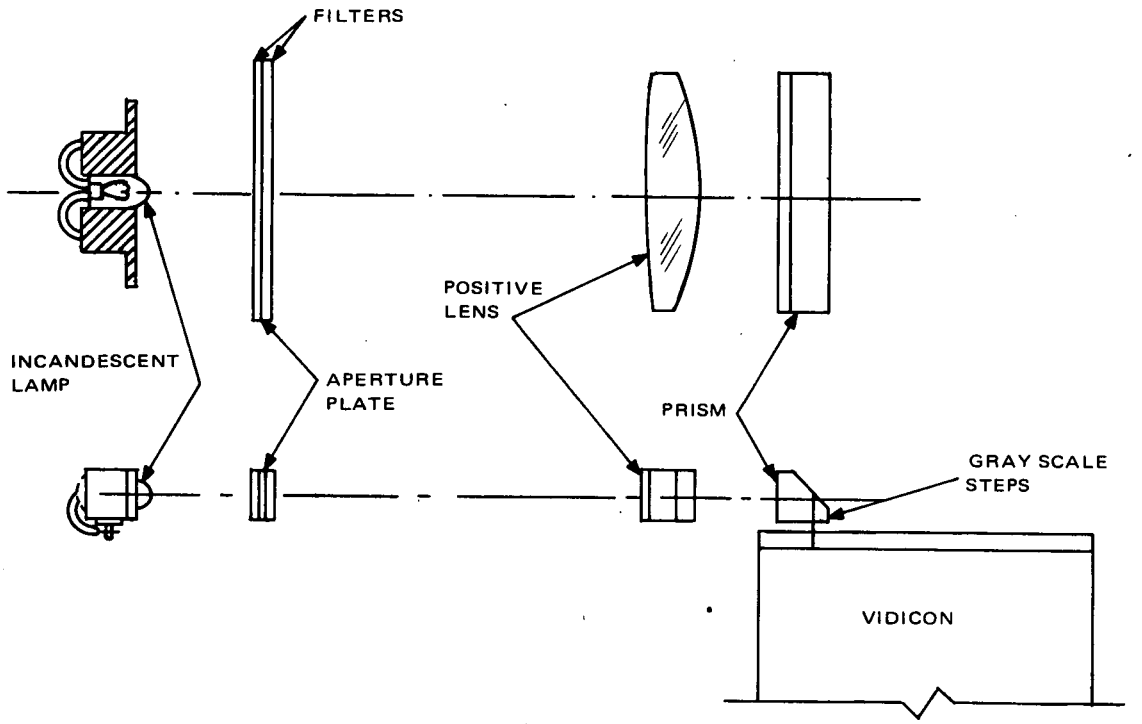


Figure 2-V-8. Gray Scale Calibrator, Schematic Diagram

to minimize deflection signal electrostatic crosstalk. A magnetic shield is placed over the entire assembly, which shields the vidicon from external magnetic fields and also shields external components from the deflecting fields.

This assembly is potted in an outer shell that facilitates mounting the vidicon to the overall housing. Three ears on this shell are used to keep the yoke aligned with respect to the housing. Thus, with the aid of adjustment rings on the overall housing, the vidicon and yoke can be accurately moved back and forth with respect to the lens to permit optical focusing.

Provisions are made to support a strip of finger contact material to make electrical contact with the vidicon target ring.

The yoke is designed to support and retain the vidicon assembly and to maintain correct electrical alignment between these two components. This combination of the yoke and vidicon plays the major part in camera focus and alignment. Focus is accomplished by a precise axial adjustment of the yoke-vidicon assembly. Centering the vidicon with respect to the optical axis is achieved by adjusting the yoke-vidicon assembly in a plane perpendicular to the optical axis; a roll adjustment is also performed at this time. Also during this adjustment, the yoke-vidicon assembly can be rotated about the optical axis so that correct orientation of the vidicon format is assured.

4. Shutter Assembly

The double-bladed shutter is 5.75 inches long, 3 inches wide, and 1.5 inches across the solenoids. The maximum weight is 0.5 pound. The housing is made from magnesium alloy.

The shutter is a focal plane type. The main components are two blades, one for starting the exposure and the other for stopping it. Each blade is driven by a solenoid.

5. Lens

The lens is a Tegea Kinoptic Apochromat, focal length 5.7 millimeters, aperture f/1.8. A Y-10 filter has been incorporated in the lens. The lens has been ruggedized and vented between the larger elements and is 6.18 inches long, 3.86 inches at its greatest diameter, and weighs 2.6 pounds. It is provided with a flange mount and pilot diameter to facilitate mounting. The lens is bolted into the housing and supported at both ends. The iris can be adjusted for optimum performance and then locked in position.

6. Preamplifier

The preamplifier is located on the vidicon sensor housing in close proximity to the vidicon target. A low noise, high input impedance, field effect transistor comprises the input stage. This provides an input impedance of 1 megohm and thereby optimizes noise input. An emitter follower output stage, in the feedback amplifier, provides the necessary output drive for the camera electronics.

7. Vidicon Electrode Decoupler

The vidicon electrodes G1, G2, G3/G6, and G5 are isolated by low pass, RC filter networks, in series with their power supplies. These filters are located close to the vidicon pins and buffer the electrodes from converter ripple and extraneous signals.

(b) Camera Electronics

The camera electronics provides the interface between the spacecraft, the AVCS camera sensor, and the tape recorder. In addition, it provides

necessary electronics for operation of the camera sensor and telemetry outputs. The following circuits are contained in the camera electronics:

- AC video amplifier;
- Video clamp, dark current sampling;
- Shading correction;
- DC amplifier;
- Black and white clippers, video blanking and porch, and time code insertion;
- Output emitter follower and sync insertion;
- Horizontal deflection;
- Vertical deflection;
- Yoke skew corrector;
- Main DC-to-DC converter;
- Filament DC-to-DC converter;
- +13-volt regulator;
- Beam current regulator;
- Standby power switch;
- Shutter drive;
- Command buffers;
- Gray scale calibration regulator; and
- Telemetry.

The camera electronics (CE) is housed in an aluminum container 9.6 by 7.9 by 4.8 inches, finished with a chemical dip and painted with an epoxy blue paint. Mating portions of the container are free from paint to ensure good electrical bond.

The two DC-to-DC converters are housed within an RF-tight compartment. The remainder of the electronics are mounted on five printed circuit component boards which plug into a harness board. Feed-through capacitors are used between the harness board and the unit connectors to improve the RF immunity of the camera sensor.

(2) FUNCTIONAL OPERATION

(a) AVCS Camera Sensor

Figure 2-V-9 shows the position of the vidicon electrodes, their potentials with respect to the cathode, the equipotential lines of the fields created by them, and the approximate path of the deflected electron beam. The radial distances, however, are greatly exaggerated. Grids 3, 4, and 5 form a low voltage Einzel-type electrostatic lens.

The paths of three electrons are shown. The first electron's path is straight down the tube. Since its path is normal to the equipotential lines between grids 3, 4, and 5, it is undeflected by these fields. The magnetic field produced by the deflection yoke causes the electron to be deflected upward. When the electron enters the accelerating field between grids 5 and 6, a velocity component is added in a direction normal to the equipotential lines and the path of the electron is changed to one that is parallel to the axis of the vidicon.

This collimating field produced by grids 5 and 6 causes the electron beam to land nearly normal to the target. The result is less shading due to beam landing error than with conventional "all magnetic" vidicons.

The second electron is a divergent electron which enters the field between grids 3 and 4 at an angle. Since this is a decelerating field, the component of the velocity which is normal to the equipotential lines is reduced. This causes the electron's path to curve outward and decrease in speed. When the electron enters the accelerating field between grids 4 and 5, it is accelerated towards

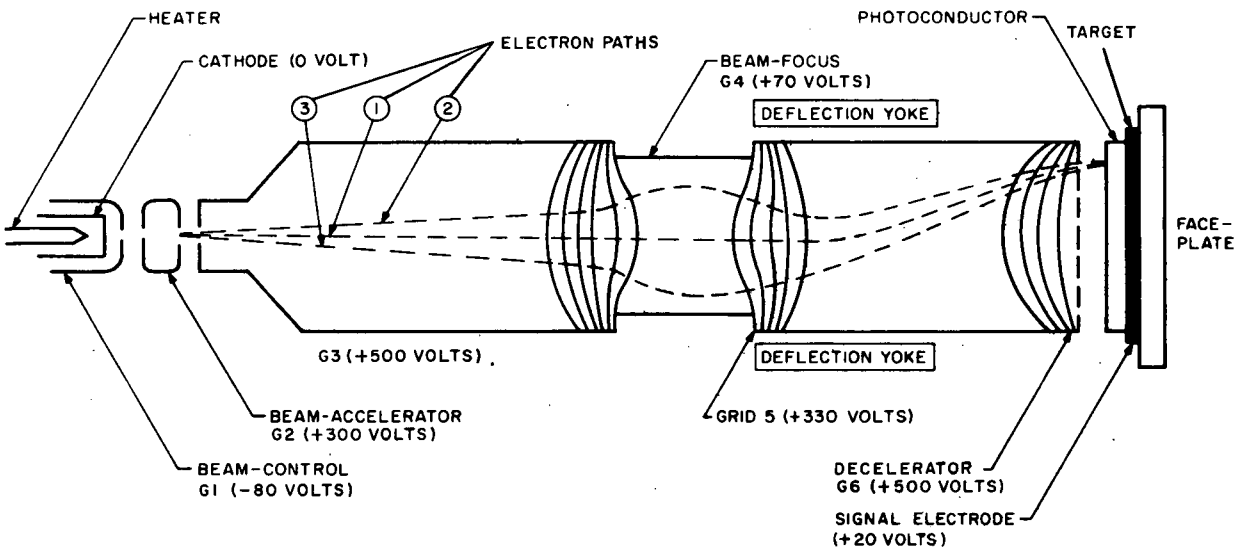


Figure 2-V-9. Hybrid Vidicon Tube

the axis of the vidicon. As before, the collimating field of grids 5 and 6 "straightens out" the electron path after it has been deflected by the magnetic field of the yoke. The third electron's path is similar to that of the second, excpet that it is divergent in the opposite direction.

The conversion of light energy to electrical modulation takes place at the target. The target consists of a transparent conducting film (signal electrode) deposited on the inner surface of the optically-flat glass faceplate and a thin layer of photoconductive material deposited on the signal electrode. The photoconductor is a continuous semiconductive layer, which is so thin that it has a high lateral resistance and can therefore be considered as many separate elements. The transverse resistance of each element depends upon the amount of light falling on the element. Each of the elements acts as a capacitor shunted by a variable resistor as shown in Figure 2-V-10.

The video output circuit consists of a load resistor connected from the target ring to the target voltage source and a coupling capacitor connected from the target ring to the video preamplifier.

The cycle of operation for the hybrid vidicon as used in this manner consists of the following cycle of events:

- Photoconductor preparation,
- Exposure, and
- Readout.

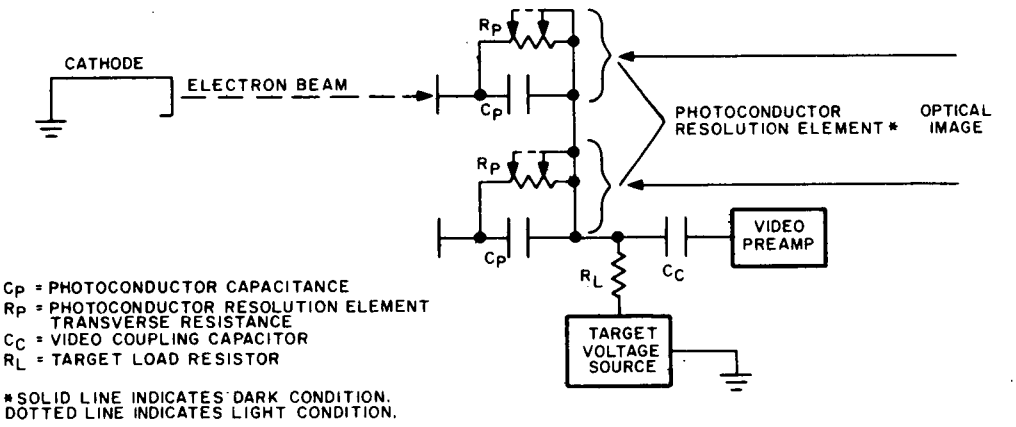


Figure 2-V-10. Equivalent Circuit of Vidicon Target, Simplified Schematic

The preparation period is actually a combination erase and prepare period. During the six scans prior to exposure, the residual charge pattern from the previous cycle is neutralized and the beam side of the photoconductor is brought to cathode potential. When the beam side of the photoconductor is at cathode potential, the electrons in the beam will not land on the photoconductor but will be collected by the electrodes in the gun. Since the shutter is closed during this period, the transverse resistance of each resolution element is high and, therefore, very few electrons can move through the photoconductor. At the end of the vidicon preparation period, the photoconductor is fully charged. The beam side is at cathode potential (V_K is approximately 0 volt) and the signal electrode side is at the target potential (V_T is approximately 20 volts positive). The preparation sequence is illustrated in Figure 2-V-11 A and B.

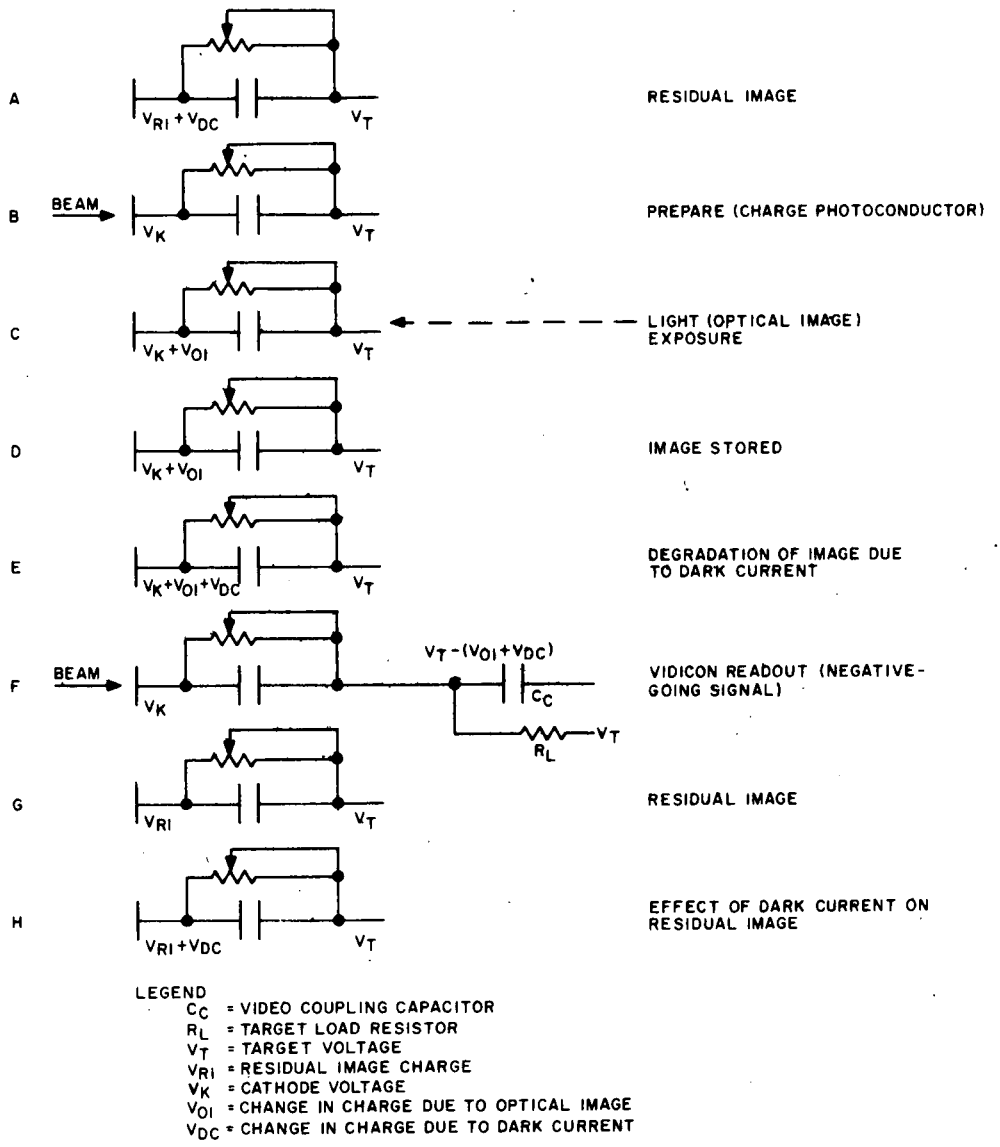


Figure 2-V-11. Vidicon Signal Sequence Diagram

When the shutter opens, the lens focuses the optical image on the photoconductor through the glass faceplate and transparent signal electrode. The presence of light increases the conductance of the photoconductor, and conduction from the beam side to the signal electrode side takes place, effectively discharging the capacitive component. In other words, the electrons stored on the beam side are allowed to pass through the resolution element to the more positive signal electrode. Since the electron beam is not scanning the photoconductor, electrons passing through the resolution element are not replaced. Thus, the beam side of each resolution element assumes a potential somewhere between V_K and V_T (Figure 2-V-11C). When the shutter closes and removes the light, each resolution element returns to the low conductivity (high transverse resistance) condition. The beam side of the photoconductor now has a charge pattern that corresponds to the image pattern that was focused on it, as indicated in Figure 2-V-11D.

However, even in the absence of light, the photoconductor is not a perfect insulator. This inherent characteristic allows some electron movement through the photoconductor (from the beam side to the signal electrode side). Refer to Figure 2-V-11E. Since this electron movement occurs in the unexposed (dark) areas as well as picture areas, it is referred to as dark current. Dark current is very sensitive to temperature changes, increasing as temperature increases. If compensation for dark current charges were not made, the output voltage for scene black would change with changes in temperature. It is the function of the video clamp, described later, to adjust for the variation in dark current due to temperature.

During vidicon readout, the shutter is closed. The beam scans the photoconductor once, depositing a sufficient number of electrons to lower the beam side of each resolution element almost to cathode voltage (V_K). Electrons that approach resolution elements that are already near V_K (black or dark areas) do not land but are collected by the high-potential electrodes, mostly grid 2. Electrons deposited on the beam side of the resolution element replace charges that were lost from the capacitive component during optical exposure and during dark current degradation. Thus, the potential on the beam side of the resolution element is quickly dropped toward V_K. The charging current (electrons deposited) flows through the photoconductor capacitor Cp, load resistor R_L, target voltage supply, vidicon cathode, and back to the photoconductor by way of the beam. The circuit is shown in Figure 2-V-10. The voltage drop caused by this current (in the order of a few nanoamperes) through R_L is coupled by capacitor C_c to the preamplifier. The amount of current and hence the peak video signal is proportional to the light intensity falling on the resolution element, and the change in charge due to dark current (see Figure 2-V-11 F, G, and H).

A schematic of the video preamplifier is shown on Figure 2-V-12. A 1-megohm input impedance was selected to optimize the noise characteristics of the FET and the vidicon-to-preamplifier match. The emitter follower output stage in the feedback amplifier provides the necessary drive for the following video amplifier which is located in the camera electronics package.

Precision resistors R8 and R14 maintain the preamplifier gain, which is typically 16.7. The input impedance of the preamplifier is set by resistor R2, R4, and R5.

Shutter operation was explained in Paragraph 2.V.B.2.a and illustrated on Figure 2-V-3.

(b) Camera Electronics

A functional block diagram of the camera electronics is shown on Figure 2-V-5. The circuits contained in the camera electronics are listed in Paragraph 2.V.B.3.a.(2). The following paragraphs explain the functional operation of each of these circuits.

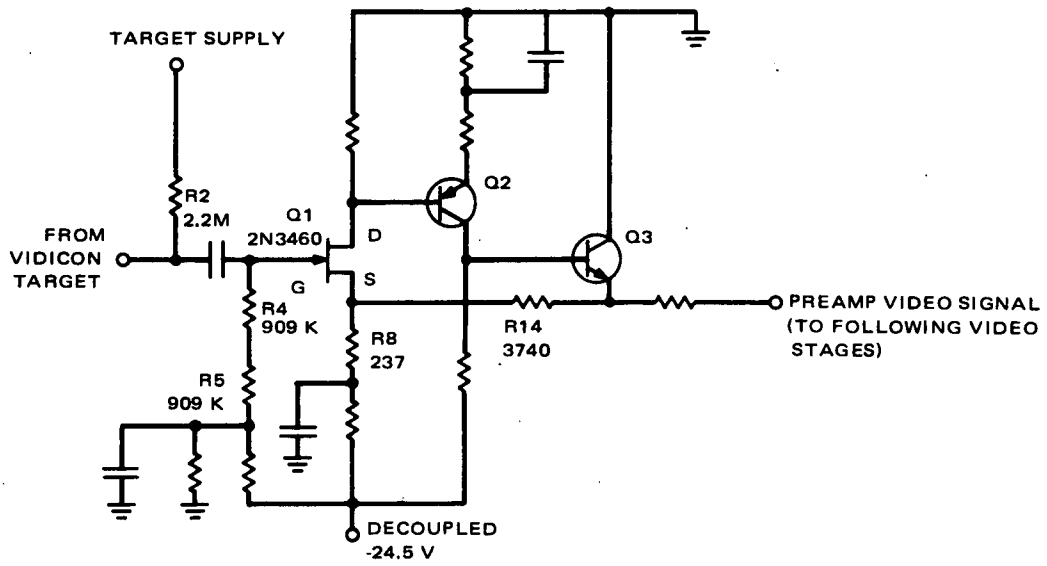


Figure 2-V-12. Preamplifier, Schematic Diagram

1. AC Video Amplifier

As shown on Figure 2-V-13, the video signal from the preamplifier is fed into a single-stage transistor amplifier which has a midfrequency gain of approximately 1.1, and contains low frequency phase compensation and high frequency peaking. Resistor R2 and capacitor C2 constitute the phase correction which compensates for the low frequency attenuation of the coupling capacitors. The video high frequency roll-off that occurs at the preamplifier input is compensated for by the high frequency peaking of components R5 and C4. In addition to the phase and high frequency compensation, this stage has a capacitor (C3) in its collector circuit to begin rolling off the amplifier response beyond the system bandpass. The output of this amplifier is applied to emitter follower Q2, and output gain is controlled by potentiometer, R2.

The video signal is next applied to a three-stage complementary feedback amplifier. The midfrequency gain of this amplifier, which is controlled by R12, R13, and R16, is approximately 10.2. The first of two vidicon aperture correction networks is located within this amplifier. R12 and capacitor C7 make up the high frequency amplitude peaking network that compensates for the finite vidicon beam size, and a single transistor stage with resistor R19 and capacitor C9 make up the vidicon aperture phase correction circuit. This stage is adjusted to approximate a linear phase shift, or constant time delay throughout the video system passband.

From the correction networks, the video signal is applied to another complementary feedback amplifier, (Q7, Q8, and Q9) similar to Q3, Q4, and Q5. A midfrequency gain of approximately 4.7 is controlled by R26, R27, and R30. A second vidicon aperture amplitude correction network is located within this feedback amplifier. This high frequency amplitude peaking is controlled by R26 and C11.

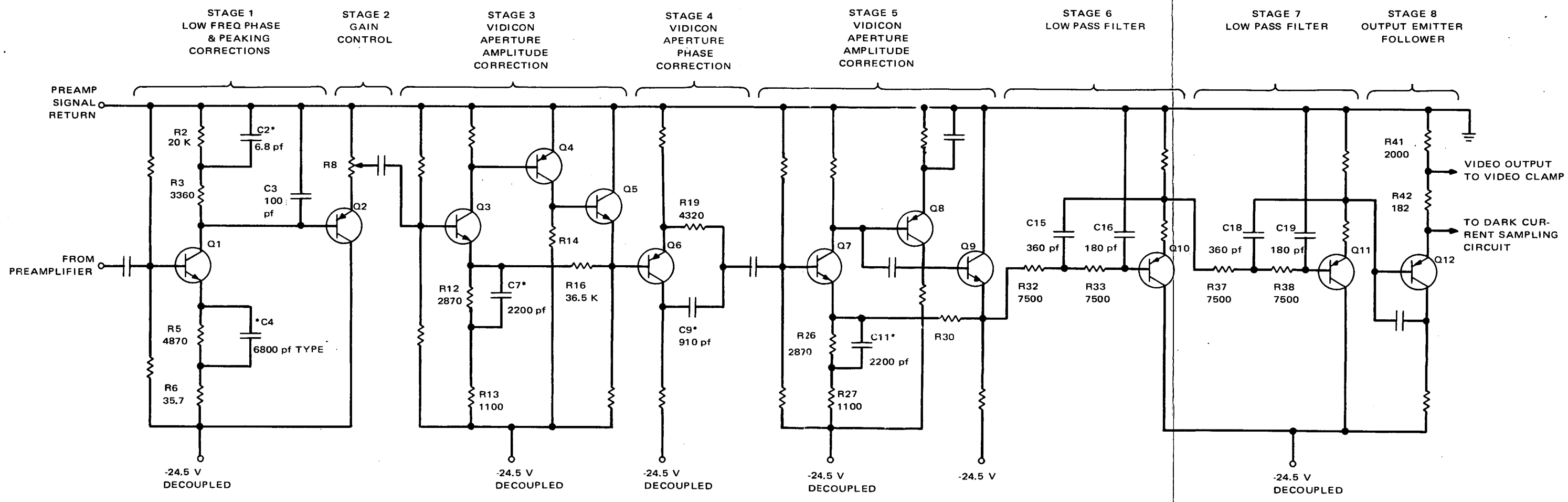
From the output of stage 9, the signal is applied to two identical low-pass active filter stages, in series. Each of these filters is made of two filter sections which roll off the response beyond the system passband.

The final amplifier stage is an emitter follower which provides low output impedance for the following video clamp and dark current sampling circuit.

2. Video Clamp Dark Current Sampling

The video clamp (Figure 2-V-14) serves two functions:

- It restores the DC video level and
- It compensates for the vidicon dark current pedestal.



*SELECT AT TEST

FOLD IT FRAME 1

Figure 2-V-13. AC Video Amplifier, Schematic Diagram

FOLD OUT FRAME 2

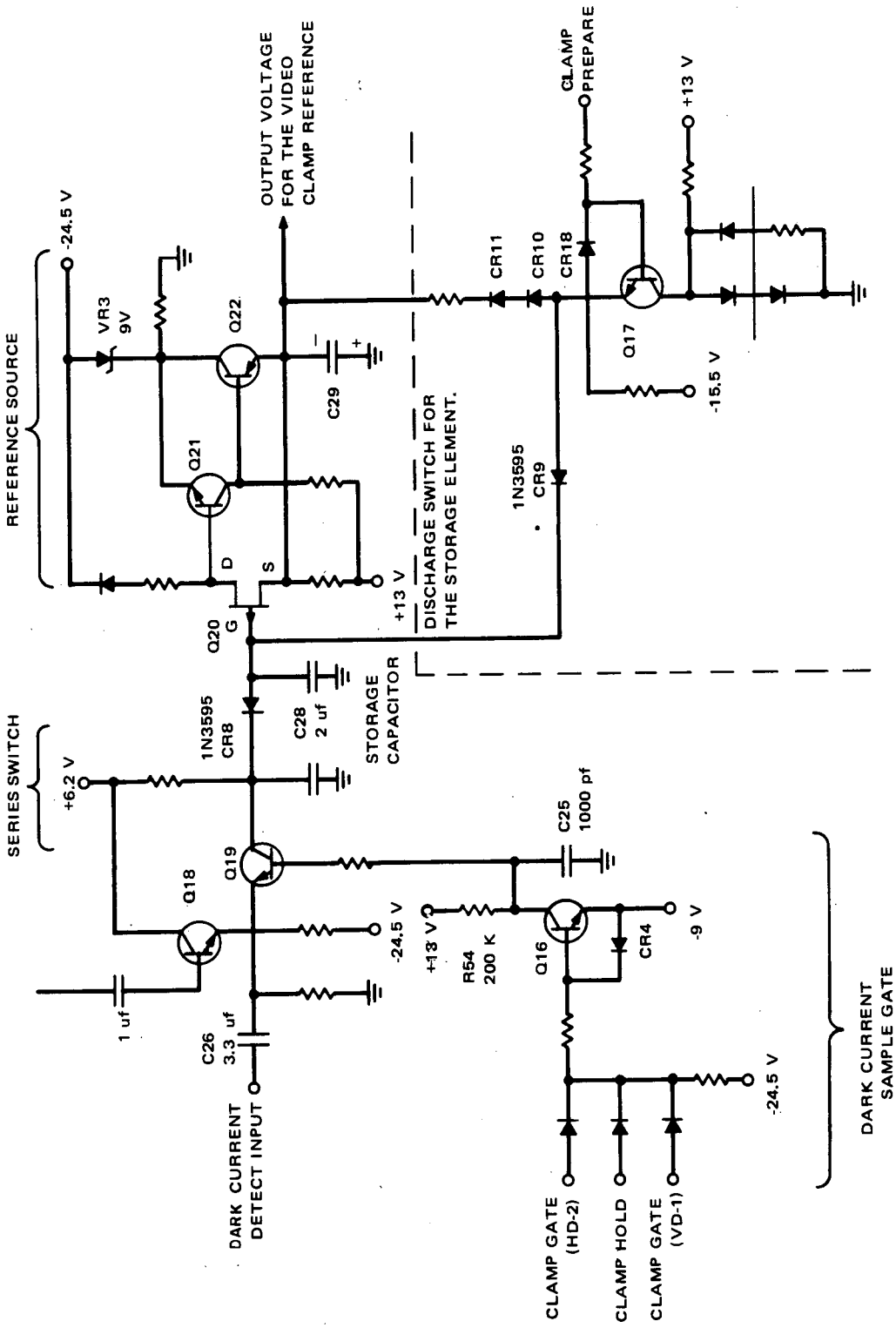


Figure 2-V-14. Dark Current Sampling Circuit, Schematic Diagram

To understand the operation of the clamp, first consider the video signal shown in Figure 2-V-15. This is the case wherein there is no light input to the vidicon. Notice, however, that there is a signal output even though there was no incident light. This residual dark current signal is always present to some degree in the vidicon output and would pose no problem if the level was fixed. Unfortunately, this is not the case, since dark current is temperature sensitive. The higher the vidicon photoconductor temperature, the greater the dark current signal. Dark current, then, makes the output form a vidicon appear to sit on a dark current pedestal as shown in Figure 2-V-16. In this illustration, the dark current is shown to be about one-half of the total useful video swing. Under some conditions, this dark current signal may become two to three times as great as the useful video level.

Besides restoring DC level to the video, the clamp must also provide a means for removing the dark current signal without losing useful video. These two tasks are accomplished simultaneously by sampling the dark current signal for one complete vertical field prior to an optical exposure. Thus, an average of the dark current for the entire vertical field is obtained at the same temperature as the following field during which optical exposure takes place.

Assume that the 2.0-microfarad storage capacitor at the gate of Q20 (Figure 2-V-14) is discharged to approximately 0.6 volt. Also assume that the dark current in the composite video signal is 1.5 volts peak-to-peak at the video amplifier output. This signal is applied through a 1-microfarad coupling capacitor to the base of emitter follower (Q18).

Since the pulse duty cycle is 8.3 percent, the peak negative excursion of 1.5 volts represents the dark current signal at the base of emitter follower (Q18).

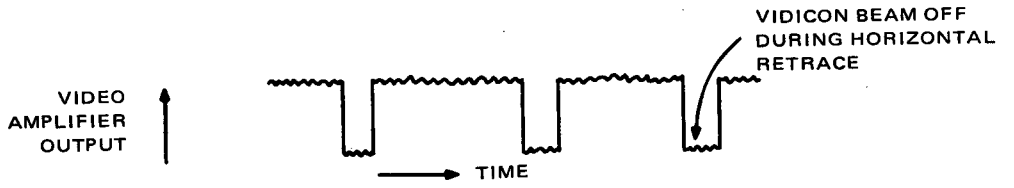


Figure 2-V-15. Video Signal With No Incident Light

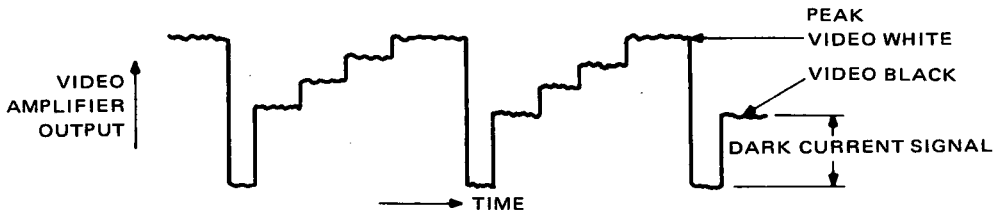


Figure 2-V-16. Dark Current Pedestal

The output from the emitter follower goes to a series switch (Q19) that is gated to sample the dark current signal only during the time when the dark current pulses are present.

Sampling of the first portion of each pulse is delayed by the R54 and C25 time constant in the collector of the dark current sample gate, Q19. Delay at the end of the dark current signal results directly from the video amplifier. Because the video is delayed approximately 5 microseconds, the trailing edge of the video sample will be automatically removed when the sample gate is turned off. Thus, only the center portion of each pulse is sampled and applied through a diode to the low leakage 2.0-microfarad storage capacitor.

The remaining portion of the clamping circuit is shown in Figure 2-V-17. A typical 1.5-volt peak-to-peak video dark signal is sampled and stored on a 2.0-microfarad capacitor (Figure 2-V-14) as -1.5 volts DC. This voltage is read out by field effect transistor (Q20) giving a -1.3-volt DC offset to the 1.5-volt DC signal, resulting in a net -2.8 volts for the video clamp reference. In clamping the video to -2.8 volts, the video black always appears at -1.3 volts. Figure 2-V-18 shows the timing diagram for sequencing the dark current sampling.

The only remaining consideration is the switch used to discharge the dark current storage capacitor after video readout. Since the vidicon target temperature can vary from one exposure to the next, a corresponding change in the dark current signal may also be expected. Consequently, one field prior to optical exposure, a 250-millisecond "clamp prepare" pulse is applied to a transistorized discharge switch (see Figure 2-V-17) to remove the dark current charge accumulated on the 2.0-microfarad storage capacitor.

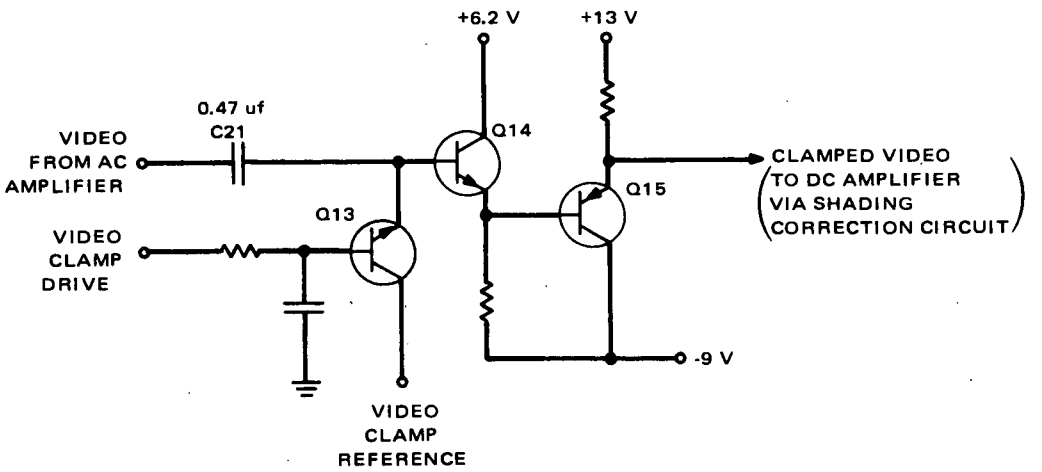


Figure 2-V-17. Clamp Circuit, Schematic Diagram

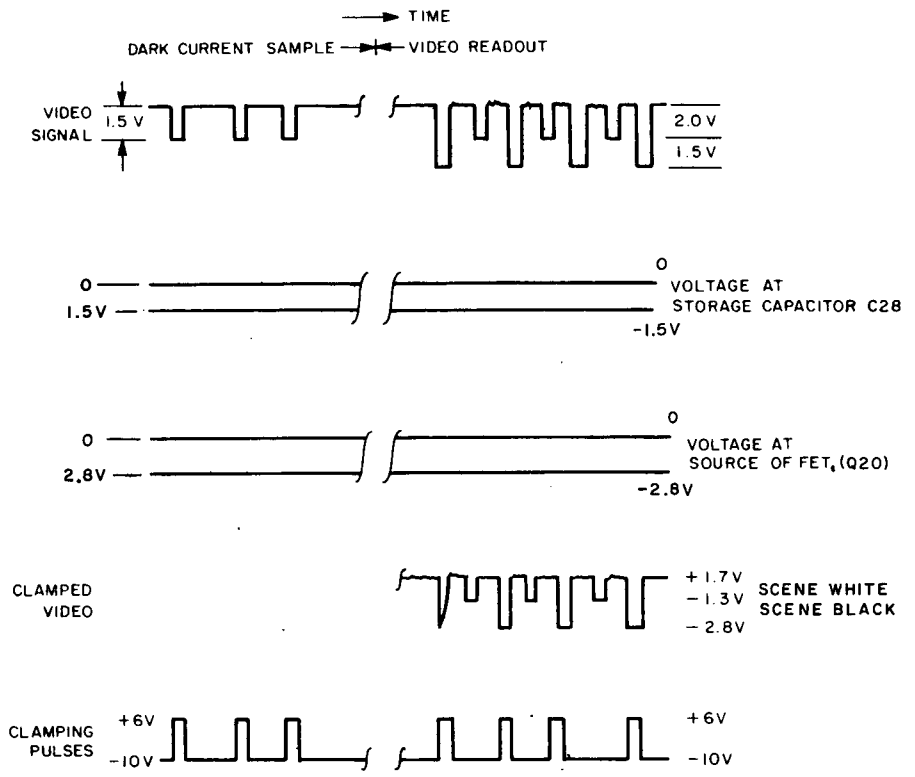


Figure 2-V-18. Dark Current Sampling, Timing and Sequencing Diagram

3. Shading Correction

The shading correction circuit (Figure 2-V-19) reduces the effect of nonuniformities in the vidicon and changes in the relative illumination of the lens to an acceptable level. Shading due to the lens alone or the vidicon alone is generally less than the maximum permissible. However, the two together may produce an unacceptable level of shading, and, hence, the need for correction.

Lens shading is caused by decreased lens efficiency, and reduced illumination on the image plane toward the edge of the image. It is generally symmetrical about the optical axis of the lens. The shape approximates a parabola in both the horizontal and vertical directions.

The shape of the vidicon shading is similar to the lens shading except that there is often some horizontal tilt, either to the right or to the left. In the vertical direction, there is often a loss of storage within the photoconductor. This means the signal output at the end of the read frame is of a lower amplitude than the signal output at the beginning of the frame, for equal values of illumination. Therefore, vertical shading usually has a tilt component in only one direction, as well as a parabolic component.

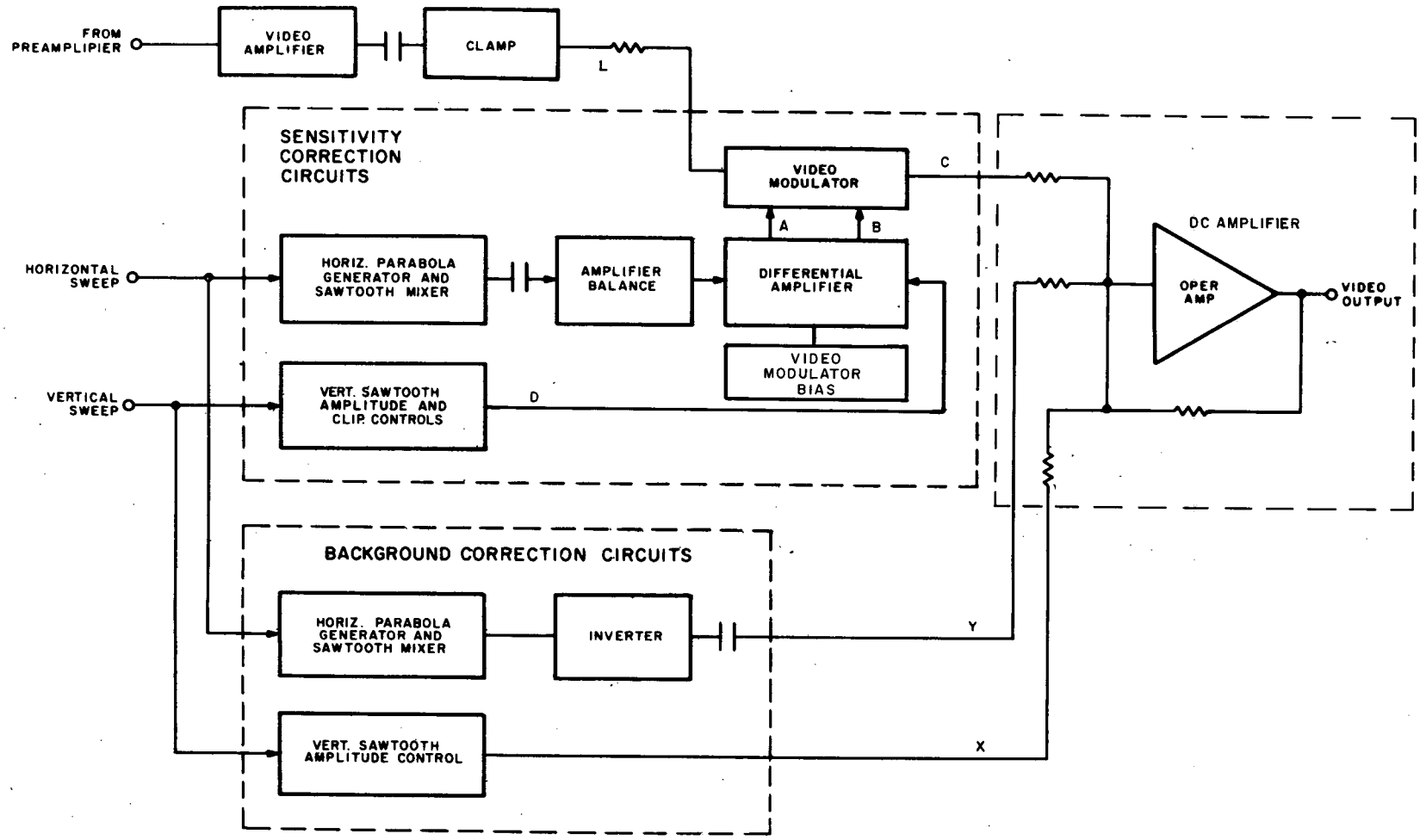


Figure 2-V-19. Shading Correction Circuit, Block Diagram

It would be desirable to correct the vertical parabolic shading component and the loss of storage component independently. The loss of storage component can be corrected with a sawtooth signal which is already available from the vertical deflection generator. The generator of a vertical parabola with a 6.5-second period would require either a very large integrating capacitor, a medium size capacitor with an operational amplifier, or a diode network to construct a linear parabola from positive and negative sawtooth signals. In short, the vertical parabola is much more difficult to generate than a horizontal parabola and, for the reason to be given later, it was felt that the usefulness of a vertical parabola did not warrant the additional circuitry that would be required. Further consideration of vertical shading reveals that the parabolic shading and the loss of storage shading tend to cancel each other in the first half of the vertical scan as shown in Figure 2-V-20.

The resultant vertical shading can be corrected by sawtooth signals with positive slope that starts in the middle of the vertical scan. Thus, if the parabolic and sawtooth components of vertical shading are present in the proper proportion there is no need for vertical parabolic shading correction.

In addition to the sensitivity variations described above, there is also background shading (or black level shading) which is due to vidicon dark current variations. Although the background and sensitivity shadings have similar

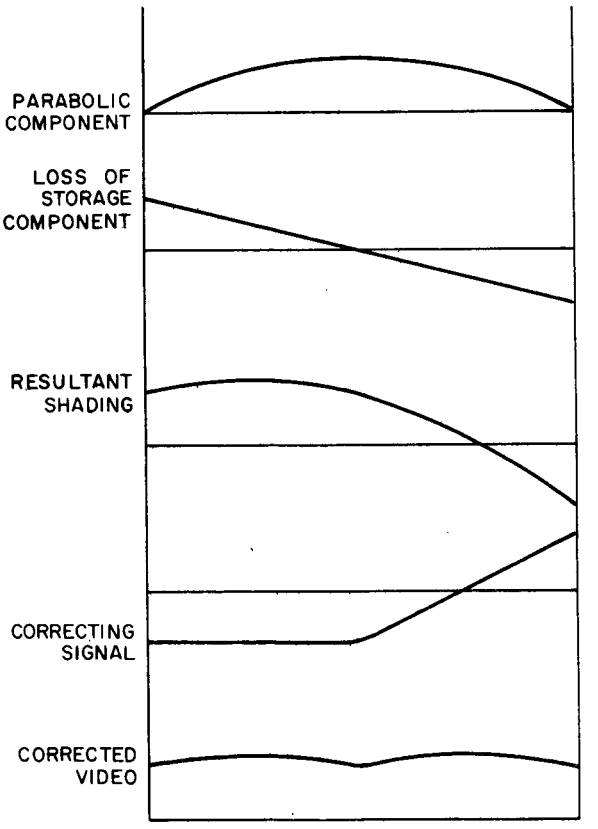


Figure 2-V-20. Vertical Shading Components

shapes, the tilt and parabolic components of each may not have the same relative magnitudes. It is therefore desirable to control the sensitivity shading correction independently.

The shading correction circuit is capable of correcting or minimizing the follow-shading components:

Sensitivity Correction

- Horizontal parabola,
- Horizontal sawtooth, both positive and negative slopes, and
- Vertical sawtooth, positive slope only, which can be started at any part of the vertical scan.

Background Correction

- Horizontal parabola,
- Horizontal sawtooth, both positive and negative slopes, and
- Vertical sawtooth, positive slope only.

The sensitivity shading correction circuitry can correct for 60 percent of shading, provided the shape of the shading closely approximates a combination of sawtooth and parabola. The background shading correction circuitry can correct for 50 percent of background shading, providing it also approximates a combination of sawtooth and parabola.

The shading due to dark current in the vidicon is very dependent on temperature, whereas lens shading is not. It would be difficult and costly in terms of weight and power to have the shading correction circuitry track the change in vidicon shading over temperature. When the shading correction circuitry is set up for a particular lens-vidicon combination, a compromise is made to obtain the best overall performance over the temperature range.

The heart of the sensitivity correction circuitry is the video modulator (Figure 2-V-19), a network of six diodes and eight resistors, shown in Figure 2-V-21, that serves as a variable attenuator. The correcting signals are applied to the network at points A and B. These signals are equal amplitude but opposite polarity. Since the network is balanced, the signal at A and the signal at B cancel at point C. Consequently, the correction signal itself does not appear in the video.

As point A goes positive and point B goes negative, diodes CR2 and CR3 will start conducting when the potential across the 75-kilohm resistors is approximately 0.6 volt. When CR2 and CR3 are conducting, the 75-kilohm resistors are effectively shorted, and the impedance of each half of the network has decreased by 75 kilohms. As the amplitude of the signals at A and B increases

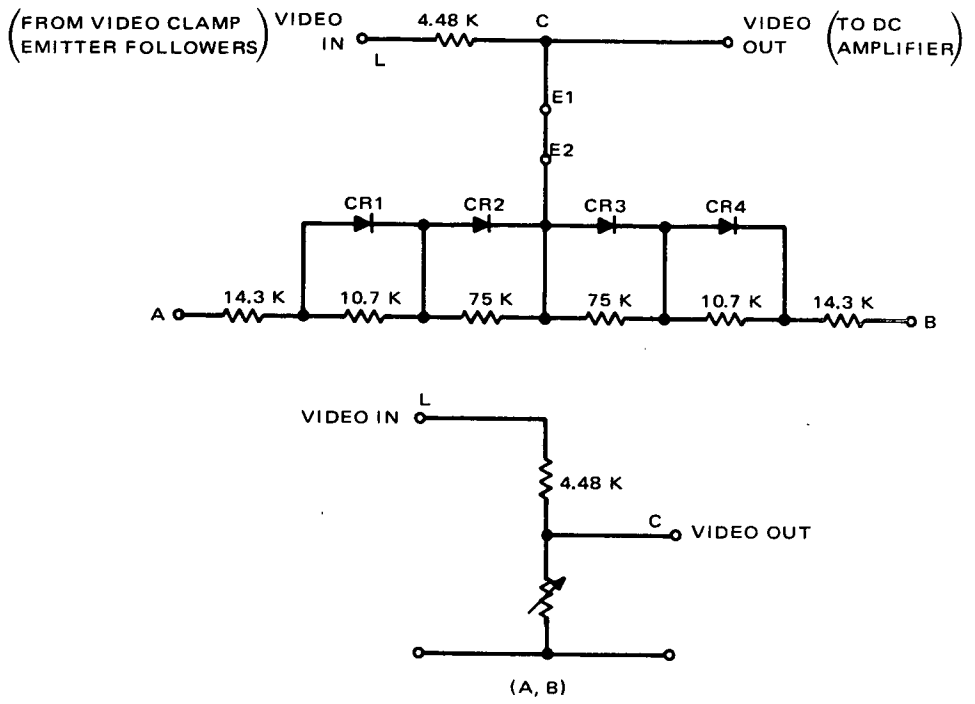


Figure 2-V-21. Video Modulator Operation, Simplified Schematic Diagram

further, the 10.7-kilohm resistors are shorted out, so that only the two 14.3-kilohm resistors remain. Because points A and B are driven by emitter followers with very low impedances, they are effectively at AC ground. Thus, the impedance from point C to AC ground can change from 50 kilohms when no diodes are conducting to 7.15 kilohms when all diodes are conducting. Since the characteristic curves of the diodes have "rounded knees", there is a continuous impedance change with no discontinuities. The transfer ratio of the modulator can vary between 0.92 and 0.61, giving a gain change ratio of 1.5 to 1.

The two signals applied to points A and B are supplied from the differential amplifier shown in Figure 2-V-22. This circuit and the associated current source perform the following functions:

- Mix the horizontal and vertical correction signals,
- Provide a gain of 2.4 for the correction signals,
- Control the DC level of the video modulator so that the modulator will not shift the video black level.
- Control voltage offset points A and B so that the diodes in the video modulator will begin conducting at the proper part of the correction signal, and
- Provide two outputs of equal amplitude but opposite polarity.

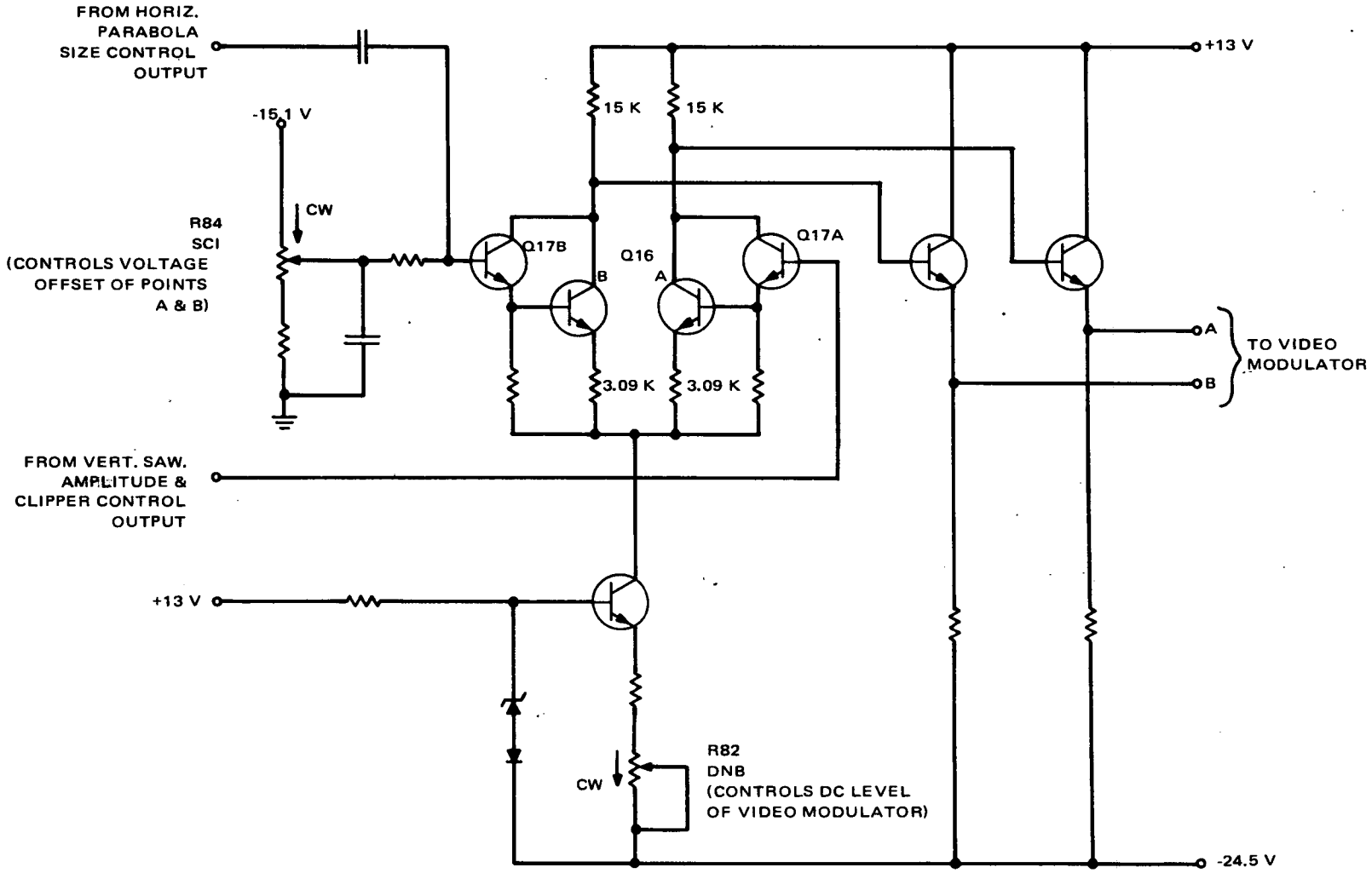


Figure 2-V-22. Differential Amplifier, Video Modulator Bias, Differential Amplifier Balance and Emitter Followers, Schematic Diagram

The vertical sawtooth amplitude and clipper control signal is direct-coupled to the base of Q17A. Direct coupling is necessary because the period of the vertical signal is 6.5 seconds. The horizontal size control signal, as well as the signal correction insertion, is connected to the base of Q17B. R84 controls the offset voltage between points A and B and is set up so that maximum sensitivity correction can be obtained with a minimum of video signal attenuation. Minimum attenuation occurs when all diodes are "off"; so R84 should be set so that all diodes are "off" during the readout of the areas of the vidicon which have minimum sensitivity. When the areas of higher sensitivity are read out, the correction signals will have switched "on" one or more pairs of diodes, thus attenuating the video signal from these areas and making it equal in amplitude to the video signal from the low sensitivity areas.

R82 adjusts the amount of current supplied by the bias source and therefore the in-phase voltage levels of points A and B. R82 is set so that the voltage level of point E1 (in Figure 2-V-21) is exactly equal to the voltage of picture black. When this is done, there will be no DC current flow between the video modulator and the rest of the video circuits.

Figure 2-V-23 shows the horizontal parabola generator and size controls. R21 and C9 integrate the horizontal sawtooth thus generating a parabola which is amplified by transistor Q3. Emitter follower Q9 and resistor R51 provide the parabola size control for the sensitivity correction circuit.

The vertical sawtooth amplitude and clipper controls for the sensitivity correction are shown in Figure 2-V-24. The level at which the sawtooth is clipped is set by R22. When R22 is in midposition, the voltage at the anode side of CR8 is near 0 volt. The first half of the vertical sawtooth, which is negative, reverse biases CR5. The resultant signal at the diode side of R15 is a steady DC level. The second half of the vertical sawtooth, which is positive, forward biases CR5 and reverse biases CR8. This portion of the sawtooth, therefore, appears at the diode side of R15. Thus, a clipped vertical sawtooth is present at the diode side of R15. R15 and R14 form a level shifter to obtain the proper DC level for the differential amplifier. R18 controls the amplitude of the clipped vertical sawtooth.

The background correction signals are added to the video by an operational amplifier, as shown in Figure 2-V-22. The horizontal parabola signal source for background correction is shown in Figure 2-V-23. The signal from the parabola generator is amplified and inverted by transistor Q6 and the amplitude of the parabola is controlled by R43 before it is added to the video in the operational amplifier. Figure 2-V-24 shows the vertical sawtooth amplitude and clipper controls for the background correction. This operation of this circuit is similar to the operation of the vertical amplitude and clipper sensitivity circuit which was described previously. Resistor R19 controls the point at which the sawtooth signal starts. The amplitude of the clipped vertical sawtooth is controlled by R17.

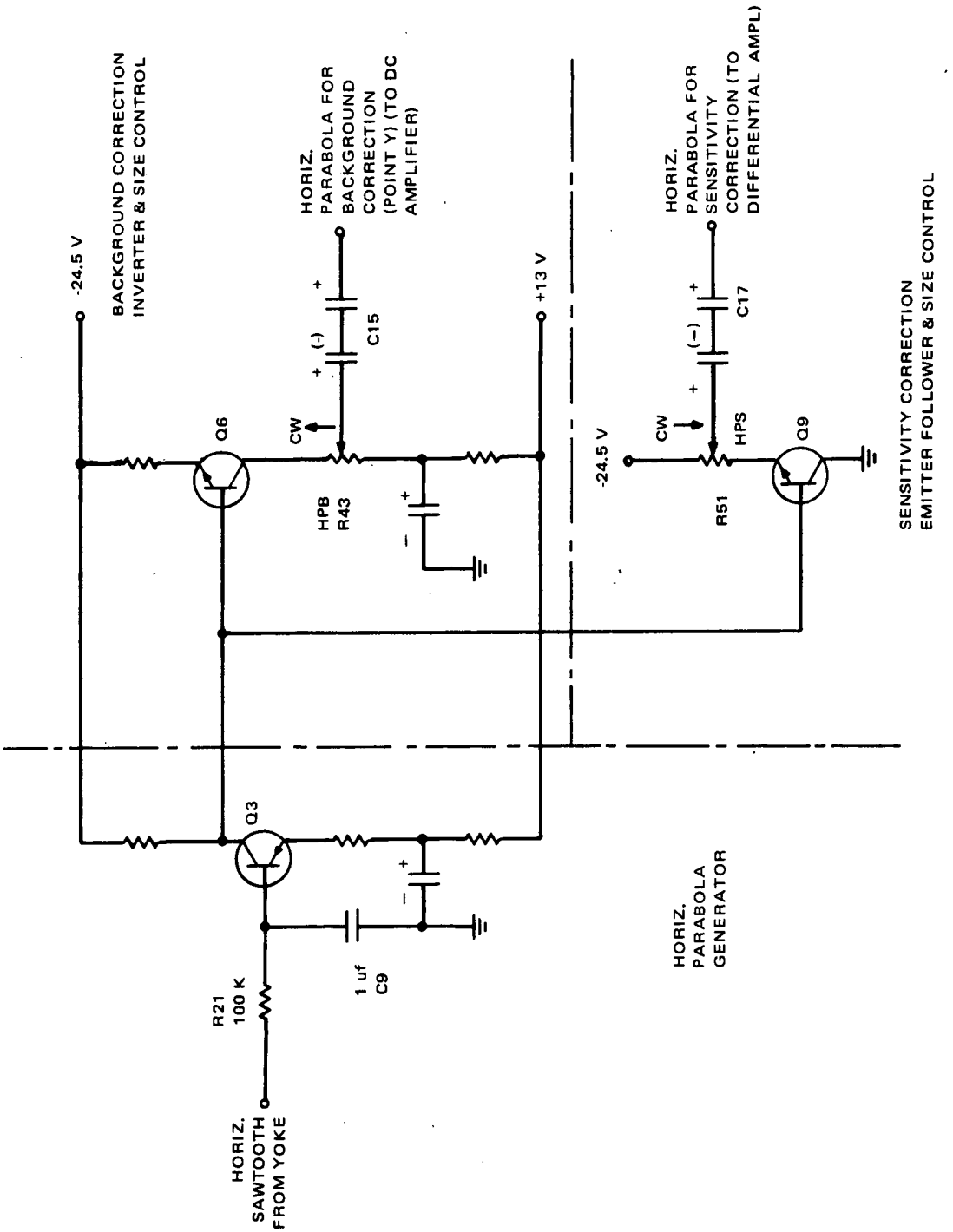


Figure 2-V-23. Horizontal Parabola Generator and Size Controls

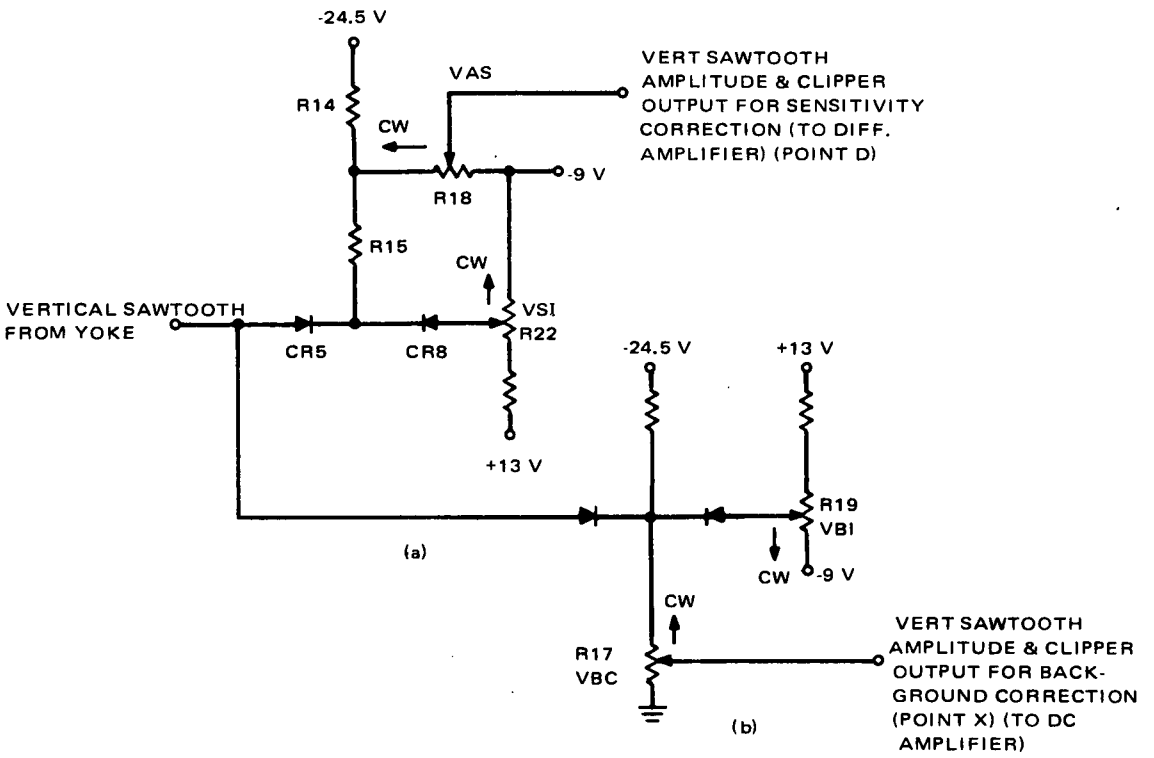


Figure 2-V-24. Vertical Sawtooth Amplitude and Clipper Controls for Sensitivity and Background Corrections

The sensitivity shading correction circuit can correct for 30-percent shading, provided the shape of the shading closely approximates a combination of a horizontal parabola and a vertical sawtooth, which is initiated before the center of the vertical scan. The background shading correction circuitry can correct for 20-percent background shading, provided it approximates a combination of a horizontal parabola and a vertical sawtooth, which is initiated before the center of the vertical scan.

The shading due to dark current in the vidicon is dependent upon temperature, whereas the lens shading is not. It would be difficult and costly in terms of weight and power to cause the shading correction circuitry to track the change in vidicon shading over the entire temperature range.

Some combinations of lens and vidicon are well below the shading specification limit without the use of shading correction. In those instances, it is likely that the shading correction circuitry will be unnecessary because the power saving and improved stability may outweigh the improvement in shading that can be obtained.

4. DC Amplifier

The video signal from the shading corrector is amplified and level-shifted by the DC amplifier shown in Figure 2-V-25. This is an operational amplifier, consisting of a dual differential transistor input stage followed by a common emitter transistor stage, Q4.

The dual differential transistor is used in the input stage of the operational amplifier to both minimize V_{BE} temperature drift and provide the video black level adjustment for the video signal. Overall operational amplifier gain is controlled by R16, the 200-kilohm feedback resistor, and the associated series input resistor. Video gain is approximately 2.5, while the gain is only 0.7 for horizontal base line correction, and 0.2 for vertical base line correction. This amplifier configuration readily lends itself to this operation and the bandwidth is controlled by the 4-picofarad capacitor in the feedback loop.

Diode CR6, between the two bases of the differential pair, protects the base to emitter junction of the first differential transistor and limits the peak dark current excursions of the video.

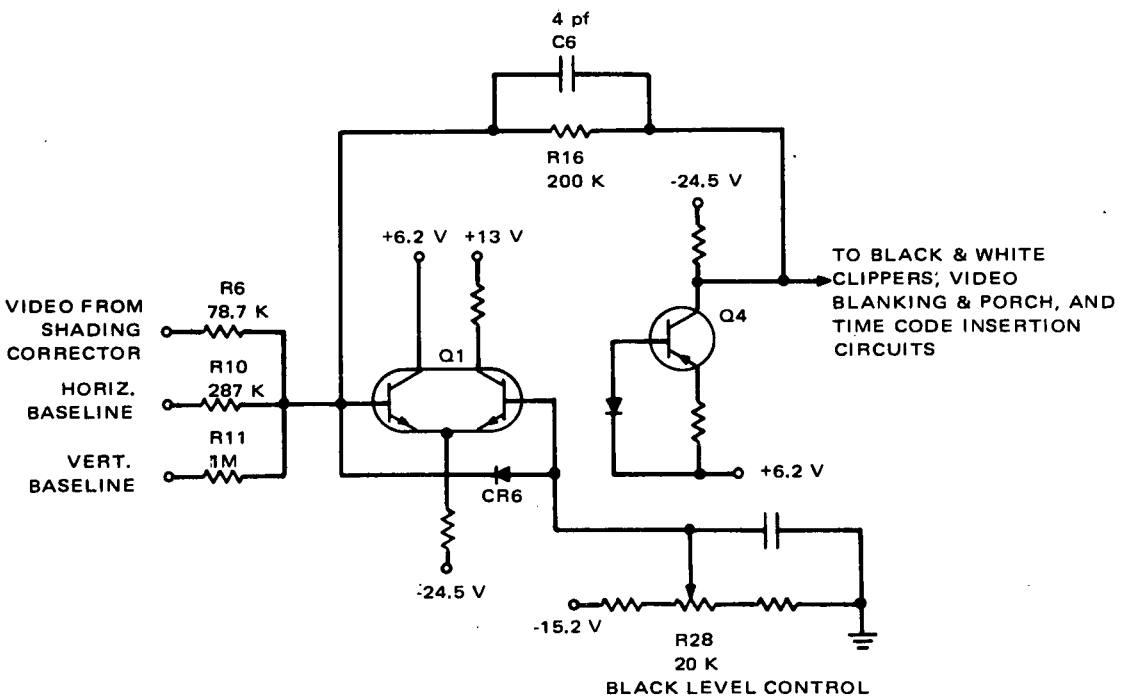


Figure 2-V-25. Amplifier, Schematic Diagram

5. Black and White Clippers, Video Blanking and Porch, and Time Code Insertion

Following the DC amplifier are the clippers, blanking, porch, and time code insertion circuits, as shown on Figure 2-V-26. Resistor R49 is inserted in the input to provide current limiting and isolation for black clipping, porch, and time code insertion.

The black clip control resistor, R49, and the emitter follower transistor, Q8, provide the bias level and low impedance for clipping diode CR15. Positive excursion of video is limited to approximately 0.6 volt more positive than the DC level at emitter of Q8. Temperature drift of the clip level is minimized by the canceling effects of the Q8 V_{BE} and CR15.

The porch level reference is provided by adjustable resistor R30 and complementary PNP-NPN emitter followers, Q2 and Q5. The complementary emitter follower provides a low impedance reference and cancellation of temperature drift of the two transistors.

During the horizontal porch and vertical blanking periods, transistor switch Q10 is turned on by either vertical porch or video blanking pulses. When Q10 saturates, a "hard" DC porch reference is applied to the junction of R49 and R55. Resistor R55 is inserted between R49 and the output stage to provide current limiting and isolation for white clipping and time code insertion.

Low impedance and bias level for white clip diode CR17 is provided by transistor emitter follower Q7 and white clip control resistor R46. Negative excursion of the video is limited to approximately 0.6 volt more negative than the DC level at the emitter of Q7. The canceling effects of Q8 V_{BE} and CR17 minimizes the temperature drift of the clip level.

After the video readout frame, the time code data is inserted into the video when the time code gate pulses TC-1 and TC-2 are applied. The time code gate pulses cause transistors Q10 and Q11 to saturate. The time code data input signal has its amplitude reduced by approximately one-half and is level shifted before the signal is applied to the output emitter followers.

The junction of R49 and R55 is approximately at AC ground; therefore, the time code amplitude is attenuated by the voltage divider effect of R55, R56, R57 and the output impedance of the time base unit.

The level of the time code data is shifted by applying a negative potential to the R55 end of the divider string. During the time code period diode CR9 is biased on, thus switching R31, R33, and -24.5 volts into the base circuit of Q2. The addition of the voltage from R31, R33, and -24.5 volts, generates the required negative shift level at the Q5 emitter.

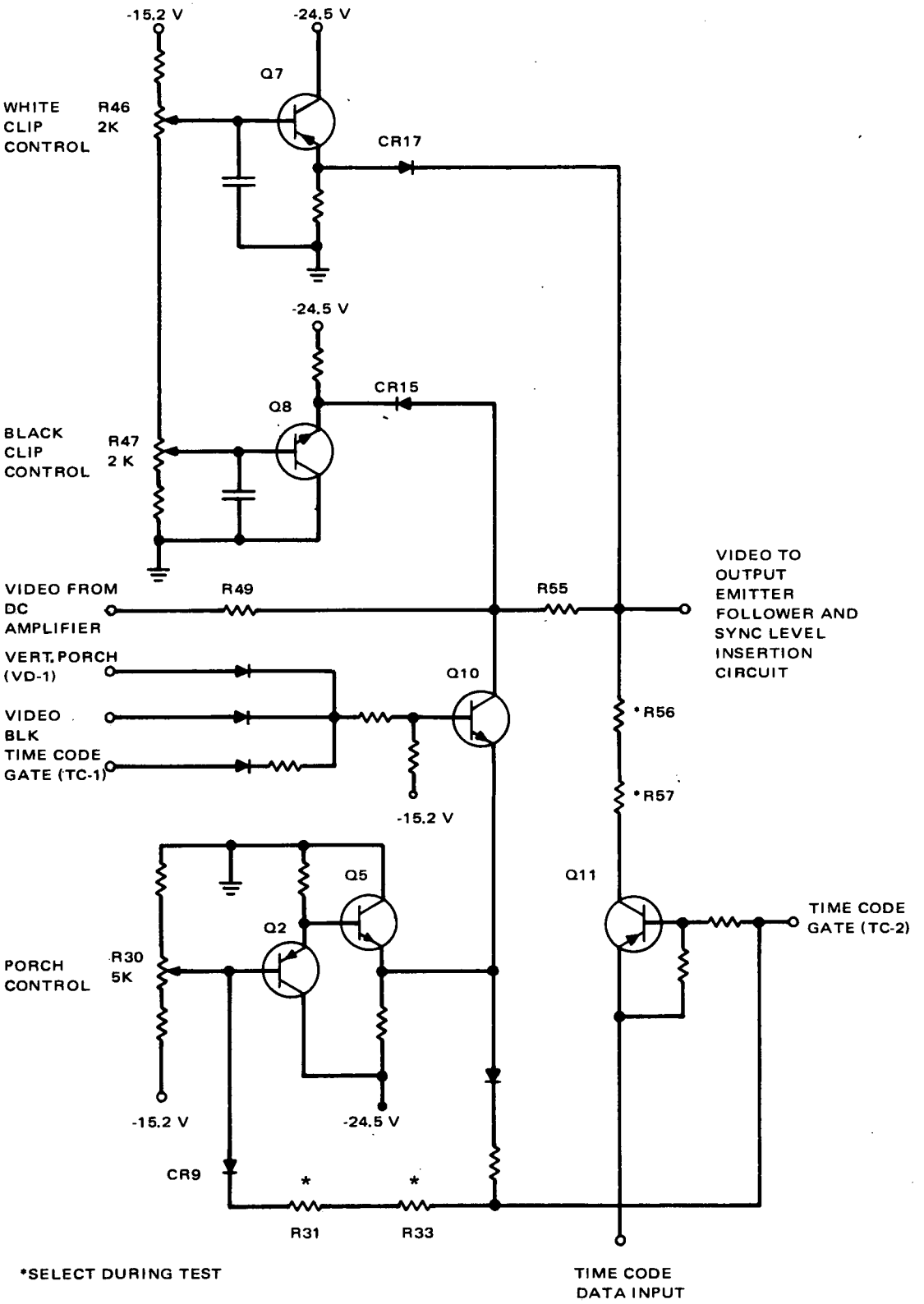


Figure 2-V-26. Black and White Clippers, Video Blanking and Porch, and Time Code Insertion, Schematic Diagram

6. Output Emitter Follower and Sync Insertion

Following the clippers, blanking, porch, and time code insertion circuits, the signal is applied to the complementary emitter follower Q12 and Q15, where the synchronization tip is inserted. This is shown on Figure 2-V-27.

The complementary NPN-PNP emitter follower Q12 and Q15 provides low distortion video output, compensation of all video levels, two video outputs, and short circuit protection.

Two transistor switches Q13 and Q14, located between the two emitter followers, bias the output to the synchronization level. The sync level control resistor, R80, and the emitter follower transistor, Q18, provide the bias and low impedance for the synchronization level. The sync level temperature drift is minimized by V_{BE} cancellation in Q18 and Q15.

The rise and fall times of the synchronous pulse are slowed down by C18, the capacitor feedback from collector to base of Q14. Switch Q13 removes the feedback capacitor loading effect on the output emitter followers during readout and time code.

Two isolated video outputs are provided through R77 and R78. The output isolation resistors, together with R71, protect the camera video output from an accidental shorting. If one of the two outputs was shorted, the second video output would still provide a video signal.

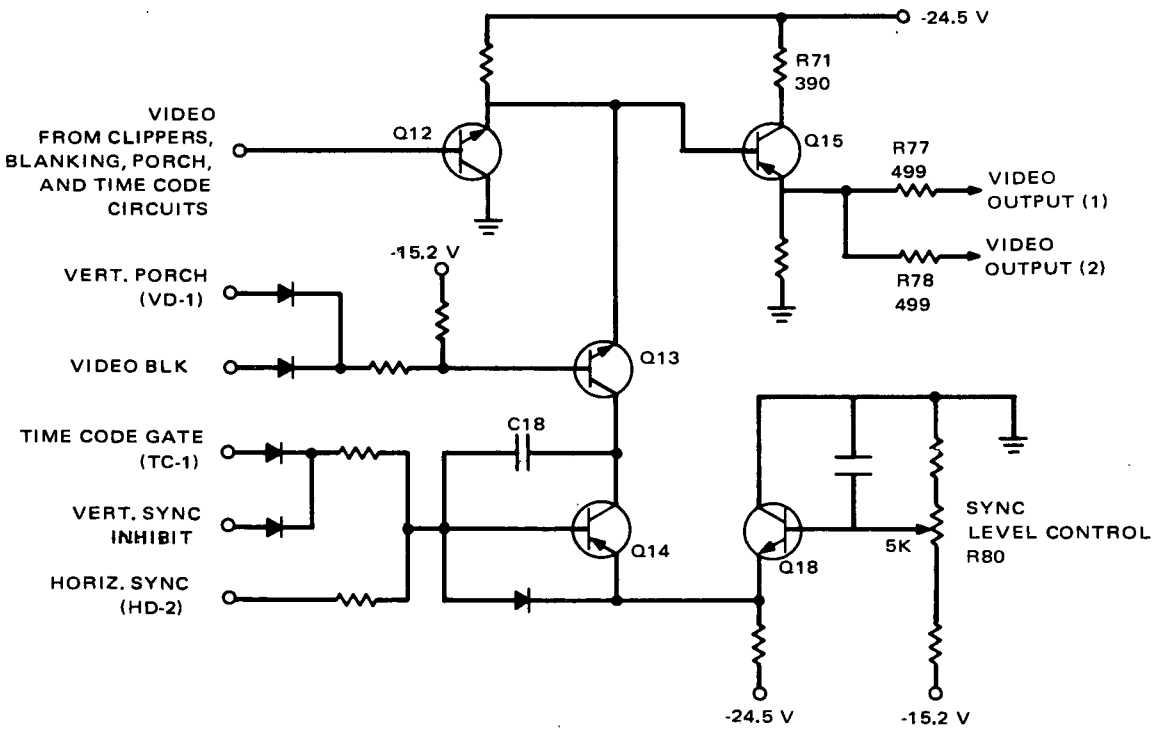


Figure 2-V-27. Output Emitter Follower and Sync Insertion, Schematic Diagram

7. Horizontal Deflection

The horizontal deflection circuit is a Miller integrator type sweep generator with an inverted mode switch, Q12, used to discharge the integration capacitor. Figure 2-V-28 shows the basic configuration.

Sweep circuit operation begins with the inverted mode switch saturated. This causes the entire amplifier output to be fed back to the input of the differential amplifier via Q12 and R19. Input 2 of the amplifier is then forced up to the same level as input 1. Thus the voltage at the position potentiometer, R48, is the same as the voltage at the other input, which is also the same as the voltage at the top of R24, the 499 Ω yoke current sampling resistor.

The sweep begins when Q12 is cut off. Input 2, through R14, tends to go negative, causing the output voltage to rise in an attempt to maintain a constant input voltage at input 2 and results in a constant current through R14. This gives rise to a linear sweep since the capacitor charging current is constant. Sweep stops when the inverted mode switch Q12 is gated ON, discharging the integration capacitor and returning the deflection current to its starting position.

Figure 2-V-29 shows a simplified schematic diagram of the circuit. A dual differential transistor Q8 is used in the first stage to minimize V_{BE} temperature differentials causing changes in either size or centering. To ensure minimum interaction between size and centering controls and maximum common mode

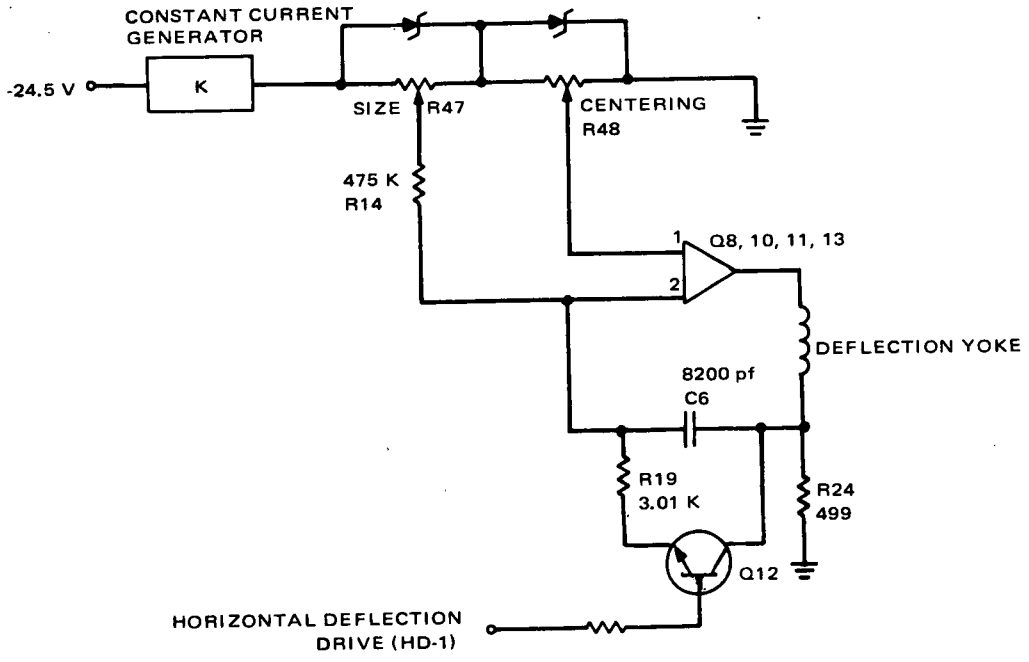


Figure 2-V-28. Horizontal Deflection Circuit, Simplified, Schematic Diagram

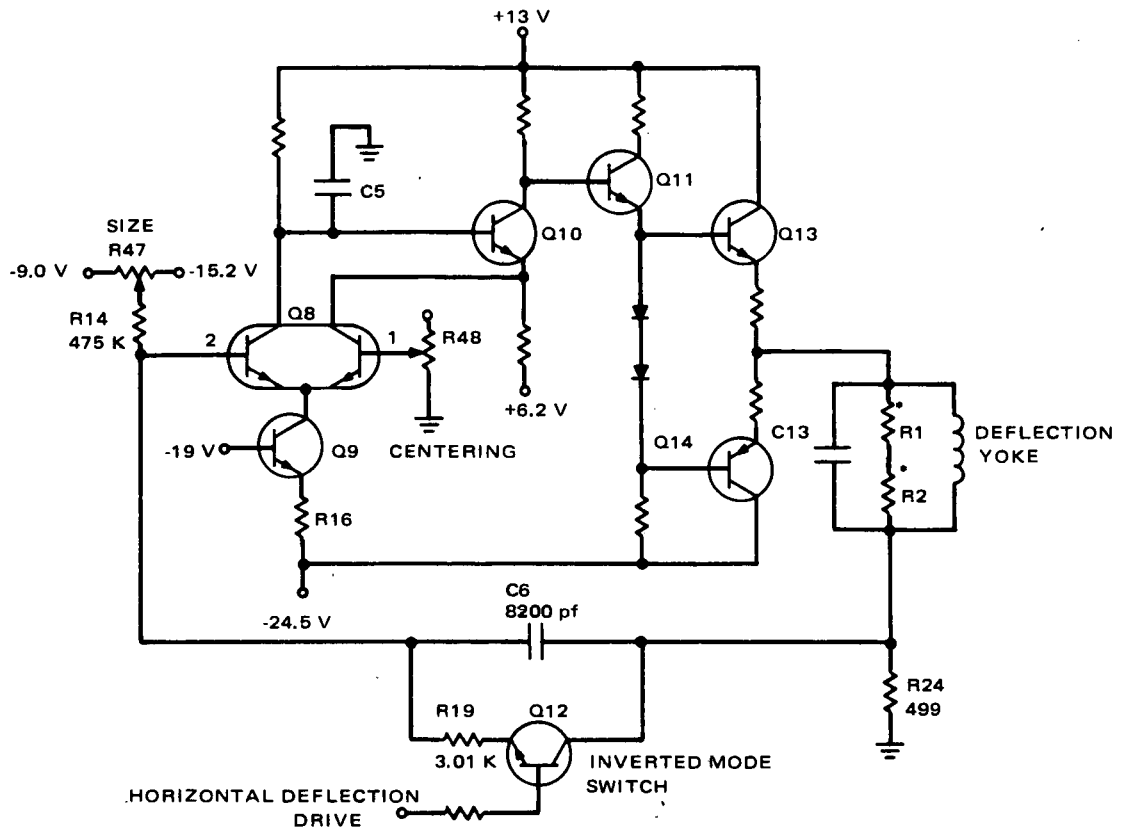


Figure 2-V-29. Horizontal Deflection Generator, Simplified, Schematic Diagram

rejection at the input differential amplifier, a constant current source, Q9 and R16 is connected to the emitters of the differntial input amplifier.

Following the input stage are two common emitter amplifiers, Q10 and Q11, that drive a complementary emitter follower. The emitter followers, Q13 and Q14, provide a low yoke driving impedance for either positive or negative signals.

Capacitor C5 between ground and the collector of the first differential amplifier, rolls off the entire amplifier at about 6 dB per octave to ensure a stable DC amplifier configuration.

Deflection yoke damping is accomplished with resistors, R1 and R2, placed across the yoke. Resistor R1 has a positive temperature coefficient to match the deflection yoke resistance and resistor R2 has a zero temperature coefficient. The resistance combination of R1 and R2 was selected to match the change in yoke sensitivity due to temperature. Capacitor C13 is placed across the yoke-winding to compensate for the yoke-winding stray capacitance to ground.

To ensure a stable reference supply for both the size and centering circuits, a constant current generator is used to drive two zener reference diodes. Figure 2-V-30 shows a simplified schematic of this circuit. The current through the

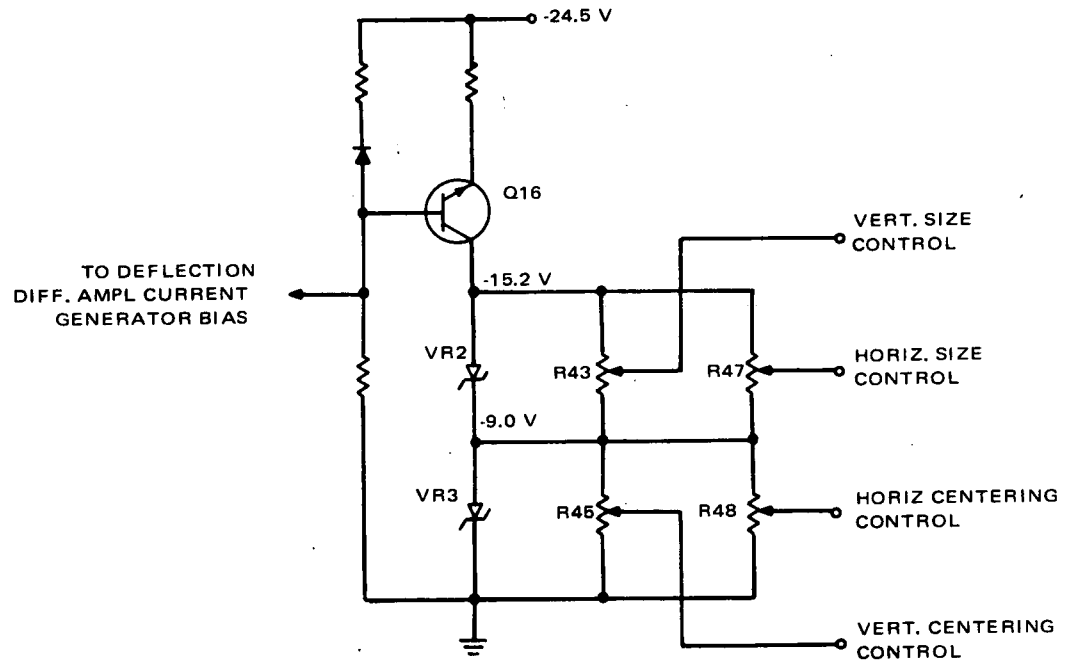


Figure 2-V-30. Constant Current Generator, Schematic Diagram

zener diodes VR2 and VR3 is thus maintained within the regulation of the -24.5-volt supply. This generator configuration maintains a more uniform reference current than a single resistor connected from the -24.5-volt supply to the zener diodes, when the wide range of zener voltages is considered.

8. Vertical Deflection

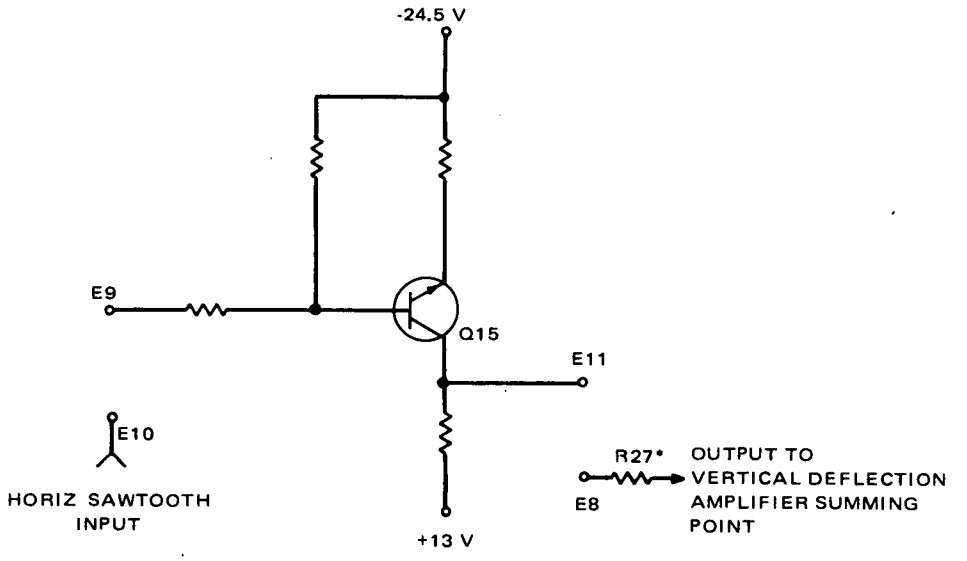
This deflection generator contains the same amplifier as the horizontal deflection generator. The values of the integration capacitor and constant current resistor are changed to obtain slower sweeps. Reference voltages are taken from the same zener diodes as for the horizontal circuit.

9. Yoke Skew Corrector

The deflection circuit board includes a circuit that permits the introduction of a small sample of horizontal deflection sawtooth to the vertical deflection circuit. This circuit is shown in Figure 2-V-31. A common emitter amplifier Q15 is provided to allow for horizontal sawtooth signal inversion.

10. Main Converter

A simplified schematic diagram of the main converter is shown in Figure 2-V-32. Main power (-24.5 volts) is applied to the DC-to-DC converter



NOTE: HORIZ. SAWTOOTH INPUT SIGNAL MAY BE CONNECTED TO E9 AND E11 (Q15 COLLECTOR) CONNECTED TO E8; OR E10 MAY BE CONNECTED DIRECTLY TO OUTPUT (E8), DEPENDING UPON PHASE OF SAWTOOTH DESIRED.

*SELECTED DURING TEST

Figure 2-V-31. Yoke Skew Corrector, Schematic Diagram

via the main power switching circuit. A low pass LC filter in series with this supply, buffers the converter chopper transistors, Q1 and Q2, from the system.

A nonsaturating transformer, T1, is used to couple the chopper transistor output. The secondary of this transformer is coupled to each converter transistor base via a small saturating transformer, T3. This transformer controls the main switching frequency and provides the flattop base drive characteristic desired for the converter transistors. Small speedup capacitors, C9 and C10, are placed across the base-drive current limiting resistors. These capacitors minimize the transistor switching time and thus reduce the dissipation of the transistors.

Four secondary windings on T1 supply the vidicon and the +13-volt regulator voltages. Secondary winding 7-8 couples to a half-wave voltage doubler that supplies the positive high voltages for G3/G6 and G2 of the vidicon. Secondary winding 9-10 drives a full wave bridge rectifier that supplies negative voltage to the vidicon beam current regulator. Two remaining windings supply the voltages to the +13 volt regulator. Winding 11-13 supplies the square wave signal for the saturating base drive transformer T3.

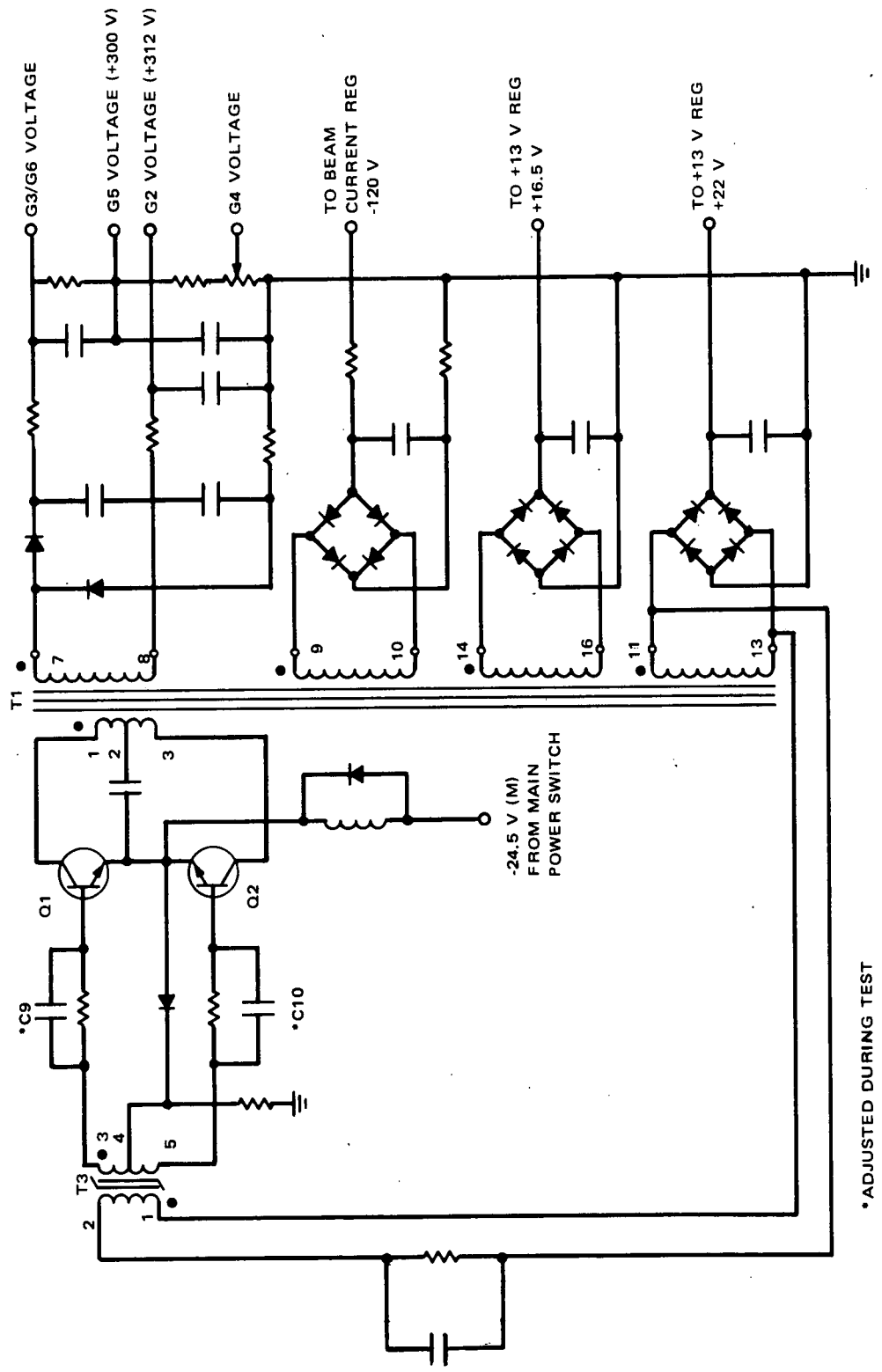


Figure 2-V-32. Main Converter, Simplified Schematic

11. Filament DC-to-DC Converter

The schematic diagram of the filament converter is shown on Figure 2-V-33. Standby power via the low pass filter is applied to the filament DC-to-DC converter. Saturating transformer T2 controls the switching frequency and provides the required drive for the converter switching transistors Q3 and Q4. Speedup capacitors C11 and C12 shunt the base drive current limiting resistors, minimize the transistor switching times, and thus increase the converter efficiency.

The secondary winding drives a full wave rectifier bridge that supplies the filament voltage through a low pass LC filter.

12. +13-Volt Regulator

As shown on the schematic of the +13-volt regulator (Figure 2-V-34), a balanced dual differential transistor circuit, Q6, is used to sample the supply voltage and compare this sample with a reference diode, VR2. A single transistor, constant current supply, Q13, is used on one output of the differential amplifier to drive the Darlington series regulator transistor configuration (Q10 and Q12). This configuration provides high amplifier gain by maintaining a minimum load for the differential amplifier collector without the use of inordinately low collector load resistors for the output stage.

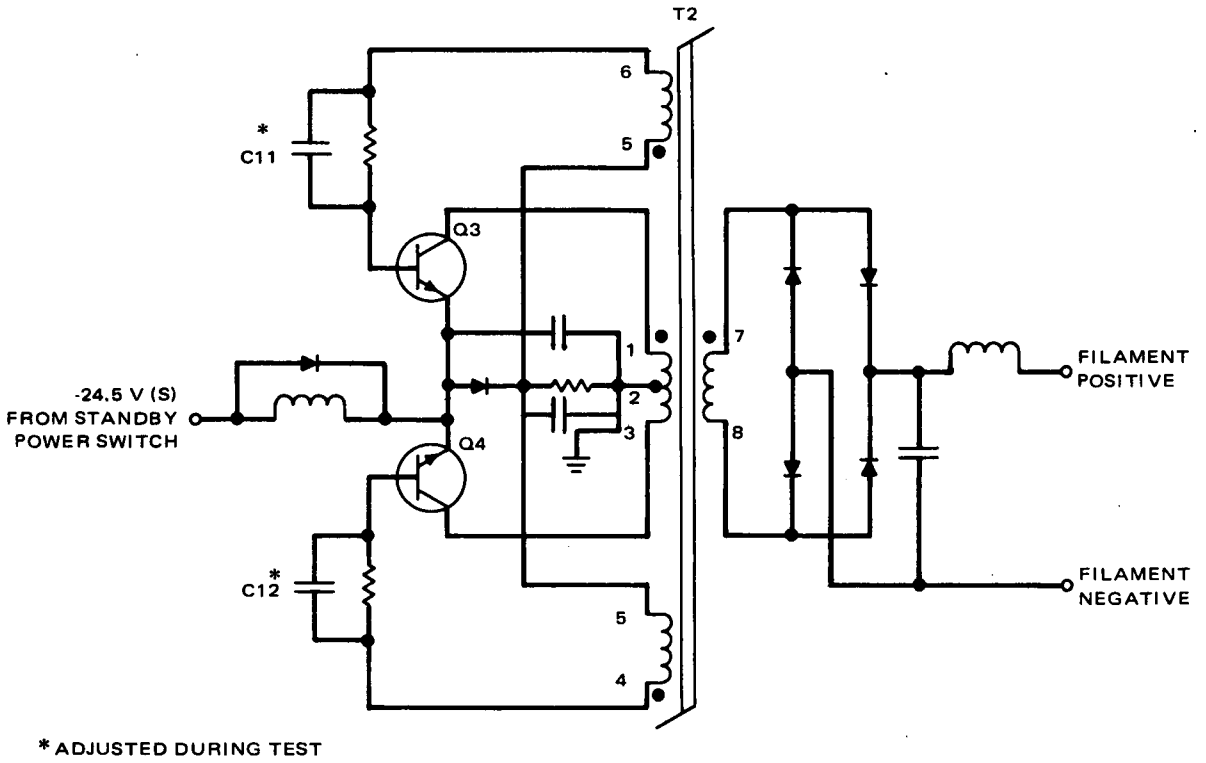


Figure 2-V-33. Filament DC-to-DC Converter, Schematic Diagram

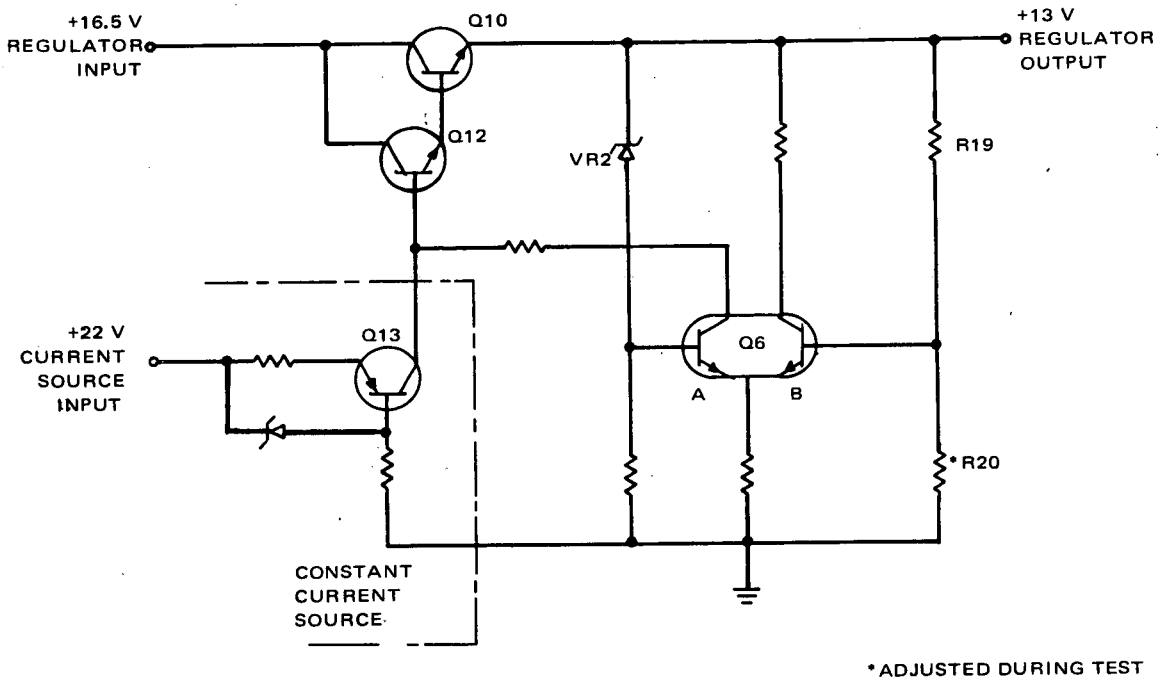


Figure 2-V-34. +13-Volt Regulator, Schematic Diagram

Regulator operation may be best explained by considering the regulator in terms of a feedback amplifier that maintains the voltage differential across the bases of the input amplifier near zero, and thus opposes any tendency for the load or line changes to upset the balance.

Initially the voltage drop across both sides of the differential amplifier are equal and the zener voltage equals the voltage drop across R19. A voltage drop on the +13-volt output bus will be reflected as a voltage decrease across both R19 and R20. Since the zener voltage on the A side is fixed, the voltage drop on the B side results in an increase in the base-to-emitter voltage on the B side, causing the collector voltage at the A side to increase. This increase is reflected directly as an increase in output voltage. Overall amplifier open-loop gain is greater than 1000 to ensure more than adequate regulation for all expected line and load variations.

13. Beam Current Regulator

The vidicon beam current regulator maintains constant vidicon beam current by maintaining constant cathode current. This assumes the ratio of cathode current to beam current is constant, which is reasonably accurate for a given set of vidicon electrode voltages and a given vidicon geometry. The vidicon cathode blanking circuit is included in the regulator circuit.

Figure 2-V-35 shows a partial schematic diagram of the regulator and cathode blanking circuits. The vidicon beam is blanked by grounding the vidicon cathode. The nominal cathode current is given by (120 -24.5) volts/R70. This assumes no base current to Q24 and that Q23 is cut off.

Regulation is maintained by varying vidicon G1 potential to hold the cathode at a constant potential, set at the base of Q24 via the V_{BE} drops of Q24 and Q25. Essentially the beam current regulator is only a voltage regulator in that it maintains the potential at the vidicon cathode at -24.5 volts. Once this is accomplished, the cathode current is a function of the variables shown previously.

Diode CR17 clamps at the diode side of R74 when Q23 is saturated. Diodes CR15 and CR16 protect their respective base-to-emitter junctions. Resistor R76, in the collector circuit of Q25, protects the transistor from high peak currents. Capacitor C30 resistor R77, in Q25 circuit, reduce the switching ripple during horizontal blanking.

14. Main Power Switch

The main power switch is a solid-state switch, with overvoltage and turn-on transient provisions. This switch is turned on or off by command and supplies -24.5 volts from the spacecraft power supply to the entire AVCS, except the vidicon filament.

A schematic diagram of the main power switch is shown on Figure 2-V-36. An "ON" command applies +4.4 volts to the emitter of Q8 and an "OFF" command applies 0 volt to the same point. When the ON command is given, Q8 is turned on, which causes Q11 to become saturated, and this, in turn, causes Q9 (the main power switching transistor) to saturate. This then switches the spacecraft power to the AVCS. The rate of rise of the turn-on surge current is controlled by the resistance-capacitance network (R46, R45, and C4) between Q8 and Q11.

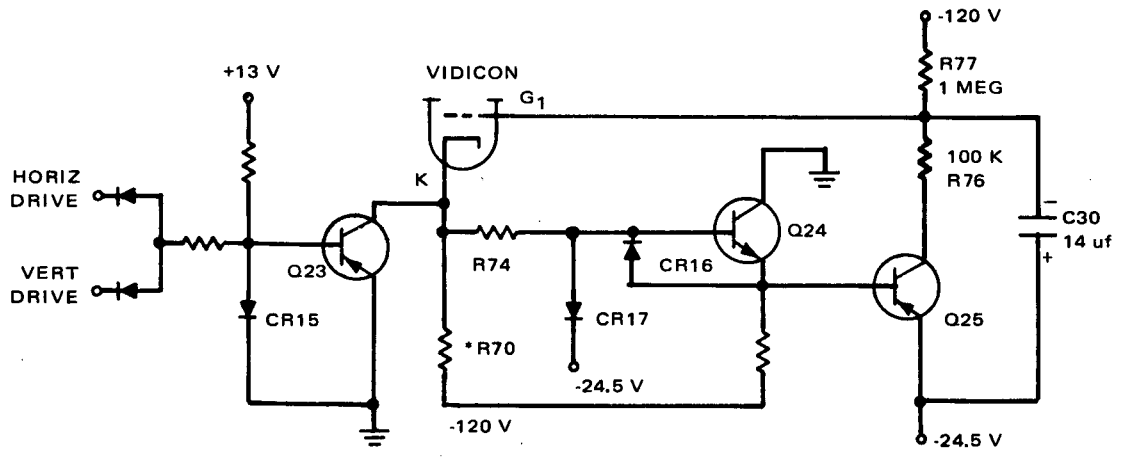


Figure 2-V-35. Beam Current Regulator, Schematic Diagram

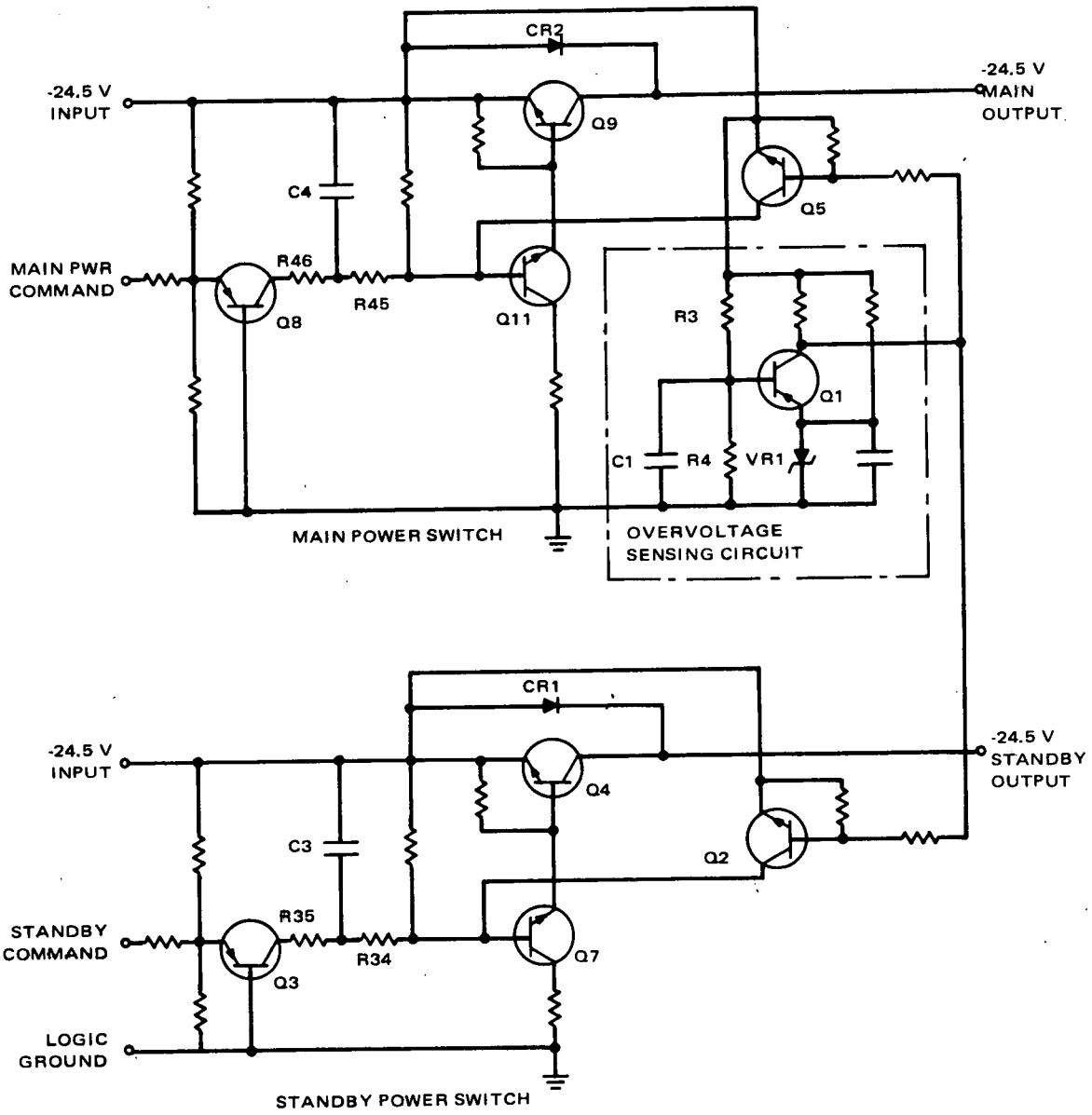


Figure 2-V-36. Main and Standby Power Switches, Schematic Diagram

The overvoltage protection section of the power switch consists of an overvoltage sensing stage Q1 and a protection switch Q5.

The voltage at the junction of R3 and R4 is compared with the zener voltage of VR1, and the difference voltage is applied to Q1 emitter base. When the input voltage exceeds a certain threshold voltage, Q1 saturates and in turn saturates Q5. The turned-on Q5 will "short" the base drive from transistor Q11 which removes the base drive from the main power switch Q9, thus removing power from the AVCS.

A low pass filter, which consists of capacitor C1 and resistors R3 and R4, keeps the overvoltage sensing circuit from reacting to overvoltage transients on the input power line.

Diode CR2 protects the power switch transistor Q9 during switching of spacecraft regulators.

15. Standby Power Switch

Figure 2-V-36 also shows the standby power switch circuit. An external command controls the application of the spacecraft power to the AVCS vidicon filament. The overvoltage protective circuit is common to both the main and standby power and thereby protects the filament from overvoltage. Surge protection is provided by the network provided by R34, R35 and C3.

The standby power switch circuit functions identically to the main power switch except that turn-on time constant and transistor base drive resistors have been modified for the filament load current.

16. Shutter Drive

The shutter drive circuit contains two identical shutter drive channels accepting shutter command pulses at their inputs and delivering corresponding shutter solenoid excitations at their outputs.

As shown on Figure 2-V-37, the shutter drive consists of two electronic switches and a solenoid drive circuit. The shutter 1 solenoid switch consists of Q29 through Q32 and the solenoid 2 switch consists of Q33 through Q36. The common solenoid drive consists of Q25 through Q28. Timing of the shutter open and close commands is furnished by the spacecraft programmer subsystem.

When a shutter open command voltage is applied to the bases Q29 and Q25, switch Q29 through Q32 is effectively closed between the emitter of Q28 and the shutter 1 solenoid. At the same time, the shutter drive circuit one-shot (Q25 through Q28) is activated and supplies power to energize the shutter 1 solenoid, through the closed switch. These circuits remain energized until the shutter close command is applied to Q33. The interval between these commands is approximately 20 milliseconds.

When the shutter close command is applied to Q33 and Q25, the switch (Q33 through Q36) closes between the emitter of Q28 and shutter 2 solenoid. The solenoid drive one-shot is again activated, energizing the shutter 2 solenoid.

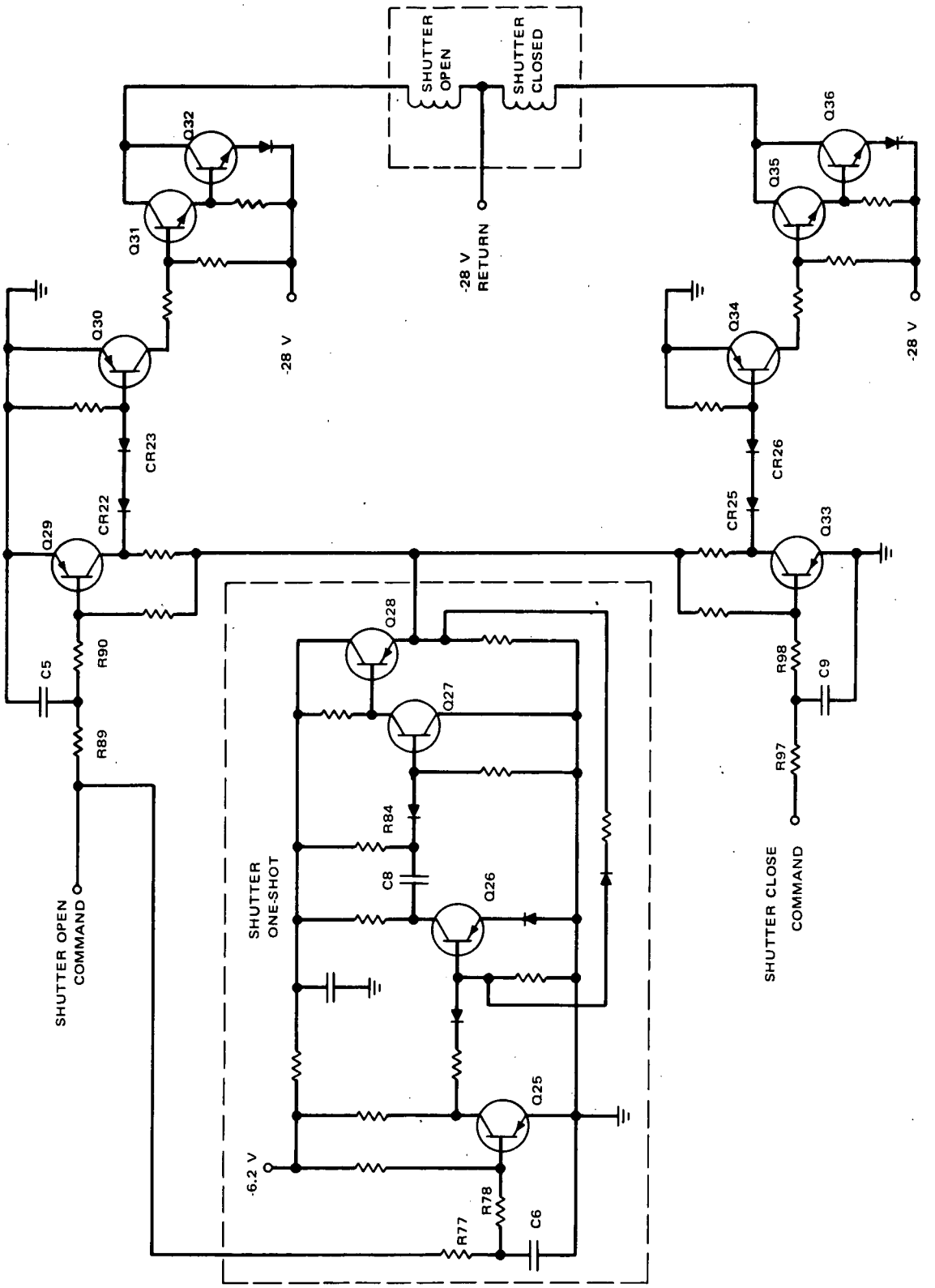


Figure 2-V-37. Shutter Drive, Schematic Diagram

A spring release mechanism then causes shutter 1 solenoid to drop out and at the expiration of the shutter close command pulse, shutter 2 solenoid drops out.

The sequence of operation of the shutters is shown on Figure 2-V-3 and is explained in Paragraph 2.V.B.2.

The two solenoid drive circuit inputs and the shutter one-shot input have low pass RC networks which provide noise filtering. They are comprised of R89, R90, and C5 on the open command input; R97, R98, and C9 on the close command input; and R77, R78, and C6 on the one-shot input.

The shutter one-shot circuit consists of trigger inverter stage Q25, a one-shot circuit, Q26 and Q27, and buffer stage Q28. The one-shot period of approximately 150 milliseconds is determined by resistor R84 and capacitor C8.

17. Command Buffers

The command buffers used in the camera subsystem are shown on Figure 2-V-38. The characteristics of the command signals are as follows: +4.4 volts for a "command pulse" and 0 volt for a "no command pulse". The input stages on all the command buffers are similar in configuration to provide the maximum spurious noise immunity and the required load impedance.

The following diodes, which are located in emitter circuits, provide an increase in the turn-on threshold voltages of their respective transistors:

- View a, diode CR3 in Q3 circuit,
- View c, diode CR5 in Q5 circuit,
- View d, diode CR5 in Q7 circuit, and
- View f, diode CR11 in Q13 circuit.

Transistor base-to-emitter junctions are protected by the following diodes:

- View b, diode CR10 in Q10 circuit,
- View c, diode CR4 in Q4 circuit, and
- View e, diode CR12 in Q16 circuit.

The video blanking buffer, view c, is inhibited during the time code period by applying TC-1 via CR6 to the base of Q4.

18. Gray Scale Calibrator Regulator

A schematic diagram of the gray scale calibrator is shown on Figure 2-V-39. The series switch transistor, Q23, controls the application of the supply voltage to the regulator. When both calibrator enable pulses are present, transistor Q24 saturates, thus driving Q23 into saturation and applying -28 volts to the input of the regulator.

Sampling the output voltage and comparing it with a fixed reference (R70) is performed by a dual differential transistor Q21. The error signal from the differential amplifier stage drives the complementary pass transistors Q19 and Q20.

The reference voltage is obtained by supplying constant current to zener diode VR4 for transistor Q22.

19. Telemetry

The standby telemetry is obtained from the voltage divider shown in Figure 2-V-40(a). When standby power is on, the output will be -4.5 ±0.2 volts. If standby power were to fail, the telemetry would be 0 volt.

Figure 2-V-40(b) shows the voltage divider string that provides the -24.5-(M) and +13-volt telemetry. With the main power on and the +13-volt regulator functioning properly, the telemetry output will be -1.8 ±0.2 volts. If the main power were to fail, the output will be 0 volt. With the main power on, but 0 volt on the +13-volt regulator output, the telemetry output will be -3.6 ±0.3 volts.

The circuit for the filament current telemetry is shown in Figure 2-V-40(c). Resistor R52 samples the filament current and provides a difference voltage across the two bases of the differential amplifier Q14. This difference voltage sets the collector current flowing from Q14a, thus setting the telemetry voltage which appears across resistor R50. When the filament is drawing nominal current, the telemetry output will be -2.2 volts. The telemetry will be -4.25 ±0.3 volts if the filament opens.

b. AVCS TAPE RECORDER

(1) GENERAL DESCRIPTION

The AVCS tape recorder is a one-speed recorder which is used to record data from the camera subsystem. The record and playback speed is 30 inches per second, and the recorder has 1360 feet of 1/4-inch width usable magnetic tape.

Each of the two redundant AVCS recorders is composed of two units. The transport contains the tape transport and the playback preamplifier within a pressurized enclosure. The electronics unit contains the motor drive circuits and the record/playback signal electronics.

The functions of the recorder are:

- To record, playback, and erase signals supplied by the spacecraft,
- To provide telemetry signals to the beacon and transmitter subsystem, and
- To provide internal control and switching for the above functions from commands supplied by the spacecraft command subsystem.

The principal elements of the AVCS tape recorder are shown in Figures 2-V-41 and 2-V-42. The analog signals supplied by the camera subsystems frequency modulate a subcarrier before being recorded, and all playback signals are amplified and amplitude-limited. Playback and signal transmission occurs in a direction opposite from that used in recording.

Of the three data-recording channels in each tape recorder, channels 1 and 3 are used for recording and playing back camera video (from cameras 1 and 2, respectively) and picture time code. Channel 2 records a constant 50-kHz tone which is used by the ground station processing equipment to detect tape recorder speed variations and to compensate for these variations in the received video.

The record and playback electronics are powered by the spacecraft -24.5-volt DC regulated bus. Power is applied to the appropriate record and/or playback electronics through power switches that are actuated by spacecraft commands. The motor-drive circuit is powered from a separate -24.5-volt bus, and is synchronized by a stable 400-Hz signal from the command subsystem.

AVCS tape recorder characteristics are summarized in Table 2-V-3.

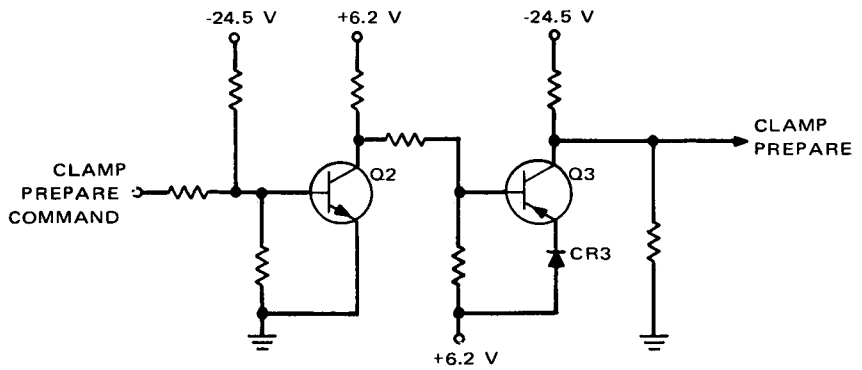
Table 2-V-4 contains pertinent information on tape recorder signals.

The tape transport is mounted in an enclosure which is hermetically sealed and pressurized, and the electronics container consists of a sheet metal frame with printed circuit boards. Multipin connectors provide signal outlet to the tape transport and other spacecraft systems. The recorder is designed to operate over the temperature range from -10° to +45° C for a period of one year.

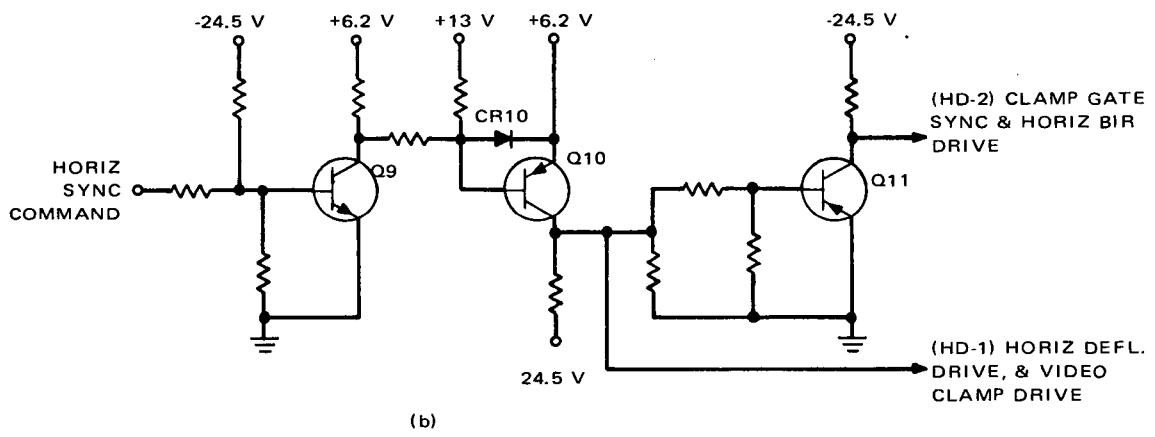
(a) Interface Signals

The tape recorder interface signals are described in Table 2-V-5.

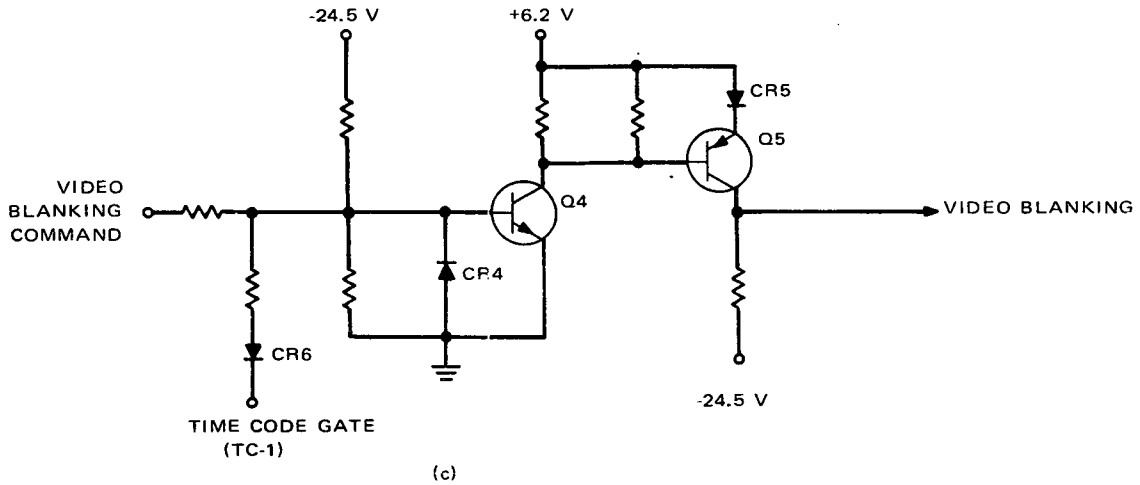
The succeeding paragraphs describe in more detail the tape transport, motor drive circuit, video record and playback circuits, and the flutter-and-wow record and playback circuits, in that order.



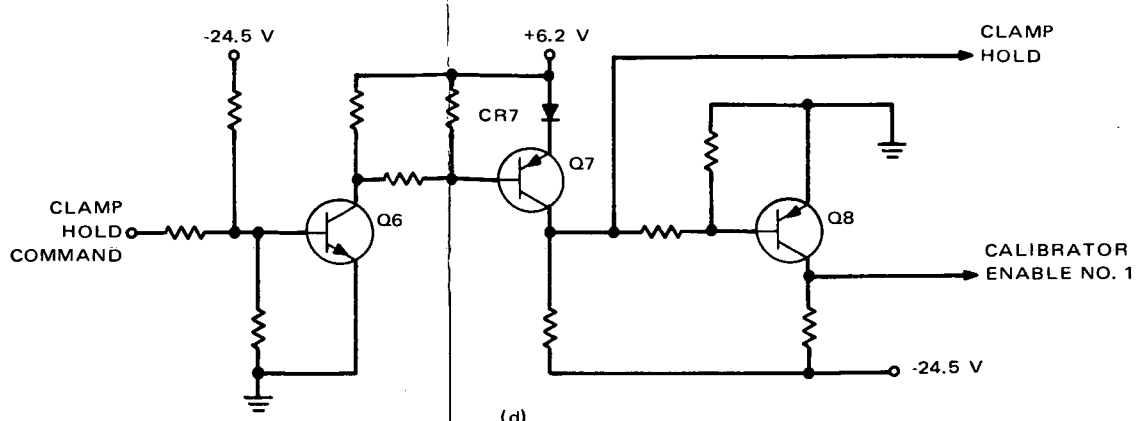
(a)



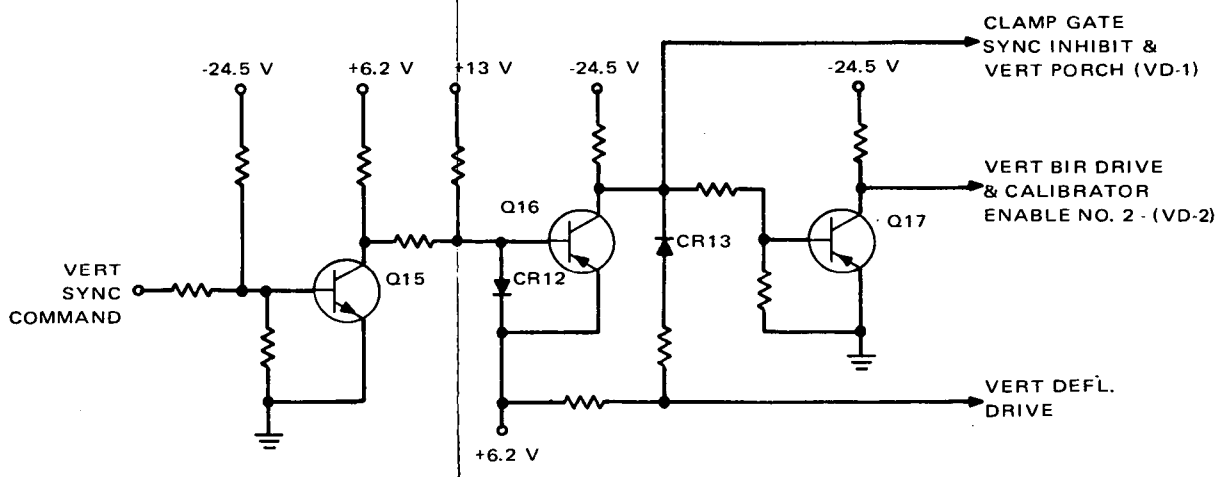
(b)



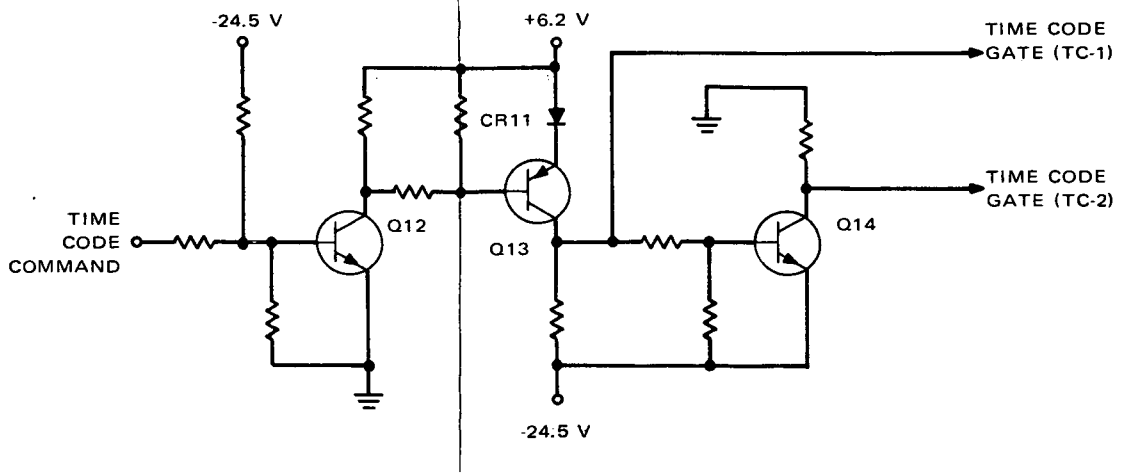
(c)



(d)



(e)



(f)

Figure 2-V-38. Command Buffers, Schematic Diagram

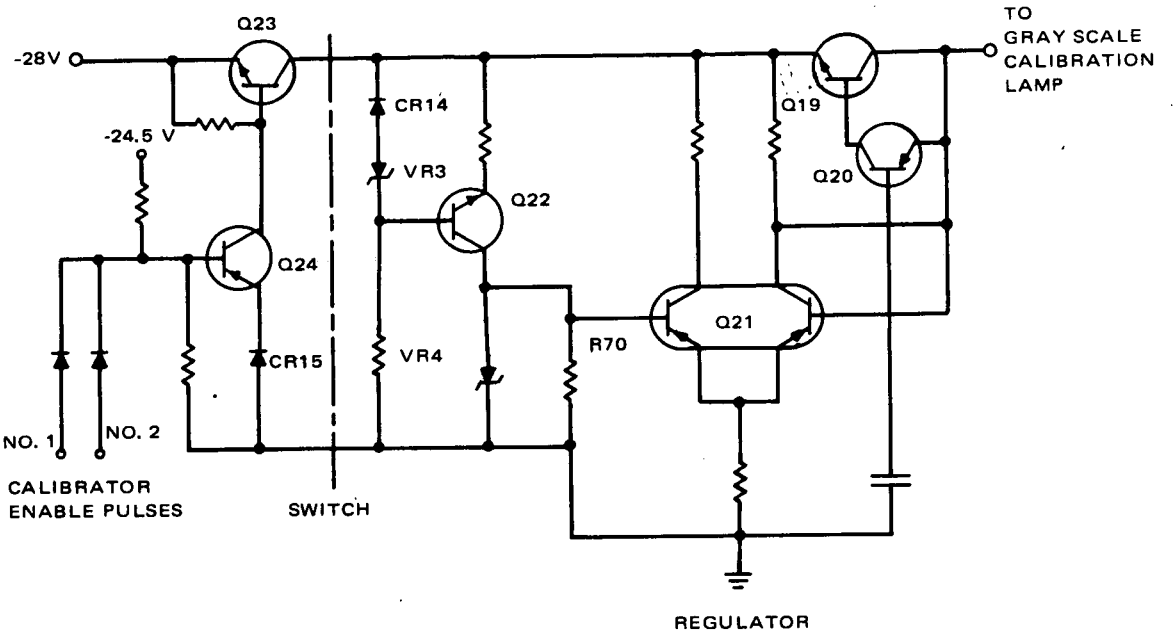


Figure 2-V-39. Gray Scale Calibrator Regulator, Schematic Diagram

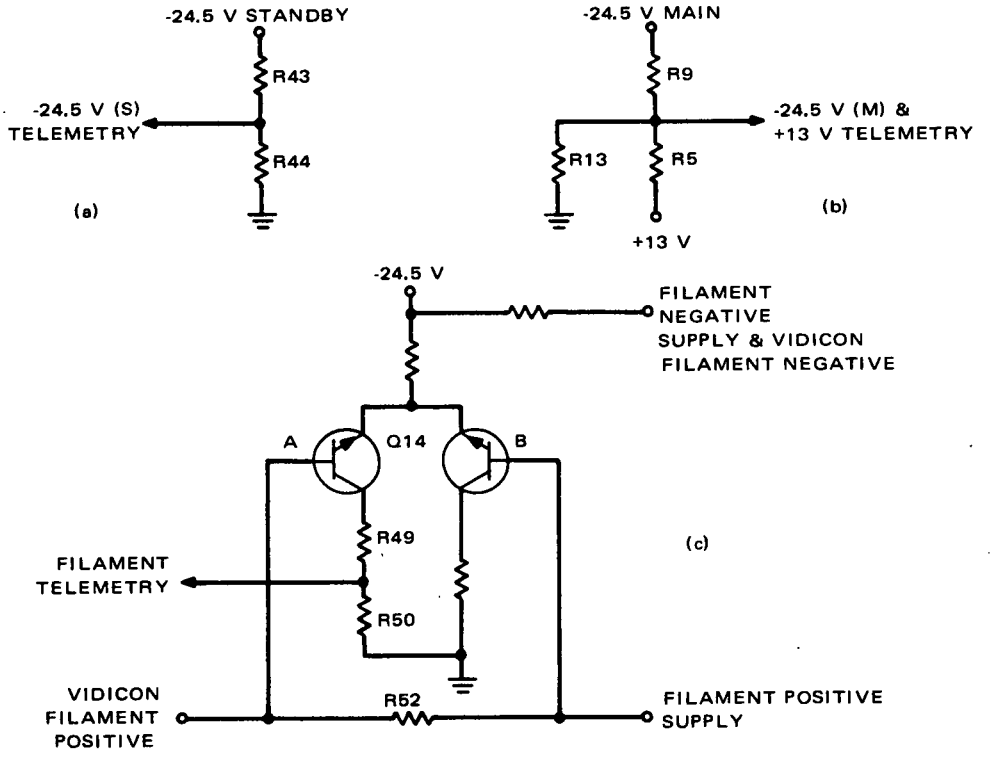


Figure 2-V-40. Standby Telemetry, Schematic Diagram

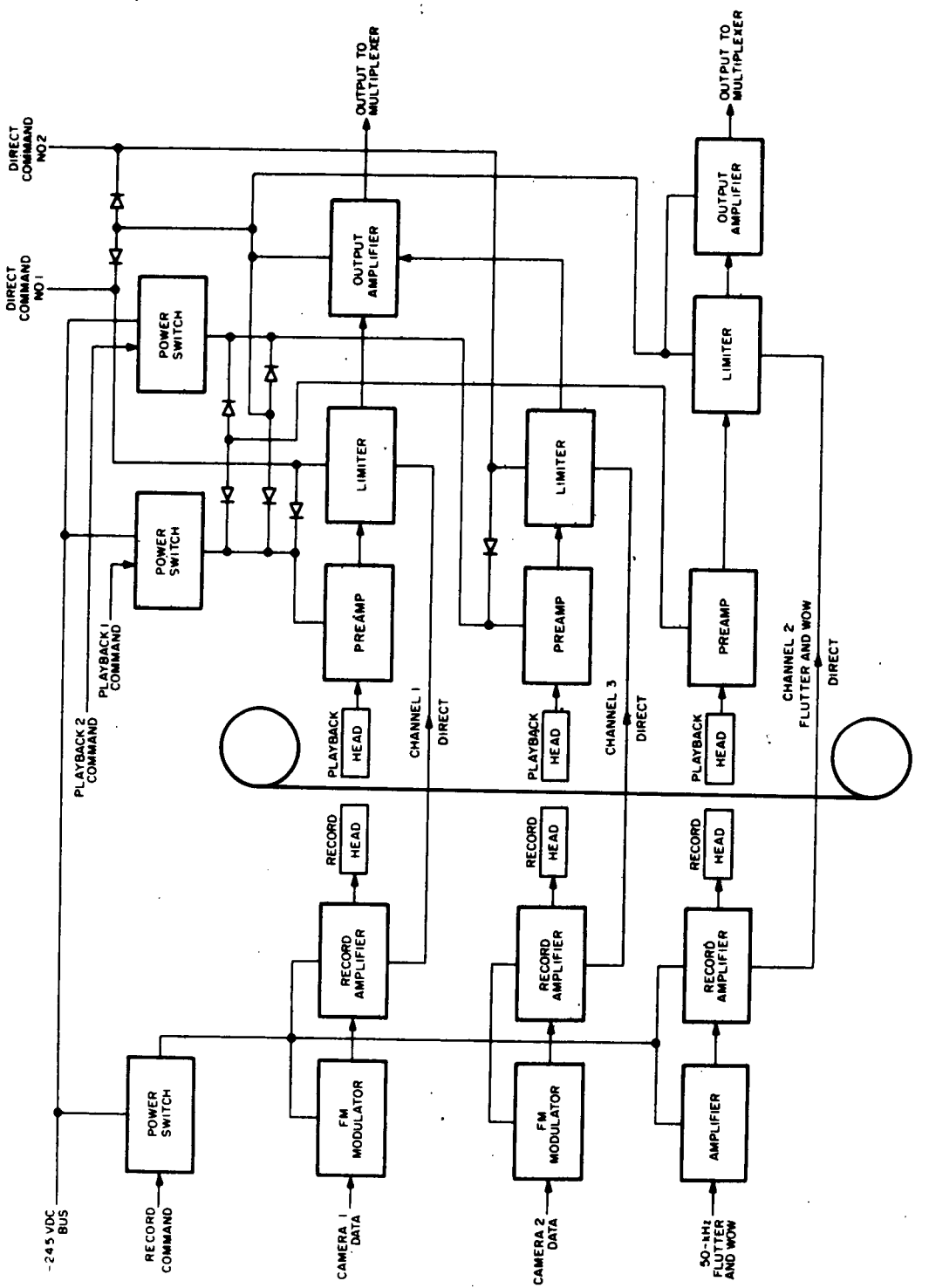


Figure 2-V-41. AVCS Tape Recorder/Playback Electronics, Block Diagram

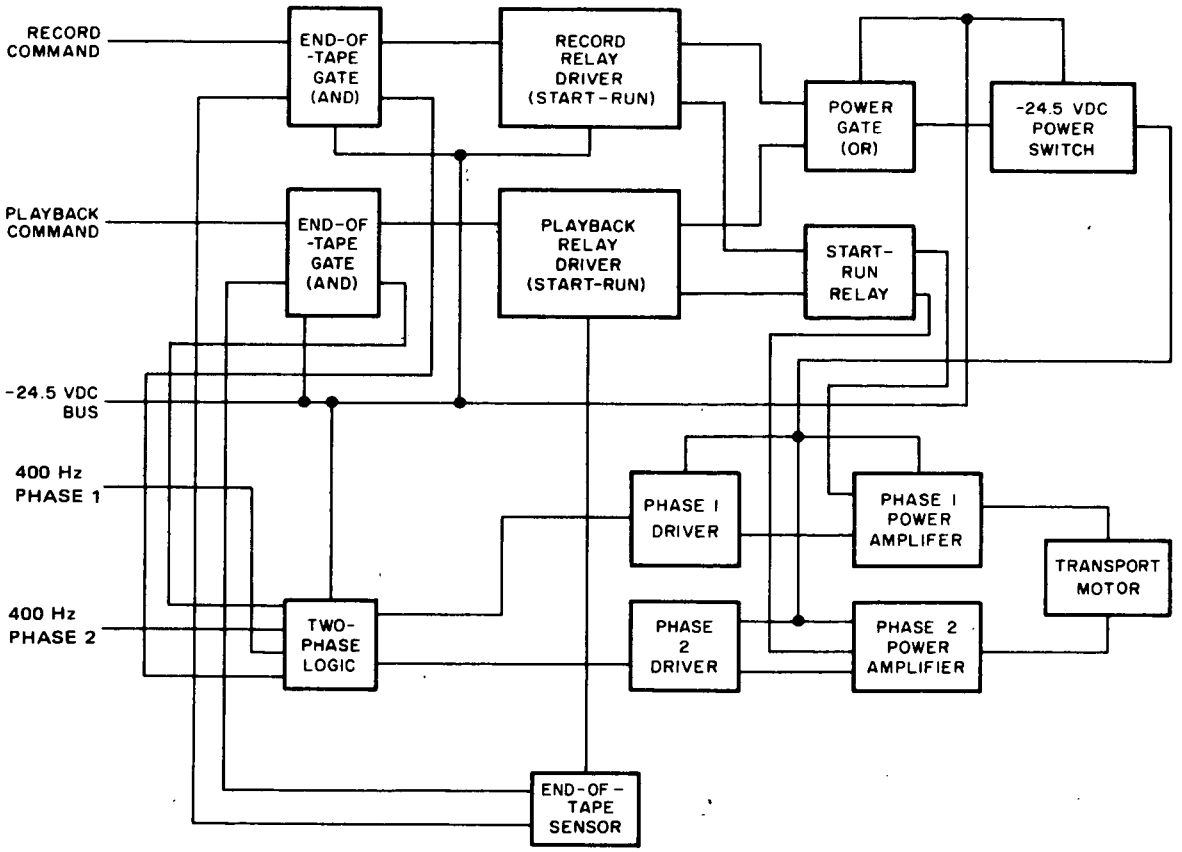


Figure 2-V-42. AVCS Tape Recorder Drive and Control, Block Diagram

(b) Tape Transport Assembly

The tape transport assembly consists of a base casting on which the following are mounted: two coaxial reels, a capstan, record head, playback head, erase head, three tape rollers, flywheel, and negator spring assembly. A constant torque is applied to each of the two tape reels by negator springs to provide constant tape tension. As the tape unwinds from one reel, it makes a 180-degree wrap around the capstan, passes over three rollers, and then loops around the capstan again for 180 degrees, and in the opposite direction, before it is taken up by the second reel. The closed loop formed with respect to the capstan reduces flutter, since any transient changes in tape tension produce essentially equal and opposing torques at the capstan. The slight twist required to move the tape from the plane of one reel to the plane of the other is imparted by the rollers.

The tape is 1/4-inch wide, 1360 feet long, instrumentation grade magnetic tape. The tape is wound and threaded so that the oxide-coated side does not contact any part of the transport except the magnetic heads. The record and playback heads contain three tracks each. The erase head is a single permanent magnet, spanning the full width of the tape, which removes the previous

TABLE 2-V-3. AVCS TAPE RECORDER CHARACTERISTICS

Item	Characteristics
Tape Speed, Record or Playback	30 inches per second
Record Time or Playback Time	9.1 minutes maximum (end-to-end)
Heads	One 3-channel record head; one 3-channel playback head; one permanent magnet erase head, full tape width
Tape	1360 feet of 0.25-inch wide, 0.0011-inch thick, mylar base, instrumentation magnet tape
Pressurization	16.5 psia with 90-percent air (rel. humid. ≅35 percent) and 10-percent helium
Seal	O-ring, sealed flange, and pressure fitting
Weight	
Transport	13.6 pounds
Electronics	4.5 pounds
Dimensions	
Transport	15.4 inches maximum diameter by 7 inches in height
Electronics	8-1/2 by 4-3/8 by 4-1/8 inches
Motor	2-phase, reversible
Speed	12,000 rpm
Operating Voltage	48 volts p-p, 400-Hz square wave
Supply Voltage	-24.5 volts DC
Power Consumption (tape transport and electronics)	
Standby	0.9 W (37 mA)
Record	18.4 W (750 mA)
Playback	15.9 W (650 mA)
Start Mode	61.0 W (2,500 mA)

TABLE 2-V-3. AVCS TAPE RECORDER CHARACTERISTICS
(Continued)

Item	Characteristics
Input Signals	
Video Channel	Camera video ranging in amplitude from -6.5 ±0.2 volts DC (horiz sync tip) to -11.25 ±0.2 volts DC (white level) at a baseband of 0 to 60 kHz; and time code with a pulse amplitude from -8.5 to -10.75 volts.
Flutter-and-Wow Channel	50-kHz square wave, 4.4 ±0.6 volts in amplitude.
Output Signals	
Video Channel	Amplitude limited FM subcarrier ranging in frequency from 72 to 120 kHz at an amplitude of 2 volts ±1 dB p-p.
Flutter-and-Wow Channel	50-kHz square wave, 2 volts ±1 dB p-p.
Telemetry	
Transport Pressure	-0.5 to -4.5 volts
Transport Temperature	-0.5 to -4.5 volts
Line Current	-0.5 to -4.5 volts

TABLE 2-V-4. AVCS TAPE RECORDER SIGNAL DATA

Item	Baseband	Subcarrier ± Deviations	FM Spectrum
F&W Record		50 kHz	
F&W Playback	DC to 5 kHz	50 kHz	
Record and Playback	DC to 60 kHz	96 ±24 kHz	12 to 180 kHz
Sync Tip -6.50 White Level -11.50 volts		Data Inputs	
Demodulated Baseband Signal-to-Noise (p-p to rms)		35 dB minimum	

TABLE 2-V-5. AVCS TAPE RECORDER AND SPACECRAFT INTERFACE SIGNALS

Signal	Description
Power Bus 1 (-24.5 VDC regulated)	This voltage is present whenever the tape recorder is in the record, playback, or standby mode. Power for the signal processing circuits is drawn from this line.
Power Bus 2 (-24.5 VDC regulated)	This voltage is present whenever the tape recorder is in the record, playback, or standby mode. Power for the motor drive circuits is drawn from this line.
Record Signal	On receipt of a record signal, the tape recorder operates in the record mode unless one of the playback commands is present. In this case the record signal is ignored. In the record mode, the two FM modulators and the three record amplifiers are activated to process and store the incoming AVCS data and the flutter-and-wow information. The motor drive circuits are activated to drive the transport mechanism in the record direction. The record signal arrives 1.5 seconds prior to the arrival of the incoming AVCS data.
Playback No. 1 Signal	On receipt of playback No. 1 signal, the tape recorder operates in the playback 1 mode. The playback amplifiers for channel No. 1 (stored AVCS data from sensor No. 1) and channel No. 2 (stored flutter-and-wow information) is activated. The motor drive circuits are activated to drive the transport mechanism in the playback direction. The record mode of operation is inhibited.
Playback No. 2 Signal	On receipt of playback No. 2 signal, the tape recorder operates in the playback 2 mode. The playback amplifiers for channel No. 3 (stored AVCS data from sensor No. 2) and channel No. 2 (stored flutter-and-wow information) are activated. The motor drive circuits are activated to drive the transport mechanism in the playback direction. The record mode of operation is inhibited.

TABLE 2-V-5. AVCS TAPE RECORDER AND SPACECRAFT INTERFACE SIGNALS (Continued)

Signal	Description
Direct No. 1 Signal	On receipt of direct No. 1 signal, the tape recorder operates in direct mode 1 when the record signal is received. Channel No. 1 and channel No. 2 of the record and playback electronics are activated in direct mode 1.
Direct No. 2 Signal	On receipt of direct No. 2 signal, the tape recorder operates in direct mode 2 when the record signal is received. Channel No. 2 and channel No. 3 of the record and playback electronics are activated in direct mode 2.
Motor Phase 1	This control signal is supplied continuously to the subsystem for use in the motor drive circuits. The signal is a square wave at 400 Hz.
Motor Phase 2	This control signal is supplied continuously to the subsystem for use in the motor drive circuits. The signal is a square wave at 400 Hz, delayed by 90 degrees with respect to that of phase 1.
Flutter Clock Signal	The flutter clock signal is present continuously for use in the flutter-and-wow channel during record mode. The signal is a square wave at 50 kHz.
Playback End-of-Tape	The tape recorder provides a signal indicating that the end-of-tape has been reached during playback. This signal consists of two levels: -24 volts DC when not at end-of-tape, and an open circuit when at end-of-tape during playback, or when the recorder is in the OFF mode.
Telemetry Power	Upon command, -24.5 volts DC regulated voltage is supplied for monitoring the pressure and temperature telemetry points.
Advance Tape Signal	The motor drive circuits and record electronics are activated to drive the transport mechanism in the record direction. Operation is much the same as for the record signal.

recorded information after the tape passes the playback head and again before information is recorded on the tape. Therefore, the tape is erased twice before each recording operation.

The capstan is driven by a reversible, 2-phase, synchronous motor through a belt. The mean angular momentum of the transport is reduced to less than 0.02 pound per inch per second by means of the flywheel mounted on the shaft of the capstan. For both record and playback, speed of the 12,000-rpm motor is reduced by the pulley and belt coupling between the motor and capstan shafts to provide a tape speed of 30 inches per second.

The recorder incorporates several end-of-tape sensing devices. The playback end-of-tape indicator consists of a 4-foot length of silver-coated conductive tape fastened near the end of the magnetic tape, and is sensed by a two-contact pickup located near the reels. Should the normal playback end-of-tape sensor fail to function, a microswitch actuated by tape reel diameter buildup will interrupt the recorder playback signal, stopping the recorder. A fail-safe tape mounting is also used to anchor the ends of the tape to both reels. The record end-of-tape sensor consists of a microswitch actuated by tape buildup which interrupts the record signal, stopping the recorder.

(c) Motor Drive Circuit

A solid-state power amplifier, excited by a 400-Hz square wave synchronizing signal from the command subsystem and powered by -24.5 volts DC supplied through the power switching circuits, is used to drive the tape recorder motor. The motor is wound with separate "start" taps, switched by a relay. The "start" tap allows the motor to accelerate rapidly to synchronous operating speed. The acceleration period is internally controlled and lasts approximately 1.5 seconds for record and playback. After the motor has reached synchronous speed, the motor drive outputs are switched to the "run" taps. Motor reversal is accomplished by reversing the phase of the 400-Hz signal at one of the two motor windings.

(d) Video Signal Record and Playback Circuits

Channel 1 and channel 3 of the recorder are used for recording video data from camera 1 and camera 2, respectively. Since only one camera will be activated at a time, only one of the two channels will be recording video data on a given pass.

The video signal from the active camera is applied to an FM modulator wherein the signal is fed to a voltage-controlled oscillator to produce an FM subcarrier with a deviation ranging from 72 to 120 kHz. This subcarrier is then applied to a record amplifier and to the appropriate channel of the record head.

During playback, the recorded FM subcarrier is amplified by the playback preamplifier circuit, amplified and limited by the playback amplifier circuit, and routed to the multiplexer. During playback mode and direct mode operation, the active record and playback channels are selected by command. See Table 2-V-5.

(e) Flutter-and-Wow Record and Playback Circuit

During the record mode, a stable 50-kHz signal generated in the command subsystem is recorded on track 2. During readout, this signal is amplified, limited, and filtered to provide a constant amplitude FM signal having a center frequency of 50 kHz and frequency deviations proportional to the flutter-and-wow characteristics of the recorder.

(2) FUNCTIONAL OPERATION

(a) Electronics

The electronic circuits used in the FM modulators, record head driver flutter-and-wow head drivers, and the direct mode circuitry have been previously used on the TOS program. The logic diagram of the tape recorder electronics component is RCA 1976089, which is published under separate cover.*

1. Record Power Switch

The record power switch is activated in the record mode and supplies 130 milliamperes to the record circuitry. The record power switch circuitry consists of a diode, resistor, and transistor switching circuit (see RCA 1976089, sheet 1). The input to the circuit is at P1, 4, and the record signal is at a voltage level of +4.4 ±0.6 volts. When the record signal is applied, transistors Q16 and Q17 are turned off. As a result, the output Darlington pair Q18 and Q19 switch to -23.5 volts, thus applying power to the flutter-and-wow record head driver, the channel 1 and 3 modulators, and the record head drivers.

2. Playback Power Switch

One of the two playback power switches may be activated during playback. Each power switch supplies 25 milliamperes at -24.5 volts to the preamplifier and limiter. See RCA 1976089, sheet 1.

*RCA Corporation, Astro Electronics Division, TIROS M/ITOS Spacecraft Logic Diagrams, AED M-2175, Contract NAS 5-10306, Princeton, N. J., June 15, 1969.

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The playback power switch consists of a diode, resistor, and transistor switching circuit. The playback signals are applied to P1, 17, and P1, 26 with a DC level of -21 ±3 volts. On application of playback signal No. 1, Q1 and the output power Darlington transistors Q2 and Q3 turn on. This causes a -23.5-volt signal to be applied to playback No. 1 circuitry.

Playback signal No. 2 turns on Q4, Q5, and Q6 transistors and consequently applies -23.5-volt power to playback No. 2 circuitry.

3. Playback End-of-Tape Circuit

The playback end-of-tape circuit supplies 5 milliamperes at -20 volts to the external circuit when the recorder is not at the end of playback. This circuit consists of a diode, resistor, and transistor switching circuit (see RCA 1976089, sheet 1). When the tape is not at the end-of-tape playback position, the input to P1, 15 is open-circuit, Q22 is off, and Q21 is saturated, hence supplying 5 milliamperes to the external circuitry, via CR30 and R61. When the tape is at the end-of-tape playback position, a ground potential is supplied to P1, 15 which turns Q22 to saturation and turns Q21 off.

4. Operating Status Telemetry

The operating status telemetry provides a different DC level for each control signal. This circuit consists of diode and resistor circuitry (see RCA 1976089, sheet 2). The telemetry voltage output at P1, 1 (the voltage that appears across R56), forms a potential divider of R55, R54 and R53. Diodes CR14, CR15, and CR16 provide isolation among signals.

5. One-Shot and Differentiating Circuit

The one-shot and differentiating circuit provides a 1.3-second pulse which is used to accelerate the tape drive mechanism during the start mode.

The differentiating circuit and one-shot (with its power output stage and relay driver) are shown on RCA 1976089, sheet 1. The purpose of the playback and record differentiating circuit is to provide a 15-millisecond pulse input to the 1.3-second duration one-shot. The one-shot, the motor drive circuitry, and the motor drive relay increase the motor current during start-up mode. The differentiating circuits consists of diode, resistor, and transistor circuits, with an added RC differentiating circuit. CR4, the input diode in the record differentiating circuit, goes to -24.5 volts only if the record signal is present. Input diode CR5 is at -24.5 volts when no playback signal is present. Under

these conditions, Q2 saturates to ground, applying +24 volts to the cathode of CR9 and turning Q3 off. Q3 will remain off until the voltage at the cathode of CR9 decays exponentially to about -2 volts.

During the period in which transistor Q3 (board A6) is off, Q16 on board A5 saturates to -24 volts. After 15 milliseconds, Q3 (A6) saturates to ground, which initiates the positive-going ramp voltage waveform generation (1.3 seconds) at the Q16 (A5) collector and Q7 (A6) base. About 1.3 seconds later, the voltage at Q7 (A6) base reaches -6 volts (from -12 volts), which equalizes the circuit (in the sense that the Q7 (A6) collector current has approached zero), and the circuit switches back to its quiescent state. The worst-case analyses show that the output pulse duration can vary between 1 and 1.50 seconds. During the 1.3-second period when the one-shot pulse is on, the voltage at the Q16 (A5) collector decreases from -24.5 to -18 volts. Consequently, Q17 and Q18 (relay driver) and Q19 and Q20 (power output stage of the 1.3-second one-shot) are turned on.

6. Motor Drive Circuit

The motor drive circuit is a four-phase, two-bridge circuit (see RCA 1976089, sheet 1). The functions of the motor drive circuit are as follows:

- To drive the motor such that the tape is moving in record direction when in record mode with no playback signal present,
- To drive the motor such that the tape is moving in playback direction when in playback mode, regardless of record status,
- To provide high start-up current to the motor during record and playback start mode, and
- To stop the motor current when either record or playback end-of-tape signal has been received.

The function of the motor power switch circuit is to supply the motor driver circuit with -24.5-volt power in normal operation.

The low power drive circuitry is shown in RCA 1976089, sheet 1. Whenever a record signal or an advance tape signal is present along with the two 400-Hz phases (P1, 4 and 30), the following conditions prevail:

- Q4 is cut off, which saturates Q2 to ground and initiates the 15-millisecond and 1.3-second pulse generation;

- The $\phi 1$ and $\phi 2$ square wave input signals ($\phi 2$ lags $\phi 1$ by 90 degrees) switch Q14, Q8, Q9, and Q5 on and off, yielding the waveforms shown in Figure 2-V-43A; and
- The two-phase input waveforms are introduced to the A5 board (high level logic and motor drive) at pin numbers 3 and 22 on connector P1.
- These signals switch Q1, Q2, Q3, Q4, Q10, Q11, Q12, and Q13 on and off, causing the waveforms shown in Figure 2-V-43B to appear at the emitters of Q5, Q6, Q14, and Q15.

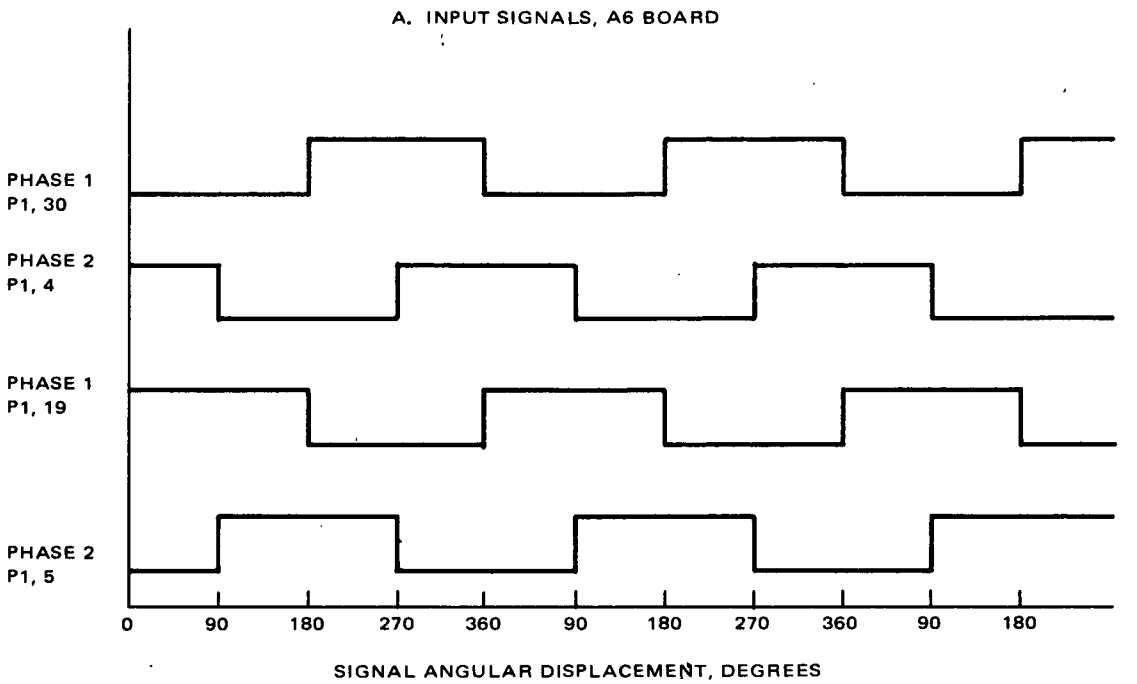
7. Start Mode

During the start mode, Q19 and Q20 (1.3 second one-shot power output stage) and Q17 and Q18 (relay driver) transistors are "on". When Q19 and Q20 are saturated, diodes CR24, CR26, CR27, CR28, and CR29 provide gating which allows the following:

- Q15 shorts out R55 when Q13 is "on",
- Q14 shorts out R42 when Q11 is "on",
- Q6 shorts out R14 when Q4 is "on", and
- Q5 shorts out R12 when Q2 is "on".

When Q17 and Q18 are "on" they activate the relay which connects approximately one-half of the motor winding across the drive bridge, thus providing increased motor torque.

Also during the start mode, the two bridge circuits (A7) turn on and off and reverse current through the two windings in the following manner. When Q14 emitter (A5) is at ground potential and Q15 emitter (A5) is cut off, then the bridge (A7) transistor Q5 is turned "on", Q8 is saturated to -24 volts and Q6 and Q7 are cut off. Hence, the common $\phi 2$ line (P1, 17) is at ground. When the Q14 (A5) emitter is cut off and Q15 (A6) is at ground potential, then Q6 and Q7 are cut off. Hence, the common $\phi 2$ line (P1, 14) is at -24 volts and the start $\phi 2$ line (P1, 17) is at ground. When the Q14 (A5) emitter is cut off and Q15 (A6) is at ground potential, then Q6 (A7) is saturated to -24 volts and Q7 (A7) is turned on. Hence, the common $\phi 2$ line is at ground potential and the start $\phi 2$ line is at -24 volts. This results in a current reversal. The phase 1 bridge, which employs Q1, Q2, Q3, and Q4 transistors, operates in an identical manner to the phase 1 bridge, except the driving waveforms have different phasing, as depicted in Figure 2-V-43B.



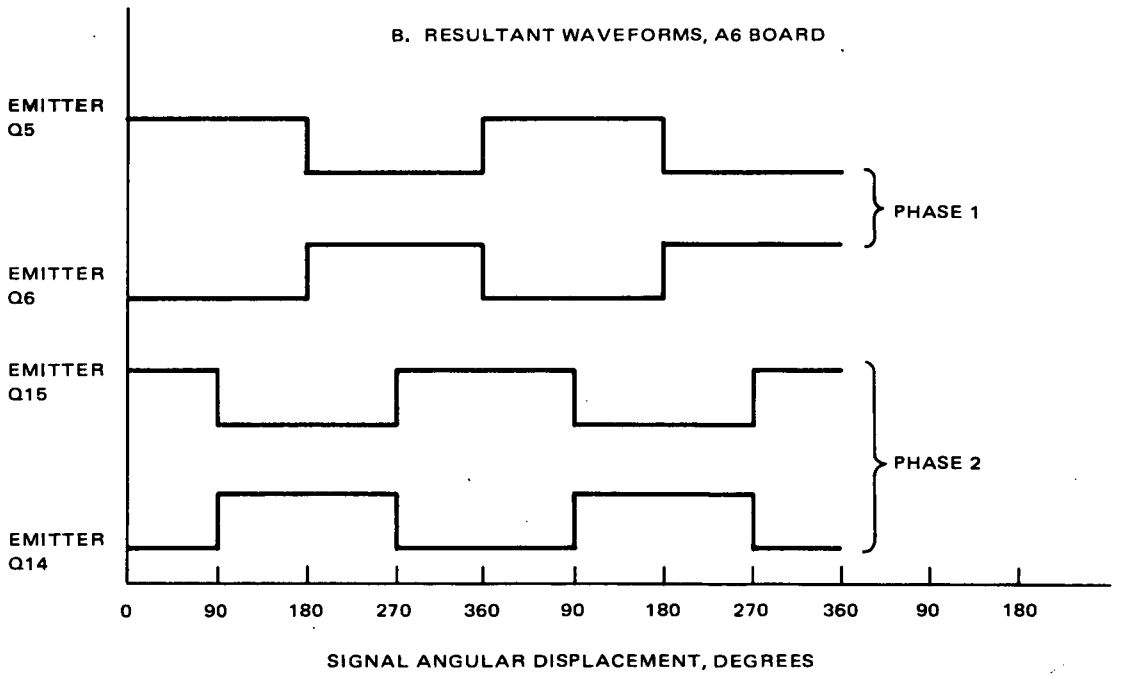


Figure 2-V-43. Waveforms, Power Drive Circuitry

The start mode operation continues until the one-shot pulse (1.3 seconds) terminates, turning off the relay driver, which switches the relay to the run mode. The one-shot power output stage (A5) is also turned off, thus switching off Q5, Q6, Q14, and Q15 (all on A5). The operation in the run mode is similar to the start mode, except that the bridges drive the full motor winding, due to the lower torque requirement during the run mode.

8. Record Mode

(See RCA 1976089 in Logic Diagram Manual previously referenced.) Record mode operation is performed whenever a record signal is present (J1, 12) along with the 400-Hz ϕ1 and ϕ2 (J1, 8 and 9), and neither of the playback signals is applied. Under these conditions the gate A6-Q4 output enables A6-Q2 which in turn initiates the 1.3-second start mode one-shot. The output of the one-shot enables relay driver A5-Q17, which sets the relay to the start mode. The output of the one-shot also enables Q19 and Q20, which results in the necessary increase in drive current to the two bridges during the start-up mode. The A6-4 gate also enables the A6-Q5 gate. The A5-Q2 output is applied to the motor bridge input, and the A5-Q4 output is applied to the opposite side of the motor bridge input (i.e., one half of the bridge is on while the other half is off). A5-Q2 and A5-Q4 outputs are also feeding A5-Q5 and A5-Q6 which apply base current drive to the bridge. The bridge output voltage at A7, 24 and A7, 11 switches from 0 volt and -24 volts to -24 volts and 0 volt, respectively, at 400 Hz.

The ϕ2 input at J1, 9 is applied to the second motor drive bridge (via gates A6-Q14, Q10, Q11, Q12, Q13, Q14, and Q15) and is implemented in a similar manner to the ϕ1 input described above. The outputs of the two bridges are applied to the motor, and the sequence of the phases drives the tape in the record direction. During the start-up one-shot period of 1.3 seconds, the tape reaches its final velocity of 30 inches per second. When the one-shot pulse terminates, it causes the turn-off of the base drive current changers (Q5, Q6, Q14 and Q15) and turn-off of the relay driver which switches the relay to the run mode.

Upon application of the record signal, A6-Q16 gate is enabled via A6-Q4 and the backup end-of-tape microswitches which saturate the motor power switch to -24 volts. The record power switch is saturated to -24 volts via J3, 4 which powers the CH1, CH2, and CH3 record electronics.

Direct No. 1 signal (J3, 20) may also be applied during the record mode. This signal powers the channel No. 1 limiter and channel No. 2 limiter, so that the channel 1 and 2 input data is transmitted via limiters in real time. J3, 19 and J3, 5 are the respective data output pins.

Direct No. 2 signal (J3, 7) may be applied during the record mode. This signal powers the channel No. 3 limiter and channel No. 2 limiter, so that channel 3 and 2 input data is transmitted via limiters in real time. J3, 19 and J3, 5 are the respective data output pins. Data recording may commence 1.5 seconds after the application of the record signal.

The record signal may be terminated at any time, disabling the A6-Q4 gate. Consequently the tape recorder is switched to standby mode, except for the direct signal modes No. 1 and No. 2. These direct signals are terminated along with the record signal. By applying a new record signal or an advance tape signal, the previously described sequence of events takes place until the end-of-tape record signal is received. The recorder is then switched to the standby mode.

When the record mode is terminated, Q4 (A6) saturates to ground and inhibits the motor power switch via the normally-closed contacts of the record microswitch. As a result, Q16, Q18, Q19 (all on A6), Q7 (A5), and Q9 (A7) are switched off.

When the record end-of-tape (EOT) signal is received, a ground potential is applied to P1, 11 (A6) which again causes the motor power switch to turn off.

9. Playback Signal

(See RCA 1976089 in Logic Diagram Manual previously referenced. Playback mode operation is performed whenever playback No. 1 signal (J3, 3) or playback No. 2 signal (J3, 16) is received. Under these conditions either channel Nos. 1 and 2, or channel Nos. 3 and 2 playback electronics (preamplifier and limiter) are powered from playback switch Nos. 1 or 2.

The playback signal is also applied to A6-Q13 switch which disables the record signal and enables the 1.3-second start mode one-shot via A6-Q10, A6-Q11, and A6-Q7. The 1.3-second one-shot performs the same functions as in the record mode. At the same time, the motor power switch is enabled via A6-Q17 and backup end-of-tape microswitch. The 400-Hz ϕ1 (J1, 8) is inverted

in comparison to the record mode as shown at the output of the gates Q2 and Q4. This phase 1 inversion reverses the motor rotating field, and, consequently, the motor direction is reversed in comparison to the record direction.

The sequence of events for the start and run modes during playback is similar to the sequence which occurs during the record operation; 1.3 seconds after the application of the playback signal, the base drive current-changing transistors are switched off, and the relay driver is switched off, thus returning the relay to the run mode. The tape continues to move at 30 inches per second until the end-of-tape playback signal is received. A6-Q17 is inhibited, and the motor power switch is turned off. At the same time, the end-of-tape circuit, which was enabled during the playback mode, is disabled.

If the end-of-tape sensor fails, the tape continues to move until the backup microswitch operates. The motor power switch is then disabled, via A6-Q17.

When the playback signal is applied, events similar to the record mode occur, except that the playback differentiator circuit [Q10 and Q11 (A6)] initiates the 1.3-second start-up one-shot. For the playback signal, the 400-Hz ϕ 1 goes through double inversion only, (record has 3 inversions) via Q8 and Q15. Hence, ϕ 1 waveforms are the inverse of those depicted on RCA 1976089, sheet 1. The motor windings receive current pulses which cause the developed torque to be opposite to the record direction; hence, the motor will reverse direction.

If the ϕ2 signal disappears at P1, 3 (A5), then C8 and CR14 (A7) become inactive, permitting C4 (A6) to discharge and turn Q20 off. Q21 saturates to ground, thus causing the turn-off of the motor power switch via CR61 and CR62.

The function of L1, L2, L3, and L4 (on A7) is to prevent the short circuiting of the bridges due to unequal rise and fall times or saturation delays incurred in the drive circuitry transistors.

Components L5, C5, C6, and C7 (on A7) limit the rate of current change during turn-on of the motor power switch.

10. Telemetry Circuits

The motor current telemetry circuit, shown on the A5 board, consists of a differential amplifier (Q9) and a constant current source (Q8 and VR1). Any voltage difference between P1, 16 and P1, 6 appears as a voltage difference between Q9-2 and Q9-6. Hence, the output voltage at P1, 8 is proportional to the voltage at P1, 6, the voltage drop caused by the motor current across a known resistor.

Command status telemetry output is provided on J3, 22, and the motor current telemetry output is provided on J1, 24. Temperature and pressure telemetry power input is on J1, 5, and outputs are provided on J1, 11 and J1, 10.

(b) Mechanical

Figure 2-V-44 is a photograph of the AVCS tape transport, showing the negator side of the chassis. Figure 2-V-45 depicts the reel side of the transport, showing the three idlers, capstan, and the magnetic head assembly.

1. Motor and Drive

The motor torque is 0.65 inch-ounce. The motor is mounted to an eccentric plate which can be rotated for belt-tightening and tilted to provide belt tracking.

2. Chassis and Container Mounting

The AVCS transport chassis has a three-point mounting system for attachment to the container, and the container is surface-mounted to the spacecraft.

3. Negator Springs

The negator springs for the AVCS transport are 1/2-inch-wide Havar, to provide increased life at the proper torque.

C. APT CAMERA SUBSYSTEM

1. General Description

The APT camera subsystem is used to take wide-angle TV pictures of the earth and its cloud cover during subpoint daylight; these pictures are transmitted in real time to APT field stations for reproduction on facsimile equipment. The APT camera subsystem is controlled by ground-initiated commands that are transmitted to the satellite from the CDA stations and are processed and stored by the satellite's command subsystem. The program of commands directs the APT camera subsystem to start taking a sequence of pictures at a predetermined point in the orbit. A full APT picture sequence contains 11 pictures taken at 260-second intervals. Any of the 11 pictures may be omitted by programming, so that a sequence may contain from 1 to 11 pictures, and the pictures takem may be located at any desired positions in the sequence. Once

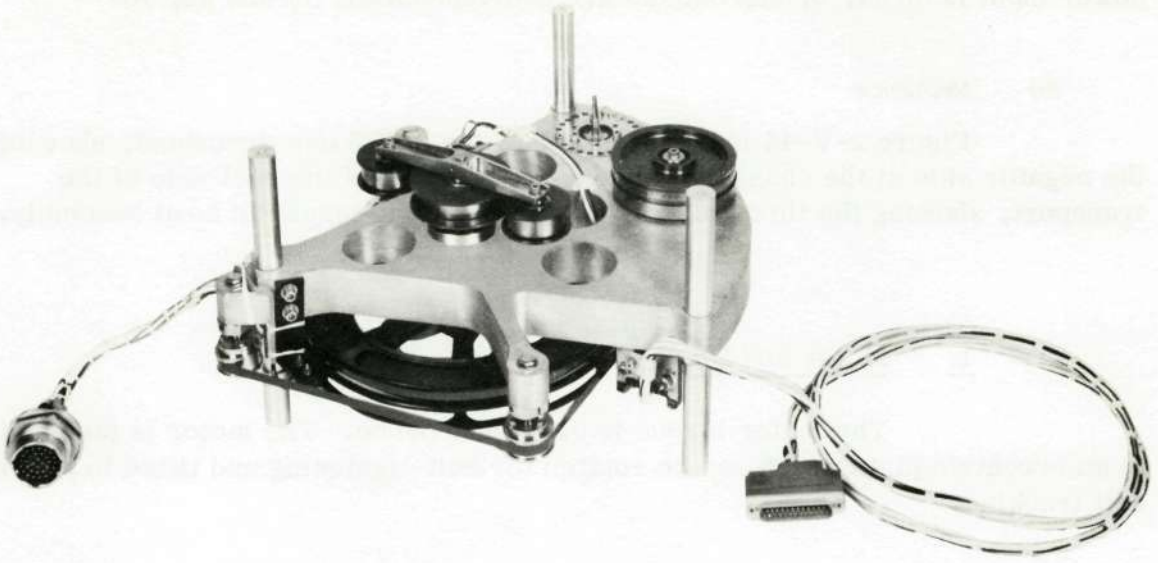


Figure 2-V-44. AVCS Recorder Transport, Negator Side

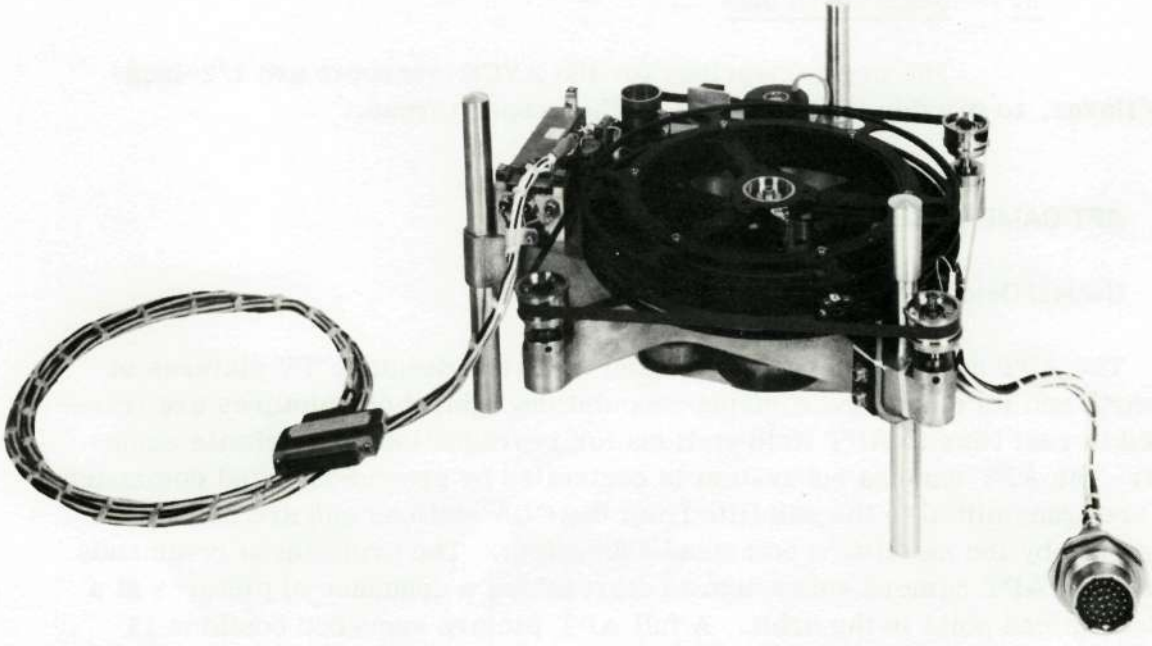


Figure 2-V-45. AVCS Recorder Transport, Reel Side

the sequence is initiated, the camera will take pictures under satellite command until the programmed picture sequence has been taken. These pictures are transmitted to APT field stations within communications range of the satellite by a transmitter in the real-time data link. The sequence is repeated automatically during each orbit of the satellite until the command subsystem is turned off or programmed otherwise by a CDA station.

The APT camera employs a high-persistence vidicon that provides a 600-scan-line image. Use of this vidicon permits very slow (150-second) readout of the exposed image and thus permits narrow band transmission of the video signal which, in turn, allows the use of relatively simple equipment at the APT field stations.

There are two APT camera subsystems aboard the spacecraft, only one of which is selected by ground command for operation during any picture-taking sequence. The output of either subsystem may be connected by ground command to either of two transmitters in the real-time data link.

The major elements of the redundant APT camera subsystems are shown in the block diagram of Figure 2-V-46 and in the composite photograph of Figure 2-V-47. Each subsystem comprises a camera sensor assembly that converts optical images into electrical signals and a camera electronics module that

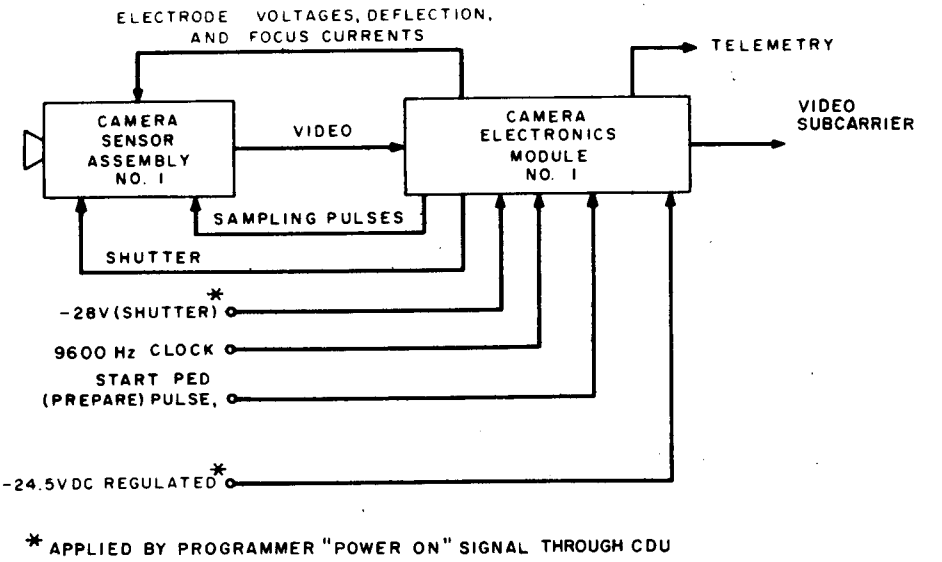


Figure 2-V-46. APT Camera Subsystem Block Diagram (One of Two Redundant Cameras)

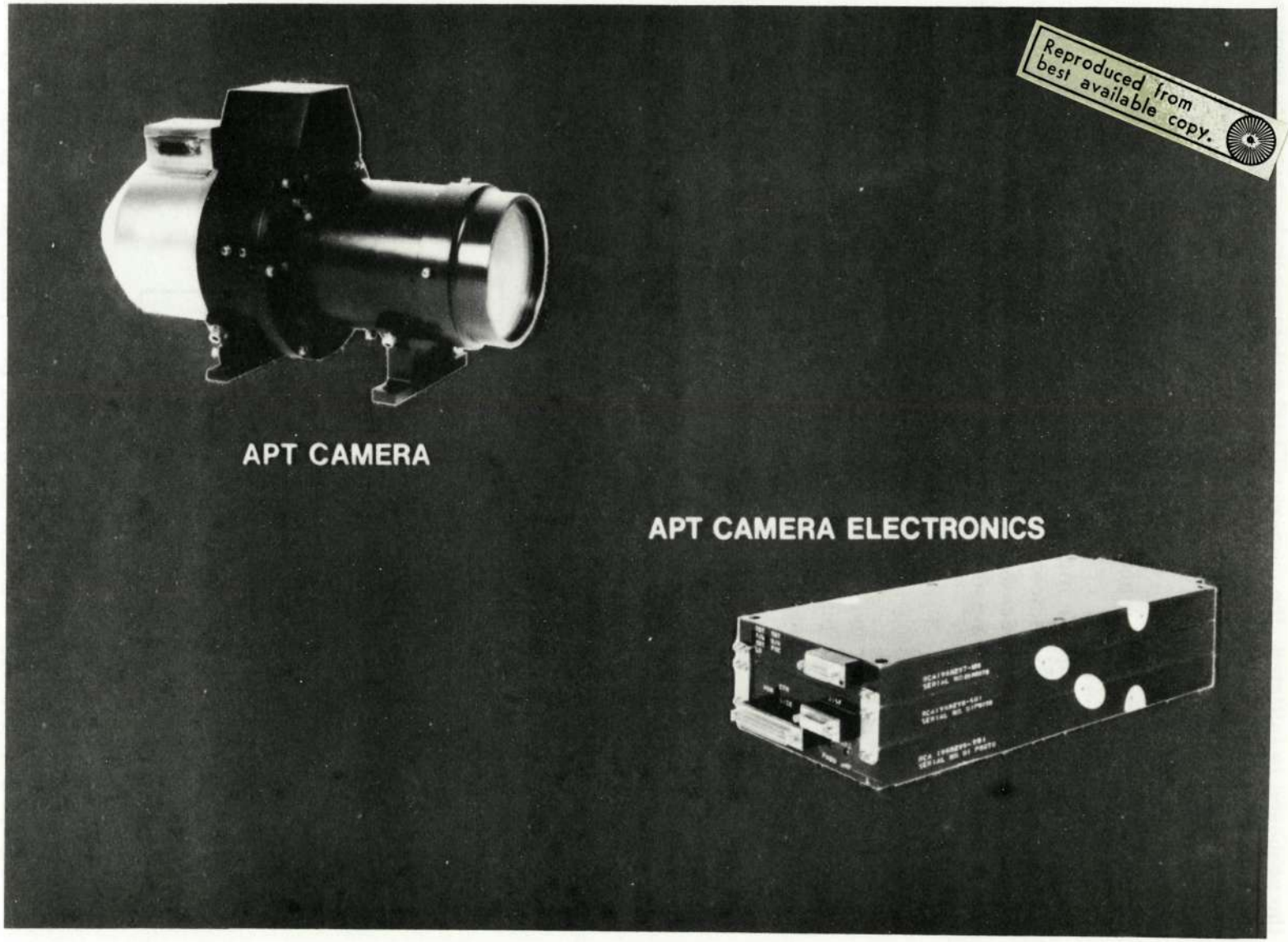


Figure 2-V-47. APT Camera Subsystem

incorporates the timing, control, video processing, and power circuits for the associated camera sensor. All APT camera subsystem operations are controlled by a sequence timer in the camera electronics module; the sequence timer, in turn, is controlled by the selected programmer in the command subsystem. The digital functions in the sequence timer are performed by integrated circuits.

2. Functional Description

For the following discussion, refer to Figure 2-V-48, a timing diagram of APT camera operation. The first picture of a sequence is exposed 57.5 seconds after the programmer overflows at time T_0, where T_0 is the subpoint night-to-day transition time reference in the programmer counter logic. Approximately 6.5 seconds before T_0, a "power on" signal from the programmer connects -24.5 volts DC from the regulated bus of the spacecraft to the APT camera subsystem. A -28-volt DC potential from the unregulated bus is also applied at this time to the shutter drive control circuit in the camera electronics module. With the application of primary power, the APT camera subsystem enters a warmup and stabilization period during which the circuits in the camera electronics module attain a stable operating status and the vidicon filament is energized. At T_0 plus 52.25 seconds,* a "prepare" signal from the active programmer is applied to the sequence timer to initiate the picture-taking and readout period. (The first 8 seconds of this period are known as the prepare-expose-delay, or PED, cycle.) Coincident with the leading edge of the prepare pulse, the horizontal and vertical sweep circuits are enabled, and the target (erase) lamps, mounted on the target lamp ring around the periphery of the vidicon and in proximity to the photoconductive layer, are turned on. The lamps are energized for 1 second, during which the vidicon is flooded with light to completely discharge the photoconductor to a uniform white level, thereby removing any residual image from the previous exposure. At the same time that the lamps are energized, the vidicon beam is gated on and scanned rapidly across the image area by a 4-kHz vertical deflection voltage and a 4-Hz horizontal deflection voltage. This rapid scanning process lasts 5 seconds and deposits a uniform black level charge on the photoconductor. Vidicon scanning is terminated and the beam is gated off 1/2 second before exposure.

During the 1-second exposure window, the sequence timer delivers an "expose" pulse to the shutter drive circuit in the camera electronics module. This circuit controls the operation of two solenoids that actuate the double-bladed, focal plane shutter in the camera sensor assembly. The shutter blades are actuated sequentially and, in moving from one side of the lens to the other, expose the

*During the 52.25-second period after T_0, the AVCS camera is executing its prepare-expose-and-readout cycle. The APT camera shutter is actuated about 3-1/4 seconds after power is removed from the tape motor drive in the AVCS subsystem.

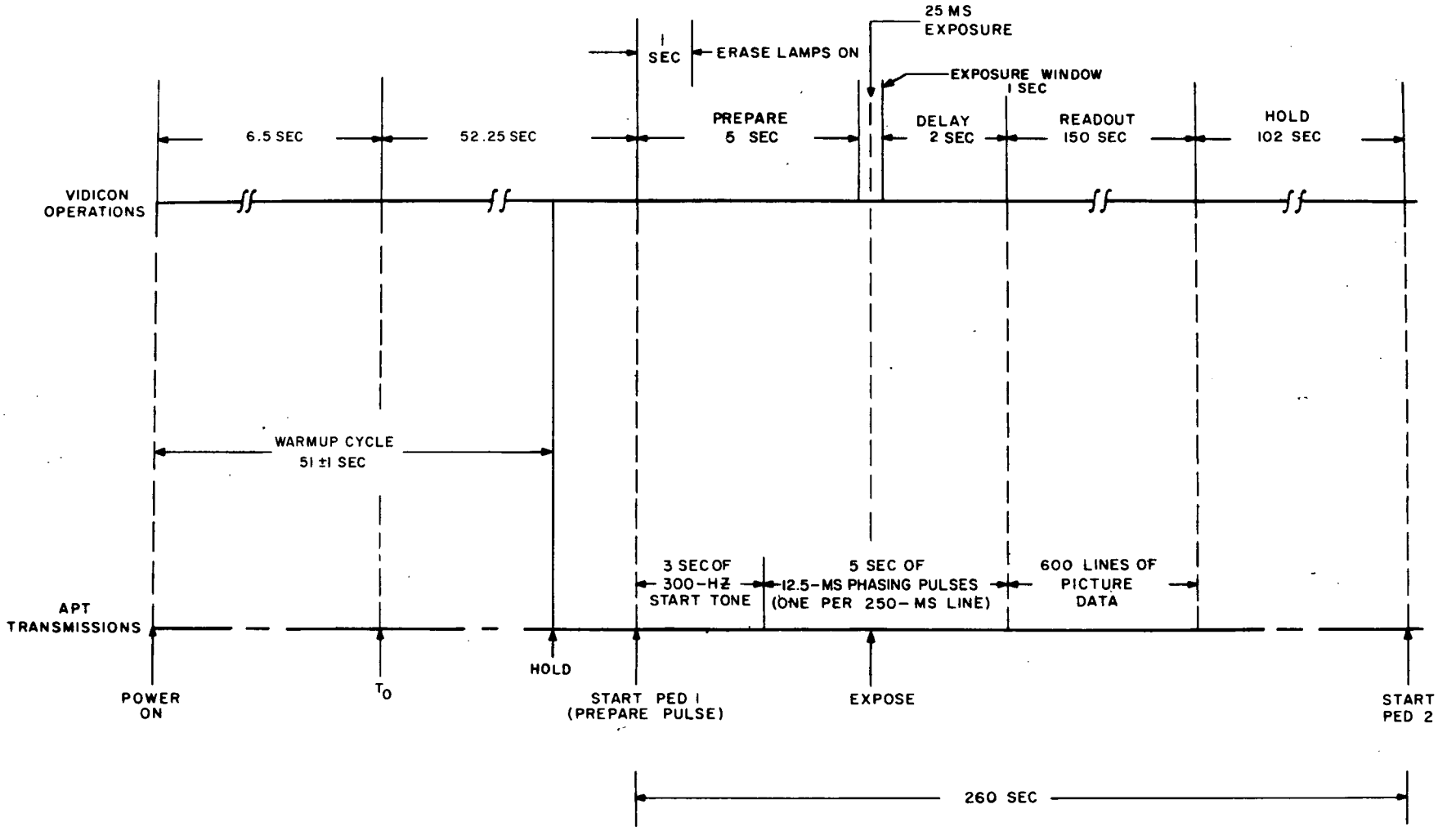


Figure 2-V-48. APT Camera Subsystem, Timing and Sequencing Diagram

vidicon for 25 milliseconds. Exposure alters the uniform charge pattern of the photoconductor by inducing each resolution element to discharge in proporation to the amount of incidient light.

After a 2-second delay period, the video readout cycle is begun by gating on the vidicon beam and the horizontal and vertical sweep voltages. During the 150-second readout period, 600 discrete lines of video are produced. As the electron beam scans the photoconductor line by line, it deposits a charge on the resolution elements that have been discharged by exposure to varying intensities of light. The charging currents flowing through a load connected externally to the vidicon target electrode produce the video signal. To improve the signal-to-noise ratio, a sampling technique is used to extract the video in the stored image. During the active portion of each scan line, which lasts 237.5 milliseconds, the vidicon beam is turned on for 22 microseconds out of every 208-1/3 microseconds for a total of 1140 times per line. Consequently, the output of the vidicon is a train of 22-microsecond pulses having a repetition rate of 4800 pps. The amplitude of each pulse is proportional to the light incident at the sampling point. This video pulse train is amplified and detected by video processing circuits to produce an analog signal that is used to amplitude-modulate a 2400-Hz subcarrier. The maximum video modulation frequency is 1680 Hz, corresponding to an 800 TV line response, the video processor attenuates all frequencies above this value at a rate of 24 decibels per octave. The amplitude-modulated subcarrier is applied through a buffer amplifier to the selected transmitter in the real-time data link.

In addition to the video information, the 2400-Hz subcarrier is modulated with a 300-Hz start tone and a series of 12.5-millisecond phasing pulses, both generated in the camera electronics module. The 300-Hz start tone is generated during the first 3 seconds of the PED cycle and is used at the APT field stations to automatically transfer the receiving and processing equipment from a standby to an operational status. For the 5 seconds of the PED cycle immediately following the start tone, a group of 12.5-millisecond phasing pulses, occurring at the rate of 1 pulse every 250 milliseconds, is provided to synchronize the horizontal scan circuits in the APT processing equipment to the vidicon scanning frequency. During the 150-second period that follows, the facsimile equipment in the APT field stations reproduces, line by line, the picture data readout of the vidicon.

At the conclusion of the 150-second readout period, the sequence timer places the APT camera subsystem in a "hold" status for 102 seconds. During the hold period, there is no output from the camera. The arrival of the next programmer "prepare" pulse, displaced from the previous one by 260 seconds, initiates another PED and readout cycle. When a complete sequence of 11 pictures is taken, the programmer removes -24.5- and -28-volt DC power from the APT subsystem. Subsystem power is reapplied 6.5 seconds before T_0 on the next orbit. Thus, the picture-taking sequence is repeated as described in the preceding discussion,

once during each orbital revolution, until the active programmer is reloaded or turned off.

3. APT Components

a. APT CAMERA SENSOR AND CAMERA ELECTRONICS

(1) GENERAL DESCRIPTION

The APT camera subsystem was designed by modifying the camera subsystem used on TOS F and H to accommodate the ITOS spacecraft requirements for an APT-type television subsystem. This section summarizes the results of AED engineering efforts in the redesign of the earlier APT camera and its associated camera electronics, performed under NASA Contract NAS5-10306.

The design of the APT camera subsystem for ITOS was limited in scope, being restricted to redesign of certain specific circuits and mechanical assemblies. The objectives of reliability for the most part dictated these changes. The remaining circuits are for the most part, unchanged from the TOS F and H APT camera subsystem. However, due to repackaging requirements, a number of board assemblies and layouts required redesign. The characteristics of the camera sensor and electronics units are given in Table 2-V-6. The spacecraft interface signals are listed in Table 2-V-7.

All new or redesigned portions of the APT camera subsystem for ITOS embodied worst-case ITOS environmental parameters in the designs. The effects of environmental parameters (temperature range, radiation levels, and life degradation on components) were included insofar as these are known or may be estimated. These environmental factors are embodied in the circuit modification discussions that follow. Circuit components, transistors, diodes, resistors, capacitors, etc., were chosen from the ITOS standard parts list wherever feasible. Components not appearing on this list required separate approval from the AED reliability group. Transistor h_{FE} curves and I_{CBO} values prepared by reliability, indicating the extrapolated effects cf radiation and life degradation, were used to obtain worst-case values when available. In addition, the following resistor tolerances were employed to include initial, temperature, radiation, and life effects.

Resistors	Total Tolerance
• Carbon composition	±15 percent
• Carbon film	±4 percent
• Metal film	±3 percent

TABLE 2-V-6. APT CAMERA SUBSYSTEM CHARACTERISTICS

Characteristics	Description or Value
Picture Coverage	
Picture Projection*	1830 by 1200 nmi
Pictures per Orbit	11
Time for an 11-Picture Sequence	Approximately 52 minutes
Time Between Pictures	260 seconds
Picture Overlay (along orbital track)	33-1/3 percent
Camera and Associated Electronics	
Lens	f/1.8, 5.7 mm focal length
Field of View	Approximately 95 degrees across the picture diagonals; effectively 89 ±1 degrees across the picture flats
Ground Resolution	Approximately 2 nmi per scan line
Image Area (scanned)	0.36 inch vertical by 0.48 inch, horizontal
Resolution (horizontal)	25-percent response at 600 TV lines
Aspect Ratio	3:4
Prepare-Expose-Delay (PED) Cycle Duration	8 seconds
Vidicon Exposure Time	25 milliseconds
Vidicon Readout Time (frame period)	150 seconds
Horizontal Sweep Period	250 milliseconds per line
Horizontal Sweep Time	237.5 milliseconds
Horizontal Blanking and Retrace	12.5 milliseconds
Horizontal Lines per Frame	600 (noninterlaced)
Video Sampling Pulse Width	22 microseconds
Video Sampling Pulse Rate	4800 pps

*Based on an altitude of 790 nautical miles.

TABLE 2-V-6. APT CAMERA SUBSYSTEM CHARACTERISTICS (Continued)

Characteristics	Description or Value
Number of Video Sampling Pulses per Line	1140
Start Tone Frequency	300 Hz
Start Tone Duration	First 3 seconds of PED cycle
Phasing Pulse Repetition Rate	4 pps
Phasing Pulse Width	12.5 milliseconds
Phasing Pulse Gating Time	Last 5 seconds of PED cycle
Video Subcarrier	2400 Hz
Modulation Frequency	1680 Hz maximum
Type of Modulation	Amplitude, double-sideband with carrier
Percentage of Modulation	95 percent
Video Subcarrier Amplitude for Start Tone, Phasing Pulses, and Video	2.8 volts peak-to-peak (white), 0.07 volt peak-to-pkeak (black)
Signal-to-Noise Ratio	32 dB minimum

Power supply voltages and tolerances used in the new designs are shown in Table 2-V-8.

In general, the following contraints were also observed where applicable:

- "Off" biases of nonreverse biased stages. A maximum of 0.1-volt V_{be} forward bias was allowed due to worst-case leakage currents flowing in input circuitry. Impedance levels were adjusted to ensure this maximum V_{be}.
- Reverse bias voltages on transistors were limited to a maximum of 0.8 or less of maximum rated $(V_{be})_{Rev}$.
- Continuous dissipations in resistors and transistors were limited to 0.5 of power rating and 0.1 whenever possible.

TABLE 2-V-7. APT CAMERA SUBSYSTEM AND SPACECRAFT INTERFACE

Interface Signal	Description
Spacecraft Power	
-24.5 VDC	Regulated within ±2 percent. This is the main power source for the APT subsystem. It is switched on and off in accordance with the "power on" signal described below.
-28 VDC	Unregulated. Powers the solenoids that operate the shutter when the shutter drive circuit is triggered by the sequence timer. This power source is also switched on and off by the "power on" signal.
Timing	
9600 Hz	A synchronizing signal supplied by the time base generator to the sequence timer. The clock signal is from 0 to +4.4 volts peak-to-peak.
Power On	A -24.5-volt DC level that is switched on 58.75 seconds before the first "prepare" signal is delivered to the APT subsystem. The "power on" signal is maintained at -24.5 volts DC throughout the entire 11-picture sequence.
Prepare	A 0- to +4.4-volt DC pulse, 1.25 seconds in duration, delivered to the sequence timer 5.5 seconds prior to vidicon exposure.
Video	An amplitude-modulated 2400-Hz subcarrier, 2.8 volts peak-to-peak amplitude (10,000-foot-lambert scene), 95-percent modulation, 1680-Hz modulation signal bandwidth.
Telemetry	See Table 2-VII-3 in Section VII of part 2 for a complete list of the telemetry points in the APT subsystem.

(a) APT Camera Sensor

1. Introduction and Design Changes

The APT camera sensor assembly is made up of the elements shown in Figure 2-V-49. These elements are mounted on a cylindrical, magnesium camera housing, which is equipped with an RF shielded enclosure to prevent pickup of RF interference; an internal magnetic shield, incorporated

TABLE 2-V-8. POWER SUPPLY AND TOLERANCES

Supply Voltages	Tolerances
+5.3 volts regulated	±0.25 volt max
-6.3 volts regulated	-6.25 ±0.25 volts max
-24.5 volts spacecraft	-24.5 ±0.5 volts max
+24.5 volts regulated	+26 ±1.5 volts
-28.0 volts spacecraft	Shutter power -26 to -33 volts
+18.0 volts regulated	±0.5 percent of initial
-18.0 volts regulated	±0.5 percent of initial

into the yoke assembly, is employed to protect the camera sensor assembly against the adverse effects of the combined earth and satellite magnetic fields, which would cause distortion of the picture received at the ground station.

The camera housing was redesigned to accommodate the new shutter assembly and yoke magnetic shield. Both outside and inside diameters were increased by 0.14 inch. The method of retaining the shutter on the bottom of the housing was changed so that the shutter is now retained by a fitting into a urethane bushing which, in turn, is cemented into the housing, thus limiting the shutter's lateral

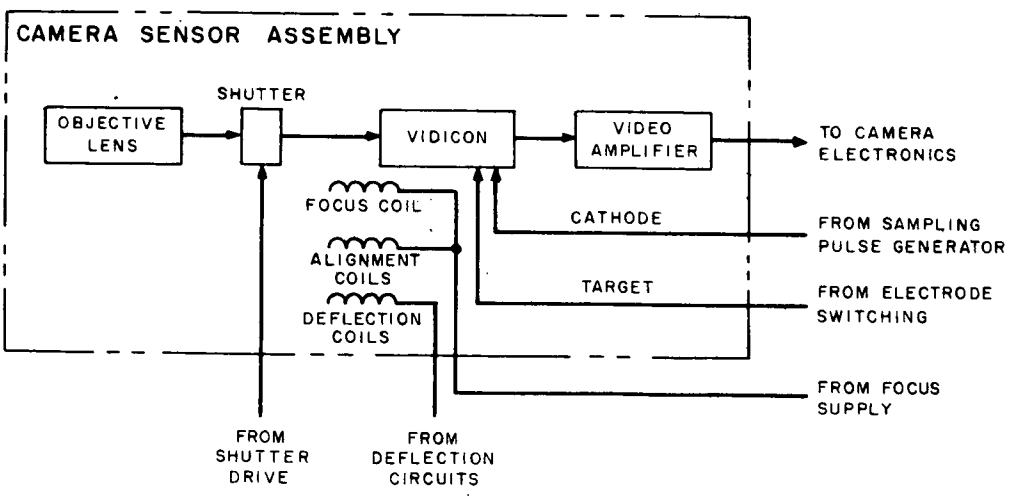


Figure 2-V-49. Camera Sensor Assembly, Block Diagram

motion with a minimum of restraint. Since the bottom end of the shutter is free to move in the vertical direction, shock transmission to the housing is minimized.

The camera assembly has provisions for mechanical adjustments of the yoke-vidicon combination relative to the lens optical axis. This was necessary to facilitate optical alignment.

The shield cans as well as the boards for the sample pulse amplifier and de-coupling assemblies were slightly modified to make them conform to the inside wall circumference of the camera housing. The shield cans and circuit boards fit inside the front cavity of the sensor housing. Slight increase in radii (0.07 inch) of the kidney-shaped assembly was required to match the new diameter of the sensor housing with some relocation of components.

The single-bladed shutter assembly was replaced by a modified version of a Nimbus-type double-bladed shutter. The main components of this focal plane shutter assembly are the two blade assemblies: one to starting the exposure and the other to stop it. Each shutter blade assembly is driven by a solenoid. The exposure time is controlled by the shutter drive circuitry located in the camera electronics assembly.

The shutter drive circuit probides a pulse to the first solenoid, causing the solenoid plunger to be drawn into the solenoid housing. The plunger, to which the blade assembly is attached, positions the blade assembly so that its opening exposes the photo sensitive area of the vidicon to the lens. This is the start of the exposure (see position 2, Figure 2-V-50).

At the end of the exposure, a pulse is supplied to the second solenoid which, by drawing in its plunger, positions the second blade assembly to obscure the photo-sensitive area of the vidicon from the lens (see position 3, Figure 2-V-50).

Power is now withdrawn from the first solenoid and a spring returns the blade assembly to its preexposure position (see position 4, Figure 2-V-50). Power is next withdrawn from the second solenoid and the second blade assembly is returned to its preexposure position by the spring (see position 1, Figure 2-V-50).

To reduce vidicon microphonics, the shutter has a built-in damping mechanism and is attached to the camera housing by means of isolator bushings.

Shutter assembly covers were designed to mount over the shutter assembly and provide light seal protection.

The external magnetic shield assembly was replaced by an internally-mounted, two-part yoke shield which envelopes the yoke and protects it from external magnetic fields. A rear portion of the shield is an open end cylinder with three cutouts to fit over the yoke ears. It is made of 0.031-inch thick co-netic

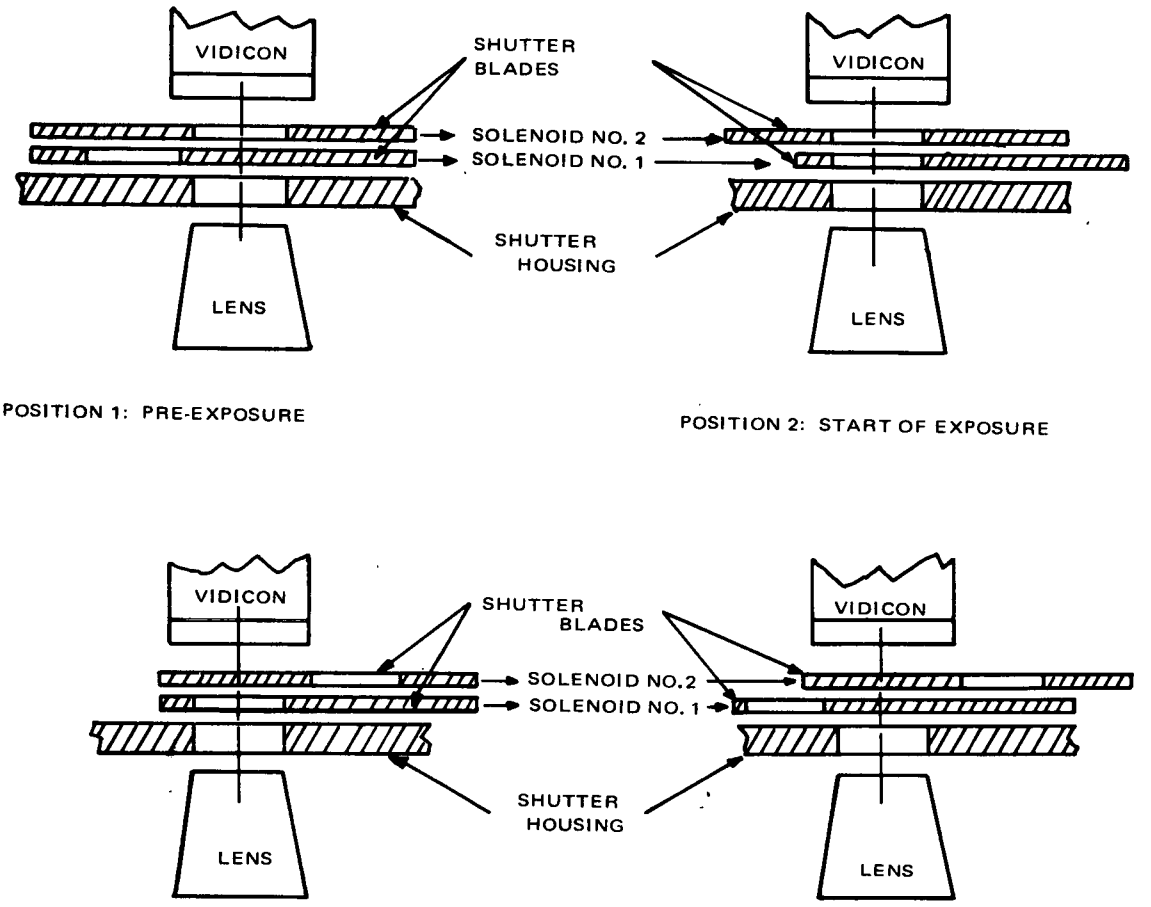


Figure 2-V-50. Shutter Blade Sequence of Operation

material and is potted onto the yoke's outside surface, thus becoming an integral part of the yoke. The front part of the shield, also made of 0.031-inch co-netic material, is shaped like a cup with a 0.75-inch diameter cutout for the vidicon faceplate. After installation of the light ring assembly, this shield is slipped over the front part of the yoke. The area where the front part of the shield overlaps the rear part is clamped together with a circular clamp. The clamping ensures continuity of the shield.

A cutout was incorporated into the vidicon faceplate to facilitate the forward protrusion of the double-bladed shutter assembly.

2. Camera Lens

The camera lens, used to focus optical images on the photoconductor in the vidicon, is located in a magnesium support tube which is mounted on the front of the camera housing. The lens is a Tegea-Kinoptic, 108-degree, wide-angle, f/1.8 type objective lens with a focal length of 5.7

millimeters, and is equipped with a manual iris adjustment. Radiation shielding is provided by a 0.250-inch thick fused silica window in front of the lens. A yellow haze filter, having a transmission at 530 millimicrons of not less than 80 percent, and a transmission at 480 millimicrons of not more than 5 percent, is used within the lens.

3. Vidicon Tube

The image sensor used in the APT camera sensor assembly is a high resolution, 1-inch diameter vidicon tube with extended image storage capability. Essentially, the tube is a conventional vidicon, but has dielectric properties so that it can store an image for the relatively long period that is required for APT camera system readout. As shown in Figure 2-V-51, the vidicon consists of the following elements: a target, which is made of metallic film (signal electrode) deposited on the inner surface of an optically flat glass faceplate, and a thin layer of photoconductive material which is deposited on the transparent metallic film; a separate wall and mesh electrode (G4); a focusing electrode (G3); an accelerating grid (G2); a control grid (G1); and a heated cathode. The faceplate of the vidicon has reticle marks to aid in determining

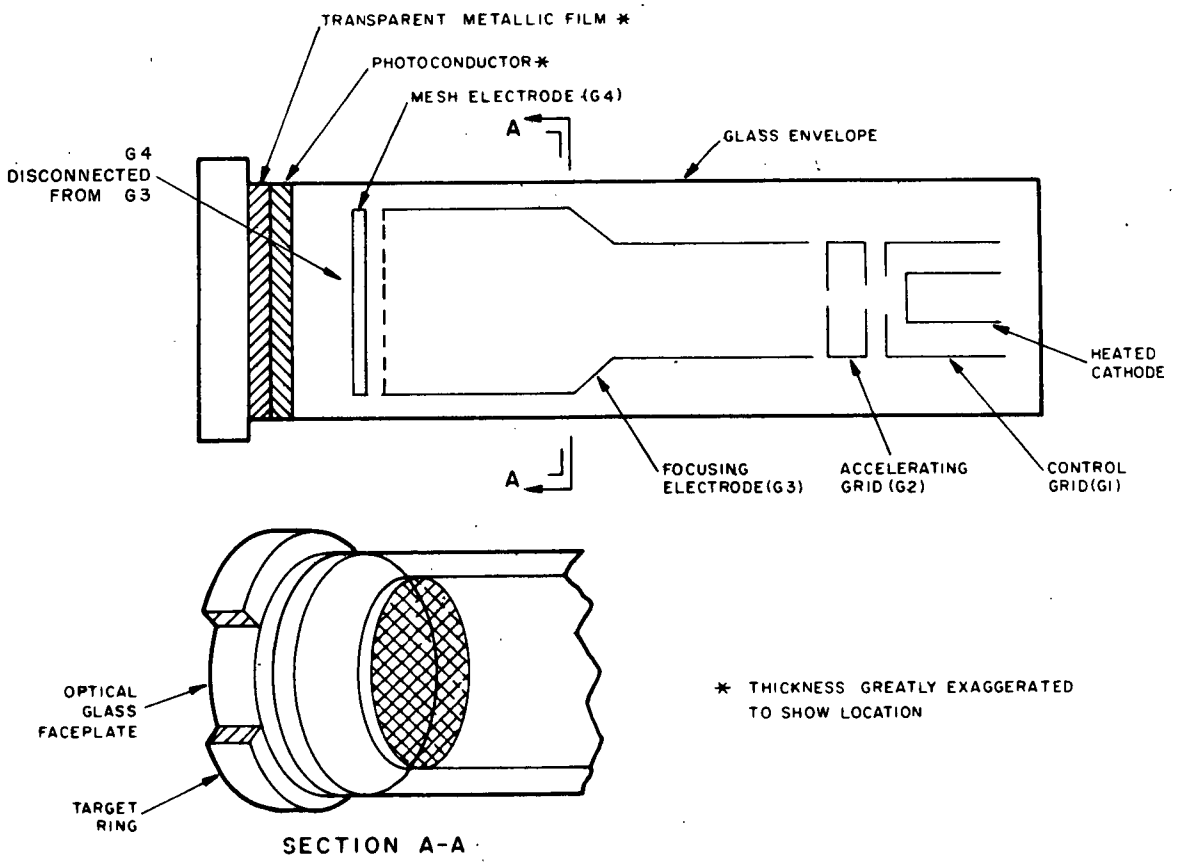


Figure 2-V-51. Vidicon Construction

cloud position during picture-taking operations. The reticle marks are transmitted as a part of the video information and are reproduced as part of the composite facsimile picture. (If distorted pictures are received from the APT camera, the reticle marks can be used to determine the nature and amount of distortion when the picture information is interpreted.) The configuration of the reticle pattern within the scanned area is shown in Figure 2-V-52. This pattern consists of 25 reticle marks evenly spaced over the raster area. The line width of each mark is 1 mil; i.e., twice the width of a scanning line.

4. Focus and Deflection Yokes

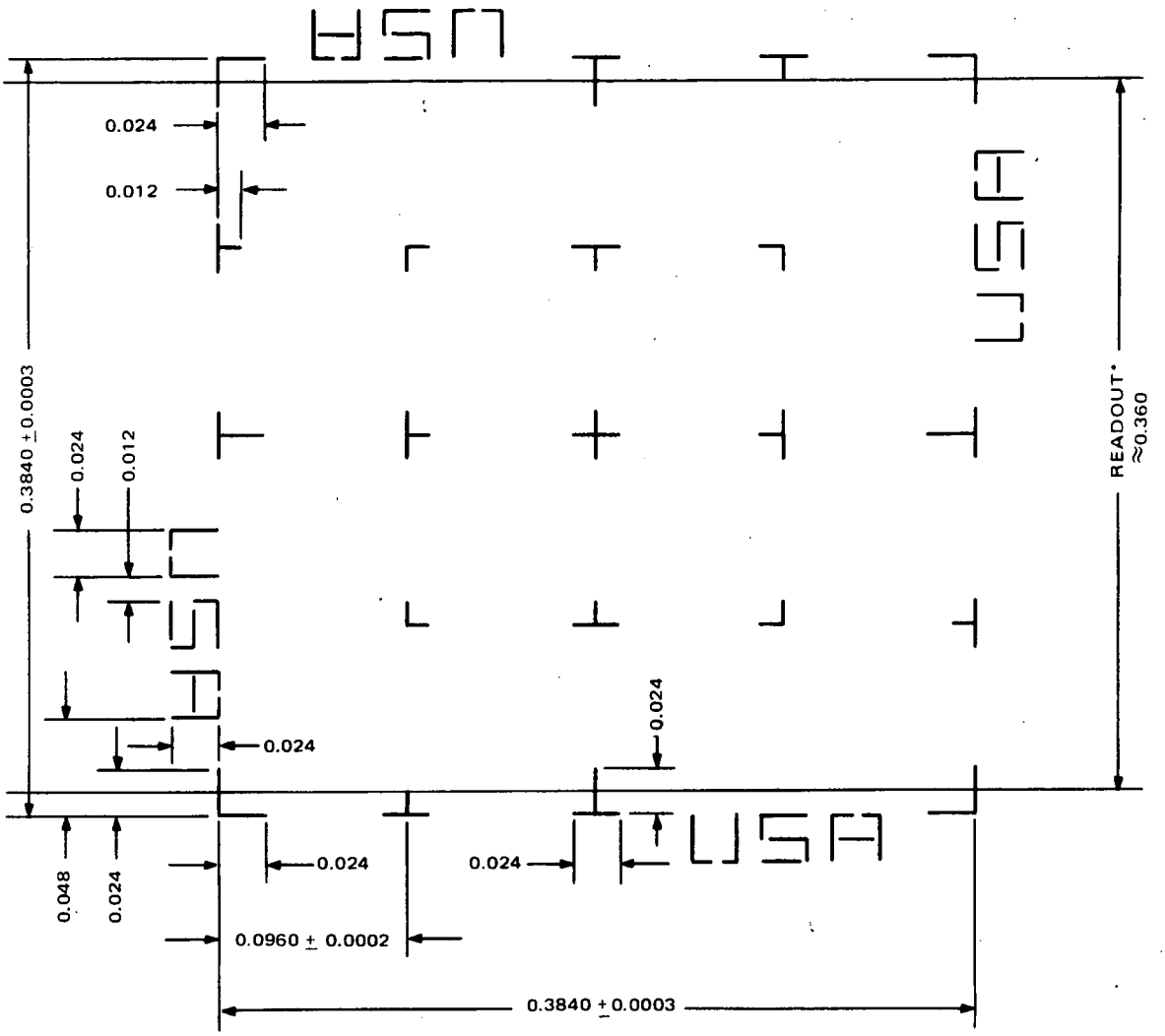
The electron beam is focused at the surface of the photoconductor by the combined action of the electromagnetic field of the focus coil and the electrostatic field of grid G3. Horizontal and vertical deflection of the beam across the photoconductor face is accomplished by the transverse electromagnetic fields produced by the deflection yoke windings. Alignment coils serve to position the undeflected beam properly.

5. Shutter Mechanism

The ITOS APT camera utilizes a solenoid actuated, double-bladed focal plane shutter assembly for optical exposure of the vidicon (image sensor). Two timing signals, derived from the sequence timer logic in the camera electronics assembly, provide pulse inputs to the shutter drive circuit (also in the camera electronics unit) to control operation of the shutter mechanism.

Optical exposure of the vidicon begins at time T3 of the camera timing cycle (Figure 2-V-48) immediately after the 5-second "prepare" interval. Sequential application of two 50-millisecond shutter pulses ("start expose" and "end expose") occur in the center of the 1-second "expose" interval (T3 to T5B) at times designated T5A1 and T5A2. The delay between the leading edges of these two shutter pulses determine the exposure time, about 25 milliseconds. The shutter blades move sequentially from one side of the camera lens to the other side as shown in Figure 2-V-50.

Shutter actuation occurs during vertical retrace time, at the conclusion of which the horizontal and vertical scan pattern is resumed for readout of the data imaged on the vidicon. Exposure alters the uniform charge pattern of the vidicon photoconductor by causing each resolution element to discharge in proportion to the amount of incident light. Readout of the stored image commences after a 2-second delay following the exposure interval, and lasts for a period of 150 seconds (during T6 and T1). At the completion of "read" (at T1), the "hold" period commences and this interval is determined by the spacecraft programmer. Upon receipt of the next "prepare" command, the next PED-read cycle commences.



*THE READOUT LIMITS INDICATED IN THE DRAWING ARE THE APPROXIMATE LIMITS OF THE 600-LINE APT SCAN. THE PORTIONS OF THE RETICLE PATTERN OUTSIDE THE SCANNED AREA WILL NOT APPEAR IN THE APT PICTURES.

Figure 2-V-52. Vidicon Reticle Pattern

6. Video Preamplifier and Amplifier

The video preamplifier and amplifier is a two-stage circuit comprising three board assemblies (BD4VAA, BDVAB, and BD4PA). The video signal from the vidicon target is in the form of 26-microsecond pulses and is coupled to a low noise nuvistor-type preamplifier. This amplifier produces a video signal having a high signal-to-noise ratio. The low impedance output of

the preamplifier drives a 24-kHz bandwidth video amplifier which provides a 1-volt, peak-to-peak output of sampled video information; this, in turn, is applied to the video inverter and detector in the camera electronics assembly.

(b) Camera Electronics Unit

1. Introduction

The camera electronics unit is made up of the elements shown in Figure 2-V-53.

2. Design Changes

a. SHUTTER DRIVE CIRCUIT

(1) INITIAL DESIGN CONSIDERATIONS AND CONSTRAINTS

For the ITOS APT shutter drive circuit, it was decided to provide shutter timing directly from the system logic thus avoiding the problem of generating timing intervals with independent timing circuits. The system sequence timer logic was, therefore, arranged to provide two shutter drive command pulses delayed from each other by the required exposure time. The shutter drive circuit was then required to utilize these pulses directly for shutter timing. Based on the above and other considerations, the design of the ITOS APT shutter drive circuit was subjected to the following general considerations and constraints:

- Reliable operation over required mission life under specified environmental conditions of the ITOS mission.
- Design to accommodate APT and AVCS camera systems without major change.
- Minimized power consumption.
- Compatibility with shutter and solenoid design.
- Shutter operation determined by two command timing pulses derived directly from APT system sequence timer logic.
- Shutter operation to be in direct synchronism with shutter command pulses as shown in Figure 2-V-54.
- Protection of shutter circuit and solenoids against possible shutter command pulse "hangups" (command lines remaining in their "ON" state).

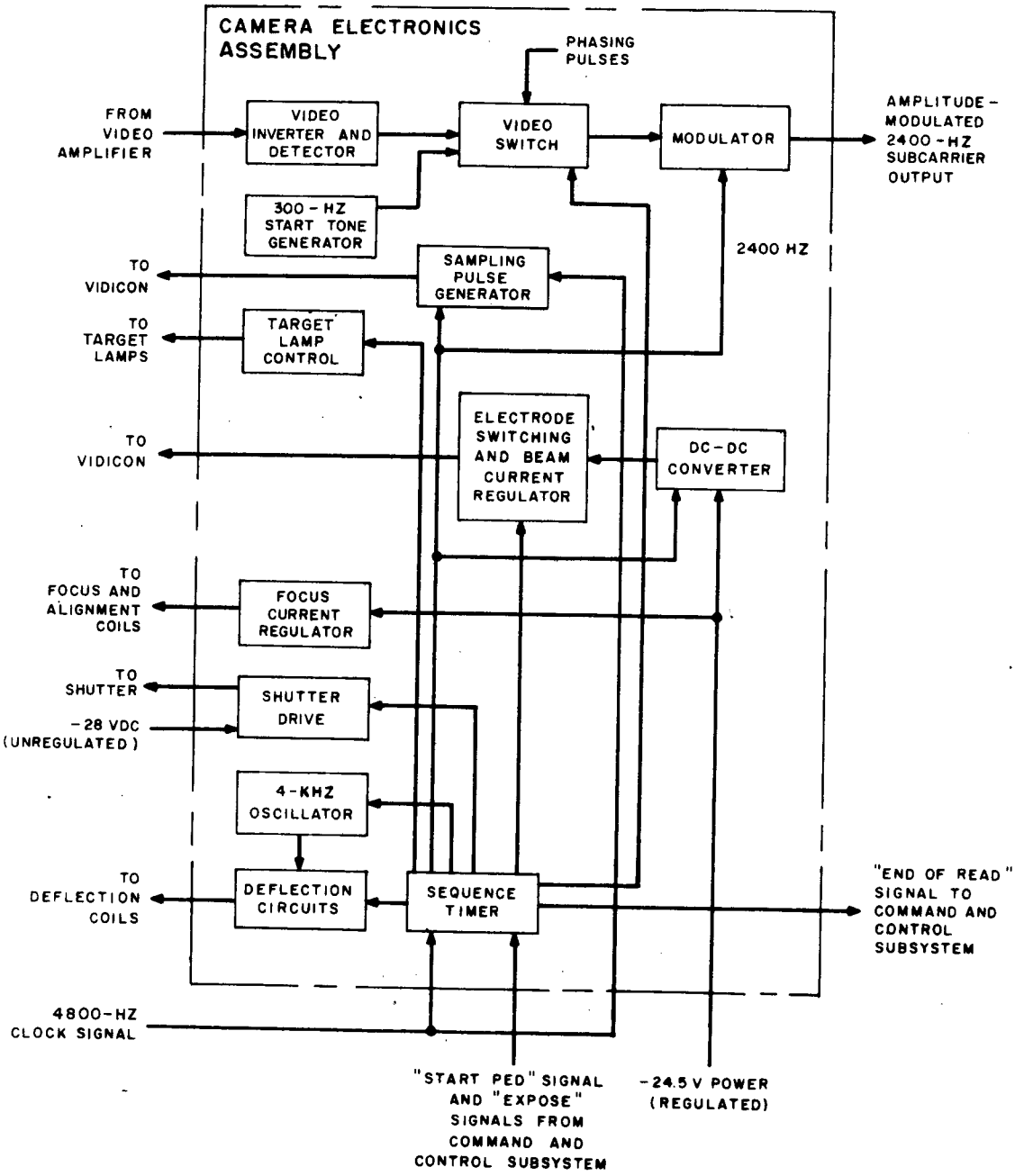


Figure 2-V-53. APT Camera Electronics Assembly, Block Diagram

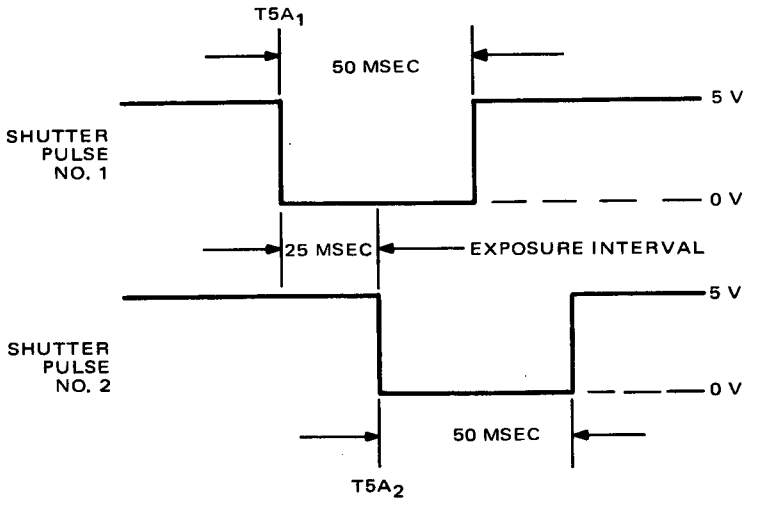


Figure 2-V-54. Shutter Command Pulses

- Minimized susceptibility to false shutter triggering from noise on command line inputs, power application sequence, and general circuit noise sensitivity.
- Operation of the solenoids directly from the unregulated -28-volt DC spacecraft bus (instead of the previous -24.5-volt DC regulated bus); remaining part of circuit to utilize voltage supplies available. Operation of the circuit to be over the normal tolerance ranges.
- Restriction of type of devices to be used in the design to those approved by the reliability group for TIROS M applications.

(2) DESIGN APPROACH

In order to satisfy the above requirements, the following general design approach was taken:

- Use of less noise-sensitive type of monostable circuits where required.
- Elimination of monostable circuits, where possible, and elimination of critical timing stability requirements on monostable circuits where used.
- Deactivation of shutter drive channels until a pulse of duration $\geq \Delta T$ is present on command input "A". Activation of shutter drive channels for a period only slightly in excess of that required to pass the two shutter command signals.
- Solid-state devices to be restricted to conventional diodes and transistors (no unijunction, SCR's, etc.).

- Minimization of number of supply voltages required.
- Use of low voltage supplies, where possible, to minimize dissipations and impedance levels.
- Use of noise filtering and thresholding, where possible.

Based on the design constraints and considerations, a shutter drive circuit was evolved as shown in the block diagrams of Figure 2-V-55 and 2-V-56. Because of the need for protection of shutter circuit and solenoids against possible shutter command pulse "hangups", the first approach shown in (a) of Figure 2-V-55 could not be used. A circuit that would automatically turn itself off in the event of command input "hangup" (constant application of a command "on" level) due to a command source malfunction was needed. The new designed circuit is characterized by the following items:

- The number of one-shot multivibrators has been reduced from three to one.
- The multivibrator type has been changed from the previous complementary type to the conventional type (one side on, other side off).
- The exact value of the one-shot timing period is no longer critical and may vary over a considerable range without adversely affecting circuit operation.
- A DC trigger stage is used to provide a positive triggering action relatively independent of command pulse rise time.
- Use of solenoid driver stages similar to the previously proven type.
- Noise filtering is employed to discriminate against short (T_n < 100 μs) pulse widths. Thresholding is provided by two series diodes at the input to driver stages.
- Transistor diode circuits are used throughout.
- Two supply voltages are used (exclusive of -28-volt DC shutter power).

(3) ETM SHUTTER TESTS

A shutter exposure uniformity test was performed on the ETM shutter. The exposure was checked at three points: right, center, and left portions of the format; the recorded times of exposure were 24.8, 25.0, and 25.5 milliseconds, respectively. The resultant maximum deviation from nominal (25.0 milliseconds) is 1.5 percent, well within the ±10-percent limit of the performance requirements.

The shock transmission test was performed on the ETM camera assembly and shutter assembly. The accelerometer readings on the camera housing indicated shutter shock transmission to be 6 G's. This is within the 7-G maximum limit of the performance requirements.

No built-up static electric charge on the shutter blades was detected during testing.

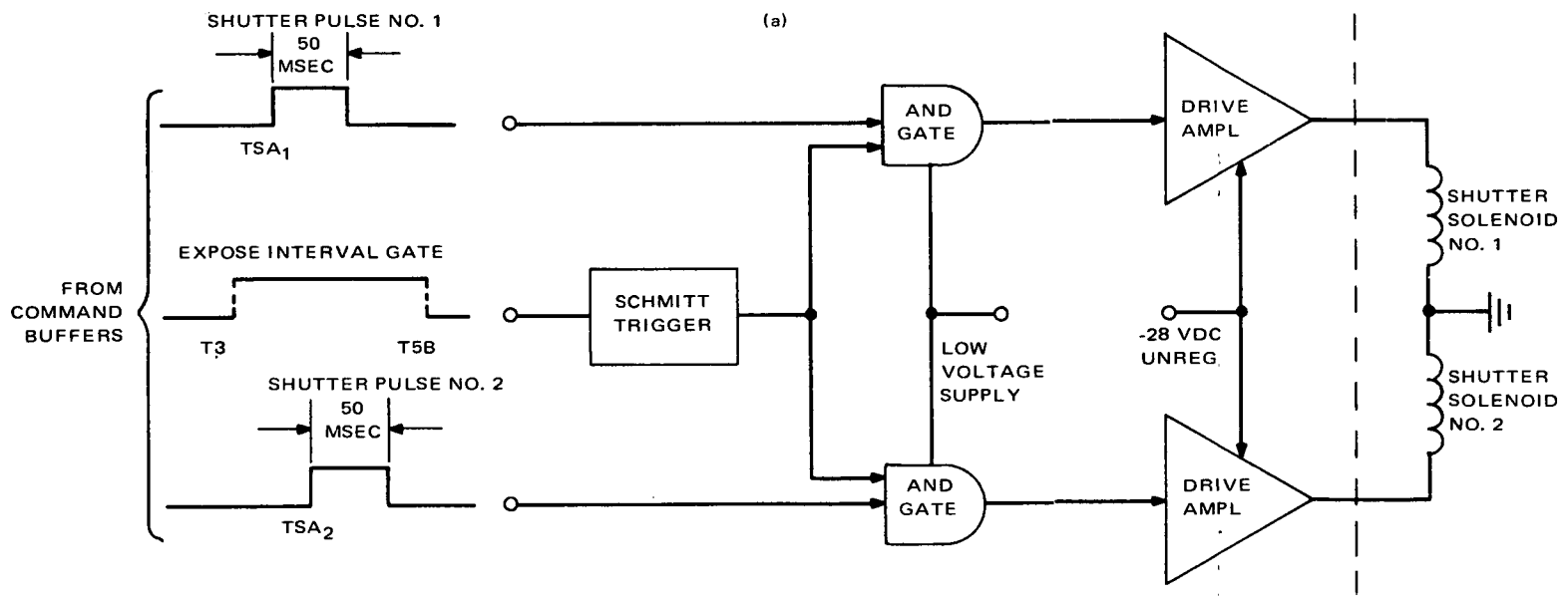
Accumulated shutter operations of 66,100 cycles showed no shutter failure during shutter life tests.

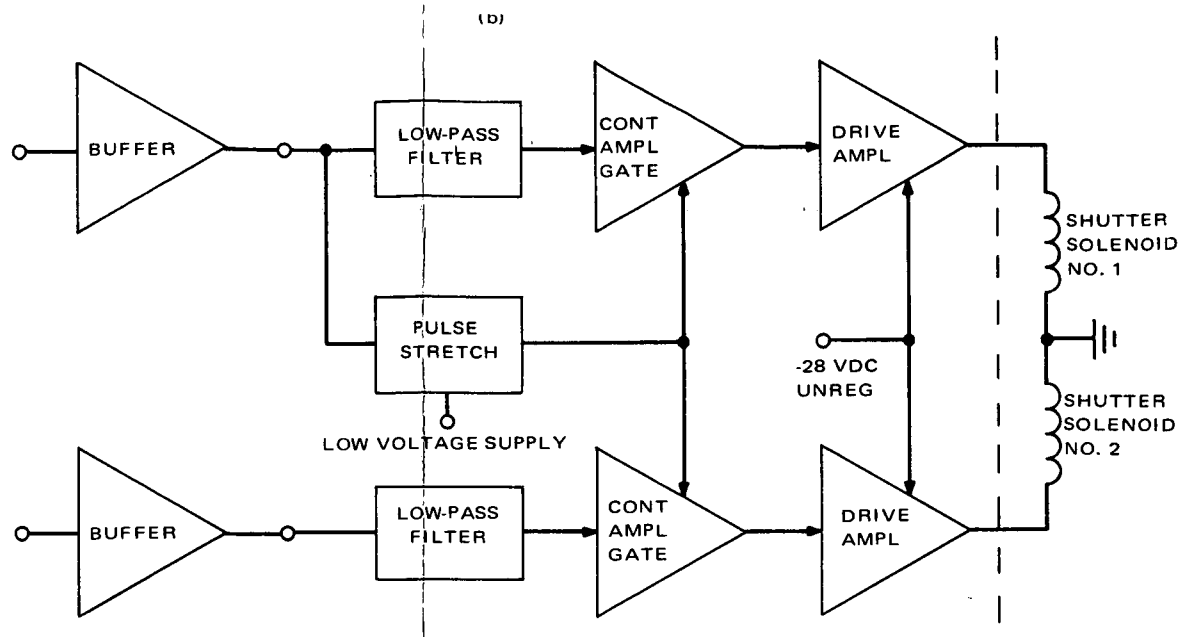
(4) BREADBOARD EVALUATION

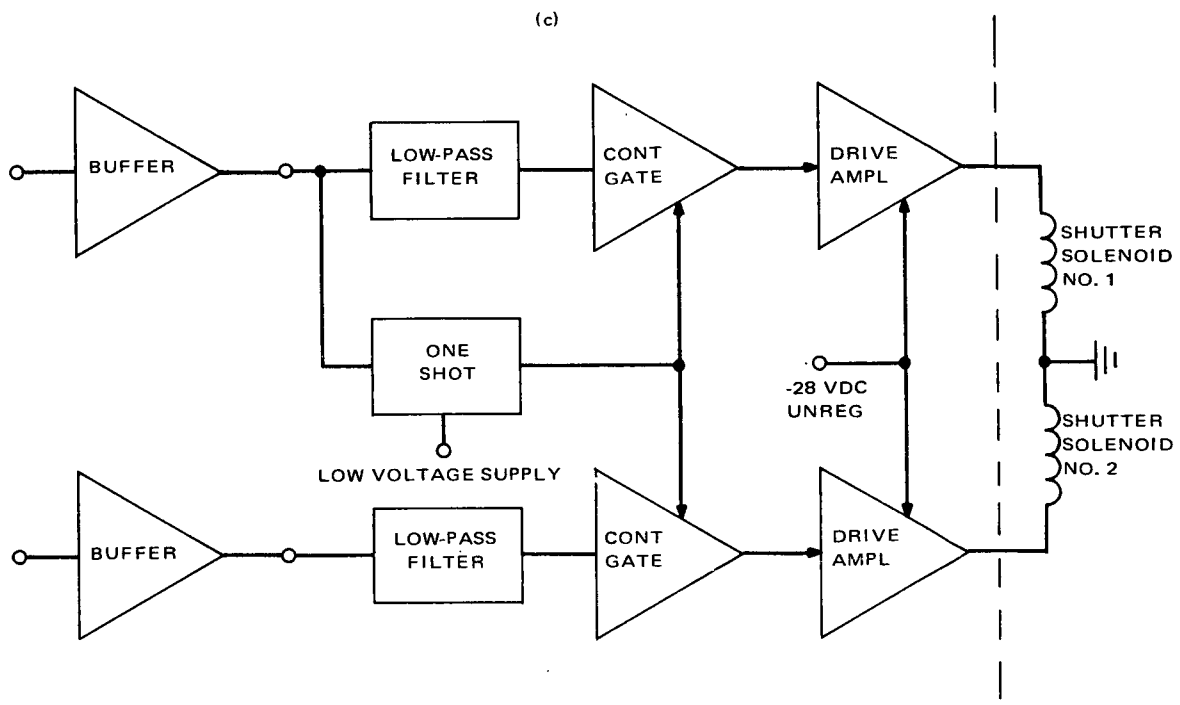
The APT shutter drive circuit (see Figure 2-V-56) was breadboarded and tested, and the general operating principle was verified. However, as a result of tests and design review evaluations, several items were deemed advisable. These were:

- Additional drive margin, above the indicated worst-case values, required to the output driver stages Q15, Q18 (A force h_{FE} of 10 was assumed instead of the (h_{FE}) minimum obtained from ITOS h_{FE} curves).
- Filtering at the input to the one-shot, in addition to the channel input filtering.
- Decoupling filter in the supply lead to the one-shot.
- Ensure that the minimum one-shot period over all worst-case values of circuit parameters is sufficient to pass both the command pulses.

To accommodate item (a), the interstage coupling network between Q10, Q11 and Q10, 15 was adjusted to provide the extra drive specified. This necessitated increasing the worst-case drive to Q10, Q11. Since at this time the +5.3-volt supply was used to supply reverse bias to stage Q10, Q11 base, it was decided to eliminate this reverse bias and make the circuit "off" state independent of the presence or absence of this supply. Thus, the base was returned directly to ground through an appropriate base return register. Since Q10, Q11 now had no reverse bias applied, it was felt some additional input threshold would be desirable. Therefore the resistive coupling between Q7, Q5 and Q10, Q11 was replaced by two series of diodes. This arrangement provided a relatively high and sharp input threshold to the drive amplifier as well as providing the extra drive required to Q10, Q11. Any noise signals at Q7, Q8 collector must exceed the level determined by the two series diodes and the base emitter junction of Q10, Q11 before they can affect shutter operation.







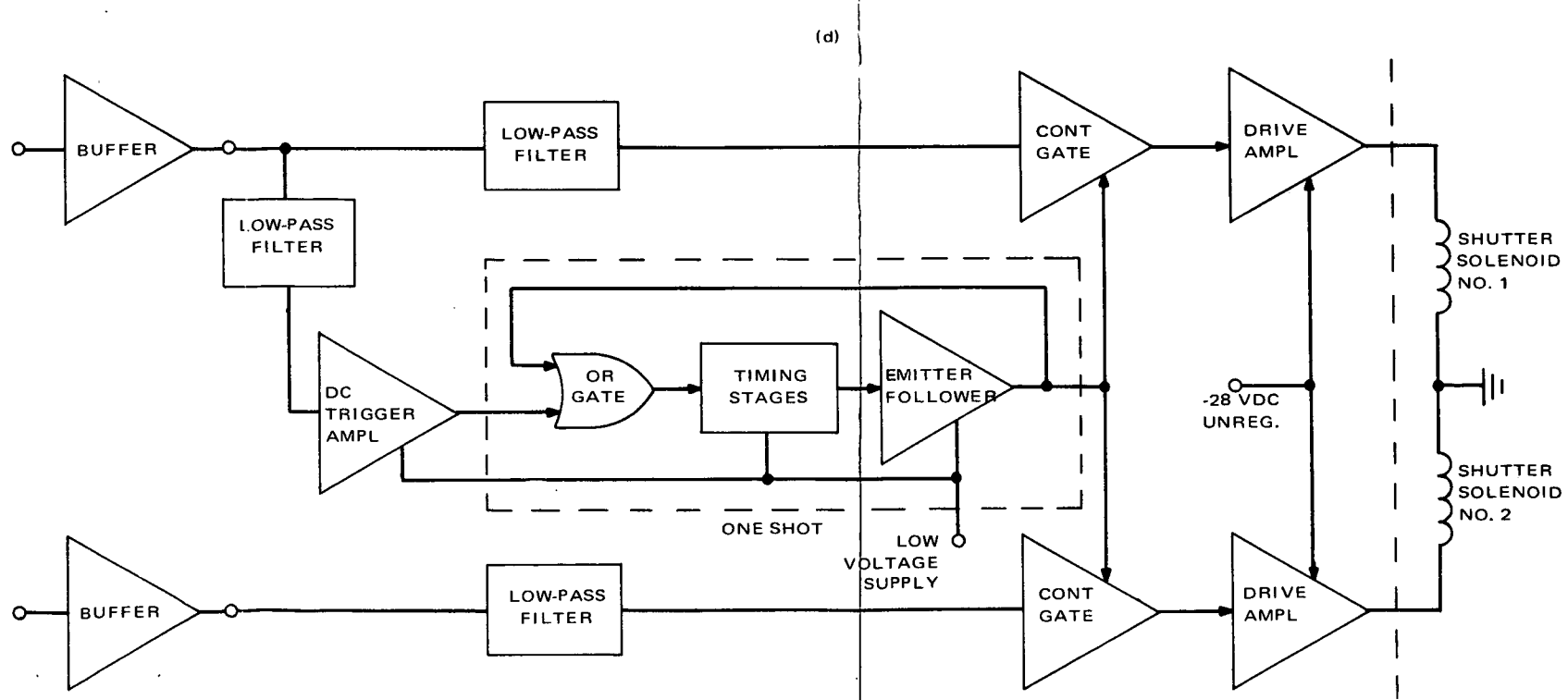


Figure 2-V-55. Evolution of Shutter Drive Circuit, Block Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

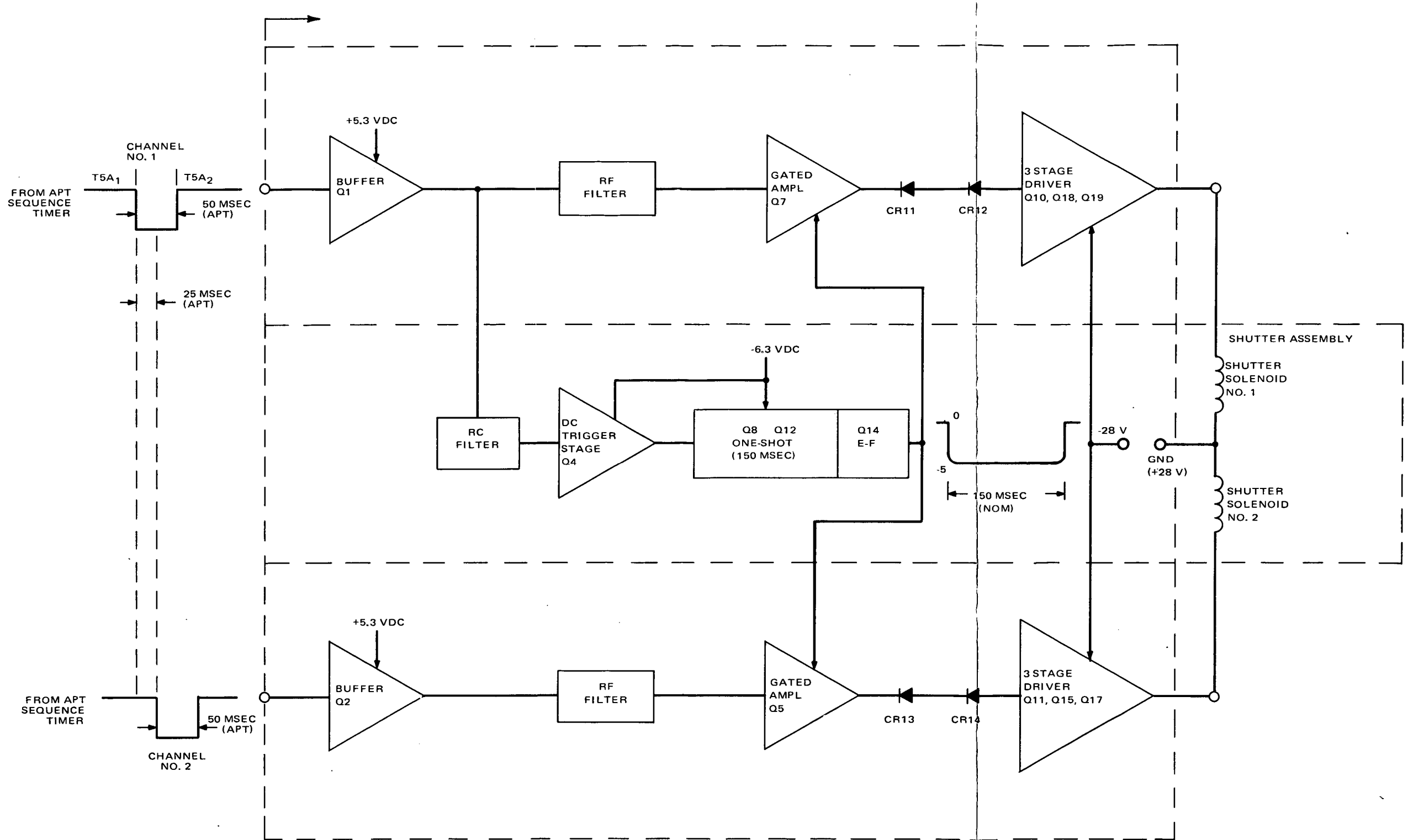


Figure 2-V-56. ITOS APT Shutter Drive Circuit, Block Diagram

To accommodate item (b), an RC filter similar to that used in the shutter drive channels was added at the input of the DC trigger stage of the one-shot. This filtering acts to provide some noise immunity to false triggering of the one-shot by short noise pulses, just as in the command channels. The filtering is necessarily restricted to short pulses (0.1 millisecond) in order not to appreciably affect the one-shot trigger pulse rise time or delay.

Item (c) was affected by insertion of an RC network in the common -6.3-volt supply to the one-shot stages Q8, Q12, and Q14. This provided a small delay upon application of the -6.3-volt supply to ensure that the DC trigger stage, Q4, was "on" and saturated before appreciably voltage was applied to the one-shot portion. This decoupling also attenuates any noise on the -6.3-volt supply line transmitted to the emitter follower output when activated.

The one-shot period variation of item (d) over worst-case environmental parameter ranges was investigated and suitable resistance values chosen in the timing-sensitive portion to ensure the required minimum period; this guarantees that shutter command trailing edges control the release time of the shutters. This is necessary since the shutter blade return times are staggered to prevent any possibility of partial reexposure due to possible overlap of shutter blade apertures during return. This overlap may occur if release of the first and second shutter blades occur close in time.

The one-shot controlled channel activation effectively protects against command "hangup" conditions, limiting the maximum possible shutter energization time to typically less than 150 milliseconds. Power supply sequencing caused no false shutter activation. Short duration noise pulses (0.1 millisecond) of full command amplitude (5.0 volts) at the input were effectively filtered. Circuit operation was checked at high and low tolerance levels of the command pulse source.

Solenoid excitation pulse waveforms showed good rise times with tests over the temperature range (-10° to +55°C) indicating proper shutter circuit operation over the full range.

Complete camera system ETM tests also indicated proper shutter operation and exposure times over the required range.

(5) CIRCUIT DESCRIPTION

As shown in the block diagram of Figure 2-V-56, the shutter drive circuit contains two identical shutter drive channels which accept shutter command pulses at their inputs and deliver corresponding shutter solenoid excitations at their outputs. The channel transmission is interrupted until a common one-shot is triggered from a channel No.1 input signal. At this time, both channels are activated and prepared for the period of the one-shot, to amplify an command signals appearing at the respective inputs. After return of the one-shot

to its untriggered state, the two channels are once again deactivated and are inactive until the one-shot is triggered again.

Each shutter drive channel consists of a 3-stage solenoid driver amplifier preceded by a controlled (gated) amplifier stage Q7, Q5. Gated amplifier Q7, Q5 is preceded by a DC low pass coupling network driven from a command buffer stage Q1, Q2. The 3-stage solenoid drive amplifier consists of the output solenoid power drive transistors Q17 and Q19 which together are capable of handling the required solenoid drive currents and voltages. This stage is driven, in turn, by Q18, Q15 which provides the required base drive to Q17, Q19 when driven into saturation by Q10, Q11. Driver Q10, Q11 provides the required level shifting and voltage gain to transfer signal levels from the low voltage input stages to the -28-volt DC unregulated solenoid supply. Driver Q10, Q11 is coupled to driver Q18, Q15 through two diodes CR11, CR12 (or CR13, CR14). These diodes, in conjunction with the base emitter input characteristics of Q10, Q11 provide an input threshold to Q14.

Q5, Q7 is a controlled (gated) amplifier stage. Its collector and base bias voltages are derived from the output of a one-shot circuit. When this one-shot is triggered, these bias voltages are presented to Q7, Q5 through emitter follower Q14 and, in the absence of a command input, are caused to saturate with their collectors being clamped near ground. Thus, the input to the following solenoid driver amplifier is clamped "off" and the shutters are not energized. If the one-shot is not triggered, the collector and base bias voltages of Q7, Q5 are essentially zero, blocking the channel at this point.

If a command output from Q1, Q2 and bias voltages to Q7, Q5 are simultaneously present, Q7, Q5 will be driven toward cutoff. This provides drive to Q10, Q11, driving it into saturation and resulting in the consequent turn-on of Q17, Q19 and application of the -28-volt DC unregulated supply to the solenoid. The coupling network between buffer Q1, Q2 and Q7, Q5, the controlled stage, consists of an RC low pass network which provides some measure of noise filtering. This network provides an integrating time constant sufficient to discriminate command pulses from noise pulses of less than approximately 0.1-millisecond duration. Thus, input pulses somewhat in excess of 0.1 millisecond are required to energize the channel. Q1, Q2 functions as a command buffer stage and provides a standardized command source characteristic.

The one-shot circuit consists of three basic sections: a DC-coupled trigger inverter stage Q4; a two-stage pulse generating section Q8, Q12; and an emitter follower output stage Q14.

The DC-coupled trigger inverter stage Q4 provides a DC-coupled trigger to the one-shot section. This trigger stage, normally in the saturated state, is driven "off" from the command pulse from Q1 driving the No. 1 shutter channel. An RC low pass network is used at its input and functions as in the

case of the shutter channels. When the recommand input No. 1 occurs, the resulting signal to the trigger stage turns if "off". This provides a trigger signal to Q8 of the one-shot initiating the timing period. This DC trigger stage provides improved triggering reliability of one-shot by eliminating the conventional capacitor-diode trigger network.

At the initial portion of the one-shot period, Q8 receives its base drive from both the trigger stage (Q4) and the one-shots own feedback loop, CR5 and R30. The drive contribution from the trigger stage Q4 ends with the termination of the command pulse No. 1; the hold-on drive to Q8 then being supplied by the feedback loop alone for the remaining portion of the one-shot period. The decoupling diode CR1 reverse biases when the trigger stage Q4 goes back into saturation at the end of the command pulse No. 1 period, thus preventing extra loading on the one-shot feedback loop.

Once the one-shot is triggered, the normal timing sequence takes place. That is, Q8 is driven into saturation suddenly applying a step transient of approximately +6 volts through C4. This step reverse biases Q12 with diode CR6 used to absorb some of the reverse bias in order not ot exceed $(V_{BE})_{Rev.}$ rating of Q12. The conventional recharging of C4, through R28, takes place until the voltage at the cathode of diode CR6 has fallen sufficiently to begin turning Q12 back "on". This recharging time determines the one-shot period which is nominally about 150 milliseconds. The activated period of the one-shot is used to control the time that bias voltages are applied to the controlled stages Q5 and Q7, controlling the activation of the two shutter drive channels. The emitter follower Q12 provides a low impedance source for the controlled bias voltages for Q5 and Q7 as well as a source for the one-shot's own feedback loop avoiding loading of the one-shot output directly. The diode CR5 in the one-shot feedback loop provides isolation of the emitter follower output from the trigger stage.

b. SEQUENCE TIMER

(1) GENERAL

The sequence timer is that section of the APT camera electronics assembly which generates all timing signals required to produce the sequence of operations of the APT picture-taking cycle.

While the main functions of the ITOS sequence timer are similar to those of previous APT camera systems, the implementation in terms of components and board assembly is of new design.

The ITOS sequence timer is implemented using integrated logic circuits as contrasted to previous use of discrete component circuits. The integrated circuits are of the DTL type. The entire sequence timer circuit is assembled

on a single 4-layer printed circuit type board. This design leads to a minimal number of component connections required as well as minimized interconnection lead lengths with an overall gain in reliability.

The construction consists of an interconnection pattern formed on the top layer. A second layer consists of a copper plate layer etched away in appropriate positions and provides a ground plane common electrode to which connections to the upper layer are made by appropriate solder-through-holes. A third layer similar to the second, except with different etched-away regions, serves as the 5.3-volt distribution plane. A fourth layer provides additional interconnection pattern and is needed to avoid crossovers in the first interconnection plane. This bottom layer is utilized by providing holes through the upper planes with etched-away-areas surrounding the holes through which connections can be made from the top layer to the bottom pattern, thereby providing additional interconnections without crossover. The various patterns are formed on epoxy boards which are sandwiched and bonded together, producing a single 4-layer board structure on which the integrated circuit flat packs are mounted by solder-welding the terminals to the printed circuit pattern. The resultant assembly constitutes a single, compact, lightweight unit.

The logic of the various integrated circuits employed is of the current sinking type and was chosen for its relatively low power consumption and good noise immunity. All integrated circuits are preconditioned and were subjected to various selection tests accordance with RCA Specification No. 1840890.

The sequence timer logic diagram is shown on sheet 2 of RCA 1976093, in the Logic Diagram Manual previously referenced. The basic form of the logic diagram consists of a continuous countdown from the basic input clock frequency (9600 Hz) through various blocks of counters and then finally through the 10-stage counter which drives the digital-to-analog converter. All required timing output signals are derived by decoding in integrated circuit gates and appropriate combinations of outputs at various points throughout the counter.

(2) SIGNAL INPUTS TO SEQUENCE TIMER

The signal inputs to the sequence timer are as follows:

- Clock Signal 9600 Hz (from spacecraft) - This is the main timing reference for the camera to which all counters and output waveforms are related.
- Prepare Pulse In (from spacecraft) - This pulse is used to initiate the beginning of the picture-taking cycle. This cycle takes 158 seconds (8-second PED + 150 seconds READ) after which the camera goes into a "hold" condition until another "prepare" pulse is received.

- Power Reset Pulse (applied by the power reset time circuit) - This input is initiated upon turn-on of power to the camera from an "off" state. It is used to preset the 10-stage counter to an intermediate point in the READ cycle such that, upon release of the preset signal (3 ±1 seconds), a partial read cycle (48 seconds) is generated after which the camera enters the "hold" state, a standby condition from which picture-taking cycles are initiated upon receipt of a "prepare" command. This 51 ±1-second total warmup period is provided to allow vidicon warmup and settling of various supply voltages. The warmup period used in the ITOS circuit is reduced from previous APT cameras because of ITOS system requirements.
- Supply Voltage and Ground - The single supply voltage to the sequence timer is +5.3 volts with its associated ground, and is derived as one of the supply voltages within the APT camera electronics assembly, replacing the earlier used +6.3-volt supply.
- "Reread" and Abbreviated "Read" (22 seconds) Inputs - These inputs are provided only for testing and are not used, as such, during normal camera operation.

(3) OUTPUT TIMING SIGNALS GENERATED BY THE SEQUENCE TIMER

The output timing signals generated by the sequence timer are as follows:

- Gated 4800 Hz - Provides trigger for 50-microsecond one-shot video sampling gate window.
- Cathode Pulse - Provides the sampling pulse input for vidicon cathode.
- 5-Percent Horizontal Sync - Provides the horizontal deflection sync and video blanking.
- Shutter Timing Pulses (two) - Provides pulse inputs to shutter drive circuit to control "start expose" and "end expose" of shutter.
- Target Lamp Timing - Provides input to target lamp switch, and regulator controls target lamp timing.
- "White" Clamp - Provides 300-Hz square wave start tone and horizontal phasing pulses during PED to the video processor for insertion in the video output for ground station synchronization.
- Video Clamp - Provides clamp timing signals (5-percent horizontal) to video clamp/DC restorer switch in video processor.

- Video Switch - Provides timing signals to video switch in video processor to control insertion of 300 Hz and phasing signals and "white" clamp level in video modulator.
- G1 Regulator Switching - Provides timing signals to G1 regulator to switch G1 voltage levels during the PED interval.
- Mesh and Target Relay Switching - Provides timing signals to the mesh and target relay drivers to switch mesh and target voltages during PED.
- Power Supply Sync - Provides a 2400-Hz square wave to the power supply chopper input to produce synchronization of the chopper switching transients between video sampling times.
- Video Modulator Carrier - Provides 2400-Hz square wave input as the carrier for the video modulator in the video processor.
- T1 - T6, PED Period Output - T1 - T6 is the PED period (8 seconds) which provides a control signal to the following circuits: G1 regulator, 4.2-kHz oscillator, vertical deflection, and hold and PED telemetry.
- 2- to 1/256-Hz, 10-Stage Divider Outputs - Provides binary inputs to the D/A converter which generates the staircase vertical sweep waveform.

(4) SEQUENCE TIMER VERSUS APT CAMERA CYCLE TIMING

Figure 2-V-58 shows the various input and output signals of the sequence timer and their respective timing with regard to the APT camera cycle.

The APT camera cycle consists of three main time intervals:

- "Hold", T1 - T1A = indefinite (determined by spacecraft programmer),
- "PED", T1A - T6 = 8 seconds, and
- "Read", T6 - T1 = 150 seconds

The PED position is further divided into three subdivisions:

- P = Prepare, T1A - T3 = 5 seconds,
- E = Expose, T3 - T5B = 1 second, and
- D = Delay, T5B - T6 = 2 seconds.

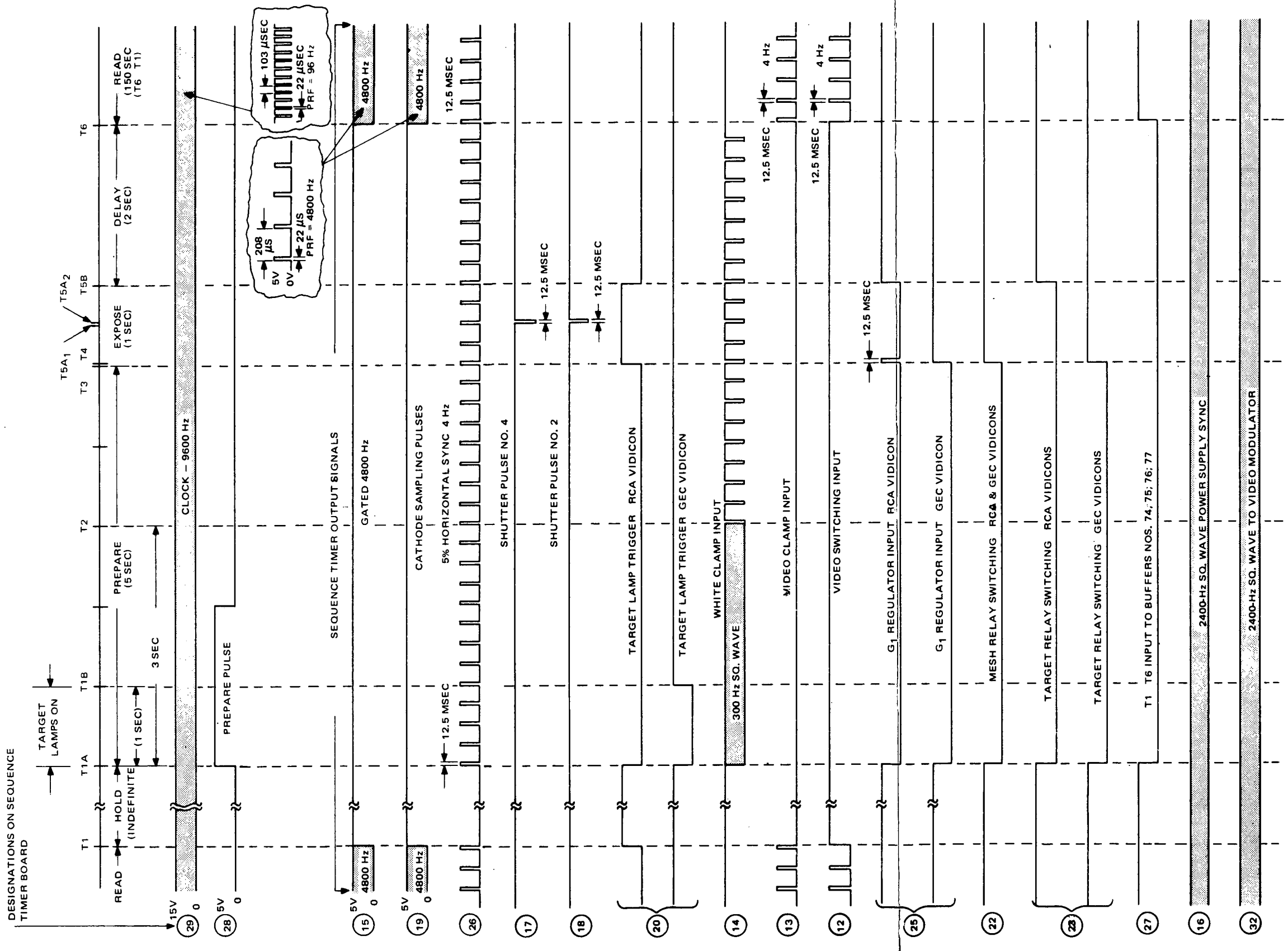


Figure 2-V-58. Sequence Timer Versus APT Camera Cycle, Timing Diagram

The shutter pulses occur in the center of the "expose" interval at times designated T5A1 = (T1A + 5.500 ±25 milliseconds) and T5A2 = (T5A1 + 25 milliseconds).

The readout of the stored picture occurs during the period T6 - T1. At completion of "read" (at T1), the "hold" period commences and is terminated upon receipt of the prepare command which initiates the next PED-read cycle.

All signal levels of the sequence timer are binary with logic "0" ≅ 0 volt and logic "1" ≅ 5 volts. Additional buffering, where required, is provided by buffer amplifiers external to the sequence timer board.

(5) SEQUENCE TIMER/APT CAMERA INTERFACE CIRCUITS

Matching circuits are required between the output characteristics of integrated circuits of the new sequence timer to the unmodified circuit portions of the APT camera subsystems. This matching was accomplished by adding suitable buffer stages or by modifying existing input circuitry. An effort was made to standardize, as much as possible, the buffer circuits where they occur.

These interface circuits, labeled with respect to the functional circuits which they buffer, are listed in Table 2-V-9.

Figures 2-V-59 through 2-V-74 show the schematics of these modified, added, or new interface circuits, enclosed in dashed lines, and indicate their respective board number assignments.

c. POWER SWITCH AND OVERVOLTAGE PROTECTION CIRCUIT

(1) GENERAL

The power switch and overvoltage protection circuit provides a command controlled application of the spacecraft -24.5-volt bus to the APT camera. In addition, the circuit contains an overvoltage protection feature which acts to turn off or inhibit application of the -24.5-volt spacecraft power to the APT camera subsystem in the event of abnormal voltage levels occurring on this bus.

The design of the circuit was subjected to the following constraints:

- Environmental specifications, as per Paragraph C.2.b (General Worst-Case Design Information).

TABLE 2-V-9. INTERFACE CIRCUITS

Interface Circuit	Figure
PA-62 — Cathode Sampling Switch	2-V-54
PA-63 — Target Lamp Switch	2-V-55
PA-64 — Prepare Command Input	2-V-56
PA-65 — Horizontal Blanking to Horizontal Deflection	2-V-57
PA-66 — Power Supply Sync	2-V-58
PA-67 — Clock Buffer	2-V-59
PA-68 — Target Relay Driver	2-V-60
PA-69 — Mesh Relay Driver	2-V-60
PA-70 — Subcarrier Generator Buffer	2-V-61
PA-73 — T1A - T3, T4 - T5B to G1 Regulator	2-V-62
PA-74 — T1 - T6 to G1 Regulator	2-V-63
PA-75 — T1 - T6 to 4.2-kHz Inhibit Input	2-V-64
PA-76 — T1 - T6 to Vertical Deflection	2-V-65
PA-77 — T1 - T6 to Hold and PED Telemetry	2-V-66
PA-78 — Start Tone, Phasing, and White Clamp	2-V-67
Power Reset Circuitry (modified)	2-V-68
Gated 4800 Hz to 50-microsecond one-shot	2-V-69

- Insertion voltage drop at full load not to exceed 0.3 volt.
- Operation of circuit directly from the -25.4-volt spacecraft bus.
- Compatibility with spacecraft command source.
- Turn-off or inhibition of power switch whenever main power (-24.5 volts) bus level "exceeds" a level V_T; where $25.0 < V_T < 28.0$ V with automatic return to normal operation when main power bus voltage returns below the V_T level.
- Reliable operation of circuit with overvoltages of the -24.5-volt bus to -36 volts.

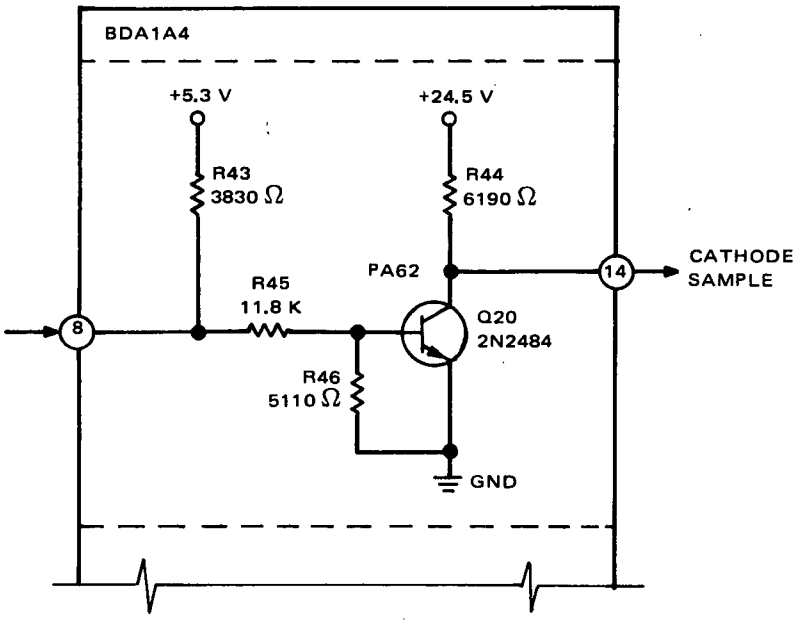


Figure 2-V-59. Cathode Sampling Switch Circuit

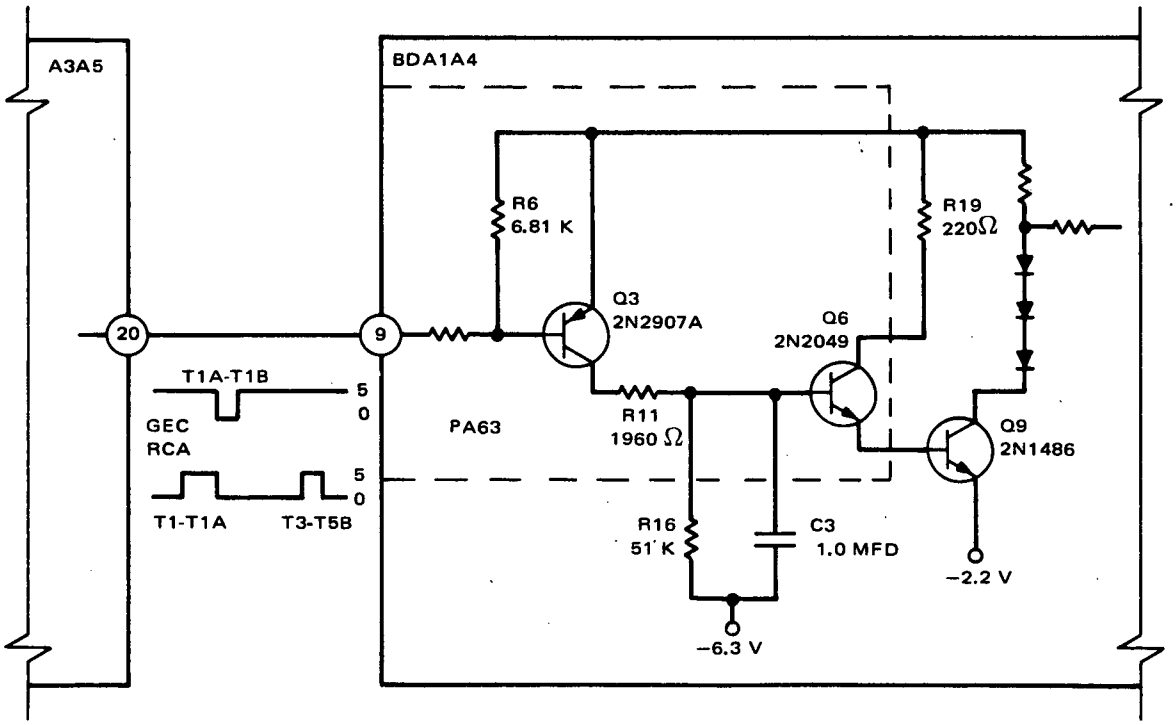


Figure 2-V-60. Target Lamp Switch Circuit

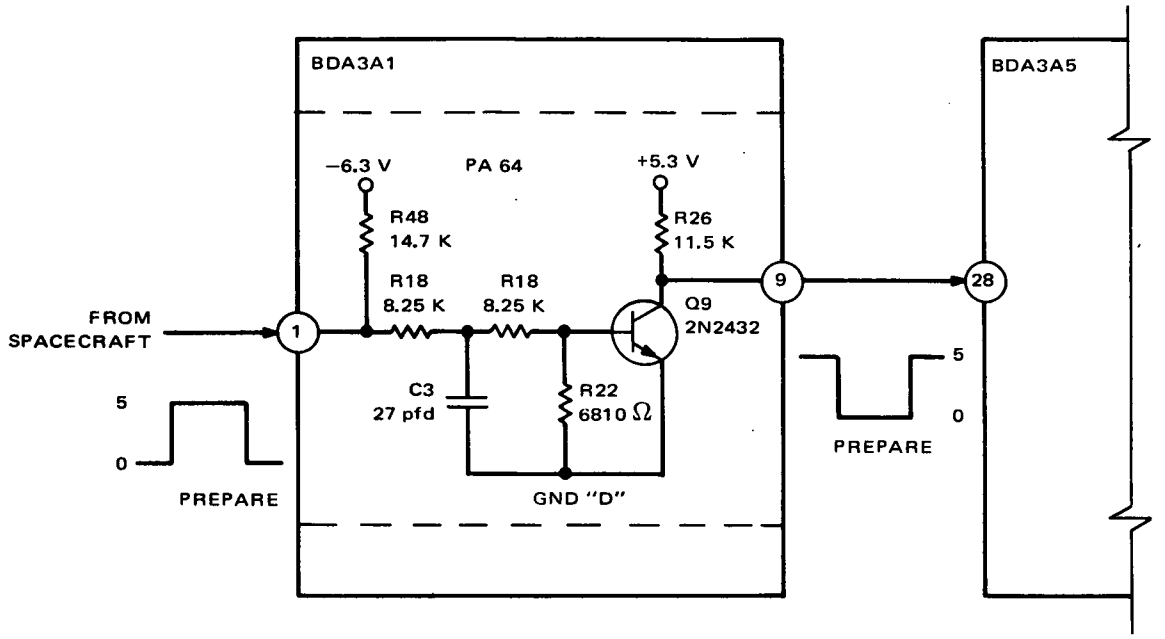
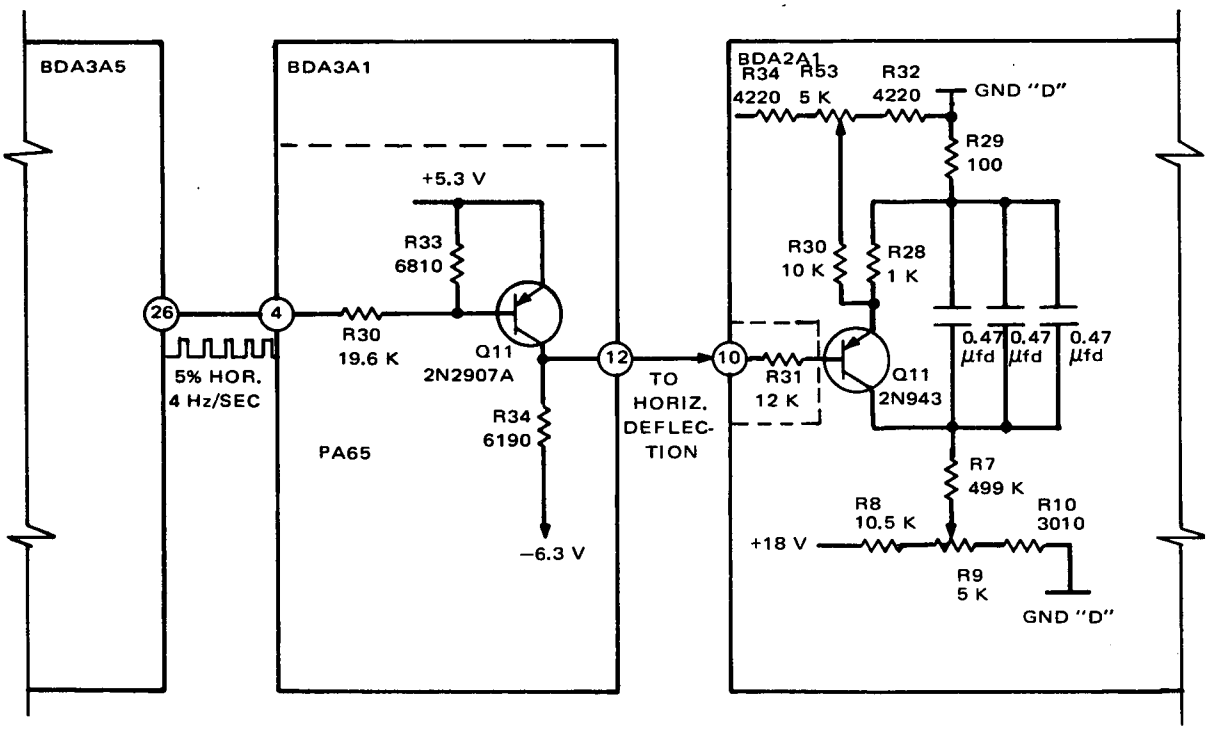
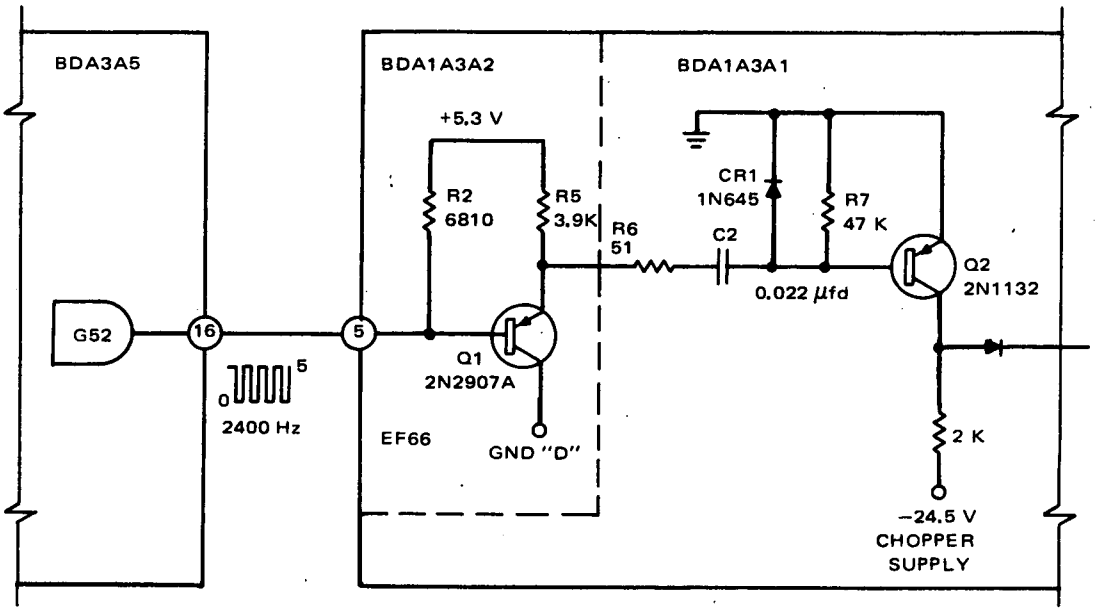


Figure 2-V-61. Prepare Command Input Circuit



NOTE: RESISTANCE IN OHMS UNLESS OTHERWISE INDICATED.

Figure 2-V-62. Horizontal Blanking to Horizontal Deflection Circuit



NOTE: RESISTANCE IN OHMS UNLESS OTHERWISE INDICATED

Figure 2-V-63. Power Supply Sync Circuit

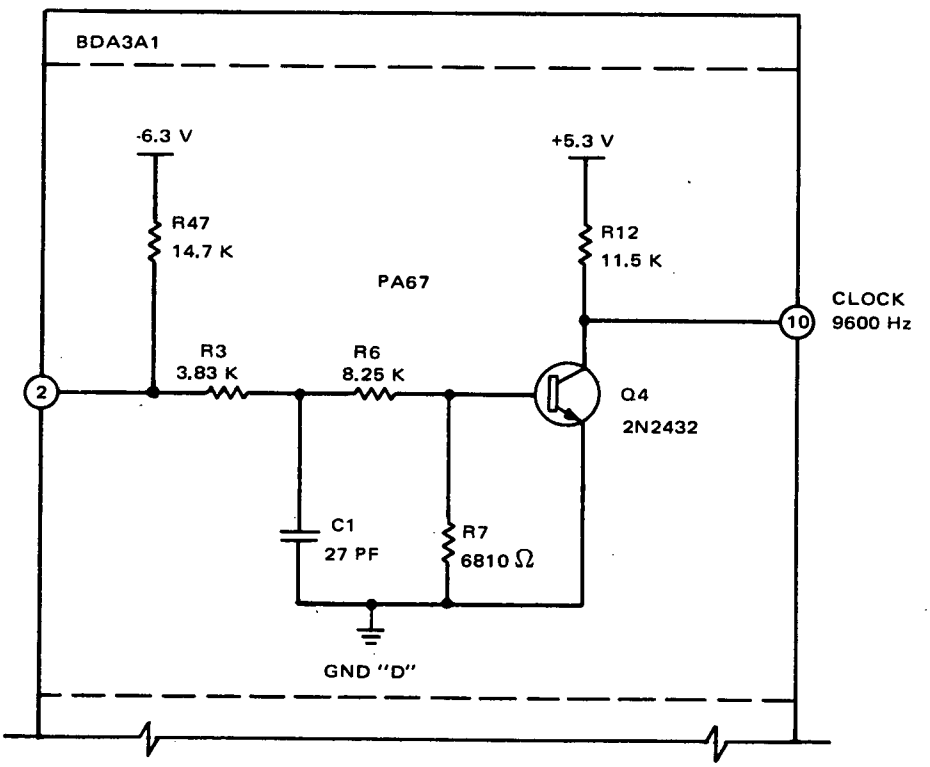


Figure 2-V-64. Clock Buffer Circuit

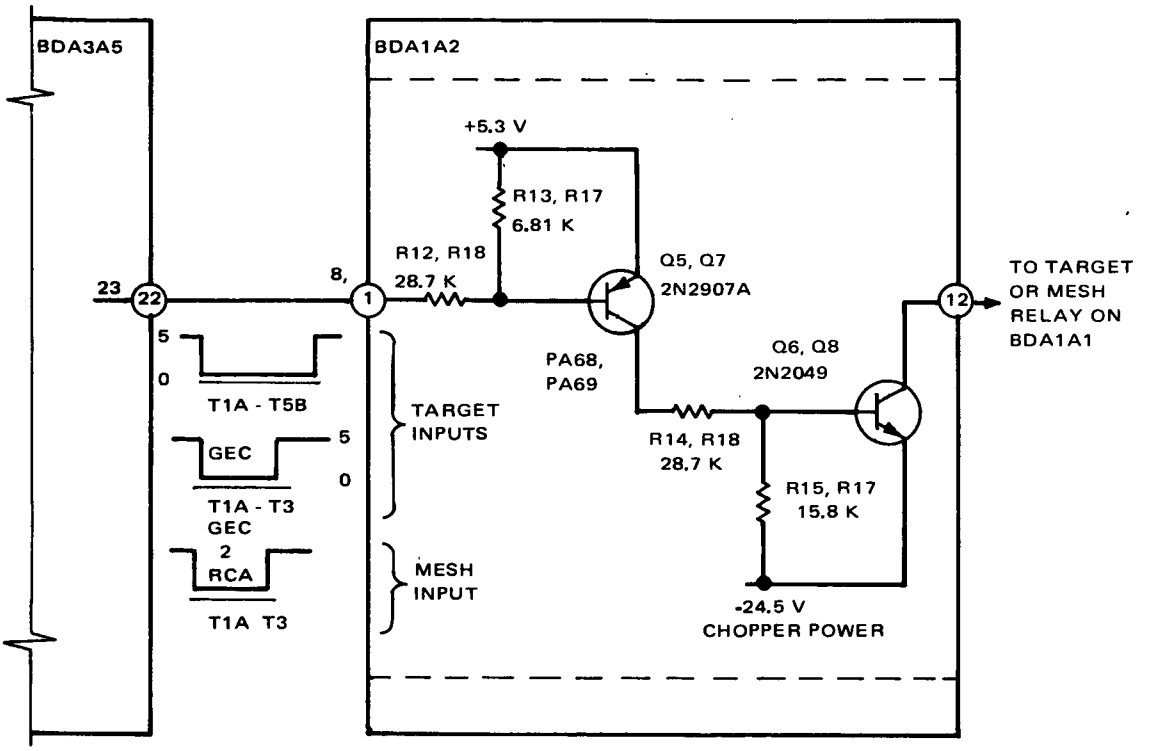


Figure 2-V-65. Target or Mesh Relay Driver Circuit

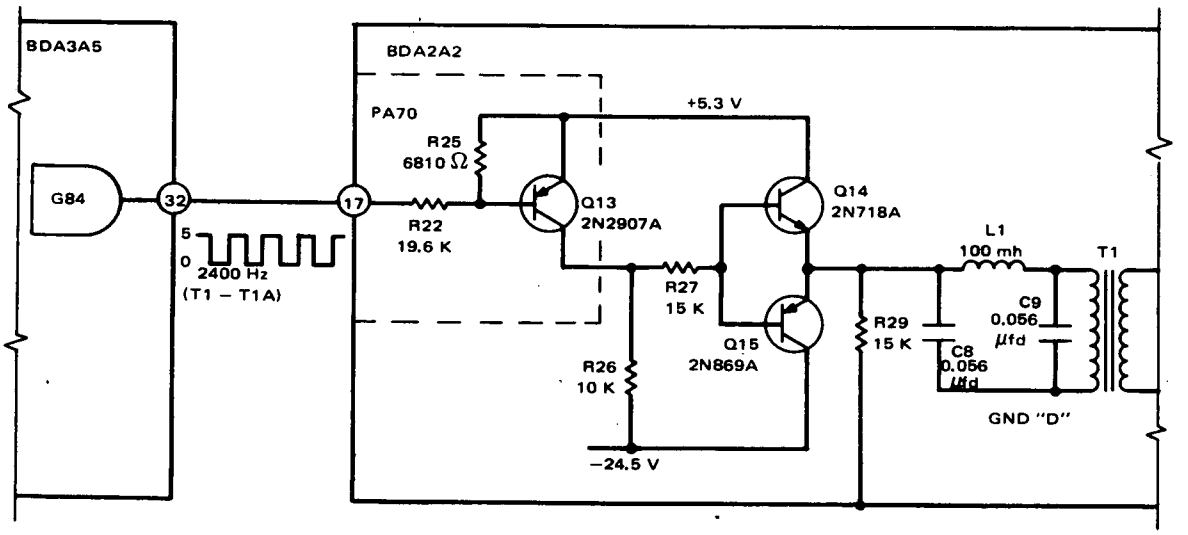


Figure 2-V-66. Subcarrier Generator Buffer Circuit

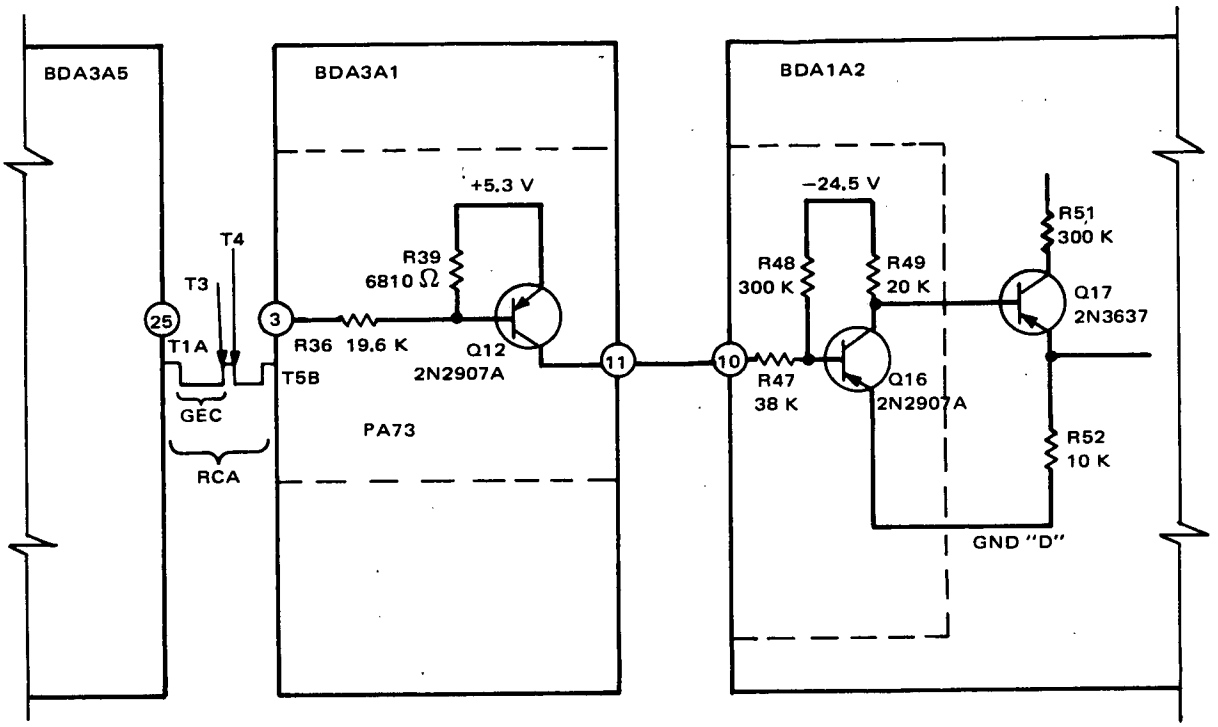


Figure 2-V-67. T1A-T3, T4-T5B to G1 Regulator Circuit

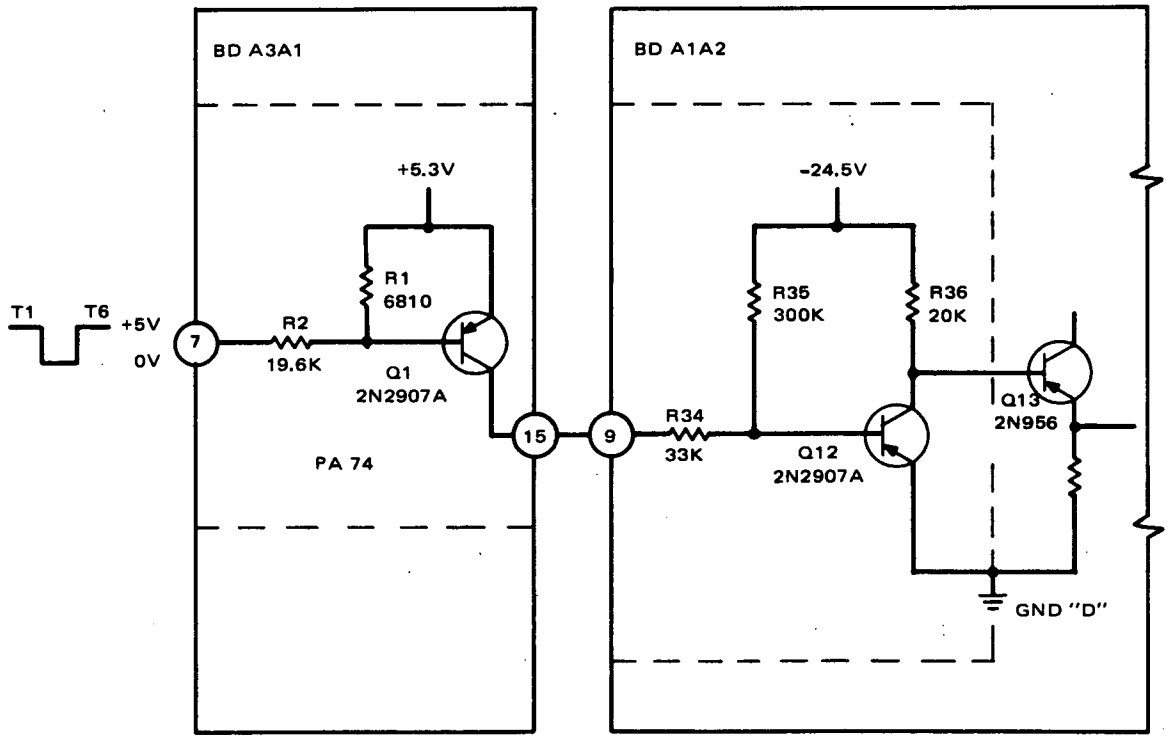


Figure 2-V-68. T1-T6 to G1 Regulator Circuit

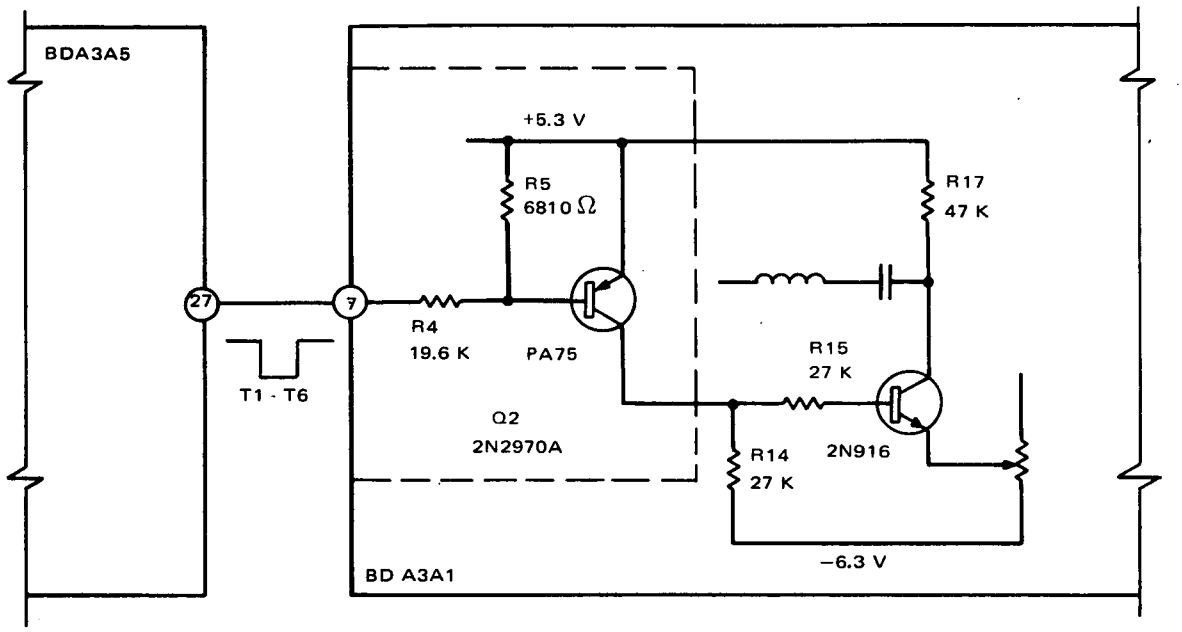


Figure 2-V-69. T1-T6 to 4.2-kHz Inhibit Input Circuit

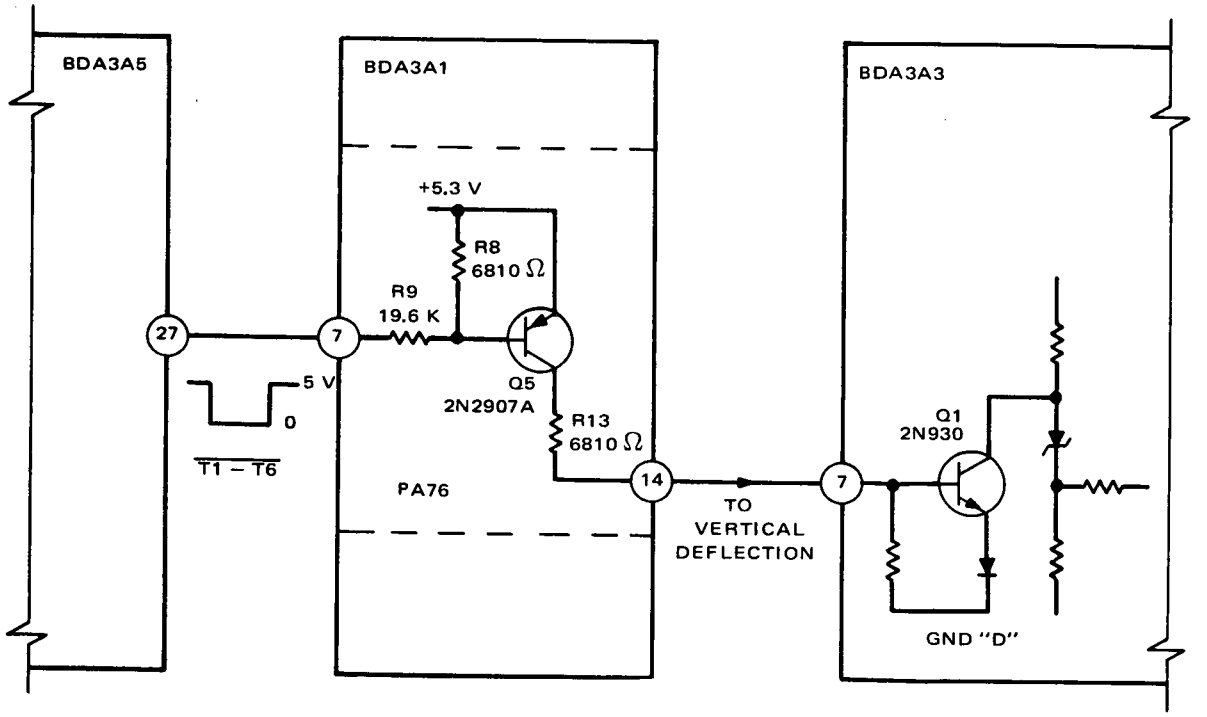


Figure 2-V-70. T1-T6 to Vertical Deflection Circuit

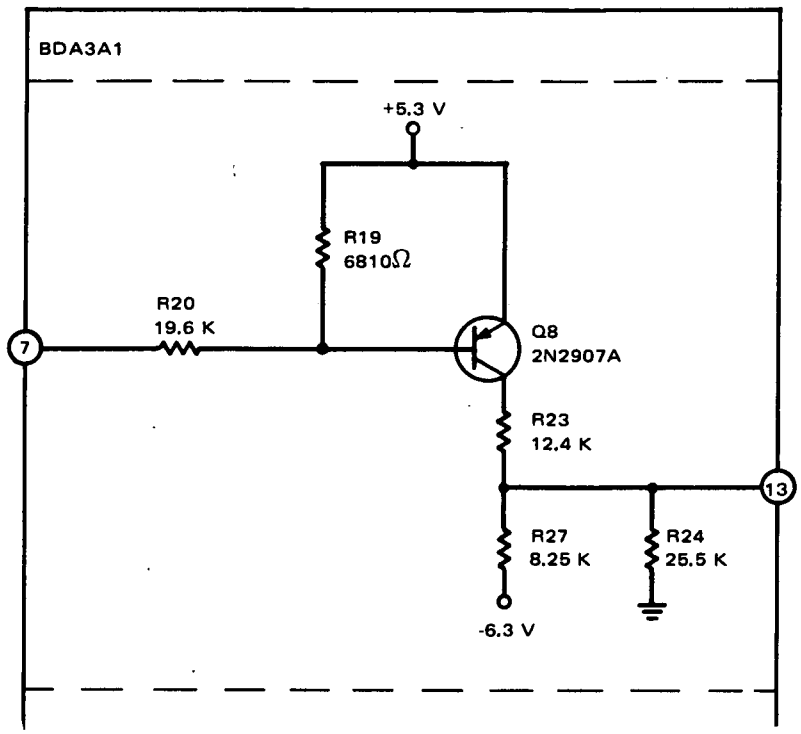


Figure 2-V-71. T1-T6 to Hold and PED Telemetry Circuit

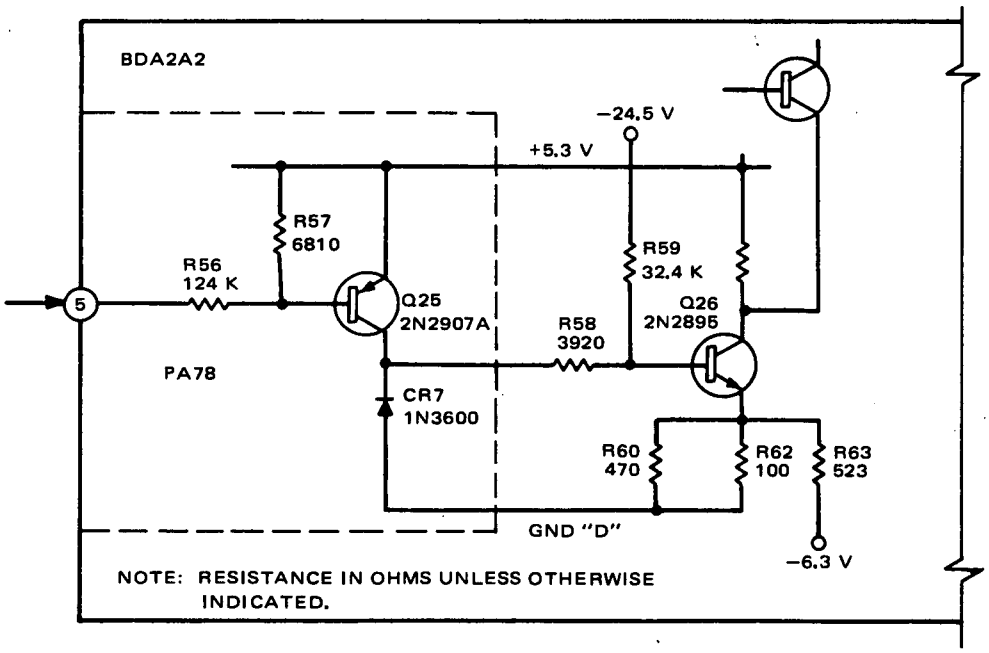


Figure 2-V-72. Start Tone, Phasing, and White Clamp Circuit

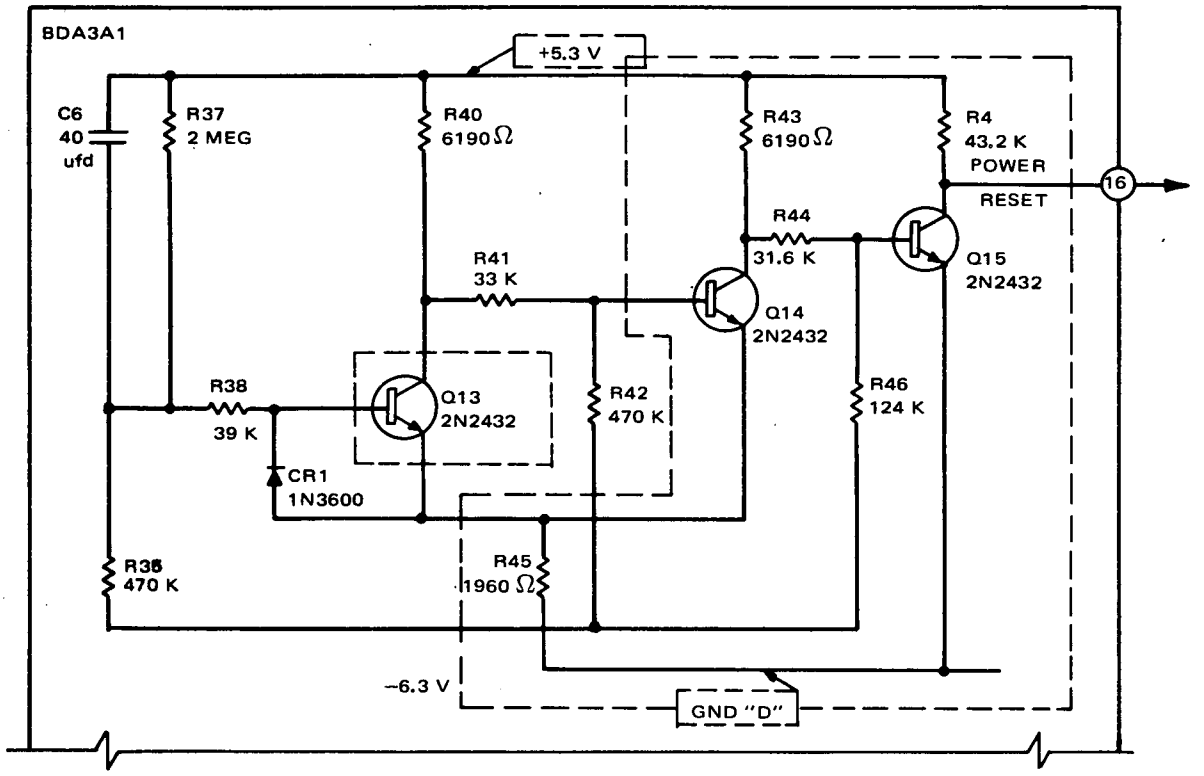


Figure 2-V-73. Power Reset Circuit

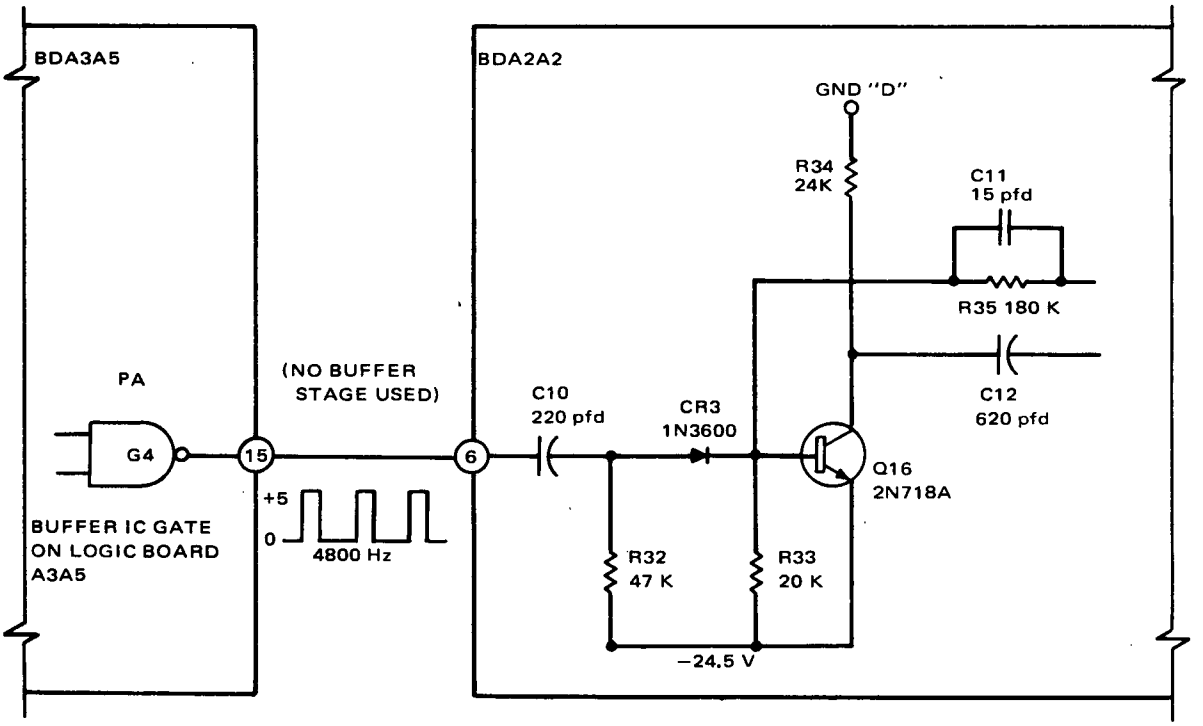


Figure 2-V-74. Gated 4800-Hz to 50-Microsecond One-Shot Trigger Circuit

- Minimal power consumption.
- Provision for specified overvoltage circuit response to -24.5-volts bus transients and speed of response to prevent damage to camera system.
- Minus 24.5-volt input turn-on surge current limits:

$$I_{in}\ (\text{surge})\ \max \leq 5\ \text{amperes}$$

$$\frac{dI_{in}\ (\text{surge})}{dt}\ \max \leq 5\ \text{milliamperes per microsecond.}$$

(2) CIRCUIT DESCRIPTION

The PSOP circuit comprises two functional sections: the power switch section and the overvoltage protection section. A block diagram of this circuit is shown in Figure 2-V-75, and the schematic of this circuit is shown in Figure 2-V-76.

The power switch section consists of a switching transistor, Q22, in series with the spacecraft -24.5-volt bus input to the APT camera. This transistor receives its drive from Q21 which, in turn, is driven by the common base input stage, Q19. The remaining stages are associated with the overvoltage protection circuit.

Upon appearance of a command "on" level (+5.0 volts) at the input, the power switch is driven onto saturation effectively connecting the -24.5-volt spacecraft bus to the camera input. The input stage Q19 acts as a buffer to prevent excessive loading of the command source in the spacecraft programmer whenever the overvoltage condition occurs. Thus, the common base buffer allows utilization of the maximum current drive available from the command source. The command source is shown in the schematic (Figure 2-V-76), and has a specified maximum loading of 1.8 kilohms. The "on" command at the input causes Q19 to be driven into saturation which provides a base drive to Q21 (Q20 is normally held of in the nonovervoltage condition). Driver Q21 is, thus, caused to turn on, applying base drive to power switch transistor Q22. The base drive to Q22 is adjusted to ensure saturation for the load current passed by the power switch under worst-case conditions. Under overvoltage conditions, the power switch is turned off (regardless of the state of input command) by clamping the base of Q21 (via Q20) to -24.5-volt bus input, thus holding Q21 and, therefore, Q22 off.

Overvoltage levels on the input -24.5-volt spacecraft bus are detected by the threshold detector stage, Q18. The voltage at the junction of R56 and R57 is compared with a zener derived reference voltage, provided by VR3. The difference voltage appears as the base emitter bias voltage of stage Q18.

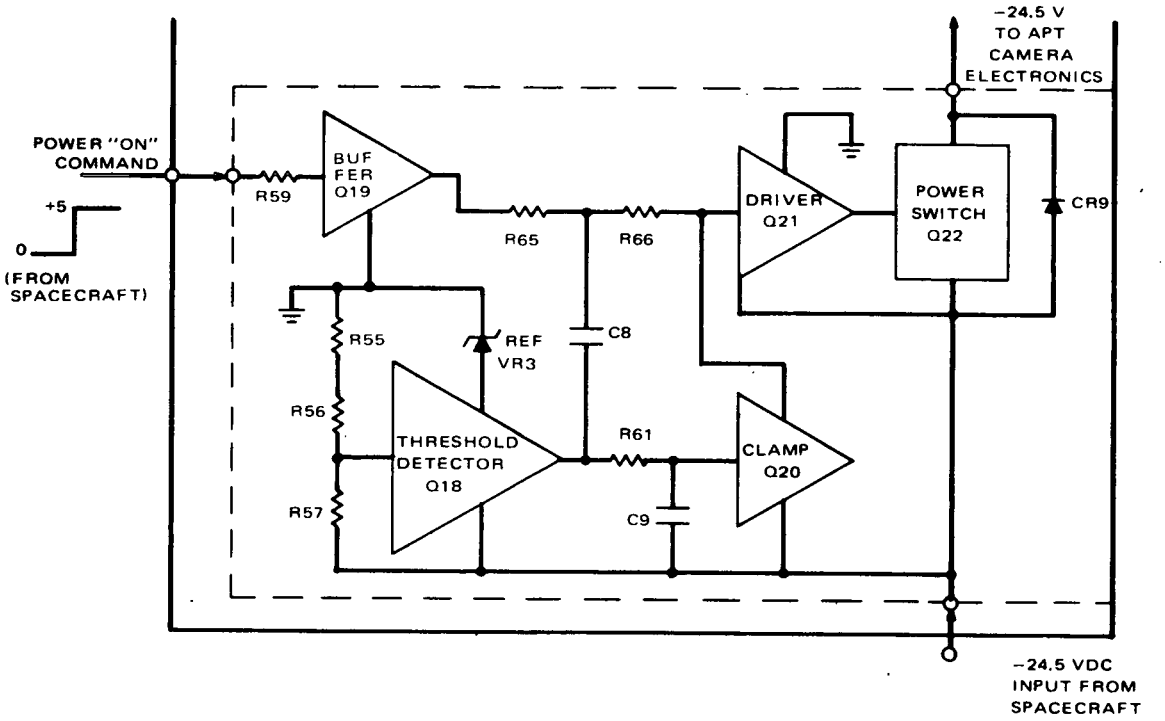


Figure 2-V-75. Power Switch and Overvoltage Protection Circuit, Block Diagram

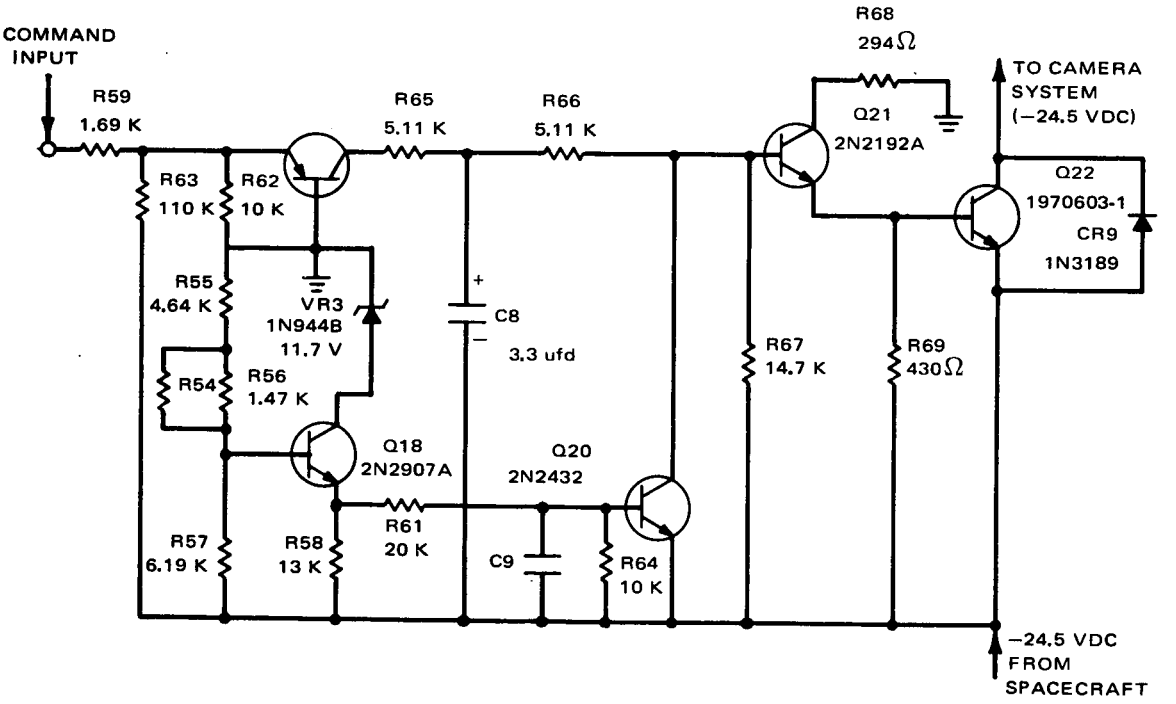


Figure 2-V-76. Power Switch and Overvoltage Protection Circuit, Schematic Diagram

When the -24.5-volt bus exceeds a certain threshold level V_T, Q18 is caused to turn "on". The turning on of Q18 drives Q20 into saturation, thereby effectively clamping "off" the input to the power switch driver by diverting the base drive to Q21 through Q20 to the -24.5-volt bus. If a command "on" level is not present, then no base drive is available initially, and the overvoltage clamping stage (Q20) merely acts to provide a low impedance for the leakage (off) currents of Q19 and Q21.

(3) TRANSIENT RESPONSES

The transient responses of the PSOP circuit to be controlled were specified as:

- Turn-On Surge Current into Camera System (normal supply voltage)

  Limts:

  $\frac{dI}{dt}_{surge}$ Max ≤ 50 milliamperes per microsecond

  (I) surge Max ≤ 50 amperes

- Overvoltage Circuit Response

Normal Transients	Power Switch Response
Transient I	No turn off
Transient II	Indefinite (diode protected)
Abnormal Transients	**Power Switch Response**
Transient III	Turn off

The turn-on surge transients are due to the nature of the camera input load which is essentially capacitive. This fairly large capacitance must be charged at the instant of turn-on, resulting in large capacitive charging currents flowing initially in the power switch.

The rate of change of the initial turn-on surge current, $\frac{dI}{dt}_{\text{surge Max}}$, is controlled by the RC network between Q19 and Q22. Capacitor C8 provides a slow-down of the application of base drive current to Q21 when an "on" command is suddenly applied. The maximum rate of base current drive to Q21 is thus limited to a value to ensure that the resulting rate of increase of base drive to Q22 is proportionately limited to a value insufficient to support a rate

of change of Q22 collector current greater than 50 milliamperes per microsecond. The time constant is adjusted to produce these conditions under assumed worst-case maximums of $h_{FE_{21}}$, $h_{FE_{22}}$, and other parameters (I_{surge}) maximum.

The maximum value attained by the input surge transient is limited by specification on the power switch transistor Q22. The maximum h_{FE} of Q22 is specified to be less than a value sufficient to ensure that a collector current in excess of 5 amperes cannot be supported with the worst-case maximum base drive available. In addition, the previous slow-down feature helps to limit the maximum surge current attained. If the collector current attempts to increase above the level set by the base drive and $h_{FE_{32}}$, power switch transistor Q22 comes out of saturation, thus limiting the current to this maximum.

Transient I is a transient due to power supply load switching which may cause the -24.5-volt bus to jump from its normal range value to a value not more negative than -36.0 volts and back to its normal range value in less than 5 microseconds. Under this transient condition, it is required that the overvoltage circuit not turn off the power switch. Thus, the delay time of the overvoltage circuit must be slowed sufficiently to allow this transient to occur without interrupting the base drive to Q21. This is accomplished by providing a time constant at the base of Q20 to slow down the application of base drive after Q18 has turned on. The time constant is sufficient to allow this transient to pass without activation of the overvoltage clamping stage Q20.

Transient II occurs as a result of spacecraft power supply switching. This transient presents the possibility of a reverse transient surge back through the power switch to the uncharged output capacitance of the newly switched-in spacecraft power supply. Since the power switch could be subjected to excess base emitter voltage as well as large surge currents, a protective measure is required. This protection is afforded by the diode (CR9) connected across the collector emitter of the power switch, Q22. The diode acts to bypass the power switch whenever collector-to-emitter potentials are reversed as in the case of the transient condition II. Thus, the input capacitance of the APT camera, (previously charged to -24.5 volts) discharges through this diode and through the uncharged spacecraft supply output capacitance until the spacecraft supply's own voltage has risen sufficiently to again produce the normal collector emitter bias on the power switch transistor. At this time, the diode becomes reverse biased and the power switch transistor resumes its normal function.

Abnormal transients are those occurring under malfunction or failure of the spacecraft -24.5-volt regulators. Under worst-case conditions, this may cause the -24.5-volt spacecraft bus to increase suddenly to -36.0 volts (in a time > 250 microseconds and remain for indefinite periods, < 10.0 milliseconds). Under such conditions, it is required that the overvoltage circuit provide protection to the camera system by turning off the power switch (if

commanded "on" at the time). The response must be sufficiently fast to prevent excessive voltage rises (> 28 volts) at the input to the camera. Since the malfunction transient step has been specified to occur in a time greater than 250 microseconds and less than 10 milliseconds, it is sufficient to ensure that the overvoltage circuit delay is less than the time required to charge the camera input capacitance from the initial normal voltage level to -28 volts. This minimum time is calculated to be 0.15 millisecond for a 250-microfrarad input capacitance charge at a maximum 5-ampere rate. Thus, the delay provided by capacitor C2 is set for a value < 5 microseconds and > 0.5 millisecond, allowing uninterrupted operation under type I transients while protecting against type III transients.

d. DIGITAL-TO-ANALOG CONVERTER AND LADDER

(1) GENERAL

The vertical sweep waveform as employed in the APT camera consists of a digitally derived staircase function of 600 discrete equal increments (or steps) during the 150-second vertical scan period and 32 additional steps during the 8-second PED period. The staircase wave is generated by decoding the output of a 10-stage countdown chain in the sequence timer. The input clock rate to this 10-stage counter is 4 Hz which is also the horizontal line frequency. Thus, the successive binary states of the counter are changed each horizontal line time. The digital-to-analog (D/A) converter functions by accepting these 10 binary inputs from the counter and applying corresponding -18 volts or ground signals to a resistive ladder summing network which produces an output signal proportional to the equivalent binary number represented by the counter. (This count, in actuality, starts at 200 by presetting the counter in the logic at the beginning of the "read" cycle.) This preset count arises from the abbreviated vertical format which was part of the TIROS M modifications (Paragraph 3.1.14 of Performance Specification Revision 3 C.I.S.).

(2) CIRCUIT DESCRIPTION

The D/A converter and ladder circuit is shown in Figure 2-V-77. The converter consists of two inverted mode switches (Type 2N4008) per input and a driver (Q3) which are used to alternately connect the respective input of the ladder network to either ground or -18 volts depending upon the state of the input from the respective counter stage. The state of the counter is changed at the horizontal line rate and at each step of the counter the various activated inputs (-18 volts) to the ladder are weighed in the resistive network to produce the resulting staircase waveform at its output terminal.

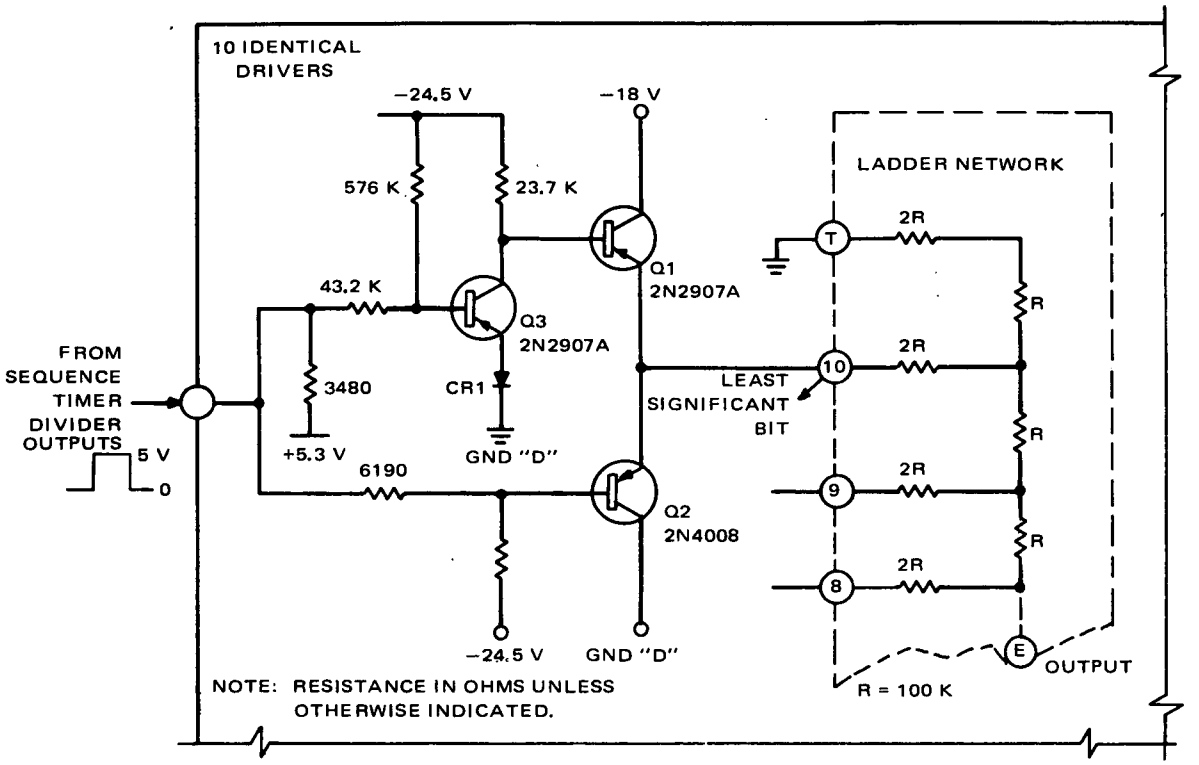


Figure 2-V-77. Digital-to-Analog Converter and Ladder Circuit, Simplified Schematic Diagram

In an effort to meet the tolerance requirements on linearity and "ladder line" perceptibility without the need for external resistance tailoring of the ladder, investigations of various precision resistor network vendors led to the choice of a ladder resistance network supplied by Angstrom Precision, Inc. (manufactured to RCA specifications under Specification No. 1970565). This network consists of discrete, fixed, film resistors of nominal 100-kilohm value with close matching in absolute value, encapsulated in a single package, 1 by 1.5 inches. The network is mounted directly on the D/A converter circuit board. The reduced number of hard wire connections and common substrate composition provides an increase in reliability as well as improved relative resistance tracking with temperature.

The driver circuitry utilizes the low and stable saturation drop in the inverted mode configuration of special preselected transistors, Q1 and Q2. The performance requirements for these transistors are given in RCA Specification No. 1970589. The overall accuracy tolerances on the suitcase waveform at the peak-to-peak vertical sweep signal per step with an accuracy of 1/3000th of this peak-to-peak signal; i.e., step accuracy equals ±20 percent of a nominal step.

(3) BREADBOARD AND ETM TEST

In order to spot check the specified uniformity of step increments at the output of the D/A circuit, a laboratory breadboard circuit using a sample ladder network (Angstrom LN10-100-A, SN03 and unpreselected 2N4008's) was tested at step transitions corresponding to counts $2^h - 1$ to 2^h in = 0, 1 through 10 at 25°, 60°, and -10° C. The maximum deviations (Table 2-V-10) measured from the average step value for each set of 10 sample steps were obtained. This compares with the 20-percent maximum deviation implied above. Complete raster checks on the ETM showed no perceptible ladder line evidence.

TABLE 2-V-10. BREADBOARD TEST RESULTS

Temp (°C)	I Max Deviation From Avg Step (millivolts)	II Avg Step (millivolts)	Percent Deviation = $\frac{I}{II} \times 100$
25	0.30	17.47	1.7
60	0.37	17.48	2.0
-10	0.28	17.50	1.6

e. TELEMETRY CIRCUITS

(1) GENERAL

The APT camera subsystem contains the following telemetry circuits:

- Vidicon Target Temperature
- Vidicon Filament Current
- -6.3-Volt Regulator Output
- G_1 Electrode Voltage
- Combined Horizontal and Vertical Deflection
- Telemetry
- Hold and PED Pulse

(2) TELEMETRY CIRCUIT DESIGN CONSTRAINTS

The telemetry circuit design constraints (as per Paragraph 3.3.8.2 of PS-1964120) are listed in Table 2-V-11.

TABLE 2-V-11. TELEMETRY CIRCUIT DESIGN CONSTRAINTS

Telemetry Circuit	Voltage Range Maximum Limits (volts)	Output Impedance Maximum (kilohms)	Output Impedance Tolerance* (kilohms)	Repeatability of Initial Calibration (percent)
Vidicon Target Temperature	-1.0 to -5.0 $V_{on} - V_{off} \geq -4.5$	30	±3	5
Vidicon Filament Current	-1.0 to -5.0 $V_{on} - V_{off} \geq 1.0$	30	±3	5
-6.3-Volt Regulator Output	-1.0 to -5.0	30	±3	5
G_1 Electrode Voltage	-1.0 to -5.0	30	±3	5
Combined Horiz & Vert Deflection	-1.0 to -5.0	30	±3	5
Hold & PED Telemetry	-1.0 to -5.0 $V_{Hold} - V_{PED} \geq 1.0$	30	±3	

*From nominal

All telemetry circuits listed in Paragraph e.(1), were redesigned. In addition these circuits were subjected to the general worst-case constraints as discussed in Paragraph C.2.b of this section.

The circuits were breadboarded using available components and measurements made. Temperature tests on the engineering model indicated required performance of the telemetry outputs. Telemetry outputs are short-circuited-proof, allowing the camera system to operate within specifications in such event. The design also allows for the failure of any single component without resulting in a telemetry output voltage in excess of -36 to +10 volts, under malfunction conditions.

(3) DEFLECTION CIRCUITS

The 4-pps square wave from the sequence timer frequency divider triggers a horizontal sync and blanking generator which, in turn, generates 12.5-millisecond pulses at a 4-pps rate. These pulses drive the horizontal deflection amplifier, producing a sawtooth, horizontal sweep voltage of 237.5-millisecond duration for the vidicon horizontal deflection coils. The 12.5-millisecond portion of the total 240-millisecond output waveform from the horizontal sync generator is used for blanking during horizontal retrace. The 4-pps horizontal deflection sawtooth and blanking pulses are generated continuously during the 158-second duration of the prepare, expose, delay, and readout cycles. The horizontal sync generator also provides 12.5-millisecond pulses, at a 4-pps rate, to the video switch for gating purposes.

The vertical deflection circuits provide both the rapid scan and slow scan sweep voltages to the vertical deflection coils. The rapid scan, during the PED cycle, uses a 4-kHz oscillator in the deflection circuit; the oscillator output is applied to the vertical deflection amplifier, amplified, and applied to the vertical deflection coil. During readout, the 4-kHz oscillator is biased off by the sequence timer. The slow scan signal for readout is generated by a D/A converter from the 10-bit digital input from the sequence timer. The converter counts the digital input, in 250-millisecond steps, during the 150-second readout period and during the 8-second PED cycle, and produces a "staircase" output waveform of 632 discrete steps. However, the output of the converter is inhibited during the 8-second PED cycle. Hence, a 600-step staircase signal, which provides the required 600-line readout of the vidicon, is applied to the vertical deflection amplifier.

(4) FOCUS CURRENT REGULATOR

The satellite power supply applies -24.5 volts DC through the focus current regulator to the focus coil of the vidicon. The amount of current in the coil is held constant by the regulator circuit to ensure uniform focus during picture readout. A portion of the regulated focus current is used by the alignment coils to provide proper alignment of the vidicon beam.

(5) ELECTRODE SWITCHING AND BEAM CURRENT REGULATOR

The electrode switching circuit and beam current regulator control the operation of the vidicon and regulate the operating currents. To maintain constant quality vidicon performance, a beam current regulator is used to compensate for the effects of vidicon heater and cathode aging with the resultant change of beam current. This is accomplished by sampling the accelerating grid, G2, current in the beam current regulator; the regulator detects changes in the G2 current and compensates for these changes by varying the voltage on

control grid, G1. Any decrease in the G2 current causes the G1 voltage to go less negative, thereby increasing the beam current and maintaining optimum picture quality.

The changing of the potentials on vidicon grid G1 during the hold period, the PED cycle, and the readout cycle is accomplished by transistor switches, which are operated by pulses generated in the sequence timer. The required switching of the target voltage during the prepare cycle is accomplished by a switching relay, operated by a pulse generated in the sequence timer. The prepare potential is applied to the normally open contact; the hold, and the expose, delay, and readout potentials are applied to the normally closed contact. The relay coil is connected to the -24.5-volt supply and is energized during the prepared cycle by a ground signal from the relay driver in the sequence timer.

(6) TARGET LAMP CONTROL

The target lamp control circuit applies power to the vidicon flood lamps. This circuit is driven by a control pulse from the sequence timer. The lamps are turned on, by means of a transistor switch, for 1 second during the prepare phase of vidicon operation and turned off during the remaining phases. The voltage applied across the lamps is held constant by reference diodes and a series voltage regulator.

(7) SAMPLING PULSE GENERATOR

To improve the signal-to-noise ratio of the video signal, a pulse modulation technique is employed. This technique involves gating the electron beam during the readout operation to obtain video pulses at peak current levels. The pulsed readout of the vidicon is accomplished by gating the vidicon cathode with 26-microsecond intervals at a 4800-pps rate, using the output from the sampling pulse generator. In addition, the 12.5-millisecond blanking pulses from the horizontal sync generator are applied to the sampling pulse generator to blank the sampling pulses during the 12.5-millisecond horizontal sweep retrace time, which occurs once every 250 milliseconds. An output from the sequence timer activates a transistor switch, at the output of the sampling pulse generator, which clamps the output to ground during the hold and PED cycles.

(8) VIDEO CHAIN

The video chain consists of a video inverter, a video detector, a video switch, a start tone generator, and a modulator stage. The video pattern at the vidicon target is sampled for 26 microseconds out of every 208-1/3 microseconds, 1140 times during each 237.5-millisecond horizontal line. The output of the vidicon is a negative-going pulse train with a pulse repetition rate of 4800 pps and with the pulse amplitude proportional to the light incident on the vidicon target. This train is amplified by the video amplifier in the camera sensor assembly and applied to a video inverter for processing by the video detector circuit in the camera electronics module. The video detector converts the pulse-modulated signal to a conventional analog video signal and again inverts the polarity. (During the interval between the video sample pulses, the input of the video detector is clamped to a negative voltage through a transistor switch, eliminating any random noise generated in the video chain. The transistor switch is open at the beginning of each 25-microsecond sampling period by a 50-microsecond, 4800-pps output from a one-shot multivibrator triggered by the 25-microsecond, 4800-pps output from the sampling pulse generator.) Since the video detector is designed to attenuate all frequencies above 1600 Hz (at the rate of 24 decibels per octave), the output of the detector contains only the average video variations. The output signal has a peak-to-peak value equal to the average peak-to-peak value of the amplitude variations in the input pulse train. Blanking pulses from the horizontal sync generator are applied to the output circuit of the detector during the horizontal retrace time to provide DC level restoration.

The video switching circuit, used in conjunction with the start tone generator and the horizontal sync generator, couples the 300-Hz start tone and the phasing pulses into the camera system transmission. The sequence timer, at the beginning of the PED cycle, permits the 300-Hz square wave output of the start tone generator to be applied to the modulator for 3 seconds by activating the video switch. After 3 seconds, the video switch then permits the 4-pps phasing pulses to be applied to the modulator for the rest of the 8-second PED cycle. At the beginning of the 200-second readout period, the video switch allows only the video information to be passed to the modulator.

The modulator stage combines the video with a 2400-Hz sine wave to produce the 2400-Hz amplitude-modulated video subcarrier used for modulating the TV transmitter. The start tone and phasing signals also amplitude modulate this subcarrier; the modulated subcarrier, in turn, is applied as modulating signal to the 137.5-MHz TV transmitter.

(9) POWER SUPPLY

All voltages for the camera, except the -24.5-volt regulated and -28-volt unregulated supplies, are derived in a DC-to-DC converter that changes the -24.5-volt power to values required for vidicon and control circuitry operation. Several converter outputs are fed through voltage regulators to produce stable voltages for use in critical circuits of the camera system.

D. SCANNING RADIOMETER SUBSYSTEM

1. General Description

The scanning radiometer (SR) subsystem measures emitted radiation from the earth during orbit day and night and measures reflected radiation from the earth during daytime. The data obtained is transmitted in real time to local user stations and is also recorded for later playback to the CDA stations.

The scanning radiometer is a meteorological instrument built especially for use on the ITOS spacecraft. The radiometer is unique in sensing two spectral regions and in its high spatial resolution. The radiometer measures reflected radiation from the earth in the 0.52- to 0.73-micron region (visible) during daytime, and measures emitted radiation from the earth in the 10.5- to 12.5-micron region (infrared) during day and night.

A functional block diagram of the subsystem is shown in Figure 2-V-79 and the subsystem components are illustrated in Figure 2-V-78.

The subsystem permits determination of the surface temperatures of ground, sea, or cloud tops viewed by the radiometer. Sensitivity in the 10.5- to 12.5-micron spectral region permits surface temperatures to be determined in daylight as well as at night, since reflected solar radiation in this wavelength region is small compared with emitted radiance. The visible region measurement of reflected solar radiation has a higher calibration accuracy capability than television camera systems presently in use and is not subject to shading which occurs in the vidicon camera systems. Table 2-V-12 lists characteristics of the scanning radiometer subsystem.

The SR subsystem shown in the composite photograph of Figure 2-V-78, comprises: (1) two scanning radiometers, (2) a dual SR processor, and (3) two scanning radiometer recorders (SR recorders). A block diagram of the subsystem is shown in Figure 2-V-78. Each radiometer and tape recorder can be turned on or off by command from a CDA station. Each half of the SR processor is associated with one radiometer and is powered when that radiometer is powered. The radiometers are mounted on the spacecraft structure in a manner to provide them with maximum sun shielding and to permit a scan of approximately 150 degrees without obstruction.

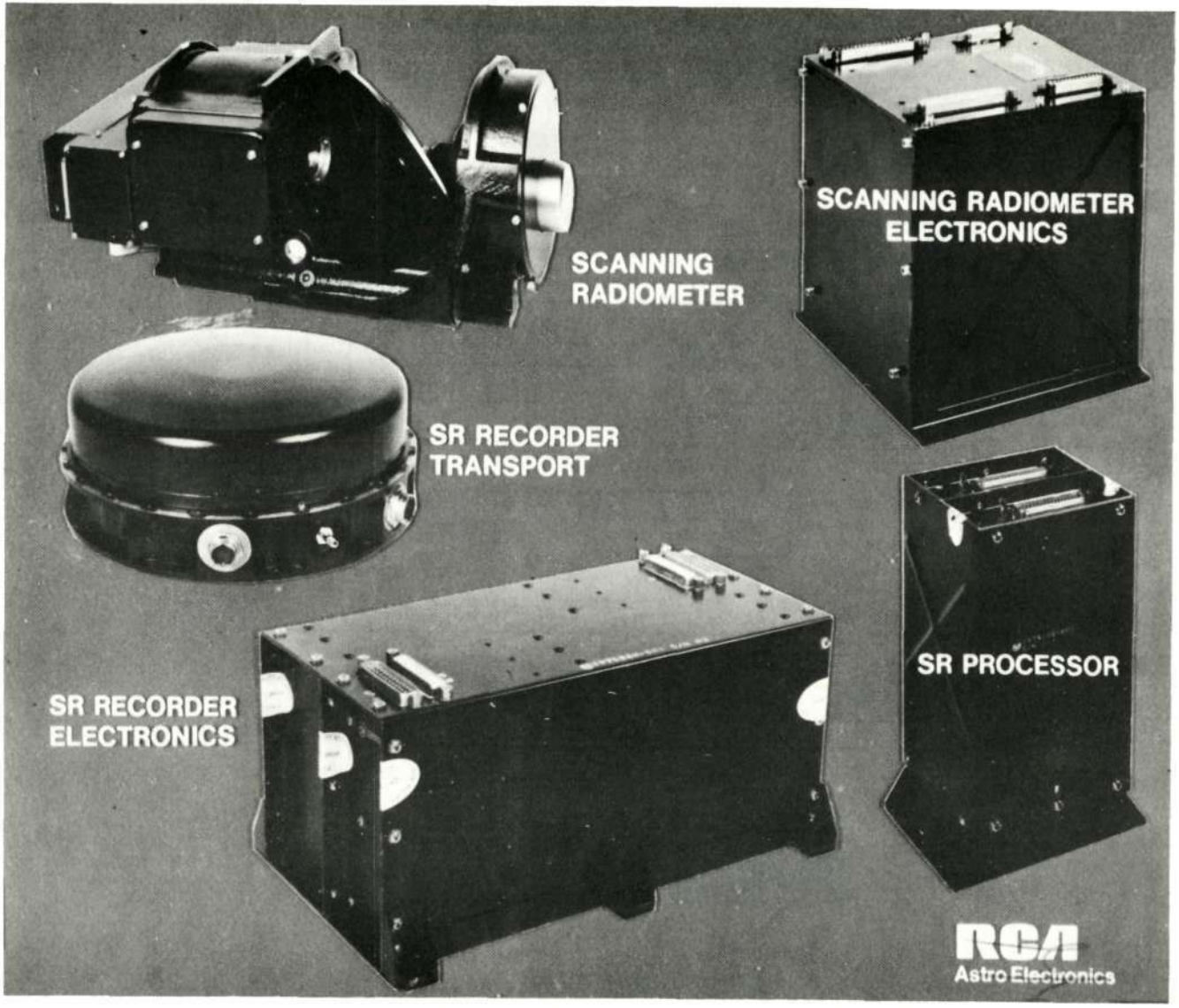


Figure 2-V-78. Scanning Radiometer Subsystem

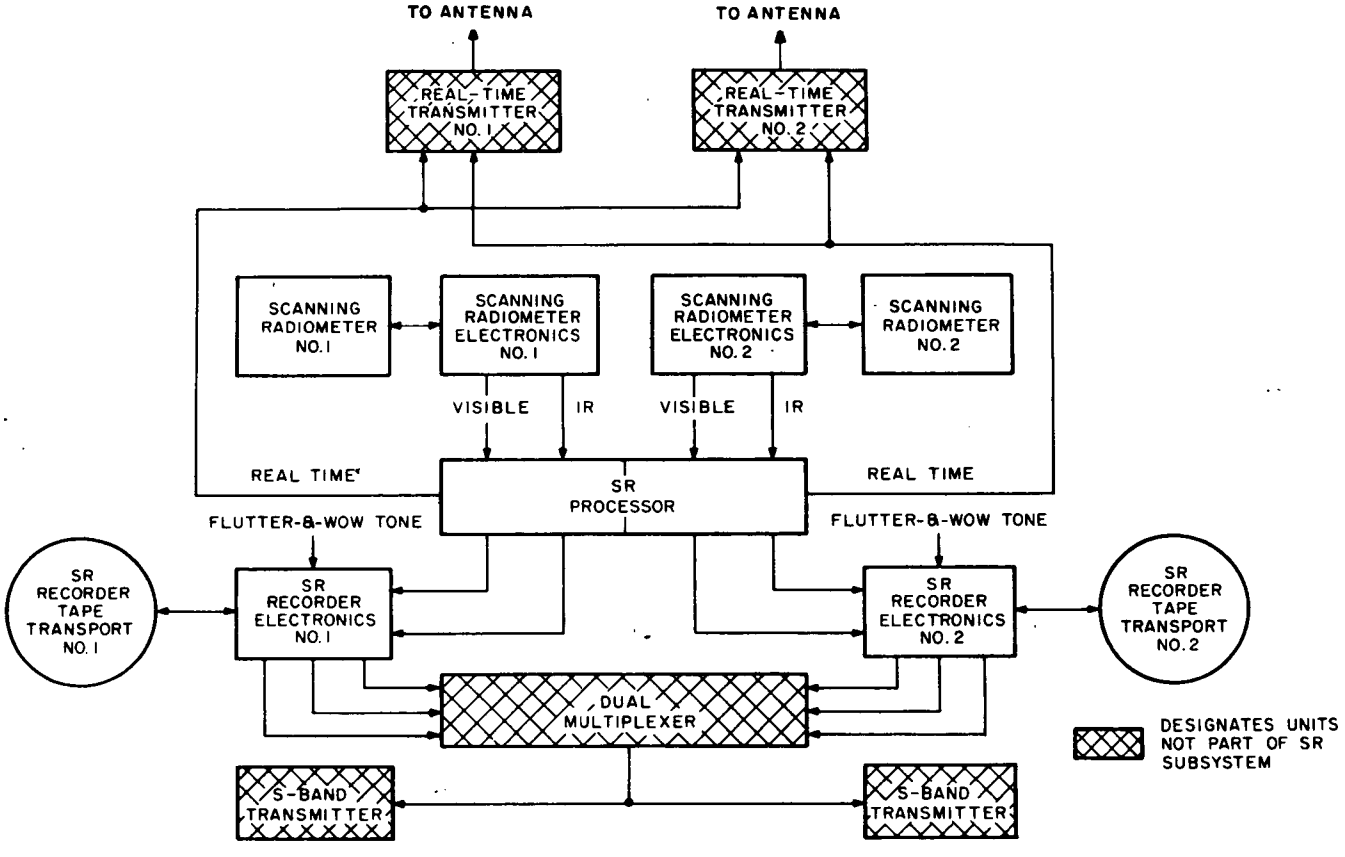


Figure 2-V-79. Scanning Radiometer Subsystem, Block Diagram

2. Functional Description

As the spacecraft proceeds along its orbit, the radiometer scans the earth's surface from horizon to horizon, perpendicular to the orbital plane. The radiometer scans the earth by means of a continuously rotating mirror which is inclined 45 degrees to its axis of rotation (parallel to the satellite's velocity vector). The optical axis scans in a plane perpendicular to the satellite's velocity vector as shown in Figure 2-V-80.

Mirror rotation causes a transverse scan across the earth (shown in Figure 2-V-80 as scan n). In the time required for one complete mirror rotation, the satellite progresses approximately 5 miles along the orbit track. Another area is then scanned, shown as scan n + 1, and this is repeated throughout the orbit.

The scanning radiometer output is processed in the SR processor, where time code data and scanning radiometer telemetry data are combined with the IR and visible radiation signals, for recording on tape. (Time code and telemetry data are not included in the real-time transmitted data.)

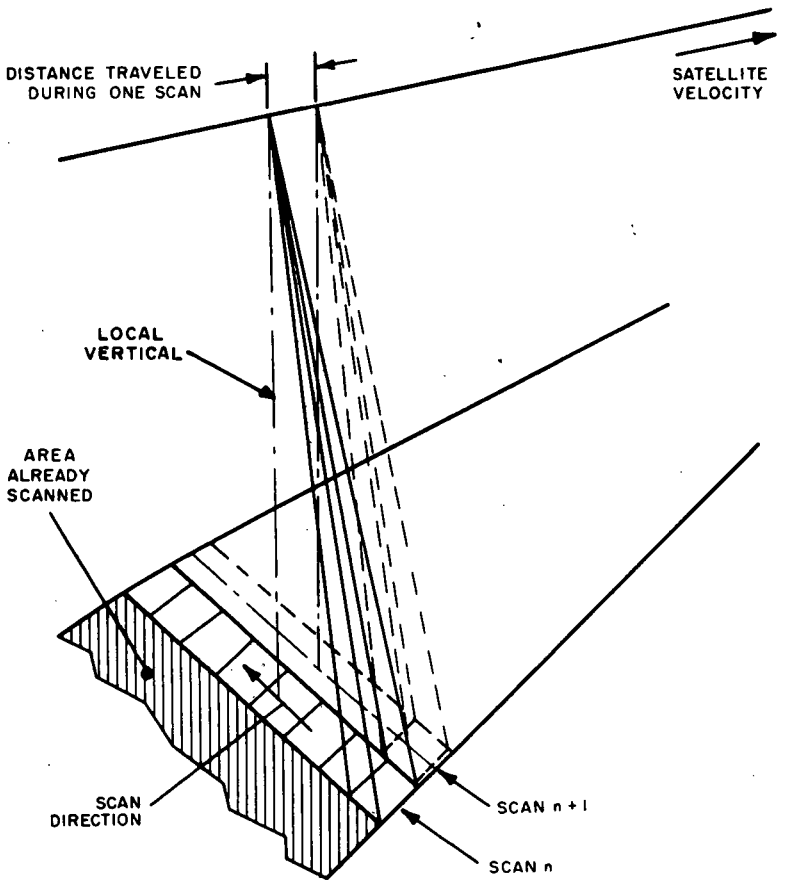


Figure 2-V-80. SR Scan Projection

The SR processor outputs frequency modulate a subcarrier in the SR recorder. The subcarrier frequency range is from 2.4 to 3.3 kHz. The two frequency-modulated radiometer signals and a 3.125-kHz flutter-and-wow signal are recorded simultaneously on the three recorder channels. The recorder tape speed is 1.875 inches per second; it has a total recording capability of 145 minutes.

When the playback command is received, power is removed from the record circuits and applied to the playback circuits; the direction of tape travel is reversed; and all three tape tracks are played back simultaneously at a tape speed of 30 inches per second (16 times the recording speed). During playback, the subcarrier frequency range becomes 38.4 to 52.8 kHz.

In normal operation SR signals are recorded only during the nighttime portion of one orbit and then played back on the succeeding orbit. However, during at least one orbit per day, no CDA ground station contact is available, and, on occasion, two orbits in succession do not have satisfactory CDA station contact. The recorders are, therefore, provided with the capacity to store at least two orbits of data. The command structure of the spacecraft permits one orbit to be stored on each recorder or both orbits to be stored on one recorder.

Playback of the recorders can be commanded to occur either simultaneously or separately. Where simultaneous playback is commanded, only the IR channel of each recorder is transmitted, together with the associated flutter-and-wow signals. When only one recorder is played back, both the IR and the visible channels, together with the one flutter-and-wow signal, are transmitted.

An alternative operating mode permits recording to take place continuously (during both day and night). In this case (as in the previously mentioned case, where only one orbit is stored on each recorder), switching from one recorder to another takes place automatically as the spacecraft crosses the night/day terminator. On receipt of the playback command the recorder that is not recording is played back. If the night/day switching is to take place while playback is in progress, the switchover is delayed until playback is completed.

3. Scanning Radiometer Subsystem Components

a. SCANNING RADIOMETER AND SCANNING RADIOMETER ELECTRONICS

(1) GENERAL DESCRIPTION

The scanning radiometer (SR) was developed specially for use on the ITOS spacecraft and is supplied by the Santa Barbara Research Corp. of Santa Barbara, California. The SR is capable of providing pictures of the earth's cloud cover during orbital day and night, with the additional capability of providing quantitative radiometric data.

There are two channels in the radiometer: a visible channel and a thermal, or infrared, (10.5- to 12.5-micron) channel. The visible channel provides TV-analogous coverage during the day, in the same spectral region used by the TIROS television cameras. The infrared (IR) channel operates in an atmospheric window region which has sufficiently low reflected solar radiation so that day performance is comparable to night performance. This channel is calibrated for surface temperatures in the region of 185° to 330°K, thus permitting measurement of cloud top and surface temperatures.

The design of the radiometer permits a large variation in spacecraft operating parameters. The performance of the radiometer will not be compromised if the spacecraft altitude is varied over the range of 600 to 900 nautical miles, although the nominal design altitude of the radiometer is 790 nautical miles. Similarly, the radiometer is designed to operate satisfactorily in sun-synchronous orbits within 1 hour of the nominal 9 AM descending and 3 PM ascending node orbits.

The life expectancy in orbit is a minimum of 6 months, with a design goal of 1 year.

Table 2-V-13 presents pertinent parameters of the scanning radiometer.

(2) ELECTRICAL DESCRIPTION

The block diagram, Figure 2-V-81, shows the two separate boxes which make up the radiometer. The scanner unit is mounted on the earth-facing side of the spacecraft. The electronics module is located in the electronics bay of the spacecraft.

The scanner unit has an elliptically shaped flat scan mirror and primary optics which are common to both the thermal and visible channels. The scan mirror is set at an angle of 45 degrees with the scan axis and rotates at 48 rpm. The two channels are optically separated by a dichroic beam splitter, after which the radiation in each channel is imaged onto the channel detector. The dichroic beam splitter is a 10.5- to 12.5-micron bandpass filter, which has a short wavelength reflecting front surface. Figure 2-V-80 illustrates how the visible and thermal channels are optically separated and the manner in which the signals are processed.

The detected signals are amplified by the two channel preamplifiers. The IR detector (bolometer) requires a DC bias which is supplied by the bias power supply. This power supply contains a DC-to-DC converter whose voltage output is controlled by two temperature compensating circuits. The first circuit senses the temperature of the detector and varies the bias voltage to give a constant signal output for constant radiance input over the temperature range of -5° to +45°C.

TABLE 2-V-12. SUBSYSTEM CHARACTERISTICS

Parameter	Channel	
	Visible	Thermal (IR)
Radiation Source of Interest	Reflected Sunlight	Self-Emitted Earth Radiation
Range of Sensitivity	< 50 to 10,000 foot-lamberts	180° to 330°K
Ground Resolution at Nadir (spacecraft altitude 790 nautical miles)	2.1 square nautical miles	4.2 square nautical miles
Spectral Bandwidth (microns, at 1/2 amplitude points)	0.52 to 0.73	10.5 to 12.5
Detector	Silicon photovoltaic	Immersed bolometer
Scan Rate, Lines per Minute	48	
Collecting Aperture of 5-inch Mirror with Obscuration (cm^2)	101.7	
Primary Optics Effective Focal Length (inches)	16.9	
Size		
Scanner Unit (inches) not Including Sunshield	15.8 by 8.4 by 6.4	
Electronics Module (inches) not Including Mounting Flanges	6.0 by 6.0 by 6.5	
Weight		
Scanner Unit (lb)	12.1	
Electronics Module (lb)	6.2	
Sun Shield (lb)	0.9	
Power Requirement		
Maximum at -24.5 Volts	7.4	

TABLE 2-V-13. SCANNING RADIOMETER CHARACTERISTICS

Parameter	Visible Channel	IR Channel
Resolution		
Angular	2.8 milliradians	5.3 milliradians
Ground at 790 nmi	2 nmi	4 nmi
Spectral Region	0.52 to 0.73 microns	10.5 to 12.5 microns
Sensitivity, Noise Equivalent Irradiance	7.5×10^{-10} w cm^{-2}	4.2×10^{-10} w cm^{-2}
Dynamic Range	20 to 10-k foot-lamberts (scene brightness)	185° to 330°K (scene temperature)
Detector	Silicon photovoltaic	Thermistor bolometer
Electrical Bandwidth	900 Hz	455 Hz
Diameter of Optics	5 inches	
Scan Rate	48 rpm	
Power Requirement	7 watts	
Weight	19.2 pounds	

*These values are for the radiometer only, not for the subsystem.

The second circuit, which also senses the bolometer temperature, sharply reduces the bias voltage at temperatures over +47 C to assure safe internal bolometer temperatures.

The thermal channel preamplifier has two capacitor-coupled sections. The first section is a differential field effect transistor (FET) pair, followed by additional amplification using bipolar devices. A capacitor between the detector and first section is used to block the DC voltage variations which are the result of the two bolometer flakes not tracking accurately over the temperature range. The second section is made up of a differential FET pair followed by an integrated circuit operational amplifier.

An RC network between the first and second sections permits "tuning out" the secondary time constant of the bolometer.

The preamplifier for the visible channel is a low noise operational amplifier with field effect transistor differential input. It is connected in the current mode, causing the photovoltaic diode to operate into very nearly a short circuit. This

preamplifier is DC-coupled in contrast to the thermal channel preamplifier, which is capacitor-coupled.

The DC restore amplifier (both channels) consists of a main amplifier with provisions to select gain, a feedback/error amplifier, and an FET switch. In the amplifying mode, the main amplifier passes the signal, the FET switch is open, and the error amplifier does not function. In the thermal channel, an RC feedback network creates a boost of 6 decibels per octave over the range of about 150 to 450 Hz in order to compensate for the rolloff of the bolometer, whose behavior is approximately that of a single pole at 150 Hz. When a "DC restore" signal from the logic is applied to the switch, the FET conducts with a low ON resistance. This connects the error amplifier output to the main amplifier input, driving the main amplifier output to -0.25 volt.

The bandlimiting filter which follows the DC restore amplifier (both channels) limits the high frequency of the channel. This is an RLC passive filter with a rolloff of 40 decibels per decade and a -3-decibel frequency of 450 Hz for the thermal channel and 900 Hz for the visible channel. The shape of the filter characteristic in the region of cutoff is selected to minimize the product of rise time and noise bandwidth. This also results in good phase linearity for low phase distortion.

The shorting switch in each channel disconnects the signal from the output buffer so that synchronization and calibration waveforms will appear at the output, unaltered by the channel noise.

The output buffer is an operational amplifier which can perform a number of functions without interaction. As a summing device, it combines the signal, sync pulse, and calibration waveform with independently adjustable gains. A capacitor across the feedback resistor creates a first order rolloff at 1.1 kHz to attenuate the high frequency components resulting from the fast rise times of the digital signal inputs. The output buffer (in the inverter mode) also converts the positive signal levels at its input to a negative voltage at a low impedance for distribution to the other circuits in the subsystem.

The motor control logic, which is located in the scanner unit, provides a two-phase 100-Hz signal, from which the motor power amplifier is driven, by dividing a 400-Hz square wave into two 100-Hz square waves 90 degrees apart. The 400-Hz signal comes from a free-running multivibrator which is synchronized to a 400-Hz square wave taken from the spacecraft system. If the spacecraft signal fails, the multivibrator will continue to oscillate at a slightly lower frequency, but the motor will continue to rotate. The motor logic and drive are normally powered by the spacecraft -24.5-volt supply. However, if this power should fail, the load is automatically switched to the unregulated -28-volt supply until the -24.5 voltage again is available. Power for the motor, its logic, and power amplifier is supplied through a command relay so that the scanning action may be turned OFF and ON.

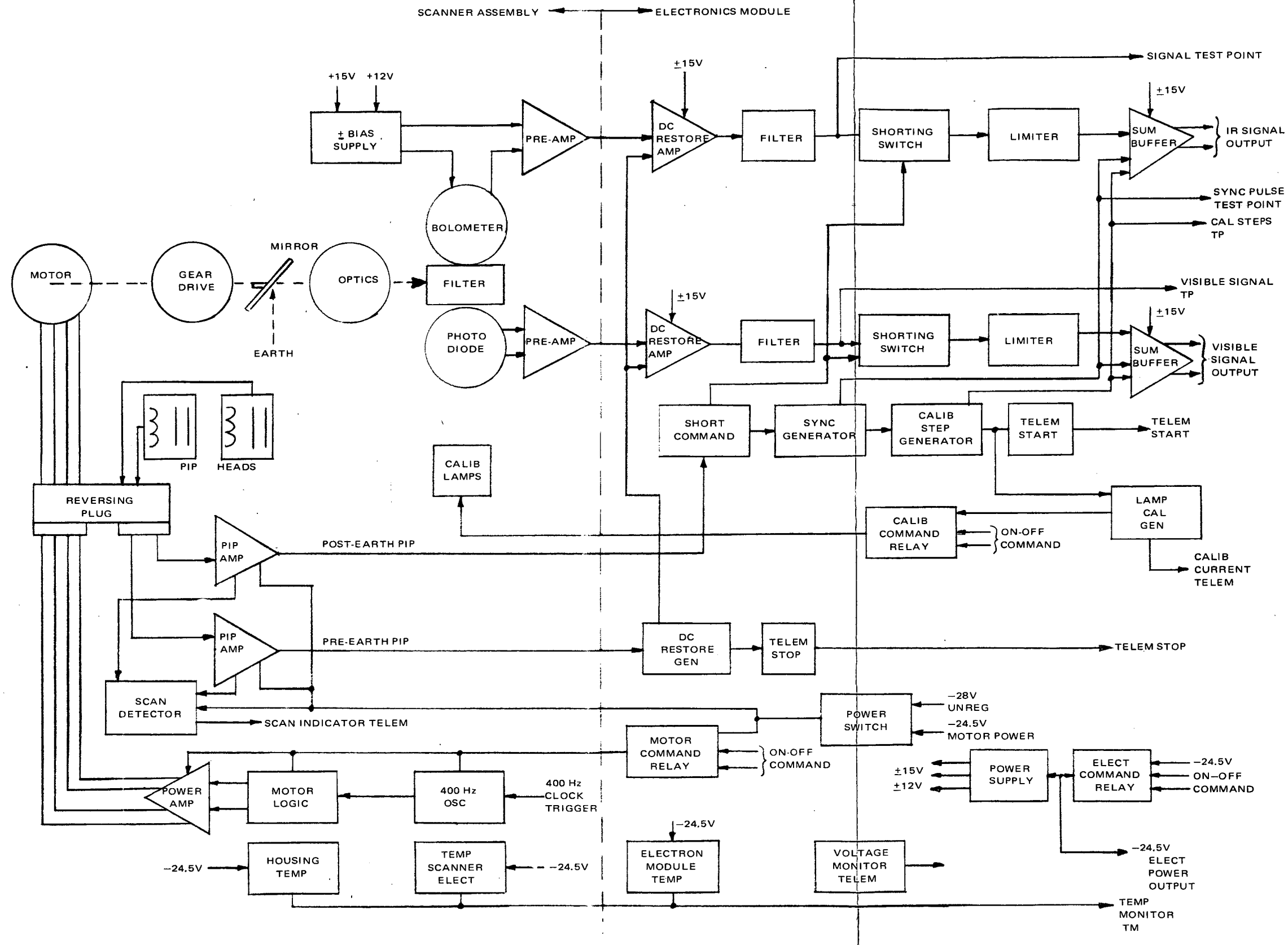


Figure 2-V-81. Scanning Radiometer, Block Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

As the mirror rotates, its phase is detected by two magnetic pickup heads. The phase of these pulses is shown in Figure 2-V-82. As the mirror scans out of its housing and views outer space on the end of the spacecraft away from the sun, the pre-earth pip occurs, determined by the first magnetic pickup. This signal is amplified and is processed to produce the "DC restore" pulse. A buffered output of the "DC restore" signal is used as the "telemetry stop" signal.

A second magnetic pickup determines when the post-earth pulse is to occur. After this signal is amplified, it triggers logic which simultaneously initiates the shorting command and the synchronization signal. The synchronization signal is at ground potential for 20 milliseconds followed by 60 milliseconds at -8 volts, and then ground potential for 20 more milliseconds. At the end of the synchronization signal, the "telemetry start" signal and the voltage calibration stair-step are initiated. This signal consists of six voltage levels at 1-volt intervals from 1 to 6 volts, and the duration is 120 milliseconds. The end of the voltage calibration signal causes the shorting command to be terminated, and the 120-millisecond delay for the start of the visible calibration lamps.

The visible calibration lamps are commanded ON and OFF by ground command. When calibration is initiated, a 2-milliampere current is applied to the lamps. The current is then increased to about 3 milliamperes for 120 milliseconds (upon signal from the logic section), and then returns to the 2-milliampere level. The two lamps are operated with a resistor wired in parallel across each lamp. If one lamp were to burn out, the other lamp would still be operated, but at a slightly different level.

Telemetry is provided for several radiometer functions to establish calibration of the instrument and to monitor its operating status. Four temperature sensors are located in the portion of the housing viewed during back scan. These are used to establish an in-flight calibration of the thermal channel. Another temperature sensor monitors the case temperature of the bolometer, while two more monitor the temperature of the electronics in the scanner unit and in the electronics module. A telemetry output is provided to indicate if the -24.5-volt power is switched ON for the radiometer electronics. Another telemetry output monitors the rotation of the scan mirror; this output operates from either the -24.5-volt supply or the -28-volt supply anytime the scan motor is commanded ON.

Five test point locations are monitored in the electronics, and their outputs are brought to a connector on the electronics module, thus monitoring internal points in the electronic circuits without opening up the modules.

(3) OPTICAL DESIGN

The optical system consists of a scan mirror, a primary mirror, a secondary mirror, and a dichroic beam splitter which divides the energy into

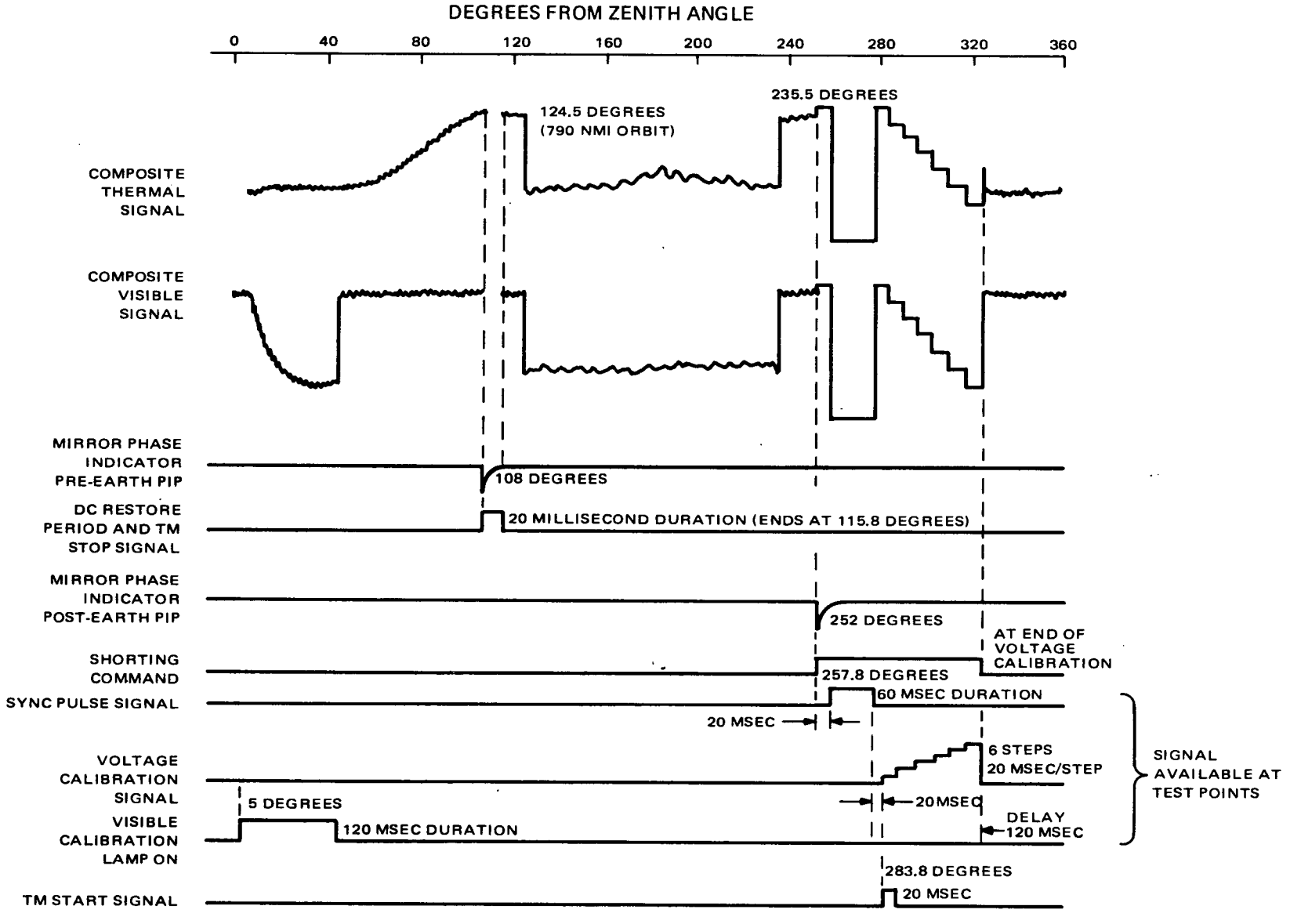


Figure 2-V-82. Scanning Radiometer, Signal Phase Relationships

two channels (see Figure 2-V-83). The 2.8-milliradian visible channel detects energy in the 0.52- to 0.73-micron band and consists of a visible filter, a field stop, and a silicon photovoltaic detector. The visible filter defines the spectral band width of the visible channel. The 5.3-milliradian infrared channel detects energy in the 10.5- to 12.5-micron band and consists of a bandpass filter (transmission portion of a dichroic), an Irtran II field lens (a relay lens) which also serves as a long-wavelength blocking filter, a folding mirror, and the germanium immersed thermistor bolometer. The combination dichroic filter beam splitter assembly defines the spectral bandwidth of the infrared channel. The design configuration of the radiometer is illustrated in Figure 2-V-84, which is an optical schematic showing the telescope and the filter detector module.

The "stop" at the primary mirror establishes the 5.0-inch diameter entrance aperture of the telescope. The obscuration by the secondary mirror and its holder is a 2.160-inch diameter. A concomitant objective of the telescope design was to provide baffling which prevents rays (energy) from the object scene from directly reaching the radiometer field stops. The design of the telescope baffles prevents this object scene radiation from reaching the field stops along calculated paths with less than two reflections from optically black painted surfaces. The design of a sunshade will further reduce the number of optical paths which have a small number of "reflections". Radiation which is diffusely reflected from the inside of the finned primary mirror baffle will reach the radiometer field stops and detectors by reflection from the center of the secondary mirror and, also, directly into the field stops. Consequently, a sunshade is needed to minimize the exposure of the finned primary mirror baffle (interior) to the sun's rays. The telescope baffling is designed to be compatible with the presence of a sunshade. The telescope tubular structure is grooved (for trapping stray radiation) and painted with 3M Velvet Black paint.

The telscope design provides a 101.7-cm^2 clear aperture area. While this is less than the 110-cm^2 design goal, the resulting loss in clear aperture area was offset by an increase in the energy obtained from the corners of the radiometer IFOV* in the infrared channel. The choice of the condensing optics design (in the filter detector module) utilizing a relay optical system provides more energy in the corners of the IFOV.

The telescope optical design utilizes spherical primary and secondary mirrors. The all-spherical mirror design provides a predicted image "spot size" of 1.5 milliradians within the 5.3-milliradian IFOV. The telescope focuses the image in the plan of the pseudo field stop. This image is relayed by an Irtran II lens onto the flake of the square thermistor bolometer, which is the actual field

*IFOV denotes "instantaneous field of view" as defined by the field stop in the visible channel, and defined by the bolometer flake in the infrared channel.

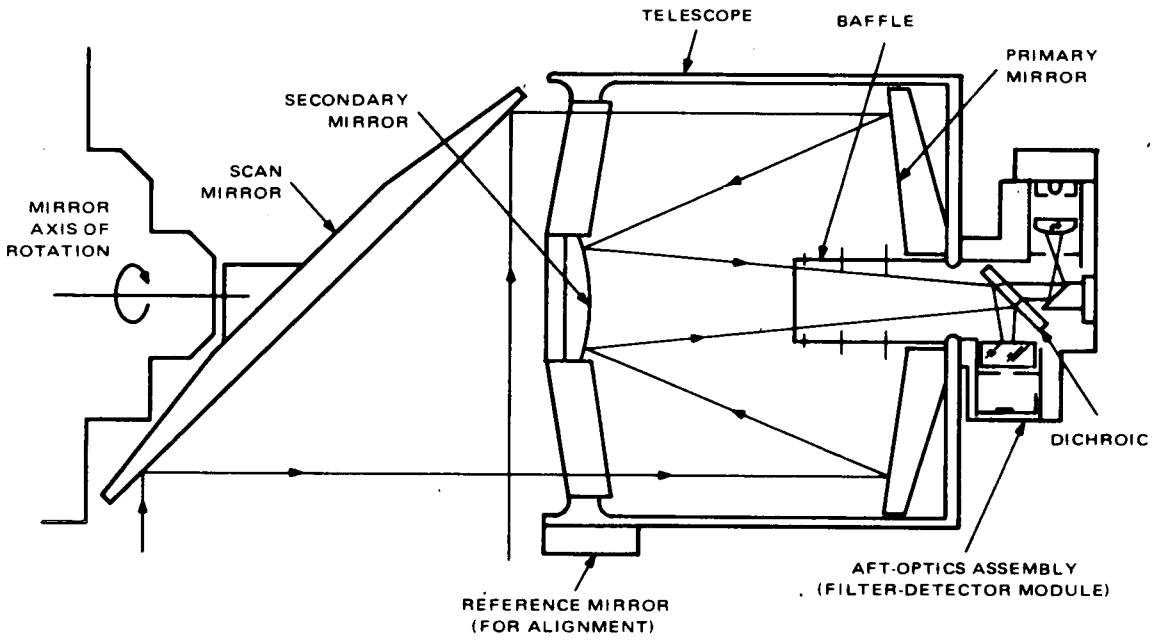


Figure 2-V-83. Scanning Radiometer, Optical Schematic

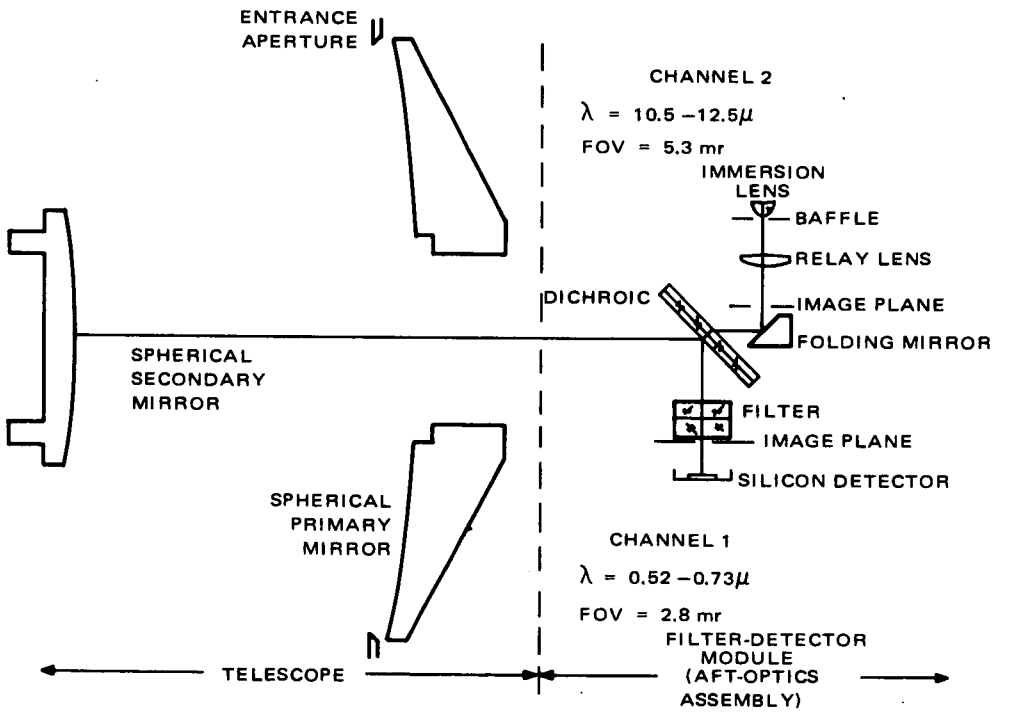


Figure 2-V-84. Scanning Radiometer, Detailed Optical Schematic

stop defining the IFOV of the infrared channel (see Figure 2-V-85). An oversized square "field stop-baffle" is located at the prime image to function as an additional baffle to reject stray radiation. If, however, the bolometer flake is slightly oversize, resulting in an out-of-tolerance IFOV, the field stop-baffle may be used as a "trimmer field stop" to accurately control the size of IFOV.

The telescope nominal back focus distance setting is accomplished by the adjustment of the secondary and primary mirror spacing, with the use of a shim at the rear of the secondary mirror. Fine focus adjustments of the filter detector module (aft optics section) to the telescope image location are accomplished with a shim installed between the telescope back reference surface and the mating surface of the filter-detector module.

The defocusing of the telescope over a $\pm 25^{\circ}C$ temperature range (caused by thermal expansion of the telescope tube and by mirror radii changes) is calculated to be ± 0.008-inch net change in back focus distance. The ± 0.008-inch shift from the nominal image plane is well within the "depth of focus" for a 0.026-inch diameter blur circle formed by a f/3.4 optical system. This consclusion was confirmed by data taken on a similar telescope design used in the NASA/GSFC Two-Channel Radiometer.

The active optical axis of the telescope is defined by the center of the IFOV of the infrared channel. The alignment of the telescope to the two reference mirrors mounted on the radiometer scanner housing is determined only after the assembly of the telescope and the filter detector module (aft optics). The filter detector module will be assembled and aligned to provide a nominal channel-to-channel alignment at the subassembly level. Final alignment, channel-to-channel, will not involve any changes in the telescope since the final alignment adjustments are provided in the filter detector module at the visible channel subassembly mounting.

Two types of condensing optical designs (in the filter detector module) were used in the design study: (1) aperture imaging on the bolometer flake and (2) field imaging on the bolometer flake. The latter case of "field imaging" was chosen for the scanning radiometer design.

The entrance aperture of the telescope is imaged on the immersed bolometer flake. The IFOV is defined at the field stop immediately in front of the germanium immersion lens. The simplicity of this optical configuration is desirable; however, the effectiveness of this approach depends upon the fixed optical parameters built into the immersed bolometer. In addition, the corners of the IFOV are almost entirely lost due to internal reflections of rays incident at angles exceeding the "critical" angle at the rear surface of the immersion lens.

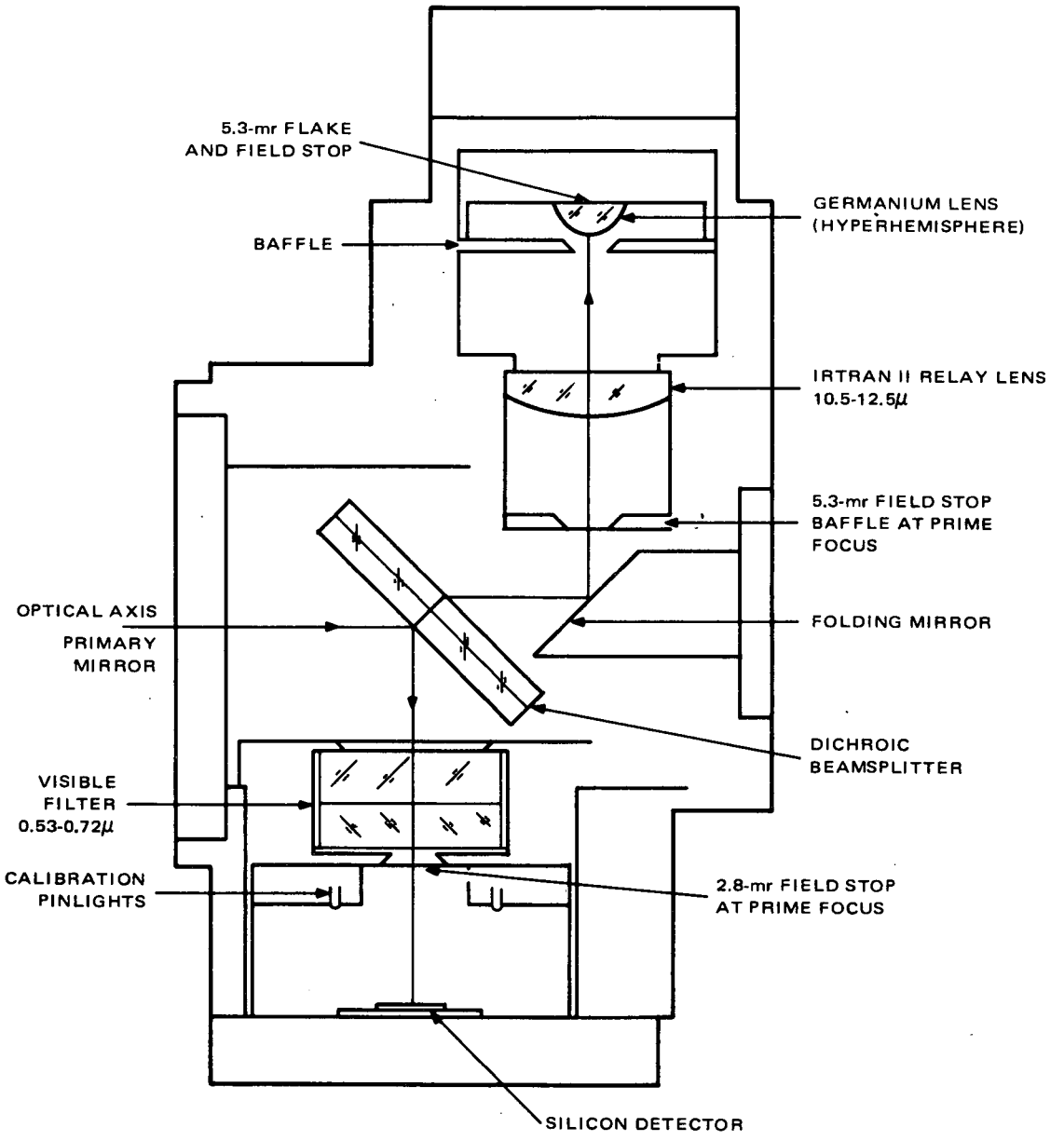


Figure 2-V-85. Aft Optics Assembly

Tests performed with aperture imaging condenser designs have indicated narrower measured IFOV's than predicted by the nominal optical design. In addition, the immersed bolometer optical tolerances have not always been held by the detector manufacturer. Consequently, the condenser optical design study was conducted to determine the IFOV-degrading effects of all combinations of optical tolerances in the immersed bolometer. The lowest reported value of the index of refraction of the modified selenium glass layer (2.45) was used because it sets the tightest limits on the bolometer internal acceptance angle. (The selenium glass layer, 0.0005-inch thick, is the optical immersion medium between the bolometer flake and thermanium immersion lens.)

Concurrent with a tolerance analysis of the aperture imaging condenser system, other condenser optical design configurations were evaluated. The basic approach to an improved condenser design was to distribute the optical tolerances among a greater number of optical surfaces and to provide degrees of freedom for corrective adjustments. The design goal was to use the same flake size as that used in the initially proposed aperture imaging condensing design (maintaining the needed optical gain of the system) but with "less critical" optical tolerances.

The bolometer flake size achieved for the optics using the field imaging condenser design is nearly identical to that originally calculated for the nominal aperture imaging design. In addition, the energy at the corners of the IFOV will be collected on the bolometer flake.

A more detailed diagram of the filter detector module is shown in Figure 2-V-85. Note the location of the visible calibration test lamp.

Figure 2-V-86 shows the distribution of energy across the field of view. The overall spectral response of each channel is given in Figures 2-V-87 and 2-V-88. These curves, which are typical for all scanning radiometers, were measured on the P-1 radiometer.

The dichroic filter/beamsplitter has undergone a major improvement during the development of this radiometer. The earliest model had a marked variation in reflectance over the spectral region sensed by the visible channel. This variation took the form of a cycle variation with 6 complete cycles in the interval of 0.50 to 0.86 microns. The minimum reflectance was as low as 4 percent, while the maximum was as high as 60 percent. Optical Coating Laboratories, Inc. was later able to produce dichroic filters/beam splitters with a reflectance characteristic which peaked near the center of the visible channel spectrum and gradually fell off at the two ends to a value of about 80 percent of the maximum transmission. This new filter proved to be durable and have a high thermal channel transmission.

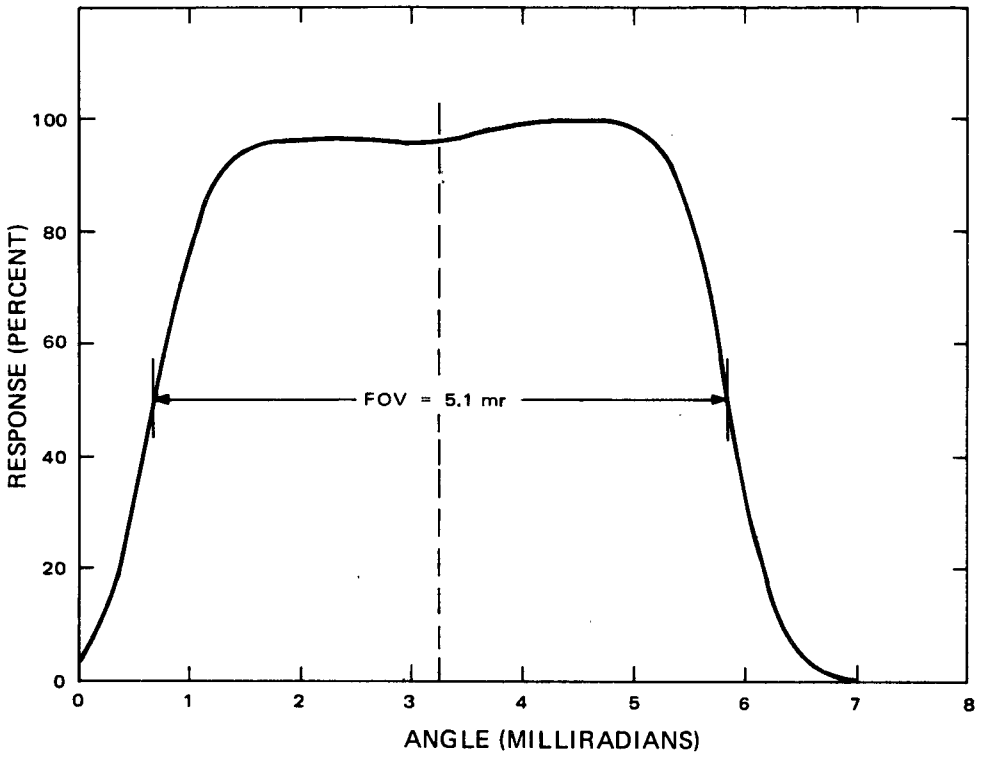


Figure 2-V-86. IR Response versus Displacement Angle

Three alignment mirrors are attached to the main housing casting. The mirror on the bottom of the scanner unit and one of the side mirrors are required to establish the coordinate system of the radiometer. During the assembly and alignment of the optics, the position of the scanned field of view is determined and related to the alignment mirror.

(4) MECHANICAL DESIGN

The scanner unit, which is on the outer spacecraft structure, was designed with a low profile in order to keep it within the constraints established by the launch rocket fairing. This requirement made necessary a very narrow neck area (with beryllium reinforcement rods) connecting the telescope and the scan mirror drive. The length of the radiometer has also been held to a minimum in order to reduce the overall profile.

The scanner consists of four subassemblies:

- Scanner housing
- Scan mirror drive assembly,

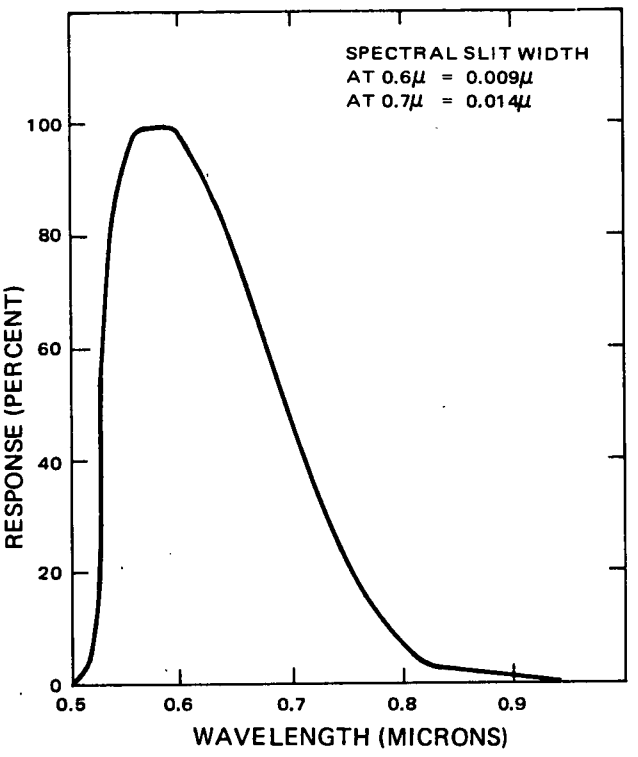


Figure 2-V-87. Visible Channel, Relative Spectral Response

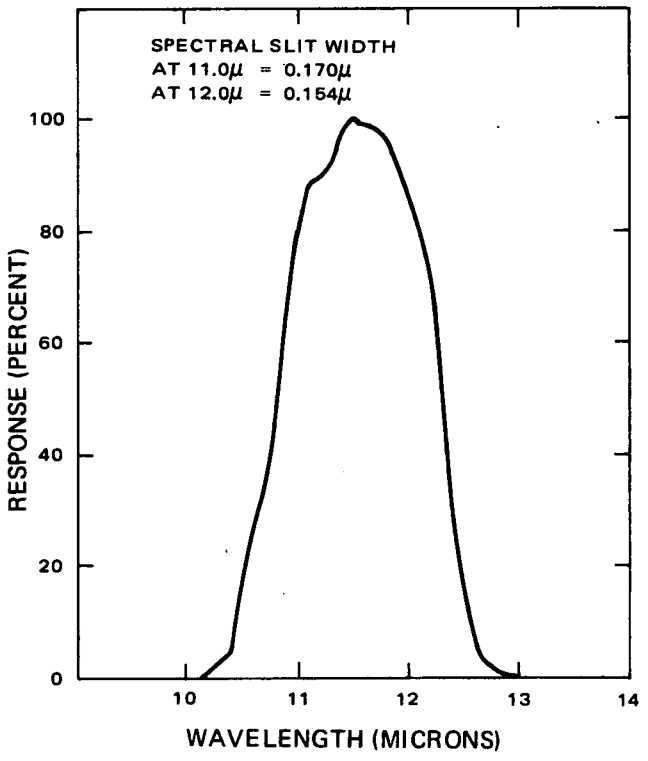


Figure 2-V-88. IR Channel, Relative Spectral Response

- Telescope assembly, and
- Aft optics assembly.

Figure 2-V-89 identifies the subassemblies and their locations. In addition, it shows the alignment mirrors to indicate necessary "clear paths" required for radiometer installation.

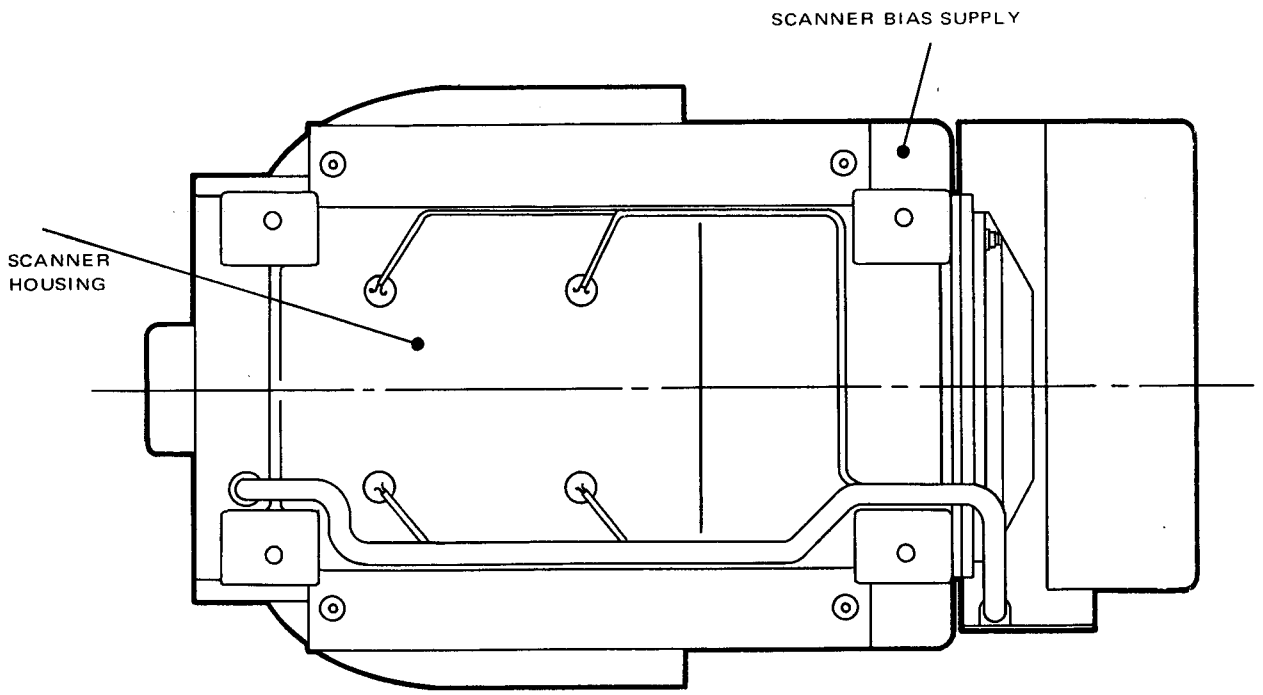
The main housing for the scanner is a cast magnesium tube (AZ91C alloy), open at the ends and locally along the wall to permit a scan mirror view of ±75 degrees. Four mounting pads (integrally cast) on C Section legs extend from the tube, 180 degrees from the mirror view opening. To ensure structural integrity through the throat section, two cylinders, also integrally cast, run parallel to the main radiometer axis between the C Section legs. A beryllium tube is held to withstand torsional loading but allowed to float axially to accommodate any expansion differential between the beryllium and magnesium.

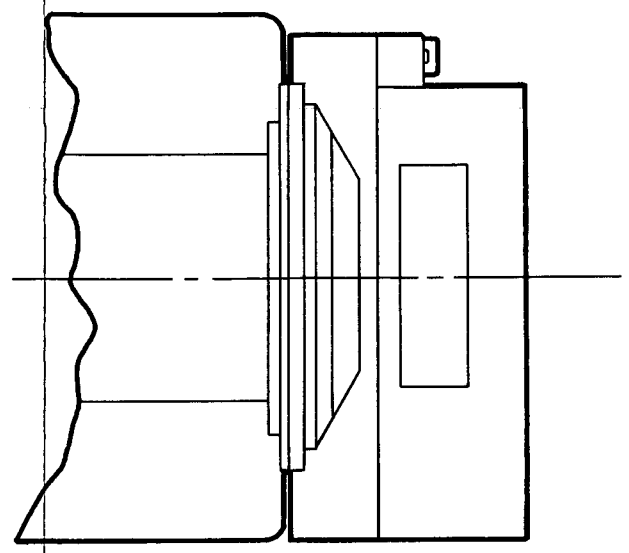
A serrated surface is machined into the housing wall directly opposite the mirror view opening and coated with a high emissivity paint to serve as a blackbody calibrator for the thermal channel. The temperature of this surface is monitored by four thermistors spaced on the surface.

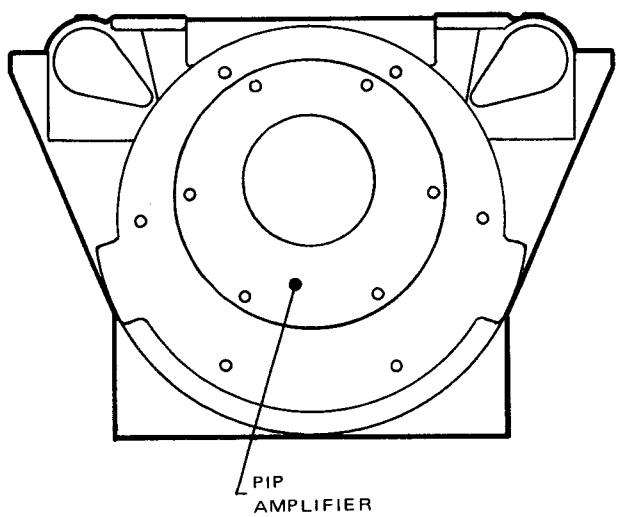
Alignment mirrors are located on the sides and bottom of the scanner to implement the spacecraft/radiometer alignment. The reference mirrors are Pyrex blanks with aluminum vacuum-deposited on the surface, epoxied into the casting.

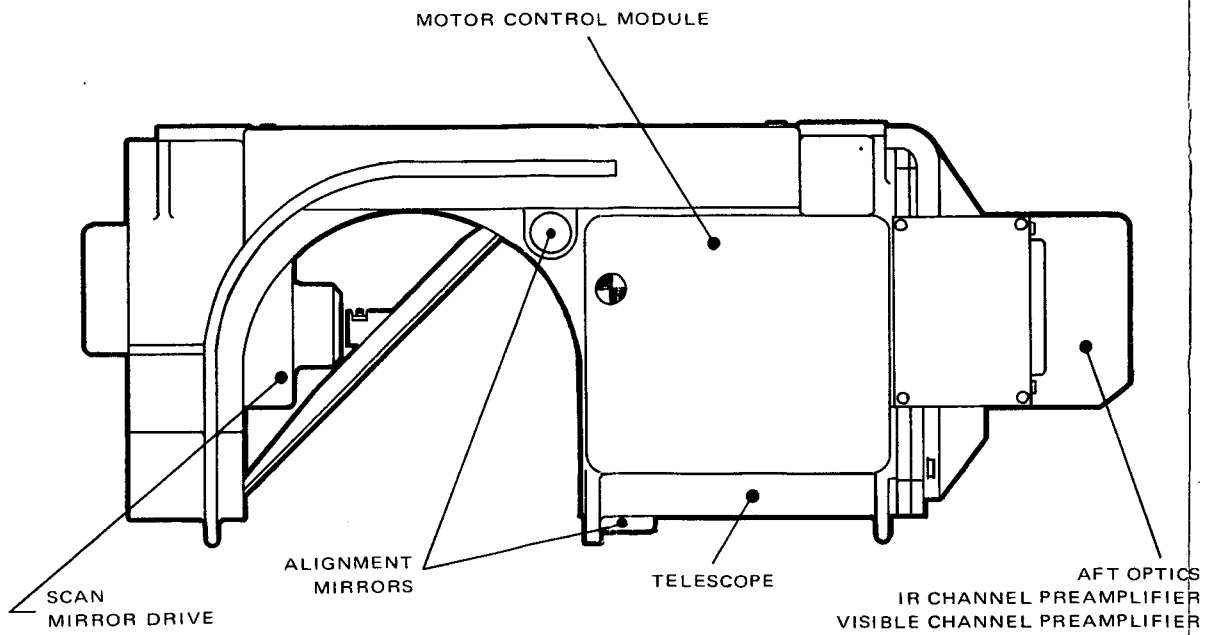
The scan mirror is driven by a 2000-rpm synchronous motor having an output torque of 0.12 oz-in. The ball retainers in the motor bearings are phenolic, vacuum impregnated with Pioneer P10 oil. A nylasint reservoir impregnated with P10 oil is also contained in the motor case. The motor has a labyrinth seal at the output shaft and is otherwise sealed from the environment.

A magnesium casting forms the outside housing of the scan mirror drive assembly. The register diameter is machined into the scan mirror drive housing to mate with the scanner housing. The mount flange and cover provide an external mounting surface for those subassemblies associated with the mirror drive and position readout; i.e., the magnetic head assemblies, the pip amplifier and a terminal board. Thus, the scan drive module allows head-to-magnet spacing, gear train run-in, and electrical checkout before assembly into the scanner housing.









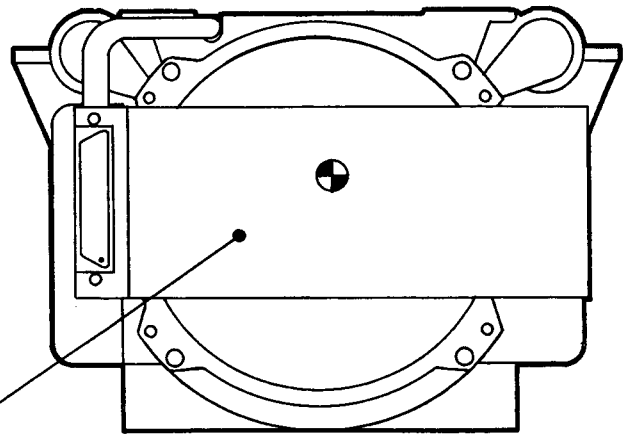


Figure 2-V-89. Scanner Housing Module, Outline Dimensions

FOLDOUT FRAME 1

FOLDOUT FRAME 2

A stainless steel (type 416) shell with grooves for O-ring seals is fitted into the magnesium casting to provide support for the bearings and the gear shafts. The advantages gained from this design are:

- Precision inline boring of the bearing supports;
- Similar thermal-expansion characteristics; i.e., stainless steel sheel, bearings, shafts and gears; and
- Bearing preload adjustment and overall gear train inspection and checkout can be performed before assembly into the scan drive castings.

The gear train consists of two meshes with an overall reduction ratio of 40.67:1. The reduction from the motor to the mirror is in two steps, as follows:

- 2000:288 rpm, and
- 288:48 rpm.

The gears and pinions are made from 416 stainless steel to AGMA No. 14 quality, with contract surfaces electrolized to obtain maximum wear resistance.

Although antibacklash gears are used, the combined residual backlash and transmission error remaining in the system was calculated to be 0.00345 radian total. Test data indicates that the jitter resulting from backlash is less than 0.0005 radian.

The seal at the output shaft of the scan drive assembly is a modified labyrinth arrangement with a nominal 0.0004-inch clearance around the shaft exposed to the space environment. A bypass arrangement encourages vapor flow around, rather than through, the bearing immediately inboard of the labyrinth opening. Calculations show a flow rate of 1.05×10^{-4} grams per year, based on Pioneer P10 oil, through a 0.0004-inch clearance around a 0.375-inch diameter shaft.

The telescope assembly is simply a tube closed at one end with a bracket. The bracket is common to the telescope and the aft optics housing; it is the support for the primary mirror on the forward side and provides registry and support for the aft optics on the back side.

The aft optics housing assembly consists of a rectangular block with the detectors and optical elements mounted in tubes which assemble into and register to the block. The dichroic mirror is inserted into one end of the block and is pinned for accurate alignment. The 45-degree folding mirror is inserted into the back side with a register diameter and pins for accurate alignment.

The scanner cavity from the mirror view opening through the detector preamplifiers will be gasketed to minimize radio frequency interference. The gasketing

used will be Metex strips bonded where necessary with space-qualified electrically conductive adhesive. It is impossible to effectively eliminate RFI through the scan mirror look opening.

The electronics module (Figure 2-V-90) contains five circuit boards. Four of these boards are mounted in conventional printed circuit board slides and they plug into a mother board which is keyed to prevent insertion of the wrong board. These boards may be removed by unscrewing a side cover.

The power supply board is located in the machined-out base of the module. This location provides improved heat sinking for the power transistors and provides a metallic shield around the DC-to-DC converter. This circuit board is covered with a dust cover, which is flush with the mounting flanges. All joints between covers and the main machining of the module are fitted with Metex strip RF gaskets.

Each of the four connectors on the box is used for a separate type of signal, as follows:

- J1 - output signals,
- J2 - power input and commands,
- J3 - telemetry outputs and test points, and
- J4 - radiometer interconnections.

b. DUAL SR PROCESSOR

(1) GENERAL DESCRIPTION

The dual scanning radiometer (SR) processor is designed to form the necessary interfaces between the scanning radiometers, the SR tape recorders and the real-time transmitters of the spacecraft. Two complete SR processors, each associated with one scanning radiometer, are contained within the one dual SR processor module. Only the processor associated with the radiometer in use operates at a given time. Each processor consists of a real-time, double-balanced AM modulator, a seven-pulse sync generator to identify the start of each scan line of real-time data, and a dual commutator.

All the circuits in the SR processor were generated specifically to interface the scanning radiometer to the spacecraft; they are all solid-state, use low power, are lightweight, require no adjustment at the box level, and provide high accuracy.

The real-time AM modulator operates at a very stable carrier frequency of 2.4 kHz generated within the TBU.

This channel processes only IR data during the night portion of the orbit, and either visible or IR data in the day portion as dictated by ground command.

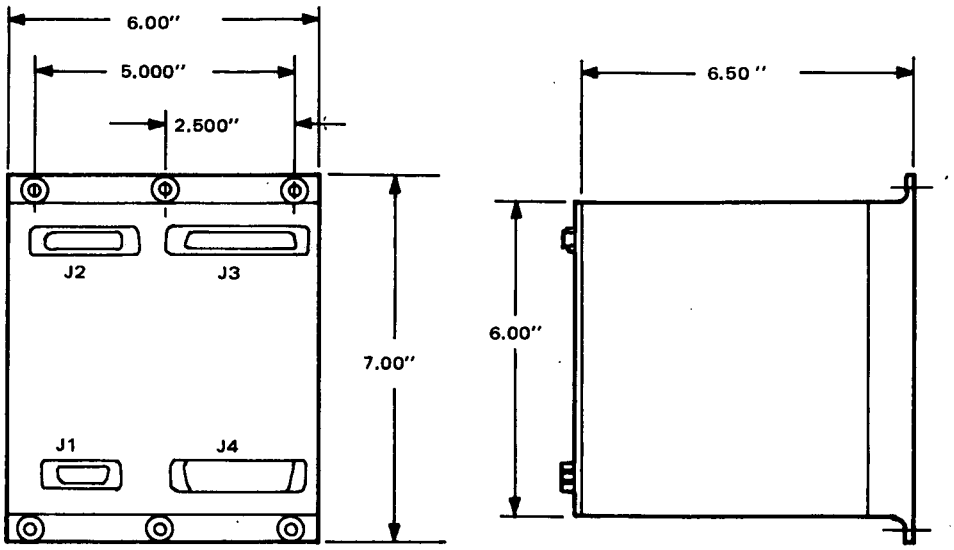


Figure 2-V-90. SR Electronics Module, Outline Dimensions

The IR data is inverted and level-shifted prior to processing, so that both IR and visible data will be displayed in the same format (i.e., black being lack of signal and white being maximum signal).

Both types of data are limited to a maximum output of -6.0 volts to prevent overmodulation of the transmitter during the radiometer housing scan; in addition, a signal of -0.110 volt is injected at all times to guarantee a minimum amount of carrier for maintaining sync of the ground equipment during flyback time, when the data level is expected to be very low.

Each scan line of either visible or IR data is preceded by a seven-pulse synchronization signal at 300 Hz. This signal is introduced by the SR processor at the completion of the radiometer housing scan.

The purpose of the dual commutator is to interleave IR and visible data with spacecraft telemetry data. The IR and visible data vary during the earth scan, but are constant during the housing scan, when calibration is introduced. As a result, 50 percent of the recorded data would be always constant. During the housing scan, therefore, the IR and visible data outputs are disconnected from the recorder and telemetry is connected in their place; this occurs in all cases, except once during each data frame, when the housing calibration is recorded.

The two commutators are controlled by a single address register and set decode gates; they therefore advance simultaneously.

The timing signals for stepping are generated by the scanning radiometer; the TLM OFF signal occurs at the end of the housing scan and is used to connect IR

and visible data to the recorders; likewise, the TLM ON signal, which occurs at the beginning of the housing scan, is used to connect telemetry.

The IR and visible data streams are identified by marker frequencies occurring in place of telemetry in channel 2 (see Table 2-V-14 for complete channel assignments). The IR marker frequency is 300 Hz, the visible marker frequency is 150 Hz.

(2) FUNCTIONAL OPERATION

(a) Real-Time Channel

The real-time channel of the SR processor consists of a signal conditioner and selector, a signal limiter and carrier injection circuit, a double-balanced AM modulator, a low pass filter, an output buffer amplifier, a real-time selection circuit, a modulator chopper, and a disable circuit. A block diagram of the real-time channel is shown in Figure 2-V-91. Details of this circuit are explained in the following paragraphs and are shown on RCA 1976099, sheet 3, in the Logic Diagram Manual previously referenced.

TABLE 2-V-14. IR COMMUTATOR INPUT POINTS

IR Commutator Point on Figure 2-V-92	Description
a	IR signal
c-f-j	300-Hz marker signal
d-f-j	Roll sensor 1 and pitch indicator pulse TLM
e-f-j	Roll sensor 2 and pitch indicator pulse TLM
b-g-j	SR housing temperature A TLM
c-g-j	SR housing temperature B TLM
d-g-j	SR housing temperature C TLM
e-g-j	SR housing temperature D TLM
b-h-j	Electronic module temperature TLM
c-h-j	IR bias voltage TLM
d-h-j	Scan monitor TLM
e-h-j	SR power monitor TLM
b-i-j	-24.5-volt SR processor power TLM
c-i-j	Time code
d-i-j	0-volt reference
e-i-j	Full-scale calibrate voltage

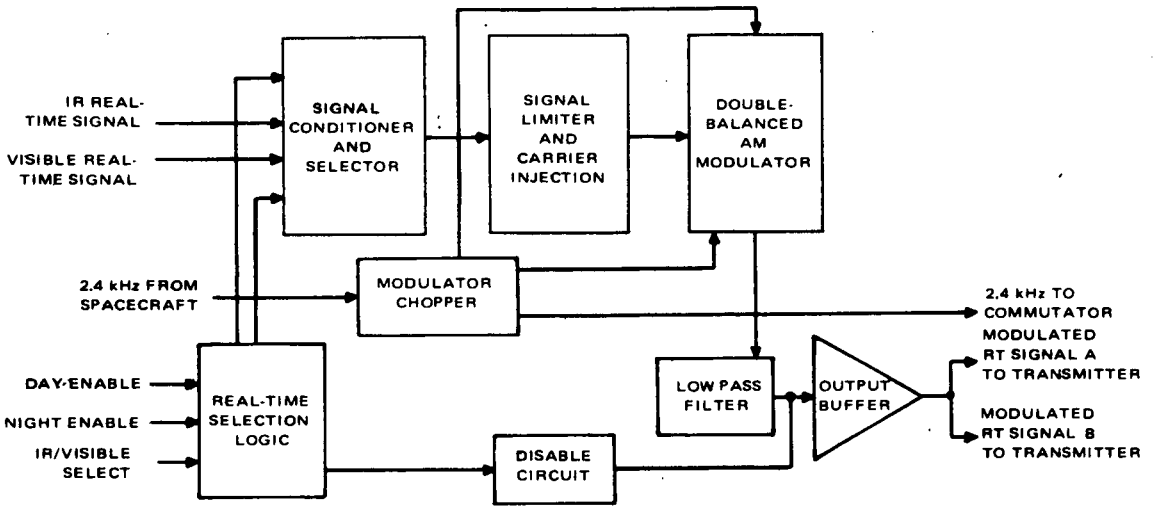


Figure 2-V-91. SR Processor Real-Time Channel, Block Diagram

1. Signal Conditioner and Selector

The IR channel data, which is to be level-shifted and inverted, is connected to the amplifier inverting input by turning on FET Q1. The level shifting is accomplished by adding a fixed positive voltage to the IR input data, the voltage level being determined by VR1 and resistors R6 and R69. Note that when FET Q1 is on, FET Q3 is also turned on, thus balancing the impedances in the two operational amplifier inputs to minimize current offset errors. The feedback resistor R13 determines the overall gain of the IR signal as it is applied to the limiter and signal injector stage.

The visible channel data is applied to the voltage follower input of Z1 by turning on FET Q2. When Q2 is turned on, Q1 and Q3 are turned off. The gain of the visible signal channel is made equal to the gain of the IR signal channel by selection of the resistance values of R71, R10, and R14. Resistors R9 and R68 are included in the input leads to make the load impedance on the IR and visible signal channels 10 Kilohms, as dictated by system requirements.

2. Limiter and Signal Injector

The limiter and signal injector functions are performed by operational amplifier Z2. The output of Z1 is normally a negative voltage. Should this voltage tend to go positive, it will be clamped to ground by the dual transistor Q17. Temperature effects on the limiter circuit are minimized by means of two identical base emitter junctions. The current variation offset as

the input voltage increases has been reduced to less than 30 millivolts by biasing the diode-connected transistor at the midpoint of the expected input voltage excursion. When the input becomes more negative than -3.75 volts, the output of Z2 is clamped at +6.8 volts by zener VR3 in its feedback loop.

Signal injection is necessary to maintain the output of Z2 at a positive level at all times so that the carrier will not disappear when the IR or visible input data goes to zero. This is a ground station requirement to allow the facsimile equipment to maintain sync during flyback. Injection is performed by adding a small voltage, as determined by VR2, R19, and R20, to the input of the limiter stage. This bias voltage causes reduction in dynamic range, and a slight offset of the DC level in the data provided by the SR. Since the range is compressed only in areas of low sensor accuracy and since the output signal of the modulator is AC in nature, these two effects are not significant.

3. Double-Balanced Modulator

The double-balanced modulator consists of operational amplifier Z3, FET's Q4 and Q5, and associated resistor networks.

The 2.4-kHz modulator chopper outputs are used to alternately ground the inverting and non-inverting inputs of the operational amplifier by means of FET's Q4 and Q5. The feedback resistor R33 in conjunction with resistors R26 and R27 determines the gain in the inverting mode, while the gain in the voltage follower mode is determined by the divider network composed of resistors R31, R29, and R28. The two series resistors in each amplifier input are chosen to minimize amplifier offset by matching the impedances of the two inputs in either state. The output of Z3 is thus a 2.4-kHz square wave, symmetrical about ground, whose amplitude is a function of the modulating input. This amplitude-modulated waveform contains all the odd harmonics of the carrier, of each of the sidebands, and of the modulating signals. Therefore, it is necessary to use a low pass filter to eliminate the unwanted higher harmonics and to generate the sine-wave carrier amplitude-modulated signal required to modulate the transmitter.

4. Output Buffer Circuit

The output buffer circuit is used to provide a low impedance source to drive the transmitter. It is composed of a Middlebrook stage, which has all the advantages of a Darlington amplifier and, in addition, causes only one base-to-emitter drop between the input and the output. Two isolated outputs are provided to feed the two redundant transmitters used in the spacecraft. The 100-ohm resistors in the output provide short-circuit protection.

5. Output Disable Circuit

The output disable circuit is used to short the output of the SR processor to ground in case neither a day enable nor a night enable signal is present from the spacecraft command subsystem, as indicated by the output of the two logic gates contained in Z4.

6. Modulator Chopper Signals

The two buffers, C and D, are always opposed in phase and are used to interface the 0- to +5-volt square waves available from the spacecraft command subsystem with the 0- to -24.5-volt signal required to operate the FET's. The -24.5-volt signal is required to ensure reliable turn-off of the FET's in the space radiation environment specified for ITOS.

7. Mode Selection Circuit

The mode selection circuit consists of the logic necessary to select the signal to be modulated (either IR or visible) and the buffers required to turn off the appropriate FET's in the signal conditioner to inhibit the unwanted signal.

The output signal and the associated programmer signals are as follows:

Output Signal	Programmer Signals
IR	Night enable or day enable and IR enable
Visible	Day enable and visible enable
No Signal	Lack of either day enable or night enable

Note that buffer A swings between +5 and -24.5 volts, while buffer B swings between ground and -24.5 volts. This voltage swing prevents pinchoff of FET Q1 when its drain swings positive due to the lack of an input from the scanning radiometer.

(b) 7-Pulse Sync Generator

Each of two circuits in the board (one associated with each radiometer) generates a 7-pulse train at a frequency of 300 Hz and inserts it at the beginning of each scan line of both the IR and visible data. The pulse train is synchronized by means of the TLM STOP signal, which occurs when the scanning mirror completes the housing scan. See RCA 1976099, sheet 5, in the Logic Diagram Manual previously referenced.

1. Sequencer

The sequencer controls the generation of the 7-pulse train, its insertion into the data stream, and its termination. The sequencer is made up of flip-flops 6F and 7F. The sequencer is normally in the rest state, at which time the scanning radiometer outputs are connected to the SR processor real-time channel by the series FET switches Q1 and Q2. As soon as the TLM OFF signal is received, the 1F flip-flop is set on the next 2.4-kHz clock pulse causing the following events:

a. The 2.4-kHz is applied through gate G4 to the divide by 8 chain, composed of 2F, 3F and 4F. These flip-flops generate 300 Hz; flip-flop 5F follows 4F but delayed by one 2.4-kHz clock pulse. This delayed 300 Hz is gated out by G15 and then becomes the 300-Hz sync frequency.

   Flip-flops 2F through 5F are held set by gates G1 and G2 (paralleled to obtain the required fanout) during the time that the TLM OFF signal is not present. This ensures the proper starting condition so that a complete 300-Hz pulse is generated at the start of the sync pulse train.

b. One 2.4-kHz clock pulse after 1F is set, 6F is set, taking the sequencer to state 2 and allowing the 300-Hz output from G15. At the same time, G10 goes low, turning off the series FET's Q1 and Q2.

c. The 300-Hz clock, gated by G6 and inverted by G7, is applied to the 7-pulse counter composed of 8F, 9F, 10F and 11F. This counter was reset by G1 and G2 so that it starts always from count zero.

d. When the 7-pulse counter reaches the count of seven, the sequencer is advanced to state 3, stopping the 300-Hz sync frequency and turning on FET's Q1 and Q2 again.

e. The sequencer remains in state 3 until the TLM OFF signal is terminated. This is necessary to prevent the generation of a second set of 7-pulses in case the TLM OFF pulse should last the maximum time of 25 milliseconds.

f. At the termination of TLM OFF, the sequencer advances to state 4 on the next 2.4-kHz clock and from there back to state 1, at the same time resetting flip-flop 1F, so that it will be ready to start the entire sequence on the next TLM OFF pulse.

2. Buffer

This circuit is also used in the real-time channel board to control the same type of FET's. It operates as described below.

When the input to R4 is high, transistors Q3 and Q4 are both off and the gates of FET's Q1 and Q2 are grounded to keep the devices on; but when the input is low, both Q3 and Q4 turn on, applying -24.5 volts to the FET gates to turn them off.

The diodes CR1 and CR2 used to isolate Q1 and Q2 are very-low-leakage units, chosen to minimize crosstalk between the IR and visible data.

3. Signal Conditioners

These circuits are used to change the positive logic levels of the 300 Hz to negative levels compatible with the IR and visible data. Two identical circuits are used, one for the IR and one for the visible data channels. They operate as described below.

When the input from G15 is high, transistors Q5, Q6, Q7 and Q8 are off and the output is grounded by the 10-kilohm load resistor located in the real-time channel board IR and visible inputs; when the input is low, however, transistors Q5 and Q7 conduct and saturate Q6 and Q8 so their collectors are held at -8volts. The -8-volt level has been chosen to ensure full swing of the modulated signal output when the sync pulses are present. By using this type of circuit, no further circuitry is necessary to isolate the signal conditioners from the data. The 2N2222A transistors used in the output are very low in leakage so that there is no loading of the IR and visible data when the transistors are off.

(c) Commutator

The commutator in the SR processor consists of two completely isolated, synchronously-switched commutators, each having 16 inputs. A block diagram of the commutators is shown in Figure 2-V-92. (Details of the SR processor commutator are explained in the following paragraphs and are shown on RCA 1976099, sheet 4, in Logic Diagram Manual previously referenced.)

The 16 inputs of each commutator are not sampled sequentially; channel 1 (IR or visible signal) is interleaved with the other 15 points so that the sequence is as follows: 1, 2, 1, 3, 1, 4, 1, 5...1, 16. The purpose of interleaving the telemetry points with the SR data signal is to make use of the inactive period of the radiometer which occurs when the scan is directed into the mirror housing. This period occupies approximately 50 percent of the total

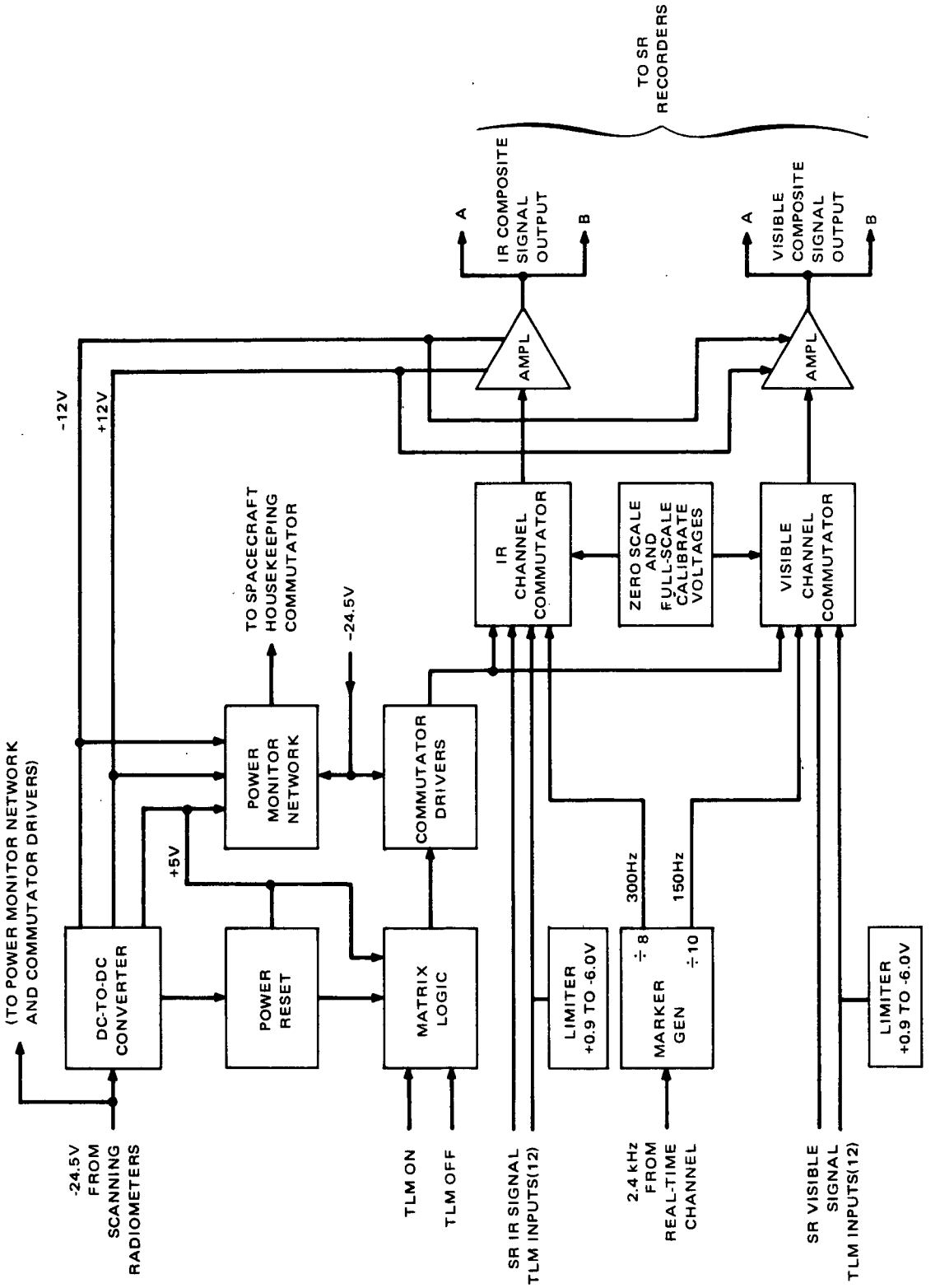


Figure 2-V-92. SR Processor Commutators, Block Diagram

scan, during which the radiometer produces only a calibration signal. The calibration signal does not have to be monitored continuously since it is not expected to change appreciably from scan to scan; it is, rather, an indication of component drift due to aging. The calibration data is recorded once per data frame by maintaining channel 1 on during the housing scan.

The commutator consists of a three-level tree of FET enhancement mode switches which are turned on by an address register and associated decode gates. Figure 2-V-93 shows the FET connections; Figure 2-V-94 is the corresponding timing diagram.

The timing signals required for advancing the commutator are provided by the scanning radiometer as the scanning mirror is rotated, so that there can never be loss of synchronization between the incoming data and the processor output.

From the connections of Figure 2-V-93 it is seen that IR and visible data are switched by turning on FET "a", while the telemetry inputs require the turning on of three series FET's, namely "j", one of "f", "g", "h", "i", and one of "b", "c", "d", "e".

The timing diagram of Figure 2-V-94 shows that "a" and "j" are mutually exclusive. The diagram also shows that "f", "g", "h", and "i" are on during eight states each, during which time "b", "c", "d", and "e" are each on during two states.

Descriptions of the inputs to the IR commutator points are given in Table 2-V-14 and of the inputs to the visible commutator points in Table 2-V-15.

1. Address Register Decode Gates

The address register is composed of flip-flops A1F, A2F, A3F, and A4F. These flip-flops make up two synchronous Johnson counters of 2 stages each, thus providing a total of 16 states. Each state is gated with the clock to generate the 32 timing states of Figure 2-V-93, Paragraph 2.V.D.3.b.(2).

The timing signals that advance the commutator are the SR TLM ON signal and the SR TLM OFF signal. These two signals are used to indicate the transmission of telemetry and IR/visible data, respectively, and to set and reset the flip-flop made up of two cross-coupled gates with the output taken from pin 8 of Z10. This comprises the clock that advanced the address register and turns on FET "j" in the timing and connection diagrams.

The decoding of the timing states can be accomplished by two input gates since flip-flops 1AF and 2AF are common to gates b, c, d, e and flip-flops 3AF and

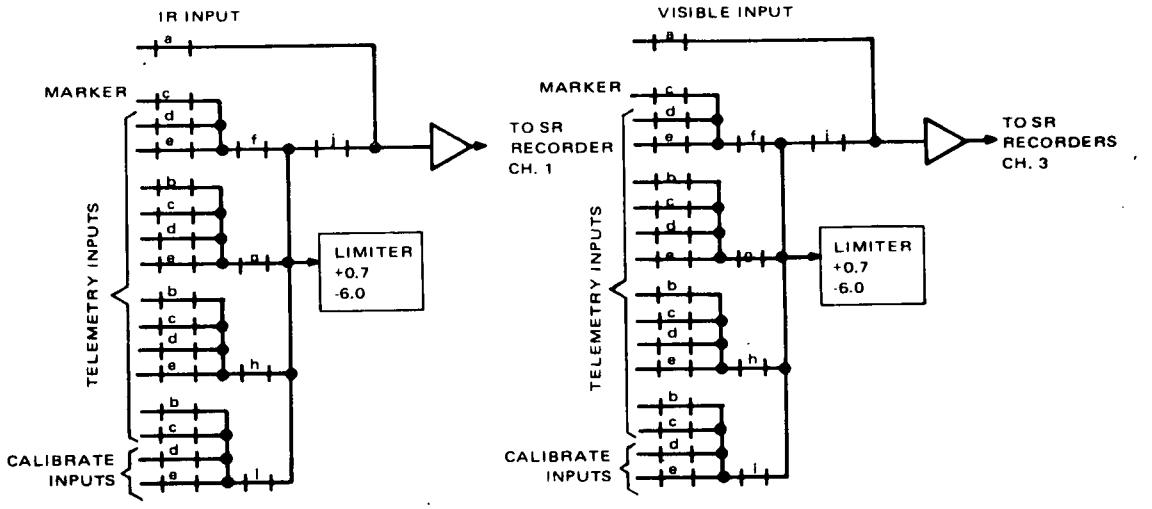


Figure 2-V-93. Commutator FET Connection Diagram

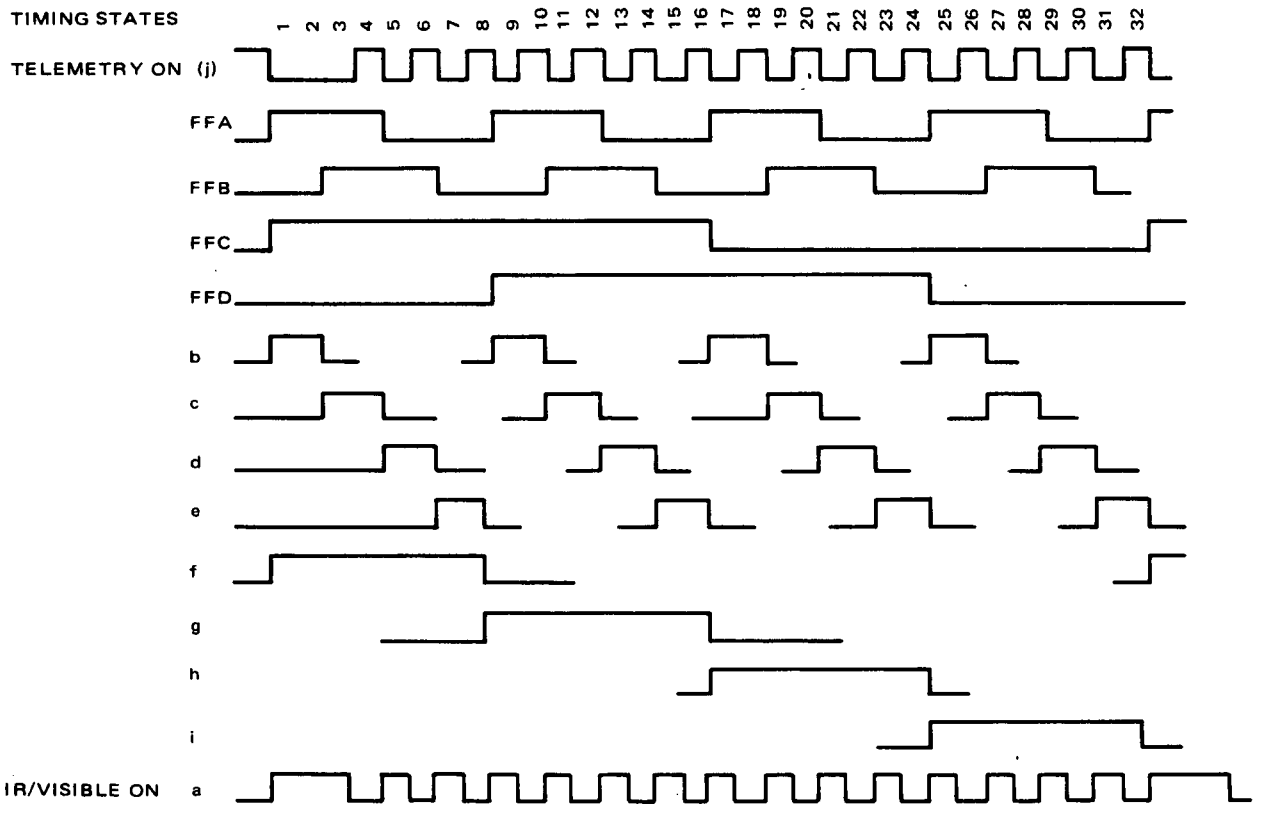


Figure 2-V-94. Timing Diagram for Commutator FET's Showing One Complete Frame of 32 States

TABLE 2-V-15. VISIBLE COMMUTATOR INPUT POINTS

Visible Commutator Point on Figure 2-V-92	Description
a	Visible signal
c-f-j	150-Hz marker signal
d-f-j	Pitch sensor 1 TLM
e-f-j	Pitch sensor 2 TLM
b-g-j	Spare
c-g-j	SR scan electronic temperature TLM
d-g-j	SR optics temperature TLM
e-g-j	APT camera 1 TLM
b-h-j	APT camera 2 TLM
c-h-j	Spare
d-h-j	Spare
e-h-j	Housekeeping TLM 1
b-i-j	Time code
d-i-j	0-volt reference
e-i-j	Full-scale calibrate voltage

4AF are common to gates f, g, h, i. Gate "a", however, requires four inputs since it selects state 2 from the 32 states in the frame.

2. MOS Drivers

The metal oxide semiconductor (MOS) driver circuit is used to interface the 0- to +5-volt logic levels to the 0- to -24-volt signals required to switch the FET's. The circuit is composed of a one-transistor, common

base stage with fast turn-on and slow turn-off, thus providing isolation between two adjacent channels of the commutator by turning one channel completely off before turning on the next one.

3. FET Switching Matrix

The connection and switching of the FET matrix are described in Paragraph 2.V.D.3.b.(2) and Figures 2-V-92 and 2-V-93, except for the control voltages necessary for the switching to be accomplished. The FET's used are p-channel, enhancement mode devices. They are normally off, thus presenting a high input impedance to the input data and are turned on by the application of a negative voltage to the gate. This voltage is normally -6 volts, but degrades with radiation to as high as -14 volts. Therefore, the gate voltage used in this application is -24.5 volts so that there will always be enough voltage to turn the devices fully on, even with the most negative data input. The body of the FET is tied to the substrate bias circuit, which is normally +1 volt, to prevent forward-biasing of the source-to-body diode in the event the input should go slightly positive; this same diode is protected if the source should be shorted to a positive voltage. The diode can carry up to 16 milliamperes of current, but the substrate bias circuit will limit the maximum current to 1.3 milliamperes in the event of a short to +12 volts. Noise filtering is provided by a 330-picofarad capacitor at each commutator input.

4. Limiter Network

The purpose of the limiter network is twofold: to prevent damage to the operational amplifier and the FET's in case of a malfunction and to limit the commutator output to levels compatible with the tape recorders. These functions are accomplished by diode CR1 for positive inputs, and by VR1 and Q1 for negative inputs, with resistor R2 acting as the major power dissipation element. In normal operation, R2 causes a very minute error due to high input impedance of the operational amplifier.

5. Power Reset Circuit

The purpose of the power reset circuit is to reset the commutator to state 32 upon application of power to the SR processor, so that a complete frame of data will be obtained. The output of this circuit is used to reset the address register. When power is first applied, capacitor C1 has no charge. Q1 and Q2 turn on and reset the address register by grounding the DC reset inputs of the flip-flops. As C1 charges, it reaches a voltage at which Q1 turns off, and Q2 cuts off. It then applies +5 volts to the flip-flops which allows

them to operate normally under the control of the SR TLM ON and SR TLM OFF signals. The pulse output of the power reset circuit lasts about 100 milliseconds, allowing time for any transients to decay before normal operation begins.

6. Full-Scale Calibrate Voltage

This reference voltage is generated by VR1 and resistors R8, R9, and R10. VR1 is a stable, temperature-compensated zener, and the resistors are chosen to produce a nominal -5-volt level. This level can differ from unit to unit because of variations in zener breakdown voltage and in resistance values. However, once established, this voltage will remain constant to provide the full-scale calibration level which is wired directly to channel 16 of each commutator. This voltage, in conjunction with the ground level applied to channel 15, will give zero and full-scale calibration references for each frame.

7. Marker Generator

Flip-flops M1F, M2F, M3F, and M4F are used to divide a 2.4-kHz input signal to obtain 300- and 150-Hz marker signals. These signals are level-shifted, by networks CR1, C3, and R6, and CR2, C4, and R7, to swing between ground and -5 volts. The 300-Hz marker signal identifies the IR commutator, and the 150-Hz marker signal is applied to the visible commutator. The marker signals make it possible to distinguish the IR data from the visible data on playback of the tape recorder, without having to keep track of recorder channel assignments. The spacecraft time code is also applied to channel 3 of each commutator and recorded for each data frame to obtain correlation between the data and the spacecraft position in orbit.

8. Power Monitor Telemetry Circuit

This is a housekeeping telemetry function which is not related to commutator operation, but only indicates normal operation of the DC-to-DC converter. If all converter outputs are present, the output of this circuit will be -4.5 volts; if any voltage fails, the output will change accordingly.

c. SCANNING RADIOMETER RECORDER (SRR)

(1) GENERAL DESCRIPTION

The scanning radiometer recorders (SRR's) provide the recording capacity for both the visible spectrum SR signals and the IR spectrum SR signals, as well as other ancillary signals generated within the SR subsystem. The functions of the SR recorders are to record, playback, and erase these signals, as required in the overall functions of the SR subsystem, and to provide the necessary internal control and switching for these functions from commands supplied by the spacecraft.

Each SRR is composed of two units. The SR recorder transport contains the tape transport and several component boards mounted within a pressurized spun-aluminum dome and base pan enclosure. The enclosure is 14 inches in diameter and approximately 7.5 inches deep; it is pressurized to 16.5 psia with a mixture of 90-percent nitrogen and 10-percent helium. The SR recorder electronics unit contains the majority of the signal and drive circuits, mounted on plug-in printed circuit boards, and an internal harness. Multipin connectors provide signal outlets to the spacecraft and SR recorder transport. The maximum total weight of the SR recorder is approximately 18.7 pounds, the recorder transport weighing approximately 13.3 pounds and the recorder electronics weighing 5.4 pounds.

The SR recorder transport assembly includes, in addition to the tape and DC torque motor, the component board assemblies listed in Table 2-V-16.

TABLE 2-V-16. SRR COMPONENT BOARD ASSEMBLIES

Board	Circuit or Components
A1 (plug-in)	Encoder shaper
A2 (plug-in	Motor driver
--A1	IR playback preamplifier
--A2	Flutter-and-wow playback preamplifier
A3	Visual playback preamplifier
A4	EOT playback and record switches (S1 and S2)
A5	Optical encoder
PU1	Playback heads (Tracks 1, 2, and 3)
PU2	Record heads (Tracks 1, 2, and 3)

The SR recorder electronics unit houses six plug-in circuit boards (see Table 2-V-17).

TABLE 2-V-17. SRR CIRCUIT BOARDS

Board	Circuit
A1	IR FM modulator; IR playback limiter
A2	Flutter-and-wow record head driver; flutter-and-wow playback limiter
A3	Visible FM modulator; visible playback limiter
A5	X2 multiplier (record); operational amplifier (including servo-loop stabilization components) and pulse width modulator including differential comparator and 12-kHz sawtooth generator); 5-second delay between playback and record commands
A6	-5.2-volt regulator supply; digital frequency and phase detector; phase error and 1200-Hz low pass filter
A7	1200-Hz record and 2400-Hz playback enable; EOT playback; command IR and flutter-and-wow playback command power gate logic and level set circuits

A simplified block diagram of the SR recorder is shown in Figure 2-V-95. Three channels of data storage are provided. Two channels (D1 and D3) store sensor video data (one IR and ove visible) from the SR processor in the form of frequency-modulated subcarriers. The third channel (D2) records a continuous pilot tone (3.125-kHz signal) from which tape speed variations (flutter-and-wow) can be detected and compensated for in the ground equipment. The frequency-modulated subcarriers, along with the 3.125-kHz pilot tone, are recorded on three tape tracks at a speed of 1.875 inches per second. The 1/4-inch magnetic tape passes over the erase head, over the record head, and then over the reproduce head. Each track has a total recording capability of 145 minutes. The record circuits are powered during the record cycle only. When the playback command is received, power is applied to the playback circuits, and simultaneously power is removed from the record circuits; the direction of tape reverses, and all three tracks may be played back simultaneously at a speed of 30 inches per second (16 times the record speed).

The input control signals and their functions to the SR recorder are listed in Table 2-V-18. The SR recorder's characteristics are summarized in Table 2-V-19.

TABLE 2-V-18. SRR INPUT CONTROL SIGNALS

Signal	Functions
Record	To activate tape recorder in the record mode.
Playback	To activate tape recorder in the playback mode and supply power to IR and flutter-and-wow playback electronics.
Playback Enable/Visible Power	To supply power to visible playback electronics.
Playback End-of-Tape (output)	To indicate completion of playback cycle.
2400-Hz Reference	To provide reference frequency for motor speed control.

TABLE 2-V-19. SRR CHARACTERISTICS

Parameter	Characteristic
Input Signals:	
Data Channels (1 and 3)	Composite video and sync signal; dual inputs single-ended amplitude: between 0 and -8.16 volts (unloaded)
F&W Channel (No. 2)	FM square wave subcarrier; amplitude: +4.4 ±0.6 volts; frequency: 3.125 kHz
Output Signals:	
Data Channels (Nos. 1 and 3)	FM subcarrier, AC coupled; amplitude: 2.0 volts (p-p) ±12.5 percent; frequency: 52.8 kHz corresponds to 0-volt input; 38.4 kHz corresponds to -8.16-volt input
F&W Channel (No. 2)	FM subcarrier, AC coupled; amplitude: 2.0 volts (p-p) ±12.5 percent frequency: 50 kHz ±0.5 percent
Track Allocation:	
Track 1	(SRIR)
Track 2	(F&W) 3.125 kHz
Track 3	(SR visible)
Tape Speed:	
Record	1.875 inches per second
Playback	30 inches per second
Speed Ratio	16:1

TABLE 2-V-19. SRR CHARACTERISTICS (Continued)

Parameter	Characteristic		
Tape Travel:			
Record	145 minutes (maximum)		
Playback	9.1 minutes (maximum)		
Tape Dimensions:			
Usable Length	1360 feet (Mylar base, magnetic tape)		
Width	0.25 inch		
Thickness	0.001 inch (nominal)		
Heads	One three-channel record head, One three-channel playback head, and One permanent magnet erase head (full tape width)		
Data Bandwidths:	Baseband	Subcarrier (± Deviation)	FM Spectrum
Data 1 & 3 Record (incl. sync tip)	0-0.45 kHz	2.85+0.45 kHz	1.95 to 3.7 kHz
Playback	0-7.2 kHz	45.60 ±7.2 kHz	31.2 to 60.0 kHz
F&W Data 2 Record		3.125 kHz	*
Playback		50.00 kHz	
Cumulative Flutter (Demodulated Baseband)	0.3 percent rms (0.5 to 7200 Hz)		
Power Drain:			
Standby	Less than 0.6 watt		
Record	Less than 7.5 watts		
Playback	Less than 10.0 watts		
Telemetry Signals (Analog):			
Off	0.0 volt nominal		
Standby/Record	-0.9 volt nominal		
Record	-1.8 volts nominal		
Playback	-2.7 volts nominal		
Transport pressure	From -0.5 to -4.5 volts		
Transport temperature	From -0.5 to -4.5 volts		

*Flutter-and-wow performance is measured in test over a 7.2-kHz baseband; however, because of the actual energy distribution, the baseband in the ground receiver is limited to 2.0 kHz.

TABLE 2-V-19. SRR CHARACTERISTICS (Continued)

Parameter	Characteristic
Motor: Running Voltage	DC Torque 24.5 volts
Recorder Transport: Angular Momentum (uncompensated) Acceleration Deceleration Mission Life	 Less than 0.02 inch-pound per second in either direction Less than 1.0 second (record mode): Less than 3.0 seconds (playback mode) Less than 1.0 second (record mode); Less than 5.0 seconds (playback mode) 1 year
Pressurization (Recorder Transport)	16.5 psia (90-percent nitrogen and 10-percent helium)
Seal (Recorder Transport)	O-ring, flange, and pressure fitting
Weight: Recorder Transport Recorder Electronics	18.7 pounds total (approx.) 13.3 pounds 5.4 pounds
Size: Recorder Transport Recorder Electronics	 14-inch diameter by 7.5-inch height

(2) DESIGN HISTORY

(a) Basic Source of Design

1. Electrical Design

With the exception of minor interface changes, the following were previously utilized for other spacecraft systems (refer to RCA 1976090 in the Logic Diagram Manual, previously referenced).

- The IR and visible channel FM modulators are identical. The IR and visible channel preamplifiers and limiters are identical and were used on a classified program. In both cases, minor interface and frequency changes were made.
- The flutter-and-wow channel preamplifier and limiter are identical to the IR and visible channel counterparts.

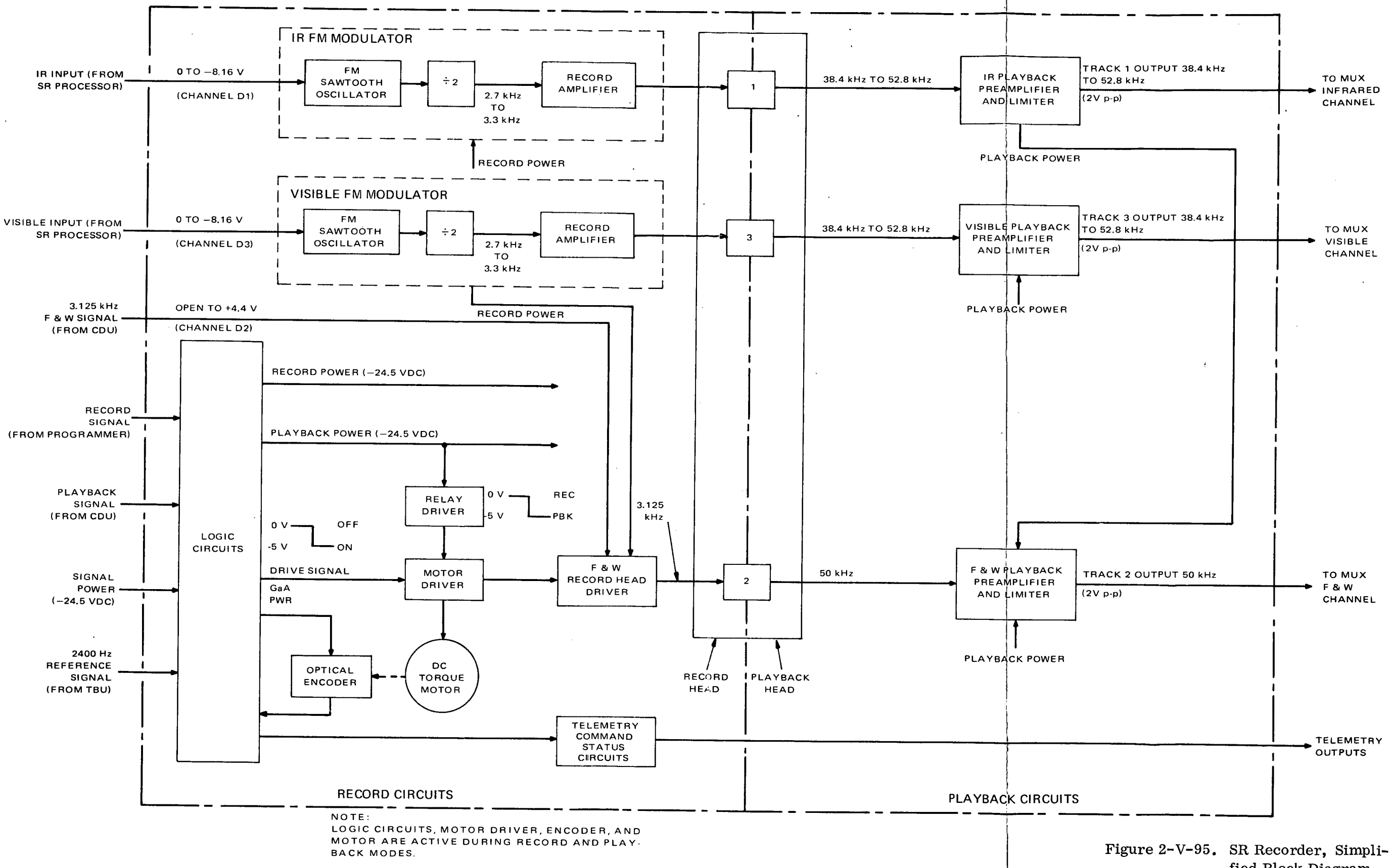


Figure 2-V-95. SR Recorder, Simplified Block Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

- The flutter-and-wow channel record head driver is similar to the IR and visible channel drivers.
- The record and playback heads are physically identical to the TOS AVCS heads and are electrically similar, except for small differences in frequency response.

The electronics for the command and control, power switching, tape drive, and telemetry circuits are of a new design, but the analog and digital circuitry is of a conventional type. The parts which have not been previously used include one Fairchild 710 μa comparator, one optical encoder (Gurley, RCA SCD No. 1970640), and one DC torque motor (Inland, RCA SCD No. 1970651).

2. Mechanical Design

The basic transport mechanism design is similar to the AVCS tape recorder used on the Nimbus, ATS, and TOS programs. The electronics container consists of a machined frame for the electronic circuit boards, instead of a casting.

(b) New Design

The following circuits were newly designed for the TIROS M SR recorder (refer to RCA 1976090 in the Logic Diagram Manual previously referenced):

- Command and control,
- Power switching, and
- Tape drive.

1. Command and Control Circuitry

The command and control circuitry is implemented with 12 Fairchild low power, integrated circuit gates, and interface and level-shifting networks. Although this type of circuitry has not been used previously for tape recorders, low power gates have been used very successfully on classified programs. The main reason for selecting integrated circuit elements for this application was the servo tape-drive system requirement for 6 flip-flops and 19 gate elements. The advantages of using IC elements as compared to discrete parts are higher reliability, lower power consumption, fewer number of printed boards, lower weight and volume, reduced design, analysis, and testing time, and lower production cost.

2. Power Switching Circuits

The servo loop and record mode power switches were specifically designed to control the turn-on current rate from the -24.5-volt supply line. The rate of current increase is controlled by current limiting, producing only 0.3-volt drop across the switches. The circuitry is conventional and operates within safe limits.

3. Tape Drive and Circuits

The tape drive consists of a phase-locked servo drive system using a DC torque motor and an optical encoder connected to the capstan. This type of design greatly reduces the mechanical complexity while still retaining the advantages of the basic AED coaxial reel-to-reel concept.

The electronics circuitry was designed for minimum power consumption, weight, volume, and high reliability. The circuit elements described in the following paragraphs make up the total servo drive.

The optical encoder shaper is a hard limiter which produces a 5-volt square wave output upon application of a 5- to 100-microampere sine wave current input. The optical encoder output currents range between 20 and 37 microamperes, over the operating temperature range. The function of the motor driver circuit is to supply a current to the DC motor that is proportional to the 12-kHz pulse width. On the same board is a 500-Hz critically damped (worst-case) supply line filter to attenuate high-frequency current components from the supply line and a relay and relay driver to reverse the motor current in the playback mode (the relay is not energized in the record mode). The motor driver circuit is essentially a power Darlington pair, with a saturating switch at the input to handle a playback turn-on current transient of 1.3 amperes, and yet provide an efficient drive during the record mode when current taken from the supply line is only 20 milliamperes.

Phase and frequency detection and digital control of the servo loop is accomplished with low power flip-flops and gates. A -5.6-volt zener regulated supply powers all the IC elements and provides signal clipping bias voltage at the interface circuits to eliminate excessive voltage being applied to the IC elements.

The logic is of conventional design, performing NAND functions, division, and frequency doubling of the encoder output pulses. The phase and frequency detector, also consists of flip-flop and gates. The three flip-flops, Z4, Z5, and Z6, are interconnected via gate elements 1A, B, C; 2A, B, C; and 3A, B, C in such a fashion that if the reference frequency is greater than the encoder freqeuncy, (this happens when either a record or playback command is applied), then the Z5Q output is at -5 volts. The Z5Q output remains at -5 volts until the encoder frequency is greater than or equal to the encoder frequency plus a count of 2 (or more than 2).

When the encoder frequency plus a count of 2 is greater than or equal to the reference frequency, then the Z5Q output becomes 0 volt and it remains at 0 volt until the encoder frequency equals the reference frequency. At that time, the influence of flip flops Z4 and Z6 is no longer present and the Z5Q output consists of a train of pulses. The pulse width is then proportional to the time difference between the reference and encorder pulse negative edges. This type of detector has the advantage of applying 100-percent error voltage to the system, which is very desirable for attaining the desired tape speed quickly.

The low pass filter is a three-stage linear phase filter (LC) and it attenuates the 1200-Hz frequency and higher frequencies by 50 decibels. The Z5Q output is applied to the input of the LC filter. In front of the filter is a saturating and inverting switch followed by a 6-volt zener diode, which standardizes the error amplitudes, followed by an emitter follower filter driver.

The gain set and operational amplifier circuits stabilize the servo loop. Operational amplifiers Z1 and Z2 have a gain of approximately one at very low frequency, but the gain (and hence the phase lead) is increased with increasing frequency. Maximum phase lead (75 degrees) occurs at 150 Hz and the phase lead is necessary to oppose the phase lag from the 1200-Hz filter and motor electrical time constant and to provide a phase margin. The phase lead is accomplished with simple lead-lag networks. Between Z1 and Z2 is a 600-Hz band stop filter (BSF). This is necessary to attenuate the half-frequency components resulting from doubling the 600-Hz encoder output frequency.

The sawtooth generator and differential comparator provide a pulse output at 12 kHz, whose duration is proportional to the DC level output from Z2. The sawtooth output is 8 volts and swings between -8 and -16 volts. The sawtooth circuitry is similar to the IR and visible FM modulators; the chosen 12-kHz frequency is well above any resonant frequency and yields low switching losses and low incremental speed variations (flutter). The 8-volt sawtooth amplitude choice was a compromise between the amount of tolerable noise and the loop gain. The differential comparator is a conventional one stage amplifier with a constant current source to handle large voltage swings at either input.

(c) Major Tradeoffs

1. Capstan Drive System Parametric Evaluation

The parametric evaluation of the capstan drive system showed that the best results would be obtained by using a DC servo drive system. Adaptability, mechanical complexity, size, weight, torque margin, drive system power, signal flutter, and mechanical reliability of the transport all favor the DC drive system. The SRR drive system major tradeoff characteristics are summarized in Table 2-V-20.

TABLE 2-V-20. SRR DRIVE SYSTEM TRADEOFF CHARACTERISTICS

Factor	Two-Speed Hysteresis Sync Motor and Belt	Two-Hysteresis Sync Motors and Five-Belt Planetary	Two-Hysteresis Sync Motors, Clutch, and Four-Belts	Servo, DC Capstan Motor and Optical Encoder
History at AED	Nimbus HRIR* at 8:1 ratio	Nimbus HDRSS** at 32:1 ratio	Nimbus HDRSS** (alternate bread-board only)	None. But used by CSD, Leach, Lock-heed, etc.
Adaptability	Poor speeds and ratios limited	Fair, constrained mechanically	Fair, constrained mechanically	Good, no mechanical constraints***
Mechanical Complexity	Moderate	High	Very High	Low
Size	Fairly compact	May require in-crease in can size	May require in-crease in can size	Very compact
Weight	1.8 pounds	1.7 pounds	2.0 pounds	1.75 pounds
Torque Margin	Marginal	Adequate	Adequate	70 percent in record 100 percent in play-back

*High Resolution Infrared

**High Data Rate Storage System

***A wide range of speeds and speed ratios are possible by changing:

(a) The reference frequency (external),
(b) The divide factor of the encoder frequency,
(c) The encoder lines per revolution,
(d) The clock pulses taken from the tape, and
(e) The capstan diameter.

TABLE 2-V-20. SRR DRIVE SYSTEM TRADEOFF CHARACTERISTICS (Continued)

Factor	Two-Speed Hysteresis Sync Motor and Belt	Two-Hysteresis Sync Motors and Five-Belt Planetary	Two-Hysteresis Sync Motors, Clutch and Four-Belts	Servo, DC Capstan Motor and Optical Encoder
Drive System Power	Rec: Very high 11.0 watts PB: 8.0 watts	Fair 3.5 watts Fair 7.0 watts	Fair 3.8 watts High 8.0 watts	Low 2.5 watts Low 4.0 watts
Flutter of Drive System	Bad 6 percent rms	Good < 0.3-percent rms	Good < 0.3-percent rms	0.2-percent rms 25° C
Mechanical Reliability of Transport	Good 0.18/1000 hours	Fair 0.43/1000 hours	Fair 0.37/1000 hours	Very Good 0.12/1000 hours

2. Optimization and Analysis of DC Servo Drive System

A comparison was made between the DC servo drive system and a synchronous drive system with regard to reduction of flutter. Servo loop stability calculations were made to determine overall gain and closed loop response measurements were made to determine the ability of the loop to correct flutter resulting from torque perturbations.

A mathematical model was used to determine the percent flutter-to-percent torque ratio of the synchronous motor drive; this was made suitable for a computer input, then solved, and the results are shown on the graph in Figure 2-V-96. The results depict very poor ability to reduce flutter produced by torque variations at 10 and 35 Hz. Five different Q factors were used because, although the actual Q is not known, it is estimated to be between 2 and 4.

The servo motor drive closed loop response curve (also shown on the graph in Figure 2-V-96) was obtained from the worst-case analysis and plotted for comparison with the synchronous motor drive hysteresis curves.

The detailed servo loop stability calculations involved an analysis of the servo drive system in both the record and playback modes of operation. An overall gain margin of 7 to 10 decibels and a phase margin of from 42 to 55 degrees were realized. The parameters and circuit components considered (shown on Figure 2-V-97) in the servo loop calculations are as follows:

- Gain calculation at one radian per second,
- Encoder,
- Phase and frequency detector,
- Servo loop frequency response,
- Operational amplifiers and loop compensating networks.
- Capstan maximum torque at -10° C and minimum torque at +50° C,
- Record and playback modes torque margins,
- Record and playback modes worst-case stopping times,
- Record and playback modes start times, and
- Applied tape tension and slippage during playback acceleration.

In the record mode, the 2400-Hz square wave input reference frequency is divided by two and applied to the phase and frequency detector, which effects the turn-on of the motor current. This condition prevails until the encoder produces 600 pulses per second and, hence, motor speed is 0.6 revolution

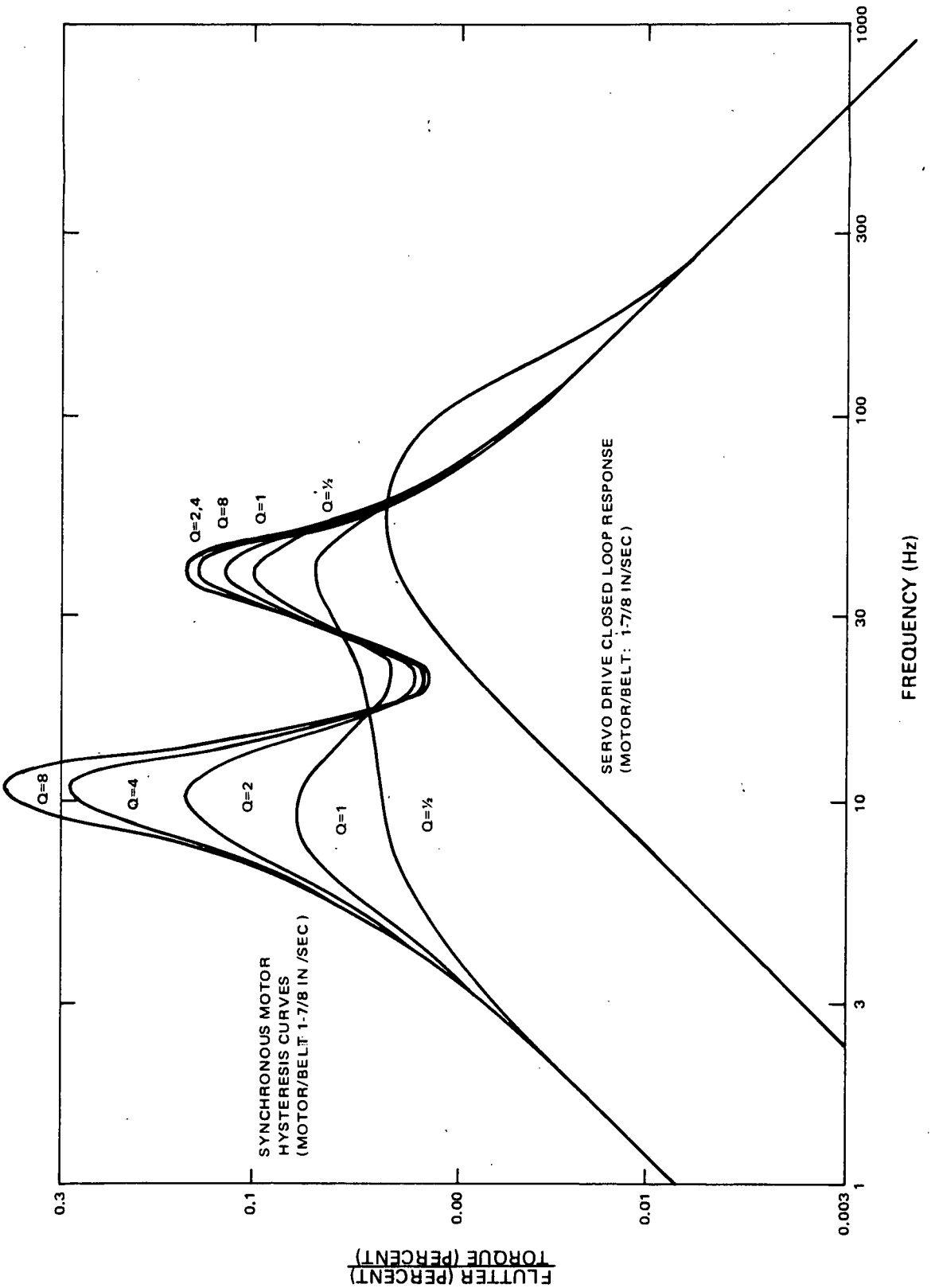


Figure 2-V-96. Flutter-to-Torque Ratio versus Frequency

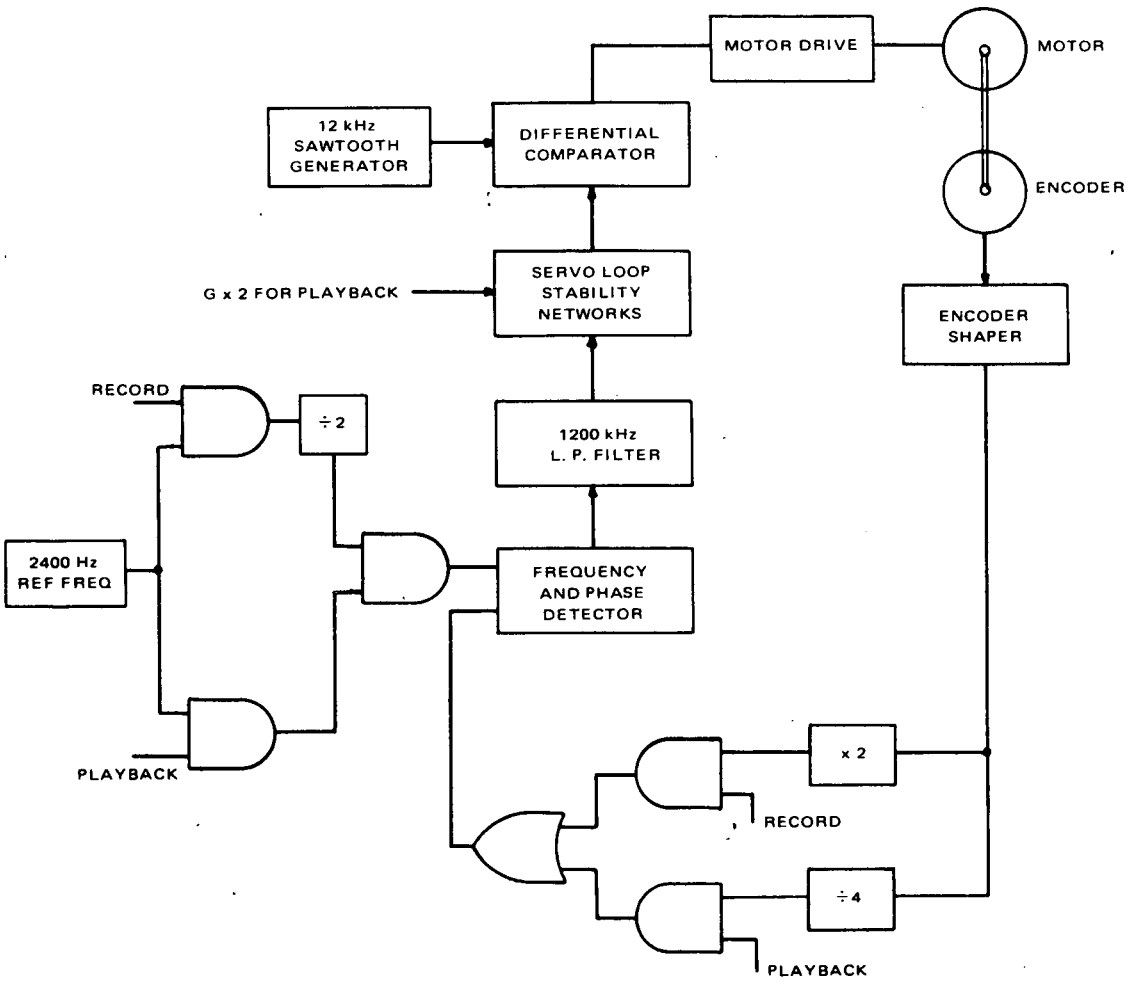


Figure 2-V-97. Simiplified Servo Drive, Block Diagram

per second. At that time, both of the input frequencies applied to the frequency and phase detectors are equal, but the encoder output pulses are lagging in phase and the incremental change of the lag is determined by the change of torque variation or by any other servo loop parameter change.

The encoder and phase detector has a gain of 1591 volts per radian, because the encoder output is multiplied by two and the pulse output amplitude is 5 volts. Therefore, the spatial error is 1/2000 of a revolution. The three-stage, 1200-Hz cutoff filter was designed and computer analyzed, yiedling the following essential parameters:

Frequency (Hz)	1	10	50	100	200	300
Phase lag (degrees)	0.26	2.6	13	27	50.3	74

There is no amplitude change up the frequencies of interest and the attenuation at 1200 Hz is 50 to 54 decibels.

The two operational amplifiers and the associated loop compensation networks provide phase lead to counteract the lags introduced by the mechanical time constant, the LC filter and electrical time constant. Also included in the servo loop are two lead-lag networks and a 600-Hz band stop filter. The networks were manually designed and then computer analyzed on a nodal program.

The total loop gain at 1 radian per second was calculated to equal 82.4 decibels. The 1-radian-per-second gain variations over the life and temperature limits was calculated to be ±25 percent or ±2 decibels.

The servo loop frequency-determining components were worst-case analyzed with regard to life and temperature and an equivalent circuit was prepared suitable for nodal analysis on a computer. The computer plot showed that the gain and phase margins were adequate for worst-case conditions. Therefore, the servo loop was considered stable in the record mode.

In the playback mode, the 1 radian-per-second loop gain margin is 20 decibels, 12 decibels below the record gain margin.

The required torque at the capstan in the record mode is made up as shown in Table 2-V-21.

TABLE 2-V-21. RECORD MODE REQUIRED TORQUE

Item	Max Torque at -10° C (inch-ounces)	Min Torque at +50° C (inch-ounces)
Negators	-1.1	+0.69
Motor Brushes	-1.1	-0.70
Heads and EOT Posts	-0.39	-0.19
Bearings	-1.6	-0.08
Total	4.19	0.28

Hence, the maximum required torque at the capstan is 4.19 inch-ounces, and the minimum retarding torque is 0.28 inch-ounce.

The minimum torque capability in the record mode with regard to the 12-kHz, 8-volt sawtooth signal was calculated to equal 7.1 inch-ounces. Consequently, the record torque margin is 2.91 ounce-inches, and the retarding or deceleration torque is 0.28 inch-ounce. Both of the margins were considered adequate.

The maximum required torque in the playback mode is made up as shown in Table 2-V-22.

TABLE 2-V-22. PLAYBACK MODE MAXIMUM REQUIRED TORQUE

Item	Maximum Required Torque (inch-ounces)
Motor Brush	1.10
Load Torque	2.17
Motor Losses	2.40
Encoder	0.20
Total	5.87

The minimum torque capability in the playback mode equaled 14.0 inch-ounces, which was considered an adequate margin.

The record mode maximum stopping time was determined to be 0.847 second, and the playback mode maximum (worst-case) stopping time was calculated to be 3.07 seconds.

The record and playback start times are considerably less, because the acceleration torque is higher than the deceleration torque.

The maximum tension applied to the tape during playback acceleration was calculated to equal 8.64 inch-ounces.

Because the capstan and tape interface coefficient of friction is not known, a simple test was performed to determine the tape slippage properties during playback acceleration.

Data was recorded on the tape at 2900 Hz per inch. The playback signal was then photographed from an oscilloscope which displayed the encoder output (320 pulses per inch) simultaneously, as a reference. Examination of many cycles of playback starts showed no slippage in the tape; the ratio of signal pulses per inch to encoder pulses per inch was approximately 9. Tests made at -10° C and at +25° C showed no essential differences.

(3) FUNCTIONAL DESCRIPTION

(a) General

The SR recorder is in a standby mode and remains so until activated by either the record signal from the spacecraft programmer or the playback signal from the command distribution unit (CDU). While in the standby mode, -24.5-volt power from the CDU is applied to the signal electronics and to the

-5.2-volt regulator supply which powers the command/control logic gate and level set circuits. The -24.5-volt motor drive power is obtained from the spacecraft power supply. Teh input 2400-Hz reference frequency signal from the time base unit (TBU), from which is derived a reference frequency for control of the motor speed during the record and playback modes, is also present during standby. Input power, command, and control signals, as well as the circuits which perform the logic for operation in the record and playback modes, are delineated on RCA 1976090 in the Logic Diagram Manual previously referenced. The functional descriptions of the record and playback operations refer to this logic diagram.

(b) Record Mode

The record signal electronics comprises the IR and visible FM modulators and record head drivers, flutter-and wow record head driver, the three record heads, logic gates, and the servo drive circuitry.

When a record command is applied, assuming the 2400-Hz reference signal and the -24.5-volt motor drive power are also applied, the following sequence takes place. Logic gate 4A output swings low to -5 volts and this output effects the turn-on of the record power switch (on board A7) which applies -24.5-volt power to (1) the record circuitry (the IR and visible FM modulators and video record amplifiers on board A1 and A3, respectively); (2) the flutter-and-wow record head driver (on board A2); and (3) the transport drive servo circuitry (the DC motor, optical encoder, encoder shaper, frequency and phase detector), thereby activating these circuits. The servo loop and record mode switches (on board A7) control the turn-on current from the -24.5-volt supply line for selecting the motor speed, the direction of motor rotation, and motor torque during starting and running.

The IR and visible radiometer input signals (0 to 8.16 volts) from the SR processor are applied to the respective modulators where they each frequency-modulate a subcarrier; the resultant frequency deviation from the FM modulators and divide by 2 circuit is from 3300 to 2400 Hz. The modulated signals are applied to their respective record amplifiers which produce a current change of 5 milliamperes. At the same time, the 3.125-kHz signal open circuit (0 to +4.4 volts) is applied to the futter-and-wow record amplifier which produces 5 milliamperes of current to the record head. A permanent magnet erase head provides a saturated erase condition at the tape immediately before the tape passes the record head. If a playback command is not received, recording continues until the end of the tape is reached. Then the recording mode stops, the SR recorder reverts to standby and awaits a playback signal.

The servo drive function embodies logic gate operation, phase and frequency detection, filtering, and digital control of the servo loop. The electromechanical loop components are a DC torque motor and an optical encoder connected to the tape drive capstan.

Logic gate 5B output enables gates 7D and 7A; the latter enables gate 8A, and the 2400-Hz square wave reference signal is divided by 2 by virtue of flip-flop Z10. This 1200-Hz signal now appears on gate elements 1A, 2A, and 3A of the frequency and phase detector (on board A6). The three flip-flops Z4, Z5, and Z6 are interconnected by gate elements 1A, B, C; 2A, B, C in a in such a manner that if the 1200-Hz reference frequency is greater than the encoder frequency, the Z5Q output is at -5 volts. The Z5Q output remains at -5 volts until the reference frequency is greater than or equal to the encoder frequency plus the count of 2 or more. This condition exists when the motor starts to accelerate. When the Z5Q output is -5 volts, and the input to the 1200-Hz low pass filters (on board A6) from the frequency and phase detector is high, resulting in no current being injected by the gain-set amplifier to the operational amplifier Z1 (on board A5). Hence, the output from the operational amplifier is -12-volts, and the differential comparator Q4 produces approximately 50-per-cent duty cycle 12-kHz pulses. The sawtooth generator (whose output swings between -8 and -16 volts) and differential comparator provide a pulse output at 12-kHz, whose duration is proportional to the DC level output of Z2.

The output from the differential comparator is applied to logic gate 4B and from here to the motor driver (on board A2) which drives current through the motor winding and turns the capstan. The encoder shaft is coupled to the capstan also and, hence, the 1000-line optical encoder starts to develop output pulses via the encoder shaper (on board A1) whose output is applied to logic gate 6B (on board A7). The output of gate 6B enables gate 6C and the pulses are then applied to the X2 multiplier (on board A5). When 601 encoder pulses per second are produced, then the digital phase detector Z5Q starts to produce output pulse width modulated pulses at 1200 Hz. The pulse train is then integrated by the 1200-Hz low pass filter, differentiated, and suitably shaped by Z1 and Z2, and passed to the differential comparator in such a phase as to produce negative feedback.

The tape continues to move until it reaches the metallic strip which shorts the "end-of-tape" (EOT) signal to ground and forces logic gate 4A output high. This, in turn, disables the record power switch, the servo power switch, and the record mode servo gates. The recorder is now in standby mode until -24.5 volts is applied (via P1, pin 25) which initiates playback.

(c) Playback Mode

The playback signal electronics consists of the three playback heads, three preamplifiers, three limiters and preamplifier power supply filters, logic gates, and the servo drive circuitry. The three playback heads and preamplifiers are identical and produce 4-volt (p-p) output signals which are fed to three identical 20-decibels gain limiters (on boards A1, A2 and A3). The limiter outputs have a 2-volt (p-p) signal and a 50-ohm output impedance.

The SR recorder is in standby mode until a playback command is received from the CDU via the ground station. Power is then removed from the record circuits and the -24.5-volt DC power is applied to (1) the IR and flutter-and-wow limiters and (2) the IR and flutter-and-wow preamplifiers.

Logic gate 1C is off, which, in turn, enables the servo loop switch (on board A7) and the two operational amplifier switches Z1 and Z2 (on board A5). One of the switches (Z1) multiplies the 1-radian-per-second loop gain by 2 (via pin 13 on board A6) and the other switch (Z2) shifts the bias voltage from -12 to -17 volts. At the same time, the playback enable gate 7C is operated which allows the 2400-Hz reference frequency to be applied to the frequency and phase detector. The DC torque motor is powered in reverse direction because the relay driver (on board A2) is enabled and the encoder generates output pulses, in a similar manner to the record mode, until the number of pulses reaches 9600 per second. At this time the frequency and phase detector receives 2400 pulses per second via the divide by 4 circuit (Z9 and Z11). This is compared to the 2400-Hz reference frequency and the result and loop control is similar to the record mode.

The condition continues until the end-of-tape metallic strip shorts the EOT signal to ground, which effects the turn-off of the relay driver, servo loop power, playback preamplifiers and limiters, gain and bias switches, and disables the playback servo loop. The motor decelerates and the SR recorder returns to the standby mode. (When the next record signal is applied, the previously described record mode conditions apply, except for the 5-second disable delay, which operates every time the recorder is switched from playback to record mode. Consequently, the current applied to the motor is delay by 5 seconds.)

(d) Erase Head

A permanent magnet erase head, effective for all tracks, is mounted adjacent to the record head so that the recorded signal is erased immediately after playback, and immediately before recording, thus ensuring a "clean" tape and optimum signal-to-noise ratios. This head is not in contact with the tape and therefore does not cause tape degradation.

(e) Tape Transport

Each tape transport consists of a machined base on which are two coaxial tape reels, mounted one above the other, a tape-driver motor, a capstan, two magnetic tape heads, a permanent magnet erase head, three tape idlers and a negator spring assembly (see Figures 2-V-98, 2-V-99, 2-V-100).

Figure 2-V-98. SR Tape Transport Top View, Dome Removed

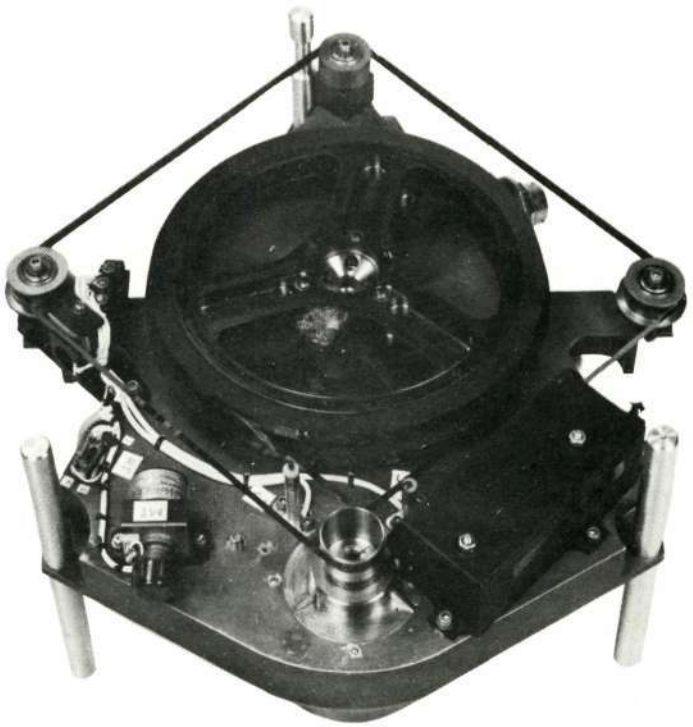


Figure 2-V-99. SR Tape Transport Removed from Enclosure, Top View

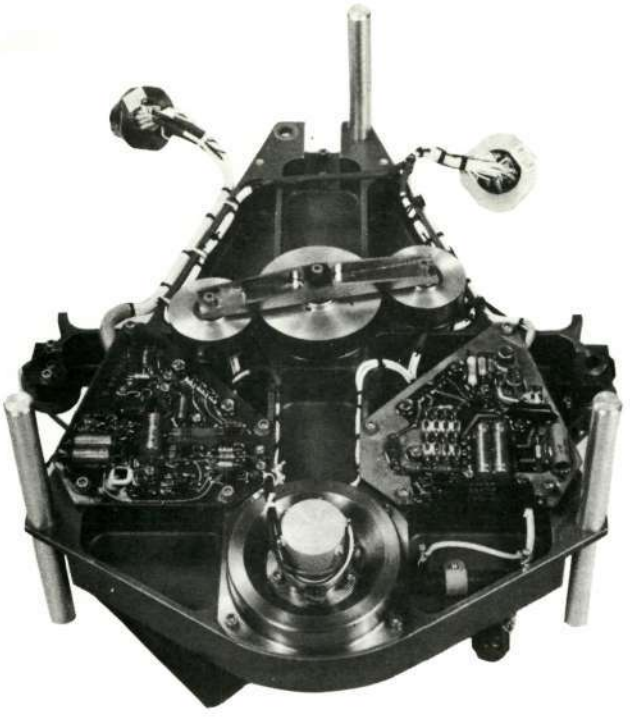


Figure 2-V-100. SR Tape Transport Removed from Enclosure, Bottom View

The two tape reels are torqued against each other by the negator spring assembly to provide constant tape tension. In the record mode, the capstan driven tape is wound from the top reel, around the idlers to change its level, past the magnetic head assembly, and onto the lower reel. In the playback mode, the direction is reversed, and the tape is rewound from the lower to the upper reel. All signals are played back in a direction opposite to recording. The permanent magnet erase head is mounted so that the signal is erased after playback and before record. The erase function occurs without adding time to either the record or playback function.

The idlers that change the tape level require no angular adjustments. When mounted in the transport base assembly, they are automatically set at the correct angle. Two of the idlers are crowned and stability of tape motion is aided by the self-centering effect of the crowned idlers on the tape.

Head tracking is not affected by the slight twist required to move the tape from the plane of one reel to the plane of the other reel via the tape idlers, even for significant differences in the effective diameters of the two reels. (The effective diameter of a reel is the nominal diameter plus an amount equal to twice the thickness of the tape wound on the reel.)

The record head and the playback head are similar three-channel heads. Recording or playing back occurs on all three tape tracks simultaneously.

The tape is 1/4-inch Mylar-base tape, 1360 feet long, with an oxide coating on one side to provide the magnetic medium. The tape is wound on the tap transport in such a fashion that the oxide-coated side of the tape does not contact the tape idlers or the capstan.

The motive power for the tape transport is a DC torque motor that is rated at 35-ounce-inch peak torque. The rotor is mounted directly to the capstan. Minute speed variations are sensed by a capstan driven optical encoder and correction signals are fed back so as to provide constant drive. The coupling between the motor and the capstan provides a tape speed of 1.875 inches per second for record and 30 inches per second for playback. The maximum record time is 145 minutes, and the maximum playback time is 9.1 minutes. The motor receives the excitation signals from the motor drive circuits. Starting and running torque of the motor, and the direction of rotation are controlled by the logic circuits and the motor drive circuits.

End-of-tape sensing is performed during each cycle of the SR recorder and is activated at a specific position on the tape. There is a contact type end-of-tape switch for each reel. The switches are operated when contacted by strips of conductive tape attached to the magnetic tape near both ends of the tape. As a backup, there are also microswitches located so as to be activated by either full reel of tape should the contact type switch not be activated by the conductive tape. A fail-safe tape mounting clamp is also used, the recording tape is physically clamped to the reel. The clamp, in conjunction with a buffer spring to take up the shock, would prevent the tape from leaving the reel, even if run out entirely to the end of the tape.

1. Motor Design Life

The design life of the motor is 12 months, continuous operation, under orbital environmental conditions. The motor drives the capstan directly. The results of an accelerated life test, performed on another program using a similar motor, indicated that the life of the motor is approximately 2 years, continuous operation.

2. Negator Springs Design Life

The negator springs are procured to the same requirements as those for the AVCS transport. Negator spring cycling is approximately 14 cycles per day. This rate of cycling provides a minimum design life of approximately 3 years.

3. Magnetic Tape.

A test program was performed on magnetic tapes to select the tape which provided the best characteristics for the thermal environment. The tape selected for the best thermal characteristics was then subjected to a life test. Test results are included as Appendix D of this report.

4. Bearing Lubrication

The bearing lubrication used on the SR recorder is the same as that used for the AVCS tape transport assembly.

(f) Telemetry Circuits

1. SR Recorder Operational Status

The telemetry combiner (on board A7) provides an output digital signal variable at five levels to indicate the recorder operational status. The telemetry voltage for each operational status (or mode) is given in Table 2-V-23.

TABLE 2-V-23. SRR OPERATIONAL STATUS TELEMETRY

Status	Telemetry DC Voltage
Off	0
Standby	-0.9
Record	-1.8
Playback	-2.7
Record and Playback	-3.6

2. Motor Current Telemetry

The motor current telemetry circuit, located on board A2 of the transport assembly, provides an output signal variable between -0.5 to -4.5 volts DC. This telemetry signal is derived from the motor driver circuit (on board A2).

3. Temperature and Pressure Telemetry Circuits

One temperature sensor (R_T) and one pressure sensor (M_T) are located inside the recorder transport enclosure to provide telemetering of the immediate environment of the tape transport. The temperature sensor is a thermistor with a negative temperature coefficient. This sensor provides a temperature telemetry signal (-0.5 to -4.5 volts DC) for the hottest point in the tape recorder. The pressure sensor is a transducer located on the transducer assembly board. This transducer provides a negative DC voltage output (-0.5 to -4.5 volts DC) which is proportional in absolute value to the pressure inside the tape recorder enclosure. The pressure transducer is a variable potentiometer in which the wiper arm is mechanically connected to a pressure-sensitive bellows.