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TDRS MULTIMODE TRANSPONDER PROGRAM

PHASE I - DESIGN

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2829 Maricopa Street
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15 July 1972

Final Report for Period March - July 1972

Prepared for

GODDARD SPACE FLIGHT CENTER

Greenbelt, Maryland 20771

227

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
4. Title and Subtitle TDRS MULTIMODE TRANSPONDER PROGRAM PHASE I – DESIGN		**5. Report Date** 15 July 1972
		6. Performing Organization Code
7. Author(s) Richard S. Cnossen		**8. Performing Organization Report No.** R-4403
9. Performing Organization Name and Address The Magnavox Company Magnavox Research Laboratories 2829 Maricopa Street Torrance, California 90503		**10. Work Unit No.**
		11. Contract or Grant No. NASS-20330
12. Sponsoring Agency Name and Address National Aeronautics And Space Administration Goddard Space Flight Center Greenbelt, Maryland 20771		**13. Type of Report and Period Covered** Type III (draft) 1 March to 15 July 1972
		14. Sponsoring Agency Code
15. Supplementary Notes		

16. Abstract

In recent years NASA has considered the use of geosynchronous tracking and data relay satellites (TDRS) which can serve both low data rate users at VHF and high data rate users at other frequencies. The effects of radio frequency interference (RFI) from the earth and of multipath propagation due to reflections from the earth are expected to pose problems for the TDRS system at VHF. Investigations have suggested several modulation techniques that offer promise to overcome these problems. This report provides NASA with a complete design of a VHF/UHF multimode transponder and its associated ground support equipment. The transponder is designed for installation aboard an aircraft and will demonstrate candidate modulation techniques to provide the required information for the design of an eventual VHF/UHF transponder suitable for installation in a user satellite, capable of operating as part of a Tracking and Data Relay Satellite (TDRS) system.

17. Key Words (Selected by Author(s)) RFI, Multipath, Modulation Evaluation		18. Distribution Statement		
19. Security Classif. (of this report) Unclassified		**20. Security Classif. (of this page)** Unclassified	**21. No. of Pages** 235	**22. Price***

PREFACE

For several years NASA has considered the use of geosynchronous tracking and data relay satellites (TDRS) which can serve both low data rate users at VHF and high data rate users at other frequencies. A TDRS antenna pattern covers the earth and the surrounding regions with 3 dB points about 5000 km above the surface of the earth. The effects of radio frequency interference (RFI) from the earth and of multipath propagation due to reflections from the earth are expected to pose severe problems for the TDRS system at VHF.

The objective of this program is to provide NASA with (1) a design and (2) an engineering model of a VHF/UHF Multimode Transponder (MMT) and its associated ground support equipment. The transponder is to be capable of being installed aboard an aircraft which will demonstrate the modulation techniques specified herein. The Multimode Transponder will provide the required information for the design of a VHF/UHF transponder suitable for installation on a low altitude earth orbiting satellite, capable of operating as part of a TDRS system consisting of one or more geosynchronous satellites together with the associated ground equipment.

On 1 March 1972, the Magnavox Research Laboratories was awarded the contract to design (Phase I) and fabricate (Phase II) a VHF/UHF Multimode Transponder which would meet the stated objectives. To complement the experience of MRL in the area of satellite communications and PN technique, the Advanced Systems Analysis Office (ASAO) of Magnavox and Hekimian Laboratories, Incorporated (HLI) were engaged as team members to provide expertise in the areas of TDRS system tradeoff studies and for the design of the Adaptive Burst Communications Mode, respectively.

This report contains the results of the Phase I effort. Along with the necessary system and trade-off studies, it contains a complete design of the MMT and the associated ground support and test equipment. The contractor has identified all the forseeable technical problems in the design of the equipment and provided solutions for these problems. Particular emphasis has been given to the compatibility of the transponder with the supporting relay satellite.

Upon approval from NASA, Phase II will be initiated and the system described in this volume will be fabricated. The Multimode Transponder will receive, decode as required, and deliver to a simulated spacecraft command signals transmitted from a Multimode Transmitter and Receiver (MTAR) at a ground station. It will receive from a simulated satellite, process as necessary, and transmit telemetry data to the MTAR. Finally, the MMT will receive from, process as necessary, and retransmit to the ground station, coded signals suitable for a range and range rate determination.

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INTRODUCTION

1.1   <u>BACKGROUND SUMMARY</u>

The TDRS system concept was developed by NASA to provide a virtual real time data acquisition and tracking capability. This capability is to be used by low, medium, and high-data-rate users consisting of manned and unmanned scientific satellites. The TDRS system, will provide the data acquisition and tracking capability for those manned and unmanned missions whose orbits are less than 5,000 kilometers.

Currently, unmanned scientific satellites are supported by MSFN (STDAN systems unified with MSFN) network consisting of ground stations strategically located on the globe. These stations are connected to communications centers, such as the Goddard Space Flight Center, through NASCOM facilities, Manned missions, on the other hand, are supported by the Manned Space Flight Network (MSFN). This network is also a multiplicity of worldwide ground stations connected to mission control and the Goddard Space Flight Center through the NASCOM facilities. A third network, the Deep Space Network (DSN), also services NASA. The DSN is operated by JPL, services deep space exploration missions, and can be used as backup for manned missions.

The TDRS system concept was a result of the phase A study and a product of the joint effort between NASA, Goddard, and JPL. The phase A study dealt primarily with spacecraft design, orbital station keeping, payload, etc., with some attention to a VHF communications link with the low-data-rate users of the TDRS system. An important outcome of the phase A study was the recommendation that pseudonoise modulation be used to provide multipath resistance, data transfer, and tracking for up to 40 low-data-rate scientific satellites.

The phase A study was not a detailed VHF communications link study because a variety of candidate systems were not examined. Following the Phase A

effort, NASA-Goddard contracted several detailed VHF link communications studies. Among these were: 1) the multipath modulation study conducted by Magnavox under contract NAS5-10744, 2) the multipath modulation study conducted by Hekimian Laboratories under contract NAS5-10749, and 3) the VHF communication study for low-data-rate users conducted by Hughes Aircraft under contract NAS5-11602. As a results, two prime candidata systems were evolved. Pseudonoise modulation was recommended by Magnavox and Hughes while adaptive burst communications (ABC) was recommended by Hekimian. Hughes considered a narrowband forward link with a wideband return link, while Magnavox considered a narrowband PN forward link and options of either wideband or narrowband PN return links.

NASA issued to industry an RFP, dated May 1971, for a configuration and trade-off study of the TDRS system. Subsequentially, two contractors, North American Rockwell and Hughes Aircraft, were awarded system trade-off studies. Shortlay afterward NASA issued to industry another RFP, number 46400-303, for a multimode transponder for use on board a low-data-rate, unmanned, scientific satellite. Shortly afterward this RFP was amended to permit the design of a multimode transponder for installation and use on board an aircraft simulating a user spacecraft as part of a TDRS system. On March 1, 1972, a contract for the design and development of a multimode transponder was awarded to the Magnavox Research Laboratories.

1.2   CURRENT TDRS SYSTEM CONCEPTS

The purpose of these paragraphs is to summarize the specification detailed in that RFP and to discuss the impact of these specifications on the low-data-rate user satellite transponder. Figure 1-1 illustrates the forward and return links and the links between the TDRS satellites and the ground station. One TDRS satellite is located at 14 degrees west, the other at 144 degrees west resulting in a total separation of 130 degrees. The two TDRS satellites are active repeaters (amplifiers). A third satellite will be on a parking orbit for backup purposes. The forward link is defined as the link from the ground station to TDRS to low-data-rate user: the return link is from user to TDRS to ground station. Forward user-TDRS links are on VHF or UHF frequencies and return user-TDRS links are on VHF frequencies. TDRS-ground station links are in the Ku band.

VHF/UHF

VHF/UHF

KU

KU

USER SPACECRAFT

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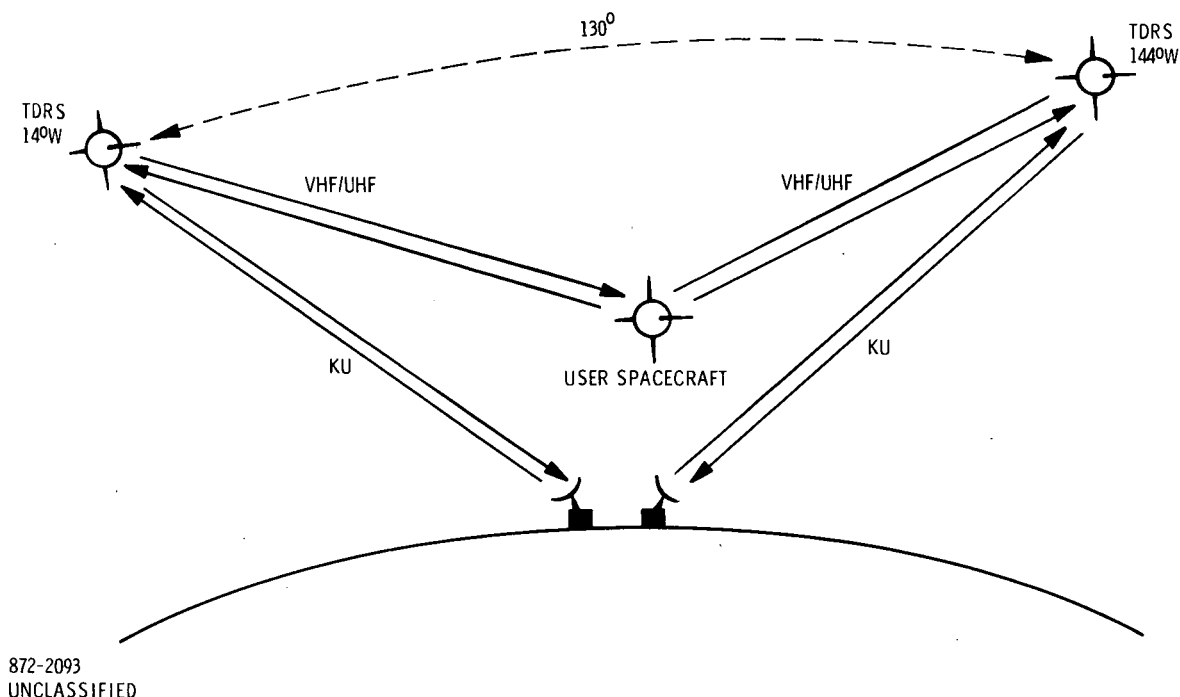
Figure 1-1. Simplified TDRS-User Geometry

The band allocated for the user-to-TDRS link is between 136 and 144 MHz with the 136 to 138 MHz band being the most probable return link. The forward link will be between 148 and 149.9 MHz or 126 and 130 MHz. Several studies have indicated that the RFI in the 148 to 149.9 MHz band is too severe, making it virtually unusable. Thus, the 126 to 120 MHz band is expected to be used for the forward link. The ground station to TDRS link will be in the Ku band at 14.4 to 15.35 MHz. The TDRS-to-ground station link will be in the Ku band at 13.4 to 14.2 MHz.

Unmanned scientific satellites are required to dump accumulated data upon command as they pass over designated ground stations. Scientific data is accumulated on board by means of tape records and is transmitted to the appropriate ground station at greater than real-time speed. The TDRS system will circumvent the need for on-board recorders by providing essentially real-time data transfer and tracking commands for the low-data-rate users. During a single orbit, low-data-rate users can accumulate 5 to 6 megabits of data.

This data accumulation is based on a 100-minute orbit and a typical low-data-rate user. This means that a low-data-rate user, during a six-minute pass, would transmit recorded data to the ground station network at a rate of 15 to 20 kilobits per second. With the use of the TDRS system capacility, this rate equated to a continuous rate of about 1 kilobit per second.

The corresponding rate requirement for the torward link is to accommodate a command data rate of 100 to 1,000 bits per second.

In addition to providing forward and return link data transfer, the TDRS system must provide real-time tracking of range and range-rate measurements of the low data rate users. This can be accomplished through the use of one or two TDRS systems. Simultaneous tracking of a user with both TDRS systems is accomplished when the user is in the field of view of both TDRS systems.

Regardless of tracking techniques used, the range and doppler tracking uncertainty requirements below have been applied in the TDRS configuration and trade off study.

● Systematic Range Errors - less than 10 meters

● Random Range Errors - less than 15 meters

● Doppler Uncertainties - systematic 10 centimeters per second

● Random Range Rate Errors - 10 centimeters per second for a doppler observation interval of one second or one centimeter per second for a doppler observation of 10 seconds

The TDRS relay for the forward link will be configured as a hard-limiting repeater. This design will maximize the available forward link EIRP. The TDRS will be capable of transmitting a minimum of two simultaneous coded forward link signals for commanding user satellites. These two signals will provide command data, range and range rate data, and emergency voice. Each channel will have minimum EIRP of 30 dBw. This power level will be obtained over a circular field of view of not less than 26 degrees centered about the local nadir. This requirement

means that each TDRS system will be capable of transmitting two simultaneous channels of information. A user in the field of view of both TDRS systems should be capable of receiving and monitoring four channels, two from each TDRS system.

In the return link, 20 simultaneous accesses must be accommodated by each TDRS system. Although it is anticipated that more than 20 different low-data-rate satellites will be in orbit at any time, 20 low-data-rate accesses are anticipated for each TDRS system. The user-to-TDRS link will have an effective G/T (antenna gain-to-system thermal noise temperature ratio) of not less than -14dB per degree K. This corresponds to an approximate TDRS antenna gain of 14 dB at ± 13 degrees covage angle and an equivalent system noise temperature of about 500 degrees K. For both forward and return links, the design goal is to provide the user and the ground station with a binary-data-train-bit-error probability of not greater than 10^{-6}. In table 2-1, we summarize forward and return link requirements for the low-data-rate users of the TDRS system in terms of command rates, return-link data rates, bit-error probability, and desired range and range-rate tracking accuracy.

1.3   TDRS PROBLEM AREAS

Although the TDRS system concept is straight forward, the problem areas below confront system implementation:

- Multipath
- RFI
- User antenna pattern anomalies
- Multiple access of 20 users to a common repeater
- Power output limitations inherent in the low-data-rate, unmanned, scientific satellites

Multipath exists between the user and TDRS because it is anticipated that the unmanned users will not have a stabilized antenna system capability but will be esentially omni-directional. Furthermore, satellite tumbling will create a time varying multipath situation. Multipath will exist in links from TDRS to user and from user to TDRS.

In addition to additive noise at both the user and TDRS, RFI generated on the earth will serve to reduce system performance. The RFI can exist in both the forward and return links.

In fact, recent studies indicate that RFI is a major threat. Data collected from ECAC and ITU published files indicate RFI levels of - 123 dBM/Hz at 127 MHz, - 135 dBM/Hz at 137 MHz and - 130 dBM/Hz at 149 MHz. This data however does not consider duty factors and scaling for satellite attitudes.

1.4 MULTIMODE TRANSPONDER REQUIREMENTS

The multimode transponder described in this report is intended for installation and use on board an aircraft simulating a user spacecraft as part of a TDRS system. The overall TDRS system shall be assumed to consist of one ground station, two relay satellites approximately 130 degrees apart (both in view of the ground station), and up to 20 user spacecraft in low-altitude (5000 km or less), earth orbits. All user spacecraft may utilize the return link simultaneously transmitting telemetry data in a single-shares, VHF band at 137 MHz. A relay satellite will transmit commands and/or ranging signals over the forward link to only one user spacecraft at a time in an assigned VHF or UHF band. Both the forward and the return links will employ polarization diversity reception.

The communication system of the relay satellite may be assumed to be of the type planned for ATS-F, GSFC Mark 1, and TDRS. The forward link from the ground to the user spacecraft will employ hard limiting in the relay satellite in order to maximize the radiated power. The return link from the user spacecraft to the ground will utilize two highly linear repeater channels in the relay satellite, one for each of the two polarization diversity signals. All frequency conversions in the relay satellite may be assumed to be phase coherent with respect to a reference signal standard located on the ground.

The Multimode Transponder (MMT) along with the associated ground support equipment (MTAR) will demonstrate the following modulation techniques:

- Conventional PSK Command and telemetry mode and tracking with GRARR equipment

- Narrowband pseudo random noise (PN) mode

- Wideband PN mode

- Adaptive burst communication (ABC) mode

The following functions can be simulated with various combinations of the transponder subunits and associated ground equipment:

- Reception, demodulation, and delivery to the user spacecraft of command signals received by the transponder via the forward link

- Acceptance, modulation, and transmission via the return link of the telemetry data generated by the spacecraft user

- Reception via forward link, processing on board, and retransmission via return link of coded signals suitable for ranging and range-rate determination

SECTION II
SYSTEM DESIGN

This section describes the operation of the multimode transponder (MMT), summarizes the modes of operation and provides a rational for the design parameters. It includes the system design and tradeoff studies which were used to define the system performance specifications. TDRS system problems such as RFI, multipath and signal/noise power budgets are discussed in this section along with a summary of the Multimode Transponder characteristics which can be used to evaluate these problem areas.

2.1   EQUIPMENT CONFIGURATION

The MMT and MTAR equipments are designed to operate in an equipment configuration as shown in figure 2-1. In this configuration, the multimode transponder in the aircraft simulates a user satellite transponder. The multimode transmitter and Receiver in the mobile test station simulates the TDRS satellite. For purposes of this experiment, the Ku band link between the eventual TDRS satellite and the ground station is eliminated since the Ku band link is reasonably well defined with good signal to noise characteristics.

The engineering model of the transponder equipment has been designed to meet all of the electrical performance requirements of a space flight model less packaging, reliability and space qualifications. With the equipment configuration shown in figure 2-1, many experiments can be conducted to simulate the actual TDRS environment and evaluate various modulation techniques.

2.2   MODES OF OPERATION

As the name implies, the multimode transponder has many modes of operation. The many equipment characteristics designed into the equipment are summarized in this section.

As shown in figure 2-2, the MMT transmitter will operate at 137.0 MHz only and the MTAR will transmit at 127.750, 149 or 401 MHz. The multimode transponder has been designed to operate in the modulation modes shown in
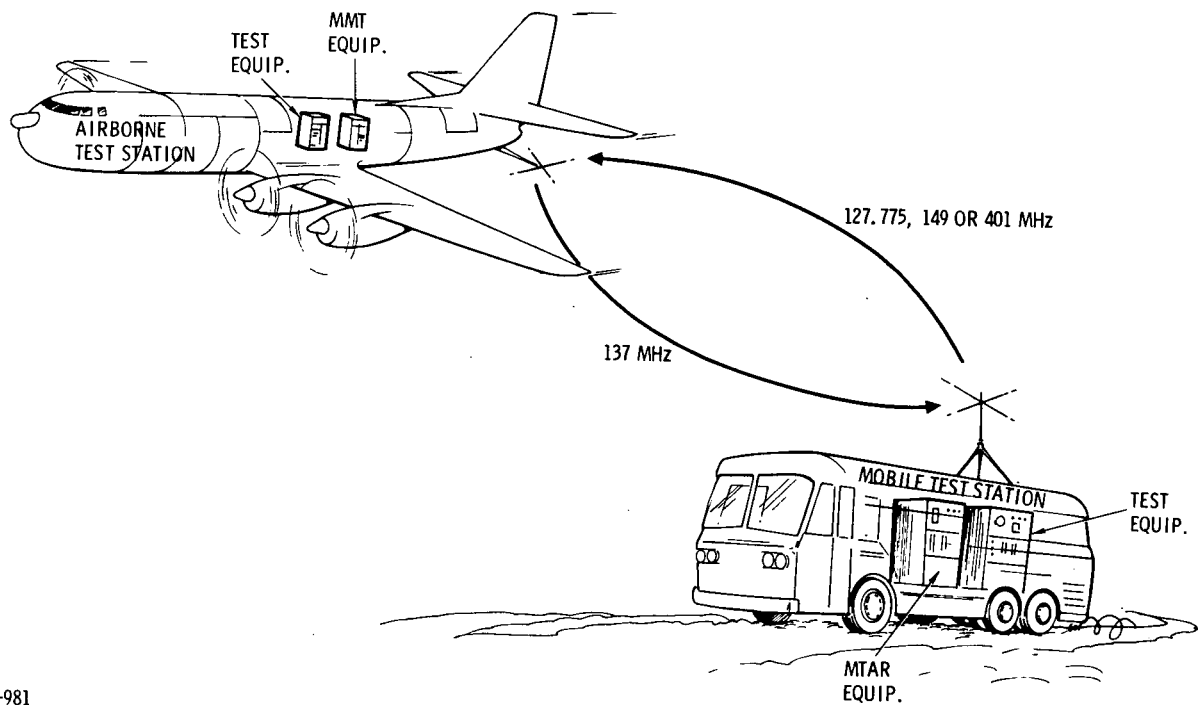
Figure 2-1. Multimode Transponder Test Configuration

| RECEIVER | TRANSMITTER | MMT (AIRBORNE UNIT) |

QUADRIPLEXER
ANTENNA

FORWARD LINK
FREQUENCIES

127. 750 MHz
149. 0   MHz
401. 0   MHz

RETURN LINK
FREQUENCY

137. 0 MHz

ANTENNA
QUADRIPLEXER

| TRANSMITTER | RECEIVER | MTAR (GROUND UNIT) |
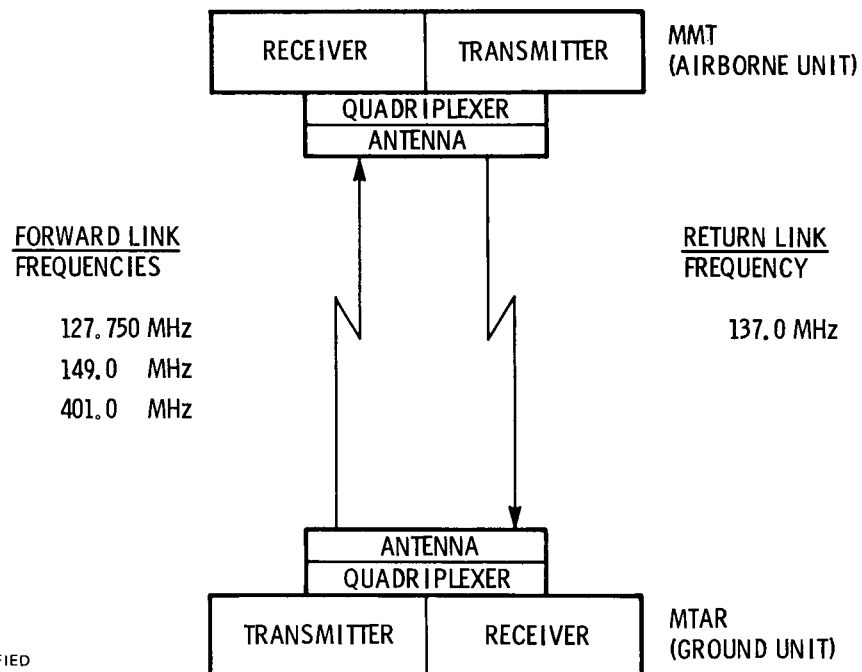
Figure 2-2. Frequency Plan

2-2

figure 2-3. Data rates selected on the basis of prior TDRSS studies are summarized in figure 2-4. Techniques for range and range rate measurement are outlined in figure 2-5. A chart of the MMT/MTAR RF frequencies and their associated bandwidths along with the selectable PN chip rates are shown in figure 2-6.

2.3   BASIC FUNCTIONAL DESCRITION

The roles and functional interactions of various subunits of the transponder during equipment operation in each of the above modes are described in the following paragraphs. The explanation of transponder circuit design details follows the functional description.

The multimode transponder unit consists of two parallel receivers and a transmit channel as shown in the overall block diagram in figure 2-7.

The inputs for the two receivers are provided by orthogonally polarized antenna elements. The outputs of the two receivers are, after coherent detection, summed to provide a diversity combined output data signal. The receiver will operate in any one of three frequency bands; 127.750, 149 or 401 MHz.

In a similar manner, the transmitter is connected via quadriplexers to the polarization diversity antennas. However, in contrast to the receivers, which are always connected to their respective antennas, RF input to the transmitter is selected from the synthesizer of the receiver which is receiving with the highest signal-to-noise ratio. This procedure optimizes the coherent transponding signal radiation strategy. The transmitter will operate in one frequency band at 137 MHz.

The multimode transmitter and receiver (MTAR) consists of two parallel receivers and a single transmit channel which is shown in figure 2-8. The MTAR is very similar to the MMT; however, unlike the MMT which functions as a coherent transponder, the MTAR has a transmitter which functions independently from its two tracking receivers used for diversity. Another difference between the two equipments involves the external equipment interface.

2.3.1   CONVENTIONAL PSK MODE

In the conventional mode, the received command and the transmitted telemetry data is modulated, respectively, on the incoming and outgoing carriers as a differential phase shift keying (DPSK) with a phase shift of 90 degrees. This implies additional demodulators, such as bandwidth spreading by PN or data burst reception and transmission as with ABC will not be used in this mode. Essentially, this

RECEIVER TRANSMITTER MMT

QUADRIPLEXER
ANTENNA

FORWARD LINK

- QPSK
- PSEUDONOISE
    34.133 K CHIP/S
    102.4   K CHIP/S
- ABC
    2 MS BURST
    4 MS BURST
    6 MS BURST
    8 MS BURST
    10 MS BURST

RETURN LINK

- QPSK
- PSEUDONOISE
    34.133 K CHIP/S
    102.4   K CHIP/S
    1024.0   K CHIP/S
- ABC
    2 MS BURST
    4 MS BURST
    6 MS BURST
    8 MS BURST
    10 MS BURST

ANTENNA
QUADRIPLEXER

TRANSMITTER RECEIVER MTAR

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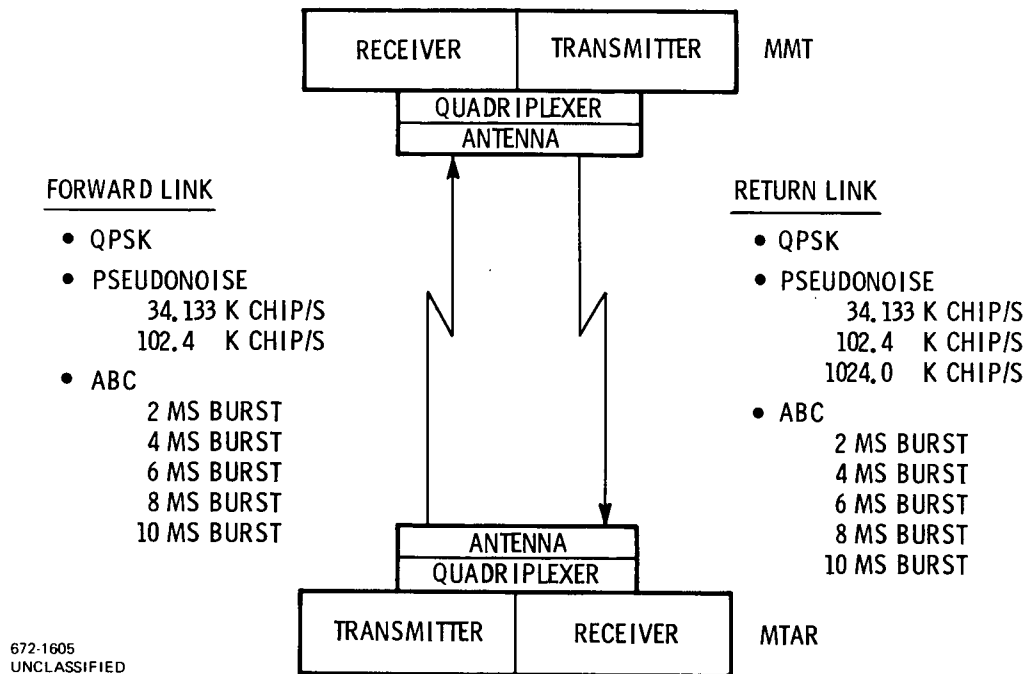
Figure 2-3. Modulation Modes

RECEIVER TRANSMITTER MMT

QUADRIPLEXER
ANTENNA

FORWARD LINK

(COMMAND)

100 BPS
300 BPS
1000 BPS
VOICE (PDM 10 KHz)

RETURN LINK

(TELEMETRY)

300 BPS ⎫
1000 BPS ⎬ X2
3000 BPS ⎬ WITH
          ⎬ ENCODING
10K BPS ⎭

VOICE (PDM 10 KHz)

ANTENNA
QUADRIPLEXER

TRANSMITTER RECEIVER MTAR

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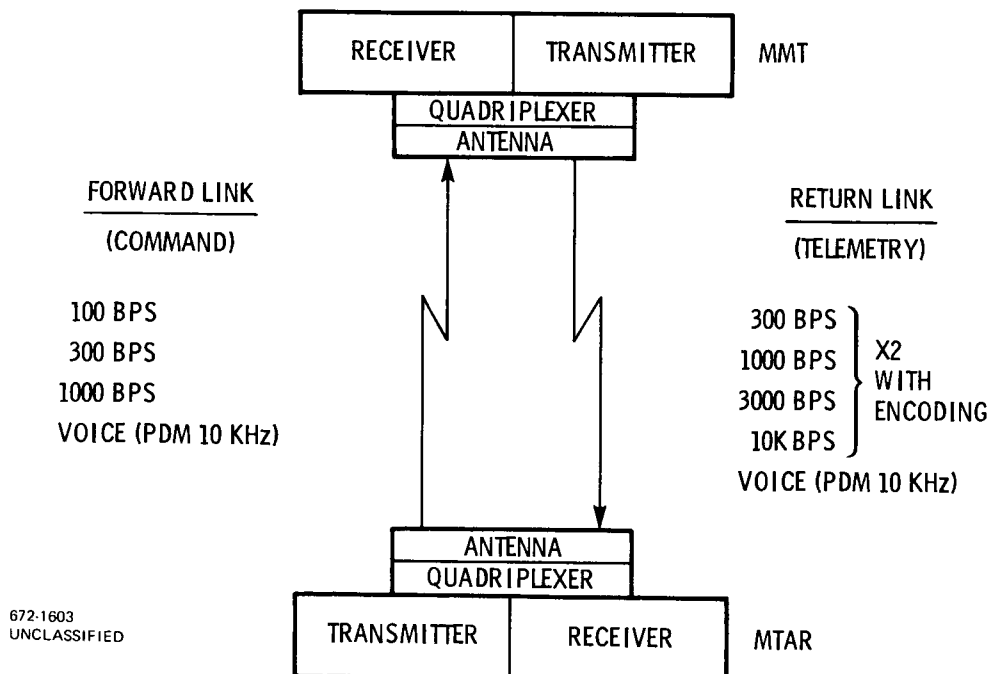
Figure 2-4. Data Rates

2-4

- PSEUDONOISE MODE

  RANGE - TX/RX PN CODE OFFSET
  RANGE RATE - TX/RX CARRIER OFFSET

- PSK (CONVENTIONAL) MODE
  GODDARD RANGE AND RANGE RATE SYSTEM (GRARR)

- ABC MODE

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  UNCLASSIFIED
  GODDARD RANGE & RANGE RATE SYSTEM (GRARR)

Figure 2-5. Techniques for Range and Range Rate Measurement

RECEIVE FREQUENCY	BANDWIDTH	PN CHIP RATES
MMT		
127.750 MHz	50 KHz	34.133 K CHIPS/5
149	50/150	34.133/102.4
401	50/150	34.133/102.4
MTAR		
137	50/150/1500	34.133/102.4/1024

672-1614
UNCLASSIFIED

Figure 2-6. RF Frequency/Bandwidth/PN Code Rate

conventional mode is the basic, most fundamental mode of operation against which the performance improvements in all the other modes will be compared.

Briefly, the two signals, each derived from the separate diversity antenna, are coupled through the respective diplexers to the two separate receivers. In these receivers, the command signals are amplified and the ±90 degree command modulation recovered coherently by means of Costas-loop demodulation. Because the demodulators independently track the phase of each of the received carriers, the data recovery process is optimized in each demodulator regardless of relative phase and frequency shifts between the two received carriers.

Separate voltage controlled oscillators (VCO), inside each receiver unit, track their respective carriers and provide the reference signals to their individual frequency synthesizers. These synthesizers provide both the local oscillator signals to their respective receivers and the selected transmitter carrier to the transmitter modulator and drive circuitry.

BASEBAND IN

MODULATOR

RF CARRIER
FREQ

FROM
FREQUENCY
SYNTHESIZER

RF
POWER
DIVIDER

QUADRIPLEXER

ANTENNA

ANTENNA

QUADRIPLEXER

RECEIVER 1

L.O.

TO MODULATOR

FREQ.
SYNTH

VCO

DIVERSITY
COMBINER

BASEBAND OUT

L.O.

RECEIVER 2

GRARR
DIGITAL
SIMULATOR
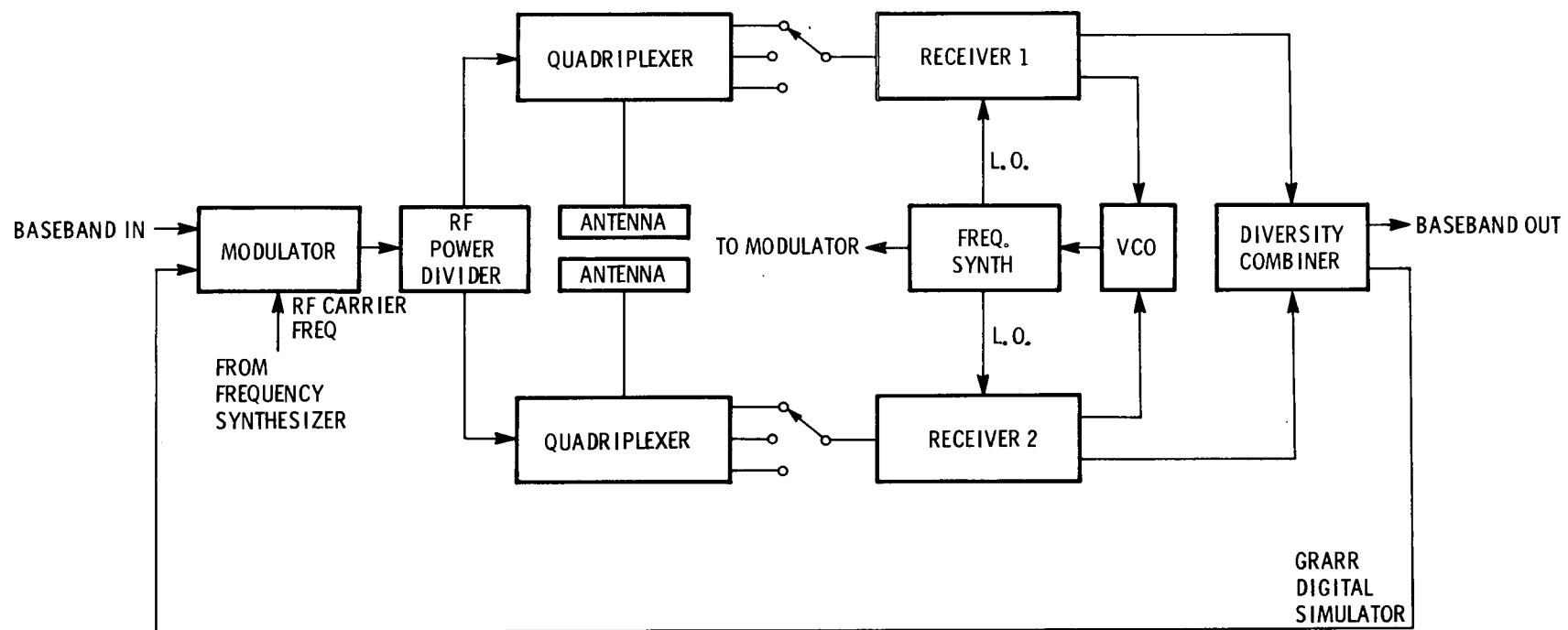
672-1615
UNCLASSIFIED

Figure 2-7. MMT Block Diagram

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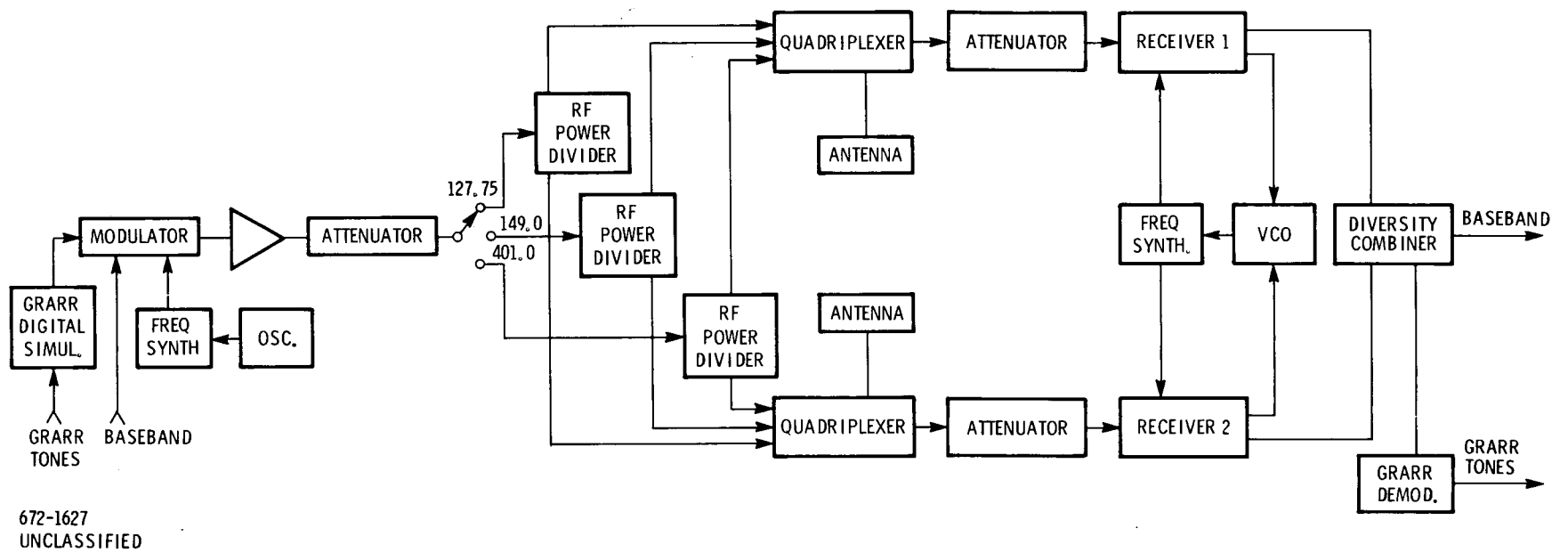
Figure 2-8. MTAR Block Diagram

Because of the coherent tracking of the incoming carriers, each receiver portion of the transponder is simply a superheterodyne phase-locked loop tracking the received carrier (f_r) for coherent data demodulation. In phase lock,

$$f_r = N_1 f_o + f_o = (N_1 + 1) f_o$$

where f_o is the IF frequency and N_1 is the multiplication factor in the receive synthesizers. The transmit carrier frequency f_t is obtained in the synthesizers by multiplying f_o by N_2, $f_t = N_2 f_o$, so that

$$\frac{f_r}{f_t} = \frac{N_1 + 1}{N_2}$$

which is the necessary conditions for a coherent transponder. The constant N_2 is selected to yield an f_t of 137 MHz. Similarly, constant N_1 is selected to yield a local oscillator frequency required for the reception of one of the three selectable receive channels. The command data which appears at the outputs of the two respective in-phase demodulators, i.e., I-channel data No. 1 and No. 2, is applied to the I channel combiner where the two data streams are collected into one using an optimum diversity combining technique. The rates at which the data appears at the output of the I channels, is, in the conventional mode, 100, 300 and 1000 bps, depending on the rate selected by a command from the ground station.

For transmission of telemetry data from SC to ground station (return link), the transmitter modulators will accept the binary telemetry data from SC and will superimpose this data on one of two carriers selected according to the optimum diversity strategy. In the conventional telemetry transmit mode the modulation riding on the transmitter carriers is DPSK with phase modulation index of ±90 degrees. The data rates are discrete 300, 1000, 3000 or 10,000 bps.

In the conventional mode of operation, the GRARR tone package, at the ground station biphase modulates a suppressed quadriture carrier component and at the same time command data biphase modulates the in-phase carrier component.

For reception, the multimode transponder contains a carrier tracking phase locked loop and the digitized GRARR tone package is extracted from the Q-channel at baseband while the command data is extracted from the I-channel. Subsequently, the GRARR data stream and command data quadriphase modulate a coherent transmit carrier at 137 MHz. In essence, the modulator in this case

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performs the inverse function of the Costas loop demodulator. Note that diversity reception is used with GRARR signals in a manner similar to that of all other modes i.e., each carrier is tracked coherently, baseband signals recombined after recovery, and the transmitter carrier is selected according to an optimum diversity strategy.

2.3.2   NARROW-BAND PN MODE

In the narrow-band PN mode, the forward commands and the return telemetry data will be superimposed on PN binary codes clocked at rates consistent with a 50 kHz and 150 kHz channel bandwidth. Specifically, the chip rates will be 34.133 or 102.4 kilochips per second respectively.

The major additional subunits added to the transponder for this mode of operation are:

- Receiver coder
- Transmitter coder
- Code clock
- Variable time sequential detector
- Search logic
- Code error tracking loop (includes code error combiner).

Briefly, in the PN mode, the receiver coder generates the PN code which, after initial synchronization is in phase with the received code. The code modulation is them removed from the incoming signal and the commands are then demodulated in a conventional manner by means of a Costas loop. Initial search for the proper code phase is performed by search logic which, in turn, is controlled by the doppler processor. Once synchronism is established the code tracking loop maintains it. Note that code tracking error is obtained by combining the outputs of the two diversity channels. In this manner, code tracking will be maintained regardless of signal fading on either one of the channels.

The outgoing telemetry data is modulo-2 added to the transmit coder output and the combined binary stream modulates the transmit carrier. The selection of the transmitter drive signal is performed in the PN mode in the manner identical to the conventional mode.

The receive and transmit PN code chip rates are independently selected from the MMT control panel. However, these coders are driven from a common clock and the phases of the receive and transmit codes have a definite integral relationship.

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2.3.3 WIDE-BAND PN MODE (RETURN LINK ONLY)

Transponder configuration in this mode is identical to the one in the narrow-band PN mode with the exception of the rate at which the transmitter coder is clocked. The chip rate for the wide-band transmit mode is 1024 kilochips per second. Also, to provide for an extended code length, a special switching arrangement is used to extend the repetition period of the wide-band code by a factor of 20. Since the receiver portion of the transponder is not modified when the wide-band transmission is used, the receive code search and tracking functions are the same as described in the preceding paragraph.

2.3.4 ADAPTIVE BURST COMMUNICATION (ABC) MODE

In the ABC mode the demodulated, diversity-combined signal from the receiver is supplied to the format sync and data regenerator block circuits. The ABC burst-blank format is derived and synchronized and bit sync is also obtained.

There are three signals supplied to the command data buffer. They are: bit sync, bursted-command data, and a data-present pulse. The bit sync is used to read the bursted-command data into the command buffer memory, and the data-present pulse indicates when commands are present in the received signal and also provides burst-sync information. The command data buffer debursts the received command data and derives the clock for the continuous stream of data. Both the data and the clock are then supplied to the command decoder.

In addition to deriving a data-present pulse, the format regenerator also provides the correct burst format (i.e., frame sync) to both the transmitter and receiver. This is necessary to reject the multipath. It should be noted that the only difference between the data-present pulse and the burst format is that when command data is not being received, the data present line is "down" while the burst format line is "up." This guarantees that the spacecraft receiver will not be gated off before the received signal is acquired.

The telemetry data and clock are supplied to the telemetry data buffer by the spacecraft. The telemetry buffer memory accepts the data and supplies it in bursted format to the transmitter. Programming of the desired telemetry data rate is selected from the MMT control panel along with the proper command data rate signals to the command data buffer. The control panel also selects 1 of 5 burst formats ranging from 2-10 m to the format regenerator when the regenerator is not in the format search mode.

2.3.5   GROUND SUPPORT EQUIPMENT

The basic complement of ground support equipment for the multimode transponder experiment includes a mobile test station consisting of a GSFC van, a top-mounted antenna, the Magnavox MTAR equipment, and several racks of associated test equipment. This basic ground station configuration could be transported to various locations for special tests.

2.4   INTERFERENCE CONSIDERATIONS

The TDRS and user spacecraft will be confronted with four basic types of interference, namely:

a.   Unintentional, upward directed, radio frequency interference (RFI) originating from communications equipment located on earth.

b.   Background interference (i.e., "Trash Noise") originating primarily in urban areas and is the composite of such things as ignition noise, switching transients, corona, and other forms of man made noise.

c.   Multipath interference between the direct path signal in the User-TDRS link and a replica of that signal which has been reflected off the earth.

d.   Co-channel interference between one user and all the other users in the same band. This is peculiar to the return link where all users are simultaneously accessing TDRS through the same channel.

A functional description of the interference problems in the forward and return link is shown in figures 2-9 and 2-10 respectively. In the sections that follow each of the aforementioned sources of interference will be discussed and their impact on the channel performance evaluated.

2.4.1   RADIO FREQUENCY INTERFERENCE

Unintentional, upward directed RFI from emitters located on the earth and in view of both the TDRS and user spacecraft can be a source of interference which will be deleterious. In this section is presented RFI data for the following TDRS/ User links:

Forward Link	Return Link
127.750 MHz	137 MHz
149 MHz	
401 Mhz	

2-11
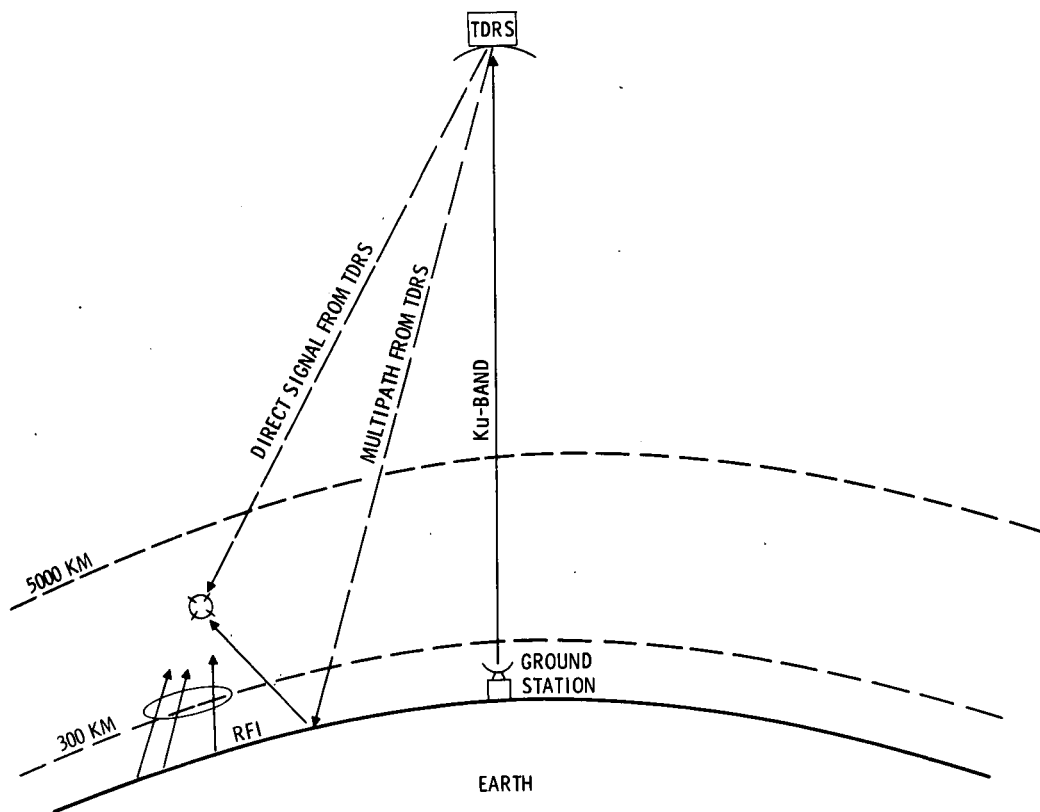
Figure 2-9. Forward Link Interference Diagram
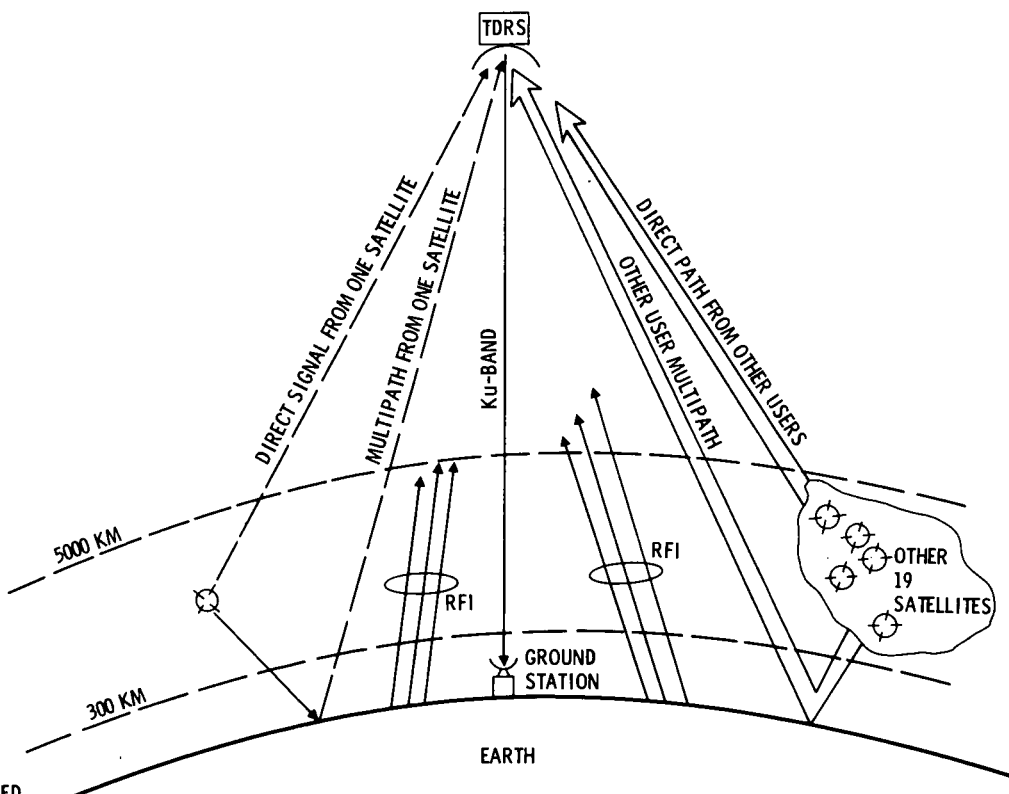
Figure 2-10. Return Link Interference Diagram

Some of these bands contain relatively high-powered, constant-envelope, narrow-band RFI. In order to evaluate the impact of RFI on the performance of the forward and return links Magnavox has, with the assistance of Mr. John W. Bryan of NASA/ Goddard Space Flight Center, evaluated pertinent information relative to RFI in the bands of interest. From computer tabulations provided by Bryan, an estimate of the worst case RFI distribution at the TDRS and user has been derived.

Morever, ESL Incorporated has recently concluded two related studies for NASA/GSFC* which examine the radio frequency interference problems relating to the TDRSS and the user spacecraft. The RFI modeling by ESL consists of examination of data contained in the International Frequency List compiled by the International Frequency Registration Board of the International Telecommunications Union, the Jeppesen Air Manuals, CONUS emitter tabulations from the Electromagnetic Compatibility Analysis Center and other sources. By a series of prediction programs ESL was able to provide an estimate of the power that would be received from each source of RFI at the TDRS in synchronous orbit with a 16 dB antenna gain. Figures 2-11 and 2-12, present a graphical indication of the RFI power density at TDRSS positions of 11°W and 143°W, respectively. These densities are distributed over the frequency band 120-170 MHz.

An assessment has been made of the impact of RFI on the user spacecraft. The user location is assumed 38°N/88°W, and the RFI density levels at the user spacecraft are shown in figure 2-13. In this case the user spacecraft is equipped with an omnidirectional antenna and is at an altitude of 1,000 kilometers. As an indication of the coverage of this user spacecraft, a satellite at 1000 km centered at 38°N and 88°W will, with an omnidirectional antenna, be in view of all of CONUS, and parts of Mexico and Canada.

Through our own research, that of John Bryan of NASA, and ESL, we have concluded that of the bands of interest the 149 MHz band is the least usable as a

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*Jenny, J.A., and Weiss, S.J., "The Effects of Multipath and RFI on the Tracking and Data Relay Satellite System," prepared under NASA Contract No. NAS5-20125, 19 March, 1971.

Jenny, J.A., and Shaft, P., "The Effects of Multipath and RFI on the TDRSS Command and Telemetry Links — A Final Report, prepared under NASA Contract No. NAS5-20228, 9 March 1972.

FREQUENCY (MHz)
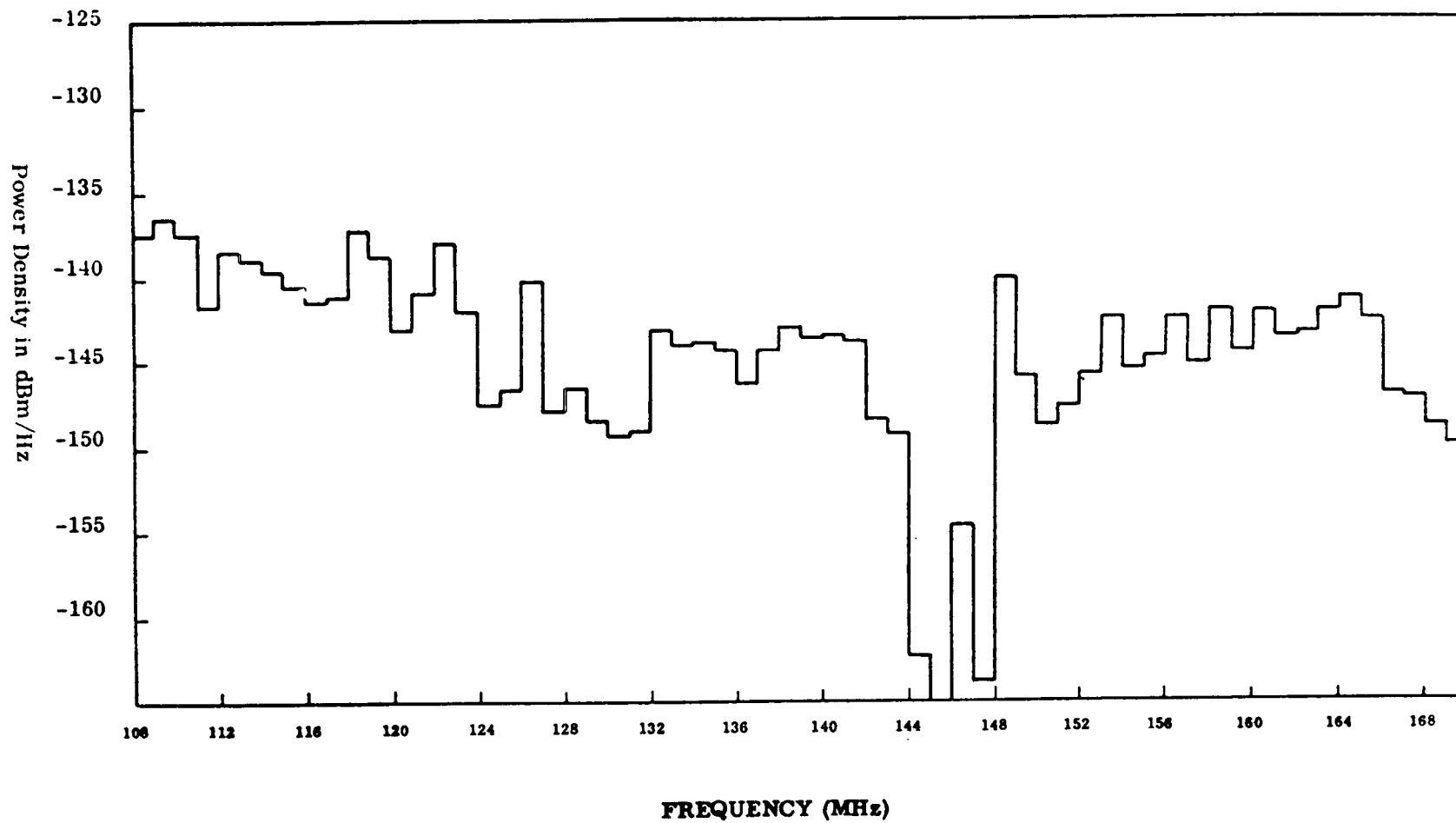
Figure 2-11. RFI Power Density for TDRS Located at 11°W
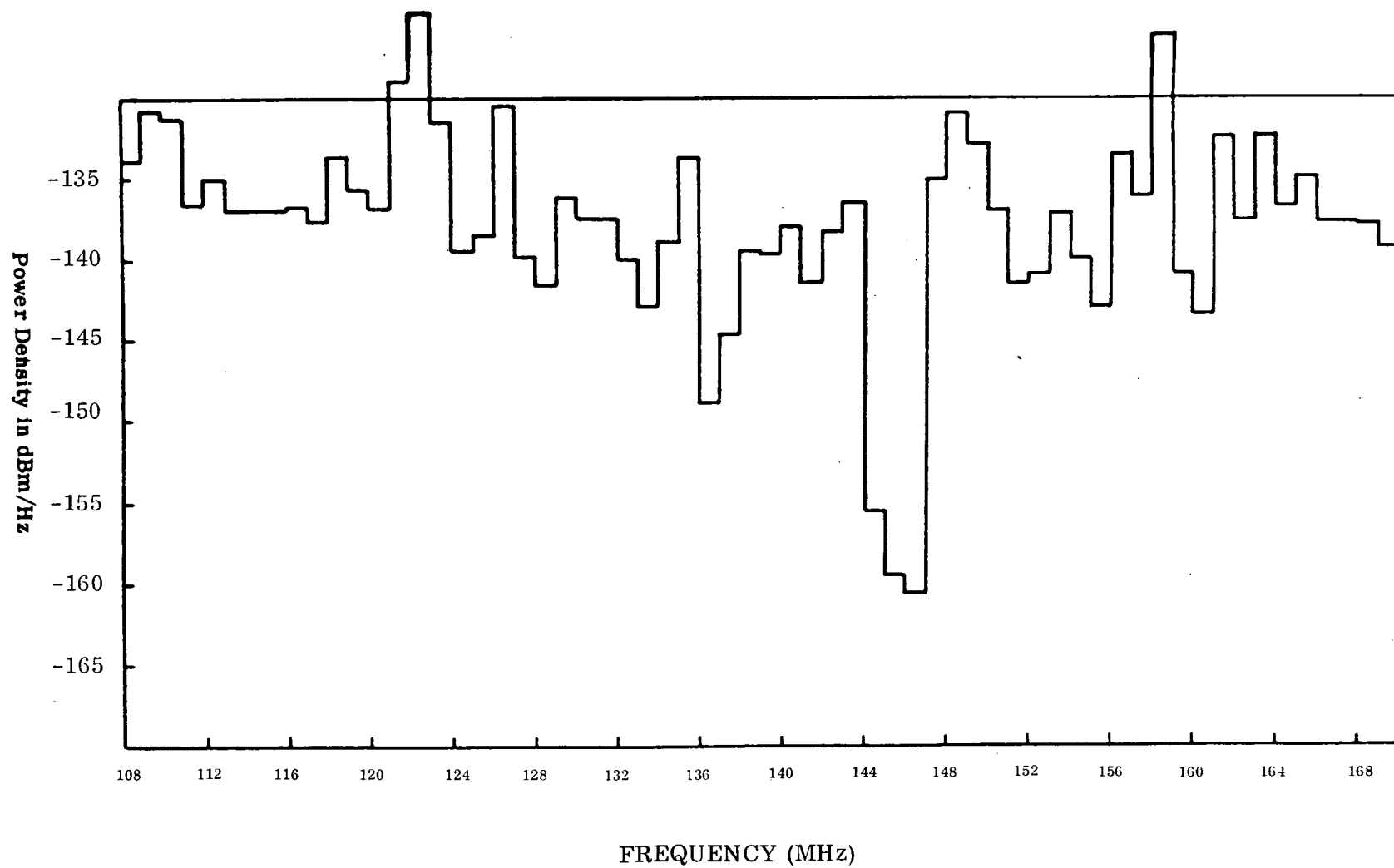
672-1640
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Figure 2-12. RFI Power Density for TDRS Located at 143°W
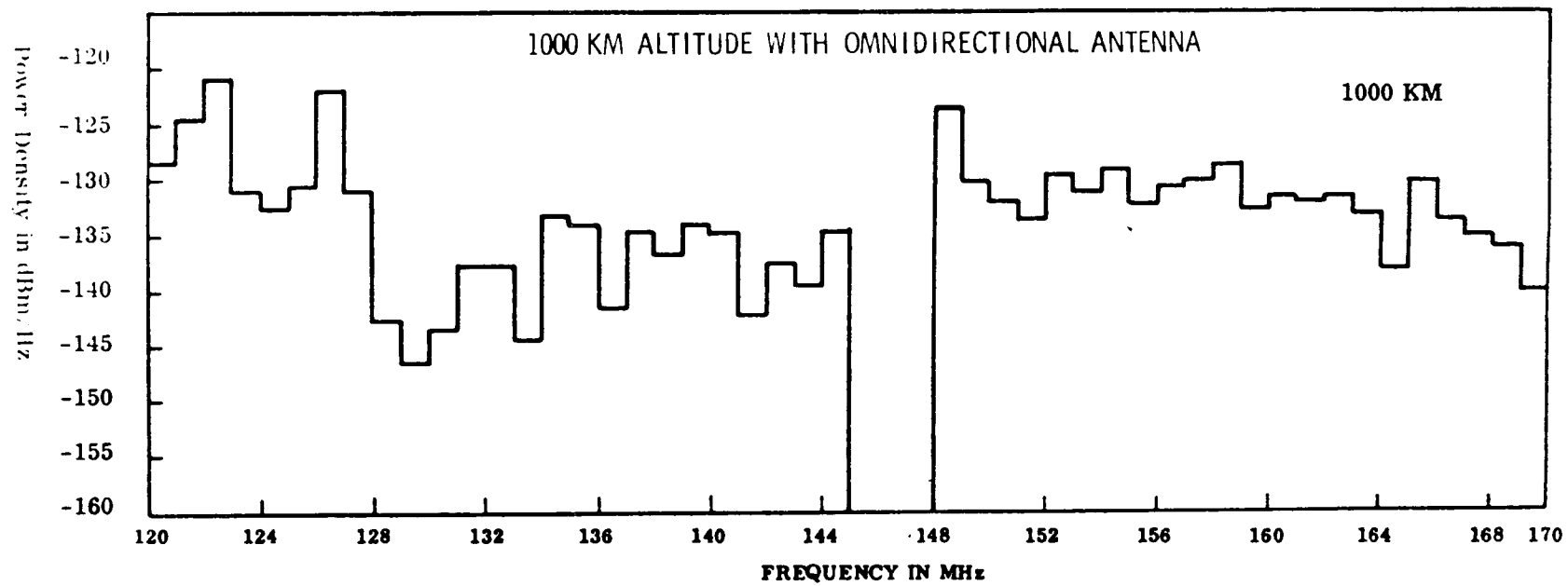
Figure 2-13. RFI Power Density at User Spacecraft

command band. The number of emitters in the 127.70 - 127.85 MHz band has been estimated as being:

a. 28 communication emitters assigned to the band

b. 122 communication emitters capable of being tuned in the band.

Bryan has conducted a frequency search in this band so that their effect on the user S/C might be assessed.

The assumptions made for this assessment are as follows:

a. User satellite is over central U.S.A.

b. User satellite altitude is 1000 km.

c. User satellite has an omnidirectional antenna (zero dB gain).

d. All ground based emitters are on and modulated.

e. All antennas patterns are uniform, omnidirectional and zero dB gain.

f. Ground based emitters are uncorrelated.

The input RFI power at the user/SC in a 10 kHz band centered around the carrier has been computed and is shown in table 2-1.

The number of emitters in the bands 136-138 MHz and 148-155 MHz both at the TDRS and the User S/C has been compiled by ESL and are presented in tables 2-2 and 2-3 respectively. Also shown in the table are the expected RFI power levels at the TDRS and the user spacecraft for various satellite locations.

The remaining band of interest is that in the range 400.5 MHz to 401.5 MHz. As of this time no attempt has been made to assess the effective RFI power at the user spacecraft. We have, however, compiled through the International Frequency List an estimate of the number of potential RFI sources in this band. This compilation is presented in table 2-4 for the various ITU regions.

2.4.2 TDRS "TRASH NOISE"

There is another important source of noise which should be considered and evaluated for its impact on TDRS/user channel. Specifically, this interference is the sum total of the "trash" — A more or less continuous background noise which originates in an urban environment and is due primarily to such things as ignition noise, switching transients, corona, etc. This continuous low level interference will

Table 2-1. RFI Sources at User S/C in the 127.7-127.85 MHz Band

Frequency	Average Power in 10 kHz Band	No. of Emitters
127.70 MHz	-83.4 dBm	6
127.75 MHz	-84.5 dBm	2
127.80 MHz	-81.0 dBm	14
127.85 MHz	-85.0 dBm	1

Table 2-2. Estimated RFI Sources at the TDRS

	TDRS Location - (Synchronous Altitude)					
	11°W		143°W		112°E	
Band	Power (dBm)	Number of Emitters	Power (dBm)	Number of Emitters	Power (dBm)	Number of Emitters
136-137	-81.3	132	-87.8	56	-99.4	5
137-138	-79.4	235	-84.3	100	-91.8	10
148-149	-75.1	114	-70.8	789	-79.3	25
149-150	-81.0	70	-72.9	852	-76.9	58
154-155	-80.6	252	-79.9	216	-89.5	46

Table 2-3. Estimated RFI Sources at the User

	USER LOCATION (Altitude - 1000 km)			
	38°N-88°W		50°N-30°E	
Band	Power (dBm)	Number of Emitters	Power (dBm)	Number of Emitters
136-137	-86.7	5	-71.0	130
137-138	-79.4	25	-70.0	178
148-149	-68.7	80	-69.0	15
149-150	-75.2	53	-97.0	2
154-155	-74.0	127	-89.6	6

Table 2-4. RFI Sources in the Band 400.5-401.5 MHz

ITU	EMITTER POWER ON THE GROUND (Watts)				
Region No.	0 - 0.9	1 - 9	10 - 99	100 - 999	$\geq$1000
I	59	4	1	1	1
II	61	1	-	-	-
III	62	12		10	

interfere with the desired signals in the command band, and can have a deleterious effect on the antenna temperature at the user spacecraft.

Lincoln Laboratories associated with the Massachusetts Institute of Technology has carried out over the past several years the most comprehensive measurement and evaluation of this continuous background noise. They have concluded that those cities associated with the eastern seaboard can be modeled as an interference source with power uniformly distributed over an aperture which represents the city, and that in the UHF band (216-369 MHz) the power density/square meter/Hz will be in the range of 3×10^{-18} to 1×10^{-18} watts per meter square per Hz. These numbers are representative for moderately large cities such as Miami and Philadelphia, whereas New York City and its associated metropolitan area would produce as much as a 0.6 dB increase.

Based on experimental data the "α" law equation has been developed* to predict galactic noise temperatures with reasonable accuracy in the VHF-UHF frequency and is as follows:

$$T_g = C_g \lambda^{\alpha}, \quad C_g = [30 \text{ to } 300], \quad \alpha = [2.5 \text{ to } 2.86]$$

In the equation above the constant C_g is a function of the galactic activity of the region of space at which the antenna is looking. C_g is maximum at the galactic center and minimum at its pole. Figure 2-14 plots this function at its extremes.

It can be shown that the equation for the noise temperature at a satellite at altitude h, with an omni-directional antenna due to a distributed noise source, such

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*G Ploussios, et al., Noise Temperature of Airborne Antennas at UHF, Technical Note ESD-TR-66-237, Lincoln Laboratory, Massachusetts Institute of Technology, 6 December 1966.

as "trash noise," radiating from a circular urban area with radius r, is

$$T_{tr} = \frac{\lambda^2 C_o}{16\pi K_o} \left(\frac{r}{h}\right)^2$$

The assumptions made to arrive at the above expression include a constant power density over an area of interest and a user spacecraft altitude which is much greater than the radius of the urban area.

Presented in figure 2-15 is a graph depicting the "trash noise" density as a function of urban radius for various frequency bands and user spacecraft altitudes. For further details on this subject the reader is directed to Appendix C.

It is important also to realize that due to the large field of view of even low orbiting satellites* that the radius, r, used above can be large. This is the result of the appearance of many discrete point sources acting as one large area distributed source. Radius values can range from 200-400 KM for the NYC area, to 100 KM for the Chicago area, to negligible for water or desert areas.

2.4.3   USER PROPAGATION PATH ANALYSIS

As shown in figures 2-9 and 2-10, a signal transmitted from either TDRS or user satellite will arrive at the other satellite by direct and indirect (reflection off a nonsmooth earth) channels. This indirect path, commonly referred to as the multipath signal must be understood in order to predict the operation of the communication link. Therefore, it is necessary to define and analyze the parameters in both the direct and multipath channels. A brief summary is presented here and for a more detailed explanation readers should refer to "Multipath/Modulation Study for the Tracking and Data Relay Satellite System" by J.N. Birch, Final Report Contract NAS5-10744 prepared by The Magnavox Company, Silver Spring, Maryland.

2.4.3.1   The Multipath Signal

A multipath signal is characterized by a time varying process which is statistically nonstationary because of the changing velocities and geometry between a user and the TDRS; however, the short-term statistics of this link can be considered stationary. This reflected signal will consist of a diffuse and specular component. The degree of diffuseness or specularity of the reflected signal will depend upon such

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*The area of the U.S. is 9.37×10^6 KM^2 or 1.8 percent of the earth's surface. The field of view of a 300 KM orbiting satellite is 2.2 percent.
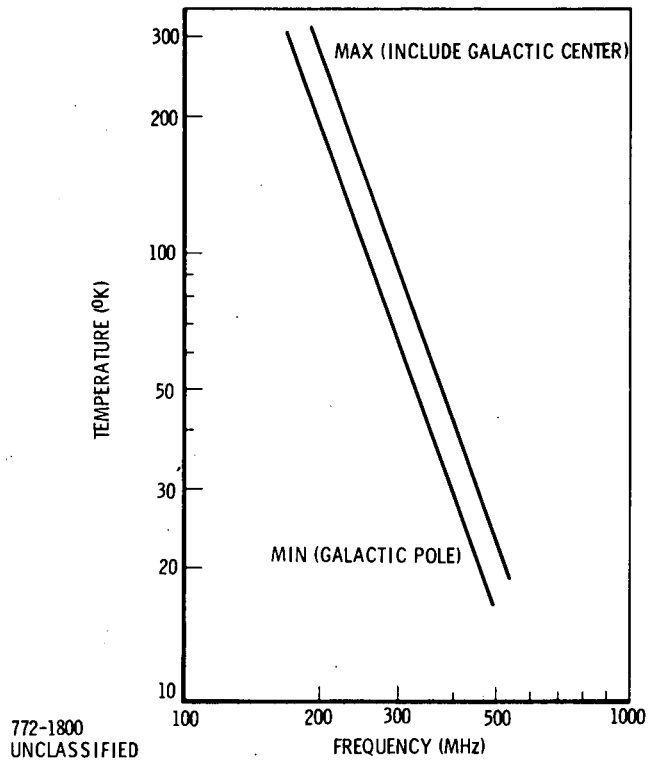
Figure 2-14.   Galactic Temperature Over a Hemisphere
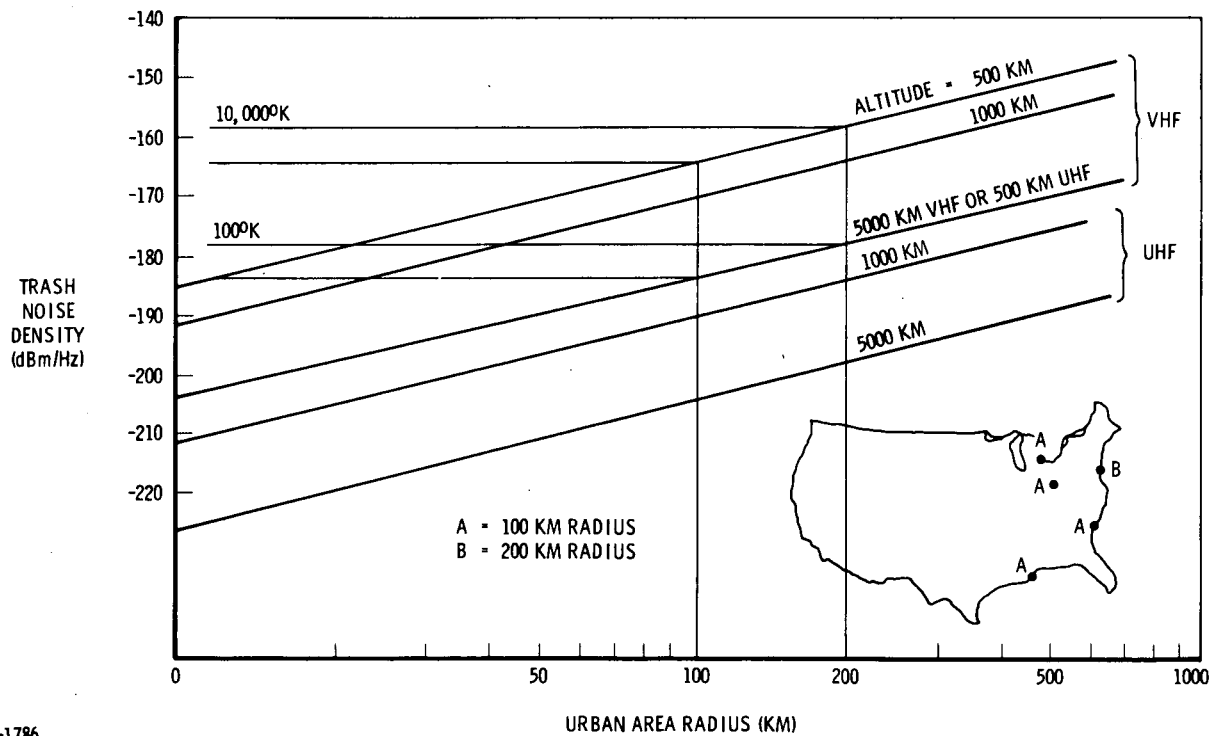
Figure 2-15.   Trash Noise at User Spacecraft

2-21

factors as the grazing angle ψ, the roughness σ of the earth near the point of reflection, and the correlation length L across the surface of the earth. Roughness factor σ is a measure of the RMS height variations along the surface of the earth, and the correlation length L is a measure of the degree of correlation between points along the surface of the earth. The reflected power can consist of both specular and diffuse components. The specular component is essentially a delayed replica of the transmitted signal, whereas the diffuse component is noise like.

The relative expected specular and diffuse reflected power are illustrated in figure 2-16, as a function of the grazing angle ψ for 136 MHz and an average earth toughness and correlation distance. It should be noted that the specular power decreases with frequency and the diffuse power is essentially independent of frequency. It can be seen that at low-grazing angles the divergence factor serves to diminish the multipath signal, while at high grazing angles the primary reflected energy is diffuse. Furthermore, for reasonable roughness factors and correlation lengths, the primary source of reflected power will be diffuse for grazing angles in excess of 20 degrees at VHF and UHF frequencies. Figure 2-17 provides an indication of the multipath signal level as a function of orbital altitude of the user satellite.

2.4.3.2   The Effect of Other User's Co-channel Multipath

It is obvious from the above (figure 2-17) that the multipath contributed by a user depends upon its altitude and user antenna anomalies. For the moment we will defer the discussion of antenna anomalies but anomalies will be considered in our concluding statements.

In the forward link the plot of figure 2-17 can be used directly, however, consider for the moment the return VHF link where 20 user signals are accessing a TDRS simultaneously. Obviously the total multipath signal consisting of the multipath from 20 users in the field of view of a TDRS will depend upon the user altitudes. These altitudes are in turn determined by the population and orbits associated with the respective users. In table 2-5 we list the projected satellite populations for the low altitude user spacecraft from 1976 through 1980. We see from the table that the 1976 user population is the largest. In figure 2-18 we show the total multipath contributed by the total satellite population by year.

Summing up the multipath signal contributed by 20 simultaneous users in 1976 we find that the total multipath relative to one user is +7 dB. Thus, we find that

PROPAGATION FREQ = 136 MHz
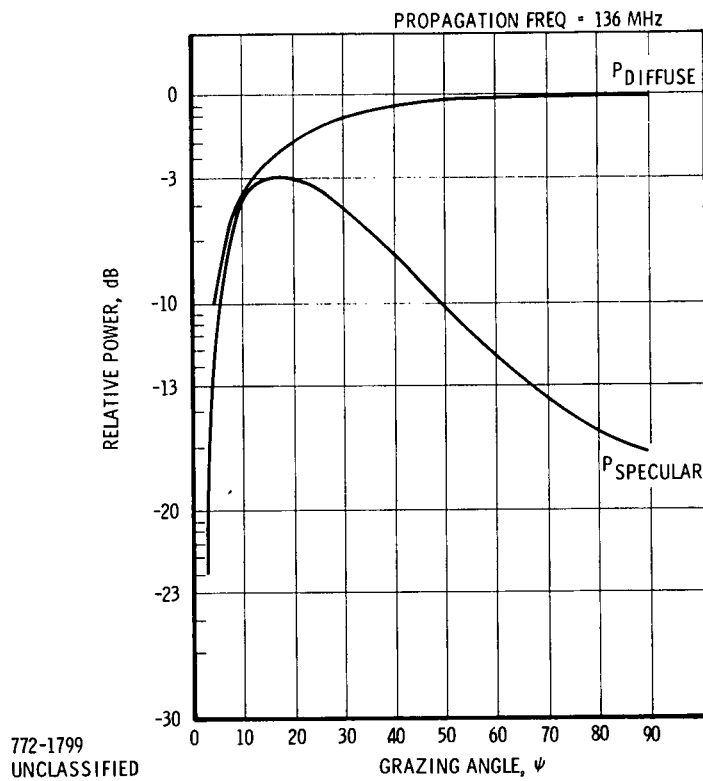
Figure 2-16. Relative Specular and Diffuse Reflected Power vs Grazing Angle
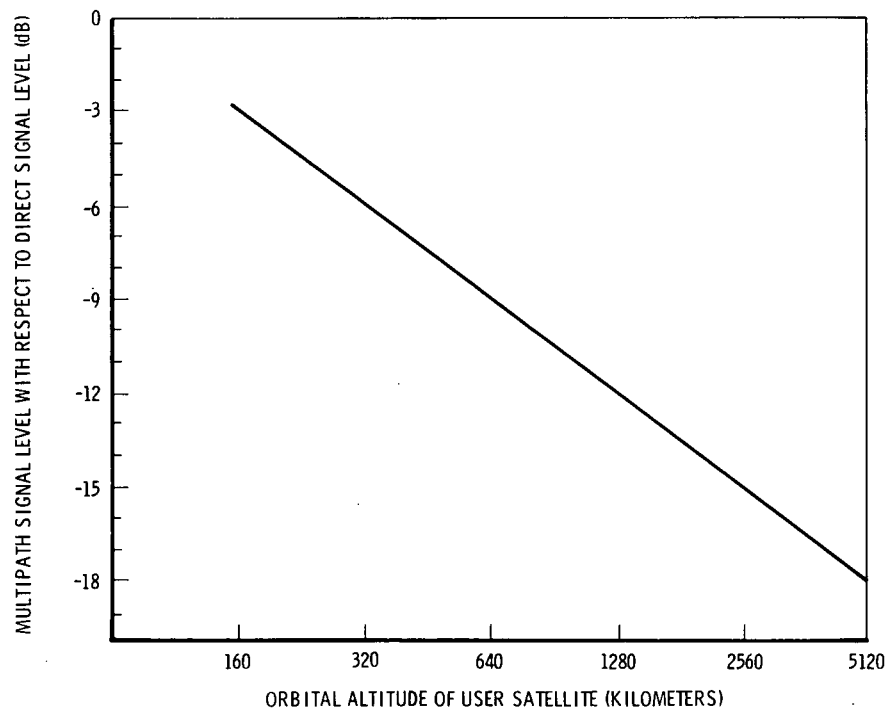
Figure 2-17. Multipath/Direct Signal Ratio as a Function of Orbital Altitude

2-23

Table 2-5. Low Altitude Spacecraft Population Projections: 1976-1980

Year	76	77	78	79	80
ALTITUDES 150-275 km	1	1			
275-300	4				
300-4000	7	7			
550	9	9	8	7	6
700-800	10		8	6	
600-900	9	8	7		
1000	10	9	10	7	8
1100		8	7		6
6000	8				
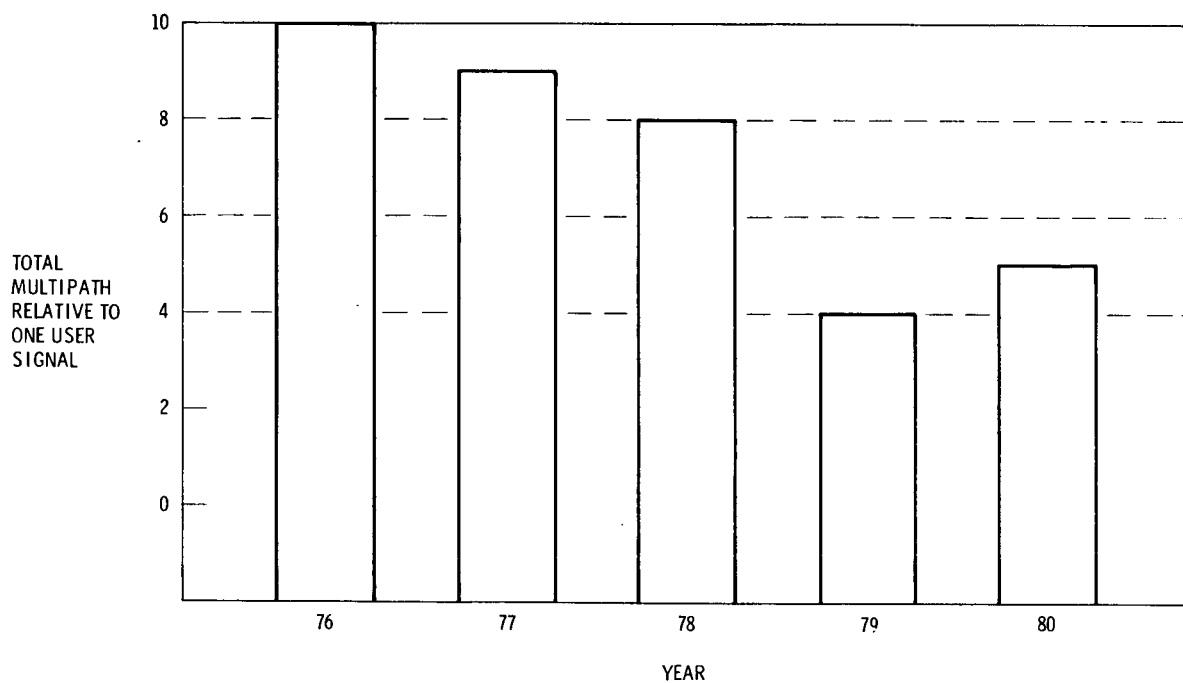
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Figure 2-18. Projected Multipath Level

2-24

the multipath problem in the return link is diminished from the worst case condition where all 20 users are considered to be in low orbits, e.g., 300 km.

Unless stringent and relatively expensive antenna designs are used by the low orbit user, antenna anomalies can occur in the antenna patterns. We have evaluated some of the antenna patterns associated with low data rate user spacecraft and we have concluded from our research that a nominal 0 dB antenna is impractical and one must consider at least a ± 3 dB variation in the low data rate user antenna. In other words, the direct path signal can be reduced by 3 dB while energy directed toward the earth can be enhanced by 3 dB producing a 6 dB variation at times between the direct desired signal and the multipath signal.

It can be shown that when a large number of user signals are accessing the TDRS the antenna anomalies average out in the multipath signal so that for purposes of analysis the multipath signals from the various users can be considered as originating from 0 dB omni-directional antennas.

2.4.3.3   The Direct Path Interference Due to Other Users

As shown in figure 2-10 a return link signal will be subjected to interference not only from RFI and user multipath signals, but from other signals originating from the 19 other user spacecraft and propagating along the direct path from user-to-TDRS. One must assume that at the point of transmission these signals are of equal power. Their effect, therefore, will be much more pronounced than that of the return link multipath signals because while the multipath/signal ratio over the user altitudes of interest are on the order of 7 dB and the direct path interference/signal ratio is on the order of 12 dB. Moreover, as the user s/c of interest increases its altitude, the effect of its own multipath decreases significantly whereas an increase in altitude over the range of interest (300- 500 km) produces almost no change in the ratio of other users direct path power to desired signal. This effect will be shown in more detail in following sections.

2.5   SIGNAL/NOISE POWER BUDGETS

2.5.1   FORWARD LINK PERFORMANCE

As illustrated in figure 2-9, the forward link signal must contend with the multipath signal and RFI in addition to ambient noise at the user spacecraft. The impact of these effects can be minimized by obtaining the maximum processing gain

through a specific bandwidth allocation. It has been shown* that for a specified RF signal bandwidth the processing gain (PG) can be maximized, but once the chip rate exceeds the RF bandwidth, increasing the PN chip rate to increase PG is offset by correlation losses due to bandwidth restriction. In practice, there are other losses not covered by theory but inherent to the system. For this reason it is advisable to maintain an RF bandwidth equal to a factor of approximately 1.4 times the chip rate, thereby ensuring minimum PG losses due to bandwidth restrictions. The forward link PN chip rates, therefore, will be as follows for the TDRS configuration:

Bandwidth Restriction	PN Chip Rate
50 kHz	34 kilochips/sec
150 kHz	100 kilochips/sec

The processing gain (PG) obtainable within the system RF bandwidth constraints is proportional to the ratio of PN chip rate to bit rate. The bit rates of interest for the MMT are 100, 300 and 1000 bps. The forward link communications performance in terms of output signal-to-noise ratio can be shown to be equal to

$$\frac{S}{N} = \frac{P_u \ (PG)}{N' + RFI + Multipath} \qquad 2-1$$

where

$$P_u \qquad = \text{ signal power received at user}$$

PG $\qquad$ = Chip Rate/Bit Rate = Processing Gain

N' $\qquad$ = input noise power

RFI $\qquad$ = effective RFI at receiver input

Multipath = $4P_u/\alpha$ (worst case)

$\alpha \qquad$ = $2h/300$

h $\qquad$ = user altitude (= 300 to 5000 km)

This expression may be rewritten in terms of output carrier-to-noise density, as follows:

$$\frac{C}{N_o} = \frac{P_u}{N_1 + RFI_o + 1/CR \ [4P_u/\alpha]} \qquad 2-2$$

$\qquad$ PN chip rate

$\qquad$ RFI noise density

$\qquad$ input thermal noise density

*J.N. Birch, "Multipath/Modulation Study for the Tracking and Data Relay Satellite System" Final Report Contract NAS3-10744 prepared by The Magnavox Co., Silver Spring, Maryland.

The expected output carrier-to-noise density at VHF (i.e., either 127.775 or 149 MHz) as a function of input RFI density with system temperature and user altitude as parameters, is shown for a chip rate of 32 kilochips per sec in figure 2-19. For 100 kilochips per sec the curves are similar except the C/N_o is about 1 dB higher in the region of -180 to -200 dBm/Hz. A similar set of curves is presented in figure 2-20 for UHF frequencies (i.e., 401 MHz). For 100 kilochips in this case the curves are the same except for No. 1 which has a C/N_o about 2 dB higher in the region of -180 to -200 dBm/Hz.

An estimate of the impact of ground based RFI sources on the forward-link bit rate at VHF frequencies is shown in figure 2-21. For each of the aforementioned analyses the following system budgets were assumed.

TDRS EIRP = 30 dBw

User Antenna Gain = -3 dBw

Extraneous Losses = 3 dB

BER for Δ-PSK = 10^{-5}

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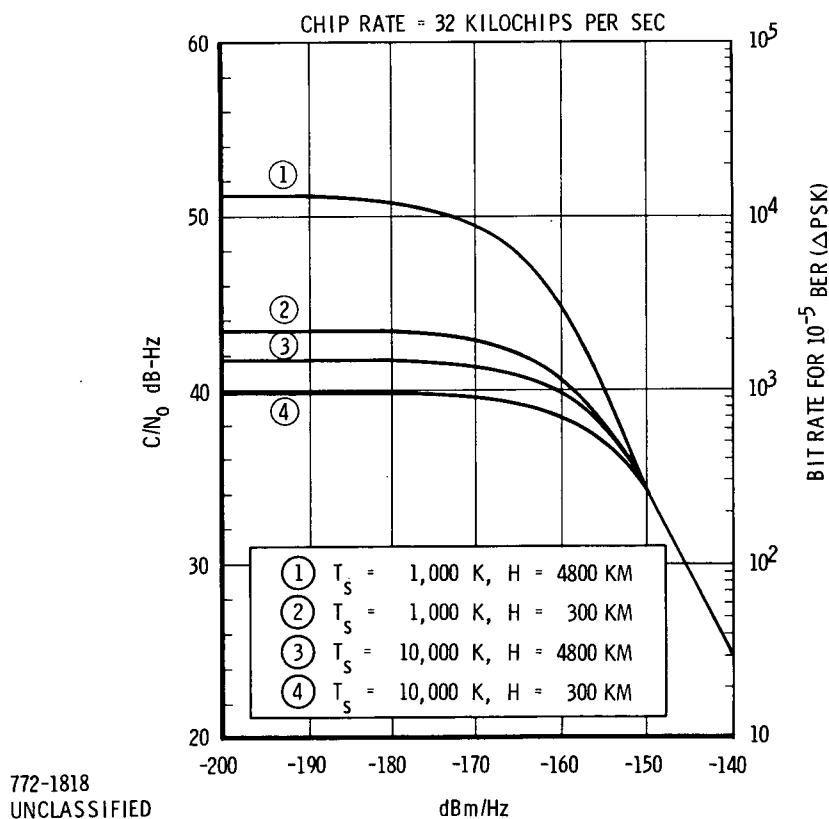
Figure 2-19. Forward Link Performance at VHF

2-27
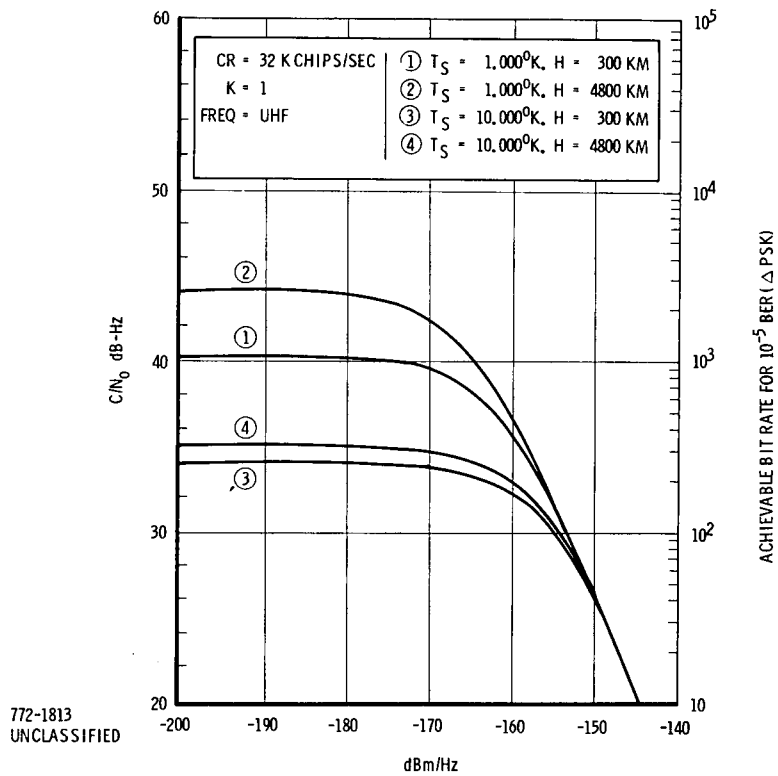
Figure 2-20. Forward Link Performance at UHF
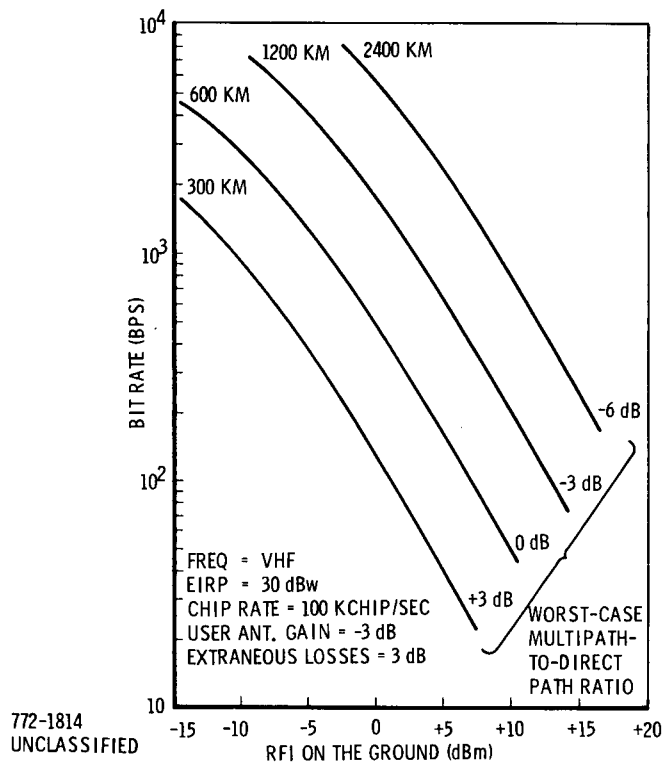
Figure 2-21. Forward Link Bit Rate as a Function
of the RFI Source on the Ground

2-28

2.5.2 RETURN LINK PERFORMANCE

The curves of figures 2-22 and 2-23 are based on the following general equation

$$\frac{C}{N_0} = \frac{P_{TDRS}}{N_1 + RFI_0 + \frac{1}{CR}\left\{K\left[\frac{4\,P_{TDRS}}{\alpha} + \frac{(n-1)}{19}RP_{TDRS}\right] + (n-1)\,P_{TDRS}\right\}} \qquad (2\text{-}3)$$

where

N_1 = the input noise density at TDRS

RFI_0 = the input RFI density at TDRS

k = an attenuation factor proportional to the reflection coefficient

n = the number of users per channel

R = the ratio of average multipath contribution of other users to the desired signal power (= 7 dB for the 1976 user spacecraft distribution)

α = $2h/300$; h = user altitude

P_{TDRS} = 37 dBm + 14 dB - 167.5 dB - 3 dB - 3 dB = 122.5 dBm

    ↑ user power 5 watts typical   ↑ TDRS antenna   ↑ path loss   ↑ user antenna   ↑ extraneous losses

Equation 2-1 relates the output signal-to-noise ratio for each user given the user power level at the TDRS, the ratio of the chip rate to data rate (processing gain), the noise density per channel, the number of users accessing each channel, the RFI per channel, and the multipath per channel. The curves in figures 2-22 and 2-23 are conservative in that all potential losses including path loss, extraneous losses, user antenna anomalies and lowest altitudes have been considered. The curves in figures 2-22 and 2-23 are drawn for 5 watt user power levels. There are two distinct regions associated with the performance curves. A region where all curves converge and have essentially equal performance. This region illustrates that RFI limits the performance of all the systems whereas in the second region where the curves separate, the systems are limited by noise and multipath and other user signals.

ALTITUDE = 300
K = 1.0
ERP = 5w
FREQ = 136 MHz

① CR = 100, N = 1
② CR = 100, N = 2
③ CR = 1000, N = 20
④ CR = 500, N = 20

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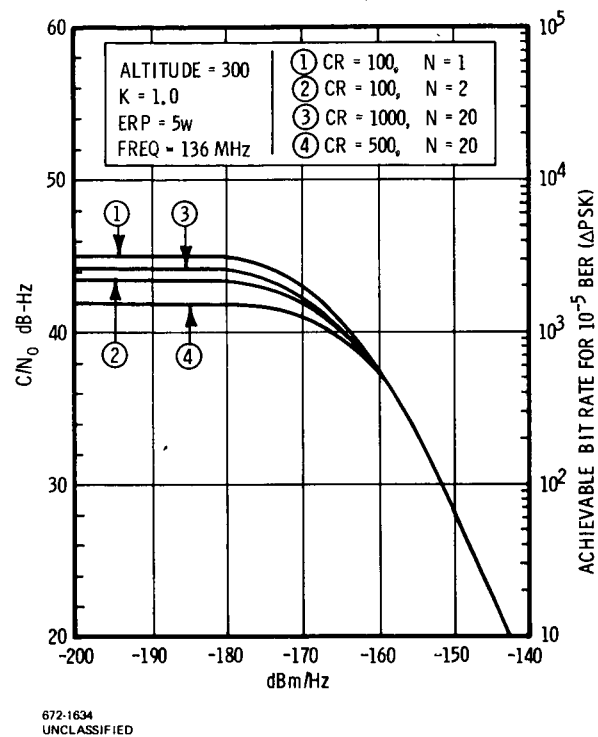
Figure 2-22. Return Link Performance

ALTITUDE = 300
K = .05
ERP = 5w
FREQ = 136 MHz

① CR = 100, N = 1
② CR = 100, N = 2
③ CR = 1000, N = 20
④ CR = 500, N = 20

672-1636
UNCLASSIFIED
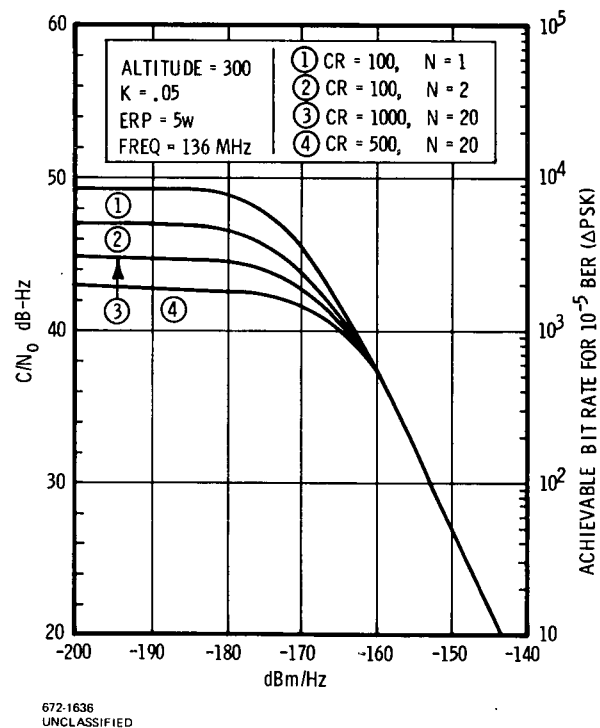
Figure 2-23. Return Link Performance

2-30

The total multipath for the wide-band curves is based on the 1976 satellite population estimates. We see from the curves that the narrow-band (100 kilochip/sec) mode can out-perform the 500 kilochip wide-band mode under the following assumptions:

User Power	5 watts
Extraneous Loss	3 dB
User Antenna Gain	-3 dB
Frequency	137 MHz
TDRS Antenna Gain	14 dB
TDRS T_s	500° Kelvin

However, the final choice of return link chip rates will be greatly influenced by the return link ranging errors.

We see from the curves that all the systems are RFI limited and when the RFI level is -160 dBm/Hz (a realistic value) none of the techniques will support a data rate of 1000 bit per second.

They also indicate which user bit rates can be supported by the return link with a 5 watt user power level. If forward error control is applied to the return link (e.g. rate 1/2 (48,24) nonsystematic convolutional code) the data-rate capacity can be increased by a factor of four. Thus forward control is highly recommended for the return link. With error control, the return link can support 2000 bit per second at BEP of 10^{-5} in the presence of -160 dBm/Hz RFI.

Increasing user power levels in the return link is a tempting approach to enhance the performance of the return link. However, power sources on board the low data rate user satellites limit the available EIRP. Shown in figure 2-24 is the uncoded user bit rate which can be supported at a 10^{-5} bit error probability as a function of the RFI level in the return link. These curves are based on equation 2-3 and are drawn for user power levels of 5, 10, 20, and 40 watts and in all cases the PN chip rate is 1000 kilochips per second for all users. Note that an increase in user power levels of 3, 6, or 9 dB with reference to 5 watts does not result in a comparable increase in user data rate. Thus, there are diminishing returns when user power is increased beyond 5 to 10 watts.

2.5.3   MULTIMODE TRANSPONDER RF POWER REQUIREMENTS

The previous discussion predicts that the TDRS received signal strength from a typical user satellite with 5 watts of RF power output will be on the order of
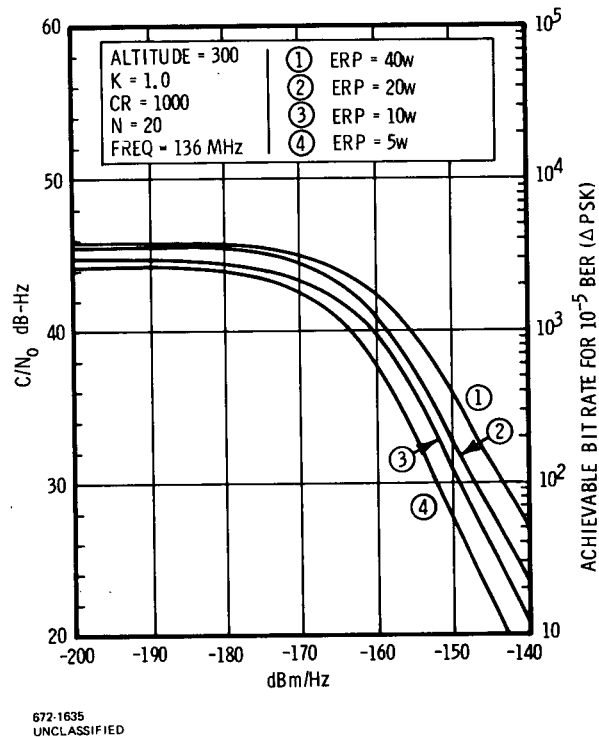
Figure 2-24. Return Link Performance as a Function of User EIRP

-122.5 dBm. This then should be the nominal received signal level for the multimode transponder. Accordingly, the statement of work has specified the dynamic signal range for the multimode transponder at -100 to -140 dBm. Adequate provision has been made for both the largest and smallest anticipated user signals.

The range of received RF signal levels for a possible future experiment using the MMT in an aircraft test bed with the MTAR in a ground based vehicle is summarized in table 2-6. A budget is presented for both a 1 watt and a 20 watt transmitter. The maximum received signal level calculation is based on a 4 mile range with no transmitter attenuation and the minimum signal level calculation is based on a 200 mile range with the transmitt output attenuated 30 dB. It is quite evident from table 2-6 that an RF output of 1 watt is more than adequate to average the MMT and MTAR receivers over the dynamic signal range of interest.

Table 2-6. RF Signal Level Budget

F_o	Rx SIGNAL LEVEL* (Tx 20w)	Rx SIGNAL LEVEL* (Tx = 1.0 W)	Rx SIGNAL LEVEL (S.O.W.)
127.750 MHz	-48 to -114 dBm	-73 to -137 dBm	-100 to -145 dBm
149 MHz	-31 to -115 dBm	-74 to -138 dBm	-100 to -145 dBm
401 MHz MMT	-58 to -122 dBm	-81 to -145 dBm	-100 to -145 dBm
MTAR 137 MHz	-57 to -121 dBm	-77 to -141 dBm	-100 to -140 dBm

*Max. level based on 4 mi. and no attenuation.
Minimum level based on 200 mi. and 30 dB attenuation.

2.6   MULTIPLE ACCESS CAPABILITY OF TRANSPONDER MODES

The multiple access capability of two different possible modulation schemes is determined here for the case of a significant multipath environment. The two schemes are: 1) the pseudonoise, spread spectrum one-random access by various users occurs in the same wide bandwidth-against multipath, the modulation is designed only to discriminate against it; 2) the narrow-band, adaptive burst modulation one-orthogonal access by various users occurs on an FDMA basis-the burst transmission on a given channel is designed to avoid multipath.

2.6.1   PN (PSEUDONOISE)

The multipath medium is represented by the differential time delay structure where the zero delay and unity gain path is the direct one, and all other paths correspond to resolvable multipaths having a delay τ_m and a time-varying vector gain $\hat{a}_m$. The characteristic of each path is actually a time-varying random variable, with the average interval of stationary corresponding to the differential Doppler, or fade rate, for that path. The receiver output Y(t) consists of the transmitted signal X(t) which is received on the direct path plus M multipaths, plus additive noise N(t), and the additive interference of L random accesses which are each received via similar but independent multipath structures. The expression for Shannon capacity in this situation is

$$C = [W]max \left[\log_2 \frac{1}{1-\rho^2} \right]$$

2-33

$$W = \text{system bandwidth}$$

ρ^2 = normalized crosscorrelation between $X(t)$ and $Y(t)$

$$\rho^2 = \frac{<X(t)\ Y(t+\tau)>^2}{<X^2(t)>\ <Y^2(t)>}$$

Now the crosscorrelation between $X(t)$ and the output of each multipath is zero. This is due both to the fact that the minimum multipath delay is greater than a PN chip width (the PN correlation function goes to a negligible value for this case), and the fact that the random time variation of the characteristic of each path will give a zero average crosscorrelation. The crosscorrelation of $X(t)$ and the noise and the other multiple access terms of course also is zero. Only the direct path contributes to the numerator of ρ^2. However all the multipaths and the other factors constitute inter-ference power and thus contributes to the denominator of ρ^2. One then gets the following result for the crosscorrelation. (See figure 2-25.)

$$\rho^2 = \frac{S_i^2}{\left[S_i\right]\left[S_i + A_m\ S_i + N_i + LA_L\ (1+A_m)\ S_i\right]}$$

S_i = desired received signal power on direct path

A_m = relative power level of all the multipaths

A_L = average relative power level of each interferring access

L = total number of interferring accesses

N_i = $N_o W$ = receiver noise power in bandwidth W.

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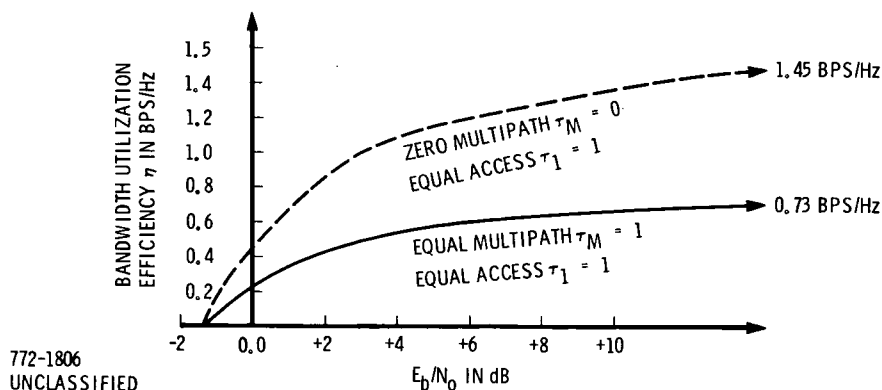
Figure 2-25. Shannon-Type Bound for Bandwidth
Efficiency vs. Power Efficiency for PN

2-34

2.6.2   PN RANDOM ACCESS PERFORMANCE

The performance of a wideband PN, random access link in a multipath environment is given by the following simple, conventional expression.

$$S/N_o \;=\; \frac{T_b W S_i}{n_o W + a_m S_i + La_L (1+a_m) S_i}$$

$$S/N_o \;=\; \text{output S/N available for bit detection}$$

The other symbols here have the same definition as in the previous discussion on Shannon bounds. Note however, now that we are discussing practical systems, that W is the effective system processing bandwidth, and approximately equals the PN chip rate. In contrast, the allocated system bandwidth must be greater than this value, since the power spectrum attenuation must be defined relative to the PN clock rate bandwidth as a unit. The use of techniques such as staggered quadri-phase PN will minimize the allocated spectrum required. However, otherwise such techniques do not change performance given by the above expression in terms of clock rate bandwidth. Also note that in the above expression the spectral density N_o pertains to the sum total of all ambient Gaussian noise at the receiver, i.e., the sum of receiver noise and of RFI which because of its density will average out to look like Gaussian noise.

One can manipulate the above expression to put it now into the same form as for the Shannon-bound determination

$$S/N_o \;=\; \frac{1}{\dfrac{n_o}{S_i T_b} + \dfrac{a_m + La_l(1+a_m)}{T_b W}}$$

$$\frac{S_i T_b}{n_o} \;=\; \frac{E_b}{n_o} \;=\; \frac{\text{received energy per bit}}{\text{ambient Guassian noise spectral density}}$$

For $L \gg 1$, the second term in the denominator approximate to $\dfrac{La_L (1+a_m)}{T_b W}$

$$n \;=\; \frac{(L+1)}{T_b W} \approx \frac{L}{T_b W} \quad \text{bandwidth utilization efficiency}$$

Therefore

$$S/N_o = \frac{1}{\frac{n_o}{E_b} + n\, a_L\, (1+a_m)}$$

$$n = \frac{1}{a_L\,(1+a_m)} \left[\frac{1}{S/N_{o_{req'd}}} - \frac{1}{E_b/n_o} \right]$$

for PN, non-coded data

For a noncoded, ΔPSK modulated digital data signal, the $S/N_{o_{req'd}}$ is about 10 dB for a 10^{-5} bit error rate. Using this value, bandwidth efficiency versus power efficiency, for the case of equal strength access and equal strength multipath, is indicated in figure 2-26. For other cases of relative multipath strength, and/or relative access strength, one merely scales the ordinate n by the values of these relative strengths.

For the case of coded data modulation of the PN carrier, the above expression still applies, but now one uses the smaller value of $S/N_{o_{req'd}}$ that is achievable with coding to obtain improved performance. For an optimized rate 1/2 sequential decoding, and a bit detection error rate of 10^{-5}, an $S/N_{o_{req'd}}$ per bit of 5.5 dB is achievable with hard decisions, whereas 4.5 dB is achievable with soft decisions. The results for the hard decision, sequential decoding case are superposed on figure 2-26.

For the case of PDM voice modulation of the PN carrier, the form of the above expression also still applies, except that now n must be interpreted as the product of the number of accesses times the PDM bandwidth (or clock rate) all
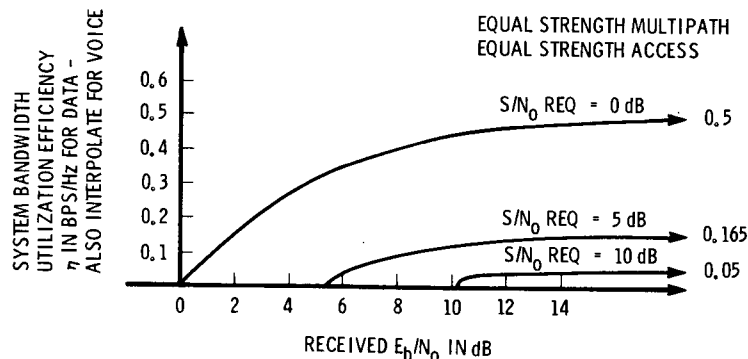
Figure 2-26. Bandwidth Utilization Efficiency
vs Power Efficiency for PN

2-36

divided by the PN bandwidth (or chip rate). Also the appropriate $S/N_{o_{req'd}}$ of 0 dB (threshold) or 10 dB (good quality) must be used. Noting that the appropriate interpretation is required, the results for PDM are also superposed in figure 2-26, where the case of $S/N_{o_{req'd}} = 0$ dB applies to it but not to data transmission.

2.6.3 ABC (ADAPTIVE BURST COMMUNICATION)

In this case the same time delay structure is used for the multipath medium. However the switching action of the receiver, in blanking communication periodically (on for τ_1 secs and off for τ_m secs), must be included. Also since the design is an orthogonal access one, we do not have multiple access interference.

The crosscorrelation during the on-time of the switch has no multipath contribution either in the numerator or denominator of the expression, because of the nature of the design.

$$\rho^2 = \frac{S_i^2}{[S_i][S_i + N_i]}$$

$$\ln 2 = \frac{1}{\log_2 \epsilon} = -1.6 \text{ dB}.$$

Nevertheless, the corresponding peak power for the ABC scheme is greater than this amount by the reciprocal of the burst duty factor. In contrast the peak and average powers for the PN scheme are both equal to the above amount. For peak power limited situations (such as seem likely to apply here because of the absolute parameter sizes of on-time), this is significant. The efficiency expression in terms of peak power is as follows:

$$\boxed{S/N_{\substack{peak \\ 1 \text{ bit} \\ \text{for ABC}}} = \frac{1}{n} \left[2^n \left(\frac{\tau_1 + \tau_m}{\tau_1} \right) - 1 \right]}$$

The bandwidth versus power efficiency results for the ABC scheme are indicated in figure 2-27 for the case of a 1/5 duty factor.

BANDWIDTH UTILIZATION EFFICIENCY IN BPS/Hz

1.2
1.0
0.8
0.6
0.4
0.2

DUTY FACTOR $= \frac{1}{5}$

5.4

0   +2   +4   +6   +8   +10   +12   +14   +16

PEAK S/N PER BIT IN dB

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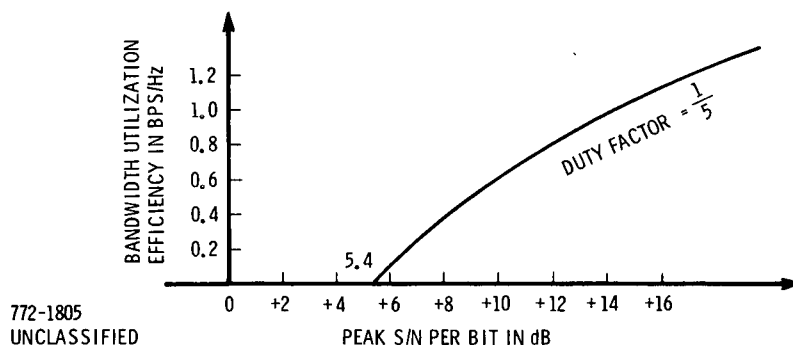
Figure 2-27. Shannon-Type Bound for Bandwidth Efficiency
vs. Power Efficiency for ABC

2.6.4   ABC RANDOM ACCESS PERFORMANCE

For an orthogonal access ABC link, the matched filter value of bandwidth utilization efficiency is just the burst duty factor. The efficiency then is 0.2 bps/Hz for the case illustrated in the previous discussion on Shannon-bound. Now the channel allocation bandwidth for ABC is of course greater than the matched filter value, so that in this sense the bandwidth efficiency is actually about 2/3 the above values for data. However since, as mentioned, the PN scheme also requires a bandwidth allocation greater than the chip rate, and since for convenience the efficiency results were given relative to the latter, then for comparison purposes the 0.2 bps/Hz value for ABC should be used. It is seen then that for low values of $S/N_{o_{req'd}}$ that the PN scheme is more efficient, whereas for high values of $S/N_{o_{req'd}}$ it is vice versa.

Now in the case of power efficiency, the peak power, i.e., signal power during the on-time, for ABC must be greater than the average value by the amount of the reciprocal of the duty factor. This means 7 dB for the case cited. Presuming the same baseband modulation/coding, and presuming phase coherence can be maintained from burst-to-burst, then the ABC scheme is less power-efficient than PN by 7 dB.

2.7   PSEUDONOISE TECHNIQUES

2.7.1   PRIMER ON PN MODULATION

The advantages of pseudonoise communications and the reasons for each are summarized below.

- Jamming protection is achieved because all unsynchronized signals are rejected owing to the narrow bandpass of the post-correlation circuits. Since the communicate codes are complex and can be changed at any time by the operator, the difficulty of recreating the spread-spectrum signal and achieving synchronization is apparent.

- Message privacy is assured by modulating the baseband intelligence on the code rather than superimposing it directly on the carrier. The hostile monitoring station is thus required to break the code and synchronize in order to modulate the baseband data.

- The low detectability of the spread-spectrum signal stems from the fact that its total power is distributed over a wide bandwidth, and the concentration of power at any given frequency over this band is far less than that normally associated with a conventional narrowband signal at the same frequency.

- The selective calling capability is an inherent feature, since stations that share the same frequency channel can be called individually (and privately) by using orthoganal codes.

Basically, the pseudonoise wideband signal generated by the transponder is a double-sideband, suppressed-carrier signal centered at the selected RF frequency. This signal is produced by combining carrier with a digital pseudorandom modulating sequence, referred to as a code. The codes consist of various combination of "ones" and "zeros" which occur in what appears to be random order. The pseudorandom modulating voltage has characteristics similar to thermal noise; thus, the spread-spectrum signal is said to be psuedonoise-modulated. Despite its apparent randomness, the code possess a definite structure and is repetitive over a long period of time. The pseudorandom-noise codes are not derived from a noise source but are generated by circuits in the modem.

Figure 2-28 shows the essentials of a pseudonoise system. In the transmitter, the data modulates a carrier in conventional fashion i.e., PSK for digital data.

(a) TRANSMITTER

(b) RECEIVER
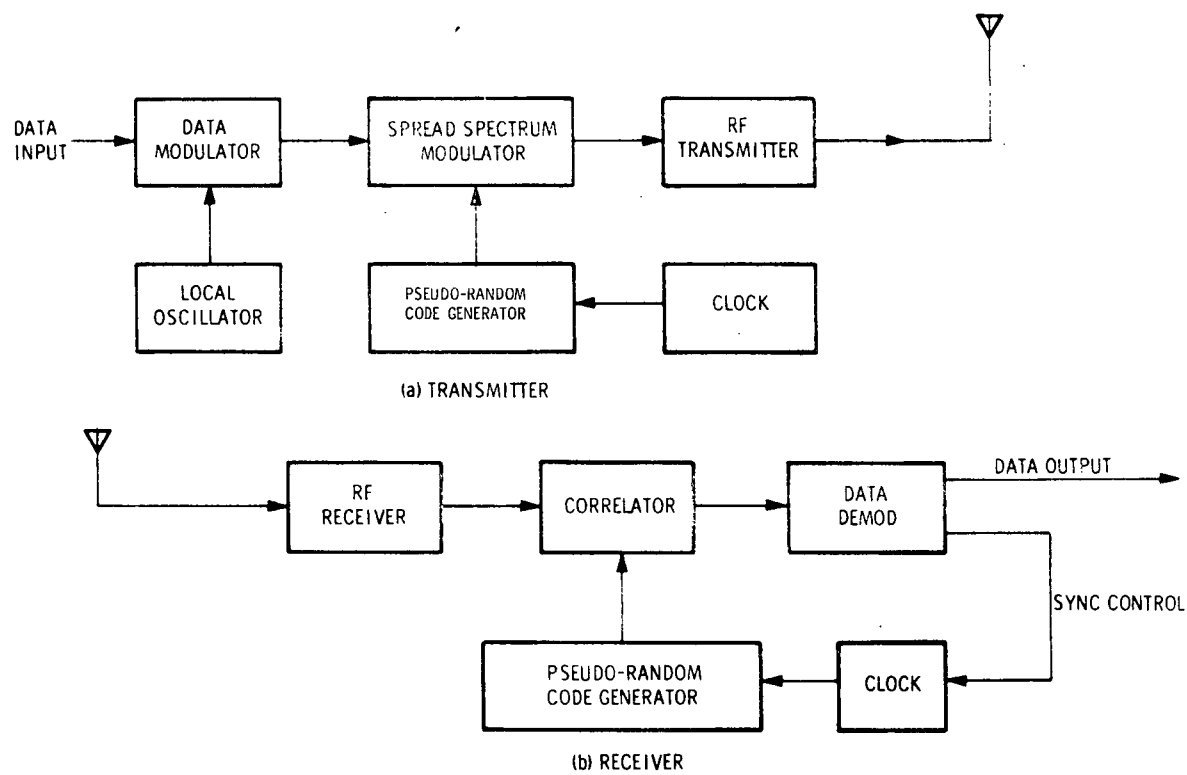
Figure 2-28. Block Diagram, Pseudonoise System

The resulting intelligence modulated carrier is then spread over a wide bandwidth by the pseudorandom code sequence from the code generator and amplified to rf.

If correlation occurs during the synchronization interval, the digital codes associated with the two signals are, in effect, cancelled, leaving a narrowband if. signal which contains only the subcarrier. The bandwidth of the post correlation demodulation circuits is just wide enough to accommodate this signal. If the locally generated code does not match the incoming signal, the power of the wideband received signal is spread over an even wider band. Thus, the received signal is rejected owing to the inconsequential power of the signal in the single narrowband slot.

The receiving system accepts a particular pseudorandom-coded signal and rejects all others, thereby affording substantial jamming protection. This pseudorandom code sequence has a definite time length and is repetitive. The receiving system generates an rf signal modulated with a pseudorandom code identical to that of the received signal. The code of this local signal must be synchronized with the received signal to permit recovery of the modulation signal. The receiver searches for synchronization to determine whether the code being used to modulate the locally generated rf signal is identical to the code in the received signal. This search operation consists of comparing the two signals until correlation is recognized. The synchronization search procedure consists of reducing the frequency of the locally generated code slightly, causing the two signals being compared to undergo a constant displacement in phase. This is equivalent to sliding one coded rf signal past the other.

2.7.2   LINK ESTABLISHMENT IN THE PN MODE

Figure 2-29 shows the sequence of operations performed in both the MMT and MTAR to establish a duplex communications link. The box in the upper left hand corner is the state that the system will be in when the satellite is out of sight of the relay satellite. Whenever the earth blocks the transmission path between the TDRS and the user satellite, both receivers will be out of synch and searching. Since the MMT transmitter (in transponder PN mode) will not be turned on until the MMT receiver is in synch, the sequence of acquiring synch will always be the same.

First, the MMT receiver will search until it synchronizes with the MTAR transmission. Once the MMT verifies the presence of a real synchronization point and not a multipath reflection, the MMT transmitter will be turned and will transmit at a data rate of 100 bits per second and a coder chip rate of 34.1166...kHz. The MTAR receiver which has been continuously searching will eventually achieve correlation

- MMT TX OFF
- BOTH MMT AND MTAR RECEIVERS SEARCHING
- MTAR TRANSMITS NORMAL DATA
- MTAR RECEIVER FORCED TO 100 BITS/SEC DATA RATE

INITIAL CONDITION BLOCK

MMT RECEIVER SYNCH →

- MMT TX ON - TRANSMITS AT 100 BITS/SEC DATA RATE
- MTAR TRANSMITS NORMAL DATA

MTAR RECEIVER SYNCH

- MTAR TRANSMITS LEGENDRE SEQUENCE, THEN RETURNS TO NORMAL DATA TRANSMISSION

MMT DETECTS LEGENDRE SEQUENCE

- SYNCH STATUS IS MONITORED

OUT OF SYNCH

- MTAR SWITCHES TO SELECTED DATA RATE AT THE NEXT CODE REPETITION

MTAR DETECTS BARKER SEQUENCE

- MMT TRANSMITS BARKER SEQUENCE AND THEN SWITCHES TO SELECTED DATA RATE AT THE NEXT CODE REPETITION

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Figure 2-29. Link Establishment Sequence

with the MMT transmission and will verify that it is not locking on a multipath transmission. After this verification from the MTAR will interrupt the normal data stream to send a special sequence to the MMT. The one chosen is a 31 bit Legendre sequence. This sequence simulates the user address and command data that would be sent in a complete TDRS system with many simultaneous users.

Detection of this sequence at the MMT tells the MMT controller that the MTAR is in synch with the MMT's special transmission. The MMT controller now sends a 7 bit Barker sequence back to the MTAR to specify the time to switch from a special acquisition transmission to a regular transmission. This process may seem rather complicated but it is required to provide (1) phase coherent data clocks for differend data rates at each link and (2) reasonable acquisition in the return link which uses a long code to provide multipath rejection and a 1 megachip rate. The conflicting requirements of a long code repetition period to maximize multipath rejection versus a short code length to minimize search time become serious at the highest chip rate. The reason is that the number of chips in a 40msec code repetition time is directly proportional to the chip rate while the time to search for correlation through a code depends solely upon the length of the code and not upon the chip rate of that code.

The 30 to 1 factor in chip rates would mean a 30 fold increase in search time for the return link if the process described above were not used.

After all of the information transfer described above is completed both the MMT and MTAR receiver should be in synch and receiving data from the other end of the link. As long as they stay in synch no further steps are taken. If they drop out of synch a short search will be made to try to reacquire quickly. If that doesn't work the system will revert to the original state in the upper left hand corner of the diagram.

2.7.3   SEARCH STRATEGY FOR MULTIPATH

To provide a practical and implementable acquisition scheme for the multimode transponder which would be compatible with the current TDRS concepts and at the same time provide a reasonable link acquisition time (< 40 sec.) several assumptions were made:

- In a normal mission TDRS handover will occur within ±20 degrees of the horizon.

- Multipath energy for a 5000 Km orbit is approximately 12 dB lower than for a 300 Km orbit.

- Diffuse multipath is not stable and will not cause false lock.

- The relative power contained in the specular component of multipath is reduced about 15 dB at high grazing angles.

Since a multipath signal is always time delayed with respect to the true signal, the strategy for preventing lock to a multipath signal would be to advance the code phase in excess of the worst case multipath (≈40 mS) upon first detecting the presence of a signal and resume search until the local code correlates with the real direct path signal.

The strategy for multipath rejection during a PN acquisition mode will be to shift the local PN code phase backward in time in 1/2 chip steps. Upon detecting the presence of a signal, the code phase will be advanced approximately 2 ms and

backward search will be resumed until correlation has been achieved a second time. This two-step procedure disallows acquisition to a multipath signal within 20° of the horizon, since multipath signals in this region are always delayed 2 mS or less as shown in figure 2-30.
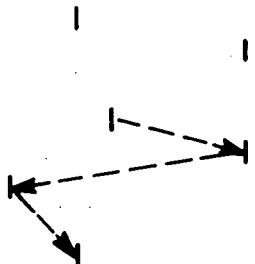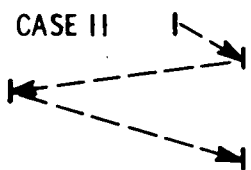
During a PN track mode multipath signals will be rejected because the minimum code length will be 40 which is longer than the greatest multipath delay in the TDRS configuration.

Details of the PN acquisition strategy in the presence of multipath are shown in figure 2-31. Two cases are illustrated: The first is where the local PN replica of the receiver is between the arriving signal and the multipath signal. The second case is where the local signal is ahead of the arriving and multipath signals.
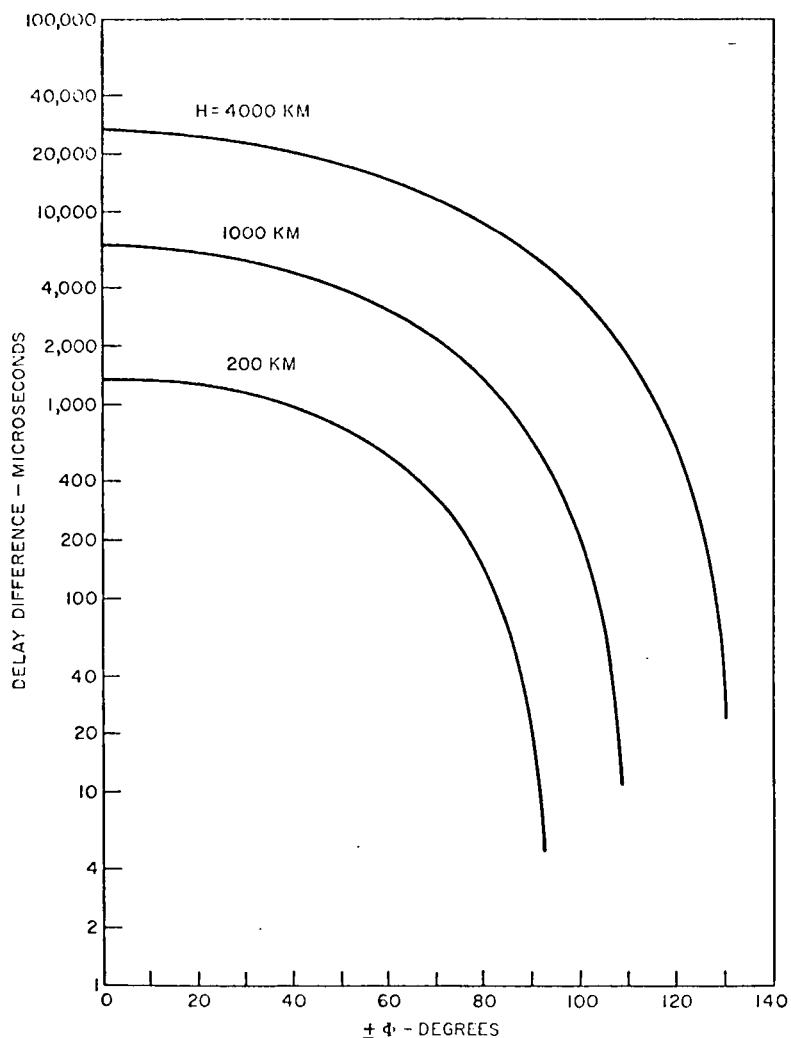
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Figure 2-30.   Multipath Time Delay

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ADVANCE ← CODE PHASE → RETARD	TIME	CODE	COMMENT
	$t_0 - t_3$	ARRIVING	
	$t_0 - t_3$	MULTIPATH	
CASE I	t_0	LOCAL	SEARCH MODE
	t_1	LOCAL	SIGNAL ALARM
	t_2	LOCAL	2 mS RETRACE THEN RESUME SEARCH
	t_3	LOCAL	SIGNAL VERIFY
	$t_0 - t_3$	ARRIVING	
	$t_0 - t_3$	MULTIPATH	
CASE II	t_0	LOCAL	SEARCH MODE
	t_1	LOCAL	SIGNAL ALARM
	t_2	LOCAL	2 mS RETRACE THEN RESUME SEARCH
	t_3	LOCAL	SIGNAL VERIFY

Figure 2-31. Acquisition Strategy in the Presence of Multipath

2.7.4 DIGITAL MATCHED FILTER VS DOPPLER PROCESSOR AS AIDS TO SYNCHRONIZATION

With the progress in fast low power circuitry the digital matched filter as an aid to synchronization to pseudonoise systems has past from the theoretical stage into the laboratory implementation stage. In principle a digital matched filter, as shown in figure 2-32, can be programmed to recognize a specific digital sequence such as a pseudonoise sequence, thus reducing the time required to search to a minimum. Several programs, with support from DOD, are now under way to develop digital matched filters as synchronization aids. However, these programs are still considered exploratory.

The voltage output from a digital matched filter when the input is mistuned in frequency by an amount $\Delta\omega$ is given by

$$\sin\frac{(\Delta\omega\ T/2)}{\Delta\omega\ T/2}$$

where $\Delta\omega$ is the tuning error and T is the matched filter time window or the length of the pseudorandom sequence for which the matched filter is designed. Thus the digital matched filter shown in figure 2-32 rapidly resolves the time ambiguity but must be properly tuned in frequency for optimum performance. The latter requirement can be attained by moving the local oscillator preceding the digital matched filter in incremental steps to perform the necessary frequency search.

Attendent to the frequency losses associated with the digital matched filter for mistuning is the inherent signal suppression loss for deferring interference, i.e., if the interference is Gaussian; a 2 dB suppression can be incurred under poor signal-to-noise conditions. If the interference is CW the suppression can be as high as 6 dB under poor signal-to-interference conditions. The above losses are typical when the digital matched filter uses hard limiting in the input to the digital shift registers. To avoid these suppressions quantization of two or three bit PCM is often used. This increases the complexity associated with the implementation of the digital matched filter since it increases the number of registers by a factor of two or three depending on whether four level or eight level quantization is employed. In some instances an additive dither signal is employed to reduce the suppression losses. This technique also results in a signal to noise loss of about 2 dB.
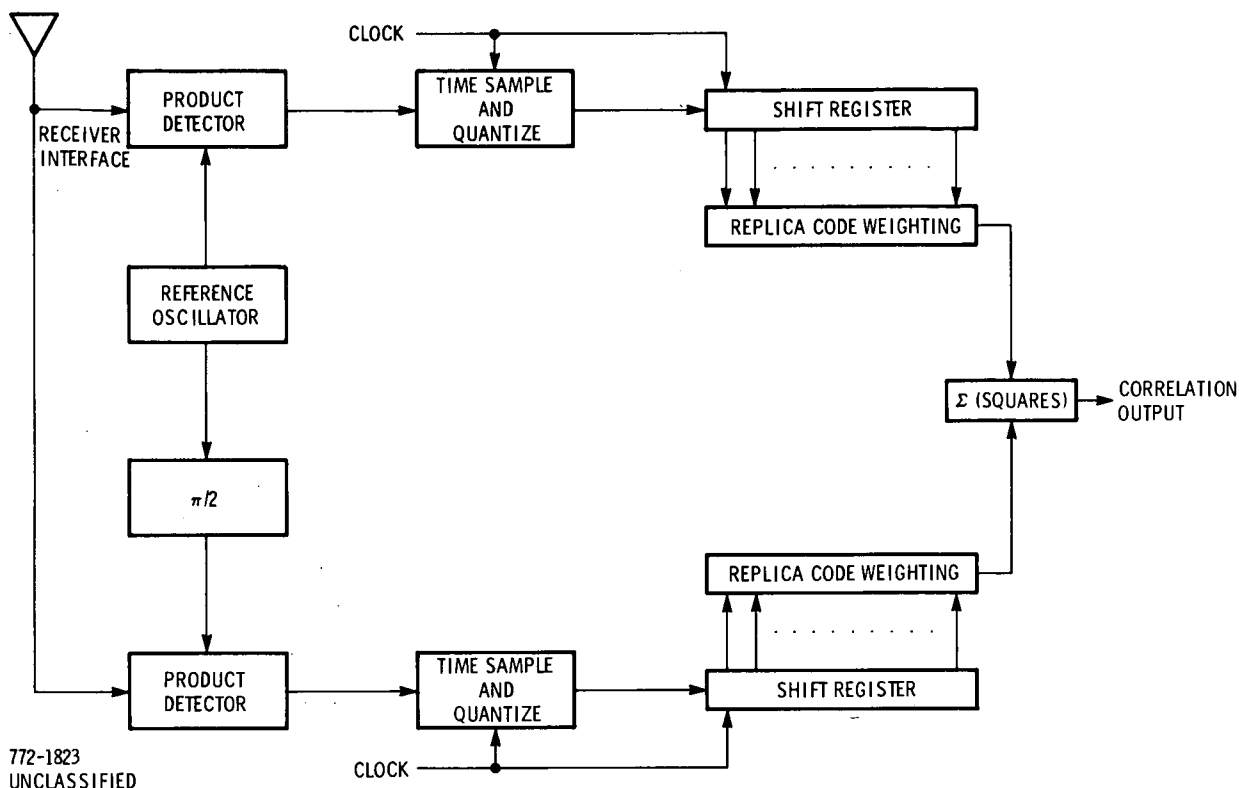
Figure 2-32. Digital Matched Filter for Biphase PN

To avoid these losses and/or complexity an alternate approach to synchronization is advisable. This alternate approach involves an all-digital discrete Fourier transform which minimizes synchronization time resulting from doppler uncertainties. In this case, contrary to the digital matched filter, the time uncertainty is searched in 1/2 chip increments over the pseudonoise code length and for each increment the total doppler uncertainty is searched in real time. A simplified diagram of the real time doppler uncertainty resolver is illustrated in figure 2-33.

The primary advantage of the doppler resolving processor over the digital matched filter is that the doppler resolver can be constructed with off-the-shelf, inexpensive circuitry. Also the doppler processor is universal from the standpoint that any particular unit can be used for synchronizing any number of PN sequences. Shown in figure 2-34 is a summary of the synchronization time for a PN mode where the parameters of interest are the length of the pseudonoise sequence and the data rate.

2-47
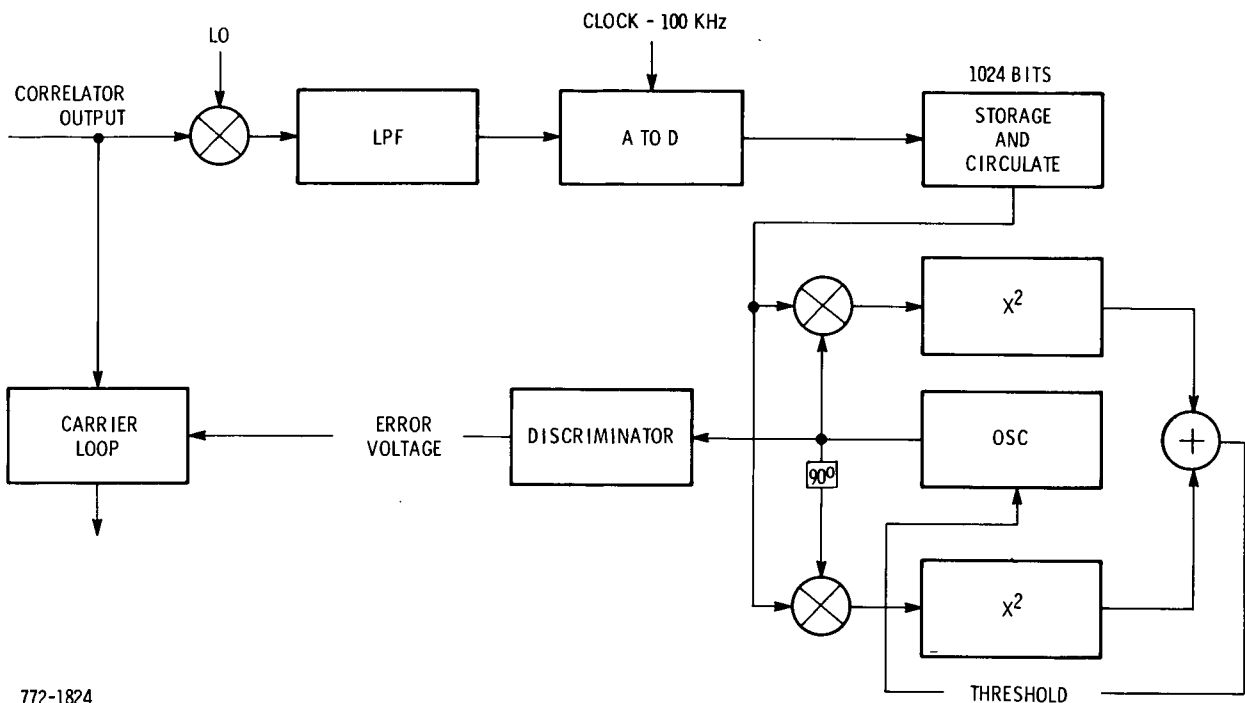
Figure 2-33. Fast Acquisition With Doppler Processor

2.7.5   DOPPLER PROCESSOR DESCRIPTION

2.7.5.1   Theory

It is well known that the optimum detector for a CW pulse of known frequency in Gaussian noise is a matched filter. When the frequency is known only within some range, the best strategy is to employ a number of matched filters, one for each resolvable frequency in the range. A practical digital implementation using this technique was used for mechanization of the doppler resolver.

If the frequency is known, a classical matched filter is optimum for enhancing the signal-to-noise ratio when the signal is accompanied by additive Gaussian noise, prior to envelope detection and decision. By "known" is meant that product of the pulse duration, T, and the frequency uncertainty, W, is less than 1. If the product is on the order of 1, or a little more, then without much loss in the quality of detection, the matched filter may be segmented so that it effectively integrates over n intervals T/n seconds long, such that $WT/n < 1$. Each segment is detected and the n detected values are then added. Thus, some postdetection integration is used in place of predetection integration. As n gets large the process
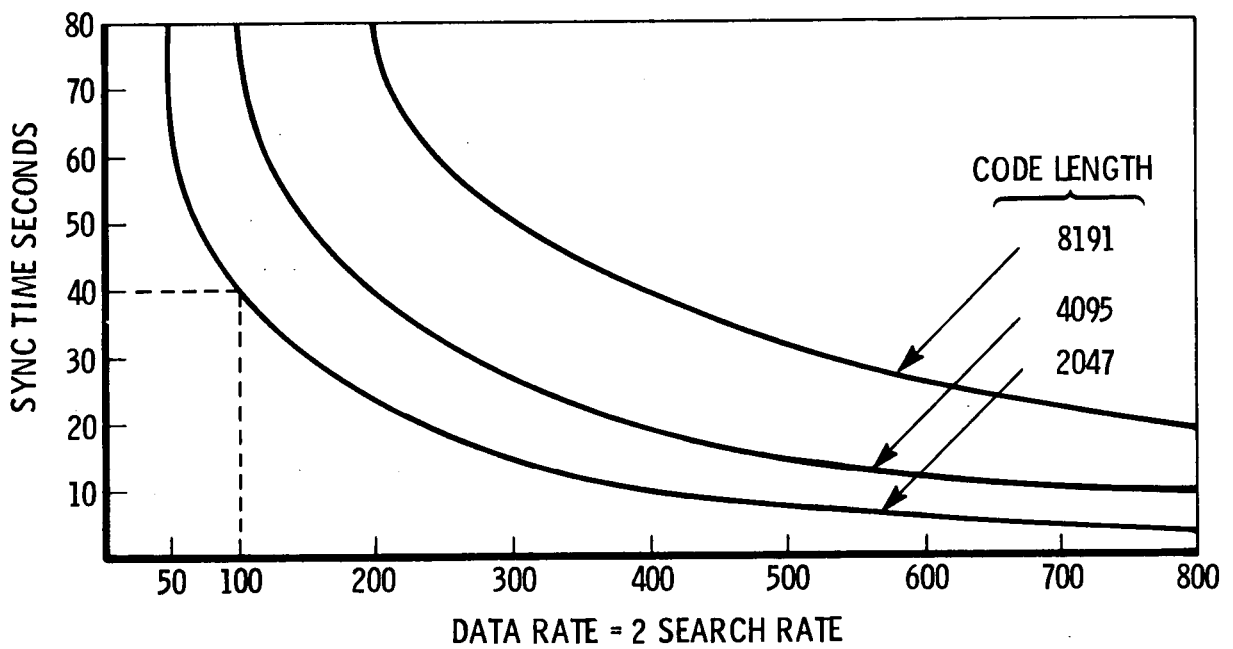
Figure 2-34. PN Synchronization Time

becomes increasingly inefficient. For example, when n = 100, the loss relative to ideal predetection integration (the matched filter) is on the order of 4 to 6 dB.

The superior approach is to provide a set of matched filters, one for each frequency across the uncertainty region at intervals of about 1/T Hz. Thus, the number of filters required is on the order of WT.

The pulse of unknown frequency can be represented as

$$P(t) = A \cos \left[(\omega_c + \omega_a)t + \theta \right] \qquad o < t < T$$

where ω_c is the nominal center frequency and ω_a is unknown, uniformly probable over the range $\pm 2\pi W$. Assume WT to be an integer, M; if necessary by over-estimating W slightly.

The first step in the process is to bandpass filter the signal-plus-noise using a filter of bandwidth 2W centered at $\omega_c/2\pi$ Hz. The principal operation next performed is the computation of the Fourier coefficients of the filtered signal-plus-noise on the interval (O, T). In particular, it is desired to compute the power in each component corresponding to frequencies in the filter passband. These quantities are the values of Cu^2 where

$$Cu = \frac{1}{T} \int_0^T f(t) \exp (-j2\pi n/T) dt$$

for values of n in the region $\dfrac{\omega_c T}{2\pi} \pm WT$.

Alternatively, Cu^2 can be obtained through

$$Cu^2 = a_n{}^2 + b_n{}^2$$

where

$$a_n = \frac{1}{T} \int_0^T f(t) \cos 2\pi nt/T \, dt$$

$$b_n = \frac{1}{T} \int_0^T f(t) \sin 2\pi nt/T \, dt$$

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In the mechanization it is necessary to store f(t) (which is ^{P}(t) + noise) at the filter output. This is conveniently done by resolving f(t) into its quadrature components, sampling and quantizing so that digital memory can be used. The quadrature components of f(t) with respect to a carrier at ω_c are f_c (t) and f_s (t) such that

$$f(t) = f_c(t) \cos \omega_c t + f_s(t) \sin \omega_c t$$

where

$$f_c(t) = A \cos (\omega_a t + \theta) + n_c(t)$$

$$f_s(t) = -A \sin (\omega_a t + \theta) + n_s(t)$$

in which n_c and n_s are independent Gaussian noise processes of zero mean, the same power, both bandlimited to the frequency interval (-W, +W). On the basis of sampling theory, it would be adequate to sample f_c and f_s at the rate of 2W samples per second, however, as a practical matter sampling should be at 3W to 4W samples per second to allow for nonideal filtering and to improve the accuracy of the numerical approximations to the integrals. Call the actual sampling rate R, such that RT is a convenient integer. Amplitude quantization of the samples can be performed as crudely as one bit, however, this entails a loss of nearly 2 dB in output signal-to-noise. The use of 3 bit (8 level) quantization reduces this loss to a few tenths of a dB. The sampled, quantized values of f_c(t) and f_s(t) will be represented by F_c(m/R) and F_s (m/R) where the range of the integer m is 1 to RT corresponding to the range of t: $0 < t \leq T$.

Before writing a final expression for a_n and b_n, it is useful to note certain symmetries in the expressions for values of n spaced equally above and below the midband value, $\omega_c T/2\pi$. To make these evident, let $n = k_c + k$ where k_c $\omega_c T/2\pi$. The range of k which is of interest is $\pm WT$. Making these changes in notation, approximating f_c(t) and f_s(t) by their sampled, quantized counterparts, and approximating the integrals by sums, we obtain:

$$a_{\pm k} = \frac{1}{2RT} \sum_{m=1}^{RT} F_c \left(\frac{m}{R}\right) \cos \frac{2\pi km}{RT} \mp \frac{1}{2RT} \sum_{m=1}^{RT} F_s \left(\frac{m}{R}\right) \sin \frac{2\pi km}{RT}$$

$$b_{\pm k} = \frac{1}{2RT} \sum_{m=1}^{RT} F_s \left(\frac{m}{R}\right) \cos \frac{2\pi km}{RT} \pm \frac{1}{2RT} \sum_{m=1}^{RT} F_c \left(\frac{m}{R}\right) \sin \frac{2\pi km}{RT}$$

Having computed the 2WT pairs of coefficients, a_k and b_k, the 2WT coefficient C_k^2 are formed. Since only one signal is sought, it is the maximum of all the C_k^2 which need be compared to a threshold to make the detection decision. Since the threshold setting should be proportional to the noise power, β is chosen to achieve a given false alarm rate, or a given detection probability for a given signal-to-noise ratio. A complete functional description of the doppler processor is presented in section III.

2.7.5.2   Characteristics

Doppler rates for the forward and return links are shown below:

RF Freq	Doppler Offset
User Satellite 127.750 MHz 149 401	 ± 3.6 kHz ± 4.2 ± 11.5
Ground Station 137 MHz	 ± 7.6 kHz

The doppler processor has been implemented to cover the doppler uncertainty shown above.

Actually the doppler processor has two modes of operation. Although it will operate with all the data rates specified in the forward and returns links, it will demonstrate optimal detection threshold for a 100 and 1000 BPS data rate link as summarized below:

Data Rate	Threshold (C/No)	Doppler Coverage
100 BPS	30 dB	+ 4 KHz
1000 PPS	40 dB	+ 16 KHz

2.7.5.3 PN Acquisition Time

The PN acquisition time is determined by (1) the PN code rate required to provide the necessary processing gain (2) the code length required to provide a nonrepeating code sequence in excess of 40 ms for protection from multipath (3) the signal detection bandwidth constrained by the desired system signal-to-noise threshold for a given data rate (4) the range of doppler uncertainty which must be resolved and (5) the use of diversity channels. A summary of the average acquisition time for the various multimode conditions is summarized in table 2-7.

Table 2-7. PN Acquisition Time

Channel Bandwidth	Diversity Channels	Data Rate	Signal Threshold (C/No.)	Average Acquisition Time
50 kHz	1	100 BPS	30 dB	25 sec.
		1000	40	2.5
	2	100	30	50
		1000	40	5.0
150 kHz	1	100	30	50
		1000	40	5.0
	2	100	30	100
		1000	40	10.0

2.8   VOICE CODING TECHNIQUES

Manned users of TDRS require one or more voice links and an emergency voice link at VHF on an omni-mode. At VHF, where a potential multipath problem exists in the command and return links, a high-quality voice circuit may be difficult to establish. Although the EIRP available for a voice link at VHF or a combination of voice and data links at VHF is 30 dBw per channel from the TDRS; worst-case multipath causes this channel to be processing gain limited. More specifically, even though the high EIRP will guarantee a large desired signal at a manned user spacecraft, the multipath signal will be proportionately large; thus, a requirement exists for a voice coding technique that will provide high intelligibility at low values of C/N_0 in dB-Hz.

A review was made of the state of the art in voice coding techniques to determine the best system available from the standpoint of high intelligibility at minimum C/N_0 values. Table 2-8 compares the two candidate digital voice coding techniques. The table also lists comparative costs, size, weight, power requirements, performance in terms of intelligibility, threshold requirements in terms of dB Hz and other important features such as compatibility with range and range rate signals and antimultipath signals. It is seen from the table that adaptive delta modulation and pulse duration modulation (PDM) are prime candidates when high intelligibility is required at low values of C/N_0.

Relative performance in terms of intelligibility between PDM and adaptive delta modulation is largely a function of the word list used for comparative tests. Using a 50-word, phonetically-balanced word list, both schemes perform to within 1 dB and using a 1000 word phonetically-balanced word list ADM provides a 2 to 3 dB improvement over PDM.

PDM has been implemented in the multimode transponder design as specified by contract. PDM has been previously implemented and tested by MRL, represents no technical risk, and is quite suitable for evaluating coded voice techniques over simulated TDRS forward and return links.

2.8.1   SUPPRESSED CLOCK PULSE DURATION MODULATION

The multimode transponder uses PDM/PSK modulation. This type of modulation permits near-optimum receivers that do not exhibit threshold in the range of operation of interest. The form of PDM is called SCPDM (Suppressed Clock PDM). As developed by MRL, SCPDM allows 100 percent modulation (negligible guard time) and transmits only information transitions by suppressing the clock transitions in the

Table 2-8. Comparison of Voice-Coding Techniques

PARAMETER	Voice Coding Technique	
	PDM	Adaptive Delta Mod
Cost Per Channel ($)	1500	500
Size In. ^{3}	300	VS
Wt. (Lb)	15	VS
Power (Watts)	10	VS
Quality	VG	VG
Intelligibility (PB)	95%	95%
Reliability MTBF	20,000	50,000
Bandwidth	20 kHz	20 kHz
Availability	OTS	OTS
Threshold of Performance	40 dB Hz	44 dB Hz
Multiplex	FTθ	FTθ
Error Cont'l	No	No
Antimultipath	Yes	Yes
R&R	Yes	Yes
Constant Envelope	Yes	Yes

FTθ = Freq − Time − Phase   VS = Very Small
VG = Very Good
OTS = Off-the-Shelf

transmitter. These two features make SC PDM very efficient in terms of modulation theory. Since PDM is a form of pulse time modulation, it is required to sample the information in order to generate the basic pulse train.

Sampling techniques permit transformation of analog signals which are inherently two-dimensional variables, amplitude and time (frequency), into signals of one fixed dimension (sampling rate) and one variable (containing the amplitude information). The minimum sampling rate that permits perfect reconstruction of the analog signal (the Nyquist rate) is twice the highest frequency component of the analog signal. As an illustration, consider an analog spectrum extending to f_c as shown in figure 2-35. If this signal is sampled by multiplying it by unit impulses at a rate of $F = 2f_c$, the resultant spectrum is shown in figure 2-36. It is easily seen that if $f_c > F/2$, the upper and lower sidebands around n x F overlap producing an irresoluble ambiguity.
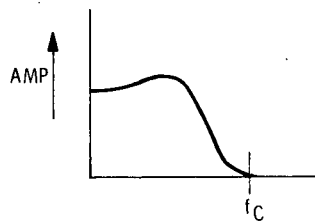
Figure 2-35. Analog Spectrum
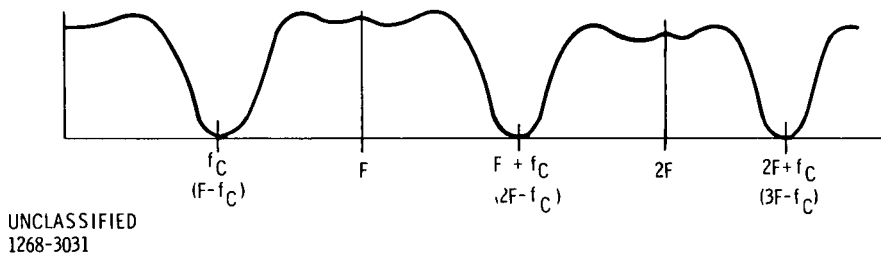
Figure 2-36. Clocked Analog Spectrum

There are two basic modulation schemes associated with the sampled information: One varies a pulse amplitude to represent the sampled analog amplitude, and the other varies pulse timing to represent the analog amplitude. These are shown in figure 2-37.

The first scheme is called pulse amplitude modulation (PAM) and is the most rudimentary. The PAM receiver is a low pass filter. Since pulse amplitudes must be preserved in the RF receivers, PAM is identical to AM. It finds application in power-limited pulsed transmitters. The PAM samples are made narrow and large, and thus tower above the background noise during the "on" time. To realize the advantage, the receiver must be gated coherently.

The second scheme is called pulsed time modulation (PTM). One type of PTM is pulse duration modulation (PDM) or pulse width modulation (PWM). Here the pulse width represents the analog amplitude. It is suited to constant-power

2-56
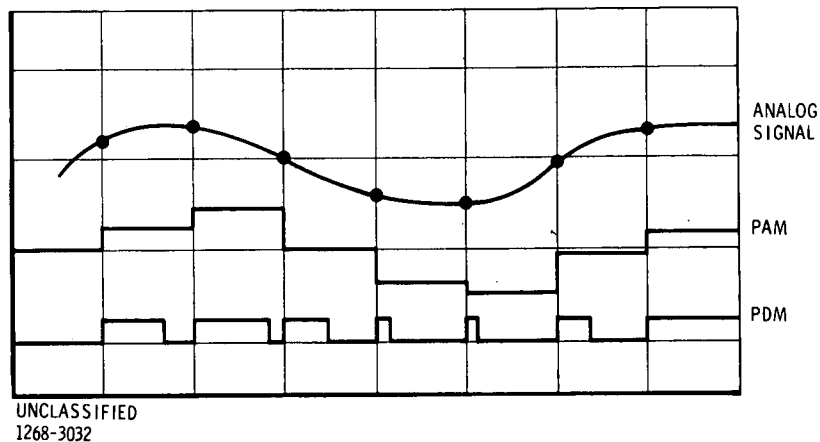
Figure 2-37. Two Types of Modulation for Sampled Information

transmission techniques such as PSK or FSK transmission. Signal recovery is optimized by an "integrate and dump" (I and D) filter following a hard limiter.

Any type of PTM requires a coherent clock. Pulse duration modulation usually uses the leading edge to transmit the clock and the trailing edge to transmit the analog information. An efficient way to receive PDM is to detect the crossovers. However, a more efficient way is to phase-lock a local oscillator to the leading (clock) edge of the samples and recover the samples by an I and D filter.

The technique developed by MRL goes one step further and has a very efficient transmission and recovery technique. The clock crossovers are deleted at the transmitter and are reinserted, essentially noiseless, at the receiver by means of a VCO loop. This halves the bandwidth of the principal sidebands of the transmitted signal, allowing a 3-dB improvement in the tracking of the Costas loop in the modem.

2.9   RANGE AND RANGE RATE MEASUREMENT

2.9.1   FORWARD AND RETURN LINK RANGING

In order to evaluate the impact of the specified chip rates on forward and return link range and range rate accuracies the assumptions of the link power budgets used to evaluate data rate capacities were assumed.

The expression for the RMS range error due to noise can be expressed as, (on a worst case basis):

$$\Delta R_{rms} = \frac{\tau}{5} \frac{C \, T_c}{\sqrt{2 \left(\frac{S}{N}\right)_L}} \qquad \text{2-4}$$

where

$$C \quad = \text{velocity of light}$$

$$T_c \quad = \text{PN chip duration}$$

$$(S/N)_L \quad = \text{code loop SNR} \quad = \left[\frac{C}{N_o} \left(\frac{1}{B_L} \right) \right]$$

$$B_L \quad = \text{the one sided code loop beamwidth}$$

Therefore, either equation (2-2) or (2-3) which is used to evaluate the carrier-to-noise density for the forward and return links respectively can be inserted into equation (2-4) to determine the forward and return link rms range error. Thus, the estimates of range error includes all potential loss, RFI, multipath, other user signals and expected ambient Gaussian noise at the receiver.

In figure 2-38 is presented the forward link rms range error at VHF for 34 and 100 kilochips per sec. The curves at UHF are almost identical. Likewise, figure 2-39 depicts the return link range error at 126 MHz. In all cases range error is compared with RFI density with chip rate as a parameter; other conditions assumed are the same as those (for the forward and return links) in paragraph 2.5, except where noted in the figures.

The range-rate rms error in the forward and return links can be determined from the standard range-rate error equation which has been developed in the Multipath/Modulation Study for the Tracking and Data Relay Satellite,* namely

$$\Delta R_{rms} = \frac{C}{2\sqrt{2\pi} \, T_{ob} \, f_c \, \sqrt{(S/N)_L}} \qquad \text{2-5}$$

where

$$C \quad = \text{velocity of light}$$

$$T_{ob} \quad = \text{observation time}$$

$$f_c \quad = \text{carrier frequency}$$

$$(S/N)_L \quad = \text{carrier tracking loop SNR} \left[= \left(\frac{C}{N_o} \right) \left(\frac{1}{B_{cL}} \right) \right]$$

$$B_{cL} \quad = \text{carrier tracking loop Bandwidth}$$
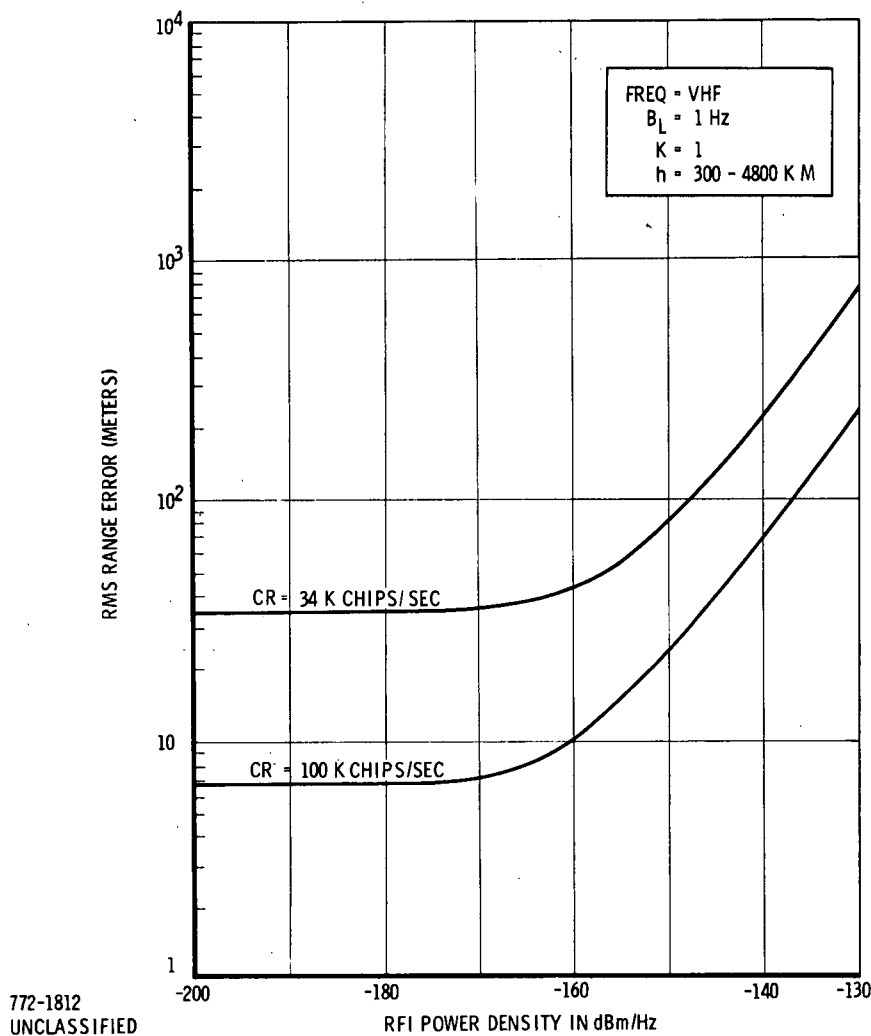
Figure 2-38. Forward Link RMS Range Error vs RFI Power Density at VHF

As in the aforementioned case equations (2-2) or (2-3) are inserted into equation (2-5) to obtain an indication of the expected ΔR for the forward and return link. Presented in figure 2-40 is the expected forward link rms range rate error at UHF. In addition, the range rate error is estimated for the return link (i.e. 136 MHz) and is shown in figure 2-41.

2.9.2   GRARR INTERFACE - PSK

Range measurements with the MMT/MTAR equipment are performed in all modes of operation. An interface was designed to use the Goddard Range and Range Rate system (GRARR) for making range measurements in the ABC and PSK (conventional) modes of operation.

2-59
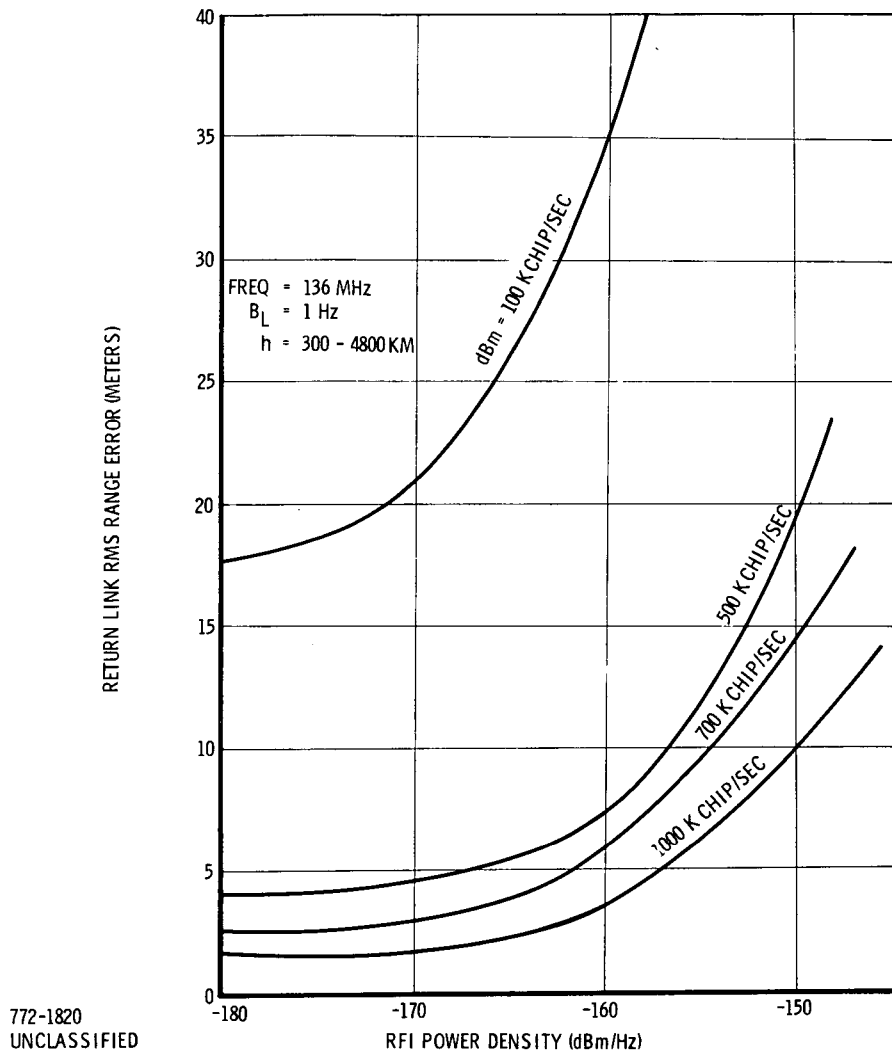
Figure 2-39. Return Link RMS Range Error vs RFI Power Density at 136 MHz

The interface between the MTAR and the GRARR is made at baseband.
The RF portions of the GRARR modulator, transmitter, and receiver are not required
for measurements made in conjunction with the MMT/MTAR equipment. As shown in
figure 2-42 the composite range tone signal from GRARR is converted to a digital
sequence. This digital sequence was calculated to contain equal spectral power for
each of the range tones. The digital simulation is transmitted at a 40 K bit per sec rate.
Normal digital data or PDM voice may be transmitted simultaneously in phase quadra-
ture with the GRARR digital sequence.
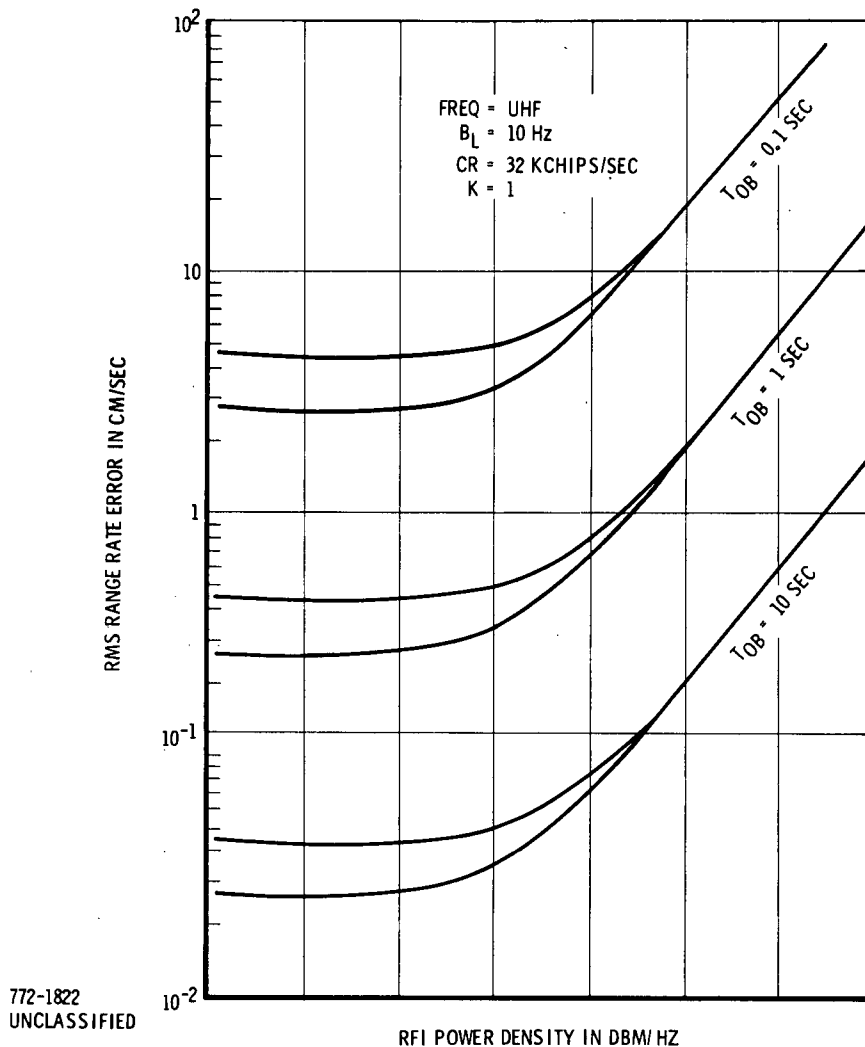
Figure 2-40. Expected Forward Link Range Rate Error at UHF

The MMT receiver detects both command digital data/PDM voice and the GRARR digital sequence. The 40 Kbit/sec GRARR digital sequence goes directly to the MMT transmitter. Normal telemetry digital data or PDM voice may be transmitted simultaneously in phase quadrature with the GRARR sequence.

The MTAR receives and detects the GRARR digital sequence, which goes directly to the GRARR range tone processor. Since the digital sequence was chosen to simulate the amplitude of each range tone, the range tone detection and round trip time measurement functions of GRARR operate normally. Provision is made in the digital simulation circuitry for phase delay adjustment in order to calibrate the system.

FREQUENCY =136 MHz
B_L =10 Hz
K =1

300 KM

T_{dB} = .1 SEC

4000 KM

300 KM

T_{dB} = 1 SEC

4000 KM

300 KM

T_{dB} = 10 SEC

4000 KM

10^{-1}

10^{-2}

10^{-3}

10^{-4}

RMS RANGE RATE (METERS/SEC)

100 200   500   1000

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CHIP RATE IN KCHIP/SEC
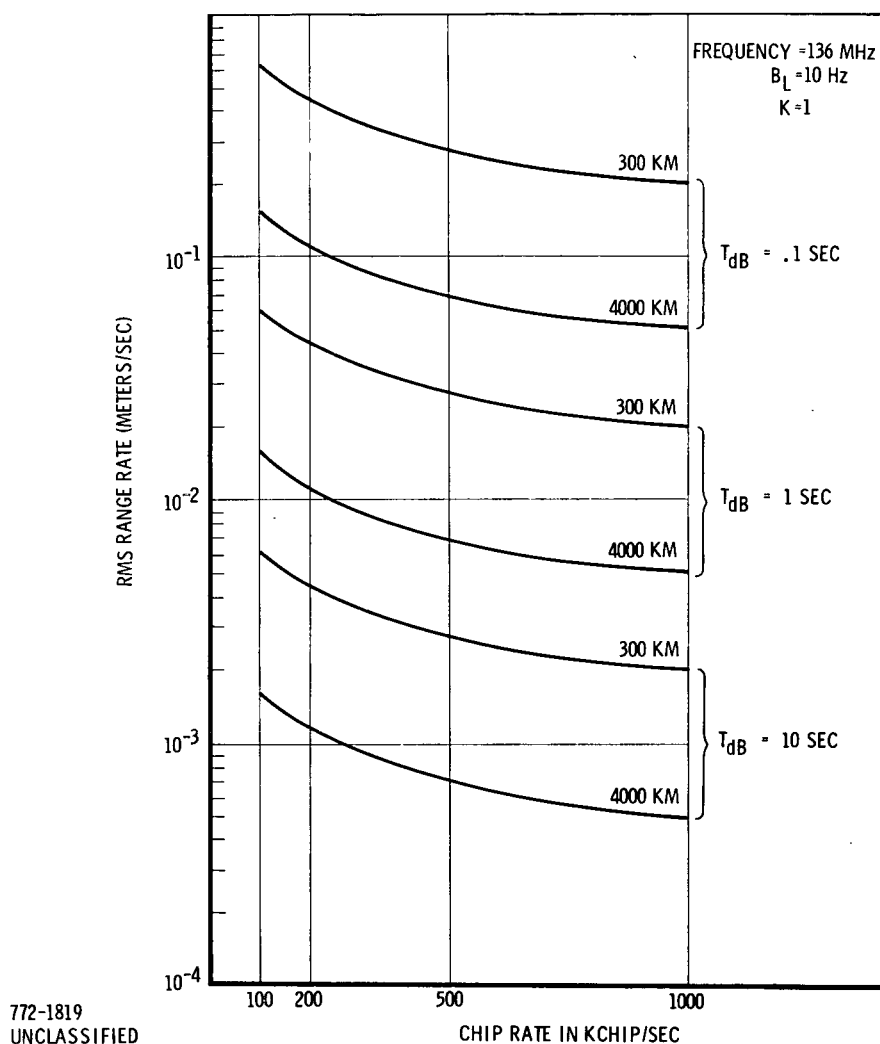
Figure 2-41.   Return Link RMS Range Rate Error at 136 MHz

2.9.3   GRARR INTERFACE - ABC

The possibility of obtaining range and range-rate data in the ABC mode by using the Goddard Range and Range Rate System (GRARR) was first suggested in Reference (1). It was determined during a visit to the Rosman, N. C. STADAN site in 1969 that the bandwidths of the carrier and subcarrier phase locked loops (PLL's) are sufficiently narrow to enable the voltage-controlled oscillator's (VCO's) to flywheel thru the blank intervals of the ABC System. The performance of the GRARR system when employed in the ABC mode was derived in (1) and found to be satisfactory for the Tracking and Data Relay Satellite System. The use of GRARR in conjunction with the ABC mode permits a channelized system which allows frequency sidestepping to avoid RFI.

(1) "Multipath Modulation; Adaptive Techniques", Hekimian Labs. Inc., Final Report
    NAS5-10749, March, 1970.

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```
                     GRARR DIGITAL SEQUENCE
        ┌────────────────────────────────────────┐
        │                                        ▼
  ┌───────────┐                          ┌───────────┐
  │   MMT     │                          │   MMT     │
  │ RECEIVER  │                          │TRANSMITTER│
  └───────────┘                          └───────────┘
        ▲                                      │
        │                                      ▼
  ┌───────────┐                          ┌───────────┐
  │   MTAR    │                          │   MTAR    │
  │TRANSMITTER│                          │ RECEIVER  │
  └───────────┘                          └───────────┘
        ▲                                      │
        │                                      ▼
  ┌───────────┐                          ┌───────────┐
  │  DIGITAL  │                          │  DETECT   │
  │SIMULATION │                          │  GRARR    │
  │           │                          │   DATA    │
  └───────────┘                          └───────────┘
        ▲                                      │
        │                                      ▼
  COMPOSITE TONES                    DIGITAL SEQUENCE TO GRARR
  (FROM GRARR)                       (CONTAINS TONE COMPONENTS)
```

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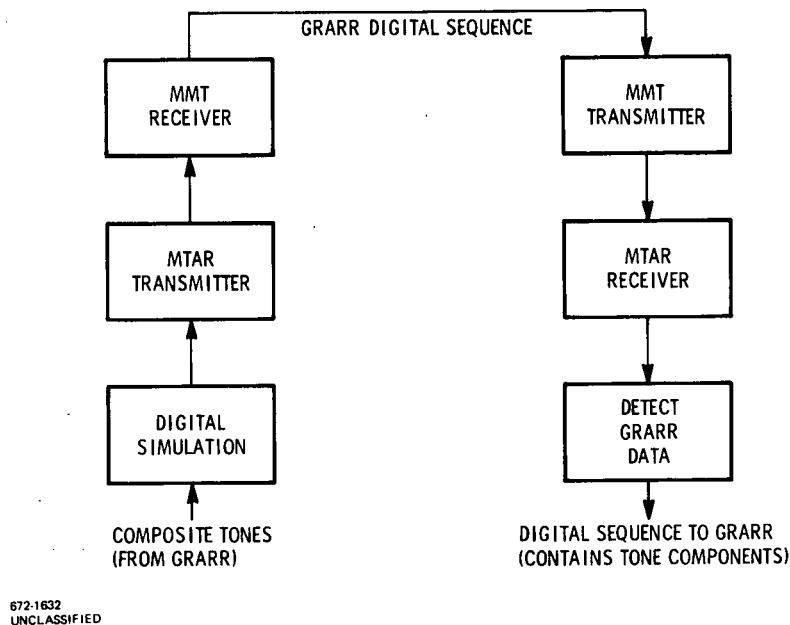
Figure 2-42. GRARR Range Measurement

2.9.3.1   GRARR System

At VHF, the GRARR sidetone ranging technique utilizes tones of 20 kHz, 4 kHz, 800 Hz, 160 Hz, 32 Hz, and 8 Hz. The 20 kHz major sidetone provides resolution and the remaining minor sidetones are used to resolve ambiguities. These tones are phase modulated onto the uplink carrier, translated and modulated onto a subcarrier by the user transponder and retransmitted on the downlink. The subcarrier is not required if a quadrature modulation technique is employed on the down-link to permit simultaneous transmission of data/voice and range information. It should be noted that the ABC System is transparent to either technique. The ground carrier PLL locks to the received carrier and, if the subcarrier technique is used, provides a demodulated subcarrier signal to the subcarrier receiver. The subcarrier receiver locks to this and provides demodulated range tones to the range tone processor.

The range measurement is obtained by determining the time required for the event represented by sidetone phase coincidence to traverse the round-trip distance to the user spacecraft. The range-rate is measured by comparing the uplink and downlink carrier frequencies and recording the number of Doppler cycles per unit time over the counting interval.

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2.9.3.2   GRARR Modifications

The signal aliases introduced by the ABC burst-blank format must be eliminated if proper GRARR operation is to be obtained. This is accomplished by the following modifications:

The signal aliases introduced by the ABC burst-blank format must be eliminated if proper GRARR operation is to be obtained. This is accomplished by the following modifications:

1)   gating and adjunct frequency control of the carrier PLL and the major sidetone PLL; and

2)   gating of the low-pass filtered minor sidetones in the range tone processor; or

3)   gating and reference scaling of the integrator in the Analog-to-Digital Phase Converter.

The choice of (2) or (3) is governed by the bandwidths of the bandpass filters used to reject the low-side output of the 4 kHz balanced mixer in the range tone processor. Gating the minor sidetones is the best solution if the sidetone bandpass filters are narrow enough to reject the nearest possible aliases (± 20 Hz away) and thus provide phase memory during the blank interval. Reference document (2) was examined carefully but provided no indication of the bandwidths in question and therefore it will be necessary to obtain the technical manual for GRARR-2 in order to choose the proper technique.

The design and measured performance of a gated PLL in the presence of noise and a Doppler shifted signal is discussed elsewhere in this report. The design of a frequency discriminator to provide adjunct frequency control to the gated PLL is also presented elsewhere. It is felt that the use of these techniques in conjunction with the GRARR PLL's will enable the recovery of alias-free range and range-rate information and permit use of the entire GRARR signal processor with minimal modification. An example of the ease in modifying the GRARR system is the fact that PLL switching is an integral part of the major sidetone PLL in the present GRARR-2

(2) "Final Project Report for GRARR System Modification", General Dynamics Elect. Div., Contract NAS5-10555, April, 1970.

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system and is controlled by the digital ranging electronics. This is easily adapted to permit PLL burst-blank gating.

2.10   ABC ACQUISITION AND TRACKING CONSIDERATIONS

2.10.1   ADJUNCT FREQUENCY CONTROL LOOP

A frequency control loop is required to prevent the carrier acquisition phase locked loop from locking on a signal alias. The following is a description of a frequency discriminator that generates an error voltage that is proportional to the frequency difference between the incoming signal and the carrier PLL. This is accomplished by comparing the two frequencies during the burst interval.

Given a basic VCO frequency of 5 MHz, and a burst interval of 10 ms, the total number of counts per burst is expressed by:

$$(5 \times 10^6 + 100)(10 \times 10^{-3}) = 5 \times 10^4 + 1$$

where 5×10^6 is the nominal VCO frequency, 100 Hz is the worst-case alias from the frequency discriminator standpoint, and 10×10^{-3} is the burst interval. When the burst interval is 2 ms, the counts per burst remain the same as shown by:

$$(5 \times 10^6 + 500)(2 \times 10^{-3}) = 5 \times 10^4 + 1$$

where 500 Hz is the worst-case alias for this burst interval.

The variation in counts per burst in each case is ± 1 count. In order to get adequate error resolution, many bursts may be accumulated before evaluating the frequency error. A 7-bit counter is employed to count 128 bursts before comparing the input frequencies.

Referring to the diagram of the frequency control loop in Figure 2-43 (not included in the design data package) note that the reference VCO input and the signal input are gated and applied to two 8-bit counters. Each counter output is connected to a digital-to-analog converter. The accumulated count at the end of each 128 burst period is compared in an analog comparator and strobed into a storage capacitor by a FET switch at the conclusion of the interval. Each burst count interval is determined by processing the input burst in a programmable one-shot. The period of the one-shot is varied by adjusting the charging current on the timing capacitor through a constant-current source composed of the PNP transistor and the variable base-voltage source decoded from the input information. The programmable one-shot yields a burst period that is approximately 1 ms less than the total input

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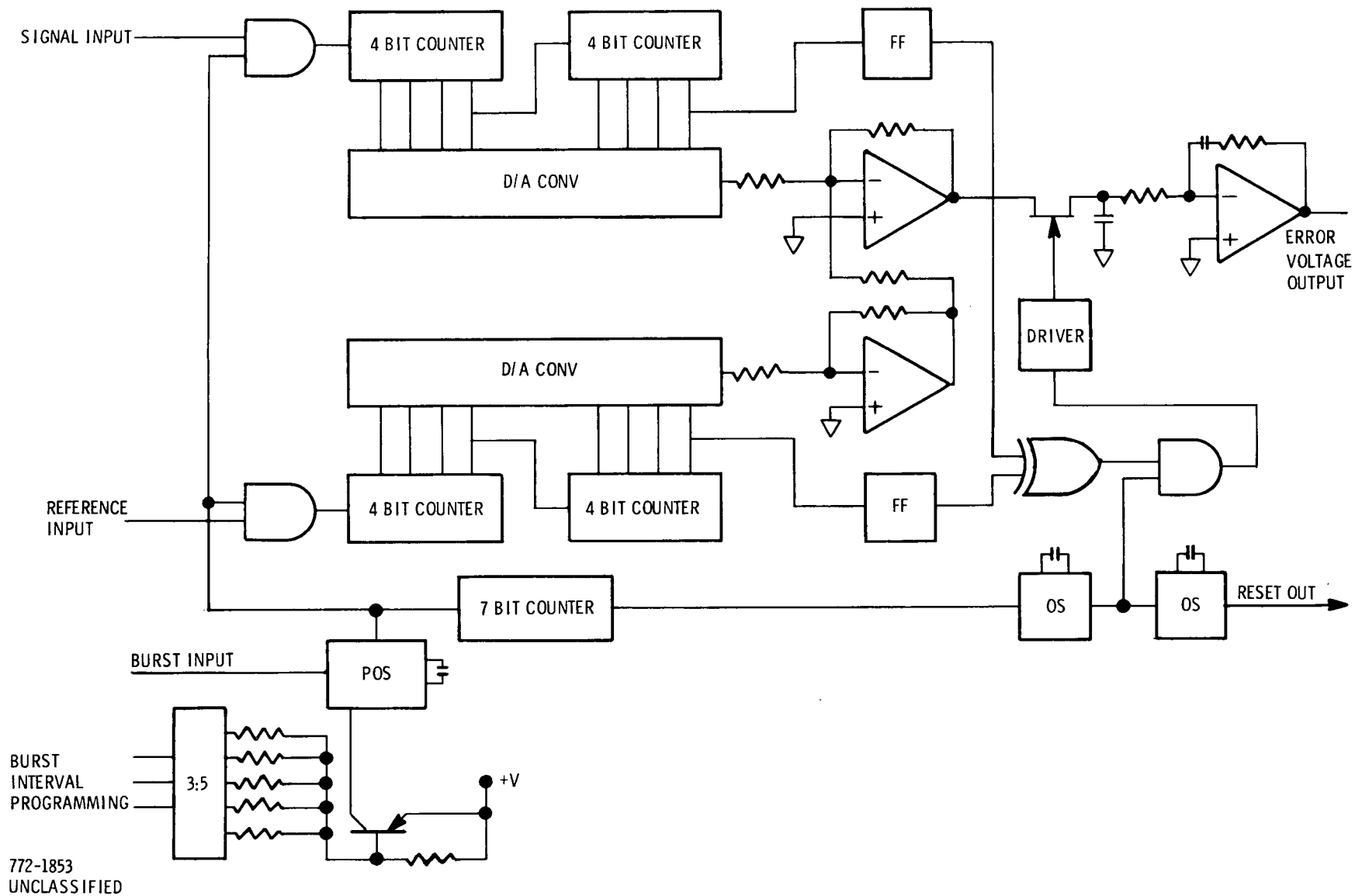
Figure 2-43. Proposed Frequency Discriminator

burst. To accumulate the desired number of burst cycles, two 4-bit counters are arranged to toggle a one-shot every 256 input bursts. The one-shot, through a level translator, drives the FET switch. After the information is dumped into the storage capacitor, another one-shot resets the counters and the system is ready for the next cycle. The error voltage from the storage capacitor is then fed to the carrier PLL and forces the loop to lock onto the carrier and not one of the carrier aliases. An analysis of the carrier PLL with the adjacent frequency control was not performed.

2.10.2   ACQUISITION AND TRACKING

The design of a gated PLL to acquire and track the Doppler-shifted carrier component in the presence of noise is an interesting problem, due to the theoretical complexity of a gated PLL.

It is possible to calculate the steady-state phase error of a continuous PLL when locked onto a noise-free, doppler-shifted signal and it is also possible to determine the pull-in range for the same situation in terms of the Doppler rate. The steady-state phase error due to a doppler rate of 4.5 Hz per sec is less than 0.03 radians and the pull-in range is greater than 100 Hz. These results are for a 2nd-order noise-free PLL with a perfect integrator, a damping factor of 0.707, and a natural frequency of 5 Hz. It should be noted for comparison purposes that the -3 dB frequency is identical to the natural frequency when the loop damping factor is equal to 0.707. The noise bandwidth is 33 Hz.

At the other extreme, it is also possible to determine the stability criterion for an instantaneous sampled noise-free PLL. This is of interest since the sampled PLL is a worst-case example of a gated PLL. It is shown in appendix B that a sampled 2nd-order PLL with a perfect integrator, a damping factor of 0.707, and a natural frequency of 5 Hz, will be stable if the sampling frequency is greater than 10.6 Hz. The lowest sampling frequency encountered in the ABC system is 20 Hz which corresponds to the longest burst format. Therefore, the PLL sampled at 20 Hz would always be stable.

Though the limit cases of a continuous PLL and an instantaneous sampled PLL can be analyzed mathematically to a useful degree, the actual case of a 20 percent gated PLL poses almost insurmountable analytical problems. Further, the presence of noise in the real case indicated that a satisfactory answer could be obtained only by the use of the ultimate analog computer, namely a functioning, real-life circuit, as shown in the form of a block diagram in figure 2-44.

VCXO → RF SWITCH → SUMMING AMPLIFIER → TO RMS METER → PHASE DETECTOR → SWITCH & LOOP FILTER

RAMP GENERATOR

BURST GATE GENERATOR

BANDPASS FILTER

CONTROLLED VCXO

NOISE INPUT
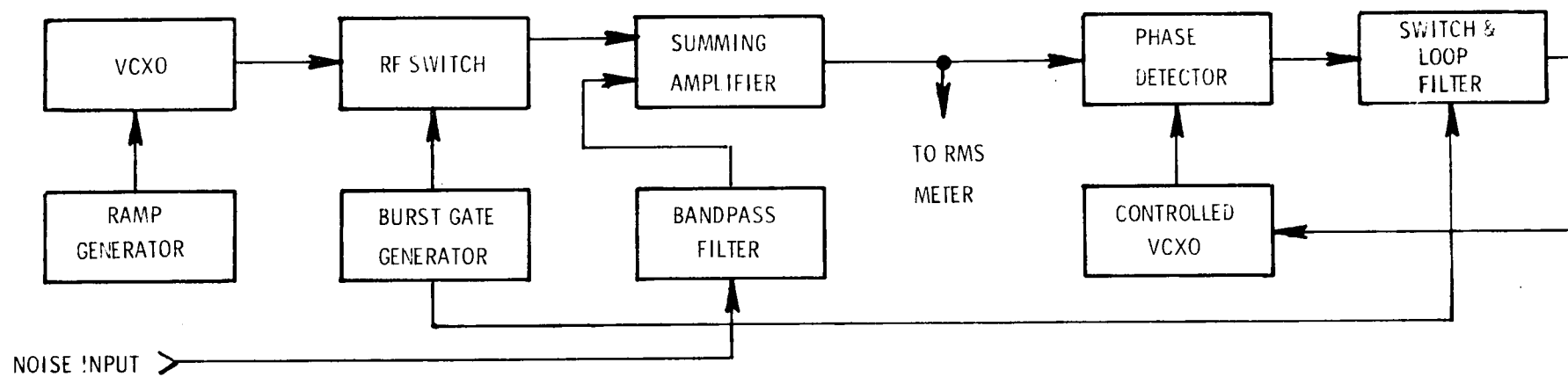
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Figure 2-44.   Gated PLL Breadboard, Block Diagram

Since all of the above calculations indicated that a stable and precise carrier PLL could be realized, it was decided to build a PLL for demonstration purposes.

Figure 2-44 is a block diagram of the entire system operated at a nominal frequency of 3101 kHz. The bursted RF generator consists of a voltage-controlled crystal oscillator, an RF switch, and a summing network which combines band-limited noise from the noise generator with the gated RF signal. The burst-gate generator provides a 20 percent duty cycle gate; the ramp generator output shifts the voltage-controlled crystal oscillator (VCXO) at a 6 Hz per sec rate to synthesize Doppler in the bursted signal.

The loop gain and loop filter were adjusted to provide a PLL natural frequency of 5 Hz and a damping factor of 0.707. The two-sided noise bandwidth for this loop is $6.67 f_n = 33$ Hz.

The measured PLL threshold signal-to-noise ratio was -21 dB in a 60 KHz noise bandwidth in the presence of a Doppler rate of 6 Hz per sec. Since the bandwidth improvement factor is $10 \log (60,000/33) \simeq 33$ dB, the threshold signal-to-noise ratio in the PLL bandwidth is $-21 + 33 = 12$ dB. The results are summarized in table 2-10.

2.10.3   ACQUISITION TIME

The ABC portion of both the MMT and the MTAR accepts baseband information and derives a data clock and a burst gate.

The data clock is regenerated by a second-order phase-locked loop (Pll) whose bandwidth is restricted sufficiently to prevent locking onto an alias of the bit rate. This is possible since the carrier PLL tracks the carrier Doppler and the differential Doppler remaining on the baseband data will be less than one part in 20,000. That is, the frequency uncertainity of the worst-case five-times faster PDM will be less than 11 Hz. The frequency spacing to the nearest possible alias will be 20 Hz and therefore it is feasible to lock the PLL onto the correct component.

If the natural frequency of the bit-clock-recovery second-order PLL is 1 Hz, reference to (3) yields the fact that the pull-in time will be about 3 seconds. This pull-in time is based upon a noise-free situation which is closely approximated since the PLL bandwidth of 1 Hz is two orders-of-magnitude less than the smallest data bandwidth in which the usable signal-to-noise ratio must be greater than 10 dB.

Table 2-9. Gated PLL Breadboard Specifications

Specification	Performance
Loop Natural Frequency	5 Hz
Loop Damping Factor	0.707
Pull-In Range Without Noise Or Doppler	>500 Hz
Pull-In Range With Doppler Alone	>200 Hz
PLL Threshold (S/N) With Doppler	12 dB
Pull-In Range With (S/N) = 12 dB and Doppler	>100 Hz
PLL Phase Error With 12 dB S/N And Doppler	<20° RMS
Center Frequency	3101.0 kHz
VCXO Range	3100.4 to 3101.6 kHz
Burst-Blank Duty Cycle	20%
Burst Interval	10 MSEC
Bursted RF Level (Measured by RMS Meter)	-37 dBm
Filtered Noise Bandwidth	60 kHz
Noise Amplitude	Adjustable
Doppler Rate	6 Hz/Sec

The bursted RF generator consists of a voltage-controlled crystal oscillator, an RF switch, and a summing network which combines band-limited noise from the noise generator with the gated RF signal. The burst gate generator provides a 20 percent duty cycle gate; the ramp generator output shifts the voltage-controlled crystal oscillator (VCXO) at a 6 Hz per sec rate to synthesize doppler in the bursted signal.

The loop gain and loop filter were adjusted to provide a PLL natural frequency of 5 Hz and a damping factor of 0.707. The two-sided noise bandwidth for this loop is $6.67 f_n = 33$ Hz.

The measured PLL threshold signal-to-noise ratio was -21 dB in a 60 kHz noise bandwidth in the presence of a doppler rate of 6 Hz per sec. Since the bandwidth improvement factor is $10 \log \left(\frac{60,000}{33} \right) \simeq 33$ dB, the threshold signal-to-noise ratio in the PLL bandwidth is -21 + 33 = 12 dB. The results are summarized in table 2-10.

2.10.4   ZONE OF COVERAGE

The Adaptive Burst Communication (ABC) system transmits data in bursts of a duration such that the delayed multipath return does not overlap the direct path signal. Time-gating is then used to provide complete immunity to the earth-reflected multipath return and thus reduce the DRSS multipath to a simple line-of-sight path. This immunity is achieved by choosing the burst duration to be slightly less than the minimum path length time difference (PLTD) encountered during an orbit. The ABC System is called adaptive due to the fact that the burst duration employed for a given user is a function of the altitude of the user.

The maximum burst duration will be equal to the minimum PLTD for a given user altitude. This is necessary to prevent overlap of the direct and multipath signals a burst duration that permits an integral number of bits per burst. Therefore, the lowest data rate determines the minimum burst duration. It should be noted that decreased burst durations are permissible if super-sampling is employed. If the lowest thruput data rate was equal to 200 bps, the data rate during the burst would be 1000 bps for a 20 percent duty cycle format and the minimum burst duration would be 1 ms. On this basis, users having circular orbit altitudes from 500 to 5000 km can be serviced with a fixed 20 percent duty cycle format.

The length of the interval between bursts is determined by the maximum PLTD for a given user altitude and the amount of multipath spreading that occurs. The maximum PLTD will occur when a relay is directly above a user and will be 3.3 ms for a user at 500 km, and 33 ms for a 5000 km user. A user at 5000 km employing a 10 ms burst duration will receive a negligible amount of multipath if the next burst is 40 ms after the direct path burst. The mean reflected power at a 500 km user will be more than 30 dB below the direct path power at the time corresponding to the reception of the next direct path burst, if a 4 ms inter-burst interval is employed.

The zone of coverage for an ABC System employing a 20 percent duty cycle format will be determined by the minimum PLTD for a given user altitude. For example, a user at 5000 km can be serviced out to an earth-referenced angle of 90 degrees from a data relay satellite if the burst duration is 10 ms. However, 5000 km user positions which result in values of PLTD less than 10 ms will not be covered.

The shaded area in figure 2-45 indicates the region not covered by a 20 percent duty cycle ABC System. Thus, the ABC System provides more than 8 80 percent coverage of the region between 500 km and 5000 km when the TDRS configuration consists of two relay satellites with 130 degrees spacing.

2-71

REGION NOT COVERED BY PN MODE

REGION NOT COVERED BY 20% DUTY CYCLE ABC SYSTEM

5000 KM

88°

50°

30°

500 KM

EARTH SURFACE

130°

RELAY (33.75 CM FROM EARTH CENTER)

RELAY (33.75 CM FROM EARTH CENTER)

SCALE: 1 CM = 1.25X10^6 METERS
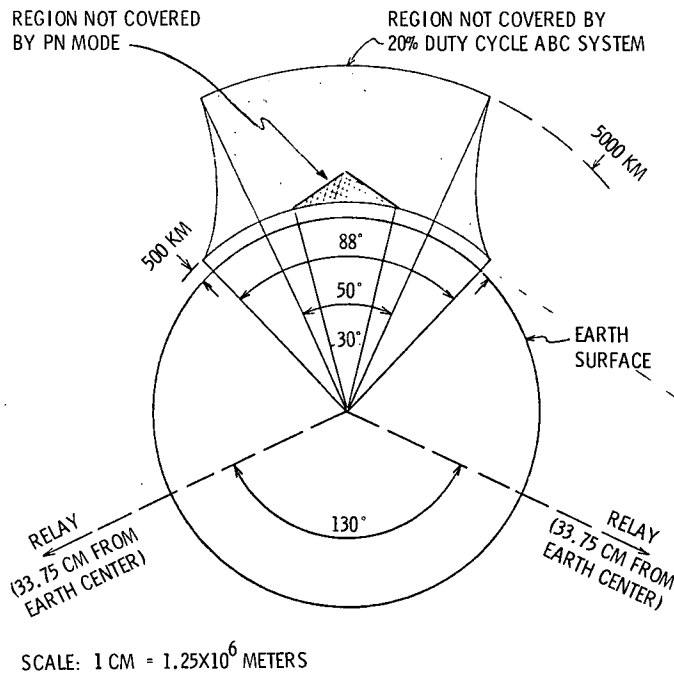
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Figure 2-45. Regions Unprotected from Multipath

2.11   TDRS USER TRANSPONDER - SIZE, WEIGHT, AND POWER CONSIDERATIONS

2.11.1   SUMMARY

Four candidate modulation techniques which are being considered for use in the TDRS User Transponder design are listed below:

- Conventional PSK
- Pseudonoise
- Adaptive Burst Communications
- Frequency Agility

This section presents a summary of the size, weight, power, and cost considerations for transponders using these modulation techniques.

Some assumptions were made to form a basis for comparing the different modulation techniques. They are:

- 1974 Technology
- Spaceborne Equipment

2-72

- No Secondary Power Supply Included
- Cos/Mos Logic
- No Custom Hybrids
- No Radiation Hardening

This section presents size and power estimates for current modulation techniques. In addition, size, and weight estimates are given for a PN transponder using 1977 technology hardware and custom hybrids.

Recurring and non-recurring costs for a space qualified transponder will vary considerably. Costs will depend on the equipment qualification requirements and on the (1) mechanical and (2) electrical specifications which will be imposed on the transponder design.

The conventional PSK equipment contains a group of assemblies which are common to each modulation technique. This equipment configuration includes a diplexer, transmitter, receiver, and modem. It contains provision for both data and voice modes of operation with no range or range-rate capability.

2.11.2   CONVENTIONAL PSK MODULATION

A list of the assemblies required for a user satellite transponder is shown in table 2-10. An EIRP of 5 watts is assumed for the power amplifier. The equipment provides data and voice processing for both the forward and return links. The transponder design will occupy 250 cubic inches and will weigh approximately 8 pounds with a primary power requirement of 5 watts.

Table 2-10. Size and Power - Conventional PSK

Assembly	Size (in^3)	Power (watts)
RF/IF Assembly	30	1
RCVR L.O. Synthesizer	30	2
Costas Demodulator	45	3
Data Processor	15	1
PDM Voice	30	2
Modulator	30	2
XMTR L.O. Synthesizer	30	2
RF Power Amplifier (37 dBm)	150	15
Diplexer	25	-
TOTAL	385	28

2.11.3 PSEUDONOISE MODULATION

A transponder implemented to provide PN-PSK modulation requires the assemblies shown in table 2-11. The unique assemblies required in addition to the assemblies for conventional PSK are:

- Local Reference/Correlators
- PN Coder Clock
- Controller
- Doppler Resolver

These assemblies generate and correlate the PN sequence and resolve the large Doppler uncertainty for rapid acquisition. This equipment configuration provides data and voice processing in both the forward and return links and in addition provides

Table 2-11. Size and Power – Pseudonoise Modulation

Assembly	Size (in^3)	Power (watts)
Basic Configuration		
RF/IF Assembly	30	1
RCVR L.O. Synthesizer	30	2
Costas Demodulator	45	3
Data Processor	15	1
PDM Voice	30	2
Modulator	30	2
XMTR L.O. Synthesizer	30	2
RF Power Amplifier (37 dBm)	150	15
Diplexer	25	–
SUB TOTAL	385	28
Unique Assemblies		
Local Reference/Correlator	30	1
PN Coder/Clock	15	1
Controller	15	1
Doppler Resolver	15	2
TOTAL	460	33

a range and range-rate measurement capability. This transponder requires a volume of 460 cubic inches and weighs 10 pounds with a primary power requirement of 33 watts.

2.11.4   ABC MODULATION

A transponder implemented to provide adaptive burst communications requires the assemblies listed in table 2-12. It is estimated that the unique assemblies required in addition to the assemblies for conventional PSK are:

- ABC Controller
- PDM/Binary Converter
- Acquisition Logic
- Adjunct Frequency Control
- GRARR Transponder

Table 2-12.   Size and Power – ABC Modulation

Assembly	Size (in^3)	Power (watts)
Basic Configuration		
RF/IF Assembly	30	1
RCVR L.O. Synthesizer	30	2
Costas Demodulator	45	3
Data Processor	15	1
PDM Voice	30	2
Modulator	30	2
XMTR L.O. Synthesizer	30	2
RF Power Amplifier (37 dBm)	150	15
Diplexer	25	–
SUB TOTAL	385	28
Unique Assemblies		
ABC Controller	15	1
PDM/Binary Converter	15	1
Acquisition Logic	15	1
Adjunct Frequency Control	30	2
GRARR Transponder	30	2
TOTAL	490	35

Even though the current ABC implementation requires seven printed circuit board assemblies, it is estimated that a mechanical redesign would reduce the required volume and unique printed circuit board assemblies. The power, size, and weight requirements for unique ABC assemblies are tabulated below:

ABC	Power	Size	Weight
TTL Design	25 watts	156 cubic inches	2.7 pounds
CMOS Design	2.7 watts	156 cubic inches	2.7 pounds

With the addition of an adjunct frequency control and GRARR transponder, it is estimated that the size, weight, and power requirements for this transponder design is 490 cubic inches, 11 pounds and 35 watts, respectively.

2.11.5   FREQUENCY AGILITY

To provide frequency agility four additional assemblies will be required as listed in table 2-13. These assemblies would provide dual receiver channels,

Table 2-13. Size and Power - Frequency Agility

Assembly	Size (in^3)	Power (watts)
Basic Configuration		
RF/IF Assembly	30	1
RCVR L.O. Synthesizer	30	2
Costas Demodulator	45	3
Data Processor	15	1
PDM Voice	30	2
Modulator	30	2
XMTR L.O. Synthesizer	30	2
RF Power Amplifier (37 dBm)	150	15
Diplexer	25	-
SUB TOTAL	385	28
Unique Assemblies		
RF/IF Assembly - No. 2	30	1
Costas Demodulator - No. 2	45	3
Diversity Combiner	15	1
GRARR Transponder	30	1
TOTAL	505	34

a signal combiner and a range capability. It is estimated that this transponder will require 505 cubic inches of volume and weigh 12 pounds with a primary power requirement of 34 watts.

2.11.6 PSEUDONOISE USING 1977 TECHNOLOGY

Table 2-14 shows the anticipated equipment configuration for a pseudonoise transponder using hardware which will be available in 1977. Full advantage would be taken of low power logic, custom hybrid circuits, and standard LS1 circuits. The anticipated design would require 250 cubic inches and 25 watts of primary power.

Table 2-14. Size and Power – Pseudonoise Modulation
Using 1977 Technology

RECEIVER	Size (IN^3)	Power (Watts)
UHF/IF Assy.	30	0.5
RF Synthesizer	10	1.5
Local Ref./Correlator	10	0.5
Synchronous Demodulator	15	1.5
Doppler Resolver	15	2
PDM Voice	10	1
Controller	10	0.5
PN Coder/Clock/Data Processor	10	0.5
	110	9
TRANSMITTER		
Transmitter (37 dBm – EIRP)	100	15
Modulator/Up-Converter	10	1
Diplexer	30	–
	140	16

2.12 COMPARISON OF MODULATION TECHNIQUES

- Conventional PSK
- Pseudonoise
- Adaptive Burst Communications

Comparisons are made in tables 2-15 through 2-17 on the basis of advantages and disadvantages for each technique, since many of the performance parameters do not lend themselves for comparison for all three modulation techniques.

Table 2-15. Performance Parameters - Conventional PSK

Advantages	Disadvantages
• Relatively simple to implement (compared to PN or ABC)	• Requires coherent detection
• More reliable due to simplicity than PN or ABC	• Multipath sensitive
• Less cost due to less hardware over PN or ABC	• Attainable data quality limited by EIRP of transmitter
• Theory and implementation well established	• Sensitive to system phase distortion (TWT AM/PM conversion, etc., oscillator instability, etc.)
• Optimal system in an additive Gaussian channel such as the space medium	• No inherent range and range rate
• Allows use of saturated amplifiers thereby giving higher system efficiency	
• Uses channel bandwidth reasonably well	
• Channelization possible to avoid interference	

Table 2-16. Performance Parameters - Pseudonoise Modulation

Advantages	Disadvantages
• Multipath rejection properties	• Requires more channel bandwidth than PSK or ABC.
• RFI rejection properties	• Requires code coherence at the receiver
• Available for ranging if needed	• Requires coherent detection of data as PSK
• Encoding implementation trivial; decoding requires little added complexity	• Sensitive to system phase distortion
• Still allows use of saturated amplifiers as in PSK	• Data quality limited by transmitter EIRP in the thermal noise case (no RFI, multipath, etc.)
• End to end system is transparent and so is again optimal on the space channel	• Added system cost over PSK
• Code diversity possible	• Sensitive to PN timing problem
• Theory and implementation well established	• Catastrophic failure possible if PN can't lock-up
	• No channelization possible to avoid interference

Table 2-17. Performance Parameters - Adaptive Burst Communication

Advantages	Disadvantages
● Multipath rejection	● Timing (Burst) sensitive
● Simplicity in theory	● Relatively complex to implement
● Optimal system for an equivalent PSK E_b/N_o	● More cost over PSK
● Efficient utilization of channel bandwidth	● If EIRP is limited, the data quality is degraded due to duty cycle
● Channelization possible to avoid interference	● Excessive dwell period for low grazing angles
● Allows use of saturated amplifiers	● RFI sensitive
	● Requires enough system memory to keep carrier loops locked during dwell period
	● Requires coherent detection of data as PSK
	● Sensitive to system phase distortion
	● In a low multipath signal environment it is equivalent to PSK
	● Catastrophic failure possible if ABC timing is lost
	● No inherent range and range rate

SECTION III

FUNCTIONAL DESCRIPTION

3.1 SYSTEM DESCRIPTION

This section includes functional descriptions of both the MMT (airborne unit) and the MTAR (ground unit). The MMT functions as a coherent transponder with the transmit carrier frequency synthesized from the receiver VCO tracking the forward link signal. The MTAR transmits to and detects the signal received from the MMT. These units were designed to be used in a series of experiments to compare pseudonoise modulation and adaptive burst communication to conventional QPSK modulation under actual RFI conditions. Control box selection of modulation mode, command and telemetry data rates, pseudonoise chip rates, and ABC burst modes is provided. Digital data error rates can be measured both with and without convolutional encoding. A voice channel can be selected for both forward and return links. The return link carrier frequency will be 137.0 MHz while one of three frequencies (127.75 MHz, 149.0 MHz or 401.0 MHz) can be selected for the forward link.

The MMT consists of a diversity receiver and a transmitter operating through two quadriplexers into two antenna elements. The receiver functional block diagram is shown in figure 3-1. Selection of the expected receive frequency is made by connecting the appropriate input bandpass preselector and local oscillator frequency to the first mixer. Intermediate-frequency amplifiers at 67.75 MHz and 16.25 MHz amplify the received signal. The third mixer stage serves as a correlator in the pseudonoise mode of operation. The local reference circuitry balance modulates the receiver pseudonoise code with the 15 MHz local oscillator signal. When the code on the received signal is in phase with the locally generated code, a narrowband IF signal results. These signals are amplified and drive the phase-lock detectors in each of the two diversity receivers. When the incoming carrier signal is being tracked, each VCO provides a phase coherent drive to a frequency synthesizer which generates the local oscillator (LO) frequencies and transmit carrier frequency.

Figure 3-1. MMT Receiver
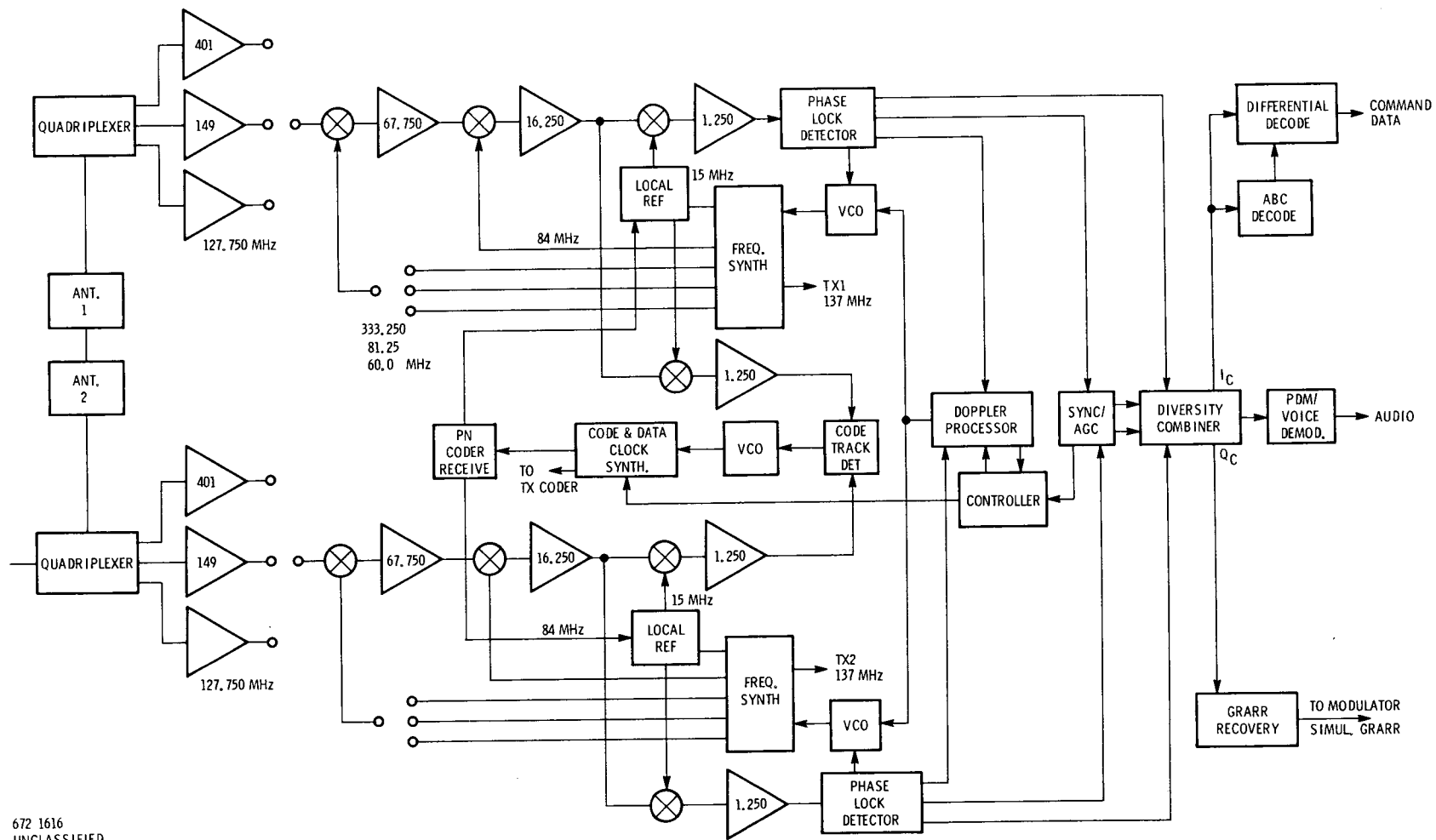
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In the pseudonoise mode the code tracking loop keeps the receiver reference code in phase with the code on the received signal. In each receiver the incoming signal goes to a separate correlator and 1.25 MHz IF amplifier. The local reference provides this correlator with an early/late code from which a tracking error signal is derived. These error signals are combined and filtered in the code track detector and drive a single clock VCO. Note that diversity reception requires two receivers because the propagation time difference due to the spatial relationship of the antennas is in the order of a full cycle at the RF carrier frequency. The code track error signals can be combined to drive a single VCO because the 10 ns time difference in the received signals is insignificant at the code-chip rates used. The code and data clock synthesizer is driven by the clock VCO and generates clocks for the receive and transmit coders. In the QPSK mode the clock VCO and synthesizer are used to recover the receive digital data clock.

The in-phase (I) and quadrature (Q) outputs of the phase lock detectors are combined in the diversity combiner. The command digital data, bursted ABC data or PDM voice is extracted from the I-combined signal. The GRARR digital simulation is extracted from the Q-combined signal.

The Doppler processor in conjunction with the controller searches out the Doppler frequency uncertainty to obtain carrier lock. The anticipated Doppler frequency error for the TDRS system is much greater than the carrier loop filter bandwidth. The doppler processor employs a technique that searches out the doppler uncertainty much faster than a linear cell by cell frequency search. Both the carrier frequency and code phase uncertainties must be resolved. The controller advances or retards the code clock phase to obtain pseudonoise code synchronization. The sync/AGC circuitry makes the sync-search decision and generates the AGC signals to control IF amplifier gain.

The MMT transmitter functions are shown in figure 3-2. The output amplifier drives a power divider to provide outputs to the dual quadriplexer and antenna arrangement. Provision is made to adjust the output power level with a front panel control. The output amplifier is driven by a modulated 137 MHz RF signal. The carrier is selected to be taken from the frequency synthesizer of the diversity receiver phase locked to the strongest received signal.

Figure 3-2. MMT Transmitter

In the QPSK mode the GRARR digital simulation detected by the receiver is balance modulated on the 90-degree, phase-shifted carrier. The digital data or PDM voice is balance modulated on the in-phase carrier. The two signals are summed before driving the output amplifier.

In the PN mode the digital data/PDM is combined with the pseudonoise code before being balance modulated with the in-phase carrier. The 90-degree carrier is switched off in the PN mode. The transmit code clock is generated by the code and data clock synthesizer driven by the receive code clock VCO.

In the ABC mode the telemetry digital data or PDM voice is encoded into the ABC burst format and then balance modulated on the in-phase carrier. The GRARR digital simulation detected by the receiver is balance modulated on the 90-degree, phase-shifted carrier. The RF drive to the output amplifier is gated by the ABC burst gate signal generated by the ABC receiver decode circuitry.

3-4

The telemetry digital data can be transmitted either with or without convolutional encoding. This feature allows for comparative data error rate tests to be run for evaluating performance improvement with convolutional encoding. A data clock output is provided to clock the external instrument that will generate the telemetry digital data.

The MTAR consists of a diversity receiver and a transmitter operating through two quadriplexers into two antenna elements. The receiver functional block diagram is shown in figure 3-3. The first mixer converts the 137.0 MHz receive frequency down to 57.0 MHz. The IF amplifiers at 57.0 MHz and 12.0 MHz amplify the received signal.

The third mixer stage serves as a correlator in the pseudonoise mode of operation. The local reference circuitry balance modulates the receiver pseudonoise code with the 10.75 MHz local oscillator signal. When the code on the received signal is in phase with the locally generated code, a narrowband IF signal results. These signals are amplified and drive the phase-lock detectors in each of the two diversity receivers. When the incoming carrier signal is being tracked, each VCO provides a phase coherent drive to a frequency synthesizer which generates the receive local oscillator frequencies.

In the pseudonoise mode the code tracking loop keeps the receiver reference code in phase with the code on the received signal. In each receiver the incoming signal goes to a separate correlator and 1.25 MHz IF amplifier. The local reference provides this correlator with an early-late code from which a tracking error signal is derived. These error signals are combined and filtered in the code track detector and drive a single-clock VCO. Diversity reception requires two receivers because the propagation time difference due to the spatial relationship of the antennas is in the order of a full cycle at the RF carrier frequency. The code-track error signals can be combined to drive a single VCO because the 10 ns time difference in the received signals is insignificant at the code-chip rates used. The code and data-clock synthesizer is driven by the clock VCO and generates the selected chip-rate clock for the receive coder. In the QPSK mode the clock VCO and synthesizer are used to recover the receive digital data clock.
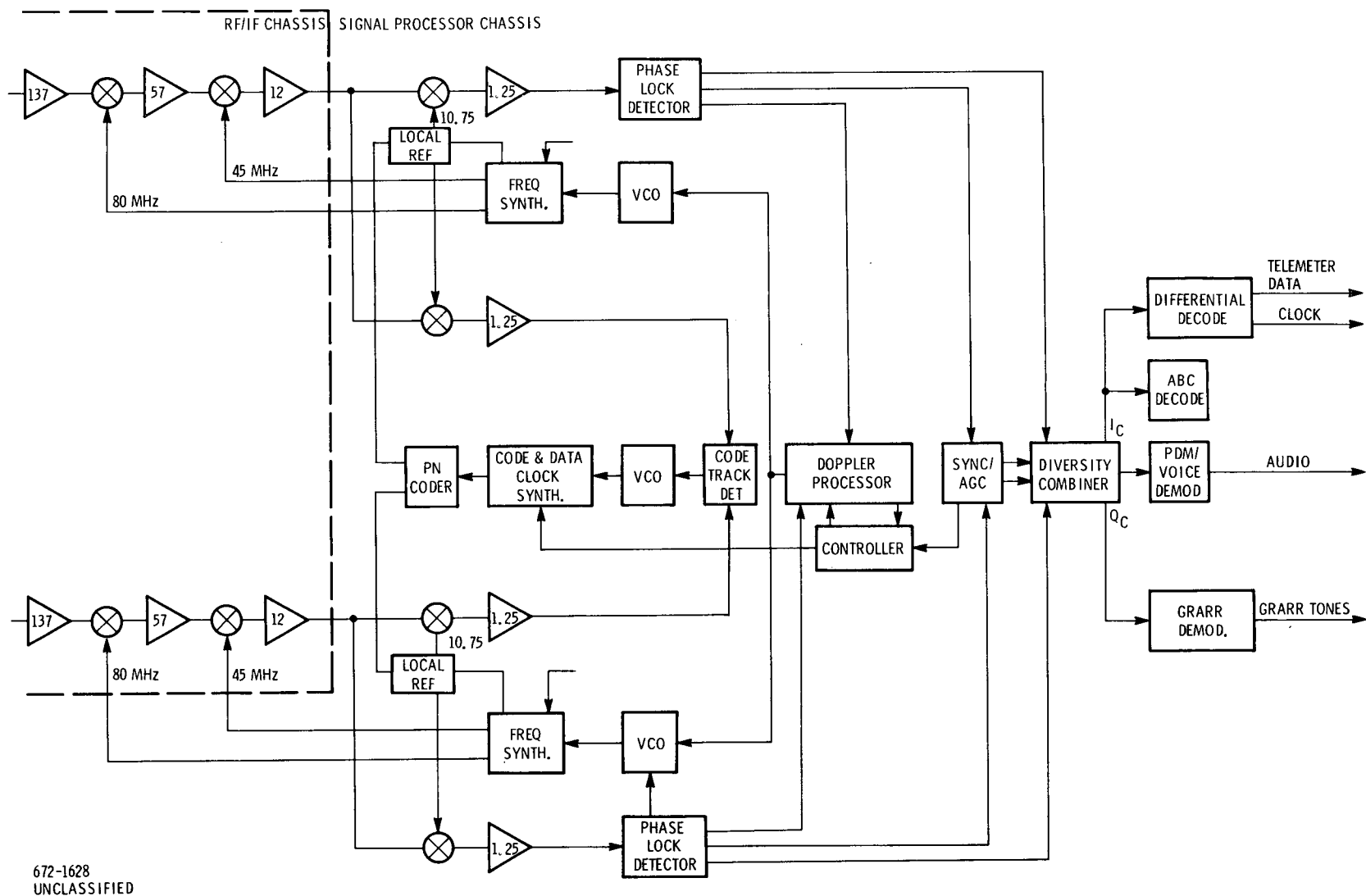
Figure 3-3. MTAR Receiver

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The in-phase (I) and quadrature (Q) outputs of the phase-lock detectors are combined in the diversity combiner. The telemetry digital data, PDM voice, or bursted ABC data is extracted from the I-combined signal. The GRARR digital simulation signal is extracted from the Q-combined output of the diversity combiner.

The doppler processor in conjunction with the controller searches out the doppler frequency uncertainty to obtain carrier lock. The anticipated doppler frequency error for the TDRS system is much greater than the carrier loop filter bandwidth. The doppler processor employs a technique that searches out the doppler uncertainty much faster than a linear cell-by-cell frequency search. Both the carrier frequency and code-phase uncertainties must be resolved. The controller advances or retards the code clock phase to obtain pseuodnoise code synchronization. The sync-AGC circuitry makes the sync-search decision and generates the AGC signals to control IF amplifier gain.

The MTAR transmitter functions are shown in figure 3-4. The output amplifier drives into a variable attenuator for output power control. The attenuator is connected to the appropriate bandpass filter for the frequency to be transmitted. An RF power divider for each of the bandpass filters provides the outputs to the dual quadriplexer and attenuator arrangement.

A frequency synthesizer driven by a stable crystal-controlled oscillator provides three transmit local-oscillator frequencies and the transmit carrier. One of the three local-oscillator frequencies is selected for mixing with the modulated 67.75 MHz transmit carrier to obtain the desired output frequency.

In the QPSK mode the GRARR digital simulation derived from the GRARR range tone signal is balance modulated on the 90-degree, phase-shifted carrier. The digital data or PDM voice is balance modulated on the in-phase carrier. The two signals are summed, amplified, and mixed with a transmit local oscillator before driving the output amplifier.

In the PN mode the digital data or PDM voice is combined with the pseudo-noise code before being balance modulated with the in-phase carrier. The two 90 degree carrier is switched off in the PN mode. The selected code-chip-rate clock is generated by a synthesizer driven by a stable oscillator.
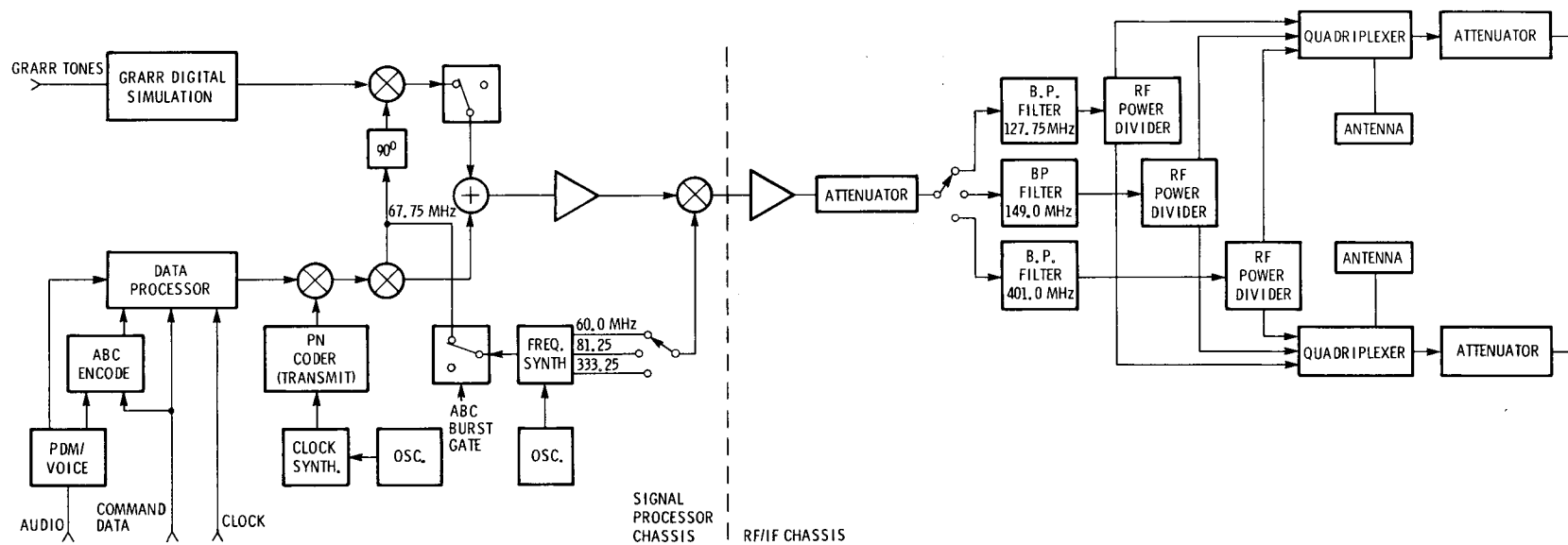
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Figure 3-4. MTAR Transmitter

In the ABC mode the command digital data or PDM voice is encoded into the ABC burst format and then balance modulated on the in-phase carrier. The GRARR digital simulation signal is balance modulated on the 90° phase shifted carrier. The 67.75 MHz transmit carrier is gated by the ABC burst gate signal generated by the ABC encode circuitry.

3.2 MMT (AIRBORNE UNIT)

The multimode transponder (MMT) consists of an antenna assembly, RF/1F chassis, signal processor chassis, control box, and power supply chassis. This section gives a detailed functional description of each of these assemblies. Individual descriptions of each unique printed wiring board and subassembly are included with their functional block diagrams.

3.2.1 ANTENNA

Chu Associates Incorporated has provided engineering services directed toward the establishment of design specifications for VHF/UHF antenna systems to be used with the Magnavox Research Laboratories Multimode Transponder (MMT) and its associated ground station Multimode Transmitter and Receiver (MTAR) systems. This study was performed under MRL Contract No. XT-707-02 AIM in conformance with the associated Statement of Work.

MMT equipment will ultimately be installed in low-orbiting satellites. For initial test and evaluation purposes, however, it is to be installed in an aircraft and operated in conjunction with the associated ground equipment (MTAR). Transmitting and receiving antennas operating in the VHF/UHF band will be required for both the airborne and ground terminals during this evaluation period. Additional testing is required, prior to the airborne evaluation, during which the airborne (MMT) equipment will be located on the ground. The first antenna supplied for the (MMT) equipment will be suitable for use during this ground test period.

3.2.1.1 Ground Tests

3.2.1.1 Multimode Transponder (MMT) Antenna

During the initial test phase, the (MMT) system will be mounted on the ground and will communicate with a ground mounted (MTAR) system. Examination of the general (MMT) antenna requirements indicated three significant areas which would

influence the selection of a suitable antenna. First is the relatively wide separation (approximately 3:1) between the VHF and UFH operating frequencies. This wide range tends to preclude use of a single narrow-band antenna to cover all four bands. Many antenna types which exhibit the desired impedance, pattern, and polarization character-istics over narrow frequency ranges would not maintain these characteristics over 3:1 bandwidths. This includes orthogonal dipoles, axial mode helices and fractional turn quadrifilar volutes. Alternate solutions to the wide frequency requirements would be either the use of multiple narrow-band antennas, or a single broad-band antenna having the desired characteristics over the entire band. Various types of log-periodic arrays exhibit these wide-band characteristics, usually at the price of some increase in overall size.

The second consideration is the requirement for full duplex operation – simultaneous transmission and reception – with different polarization requirements for each. Attempting to use a single antenna for both functions would, first of all, require a diplexer capable of isolating a transmitter and receiver potentially separated in frequency by as little as 7 percent. With the common antenna, all space isolation would be eliminated and all of the isolation required for interference-free receiver performance at f_o-7 percent would have to be supplied by the diplexer circuitry. The single antenna approach would also require a radiator which would simultaneously provide a circularly polarized terminal for transmission and multiple polarization diversity outlets for reception. This could be done with diplexers and phase shifters or by using separate transmitting and receiving antennas, each inherently providing the desired polarization.

The third consideration is the desire for "omni-directional" pattern cov-erage. In the initial tests, with the (MMT) system mounted on the ground and com-municating with a fixed ground based (MTAR), it is felt that suitable pattern coverage would be obtained using one or more unidirectional antennas directed toward the (MTAR). For this point-to-point link radiation in directions other than the (MTAR) would serve no useful purpose. The directional antenna approach would provide addi-tional system gain and would minimize spurious radiation from backlobe reflections.

Reviewing the above considerations, it appears that the simplest approach for the ground based (MMT) antenna system is the use of two antennas, one used exclusively for receiving and the other for transmitting. Each should be unidirectional and oriented to provide maximum radiation along the horizon in the direction of the

(MTAR) terminal. The receiving antenna should operate broadband at any of the receiving frequencies, from 126-402 MHz, and have multiple output terminals for selection of the desired polarization. The transmitting antenna requires only a single input terminal providing circular polarization.

For simplicity and economy of design, it is desirable to utilize two identical antenna structures which are capable of providing both the receiving and transmitting characteristics. This can be done with a trapezoidal log-periodic array. The basic array, as shown in figure 3-5 consists of two periodic half-structures oriented at an angle ψ with respect to each other. These two half-structures form a balanced antenna which, when fed against each other from their vertex, radiate a unidirectional beam directed along the apex in the positive Y direction. This radiation is linearly polarized in the plane of the radiating elements. By placing a second pair of half-structures at right angles to the first, sharing a common apex, a second unidirectional linearly polarized beam can be obtained. By feeding each pair separately from coaxial inputs at the rear of the array, two independent, orthogonal, linearly polarized beams can be obtained for polarization diversity. Circular polarization can also be obtained from the same array by combining the two linear pairs with a 90-degree phase shift between them. This can be done inherently by scaling the physical size of one pair of structures to effect a constant 90-degree shift with respect to the other. It can also be done externally, using two in-phase antenna pairs combined through a broadband quadrature hybrid. The result in either case is a unidirectional, circularly polarized beam.

The radiation characteristics of the array can be controlled by proper selection of the design parameters. For this application, it is desirable to have E and H plane beamwidths which are approximately equal. An array with such beamwidths, designed to operate over the entire 126-402 MHz range, would be pyramidal in shape with a square base of approximately 54 inches on a side and a base-to-apex height of approximately 36 inches. Each linear array would have a 1/2 power beamwidth of about 65 degrees in the E-plane and 70 degrees in the H-plane. The gain of one array would be in the order of 8 DBI with front-to-back ratios of 12-15 dB. The input VSWR on 50 ohms would be less than 2.0:1 at all frequencies.

Two of these arrays would be located side by side, one for receiving, one for transmitting. For receiving, it is not known what degree of polarization diversity is desired as two orthogonal linear modes and a circular mode can be obtained. If the two linear modes are sufficient, they are available from the two antenna feed ports without need for the switches or hybrid. Similarly for transmitting, which requires only circular polarization, the two inputs from the antenna would be connected directly to the hybrid.

3.2.1.1.2 Multimode Transmitter and Receiver (MTAR) Antenna

During the ground test phase of this program, the companion (MTAR) equipment can utilize the same type of antenna described above for the (MMT) equipment. Two trapezoidal log-periodic arrays would be mounted side by side and oriented for maximum radiation in the direction of the (MMT) ground site. One antenna would be configured for polarization diversity reception in the 136-138 MHz band. The other would be configured for circularly polarized transmission in the 126-130, 148-150, and 400-402 MHz bands.

Use of identical antenna systems for both the (MMT) and (MTAR) terminals offers the most economical approach and will provide maximum system flexibility.

3.2.1.2 Airborne Tests

During the airborne test phase of this program, the (MMT) terminal will be installed in an aircraft and operated in conjunction with the ground-based (MTAR) equipment. From the standpoint of electrical performance, the same log-periodic array could be utilized. The primary limitation on test flexibility is the pattern coverage that can be obtained. Because of its inherent directional characteristics, the coverage obtained on the aircraft will not differ greatly from the ground-based condition. As discussed, the E and H plane half-power beamwidths of this array are nearly constant at approximately 65 degrees to 70 degrees. Assuming a nominal gain of 8 dBi for the linear polarized mode, the beamwidth over which the response is above iso-tropic level is approximately 120 degrees. Beyond this point the response decreases steadily and reaches low levels at angles normal to the axis. This will limit the flight pattern of the aircraft, depending upon where the antenna is mounted on the aircraft and also upon the orientation of the ground antenna.
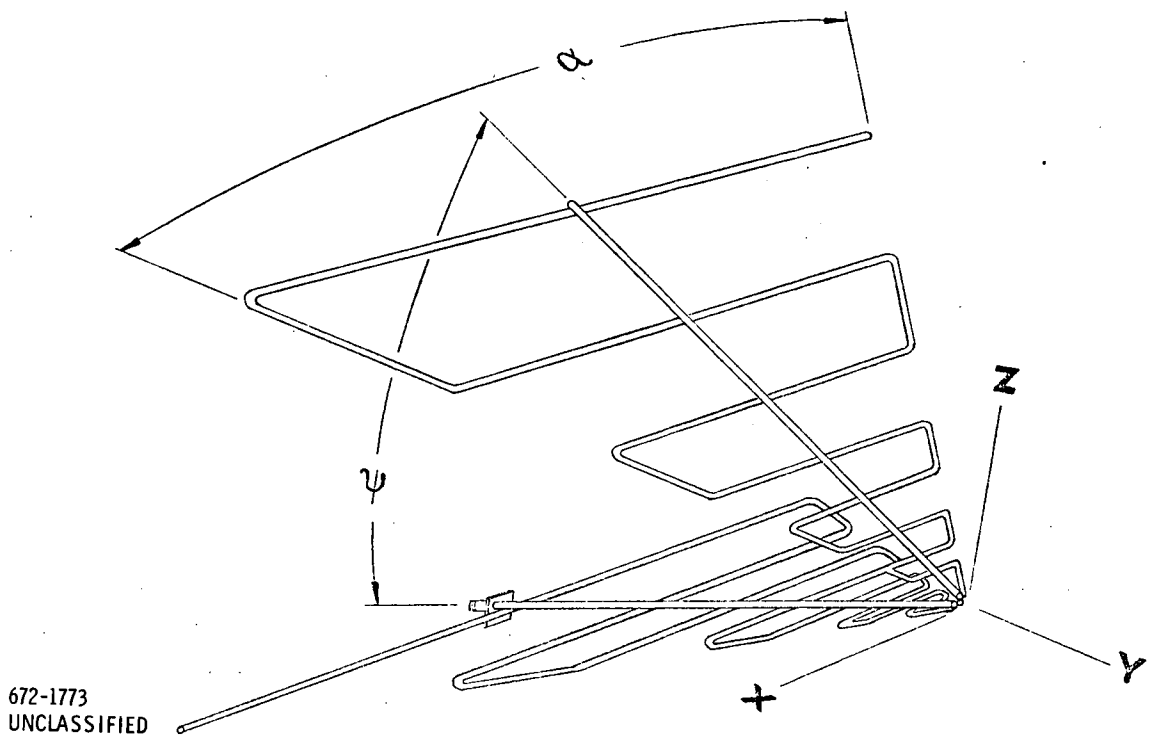
Figure 3-5. Trapezoidal Log-Periodic Antenna Array

With the array mounted off the side of the aircraft, normal to the line of flight and angled downward toward the ground, the aircraft could make straight fly-bys some distance away from the ground site, generally observing the 120-degree sector limitation. Maximum signal level would be obtained during this flight pattern by tilting the ground antenna toward the line of flight. Obviously on the return fly-by the aircraft array would be pointed away from the ground site and relatively little response would be obtained.

Greater usable pass time could be obtained by flying circular patterns at a fixed radius from the ground site. During such passes, the ground antenna could be tilted to favor a particular path sector. It could also be mounted vertical for uniform, but reduced, response over the entire circle.

Depending upon the type of aircraft used, it may also be operationally feasible to mount the array near the rear of the fuselage pointing aft and downward. This would permit radial passes, vectored outward from the base site. For optimum response, the base antenna should be tilted toward the direction of flight.

The most severe obstacle to use of the log-periodic arrays for flight tests
is one of mechanically adapting them for installation on the aircraft. It will be a major
task to ruggedize these arrays and suitably fit two of them to the aircraft environment.
Every effort should be made to minimize this task. It would be highly desirable for
the airborne terminal to utilize a single antenna array suitable for simultaneous trans-
mitting and receiving use.

It should be noted that the requirement for reception in the 126-130 MHz
and 400 MHz bands would require a base width of approximately 50 inches and base-
to-apex height of about 34 inches.

A cursory wind load analysis was made for the worst-case condition, with
an array mounted on the side of the aircraft, normal to the direction of flight. Using
radiating elements of 3/8-inch diameter, dielectrically braced at the edges to the
adjoining array, the size of the central support tubes would vary from approximately
1 1/4-inch O.D. with 3/32-inch wall at speeds of 100 knots to 2 1/4-inch O.D. with
3/16-inch wall at 250 knots. At 175 knots (200 mph) tube sizes in the order of
1 3/4-inch O.D. would be required. It is felt that a satisfactory electrical design
could be obtained within these physical design parameters.

It is visualized that the most simple means of installing this antenna on the
aircraft would be a fixed, base mounted against a side door or bottom cargo hatch. Base
mounting should provide maximum support for the antenna and would require minimum
aircraft modification. An alternate method would be to support the antenna from the
end of a movable boom extending horizontally out from a side door. Axial rotation of
the boom would turn the array to point toward the ground during test or swing it upward,
if necessary, for clearance while on the ground. The best method will obviously be
dependent upon the type of aircraft selected for the tests. It may also be necessary to
incorporate means for folding the array for stowage against the side of the aircraft in
essentially a two dimensional triangular shape. This, of course, would complicate the
mechanical design and should not be done unless necessary under the operating
conditions.

3.2.1.3   Design Specification

It is recommended that the coincident orthogonal trapezoidal log-periodic
arrays discussed above be utilized for both the (MMT) and (MTAR) terminals. For
greatest simplicity and economy both terminals should use the same antenna

configuration. The (MMT) antenna system should be designed during the ground test phase to permit direct adaption of the same antenna to the aircraft during subsequent airborne phases of the program.

Each antenna will be identical in electrical performance. Each would consist of identical orthogonal arrays with dual coaxial outputs. These outputs would be in-phase, but would provide orthogonal linear polarization. They would provide circular polarization when externally combined through an external 90-degree phase shifter as part of the terminal equipment.

The (MMT) terminal, at least during the airborne phase, should use a single antenna for the receive and transmit modes as shown in figure 3-6. This requires a quadriplexer and phase shifters as part of the terminal equipment. It is recommended that the same configuration be used during the ground phase and also for the (MTAR) terminal, although, if desired, separate receiving and transmitting antennas could be used to eliminate the diplexer requirement.

Each array should have the following electrical characteristics:

Frequency range:	126-402 MHz covering four discrete bands; 126-130, 136-138, 148-150, 400-402 MHz
VSWR:	2.0:1 maximum on 50 ohms in each frequency band
Outputs:	Dual 50 ohm coaxial
Pattern:	Unidirectional with each linear array displaying average half-power beamwidths of: E-plane = 65° H-plane = 70°
Front-to-Back ratio:	15 dB average
Gain:	6 dBi, each linear input

3.2.2   RF/IF CHASSIS

A block diagram of the multimode transponder RF/IF is shown in figure 3-7. The unit is a combined transmitter and receiver. The transmitter will transmit one VHF frequency from each antenna and the two receivers will each receive one of three

frequencies. Two of the receiver frequencies are VHF and one will be a UHF frequency. The power amplifier (A1) is capable of two distinct modes of operation, and will supply a total RF power of 37 dBm to the antennas. The RF power output may be reduced by 30 dB in 1 dB steps by adjusting the voltage-controlled attenuator R1.

The power amplifier is driven with a 137 MHz 0 dBm signal, and has an amplification factor of 42 dB. The output of the amplifier A1 is first filtered by transmitter bandpass filter (F1). The bandpass filter has a center frequency of 137 MHz and a 3 dB bandwidth of 4 MHz. The output of the transmitter bandpass filter is followed by a power divider used to divide the RF power between the two quadriplexers. The outputs are connected to the 137 MHz ports of the quadriplexers. The power divider lets one power amplifier drive both antennas to obtain polarization diversity. The quadriplexers (P1 and P2) permit the common use of the antennas for transmitting and reception. The antennas are capable of receiving one of three frequencies and will drive each quadriplexer, which will separate each frequency and route it to the appropriate preselector bandpass filter. The preselector bandpass filters (F2 through F4) provide band selection for receiver No. 1 and preselector bandpass filters
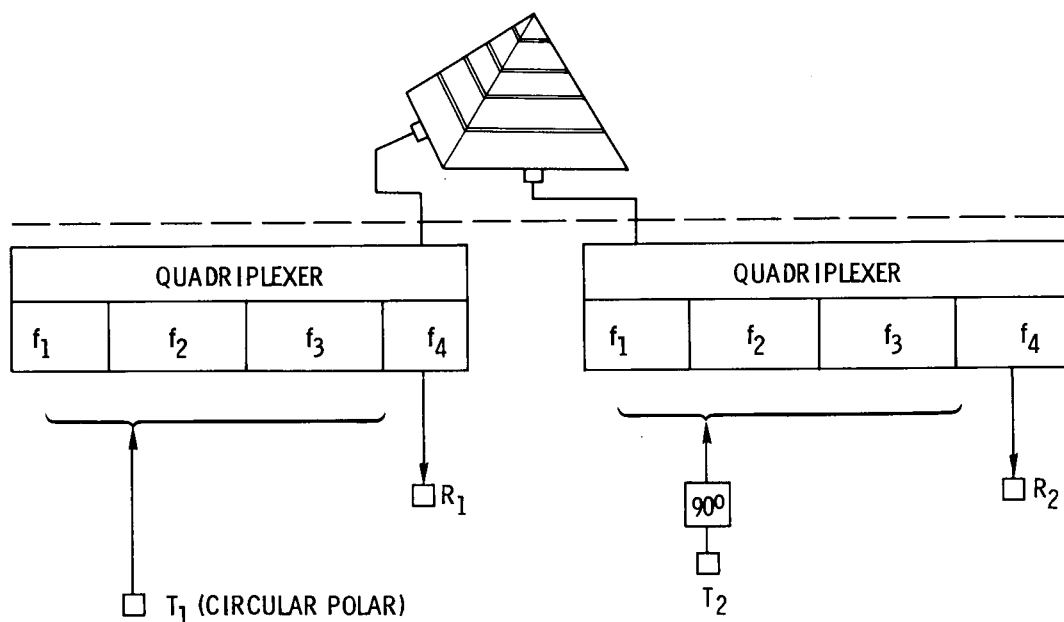
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Figure 3-6. Feed Schematic for Orthogonal Log-Periodic Arrays

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(F5 through F7) provide band selection for receiver no. 2. The preselector's output will be manually connected to each of the receivers. The receivers are low noise, wideband receivers with high gain. The receivers are discussed in detail in part 2 of multimode transponder (MMT) receiver. The multimode transponder RF/IF as a one-of-a kind unique test equipment is procured from off-the-shelf components whenever possible. The design features of the individual blocks in figure 3-7 are briefly discussed in the following paragraphs.

3.2.2.1   RF Power Amplifier (A1)

The RF power amplifier is a commercial, solid-state, broadband amplifier. The amplifier is a unique combination of lumped elements, microstripline and ferrite hybrid techniques. The combination of these techniques and utilizing the latest silicon transistor offer a power-frequency capability, that permits the wideband width of 125 MHz to 155 MHz. The design also insures stable performance and high reliability over the temperature range. The input drive will be supplied at a power level of 0 dBm and a frequency of 137 MHz. The gain of the power amplifier is approximately 42 dB and all intermodulation products and spurious responses are down at least 30 dB. The device is capable of two distinct modes of operation: (1) Mode A - The input drive will consist of a 2 ms, burst of carrier frequency at a 20 percent on and 80 percent off duty cycle; (2) Mode B - The input drive will be a constant envelope carrier. The output power gain is adjustable from 42 dB to 12 dB in 1 dB steps. A voltage controlled attenuator R1 supplies a 0 to 10 VDC voltage to the attenuator input of the amplifier. The power amplifier will deliver 20 watts into a 50 ohm load. The output stage is protected and will not be damaged as a result of the output port being indefinitely opened or short circuited. As an added safety feature, B+ reversal protection circuitry is included to prevent damage to the amplifier. The DC power requirement for the power amplifier is +28 VDC, and power efficiency is greater than 30 percent in either mode A or B. Design and construction of this rugged amplifier meets the requirements called out in drawing no. X625195.

3.2.2.2   Transmitter Bandpass Filter (F1)

The power amplifier is followed by a bandpass filter (F1), which limits the output amplifier to a center frequency of 137 MHz and a 4-MHz, 3-dB bandwidth. The bandpass filter has a 15-MHz 40-dB bandwidth, that is used in conjunction with the quadriplexer. The bandpass filter and the quadriplexer supply 120 dB of isolation
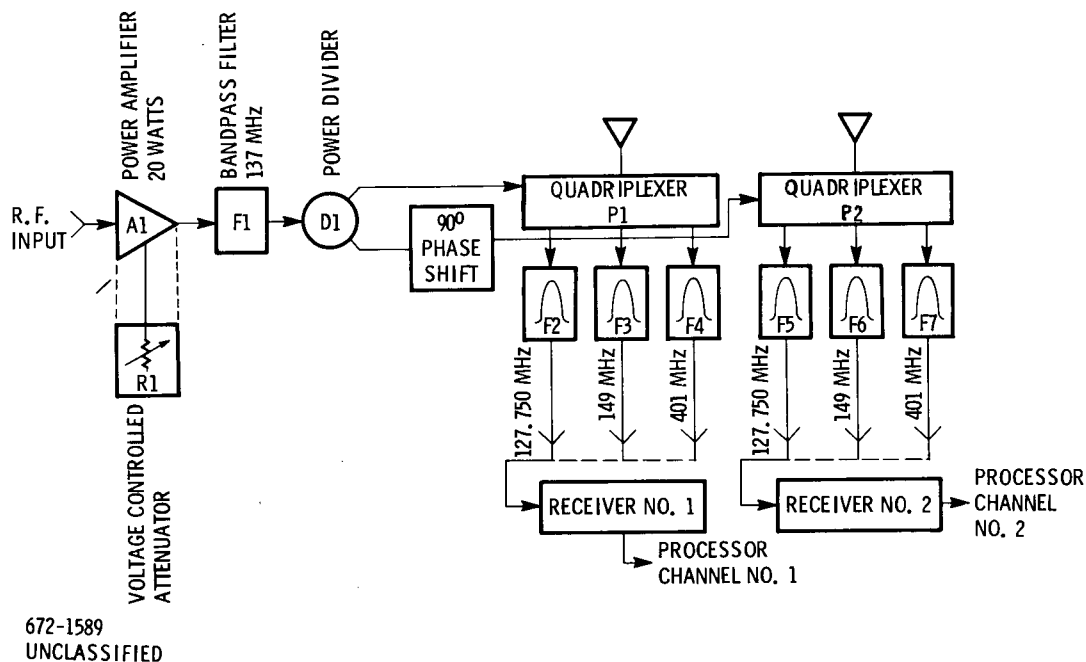
Figure 3-7. MMT RF/IF

between the transmitter band and the receiver bands. The cavity type bandpass filter
has unique characteristics, which are required to obtain low insertion loss, and still
meet the high power requirements. The cavity filter offers suitable size and form
factor. The bandpass filter serves to assure that all superior radiation is down 40 dB
below the fundamental. The basic design techniques for the bandpass filter are well
established so that filter manufacturer claim off-the-shelf availability. The 137 MHz
bandpass filter's characteristics are specified in drawing X625187.

3.2.2.3   Power Divider (D1)

The power divider is used to divide the output signals of transmitter band-
pass filter (F1). The device is a low-insertion, loss-reactive, power divider with two
outputs. The input is matched with a multisection dielectrically loaded transformer
with a Tchebyscheff type low-ripple response. Power division difference at the outputs
is in the order of 0.1 dB. The output signals are in phase with each other. The band-
width of the device is 100 MHz to 200 MHz and has an insertion loss of 0.1 dB maximum.
The power divider characteristics are specified in drawing X625200.

3.2.2.4   Quadriplexers (P1 and P2)

The outputs of the power divider D1 are routed into the 137 MHz ports of the quadriplexers. A quadriplexer permits the use of a common antenna for transmission and reception. Each unit will drive an antenna with a VHF frequency of 137 MHz. The antennas will receive and drive the quadriplexers with one of three frequencies, two VHF frequencies (127.750 MHz and 149 MHz) and one UHF frequency of 401 MHz. The two VHF and one UHF frequencies will be routed to the corresponding preselector bandpass filters. The quadriplexers are an advancement in the technique of filter design which will enable the different frequencies to be separated and routed to the individual frequency port. Each quadriplexer will have a total of five ports, which are (1) 137 MHz, (2) 127.750 MHz, (3) 149 MHz, (4) 401 MHz and (5) the antenna port. The antenna port is capable of receiving or transmitting two of the four frequencies. The primary functions of the quadriplexers are to separate and isolate each frequency. The quadriplexers must have adequate isolation since transmitter and receivers will both be on at the same time. To maintain separation from the transmitter's frequency and the receiver's frequency, a 120 dB of isolation is required between the transmitter band and receiver band. Refer to table 3-1 for a summary of isolation necessary to obtain separation. The design for the required quadriplexers only permits 80 dB of isolation between bands. The parameters that were consistent in designing the quadriplexers were as follows: (1) the insertion loss of the quadriplexers to be held to a maximum of 2.8 dB, (2) the 3 dB bandwidth a minimum of 2 MHz, (3) the 80 dB bandwidth a maximum of 15 MHz and (4) the quadriplexers must be capable of 20 watts average power. Since only 80 dB is obtainable in quadriplexers, the other 40 dB will be obtained from the bandpass filters. The quadriplexers in conjunction with the bandpass filters will supply the required 120 dB isolation between transmitter band and the receiver bands.

3.2.2.5   Preselector Bandpass Filters

Quadriplexer (P1) supplies drive to three bandpass filters F2, F3, and F4. The filters are used in conjunction with the quadriplexer (P1) to obtain a 120 dB of isolation between the transmitter band and the receiver band. The three bandpass filters are connected to the receiver ports of the quadriplexer (P1) and serve as a preselector for receiver No. 1. The bandpass filters are tuned to have the following characteristics: The F2 center frequency is 127.750 MHz and has a 3 dB bandwidth of 4 MHz, F3 center frequency is 149 MHz and has a 4.5 MHz 3 dB bandwidth, F4 center frequency is 401 MHz and has a 4 MHz 3 dB bandwidth. All three filters have a 15-MHz,

Table 3-1. Transmitter - Receiver Isolation Requirements

$$\text{ISOLATION REQUIREMENTS} \geq \left(37 + 145 + 10 - 20 \log\pi \frac{\Delta f}{f_c} - 10 \log \frac{f_c}{f_b}\right) \text{ dB}$$

WHERE: Δf = FREQUENCY SEPARATION
f_c = CHIP RATE
f_b = DATA RATE (100 BPS)

Δf (MHz)	f_c (KHz)	$20 \log \frac{\Delta f}{f_c}$ (dB)	$10 \log \frac{f_c}{100}$ (dB)	Transmitter Power in Receiver Bandwidth (dBm)	Isolation Necessary (dB)
137-127.750 = 9.250	800	31	39	-33	122
	100	49	30	-42	113
	25	61	24	-48	107
149-137 = 12	800	33	39	-35	120
	100	51	30	-44	111
	25	63	24	-50	105
401-137 = 264	800	60	39	-62	93
	100	78	30	-71	84
	25	90	24	-77	78

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40-dB bandwidth, which is used in conjunction with the 15-MHz, 80-dB bandwidth of the quadriplexer (P1) to give a total 15-MHz, 120-dB bandwidth. The 15-MHz, 120-dB bandwidth provides the necessary isolation between transmitter and receiver. The bandpass filters are cavity type to provide the lowest insertion loss and still maintain a reasonable size. The output of the selected bandpass filter is switched manually to the input of the receiver no. 1.

Quadriplexer (P2) supplies drive to three bandpass filters F5, F6 and F7. The filters are used in conjunction with the quadriplexer (P2) to obtain a 120 dB of isolation between the transmitter band and the receiver band. The three bandpass filters are connected to the receiver ports of the quadriplexer (P2) and serve as a preselector for receiver no. 2. The bandpass filters are tuned to have the following characteristics: F5 center frequency is 127.750 MHz and has a 3 dB bandwidth of 4 MHz, F6 center frequency is 149 MHz and has a 4.5-MHz, 3-dB bandwidth, F7 center frequency is 401 MHz and has a 4-MHz, 3-dB bandwidth. All three filters have a 15-MHz, 40-dB bandwidth, which is used in conjunction with the 15-MHz, 80-dB bandwidth of the

quadriplexer (P2) to give a total 15-MHz, 120-dB bandwidth. The 15-MHz, 120-dB bandwidth provides the necessary isolation between transmitter and receiver. The bandpass filters are also cavity type to provide the lowest insertion loss and still maintain reasonable size. The output of the selected bandpass filter is switched manually to the input of the receiver no. 2.

3.2.3   RECEIVER

The multimode transponder receiver, which is to be fabricated and tested in the TDRS program will be capable of receiving any one of these three transmitted frequencies: (1) 127.75 MHz, (2) 149 MHz and (3) 401 MHz. The receiver's features are low noise, wideband, and high gain. The selectivity will be controlled by the quadriplexer and preselector bandpass filters. A top-level, block diagram of the multimode transponder receiver is shown in figure 3-8. The multimode transponder will have two such receivers to provide for polarization diversity. The design features of the individual blocks in figure 3-8 are discussed in the following paragraphs.

3.2.3.1   Preamplifier

The preamplifier consists of three RF amplifiers A1, A2, A3, and a bandstop filter (F1). The RF amplifiers (mic-amps) A1, A2, A3 were selected for their low noise figure of 2.5 dB. The mic-amps are unique in that a complete transistor amplifier is contained in a TO-8 transistor package. The tiny modular amplifiers are made with highly reliable sapphire substrates, microwave transistor chips, thin film resistors and chip capacitors. The units have a bandwidth of 5 MHz to 500 MHz and can be cascaded without bandwidth shrinkage. The bandwidth is maintained with a flatness of ±1.0 dB over the frequency range. The inputs and outputs are 50 ohm, with a maximum VSWR of 2.0.

The noise figure of the preamplifier is 3 dB, due to cascading two mic-amps A1 and A2, (reference to figure 3-8) the total gain of A1 and A2 is 29 dB and the compression factor of A2 is -2 dB.

3.2.3.2   Bandstop Filter

The output of mic-amp A2 is filtered by a bandstop filter (F1). The bandstop filter rejects all frequencies below 100 MHz and is tuned to have a 10 dB bandstop at 266 MHz. The bandstop filter provides rejection and suppress out-of-band noise and interference, to achieve an image suppression and to prevent radiation of the

5.5 dB LOSS
IN QUADRAPLEXER
AND BANDPASS FILTERS

BANDSTOP
100 MHz AND BELOW
BANDSTOP 266 MHz

N_o = -58.5 dB
P_s = -103.5 dB

BANDPASS FILTER
f_c = 67.775 MHz
B.W. = 10 MHz

N_o = -44.5 dB
P_s = -86.5 dB

BANDPASS FILTER
f_c = 16.225 MHz
B.W. = 2 MHz

A1 +15 dB
N/F = 3 dB

N_o = -165.5 dBm
P_s = -135.5 dBm

A2 +14 dB

F1
-63.5 dB
-108.5 dB

A3 +14 dB

M1
L.O. NO. 1
(1) 333.225 MHz
(2) 81.225 MHz
(3) 60,000 MHz

A4 +13 dB

F2
-50.5 dB
-92.5 dB

A5 +13 dB

M2
L.O. NO. 2
84,000 MHz

A6 +13 dB

F3
-40.5 dB
-78.5 dB

A7 +13 dB

A8 6 dB
ACG VOLTAGE
-24 dB ≤ G ≤ 5 dB

A9 0 dB
AGC VOLTAGE
-20 ≤ G ≤ 0 dB

A10 +13

D1 -3 dB
SPLIT

N_o = -12.5 dB
P_s = -53.5 dB

R1 -6 dB

M3 -6 dB
L.O. NO. 3
15,000 MHz

B.P. FILTER
f_c = 1.225 MHz
B.W. = 125 KHz
-2 dB
F4
-32.5 dB
-73.5 dB

A11 +40dB

A13 +10 dB

M5
L.O. NO. 4
1.225 MHz

LPF
BW = .2 TO 40 KHz
A16 0 dB
+17.5 dB
-23.5 dB

L.P.F.
A20 +19 dB
$I_{ACQ.}$

A14 +10dB

M6
L.O.
1.225 MHz

LPF
BW = .2 TO 40 KHz
A17 0 dB

L.P.F.
A21 +19 dB
$Q_{ACQ.}$

BANDPASS FILTER
f_c = 1.225 MHz
B.W. = 125 KHz
-2 dB
F5
-32.5 dB
-73.5 dB

R2

M4 -6 dB
L.O. NO. 3
15,000 MHz

A12 +40 dB

A15 +10 dB

M7
L.O.
1.225 MHz

LPF
BW = .2 TO 40 KHz
A18 0 dB
+17.5
-23.5 dB

TRACK
(2X DATA)

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Figure 3-8. Block Diagram MMT Receiver

local oscillator signal. The filter maintains a low system noise figure of 3 dB, but will contribute 2 dB insertion loss. The output of F1 is tied to the input of mic-amp A3. Mic-amp A3 has a gain of 14 dB and a compression of ±7 dB and is used as a buffer between the bandstop filter and the mixer.

3.2.3.3   The First Down Converter

The first down converter is a balanced mixer M1. The balanced mixer, a commercial unit, has a conversion loss of 7.5 dB maximum, and a maximum noise factor of 7.5 dB. The device has an RF signal and local oscillator bandwidth of 5 MHz to 500 MHz, indicating that good amplitude and phase linearity can be obtained. The mixer has a RF to local oscillator isolation of 30 dB minimum. The mixer will be supplied with one of three local oscillators (1) 333.250 MHz to be used with a received frequency of 401 MHz, (2) 81.250 MHz to be used with a received frequency of 149 MHz, and (3) 60.000 MHz to be used with a received frequency of 127.750 MHz. The local oscillator frequency will be manually selected to correspond with the received frequency. The received frequency is also manually selected by connecting the input of the preamplifier to one of the outputs of the preselector bandpass filters 127.75 MHz, 149 MHz, and 401 MHz. The RF input is supplied by A3 to the mixer and the local oscillator is selected to correspond. The output of the mixer will result in the first IF frequency of 67.750 MHz.

3.2.3.4   The First IF

The first IF is made up by using two mic-amps (A4, A5) and a bandpass filter F2. Mic-amp A4 has a gain of 13 dB and is used to maintain a buffer between mixer (M1) and F2 (bandpass filter). The bandpass filter used in the first IF has a center frequency of 67.750 MHz and a bandpass of 10 MHz. The insertion loss will be a maximum of 2 dB. The filter is followed by a mic-amp A5 with a gain of 13 dB. The A5 output is used to drive the second down converter M2.

3.2.3.5   The Second Down Converter (M2)

The second down converter (M2) is a balanced mixer, the same balanced mixer that is used for M1 is also used for M2. The mixer (M2) is supplied with one local oscillator at a frequency of 84 MHz and 4 dBm drive. The input frequency to M2 is the 67.750 MHz that was developed in the first IF. The resulting output frequency will be 16.250 MHz, the second IF frequency. The power gains at this point in the receiver will be -92.5 dB and a noise power of -50.5 dB. Refer to figure 3-8 for power budget.

3.2.3.6   The Second IF Stage

The second IF stage has an insertion loss of 2 dB and gain of 26 dB. Band-pass filter F3 is tuned for a center frequency of 16.250 MHz and has a 3 dB bandwidth of 2 MHz. Mic-amp A6 is used to provide a buffer between mixer M2 and bandpass filter F3. Mic-amp A7 drives the first AGC stage A8, with a signal power of -69.5 dB and a noise power of -27.5 dB.

3.2.4   SIGNAL PROCESSOR CHASSIS

The MMT signal processor chassis contains the receiver circuitry from the 16.25 MHz IF down to baseband processing and the transmitter modulation circuitry. The MMT signal processor chassis is made up of plug-in printed-circuit boards. The following is a list of board nomenclature and the quantities used in the MMT:

Local Reference/Correlator Board	-2
Baseband Conditioner Board	-2
Carrier Loop Filter and VCO Board	-2
Sync/AGC Board	-1
Doppler Processor Boards 1 and 2	-1
Clock Loop Filter and VCO Board	-1
MMT Controller Board	-1
Code and Data Clock Synthesizer Board	-1
Frequency Synthesizer Boards 1 and 2	-2
Receive Coder Board	-1
Diversity Combiner Board	-1
Data Recovery Board	-1
Transmit Coder Board	-1
MMT Modulator Board	-1
Data Processor-Receive Board	-1
PDM Voice-Receive Board	-1
Data Processor-XMIT Board	-1
PDM Voice-XMIT Board	-1
Convolutional Encoder Board	-1
ABC Boards 1 through 8	-13

A functional description of each type of printed-circuit board used in the MMT diversity receivers follows.

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3.2.4.1 Diversity Receivers

3.2.4.1.1 Local Reference/Correlator Board

The local reference/correlator module (figure 3-9) contains: (1) the AGC portion of the 2nd IF of the receiver's triple-conversion RF-IF circuitries, (2) correlators and 3rd IF for the carrier and code-tracking loops, and (3) logic to generate the bogey and early-late reference signals used in the correlator for PN mode operation.

The AGC function in the 2nd IF is carried out by two control signals; namely, common AGC and channel AGC (figure 3-10). Common AGC is derived from estimates of total received signal power of receivers 1 and 2, while channel AGC is derived from estimates of each receiver's own received signal power. The AGC loop's operating characteristics is graphically shown in figure 3-10. That is, when each receiver's input is below -120 dBm, channel AGC of individual receiver regulates its own power level. When combined input of receivers 1 and 2 is above -120 dBm, common AGC will reduce each receiver's IF gain such that signal power to the 2nd AGC amplifier remains around -120 dBm level, which is again within the range of the channel AGC.

In the PN mode, the spread spectrum signal from the second IF is correlated with two local reference signals to generate two separate IFs, one for carrier tracking and the other for code tracking. Except for the local reference signals used in the correlation process, the two correlator-mixers and the third IF's characteristics are identical. They are both band-limited to 125 kHz and have 40 dB gain.

The correlation process in the carrier and code correlators is best illustrated in figure 3-11.

In the carrier correlator, the incoming code, waveform A, is correlated with the local-bogey code, waveform E. If the relative displacement between waveforms A and E is τ, the carrier correlator output will be as shown in waveform F, which when averaged yields value less than 1. At code sync, τ is zero and the carrier correlator output will be a steady 1, a maximum correlation condition.

In the code-loop correlator, the incoming code is correlated with the local late code, waveform B. But the correlation is gated on and off by waveform C, which is the resulting code of modulo-two addition of the late code PN ($-\tau/2$) and an

16.250 MHz
IF

BPF
BW= 2MHz

COMMON
AGC

CHAN
AGC

POWER
DIV

1/2-BIT
SHIFT

BOGEY
LOCAL REF.

CORRELATOR

BPF

15 MHz
L.O.

POWER
DIV

CODE

E/L
LOCAL
REF

CORRELATOR

BPF

CODE IF

$\overline{PN}$ MODE

1-BIT
DELAY

GATING SIG

672-1600
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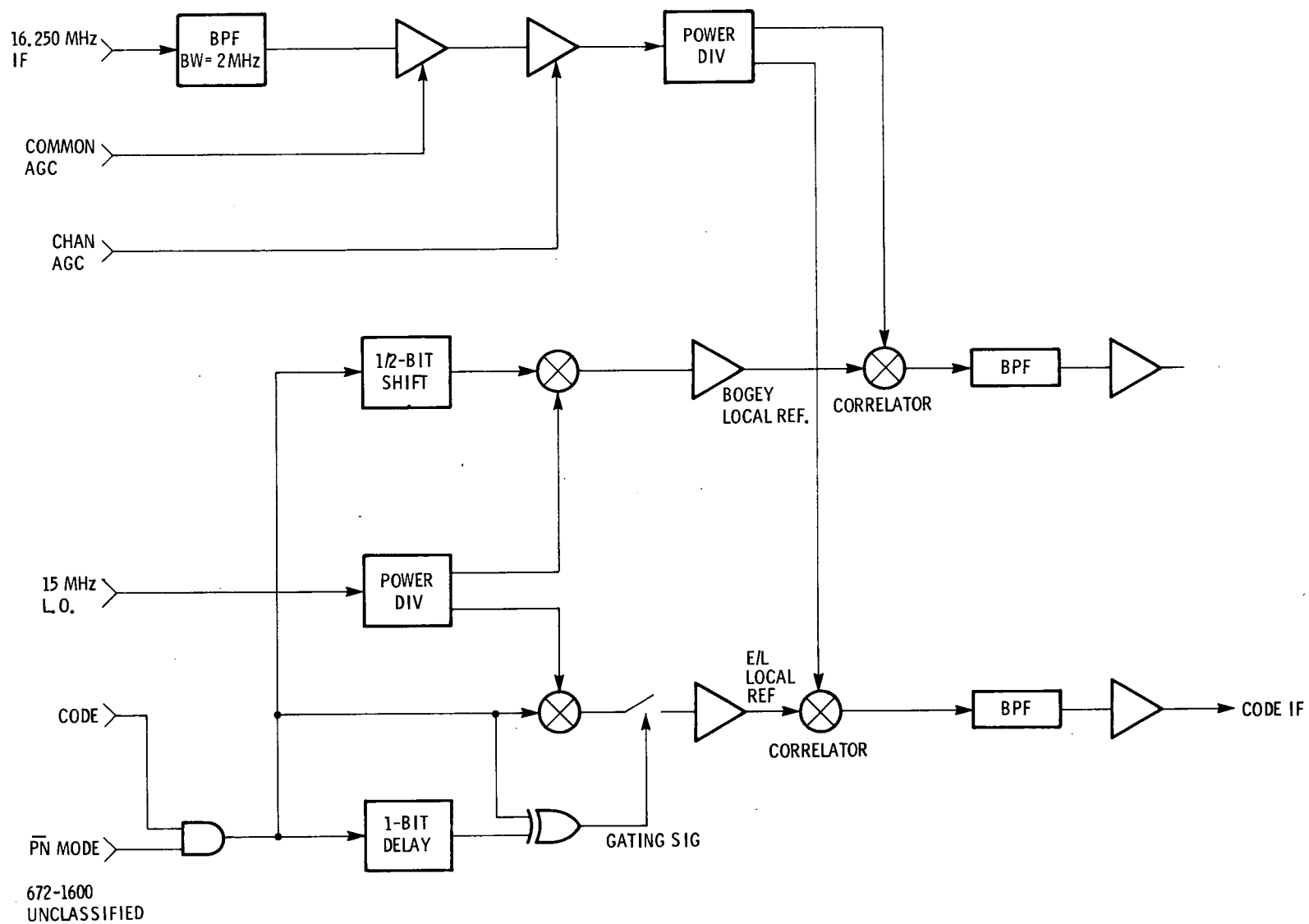
Figure 3-9. Block Diagram-Local Reference/Correlator

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Figure 3-10. Operating Characteristics of AGC Loop

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Figure 3-11. Correlation Process Waveforms

early code PN ($\tau/2$) (early and late codes are $\pm 1/2$ chip with respect to the bogey code).
Thus, if there exists a code displacement τ, the code-loop correlator output will be as
shown in waveform D, which when averaged yields a positive error signal. As
is varied, the so-called S-error curve depicted in figure 3-12 is generated. The figure
shows the desired error signal for code tracking.

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Figure 3-12. S-Error Curve

In the conventional mode, incoming carrier is not modulated by PN code. Thus, to operate the receiver, the local code is inhibited so that the carrier correlator functions only as a regular mixer. The code-correlator IF is not used.

3.2.4.1.2 Baseband Conditioner Board

The baseband processor (figure 3-13) consists of the final receiver mixing operation and low-pass filters, which reduce incoming signals to baseband or "zero" IF. The block diagram shows two separate third IF inputs and a fourth local oscillator, operating at four times the third IF or ≈ 5 MHz. The data third IF drives two high-level I and Q demodulators, supplied with references of quadrature phase, developed by different stages of the divide by four.

The second track third IF input is obtained from a separate track receiver channel, and contains PN code-tracking error information. This drives a third high-level demodulator using the same in-phase or I reference as the I data demodulator. Since the fourth local oscillator and third IF are the at same nominal frequency, the output of all three high-level demodulators will be the effective Doppler rate between the incoming signal and the internal precision reference.

A marginal, near-threshold signal will have a signal power of ≈ -16 dBm at the third IF inputs, while noise power will be $\approx +4$ dBm, measured in the 100 kHz third IF bandwidth. A gain of 10 dB is provided by the drivers, while the demodulators themselves convert the signals to baseband with very little loss (<0.5 dB). After filtering the now baseband signals are buffered by a unity gain noninverting amplifier, and bandwidth limited to 80 kHz. Total noise power will be $\approx +12$ dBm while the signal

G = 20 dB
BW = 10 MHz

G = 0 dB
BW = 80 kHz

Q2XD
DATA
FILTER

G = 0 dB
BW = .1-40 kHz

G = 19 dB
BW = 80 kHz

P_N = +19 DAM
P_S = +13 DAM

3RD
IF
DATA

DRV

PN = + 4 DBM
PS = -16 DBM

4TH
LO
(X4)

≈ 5.0
MHz

3 RD IF
≈ 1.25 MHz

3RD
IF
TRACK

DRV

DRV

÷ 4

DRV

BUF

BUF

BUF

LPA

LPA

LPA

ΔRC

12XD
DATA
FILTER

ΔRC

TRACK
DATA
FILTER

ΔRC

Q2XD
AMP

A

Q CARR
2XD

Q ACQ
FILTER

LPA

Q ACQ

ΔC

ACQ
BW

(5)

DATA
FET DRV

ΔC

LPA

I ACQ

I ACQ
FILTER

12XD
AMP

A

I DATA
2XD

TRACK
2XD

672-1610
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Figure 3-13. Baseband Conditioner – Block Diagram

power is $\approx$ -6 dBm. Since the PSK or clear mode requires demodulation of the GRARR 40 kHz subcarrier, the Q demodulator filter output is sent directly to the Q combiner as Q WB.

All three baseband demodulator filter outputs e.g., I DATA, Q DATA, and I TRACK, are now bandwidth limited by their respective data filters at twice the effective data rate. A closed-loop feedback type of single-pole active filter provides 6 dB per octave rolloff at corner frequencies that are two times higher than the incoming data rates. This assumes minimum interbit distortion and noncritical component selection. An arrangement of five FET switches select resistor and capacitor combinations as well as open-loop amplifier gain setting resistors to vary the corner frequency for each discrete data rate situation.

These twice-data (2XD) filters present a restrictive aperture to the total baseband noise power, and the signal-to-noise ratio is considerably enhanced. If marginal signal power is assumed to produce a signal-to-noise ratio of +10 dB in a matched data filter (BW = data rate), then the signal-to-noise ratio at threshold will be +7 dB at the output of the 2XD filters.

The twice-data or 2XD filter outputs drive their respective 19 dB gain 2XD amplifiers. The Q 2XD amplifier output is sent to the individual receiver carrier track loop, while the I 2XD amplifier output goes to the I combiner to extract data. Tracking channel or T 2XD amplifier output is sent to the track combiner to effect common code track.

Outputs of the I and Q 2XD data filters also go to the I and Q acquisition filters respectively. The bandwidth of these filters is set at 4 kHz or 12 kHz, depending on the Doppler acquisition mode selected. Two poles provide 12 dB per octave rolloff and +19 dB in-band gain. The noise power in the 4 kHz acquisition band-width is +19 dBm while the threshold signal power is +13 dBm, assuring the -6 dB minimum signal-to-noise ratio required for the 100 Hz BW Doppler processor scheme.

NOTE

4 kHz to 400 Hz = 10 dB

400 Hz to 100 Hz = 6 dB
S/N improvement   16 dB

S/N @ 100 Hz = S/N @ 4 kHz + 16 dB = +10 dB

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3.2.4.1.3 Carrier-Loop Filter and VCO Board

Each receiver channel requires its own independent carrier-loop filter and VCO board, since coherent demodulation is used to recover all data information. The carrier loop and VCO contains the carrier tracking loop filter and voltage-controlled crystal oscillator which supply the basic input reference for the carrier frequency synthesizer. The synthesizer in turn develops all receiver local oscillator signals by direct multiplication or division to assume perfect coherency.

The block diagram (figure 3-14) shows the carrier loop and VCO assembly receiving the baseband quadrature signal at twice the data rate (Q2XD) from the receiver channel. A switched differential amplifier is phase-alternated by the band-limited I combined (IcT^2L) drive applied to the FET input switches. This dedatatizer multiplies the Q2XD carrier error signal by Ic band-limited data to remove the data phase reversals from the error DC term, and allow build-up in the carrier-loop filter. During PSK or clear mode, the dedatatizer is disabled, since the Q baseband is data free due to the Manchesterized data in the PSK mode.

The carrier loop's tracking bandwidth is set at 20 Hz, which is high enough to provide adequate response for the acceleration of low-altitude satellites, while minimizing the tracking noise pertibations associated with greater loop band-widths. During acquisition, the loop bandwidth is increased to 80 Hz, to provide greater pull-in range and response. The large tracking loop capacitor is forced to assume the offset of the smaller acquisition filter, so that it can be inserted in the loop at sync without introducing a large velocity error. This forcing and switchover is effected by two FET switches or gates. An additional FET switch or gate shunts the normal integrator resistor to effectively reduce the time constant approximately five times. Since the ABC enable gate turns this FET on at ≈ 20 percent duty factor, the tracking-loop gain and bandwidth remains constant when operating in the ABC mode. The loop then becomes a sampled-data system by supplying the filter with short bursts of error and allowing the loop to "coast" between ABC bursts.

To keep the tracking loop bandwidth constant at 20 Hz, the open loop gain must be decreased when operating in the 401 MHz band to compensate for the increased VCO multiplier or ΔXN term. This ΔXN is proportional to the ratio of the high band

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Figure 3-14. Block Diagram - Carrier Loop and VCO

401 MHz to the average low band of $\approx$ 138 MHz. Open loop gain must therefore be reduced by $\frac{138}{401}$ 0.32 $\approx$ -5 dB, effected by changing the VCO buffer amplifier summing resistor with an FET driven by the 401 band select line. Another aspect of this 401 MHz band is the approximate three times increase in received Doppler uncertainty. The Doppler processor accommodates this greater search spectrum by increasing its effective frequency cell width from 100 Hz to 1000 Hz. Accordingly, the carrier loop must increase its pull-in range during acquisition to assure carrier lock or sync. Since the cell width is increased by a factor of 10, the analog Doppler correction velocity aid from the Doppler processor must also be scaled-up to properly shift the carrier VCXO to band center at acquisition. Another FET switch varies the scale factor of the Doppler correction into the VCXO summing amplifier to accomplish this.

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The remaining board area is devoted to the logic and FET drivers required to properly modify the carrier loops constants as defined above. Carrier loop characteristics may be summarized as follows:

Low-Data ACQ BW	80 Hz
High-Data ACQ BW	800 Hz
Tracking Bandwidth	20 Hz (constant)
Damping Factor	0.7 (constant)
Static Loop Gain	120 dB
Tracking Accuracy	3° (static)
Loop Type	I imp (2ND order) @rate aid

3.2.4.1.4 Sync/AGC Board

The common AGC and sync assembly is a dual unit, performing the AGC voltage development and sync determination for both receiver channels. In addition, a combined AGC voltage and combined sync decision is also included.

The block diagram (figure 3-15) shows two inputs from each receiver channel, the I 2XD and Q 2XD signals. These signals are held to ≈ 1 VRMS by the local AGC, and will have a signal-to-noise ratio of at least +7 dB. An absolute magnitude detector on each input develops a unipolarity output, regardless of the polarity of the data modulated input. In essence, this circuit acts like a precision fullwave rectifier and effectively squares the 2XD signal inputs. Since the I 4th mixer reference is in phase with the signal, the baseband I absolute magnitude output will be maximized during correct carrier track. Consequently, the Q 4th mixer reference is 90 degrees out of phase with the signal carrier and will produce zero output from the −Q absolute magnitude detector during proper carrier track. By algebraically summing these + |I| and − |Q| signals, a very reliable indication of carrier lock-on or Costas sync is provided when the I and Q combiner output is maximized. A sync decision is made by the sync comparator whenever the |I| − |Q| signal exceeds a preset threshold. Hysteresis and filtering in the sync comparator provides a smoothing effect which minimizes false decisions when noisy inputs are present.

Whenever the comparator threshold is exceeded, the sync lamp is activated on the receiver's front panel and a logic one is produced by the sync-logic OR gate.

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ABSOLUTE MAGNITUDE

RCVR #1
Q2XD

INV → FW RECT → BUF → - |Q|

DETECTOR

RCVR #1
MARGIN
METER

ΣA → COMP → DRV

|I| - |Q|

#1
SYNC
THRES.

RCVR #1
SYNC
LAMP

A-M DET

RCVR #1
I2XD

INV → FW RECT → BUF → + |I|

#1
AGC

LPA

RCVR #1
AGC

+ → LPA

COMBINE
AGC

COMB
AGC

OR

1 + 2
SYNC

A-M DET

RCVR #2
I2XD

INV → FW RECT → BUF → + |I|

#2
AGC

LPA

RCVR #2
AGC

ΣA → COMP → DRV

|I| - |Q|

#2
SYNC
THRES.

RCVR #2
SYNC
LAMP

A-M DET

RCVR #2
Q2XD

INV → FW RECT → BUF → - |Q|

RCVR #2
MARGIN
METER
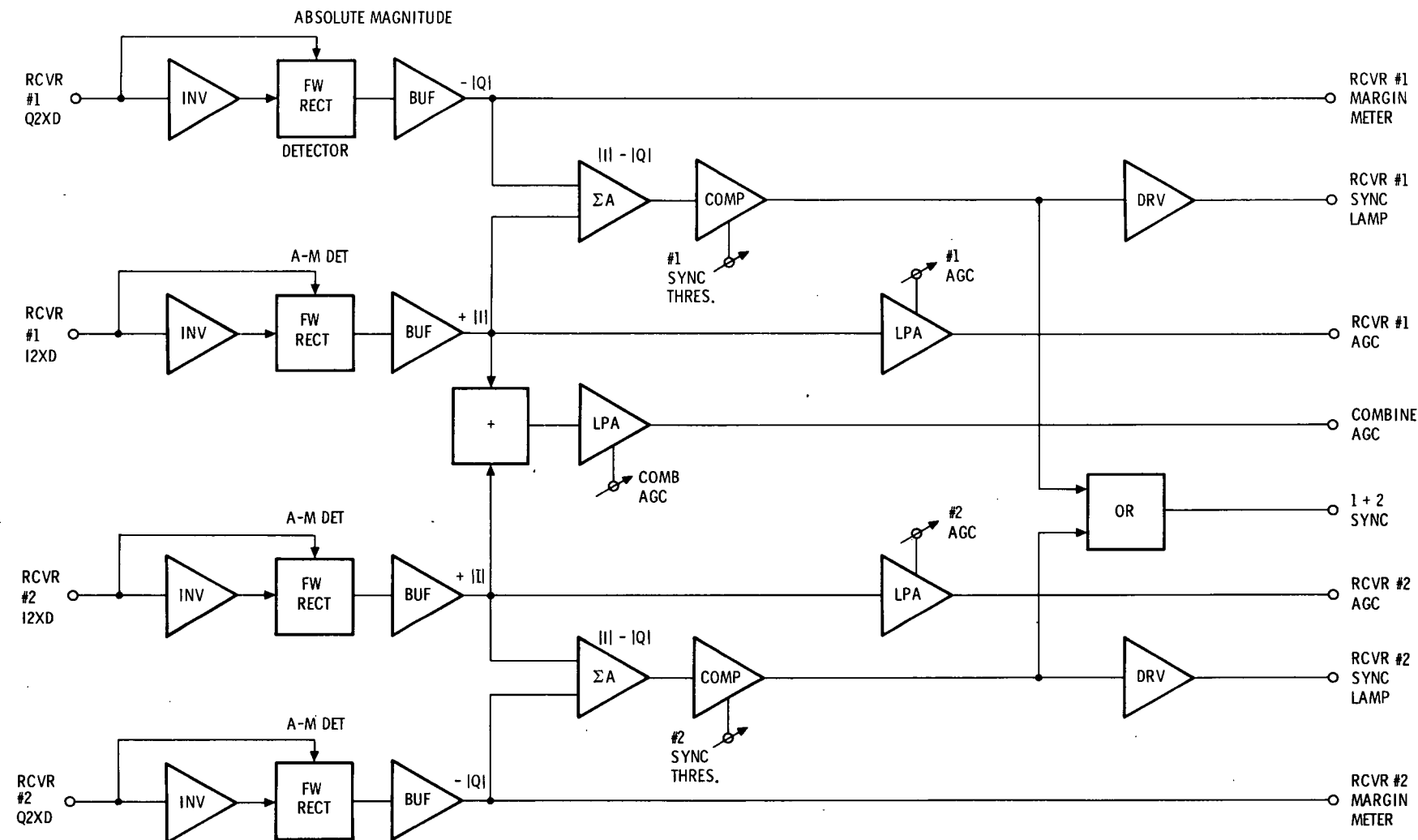
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Figure 3-15. Sync/AGC - Block Diagram

Since the Q absolute magnitude will be zero during good carrier track, a qualitative indication of the relative amount of noise can be conveyed by observing the threshold margin meter driven from the – |Q| detector.

The output of the I absolute magnitude detector is also used as an indication of signal strength and drives the individual receiver's AGC amplifier. The amplifier is scaled so that a 0 to -10 volt swing at the op amp output translates to a 0 to -1V swing at the receiver's AGC buss. A single zener diode in the amplifier's feedback hard limits its swing from +0.7V to -10V. The effective gain of the AGC amplifier is $\approx$ +25 dB once the threshold signal level is exceeded. The AGC loop carrier is set at $\approx$ 2 Hz by the AGC filter's time constants. Combined AGC is developed by simply summing the | I | signals of both receiver channels and processing it in a similar AGC amplifier/filter.

3.2.4.1.5 Doppler Processor Board

The Doppler processor is used in the multimode transponder to perform a Doppler frequency search in an accelerated time over a Doppler uncertainty range. The ranges to be covered are: 4 kHz at 100 Hz per step, which is operated in the 100 kilobits-per-second or 200 bit-per-second data mode, and the 16 kHz at 1000 Hz per step, which is operated in the 1 kilobits-per-second data mode only. The Doppler processor also provides a correctional voltage to the carrier and code tracking loop to aid in initial phase-lock acquisition. A simplified block diagram is shown in figure 3-16.

a. Mathematical Formulation

The pulse of unknown frequency can be represented as

$$P(t) = A \cos \left[(\omega_c + \omega_a)t + \theta \right] \quad o < t < T$$

where ω_c is the nominal center frequency and ω_a is unknown, uniformly probable over the range $\pm 2\pi W$. Assume WT to be an integer, M; if necessary by over estimating W slightly.

The first step in the progess is to bandpass filter the signal plus noise using a filter of bandwidth 2W centered at $\omega_c/2\pi$ Hz. The principal operation next performed is the computation of the Fourier coefficients of the filtered signal plus noise

Figure 3-16. Doppler Processor

on the interval (O, T). In particular, it is desired to compute the power in each component corresponding to frequencies in the filter passband. These quantities are the values of C_n^2 where

$$C_n = \frac{1}{T} \int_0^T f(t) \exp(-j2\pi n/T)dt$$

for values of n in the region $\frac{\omega_c T}{2} \pm WT$.

Alternatively, C_n^2 can be obtained through

$$C_n^2 = a_n^2 + b_n^2$$

$$a_n = \frac{1}{T} \int_0^T f(t) \cos 2\pi nt/T \, dt$$

$$b_n = \frac{1}{T} \int_0^T f(t) \sin 2\pi nt/T \, dt$$

In the mechanization it is necessary to store f(t) (which is P(t) + noise) at the filter output. This is conveniently done by resolving f(t) into its quadrature components, sampling and quantizing so that digital memory can be used. The quadrature components of f(t) with respect to a carrier at ω_c are $f_c(t)$ and $f_s(t)$ such that

$$f(t) = f_c(t) \cos \omega_c t + f_s(t) \sin \omega_c t$$

where

$$f_c(t) = A \cos (\omega_a t + \Theta) + n_c(t)$$

$$f_s(t) = -A \sin (\omega_a t + \Theta) + n_s(t)$$

in which n_c and n_s are independent Gaussian noise processes of zero mean, the same power, both bandlimited to the frequency interval (-W, +W). On the basis of sampling theory, it would be adequate to sample f_c and f_s at the rate of 2W samples per second, however, as a practical matter sampling should be at 3W to 4W samples per second to allow for non-ideal filtering and to improve the accuracy of the numerical approximations to the integrals. Call the actual sampling rate R, such that RT is a convenient integer. Amplitude quantization of the samples can be performed as crudely as one bit, however, this entails a loss of nearly 2 dB in the output signal-to-noise ratio. The use of 3-bit (8-level) quantization reduces this loss to a few tenths of a dB. The sampled, quantized values of $f_c(t)$ and $f_s(t)$ will be represented by F_c (m/R) and F_s (m/R) where the range of the integer m is 1 to RT corresponding to the range of t: $0 < t < T$.

Before writing a final expression for a_n and b_n, it is useful to note certain symmetries in the expressions for values of n spaced equally above and below the midband value, $\omega_c T/2$. To make these evident, let $n = k_c + k$ where $k_c = \omega_c T/2\pi$.

The range of k which is of interest is $\pm WT$. Making these changes in notation, approximating $f_c(t)$ and $f_s(t)$ by their sampled, quantized counterparts, and approximating the integrals by sums, we obtain:

$$a_{\pm k} = \frac{1}{2RT} \sum_{m=1}^{RT} F_c\left(\frac{m}{R}\right) \cos \frac{2\pi km}{RT} \pm \frac{1}{2RT} \sum_{m=1}^{RT} F_s\left(\frac{m}{R}\right) \sin \frac{2\pi km}{RT}$$

$$b_{\pm k} = \frac{1}{2RT} \sum_{m=1}^{RT} F_s\left(\frac{m}{R}\right) \cos \frac{2\pi km}{RT} \pm \frac{1}{2RT} \sum_{m=1}^{RT} F_c\left(\frac{m}{R}\right) \sin \frac{2\pi km}{RT}$$

Having computed the 2WT pairs of coefficients, a_k and b_k, the 2WT coefficients C_k^2 are formed. Since only one signal is sought, it is the maximum of all the C_k^2 which need be compared to a threshold to make the detection decision. Since the threshold setting should be proportional to the noise power, it may be convenient to set the threshold as a fixed fraction, β, of the noise power as estimated by the sum of all of the C_k^2. In the usual manner β is chosen to achieve a given false alarm rate, or a given detection probability for a given signal-to-noise ratio, or some similar basis.

b.   Mechanization

The computation of a_k and b_k are performed in two modes:

1.   R = 12,800 sample per second, T = 10 ms, and k ranges from −39 to +40. This is equivalent to having 80 filters each 100 Hz wide to cover the frequency uncertainty of ±4 kHz.

2.   R = 32,000 samples per second, T = 1 ms, and k ranges from −15 to +16. This is equivalent to having 32 filters each 1 kHz wide to cover the frequency uncertainty of ±16 kHz.

In the following only mode 1 is described since 2 is operationally identical to 1.

The first section of the mechanization concerns with obtaining and storing the F_c and F_s data. The F_c and F_s signals are the I and Q channel outputs, respectively, from the baseband signal processing module. These signals are converted to 3-bit words and sampled at the rate of 12,800 samples per second. Thus, for RT = 128,

a batch of data characterizing the signal over 10 milliseconds is obtained (i.e. 128 words each of 3 bits). The memory is of shift register type and consists of four 128-word x 3-bit sections, 2 for F_c and 2 for F_s. The two memory registers for each signal component are organized such that while one memory register is being loaded (gathering new data), the other is recirculating at accelerated rate for processing (computing a_k and b_k). The recirculating rate is 1,024 kHz so that 80 pairs of a_k and b_k are computed in 10 ms, which is the required time interval to gather a new batch of data by the other memory register. Thus, by alternating the two memory-register's functions, input signals are continually processed until the unknown frequency is found.

The computation of a_k and b_k requires the multiplication of data samples, F_c $(\frac{m}{R})$ and F_s $(\frac{m}{R})$ by the sine and values, $\cos (\frac{2\pi km}{RT})$ and $\sin (\frac{2\pi km}{RT})$ and summing the products. F_c $(\frac{m}{R})$ and F_s $(\frac{m}{R})$ are read out serially from the circulating memory register. The arguments for the sine and cosine are generated by decoding the 4 most significant bits of a 7-bit accumulator which starting at zero accumulates the value of k as m indexes from 1 to 128. (k increments each time m cycles until k ranges from -39 to +40.) At the end of the computation for a particular k, (i.e. at m = 128) the $C_k^2 = a_k^2 + b_k^2 \simeq (\sum R_m)^2 + (\sum J_m)^2$ is obtained and is presented to the "auctioneer". This is a register and comparator arrangement which is preset to zero at the start of each data batch and thereafter compares the present content of its register with the newly computed C_k^2. Whichever is greater is then stored in the register. Thus, at the end of a k cycle (i.e. as k goes through the range from -39 to +40), the greatest value of C_k^2 seen is left in the auctioneer. A final comparison is then made with β times the sum of C_k^2, which is accumulated in a separate register, to make the detection decision.

Having detected the presence of a signal as the Doppler processor scans the frequency range in one pass, the doppler processor employs a further decision strategy, whereby two out of three consecutive detections, called hits in the block diagram, are required to be declared a valid hit. This increases the true detection probability and decreases the false-alarm rate under the threshold condition of 10-dB signal-to-noise ratio in 100 Hz. At the conclusion of a valid hit, an analog voltage corresponding the detected Doppler frequency is sent to the carrier and code-loop VCO's. This voltage effectively drives the local-oscillator frequency to the input carrier for rapid acquisition.

3.2.4.1.6 Clock Loop Filter and VCO Board

The common clock-loop filter and VCO assembly (figure 3-17) receives Ic combiner outputs in both linear and T^2L (hard limited) form. The Ic TRK linear signal is developed in the track combiner, and represents the code tracking error or early-late displacement of the local and signal PN codes. The PN code tracking error is sensed in the I TRK receiver, combined with the I TRK signal of the other receiver signal and sent to the clock-loop filter and VCO. The block diagram shows the combined Ic TRK signal applied to a "dedatatizer" differential amplifier, which multiplies it with the hard-limited Ic T^2L to remove the data-phase reversals. This multiplier is similar to the dedatalizers used in the carrier loop. After removal of data, the Ic TRK code-error signal is applied to the code-loop amplifier. The code-track, error-detector, scale factor at this point is $\approx 2R/V$ when local receiver AGC is in effect.

Actually four independent loop filters are driven in parallel by this Ic TRK signal, with each properly scaled in regard to gain and response to complement its particular PN chip rate. Selection of 34.133K, 102.4K or 1.024M chip-per-second PN rate and one spare is provided by a four-input, programmable operational amplifier (PRAM), with commutated output. Output of this code-loop amplifier is summed with a similar four-channel, data-loop amplifier, either of which is enabled, depending on whether PN or PSK mode respectively is selected. The reason for varying the augmented DC gain of the loop amplifier for each PN chip rate is to compensate for the loss of open-loop gain due to the increasing $\div N$ of the VCO. This $\Delta \div N$ results from the VCO division process in the clock-frequency synthesizer, from the 10.00 MHz VCO to the selected PN chip note. The $\div N$ term increases from ≈ 10, to ≈ 100 and then ≈ 300 to generate the 1,02 MC/S, 102 KC/S and 34 KC/S PN chip rates respectively. By individually setting the DC gain and rolloff capacitor of each loop amp, the desired 2 Hz tracking bandwidth and 0.7 damping factor is maintained regardless of PN chip rate.

The output of this four-channel, loop amplifier is enabled during PN mode, and is applied to the VCO summing amp. An IC VCO is used, which is essentially a free-running multivibrator, with provision for externally varying the charging voltage and thereby producing VCO operation. The very nature of the device makes it very sensitive to frequency control voltage, power-supply voltage, and temperature variations. It is therefore necessary to slave or "crutch" this VCO to some reference frequency before it could possibly be used for PN code search and acquisition. Crutching

is accomplished prior to acquisition by forcing the divide-by-two or ≈ 5 MHz clock VCO into coincidence with the 5-MHz carrier VCXO, by means of an external input. An IC combination frequency discriminator and phase detector literally pulls or slews the unstable VCO to the correct frequency, and then assumes a modulo II operation to hold exact phase coherency. This PLL is effective by unlimited pull-in range, completely independent of the "crutch" PLL bandwidth. Once the clock VCO is tracking the carrier VCXO, virtually coherent carrier-clock operation is established, and a matched clock Doppler is impressed on the PN code during Doppler search. At the instant of a Doppler search "hit", the local PN code is static with respect to the signals code, since the PN clock is now coherent with the signals carrier Doppler. This provision greatly improves the reliability of the entire Doppler processor search and acquisition operation.

At carrier acquisition or Costas sync, the crutch loop is opened-up by a FET gate, and the VCO continues to receive a memorized error term from the crutch loop filter. The loop-amplifier capacitor and FET source follower input will provide a relatively indefinite memory term to the VCO, certainly for the duration of the satellite pass. The combination of the memorized long-term crutch offset and an external Doppler-correction voltage from the Doppler processor will provide an open-loop "push" to the clock VCO. This tends to relax the dynamic requirements of the actual PN code-track loop, since the VCO offset and estimation of Doppler offset are provided external to the loop.

The PN code tracking of the clock VCO is used only during the PN mode of operation. Since the data clocks are derived and are synchronized by the PN code's master reset, no data-clock tracking is necessary in PN. In the PSK and ABC modes, however, derivation and phase tracking of the received data clock is required, since no PN code is available.

The block diagram (figure 3-17) shows a second set of four loop amplifiers enabled during the PSK mode. This group comprises the data-clock-loop amplifier used to phase track the data clock, and synchronize the clock-frequency synthesizer. Inputs to this loop amplifier are obtained from the common data recovery board as data clock error signals. Three decades of data rate plus PDM voice are accommodated by the four individual loop filter-amps. The VCO clock divide down or ÷ N

Figure 3-17. Clock-Loop Filter and VCO Block Diagram

for the data rates are larger than the PN chip rates, being ≈1000, 10,000 and 100,000 for the 10 kilobits-per-second, 1000 bits-per-second and 100 bits-per-second data decades r decades respectively. The data-clock-error loop contains a fixed 20-dB, voltage bits-per-second gain amplifier to make a gross adjustment in open-loop gain to account for this large VCO ÷ N factor. Additional augmented DC gain must be inserted by the loop amplifier to provide a clock tracking bandwidth of a constant 20 percent of data rate for each data decade.

Each individual loop amplifier gain and rolloff is selected to maintain the loop bandwidth of 20 Hz, 200 Hz and 2 kHz for the 100-bits-per-second, 1000-bits-per-second and 10-kilobits-per-second rates respectively. The loop-amplifiers lead or breakout corner is selected to produce a 0.7 damping ratio at the lowest rate in each decade. Since typical data decades will comprise a X1, X2, X3 and X6 discrete rate increase, the fixed breakout will produce a damping ratio of 0.7 at X1, increasing to ≈2.0 at X6 within the decade. This increase from optimum to somewhat over damped seems permissible, considering the almost total lack of dynamic excursions in the apparent data rate experienced by the clock loop.

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The fourth loop filter accepts clock error from the PDM clock PD. This is a T^2L digital mod II exclusive "or" gate, which uses the Ic T^2L combiner output and a 1/2 x data clock to develop phase error. After filtering, it goes to the voice loop-amplifier which provide a 2 kHz tracking bandwidth for the 10-kilobit-per-second PDM voice suppressed carrier data demodulator.

The remainder of the clock loop and VCO board is devoted to suitable logic required to decode the data-rate and PN chip-rate-select lines and enable the appropriate data and PN loop filters respectively.

Clock loop characteristics may be summarized as follows:

CODE

Tracking Bandwidth	2 Hz
Static Loop Gain	120 dB
Tracking Accuracy	±0.01 Bit
Damping Factor	0.7
Loop Type	I imp (2^{nd} order)

DATA

Tracking Bandwidth	20 percent data rate
Damping Factor	0.7 to 2.0
Static Loop Gain	120 dB
Tracking Accuracy	±3 degrees static
Loop Type	I imp (2^{nd} order)
	@rate aid

3.2.4.1.7 Controller Board

The MMT controller board searches the receiver coder to obtain correlation, detects the 31-bit Legendre sequence in data sent from the MTAR and sends a 7-bit Barker sequence to the MTAR and switches from forced data and chip rate to selected value.

A 31-bit sequence is used to tell the MMT that the MTAR receiver is in sync because the probability that the random data being transmitted by the MTAR before its receiver is in sync will duplicate the sequence is only one in 3×10^4. A 7-bit Barker sequence is sent back from the MMT to initiate the switch to final

data and chip rates because no data will be transmitted by the MMT until after this switch has taken place and therefore, a long sequence is not required. The 7-bit sequence serves only to eliminate possible false switches due to impulse-type noise interference.

There are three different search states that the system may be in when both receivers are out of sync. The first search state is reached when the receivers have both been out of sync for some time and there have been no "hits". A hit is defined as a decision made by the Doppler processor boards that the signal level is one of the Doppler frequency offset slots is high enough to be a legitimate signal. In this search state, the controller sends a step command to the appropriate IPM every time the hit clock from the Doppler processor is received. The IPM will retard the phase of the receiver coder by 1/2-chip interval every time it receives a step command from the controller. This process is continued until the Doppler processor determines that it has a hit. Once the controller receives this information it advances the coder phase one half chip and waits for two more hit-clock times. The controller must advance coder phase this amount because the hit information given to it by the Doppler processor is delayed one hit-clock interval from the actual code correlation point.

The process of determining that the code is phased properly continues by monitoring the Doppler processor two out of three hit line. This line tells the controller that at two out of three bit clock edges the Doppler processor has found a positive indication of a received signal which correlates with the locally generated code and has the same Doppler frequency offset as the other hit. By doing this the Doppler processor reduces the probability of a false indication of code correlation greatly.

Once the controller has received the two out of three bits signal for the first time, it remembers this information by setting a flip-flop and causing the receiver coder phase to advance approximately 2 ms in time. A counter is also loaded at this time. This counter receives the same pulses used to step the coder phase. It is used to remember where the initial two out of three hits signal was received.

After the 2-ms phase advance the second search state has been reached. The controller again retards the phase of the coder 1/2 chip at a time looking for first one hit and then two out of three hits. If it receives these signals before the

counter used to keep track of the coder phase has gone past the original sync indication point the second sync indication is considered to be a good one. That is, not only is the sync indication valid but any multipath reflection within 2 ms of the direct path signal has been bypassed by this search strategy. Even though the search process might have started just behind the direct path signal the receiver will still end up at the direct path signal correlation point since the amplitude of multipath reflections delayed more than 2 ms is sure to be so low that correlation will not be detected by the Doppler processor.

After this second search state has been completed, the controller will either enable the receiver to lock up if the second two of three hits has occurred in the 2-ms interval or the system will go back to the original search state if the counter monitoring coder phase indicates that the original correlation point was passed without another indication of correlation.

When two indications of correlations are found in the 2-ms interval under discussion, the controller enables the correction of the VCO's (carrier and code tracking) frequency to remove the Doppler offset frequency. This process may be repeated more than once depending upon the linearity of the VCO's frequency-versus-control voltage characteristic. The sync/AGC board examines the I and Q signals and determines if either receiver is legitimately in sync.

At the same time that the controller enables the VCO Doppler offset frequency corrections, it fires a 1/4 second single shot. If sync indication is not produced within 1/4 second, the controller continues the previous search process since that length of time is sufficient for the VCO's to lock to a legitimate signal.

Once system sync has been reached it is monitored until it is lost which surely will happen at least once per revolution of the user satellite around the earth. When lock is lost the controller goes into the third search state which is a short search around the last valid sync point. This search is repeated four times and if correlation is not detected the controller goes back to the first search state.

3.2.4.1.8 Code and Data-Clock Synthesizer Board

The code and data-clock synthesizer boards provide signals used by the coder, receive conditioner, transmit data processor, and convolutional encoder boards. These signals are:

    a.   The forward link coder clock

    b.   The reverse link coder clock

    c.   Eight times the receiver data rate

    d.   Four times the transmitter data rate

There are two synthesizer boards in the MTAR but only one in the MMT. In the interest of minimizing the number of unique boards, the synthesizer was designed so that it be used in three different slots performing somewhat different functions in each one of them.

Starting with the forward-link transmitter of the MTAR there is one synthesizer board driven by a crystal oscillator at 10.24 MHz. This synthesizer board provides a coder clock at either 102.35 kHz or 34.1166 kHz to the PN coder and four times the transmitted data rate to the transmit data-processor board. When the system is in PN mode the data-rate clock is derived from the coder chip rate. This process guarantees that the transmit and receive data clock will be phased properly once the receiver coder is in sync with the received signal. Thus the requirement for a separate data clock tracking loop in addition to the code tracking loop is eliminated.

By referring to figure 3-18 which is the functional block diagram of the synthesizer board, it is seen that there is considerable ambiguity in the phase relationship between the coder clock and the data rate clock.

Since these two clock frequencies are derived by separate countdown chains operating from the 10.2 MHz source the relative phase of the two signals can move in approximately 100-μsecond increments with respect to each other. This ambiguity is resolved by resetting all of the data-clock counters with the master reset pulse which is derived from the MTAR transmit coder for the particular board under discussion.

Figure 3-18. Code and Data Clock Synthesizer Board - Block Diagram

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This master reset pulse, which reoccurs every 120 ms is used to phase all of the counters in the chain that produces the transmit data clock. After the first occurrence of this master reset pulse it will no longer produce any changes in the MTAR transmitter since the frequency source is fixed and the transmitter coder does not have to be slowed in time.

Since the coder repetition is 2047 bits long there is a problem in the gradual "walking" of the coder repetition with respect to an exact 100 Hz signal. This problem is solved by dropping a pulse to the coder countdown chain every 2048 cycles of the 10.24-MHz source. This clock dropping process changes the average clock frequency applied to the coder, so that it seems to be dividing by 2048 in terms of the original source frequency of 10.24 MHz. This technique is necessary because of the sensitivity of short sequences such as 2047 bits to the addition of even 1 extra bit. . This extra bit may change the correlation properties of the sequence drastically.

In the MMT there is only one synthesizer which drives both the receiver and transmitter coders and the data rate counter chains. This synthesizer is driven by a VCO whose frequency is shifted from 10.24 MHz by the amount of Doppler frequency shift present on the received signal modulation. Since the MMT is a coherent transponder it must also shift its transmitter coder clock the same amount. That is the reason that only one 10.24 MHz oscillator is required in the MMT.

In order to be able to search the receiver coder, a device called an IPM is used. IPM stands for Incremental Phase Modulator and describes a digital circuit which is capable of shifting the phase of its output signal by some fraction of a cycle for every pulse applied to its input. By so doing, it is possible to shift the phase of the coder driven by such a device until it comes into correlation with the received signal.

In the MMT, the divide-by-four IPM is used to search the receive coder. The divide-by-ten IPM is used only as a portion of the counter chain. In order to guarantee identical phasing between the receive and transmit coders this divide-by-ten IPM must be reset by the MMT master reset pulse which is derived from the receiver coder. Thus, the phases of the transmit coder, the receive data clock, and the transmit data clock in the MMT are determined by the receive coder master reset pulse.

The second synthesizer board in the MTAR is used to provide receiver code and data clocks. It is driven by a crystal VCO which has to track the Doppler offset on the return link signal. In this location the divide-by-ten IPM is used to search the

receive coder and the master reset pulse from that coder is used to reset the data clock countdown chain. Thus, the data clocks are tied to the coders all the way around the transmission path in PN mode operation.

In either PSK or ABC modes there are no coders operating. In this case the data is manchestered and the receiver synthesizer boards become part of a data clock tracking loop. The majority of the circuitry on the synthesizer board is no longer required in these modes.

3.2.4.1.9 MMT Frequency Synthesizer Boards

The MMT frequency synthesizer (figure 3-19) consists of two boards which are used to generate the corrected frequencies for use in the MMT transponder. The outputs of the MMT boards no. 1 and no. 2 are specified in table 3-2.

Table 3-2. Specifications of MMT Frequency Synthesizer Outputs

	Frequency in MHz	Power Level in dBm	Minimum Spur Isolation in dB	Use
MMT Board No. 1		TTL Squarewave	N/A	Reference
MMT Board No. 2	60.00*	+4 ± 1 dB	>50 dB	C-INJ-1
	81.25*	+4 ± 1 dB	>50 dB	B-INJ-1
	84.00	+9 ± 1 dB	>50 dB	INJ-2
	137.00	+5 ± 1 dB	>40 dB	TX-LO
	333.25*	+5 ± 1 dB	>50 dB	A-INJ-1

*Output phase must be adjustable to a minimum of ± 45 degrees.

a.   MMT Board No. 1

The MMT board no. 1 is almost identical to the MTAR board no. 1 with two major exceptions. The first exception is that the output of the BPA-7 does not drive PG-2 directly but through a power divider; the other output of the power divider is supplied to MMT board no. 2 for further synthesis operation. The second exception is that the 5 MHz buffer (EF) has been deleted and a hard limited 5 MHz output is added.
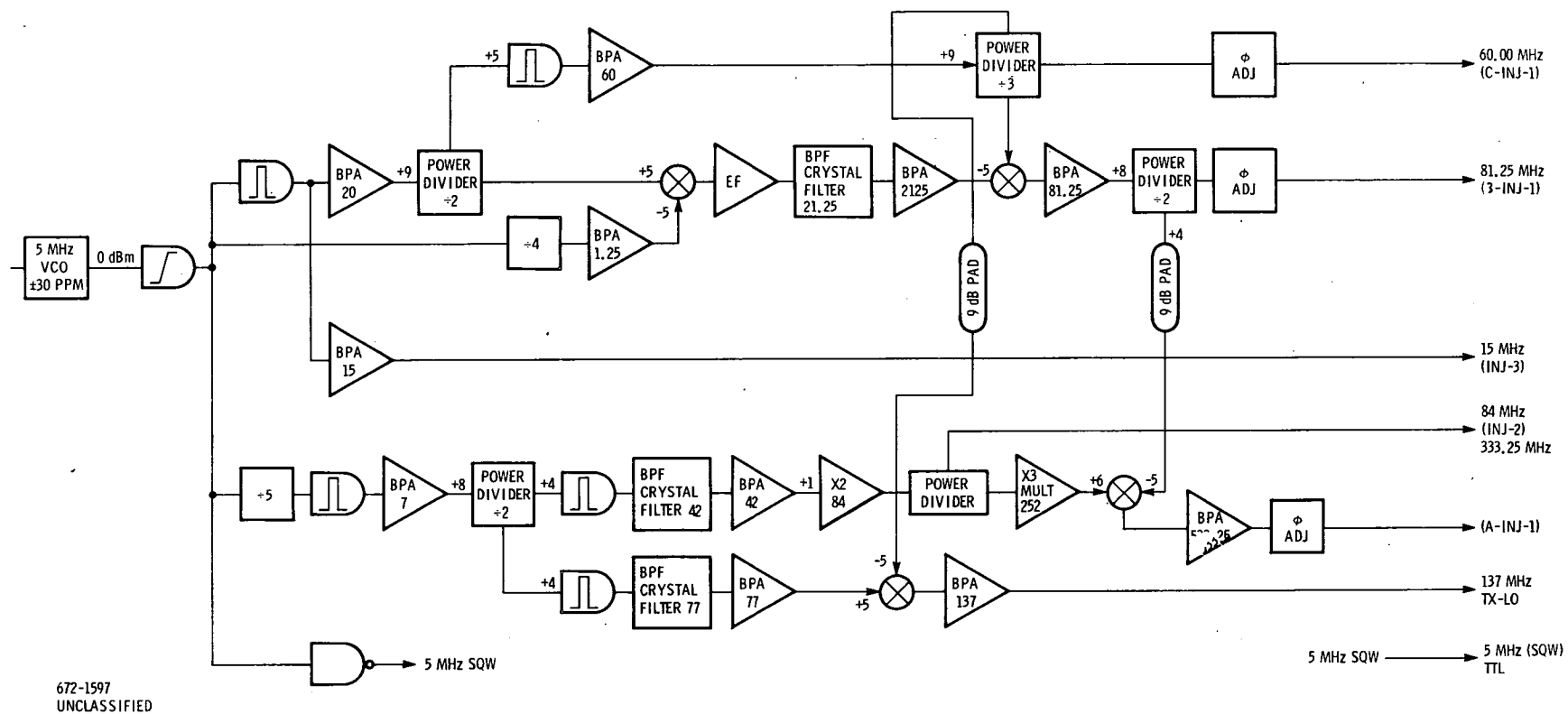
Figure 3-19. MMT Frequency Synthesizer

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b.   MMT Board No. 2

The MMT board no. 2 supplies the 15 MHz (ING-3), the 84 MHz (ING-2) and the 137 MHz (TX-LO); it also supplies the phase adjustable outputs 60 MHz (C-ING-1), 81.25 MHz (B-ING-1) and 333.25 MHz (A-ING-1). The following is a listing of each output on the MMT Board No. 2.

Output	Description
60 MHz Output (C-INJ-1)	The MMT board no. 2 simply provides phase adjustment for the 60 MHz supplied by MMT board no. 1 . PA-1 will allow a phase adjustment of the output a minimum of ± 45 degrees.
81.25 MHz (B-INJ-1)	The 81.25-MHz output is synthesized in two basic mix and amplify steps. The first step is to generate 21.25 MHz from 20-MHz and 1.25-MHz. The mixer M1 inputs 20-MHz and a 1.25 MHz signal; it outputs the sum and difference of the input frequencies. Since only the sum is desired it is necessary to filter (BPF - 21.25) and amplify (BPA - 21.25) to obtain the desired 21.25-MHz signal. The second step is to mix 21.25 MHz and 60 MHz (supplied by MMT board no. 1) in M2 and select only the sum 81.25 MHz. This is accomplished by the amplifier BPA - 81.25. The 81.25 MHz is applied to the phase adjuster PA-2 through the power divider PD-1. The output of PA-2 is the 81.25-MHz output B-INJ-1.
84 MHz Output (INJ-2)	84 MHz supplied by MMT board no. 1 is applied to PD-2. One output of PD-2 becomes the board output INJ-2.
137 MHz Output (TX-LO)	The 137 MHz is synthesized in two basic steps. The first step multiplies 7 MHz (supplied by MMT board no. 1) to 77 MHz by the rectangular pulse technique. The second step is to mix and amplify the sum of 77 MHz and 60 MHz (supplied by MMT board no. 1) using M4 as the mixer and BPA-137 as the amplifer.

Output	Description
333.250 MHz Output (A-INJ-1)	The 333.25 MHz output is generated in two basic steps. The first step multiplies the 84 MHz, supplied by PD-2, times three to 252 MHz. The second step is to mix and amplify the sum of 252 and 81.25 MHz using M3 as the mixer and BPA - 333.25 as the amplifier. The 333.25 MHz which is the output frequency of BPA - 333.25 is applied to PA-3. PA-3 allows the output phase of 333.25 MHz to be adjusted a minimum of ±45 degrees.

3.2.4.1.10   Receive Coder Board

Figure 3-20 is a block diagram of a receive coder. The transmit coder diagram is similar with the addition of a coder-start input line and the removal of the CRP and MRP phased output signals. The PN coder consists of two 11-stage shift registers with feedback to generate a pair of maximal length codes that are combined to form the Gold code structure. To provide for multiple access and to extend the length of the code, the initial condition of the lower pseudonoise generator (PNG) is modified by both a five-stage counter on the board and chassis wiring external to the board. This chassis wiring selects a group of Gold codes from the total of 2047 of them available for the particular coder mechanization. The five-stage counter is used to provide a code repetition period of either one, two, or twenty times the repetition time of a straight 2047-chip code. It accomplishes this by ingesting one, two, or twenty different initial conditions in the lower PNG (figure 3-20) everytime the upper PNG repeats. The repetition of the upper PNG is detected by an 11-input AND gate which looks for the all-ones state in the 11 flip-flop in the upper PNG. This all-ones vector occurs only once to every 2047-chip time. The all-ones vector causes a new initial condition to be injected into the lower PNG and supplies the five stage counter with clock. At the three different chip rates, the upper PNG has repetition times of 60, 20, or 2 ms. The five-stage counter by injecting different initial conditions modifies the shorter code repetition period to 40 ms. The code then becomes either two or twenty different Gold codes each of which is 2047 chips long.

The Gold code generator is useful because of the large number of codes it supplies while requiring only one pair of feedback tap sets. The Gold codes are generated by modulo-2 addition of a pair of maximal linear sequences. Every phase portion between the two maximal linear generation (PNG) causes a new sequence to be generated.
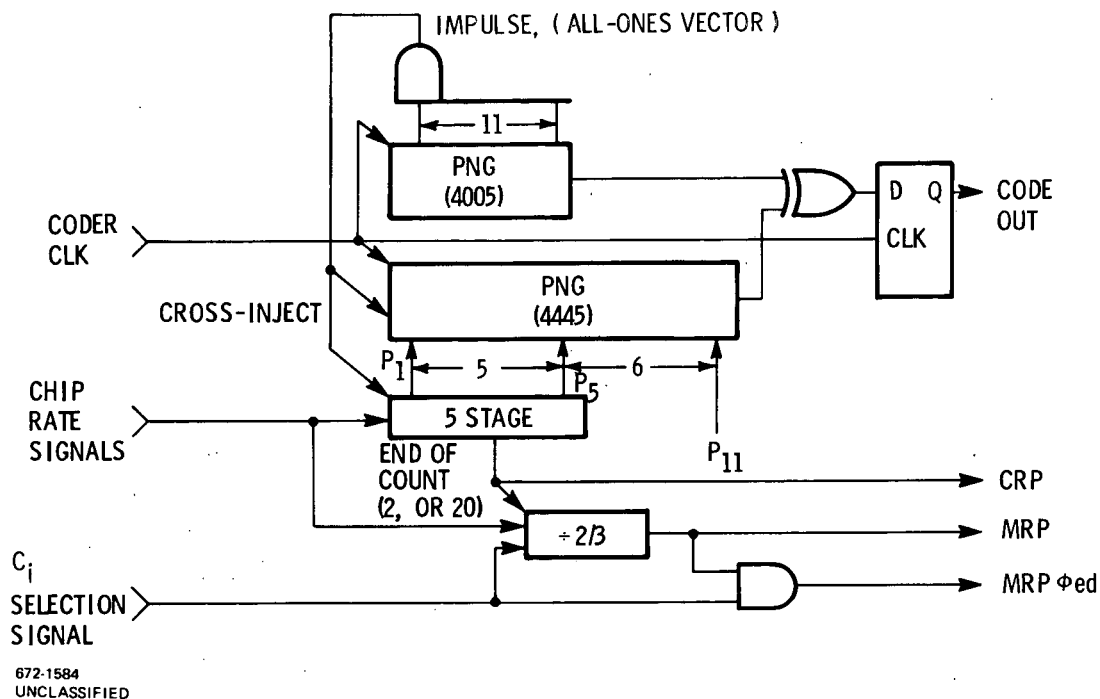
Figure 3-20. PN Receive Coder

The basic 11-stage maximal sequence generators are flip-flop sequence generators. This method of code generation is the simplest known and results in (1) the minimum number of components, (2) increased reliability, and (3) decreased power requirements.

The divide-by-two or -three counter shown at the bottom of the block diagram serves to generate the master reset pulse (MRP) every 120 ms. This pulse is used for synchronizing the data countdown chains at both ends of a link as well as providing the signals used for ranging at the MTAR. The master reset pulse occurs every second code repetition at a 34K-chip rate and every third code repetition (not the upper PNG repetition) at either 100K- or 1M-chip rates. Since at the MMT it is possible to be receiving with a basic repetition rate of either 40 or 60 ms and transmitting at either 60 or 40 ms, some method of transferring phase information around the complete ground terminal to user satellite back to ground terminal loop is needed. By using a repetition period of 120 ms it is possible for the phasing information to be

transmitted around the loop without any ambiguities despite the various coder chip rates possible. Thus, a comparison of the transmitter and receiver master reset pulses at the MTAR will provide satellite range information simply by determining the elapsed time between these two pulses.

3.2.4.1.11 Diversity Combiner Board

The diversity combiner module (figure 3-21) contains all the necessary circuitry to perform maximal-ratio combining of the I and Q channel signals from two diversity receivers. Specifically, the function to be performed is depicted in figure 3-22.

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CONDITION	$\overline{S}_2$	$\overline{S}_1$
$\hat{A}_1 > 1.4\,\hat{A}_2$	1	0
$0.4\,\hat{A}_2 \le \hat{A}_1 \le 1.4\,\hat{A}_2$	0	0
$\hat{A}_1 < 0.4\,\hat{A}_2$	0	1
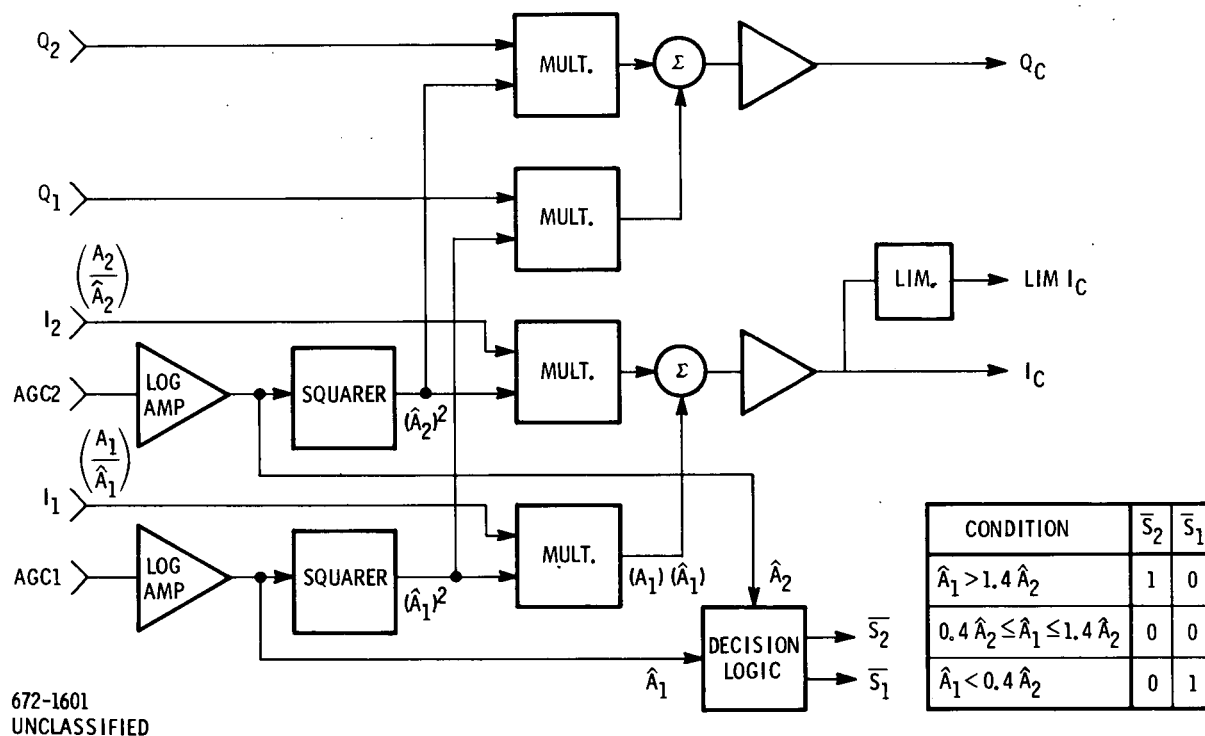
Figure 3-21. Diversity Combiner Board - Block Diagram

$$\frac{\sqrt{P_n} + MA_1}{\hat{A}_1} \longrightarrow \boxed{X} \qquad (\hat{A}_1)^2$$

$$\frac{\sqrt{P_n} + MA_2}{\hat{A}_2} \longrightarrow \boxed{X} \qquad (\hat{A}_2)^2$$
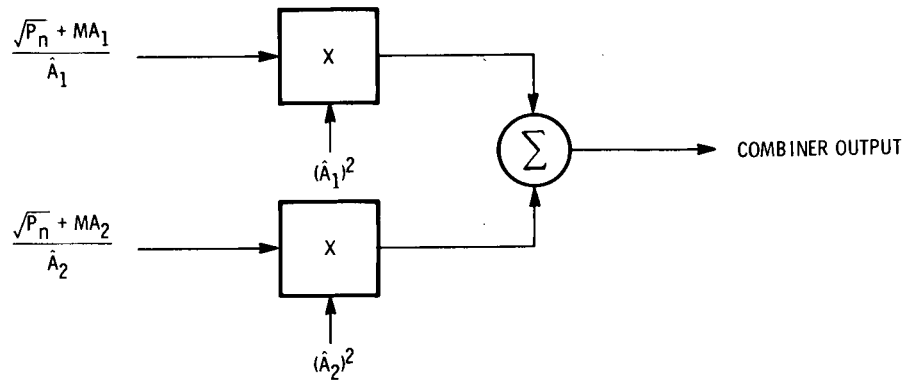
Figure 3-22. Diversity Receiver Combining

Where P_n is the received noise power in each receiver; $M = \pm 1$ is the digital modulation; A_1 and A_2 are the received signal amplitudes; and $\hat{\mathbb{A}}_1$ and $\hat{\mathbb{A}}_2$ are the local estimate of A_1 and A_2, respectively. At the combiner output, the signal power $(I_s)^2$ is:

$$(I_s)^2 = (A_1 \hat{\mathbb{A}}_1 \quad A_2 \hat{\mathbb{A}}_2)^2$$

While the noise power $(I_n)^2$ is:

$$(I_n)^2 = P_n (\hat{\mathbb{A}}_1^2 \quad \hat{\mathbb{A}}_2^2)$$

The signal-to-noise power ratio is, therefore:

$$S/N = \frac{(A_1 \hat{\mathbb{A}}_1 \quad \hat{\mathbb{A}}_2 A_2)^2}{P_n (\hat{\mathbb{A}}_1^2 \quad \hat{\mathbb{A}}_2^2)}$$

Which yields improvement over the S/N of a single channel receiver.

In addition to maximal-ratio combining, the diversity combiner module also contains circuitries to perform switching-diversity combining of code-error signals. The switching function is carried out by a decision circuit in accordance with the following logic:

(1) If $\hat{\mathbb{A}}_1 > 1.4 \, \hat{\mathbb{A}}_2$, only receiver #1's code error signal is used in the code tracking loop.

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(2) If $\hat{A}_1 < 0.4 \, \hat{A}_2$, only receiver no. 2 is used,

or   (3) If $0.4 \, \hat{A}_2 \le \hat{A}_1 \le 1.4 \, \hat{A}_2$, both receivers are equally combined and used.

The AGC amplifier used in the receiver has a transfer characteristic depicted in figure 3-23.
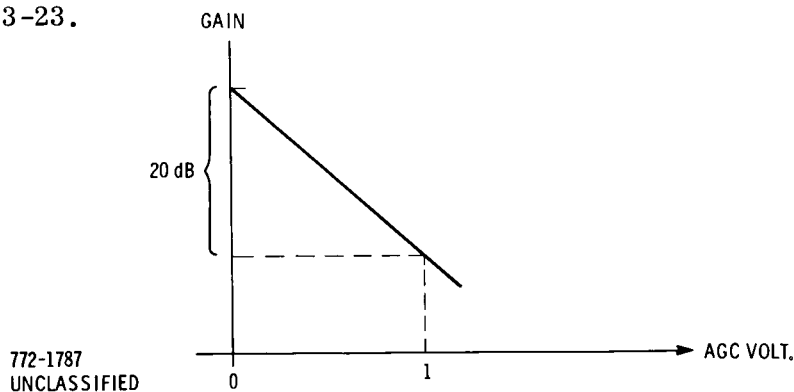
Figure 3-23. AGC Amplifier Transfer Characteristic

If X = AGC voltage, then, operation of the AGC loop will always normalize the input signal amplitude A such that $(A/10^X)$ = constant in the I and Q channels. Therefore, to derive $\hat{A}$ (i.e., the estimate of A), the AGC voltage X is amplified logarithmically so that $\hat{A} = 10^X$.

The logarithmic characteristics of the amplifier are approximated by three linear segments as shown in figure 3-24.
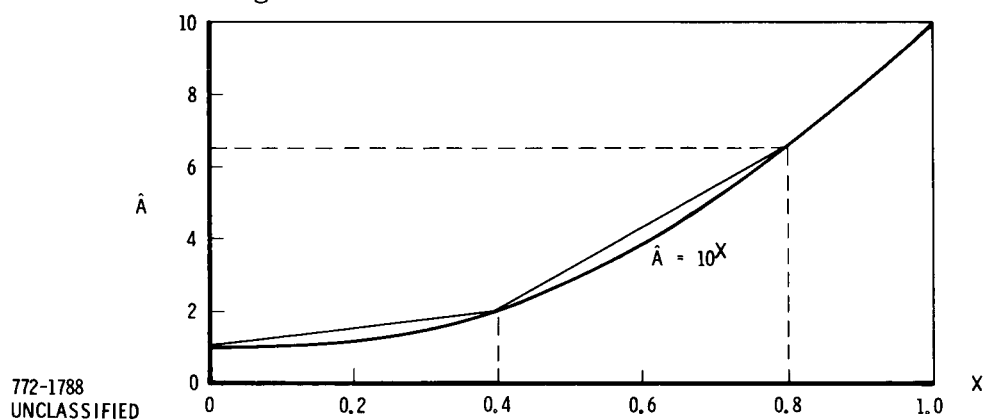
Figure 3-24. Amplifier Logarithmic Characteristics

To obtain $(\hat{A})^2$, a four-quadrant analog multiplier circuit is used as shown in figure 3-25.

772-1851
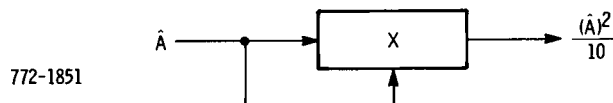
Figure 3-25. Four-Quadrant Analog Multiplier Circuit

Once $(\hat{A})^2$ is available for each received signal, maximal-ratio diversity combining can be accomplished readily with additional analog multipliers to perform $\left(\dfrac{A}{\hat{A}}\right) \times (\hat{A})^2$ and a summing amplifier for the final result.

There are two sets of such circuits, one for I-channel which carries the digital data and the other for Q-channel which carries GRARR signals.

To derive the logic signals for switching diversity combining, $\hat{A}_1$ and $\hat{A}_2$ are applied to two voltage comparator circuits whose buffered outputs, designated as $\overline{S}_1$ and $\overline{S}_2$, satisfy the following:

Condition	$\overline{S}_2$	$\overline{S}_1$	Function
$\hat{A}_1 > 1.4\,\hat{A}_2$	1	0	Select $R_x 1$ only
$0.4\,\hat{A}_2 \leq \hat{A}_1 \leq 1.4\,\hat{A}_2$	0	0	Select $R_x 1$ and $R_x 2$
$\hat{A}_1 < 0.4\,\hat{A}_2$	0	1	Select $R_x 2$ only

$\overline{S}_2$ and $\overline{S}_1$ are used in the clock loop filter and VCO board for switch-diversity combining and are also in the MMT modulator board to select the "best" carrier (i.e., either receiver No. 1's T_x carrier or receiver no. 2's) for transmission in the return link.

3.2.4.1.12 Data Recovery Board

Data recovery (figure 3-26) is common to both receiver channels and is supplied with signals from the I combiner. This assembly must extract the biphase data modulation on the combined I signal, as well as deriving the data clock in the PSK or clear mode.

Figure 3-26. Data Recovery - Block Diagram

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The block diagram shows two inputs from the I combiner. The I_c linear input is the product of linear addition operations and contains all the instantaneous phase and amplitude components of the signal plus noise in a twice data-rate (2xD) bandwidth. Since the 2xD filter presents a restrictive aperture to the total noise power, the signal-to-noise ratio is considerably enhanced and approaches 7 dB. Signal and noise power will vary considerably depending on the relative contributions of the two receiver channels as determined by the optimal combining hierarchy.

The I_c linear signal must be "demanchesterized" in the PSK or clear mode to remove the data clock from the data intelligence. This operation is similar to the carrier reinsertion for suppressed-carrier demodulation in conventional communication work. The local data clock alternately flips the phase of the I_c signal by switching the two FETS "on" sequentially. This acts to multiply-out the clock and leave only the basic data information. During PN operation, this multiplier is disabled and no phase alteration is performed in the demanchesterizer. At twice data bandwidth, the raw data is still fairly corrupted by noise, having a signal-to-noise ratio of +7 dB.

Final data bandwidth enhancement is performed in a virtually perfect matched filter, the integrate and dump.

An active integrator is composed of a high-speed operational amplifier with a FET switch across its capacitor. At the beginning of each bit interval the FET switch is opened, allowing the integrator capacitor to assume a change. All signal and noise amplitude components are integrated during the bit time. If a data one is present, the integrator will gradually recover the DC component of the data bit and assume a definite positive charge. Naturally, the longer the charge interval, the more positive the ultimate charge will become.

The data comparator continually monitors the polarity of the integrator charge, and effectively decides whether the data interval was a one or zero. At the end of the data-bit interval the reclock flip-flop is clocked and its output will assume the instantaneous sense of the data comparator. By selecting the integrator's time constant to complement the basic data rate the effective filter bandwidth becomes the reciprical of the bit interval, which is considered near optimal. Since the data-bit sense decision is withheld until the end of the bit interval, the reclocked or "clean" data is delayed by one bit.

It is now necessary to clear-out the accumulated integrator charge, allowing it to accept the next bit interval. The dump FET is pulsed "on" by the dump one-shot monostable flip-flop for the maximum time required to completely discharge the integrator capacitor. Two switched FETs select this dump interval by changing the one-shot's timing capacitor as a function of data rate.

The second combiner input is the I_c limited or T^2L signal. This hard-limited signal plus noise is either digital one or zero, depending on the instantaneous amplitude of the I_c signal. By hard limiting this signal, the large I_c signal level variations (>10:1) are effectively normalized and it may be considered as a constant amplitude. A constant amplitude input is very desirable in any phase-lock loop since it keeps the closed-loop response essentially constant, allowing optimal selection of the PLL parameters. Accordingly, the data clock PLL uses this I_c input to recover the data clock during PSK or clear mode.

Since the I_c limited signal is of T^2L format, no information is conveyed by its amplitude, and only sense and duration are meaningful. This allows a digital form of phase detection called the "sniffer" PD. During PSK mode, a local data clock is developed by counting the clock VCO. The one-times data clock is generated in quadrature with the data clock used by the demanchester multiplier described above. This clock is phased such that it is logical one during the I_c limited signal's data-bit transition, and is anded with the I_c and $\overline{I}_c$ signal. These enabled I_c and $\overline{I}_c$ are applied to FET drivers, which in turn activate the FET switches associated with a differential amplifier similar to the demanchesterizer. Only during the expected I_c data transitions will either FET be switched off, depending on the sense of the I_c input. The "sniffer" PD will assume the polarity of the I_c signal during transition interval and will go to zero during the 50 percent data interval when no transition is occurring. Thus, an effective three-state, bipolar signal is developed with a positive weight for a I_c one, a negative weight for I_c zero, and a zero weight for the interval between data transitions. Symmetrical data transitions will produce equally wide positive and negative levels about zero, and will therefore contain no DC component, regardless of the actual data makeup.

By essentially enabling or sampling phase error only during expected data transition, the noise rejection performance of the phase-lock loop is considerably improved, especially in marginal signal-to-noise ratio situations. This three-state error signal is applied to an identical integrate and dump circuit as the data described above.

There will be a buildup of the clock integrator when a phase error exists between the local data clock and the I_c data transitions. This buildup will be at maximum at the end of the data bit interval, just prior to the integrator dump or reset. The local data clock activates a sample one-shot which in turn initiates the integrator dump one-shot. The sample FET is closed briefly just prior to the dump one-shot to reestablish the change on the hold capacitor. This capacitor then holds the error change over the next data bit interval before being resampled. Thus, a sampled-data servo delay is established that complements the one bit data delay introduced by the data reclock flip-flop described above. The voltage follower unity gain amplifier presents an extremely high input resistance to the hold capacitor, thereby minimizing the loss of change from sample to sample. Total time for sample and dump operation is less than 5 percent of the data-bit time worse case, and represents less than -0.2 dB threshold deterioration.

It is now necessary to remove the bipolar data from the clock error analog before sending it to the clock error combiner. An analog dedatatizer multiplier similar to the demanchesterizer and "sniffer" PD is used, with FETs driven from the reclocked clean data. The necessity for complementry one bit data delays in the dedatatizer FET drives and input error sample is readily apparent.

Quadrature drives for the demanchesterizer and sniffer PD multipliers requires a local ÷ 4 clock divider. In addition, encoding and manchesterizing considerations may double or quadruple the effective data rate. It is therefore necessary to divide the data clock from an eight-times clock generated in the clock frequency synthesizer to accommodate all possible data modes. The master-reset pulse is differentiated and used to initialize all clock countdown flip-flop to assure positive synchronization of all functions.

Front panel data rate and mode select lines are brought into the data recovery assembly, where local logic enables the proper clock-divide-down and data select FET drivers. These drivers are used not only on this assembly but are also sent to the baseband processor for the 2xD filter's cutoff frequency selection.

3.2.4.2   MMT Transmitter

The following is a functional description of each type of printed wiring board used in the MMT transmitter.

3.2.4.2.1 MMT Modulator Board

The MMT modulator board (figure 3-27) has three modes of operation:

1.   PN Mode - The data to be transmitted is first modulo-2 added to a PN code. The resulting signal then balance-modulates a 137 MHz carrier to generate a PSK, spread spectrum signal for transmission.

2.   Conventional PSK Mode - Digital data balance-modulates one phase of a 137 MHz carrier, while GRARR signals balance-modulates another 137 MHz carrier which is in quadrature with the former. The two PSK signals are then summed with an unmodulated carrier to generate the final modulator output. The composite signal in phasor representation is shown in figure 3-27.

UNMODULATED CARRIER (π/2)

DIGITAL DATA PSK CARRIER (π/2, $-\pi$/2)

GRARR PSK CARRIER (0, π)

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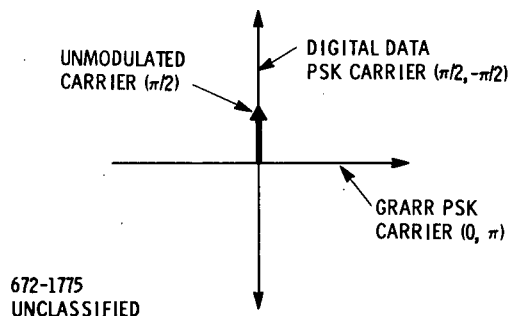
Figure 3-27. Composite Signal in Phasor Representation

Since digital data are coded in Manchester form and lowest GRARR tone is 4 kHz, there is no carrier component contributed by either PSK signals. Thus, at the receiver, the transmit unmodulated carrier will be tracked so that digital data appear at the I-channel and the GRARR signal at the Q-channel.

The power division between the PSK signal and the unmodulated carrier in the data channel is 4:1. That is, 20 percent of the total data channel power is used for carrier tracking. This results in roughly a 2-dB loss relative to the case where all power is allocated to data and carrier tracking is accomplished with a Costas loop.

3.   ABC Mode - The modulator operates identically as described in the conventional mode except with the additional requirement that the transmit signal be gated on and off in accordance with the ABC burst format. This is accomplished in the balance modulator by gating on and off the local oscillator with the ABC gating signal.

To select the carrier signal for transmission from the two diversity receivers, the switching logic signals from the diversity combiner are used. The selection is as follows:

S_2	S_1	Carrier Selected
1	0	RCVR #1
0	0	RCVR #1
0	1	RCVR #2

Selection of RCVR No. 1 carrier for $S_2 = 0$ and $S_1 = 0$ is entirely arbitrary, for under this condition both carriers are equally usable and RCVR #2 could have been selected instead.

To keep the modulator total output power constant as its operating mode changes, the modulator output is fed back through an AGC loop to regulate the carrier level. For block diagram of the MMT modulator see figure 3-28.

3.2.4.3   Baseband

The following is a functional description of each type of printed wiring board used for baseband signal processing in the MMT. Figure 3-29 shows the receiver baseband data flow. The switches shown are controlled by front-panel mode selection.

3.2.4.3.1   Data Processor Receive Board

The data processor assembly contains the PSK or clear mode ranging tone GRARR demodulator and the output-data differential decoder. In addition, necessary logic is included to transfer the data decoder and PDM demodulator from the PN or PSK data output to the ABC data output.

The block diagram shows data and clock outputs from the PN/PSK and ABC systems being switched by the appropriate mode select lines. The differential decoder output is the ultimate receiver data output available externally. External data clock is also available. The PDM data is sent back to the clock loop and VCO assembly for clock extraction and to the PDM demodulator assembly for conversion to analog voice signal. Since all data at this point is T^2L, the multi-pole, double throw switches become simple three-gate, NAND/NOR, digital-logic elements.
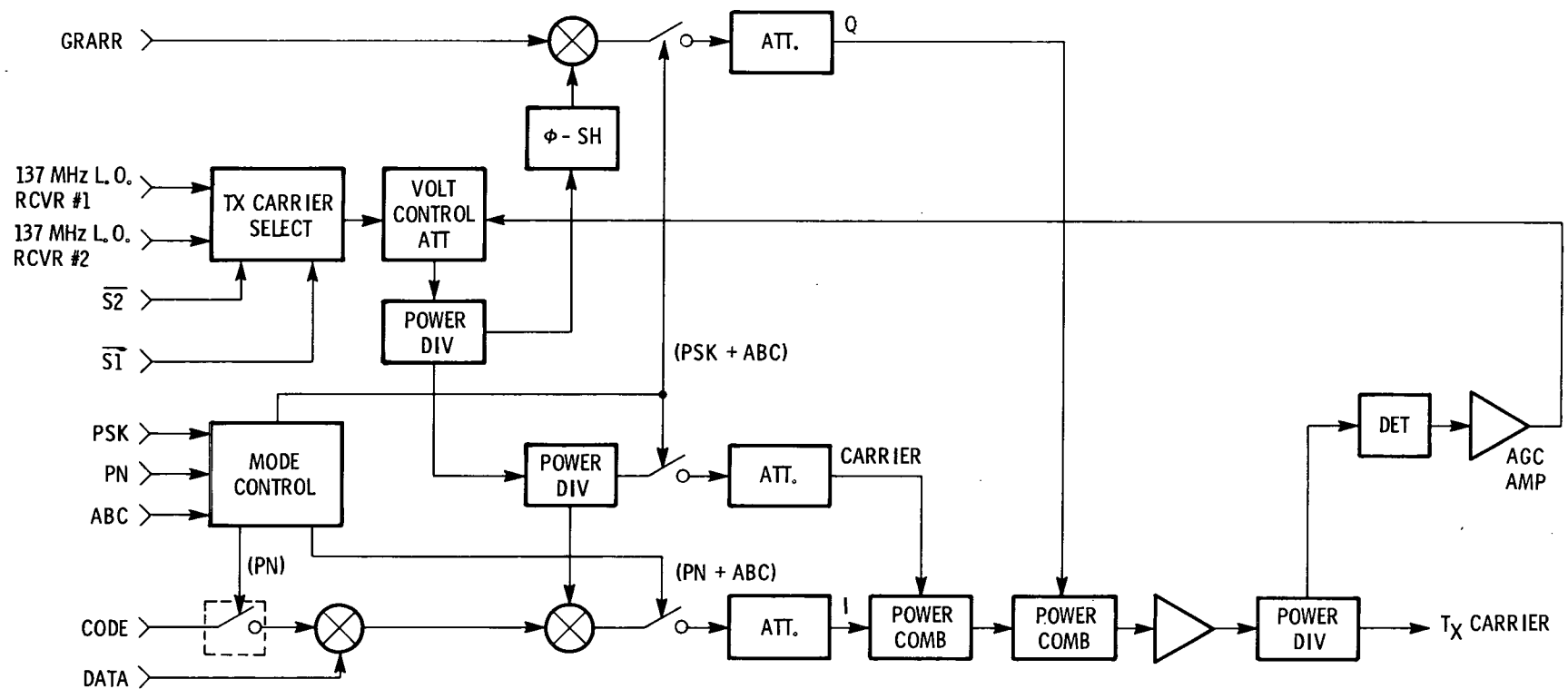
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Figure 3-28. MMT Modulator - Block Diagram
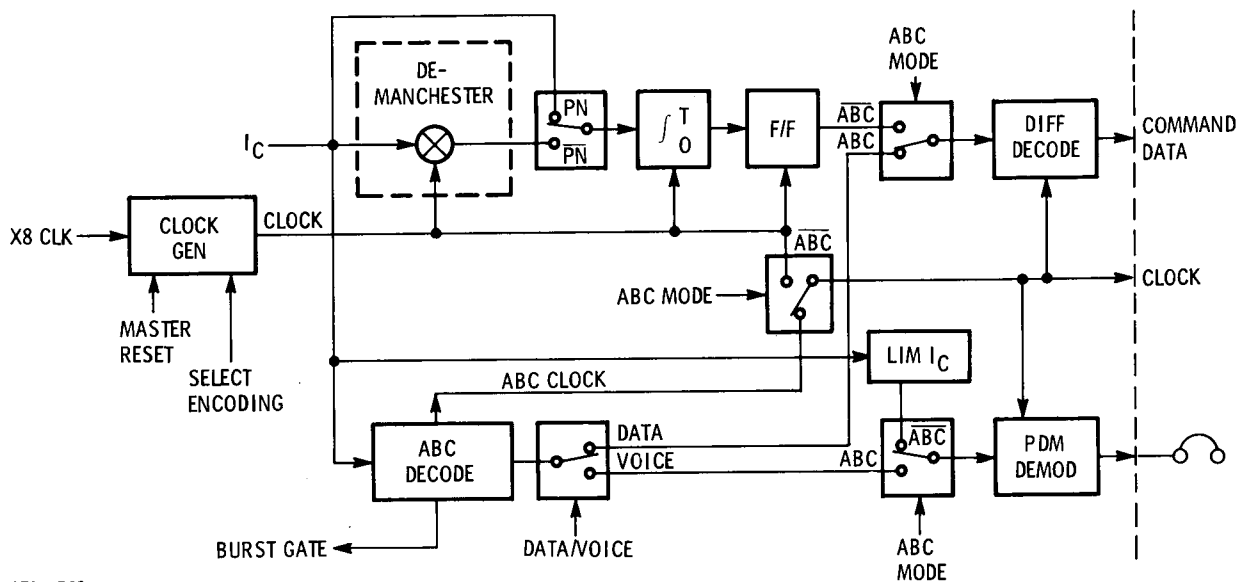
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Figure 3-29. MMT/MTAR RCVR Data Flow Diagram

The major portion of the data processor assembly is devoted to the range tone or GRARR demodulator. Since the GRARR tones are digitized at the transmitter with a 40-kilobits-per-second clock, they can be considered as data and recovered in similar manner as the I_c data recovery. They are impressed in quadrature with the I_c data on the PSK carrier and transmitted as a quadrature 40-kHz sideband simultaneous with the data information. It is therefore necessary to employ a completely independent data demodulation and clock recovery system soley for this GRARR tone detection.

Combined receiver quadrature signals Q_c WB are derived ahead of the twice data filters (2xD) to retain the 60-kHz bandwidth required to recover the 20-kHz GRARR tones on the 40-kilobit-per-second subcarrier. The Q_c WB or Q combined wideband signal is buffered and applied to the data integrate and dump, and also to the clock "sniffer" PD, for clock extraction. The time constants for the data and clock integrate and dump are optimized for the 40-kilobit-per-second data, and require no data change provision.

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In operation, the GRARR data and clock recovery system is similar to the I_c data system, except that there is no demanchesterizer multiplier, and the clock "sniffer" PD uses the same Q_c WB linear signal as the data integrate and dump.

3.2.4.3.2 PDM Voice Receive Board

The suppressed-clock PDM demodulator block diagram is shown in figure 3-30. A Costas loop tracks the suppressed PSK carrier and synchronously demodulates the PDM carrier. The recovered SCPDM signal is modulo-2 added with the 10-kHz PDM clock divided by 2.

The recovered PDM signal is processed (see figure 3-31) by an integrate-and-dump filter which makes the optimum estimation of the transmitted signal. The sample-and-hold circuit remembers the final value of the integrate and dump circuits (i.e., immediately before the integrator is dumped). The output of the S and H is the recovered audio in a PAM format. The PAM signal is processed by the voice conditioner which provides deemphasis, low-pass filtering, and buffering into a 600-ohm line and a headset output.

It should be noted that the critical aspect of the total demodulation process is the acquisition of the clock and its insertion in proper phase. This process is inherent in a PN system since the PDM clock is generated from the above source on the PN code clock. As long as PN correlation is maintained, a phase coherent PDM clock is available for PDM demodulation.

a.   Audio Processing

The audio input signal is transformer-coupled into a preemphasis network. The audio preemphasis increases the gain at a 6-dB-per-octave rate between 600 Hz and 3500 Hz.

The preemphasized audio is followed by the AGC amplifier, from which the signal is fed into the speech-compressor clipper. The speech-compressor output goes through the 3.5-kHz, low-pass filter. This active filter provides a five-pole Legendre response with a 3-dB point of 3710 Hz and 20-dB relative attenuation at 5 kHz.

The maximum low-pass filter output is approximately 4.0 v p-p, centered at -2.00 VDC. This offset is required for proper PDM modulator operation. The filtered audio drives a precision rectifier to control the audio AGC amplifier. A direct

RECOVERED CLOCK	
RECEIVED DATA	
OUTPUT 1 OF FLIP-FLOP	
OUTPUT OF EXC.-OR GATE	
OUTPUT OF I & D	
OUTPUT OF SAMPLE & HOLD	
AUDIO INPUT	
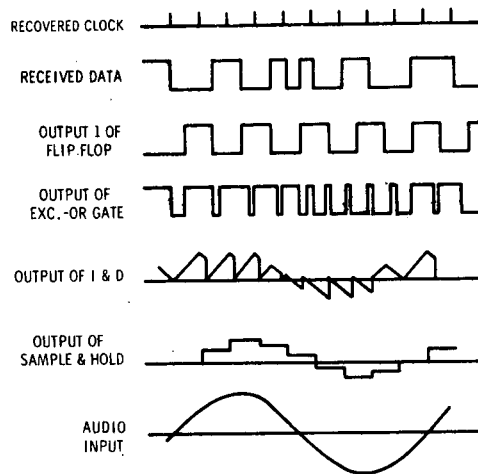
Figure 3-30. Demodulator Waveforms

voltage selected by a potentiometer controls the low-pass filter output level and also controls the depth of compression, since this is directly related to the output voltage of the speech processor.

The speech compressor is a differential amplifier which supplies a constant output clipping level regardless of operating temperature. The changes in compressor gain caused by varying temperature are compensated for by deriving a feedback signal from the speech compressor to the AGC circuit.
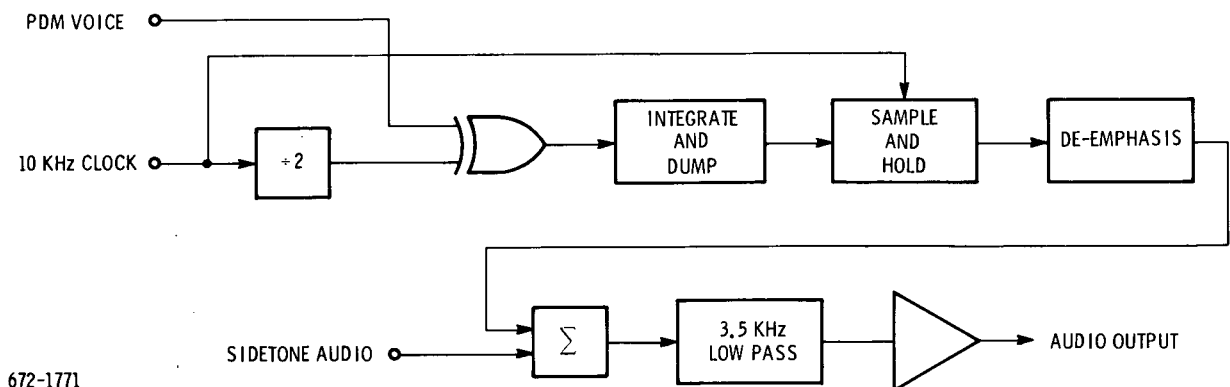
672-1771
UNCLASSIFIED

Figure 3-31. Suppressed Clock PDM Voice Receive - Block Diagram

3-67

The AGC amplifier provides constant output signal (±1 dB) for any input signal between 80 mV RMS and 1V RMS, providing a 22 dB AGC range. For applications in installations with high ambient noise, the audio input level control is adjusted to set the background noise level at least 6 dB below the AGC threshold. The AGC time constants are set for nominal attack and release times of 100 ms and 2 seconds respectively.

b.   PDM Modulator

The speech processor output drives a sample and integrate circuit. The audio is sampled at a 10-kHz rate and the samples are applied to a capacitor which is also driven by a constant current source. The audio samples always result in negative voltages between 0 and -4V on the capacitor. The constant current source then pulls the capacitor back above ground. A comparator switches state each time the capacitor voltage crosses zero. The time interval between negative and positive zero crossings is a linear function of the input signal, generating a pulse-duration-modulated (PDM), 10-kHz subcarrier. A -2.00V prebias of the low-pass filter output ensures that the PDM output is a squarewave if no audio is present.

A 5-kHz clock, derived from the input 10-kHz clock by division, is modulo-2 added to the PDM signal. This process removes the stationary, redundant clock edges from the PDM, producing the suppressed clock pulse duration modulated (SCPDM) signal.

Sidetone transmit audio is provided as an input to the receive audio amplifier to facilitate operator function. The sidetone audio may be defeated by operating the sidetone audio switch on the modulator circuit card.

3.2.4.3.3   Data Processor Transmit Board

The function of the data processor transmit board is described in figure 3-32, transmitter data flow diagram. The differential and manchester encoding and the switch functions shown are performed by this board.

Figure 3-32 shows the path of baseband signals from source input to the modulator. The MX-270 is clocked by the MMT and generates the digital data for error-rate measurements. The digital data from the MX-270 can be used directly or go through the convolutional encoder. The audio input is converted to PDM with the
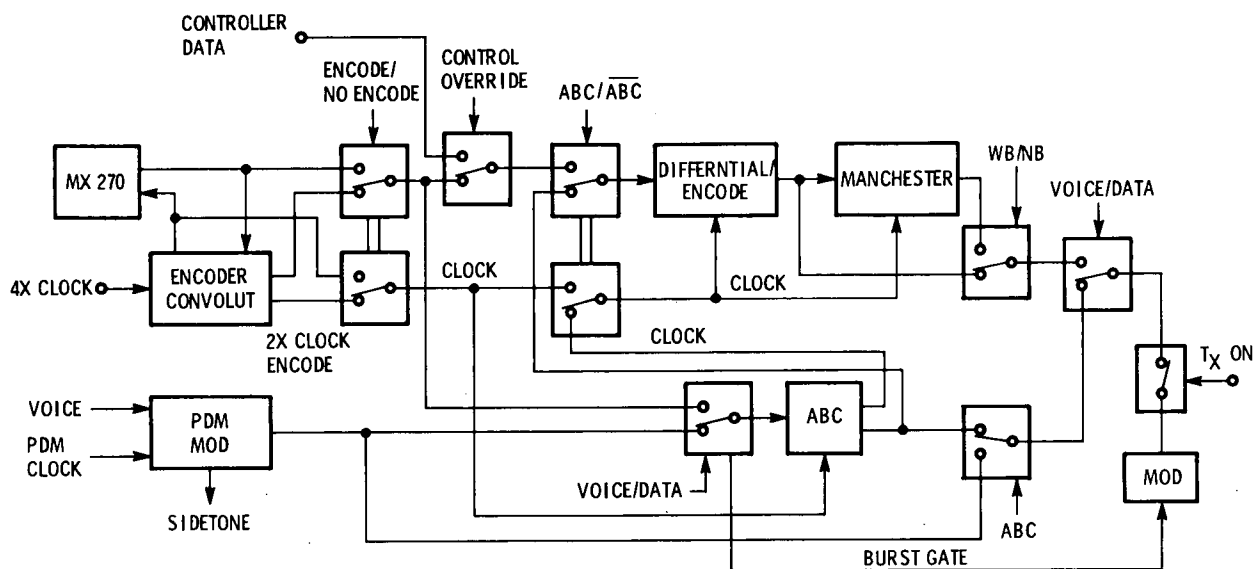
Figure 3-32. MMT XMTR Data Flow Diagram

clock supplied from the code and data clock synthesizer board. Either PDM voice or digital data (at the selected bit rate) is sent to the modulator. The switching to supply the appropriate clocks for ABC bursting, differential encoding and manchester encoding is also shown in figure 3-32.

3.2.4.3.4 PDM Voice Transmit Board

A block diagram of this suppressed clock PDM modulator is shown in figure 3-33. Speech conditioning consists of a preemphasis network, AGC, a compressor and a 3.5-kHz lowpass filter. The audio AGC circuit ensures a high index of modulation while the compressor increases the effective modulation.

A sample-and-hold circuit takes very short samples (1 microsecond) and holds them for a sample period. A ramp generated from the 10 kHz clock and a comparator constitute the PDM modulator. The modulo-2 addition of PDM and 5-kHz squarewave removes the clock transitions from PDM and results in suppressed carrier PDM.
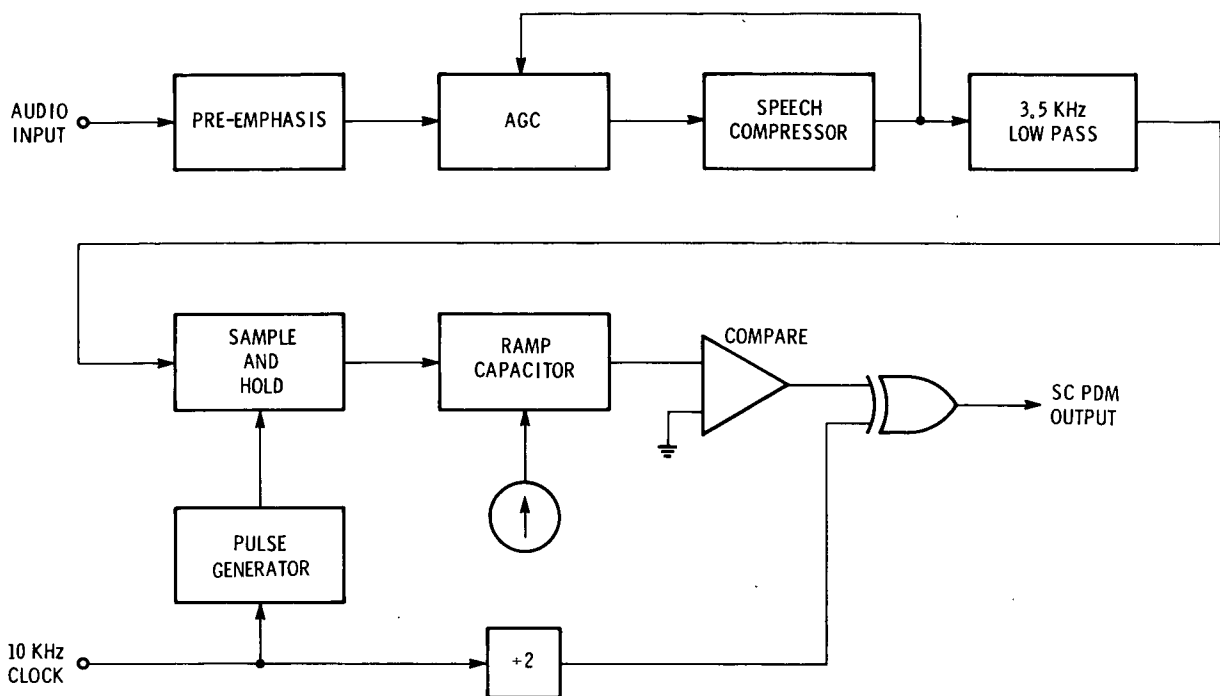
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UNCLASSIFIED

Figure 3-33. Suppressed Clock PDM Voice Transmit - Block Diagram

Figure 3-34 shows the waveforms at each significant point in the modulator, assuming a single tone at the input. The input audio is sampled and held, and compared with a sawtooth signal generated from the sampling clock. The comparator output is a pulse-duration-modulated (PDM) clock signal. The regular recurring (rising) edges of the PDM waveform are suppressed by modulo-2 addition with the half-clock signal. The resultant SCPDM binary signal keys 180-degree phase-shift modulation of the output IF carrier.
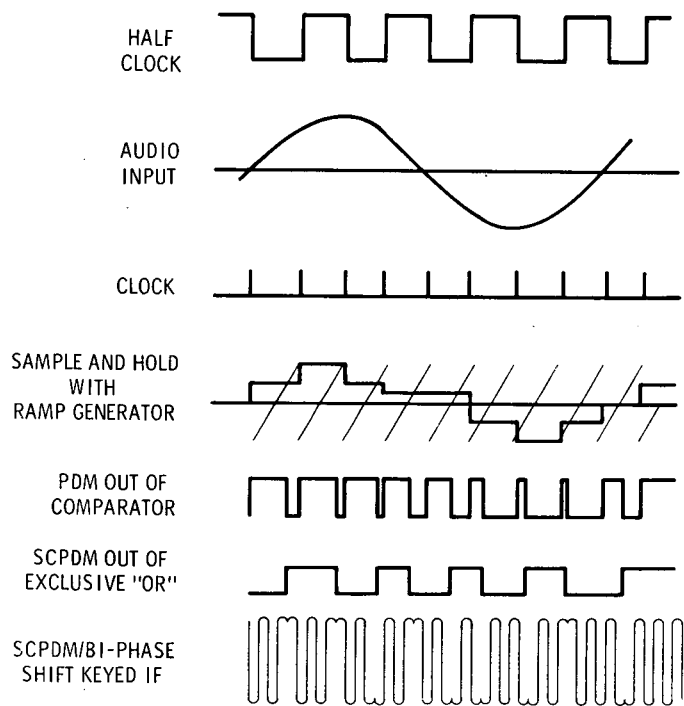
Figure 3-34. PDM Modulator Waveforms

HALF CLOCK

AUDIO INPUT

CLOCK

SAMPLE AND HOLD WITH RAMP GENERATOR

PDM OUT OF COMPARATOR

SCPDM OUT OF EXCLUSIVE "OR"

SCPDM/BI-PHASE SHIFT KEYED IF

670-1197
UNCLASSIFIED

3.2.4.3.5 Convolutional Encoder Board

The convolutional encoder function in the MMT was designed to transform a digital information sequence k into some longer output sequence such that the GSFC decoder can uniquely and with arbitrarily high probability redetermine the k in spite of binary symmetric channel perturbations. The design goal was to achieve a bit error probability of 10^{-5} at an E_b/N_o of 4 dB. The specifications are listed in figure 3-35.

The 24-bit, serial-to-parallel, shift register shown in figure 3-36 consists of three, 8-bit shift registers connected in tandem. The boolean expression for the two modulo-2 summers obtained from the parity generator codes will have the form, $A \oplus B \oplus C \oplus --$. The shaping circuits are J-K flip flops used to clean up any switching spikes in parity bit streams G1 and G2.

ENCODER RATE	1/2
CODE TYPE	NON-SYSTEMATIC
CONSTANT LENGTH	24 BITS
CODE	g_1 = 73353367 g_2 = 53353367
FRAME LENGTH	2047 BITS - ENCODER INPUT 4094 BITS - ENCODER OUT
FRAME SYNCHRONIZATION CODE	ENCODER INPUT 16 BITS 604324 ENCODER OUTPUT 32 BITS 77264244734
FLUSH CODE (ENCODER DUMP)	ENCODER INPUT 24 BITS 11702625
BIT RATES	ENCODER OUTPUT .6, 2, 6, 20 KB/S
QUANTITIZATION	TO BE DONE BY DECODER

NOTE: ALL OCTAL DIGITS SHOWN IN ORDER OF INCREASING TIME;
THE OLDEST DIGIT IS ON THE LEFT.

Figure 3-35. Specifications-Convolutional Encoder

The frame length at the input to the convolutional encoder was chosen equal to that of the telemetry simulator (MX-270), which provides a 2047-bit PN sequence. The frame length is defined as the sum of the flush-code bits, synchronization-code bits, and data bits. The flush code is used by the sequential decoder for reinitialization, and must be equal to the constraint length of the encoder. Therefore, the flush code at the encoder input will be 24 bits, and the synchronization code was selected to be 16 bits. The 24-bit flush code will generate 48 parity bits at the output of the encoder, and will be followed by a 16-bit synchronization which will generate 32 parity bits at the output of the encoder. The input flush and synchronization codes are contained in the PN sequence generator as 40 consecutive bits (24 flush bits + 16 synchronization bits). The frame synchronization code and flush code are shown in the specification chart in figure 3-35 in octal form.

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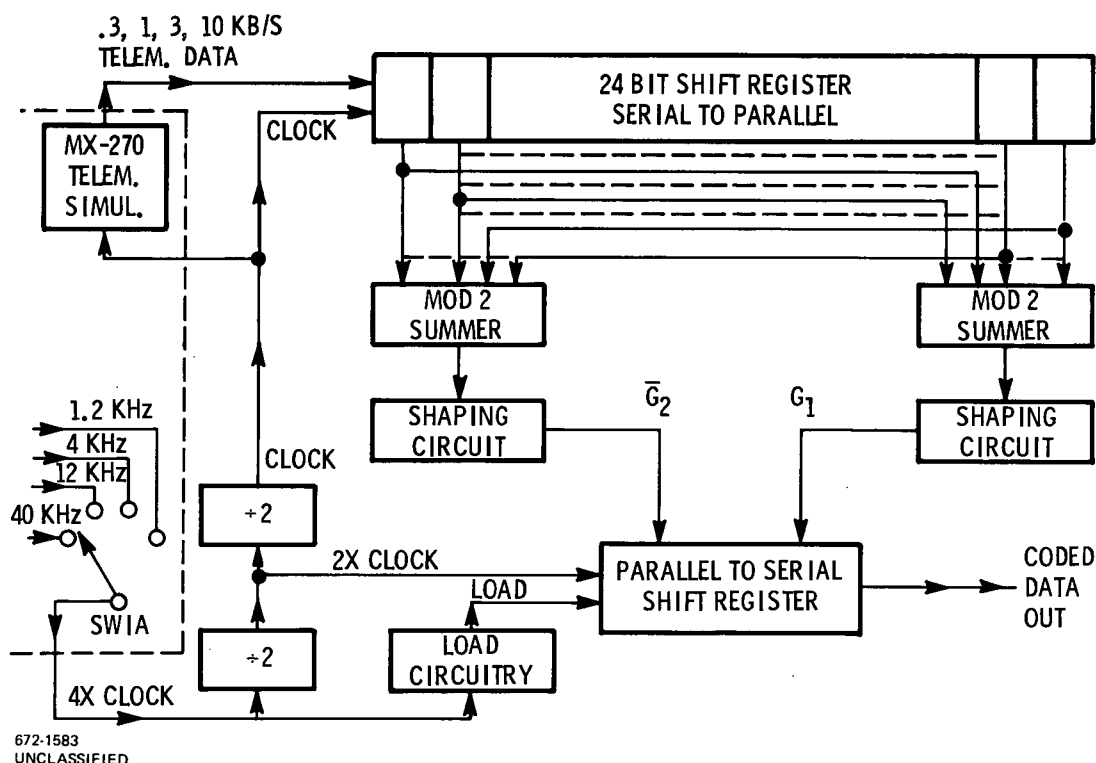
Figure 3-36. Block Diagram Convolutional Encoder Board

3-73

3.2.4.4   Description of ABC Subsystem Equipment

The following is a complete description of the ABC portion of the TDRSS electronics.

The system consists of electronic packages at two locations (MTAR and MMT) each containing an encoder and a decoder as illustrated in figure 3-37. The encoder accepts data or PDM voice, and provides bursted information to the transmitter. At the other location, the received bursted data or bursted PDM input is stored and read out by the decoder at the data rate originally encoded. Thus, the ABC system is transparent. The system is designed to handle data input rates of 100, 300, 600, 1000, 2000, 3000, 10,000 and 20,000 bits per second. The voice mode (PDM at 10 kHz) is also accepted. Data burst intervals of 2, 4, 6, 8, and 10 ms are selected by appropriate coding on the program input lines. Table 3-3 diagrams the amount of storage in bits required for all possible combinations of data rate and burst intervals. Note that the maximum data storage requirements are 1000 bits corresponding to a 20,000 bit per second data rate and a 10 ms burst interval. The voice storage requirement is 3000 bits maximum. Storage requirements are the same in either the encode or decode modes of operation, allowing identical memory organization and control.

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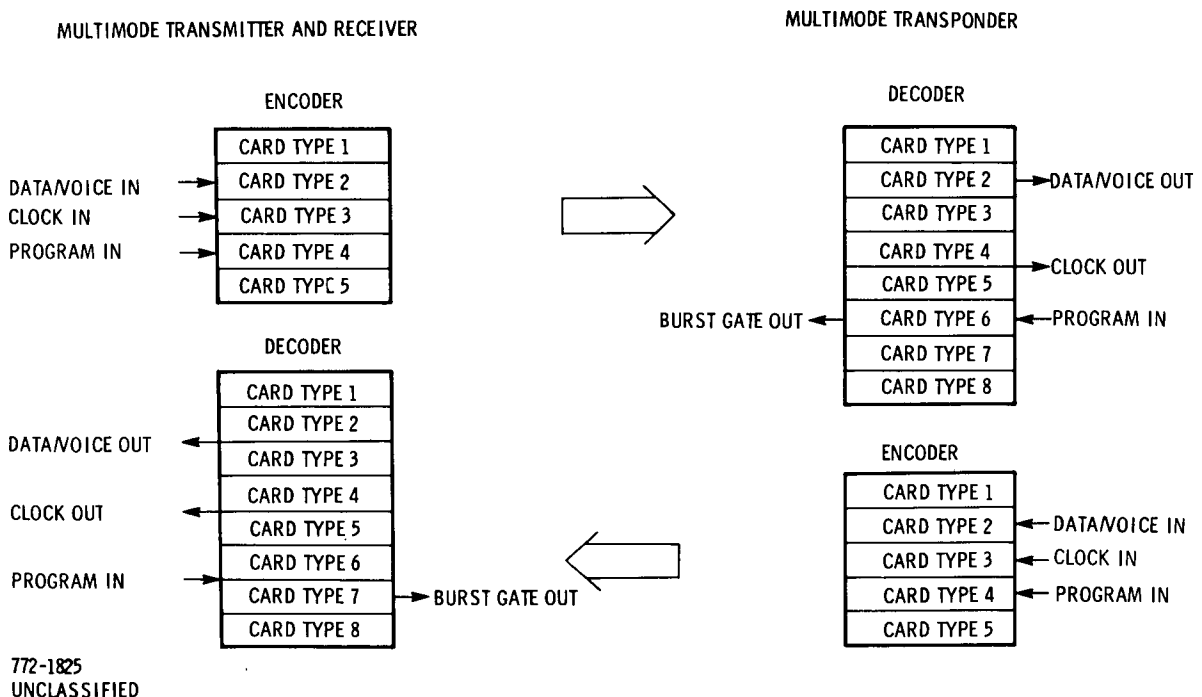
Figure 3-37. ABC Card Configuration

3-74

Table 3-3. Bit Storage Requirement

Data Rate	BURST FORMAT				
	2MS	4MS	6MS	8MS	10 MS
100 BPS	1	2	3	4	5
300 BPs	3	6	9	12	15
600 BPS	6	12	18	24	30
1000 BPS	10	20	30	40	50
2000 BPS	20	40	60	80	100
3000 BPS	30	60	90	120	150
6000 BPS	60	120	180	240	300
10,000 BPS	100	200	300	400	500
20,000 BPS	200	400	600	800	1000
VOICE	6 x 100	6 x 200	6 x 300	6 x 400	6 x 500

3.2.4.4.1 Encoding Circuitry

The encoder consists of printed circuit boards 1, 2, 3, 4, and 5, as illustrated in figure 3-38. It accepts data or PDM modulated voice and programming input commands. The encoder provides burst gate and bursted data. Coding of the program input lines determines the format of the bursted output signal and the data rate which the system accepts. Printed cirfuit boards 1 and 2 are the control boards. Board 3 is the memory; board 4 is the PDM-to-binary converter, and board 5 is the binary-to-PDM converter. Input data is written into the memory at the data clock rate. When required by the burst format in use, memory data is read out interleaved with the memory write command. This allows simultaneous write and read operations to occur during the bursted output. Figure 3-39 illustrates the timing relationships of the data bursting operation for a typical cycle. When the voice mode is selected by the program inputs, the PDM voice is converted into 6-bit binary parallel encoded voice on board 4. The parallel binary voice is then written into the memory at the PDM clock rate and read out interleaved with the write pulses, as with binary data.

DATA RATE/BURST RATE ⟶
PROGRAM INPUTS ⟶

PDM/DATA IN ⟶
CLOCK IN ⟶

PC CARDS
TYPE-01
TYPE-02

CONTROLLER

BURSTED DATA/VOICE OUT
BURST GATE OUT

DATA

MEMORY
CONTROL AND
BINARY DATA

PC CARD
TYPE-03

MEMORY

BURSTED PDM

CLOCK
PDM

PC CARD
TYPE-04

PDM-TO-BINARY
CONVERTER

BINARY 6 BIT VOICE

PC CARD
TYPE-05
BURSTED
BINARY-TO-
BURSTED
PDM CONVERTER

BURSTED BINARY
6 BIT VOICE

PDM CONVERSION CLOCK

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Figure 3-38. Encoder Block Diagram

READ PULSES

WRITE PULSES

CLOCK

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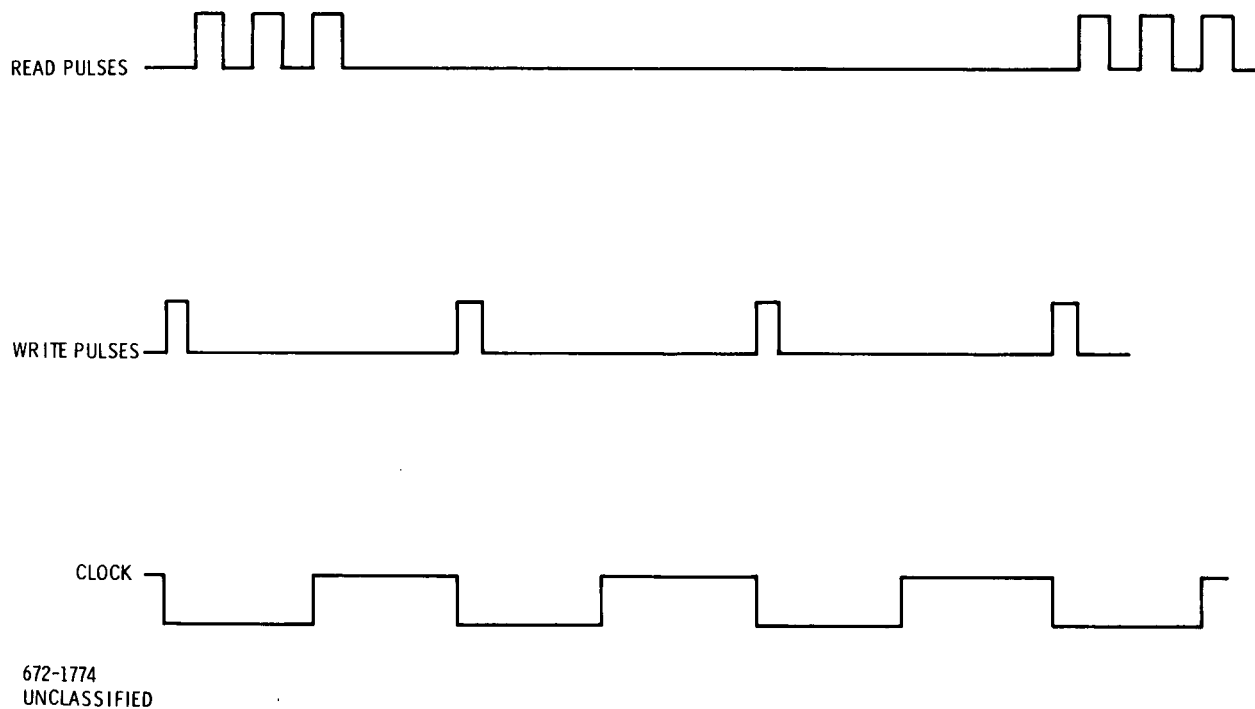
Figure 3-39. Simplified Memory Timing

3-76

The 6-bit parallel output of the memory (now in a bursted format) is converted to bursted PDM on circuit card 5. A detailed description of circuit operation on these cards appears later in this section.

3.2.4.4.2 Decoding Circuitry

The decoder uses the same printed circuit boards that are employed in the encoding electronics. Three additional boards, 6, 7, and 8 are required for data acquisition. Figure 3-40 contains a block diagram of acquisition and decoding electronics. The decoder accepts bipolar bursted data encoded in the manchester format or bursted PDM voice and automatically acquires the burst format in use and regenerates the data and data clock. The regenerated data is then debursted to yield a baseband clock output and data output or a PDM voice output. Board 6 detects the burst format in use. Board 7 regenerates the clock and data. Board 8 regenerates the burst gate for use in the receiver and memory control. The regenerated bursted data from board 7, and regenerated clock are fed to the controller boards 1 and 2. Data is written into the memory board 3 at the burst-clock rate during the burst interval and is read out of the memory at the continuous data rate. Interleaving of the memory read-write commands is accomplished by the controller boards. When the voice mode is selected, regenerated data is fed to board 4 where it is converted to 6-bit binary bursted voice and written into the memory. The 6-bit parallel output of the memory, now at the continuous PDM rate, is fed to board 5 where it is converted to PDM. The decoding system clock rate is programmed by the program input lines. The decoder utilizes burst format program input information to select the desired burst format. If the program input coding information is not present, board 6 will automatically select the correct burst format. A detailed description of printed circuit board, operation follows.

a.   Operation of Board Type 1

This board, contains the read-write address counters for the memory and switching logic to select the appropriate address information. Encoded format commands on the programming input lines are processed to set the modulus of each counter. Clock pulses toggle the appropriate counter consisting of IC 6 through IC 8 or IC 10 through IC 12. The count modulus is set by loading the counters at the

RAW BURSTED MANCHESTER DATA/PDM VOICE

1 OF 5 RATE SELECT — PCB 06

1 OF 5

PROGRAM INPUTS

DATA/CLOCK RECOVERY — PCB 07

1 + D DATA

DATA

CLOCK

CONTROLLER — PCB 01

PCB 02

MEMORY — PCB 03

BINARY 6 BIT VOICE

CLOCK OUTPUT

DATA/VOICE OUTPUT

MEMORY CONTROL AND BINARY DATA

PDM

BURST GATE OUT

PCB 08

BURST GATE REGENERATOR

PCB 04

BINARY 6 BIT BURSTED VOICE

BURSTED PCM TO BURSTED BINARY CONVERTER

PCB 05

BINARY TO PDM CONVERTER

772-1808
UNCLASSIFIED

Figure 3-40. Decoder Block Diagram

negative transition of the most-significant bit of the counter-string output. Preset inputs to the counters are derived from the read-only memory (ROM), IC1 and IC2. IC6 through IC8, having been preset from the prior cycle, are incremented by the clock pulses from IC6 to the fully loaded state of the counters. The next clock pulse increments the counters to a zero state resulting in a transition of the most-significant bit of counter IC8, setting one-shot IC9. Then IC9 feeds a fixed width roll-over pulse to the load inputs of IC6 through IC8. The count sequence is identical for IC10 through IC13.

Integrated circuits IC3 through IC5 are the memory address switches. They select, on command, whether the memory will be addressed by counters IC6 through IC8, or IC10 through IC12. Integrated Circuits IC3 through IC5 are type 74157 data switches. Integrated circuits IC1 and IC2 are fusible link type ROMs. These ROMs are custom programmed at the factory to yield the desired code pattern. Counter increment information enters the board on pins 2A and 11A; address switch information enters on pin 10A. Test points are provided for monitoring all functions.

b.   Operation of Board Type 2

        Printed circuit board type 2, generates the timing relationships for
memory operation. The clock enters the board on pin 2A. Each clock pulse sets IC2
to produce a pulse on pin 3B. The pulse on pin 3B sets IC4 to produce a strobe after a
delay introduced by one section of IC3. Roll-over pulses from controller card 01 enter
on pins 3A and 4A. These pulses set and reset IC1 to produce the burst gate. The
output of IC1 gates the five-times, clock-oscillator output produced by IC9. The gated
five-times clock output appears on pin 5B. This same output, delayed by a section of
IC3 sets a one-shot to produce a strobe. Integrated circuits IC8, IC9, and IC10 com-
prise a phase-lock loop to generate the five-times clock frequency. The center frequency
of this loop is set by the data-rate program inputs through IC10, which switches the
appropriate timing capacitor into the VCO. Integrated circuit IC6 is a 4-pole digital
switch. The state of this switch is determined by the data-rate program inputs. When
voice is selected, IC7 detects this and toggles IC6 to the voice mode. Integrated circuit
IC6 arranges the memory processing to enable voice operations.

        c.   Operation of Board Type 3

        This board performs all memory functions for encoding or decoding.
The 6-bit memory input data enters the card on pins 2A through 7A through 7A. Address
information for the memory enters the card on 8A through 17A. The memory consists
of 256-bit-by-1-bit, random-access, bipolar-memory chips, IC1 through IC14. The
memory chips are wired in parallel and the chip select function is performed by a
2-line-by-4-line decoder chip, IC15. In the voice mode, unused power to memory Ics
is switched off. Memory outputs are strobed into IC16, a 6-bit latch register, and
the output of this register is the retrieved data appearing on pins 2B through 7B. Read-
write command information enters the card on pin 19A and output latch strobe information
enters on pin 18A.

        d.   Operation of Board Type 4

        Printed circuit board type 04, is the PDM-to-binary converter. It
converts PDM voice to 6-bit binary parallel voice. The card includes facilities for
analog monitoring of the voice signal being processed. System clock pulses entering
on pin 3A are fed to a phase-locked loop consisting of Ic8, IC1, 9, 10, and 11.

This loop generates the timing pulses used on both card 04 and card 05. Integrated circuit IC11 functions as a divide-by-five ripple counter. Integrated circuits IC9 and IC10 function as a divide-by-32 ripple counter to provide the reference input to IC8. The clock pulses (appearing on pin 11 of IC11) are gated by the incoming PDM signal entering the card on pin 2A. The gated clock is applied to a 6-bit binary ripple counter consisting of IC4 and IC5. The binary count accumulated during the PDM interval is strobed into an output register consisting of IC6 and IC7 on the trailing edge of the input PDM. Integrated circuits IC6 and IC7 are 4-bit latches. The six outputs of this register appear on pins 2B through 7B. Additionally, an R/2R ladder network, IC12, provides an analog indication of the binary state of the outputs, thus yielding a voice monitoring capability. Integrated circuits IC2 and IC3 function as a ripple timing register to provide strobe pulses for the output register and reset pulses for counters IC4 and IC5. The trailing edge of the input PDM signal triggers IC2 to provide the output strobe pulse. At the conclusion of the output strobe pulse, IC3 provides a brief reset pulse to the two counters and the system is ready for the next PDM interval.

e. Operation of Board Type 5

This board converts 6-bit binary parallel coded information to PDM encoded information. Clock pulses on pin 9A toggle a counter consisting of IC4 and IC5. When the counter binary information equals the binary information fed to the magnitude comparator on pins 2A through 7A, the output of IC2 resets latch IC3 and initiates the sequence again. The output on pin 2B is dependent on the binary weighting of the 6 input lines. Integrated circuits IC1 and IC2 are magnitude comparators. Integrated circuit provides a cascaded output to IC2's inputs. Integrated circuit IC4 is a type-7493, binary-ripple counter. Integrated circuit IC5 is a dual-JK flip-flop functioning as a ripple counter. Both counters are normally held in the clear position by IC3. Count initialization occurs only when a pulse is present on pin 8A. This pulse determines the position of the leading edge of the PDM output signal. Integrated circuit IC3 is an RS flip-flop serving as an output buffer.

f. Operation of Board Type 6

Printed circuit board 6 selects the burst format in use from the raw-data input. Data enters the board on pin 2A. Integrated circuit IC3 and IC6 comprise a full-wave rectifier. The output of this circuit corresponds to the fundamental frequency

of the burst period in use. Integrated circuit IC7A buffers this information. The buffer feeds five active filters. Each active filter is tuned to a fundamental frequency of a burst format, i.e. 100, 50, 33, 25, and 20 Hz (2, 4, 6, 8, 10, ms). Following each active filter is a clamp circuit which feeds one input of a diode OR gate, charging a capacitor to a value corresponding to the voltage of the greatest filter output. This DC voltage divided by R1 and R2 serves as a reference voltage for the output comparators. The output of each clamp circuit is compared to this DC voltage. Output logic consisting of integrated circuits IC11, IC12, IC13, and IC14 allows only the higher frequency of two simultaneous outputs to go true if more than one comparator output is true. This priority chain operates except when external program inputs are fed to the decode chip IC9. When decoder chip IC9 provides an output other than position 0, it opens the gate for the comparator output corresponding to that position. The output of board 6 is a logic true output on one of the card's five output lines corresponding to the burst format in use.

     g.   Operation of Board Type 7

          Printed circuit board 7 retrieves the data and clock from bipolar manchester-encoded input data. Bipolar data enters the board on pin 3A. A programmable low-pass filter consisting of IC4 and capacitors C4 through C11, removes high-frequency noise from the data. Integrated circuits IC1, IC2, and IC3 form a digital differentiator which provides a pulse on each transition of the input signal. This pulse drives the gate of the sampling FET. A VCO located on board 8 provides a clock frequency reference output on 8A. Integrated circuits IC11 and IC8A comprise a ramp generator. This ramp is sampled by the differentiator output and fed to integrator IC8. The integrator output (loop error voltage) is fed to board 8 and used to control the center frequency of the VCO. Data entering on pin 3A is also fed to an integrate-and-dump circuit. Integrated circuit IC5 selects the time constant, while IC7 provides the sample and dump pulses. Integrated circuit IC6 functions as a high-speed slicer to recover the data. Integrated circuits IC9, IC10 and IC12 decode the manchester data and provide a clock output at the data rate. The VCO center frequency, the time constant of the low-pass filter, and the time constant of the low-lass filter, and the time constant of the integrate and dump circuit are all controlled by the data-rate program lines.

h. Operation of Board Type 8

Printed circuit board 8 regenerates the burst gate. Full-wave detected data from board 6 enters on pin 2A. A phase-locked loop, consisting of oscillator IC2, oscillator center frequency selector IC3, phase detector IC1, and scaler counter IC4 and IC5 provides a reconstituted burst-gate output. The center frequency of oscillator IC2 is determined by the 1-of-5 selection made on board 6. Also located on board 8 is the data-clock VCO and programmable divider, consisting of IC6 through IC11. The modulus of the divide chain is programmed by read-only-memory chip IC7 which is controlled by the program input lines.

3.2.4.4.3 Power, Size, and Weight Requirements

The design of the ABC encoder and decoder was subject to several constraints. Since the system was designed to verify feasibility of the ABC technique in an airplane test situation, only secondary consideration was given to power, size, and weight. The power requirements of the ABC encoder and decoder are largely consumed in the memory portions of the equipment. A reduction in memory power would reduce the total system power drastically since memory utilization in the voice mode is three times that of the maximum memory required for the data mode. The present design incorporates memory power switching to reduce the memory power in the data mode by removing unused memory elements from the circuit. The TTL logic and dual-in-line (DIP) packages were selected onthe basis of cost. A considerable reduction in size could be obtained through the use of flat packages.

Power consumption for the above design will be about 25 watts in the voice mode and 17 watts in the data modes. The system uses 14 MRL universal printed circuit boards and, for a board spacing of 1/2 inch, will occupy about 156 cubic inches.

The weight will be 2.7 pounds not including mating-card edge connectors which are part of the MRL card cage.

A secondary design for the ABC encoder and decoder has been formulated based on presently available MOS integrated circuits. This design gives foremost consideration to minimization of power requirements. Through the use of CMOS,

this design achieves identical circuit performance with less than 1/10 of the power required by TTL devices. A reduction in memory power is achieved through the use of MOS memories as opposed to bipolar TTL memories. It is anticipated that the size and weight of the entire system will not change appreciably. As in the present implementation, the system is configured on 14 MRL universal printed circuit boards. The power dissipations of the CMOS design is approximately 2.7 watts.

3.2.5   CONTROL BOX

A remote control box is provided for the MMT. Front panel switches and indicators are provided to facilitate mode selection for the experiments to be performed.

The following selector switches are provided on the MMT control Box.

- Link Mode - Forward only
            Transpond
            Return only

- Modulation Mode - PSK
            PN
            ABC

- ABC Format   - 2 (MS)
            4 (MS)
            6 (MS)
            8 (MS)
            10 (MS)
            Auto

Forward Link

- PN Chip Rate   - 34.133 K Chip/s
            102.4   K Chip/s

- Data Rate   - 100 Bit/s
            300 Bit/s
            1000 Bit/s
            Voice

Return Link

- PN Chip Rate -   34.133K Chip/s

    102.4K Chip/s

    1024K Chip/s

- Data Rate -   0.3K Bit/s

    1.0K Bit/s

    3.0K Bit/s

    10.0K Bit/s

    Voice

- Forward Error Encode - On

    Off

A margin to threshold meter scaled in dB is provided for each of the two diverity receivers.

The control panel interface board contains a pull-up resistor for each control wire from the mode selection switches listed above. This board also contains the lamp drivers for the indicator lamps.

3.2.6   POWER SUPPLY

The MMT power supply chassis contains four regulated power supply modules to supply DC voltages of +28V, +15V, -15V and +5V to the RF/IF chassis and the signal processor chassis.

The power supply module specifications allow prime input power to be 105-125 VAC, 50-400 Hz. These power supply modules feature short circuit and overvoltage protection. Full specifications are contained in drawing number X625196.

The estimated DC power requirements for the MMT are listed below.

+28V	100 watts
+15V	30 watts
-15V	30 watts
+5V	45 watts

3.3 MTAR (GROUND UNIT)

3.3.1 INTRODUCTION

This section describes the Multimode Transmitter and Receiver (MTAR). The MTAR consists of an antenna, RF/IF chassis, signal processor chassis, control box and power supply chassis.

3.3.2 ANTENNA

The same antenna is recommended for both the MMT, and MTAR. The description of the antenna design will be found in paragraph 3.2.1 of this report.

3.3.3 MTAR RF/IF CHASSIS

The MTAR is to perform the same function conceptually as the MMT. The unit is capable of transmitting to and receiving signals from the multimode transponder (MMT) in a number of test configurations in which the MTAR is always ground based. A block diagram of the MTAR RF/IF is shown in figure 3-41. The unit is a combined transmitter and two receivers. The transmitter will transmit one of two VHF frequencies or one UHF frequency. The power amplifier (A1) is capable of two modes of operation, and will supply each antenna with 2.5 watts of RF power. The amplifier will be supplied with one of three drive signals at a power of 0 dBm. The amplification factor is 33 dB and the bandwidth is 100 MHz to 500 MHz. The output level may be reduced 30 dB in 1 dB steps by adjusting the RF power attenuator (R1). The output of the attenuator will be manually connected to one of three transmitter bandpass filters (F1, F2, F3). A power divider is connected between each bandpass filter and the corresponding frequency inputs of the two quadriplexers. The quadriplexers permit the common use of the antennas for transmitting and reception.

The antennas will receive a 137 MHz signal which will supply drive to each quadriplexer. The quadriplexer routes the 137 MHz frequency to the 137 MHz preselector bandpass filters. Preselector bandpass filter (F4) provides band selection for receiver No. 1, and preselector bandpass filter (F5) provides band selection for receiver No. 2. The output of the preselectors are followed by two rotary attenuators (R2, R3), each attenuator will provide 0 to 30 dB of attenuation to each receiver. The receivers are low-noise, wideband receivers with high gain. The MTAR as a one-of-a-kind unique test equipments is procured from off-the-shelf components wherever possible. The design features of the individual blocks in figure 3-40 are briefly discussed in the following paragraphs.

BANDPASS FILTER
f_c = 127.750 MHz

BANDPASS FILTER
f_c - 149 MHz

BANDPASS FILTER
f_c = 401 MHz

R.F. POWER
AMPLIFIER

0 dBm
R.F.
INPUT

A1

R1

TRANSMITTER
ATTENUATOR

F1

F2

F3

÷2

÷2

÷2

POWER
DIVIDER
D1

POWER
DIVIDER
D2

POWER
DIVIDER
D3

90°
PHASE
SHIFT

90°
PHASE
SHIFT

90°
PHASE
SHIFT

QUADRAPLEXER
NO. 1

P1

QUADRAPLEXER
NO. 2

P2

ANTENNA
NO. 1

ANTENNA
NO. 2

PRE-SELECTOR
BANDPASS
FILTER

RECEIVER NO. 1
ATTENUATOR

F4

R2

RECEIVER NO. 1

CH-1

PRE-SELECTOR
BANDPASS
FILTER

RECEIVER NO. 2
ATTENUATOR

F5

R3

RECEIVER NO. 2

CH-2

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Figure 3-41. MTAR RF/IF

3.3.3.1   RF Power Amplifier (A1)

The RF power amplifier is a commercial solid state wideband amplifier. The unit is a unique combination of lumped elements, microstripline and ferrite hybrid techniques. The combination of these techniques and utilizing the latest silicon transistors offer a power frequency capability that permits a bandwidth of 100 MHz to 500 MHz. The design also insures stable performance and high reliability over the temperature range. The input drive will be supplied at a power level of 0 dBm and one of three frequencies (1) 127.750 MHz, (2) 149 MHz and (3) 401 MHz. The amplifier is operated class A and has 33 dB of gain. All intermodulation products and spurious responses are down at least 30 dB. The unit is capable of two distinct modes of operation: 1) Mode A: the input drive will consist of a 2 ms burst of carrier frequency at a 20 percent on and 80 percent off duty cycle; 2) Mode B: the input drive will be a constant envelope carrier. The power amplifier will deliver 2 watts into a 50 ohm load. The output stage is protected and will not be damaged as result of the output port being indefinitely opened or short circuited. As an added safety feature, B+ reversal protection circuitry is included to prevent damage to the amplifier. The DC

power requirements for the unit is +28 VDC and power efficiency is greater than 30 percent in either mode A or B. Design and construction of this amplifier meets the specification callout in drawing No. X625194.

3.3.3.2   Transmitter Attenuator (R1)

The RF power amplifier is followed by a rotary attenuator (R1) which provides 0 to 30 dB of attenuation in 1 dB steps. This 50 phm panel mount rotary attenuator occupies little more space than a potentiometer. The bandwidth is specified to be DC to 500 MHz. The maximum power dissipation is 2 watts and the peak power handling capability is 250 watts. Typical VSWR will be 1.2:1 and maximum insertion loss is 0.2 dB. The unit's rugged construction meets the environmental requirement of the MTAR unit. The attenuator will be used to reduce the RF power by 30 dB in one dB steps. The output will be manually connected to one of three transmitter bandpass filters.

3.3.3.3   Transmitter Bandpass Filters (F1, F2, F3)

The input of one of the three bandpass filters will be connected manually to the output of attenuator R1. Transmitter bandpass filter (F1) will limit the input frequency to a center frequency of 127.750 MHz and a 3-dB bandwidth of 4 MHz. Transmitter bandpass filter (F2) will limit the input frequency to a center frequency of 149 MHz and a 3 dB bandwidth of 4.5 MHz, bandpass filter (F3) will limit the input frequency to a center frequency of 401 MHz and 3-dB bandwidth of 4 MHz. All three filters have a 15 MHz 40 dB bandwidth, that is used in conjunction with the quadraplexers. The bandpass filters and the quadraplexers develop a 120 dB of isolation between the transmitter's bands and receiver's band. The cavity type filters have unique characteristics, which are required to obtain low insertion loss, and still meet the high power requirements, the cavity filter offers suitable size and form factor. The transmitter bandpass filter serves to assure that all spurious radiation is down 40 dB below the fundamental. The basic design techniques for the bandpass filter are well established so that filter manufacturers claim 2 to 4 weeks availability.

3.3.3.4   Power Dividers (D1, D2, D3)

The outputs of the transmitter bandpass filters (F1, F2, F3) are followed by three power dividers (D1, D2, D3). The power dividers permit the use of one power amplifier to supply RF power to both antennas. The devices have a bandwidth of 100 MHz to 500 MHz and are capable of handling 3 watts of RF power. The output

signals are in phase with each other and division difference is in the order of 0.2 dB. The power divider's outputs are connected to the inputs of quadriplexers P1 and P2.

3.3.3.5   Quadriplexers (P1 & P2)

The outputs of power dividers D1 are routed into the 127.750 MHz ports of quadriplexers (P1) and (P2). D2's outputs are connected to the 149 MHz ports of the quadriplexers (P1) and (P2). Divider D2's outputs are connected to the 149 MHz ports of the quadriplexers, and D3's outputs are connected to the 401 MHz ports. The quadri-units were designed to operate in conjunction with four frequencies, three of the frequencies are VHF and one is UHF. Each device will drive an antenna with one of three frequency, two VHF frequency (127.750 MHz and 149 MHz) and one UHF frequency of 401 MHz. The antennas will receive and drive the quadriplexers with one VHF frequency of 137 MHz. The 137 MHz frequency will be routed to the receiver preselector bandpass filter (F4 and F5). The quadriplexers are an advancement in the technique of filter design which enables the different frequencies to be separated and routed to the individual frequency ports. Each quadriplexer will have a total of five ports which are (1) 137 MHz, (2) 127.750 MHz, (3) 149 MHz, (4) 401 MHz and (5) the antenna port. The antenna port is capable of receiving or transmitting any of the four frequencies.

The primary functions of the quadriplexers are to separate and isolate each frequency. The quadriplexers must have adequate isolation since transmitter and receivers will both be on at the same time. In order to maintain separation from the transmitter frequency and the receiver frequency, a 120 dB of isolation is required between the transmitter's bands and receiver band.

The option design for the required quadriplexers only permits 80 dB of isolation between bands. The parameters that were consistent in designing the quadriplexers were as follows: (1) The insertion loss of the quadriplexers to be held to a maximum of 2.8 dB. (2) The 3 dB bandwidth a minimum of 2 MHz, (3) the 80 dB bandwidth a maximum of 15 MHz. (4) The quadriplexers must be capable of 20 watts average power. Since only 80 dB is obtainable in quadriplexers, the other 40 dB will be obtained from bandpass filters. The quadriplexers in conjunction with the bandpass filters will supply the required 120 dB isolation between transmitter band and the receiver bands.

3.3.3.6   Preselector Bandpass Filters (F4, F5)

The quadriplexers are followed by two preselector bandpass filters, F4, F5. The filters are used in conjunction with the quadriplexers, P1, P2, to obtain a 120 dB of isolation between the transmitter's bnads and the receiver's band. The two filters are connected to the 137 MHz ports of P1 and P2 and serve as a preselector for the two receivers. The units are tuned to have the following characteristics: Center frequency is 137 MHz and a 3-dB bandwidth of 4 MHz. The filters have a 15-MHz, 80-dB bandwidth and are used with the quadraplexers to give a total 15-MHz, 120-dB bandwidth. The 15-MHz, 120-dB bandwidth providing the necessary isolation between transmitter and receiver. The bandpass filters are cavity type to provide the lowest insertion loss and still maintain a reasonable size. The output of each preselector drives the input of attenuators R2 and R3.

3.3.3.7   Receivers Attenuators (R2, R3)

The input of R2 and R3 is connected to the output of preselectors F4 and F5. Attenuators R2 and R3 are used to provide 0 to 30 dB of attenuation in 1 dB steps. The 50-ohm, panel-mount, rotary attenuator will be used to attenuate the received RF power by 30 dB. The devices are specified to have a bandwidth of DC to 500 MHz. The maximum power dissipation is 2 watts and the peak power handling capability is 250 watts. Typical VSWR will be 1.2:1 and a maximum insertion loss of 0.2 dB. The output of attenuators R2 drive the input of receiver No. 1, and R3 drive receiver No. 2.

3.3.3.8   Preamplifier

The preamplifier consists of three RF amplifiers A1, A2, A3, and a band-pass filter (F1). The RF amplifiers (mic-amps) A1, A2, A3 were selected for their low-noise figure of 2.5 dB. The mic-amps are unique in that a complete transistor amplifier is contained in a TO-8 transistor package. The tiny modular amplifiers are made with highly-reliable sapphire substrates, microwave transistors chips, thin-film resistors and chip capacitors. The units have a bandwidth of 5 MHz to 500 MHz and can be cascaded without bandwidth shrinkage. The bandwidth is maintained with a flatness of ± 1.0 dB over the frequency range. The inputs and outputs are 50 ohm, with a maximum VSWR of 2.0.

The noise figure of the preamplifier is 3 dB, due to cascading two mic-amps A1 and A2, the total gain of A1 and A2 is 29 dB and the compression factor of A2 is -2 dB.

3.3.3.9   Bandpass Filter

The output of mic-amp A2 is filtered by a bandpass filter (F1). The band-pass filter is tuned to have a center frequency of 137 MHz, and a 3-dB bandwidth of 20 MHz. The bandpass filter provides rejection and supresses out-of-band noise and interference, to achieve an image suppression and to prevent radiation of the local oscillator signal. The filter maintains a low-system-noise figure of 3 dB, and will have a 2-dB insertion loss. The output of F1 is tied to the input of A3 a mic-amp with a gain of 14 dB and a compression of +7 dB. Mil-amp A3 is a buffer between the bandpass filter and the mixer.

3.3.3.10   The First Down Converter

The first down converter is a commercial balanced mixer. The device has a conversion loss of 7.0 dB maximum, and a maximum noise factor of 7.5 dB. The mixer's bandwidth is specified to be 5 MHz to 500 MHz, indicating that good amplitude and phase linearity can be obtained. The isolation between the RF signal and local oscillator is a minimum of 30 dB. The local oscillator frequency will be 80 MHz at a power level of +4 dBm. The 137 MHz RF signal will be supplied to the mixer by mic-amp A3. The output of the mixer will result in the first IF frequency of 57 MHz. The mixer is specified in drawing X625189, and manufacturers claim off-the-shelf availability.

3.3.3.11   The First IF

The first IF is made up by using two mic-amps (A4, A5) and a bandpass filter F2. Mic-amp A4 has a gain of 13 dB and is used to maintain a buffer between mixer (M1) and F2 (bandpass filter). The bandpass filter used in the first IF has a center frequency of 57.000 MHz and a bandpass of 10 MHz. The insertion loss will be a maximum of 2 dB. The filter is followed by a mic-amp A5 with a gain of 13 dB. mic-amp A5 is used to drive the second down converter M2.

3.3.3.12   The Second Down Converter (M2)

The second down converter (M2) is a balanced mixer, the same balanced mixer that is used for M1 is also used for M2. The mixer (M2) is supplied with a local oscillator at a frequency of 45 MHz and power level of +4 dBm. The input frequency to M2 is the 57 MHz that was developed in the first IF. The resulting output frequency will be 12.0 MHz, the second IF frequency. The power gains at this point in the receiver will be -92.5 dB and a noise power of -50.5 dB.

3.3.3.13 The Second IF Stage

The second IF stage has an insertion loss of 2 dB and gain of 26 dB. The bandpass filter F3 is tuned for a center frequency of 12.0 MHz and has a 3-dB bandwidth of 2 MHz. Mic-amp A6 is used to provide a buffer between mixer M2 and bandpass filter F3. Mic-amp A7 drives the first AGC stage A8, with a signal power of -69.5 dB and a noise power of -27.5 dB.

3.3.4 SIGNAL PROCESSOR CHASSIS

3.3.4.1 Introduction

The MTAR signal processor chassis contains the receiver circuitry from the 12.0 MHz IF down to baseband processing and the transmitter modulation circuitry. The MTAR signal processor chassis is made up of plug-in printed circuit boards. The following is a list of board nomenclature and the quantities used in the MTAR:

Local Reference/Correlator Board	- 2
Baseband Conditioner Board	- 2
Carrier Loop Filter & VCO Board	- 2
Sync/AGC Board	- 1
Doppler Processor Boards 1 & 2	- 1
Clock Loop Filter & VCO Board	- 1
MTAR Controller Board	- 1
Code & Data Clock Synthesizer Board	- 2
Frequency Synthesizer Board 1 & 2	- 1
Frequency Synthesizer Board 3	- 2
Receive Coder Board	- 1
Diversity Combiner Board	- 1
Data Recovery Board	- 1
Transmit Coder Board	- 1
MTAR Modulator Board	- 1
Data Processor - Receive Board	- 1
PDM Voice - Receiver Board	- 1
Data Processor - XMIT Board	- 1
PDM Voice - XMIT Board	- 1
Control Panel Interface Board	- 1
GRARR XMIT Processor Board	- 1
ABC Boards 1 thru 8	- 13

3.3.4.2   Diversity Receivers

A functional description of each type of diversity receiver printed circuit board not already described in the MMT section follows.

3.3.4.2.1 Controller Board

The MTAR controller board: 1) searches the receiver coder to obtain correlation; 2) interrupts the data stream to send a 31-bit Legendre sequence indicating to the MMT that the MTAR receiver is in sync; and 3) detects the 7-bit Barker sequence transmitted by the MMT and switches to selected data and chip rates from the forced value.

A 31-bit sequence is used to tell the MMT that the MTAR receiver is in sync because the probability that the random data being transmitted by the MTAR before its receiver is in sync will duplicate the sequence is only one 3×10^4. A 7-bit Barker sequence is sent back from the MMT to initiate the switch to final data and chip rates because no data will be transmitted by the MMT until after this switch has taken place and therefore a long sequence is not required. The 7-bit sequence serves only to eliminate possible false switches due to impulse-type noise interference. The search strategy used and the sequence of information transfer between the MMT and MTAR were discussed in the section on system operation.

3.3.4.2.2 MTAR Frequency Synthesizer Board

The MTAR frequency synthesizer consists of three boards. Boards 1 and 2 are used to generate the fixed frequencies for the transmitter portion of the MTAR. Two each boards 3 are used to generate corrected frequencies for the two receivers of the MTAR. The outputs of the MTAR boards 1, 2 and 3 are specified in table 3-4.

Referring to the block diagram (figure 3-42) of the MTAR, the synthesis of each MTAR output of MTAR board 1 is discussed.

     a.   5-MHz Reference Output

The output of the 5-MHz reference oscillator is buffered (EF) on the MTAR board 1 and is presented as a 5-MHz output.

     b.   60 MHz (TX-LO) Output

The 60-MHz outputs are basically generated in two steps: first, the 5 MHz is multiplied times 4 to 20 MHz; second the 20 MHz is multiplied times 3 to 60 MHz. The multiplication of the 5 MHz to 20 MHz is done by shaping the 5 MHz into

Table 3-4. Specification of MTAR Frequency Synthesizer Outputs

	FREQUENCY IN MHz	POWER LEVEL IN dBm	MIN. ISOLATION From SPURS in dB	USE
MTAR #1	5.0	0 ±1 dB	>30	Reference
	60.0	+4.0 ±1 dB	>40	TX-LO
	60.0	0 ±1 dB	>30	Range Reference
MTAR #2	67.75	+7 ±1 dB	>40	TX-IF
	81.25	+4 ±1 dB	>40	TX-LO
	333.25	+5 ±1 dB	>40	TX-LO
MTAR #3	5.0	TTl Squarewave	N/A	Reference
	10.75	+10 ±1 dB	>40	INJ-3
	80.0	0 ±1 dB	>30	Reference
	80.0	+4 ±1 dB	>50	INJ-1
	45.0	+7 ±1 dB	>50	INJ-2

a TTL rectangular pulse (PG-1) of proper duration. The spectrum of a rectangular pulse train is composed of the superimposition of a fundamental cosine wave and its harmonics. The amplitude and phases of the harmonics follow a function of the form:

$$Y = (\sin X) / X$$

$$\text{where } X = \sin (wt / 2) \text{ and}$$

$$T = \text{pulse width}$$

Through imperical analysis using TTL logic as a rectangular pulse generator, it has been found that the pulse width (TP) should be about one half the period of the desired frequency - in this case:

$$TP = \frac{1}{2\,fd} \qquad (1)$$

$$\text{where } fd = 20 \text{ MHz } (4 \times 5 \text{ MHz}) \qquad (2)$$

$$\text{then } TP = \frac{1}{2\,(2 \times 10^7)} \qquad (3)$$

$$TP = 25 \text{ nsec} \qquad (4)$$

This places the desired harmonic (20 MHz) in the middle of the first lobe of the sin X/X envelope approximately 3 dB below the fundamental (5 MHz) at the output of PG-1. Now that the desired frequency (20 MHz) has been generated what remains to be done is to filter the 20 MHz from the adjacent harmonics and amplify. This last procedure is implemented with a double-tuned amplifier (BPA-20). The next step, is to multiply
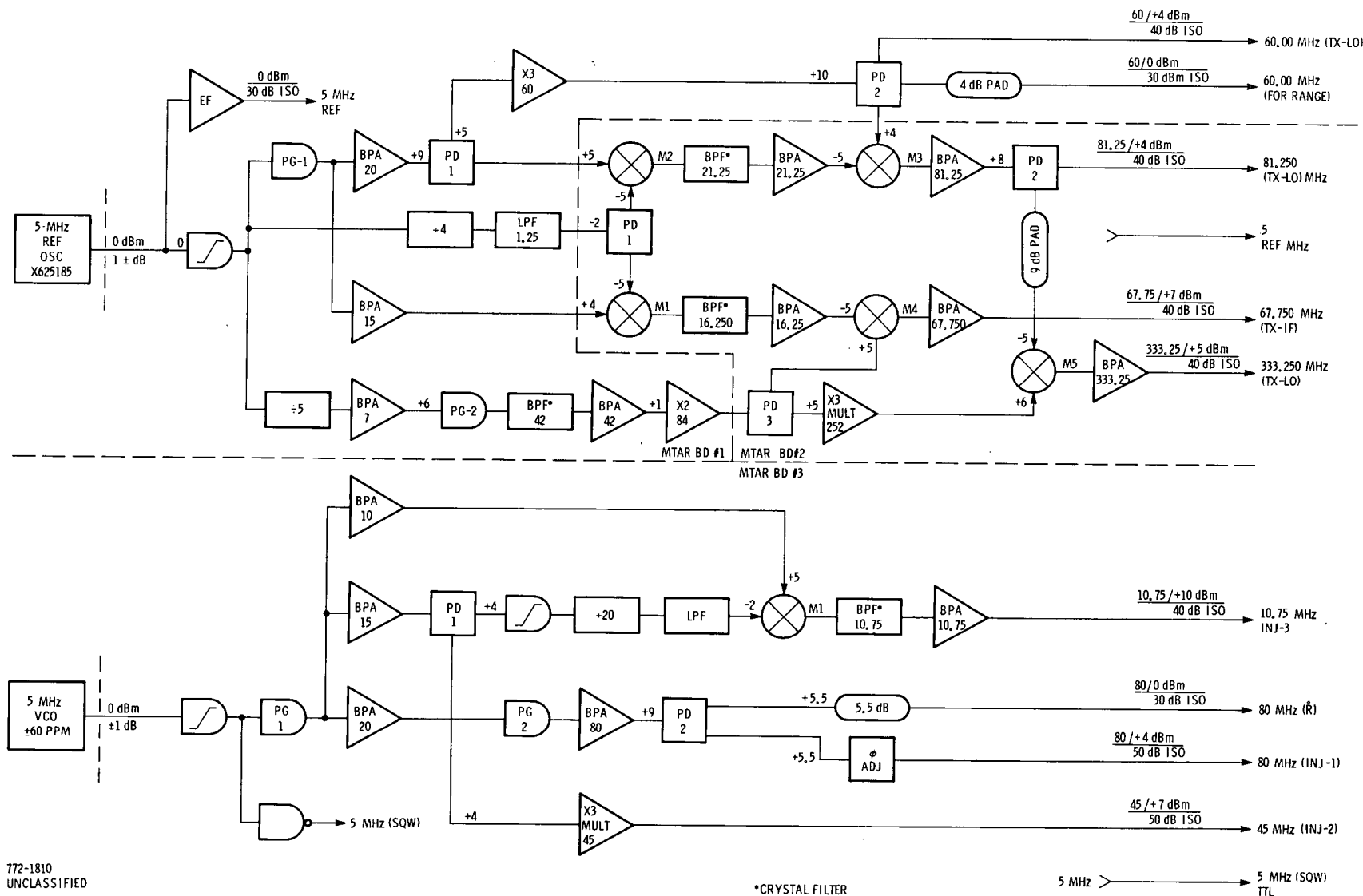
Figure 3-42. MTAR Frequency Synthesizer – Block Diagram

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the 20 MHz to the desired 60 MHz output frequency. This multiplication is accomplished by driving a class "C" amplifier (X3 - 60) with 20 MHz and tuning the output to the third harmonic or 60 MHz.

      c.   20-MHz Intersynthesizer Signal

      In the process of developing the 60-MHz outputs a 20-MHz signal is developed. This 20 MHz is first power divided where one output is used to develop the 60-MHz outputs and the other output of the divider becomes the 20-MHz intersynthesizer signal.

      d.   15 MHz Intersynthesizer Signal

      The desired 15-MHz signal is present in the sin X/X envelope discussed in paragraph 1.2.2; therefore, the double tuned amplifier (BPA-15) is implemented to filter and amplify the desired 15 MHz.

      e.   1.25-MHz Intersynthesizer Signal

      The 5-MHz reference is first counted down by a factor of four using TTL logic; this produces a 1.25-MHz squarewave which is rich in odd harmonics of 1.25 MHz. To eliminate the odd harmonics and pass only the 1.25-MHz signal a low-pass filter is used (LPF - 1.25).

      f.   84-MHz Intersynthesizer Signal

      The 84 MHz output is basically generated in four steps. The first step is dividing down the 5-MHz reference to a 1-MHz squarewave using TTL logic. Second, is to extract and amplify the seventh harmonic of the 1-MHz squarewave by following the TTL logic (5) output with a 7-MHz bandpass amplifier (BPA-7). Third step is to multiply the 7 MHz to 42 MHz using the rectangular pulse technique described in paragraph b. The fourth and last step is doubling the 42 MHz to 84 MHz using an amplifier with a push-pull tuned input and a push-push tuned output (X2/84).

      Referring to the block diagram of the MTAR board 2, the synthesis of each output is discussed.

      a.   81.25-MHz Output (TX-LO)

      The 81.25-MHz output is generated in two basic "mix and amplify" steps. The first mix and amplify step is to generate 21.25 MHz from 20 MHz and 1.25 MHa. The mixer M2 inputs a 20-MHz signal and a 1.25-MHz signal; it outputs the sum and difference of the inputs. Since only the sum (21.25) is desired it is

necessary to filter (BPF - 21.25) and amplify (BPA - 21.25) to obtain the desired 21.25-MHz signal. The second step is to mix 21.25 M_h z and 60 MHz (provided by MTAR board 1) in M3 and extract only the sum (81.25 MHz). The BPA - 81.25 selects the desired sum from M3 and amplifies the 81.25 MHz to the desired level of +8 DBM. The 81.25 MHz is now applied to the power divider (PD - 4). One of the divided outputs is used as a TX-LO; the other is employed in the synthesis of 333.25 MHz on MTAR board 2.

      1.   67.75-MHz Output (TX - IF)

        The 67.75-MHz output is synthesized in two basic "mix and amplify" steps. The first step is to generate 16.25 MHz from the sum of 5 MHz and 1.25 MHz. The mixer M1 inputs a 15 MHz signal and a 1.25 MHz signal; it outputs the sum and difference of the inputs. Since the sum (16.25) is wanted and nothing else, it is necessary to filter (BAF - 16.250) and amplify (BPA - 16.25) in order to obtain the desired output. The second step is to mix 16.25 with 84 MHz in M4 and extract only the sum of 67.75 MHz. The BPA - 67.750 selects the desired sum from M3 and amplifies the 67.750 to the desired level of +7 dBm.

      2.   333.25-MHz Output (TX - LO)

        The 333.25-MHz output is generated in two basic steps. The first step multiplies the 84-MHz signal from PD3 times 3 to 252 MHz (X3 mult. 252). The second step is to mix and amplify where the sum of 252 MHz and 81.25 MHz is extracted from M5 and amplified by BPA - 333.25 to become the desired output of 333.25 MHz at +5 dBm.

      b.   Referring to the block diagram of the MTAR frequency synthesizer, the outputs of the MTAR board 3 is discussed. Three basic internal frequencies 10, 15, and 20 MHz are first generated. The following discussion is of the synthesis of the MTAR board 3 outputs using the three basic interval frequencies 10, 15, and 20 MHz.

      1.   10.75 MHz Output (INJ - 3)

        The 15 MHz supplied by BPA - 15 is divided by a factor of 20 to produce a 750 kHz TTL logic output. This output is low-pass filtered to remove all harmonics and is applied to one port of M1. The other port of M1 has 10 MHz applied to it. The output of M1 (sum of 10 MHz + 750 kHz) is filtered and amplified to provide a 10.75-MHz output signal.

2.   80-MHz Outputs (R^0 & INJ-1)

The 80-MHz outputs are obtained in one basic step. The
20 MHz, supplied by BPA-20, is applied to rectangular pulse generator PG-2 which
will generate the fourth harmonic of 20 or 80 MHz. This 80 MHz is now filtered from
the adjacent harmonics and amplified by BPA-80. The output of BPA-80 is power
split by PD-2 to provide the two 80-MHz outputs needed.

3.   45-MHz Output (INJ - 2)

The 45-MHz output is generated in one basic step. The
15 MHz, supplied by BPA-15, is applied to a times-three tripler which multiplies the
15 MHz to 45 MHz; this now becomes the 45 MHz output (INJ-2).

4.   5 MHz (SQW-TTL)

The 5-MHz output is simply a hard-limited version (TTL
Logic) of the 5-MHz reference (VCO).

3.3.4.3   Transmitter

A functional description of the MTAR modulator board follows (figure 3-43).
For a description of the other transmitter printed wiring boards see the MMT section
of this report.
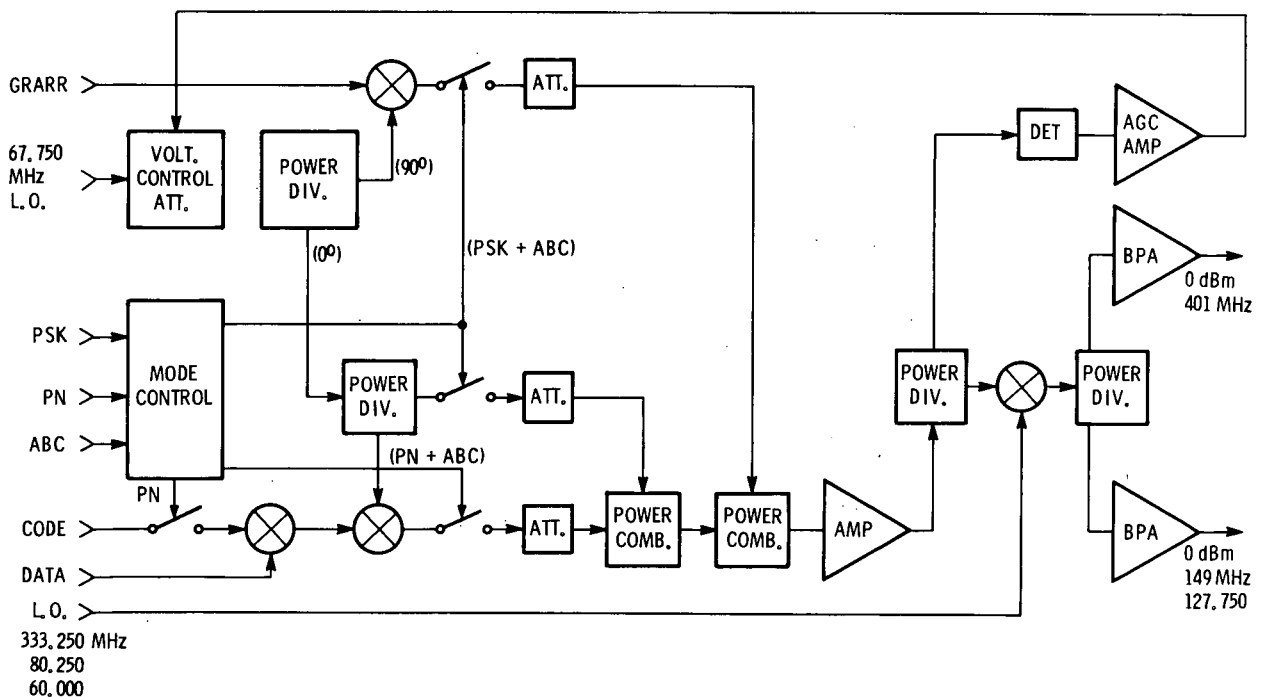
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Figure 3-43. Block Diagram, MTAR Modulator Board

3-97

3.3.4.3.1 MTAR Modulator

There are three modes of operations:

a.   PN Mode

The data to be transmitted is first modulo-2 added to a PN code. The resulting signal then balance-modulates a 67.75-MHz carrier to generate a PSK, spread spectrum signal for transmission.

b.   Conventional PSK Mode

Digital data balance-modulates one phase of a 67.75-MHz carrier, while GRARR signals balance-modulates another 67.75-MHz carrier which is in quadrature with the former. The two PSK signals are then summed with an unmodulated carrier to generate the final modulator output. The composite signal in phasor representation is shown in figure 3-44.

Since digital data are coded in manchester form and lowest GRARR tone is 4 kHz, there is no carrier component contributed by either PSK signals. Thus, at the receiver, the transmit unmodulated carrier will be tracked so that digital data appear at the I-channel and the GRARR signal at the Q-channel.

The power division between the PSK signal and the unmodulated carrier in the data channel is 4 to 1. That is, 20 percent of the total data-channel power is used for carrier tracking. This results in roughly 2 dB loss relative to the case where all power is allocated to data and carrier tracking is accomplished with a Costa's loop.

UNMODULATED
CARRIER $(\pi/2)$

DIGITAL DATA
PSK CARRIER $(\pi/2, -\pi/2)$

GRARR PSK
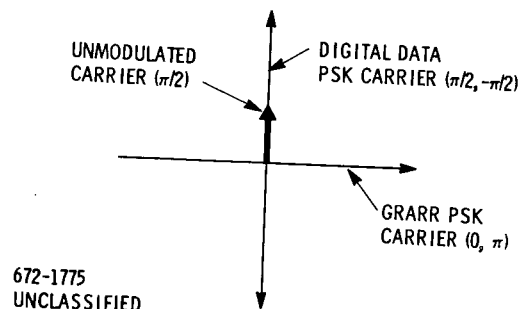CARRIER $(0, \pi)$

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Figure 3-44. MTAR Composite Signal in Phasor Representation

c.   ABC Mode

The modulator operates identically as described in the conventional mode except with the additional requirement that the transmit signal be gated on and off in accordance with the ABC burst format. This is accomplished in the balance modulator by gating on and off the local oscillator with the ABC gating signal.

To keep the modulator total output power constant as its operating mode changes, the modulator output is fed back through an AGC loop to regulate the carrier level. After the AGC feedback power divider, the modulated 67.75-MHz signal is mixed with the selected transmit local-oscillator frequency. The output frequency can be 127.75 MHz, 149.0 MHz or 401.0 MHz.

3.3.4.4   Baseband

The processing of the baseband digital data and PDM voice in the MTAR is similar to that described for the MMT. The only difference is that there is no convolutional encoder in the MTAR. Forward error encoding will be tested in the return link (MMT to MTAR) only.

3.3.4.5   GRARR Transmit Processor Board

The GRARR transmit processor board performs the digital simulation of the GRARR composite range tone signal. The input to this board is the GRARR range tone signal containing the 20-kilobits-per-second kHz, 4.0 kilobits-per-second kHz, and 4.8 kHz tones. The board output to the MTAR transmitter is a 40-kilobits-per-second digital sequence. The one-zero bit pattern of the sequence was chosen to contain equal spectral amplitudes of the three original tones and insignificant amplitudes of all other frequencies. The length of the sequence equals the time between coincident zero crossovers of the three tones. Digital simulation of the GRARR tone signal allows use of QPSK modulation for simultaneous range measurement and transmission of command-telemetry digital data.

As shown in figure 3-45 three bandpass filters separate the composite tone signal into its 20-kHz, 4.8-kHz and 4.0-kHz components. The zero crossover coincidence of the three tones is detected in order to establish the time relationship between this event and the start of the digital sequence. The 40-kilobits-per-second digital clock is derived from the 20-kHz tone. The clock drives the address counter for the read only memory containing the digital sequence.
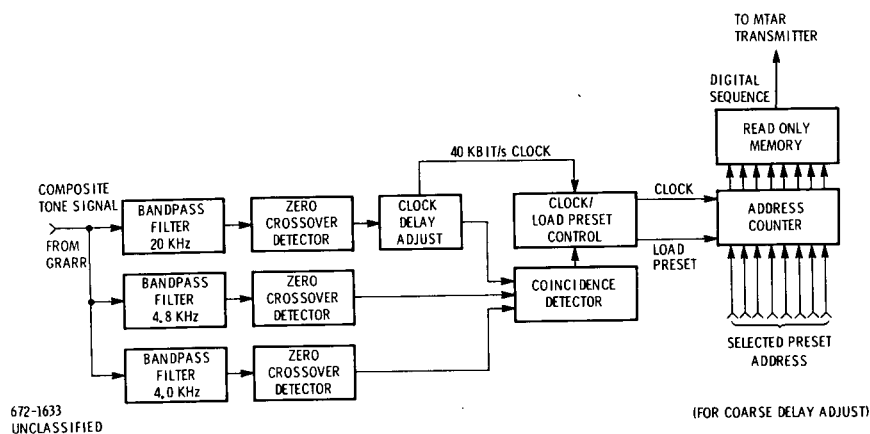
TO MTAR
TRANSMITTER

DIGITAL
SEQUENCE

COMPOSITE
TONE SIGNAL

FROM
GRARR

BANDPASS
FILTER
20 KHz → ZERO
CROSSOVER
DETECTOR → CLOCK
DELAY
ADJUST

40 KBIT/s CLOCK

CLOCK/
LOAD PRESET
CONTROL

CLOCK

READ ONLY
MEMORY

ADDRESS
COUNTER

LOAD
PRESET

BANDPASS
FILTER
4.8 KHz → ZERO
CROSSOVER
DETECTOR

COINCIDENCE
DETECTOR

BANDPASS
FILTER
4.0 KHz → ZERO
CROSSOVER
DETECTOR

SELECTED PRESET
ADDRESS

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UNCLASSIFIED

(FOR COARSE DELAY ADJUST)

Figure 3-45. Block Diagram — GRARR Xmit Processor Board

Each time zero crossover coincidence is detected, the address counter is loaded with the selected preset address. This coarse delay adjust makes it possible to start the sequence on any bit in that sequence. The fine delay adjust controls the 40-kilobits-per-second clock. The delay for system calibration will be determined experimentally. The preset address is set by adding jumpers on the board for the appropriate address lines.

The GRARR/MTAR interface as shown in figure 3-46 is made at base-band. The range tones are transmitted by the MTAR after the digital simulation described above. The digital sequence is detected and transmitted by the MMT (airborne unit). The received signal detected by the MTAR contains the range tones generated by GRARR. The GRARR modulator, transmitter, and receiver are not required for the testing with GRARR and the MMT/MTAR equipment.

The MTAR unit can be placed in or near a GRARR site (such as Rosman, N.C.) instrumentation building. Two coax cables will connect the MTAR to connectors accessible in the signal generation cabinet (U8). The composite range tone signal which normally goes to the GRARR modulator will be cabled to the MTAR unit. In order to avoid modification to the GRARR equipment, the "test" mode will be utilized for experiments with the MMT/MTAR equipment. The detected range tone signal from the MTAR will be connected to the cable that normally connects to U8A5-J16. This cable normally takes the range tone test signal from the zero-set phase shifter to the range-tone processor.

3.3.4.6 Range-Rate Outputs

Signal output connectors are provided for external range-rate measurements to be made. An MTAR transmit reference frequency from which the forward-link-carrier frequency is synthesized is brought out to a front-panel connector. An MTAR receiver local-oscillator frequency offset by the two way doppler error (the MMT is a coherent transponder) is brought out to a front-panel connector.
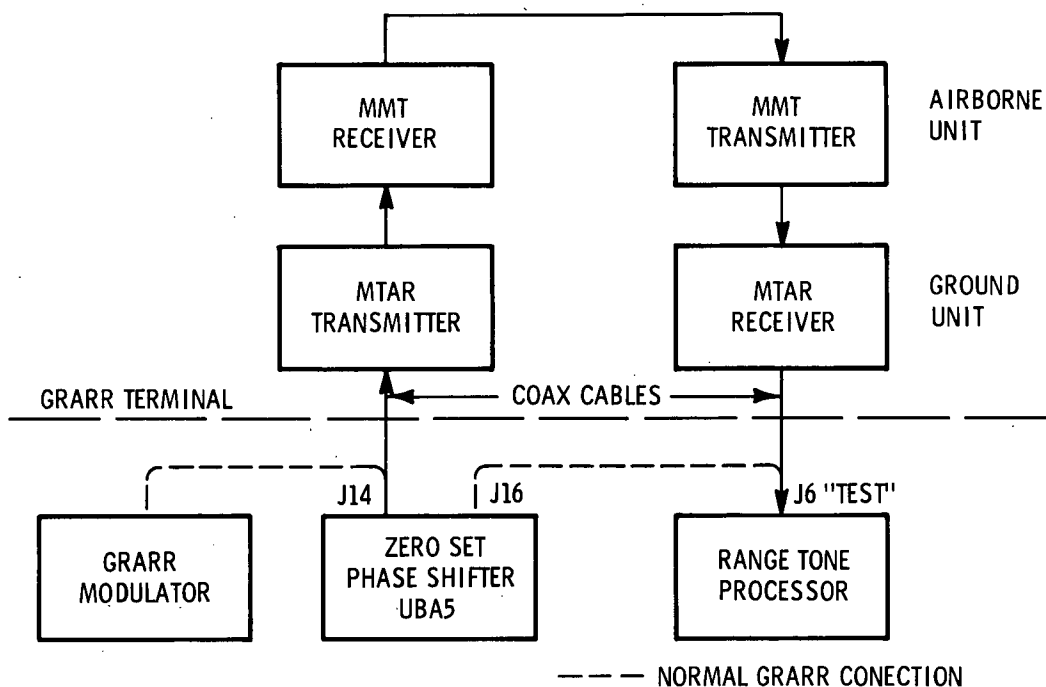
Figure 3-46. GRARR/MTAR Interface

3.3.5   CONTROL BOX

A remote control box is provided for the MTAR. Front panel switches and indicators are provided to facilitate mode selection for the experiments to be performed.

The following selector switches are provided on the MTAR control box.

* Link Mode   - Forward only
                 Transpond
                 Return only

* Modulation Mode - PSK
                     PN
                     ABC

* ABC Format - 2 (MS)
                 4 (MS)
                 6 (MS)
                 8 (MS)
                10 (MS)

Forward Link

- PN Chip Rate - 34.133 K chip/s
                     102.4   K chip/s

- Data Rate -   100 bits/s
                    300 bits/s
                    1000 bits/s

    Voice

- Frequency - 127.75 MHz
                    149.0   MHz
                    401.0   MHz

Return Link

- PN Chip Rate - 34.133 K chip/s
                     102.4   K chip/s
                     1024.0   K chip/s

- Data Rate -   0.3 K bits/s
                    1.0 K bits/s
                    3.0 K bits/s
                    10.0 K bits/s
                    Voice

- Forward Error Encode - ON
                                       OFF

A margin-to-threshold meter scaled in dB is provided for each of the two diversity receivers.

The control panel interface board contains a pull-up resistor for each control wire from the mode-selection switches listed above. This board also contains the lamp drivers for the indicator lamps.

3.3.6   POWER SUPPLY

The MTAR power supply chassis contains four regulated power supply modules to supply DC voltages of +28V, +15V, -15V and +5V to the RF/IF chassis and the signal processor chassis.

The power supply module specifications allow prime input power to be 105-125 VAC, 50-400 Hz. These power supply modules feature short circuit and overvoltage protection. Full specifications are contained in drawing X625196.

The estimated DC power requirements for the MTAR are listed below.

+28V	100 watts
+15V	30 watts
−15V	30 watts
+5V	45 watts

3.3.7 TEST EQUIPMENT

The list of test equipment for experiments with the MMT/MTAR equipment is shown in table 3-5. Each instrument is commercially available.

The Hewlett-Packard Model 5248M frequency counter will be used to measure range in the pseudonoise mode of operation. Using the time interval plug-in, start and stop pulses derived from the MTAR transmit and receiver "all ones" code vectors can be used to measure round-trip propagation time. This method will be more accurate than the earlier technique of gating a built in high frequency oscillator.

The digital recorder will be driven from the counter and will provide a range printout at the desired time intervals.

Table 3-5. Commercial Test Equipment

| ITEM	PART NO.	DESCRIPTION	VENDOR	QTY
1	5248M	ELECTRONIC COUNTER	H P	1
2	5253B	COUNTER PLUG-IN (HETERODYNE CONVERTER)	H P	1
3	5267A	COUNTER PLUG-IN (TIME INTERVAL UNIT)	H P	1
4	5050B-003	DIGITAL RECORDER	H P	1
5		RECORDER COLUMN DRIVERS	H P	4
6	OPTION 32	RECORDER INTERFACE CABLE	H P	1
7	OPTION 055	RECORDER PROGRAMMER	H P	1
8	MX-270	BIT ERROR ANALYZER	MRL	2

3.3.8   COMMAND/TELEMETRY DATA GENERATOR

As part of the overall multimode transponder design a data source will be provided at both the MMT and MTAR terminals to simulate telemetry and command data sources respectively. A pair of Magnavox MX-270 Bit Error Rate Analyzers have been selected for the task. In addition to functioning as data generators, they will provide a method for measuring bit-error rates.

The MX-270 shown in figure 3-47 provides a direct readout of error rate performance for digital communications modems. During operation, test data for the modem channel is clocked out of the MX-270 transmitter section at any rate up to 10 megabits per second. Similarly, the modem clocks data into the MX-270 receiver section. This received sequence is compared bit-by-bit with the generated test sequence and thus the error rate is directly indicated. When a channel is tested on a simplex or full duplex basis, two MX-270's are required.

A simplified block diagram of the MX-270 is shown in figure 3-48. There are four basic sections in the MX-270: a) transmitter, b) receiver, c) counter, and d) power supply. During operation, a clock pulse received from an external source generates a data pattern selected by the front-panel controls. The modem under test demodulates the data pattern and supplies the demodulated data pattern along with the data clock back into the receiver section of the MX-270. The MX-270 then injection loads a similar data-pattern generator and compares the injection-loaded pattern with the modem demodulated data pattern in a bit-by-bit comparison to generate an error pattern. This error pattern is then counted over a selected number of bits determined by the X10$^-$ front-panel control and the RESOLUTION control. The selected sample size error rate is then displayed on the ERROR RATE indicator.
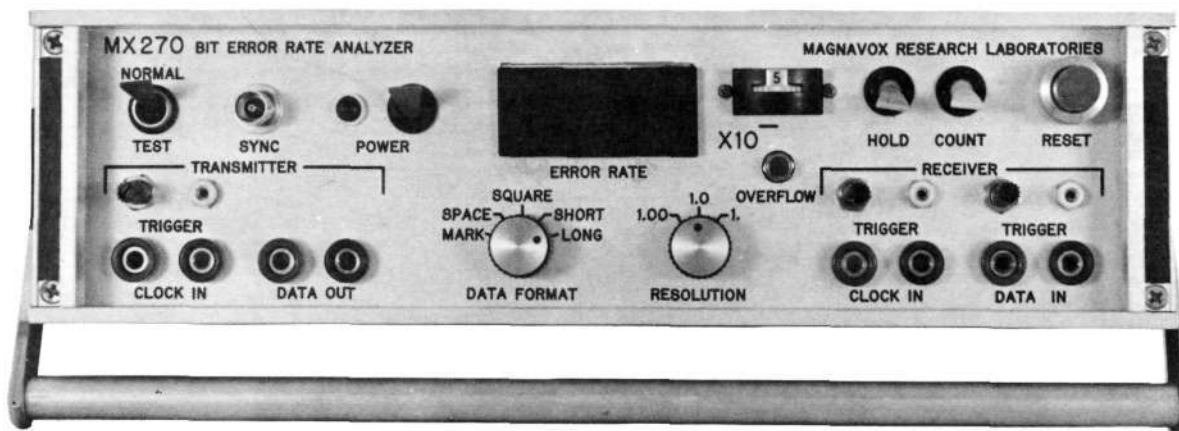
Figure 3-47.   MX-270 Bit Error Rate Analyzer
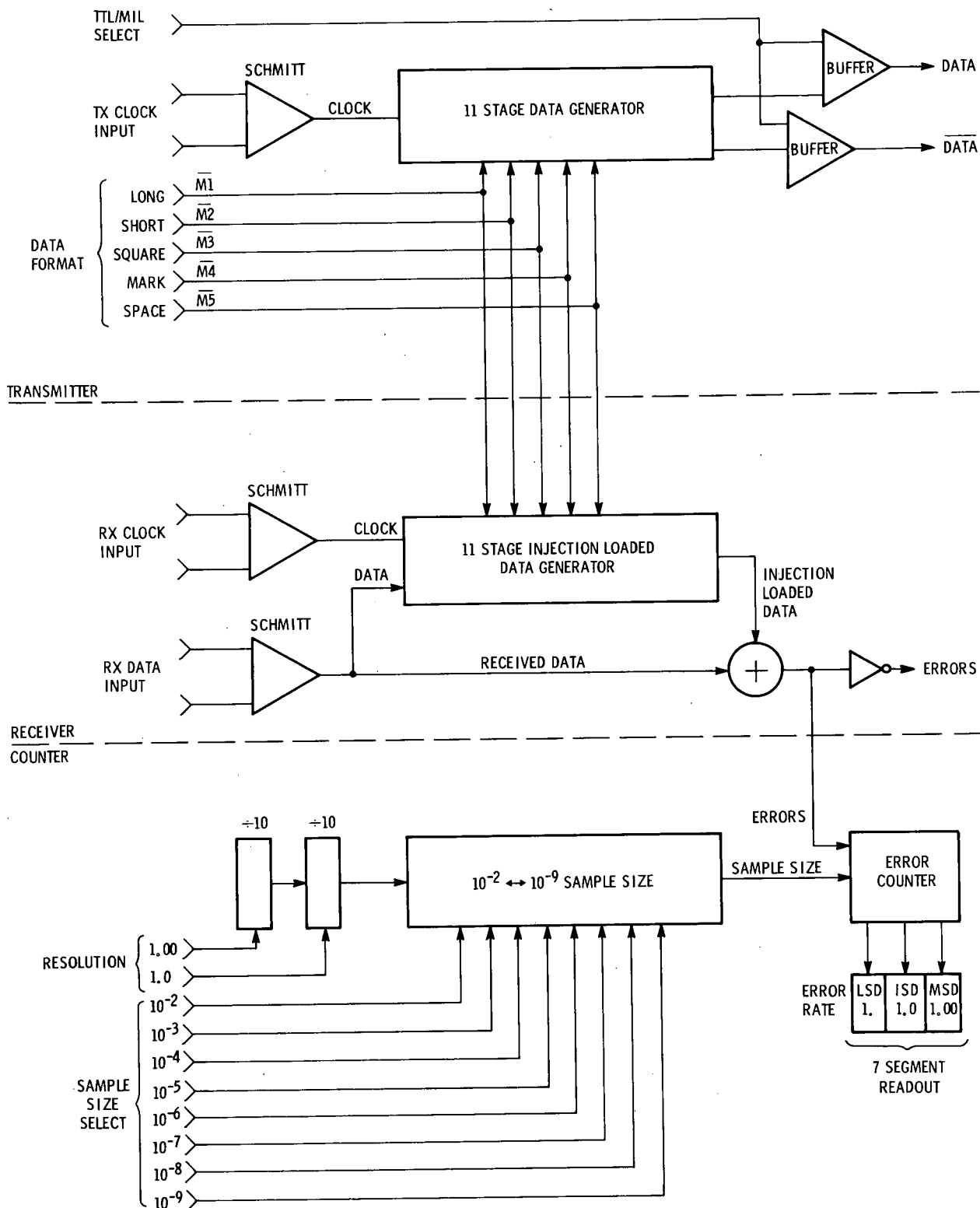
Figure 3-48. MX-270 Functional Block Diagram

SECTION IV

MECHANICAL DESCRIPTION

The TDRS equipment complement consists of the airborne MMT system and the MTAR ground system. Mechanically, the two systems are nearly identical with the chief differences being panel layouts and/or placement of electronics within a chassis. Design of both systems is based on the more stringent environmental conditions that may be experienced by the airborne MMT equipment.

Each system consists of four units: signal processor, RF/IF unit, control unit, and power supply. A description of each unit is presented in the following section. Because the MMT and MTAR systems are mechanically similar, illustrations will be limited to the MMT configuration only.
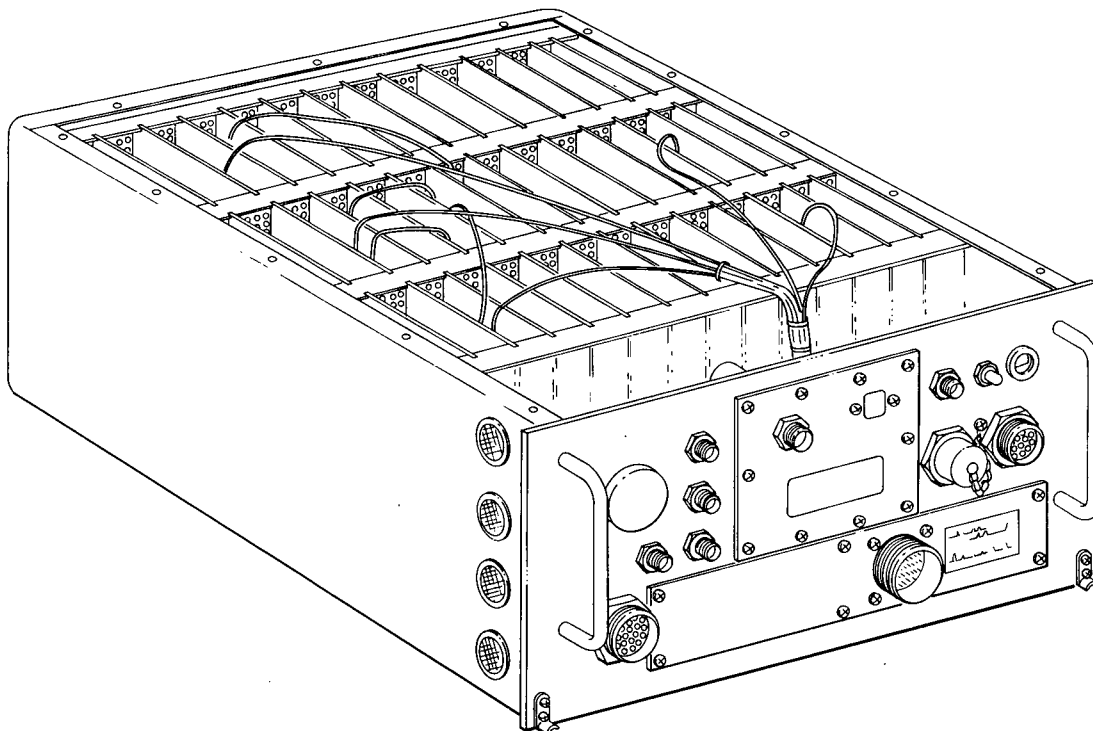
4.1   MECHANICAL DESIGN

4.1.1   SIGNAL PROCESSOR

The signal processor will be a basic 1 1/2 ATR size, 15.38-inches wide x 7.63-inches high x 18.10-inches long. The design is generally in accordance with the requirements of MIL-C-172. The design goal for total weight, including electronics will be 35 pounds. Structural and environmental design will be based upon installation aboard a transport type aircraft like a C-121G. See figure 4-1 for basic chassis configuration.
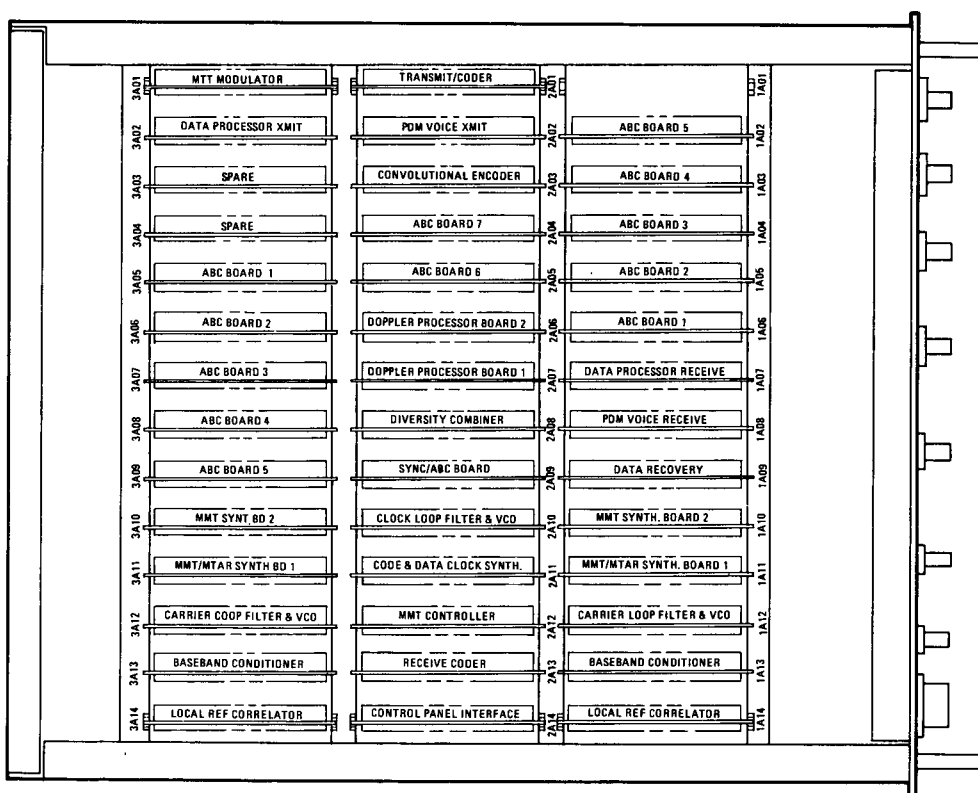
Basic construction of the unit will be sheet aluminum, with internal honeycomb sections that impart structural strength in addition to the primary task of providing free passage of cooling air and RFI protection between rows of circuit boards. A standard holddown arrangement will be provided for mounting in an MS 91405 type mounting tray.

The internal board rack is divided into three sections separated from each other by the honeycomb partitions. Each section is further divided into functional groupings of printed circuit board separated by RF shields. See figure 4-2 for the MMT signal processor plan view, indicating card location. Packaging of the circuit elements makes broad use of microelectronic techniques. The circuit boards, supported in the case by means of metallic card slides, plug into printed circuit edge connectors

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Figure 4-1. Basic Chassis Configuration

3A01 MTT MODULATOR	2A01 TRANSMIT/CODER	1A01
3A02 DATA PROCESSOR XMIT	2A02 PDM VOICE XMIT	1A02 ABC BOARD 5
3A03 SPARE	2A03 CONVOLUTIONAL ENCODER	1A03 ABC BOARD 4
3A04 SPARE	2A04 ABC BOARD 7	1A04 ABC BOARD 3
3A05 ABC BOARD 1	2A05 ABC BOARD 6	1A05 ABC BOARD 2
3A06 ABC BOARD 2	2A06 DOPPLER PROCESSOR BOARD 2	1A06 ABC BOARD 1
3A07 ABC BOARD 3	2A07 DOPPLER PROCESSOR BOARD 1	1A07 DATA PROCESSOR RECEIVE
3A08 ABC BOARD 4	2A08 DIVERSITY COMBINER	1A08 PDM VOICE RECEIVE
3A09 ABC BOARD 5	2A09 SYNC/ABC BOARD	1A09 DATA RECOVERY
3A10 MMT SYNT. BD 2	2A10 CLOCK LOOP FILTER & VCO	1A10 MMT SYNTH. BOARD 2
3A11 MMT/MTAR SYNTH BD 1	2A11 CODE & DATA CLOCK SYNTH.	1A11 MMT/MTAR SYNTH. BOARD 1
3A12 CARRIER COOP FILTER & VCO	2A12 MMT CONTROLLER	1A12 CARRIER LOOP FILTER & VCO
3A13 BASEBAND CONDITIONER	2A13 RECEIVE CODER	1A13 BASEBAND CONDITIONER
3A14 LOCAL REF CORRELATOR	2A14 CONTROL PANEL INTERFACE	1A14 LOCAL REF CORRELATOR

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Figure 4-2. MMT Plan View of Board Rack

4-2

located on the connector plate at the bottom of the unit. All circuit boards will be keyed to reduce possibility of harmful effects from improper signals when plugged into the wrong slots. In addition all like voltages will be assigned the same pin location for all circuit boards and connectors. All circuit boards will be 4.00 inches by 6.00 inches (see figure 4-3) with 50 edge contacts for input-output power and signal connections. In addition, each card will have an edge contact at the top which provides 20 test-point connections.

All interface connectors will be located on the front panel. Input-output line filters will be located behind the front panel. See figure 4-4 for the front panel configuration of the MMT version of the signal processor. Both the top and bottom covers will be provided with 1/4 turn fasteners to enhance removal and reduce downtime. Access to test points on the circuit boards and module cans will be provided from the top of the unit. All wiring with the exception of some RF-module coax interconnects will be done from the bottom. Both front and rear panels will be detachable to provide easy access during wiring and/or service operations. Basic circuit-card layout will be divided into functional groupings. As indicated in figure 4-2, the boards will be separated into three rows with honeycomb sections between rows providing RF protection. In addition, metallic shields will be placed between individual boards to provide increased isolation.

4.1.1.1   ABC Implementation

Power consumption for the ABC design will be about 25 watts in the voice mode and 17 watts in the data modes. The system uses 13 MRL universal circuit boards and, for a board spacing of 1/2 inch, will occupy about 156 cubic inches.

The weight will be 2.7 pounds not including mating-card edge connectors which are part of the MRL card cage.

The design of the ABC Encoder and Decoder was subject to several constraints. Since the system was designed to verify feasibility of the ABC technique in an airplane test situation, only secondary consideration was given to power, size, and weight. The power requirements of the ABC Encoder and Decoder are largely consumed in the memory portions of the equipment. A reduction in memory power would reduce the total system power drastically since memory utilization in the voice mode is three times that of the maximum memory required for the data mode. The present design incorporates memory power switching to reduce the memory power in the data mode by removing unused memory elements from the circuit. The TTL logic and

dual-in-line (DIP) packages were selected on the basis of cost. A considerable reduction in size could be obtained through the use of flat packages.

Future Implementation -- A secondary design for the ABC Encoder and Decoder has been formulated based on presently available MOS integrated circuits. This design gives foremost consideration to minimization of power requirements. Through the use of CMOS, this design achieves identical circuit performance with less than 1/10 of the power required by TTL devices. A reduction im memory power is achieved through the use of MOS memories as opposed to bipolar TTL memories. It is anticipated that the size and wieght of the entire system will not change appreciably. As in the present implementation, the system is configured on 13 MRL universal printed circuit boards. The power dissipations of the CMOS design is approximately 3 watts.

4.1.2   RF/IF UNIT

The RF/IF unit will be 15.38-inches wide x 7.63-inches high x 18.10-inches long. Structural and environmental design will be based upon installation aboard a transport type aircraft. The design goal for total weight will be less than 25 pounds. See figure 4-5 for the front-panel configuration of the MMT unit.

Basic construction of the unit will be a simple brazed sheet aluminum box. The case will be RF sealed by utilization of RF gasketing at the top cover. Since power dissipation is low and cooling is by natural convection, conduction and radiation to the case will be adequate. All input-output power and signal connectors as well as the power attenuator(s) will be located on the front panel. A standard holddown arrangement will be provided for mounting in a MS 91405 type mounting tray.

Access to all components will be from the top. The cover will be provided with 1/4 turn fasteners to speed removal.
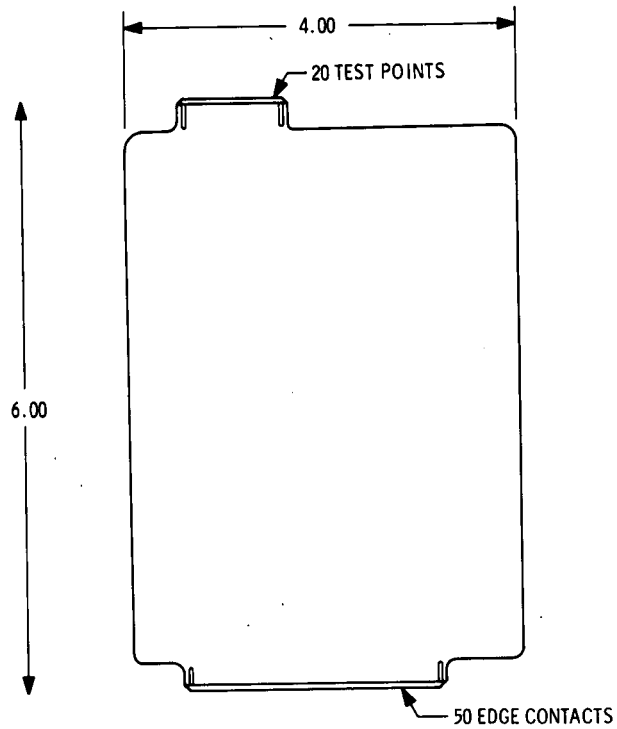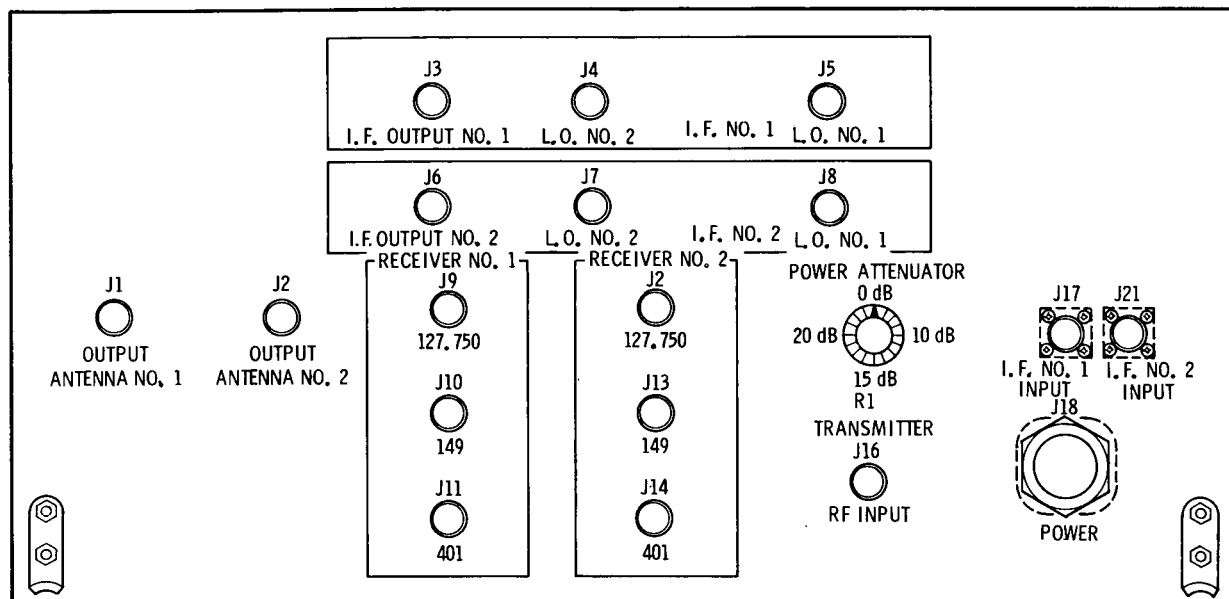
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Figure 4-3. Circuit Board Outline
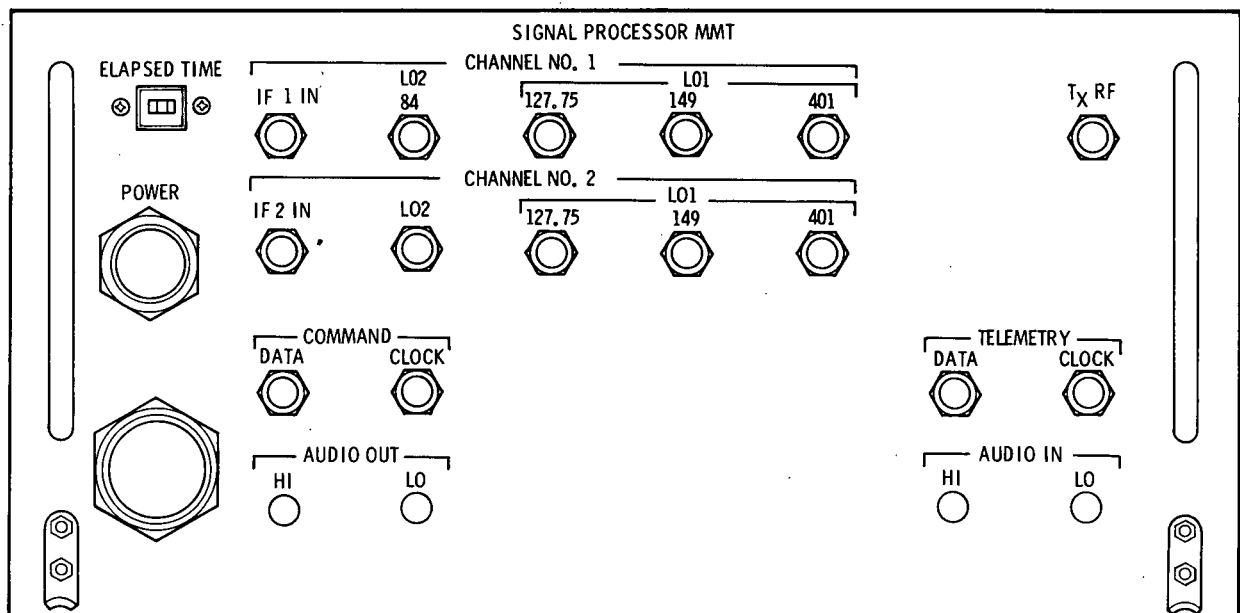
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Figure 4-4. Front Panel, Signal Processor (MMT)

Figure 4-5. Front Panel, RF/IF Unit (MMT)

4.1.3   POWER SUPPLY

The power supply chassis will be 15.38-inches wide x 10.69-inches high x 18.10-inches long. Structural and environmental design will be based upon installation aboard a transport type aircraft. Basic construction of this unit will be sheet aluminum, with liberal use of stiffening devices to support module weight. The design goal for total weight will be less than .75 pounds. See figure 4-6 for basic chassis configuration. Since prepackaged power supply modules will be used, wiring will be simplified, and will be accessible from the bottom of the unit. Each module will have a forced-air heat exchanger which extends into the air plenum. A standard holddown arrangement will be provided for mounting in a MS 91405 type mounting tray. Both top and bottom covers will be provided with 1/4 turn fasteners to expedite installation and removal.
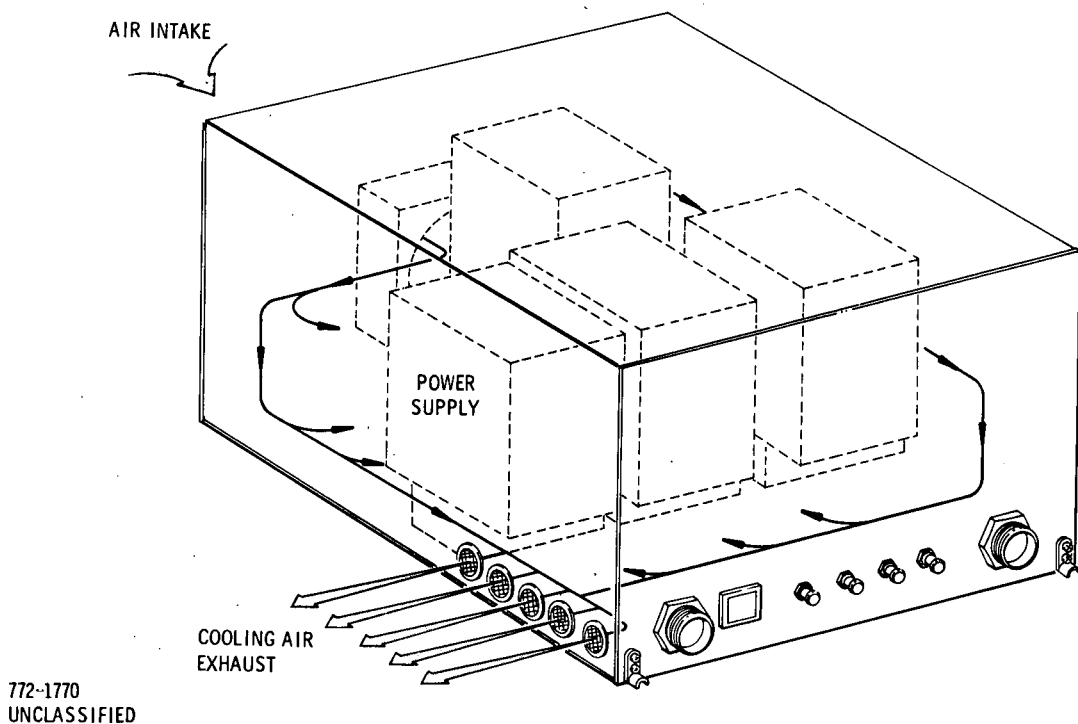
AIR INTAKE

POWER
SUPPLY

COOLING AIR
EXHAUST

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Figure 4-6. Power Supply

4.1.4 CONTROL UNIT

The control unit chassis will be 5.75-inches wide x 9.00-inches high x 3.00-inches deep. Structural and environmental design will be based upon installation aboard a transport type aircraft. Basic construction will be sheet aluminum. Total weight will not exceed 10 pounds as a design goal. Se figure 4-7 for the MMT panel arrangement. All controls and.displays will be located on the front panel. Wiring will be behind the panel. A dust cover will protect the rear portions of all components. Panel size and fastener arrangement is generally in accordance with MS 25212.

4.2 ELECTROMAGNETIC INTERFERENCE (EMI) CRITERIA

The equipment will be designed to operate satisfactorily in the intended installations without experiencing or creating abnormal EMI conditions. To accomplish this objective, reasonable care will be taken to conform to established EMI/RFI design practices. Descriptions of various design techniques are described in the following sections. Discussion is limited to those items which serve to contain interference or reject susceptibility causing signals through other than RF intentional signal paths

4-7

Figure 4-7. Control Unit (MMT)
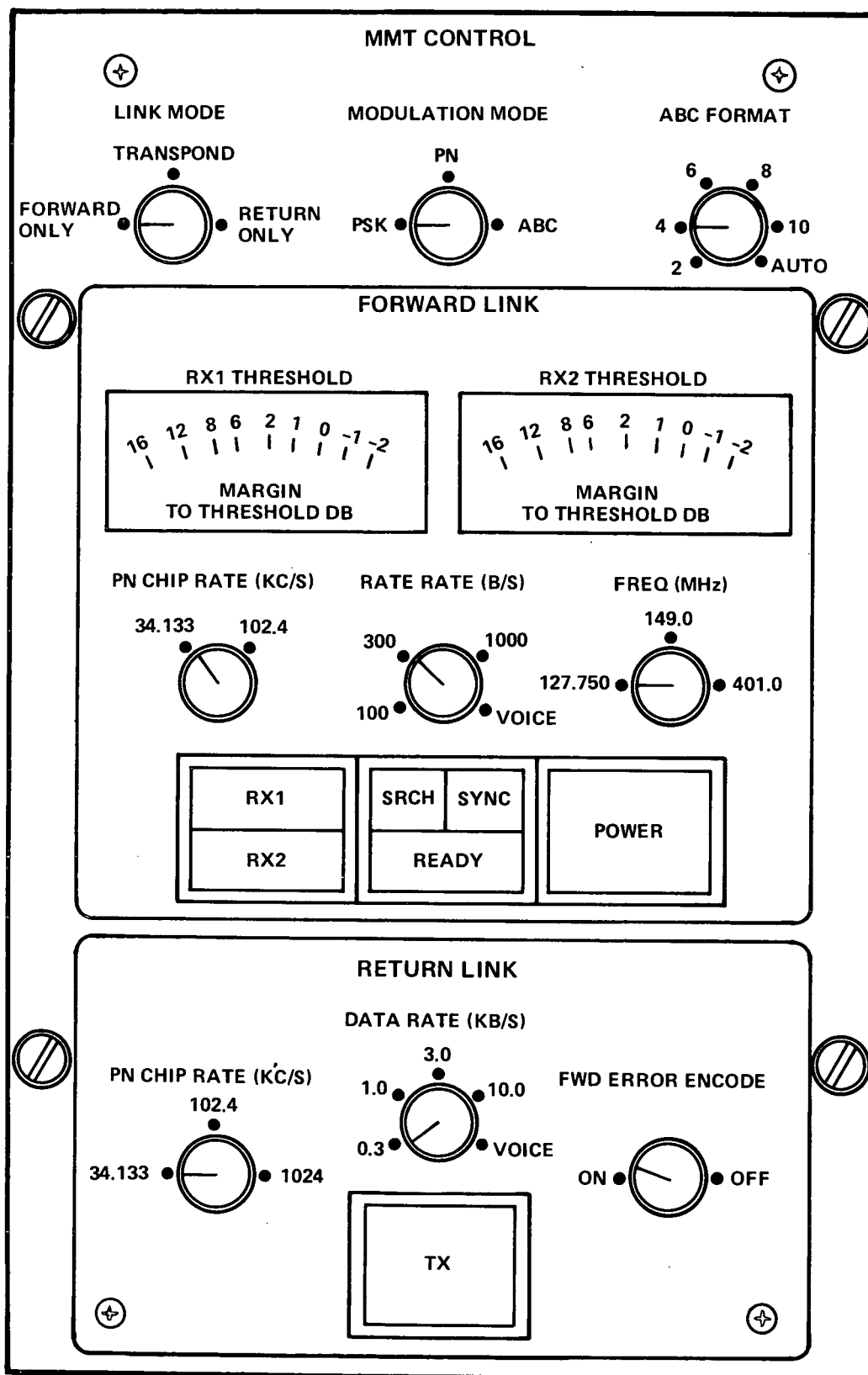
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4-8

(i.e. power line filtering, shielding and decoupling). To reduce the effects of conducted interference, filters will be provided on input-output power and signal lines.

Power line filters will be installed having minimum inertion loss of 20 dB at 1 kHz, 40 dB at 150 kHz and 63 dB at 1 MHz and above. Low-frequency ripple filters will be used on power supply outputs. Decoupling capacitors will be utilized on IF, logic, and frequency synthesizer circuits. A filter or decoupling capacitor will be installed on each digital interface lead to minimize high frequency common mode propagation. Most filters will be of feed-through construction and will be bulkhead mounted.

Radiated interference presents a more complex problem which will be attacked by a myraid of conventional methods. Inside the unit, emphasis will be placed on local isolation of RFI sources, as well as RFI sensitive circuits on the circuit boards. This isolation at the component or subcircuit level will provide the simplest and most effective control of radiation, by providing RF suppression along the circuit path.

Shielded components will be connected via feed-through filters and coax lines. Data lines will be of twisted-shielded-pair configuration. An overall cable shield will be required where long lead runs are used. An overall cable shield of 90 percent coverage will be provided for digital lines. Overall shields will be grounded to the equipment chassis at each end. All RF signals will be transmitted in coax lines.

Additional shielding will be provided around complete circuit boards or groups of boards as necessary. Since shielding at this level is only minimally effective, expensive of space, and may in some cases interfere with cooling air circulation, efforts will be made to minimize shielding requirements at this level. However, where RFI shielding is required in the board rack, a conductive plate will be installed between board with grounding provided by conductive bonding along the sides and, where required, knitted wire mesh at the top and bottom. The connector plate at the bottom of the board rack will provide a shield in addition to providing the mounting surface for the circuit-board connectors.

As was noted earlier, the honeycomb sections in the signal processor units provide RFI protection between the rows of circuit boards while allowing a relatively unimpeded flow of cooling air from the forced-air cooling source.

Separate ground busses will be maintained for signal neutral and case grounds. Provision will be made to tie these busses to case ground inside the equipment or externally as necessary by the design. Modules which are potential sources of high-level interference, and parasitics such as frequency dividers, local oscillators, etc., and circuits sensitive to interference will be individually packaged in their own shielded cases. All interface lines will be covered and/or filtered to preserve shielding integrity.

The design philosophy shall be to use feed-through filters for dc power, bias and control lines at the shielded enclosure interface.

Shielding at the chassis level will be accomplished as follows: The cases will be RF sealed utilizing overlapping riveted joints and oriented wire-silicone rubber gaskets at the top and bottom covers.

In the RF/IF units all joints will be welded. The top-cover interface will utilize knitted-wire-mesh gaskets with closer spacing for the fasteners. Fastener spacing will be determined by establishing the critical wavelength and setting the spacing at a dimension less than this value, to prevent frequency cutoff conditions for waveguide type leakage through the enclosure-cover interface.

4.3   THERMAL

The cooling design will be based on satisfying the requirements for installation in a transport aircraft of the C-121G type. Since the quality of the cooling air (cabin air) will be suitable for direct flow through the electronics, a simple fan-filter assembly attached to the rear of both the signal processor and power supply will be all that is required. Cooling air therefore enters the enclosures at the rear and exhausts at the sides just behind the front panel. No air passes directly out the front of the boxes where it could cause discomfort to an operator.

As was noted, the honeycomb partitions allow free passage of air through the signal processor electronics. Power dissipation in the signal processor will be less than 200 watts. Using a fan which is rated at 110 CFM at free delivery, airstream temperature rise will not exceed 5 degrees C.

The power supply unit contains the power supply modules which, in all but one case, are forced-air cooled. Cooling air travelling through the plenum must pass through the power supply heat exchangers before reaching the exhaust ports. Temperature rise in the airstream will be less than 10 degrees C.

Both RF/IF units and the control units are low-thermal dissipators and therefore do not require forced-air cooling. Cooling of these units is by natural convection, conduction, and radiation.

4.4 MAINTAINABILITY

In the signal processor, virtually all circuitry will be packaged on plug-in printed circuit boards. Removal of the top cover will provide access to all boards in the rack. Test points will be provided along the top edge of most boards to assist in fault isolation. All circuit boards plug into edge connectors located in the lower portion of the case. Faulty boards can, therefore, be simply extracted and replaced. Removal of the bottom cover permits access to the connector back-plane wiring and the main wiring harness. Both covers utilize quick-turn fasteners to facilitate openings and closings. Sonce each module in the power supply will be a self-contained unit, maintainability problems are minimized. The covers utilize quick-turn fasteners for ease of opening and closing.

Removal of the RF/IF unit cover (which also utilizes quick-turn fasteners) provides ready access to all elements of the electronics. Removal of the control-unit dust cover provides access to all components.

4.5 ENVIRONMENTAL CONSIDERATIONS

The modem will be designated to meet the functional performance requirements when exposed to the service condition environments specified in table 4-1. Engineering tests will be conducted during the design phase of the contract to evaluate the effects of service environments on critical design elements, thus ensuring that the final design will provide satisfactory performance under the specified service conditions.

Since moisture condensation will occur, it is possible that water can accumulate in locations that act as reservoirs. These locations are most likely to present serious problems where exposed electrical conductors are involved. A good example of this would be the vertically oriented printed circuit boards with the connectors at the bottom. Two approaches to this problem will be utilized. The first approach will be to orient all connectors such that condensation streams will not flow into the connectors. The second approach will be to orient all connectors such that drainage will be possible. The same applies to all components.

Table 4-1. Environmental Service Conditions

	STRESS LEVEL	
Environment	Operating	Non-operating
Thermal	32° F (0° C) to 122° F (50° C)	-25° F (-32° C) to 158F (65° C)
Relative Humidity	As low as 5% at 122° F (50° C); As High as 100% at All Temperatures From 32° F (0° C) to 85° F With Condensation At All Temperatures Lower Than 85° F (29° C)	Same as operating
Altitude	Up to 10,000 Feet Above Sea Level	Up to 25,000 Feet Above Sea Level
Vibration	5 Hz to 30 Hz: .02 inch double amplitude 30 Hz to 500 Hz: 1g	
Shock	As Encountered During Bench Handling	

Resistive shunting by conductive water film is a common source of unreliability in military equipment, especially if immediate turn-on capability is a requirement. These films can be prevented only by sealing the equipment and lowering the internal dewpoint through the use of desiccators. This is not an optimum solution since it places the burden of success upon diligent field assembly and maintenance. The most practical technique involves the use of appropriate conformal coatings or encapsulants over all circuits and limiting the use of exposed conductors (connectors, lugs on panel type components, transformers, etc.) to low impedance levels only.

Separation of susceptible exposed conductors will strongly influence connector pin assignments. Achieving low impedance signal levels at exposed conductors will require consideration as to where the connection will be made in the circuit or will require the addition of special circuitry to provide desirable low impedance levels.

SECTION V

RELIABILITY AND MAINTAINABILITY

5.1   RELIABILITY

The reliability of the TDRS Multimode Transponder is balanced with respect to total cost and the mission of the system for which the unit is planned. The transponder is thus constructed using the best commercial practices and designed to the extent possible to minimize weight, power consumption, and cost. All circuits are designed to operate over the temperature range of 0 degrees to 70 degrees C, and withstand a typical low performance aircraft environment:

a.   Test Vehicle

C-118 or C-121 transport aircraft

b.   Temperature

0 degrees to 50 degrees C cabin air

c.   Vibration

5 Hz to 30 Hz - 0.02 DA

d.   Altitude

25,000 feet - non-operating

e.   Humidity

5 to 100 percent

Temperature to 50 degrees C

By improving the reliability design requirements during the design phase, MRL will be able to provide production equipment with the minimum amount of change-over cost to meet the ultimate reliability requirement for the equipment.

5.2   MAINTAINABILITY

Virtually all circuitry, where possible, will be packaged on plug-in type printed circuit boards. Test points will be provided along the top edge of modules to

assist in fault isolation. All modules plug into edge connectors, so that faulty modules can therefore, be simply extracted and replaced. Removal of the top cover will provide access to all modules in the rack.

5.3 QUALITY ASSURANCE PROGRAM

The Quality Assurance Program shall meet the requirements of NASA Quality Publication NPC 200-3 (Inspection System Provisions for Suppliers of Space Materials, Parts, Components and Services) as amended by the contract. The required inspection plan will be submitted within 30 days if authorized to proceed with Phase II.

5.4 SOLDERING CERTIFICATION

During Phase II of the contract, all soldering operations will be performed and inspected by personnel that have been adequately trained and certified to the requirements of NHB 5300.4 (3A), Requirements for Soldered Electrical Connections. A solder training program is being established through the facilities of North American, Seal Beach, California, and will include training of all personnel necessary to perform Phase II of the contract.

Within 30 days of authorization to proceed with Phase II, a documented soldering program plan will be submitted for approval.

SECTION VI

SUMMARY AND CONCLUSIONS

This report contains a complete design of the multimode transponder and its associated ground support and test equipment. Candidate modes of operation being considered for use in an eventual tracking and data relay system servicing low data rate users at VHF/UHF have been implemented in this design. System trade-off studies have identified the forseeable technical problems and the solution of these problems is presented in this report.

The functional requirements of the multimode transponder are numerous and complex. The functions of command receiver, range and range-rate transponder and telemetry transmitter are to be performed in three principal modes: conventional, pseudonoise (PN) and ABC. Within each mode there is a multiplicity of selectable data rates, PN rates, and receive and transmit frequencies. Diversity reception is required in all modes.

6.1   TECHNICAL REPORT SUMMARY

Section I of this report contains the historical background for the multimode transponder program and briefly outlines the objectives and tasks associated with the program.

Section II contains a summary of the system trade-off studies and the resulting system design. Major sources of interference for the TDRS configuration are analyzed. The RFI is by far the greatest threat when compared to trash noise, multipath, and other users. Signal-to-noise power budgets for both the forward and return links are summarized and the multiple-access capability of the three major modes of operation. Techniques unique to the PN mode of operation including acquisitions and search strategy are discussed in detail. Range and range-rate measurement accuracies as a function of interference are analyzed and a method for interfacing the Goddard Range and Range Rate system is presented. Finally, the techniques for adaptive burst communications are discussed.

Section III contains a detailed functional description of the multimode transponder design which consists of two major groupings of equipment namely, the Multimode Transponder (MMT) and the Multimode Transmitter and Receiver (MTAR). The component design of the antenna, RF equipment, signal processing equipment, control-display panel and power supply is presented with emphasis on the solution of known problem areas. Commercial test equipment required to provide command and telemetry data and range and range-date readout is delineated.

Highlights of the design include:

● **RF Frequency Selection**

Four most likely RF frequencies for the Multimode Transponder design have been selected based on information from the current TDRSS study. They include 137 MHz for the return link and 127.750, 149 and 401 MHz for the forward link. All of these frequencies are provided in the Transponder design for use in future experiments and performance evaluations.

● **Diversity Combining**

Diversity combining is accomplished using the theoretically optimum maximum likelihood coherent combining method. It is found that in the PN modes, the combining must be done after correlation, but prior to data detection and developing the code tracking loop error signal. The classical coherent detectors used in PN and extracted reference PSK receivers are recognized as performing the essential function of pre-detection diversity combining, so that the combining is performed with very little more than twin PN receivers.

● **Multipath Discrimination**

In the PN modes, multipath immunity is provided for all multipath differential delays from a few microseconds up to 40 ms by suitable choice of PN sequence parameters. In the ABC mode, a set of burst program cycles includes at least one cycle which provides multipath immunity for any given altitude.

- Data Conditioning

    The transponder shall provide for demonstrating two way data trans-
    mission simultaneous with ranging or alternatively full duplex voice
    and ranging. Voice modulation shall employ the PDM technique.
    Telemetry data shall be transmitted either uncoded or with con-
    volutional encoding compatible with a GSFC decoder.

- PN Synchronization

    PN synchronization does not require special transmissions or pre-
    ambles. Synchronization will be performed on the TDRS signal even
    when it carries data destined for other users. Synchronization will
    be accomplished within a few seconds (exact values dependent on
    signal-to-noise of either TDRS coming over the horizon or handover.

- Test Equipment

    Test equipment is included in the multimode transponder unit to
    facilitate laboratory and flight testing. Among the functions to
    be provided are command message recognition and scoring, a
    telemetry data simulator and various test controls to select modes
    and facilitate test and maintenance.

Section IV contains a detailed mechanical description of all major assem-
blies. It discusses the equipment capability with respect to environment and interface.
It also includes the power, size and weight specifications.

Section V defines an "engineering model" and reliability, quality assurance
and maintenance aspects of the equipment to be fabricated in Phase II of the program.

6.2   CONCLUSIONS

The most striking aspect of this baseline design is the relative simplicity
in light of the requirements. Rather than performing the various modes of operation
in distinct circuitry, means have been found to utilize most of the circuitry in all
modes. The design was devised with reliability considerations in mind. For example,
the duality required for diversity is done in such a way that it also represents
redundancy for reliability. Should one channel of diversity fail, the transponder can
still function with only minor losses in performance.

6.2.1   ABC VERSUS PN

The strengths and weaknesses of the adaptive burst communications and pseudonoise modes of operation are documented in the contents of this report.

In summary, it is concluded that, even though the ABC system is feasible, the advantages of PN over ABC are substantial. For Phase II of the multimode transponder program, it is recommended that the overall effort be concentrated on the PN modes of operation along with a PSK mode for comparison.

6.2.2   GRARR INTERFACE

Interface with the GRARR system to provide a range capability for the narrowband PSK and ABC modes of operation in the multimode transponder design is not recommended for the following reasons:

- The anticipated integration effort required to interface the multimode transponder equipment with existing GRARR facilities is excessive.

- Actual performance capability of the GRARR will be compromised with the use of the digitized techniques necessary to interface the multimode transponder equipment.

- Existing GRARR transponders could be used to make range and range-rate comparisons in the PN mode of operation.

- MTAR must be located at the GRARR site for operation.

6.2.3   TRANSMIT POWER REDUCTION

It is recommended that the transmit output-power requirement of the transponder be reduced from 5 watts to 1 watt maximum. One watt of RF power is more than adequate for ground to aircraft testing as shown in section II of this report and it will reduce the cost of a number of major RF components.

6.2.4   PN CHIP RATES

The availability of three different PN chip rates for narrowband PN modulation consistent with bandwidth occupancies of 50, 100 and 500 kHz is recommended. The use of a 50-kHz bandwidth in the forward link would increase the processing gain in the PN mode of operation and decrease the output power flux density at the cost of additional acquisition time.

6-4

6.2.5 RANGE MEASUREMENT INTERFACE

It is recommended that the range measurement signal be supplied in the form of start and stop pulses which could be fed into an interval counter instead of a gated RF signal. The result would be a simplified interface and improved range measurement resolution.

6.2.6 RANGE RATE MEASUREMENT INTERFACE

To simplify the interface, it is recommended that a single frequency translated carrier component be supplied to an interfacing counter to measure range rate. It is not necessary to make all carrier local oscillators available to measure doppler effects.

6.2.7 FREQUENCY DIVERSITY STUDY

As a technique to provide additional RFI protection capability to the existing multimode transponder design as well as to provide an alternate to the PN mode of operation, the possibility of incorporating one or more of a number of viable frequency diversity techniques should be studied as soon as possible.

6.2.8 RETURN LINK RETRODIRECTIVITY

It is recommended that the retrodirective transmission capability be incorporated into the MMT design. It would (1) potentially improve the return link performance by 3 dB, (2) utilize information already available in the diversity receiver combining circuitry and (3) improve the system reliability by providing a second transmitter (the system already has dual receivers).

APPENDIX A

COMPUTER SIMULATION OF A GATED PHASE LOCKED LOOP

It was desired to determine the performance characteristics of the gated phase lock loop to be used in conjunction with the ABC mode of operation. Both the noise performance and tracking performance for a velocity ramp (parabolic phase input) was determined.

Gated Loop Operation

The operation of the loop is better understood by considering the equivalent model of the loop shown in figure A-1. During the gating burst (i. e. , when the switch is closed), the loop behaves approximately as a continuous phase lock loop. However, when the switch is open, the integrator portion of the loop filter causes the VCO to have a constant velocity offset corresponding to the voltage on the integrator when the switch opened. During this off portion (i. e. , switch open), the input to loop may change differently than the VCO's constant velocity output, thus resulting in a tracking error. With a noisy input, the constant velocity offset when the switch opens may be due all or in part to noise. Since the effect of noise at the opening of the switch persists as a function of time during the entire off period (i. e. , when there is no new input noise), the noise in the loop is non-stationary. Furthermore, the gated nature of the loop makes it difficult to apply the usual linear analysis techniques. Consequently, the loop performance is most expediently determined by computer simulation.
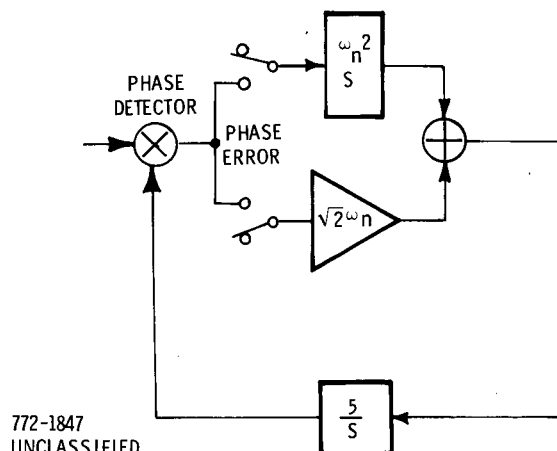
Figure A-1. Model of Gated 2nd Order Phase Lock Loop

A-1

Computer Simulation

The computer simulation is straightforward, wherein the 1/S of the loop filter and VCO is simulated by means of a shift register and adder. The loop non-linearity is simply the sin ( ) function, and the input to the loop filter (including additive white Gaussian noise) is turned on and off according to the gating function shown in figure A-2. Since the computer simulation essentially results in a sampled data system, it is important that the simulation sampling rate be high enough to accurately represent the gated loop, and consequently, a simulation sampling rate of 1000 samples per second is used. The effects of noise are simulated by adding appropriately scaled samples of white Gaussian noise to the phase detector output from a random number generator. The mean-square tracking error for a given time position is then determined by squaring and summing over 40 such time positions and dividing by 40.

Simulation Results

In order to assess the basic stability of the gated loop, the response to a step in phase was first determined. This test, along with all the following tests utilized the gating waveform shown in figure A-2 and an undamped natural loop resonant frequency (as defined by the continuous loop analog) of $f_n = 6\,Hz$. The response to the step in phase input resulted in approximately 500 percent more over-shoot than would have occurred with a continuous loop of the same f_n. This indicates a severely under damped loop (the damping was set at $\zeta = 0.707$ in terms of the con-tinuous analog). However, the loop with the specified parameters is stable, since the error eventually decayed to a negligible value.
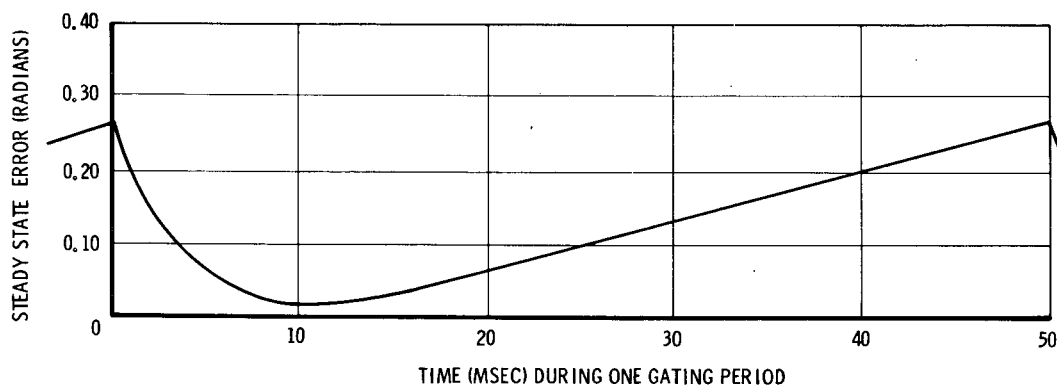
Figure A-2. Steady State Error with Velocity Ramp Input $(\dot{\omega}/\omega_n^2 = 0.1)$

A-2

The steady state error response of the gated loop to a ramp in velocity (acceleration or parabolic phase) is shown in figure A-2. The slope of the ramp was chosen such that a continuous loop with the same f_n would have a 0.1 radian steady state error. During the on burst, the error is driven down to approximately 0.02 radians. This is reasonable since during the burst, the loop gain is set to be five times the loop gain of the continuous loop. As can be see, when the loop is off, the error error builds linearly to a peak which occurs just before the burst comes on again.

The noise performance of the loop was determined by Monte Carlo simulation. The rms tracking error due to noise is shown plotted in figure A-3 as a function of peak C/N_o. Actually, three types of rms errors are plotted in figure A-3. First, there is the peak rms error, which occurs at the start of the on burst. Second, there is the rms value of the rms errors, averaged over the entire gating period. This is better understood by observing the variation of the actual rms error over the gating period. The variation of the rms error over the gating period is due to the non-stationarity of the loop noise, as discussed previously. Third, the rms error for a continuous loop is also plotted for comparison purposes. The continuous loop
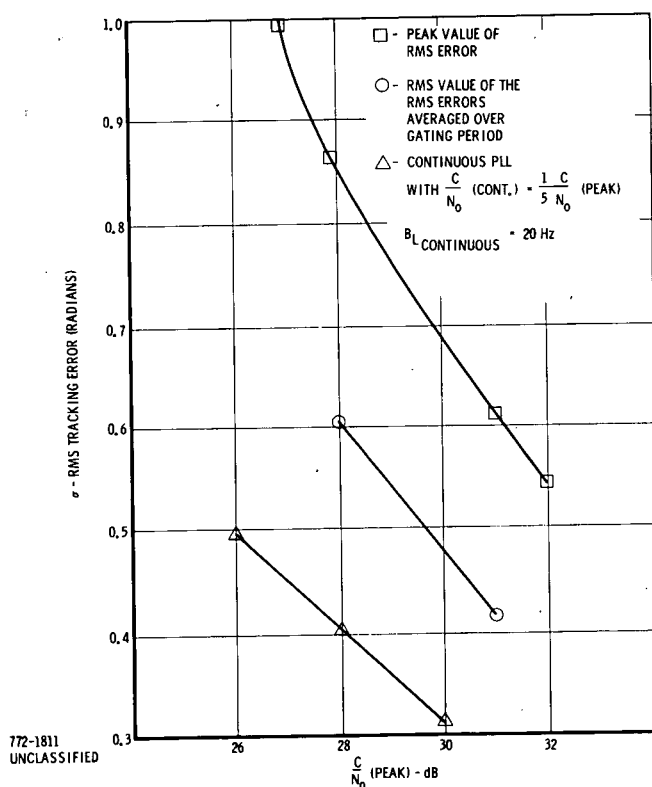

Figure A-3. Loop Error as a Function of $\dfrac{C}{N_0}$ (Peak)

A-3

error is plotted for an average C/N_O which is equal to 1/5 the peak C/N_O. This is due to the 1/5 duty cycle of the gating period.

Comparison of the curves in figure A-3 shows that, based on the rms values, the gated loop has a noise bandwidth approximately twice that of the continuous loop. Furthermore, the threshold for the gated loop appears to be at about 27 or 28 dB peak C/N_O. In terms of a continuous loop noise bandwidth, this represents a peak loop signal to noise ratio of 14 or 15 dB at threshold. If we consider the average C/N_O, and the fact that the noise bandwidth appears to be twice the hoped for value, a loop signal to noise ratio of 4 or 5 dB exists at threshold. This is consistent with established phase lock loop threshold performance. However, it is important to note that if this gated loop is to be evaluated under circumstances where a loop cycle slip carries a large penalty, i. e. , demodulation of data at low bit error rates or precision measurement of velocity from carrier doppler, the peak rms error curve is the important curve to consider.
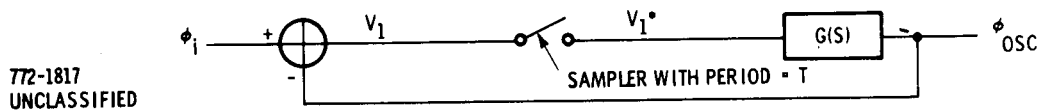
APPENDIX B

SAMPLED PHASE LOCKED LOOP CALCULATIONS

In this report, the classical second order PLL equations are examined to determine the criteria for stability of a sampled phase locked loop.

772-1816
UNCLASSIFIED

This is equivalent to:

772-1817
UNCLASSIFIED
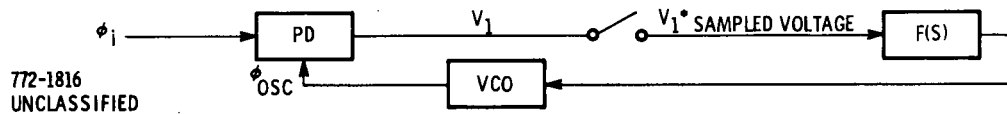
where $G(s) = K_{pd} K_{osc} \left(\frac{1}{s}\right) \left(1 + \frac{a}{s}\right) = \dfrac{Ks + Ka}{s^2}$

$V_1 = \phi_i - \phi_{osc} = \phi_i - G(s) V_1^*$ therefore $V_1^* = (\phi_i - G(s)V_1^*)^* = \phi_i^* - G^*(s) V_1^*$

or $V_1^* [1 + G^*(s)] = \phi_i^*$. Output $= \phi_{osc} = G(s) V_1^* = \dfrac{G(s)\, \phi_i^*}{1 + G^*(s)}$, it follows that:

$$\dfrac{\phi_{osc}}{\phi_i^*} = \dfrac{G(s)}{1 + G^*(s)}$$

If G(s) is stable, the stability of the closed-loop system depends exclusively on $1 + G^*(s)$, or $1 + G(z)$

$G(s) = \dfrac{K}{s} + \dfrac{Ka}{s^2}$, it follows that $G(z) = \dfrac{Kz}{z-1} + \dfrac{KaTz}{(z-1)^2}$

Therefore: $1 + G(z) = \dfrac{Kz}{z-1} + \dfrac{KaTz}{(z-1)^2} = \dfrac{(z-1)^2 + Kz(z-1) + KaTz}{(z-1)^2}$

Let $N(z) = $ numerator of $[1 + G(z)] = (1+K)z^2 + [KaT - K - 2]z + 1$

Write as:

$$N(z) = z^2 + \dfrac{[KaT - K - 2]}{1+K} z + \dfrac{1}{1+K}$$

Reference to Truxal[*] yields the following conditions for stability:

$|N(0)| < 1, \quad N(1) > 0, \quad N(-1) > 0$

$|N(0)| = \left|\dfrac{1}{1+K}\right| < 1 \quad$ O. K.

$N(1) = 1 + \dfrac{KaT - K - 2}{1+K} + \dfrac{1}{1+K} = \dfrac{KaT}{1+Ka} > 0 \quad$ O. K.

$N(-1) = 1 - \dfrac{KaT - K - 2}{1+K} + \dfrac{1}{1+K} = \dfrac{4 + 2K - KaT}{1+Ka} > 0$

Therefore, the condition for stability is:

$(4 + 2K - KaT) > 0$

[*]J. G. Truxal, "Control System Synthesis", Mc-Graw Hill Book Co., New York, 1955.

For a PLL with $\zeta = 0.707$,

$K = \sqrt{2} \; \omega_n$ and $a = \omega_n/\sqrt{2}$

The condition for stability becomes:

$$4 + 2\sqrt{2} \; \omega_n - \omega_n^2 \; T > 0$$

or $T < \dfrac{4 + 2\sqrt{2} \; \omega_n}{\omega_n^2}$

This can also be written as: $f_s = \dfrac{1}{T} > \dfrac{\omega_n^2}{4 + 2\sqrt{2} \; \omega_n}$

If $\omega_n = 10\pi$, the PLL will be stable if $f_s > 10.6$ Hz.

APPENDIX C

SIGNAL TO NOISE POWER BUDGET ANALYSIS

In general, the link from the ground to TDRS and back can be considered to be an essentially noise free link in the sense that multipath and RFI are minimized by ground antenna directivity; also high-ground transmitter power, antenna gain, and sensitive receivers promote good signal-to-noise ratios on this link.

The weak component in the user/TDRS/ground system is the/user/TDRS path. This link is characterized by low power, low-gain antennas, high RFI, and high multipath interference. These problems serve to degrade the signal-to-noise ratio (SNR) at the User or TDRS.

The following analysis will discuss the salient features of this link and as such provides the information necessary to calculate the margin available in the overall communications system.

1)   <u>TDRS Received Power</u>

The EIRP of TDRS will be approximately 63 dB. This value will be considered in the final calculations.

For the User the value of EIRP is

$$37 \text{ dBm} - L_{line} + G_t = 33 \text{ dBm}$$

(-1 dB line loss, -3 dB antenna gain)

The values of λ for the forward and return link are given below. The parenthetical numbers are the frequencies in megahertz.

2. 35(127.750), 2(149), 0.75(401) : Forward Link

2. 19(137)   : Return Link

The gain G_r is -3 dB worst case for the user and 12 dB for TDRS.

The polarization loss is 0 dB since polarization diversity is used.

The VSWR loss should be negligible relative to other factors and so will be considered to be 0 dB.

The minimum and maximum slant range are a function of satellite altitude. The values for 300-KM and 5000-KM heights are

35700 KM : 300 KM (min)

43500 KM : 300 KM (max)

31000 KM : 5000 KM (min)

50800 KM : 5000 KM (max)

Using the above data with the predetection signal power equation gives a budget of User and TDRS received power.

USER TO TDRS RECEIVED POWER (In dBm)*

λ	0.75	2.0	2.19	2.35	Orbit (slant range)
	-131	-122	-121	-121	300 KM (min)
	-133	-124	-123	-123	300 KM (max)
	-130	-121	-120	-120	5000 KM (min)
	-134	-125	-124	-124	5000 KM (max)

TDRS TO USER RECEIVED POWER (dBm)

λ	0.75	2.0	2.19	2.35	Orbit (slant range)
	-124	-115	-114	-114	300 KM (min)
	-126	-117	-116	-116	300 KM (max)
	-123	-114	-113	-113	5000 KM (min)
	-127	-118	-117	-117	5000 KM (max)

*-1 dB line loss, -3 dB user gain, 12 dB TDRS gain

2)   Galactic Noise Temperature

λ	0. 75	2. 0	2. 19	2. 35	
°K	30	450	550	650	Galactic Pole
°K	40	600	750	850	Galactic Center

3)   RFI Noise Temperature

The values of T_{RFI}* range from 10^5 °K to 10^7 °K; hence T_{RFI} has the following values. $(G_r = 0 \text{ dB})$*

$$5.89 \times 10^4 \text{ °K} : 5000 \text{ KM, low RFI}$$
$$5.89 \times 10^6 \text{ °K} : 5000 \text{ KM, high RFI}$$
$$17.14 \times 10^5 \text{ °K} : 300 \text{ KM, low RFI}$$
$$17.14 \times 10^7 \text{ °K} : 300 \text{ KM, high RFI}$$

As can be suspected from the above results RFI is a dominant factor in the system temperature.

4)   Trash Noise Temperature

Using a value of 10^{-17} watts/m^2-Hz per the Lincoln Lab report and r = 400 KM for the radius, an area such as a New York centered east coast "equivalent" urban area, and r = 100 KM as a more isolated (Chicago) urban area, the trash noise temperature is

Urban Radius (KM)	100	400	
			Orbit (KM)
	7600°K	76000°K	300
	30°K	486°K	5000
	negligible	negligible	36000

*The average case of 0 dB gain was used due to the broad RFI source.

5)   Multipath Noise Temperature

The multipath temperature will be developed for each of the three modes.

a)   PSK Mode

In the PSK mode the system is channelized, i.e., each user will have a frequency slot assigned to him. The only multipath source, then, is the user on the downlink and TDRS on the uplink. The worst case occurs at the lowest orbit (least path loss for multipath) and when the user is directly beneath TDRS (most diffuse power). The temperatures below were calculated using parameter values of 50 KHz bandwidth, 300 KM orbital altitude,[*] and 3 dB antenna gain (worst case multipath is received on a pattern peak· recall the direct path was calculated based on a pattern null hence an overall factor of 6 dB).

$$25,200°K \; : \; \text{TDRS to User,} \quad F=127.750 \text{ MHz}$$
$$2520°K \; : \; \text{TDRS to User,} \quad F=401 \text{ MHz}$$
$$5040°K \; : \; \text{User to TDRS,} \quad F=127.750 \text{ MHz}$$
$$504°K \; : \; \text{User to TDRS,} \quad F=401 \text{ MHz}$$

An illustrative calculation of one of the above is

$$T_m = (-114) - (-198.6) - 47 + 6 + 20 \log 357 - 20 \log 366$$
$$= 44 \text{ dB °K} \Rightarrow 25,200°K,$$

where P_r = -114 dBm, K = 198.6 dBm/°K-Hz, B = 47 dB (Hz)
$$= 10 \log 5 \times 10^4 \text{ Hz.}$$

b)   PN Mode

Multipath temperature in the PN mode is different, in general, from that of the PSK mode due to two factors. First, the BW is larger in most cases, and second, the system is not channelized. The larger BW manifests itself in a lower

---

[*]300 KM implies a factor of $(35,700 \div 36,600)^2$ in multipath to direct power which is negligible.

temperature, however, the nonchannelized system allows other users (up to 19) to create multipath power which can fall in band which raises it.

Now since the other users will most probably be at varying distances from the user of interest, and since the path lengths involved will be larger, an exact calculation would require considerable knowledge of orbits, etc. In lieu of this knowledge a worst case of 20 users will be assumed to be, relatively speaking, beneath TDRS with a mean altitude of 300 KM.

The multipath temperatures for bandwidths of 50 KHz uplink (narrowband PN) and 1.0 MHz downlink do not change appreciably from the PSK mode. This is because the uplink is channelized and there is no change in BW, while the downlink sees 20 times more users, but 30 times less temperature due to the increased BW (this is a factor of 2/3 which is negligible under the kind of assumptions made in this analysis, i.e., only orders of magnitude are significant).

c)   ABC Mode

In the ABC mode there is no multipath receiver response hence the value of T_m is

$0°K$: for all regions within the zone of coverage.

6)   User Interference

On the downlink in the PN mode there is the possibility of increased system temperature due to the presence of other users accessing TDRS. Since this power is not directly of use to the channel of interest (it is clutter) it merely serves to degrade the SNR. This user interference temperature will be worst case when the clutter sources are at a short-slant range relative to TDRS.

For the calculation of user interference temperature, 20 users will be assumed to be beneath TDRS at a mean altitude of 1000 KM. At this range (35000 KM) the space loss is roughly -165 dB, hence

$$T_u = 33 - 165 + 6 + 10 \log 19 - (-98.6) + 12$$
$$- 10 \log 1.5 \times 10^6 = 36 \text{ dB°K} \Rightarrow 4000°K,$$

C-5

where $P_t = 33 + 6$ dBm, $G_r = 12$, BW $= 1.5 \times 10^6$.

7) ## System Noise Temperature

A calculation of the predetection signal to noise density will now be performed. Consideration of the temperatures contributing to the overall system temperature yields the following results.

a) ### TDRS TO USER

Only T_{RFI} is significant hence the worst case is 300 KM (max), high RFI

$$\left(\frac{\eta}{C_p}\right) = -126 \text{ dBm} + 198.6 \frac{\text{dBm}}{\text{Hz-}^\circ\text{K}} - 82.3 \text{ dB}^\circ\text{K}$$

$$= -9.7 \text{ dB-Hz} (-1.7 \text{ dB-Hz})^* \qquad (K)$$

b) ### USER TO TDRS

Again only T_{RFI} is significant

$$\left(\frac{\eta}{C_p}\right)_{dB} = -133 \text{ dBm} + 198.6 \frac{\text{dBm}}{\text{Hz-}^\circ\text{K}} - 70 \text{ dB}^\circ\text{K}$$

$$= -4.4 \text{ dB-Hz}$$

8) ## Processing Gain

Consider the processing gains available for each mode.

a) ### PSK Mode

In the PSK mode the only gain available is due to any coding involved. This is at best about 6 dB. Assume coding is used, then the best margin available is for the lowest bit rate (100 bps).

---

*8 dB gain due to present TDRS design information.

$$\frac{E_b}{N_o} = -9.7 \text{ dB-Hz} + 6 \text{ dB} - 10 \log 10^2 \text{Hz}$$

$$= 23.7 \text{ dB } (-15.7 \text{ dB}^*) \text{ (uplink)}$$

This is insufficient for the error rates desired, and higher bit rates only degrade this value.

b) PN Mode

In the PN mode the processing gain available is at 100 bps.

$$C_p = 34000 \text{ chips/sec} \div 100 \text{ bps} \Rightarrow 25.3 \text{ dB}$$

$$\frac{E_b}{N_o} = 4.4 \text{ dB } (3.6 \text{ dB}^*) \text{ (uplink, 100 bps)}$$

This is insufficient. If 6 dB coding gain is also used

$$\frac{E_b}{N_o} = 1.6 \text{ dB } (9.6 \text{ dB}^*) \text{ (uplink)}$$

This is sufficient for the moderate error rates if the 8 dB present TDRS design differential is used, however, higher bit rates degrade this value further so that the link is unusable at, say, 1 Kbps.

c) ABC Mode

The ABC mode is equivalent to the PSK mode when $T_m << T_s$ as in the cases previously considered.

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*See comment on equation (K)

9) CONCLUSIONS

In the case of high RFI the SNR is not sufficient in the PSK or ABC cases. In the PN case where all the power is dedicated to the data (no voice) the SNR is at best marginal. If the RFI can be eliminated, the next dominant temperature is trash noise for low orbit satellites. This temperature is 30 dB lower and can be tolerated as seen by the following analysis in the PN mode. (T_m is still not high enough to make the ABC mode advantageous).

In this case with minimum direct signal (maximum slant range, TDRS to User), maximum trash temperature, and bit rate of 100 bps).

$$\frac{E_b}{N_o} = -126 \text{ dBm} + 198.6 \frac{\text{dBm}}{\text{Hz-}^\circ\text{K}} - 48.8 \text{ dB}^\circ\text{K} - 20 \text{ dB Hz}$$

$$+ 10 \log \frac{34000}{100} = 29 \text{ dB } (37 \text{ dB})^*$$

If coding is used the margin is even higher.

The general conclusion is to study the RFI problem to an extent where the RFI temperature can be known very accurately (experimental satellites, etc.) and then use of PN mode with as high a chip rate as can be tolerated.

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*See comment on equation (K)

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APPENDIX D

CONVOLUTIONAL ENCODER FOR THE MULTIMODE TRANSPONDER

D.1   CODING AND COMMUNICATION

Error correction coding has been used successfully on satellite communication links to obtain a given probability of error at a saving in the required energy per information bit to noise spectral density (E_b/No). A saving in power in the return link of 4 to 5dB can be achieved if the channel is disturbed only by Gaussian noise. This is not the only disturbance possible in the TDRS system. Severe multipath and RFI interference will serve to reduce system performance. This latter data outage problem can result in a loss of data. It is toward this last problem that error correction coding will be applied.

The coding problem is to determine a set of rules whereby any information sequence $\bar{x}$ can be transformed into some longer output sequence $\bar{s}$ such that the GSFC decoder can uniquely and with arbitrarily high probability redetermine the $\bar{x}$ in spite of binary symmetric channel perturbations. The binary symmetric channel has a transition probability $q_o > 1/2$ that the binary digit is received correctly, and $p_o = 1 - q_o < 1/2$ that it is received incorrectly. For a binary symmetric channel, it is convenient to measure the information rate per transmitted digit which is defined as the ratio:

$$R = \frac{\text{number of digits in } \bar{x}}{\text{number of digits in } \bar{s}}$$

By means of proper coding in a binary symmetric Gaussian channel, communication can be made as reliable as desired provided that the transmission rate R is less than the channel capacity C, which is defined by the expression:

$$C = 1 - H(P_o)$$

where $H(P_o) = P_o \log_2 P_o - q_o \log_2 q_o$. Achievement of a low probability of error at a specific E_b/No becomes an increasing difficult task for communication systems which are distrubed by multipath and RFI interference, because of the channel

discontinuities which exist. This deviation from the continuous Gaussian channel results in error bursts which cause decoder input buffer overflow and loss of incoming data.

D.2   ERROR CORRECTING CODES

The idea of error correcting codes is far more appealing than mere error detection. The impact of forward error control in terms of increased user complexity is minimal, because, in all cases, the encoding device required is extremely simple. The device consists of shift registers and modulo-2 adders. The bulk of the complexity is in the decoder found at the ground station where increased complexity can be tolerated. Ideally an error-control-code should combine reliability, efficiency, simple implementation, and invulnerability to error bursts. Not surprisingly, no known code entirely satisfies this tall order. However, there are several codes of practical interest that combine two or three of these properties.

The number of digits in which two binary words of the same length are different is called the distance or Hamming distance. Hamming proposed a systematic method of adding check digits to a message sequence such that, upon receipt, an error word can be formed to spell out the single-error correction. Consider a binary word of M + C message and check digits with at most one error. Error correction by Hamming's method then requires M + C + 1 possible error words, namely, "no error", "first digit in error", "second digit in error", and so forth. Since only the C check digits can be used to generate the error word and, since there are 2^C combinations, the expression $2^C \geqslant M + C + 1$ must be satisfied. Full utilization of the Hamming Code requires the equality to be realized, thereby restricting word length to $2^n - 1$ where N = C. Going to longer word lengths improves efficiency but increases the chances of multiple errors. Numerous variations on the basic Hamming Code are possible, of course; the check digits can be interlaced, and the code can be expanded for multiple-error correction. However, the amount of hardware rapidly gets out of hand and nullifies the inherent simplicity of Hamming's procedure.

Cyclic codes are block codes in that a specific number of successive message digits are grouped together. The check digits are arranged such that a shift register with feedback can do the encoding. For the input message 011, the output word will be 0111001. The register is then cleared and three new message

digits are inserted. It can be shown that the (7, 3) cyclic code has distance 4 and therefore is a single-error-correcting, double-error-detecting. The encoding and decoding equipment is relatively simple, and reliability is high, but the efficiency is less than 50 percent (α = 3/7), and error bursts give problems.

A type of cyclic code having greater reliability is the Bose-Chaudhuri Code. With word length $2^n - 1$ and nk check digits this code can correct k errors or detect (but not correct) 2k errors. In either mode the efficiency factor is $\alpha = \frac{(2^n - 1 - nk)}{(2^n - 1)}$. Many error patters having more than 2k errors are also detected, so the code is reasonably invulnerable to error bursts. Encoding is done by a shift register of nk stages, and error detection decoding is achieved by an identical shift register plus peripheral devices. However, error correction is more complicated and entails equipment tantamount to a small computer.

Recurrent codes, unlike all types discussed so far, do not divide the message digits into blocks but rather have a continuous encoding-decoding procedure. This eliminates the need for storage or buffering at the data terminals, thereby reducing equipment requirements. Usually, recurrent codes are designed for error-burst correction, in which capacity they have widespread interlacing and high redundancy. For example, a Hagelbarger Code with one check digit per message digit (α = 1/2) can correct up to six successive errors if the preceding 19 digits are correct. Encoding and decoding are accomplished by simple shift registers. The code therefore is well suited to applications where error bursts are the main concern, terminal equipment must be minimized, and the bit-rate reduction can be tolerated.

Random sequential codes such as convolutional tree codes can be regarded as a form of recurrent coding. At very low rates, such codes offer good error-correcting ability and will be discussed in detail in the following section.

D.3   CONVOLUTIONAL ENCODER

A convolutional encoder accepts an input sequence $\bar{x}$ of K equally - likely, statistically independent binary digits. With convolutional codes, each digit of an output transmitted sequence is a function of the preceding K encoder inputs digits. In order to illustrate the basic concepts of a convolutional encoder, a three stage encoder (constraint length of three), will be considered. The code rate in this

case is 1/2, since for every input data digit two code digits are read out. Successive input digits from an infinite stream enter the shift register at regular time intervals and shift down until they are discarded K time intervals later. If the register is initially loaded with all zeroes and the sequence 010111 is shifted in, the sequence at the output of the serial to parallel converter is 00 11 10 00 01 10. By convention these digits are written in order of increasing time and thus the oldest digit is shown on the left.

A convolutional encoder can be viewed as a linear filter from the circuit theory point of view. The impulse response of the encoder is obtained by shifting the sequence $x(t) = 10000...$ in to give the impulse response $h(t) = 11$ $10\ 11\ 00\ 00\ ...$ The output sequence can be written as the modulo - 2 convolutional summation given by $y(t) = \sum_{\tau} x(\tau) \cdot h(t - \tau)$ where the summation τ represents discrete increments at the data rate. For an input sequence $x(t)$, the equation for digital convolution can be written as: $y(nt) = \sum_{m=0}^{n} X(mt) h(nt - mt)$ where

$y(T) = X(0) h(T) + X(T) h(0)$, and

$y(2T) = X(0) h(2T) + X(T) h(T) + X(2T) h(0)$, and

$y(3T) = X(0) h(3T) + X(T) h(2T) + X(2T) h(T) + X(3T) h(0)$,

etc.

The choice of connections into the modulo-2 summers determines the choice of a particular code that may be systematic or nonsystematic. In the former, only the first stage (most recent data bit) is connected to one of the modulo-2 summers. In the latter, both modulo-2 summers have a multiple stage connection. The specific code structure for the encoder is; parity generator $G_1 = 111$ and parity generator $G_2 = 1\ 0\ 1$ where a 1 in the n^{th} digit of parity generator G_1 or G_2 is taken to mean that the connection is made to the n^{th} stage of the shift register, and a zero that the connection is not made. Since there are two modulo-2 summers which have multiple stage connections, the code chosen is nonsystematic and will generate two parity digits for each input digits. If a systematic code had been chosen, G_2 would be as shown, but G_1 would be 100 instead of 111, and the G_1 modulo-2 summer would not be needed since there is only one connection to the first stage of the shift register. The systematic code will generate an input digit (since $G_1 = 100$) followed by a parity (or check) digit determined by G_2.

One approach for determining the transmitted sequence at the receiving terminal is to find the path through the tree which is most likely, i.e., the path which has the highhest probability of being actually transmitted, given the received sequence. Unfortunately, as the length of the sequence increases the exponential growth of the number of possible paths becomes too large for the implementation of a practical decoder. However, the tree structure is generated by an encoder of a finite number of stages, three in this case, which results in certain repetitions in portions of the structure. For example, examination of the tree at a depth of 3, i.e., after the first three information digits are encoded, there are eight nodes which are possible. The tree structure leaving node 1 must be identical to that leaving node 5, with a similar relationship holding for nodes 2 and 6, 3 and 7, and 4 and 8. This pairwise identity in the tree structure results because after the third information digit is encoded, the first information digit cannot influence the values of future tree branches.

Decoding can be considered simplified by taking advantage of the pairwise relationships noted above. For example, if node 1 is more like than node 5, i.e., the information sequence 000 is more likely than the information sequence 100, the branches leaving node 5 no longer have to be considered. For any given sequence leaving node 5, the same sequence leaving node 1 will always be more likely. Thus, at a depth of three, only four of the eight possible information sequences need to be saved. Similarly, at a depth of four, there are again eight possible sequences resulting from the four nodes which were saved at a depth of three. Again, only four of these sequences must be saved. Thus, by sequentially making pairwise comparisons of the likelihood of appropriate sequences, an optimum decoder can be built which only has to save four possible sequences. In theory the length of these sequences must grow with the input data, but in practice bit decisions can be made after an appropriate delay.

The construction of convolutional code generators which provide good distance property (or large error-correcting ability) involves maximizing the minimum Hamming distance between different code words. References are available which provide a step by step method of constructing code generators up to 12 segments by hand. For more than 12 segments the labor will be tedious, and

computer searching is thus needed. Good generator codes have also been found by experimental techniques. With combined sequential decoding and Costas loop tracking in a receiver, it is necessary that the convolutional code generators be transparent, otherwise the decoder will look into an extremely noisy channel when the Costas loop flips phase. A convolutional code is transparent if the complement of the data into the encoder yields the complement of the data out of the decoder. This transparency requirement will be satisfied if each parity generator has an odd number of 1s. A nonsystematic code will generally produce a better error probability than an equal constraint length systematic code because it gives a better hamming distance. For example, a 24 bit constraint length nonsystematic encoder would produce about twice as good error probability than a 48 bit systematic encoder. Also, in general, the larger the constraint length of a systematic or nonsystematic encoder, the better will be the error probability.

D.4   SEQUENTIAL DECODER

Sequential decoding has provided a good technique of achieving digital communications over noisy channels at low-error probabilities. A sequential decoder incorporates a replica of the convolutional encoder, and operates by attempting to trace a path through the convolutional tree which yields an hypothesized transmission $\overline{s}$ that is a "close" approximation to the received sequence $\overline{r}$ consisting of n digits. By "close" it is meant that $\overline{s}$ and $\overline{r}$ should not differ in a number of digits that is a typical of the channel disturbance. The quantity the measures the closeness of fit is the metric Λ which is computed over the n symbols of a branch, and and is additive over the hypothesized sequence of branches. The metric computed for the branch is:

$$\Lambda = \sum_{\substack{j=1 \\ j=1}}^{\eta} \left[\text{LOG}_2 \ \frac{P\left(r_J/S_J\right)_-}{\omega\left(r_j\right)} \ - U \right]$$

where $\omega(r_j)$ is the (absolute) probability of r_j and U is an arbitrary bias usually set approximately equal to the code rate R. Since r is quantized (Q bits) symmetrically, there are 2^{nq} metric values given by the above equation; these can be precomputed and stored in a table for subsequent look-up.

The decoder functionally comprises data and backup buffers, a duplicate encoder, the metric look up table, and the branch computation logic. The size of the

buffer determines the extent to which decoding can fall behind before overflow occurs. The encoder and backup buffer together form the hypothesis memory. The size of the backup buffer determines the depth to which a path may be retraced in an effort to find a more suitable hypothesis. Each branch computation is in accordance with the Fano algorithm logic used to direct the search through the tree; this includes a metric table look up, the proper addition to form the new value Λ, and sensing the behavior of the metric along a given path by crossings of equally spaced thresholds.

The probability distribution of the number of computations N required to advance one node deeper into the code tree is one of the more fundamental characteristics of sequential decoding, since it determines the probability of overflow. The probability distribution of the random variable N has been bounded by upper and lower bounds of the form:

$$A_1 \left(\alpha, L \right) L^{-\alpha} < P \left(N \geq L \right) < A_2 \left(\alpha, L \right) L^{-\alpha}$$

where α is referred to as the Pareto exponent. The values of $A_1 (\alpha, L)$ and $A_2 (\alpha, L)$ change slowly with L and, hence, the dominant behavior is $L^{-\alpha}$. However, these bounds are very week and there is no proof that a fixed code can achieve the performance indicated by these bounds.

For a specified probability of overflow, the number of incoming nodes to be stored (data buffer size) is obtained from the computations distribution and speed advantage S denoting the number of forward or backward moves possible in a data bit time. It has been shown that for useful probabilities of overflow, the overflow is caused by occasional long searches initiated under the condition that the decoder has no waiting line. With this model of the overflow phenomenon, the probability of overflow is equal to P $(N \geq L)$ where L is the number of computations that can be performed during the time required to fill the data buffer. Then the number of incoming nodes to be stored, B, is given by:

$$B = L/S$$

For a given probability of reaching the limit of the backup buffer, the number of past hypotheses to be stored (backup buffer size) is similarly specified from the backup distribution, P (bm $\geq$ L). The random variable bm is the

maximum backup reached by the decoder before a path is found which allows the decoder to move forward to a new node deeper in the code tree. This backup distribution has been shown to be exponentially decreasing.

The statistics on the number of computations to advance to a node deeper into the code tree may be measured at each depth in the code tree by counting the number of moves backward and forward before the decoder advances to a new node deeper in the tree. To facilitate the evaluation of probability of error from observed distributions, the computations distributions are measured to a probability of 10^{-5} and modeled as Pareto distributions by making at least squares fit of the data on a log-log plot over the range of probabilities 10^{-3} to 10^{-5}. The slope α and intercept Ni at 10^{-5} of this least squares fit is measured. Using the measured parameters α and Ni, the probability of overflow with speed advantage S and forward buffer B is given by:

$$P_O = 10^{-5} \, (SB/Ni)^{-\alpha}$$

Since the backup buffer length can be made sufficiently long that the probability of backup buffer overflow is negligible in comparison, the total probability of error P_e now can be computed, assuming a negligible probability of undetected error. When using a systematic code, undecoded information bits can be output following an overflow; channel errors go uncorrected then between the decoding interrupt and the end of the synchromization block. Since overflow has probability P_O of occuring for each bit, the total probability of error per bit may be expressed as:

$$Pe = (0.5 + b/I) \, Po \, Pce$$

where on the average about one-half the bits in the resynchronization block I and the b bits in the backup buffer remain to be decoded when an overflow occurs. The equations of P_O and P_e show how to convert measured Pareto distribution parameters, α and Ni, into probability of error.

The decoder decodes one digit of information sequence $\bar{x}$ at a time. In order to decode the first digit, say x_1, it compares the subsequence $\bar{r}_1$ (consisting of the n digits of $\bar{r}$, beginning with x_1) with a hypothesized sequence $\bar{s}$, of the same length. The decoder constructs $\bar{s}_1$ locally, by entering some k-bit trial sequence $\bar{x}_1$ into its replica of the encoder: $\bar{s}_1$ is the resulting output sequence. If the agreement between $\bar{s}_1$ and $\bar{r}_1$ is sufficiently good according to some criterion (say K_j), the hypothesis x_1 (the first digit of $\bar{x}_1$) is accepted, i.e., X_1 is decoded. The remaining

k-1 branches of $\overline{s}$, ($\dfrac{k-1}{R}$ digits) are tentatively accepted and form the first k-1
branches of a new hypothesis $\overline{s}_2$ used to decode x_2. If the result of appending one
new branch to this hypothesis fails to satisfy the criterion K_j, then the hypothesis
(path through the tree) is systematically changed until either a satisfactory
hypothesis is found or the tree is exhausted. In the former case x_2 is decoded;
in the latter case, the entire procedure is repeated with a slightly more relaxed
criterion $k_j + 1$.

Whenever an initial hypothesis is almost correct, and the noise is con-
sistent with the transmission rate R, the decoding is rapid. An hypothesis with
several errors can lead to long searches. Sequential decoders can be designed
in such a way that the average amount of searching need grow only algebraically
(not exponentially) with the number of digits in the received sequence, provided
that no decoding errors have yet been made.