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ELECTRON-PROTON SPECTROMETER
DESIGN SUMMARY

LEC Document Number EPS- 522

Prepared by

Lockheed Electronics Company, Inc.
Houston Aerospace Systems Division
Houston, Texas

Under Contract NAS 9-11373

For

National Aeronautics and Space Administration
Manned Spacecraft Center
Houston, Texas
June 1972

(NASA-CR-128702) ELECTRON-PROTON SPECTROMETER DESIGN SUMMARY (Lockheed Electronics Co.) 147 p HC $9.50

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1. DESIGN REQUIREMENTS

The Electron-Proton Spectrometer (EPS) (Figure 1) will be placed aboard the Skylab in order to provide data from which electron and proton radiation dose can be determined. The EPS has five sensors, each consisting of a shielded silicon detector, as shown in Figure 2, these provide four integral electron channels and five integral proton channels from which can be deduced four differential proton increments.

Primary dose from high energy charged particles can be calculated utilizing the range energy relation for energy degradation; that is, a charged particle of kinetic energy E will have an energy E' after penetrating a shield with a thickness t. The relation between E and E' is given by

$$R(E') = R(E) - t$$

Where R(E) and R(E') are the ranges in the shield material of a particle with kinetic energies E and E', respectively. The energy deposited in a volume at the center point of a spherical shell of thickness t is the dose at that point and is given by

$$D(t) = 1.6 \times 10^{-8} \int_{0}^{\infty} \frac{dF}{dE'} \left(\frac{dE}{dx}\right)_{E'} dE'$$

Where $\frac{dF}{dE'}$ is the differential flux at that point, $\left(\frac{dE}{dx}\right)_{E'}$ is the stopping power for a particle with energy E' in the element of volume at the center point of the shield.

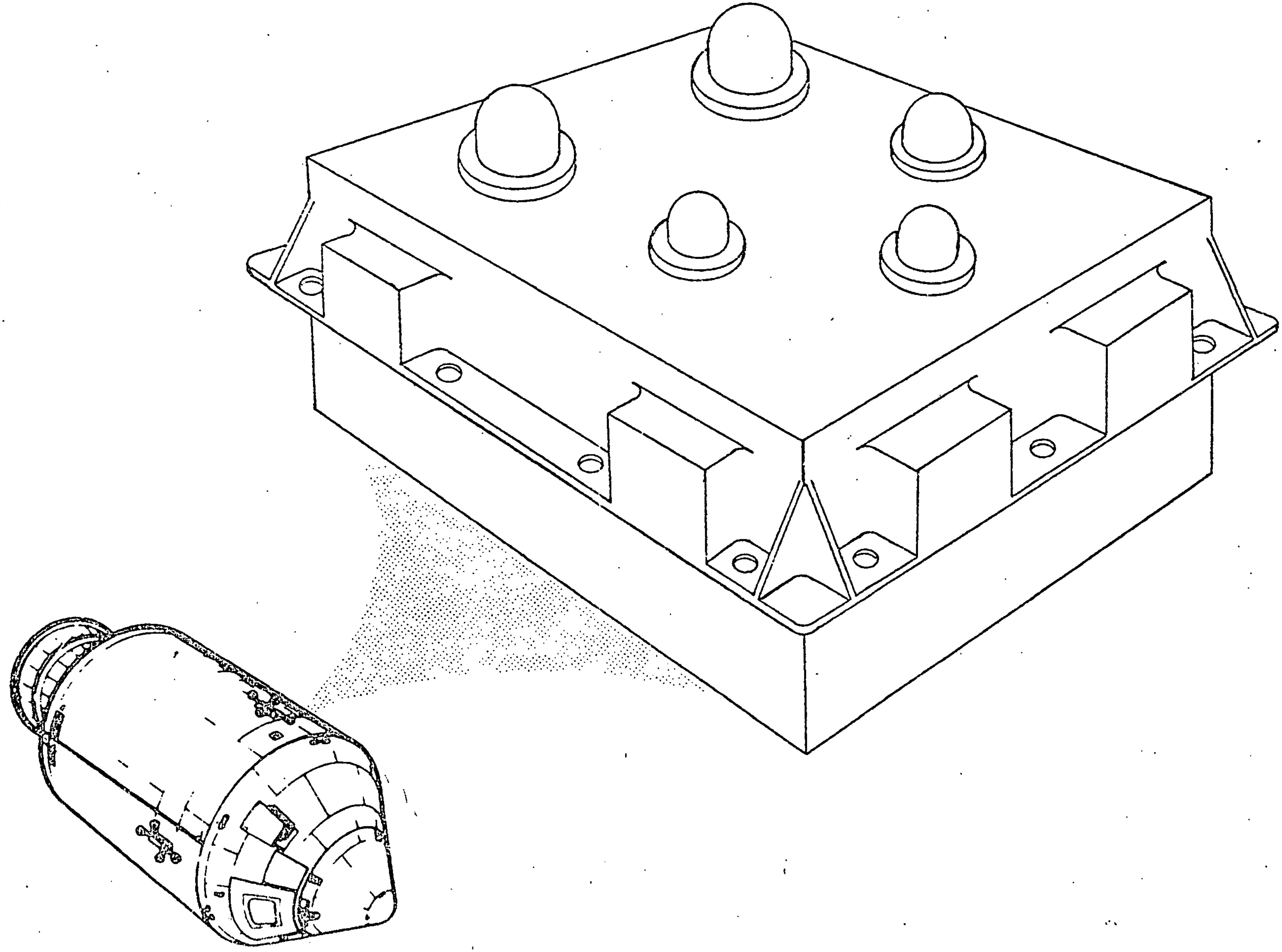

Figure 1. ELECTRON-PROTON SPECTROMETER

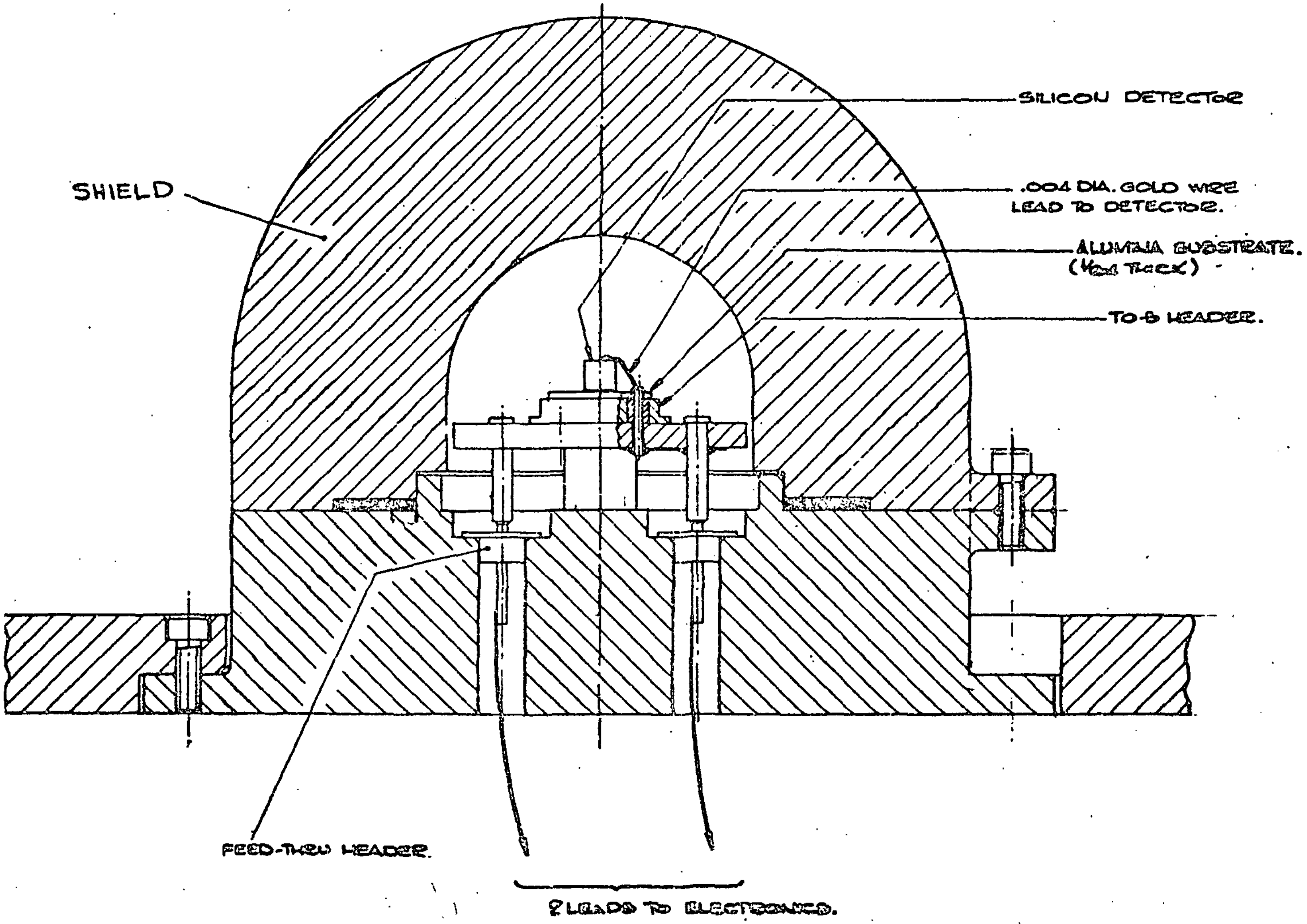

Figure 2. SHIELDED SILICON DETECTOR

All the particles in an energy interval dE about E are degraded to and contained in the energy interval dE' about E', so substituting

$$\frac{dF}{dE}\ dE = \frac{dF}{dE'}\ dE'$$

into the equation for dose gives

$$D(t) = 1.6 \times 10^{-8} \int_{R^{-1}(t)}^{\infty} \frac{dF}{dE} \left(\frac{dE}{dx}\right)_{R^{-1}\left[R\ (E)\ -t\right]} dE$$

where $R^{-1}(t)$ and $R^{-1}[R\ (E)\ -t]$ are inverse ranges corresponding to energies whose ranges are t and R(E) -t, respectively. Hence, it can be seen that determination of the radiation dose inside a shield can be accomplished with knowledge of the shield thickness and the differential spectrum, $\frac{dF}{dE}$, incident on the shield. In the case of the Skylab, the shield thickness comes from the description of the vehicle geometry and the differential spectrum of the incident particulate radiation will be provided by the EPS.

The anticipated differential proton spectrum at an orbit altitude of 235 nautical miles is shown in Figure 3 and can be represented by the sum of two expontials

$$\frac{dF}{dE} = 2.29 \times 10^{6}\ e^{-\frac{E}{4.88}} + 5.33 \times 10^{4}\ e^{-\frac{E}{58.75}}.$$

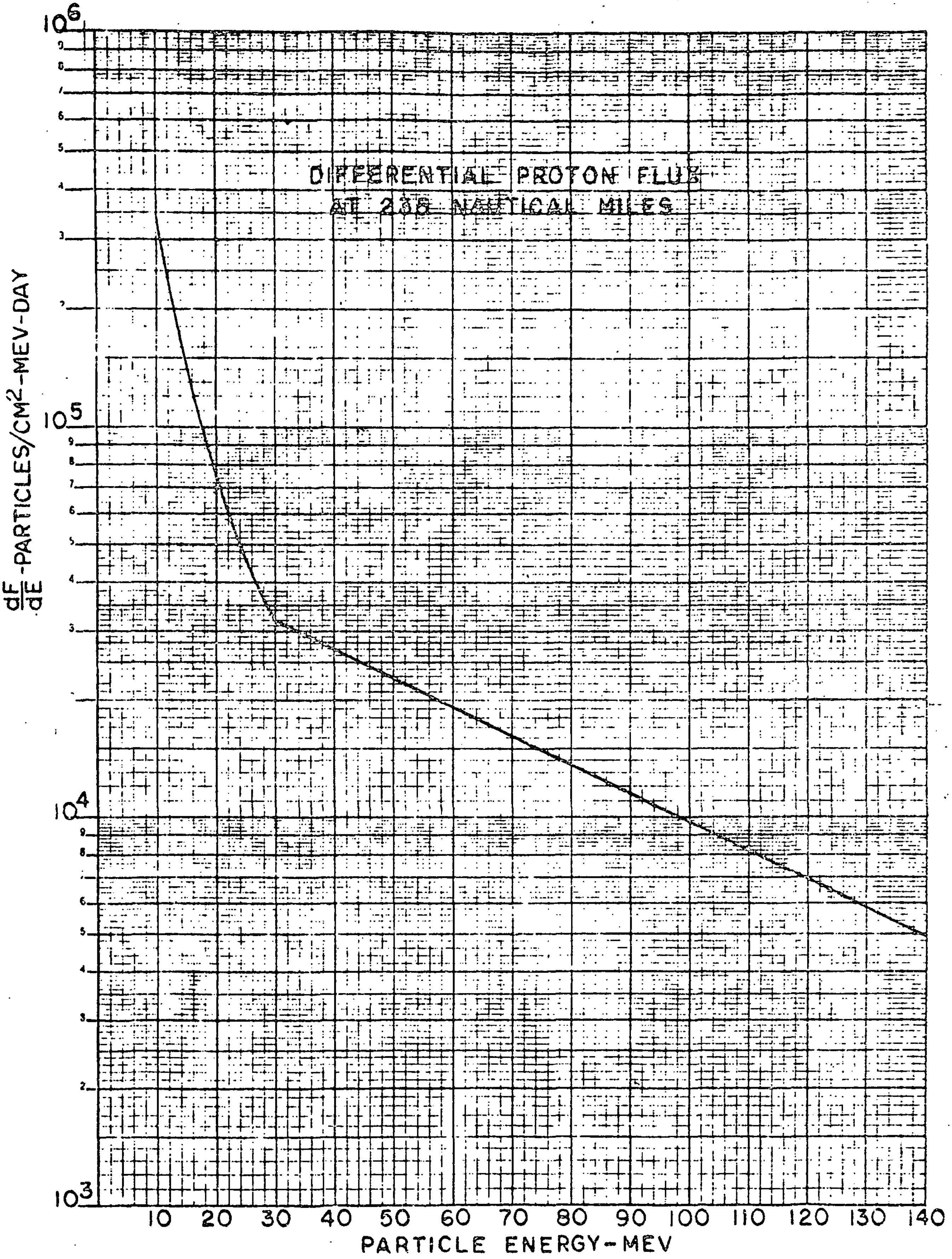

Figure 3. DIFFERENTIAL PROTON FLUX AT 235 NAUTICAL MILES

The anticipated differential electron spectrum at the orbit altitude of 235 nautical miles is shown in Figure 4. The EPS will be located on the Command-Service Module as shown in Figure 1 so as to permit a view of a proximately 2 π steradians.

The sensitive element of the EPS sensor is the silicon detector which consists of a cube of lithium-drifted silicon crystal, as shown in Figure 5. The detector is operated as a reverse-biased diode. The ionization created by the passage of an energetic charged particle through the sensitive volume of the detector is proportional to the energy lost by the particle and when collected and amplified provides a signal which is a measure of the energy deposited in the detector.

Detection of electrons in the desired energy range will be accomplished by means of a low level discriminator, 200 - 300 keV, on each of the first four detector channels. By virtue of the low level discrimination the electron measurements will be integral. Separation of the protons and electrons will be accomplished by the fact that only a negligible percentage of electrons can deposit enough energy to be counted in the proton channels. The electron channels must be corrected for the response to protons.

Electronics discriminator set at approximately 2 MeV will comprise the five integral proton channels. The proton flux in four differential energy increments is obtained by subtraction of the contents of energy-adjacent proton channels and the use of iterative procedures, if necessary.

The parameters pertinent to the five detector channels are given in Table I.

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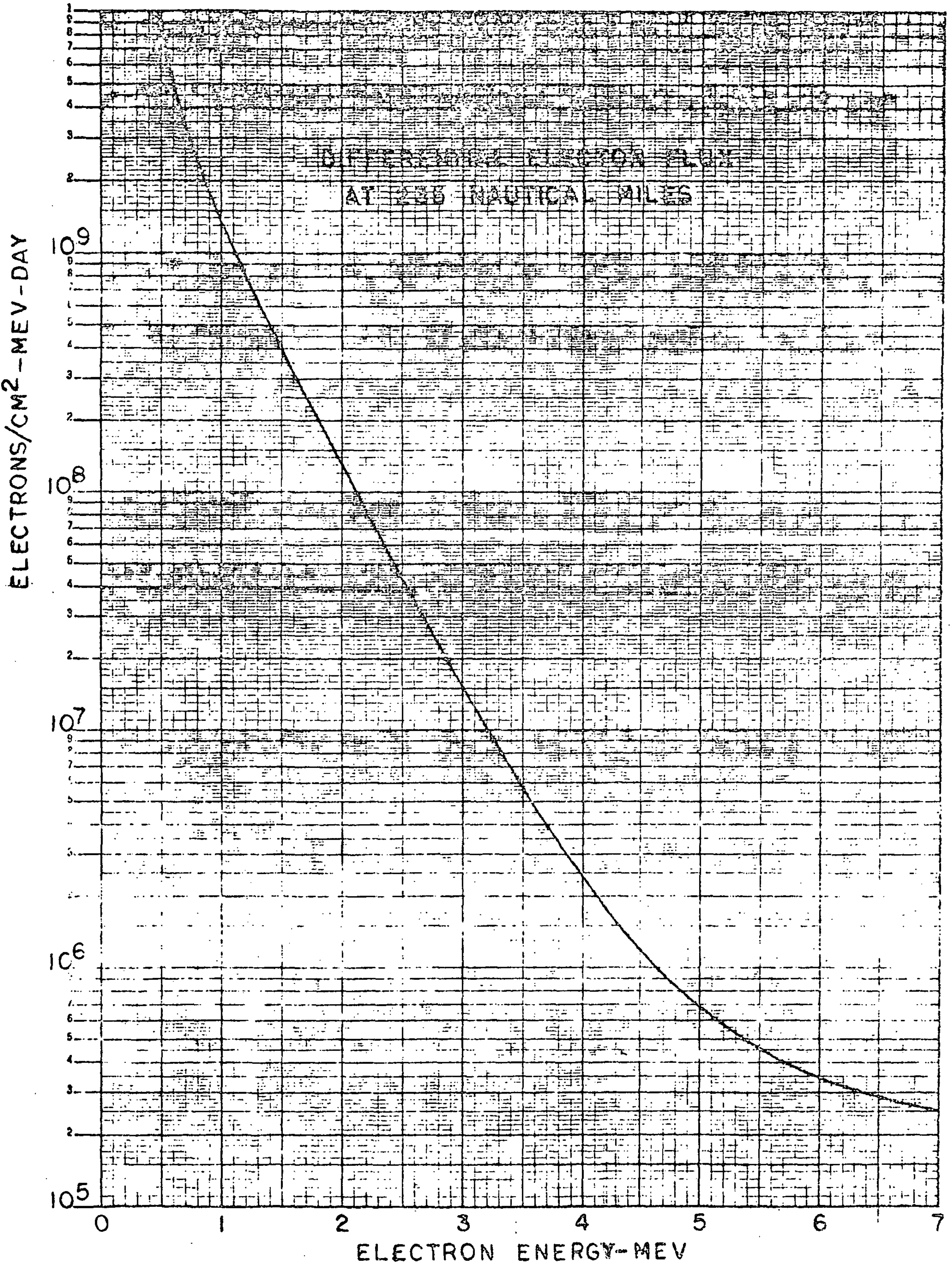


Figure 4. DIFFERENTIAL ELECTRON FLUX
AT 235 NAUTICAL MILES

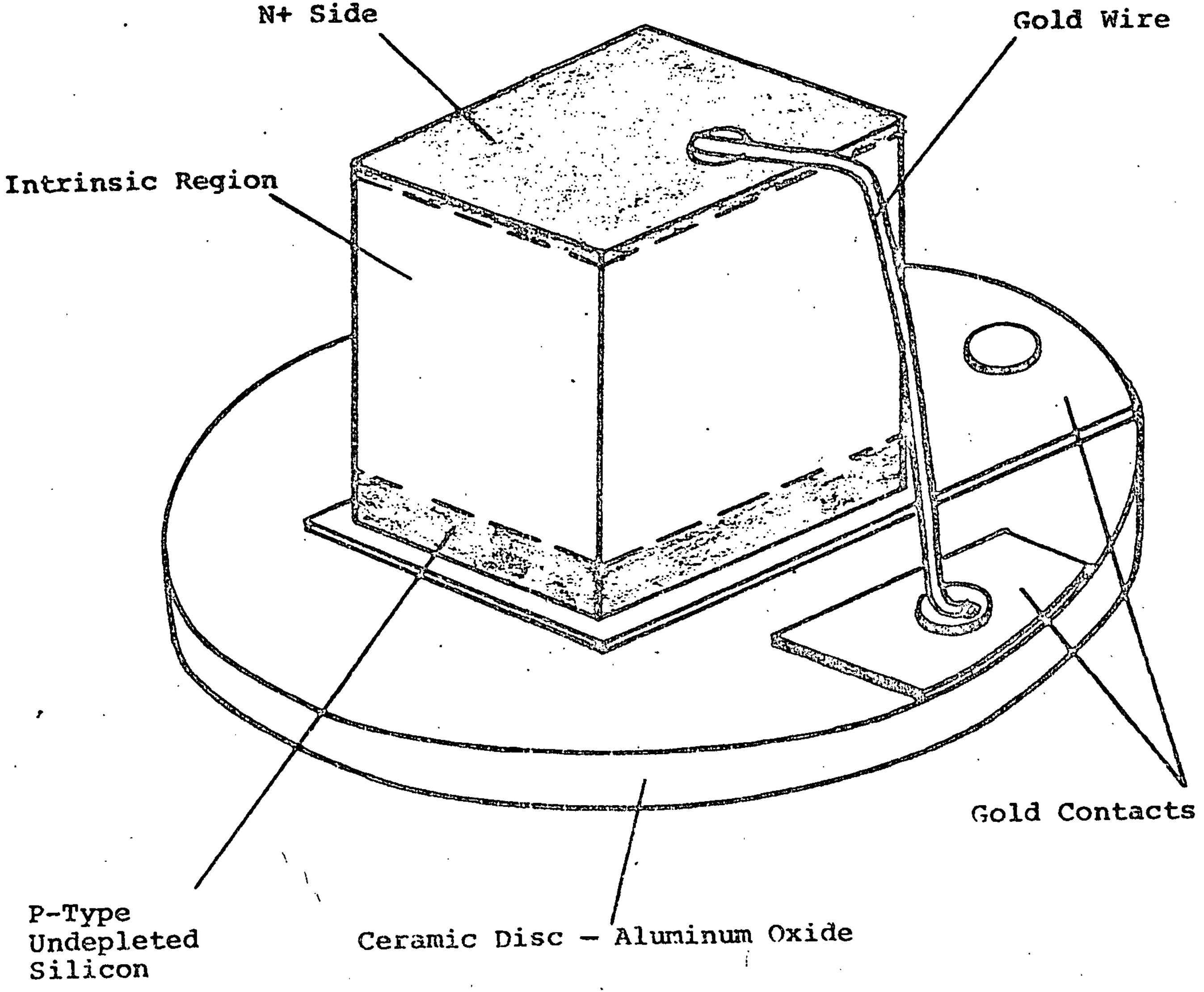


Figure 5. SILICON DETECTOR

TABLE I
CHANNEL BOUNDARIES AND ENERGY LEVELS

DETECTOR CHANNEL	DETECTOR SIZE (MM)	INTEGRAL PROTON BOUNDARIES (MEV)	SHIELD THICKNESS (CM)	DISC. LEVEL (MEV)	ELECTRON THRESHOLD ENERGY
1	2	7.9	.037	2	0.45
2	2	18.5	.180	2	1.22
3	2	29.1	.406	2	2.38
4	2	39.7	.710	2	3.90
5	2	77.3	.890 BR	2	

The response of the integral proton channels to omnidirectional protons has been calculated. The calculation was based on the range energy relation for energy degradation and consisted of determining, as a function of angle, the portion of the detector thick enough to provide a pathlength long enough to absorb enough energy to exceed the discriminator level and integrating over 2 π steradians.

A calibration program is planned to provide data needed to confirm the analytic response functions. Since the response function is strongly dependent upon the dimensions of the detector sensitive volumes, the detector thicknesses will be measured by means of penetrating protons from a cyclotron. Angular response data will be taken for protons to confirm or correct the analytic response functions. Electron angular response data will be taken in order to generate the electron response functions.

2. SENSOR DESIGN

2.1 DESCRIPTION AND PHYSICS OF DETECTORS

The detectors to be used on the EPS are constructed of lithium drifted silicon. This type of device is fabricated by starting with a moderately pure piece of P-type silicon. Lithium is deposited on one surface of the silicon and then diffused and drifted throughout the volume of silicon at elevated temperatures. The lithium, an N-Type (Donor) material, compensates electrically the principal impurity, namely, boron (acceptor) resulting in a structure of rather high resistivity.

The detector is operated basically as a reversed biased diode (Fig. 1). An ionizing particle, for example a proton, entering the detector loses energy by ionization in the silicon creating a series of hole-electron pairs along its path. Under the influence of the applied electric field (bias voltage) the holes move toward the negative electrode and the electrons toward the positive side setting up a voltage pulse across a load resistor. This pulse is then amplified and shaped by external circuitry. The number of hole-electron pairs created and hence the pulse output is linearly proportional to the energy lost in the active volume by the incident ionizing particle. In the case where the particle is stopped in the active volume the pulse output is linearly proportional to the incident particle energy. For particles energetic enough to penetrate the detector the pulse output will have a more complex energy dependency but will still be linearly proportional to the energy lost in the detector.

This type of detector has the ability to maintain a constant gain over a wide temperature range. Moreover it operates with a modest bias voltage of a few hundred volts and is relatively insensitive to bias voltage changes.

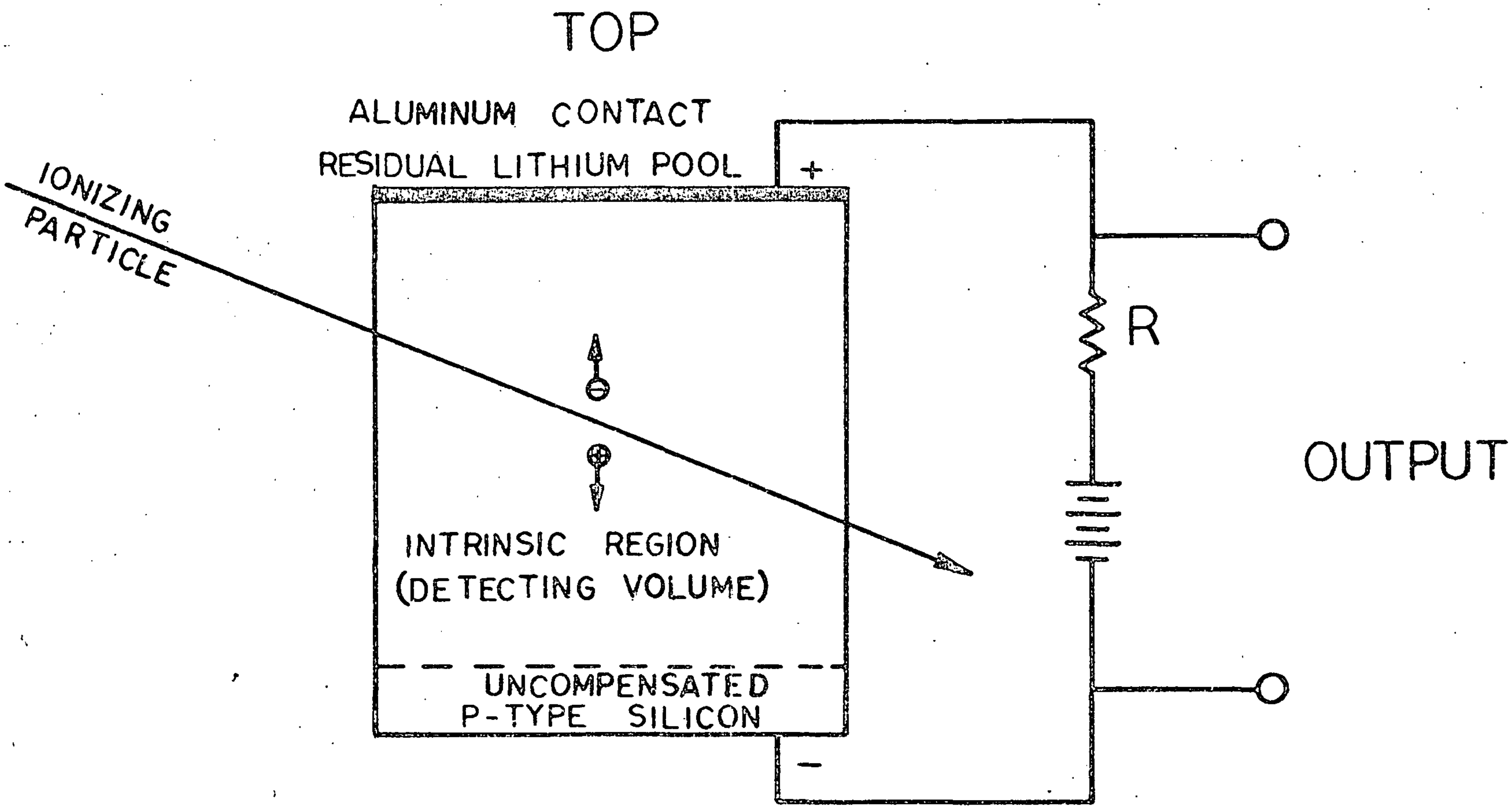


Figure 1 DETECTOR AND EXTERNAL CIRCUIT

2.2 LIMITATIONS OF THE DETECTORS

The EPS requirements of a 2 π steradian acceptance solid angle and omnidirectionality within this angle require a detector of open geometry. Figure 2 shows the geometry of an EPS detector. The silicon is mounted exposed on an aluminum oxide disc which is mounted on a T05 transistor header. Electrical contact is made to the top of the silicon by a fine gold wire bonded with conducting cement. The silicon cube is epoxy bonded to the aluminum oxide disc. The most probable point of mechanical failure, if incurred, would be at the bond between the cube and the disc during temp-cycling and/or vibration. It is intended to temperature cycle and vibration test each detector as part of the acceptance testing.

As in any type of solid state detector the EPS detectors exhibit a standing D.C. leakage current which in turn creates noise in the detector. The leakage current and hence the noise are directly proportional to temperature, although non-linearly. Detector noise affects instrument operation in two ways: 1) By contributing to the energy resolution and, 2) By contributing false counts. Neither of these are expected, however, to be significant at the anticipated flight temperatures.

Construction of this type geometry detector requires leaving a region of uncompensated P-Type silicon to accomodate the continued drift of the lithium. The lithium drift rate is temperature and bias dependent. At the anticipated flight temperatures, however, the total drift during the mission is expected to be within tolerable limits.

In the EPS detectors particles will enter the five exposed sides of the silicon cube, and in the case of the more energetic particles, will completely penetrate. A knowledge therefore of the active volume of the detector is necessary. Previous measurements have shown that the lateral dimensions can be manufactured rather accurately. The thickness in the direction of the lithium drift, however, will be ascertained for each detector by means of nuclear thickness measurements with a particle accelerator.

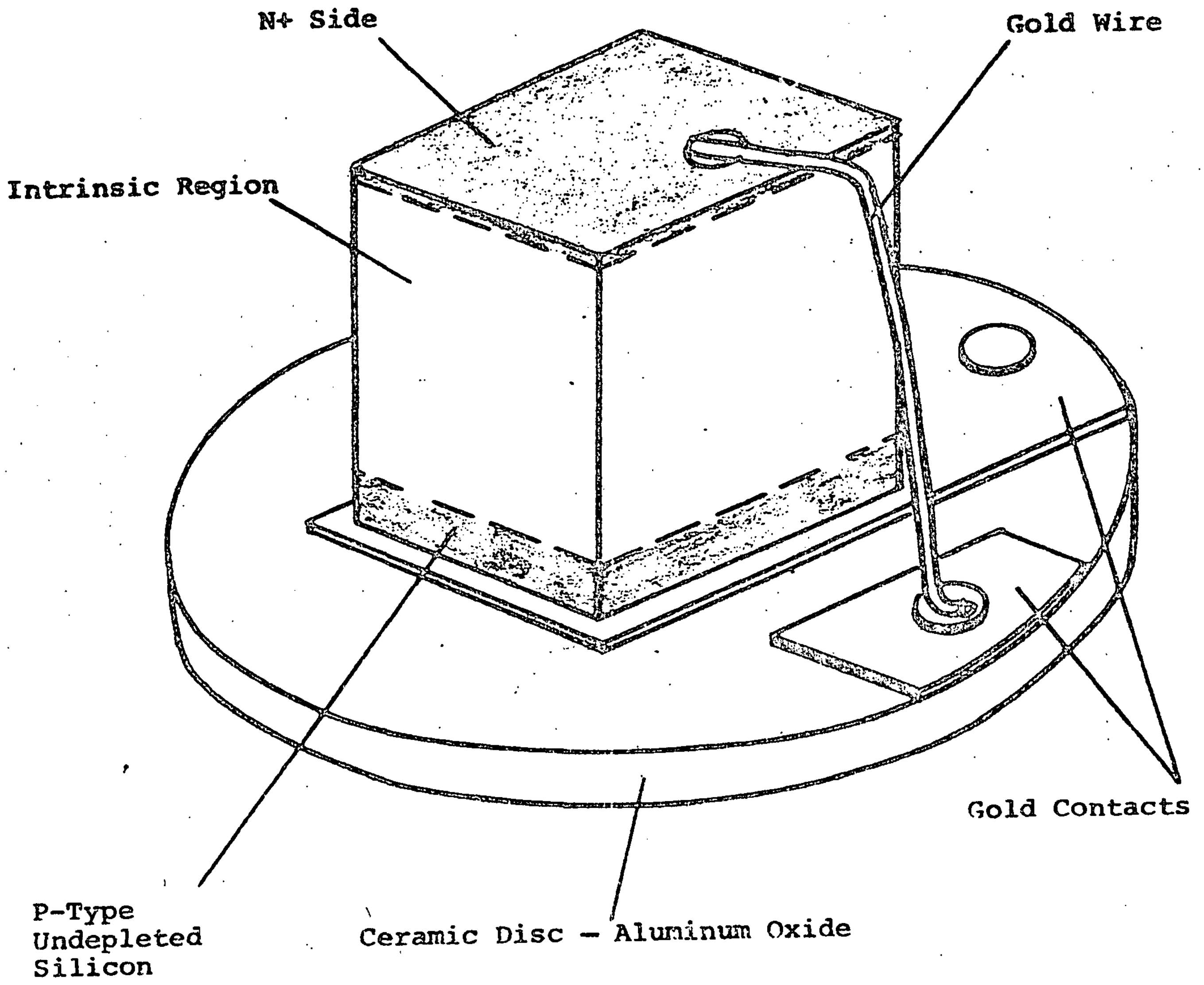


Figure 2 DETECTOR GEOMETRY

3. ELECTRICAL DESIGN

3.1 SYSTEM OPERATION

The EPS electrical package consists of five systems, namely:

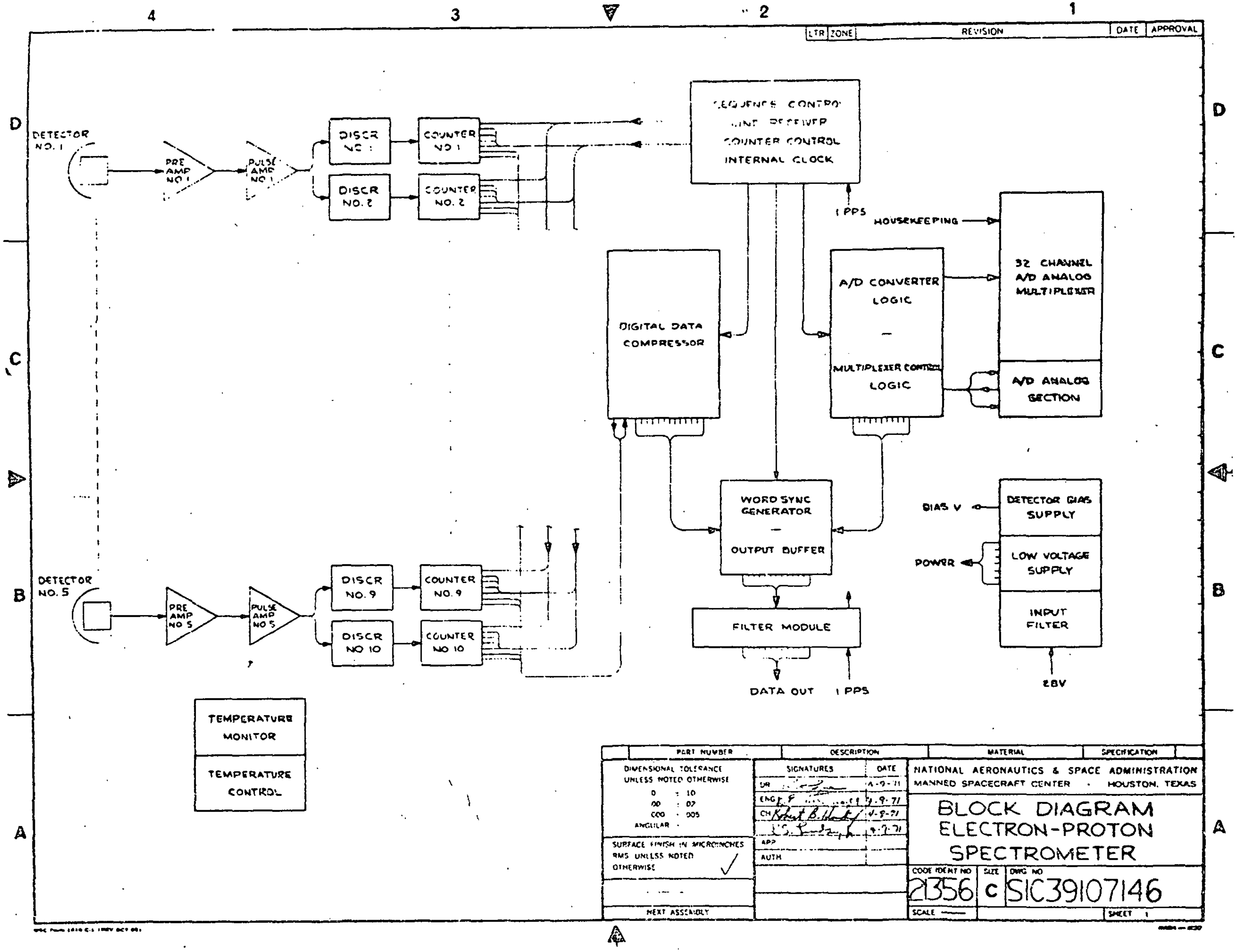
Scientific Analog System
Data Processor System
Housekeeping System
Power System
Heater System

The functional interdependence of these systems is shown in Drawing SIC39107146, Block Diagram Electron-Proton Spectrometer.

The purpose of the Scientific Analog System (see block diagram) is to detect the random occurance of current impulses eminating from EPS detectors, determine if the total impulse charge exceeds a predetermined value, and if so submit an output signal for recording by the Data Processor. There are five scientific channels which are:

Independent
Adjustable in counting level to allow use with
  detectors having variable dimensions
Capable of single valued counting-rate performance
  to 10^6 counts per second
Immune to detector generated noise

Each scientific channel is made up of a preamplifier, a pulse amplifier, and a dual pulse height discriminator.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APPROVAL
DETECTOR NO. 1
PRE AMP NO 1
PULSE AMP NO 1
DISCR NO 1
DISCR NO. 2
COUNTER NO 1
COUNTER NO. 2
SEQUENCE CONTROL LINE RECEIVER COUNTER CONTROL INTERNAL CLOCK
1 PPS
HOUSEKEEPING
32 CHANNEL A/D ANALOG MULTIPLEXER
A/D ANALOG SECTION
A/D CONVERTER LOGIC — MULTIPLEXER CONTROL LOGIC
DIGITAL DATA COMPRESSOR
WORD SYNC GENERATOR — OUTPUT BUFFER
FILTER MODULE
DATA OUT
1 PPS
DETECTOR BIAS SUPPLY
LOW VOLTAGE SUPPLY
INPUT FILTER
BIAS V
POWER
28V
DETECTOR NO. 5
PRE AMP NO 5
PULSE AMP NO 5
DISCR NO. 9
DISCR NO 10
COUNTER NO. 9
COUNTER NO 10
TEMPERATURE MONITOR
TEMPERATURE CONTROL
PART NUMBER
DESCRIPTION
MATERIAL
SPECIFICATION
DIMENSIONAL TOLERANCE UNLESS NOTED OTHERWISE
.0 ± .10
.00 ± .02
.000 ± .005
ANGULAR ±
SURFACE FINISH IN MICROINCHES RMS UNLESS NOTED OTHERWISE
✓
NEXT ASSEMBLY
SIGNATURES
DATE
DR
4-9-71
ENG
4-9-71
CH Robert B. Blank
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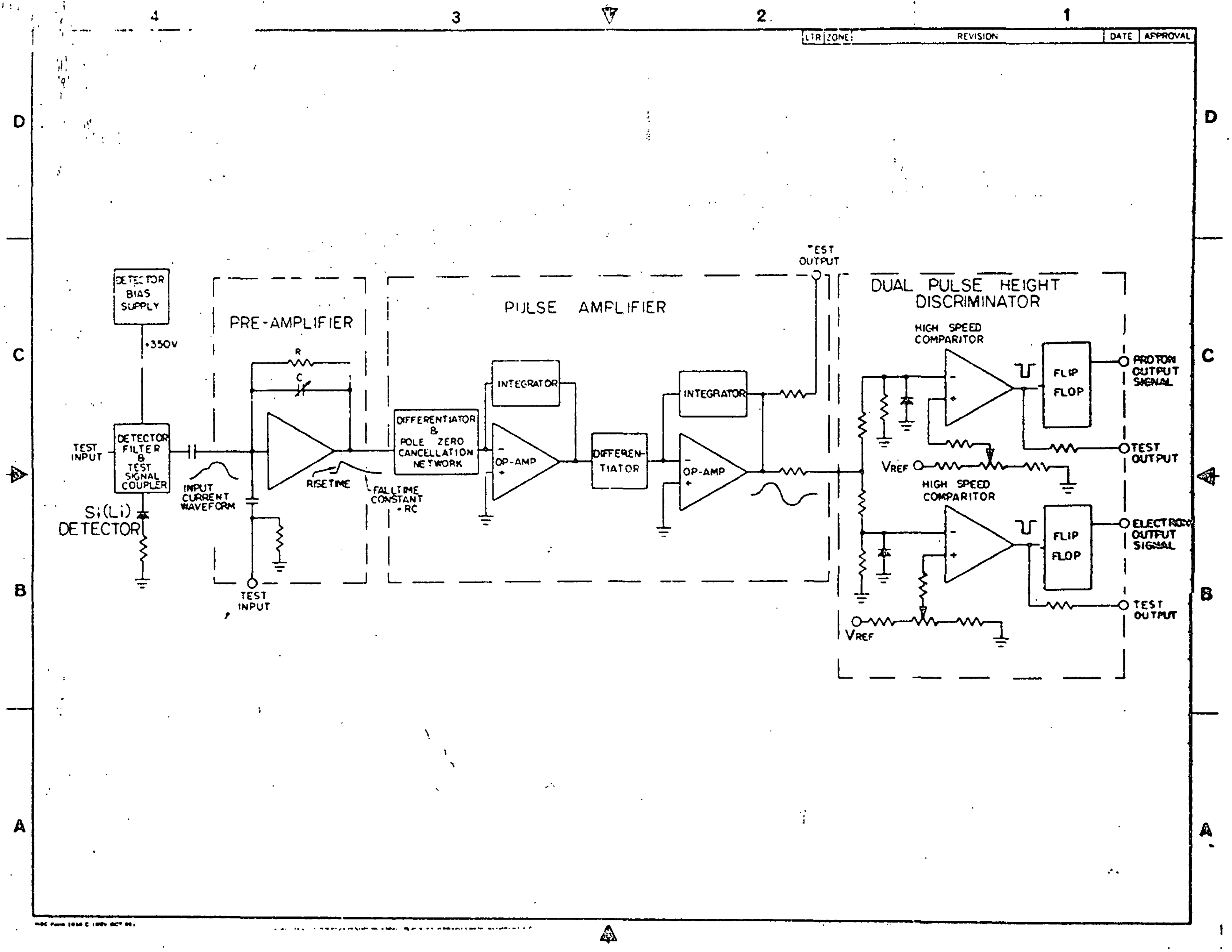
APP
AUTH
NATIONAL AERONAUTICS & SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER · HOUSTON, TEXAS
BLOCK DIAGRAM
ELECTRON-PROTON
SPECTROMETER
CODE IDENT NO
21356
SIZE
C
DWG NO
SIC39107146
SCALE
SHEET 1



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APPROVAL
DETECTOR BIAS SUPPLY
+350V
TEST INPUT
DETECTOR FILTER & TEST SIGNAL COUPLER
Si(Li) DETECTOR
INPUT CURRENT WAVEFORM
PRE-AMPLIFIER
R
C
RISETIME
FALLTIME CONSTANT = RC
TEST INPUT
PULSE AMPLIFIER
DIFFERENTIATOR & POLE ZERO CANCELLATION NETWORK
INTEGRATOR
OP-AMP
DIFFEREN-TIATOR
INTEGRATOR
OP-AMP
TEST OUTPUT
DUAL PULSE HEIGHT DISCRIMINATOR
HIGH SPEED COMPARITOR
FLIP FLOP
PROTON OUTPUT SIGNAL
TEST OUTPUT
V_{REF}
HIGH SPEED COMPARITOR
FLIP FLOP
ELECTRON OUTPUT SIGNAL
TEST OUTPUT
V_{REF}

The preamplifier converts the detector's current impulse to a slowly decaying step function whose amplitude is proportional to the total charge input. The pulse amplifier filters this step input producing a bipolar waveform at its output. The dual pulse height discriminator compares the bipolar wave form to two reference levels. If the input wave form exceeds either of these two reference levels, a corresponding output pulse is directed to a prescaler. The prescaler generates an output signal for every other excitation of the discriminator.

The function of the Data Processor is to digitally integrate the prescaler outputs individually and present the information to the spacecraft telemetry system in an acceptable form under control of the spacecraft. This integration provides 12 seconds of counting for every 13 seconds of real time. In addition, the Data Processor accepts analog housekeeping signals, digitizes them sequentially and properly mixes this with the scientific information. The data processor utilizes high reliability, low power TTL logic in its digital section and high reliability low power amplifiers in its analog to digital converter section. The Data Processor consists of the following modules:

Sequence Control, Line Receiver, Counter Control
Counter/Memory Module (10)
Digital Data Compressor and Internal Clock
Analog Digital Converter
A/D Control
Multiplexer Module
Output Buffer and Word Sync Generator

The Housekeeping System provides signals to the Data Processor analog to digital converter that yield information concerning the operational status of all important EPS parameters. Those functions monitored include:

- detector leakage currents
- detector resolutions
- electronic package temperature
- detector plate temperature
- power supply levels
- heater status

A time of 208 seconds is required to transmit a complete cycle of housekeeping information. Ground based analysis of this data allows proper manual control of EPS mode of operation.

The EPS Power System accepts spacecraft power and converts it to levels required by the EPS. Major subsystems are the Low Voltage Converter and the Detector Bias Supply.

The Heater System functions in a temperature control capacity. An internal temperature sensor is continually monitored by control circuitry. If the package temperature drops below 0°C, six watts of power is dissipated in the inner housing structure by skin heaters. When the temperature rises above 10°C, the six watts of power is removed.

3.2 SCIENTIFIC ANALOG SYSTEM

3.2.1 PREAMPLIFIER

The EPS preamplifier (Schematic SIC39106631) was designed to provide amplification of signals from semiconductor detectors which were exposed to electron and proton radiation in the energy range between a few keV and several MeV.

The preamplifier was implemented using a charge sensitive configuration whereby an impulse of current produced by energy deposition in the detector is transformed into a fast rising and slow decaying (practically a step function) voltage signal at the output of the preamplifier where the peak of this voltage is directly proportional to the amount of energy deposited in the detector.

The charge sensitive preamplifier (see block diagram) is basically an operational amplifier with the loop closed through the charge coupling capacitor (Cf) and provides good gain stability, linearity, and a fast rise time.

Upon absorbing some amount of energy the detector gives off an impulse of current containing a charge Q.

The time domain output voltage is given by:

$$Vo(t) = \frac{Q}{Cf} e^{-\frac{1}{RfCf} t}$$

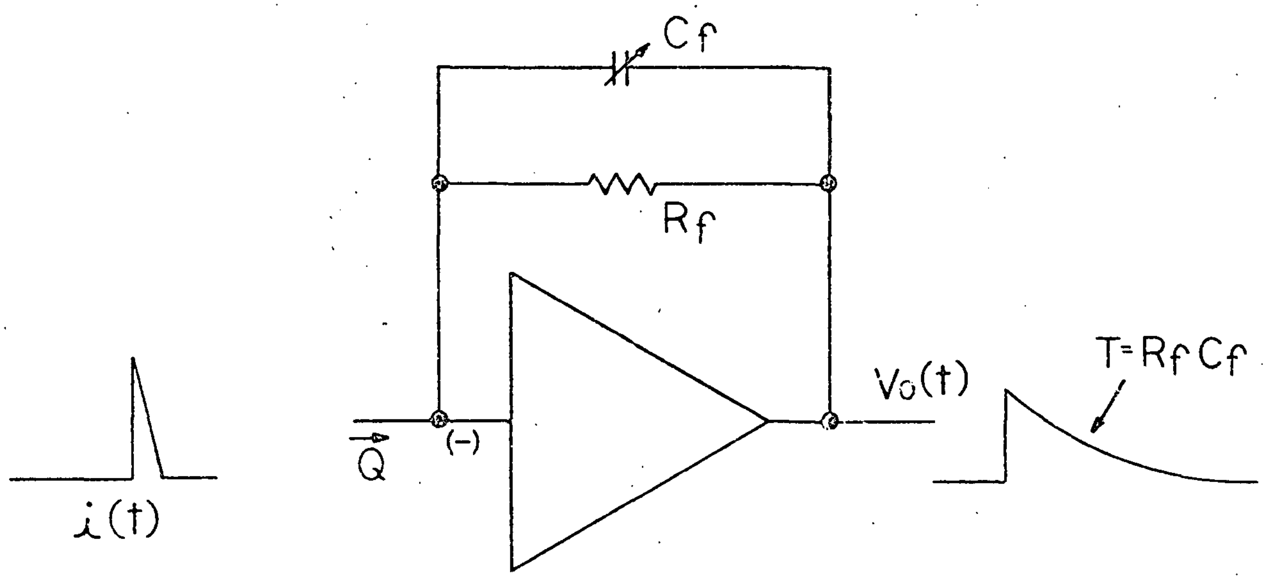
which shows that for very short times the exponential term will approach 1 and the output voltage will be directly proportional to the input charge. The feedback capacitor serves as the constant of proportionality.

In the EPS preamplifier, Cf was made variable so as to provide a means of adjusting the charge conversion gain. To optimize the performance of the EPS preamplifier, a low noise, high transconductance FET (Q_1) is used as the input stage.

The detector and the detector bias filter are ac coupled to the FET's gate electrode.

The preamplifier was designed to operate from a dual power source, therefore, it is possible to dc couple the output to the pulse amplifier, thus improving the system's high count rate capabilities.

Overall power consumption of the preamplifier is low (144 mw) and the performance meet all the EPS specifications.



PREAMPLIFIER BLOCK DIAGRAM

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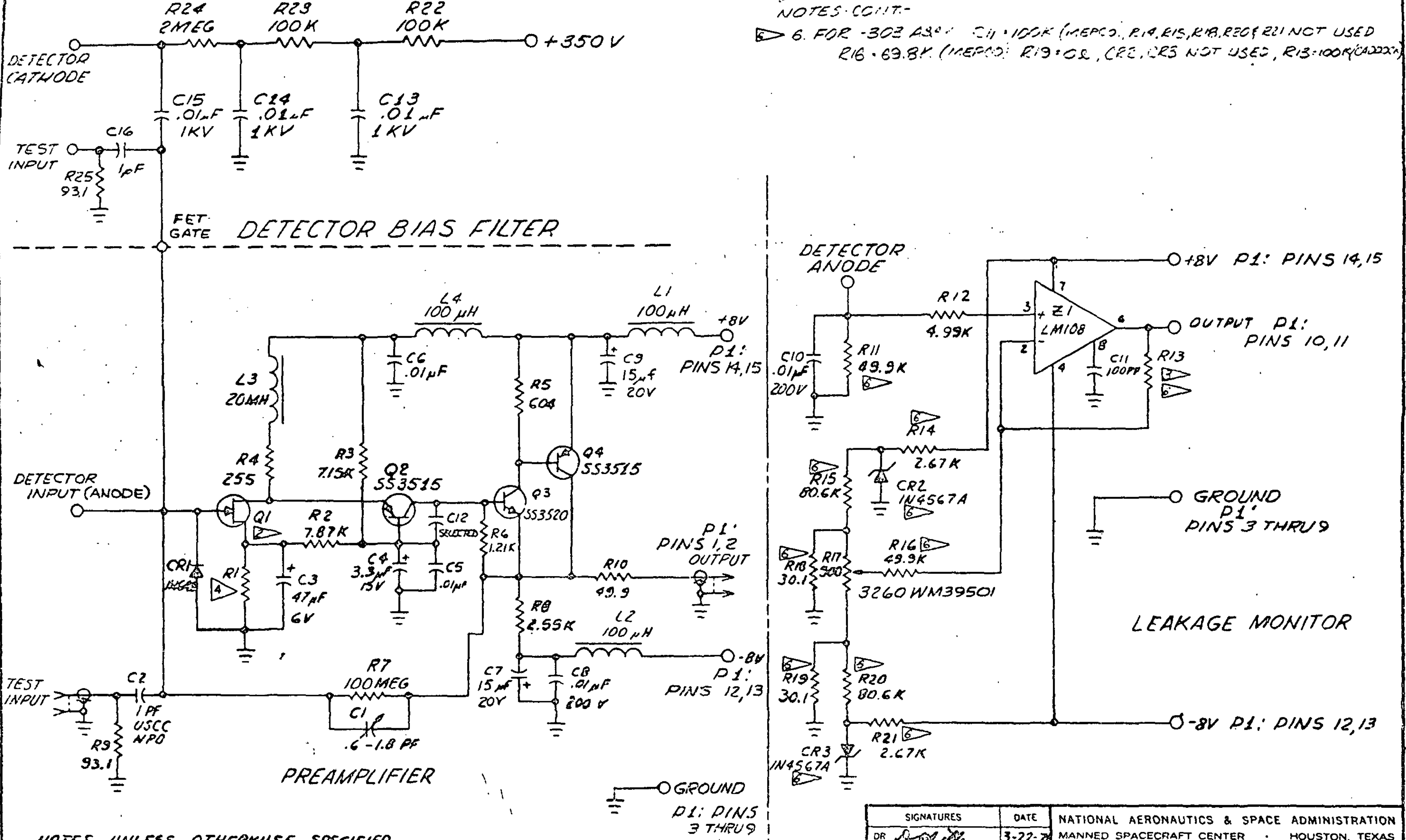


NOTES CONT.-

6. FOR -303 ASSY R11 = 100K (MEPCO), R14, R15, R18, R20 & R21 NOT USED R16 = 69.8K (MEPCO) R19 = 0Ω, CR2, CR3 NOT USED, R13 = 100K (CADDOCK)

NOTES: UNLESS OTHERWISE SPECIFIED.

1. INTERPRET PER MSC MANUAL MSCM8500.
2. Q1 SELECTED SSC6113
3. FOR 1µA INPUT R13 = 5.0 MEG. FOR 2µA INPUT R13 = 2.5 MEG. CADDOCK MK-132
4. SELECTED, DEPENDENT UPON Q1.
5. ALL RESISTORS ARE RNC50 EXCEPT: R4 & R8 (RNC55) AND R22 - R24 (CADDOCK MK-132)

-CONT-

SIGNATURES		DATE
DR	[illegible]	3-22-71
ENG	W.A.O.	5/25/71
CH	[illegible]	3-23-71
	[illegible]	5-21-71
APP RELEASE	R.P.D.	8/13/71
AUTH		

NATIONAL AERONAUTICS & SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER · HOUSTON, TEXAS

SCHEMATIC, PREAMPLIFIER & DETECTOR LEAKAGE MONITOR

ELECTRON-PROTON SPECTROMETER

CODE IDENT NO.	SIZE	DWG NO
21356	C	SIC 39106631

SCALE — ISD-EB SHEET

ELECTRON-PROTON SPECTROMETER

EPS PREAMPLIFIER
SPECIFICATION

1. Preamplifier Conversion Gain: 29.6 mV/Mev.

2. Output Rise Time vs Input Capacitance

   Less than 1.0 nsec/pf.

3. Output Amplitude vs Power Supply Change:

   Less than .002 Volt/Volt

4. Input Resolution vs Input Capacitance:

   Less than 8.0 keV for Cin up to 30 pf.
   Slope above 30 pf approximately .066 keV/pf.

5. Input Resolution vs Temperature:

   Less than .04 keV/°C.

6. Output dc Offset Voltage: Between 100 mV and 300 mV.

7. Output Pulse Decay Time Constant:

   Approximately 150 μsec.

8. PHA Peak Channel Number vs Preamplifier Input Capacitance:

   Less than .022%/pf.

9. Output Resistance: 49.9 Ω

10. Power Dissipation:

    +8.1 volts at 14 mA.
    -8.1 volts at 4 mA.
    $P_{TOTAL} = 144$ mw

3.2.2 PULSE AMPLIFIER

The pulse amplifier shapes the preamplifier's output and amplifies the signal to a level usable by the pulse height discriminators. Pulse shaping is necessary to minimize the system resolving time and narrow the bandwidth for good signal-to-noise ratio. The amplifier output is a bipolar pulse; this eliminates the need for a baseline restorer and reduces circuit complexity.

Other requirements are found in the "Pulse Amplifier Specifications" list. The circuit design has been optimized to meet these specifications with a minimum of power consumption.

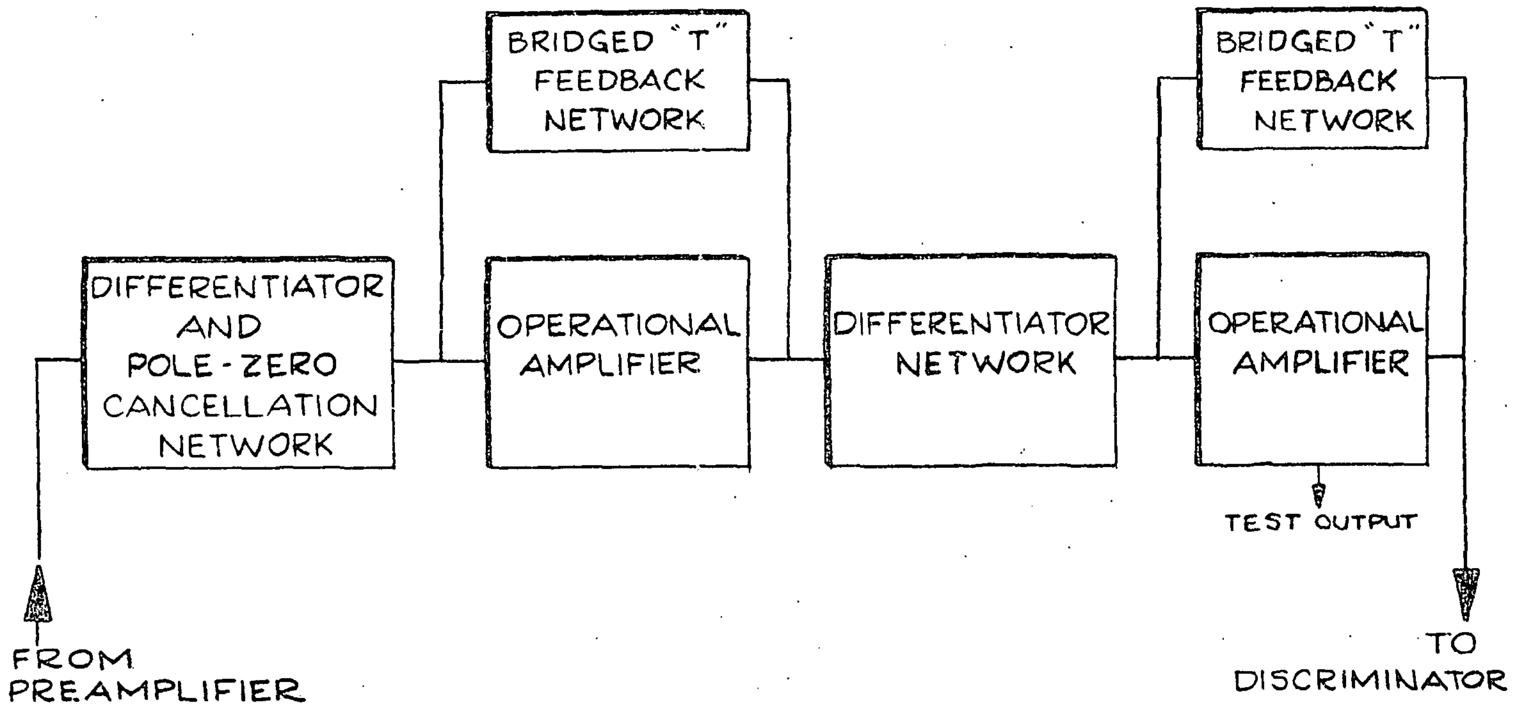
The pulse amplifier is composed of two cascaded active R-C filters (see pulse amplifier block diagram). Each filter contains a differentiator, an operational amplifier and feedback network.

The first differentiator is combined with an adjustable pole-zero concellator which is set to cancel the decay time constant of the preamplifier. This network is shown in detail on the Schematic SIC39106627 and consists of R_1, R_2, R_3, and C_1. The second differentiator consists of C_{16} and R_{27}.

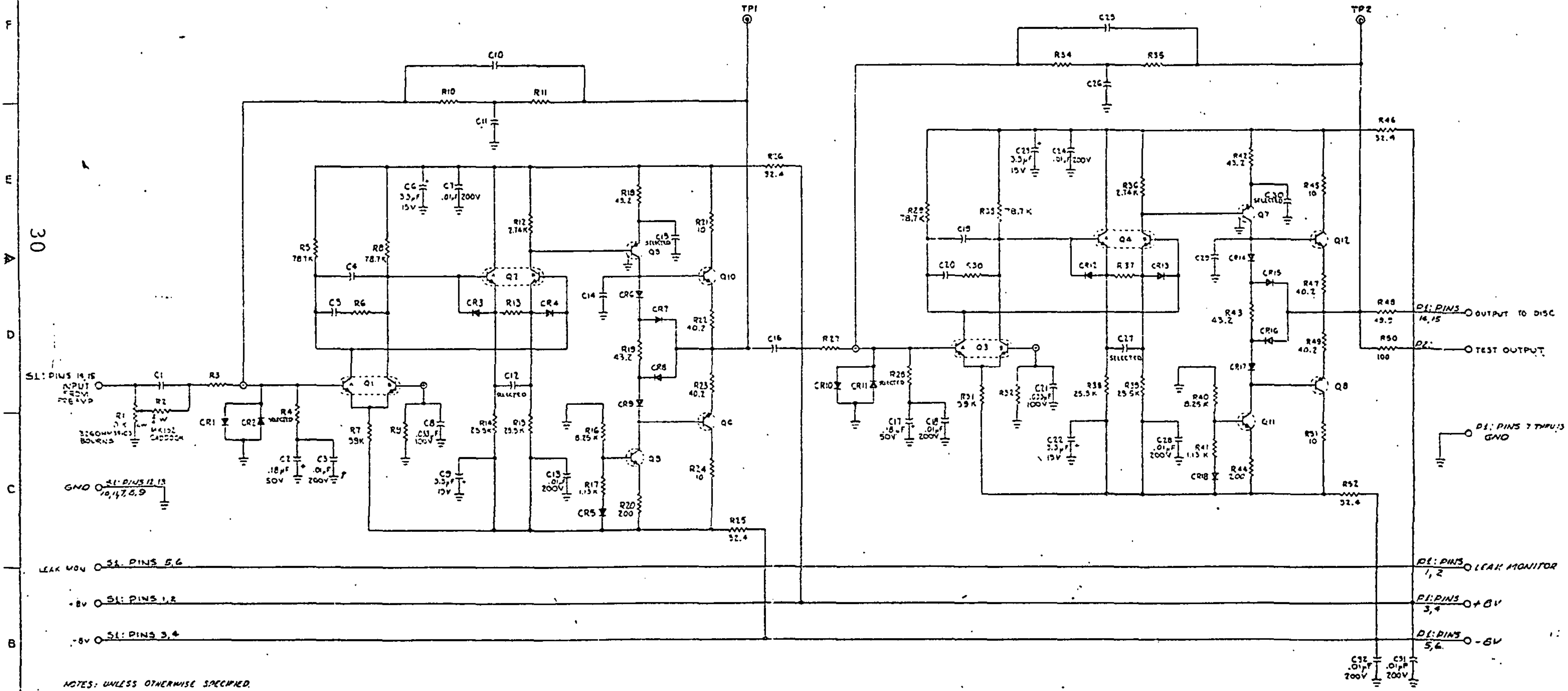
The feedback networks consist of C_{10}, C_{11}, R_{10}, R_{11}, C_{25}, C_{26}, R_{34}, and R_{35}.

The operational amplifiers are identical except for the test output of the second one. This test output is needed for calibration. To obtain sufficient slew rate with minimum power consumption the amplifiers are compensated for an open loop frequency response with a 12 dB/octave roll off. As in the case of the differentiator and feedback components the compensation values are not given in the basic schematic but are listed on the assembly drawing. Diodes CR_1, CR_2, CR_3, CR_4, CR_{10}, CR_{11}, CR_{12}, and CR_{13} are used for protection of the transistors. Short circuit protection is obtained with CR_7, CR_8, CR_{15}, and CR_{16}.

The bipolar pulse is obtained by the use of the second differentiator. Placing this differentiator between the amplifiers instead of after the second amplifier results in a requirement for a lower power supply voltage, therefore, reducing power consumption to about one half.



PULSE AMPLIFIER BLOCK DIAGRAM



NOTES: UNLESS OTHERWISE SPECIFIED.

1. INTERPRET PER MSC MANUAL MSCM8500.
2. CR1-CR18 ARE 1N4153 ; Q1-Q4 ARE 2N4878, Q5-Q8 2N4261 , Q9-Q12 2N2708 ; ALL RESISTORS ARE RNC50
3. FOR VALUES OF R2,3,4,6,7,10,11,13,27,28,30,32,34,35,37 AND C1,4,5,10,11,12,14,15,16,19,20, C25,26,27,29, AND 30 SEE ASSY DWG SEC39107187.

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MANNED SPACECRAFT CENTER . HOUSTON TEXAS

SCHEMATIC DIAGRAM,
PULSE AMPLIFIER -
ELECTRON-PROTON SPECTROMETER

21356 | E | SEC 39106627

ELECTRON - PROTON
SPECTROMETER

PULSE AMPLIFIER
SPECIFICATIONS

Pulse Gain: 16.0 ± 8%

Gain Stability:

Temperature Stability: Less than .02%/°C

Stability as a Function of Supply Voltage: Less than .2% for 0.1V change in both supplies.

Linearity: Less than 1.2% deviation from best straight line to ± 5V out.

Input Polarity: Positive

Output Polarity: Positive

Preamp-Post Amp Calibration: +5 V out = 10 mev

Pulse Shaping Time Constants: 360 ns

Pole-Zero Cancellation: Adjustable from 40 μs to infinity.

Overload Recovery: Recovers from X10 overload in $\leq$ 2 normal pulse widths to less than lower discriminator setting.

Output Noise: Less than 1.0 mV FWHM for no input.

Average Baseline Shift with Counting Rate: $\leq \pm 5$ mV

Baseline Stability Based on 10K Feedback Resistor +25°C Value:
6.6 mV max, 2 mV typ.
Temp. Stability: 72 μV/°C max.
As a function of supply voltage: 0.13 mV typ for a change in both supplies of 0.1V.

Output Coupling: Direct.

Discriminator Output Load: 1.3 KΩ min, 10 pf max.

Power Requirements: +8V @ 10.8 mA typ, -8V @ 12.2 mA typ, 220 mw max.

Output Short Circuit Protected

Test Output Load: 4 KΩ min, 60 pf max.

Slew Rate: Greater than 22V/μs for a time constant of 360 ns.

OPERATIONAL AMPLIFIER
SPECIFICATIONS

+25°C except as noted.

Open Loop Gain at 10 KC: 79 to 87 dB.

Open Loop Gain Stability: With temp. from +25°C to -25°C, less than 10%.

With supply voltage, less than 1% for 0.1 V charges in both supplies.

Linearity: Less than 12% from -5V to +5V out.

Output: ± 5V Maximum.

Input Offset Voltage (Max): 6.0 mv (2 mv typ.) +60 μV/°C

Input Offset Current (Max): 60 nA + 1.2 nA/°C

Minimum Load Resistance (including feedback network): 660Ω

Power Requirements:

± 8V, 100 mw max (90 mw typ).
+8V @ 5.4 ma typ.
-8V @ 6.1 ma typ.

Input Offset Voltage Change with Supply Voltage:

0.13 mv (typ) for any combination of 0.1V change in supply voltages.

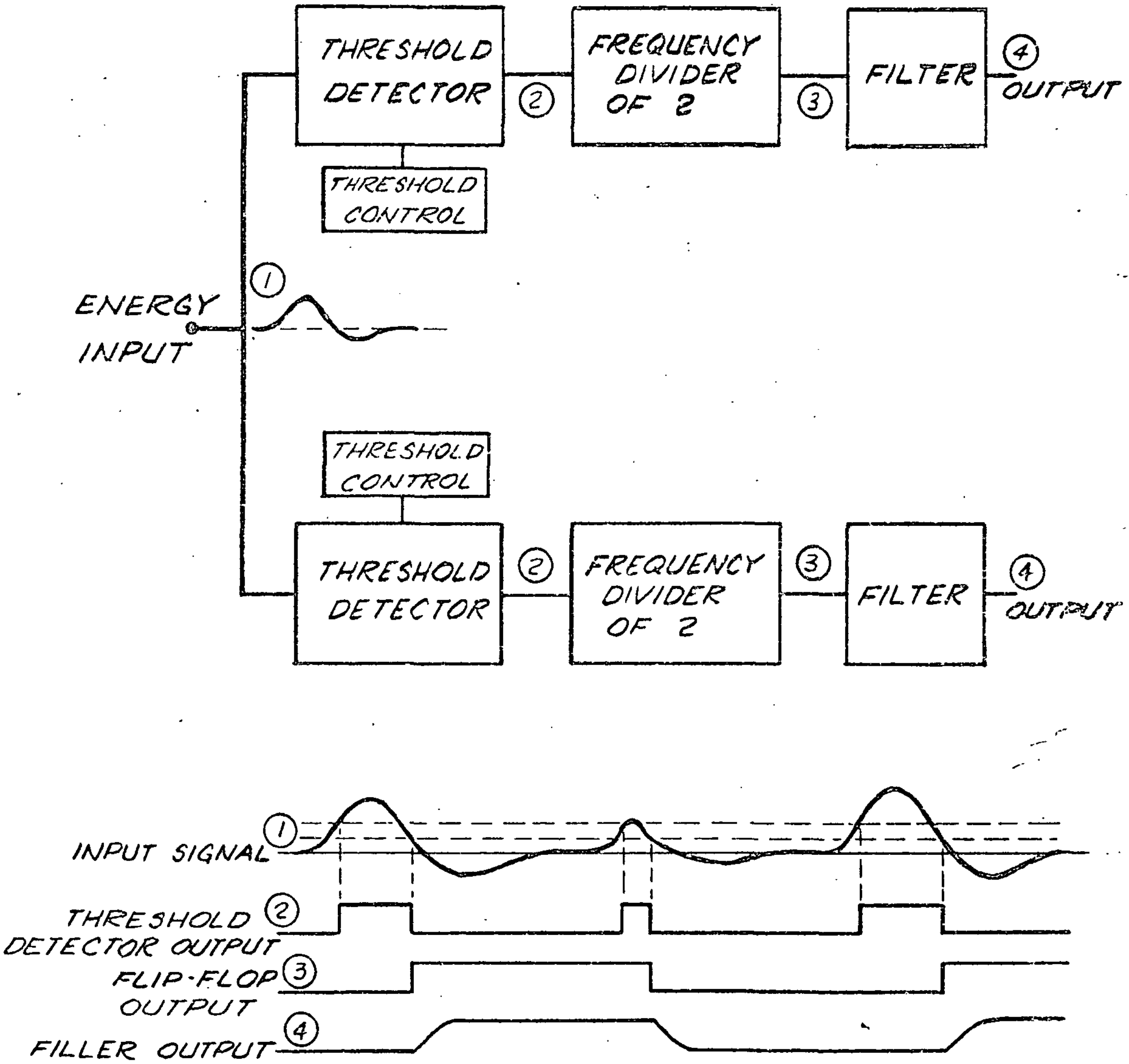
Short Circuit Protected.

For use in the inverting configuration.

3.2.3 DUAL DIFFERENTIAL PULSE HEIGHT DISCRIMINATOR

The dual pulse height discriminator consists of two functionally identical circuits whose purpose is to determine whether an energy deposition in the corresponding EPS detector exceeds two independently predetermined values. Electronically the two predetermined energy deposition values allow the detection of electron and proton events above a known energy level. A functional block diagram is included.

Due to counting-rate requirements, the portion of the input signal that is observed for analysis by the circuit is restricted to 1080 nsec for all channels. The time spent above the circuits threshold becomes vanishingly small for signals close to the threshold value, however. This requires the use of an exceptionally fast discriminator and resulting output signals may be as short as 20 nsec. Since these signals must eventually be recorded by the EPS Data Processor which is interconnected to the discriminator output by several inches of unshielded wire, a flip-flop is included to increase the pulse width to one capable of being handled by the lower frequency low-power counters. An output filter increases the rise time of signals transmitted to the data processor to approximately 30 nsec. In this way the possibility of internally generated EMI is minimized.

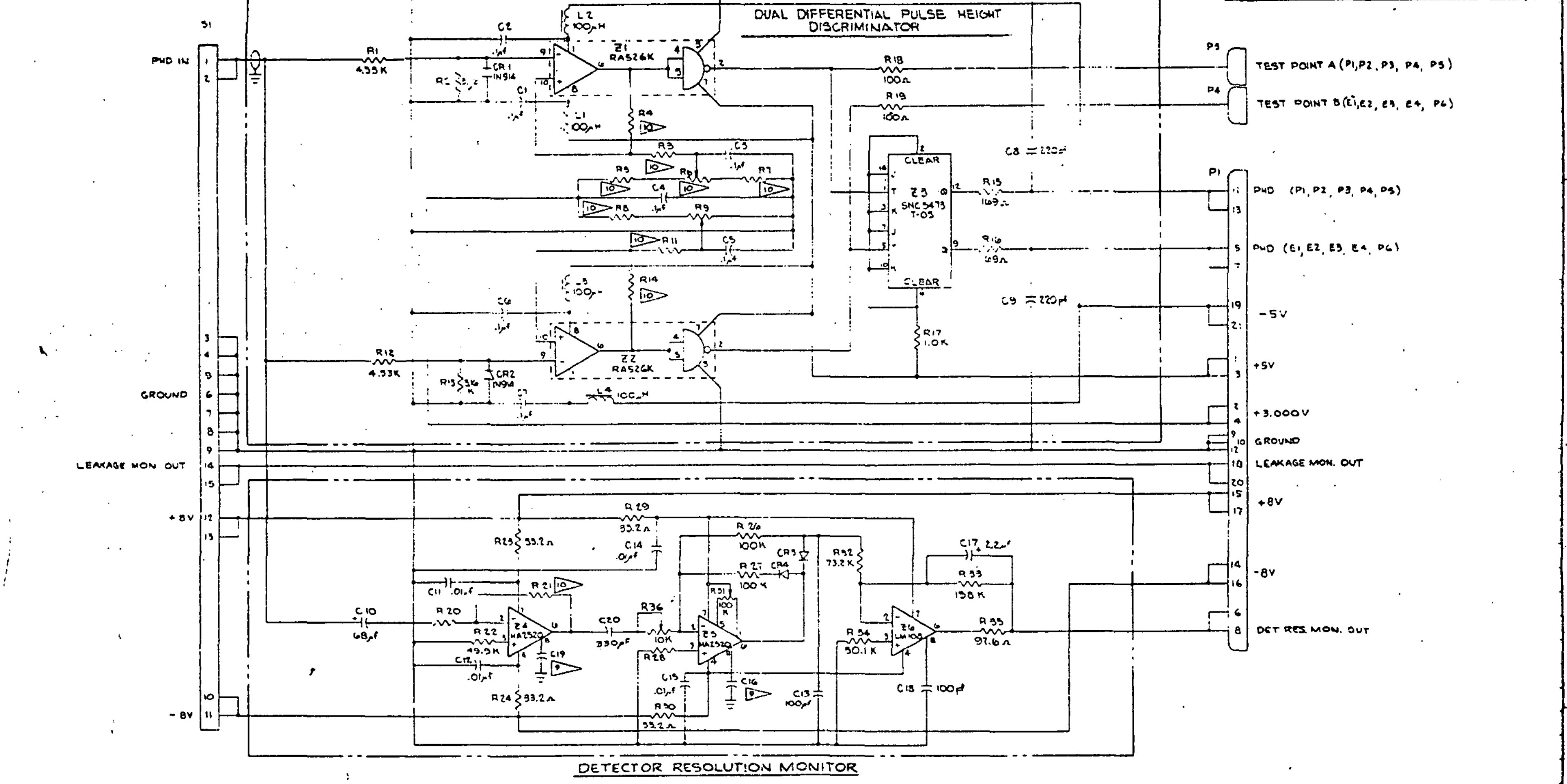


DUAL DIFFERENTIAL PULSE HEIGHT DISCRIMINATOR BLOCK DIAGRAM

The Dual Pulse Height Discriminator Performance Specification, included, presents the design criteria for this circuit. All design criteria have been met.

Drawing SIC 39106633 is the schematic diagram of the Dual Pulse Height Discriminator. Resistors R1 and R2/R12 and R13 serve as an input signal attenuator to reduce the value of the largest possible positive input signal to the derated maximum value of integrated circuit Z1/Z2. Diode CR1/CR2 serves to clamp the negative portion of any input signal to a value less than the derated maximum value of integrated circuit Z1/Z2. Integrated Circuit Z1/Z2 functions as a high speed differential amplifier. The input signal is directed to the amplifier's negative input terminal. Whenever the negative input terminal becomes more positive than the positive terminal, the amplifier's output switches from +4 volts to 0 volts. In this way the amplifier functions as a differential comparitor. The reference value (trip point) is determined by Resistors R5, R6, and R7/R8, R9, and R10 and the reference input voltage. By adjusting the values of these resistors, the threshold may be preset to any value from 50 keV equivalent energy to 10 MeV equivalent energy. Resistors R3 and R4/R11 and R14 provide the amplifier with positive feedback to ensure very crisp (non oscillating) response by making the amplifier reset point 50 keV equivalent energy less than the trip point. Integrated circuit Z1/Z2 includes a TTL compatible two input Nand Gate. This gate logically inverts the output signal to one of 0 volts to +4 volts. The gate's output is connected to the clock input of one of the flip-flops in Z3. This flip-flop

LTR	ZONE	REVISION	DATE	APPROVAL
A		[illegible]	[illegible]	[illegible]
B		ADDED [illegible] NOTE 10	[illegible]	[illegible]
C		TABULATED VALUES OF R20 & R28	[illegible]	[illegible]
D		TABULATED VALUES OF R21	[illegible]	[illegible]



DETECTOR RESOLUTION MONITOR

NOTES: UNLESS OTHERWISE SPECIFIED.
1. INTERPRET PER MSC MANUAL MSCM 8500.
2.
3. ¹MEPCO RNC50H FR.
4. ²CADDOCK MK-132 (±1%, ±50 ppm/°C).
5. ³BOURNS 3260HM39101
6. ⁴BOURNS 3260HM39500
7. ⁵BOURNS 3260HM39201
8. CR3 & CR4 ARE H.P. P/N 5082-2123.
9 ▷ C16 & C19 ARE TO BE SELECTED DURING TEST.

DETECTOR REFERENCE	R21¹	R3¹	R4²	R5¹	R6	R7¹	R8¹	R9	R20	R11¹	R14²	R28
A	100K	1.54K	500K	750Ω	200Ω³	464Ω	2.10K	50Ω⁴	49.9K	1.82K	725K	1 100K
B	100K	1.47K	440K	715Ω	"	604Ω	"	"	"	"	"	"
C	100K	1.50K	480K	737Ω	"	487Ω	"	"	"	"	"	"
D	100K	1.54K	530K	1.00K	"	294Ω	"	"	"	"	"	"
E	100K	"	550K	1.13K	100Ω³	267Ω	1.69K	200Ω³	49.9K	1.78K	750K	1 100K
A-D(-306)	36.5K	1.54K	100K	1.16K	200Ω³	69.8Ω	2.10K	50Ω⁴	4.99K	1.82K	725K	0Ω
E (-307)	36.5K	1.54K	100K	1.18K	200Ω³	69.8Ω	1.69K	200Ω³	4.99K	1.78K	750K	0Ω

10 ▷

SIGNATURES	DATE
DR B E LOPEZ	6-11-71
ENG [illegible] RSF	8-16-71
CH E. Bromfield	8-16-71
R.P. D[illegible]	[illegible]
APP	
AUTH	

ELECTRON-PROTON SPECTROMETER

NATIONAL AERONAUTICS & SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER · HOUSTON, TEXAS

SCHEMATIC DIAGRAM,
DUAL DIFFERENTIAL PULSE HEIGHT
DISC AND DETECTOR RESOLUTION
MONITOR — E.P.S.

CODE IDENT NO	SIZE	DWG NO.
21356	D	SIC 39106633

SCALE ~ | 130-025 | SHEET

changes state each time the comparitor transitions from 0 volts to +4 volts. The signals are transferred to much longer ones for processing by the EPS data processor. Resistor R15, R16 and Capacitor C8/C9 increase the rise time of the flip-flop output to approximately 30 nsec to remove the possibility of cross coupling in the wires connecting the data processor. Resistors R18/R19 serve as cable terminations for test points P3/P4. Inductors L1 and L2/L3 and L4 and Capacitors C1 and C2/C6 and C7 function as supply line filters to the differential amplifier Z1/Z2.

6-1-72
Lindsey
EPS-215

DUAL PULSE HEIGHT DISCRIMINATOR PERFORMANCE SPECIFICATION

1.0 Input Characteristics

A. Impedance: 3.85 kΩ

B. Coupling: Direct

C. Signal Range

1) Normal: 0 to +5 volts bipolar positive edge leading

2) Overload: +8.0 volts to -10.0 volts continuous

D. Threshold Range:

1) Electron 1 — 200 keV to 300 keV
2) Electron 2 — 200 keV to 300 keV
3) Electron 3 — 200 keV to 300 keV
4) Electron 4 — 200 keV to 300 keV
5) Proton 1 — 2.500 MeV to 3.500 MeV
6) Proton 2 — 2.500 MeV to 3.500 MeV
7) Proton 3 — 2.500 MeV to 3.500 MeV
8) Proton 4 — 2.500 MeV to 3.500 MeV
9) Proton 5 — 2.500 MeV to 3.500 MeV
10) Proton 6 — 0.600 MeV to 1.000 MeV

E. Pulse Pair Time Resolution: ≤ 100 nsec

F. Input Rate (Fixed Frequency): ≥ 5 MHz

2.0 Discriminator Level Stability

A. Temperature

1) 200 keV +3.0%
-25°C to +50°C ≤-1.5%

2) 7.000 MeV +0.2%
-25°C to +50°C ≤-0.4%

B. Power Supply Variation

1) 200 keV

A) +5.0 volt supply (+4.8 VDC to +5.3 VDC) ≤ +3.0% -3.5%

B) -5.0 volt supply (-4.8 VDC to -5.3 VDC) ≤ +0.5% -1.2%

C) +5.0 volt, -5.0 volt supply aggregate (4.8 VDC to 5.3 VD
≤ +3.5% -4.0%

D) +3.000 volt supply —— error equal to fractional error in supply value

2) 7.000 MeV

A) +5.0 volt supply (+4.8 VDC to +5.3 VDC) $\leq^{+0.5\%}_{-0.5\%}$

B) -5.0 volt supply (-4.8 VDC to -5.3 VDC) $\leq^{+0.1\%}_{-0.5\%}$

C) +5.0 volt, -5.0 volt supply aggregate (4.8 VDC to 5.3 VD
$\leq^{+1.1\%}_{-0.6\%}$

D) +3.000 volt supply —— error equal to fractional error in supply value

3.0 Discriminator Crispness: ≤ 10 keV

4.0 Discriminator Hysteresis: 50 keV

5.0 Prescale Factor: 2

6.0 Output Characteristics

A. Signal Output

1) DC levels: TTL

2) Fanout: ≥ 3

3) Rise Time Constant - Fall Time Constant: 10 nsec

B. Test Output

1) DC Levels: TTL

2) Output Impedance: 100Ω

7.0 Power Requirement

	-25°C	0°C	+25°C	+50°C
+5.0 VDC	43mA	44mA	44mA	42mA
-5.0 VDC	18mA	18mA	21mA	20mA
+3.000 VDC	4mA	4mA	4mA	4mA

3.3 HOUSEKEEPING SYSTEM

A definite requirement exists to measure three detector parameters in order to determine the quality of each detector. These parameter measurements are required periodically: during shelf storage of the EPS flight instruments, during the time each flight instrument is mounted on the spacecraft, and during flight. Having the capability for making these periodic measurements is of paramount importance to the overall accuracy of the EPS flight data.

Analysis of the data collected as a result of these measurements maximizes the probability of a successful mission, by providing the capability to detect and replace any degraded detector prior to flight, and by applying correction factors to the data, if required, during flight.

Because of the different non-related but dependent failure modes of the detector(s), three parameter measurements are required. None of these measurements can be eliminated due to their interdependence, as the remaining measurements will not give a positive indication of the parameter measurement or failure mode eliminated.

The required parameter measurements are: 1) detector temperature, 2) detector leakage current, and 3) detector resolution. These are discussed in detail below.

Detector Temperature Measurement

Measurement of the temperature of the detectors is required during flight as leakage current noise and lithium drift rates are dependent upon the temperature of the detectors. The leakage current increases 100 percent for approximately every 8°C increase in detector temperature, and the noise varies with leakage current, resulting in a deterioration of detector resolution, and thereby performance.

The lithium drift rate increases with an increase in temperature in addition to being linearly proportional to detector bias. Hence a knowledge of the temperature is required in order to

1) Partially or totally unbias the detector if the temperature rises too high and
2) Allow analytic corrections to the data to be made, if necessary, because of the increase of detector active volume caused by the continued lithium drift.

Detector Resolution Noise Monitor

Although the resolution of the detectors varies directly as a function of temperature, one failure mode of the detector results in a degradation of resolution which is independent of temperature. Therefore, a detector resolution (noise) monitor is required for each of the five detectors.

The detector noise monitors have been built into each of the EPS instruments. This approach eliminates any requirement to disconnect the instrument from the spacecraft to exercise and monitor the status of the detector resolution prior to launch. Instead, this measurement may be made by having spacecraft power applied to the EPS and interpreting the data fed out by the spacecraft telemetry system. Correction factors can also be applied to the flight data if required, by monitoring the detector resolution during flight.

Detector Leakage Current

The leakage current measurement provides a partial indication of the quality of the detector. Although leakage current varies directly with temperature, one particular failure mode of the detectors is that the leakage current can increase to prohibitive levels independent of the detector temperature. Therefore, a leakage current monitor is provided in the EPS for each detector.

Electronic Status Monitors

All voltages, electronics package temperature, and heater ON-OFF status are also monitored as part of the housekeeping data, and are necessary parameters for overall evaluation of the instrument prior to launch. All have redundant channels on the multiplexer. The voltage monitor data is especially helpful in evaluating malfunctions or questions relating to data validity in case unusual data occurs. Package temperature data is required in evaluating thermal design and in determining the environment experienced by the electronic circuitry, especially if the instrument power has been off for long periods in a cold, or hot environment. The heater monitor provides status of the heaters, whether in the "On" or "Off" condition. All housekeeping monitor voltages are conditioned to have a maximum value of 5 volts.

TABLE I. EPS DATA PROCESSOR HOUSEKEEPING SEQUENCE PARAMETER RANGE, ACCURACY, AND RESOLUTION CHART

PRIME FRAME NO.	HOUSE-KEEPING ID BIT 2	ID BIT 3	MEASUREMENT	RANGE	ACCURACY	RESOLUTION
1A	0	0	Package Temperature	-50°C to +50°C	±1.0°C	0.110°C
2A	0	0	Detector 1 Noise	0 to 100 keV	±10 keV	1.0 keV
3A	0	0	Detector 1 Leakage	0.05 A to 20 µA	±.05 µA	0.02 µA
4A	0	0	Detector Plate Temp	-50°C to +50°C	±1.5°C	0.110°C
5A	0	1	Detector 2 Noise	0 to 100 keV	±10 keV	1.0 keV
6A	0	1	Detector Leakage	0.05 A to 20 µA	±.05 µA	0.02 µA
7A	0	1	+5 Volt Monitor	0 volts to +10 volts	±5 mv	10 mv
8A	0	1	Detector 3 Noise	0 to 100 keV	±10 keV	1.0 keV
9A	1	0	Detector 3 Leakage	0.05 A to 20 µA	±.05 µA	0.02 µA
10A	1	0	+8 Volt Monitor	0 volts to +10 volts	±5 mv	10 mv
11A	1	0	-8 Volt Monitor	0 volts to -10 volts	±50 mv	10 mv
12A	1	0	+25 Volt Monitor	0 volts to +55 volts	±27 mv	54 mv
13A	1	1	350 Volt Monitor	0 volts to 505 volts	±250 mv	500 mv
14A	1	1	-15 Volt Monitor	0 volts to -20 volts	±100 mv	20 mv
15A	1	1	-5 Volt Monitor	0 volts to -10 volts	±50 mv	10 mv
16A	1	1	Discrim. Ref. Mon.	0 V to 6.002 V	±3 mv	6 mv
1B	0	0	Package Temperature	-50°C to +50°C	±1.5°C	0.110°C
2B	0	1	Detector 4 Noise	0 to 100 keV	±10 keV	1.0 keV
3B	1	0	Detector 4 Leakage	0.05 A to 20 µA	±.05 µA	0.02 µA
4B	1	1	Detector Plate Temp	-50°C to +50°C	±1.5°C	0.110°C
5B	0	0	Detector 5 Noise	0 to 100 keV	±10 keV	1.0 keV
6B	0	1	Detector 5 Leakage	0.05 A to 20 µA	±.05 µA	0.02 µA
7B	1	0	+5 Volt Monitor	0 volts to +10 volts	±5 mv	10 mv
8B	1	1	Heater Monitor	On/Off	--	--
9B	0	0	Heater Monitor	On/Off	--	--
10B	0	1	+8 Volt Monitor	0 volts to +10 volts	±5 mv	10 mv
11B	1	0	-8 Volt Monitor	0 volts to -10 volts	±50 mv	10 mv
12B	1	1	+25 Volt Monitor	0 volts to +55 volts	±27 mv	54 mv
13B	0	0	350 Volt Monitor	0 volts to 505 volts	±250 mv	500 mv
14B	0	1	-15 Volt Monitor	0 volts to -20 volts	±100 mv	20 mv
15B	1	0	-5 Volt Monitor	0 volts to -10 volts	±50 mv	10 mv
16B	1	1	Discrim. Ref. Mon.	0 V to 6.0020 V	±3 mv	6 mv

3.3.1 DETECTOR LEAKAGE MONITOR

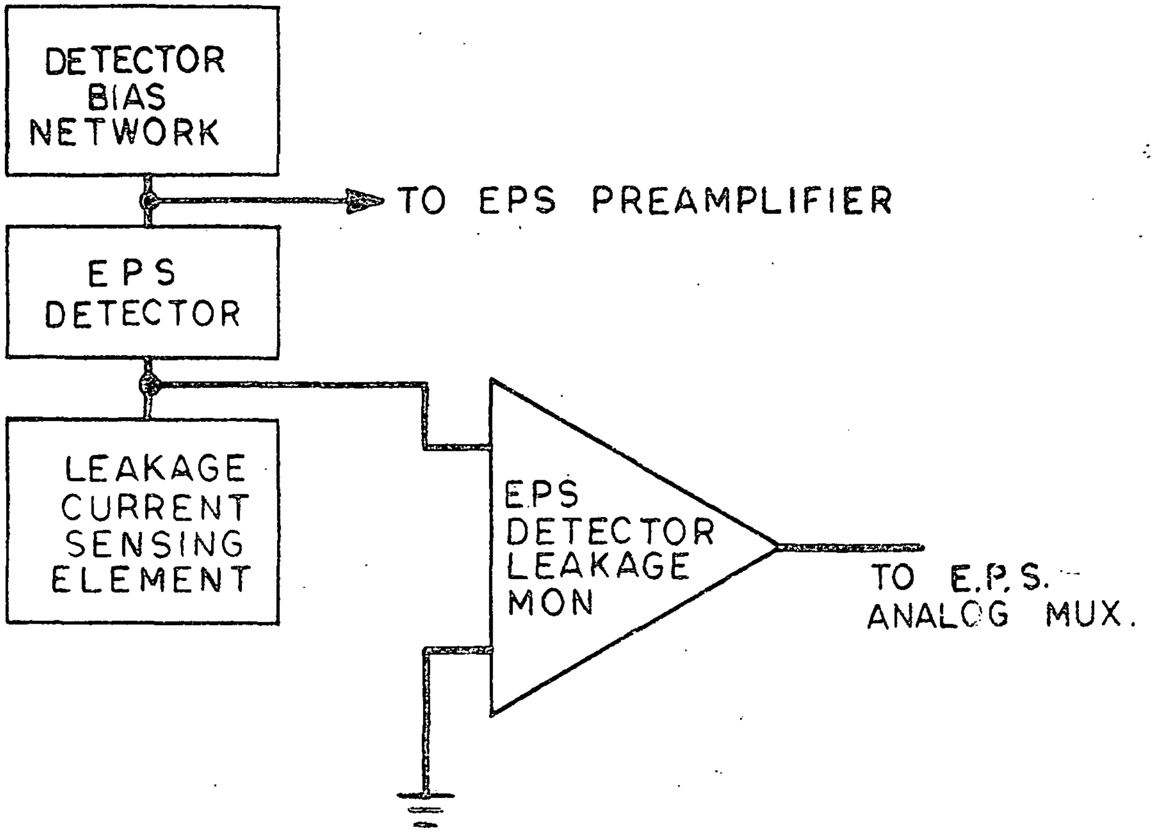
The EPS Detector Leakage Monitor provides a means of continually measuring the leakage current through the silicon energy sensing detector by amplifying the voltage drop across a resistor placed in series with the detector, as illustrated in the accompanying block diagram.

The Detector Leakage Current Monitor consists of a single gain stage utilizing a highly stable operational amplifier. This amplifier, LM 108/883, was specifically chosen because of its extremely low bias current (< 1nA) and offset characteristics (< .5mV).

The monitor is capable of responding to a current variation equal to 1/1000 of the maximum predicted current through the detector and still outputting a voltage equivalent to the least significant bit of the EPS A-D Converter (5 mV).

Both inputs of the amplifier are protected by using two series resistors, R_{12} and R_{16} as shown on Schematic SIC39106631.

The amplifier's output has built-in protection; a short circuit of its output to ground for any length of time will cause no damage to the IC.



DETECTOR LEAKAGE MONITOR BLOCK DIAGRAM

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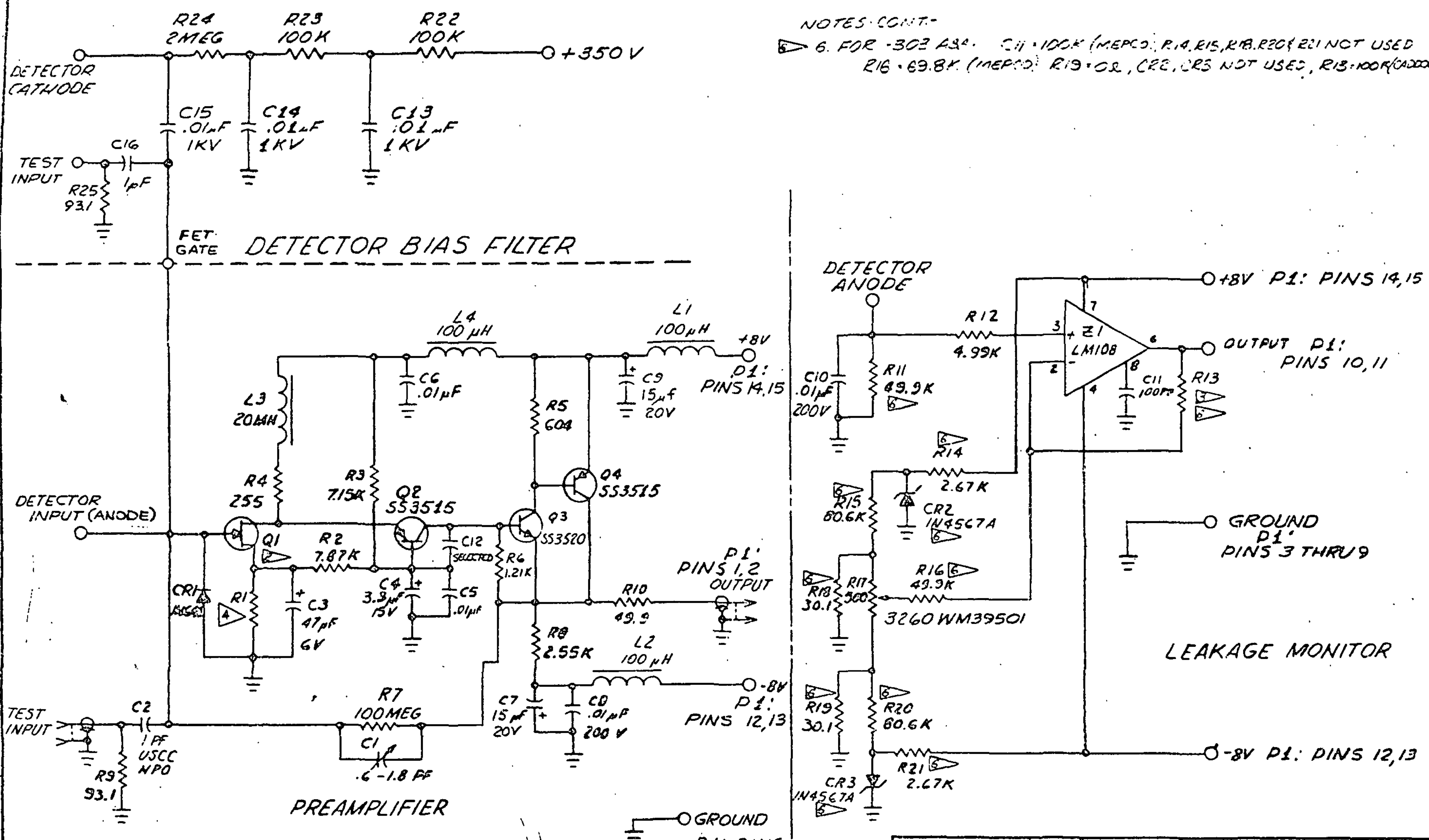
A		ADDED [illegible]	[illegible]	[illegible]	[illegible]



NOTES CONT-

6. FOR -303 ASSY. C11 = 100K (MEPCO) R14, R15, R18, R20 & 21 NOT USED
R16 = 69.8K (MEPCO) R19 = 0Ω, CR2, CR3 NOT USED, R13 = 100R (CADDOCK)

NOTES: UNLESS OTHERWISE SPECIFIED.

1. INTERPRET PER MSC MANUAL MSCM8600.
2. Q1 SELECTED SSC6113
3. FOR 1μA INPUT R13 = 5.0 MEG. FOR 2μA INPUT R13 = 2.5 MEG. CADDOCK MK-132
4. SELECTED, DEPENDENT UPON Q1.
5. ALL RESISTORS ARE RNC50 EXCEPT: R4; R8 (RNC55) AND R22 - R24 (CADDOCK MK-132)

-CONT-

SIGNATURES	DATE
DR	3-22-71
ENG	5/25/71
CH	3-23-71
	5-21-71
APP PRE-RELEASE R.P.	8/13/71
AUTH	

ELECTRON-PROTON SPECTROMETER

NATIONAL AERONAUTICS & SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER · HOUSTON, TEXAS

SCHEMATIC, PREAMPLIFIER & DETECTOR LEAKAGE MONITOR

ELECTRON-PROTON SPECTROMETER

CODE IDENT NO.	SIZE	DWG NO.
21356	C	SIC 39106631
SCALE —	150 - EB	SHEET

MSC Form 1610 C (REV OCT 66)

Power supply voltage changes have little effect on the monitor's output. A power supply change of ± 1 V results in a change of ± 1 mV at the output.

DETECTOR LEAKAGE MONITOR SPECIFICATION

1. Maximum Input Current Range:

   20 μA Full Scale

2. Maximum Output Voltage into Multiplexer:

   5.0 volts

3. Amplifier Non-Inverting DC Voltage Gain

   2.43 Volt/Volt

4. Amplifier Output Drift with Temperature:

   Less than .5 mV/°C

5. Equivalent Input Current Drift with Temperature:

   Less than .1 nA/°C

6. Transfer Characteristics: $\Delta V_{out}/\Delta I_{in}$

   250 mV/μA

7. Output Signal Power Supply Rejection:

   ΔV_{out} less than 1 mv for $\Delta V_{supply} = \pm 1.0$ volt

8. Load Driving Capacility: 1.3 mA maximum into 10KΩ load.

9. Power Requirements:

   +8.1 volts at 1.0 mA maximum
   -8.1 volts at 1.0 mA maximum

3.3.2 DETECTOR RESOLUTION MONITOR

The EPS Detector Resolution Monitor provides a means of continually measuring the noise derived from the EPS detectors. Thus allowing one to evaluate any degradation of the detectors which might occur during storage or during flight.

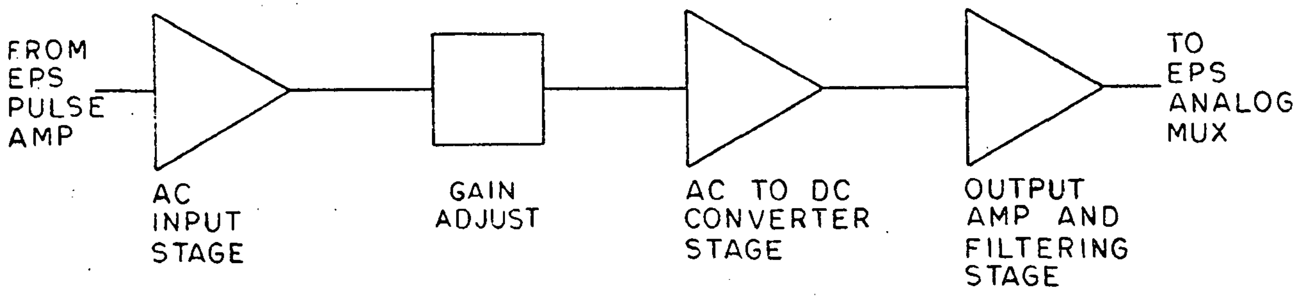
The resolution monitor senses this noise at the output of the EPS pulse amplifier and transforms it into a proportional DC voltage which is fed into the EPS multiplexer as shown in the accompanying block diagram.

The EPS Detector Resolution Monitor averages the input noise and is implemented with three high performance operational amplifiers. It is capable of responding to high frequency noise signals, having a 3 dB bandwidth of 300 KHz.

Two hot carrier diodes, CR_3 and CR_4, shown on Schematic SIC39106633, are used as the rectifying Detector Resolution Monitor elements in the monitor's second stage because of their inherent low threshold voltages.

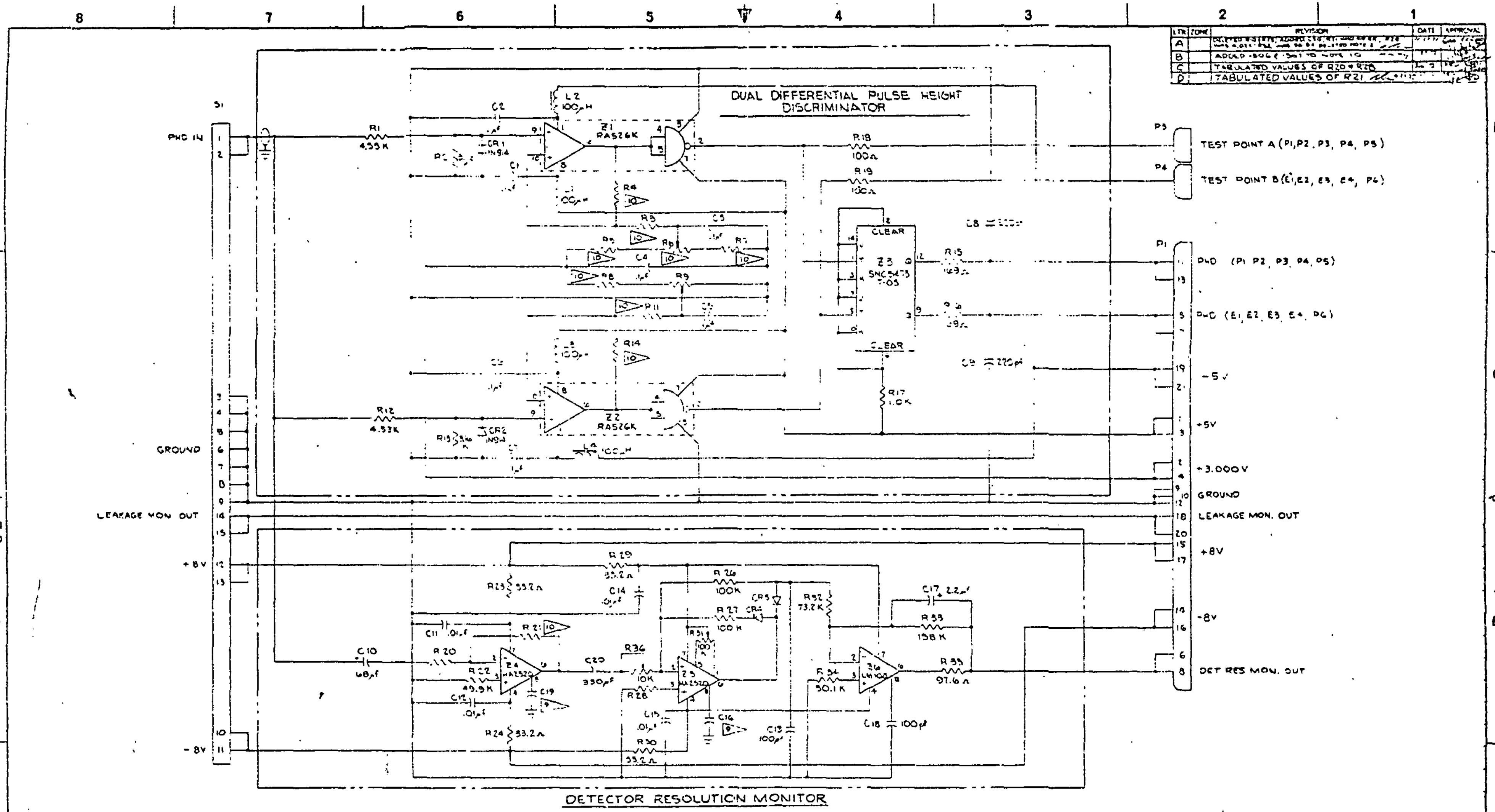
The transfer function will be represented by a fourth order equation relating preamplifier input resolution in keV and resolution monitor output voltage in volts dc.

The coefficients of this equation shall be determined during testing and calibration of the resolution monitor cards.



DETECTOR RESOLUTION MONITOR BLOCK DIAGRAM

LTR	ZONE	REVISION	DATE	APPROVAL
A		[illegible]	[illegible]	[illegible]
B		ADDED [illegible] TO NOTE 10	[illegible]	[illegible]
C		TABULATED VALUES OF R20 & R28	[illegible]	[illegible]
D		TABULATED VALUES OF R21		[illegible]



DETECTOR RESOLUTION MONITOR

DETECTOR REFERENCE	R21'	R3'	R4[2]	R5'	R6	R7'	R8'	R9	R20	R11'	R14[1]	R28
A	100K	1.54K	500K	150Ω	200Ω	464Ω	2.10K	50Ω	49.9K	1.82K	725K	1.100K
B	100K	1.47K	440K	715Ω	"	604Ω	"	"	"	"	"	"
C	100K	1.50K	480K	787Ω	"	487Ω	"	"	"	"	"	"
D	100K	1.54K	550K	1.00K	"	294Ω	"	"	"	"	"	"
E	100K	"	550K	1.13K	100Ω	267Ω	1.69K	200Ω	49.9K	1.78K	750K	1.100K
A-D(-30°)	36.5K	1.54K	100K	1.18K	200Ω	69.8Ω	2.10K	50Ω	4.99K	1.82K	725K	0Ω
E (-30°)	36.5K	1.54K	100K	1.18K	200Ω	69.8Ω	1.69K	200Ω	4.99K	1.78K	750K	0Ω

NOTES: UNLESS OTHERWISE SPECIFIED.

1. INTERPRET PER MSC MANUAL MSCM 8500.
2.
3. 'MEPCO RNC 50H FR.
4. 'CADDOCK MK-132 (±1%, ±50ppm/°C).
5. 'BOURNS 3260HM39101
6. 'BOURNS 3260HM39500
7. 'BOURNS 3260HM39201
8. CR3 & CR4 ARE H P P/N 5082-2123
9. C14 & C19 ARE TO BE SELECTED DURING TEST.

SIGNATURES	DATE
DR E. E. LOPEZ	8-11-71
ENG [illegible]	8-16-71
CH E. [illegible]	8-16-71
R. R. [illegible]	8-16-71
APP	
AUTH	

ELECTRON-PROTON SPECTROMETER

NATIONAL AERONAUTICS & SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER · HOUSTON, TEXAS

SCHEMATIC DIAGRAM,
DUAL DIFFERENTIAL PULSE HEIGHT
DISC AND DETECTOR RESOLUTION
MONITOR — E.P.S

CODE IDENT NO 21356
SIZE D
DWG NO SKC 39106633
SCALE ~
SHEET

The output stage can be short circuited to ground indefinitely and the overall circuit may be overloaded to any extent, without any damage being incurred by the components.

Power supply voltage changes have little effect on the monitor's output response; A ± 1 volt power supply change results in less than 10 mV output voltage change.

DETECTOR RESOLUTION MONITOR
SPECIFICATION

1. Overall Noise Gain:

The response curve slope can be adjusted to produce 25 mV dc at the output of the resolution monitor per keV of detector noise at the input of the preamplifier.

Maximum nominal output corresponds to 200 keV of preamplifier input resolution.

2. Minimum Input Sensitivity:

Approximately 5.5 keV.

3. Input Resolution Transfer Equation:

The transfer function will be represented by a fourth order equation relating preamplifier input resolution in keV and resolution monitor output voltage in volts dc.

The coefficients of this equation shall be determined during testing and calibration of the resolution monitor cards.

4. Resolution Monitor Signal Bandwidth (-3 db): 300 KHz.

5. Resolution Monitor Input Impedance: 5 KΩ in series with 68 μF.

6. Power Requirements: ±8.1 volts at 10 mA.

3.3.3 TEMPERATURE MONITORS (DETECTOR AND PACKAGE)

The EPS Temperature Monitors provide a means of accurately measuring the temperature surrounding the detectors and electronic hardware in the range between -50°C to +50°C.

The temperature sensors are the PNP transistors which are biased in their linear region by the resistive bias network as shown on the Block Diagram.

The transistor DC collector voltage is a linear function of the emitter-to-base junction voltage and its variation with temperature.

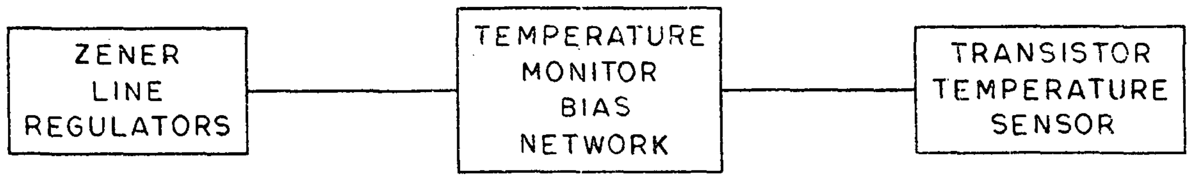
The temperature monitor response curve is a straight line given by:

$$V_o = 2,500 + 50 \times T \quad (\mathrm{mV})$$

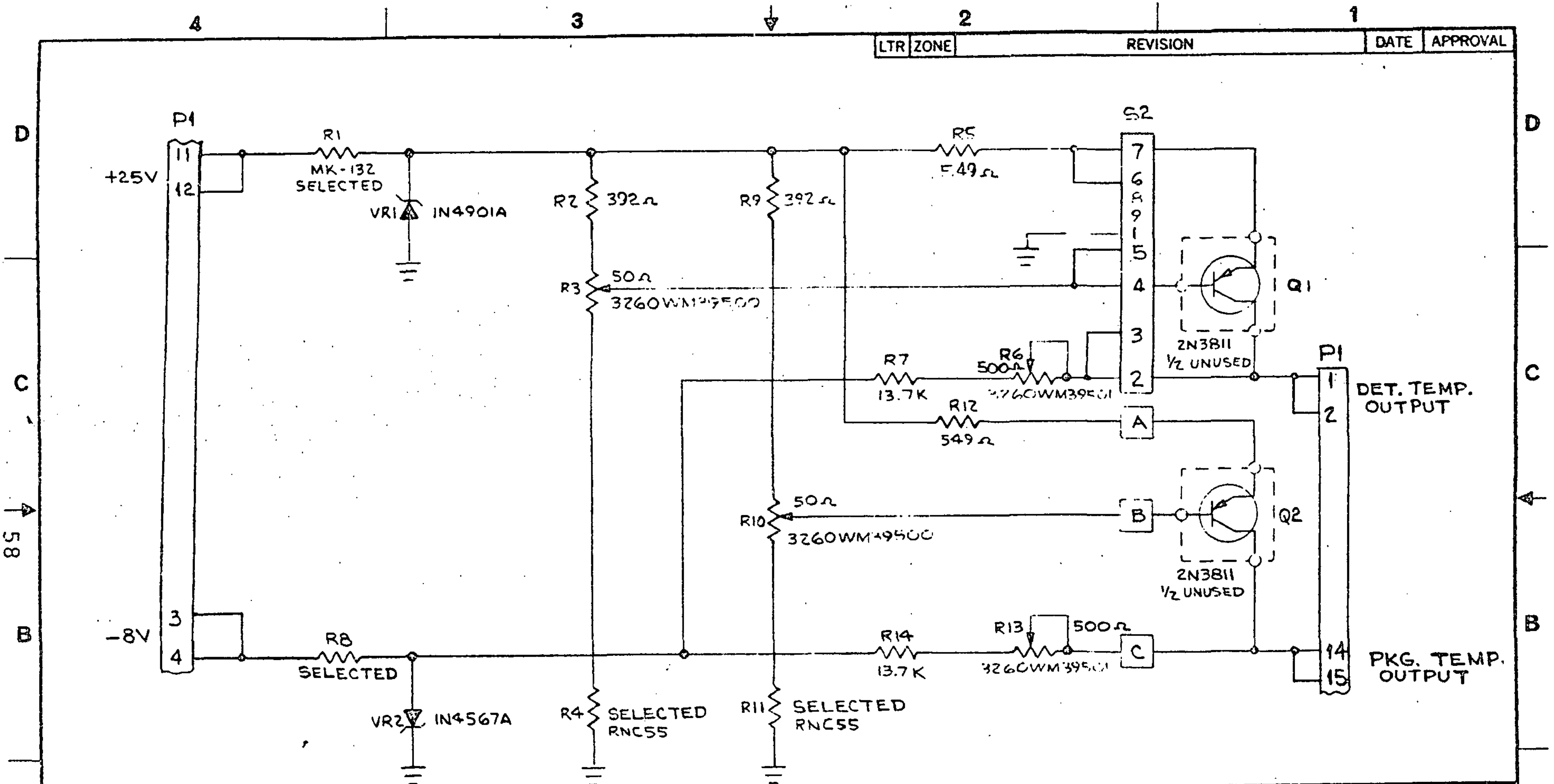
Where T is in °C.

The response curve slope and intersept can be trimmed by adjusting R_3 (R_{10}) and R_6 (R_{13}) Potentiometers shown on Schematic SIC39107145.

In order to increase the circuit's ability to reject power supply variations, two zener diodes, VR_1 and VR_2, which are temperature compensated, are used to regulate the positive and negative supply voltages.



TEMPERATURE MONITOR BLOCK DIAGRAM



NOTES - UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE RNC50.
2. COMPONENTS ENCLOSED WITH BROKEN LINES ARE EXTERNALLY MOUNTED.

SIGNATURES	DATE
DR	4-8-71
ENG	4-8-71
CH	4-8-71
PRE-RELEASE R.P.D.	8/13/71
APP	
AUTH	

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER · HOUSTON, TEXAS

SCHEMATIC - TEMERATURE MONITORS

CODE IDENT NO.	SIZE	DWG NO.
21356	B	SIC39107145

SCALE — E. P. S. SHEET 1

PACKAGE AND DETECTOR TEMPERATURE MONITORS SPECIFICATION

1. Temperature Range: -50°C to +50°C

2. Output Voltage Range: 0.0 to +5.0 Volts

3. Output Voltage Temperature Sensitivity: 50 mV/°C.

4. Worst Case Accuracy: ±1.5°C.

5. Resolution: (.1°C)

6. Power Requirements:

   +25 volts at 8.5 mA
   -8.1 volts at 2.5 mA
   Total power dissipation: 234 mw

3.3.4 VOLTAGE MONITORS

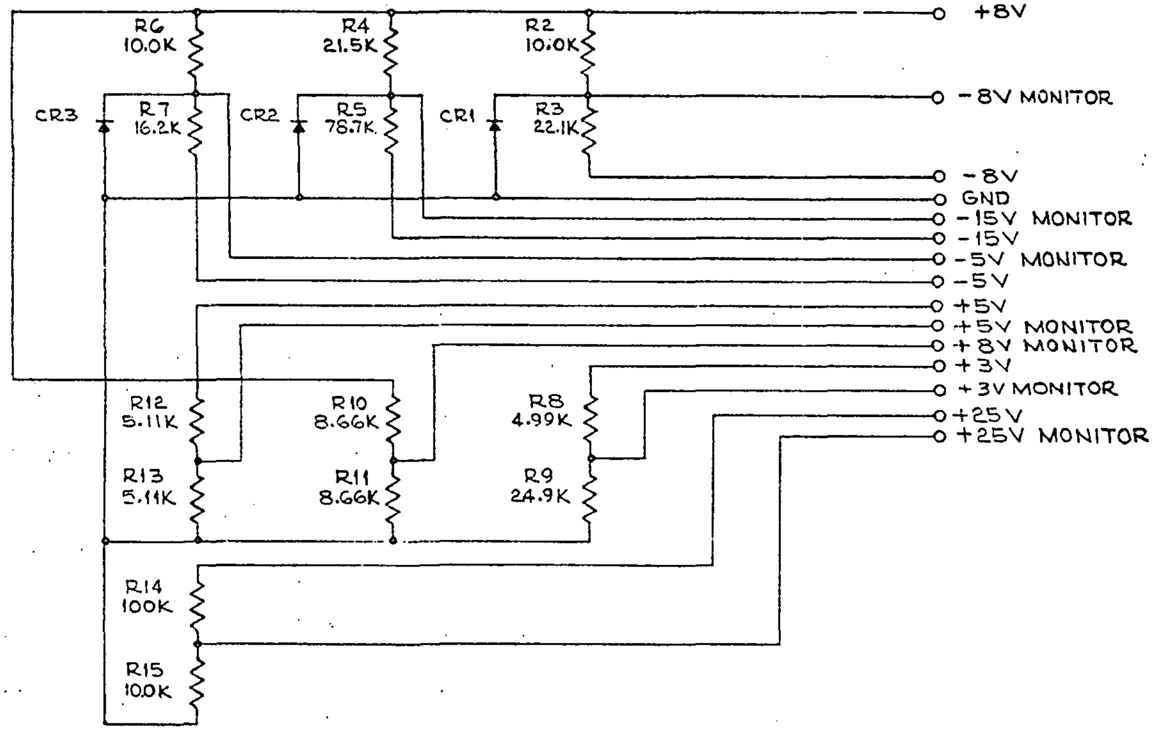
As an aid in troubleshooting the instrument in the event of a failure and to determine the operational status during flight, the internal voltages utilized by the EPS are monitored and read out thru the telemetry link.

There are seven separate low voltages within the EPS instrument, four positive and three negative. As shown in the monitor module Schematic Diagram SIC39106643 the monitor outputs for the positive voltages are generated by resistive divider networks referenced to signal ground.

To generate the monitor signals for three negative voltages, the resistive dividers cannot be referenced to signal ground since the EPS multiplexer cannot multiplex a negative voltage. For this reason, these networks are tied to the +8 voltage supply, and the resistor values were selected to give positive voltages proportional to the negative voltages. The diodes attached to the negative voltage monitor outputs ensure that large negative voltages will not be applied to the input of the multiplexers.

The relationships for the various voltage monitors are:

+8 volt monitor: $V_{mon}\ (+8) = 0.5\ V_8$
+5 volt monitor: $V_{mon}\ (+5) = 0.5\ V_5$
+3 volt monitor: $V_{mon}\ (+3) = 0.833\ V_3$
+25 volt monitor: $V_{mon}\ (+25) = 0.091\ V_{25}$
-8 volt monitor: $V_{mon}\ (-8) = 0.688\ V_8 - 0.312\ V_{-8}$
-5 volt monitor: $V_{mon}\ (-5) = 0.618\ V_8 - 0.382\ V_{-5}$
-15 volt monitor: $V_{mon}\ (-15) = 0.785\ V_8 - 0.215\ V_{-15}$



NOTES: UNLESS OTHERWISE SPECIFIED.

1. INTERPRET PER MSC MANUAL MSCM 8500.

2. RESISTORS ARE TYPE RNR50, 1/20W; DIODES ARE JANTX 1N914.

SIGNATURES	DATE
DR Bill L. Bell	6-17-71
ENG G. L. [illegible]	9-19-71
CHK J D STRINGER	6-29-71
PRE-RELEASE: R.P. Dunn	8/13/71
APP	
AUTH	
EPS	

NATIONAL AERONAUTICS & SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER · HOUSTON, TEXAS

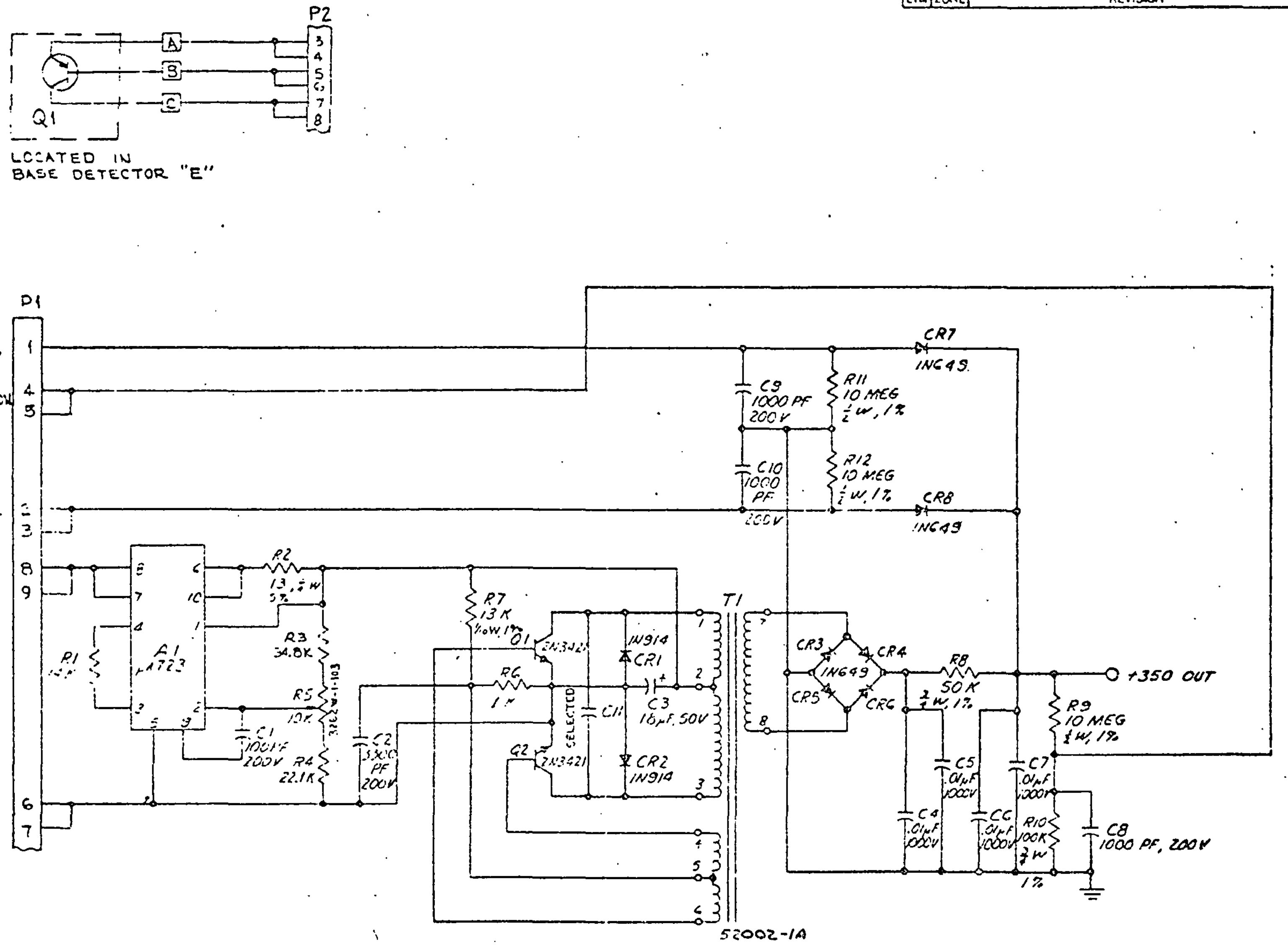
SCHEMATIC DIAGRAM
MONITOR MODULE, DATA PROCESSOR
EPS

CODE IDENT NO.	SIZE	DWG NO.
21356	C	SIC39106643
SCALE ~	ISD-EB	SHEET 1

3.3.5 DETECTOR BIAS MONITOR SCHEMATIC SIC39106638

The status of the detector bias power supply is determined by the +350 volt monitor which is part of the housekeeping data. The voltage monitor resolution is 500 millivolts. Resistors R9 and R10 shown on drawing SIC39106638 set the voltage monitor output to 3.5 volts.

LTR	ZONE	REVISION	DATE	APPROVAL



NOTES: UNLESS OTHERWISE SPECIFIED.

1. INTERPRET PER MSC MANUAL MSCM8500.
2. ALL RESISTORS 1/20 W, 1%, VALUES IN OHMS.

SIGNATURES	DATE
DR	3-30-71
ENG	4-8-71
CHK	
R.P. Dunn	
APP	
AUTH	

ELECTRON - PROTON SPECTROMETER

NATIONAL AERONAUTICS & SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER · HOUSTON, TEXAS

SCHEMATIC DIAGRAM,
DETECTOR BIAS SUPPLY-
ELECTRON-PROTON SPECTROMETER

CODE IDENT NO.	SIZE	DWG NO
21356	C	SIC39106638

SCALE ~ ISD-EB SHEET

3.3.6 HEATER CONTROL MONITOR

A buffered output from the schmitt trigger in the heater control circuit is fed to the data processor to provide the on or off status of heaters Schematic SIC39106639.

3.4 DATA PROCESSOR SYSTEM

The data processor is required to digitize all data and present it in the correct format and time to the telemetry system. The data must be identified so that after shutdown periods, specific data channels may be quickly recognized.

The data processor section is composed of seventeen modules mounted on a common motherboard. A pictorial view is shown in Fig. 1. The module breakdown is as follows:

Counter-Register	10 ea.
Sequence Control, Line Receiver, Counter Control	1 ea.
Data Compressor and Internal Clock	1 ea.
Output Buffer and Word Sync Generator	1 ea.
Analog - Digital Converter	1 ea.
A/D Control	1 ea.
Multiplexer	1 ea.
Monitor Module	1 ea.

The data processor block diagram is shown in Figure 2. Major interconnect lines are shown and identified to show the functional relationship between modules.

The data processor power requirement is as follows:

Voltage	Current	Power
+5	620 ma	3100 mW
-5	2.5 ma	12.5 mW
+8	7.5 ma	60 mW
-8	42 ma	336 mW
-15	1.8 ma	27 mW
	Total	3535 mW

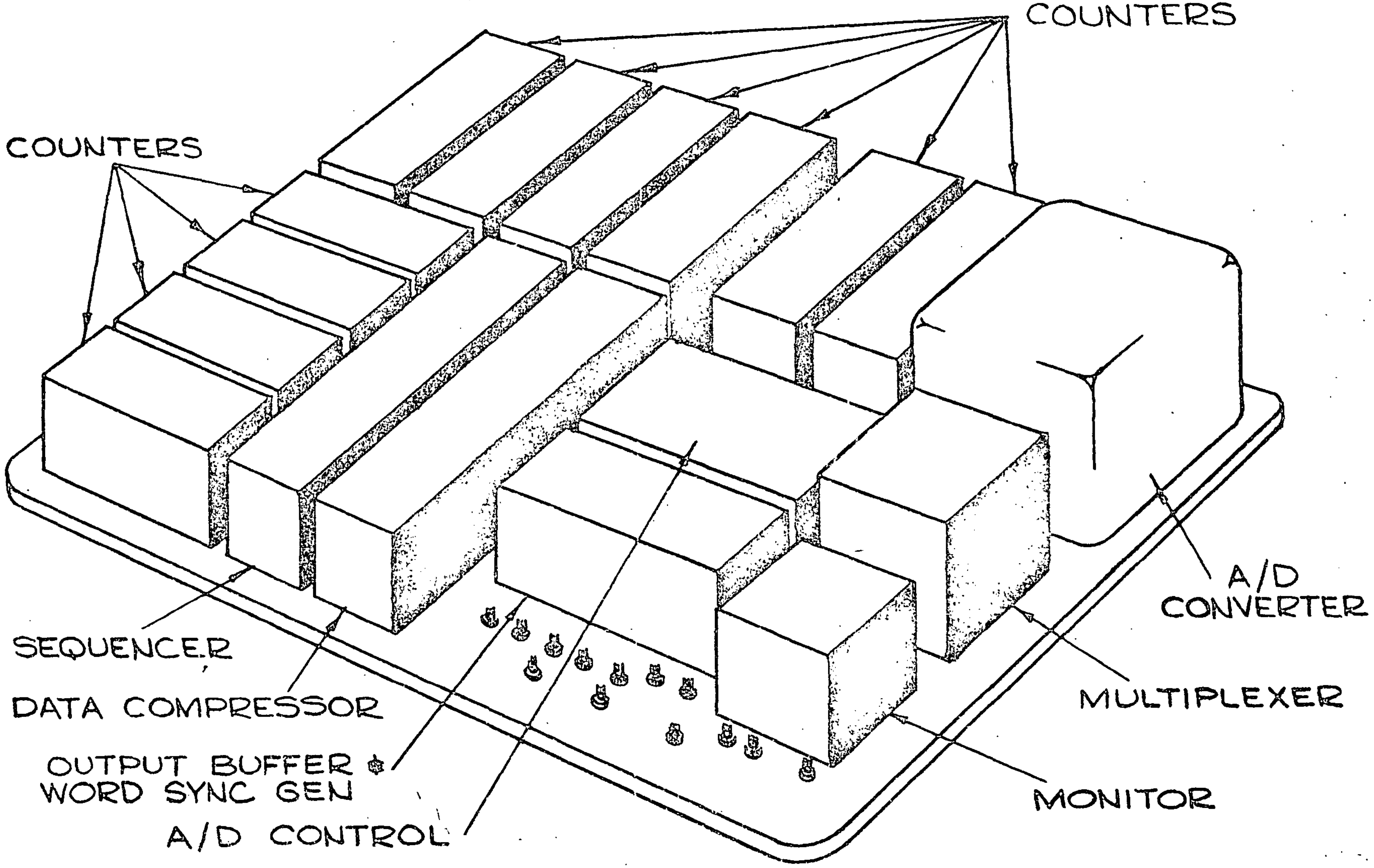


Figure 1 DATA PROCESSOR MOTHER BOARD

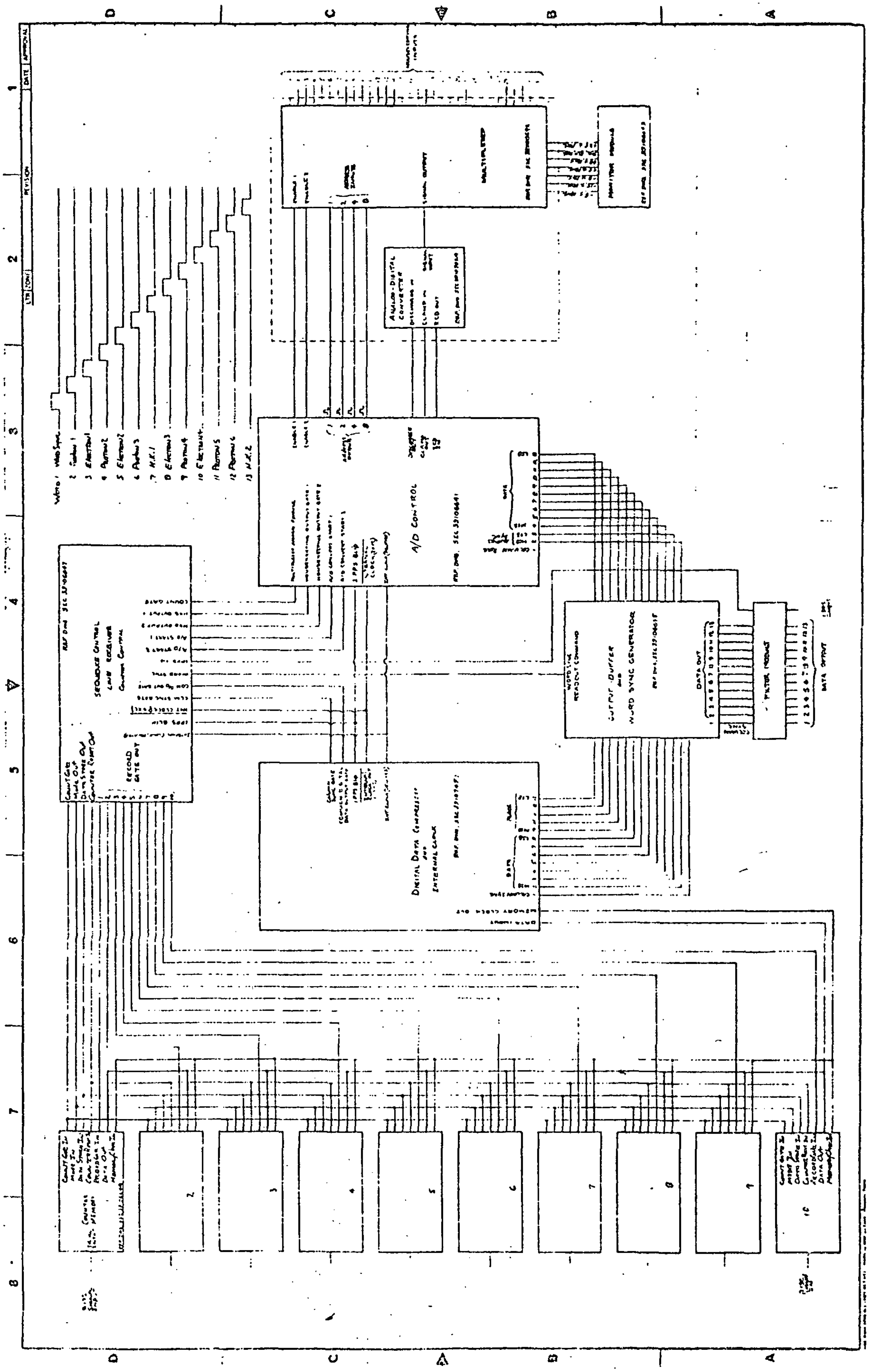


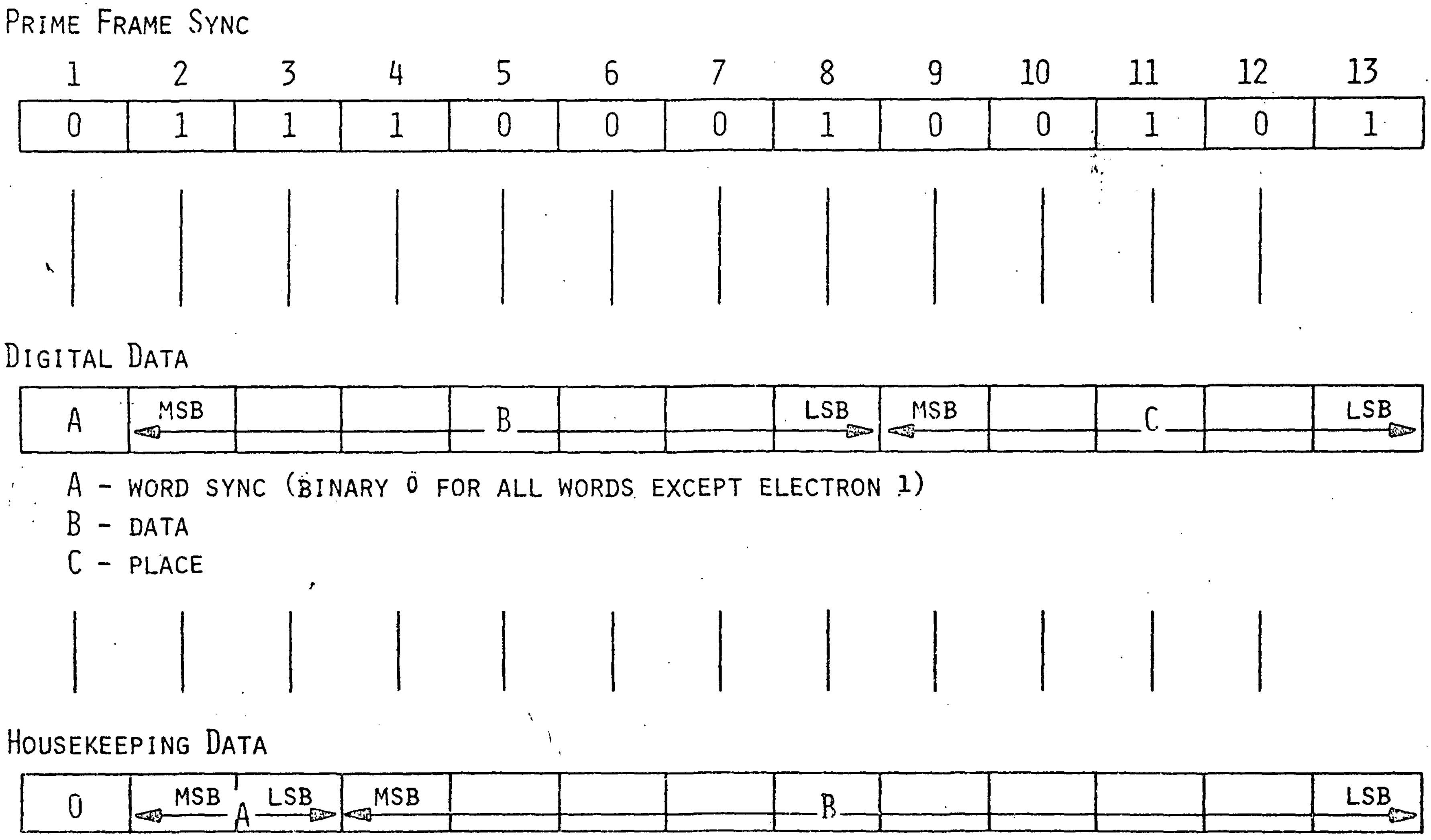
Figure 2 DATA PROCESSOR BLOCK DIAGRAM

There are ten channels of detector information, plus twenty-one sources of housekeeping information. This data is processed and formated to be read out on 13 data lines which are sampled 1 time per second. The EPS Word Format and Main Frame Format are shown in Figure 3 and 4 respectively. All timing sequences are referred to a single clock pulse of one Hertz, which is fed to the instrument from the CSM. This one Hertz timing signal is referred to in the interface control document Number MH04-02119-234 as the CTE timing signal.

The major events and related timing is shown in the timing diagram, Figure 5.

The data processor operates properly from -50°C to +70°C. All digital circuits operate properly over this temperature while V_{cc} is varied from 4.6 volts to 5.3 volts. The digital circuits are Texas Instrument low power T^2L logic, except for four standard power packages where more drive capability is required. There are also four low power one-shot packages from Advanced Micro, and one comparator from National.

EPS WORD FORMAT



A - WORD SYNC (BINARY 0 FOR ALL WORDS EXCEPT ELECTRON 1)
B - DATA
C - PLACE

A - HOUSEKEEPING SYNC
B - DATA

Figure 3 EPS WORD FORMAT

EPS MAIN FRAME

WORD LOCATION →

PRIME FRAME NUMBER	1	2	3	4	5	6	7	8	9	10	11	12	13
1	PRIME FRAME SYNC	DET 1 ELEC	DET 1 PROT	DET 2 ELEC	DET 2 PROT	DET 3 ELEC	HOUSE KPG 1A	DET 3 PROT	DET 4 ELEC	DET 4 PROT	DET 5 PROT	DET 5 PROT	HOUSE KPG 1B
2	↓	↓	↓	↓	↓	↓	2A	↓	↓	↓	↓	↓	2B
3	↓	↓	↓	↓	↓	↓	3A	↓	↓	↓	↓	↓	3B
4	↓	↓	↓	↓	↓	↓	4A	↓	↓	↓	↓	↓	4B
5	↓	↓	↓	↓	↓	↓	5A	↓	↓	↓	↓	↓	5B
6	↓	↓	↓	↓	↓	↓	6A	↓	↓	↓	↓	↓	6B
7	↓	↓	↓	↓	↓	↓	7A	↓	↓	↓	↓	↓	7B
8	↓	↓	↓	↓	↓	↓	8A	↓	↓	↓	↓	↓	8B
9	↓	↓	↓	↓	↓	↓	9A	↓	↓	↓	↓	↓	9B
10	↓	↓	↓	↓	↓	↓	10A	↓	↓	↓	↓	↓	10B
11	↓	↓	↓	↓	↓	↓	11A	↓	↓	↓	↓	↓	11B
12	↓	↓	↓	↓	↓	↓	12A	↓	↓	↓	↓	↓	12B
13	↓	↓	↓	↓	↓	↓	13A	↓	↓	↓	↓	↓	13B
14	↓	↓	↓	↓	↓	↓	14A	↓	↓	↓	↓	↓	14B
15	↓	↓	↓	↓	↓	↓	15A	↓	↓	↓	↓	↓	15B
16	PRIME FRAME SYNC	DET 1 ELEC	DET 1 PROT	DET 2 ELEC	DET 2 PROT	DET 3 ELEC	16A	DET 3 PROT	DET 4 ELEC	DET 4 PROT	DET 5 PROT	DET 5 PROT	16B

← 13 SECONDS →

MAIN FRAME = 208 SECONDS

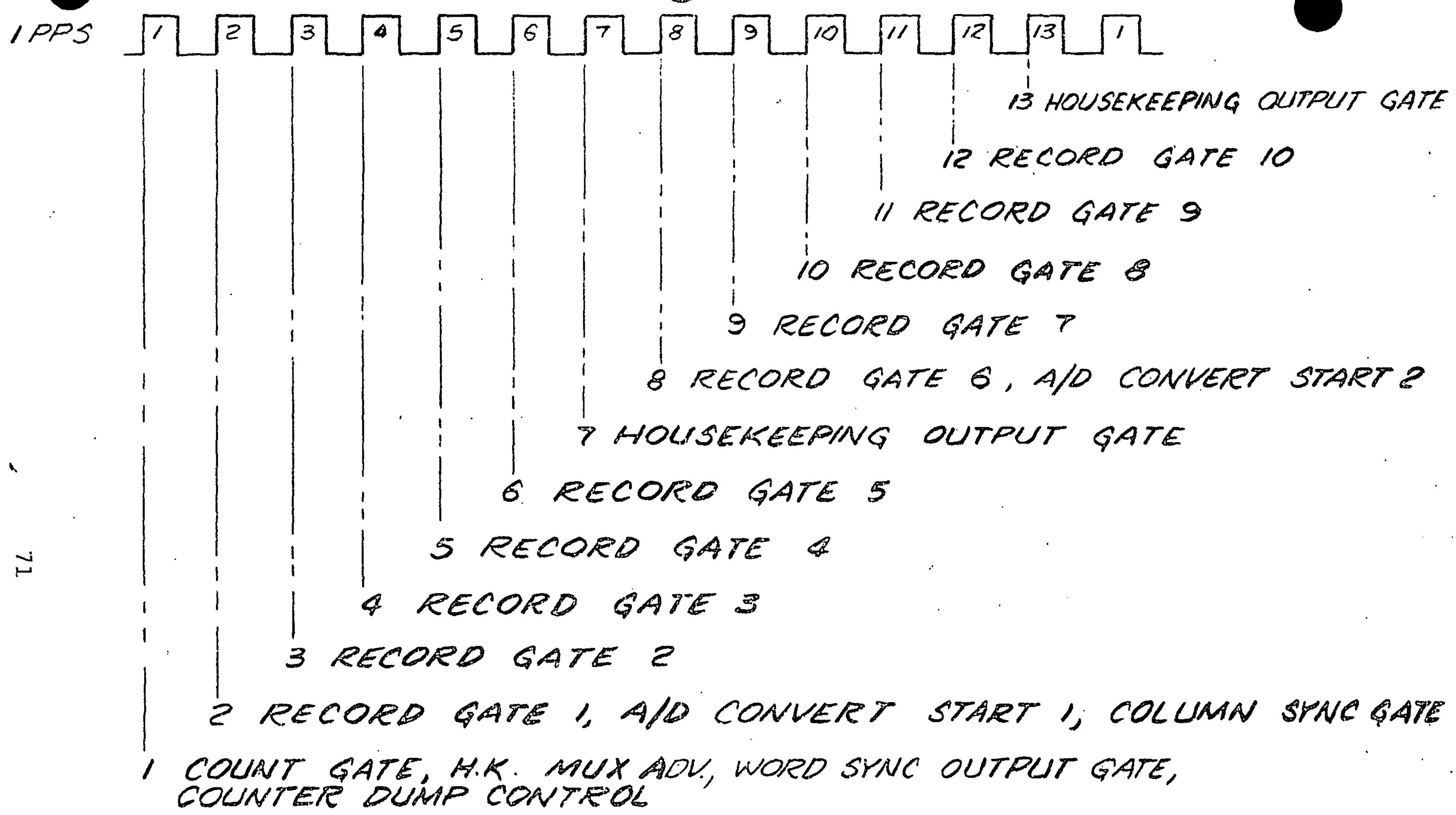


Figure 5 . TIMING DIAGRAM - WORD SEQUENCE/EVENTS

GENERAL DATA PROCESSOR SPECIFICATION

The EPS Data Processor consists of a sequence controller, ten counter registers, a digital data compressor, an analog to digital converter, A/D control, a 32 channel analog multiplexer and a parallel output buffer. The spacecraft information interface consists of thirteen bilevel data lines and one synchronizing command line. The thirteen bilevel lines are sampled, in parallel, at a rate of 1 Hz with each sample occurring a minimum of 20 milliseconds after the positive going transition of the 1 Hz synchronizing command. Scientific data accumulation specifications are:

1. Counting Interval - 12 seconds
2. Recording Interval - 13 seconds
3. Fractional Counter Livetime - 92.3%
4. Counter Capacity - $2^{24}-1$ = 16,777,215 events/channel
5. Counting Rate Maximum -2.80 x 10^6 cps/channel for no overflow.
6. Readout Format - floating point binary compression, seven bit data word plus five bit place word.
7. Digital Accuracy - ±0.5% of value

The EPS Housekeeping data accumulation specifications are:

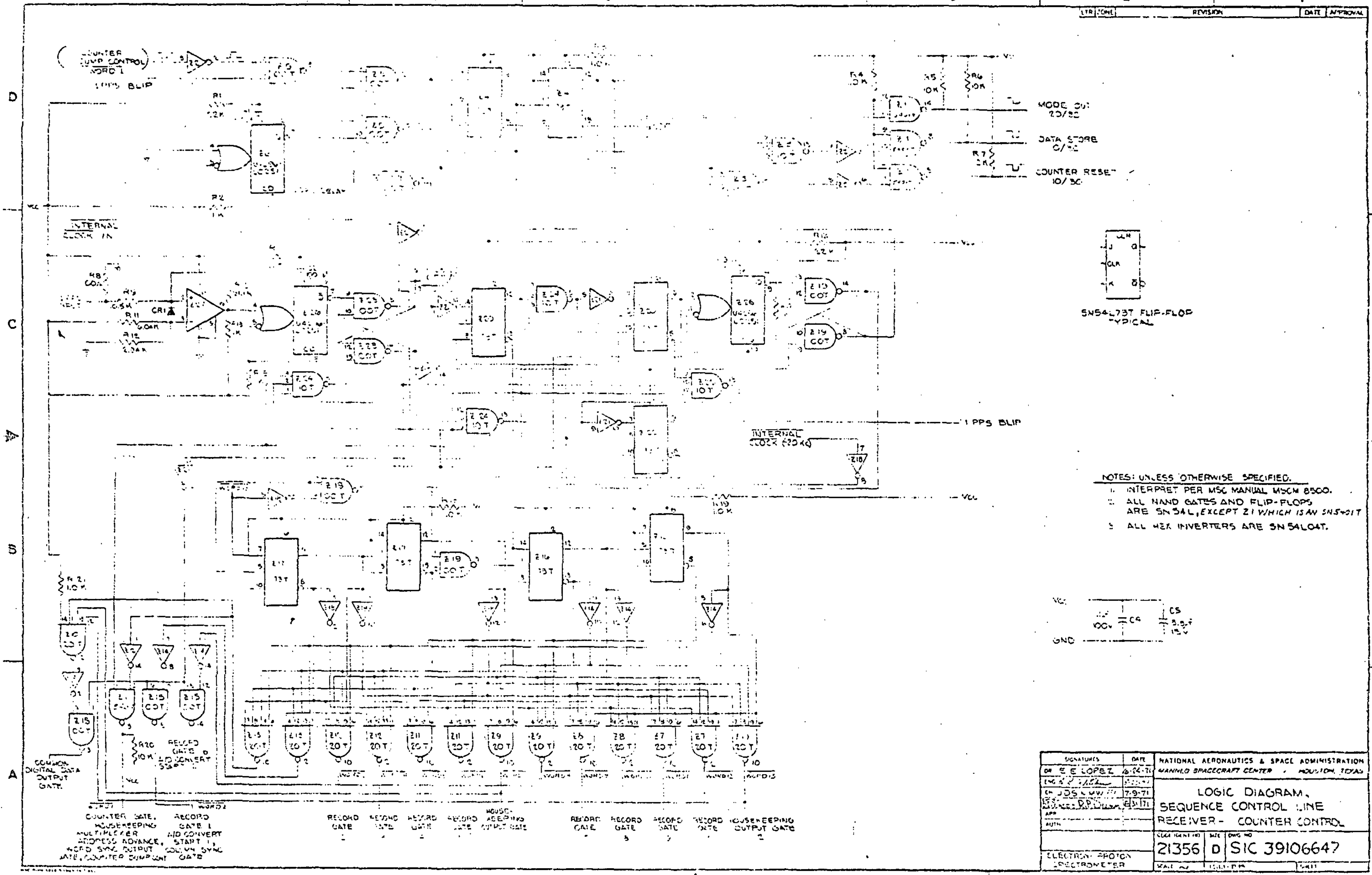
1. Sample Rate - .154/sec
2. Sample Rate Per Channel - .0048/sec
3. Conversion Gain - 10 bits
4. Number of Channels - 32
5. Address, Range, Resolution, Accuracy - See Table I

TABLE I. EPS DATA PROCESSOR HOUSEKEEPING SEQUENCE PARAMETER RANGE, ACCURACY, AND RESOLUTION CHART

PRIME FRAME NO.	HOUSE-KEEPING		MEASUREMENT	RANGE	ACCURACY	RESOLUTION
	ID BIT 2	ID BIT 3				
1A	0	0	Package Temperature	-50°C to +50°C	±1.0°C	0.110°C
2A	0	0	Detector 1 Noise	0 to 100 keV	±10 keV	1.0 keV
3A	0	0	Detector 1 Leakage	0.05 A to 20 µA	±.05 µA	0.02 µA
4A	0	0	Detector Plate Temp	-50°C to +50°C	±1.5°C	0.110°C
5A	0	1	Detector 2 Noise	0 to 100 keV	±10 keV	1.0 keV
6A	0	1	Detector Leakage	0.05 A to 20 µA	±.05 µA	0.02 µA
7A	0	1	+5 Volt Monitor	0 volts to +10 volts	±5 mv	10 mv
8A	0	1	Detector 3 Noise	0 to 100 keV	±10 keV	1.0 keV
9A	1	0	Detector 3 Leakage	0.05 A to 20 µA	±.05 µA	0.02 µA
10A	1	0	+8 Volt Monitor	0 volts to +10 volts	±5 mv	10 mv
11A	1	0	-8 Volt Monitor	0 volts to -10 volts	±50 mv	10 mv
12A	1	0	+25 Volt Monitor	0 volts to +55 volts	±27 mv	54 mv
13A	1	1	350 Volt Monitor	0 volts to 505 volts	±250 mv	500 mv
14A	1	1	-15 Volt Monitor	0 volts to -20 volts	±100 mv	20 mv
15A	1	1	-5 Volt Monitor	0 volts to -10 volts	±50 mv	10 mv
16A	1	1	Discrim. Ref. Mon.	0 V to 6.002 V	±3 mv	6 mv
1B	0	0	Package Temperature	-50°C to +50°C	±1.5°C	0.110°C
2B	0	1	Detector 4 Noise	0 to 100 keV	±10 keV	1.0 keV
3B	1	0	Detector 4 Leakage	0.05 A to 20 µA	±.05 µA	0.02 µA
4B	1	1	Detector Plate Temp	-50°C to +50°C	±1.5°C	0.110°C
5B	0	0	Detector 5 Noise	0 to 100 keV	±10 keV	1.0 keV
6B	0	1	Detector 5 Leakage	0.05 A to 20 µA	±.05 µA	0.02 µA
7B	1	0	+5 Volt Monitor	0 volts to +10 volts	±5 mv	10 mv
8B	1	1	Heater Monitor	On/Off	--	--
9B	0	0	Heater Monitor	On/Off	--	--
10B	0	1	+8 Volt Monitor	0 volts to +10 volts	±5 mv	10 mv
11B	1	0	-8 Volt Monitor	0 volts to -10 volts	±50 mv	10 mv
12B	1	1	+25 Volt Monitor	0 volts to +55 volts	±27 mv	54 mv
13B	0	0	350 Volt Monitor	0 volts to 505 volts	±250 mv	500 mv
14B	0	1	-15 Volt Monitor	0 volts to -20 volts	±100 mv	20 mv
15B	1	0	-5 Volt Monitor	0 volts to -10 volts	±50 mv	10 mv
16B	1	1	Discrim. Ref. Mon.	0 V to 6.0020 V	±3 mv	6 mv

3.4.1 SEQUENCE CONTROL, LINE RECEIVER - COUNTER CONTROL

This module (Schematic SIC39106647) generates the timing sequence for the thirteen word intervals. The one Hertz Clock pulse is used in this module to synchronize all data to the CSM data requirements. The counter control pulses are also generated in this module and are used to start the counter, shift the data from the counters to the registers and reset the counters.



NOTES: UNLESS OTHERWISE SPECIFIED.

1. INTERPRET PER MSC MANUAL MSCM 8500.
2. ALL NAND GATES AND FLIP-FLOPS ARE SN54L, EXCEPT Z1 WHICH IS AN SN5401T
3. ALL HEX INVERTERS ARE SN54L04T.

SIGNATURES	DATE
DR E E LOPEZ	6-24-71
ENG	
CH JDS / MW	7-9-71
D.P.	8-3-71
APP	
AUTH	

ELECTRON- PROTON SPECTROMETER

NATIONAL AERONAUTICS & SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER · HOUSTON, TEXAS

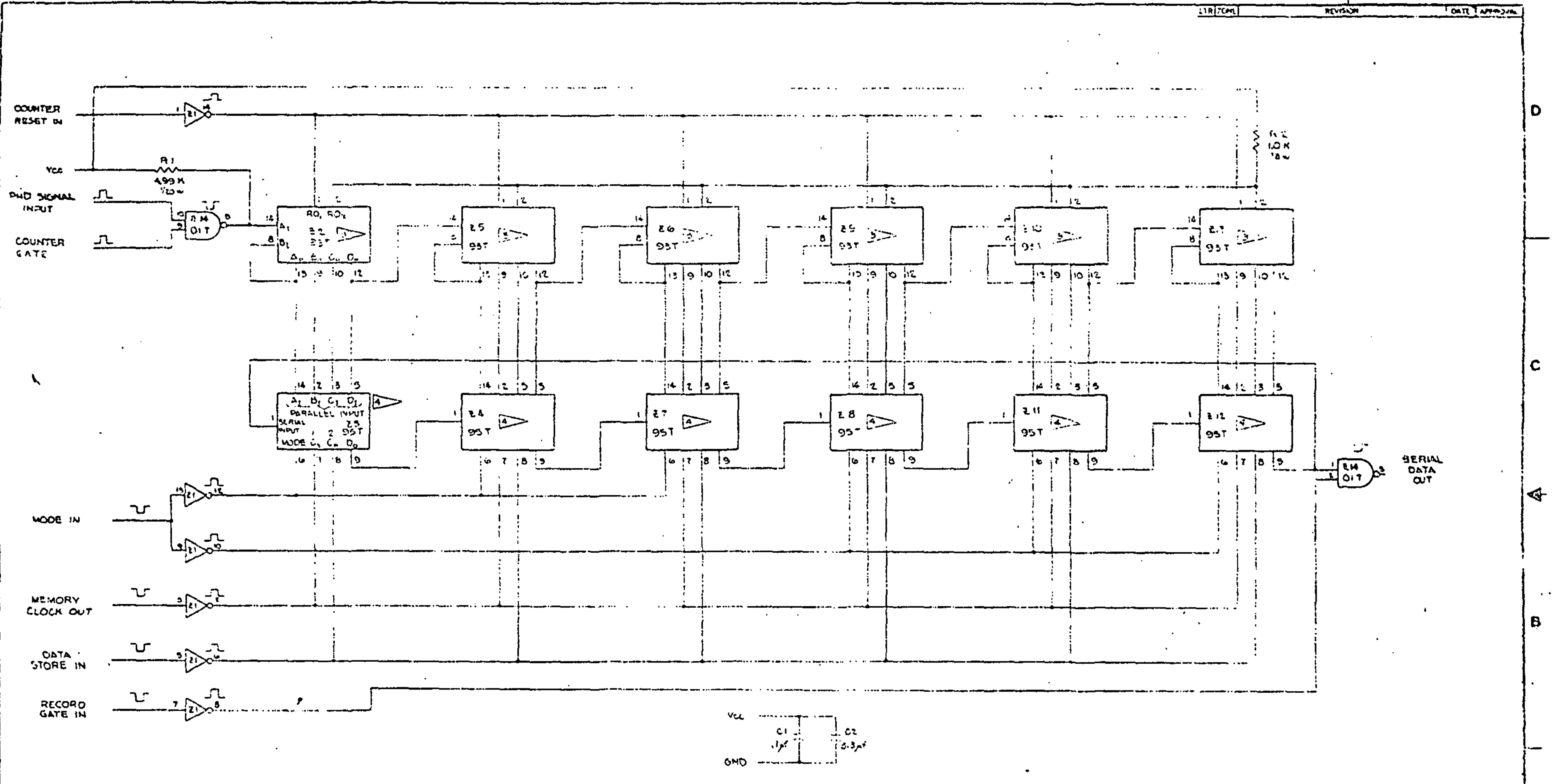
LOGIC DIAGRAM,
SEQUENCE CONTROL LINE
RECEIVER - COUNTER CONTROL

CODE IDENT NO	SIZE	DWG NO
21356	D	SIC 39106647

SCALE ~

3.4.2 COUNTER-MEMORY

The Counter-Memory Module (Schematic SIC39106648) contains a 24-bit counter and 24-bit parallel entry, serial out shift register. The counter counts pulses fed in at the PHD input. The counter has a count rate capability of 2.3 Mega Hertz. The counter is gated on by a positive counter gate signal. The normal count time is 12 seconds. Data is shifted into the register by the two signals called Mode and Data Store. The counter is then reset and ready to start another count cycle. The data is shifted through the shift register with a 24-pulse train. If the Record Gate is on, the data stored in the shift register will appear at the Serial Data output. The 24 pulses per shift cycle circulate the data by the output gate and return the data to its original position in the shift register. The data remains in the shift register until it is replaced by new data from the counters during the next data shift operation. There are ten identical counter-memory modules in the EPS instrument.



NOTES: UNLESS OTHERWISE SPECIFIED.

1. INTERPRET PER MSC MANUAL MSCM 8500.
2. ALL NAND GATES, COUNTERS & REGISTERS ARE SN54L SERIES; INVERTER IS SN54LO4T.
3. 4 BIT COUNTER TYPICAL 6 PLACES.
4. 4 BIT SHIFT REGISTER TYPICAL 6 PLACES.
5. Vcc PIN 4, GND P11 ON ALL PACKS.

SIGNATURES	DATE
DR E.E. LOPER	6/14/71
ENG	6-18-71
CH JDS & MW	7-9-71
R.P. Dean	9/21/71
APP	
AUTH	

NATIONAL AERONAUTICS & SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER · HOUSTON, TEXAS

LOGIC DIAGRAM,
EPS DATA PROCESSOR —
COUNTER -- MEMORY

ELECTRON PROTON SPECTROMETER

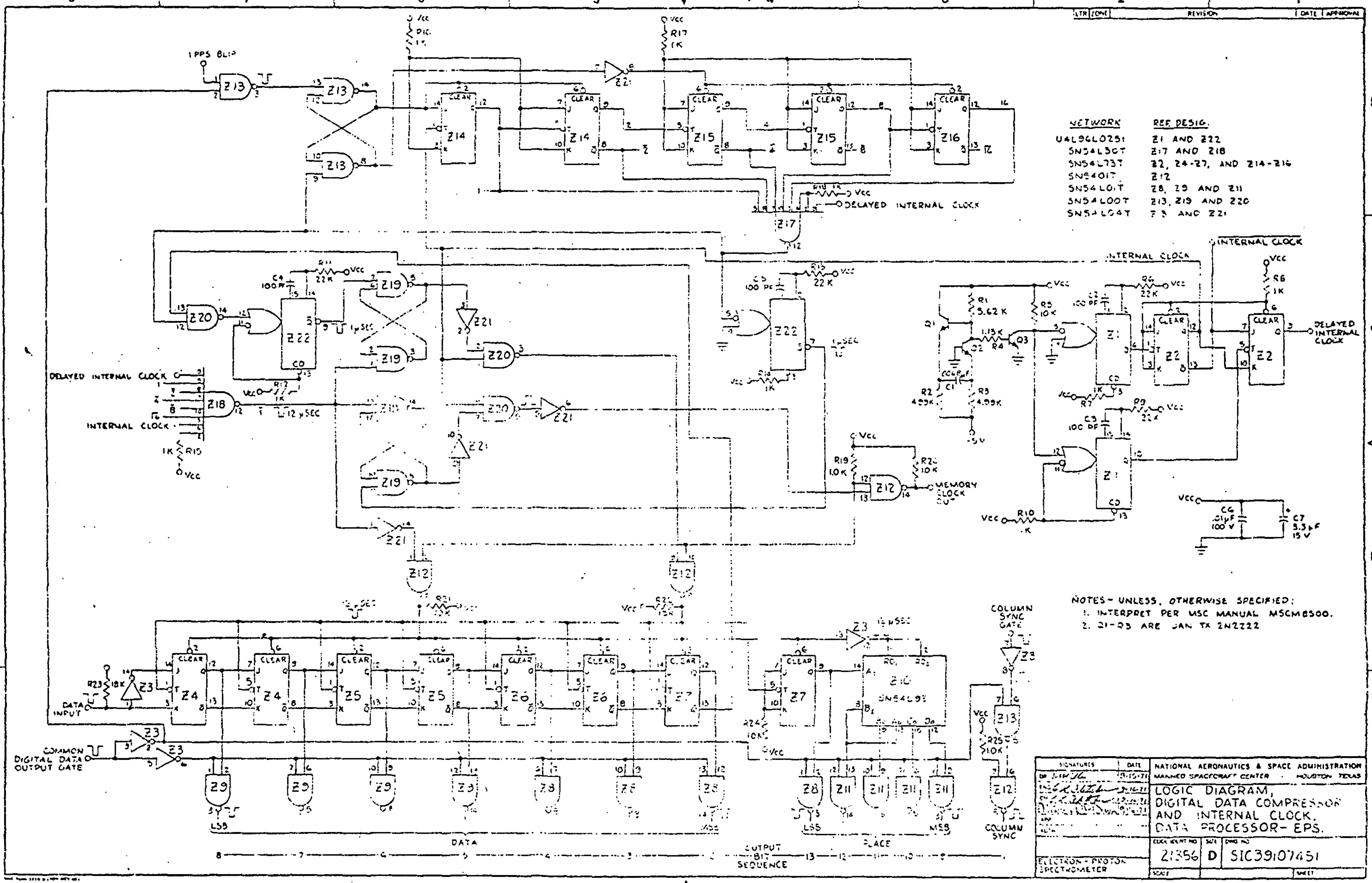
CODE IDENT NO	SIZE	DWG NO
21356	D	SIC39106648

SCALE ~ 130-00 SHEET

3.4.3 DIGITAL DATA COMPRESSOR AND INTERNAL CLOCK

The Digital Data Compressor and Internal Clock module (Schematic SIC39107451) generates the memory clock (for shifting the digital data in the counter-memory modules), compresses the digital data so that the seven most significant bits are read out, and generates the internal, biphase clock pulses. The data from the shift register is shifted into the data compressor until a "1" is shifted into the MSB position, or until 24 shifts occur. The number of shifts which occur during any one shift cycle is counted by the 5-bit shift counter. Thus, the data output consists of 7 bits of data, 5 bits of shift data, or "place", and 1 bit which is called column sync. The column sync bit is a "0" except during the second word. Then it is a "1".

The bi-phase clock consists of a basic 40 k Hertz oscillator, two one-shots and a divide by two circuit, giving an internal clock frequency of 20 k Hertz. The delayed clock output lags the clock by 90 degrees and is used in decoding circuits to inhibit glitches on decoded outputs during flip-flop transitions.



NETWORK	REF DESIG.
U4L9GL0251	Z1 AND Z22
SN54L30T	Z17 AND Z18
SN54L73T	Z2, Z4-Z7, AND Z14-Z16
SN5401T	Z12
SN54L01T	Z8, Z9 AND Z11
SN54L00T	Z13, Z19 AND Z20
SN54L04T	Z3 AND Z21

NOTES- UNLESS OTHERWISE SPECIFIED:
1. INTERPRET PER MSC MANUAL MSCM8500.
2. Q1-Q3 ARE JAN TX 2N2222

NATIONAL AERONAUTICS & SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER · HOUSTON TEXAS

LOGIC DIAGRAM,
DIGITAL DATA COMPRESSOR
AND INTERNAL CLOCK,
DATA PROCESSOR- EPS.

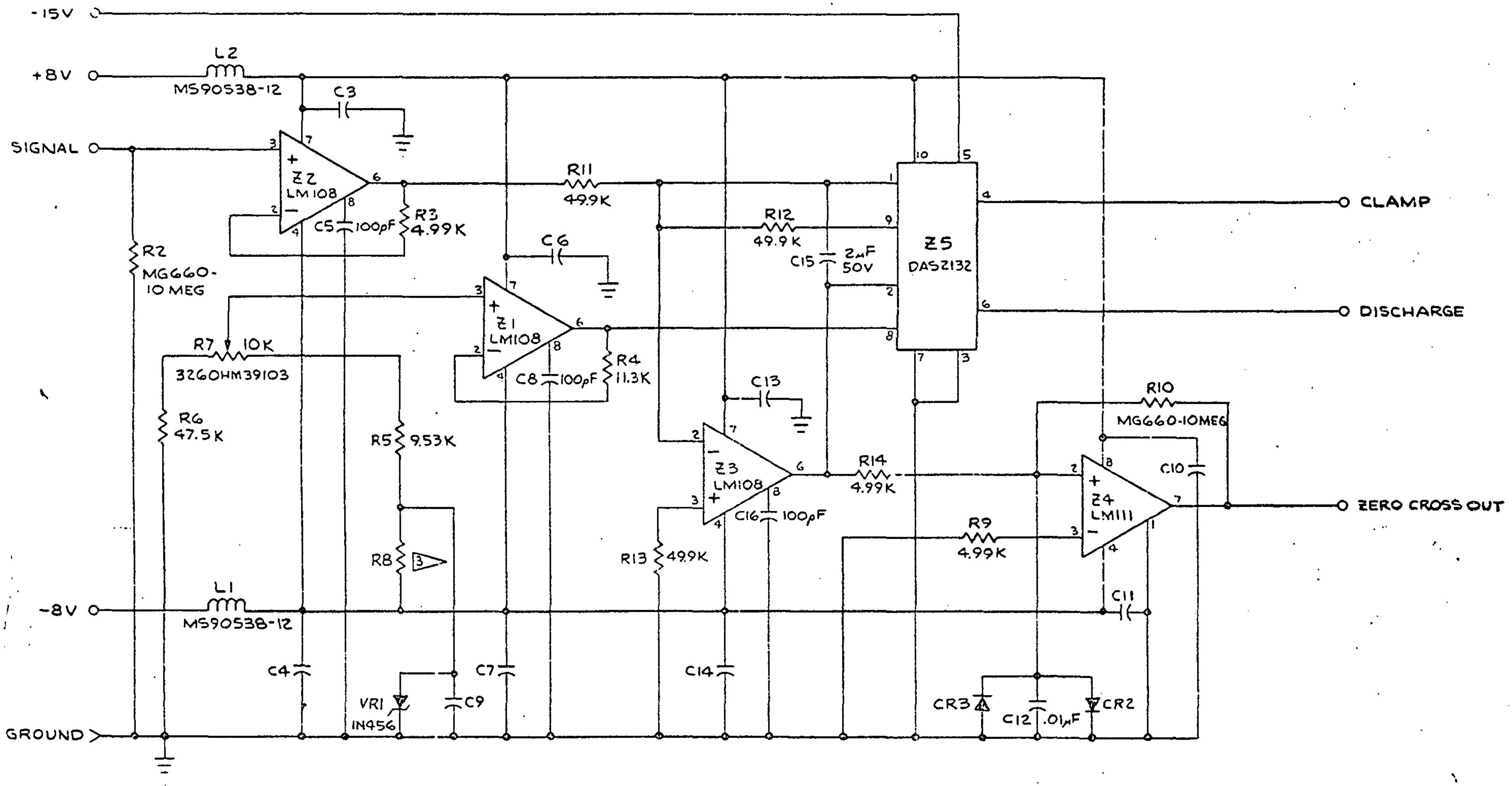
CODE IDENT NO 21356 SIZE D DWG NO SIC39107451

ELECTRON - PROTON SPECTROMETER

3.4.4 ANALOG-DIGITAL CONVERTER (SCHEMATIC SIC39107024)

The analog to digital converter is a 10-bit unit utilizing the dual-slope principle and a zero-crossing detector. The basic circuits are a buffer amplifier, reference amplifier, integrating amplifier, dual J-FET switch, and a comparator. The buffer amplifier serves as interface between all housekeeping data sources and the integrating amplifier. The reference amplifier provides a very stable source of current and its reference is a temperature controlled Zener diode. One of the J-FET switches controls the reference current to the integrating amplifier. The other J-FET switch discharges the integrating capacitor and holds it in a zero charge state during the clamp time interval. The integrating capacitor is a 2 microfarad polycarbonate with very low leakage, low dissipation factor, and low temperature coefficient. The integrating amplifier provides drive to the comparator, which has approximately 10 mV of hysteresis to eliminate false zero-crossing output. The comparator output is used in the timing control of the A/D Control Logic.

The timing sequence of the conversion process is shown in the Analog-Digital Conversion Timing Chart, Fig. 6. The operation is as follows: The multiplexer is gated on (enabled) and an analog voltage is fed to the buffer amplifier, which charges the integrating capacitor through a 49.9 K ohm resistor for a fixed time (.051 sec.). The capacitor will assume a charge dependent upon the analog voltage level which is limited to a maximum of 5 volts. The multiplexer is then switched off, the reference current is switched in, and



NOTES - UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE RNC50 1/20 W.
2. ALL CAPACITORS ARE .1μF CKR06

3 VALUE TO BE SELECTED DURING ACCEPTANCE TEST PER LEC DOCUMENT NO. EPS-403

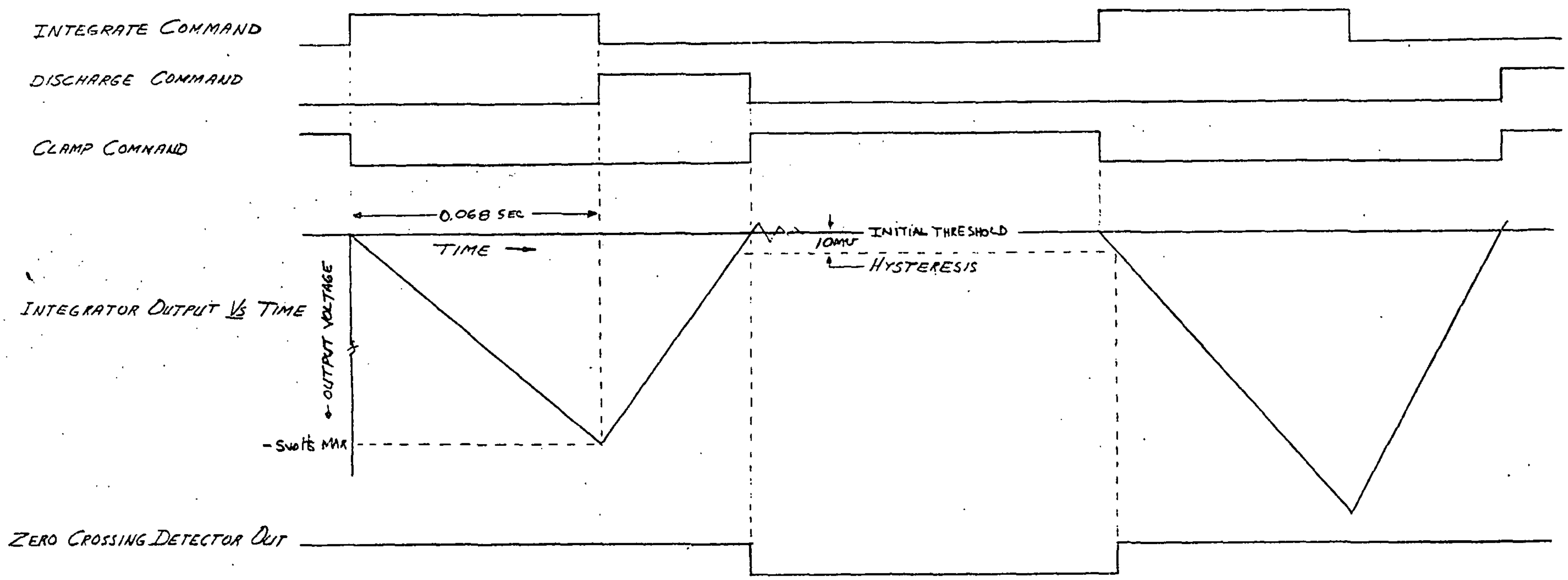
SIGNATURES	DATE
DR B Rose	9-16-71
ENG C. L. Fletcher	9-20-71
CH C. L. Fletcher	9-20-71
[illegible] P. Dunn	9/20/71
APP	
AUTH	

NATIONAL AERONAUTICS & SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER • HOUSTON, TEXAS

SCHEMATIC -
ANALOG - DIGITAL
CONVERTER

CODE IDENT NO. 21356 SIZE C DWG NO. SIC39107024

SCALE — SHEET 1



*ASSUMES AN ABSOLUTE MINIMUM CLOCK FREQUENCY OF 15.000 KHz

Figure 6 ANALOG-DIGITAL CONVERSION TIMING CHART the capacitor is discharged at a constant rate from the reference circuit. When the capacitor charge passes through zero the comparator changes state and stops the conversion process. The digital word is generated in the A/D Control Logic and is discussed in Section 3.4.5.

Sources of error in the analog-digital conversion are offset voltages in the amplifiers, leakage current through the J-FET switches, variation in the reference circuit and comparator offset. The offset voltage of the amplifiers and comparator are specified to be less than 3 mV. Leakage current through the J-FET switches was measured and caused no error under actual circuit operation. The reference circuit has a temperature compensated Zener diode reference, and the actual measured temperature coefficient for the reference circuit is .0007%/°C over the -50°C to +70°C temperature range. The maximum analog voltage which may be measured is 5 volts. The resolution is 5 mV or 1 bit.

ANALOG-DIGITAL CONVERTER
SPECIFICATION

1. ADC Analog Section

The analog to digital converter is a dual slope type, with the input range of 0 to 5 volts. The output is 10 bits with an accuracy of ± 1 LSB over the temperature range of -25° C to +50° C.

2. Reference Amplifier, Integrating Amplifier and Buffer Amplifier

V_{OFFSET}	3 mv max
V_{OFFSET} Temp. Coef.	15 μV/°C
I_{OFFSET}	.4 na max
Operating Temp. Range	-55°C to +125°C
Power Supply Requirement/Amplifier	±8 Volts @ .5 ma
Common Mode Rejection Ratio	85 dB min
Power Supply Rejection Rate	80 dB min
Large Signal Voltage Gain	300 V/mv typical

3. Analog Switch

The analog switches are J_{FET} devices with drivers. The DAS 2132 is a dual unit, each unit having separate control.

Power Supply Requirements	+8 volts	2 ma/switch "ON" 0 ma/switch "OFF"
	-15 volts	1.6 ma/switch "ON" 0 ma/switch "OFF"
Logic Level Required for "ON-OFF" Control (TTL Compatible)		"ON" + 3 Volt "OFF" 0 Volt
Operating Temp. Range		-55°C to +125°C
Resistance of Switch		"ON" = 80 ohms "OFF" 200 megohms

Turn-on Time	.5 μsec
Turn-off Time	.5 μsec

4. Integrating Capacitor

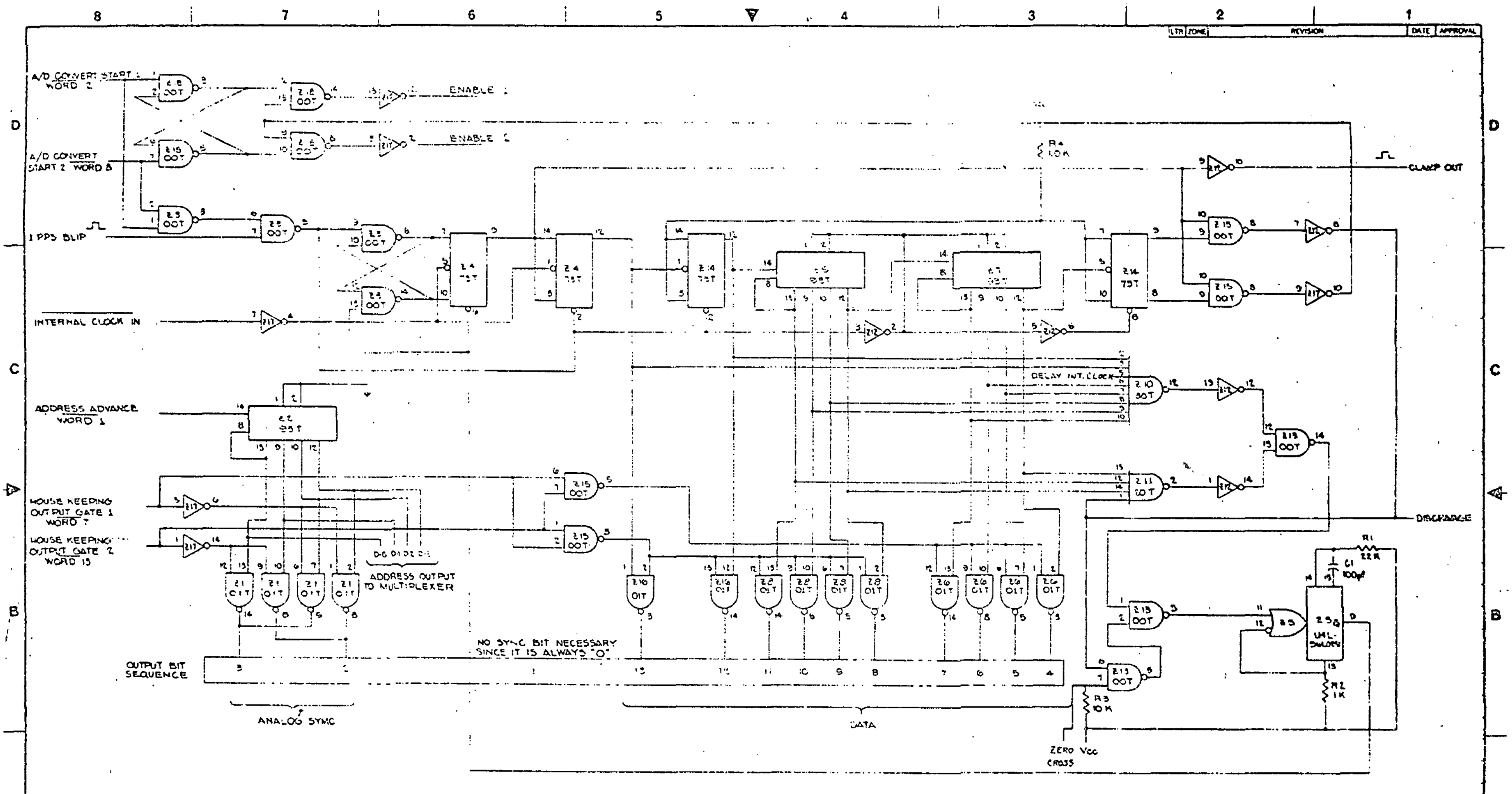
Capacitance/Voltage	2 μf/50 VDC
Insulation Resistance @ 60°C	3000 megohms - microfarads
Percentage Capacitance Change Over Temp. Range - 45°C to +90°C	+1%, -2%
Dissipation Factor (-50°C to +125°C)	+.5%, -0.0%
Capacitor Type	metalized polycarbonate

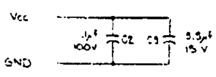
5. Comparator

Power Supply Requirements	+8 volts @ 10 ma
Operating Temp. Range	-55°C to +125°C
Input Offset Voltage	3 mv maximum
Input Offset Current	10 ηA maximum
Bias Current	100 ηA maximum

3.4.5 A/D CONTROL (SCHEMATIC SIC39106641)

The A/D Control Module provides the control functions for the A/D converter, generates the 10 bit digital word plus two sync bits for the housekeeping data word, and provides four bits of address to the multiplexer. The A/D conversion occurs during intervals 2 and 8 and is initiated by the 1 pps. The latch circuit is set and remains on until the end of the conversion. The gate that sets the latch resets all counters to zero. When the latch is set, the 11 bit counter starts, the clamp signal goes low, and enable 1 or enable 2 goes high. When the eleventh bit goes to a high state (1024 clock pulses), the enable line goes low, and the discharge line goes high. The counter continues to count until "Zero Cross" occurs, which resets the latch and stops the counter. The number in the counter is the digitized equivalent of the analog input to the A/D converter. The data appears on the output gates and is read out during interval 7 or 13.





NOTES: UNLESS OTHERWISE SPECIFIED.

1. INTERPRET PER MSC MANUAL MSCM 8500.
2. ON SN 5400 MODULES PIN 11 IS GND, PIN 4 IS Vcc.
3. ALL UNUSED GATES SHALL HAVE ONE INPUT GROUNDED.
4. ALL NAND GATES AND FLIP-FLOPS ARE SN54L SERIES; HEX INVERTERS ARE SN54L04T.

SIGNATURES	DATE
DR E.S. LOPEZ	6-16-71
ENG	6-22-71
CH JDS & MW	7-9-71
DATA RELEASE D.P.	3/21/71
APP	
AUTH	

E.P.S.

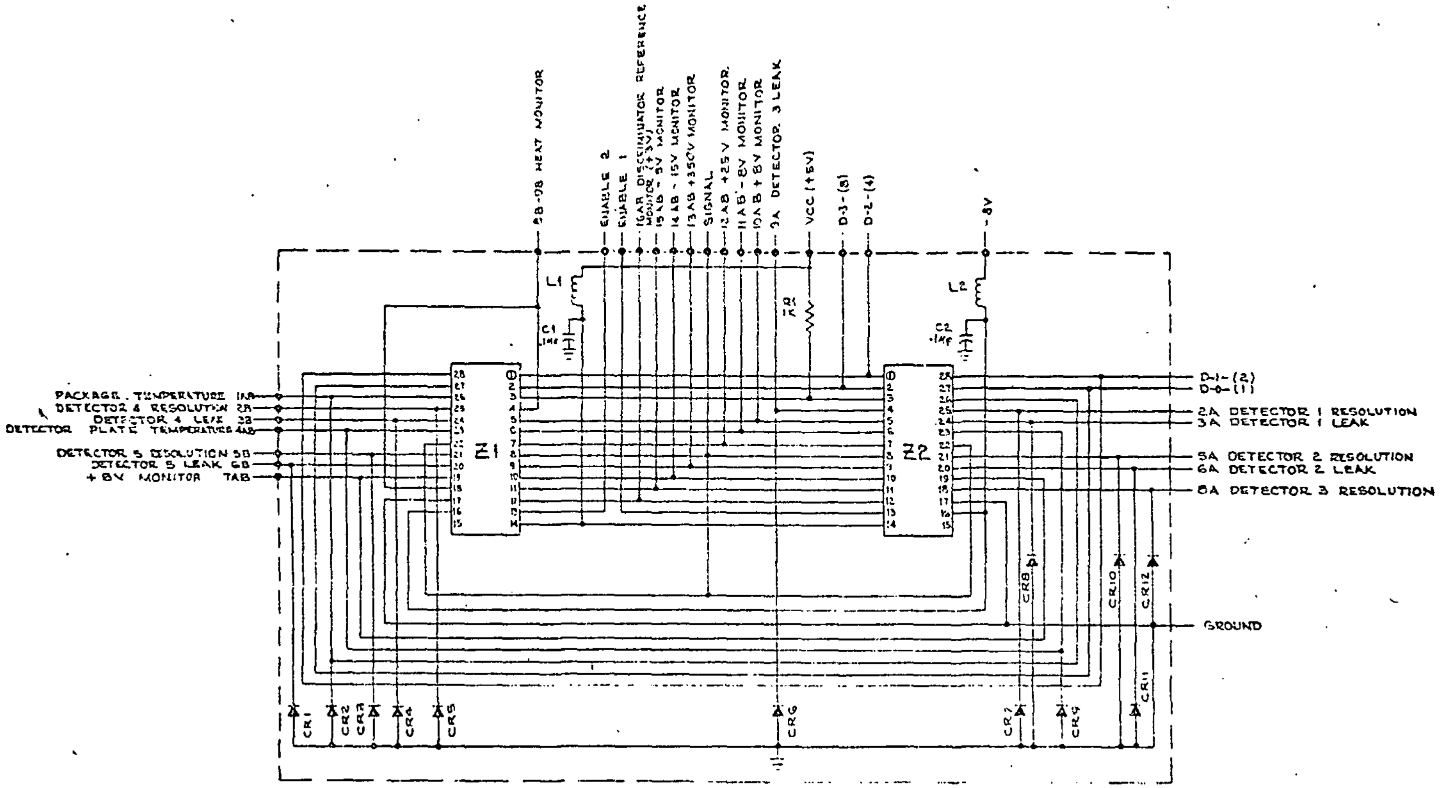
NATIONAL AERONAUTICS & SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER · HOUSTON, TEXAS

LOGIC DIAGRAM,
A/D CONTROL –
E.P.S. DATA PROCESSOR

CODE IDENT NO.	SIZE	DWG NO.
21356	D	SIC 39106641
SCALE ~	150-ED	SHEET

3.4.6 MULTIPLEXER MODULE (SCHEMATIC SIC39106642)

The Multiplexer Module consists of two integrated circuit packages each containing a 16-channel multiplexer. The two units are operated as a 32-channel unit. There are 21 sources of data fed through the multiplexer. However, all channels are used, which allows eleven channels of redundant data. The multiplexer package contains the decoding logic required for switching, so it can be operated by the binary outputs of a 4-bit counter. The multiplexer utilizes the J-FET device for switches. Diodes clamps are used to prevent negative bias being applied to the multiplexer.



NOTES: UNLESS OTHERWISE SPECIFIED.

1. INTERPRET PER MSC MANUAL MSCM 3500.
2. Z1 & Z2 - HARRIS HS-9-1000-7, 16 CHANNEL MULTIPLEXER, CAPACITORS ARE TYPE CK05; RESISTOR IS TYPE RCR05.
3. ALL DIODES ARE IN914.

SIGNATURES	DATE
DR Bill R. Bell	6-17-71
ENG	5-19-71
CK J.D. Stringer	6-29-71
PROJ. E.P. Dunn	8/11/71
APP	
AUTH	

NATIONAL AERONAUTICS & SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER · HOUSTON, TEXAS

SCHEMATIC, MULTIPLEXER MODULE,
DATA PROCESSOR -
E.P.S.

CODE IDENT NO	SIZE	DWG NO
21356	D	SIC 39106642

EPB

MULTIPLEXER SPECIFICATION

The Multiplexer Specifications are outlined below.

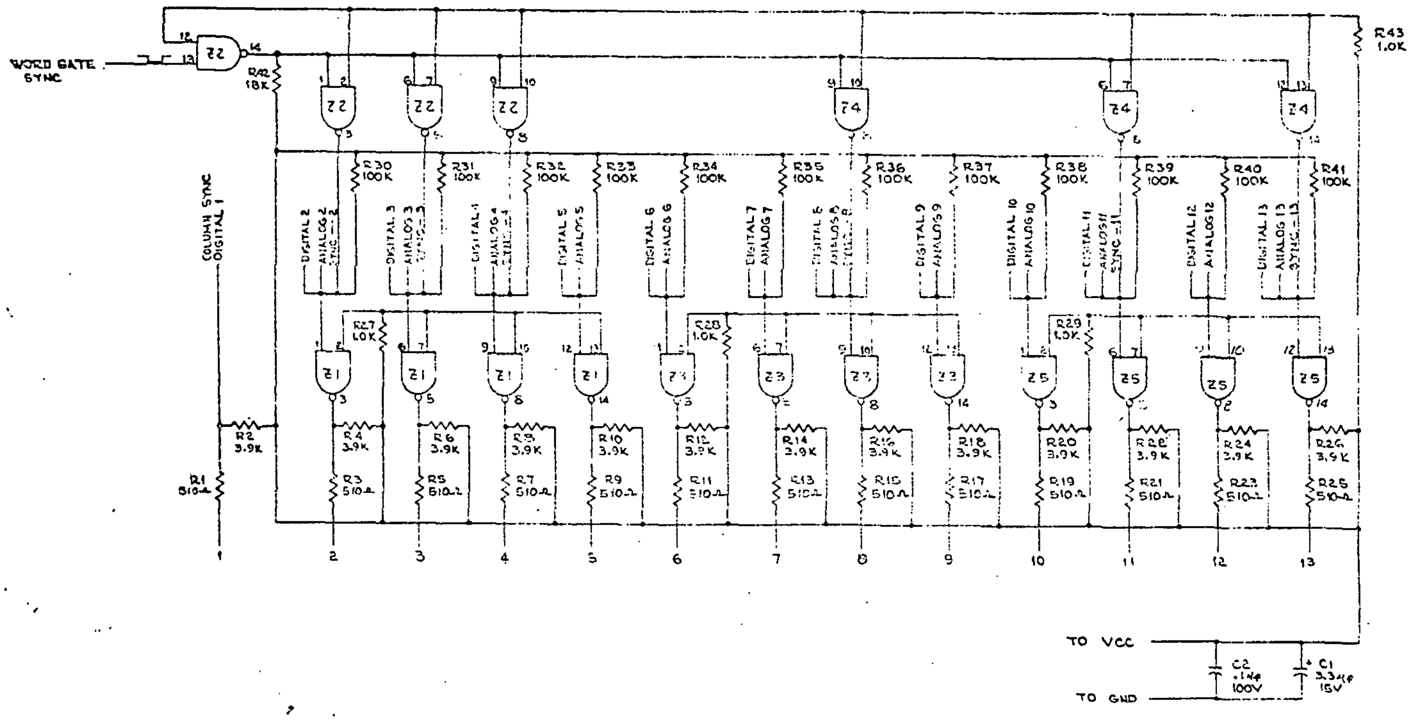
The multiplexer serves as a switching device to route various analog voltages to the analog-to-digital converter (ADC). The individual channel switches must have an "ON" resistance small such that the analog voltage being switched is not lowered significantly. The "OFF" resistance must be sufficiently high to avoid "cross-talk" or leakage from the "OFF" channels to the channel being measured.

Number of Channels	16 x 2 = 32
Power Requirement, Total	(+5 Volts @ 9.6 ma) x 2 = 96 mw (-8 Volts @ 16 ma) x 2 = 256 mw
"ON" Resistance	1200 ohms maximum
"OFF" Leakage Current	≤ 250 Picoamps
Channel Addressing	Compatible to TTL Logic
Cross Talk with V_{in}	20 VP-P, 100 kHz - - - -80 dB
Environmental	MIL-STD 883, Condition B
Analog Voltage Range Input	0.0 to +5.0 Volts

3.4.7 OUTPUT BUFFER AND WORD SYNC GENERATOR (SCHEMATIC SIC39106645)

The Output Buffer and Word Sync Generator interfaces all data from the EPS to the CSM telemetry. The sync word is also generated in this module. During Word 1 time interval the word sync gate is enabled and the sync word (0111000100101) is fed out on the data lines. The output buffers are standard power T^2L logic chosen to special parameters so that they may be driven by derated low power logic. The inputs to the output buffer are connected in the WIRED-OR configuration, and input data originates in the Data Compressor Module (digital data), the A/D control module (analog data) and the word sync generator circuit. The output of the buffer is designed to meet the interface requirements as specified in the Electrical ICD MH04-02110-234.

The output bits are required to reach their sampled voltage level within 20 milliseconds after the positive going edge of the 1 Hertz clock pulse (Section 3.4.1). This allows approximately 9 charging time constants for the output positive going pulse. The pulse will rise to 3.5 volts in 5 time constants, giving a large safety margin. The discharge time constant for a data bit "0" is approximately 10 times shorter, so no timing problems occur for the "0" bit data. All output data lines are fed out through filters.



NOTES: UNLESS OTHERWISE SPECIFIED

1. INTERPRET PER MSC MANUAL MSCM 8500.
2. Z2 AND Z4 ARE SN54L01T, Z1,3, AND Z5 ARE SN5401T.
3. TYP FOR ALL NETWORK VCC IS PIN 4 & GND IS PIN 11.
4. ALL RESISTORS ARE 1/8 W.

PART NUMBER	DESCRIPTION	MATERIAL	SPECIFICATION

DIMENSIONAL TOLERANCE UNLESS NOTED OTHERWISE
.0 ± .10
.00 ± .02
.000 ± .005
ANGULAR ±

SURFACE FINISH IN MICROINCHES RMS UNLESS NOTED OTHERWISE ✓

NEXT ASSEMBLY

SIGNATURES	DATE
DR Bill L. Bell	6-21-7
ENG	
CH	
STRESS R.P.D.	
APP	
AUTH	

EPS

NATIONAL AERONAUTICS & SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER · HOUSTON, TEXAS

LOGIC DIAGRAM,
OUTPUT BUFFER & WORD SYNC GEN.
EPS DATA PROCESSOR

CODE IDENT NO	SIZE	DWG NO
21356	D	SIC39106645

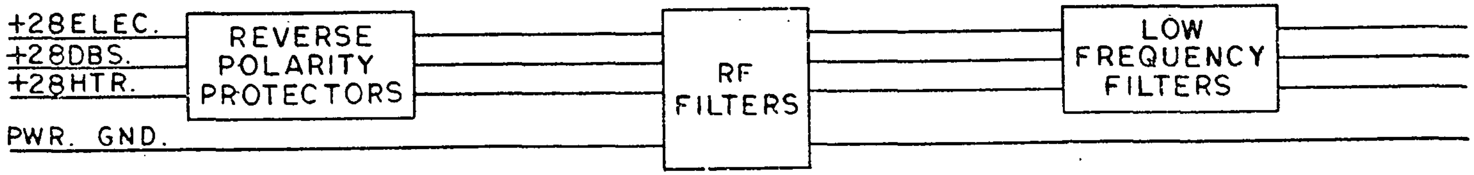
SCALE ✓
SHEET

3.5 POWER SYSTEMS

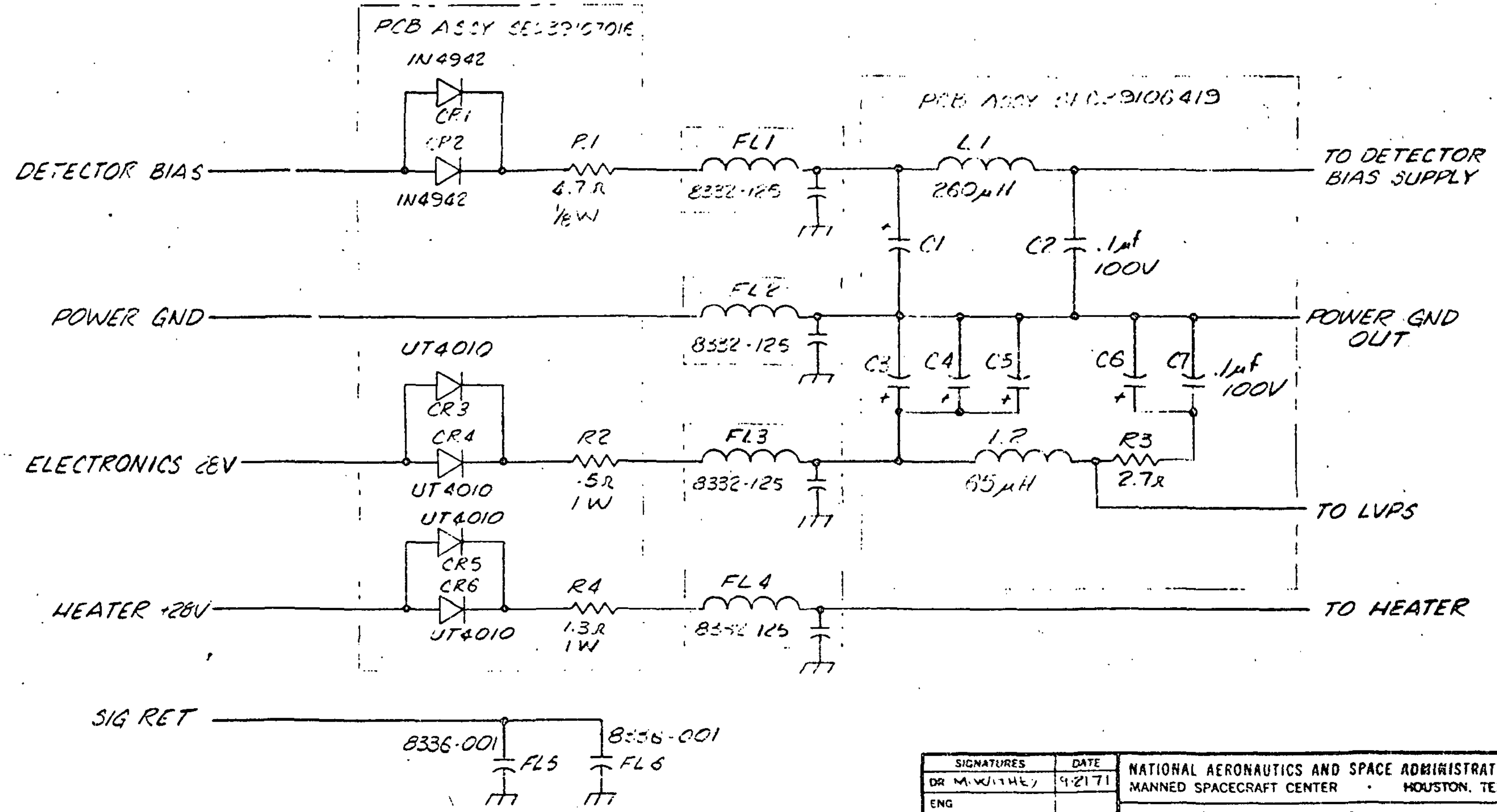
The EPS Power System was designed to receive the +28 V available from the spacecraft and provide the proper output voltages to both the EPS detectors and the electronic subsystems. The design criteria for the EPS power subsystems were partially specified in the EPS Electrical ICD NR #MH04-02119-234 and in the Electromagnetic Compatibility Design Criteria NR Document #MH04-0257-234.

3.5.1 INPUT FILTER

The three plus 28 Vdc power inputs and power ground from the CSM are routed to the EPS power input filter (see Block Diagram and Schematic SIC39106640). Within the Input Filter, all four lines are routed through circuits that protect the EPS from voltages of reverse polarity and from noise and interferences conducted into the EPS. The Input Filter also provides filtering for interference generated within the EPS and conducted out the power lines. The three power lines are then routed to the individual subassemblies.



INPUT FILTER MODULE BLOCK DIAGRAM



NOTES UNLESS SPECIFIED OTHERWISE:

1. RESISTORS ARE 2.7Ω 1/8W. CAPS ARE 15μf 15V.

LTR	ZONE	REVISION	DATE	APPROVAL

SIGNATURES	DATE
DR M. WITHEY	9-21-71
ENG	
CH	
APP	
AUTH	

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER · HOUSTON, TEXAS

SCHEMATIC
INPUT FILTER MODULE E.P.S.

CODE IDENT NO.	SIZE	DWG NO.
21356	B	SIC39106640
SCALE N/A		SHEET

MSC Form 1018 D (REV OCT 63

ELECTRON-PROTON SPECTROMETER
INPUT FILTER MODULE SPECIFICATIONS

A. <u>Inputs</u>: The EPS Input Filter Module shall accept four separate inputs. These inputs are:

1. Electronics Power Input: 27.5 Vdc ± 2.5 Vdc
2. Detector Bias Power Input: 27.5 Vdc ± 2.5 Vdc
3. Heater Power Input: 27.5 Vdc ± 2.5 Vdc
4. Power Ground

B. <u>Outputs</u>: The Input Filter Module shall provide four separate filtered power outputs to the EPS. These outputs are:

1. Electronics Power (filtered)
2. Detector Bias Power (filtered)
3. Heater Power (filtered)
4. Power Ground (filtered)

C. <u>RFI</u>: The Input Filter Module shall provide the necessary electronic circuits to meet or exceed the requirements of North American Rockwell Corp., Space Division Document MH04-02057-234, Electromagnetic Compatibility Design Criteria.

D. <u>Operating Temperature Range</u>: -25°C to +50°C

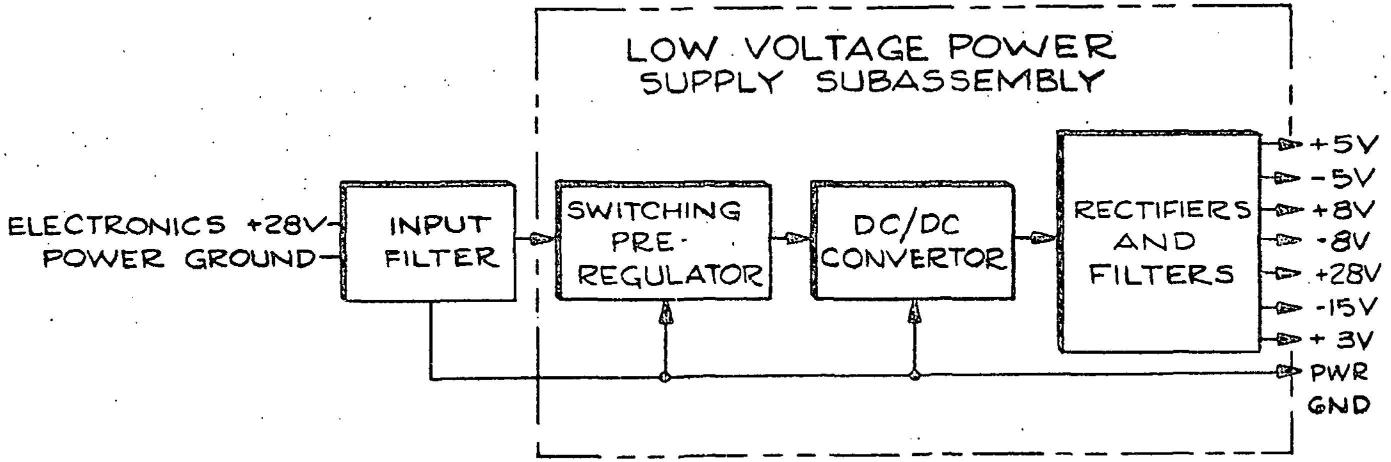
E. <u>Survival Temperature Range</u>: -50°C to +65°C

2

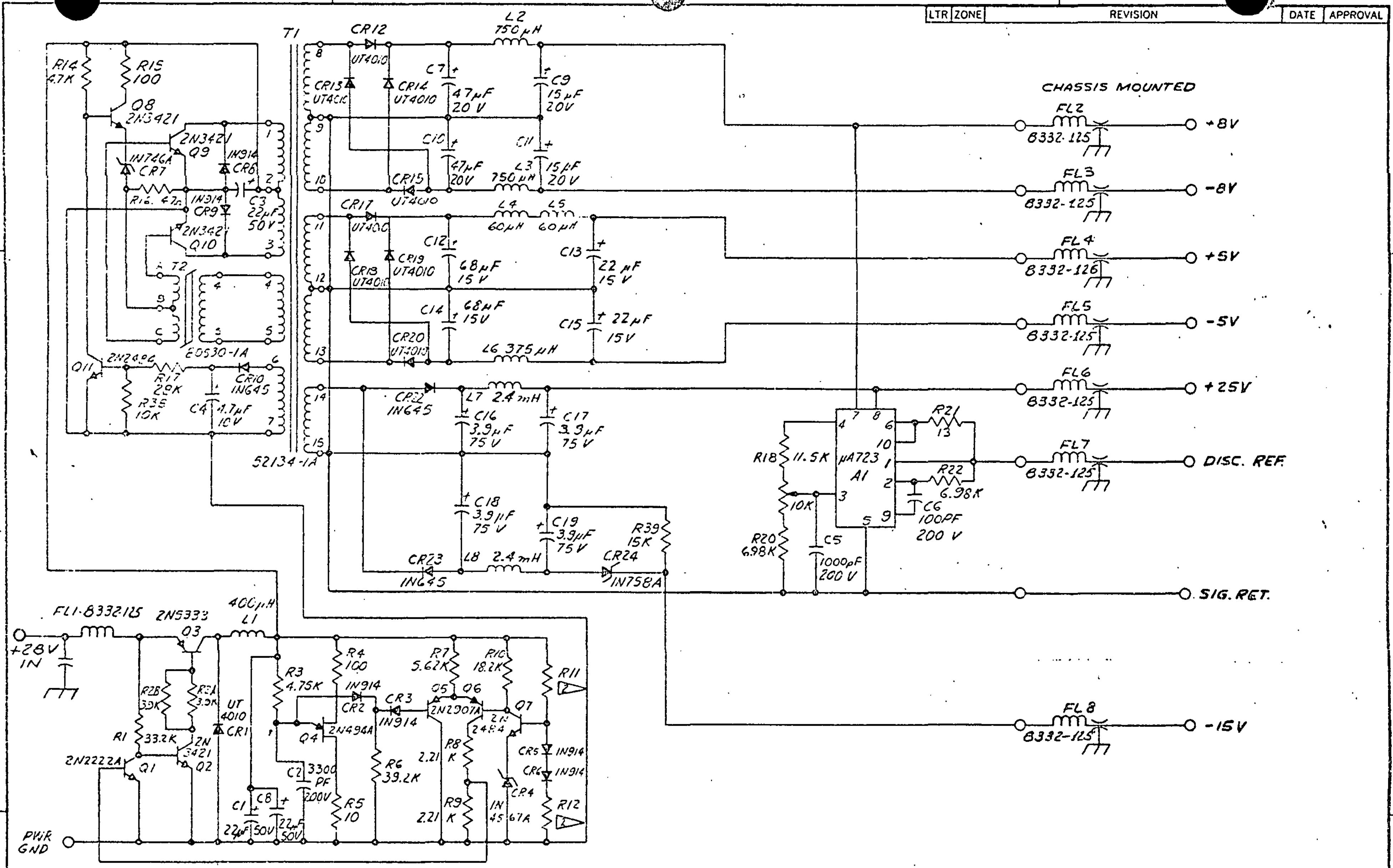
F. Ground Isolation: There shall be a minimum of 1 megohm resistance between the power ground and the EPS external structure (chassis ground).

3.5.2 LOW VOLTAGE POWER SUPPLY

The Low Voltage Power Supply (see Block Diagram and Schematic SIC39106637) receives filtered +28 V which is regulated down to +20 Vdc by utilizing a switching regulator. A switching regulator was used because of the efficiency required. The regulator output is then utilized by the dc/dc converter. There are three separate output windings on the dc/dc converter transformer. These windings produce six different output voltages. One of these outputs (the +8V) is also regulated down to +3.0 V to provide a stable reference voltage for the pulse-height discriminator subassemblies.



LOW VOLTAGE POWER SUPPLY BLOCK DIAGRAM



NOTES: UNLESS OTHERWISE SPECIFIED.

1. INTERPRET PER MSC MANUAL MSCM8500.

2. VALUES OF R11 AND R12 ARE DETERMINED BY ACTUAL VALUE OF V_Z OF CR4.

SIGNATURES	DATE
DR	3-30-71
ENG	4-8-71
CH R.P.Dunn	5/27/71
RELEASE R.P.Dunn	8/31/71
APP	
AUTH	

NATIONAL AERONAUTICS & SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER · HOUSTON, TEXAS

SCHEMATIC DIAGRAM,
LOW VOLTAGE POWER SUPPLY—
ELECTRON-PROTON SPECTROMETER

ELECTRON-PROTON SPECTROMETER

CODE IDENT NO.	SIZE	DWG NO.
21356	C	SIC 39106637
SCALE ~	150-EB	SHEET

LOW VOLTAGE POWER SUPPLY SPECIFICATIONS

A. Input Voltage: 27.5 ± 2.5 Vdc

B. Input Current: $I_{in}(\max) \leq 557$ ma @ 28 Vdc

C. RFI: Must meet or exceed the requirements of North American Rockwell Corp., Space Division Document MH04-02057-234, Electromagnetic Compatibility, Design Criteria.

D. Operating Temperature Range: $-25°C \leq T_{opp} \leq +50°C$

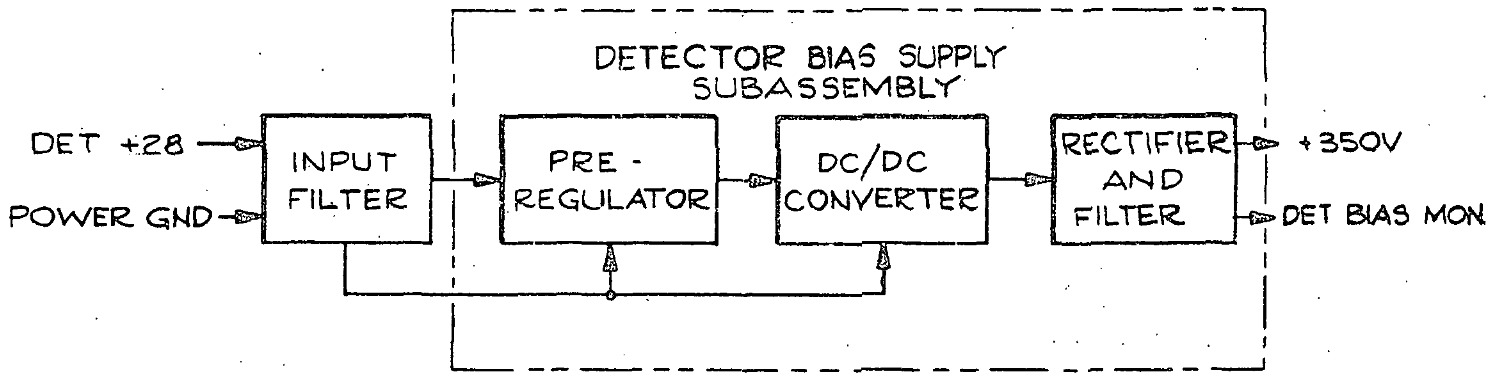
E. Survival Temperature Range: $-50°C \leq T_{surv} \leq +65°C$

F. Outputs: The LVPS must provide the following outputs (with the given specifications):

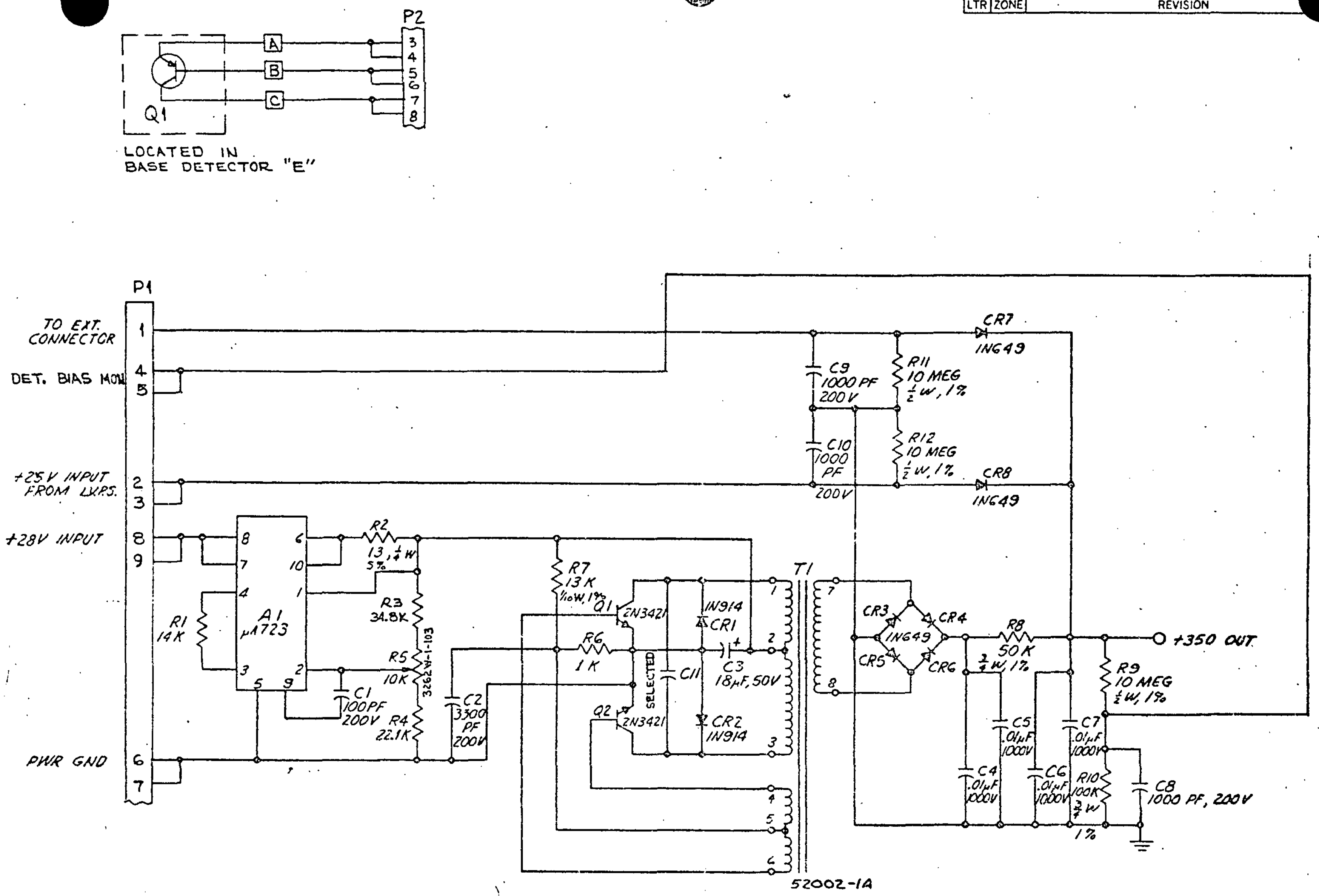
Voltage	Current	Regulation	Maximum Ripple	Maximum Spike
+8 Vdc	175 mamp	+0.2 Vdc -0.0 Vdc	25 mvpp	50 mvpp
-8 Vdc	150 mamp	+0.2 Vdc -0.0 Vdc	25 mvpp	50 mvpp
+5 Vdc	900 mamp	±0.3 Vdc	50 mvpp	50 mvpp
-5 Vdc	115 mamp	±0.3 Vdc	50 mvpp	50 mvpp
+25 Vdc	10 mamp	±2.0 Vdc	150 mvpp	50 mvpp
-15 Vdc	1 mamp	±2.0 Vdc	150 mvpp	50 mvpp
+3.0 Vdc	20 mamp	±0.01 Vdc	1.0 mvpp	5 mvpp

3.5.3 DETECTOR BIAS SUPPLY

The +28 Vdc for the Detector Bias Supply (see Block Diagram and Schematic SIC3910638) is regulated down to +21 Vdc in order that the bias applied to the EPS detectors will not be affected by fluctuations in the spacecraft power lines. This regulated +21 Vdc is then fed to the dc/dc converter which generates a 350 volt square wave. This is rectified, filtered and applied to the detectors cathode thru the bias filter subassembly.



DETECTOR BIAS SUPPLY BLOCK DIAGRAM



NOTES: UNLESS OTHERWISE SPECIFIED.

1. INTERPRET PER MSC MANUAL MSCM8500.
2. ALL RESISTORS $\frac{1}{20}$W, 1%, VALUES IN OHMS.

SIGNATURES	DATE
DR Doyille	3-30-71
ENG R.E. Cuttinger	4-8-71
CH R.E. Cuttinger	8/20/71
REL: R.P. Dunn	9/21/71
APP	
AUTH	

ELECTRON-PROTON SPECTROMETER

NATIONAL AERONAUTICS & SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER • HOUSTON, TEXAS

SCHEMATIC DIAGRAM,
DETECTOR BIAS SUPPLY-
ELECTRON-PROTON SPECTROMETER

CODE IDENT NO.	SIZE	DWG NO.
21356	C	SIC39106638
SCALE ~		1SD-EB

SHEET

MSC Form 1010 C (REV OCT 68)

DETECTOR BIAS SUPPLY
SPECIFICATIONS

A. Input Voltage: 27.5 ± 2.5 Vdc

B. Input Current: Maximum $\leq$ 50 ma @ 28 Vdc

C. RFI: Must meet or exceed the requirements of North American Rockwell Corp., Space Division Document MH04-02057-234, Electromagnetic Compatibility, Design Criteria.

D. Operating Temperature Range: -25°C to +50°C

E. Survival Temperature Range: -50°C to +65°C

F. Output: The Detector Bias Supply must provide the following output:

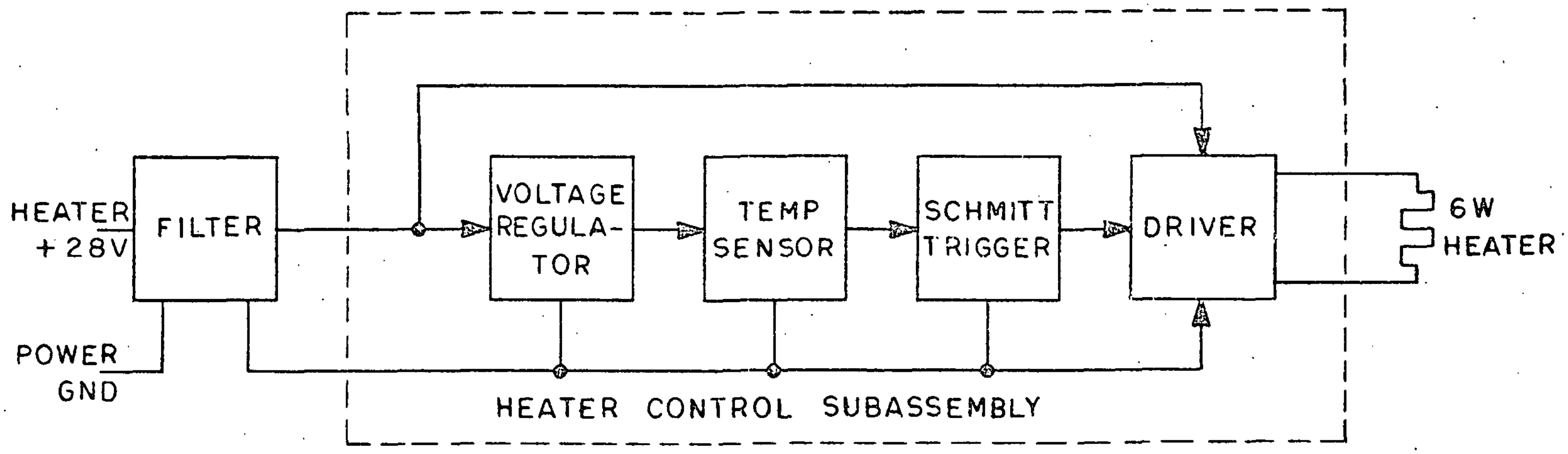
Voltage	Current	Regulation	Maximum Ripple	Maximum Spike
+350 Vdc	10 μa	±17.5 Vdc	500 mvpp	10 mvpp

G. Monitor Output: The detector bias supply must provide an analog output voltage that is directly proportional to the bias voltage. The monitor output must have the following characteristics:

Amplitude	Output Impedance
0 to 5 Vdc	$\leq$ 1 Megohm

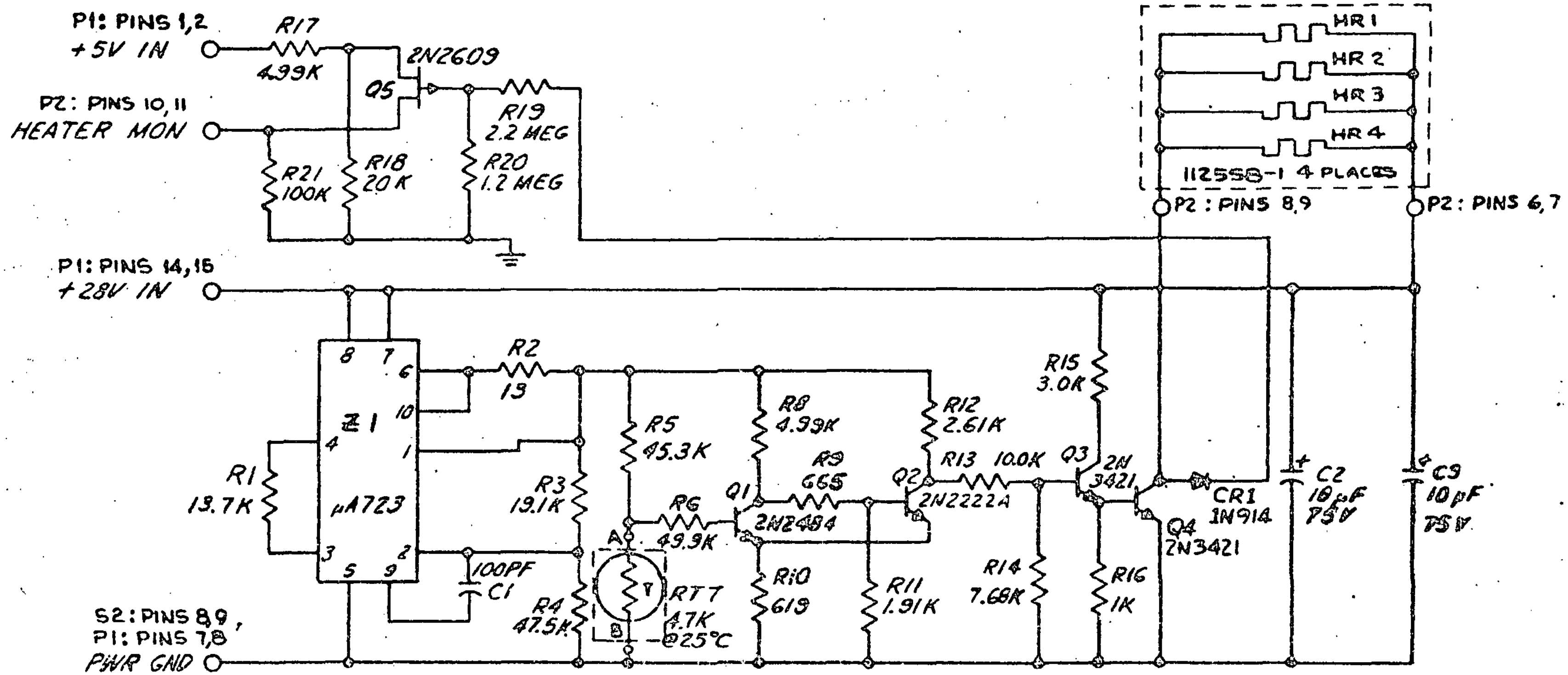
3.6 HEATER CONTROL SYSTEM

The Heater Power +28 Vdc line and power ground are routed to the Heater Control (see Block Diagram and Schematic SIC39106639) subassembly. The +28 Vdc is regulated to +10 Vdc for use as a stable reference for the temperature sensing circuit. The temperature sensing circuit consists of a thermistor and schmitt trigger, with the trip points set at 0° C (heater turn-on) and 10° C (heater turn-off). The output of the schmitt trigger is amplified and utilized to apply power, as necessary, to four individual skin heaters bonded to the electronics assembly housing. In addition to controlling the 6 watt heater, the schmitt output is also buffered and routed to the EPS Data Processor to provide the status of the EPS heaters (i.e., whether on or off).



HEATER CONTROL BLOCK DIAGRAM

LTR	ZONE	REVISION	DATE	APPROVAL
A		RIG WAS 100K, ¼W 8-2-71	11-2-71	
B		Q2 WAS 2N2484 11-9-71	8-9-71	



NOTES: UNLESS OTHERWISE SPECIFIED:

1. INTERPRET PER MSC MANUAL MSCM8500.
2. ALL RESISTOR VALUES IN OHMS.

SIGNATURES	DATE
DR	3-31-71
ENG	9-8-71
CH R.P. Dunn	4/8/71
RPD	4/8/71
APP	
AUTH	
E. F. S.	

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER · HOUSTON, TEXAS

SCHEMATIC DIAGRAM,
HEATER CONTROL-
ELECTRON-PROTON SPECTROMETER

CODE IDENT NO. 21356 SIZE B DWG NO. SIC 39106639
SCALE ~ ISD-EB SHEET

MSC Form 1016 D (REV OCT 63)

HEATER CONTROL
SPECIFICATIONS

A. Input Voltage: 27.5 ± 2.5 Vdc

B. Input Current: I in (Max) = 214 ma @ 28 Vdc

C. RFI: Must meet or exceed the requirements of North American Rockwell Corp. Document MH04-02057-234, Electromagnetic Compatibility, Design Criteria.

D. Operating Temperature Range:

$-25°C \leq T_{opp} \leq +50°C$

E. Survival Temperature Range:

$-50°C \leq T_{surv} \leq +65°C$

F. Operation: The Heater Control will sense the temperature of the EPS electronics package and provide 6 watts of heater power when the temperature drops below 0° C. When the temperature of the electronics package rises to 10° C, the Heater Control shall remove the 6 watts of heater power.

G. Outputs: The Heater Control shall provide a bi-level output to the EPS Data Processor indicating whether the heater is on or off.

3.7 PERFORMANCE OF THE EPS SCIENTIFIC DATA ACQUISITION SYSTEM

Errors, introduced by the EPS Scientific Analog and Data Processor Systems fall into two catagories, those errors affecting counting rate measurements and those errors affecting spectrum shape measurements. The following quantitative analysis is limited by the accuracy of measurements made to date.

3.7.1 ERRORS AFFECTING COUNTING RATE ACCURACY

3.7.1.1 Data Roundoff

This source is exactly known. Compensation is possible within ±0.4% as allowed by statistical variations. The error arises from the detail of the digital readout. Since only the seven most significatn bits of any counter-memory module are telemetered per recording the worst case data loss occurs when the preceeding insignificant counter-memory bits are all in a logic one condition and is the value of the least significant recorded bit. The minimum error occurs when the preceeding insignificant bits are in a logic zero condition. This error is zero. An illustration of these two conditions is:

		MSB	
Maximum Error	0 . . . 0 0	1 0 0 0 0 0 0	1 1 1 1 1 1 1 1
Minimum Error	0 . . . 0 0	1 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	Nonrecorded Leading Zeroes	Recorded Information	Lost Information

Since, to a first approximation, all combinations of unrecorded bits are equally probable a simple solution is to arbitrarily increment the EPS digital output by one half the value of the least significant recorded bit. The error is now ± 1/2 least recorded significant bit.

3.7.1.2 Inaccuracy in Correction for Loss of Data Due to Pile-Up

Since the role of the EPS is to detect the random occurrance of charged particle events considerable care was exercised to insure proper performance in this regard. In nuclear particle detection systems measuring circuits exhibit a characteristic resolving time, τ. The effect of this resolving time is evidenced by an increasing loss of data as the true input count-rate increases. The mathematical relationship between the true counting-rate, R, and the measured counting-rate, r is generally taken to be:

$$R = \frac{r}{1 - \tau r}$$

In actual practice for systems operating at near capacity counting levels, τ is a complex function dependent upon the counting threshold value, input pulse height distribution, amplifier gain stability, amplifier offset stability and amplifier overload characteristics. τ has been experimentally determined for one set of conditions to be 1 ± .5μsec for the 360 nsec time constant amplifier. This value was determined for 1 Mev monoenergetic input signals and a counting threshold of 300 keV. Graph (Figure 1) of measured counting-rate as a function of true input counting-rate, is included. Optimum values will be determined for an assumed pulse height spectrum and known counting threshold values. The error due to this source will then be reduced to approximately ±3% for an input rate of 250,000/sec.

The total error to counting rate should be less than ±3.4% at counting rates up to 250,000/sec.

3.7.2 ERRORS AFFECTING SPECTRUM SHAPE MEASUREMENT

3.7.2.1 Counting Threshold Settability

The accuracy to which a counting threshold can be set is determined by the accuracy of calibration data and the resolution of the threshold control potentiometer. Calibration data is known to within ±0.5% and the potentiometer resolution allows ±1.0% control. The total settability then is good to ±1.0 ±0.5%.

3.7.2.2 Counting Threshold Changes due to Temperature Variation

Data collected to date indicate a change in counting threshold of $^{+3}_{-5}$% for a temperature range of -25°C to +50°C.

3.7.2.3 Counting Threshold Changes due to Power Supply Variation

Data collected to date indicate a change in counting threshold of 0.4% for worst case variation of all power supplies.

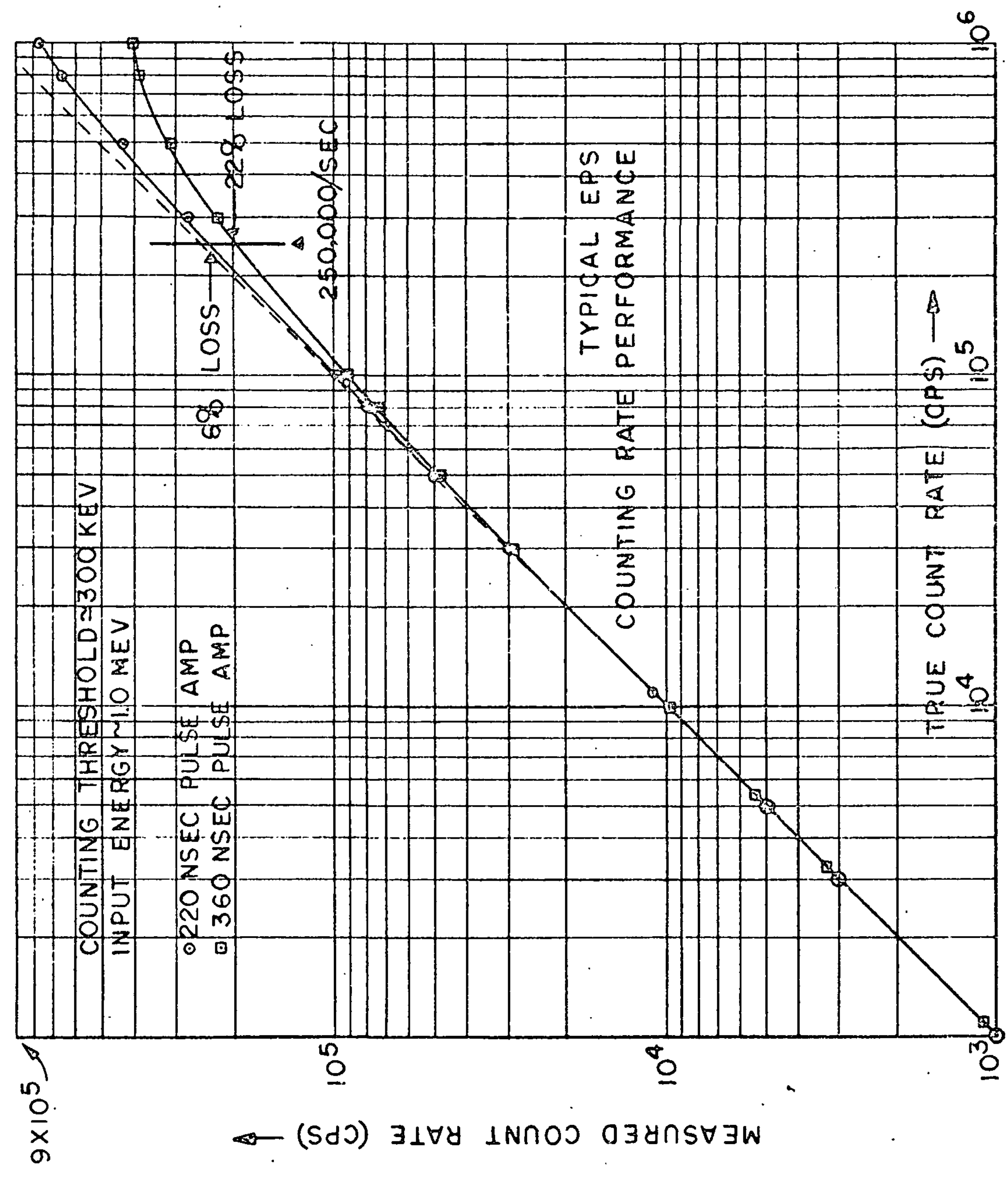


Figure 1 COUNTING RATE

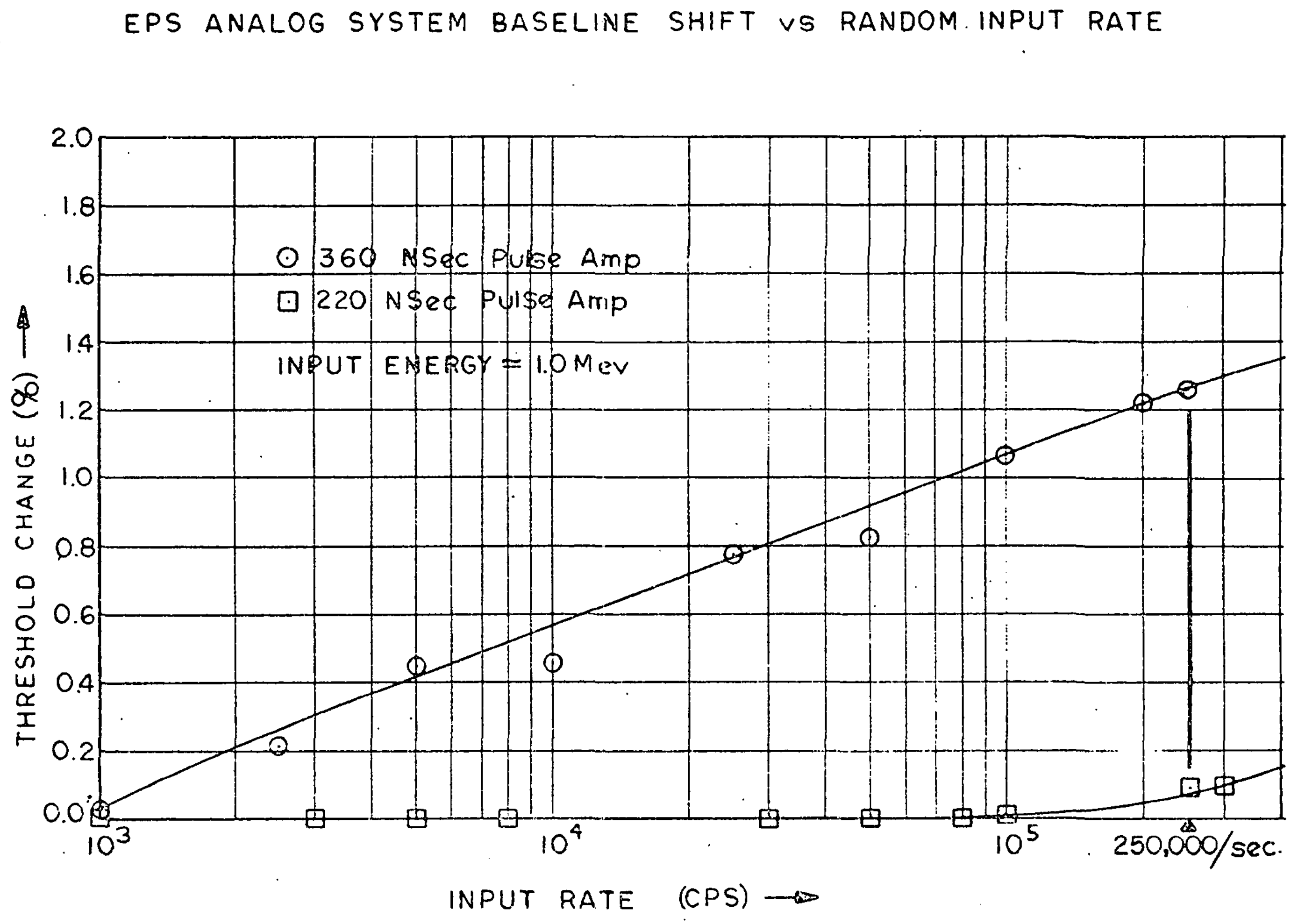
3.7.2.4 Counting Threshold Changes due to Random Input Signals

Data collected to date indicate a change in counting threshold of +1.3% for the 360 nsec time constant amplifier channel at an input rate of 250,000/sec. Similar data taken for the 220 nsec time constant amplifier channel indicate a threshold change of +0.3% (Figure 2 and 3).

The worst case threshold shift is $^{+6.2}_{-8.2}\%$ for the 360 nsec amplifier channels.

3.7.3 MAXIMUM EPS ANALOG ELECTRONIC SYSTEM ERROR SUMMARY

Error Type	
Counting-Rate Errors	
Data Roundoff	±0.4%
Pile-Up Correction	±3.0%
	3.4%
Spectral Shape Errors	
Counting Threshold Settability	±1.5%
Counting Threshold Temperature Variations	$^{+3.0}_{-5.0}\%$
Counting Threshold Power Supply Variation	±0.4%
Counting Threshold Rate Changes	+1.3%
	+6.2% -8.2%



EPS ANALOG SYSTEM BASELINE SHIFT vs RANDOM INPUT RATE

Figure 2 ANALOG SYSTEM BASELINE SHIFT VERSUS RANDOM INPUT RATE

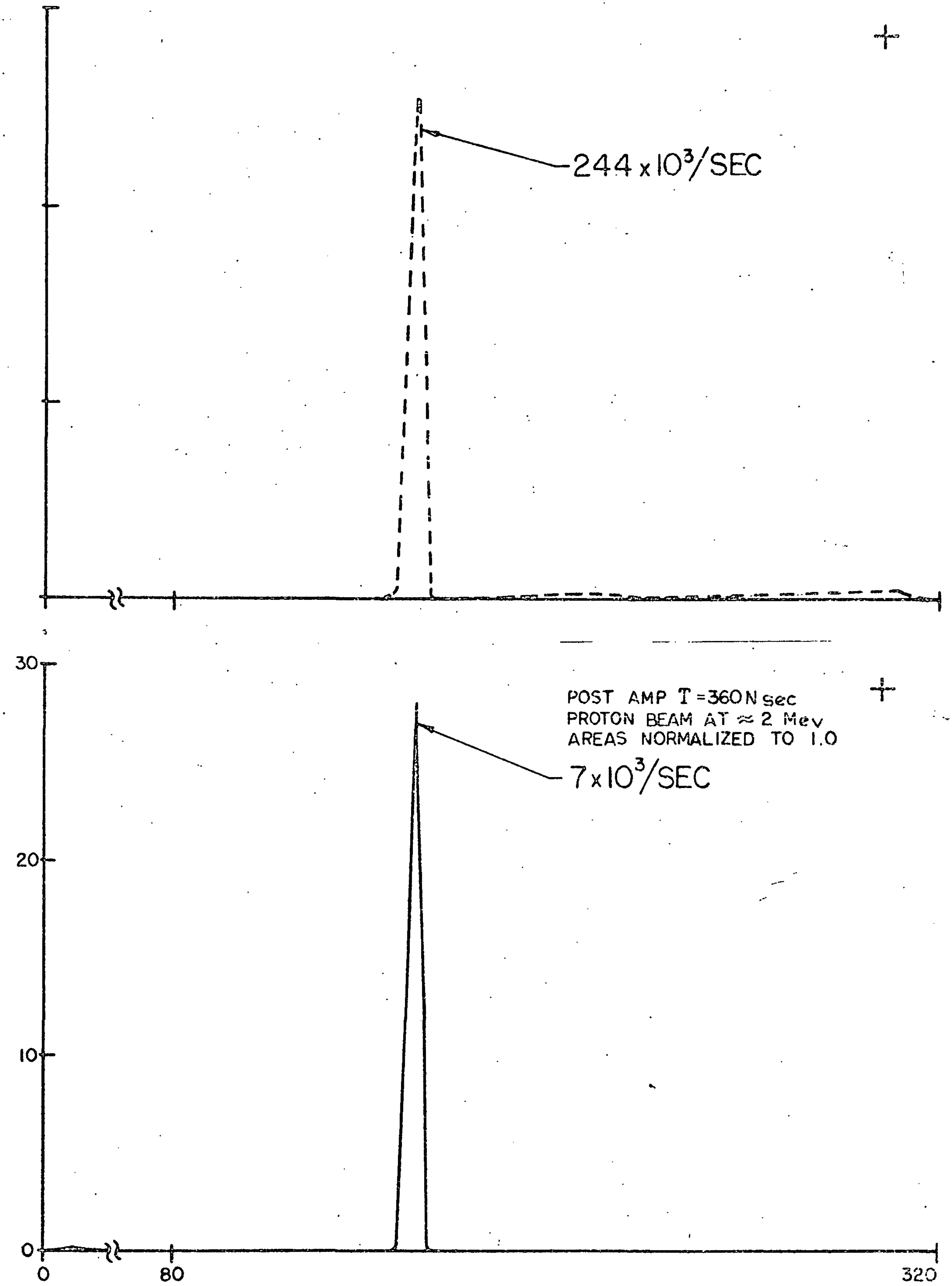


Figure 3 TYPICAL EPS DETECTOR/ANALOG ELECTRONICS END TO END PERFORMANCE AT 2 INPUT RATES

4. THERMAL DESIGN

The thermal design of the Electron-Proton Spectrometer is based on providing thermal control of the instrument by passive techniques for normal continuous operation. An integral heater for maintaining the instrument at survival temperature in the event of the need to reduce power to the instrument is provided. This heater may be used to provide additional heating during cold orbits if required.

4.1 THERMAL SPECIFICATION

Temperature limits for the Electron-Proton Spectrometer shall be:

	Operational	Survival
Detectors	-58°F to +50°F	-58°F to +122°F
Electronics	-13°F to +122°F	-58°F to +150°F

Available heater power = 6.0 watts.

The thermal design shall provide adequate thermal control for normal continuous operation of the EPS when not directly oriented toward the sun.

4.2 DETAILED THERMAL DESIGN

As can be seen from the thermal control diagram (Figure 1), the instrument is isolated from the spacecraft structure by means of glass-fibre bushings at each of the hold-down bolt locations. This minimizes the effect that variations in the spacecraft skin temperature has upon the instrument temperature. The vibration isolators, by virtue of their material (silicone rubber) and construction, provide additional isolation of the electronics package from the outer structure of the instrument.

The top plate and electronics package comprise a unit that is isolated thermally from the rest of the structure. The thermal interface between the two assemblies has been designed to provide a temperature gradient of 30 - 50° F since the electronics assembly is required to run warmer than the detectors. Cat-a-lac black enamel is applied to the two opposing faces in order that about 50% of the internal power be radiated to the top plate. Radiant coupling increases with temperature, thus tending to prevent exceedingly high or low temperatures in the electronics assembly. The remainder of the internal power is conducted to the top plate through four electrical grounding straps and twenty-one glass-fiber spacers, whose size and material have been selected to provide a controlled thermal conductance.

The heaters are mounted in the bottom slice of the electronics package, and their operation is controlled by an internal sensor monitoring the temperature of the electronics. The heaters are programmed to turn on when the electronics temperature reaches +32°F and turn off when the temperature has risen to +50°F.

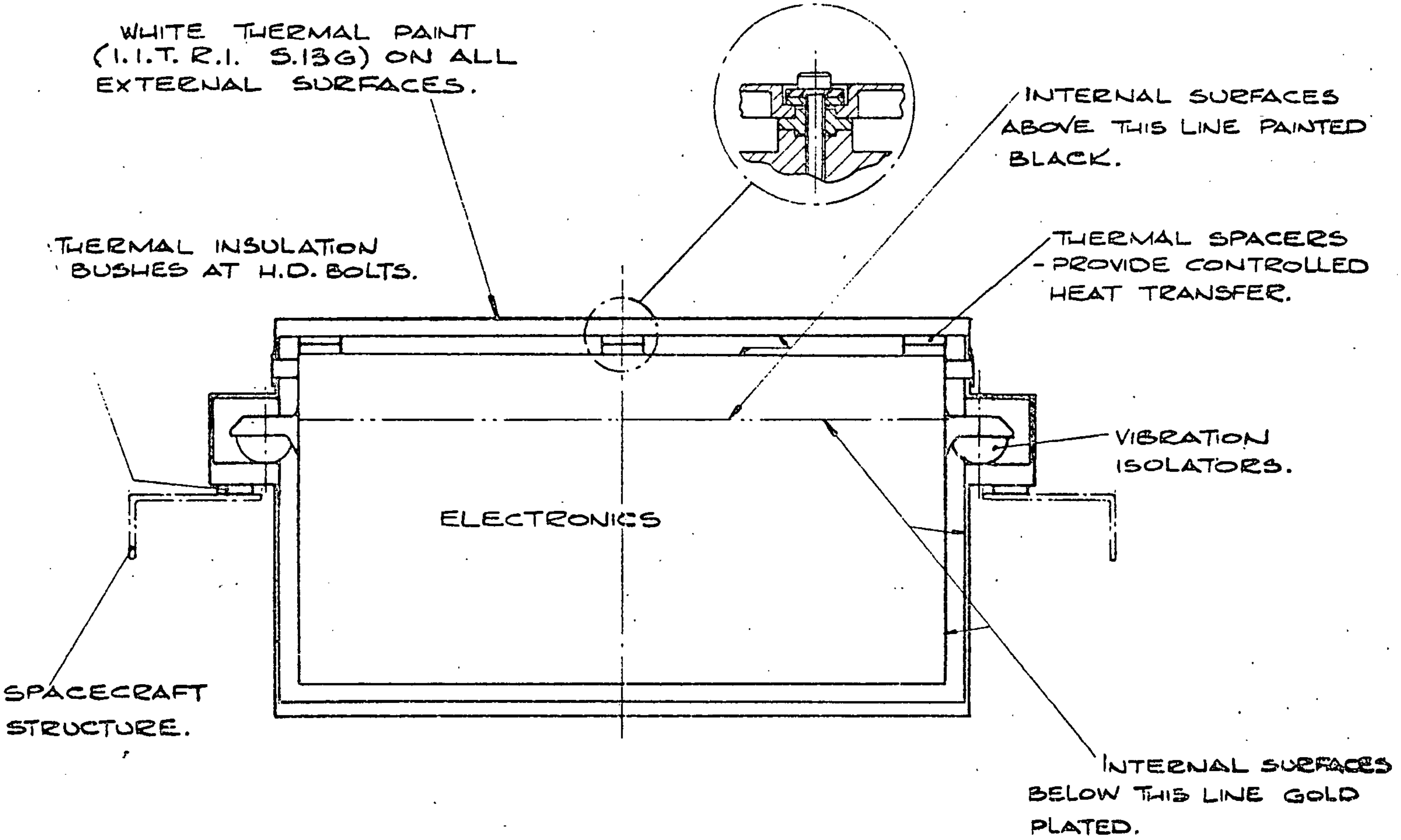


Figure 1 THERMAL CONTROL DIAGRAM

The anticipated temperatures for the Engineering Test Unit are shown in Table I.

TABLE I

EPS THERMAL VACUUM TEST - ANTICIPATED TEMPERATURES

			Power	Case (F°)	Det (F°)	Elect (F°)
1.	Cold - operating	B angle = 73 1/2°	13.4W	- 42F	- 12F	+ 20F
2.	Standby (6W heater)	B angle = 73 1/2°	6.3W	- 46F	- 52F	- 34F
3.	Standby - No Power	B angle = 73 1/2°	0W	- 50F	-100F	-100F
4.	Standby - No Power	B angle = 0°	0W			
5.	Hot - operating	B angle = 0°	13.4W	+ 56F	+ 28F	+ 79F
6.	Rendezvous & Docking	Direct sun exposure	0W	+120F	+ 75F	+ 75F
7.	Rendezvous & Docking	Direct sun exposure	13.4W	+120F	+130F	+170F
8.	Cold Operating	B angle = 73 1/2°	19.1W		+ 20F	+ 63F

4.3 THERMAL TEST UNIT RESULTS

For the thermal/vacuum test of the EPS Thermal Test Unit, seven test modes were run, simulating various flight conditions. These were:

Test Case 1.	Cold Orbit	(B = 73-1/2°)	13.4 W + 6W heater power available
Test Case 2.	Survival	(B = 73-1/2°)	6.0 W heater power only
Test Case 3.	Survival	(B = 73-1/2°)	No power
Test Case 4.	Survival	(B = 0°)	No power
Test Case 5.	Hot Orbit	(B = 0°)	13.4 W
Test Case 6.	Pre-Docking	(B = 73-1/2°)	Zero power
Test Case 7.	Pre-Docking	(B = 73-1/2°)	13.4 W

Heat inputs to the various test cases are shown in Table 2.

Test results for the detector and electronics temperature are as shown in the table of Table 3.

TABLE 2

HEAT LOADS AND BOUNDARY TEMPERATURES

TEST CASE	ABSORBED HEAT FLUX (BTU/HR-FT^2)		BOUNDARY TEMPERATURES (°F)	
	FRONT FACE	SIDES	SUPPORT PLATE	CAVITY
1	18.2	13.9	-75	0
2	18.2	13.9	-75	0
3	18.2	13.9	-75	0
4	26.8	12.9	-23	0
5	33.8	16.0	-23	75
6	128	13.9	250	75
7	128	13.9	250	75

TABLE 3
TEST RESULTS - THERMAL TEST UNIT

TEST CASE	FINAL TEMPERATURE	
	DETECTORS	ELECTRONICS
1	-24°F	54°F
2	-49°F	- 7°F
3	-73°F	-66°F
4	-45°F	-40°F
5	6°F	83°F
6	93°F	93°F
7	114°F	177°F

4.4 THERMAL ASPECTS OF DERATING REQUIREMENTS

During the design and development of the EPS printed circuit (pc) board and welded module subassemblies, due consideration was given to the elimination of thermal "hot spots" within these subsystems to comply with the derating requirements of the EPS. During the design and fabrication of the EPS Thermal Test Unit, an effort was also made to simulate, as close as possible, the actual heat profile of these subsystems. This was done, in part, to determine if there were components within certain subsystems, which might reach temperatures approaching the derating temperature limits of the electronic components.

Data from the thermal vacuum tests during a simulated "hot orbit" condition indicated that the pc board ground plane temperatures were only about 2°F higher than the 82°F temperature of the surrounding structure to which the boards were mounted. Evaluation and testing of the actual pc boards indicated that the worst-case "hot spot" of any pc board in the EPS was located on the discriminator pc board. This board contained two integrated circuits (IC); a SE526K Comparitor and a SNC5473T-03 dual flip-flop. These IC's experienced temperatures of 109°F and 136°F respectively which represented temperature increases of 25°F and 52°F above the pc board ground plane temperature (84°F).

The temperature of the data processor mother-board, measured during a simulated "hot orbit" condition, indicated that it was operating at 88°F, which was 6°F higher than the 82°F temperature of the surrounding structure to which it was mounted. The worst-case "hot spot" measured on the data processor was within the multiplexer module. This module dissipated 400 milliwatts and operated at a maximum temperature of 135°F, which was 47°F higher than the 88°F temperature of the mother-board.

5. MECHANICAL DESIGN

The mechanical design of the Electron-Proton Spectrometer is required to meet the Environmental ICD, NAR document MH04-02120-434 and the requirements of the end item specification. Additionally, the design must protect the electronics package from the extremes of the environmental requirements, where these are so severe as to be potentially damaging to the electronics, such as the random vibration requirements.

The intent has been to meet this requirement as simply as possible, using basic materials and making one component serve more than one function wherever possible. Many aspects of the design have been determined by thermal and packaging needs, together with the electronics requirements.

5.1 DESIGN SPECIFICATION

The environmental design specification is largely contained in the Environmental ICD, but portions of it are reproduced here. The basic requirements are random vibration, shock and acceleration. A pressure requirement also exists due to the controlled pressure leak from the spacecraft during launch.

The requirements for acceleration, vibration, shock, acoustic and pressure are shown in the accompanying Figures 1 through 6.

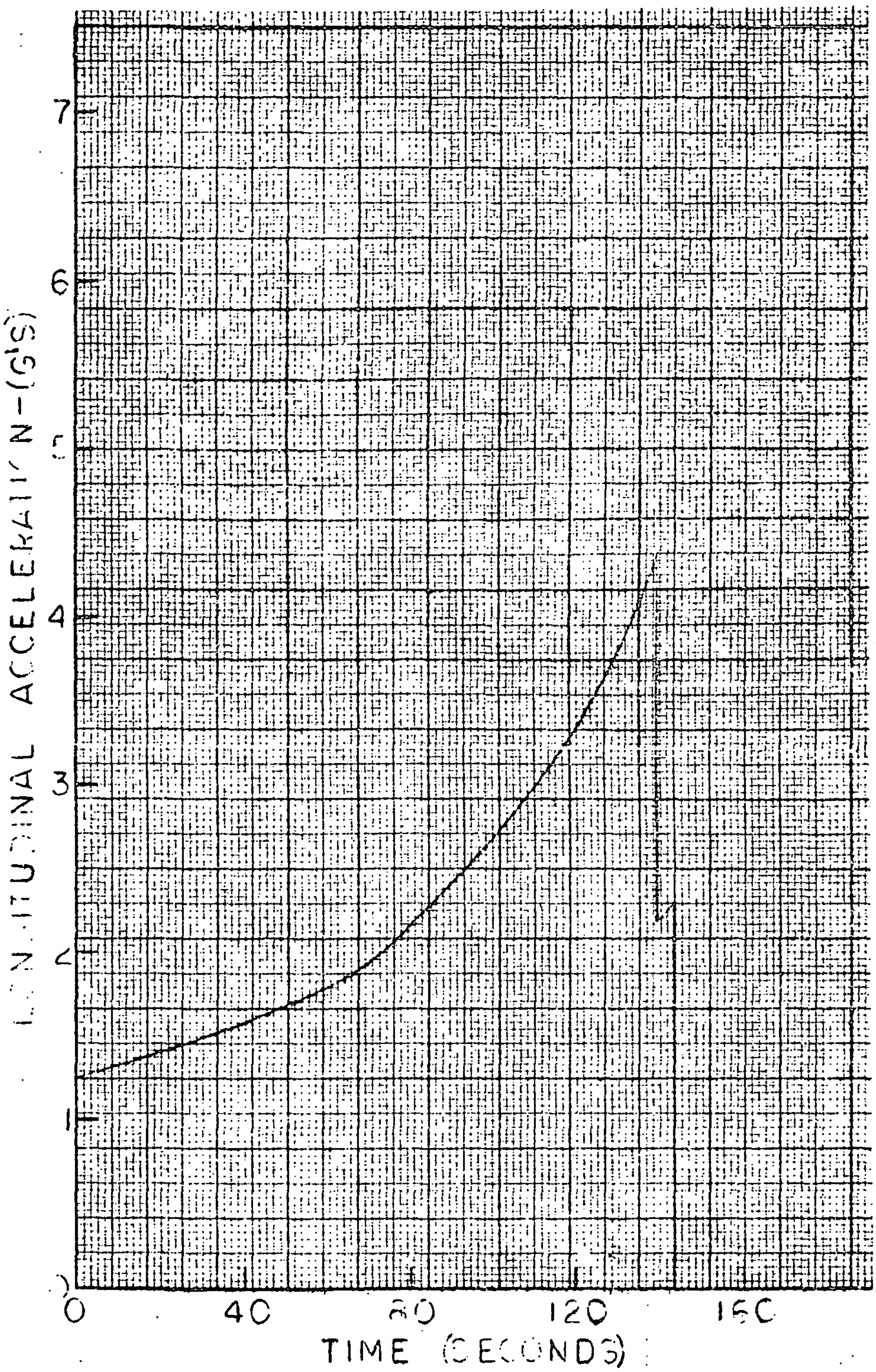


Figure 1. ACCELERATION - VARIATION WITH TIME.

Random:

R-Axis

Max Q and liftoff simulation - 80 seconds duration

20 to 175 Hz	+	9 dB/octave increase
175 to 350 Hz		6.0 g^2/Hz
350 to 2000 Hz	-	3 dB/octave decrease

Transonic/Mach 1 simulation - 10 seconds duration

20 to 175 Hz	+	9 dB/octave increase
175 to 350 Hz		10.0 g^2/Hz
350 to 2000 Hz	-	3 dB/octave decrease

X-Axis

20 to 75 Hz	+6 dB/oct increase
75 to 175 Hz	0.085 g^2/Hz
175 to 300 Hz	+6 dB/oct increase
300 to 1000 Hz	0.025 g^2/Hz
1000 to 2000 Hz	-6 dB/oct decrease

T-Axis

20 to 100 Hz	+6 dB/oct increase
100 to 440 Hz	0.04 g^2/Hz
440 to 600 Hz	+18 dB/oct increase
600 to 900 Hz	0.3 g^2/Hz
900 to 2000 Hz	-12 dB/oct decrease

The excitation shall act along each of the above axes for a duration of 80 seconds per axis. In addition, the spectral density shall be increased by 4 dB above the nominal for a duration of 10 seconds per axis.

Figure 2. VIBRATION QUALIFICATION LEVELS

Sinusoidal:

5-35 Hz @ ± .25 along each of three orthogonal axes as follows: Sweep at 3 octaves per minute from 5 to 35 to 5 Hz.

Figure 2. VIBRATION QUALIFICATION LEVELS
(Continued)

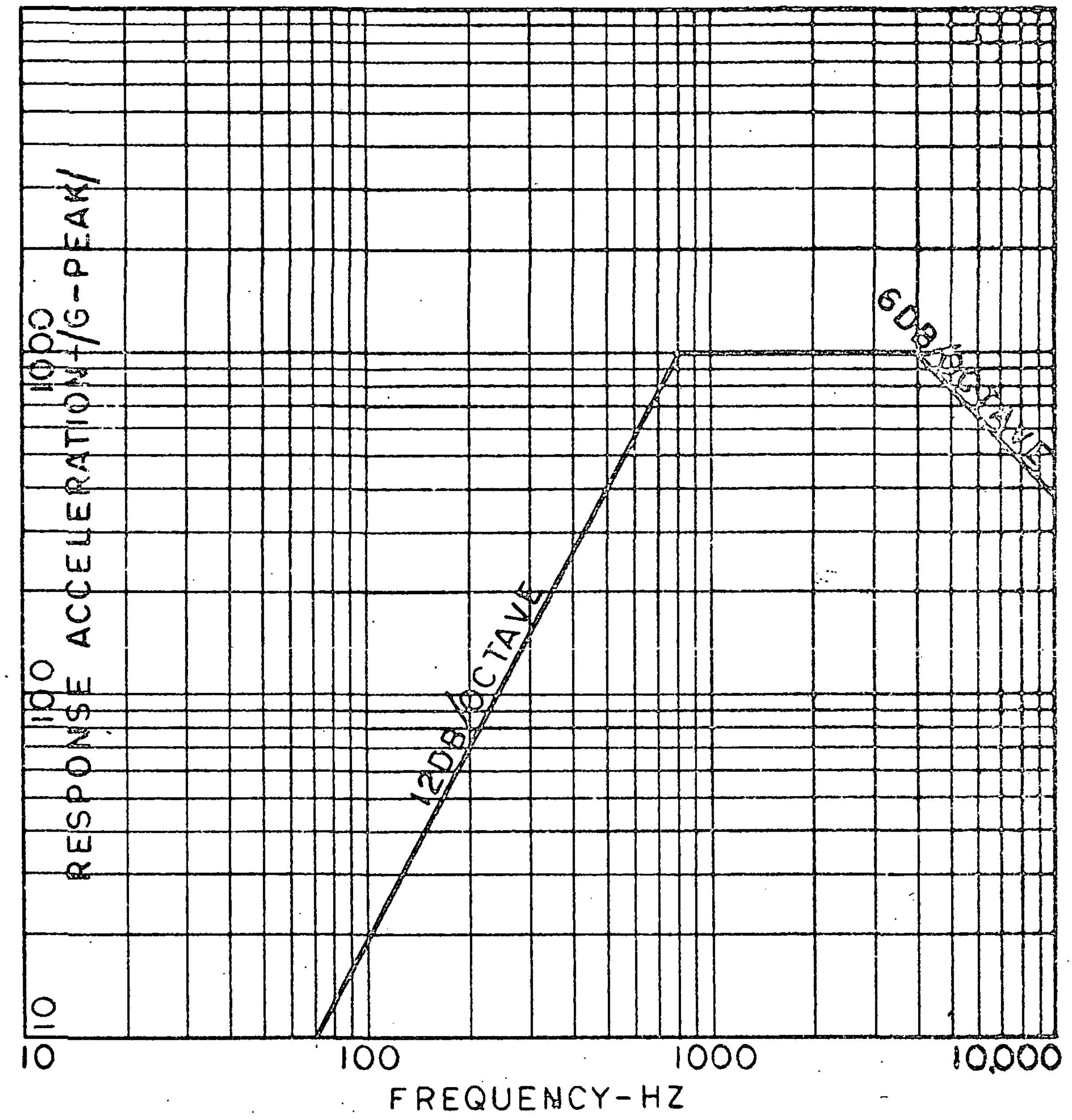
SHOCK

Qual. Test:- 20 g, 11 millisecond duration, terminal sawtooth to MIL-STD-810B, Method 516.1, Procedure 1.

Bench handling test to MIL-STD-810B, Method 516.1, Procedure V.

Additionally, to meet the requirement of the CSM fairing shock response spectrum.

Figure 3. SHOCK



CSM FAIRING

Figure 4. SHOCK RESPONSE SPECTRUM

ACOUSTIC ENVIRONMENT - CSM FAIRING EXTERNAL NOISE SPECTRA

1/3 OCTAVE BAND CENTER FREQUENCY (CPS)	1/3 OCTAVE BAND SOUND PRESSURE LEVEL - dBre 0.0002 uBar		
	BOOSTER ENGINE	MAXIMUM AERO-DYNAMIC PRESSURE	TRANSONIC BUFFETING
25	128	143	147
31.5	128	145	150
40	129	147	154
50	130	148	154
63	131	149	153
80	133	150	152
100	134	151	152
125	136	150	152
160	137	149	151
200	138	148	151
250	139	147	151
315	139	146	150
400	139	145	150
500	139	143	150
630	138	141	149
800	137	139	148
1000	136	137	147
1250	135	135	145
1600	134	133	143
2000	133	131	141
2500	132	129	139
3150	131	127	137
4000	130	125	135
5000	129	123	133
6300	128	121	131
8000	127	118	129
OVERALL	149	161	165

Figure 5. ACOUSTIC SPECIFICATION

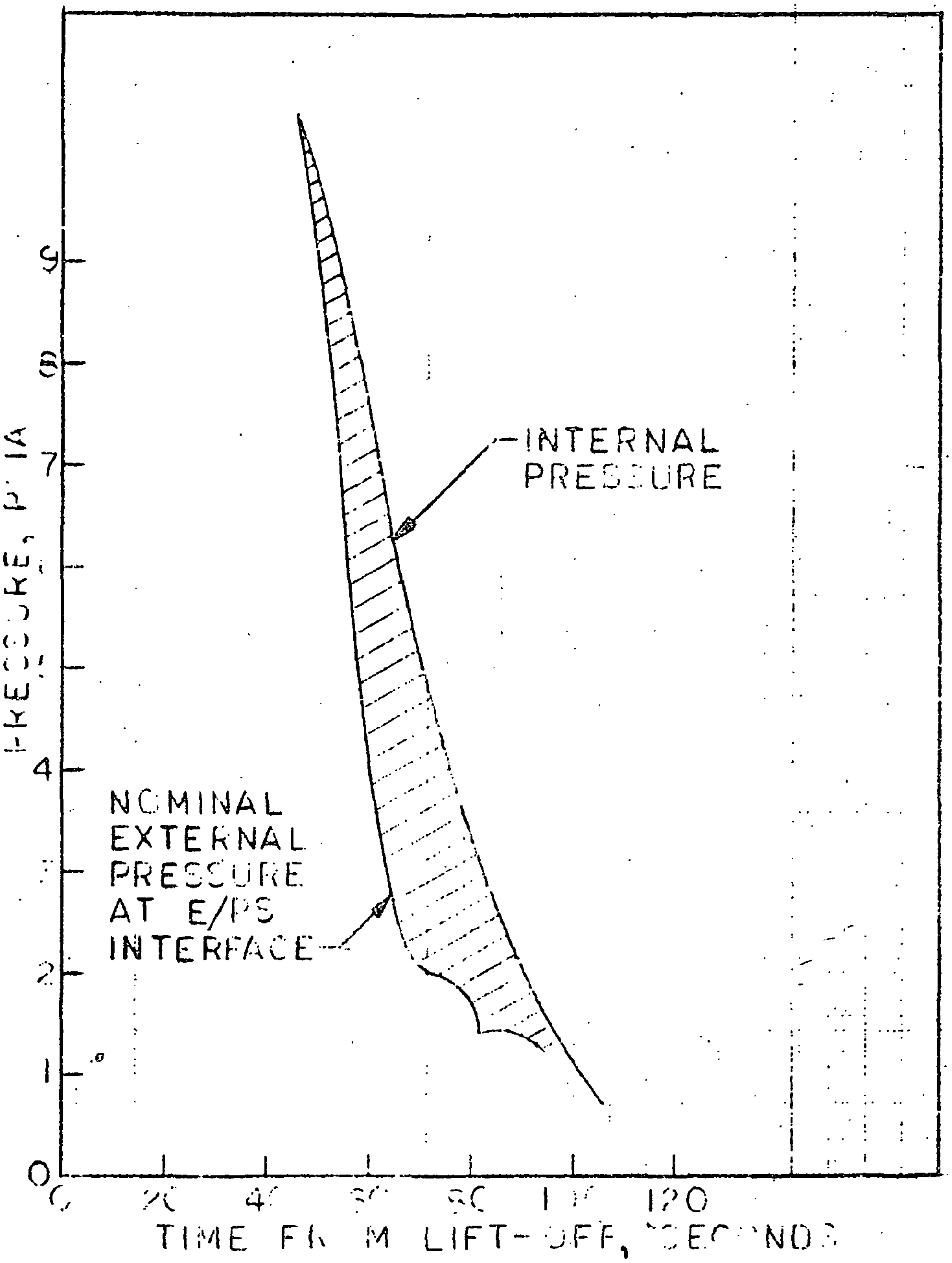


Figure 6. DIFFERENTIAL PRESSURE ON EPS

A pictorial representation of the instrument is shown in Figure 7, which indicates the axes of the instrument.

The instrument is required to meet the physical interface requirements of North American Rockwell drawing No. MH04-02118-134, Electron/Proton Spectrometer - Envelope/ Installation.

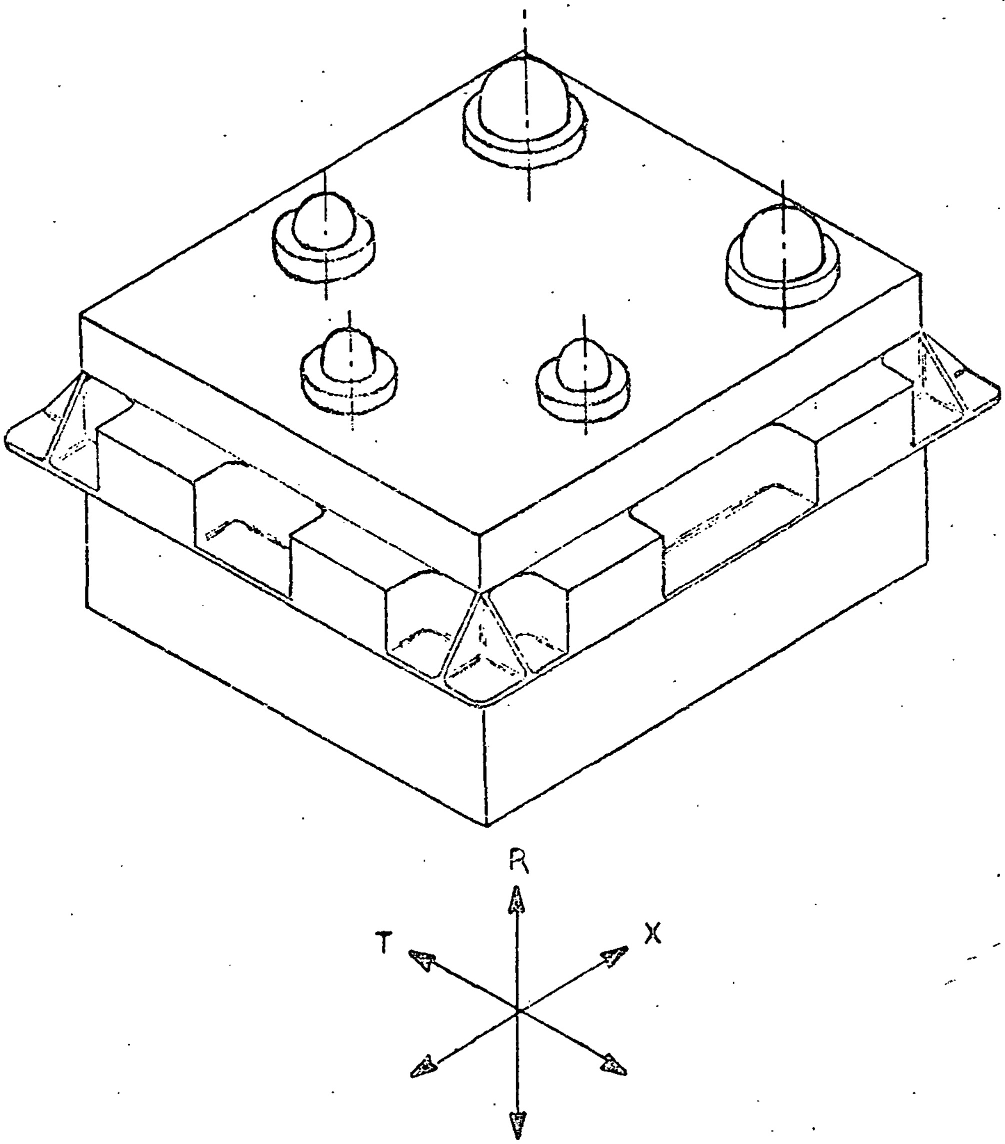


Figure 7. INSTRUMENT AXES

5.2 DETAILED MECHANICAL DESIGN

5.2.1 STRUCTURAL

As can be seen from Figure 8 Diagram of the EPS, the instrument package consists essentially of an outer housing and an electronics package.

The outer housing is combined with the mounting flange of the instrument, and is hard-mounted to the spacecraft support structure. As previously mentioned under thermal design, the mounting flange incorporates glass-fiber bushings at the hold-down bolt holes to isolate the instrument thermally from the spacecraft structure. Additionally, a silicon rubber 'O-ring' cord seal is provided on the underside of the flange to seal the 1/16" gap between the flange and spacecraft structure, to maintain N.A.R.'s differential pressure requirement for a controlled leak rate of the CSM. The baseplate is an integral part of the outer housing and carries the electrical connectors to interface with the spacecraft wiring. Two grounding straps are attached to the outer housing at two hold-down bolt locations and make contact with the spacecraft structure when the instrument is in position.

The electronics unit is supported within the outer housing by means of 8 vibration isolators. These isolators reduce the shock and vibration inputs to acceptable levels for survival of the various electronics within the unit, and also provide additional thermal and electrical isolation from the main structure.

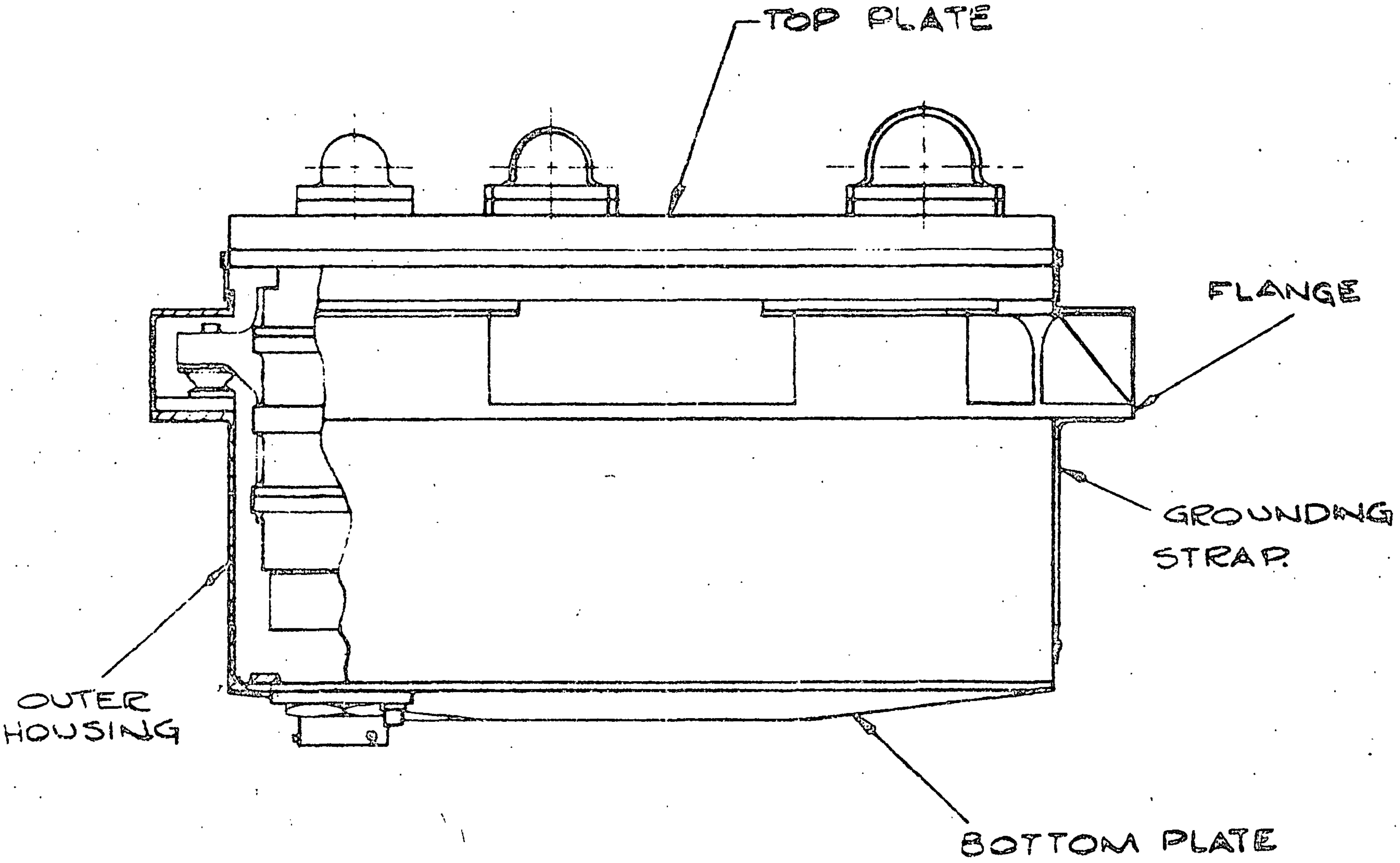


Figure 8. DIAGRAM OF EPS

The top plate and electronics housing comprise the electronics unit. Radiation detectors are mounted to the top plate and wired to their respective electronics, and the top plate is mounted on the electronics package as previously mentioned under thermal design. A reflective shield covers the gap between the top plate and outer housing required to accommodate the movement of the vibration isolators under shock, vibration and acceleration conditions. Figure 9, cross-section view of the EPS shows in more detail how the structure and electronics are arranged.

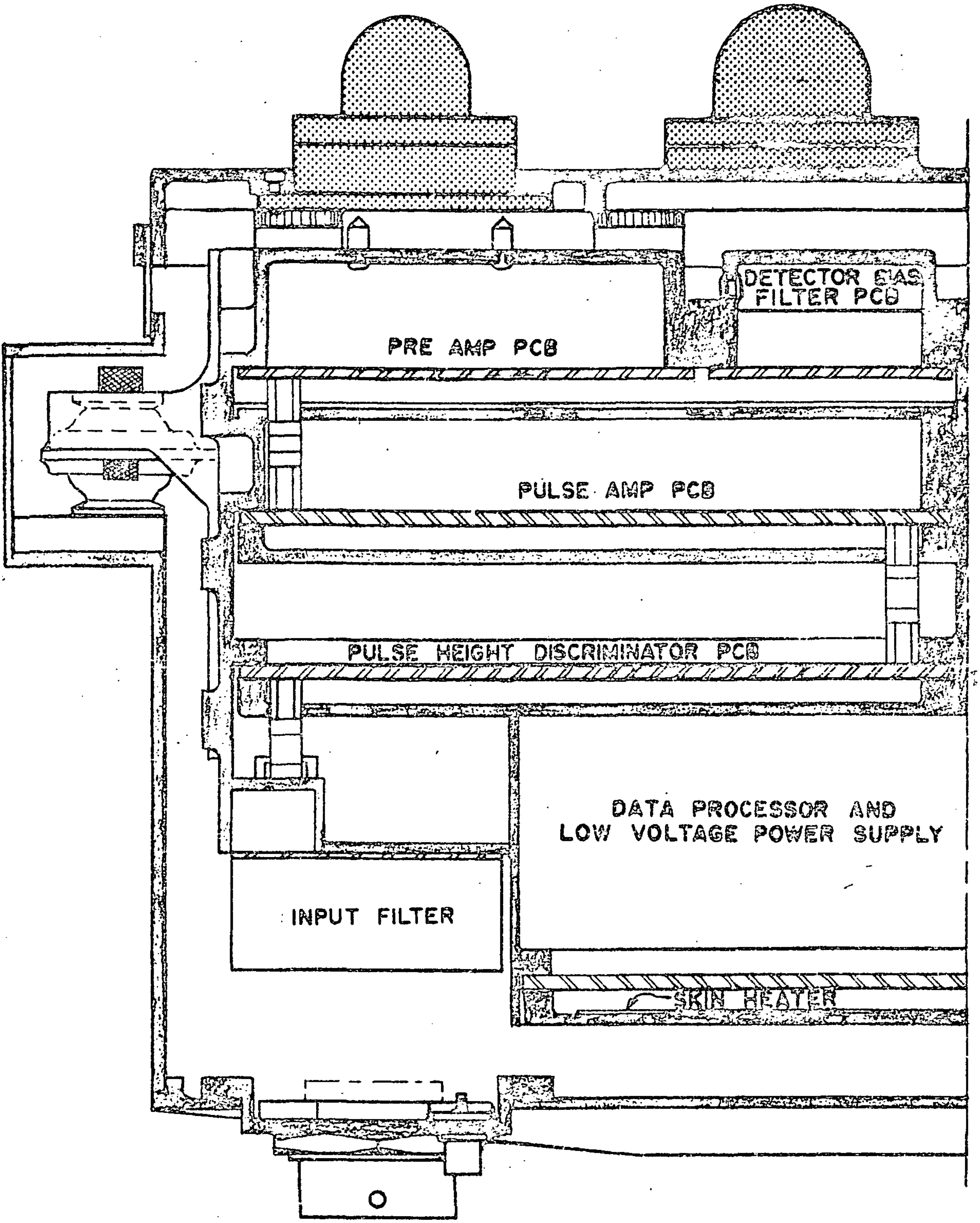


Figure 9. CROSS SECTION VIEW OF EPS

5.2.2 PACKAGING OF THE EPS

The Modular Electronic Packaging Design (Figure 10) made possible the separate development of the various portions as the circuit design for the individual functions became established.

Each slice incorporates its own housing, structural integrity, circuit board mounting thermal transfer paths, and its connectors.

Each slice is capable of being designed, built, assembled, and tested as an individual unit.

Each slice in the EPS has been designed for its electronic circuitry's own peculiar functional requirements.

Each printed circuit board mounts in a completely enclosed cavity in the slice (Figure 9). The cards' circuit ground plane around its perimeter is completely in contact with the slice mounting flange, thus providing excellent signal return and thermal transfer paths. This enables circuitry such as the detector bias supply, inherently noisy, to be placed in the pre-amplifier slice, avoiding any interference with the pre-amplifier's sensitive circuitry. Each of the five data channels are electrostatically shielded from each other as well as from the other circuitry. The exceedingly large common ground (Ground Plane) areas reduces noise pickup and capacitance and also serves as a thermal transfer path thus reducing component hotspots and at the same time providing structural integrity at minimum weight.

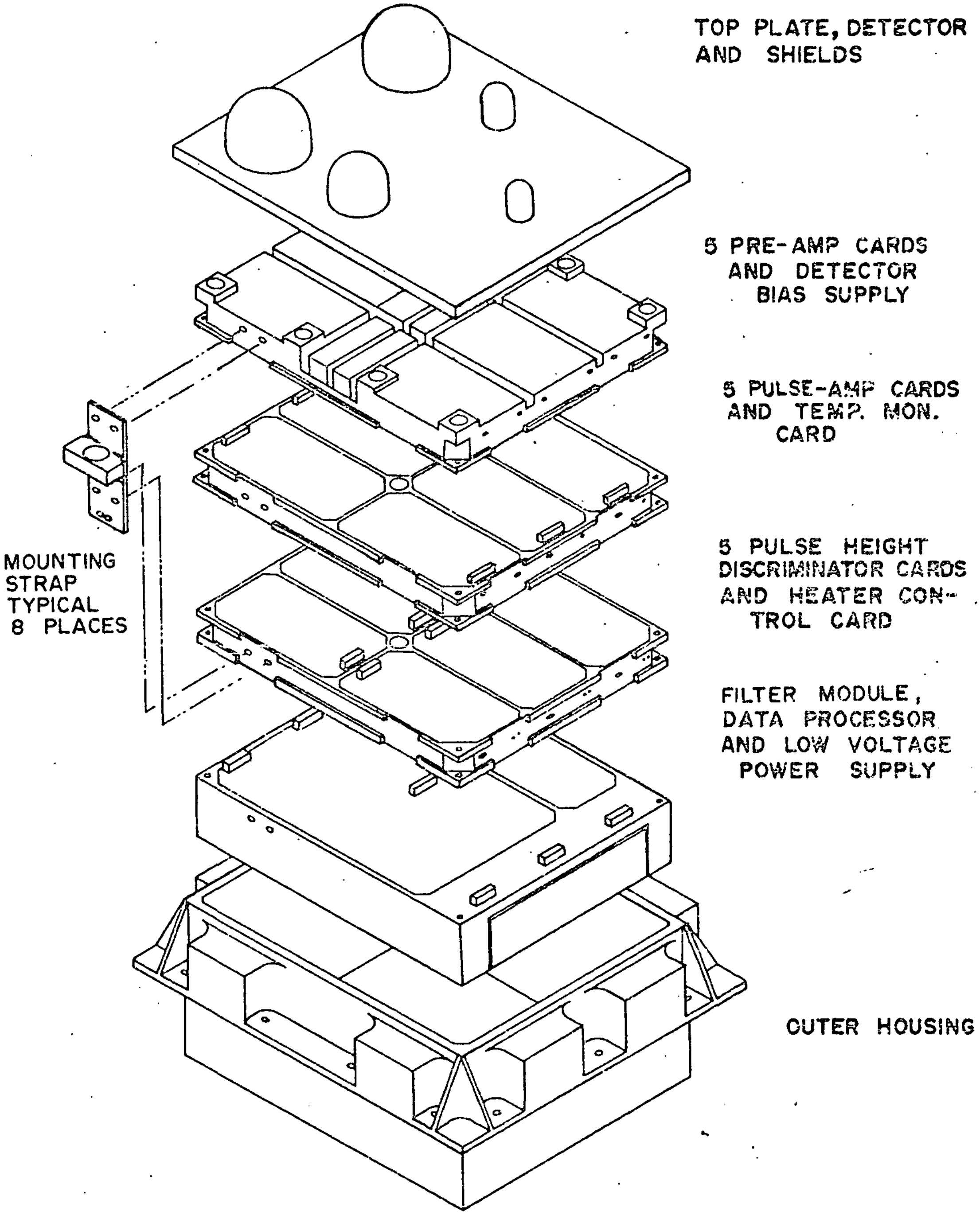


Figure 10. PACKAGING CONCEPT OF ELECTRON-PROTON SPECTROMETER

Each slice housing serves as a basic structure for the assembly, a chasis for mounting circuit boards and parts, a transfer medium for signal return, thermal heat sink, and shielding for electrostatic interference protection.

As can readily be seen, the slice housing must be fabricated as a precision machined unit. Each slice is machined from a solid billet of 6061-T651 aluminum alloy, chosen for its structural strength, light weight, thermal conductivity, machineability, and nominal cost. Such a fabrication design would have been prohibitively costly only a few years ago. However, today, with many common features between the slices and with tape-driven numerical-control machine tools, the costs are drastically reduced. Its cost effectiveness increases on the basis of design advantages and in comparison with other types of construction.

Among the advantages offered by this packaging design are:

- Provides accessibility to printed circuit boards and their components.
- Permits removal and replacement on individual slices without rewiring.
- Enabled the utilization of one printed circuit board layout for the detector bias filter, pre-amp, post amp, pulse height discriminator.

The slice module concept, as described, demonstrates its value in providing a soundly engineered packaging method for the many diverse types of circuitry required for the EPS, at the same time allowing for the changes and additions to circuitry without excessive delays in the delivery schedule.

5.3 MECHANICAL PERFORMANCE

The Qualification Test Unit of the EPS has been subjected to the random vibration criteria of qualification test requirements and successfully withstood the levels imposed. The instrument withstood Sinusoidal scans at 3 octave/min. from 5 - 35 Hz at .25 g without ill effects.

Additionally, the 20 g, 11 millisecond, terminal saw-tooth shock test has been conducted on the Qualification Test Unit with no problems.

Typical responses of the electronic package to the random vibration input at the high energy level (4 dB above nominal) were:

R axis	6.9 g rms	The responses are relatively higher in the X- and T-axes due to lower damping ratio in these axes
X axis	7.0 g rms	
T axis	4.0 g rms	

In response to the shock pulse, the electronics package response was in the order of 10 - 15 g peaks.

PACKAGING SPECIFICATION

1. Mechanical Requirements
   - A. Lightweight yet sufficiently rigid to withstand vibration environment of spacecraft.
   - B. Stress-relieving all solder connections on printed circuit boards.
2. Thermal Considerations

   Good internal heat transfer for electrical components providing adequate thermal management.
3. Electrical Requirements
   - A. Excellent shielding between analog circuitry and data channels.
   - B. A good common high frequency signal return path for the analog circuitry.
4. Cost/Functional Considerations
   - A. Modular packaging concept allowing for design and fabrication of each circuit through tests independent of other circuitry or changes elsewhere in the instrument.
   - B. Standarization of common printed circuit boards and other circuitry for minimum design, fabrication time, and minimum spare assembly requirements.
   - C. Access to circuitry test points, and adjustable components and easy maintenance.
   - D. Use of welded cordwood modules for circuitry requiring high packaging density for weight consideration.