Contract Final Report For Development of High Temperature, High Radiation Resistant Silicon Semiconductors

Ref. DCN 1-0-40-02692
Contract # NAS8-25917

Submitted to:

George C. Marshall Space Flight Center
National Aeronautics & Space Administration
Marshall Space Flight Center
Huntsville, Alabama 35812

Submitted by:

Solitron Devices, Inc.
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I. OBJECTIVE

The objective of this contract is to design, develop and fabricate a hardened power transistor that will meet or exceed the performance requirements of future electronic systems that must operate in severe nuclear space radiation environments.

Many space and missile programs are limited by the susceptibility of semiconductors to radiation damage. Of the semiconductor devices, power transistors are usually the most difficult to harden and therefore limit the hardness of an electronic system. There are now a number of design and processing techniques that can be applied to improve their post-radiation gain, saturation voltage and second breakdown characteristics for a range of currents and voltages.

Today, silicon planar transistors can be expected to degrade but to retain useful performance characteristics in the range of 1×10^{14} n/cm^2 to 1×10^{15} n/cm^2, with signal devices remaining capable of operating in the top half of the decade, but with power transistors falling in the bottom half of the decade. Since the gain of power devices after irradiation can now be made comparable to signal devices for large applied voltages by shallow base diffusion, the proposed effort concentrates on the additional requirements for power transistors of gain fall-off at high currents, saturation voltage and high temperature performance.

II. Device Hardness and Diffusion Technique

Past experience in the field of radiation hardened devices indicates that current gain is the key parameter to be considered in hardening transistors. A model which relates changes in gain to neutron fluence levels is expressed by:

$$\frac{1}{h_{FE_p}} - \frac{1}{h_{FE_o}} = K\tau_B \quad (\Phi_2 - \Phi_1)$$

which is an expression of the gain degredation $\frac{1}{h_{FE_p}} - \frac{1}{h_{FE_o}}$ as a function of:

a) the radiation fluence level $(\Phi_2 - \Phi_1)$

b) the base transit time (τ_B)

c) the radiation damage factor K.

Of these factors the only one with which the designer has any real freedom is the base transit time τ_B.

$$\tau_B = \frac{W^2}{2 D_{nB}}$$

where W = base width

D_{nB} = Diffusion Const. for electrons in base.

The main objective is to minimize the base transit time τ_B by controlling the base width of the device. This dimension can only be optimized to the limit of the voltage requirement of the application. Some effect on τ_B can also be had by changing the diffusion constant D_{nB} by various base doping modifications. Lower base concentrations tend to decrease D_{nB} but will also lower the maximum operating voltage of the device.

In order to obtain the intrinsic base transit time the gain bandwidth product must be measured at different current levels in the linear region and plotted. However, using f_t as the parameter to obtain the base transit time is not completely accurate. From the expression

$$\frac{1}{2\pi f_t} = \frac{1}{KQ} \qquad \frac{KT}{qI_e} \quad (C_{TE} + C_{TC}) + \frac{B}{2.43}$$

it can be seen that f_t is also a function of the emitter and collector junction Capacitances while τ_B is a physical property of the base.

The direct measurement of the base width W_B is a better indicator of τ_B than the above method. The Solitron device hardness is achieved by maximum base width control. Production lots are limited in size and one wafer is used as a control, this wafer is sectioned after base and emitter diffusion. The base width is measured by interference technique. Using these techniques the base width can be controlled quite easily. The devices will be double diffused NPN Silicon types. Because of the narrow highly doped base region required shallow diffusion techniques will be necessary. Solitron is using its programmed emitter diffusion techniques for these devices. This technique affords maximum reproducibility to the process. It is estimated that a base width W_B of approximately .3μ and a base doping of about 3×10^{18} atoms/cc will be needed to meet the transistor design goals of breakdown voltage and gain.

III. SCOPE OF WORK

A. 100 Ampere Transistor

Three geometries were investigated to determine which one would be best for the 100 ampere operation. The chips were designated as the 7R, 8R and 8R-DA. The geometrical details are shown in table 1.

Chip Type	Die Size (mils)	Base area $(mils)^2$	Emitter area $(mils)^2$	Emitter periphery (mils)	$EP/_{EA}$
7R	140 x 170	10,912	4,800	5,040	1.05
8R	266 x 276	57,584	29,776	5,674	0.19
8R-DA	244 x 213	40,953	18,271	2,408	0.13
3R	80 x 120	6,370	1,602	3,612	0.45
6R	120 x 160	12,740	3,204	7,224	0.45

Table 1

Geometrical Details of Hardened Power Transistor Chips.

The 8R chip geometry did not produce any devices suitable to the 100 amp application. It was found that the base area was too large to support the shallow diffusion (1.5μ-1.9μ) necessary for radiation resistance. The problem was that any type of microscopic contamination would mask the diffusion causing low breakdown voltages or collector to emitter shorts after the emitter was diffused. This type of problem is not as critical for normal power devices because the deep base diffusions ($\approx$10μ) in most cases will diffuse under microscopic contamination and wipe out its effect. The same problem was experienced with the 8R-DA chip. The base area was just too large to support the radiation type diffusion.

The 7R chip geometry proved more feasible due to the smaller total area and the design of the chip. It incorporates two bases diffused into the chip which made up the total area. This kept the possiblity of microscopic contamination to a minimum and a successful radiation type diffusion was accomplished.

This 7R geometry incorporates an interdigitated structure of sixty emitter stripes each forty mils in length and one mil in width. This is to maximize the device emitter periphery in

order to minimize the phenomenon of emitter edge injection at high current levels which would cause excessive gain degradation when subjected to a high energy neutron environment.

The radiation type diffusion that was originally proposed was for a base width of approximately 0.3U. This base width, however, was found to be too narrow for a large area device to yield any transistors with a 90 volt BVceo. In order to sustain this breakdown voltage, the base width had to be increased to a range of 0.6μ tp 0.8μ. This range should be adequate for a neutron flux density in the upper decade of the range from 1×10^{14} n/cm^2 to 1×10^{15} n/cm^2.

Since the 7R chip is a 25 Amp chip, it was proposed that this chip would be used as a unit cell and that the 100 amp capability would be accomplished by paralleling a number of these chips to reach the required capability. This is common practice in the power transistor field, however, care must be exercised to match the chips for BVceo and gain. The chips for this contract were matched for BVceo within five volts and the gain was matched within 5% at 5 volts/500 ma.

Devices were assembled to ascertain the number of chips needed in parallel to reach the 100 amp capacity. Six units with two chips were assembled and four units with three chips were assembled, all in the TO-114 package. Electrical tests indicated that the best that could be expected from these devices was 70 amp operation (see data) at room temperature. Since the TO-114 package will not hold more than three chips comfortably, it was decided to try the HKCG motor control package which was in development for a NASA project and would accept a greater number of chips. A one month delay was experienced in this portion of the project waiting for a package to become available.

An HKCG motor control package was assembled with four chips in parallel. This assembly did not meet the 100 Amp requirement due to contamination of a source gas during fabrication. No other packages were available at this time and a three months delay in this portion of the project was experienced before more packages became available. It should be noted that Solitron was

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TEST DATA SHEET

TYPE 7R LOT NO. 4 LOT SIZE _____ SAMPLE SIZE _____ RELIABILITY ○ PAGE _____ OF _____

CUSTOMER NASA CUSTOMER P. O. _____ TESTER _____ PRE-SHIP INSP. ○ FINAL INSP. ○ DATE _____

PARAMETER		V_{CBO}	V_{CEO} (SUS)	V_{EBO}	H_{FE}	H_{FE}	H_{FE}	H_{FE}	H_{FE}	H_{FE}	H_{FE}	H_{FE}	H_{FE}
TEMP. 25°C unless noted													
TEST EQUIPMENT NO.													
CONDITIONS		10 MA	100MA	10 uA	5V 500MA	5V 1A	5V 5A	5V 10A	5 V 20A	5V 30A	5V 40A	5V 50A	5V 60A
LIMITS	MIN.												
	MAX.												
UNITS OF MEASURE													
NO.	DATE CODE												
	#1	121	110	5.5	54	58	65	70	52	37	24	17	12.5
	#2	112	87	3.4	135	145	150	150	100	48	33	20	15
		H_{FE}	H_{FE}	H_{FE}	H_{FE}	$V_{CE(S)}$	$V_{CE(S)}$	$V_{CE(S)}$	$V_{CE(S)}$	$V_{CE(S)}$	$V_{CE(S)}$	$V_{CE(S)}$	$V_{CE(S)}$
		5V	5V	5V	5V	1A	5A	10A	20A	30A	40A	50A	60A
		70A	80A	90A	100A	100MA	500MA	1A	2A	3A	4A	5A	6A
	#1	10	8.5	7	6	0.08 V	0.24V	0.39V	0.62 V	0.85V	1.05 V	1.35 V	3.4 V
	#2	12	9.5	8	6.5	0.06V	0.19 V	0.36 V	0.59V	0.80V	0.98 V	1.20V	1.6V
		$V_{CE(S)}$											
		70A											
		7A											
	#1	4.4 V											
	#2	2.8 V											

fabricating these packages from raw materials for another NASA contract which had priority on their availability.

When the package problem eased, assembly procedures were started again. No problems were encountered in mounting the chips in the package but problems were experienced in hermetically sealing the package. The method of sealing that was used was to braze the cap onto the package utilizing a gold-germanium preform at 385°C in a hydrogen atmosphere. It was found that the hydrogen was absorbed in the oxide surface of the chip causing an inversion type surface electrical leakage. The unit recovered when the cap was removed and then vacuum baked at 300°C.

The obvious method of correcting this problem, that of coating the transistor chips with a silicone resin, is not feasible as the resin will not withstand a high radiation fluence level. However, a package consisting of six chips in the HKCG motor control package was assembled with varnish coating in order to secure electrical data. The device was tested for H_{FE}, V_{CE} (sat) and V_{BE} (sat) in increments up to 120 amps (see data). The device was destroyed in attempting to test above 120 amps.

Since the HKCG package presented sealing problems, six low voltage chips were assembled in a TO-68 weldable package and tested for 100 amp capability. at room temperature. The tests on this unit was favorable so assembly was begun on the twenty devices to satisfy the terms of the contract.

It was found that this package configuration would support 90 Volt Vceo (sus) at 100 amps but would fail randomly at higher temperatures. The maximum temperature achieved before failure was 210°C and the minimum was 125°C. Ten of these devices were submitted to NASA-MSFC for critical analysis. The mechanism appears to be thermal stress causing the weakest chip to go into secondary breakdown. This causes the current load to avalanche to the other chips causing complete destruction.

It was felt that a redesign of the package was necessary. The proposed package would incorporate eight transistor chips to further reduce the load on each individual chip and a much heavier copper base than the TO-68 to help dissipate the heat from the chips.

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TEST DATA SHEET

TYPE 7R-HKCG LOT NO. _____ LOT SIZE _____ SAMPLE SIZE _____ RELIABILITY ○ PAGE 1 OF 1

CUSTOMER N.P.S.A CUSTOMER P. O. _____ TESTER SH PRE-SHIP INSP. ○ DATE 5-16-91

FINAL INSP. ○

PARAMETER			h_{FE}	h_{FE}	h_{FE}	h_{FE}	h_{FE}	h_{FE}	h_{FE}				
TEMP. 25°C unless noted													
TEST EQUIPMENT NO.													
CONDITIONS			I_C=10A	I_C=20A	I_C=40A	I_C=60A	I_C=80A	I_C=100A	I_C=120A				
			V_{CE}=5V	V_{CE}=5V	V_{CE}=5V	V_{CE}=5V	V_{CE}=5V	V_{CE}=5V	V_{CE}=5V				
LIMITS	MIN.												
	MAX.												
UNITS OF MEASURE													
NO.	DATE CODE												
			132	132	83	60	33	22	16				
			$V_{CE(s)}$										
			10:1										
			0.10V	0.16V	0.30V	0.43V	0.60V	0.80V	1.05V				
			$V_{BE(s)}$										
			10:1										
			0.80V	0.87V	1.02V	1.14V	1.28V	1.38V	1.50V				
			$V_{CEO(sus)}$	—	V_{CC} = 90V	R_L = 0.1Ω	I_C = 100A						
					t_p = 10μs	f = 0.01 Kc							

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TEST DATA SHEET

EVALUATION SAMPLES SES 2410

TYPE 100 AMP LOT NO. _____ LOT SIZE _____ SAMPLE SIZE _____ RELIABILITY ○ PRE-SHIP INSP. ○ FINAL INSP. ○ PAGE 1 OF 2

CUSTOMER NASA CUSTOMER P. O. NAS8-25911 TESTER _____ DATE _____

PARAMETER		V_{CBO}	V_{EBO}	V_{CEO}	H_{FE}	H_{FE}	H_{FE}	H_{FE}	H_{FE}				
TEMP. 25°C unless noted													
TEST EQUIPMENT NO.													
CONDITIONS		1.0 MA	1.0 MA	50 MA	5V 10A	5V 25A	5V 50A	5V 75A	5V 100A				
LIMITS	MIN.												
	MAX.												
UNITS OF MEASURE		V	V	V									
NO.	DATE CODE												
1		112	6.0	116	80.5	74.5	67.5	45	31				
2		108	6.0	106	71	68	66.5	46	35				
3		108	6.0	92	104	94	98	64	47				
4		122	6.0	112	74	69	64.5	44	30				
5		112	6.0	91	124	109.5	99	64.5	46.5				
6		116	6.0	108	76.5	68	60	39	25				
7		114	5.7	110	80.5	74.5	67.5	43	28				
8		120	6.0	112	75	73.5	71	48	36				
9		120	6.0	114	71	67.5	67	49	38				
10		122	6.0	91	74.5	64	65	45.5	29				

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TEST DATA SHEET

EVALUATION SAMPLES SES 2410

TYPE 100 AMP LOT NO. _____ LOT SIZE _____ SAMPLE SIZE _____ RELIABILITY ○ PRE-SHIP INSP. ○ FINAL INSP. ○ PAGE 2 OF 2

CUSTOMER NASA CUSTOMER P. O. NAS 8-25917 TESTER _____ DATE _____

PARAMETER	$V_{CE(S)}$	$V_{BE(S)}$	$V_{CE(S)}$	$V_{BE(S)}$	$V_{CE(S)}$	$V_{BE(S)}$	$V_{CE(S)}$	$V_{BE(S)}$	$V_{CE(S)}$	$V_{BE(S)}$	$V_{CE(S)}$	$V_{BE(S)}$
TEMP. 25°C unless noted												
TEST EQUIPMENT NO.												
CONDITIONS	10A 1A	10A 1A	25A 2.5A	25A 2.5A	50A 5A	50A 5A	75A 7.5A	75A 7.5A	85A 8.5A	85A 8.5A	95A * 9.5A	95A * 9.5A
LIMITS MIN.												
LIMITS MAX.												
UNITS OF MEASURE	V	V	V	V	V	V	V	V	V	V	V	V
NO. / DATE CODE												
1	0.084	0.775	0.190	0.845	0.270	0.980	0.405	1.03	0.460	1.06	0.535	1.10
2	0.085	0.780	0.185	0.840	0.240	0.970	0.345	1.02	0.385	1.05	0.520	1.09
3	0.072	0.775	0.155	0.840	0.230	0.960	0.325	1.01	0.360	1.04	0.410	1.08
4	0.079	0.780	0.175	0.845	0.240	0.970	0.345	1.02	0.385	1.05	0.450	1.09
5	0.072	0.775	0.150	0.835	0.210	0.950	0.310	1.00	0.335	1.03	0.390	1.05
6	0.090	0.785	0.205	0.855	0.275	0.990	0.415	1.055	0.470	1.09	0.575	1.13
7	0.085	0.790	0.190	0.865	0.285	1.00	0.430	1.09	0.490	1.12	0.575	0.175
8	0.075	0.770	0.165	0.838	0.225	0.950	0.320	1.00	0.350	1.02	0.410	1.06
9	0.075	0.775	0.130	0.860	0.218	0.960	0.310	1.01	0.330	1.02	0.395	1.09
10	0.092	0.770	0.150	0.850	0.220	0.945	0.318	1.00	0.355	1.03	0.410	1.05
*	LIMIT OF TEST EQUIPMENT USED											

This new package was designed and fabricated and twenty-six devices were assembled for testing. When attempting to test these units for BVceo (sus), it was found that they were prone to severe oscillation. In fact the oscillation was so severe that it was impossible to test them, even at room temperature, without destroying them. It is felt that the oscillation was caused by the additional wiring made necessary by increasing the number of chips from six to eight since it was not observed on any of the devices previously tested. In addition, some of the chips used to fabricate these devices were from the same diffusion runs that provided chips for the devices in the TO-68 package. Twenty of these devices were submitted to NASA-MSFC to satisfy the requirements of this contract.

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INVOICE TO
NASA
George C. Marshall Space Flight Center
Marshall Space Flight Center
Alabama 35812

SHIP TO
same
Accountable Property Officer
Bldg. 4471

TERMS - ½% 10, NET 30 DAYS
F.O.B. RIVIERA BEACH, FLORIDA

OUR ORDER NUMBER	CUSTOMER ORDER NUMBER	SHIPPED VIA	REPRESENTATIVE	INVOICE DATE	DATE PROMISED
T-26-72	NAS8-25917	Hand Carry-R. Howard T-27-72		8-1-72	8-2-72

QUANTITY ORDERED	QUANTITY BACKORDERED	QUANTITY SHIPPED	DESCRIPTION	UNIT PRICE	AMOUNT
20		20	NASA Contract NAS8-25917 DCN 1-0-40-02692, & S1 High Power Transistors with read and record data (Exhibit A, Para. A)		

WE HEREBY CERTIFY THAT THESE GOODS WERE PRODUCED IN COMPLIANCE WITH ALL APPLICABLE REQUIREMENTS OF SECTIONS 6, 7 AND 12 OF THE FAIR LABOR STANDARDS ACT AS AMENDED AND OF REGULATIONS AND ORDERS OF THE UNITED STATES DEPARTMENT OF LABOR ISSUED UNDER SECTION 14 THEREOF.

ALL GOODS SHIPPED BY US AT CONSIGNEE'S RISK AFTER WE HAVE DELIVERED TO TRANSPORTATION COMPANY AND TAKEN RECEIPT FOR SAME

REJECTION OF ANY SHIPMENT MUST BE REPORTED WITHIN TEN (10) DAYS AFTER RECEIPT OF MATERIAL THE ABOVE LISTED MERCHANDISE TO REMAIN THE PROPERTY OF SOLITRON DEVICES, INC UNTIL THE INVOICE IS PAID.

No. T 69427

TYPE 100A/RADIATION LOT NO. _____ LOT SIZE _____ SAMPLE SIZE _____ RELIABILITY ○ PRE-SHIP INSP. ○ FINAL INSP. ○ PAGE 1 OF 1

CUSTOMER NASA CUSTOMER P. O. _____ TESTER _____ DATE 7-13-72

PARAMETER		BV_{CBO}	BV_{EBO}	$V_{CE,O}$	h_{FE}	h_{FE}	h_{FE}	$V_{CE(s)}$	$V_{BE(s)}$	$V_{CE(s)}$	$V_{BE(s)}$	$V_{CE(s)}$	$V_{BE(s)}$
TEMP. 25°C unless noted													
TEST EQUIPMENT NO.													
CONDITIONS		I_C=1.0MA	I_E=1.0MA	I_C=50MA	I_C=50A V_{CE}=5V	I_C=75A V_{CE}=5V	I_C=100A V_{CE}=5V	I_C=50A I_B=5A	I_C=50A I_B=5A	I_C=75A I_B=7.5A	I_C=75A I_B=7.5A	I_C=90A I_B=9.0A	I_C=90A I_B=9.0A
LIMITS	MIN.												
	MAX.												
UNITS OF MEASURE		V	V	V	h_{FE}	h_{FE}	h_{FE}	V	V	V	V	V	V
NO.	DATE CODE												
2		110	6.0	104	100	73	52	0.36	0.96	0.53	1.05	0.62	1.10
6		110	6.0	96	98	67	55	0.31	0.92	0.53	1.02	0.60	1.05
7		104	6.0	96	105	74	54	0.24	0.94	0.34	1.02	0.40	1.08
8		110	6.0	98	85	64	50	0.31	0.96	0.46	1.05	0.57	1.12
9		118	6.0	108	98	70	52	0.25	0.94	0.36	1.02	0.43	1.10
10		114	5.8	106	85	54	46	0.36	0.96	0.53	1.08	0.62	1.12
11		120	5.8	116	73	80	54	0.42	1.05	0.66	1.18	0.77	1.22
12		62	5.8	114	66	53	45	0.48	1.02	0.66	1.10	0.76	1.15
13		108	6.0	94	102	75	55	0.21	0.92	0.30	1.10	0.36	1.05
15		106	6.0	100	92	64	50	0.30	0.95	0.45	1.05	0.54	1.12
17		124	5.7	118	50	36	18	0.78	1.25	1.15	1.45	1.50	1.60
18		112	5.8	104	90	71	55	0.23	0.93	0.33	1.02	0.38	1.05
19		126	6.0	124	60	48	31	0.35	1.35	0.63	1.60	0.90	1.70
20		112	5.9	104	76	54	46	0.70	1.10	0.94	1.22	1.10	1.30
21		116	5.6	114	65	53	50	0.22	0.92	0.32	1.00	0.38	1.02
22		112	6.0	100	105	65	51	0.42	1.00	0.58	1.12	0.68	1.20
23		85	5.6	108	53	41	28	0.21	0.93	0.32	1.02	0.41	1.08
24		116	5.9	114	82	64	52	0.35	0.96	0.48	1.05	0.58	1.12
25		120	5.9	100	76	53	46	0.55	0.97	0.70	1.08	0.78	1.12
26		120	5.6	96	70	54	48	0.42	0.96	0.57	1.05	0.65	1.10

SDI FORM 84

B. Five Ampere Transistor

The proposed chip to satisfy this portion of the contract was the BR100 chip which is 62.5 mils x 90 mils in size. Upon re-appraisal of the specifications of the contract, it was decided to substitute the BR200 chip which is 80 mils x 120 mils. It was felt that the larger chip would be better able to withstand the stringent environmental conditions.

Sample devices from the initial diffusion run were assembled in the TO-111 package. These units were tested for Vceo (sus) at high temperature using single shot indictive technique. The units failed between 250°C to 260°C. It was felt that the package was too small to adequately dissipate the heat from the chip.

The next several diffusion runs were made attempting to meet the proposed base width of 0.3μ. It was found that this base width would not support the 90 volt Vceo. By increasing the base width to 0.6μ the required voltage was sustained.

In order to determine the size package needed to dissipate the heat, the next available chips were mounted in the TO-62 package. These units were tested and the failure range was between 270°C and 290°C. This indicated an improvement over the TO-111 package but the package appears to be inadequate for 300°C operation.

Since going to a larger package increased the temperature response of the chip, additional devices were assembled in the TO-61 package. Two types of devices were fabricated. One type being single chip construction and the other being dual chip construction. These devices were tested for high temperature response and the TO-61 package increased the average temperature capability approximately 5°C over the TO-62 package. It was also noted that the expected difference between the single die construction and the dual die construction did not materialize. Since the dual construction was, in general, slightly lower voltage than the single construction, it was decided to repeat the experiment.

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TEST DATA SHEET

YPE BR200 LOT NO. 3R-1 LOT SIZE 34 SAMPLE SIZE TO-111 RELIABILITY ○ PRE-SHIP INSP. ○ FINAL INSP. ○ PAGE 1 OF 2

USTOMER NASA CUSTOMER P. O. NAS8-25917 TESTER N. SQUEO DATE 8-19-70

PARAMETER		V_{CBO}	V_{CEO}	$V_{CEO(sus)}$	V_{EBO}	h_{FE}	h_{FE}	h_{FE}	h_{FE}	$V_{CE(sat)}$	$V_{BE(sat)}$		T °C
TEMP. 25°C unless noted													(MAX)
EST EQUIPMENT NO.													
CONDITIONS		I_C = 1MA	I_C = 100mA	I_C = 5A	I_E = 1MA	I_C = 0.5A V_{CE} = 5V	I_C = 1A V_{CE} = 5V	I_C = 3A V_{CE} = 5V	I_C = 5A V_{CE} = 5V	I_C = 5CA I_B = 0.5A	I_C = 1.0A I_B = 0.1A		I_C = 5A $V_{CEO(SUS)}$ > 90V
LIMITS	MIN.			90									
	MAX.									1.0			
UNITS OF MEASURE		Volts	Volts	Volts	Volts					Volt	Volt		
NO.	DATE CODE												
1		132	88	110	7	275	275	275	170	0.21	0.79		260
2		118	89	100	7	260	275	275	150	0.24	0.80		240
3		108	90	90	6.9	200	225	240	173	0.21	0.79		250
4		124	93	100	6.8	210	230	250	135	0.24	0.79		260
5		118	89	98	6.9	285	270	290	150	0.20	0.79		250
6		130	87	98	7	275	275	280	188	0.21	0.79		255
7		128	88	100	7	275	275	280	160	0.22	0.79		250
8		120	92	98	6.7	240	250	250	140	0.21	0.79		255
9		118	90	98	6.8	240	250	250	135	0.22	0.79		255
10		132	88	100	7	275	280	280	175	0.20	0.79		260
11		128	87	98	6.8	285	280	280	175	0.21	0.79		250
12		116	90	98	6.9	240	240	240	150	0.23	0.79		260
13		128	87	100	7	260	260	250	155	0.21	0.79		250
14		128	88	100	7	275	280	282	163	0.21	0.79		260
15		132	87	100	7	290	290	290	180	0.21	0.79		255
16		112	86	98	7	275	280	285	175	0.21	0.79		255
17		124	89	100	6.5	260	260	260	155	0.23	0.80		255
18		112	94	98	6.6	205	225	240	125	0.22	0.79		250
19		128	88	100	7	250	260	255	165	0.21	0.79		250
20		124	94	103	6.7	163	188	210	112	0.25	0.80		250

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...17 BLUE H... BLVD.
RIVIERA BE... LA. 33404
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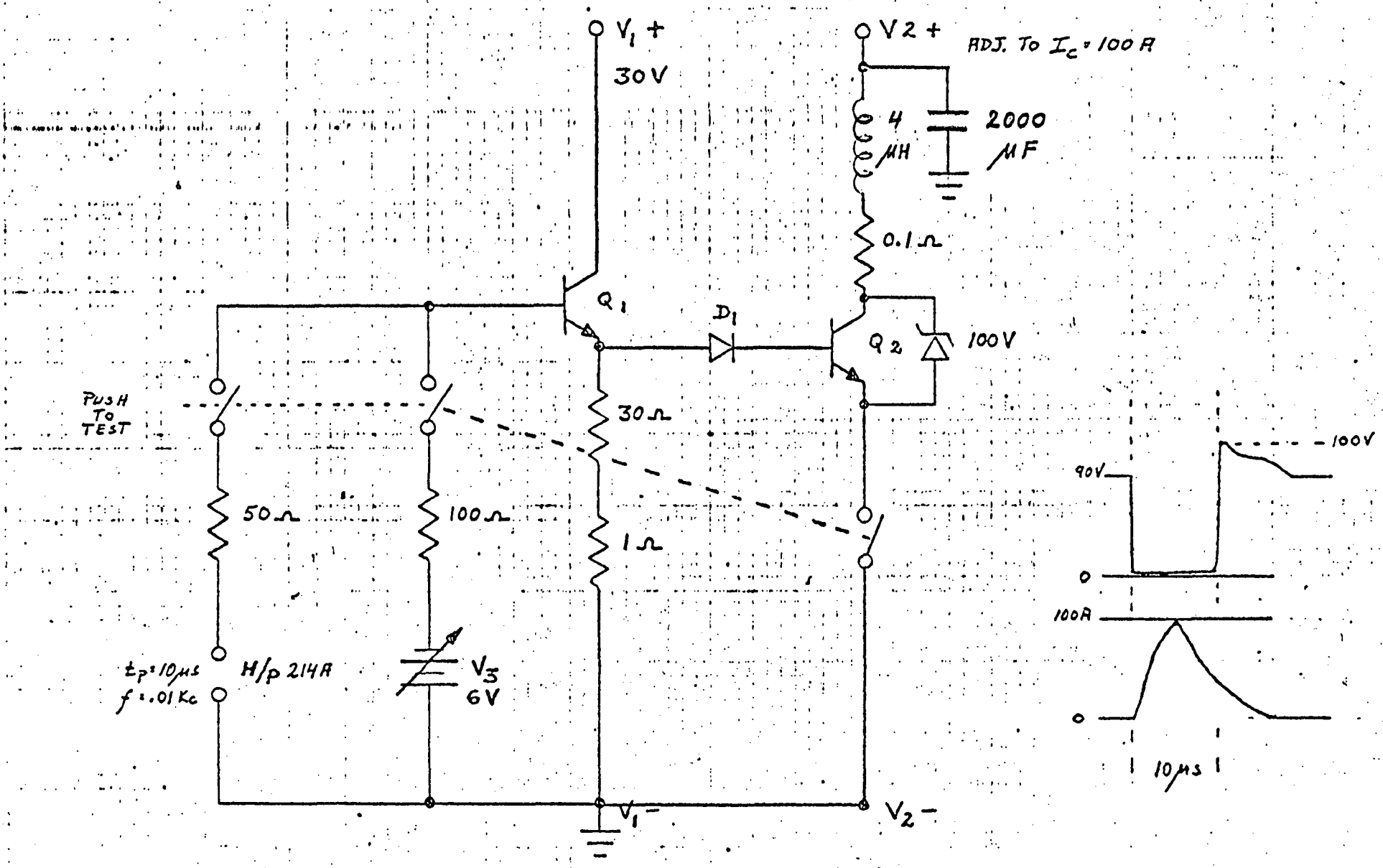
TEST DATA SHEET

TYPE BR200 LOT NO. 3R-1 LOT SIZE 34 SAMPLE SIZE TO-111 RELIABILITY ○ PRE-SHIP INSP. ○ FINAL INSP. ○ PAGE 2 OF 2

CUSTOMER NASA CUSTOMER P. O. NAS8-25917 TESTER N SQUEO DATE 2-19-70

PARAMETER		V_{CBO}	V_{CEO}	$V_{CEO(SUS)}$	V_{EBO}	h_{FE}	h_{FE}	h_{FE}	h_{FE}	$V_{CE(SAT)}$	$V_{BE(SAT)}$		T °C
TEMP. 25°C unless noted													(MAX)
TEST EQUIPMENT NO.													
CONDITIONS		I_C=1MA	I_C=100MA	I_C=5A	I_C=1MA	I_C=0.5A V_{CE}=5V	I_C=1A V_{CE}=5V	I_C=3A V_{CE}=5V	I_C=5A V_{CE}=5V	I_C=5.0A I_B=0.5A	I_C=1.0A I_B=0.1A		I_C=5A $V_{CEO(SUS)}$ 190V
LIMITS	MIN.			90									
	MAX.									1.0			
UNITS OF MEASURE		Volts	Volts	Volts	Volts					Volt	Volt		
NO.	DATE CODE												
21		124	85	95	6.6	260	260	260	180	0.20	0.79		250
22		104	87	98	6.8	250	255	260	138	0.23	0.79		260
23		106	89	96	6.9	220	220	240	123	0.22	0.79		260
24		116	83	96	7	350	350	350	170	0.24	0.79		260
25		100	88	96	6.8	250	250	260	145	0.21	0.79		260
26		110	87	100	7	260	260	260	155	0.22	0.79		260
27		104	88	90	6.8	225	225	230	129	0.22	0.79		255
28		108	89	96	6.8	260	260	275	138	0.22	0.79		260
29		124	85	95	6.8	275	275	275	175	0.20	0.79		250
30		120	82	90	6.9	420	425	410	220	0.22	0.79		250
31		94	83	96	6.6	225	225	230	143	0.22	0.79		255
32		122	86	90	6.8	260	260	260	180	0.22	0.79		250
33		116	92	98	6.4	210	225	240	130	0.21	0.79		260
34		136	88	98	7	290	290	290	175	0.21	0.79		260


V1 +
30 V
V2 +
ADJ. To Ic = 100 A
4 μH
2000 μF
0.1 Ω
Q1
D1
Q2
100 V
PUSH TO TEST
30 Ω
50 Ω
100 Ω
1 Ω
tp = 10 μs
f = .01 Kc
H/p 214A
V3
6 V
V1 −
V2 −
100V
90V
0
100A
0
10 μs

SOLITRON DEVICES, INC.
1177 BLUE HERON BLVD.
RIVIERA BEACH, FLA. 33404
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TEST DATA SHEET

TYPE 3RSK LOT NO. 3R-5 LOT SIZE _____ SAMPLE SIZE TO-62 RELIABILITY ○ PRE-SHIP INSP. ○ FINAL INSP. ○ PAGE _____ OF _____

CUSTOMER NASA CUSTOMER P.O. NAS 8-25917 TESTER _____ DATE _____

PARAMETER		V_{CBO}	V_{CEO}	I_{CBO}	V_{EBO}	h_{FE}	h_{FE}	h_{FE}	h_{FE}	$V_{CE(SAT)}$	$V_{BE(SAT)}$	$V_{CEO(SUS)}$	T_{OC} (MAX)
TEMP. 25°C unless noted													
TEST EQUIPMENT NO.													
CONDITIONS		1MA	100MA	90V	1MA	5V 0.5A	5V 1A	5V 3A	5V 5A	5A 0.5A	1A 0.1A	Ic 5A	Ic 5A $V_{CEO(SUS)}$ >90V
LIMITS	MIN.												
	MAX.												
UNITS OF MEASURE		V	V	NA	V					V	V	V	
NO.	DATE CODE												
1		126	94	50	7	135	141	145	118	0.33	0.81	—*	—
2		128	92	55	7	145	151	155	112	0.30	0.81	110	275
3		132	96	3	6.5	120	129	130	77	0.39	0.83	110	270
4		137	100	17	6.5	121	130	132	87	0.31	0.81	115	280
5		140	96	2	6.5	135	149	145	64	0.40	0.84	110	275
6		132	90	3	6.5	141	151	151	91	0.61	0.85	105	285
7		80	—	—	—	—	—	—	—	—	—	—	—
8		134	108	6	7	73	79	81	71	0.25	0.79	120	290
9		136	96	2	6.5	131	139	130	50	0.48	0.85	110	275
10		132	92	340	7	151	160	161	111	0.31	0.82	110	285
11		136	96	2	6.5	130	140	139	67	0.57	0.85	110	275
12		136	94	2	6.5	138	145	135	53	0.59	0.85	110	275
13		132	94	2	6.5	109	118	125	109	0.41	0.79	110	285
14		136	108	86	6.5	68	80	91	69	0.31	0.81	120	290

* DESTROYED DURING SET-UP

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TEST DATA SHEET

TYPE 3RSM (SINGLE) LOT NO. 3R-6 LOT SIZE _____ SAMPLE SIZE To-61 RELIABILITY ○ PRE-SHIP INSP. ○ FINAL INSP. ○ PAGE _____ OF _____

CUSTOMER NASA CUSTOMER P. O. NAS8-25917 TESTER _____ DATE _____

PARAMETER	V_{CBO}	V_{CEO}	I_{CBO}	V_{EBO}	h_{FE}	h_{FE}	h_{FE}	h_{FE}	$V_{CE(SAT)}$	$V_{BE(SAT)}$	$V_{CEO(SUS)}$	T °C (MAX)
TEMP. 25°C unless noted												
TEST EQUIPMENT NO.												
CONDITIONS	1MA	100MA	90V	1MA	5V 0.5A	5V 1A	5V 3A	5V 5A	5A 0.5A	1A 0.1A	Ic 5A	Ic 5A $V_{CEO(SUS)}$ >90V
LIMITS MIN.												
LIMITS MAX.												
UNITS OF MEASURE	V	V	NA	V					V	V	V	
NO / DATE CODE												
1	114	85	8.5	6.6	183	185	188	155	0.25	0.795	100	280
2	116	91	3.7	6.6	200	205	205	160	0.30	0.81	110	280
3	112	84	570	6.4	225	230	230	176	0.299	0.80	105	280
4	70	—	—	—	—	—	—	—	—	—	—	
5	132	112	1.6	6.4	185	188	190	85	0.49	0.79	135	280
6	120	85	165	6.6	198	205	225	155	0.29	0.79	—	—
7	112	84	1	6.5	190	195	195	155	0.25	0.79	100	280
8	136	110	2.2	6.6	198	200	200	98	0.41	0.79	135	280
9	110	85	0.5	6.6	190	188	188	155	0.24	0.795	100	285
10	112	84	0.6	6.5	180	185	185	155	0.26	0.805	100	295
11	108	76	—	—	—	—	—	—	—	—	—	
12	124	87	130	6.3	210	225	225	167	0.245	0.79	100	295

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TEST DATA SHEET

TYPE 3R SM (DUAL) LOT NO. 3R-6 LOT SIZE _____ SAMPLE SIZE TO-61 RELIABILITY ○ PAGE _____ OF _____
PRE-SHIP INSP. ○
CUSTOMER NASA CUSTOMER P.O. NAS8-25917 TESTER _____ FINAL INSP. ○ DATE _____

PARAMETER		V_{CBO}	V_{CEO}	I_{CBO}	V_{EBO}	h_{FE}	h_{FE}	h_{FE}	h_{FE}	$V_{CE(SAT)}$	$V_{BE(SAT)}$	$V_{CEO(SUS)}$	T_{oc}
TEMP. 25°C unless noted													(MAX)
TEST EQUIPMENT NO.													
CONDITIONS		1MA	100MA	90V	1MA	5V 0.5A	5V 1A	5V 3A	5V 5A	5A 0.5A	1A 0.1A	I_C 5A	I_C 5A $V_{CEO(SUS)}$ >90V
LIMITS	MIN.												
	MAX.												
UNITS OF MEASURE		V	V	NA	V								
NO.	DATE CODE												
1		126	106	21.7	6.3	188	190	195	188	0.19	0.76	100	285
2		132	112	56.2	6.3	178	188	199	188	0.18	0.758	110	285
3		114	87	17.9 uA	6.5	205	210	225	205	0.185	0.759	80	280
4		114	88	505	6.3	175	180	195	180	0.20	0.76	90	280
5		114	87	380	6.2	225	225	240	210	0.29	0.758	85	280
6		116	87	79	6.4	240	240	250	230	0.17	0.759	80	285
7		114	88	4.2	6.4	188	190	200	195	0.19	0.76	80	275
8		116	84	7.9 uA	6.2	230	240	250	240	0.19	0.759	80	280
9		130	108	1.14 uA	6.5	199	200	205	195	0.18	0.765	110	290
10		126	118	35 uA	3.2	170	177	190	175	0.21	0.765	120	280
11		112	87	90 uA	6.2	230	240	250	230	0.16	0.75	80	285
12		110	89	57	6.3	199	200	205	200	0.31	0.76	80	290
13		114	84	7.1	5.9	240	245	250	240	0.185	0.759	90	290
14		118	92	6.1 uA	6.6	180	190	200	190	0.16	0.760	100	295
15		112	84	31 uA	6.3	250	250	255	245	0.17	0.765	90	285

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TEST DATA SHEET

TYPE 3R5M (DUAL) LOT NO. 3R-7D LOT SIZE _____ SAMPLE SIZE _____ RELIABILITY ○ PRE-SHIP INSP. ○ FINAL INSP. ○ PAGE _____ OF _____

CUSTOMER NASA CUSTOMER P. O. _____ TESTER _____ DATE _____

PARAMETER	V_{CBO}	V_{CEO}	I_{CBO}	I_{CEO}	V_{EBO}	h_{FE}	h_{FE}	h_{FE}	$V_{CE(SAT)}$	$V_{BE(SAT)}$	$V_{CEO(SUS)}$	$T^{\circ}C$ (MAX)
TEMP: 25°C unless noted												
TEST EQUIPMENT NO.												
CONDITIONS	1 MA	100MA	90V	90V	1 MA	5V 0.5A	5V 3A	5V 5A	5A 0.5A	1A 0.1A	Ic 5A	Ic 5A $V_{CEO(SUS)}$ >90V
LIMITS MIN. / MAX.												
UNITS OF MEASURE	V	V			V				V	V	V	
TIC / DATE CODE												
1	122	90	2.3 uA	15.5 uA	6.5	175	210	200	0.20	0.77	90	290
2	120	92	1.6 uA	60 uA	6.5	160	200	180	0.19	0.76	95	290
3	124	92	10 nA	50 uA	6.5	155	195	170	0.22	0.79	90	290
4	116	92	18 uA	19.5 uA	6.5	130	250	210	0.19	0.76	90	280
5	120	88	170 nA	140 uA	6.5	175	220	200	0.19	0.76	90	290
6	118	86	110 nA	2.8 MA	6.5	210	250	210	0.20	0.77	100	280
7	120	92	5 uA	120 uA	6.5	130	180	170	0.20	0.76	90	285
8	122	88	120 nA	460 uA	6.5	180	210	200	0.19	0.76	100	280

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TEST DATA SHEET

TYPE 3R5M (SINGLE) LOT NO. 3R-7D LOT SIZE _____ SAMPLE SIZE _____ RELIABILITY ○ PAGE _____ OF _____

CUSTOMER NASA CUSTOMER P. O. _____ TESTER _____ PRE-SHIP INSP. ○ FINAL INSP. ○ DATE _____

PARAMETER	V_{CBO}	V_{CEO}	I_{CBO}	I_{CEO}	V_{EBO}	h_{FE}	h_{FE}	h_{FE}	$V_{CE(SAT)}$	$V_{BE(SAT)}$	$V_{CEO(SUS)}$	$T^{\circ}C$ (MAX)
TEMP. 25°C unless noted												
TEST EQUIPMENT NO.												
CONDITIONS	1MA	100MA	90V	90V	1MA	5V	5V	5V	5A	1A	Ic 5A	Ic 5A
						0.5A	3A	5A	0.5A	0.1A		$V_{CEO(SUS)}$ >90V
LIMITS MIN												
LIMITS MAX.												
UNITS OF MEASURE	V	V	nA	μA	V				V	V	V	
NO. / DATE CODE												
1	126	86	44	125	6.5	210	240	90	0.45	0.87	105	275
2	118	86	4.8	6.9	6.5	190	250	175	0.27	0.79	100	280
3	114	98	4.4	.34	6.5	120	170	130	0.23	0.79	110	290
4	124	90	2.4	5.8	6.5	190	220	145	0.30	0.80	100	270
5	122	90	92	100	7	200	50	10	—	—	—	—
6	124	90	17	23	6.5	210	250	100	0.43	0.87	100	275
7	124	90	34	82	6.5	160	200	130	0.29	0.81	105	270
8	124	90	33	170	6.5	165	200	140	0.26	0.80	105	295
9	164	88	4.4	200	6.5	220	190	72	0.84	1.05	100	290
10	122	90	11	87	6.5	150	180	125	0.28	0.81	90	290

A new sample was fabricated and the devices were tested with essentially the same results. This sample showed very little difference in the voltages of the two types of construction. At this time it was decided that reducing the duty cycle might increase the high temperature capability. Therefore, the devices were re-tested at a 10% duty cycle instead of the 50% duty cycle which had been used previously. This resulted in transistor operation at 300°C. In addition samples from lot 3R-6 were retested with the same result. The temperature was not raised above 300°C due to the limitation of the equipment.

In view of the above results a lot of forty devices of dual chip construction in the TO-61 non-isolated package was fabricated. The delivery of twenty of these units was made on 6-3-71 to satisfy the requirements of exhibit A, para. B2b of the contract.

SOLITRON DEVICES, INC.
1177 BLUE HERON BLVD.
RIVIERA BEACH, FLA. 33404
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TEST DATA SHEET

TYPE _____ LOT NO. _____ LOT SIZE _____ SAMPLE SIZE _____ RELIABILITY ○ PRE-SHIP INSP. ○ FINAL INSP. ○ PAGE _____ OF _____

CUSTOMER NASA CUSTOMER P. O. _____ TESTER _____ DATE _____

PARAMETER / TEMP. 25°C unless noted / TEST EQUIPMENT NO. / CONDITIONS / LIMITS MIN. MAX. / UNITS OF MEASURE	NO.	DATE CODE	T °C	T °C		T °C	T °C		T °C	T °C		T °C	T °C	
			LOT 3R-7 SINGLE Ic 5A VCEO(SUS) >90V	LOT 3R-7 SINGLE Ic 5A VCEO(SUS) >90V		LOT 3R-7 DUAL Ic 5A VCEO(SUS) >90V	LOT 3R-7 DUAL Ic 5A VCEO(SUS) >90V		LOT 3R-6 SINGLE Ic 5A VCEO(SUS) >90V	LOT 3R-6 SINGLE Ic 5A VCEO(SUS) >90V		LOT 3R-6 DUAL Ic 5A VCEO(SUS) >90V	LOT 3R-6 DUAL Ic 5A VCEO(SUS) >90V	
			50% DUTY CYCLE	10% DUTY CYCLE		50% DUTY CYCLE	10% DUTY CYCLE		50% DUTY CYCLE	10% DUTY CYCLE		50% DUTY CYCLE	10% DUTY CYCLE	
	1		275	300		290	300					285	300	
	2		280	300		290	300					285	300	
	3		290	300		290	300		280	300		280	300	
	4		270	300		280	300					280	300	
	5		–	–		290	300		280	300		280	300	
	6		275	300		280	300							
	7		270	300		285	300		280	300				
	8		295	300		280	300		280	300				
	9		290	300					285	300			–	
	10		290	300										

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TEST DATA SHEET

TYPE 6RSM LOT NO. FINAL LOT SIZE _____ SAMPLE SIZE TO-41 RELIABILITY ○ PAGE 1 OF 2
PRE-SHIP INSP. ○
CUSTOMER NAS 8-25917 CUSTOMER P. O. _____ TESTER _____ FINAL INSP. ○ DATE _____

PARAMETER	BV_{CBO}	BV_{EBO}	BV_{CEO}	I_{CBO}	I_{EBO}	I_{CEO}	H_{FE}	H_{FE}	H_{FE}	H_{FE}	H_{FE}	
TEMP. 25°C unless noted												
TEST EQUIPMENT NO.												
CONDITIONS	1 MA	1MA	50MA	90V	3V	90V	0.5A 5V	1A 5V	3A 5V	5A 5V	7A 5V	
LIMITS MIN.												
LIMITS MAX.												
UNITS OF MEASURE	V	V	V									
NO. / DATE CODE												
1	116	6.2	90	16 nA	6 nA	54 uA	175	190	195	170	115	
2	116	6.2	84	145 nA	6 nA	520 uA	210	210	220	200	195	
3	110	6.1	84	360 nA	42 nA	215 uA	210	215	225	225	210	
4	116	6.3	89	5.4 uA	33 nA	130 uA	160	170	180	175	175	
5	114	6.2	83	58 nA	420 nA	260 uA	220	260	265	240	220	
6	128	6.1	112	8 uA	650 nA	13 uA	175	180	190	180	155	
7	110	6.1	83	23 uA	8.2 nA	21 MA	260	270	280	260	260	
8	116	6.4	95	7.4 uA	1.2 nA	155 uA	175	190	195	180	170	
9	114	6.4	90	1.6 uA	5.9 nA	90 uA	180	190	200	190	190	
10	112	6.3	85	125 nA	32 nA	2 MA	260	280	280	260	220	
11	110	6.1	87	510 nA	45 nA	175 uA	175	180	180	175	170	
12	126	6.3	106	1.4 uA	200 nA	79 uA	195	200	200	190	170	
13	116	6.2	85	195 nA	8 nA	145 uA	200	220	220	200	200	
14	122	6.1	104	23 nA	79 nA	18 uA	180	180	190	180	160	
15	112	6.2	86	92 nA	14 nA	530 uA	220	260	260	240	240	
16	110	6.3	88	26 uA	215 uA	36 uA	195	200	210	200	200	
17	108	6.1	88	42 nA	320 nA	2.6 uA	195	200	210	195	195	
18	112	5.8	83	15 nA	66 nA	16 uA	230	250	265	260	260	
19	118	6.2	87	2.7 uA	18 nA	51 uA	210	220	240	230	210	
20	112	6.2	87	9.4 nA	17 nA	2.3 uA	180	190	195	180	180	

SOLITRON DEVICES, INC.
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TEST DATA SHEET

TYPE 6RSM LOT NO. FINAL LOT SIZE _____ SAMPLE SIZE To-61 RELIABILITY ○ PAGE 2 OF 2

CUSTOMER NAS 8-25917 CUSTOMER P. O. _____ TESTER _____ PRE-SHIP INSP. ○ FINAL INSP. ○ DATE _____

PARAMETER	$V_{CE(SAT)}$	$V_{BE(SAT)}$	C_{OBO}	C_{IBO}	$V_{CEO(SUS)}$	T_{oc}	T_{oc}					
TEMP. 25°C unless noted												
TEST EQUIPMENT NO.												
CONDITIONS	5A 0.5A	5A 0.5A	10V 1MHz	3V 1MHz	5A	5A >90V 50% D.C.	5A >90V 10% D.C.					
LIMITS MIN												
LIMITS MAX												
UNITS OF MEASURE	V	V	Pf	Pf		°C	°C					
NO. / DATE CODE												
1	0.24	0.96	180	1300	90V	280	300					
2	0.19	0.92	180	1400	90V	280	300					
3	0.16	0.87	180	1400	90V	285	300					
4	0.19	0.90	185	1400	90V	275	300					
5	0.18	0.90	185	1400	90V	280	300					
6	0.17	0.88	160	1450	110V	290	300					
7	0.16	0.88	180	1400	120V	280	300					
8	0.16	0.87	170	1450	90V	285	300					
9	0.18	0.90	180	1400	90V	290	300					
10	0.19	0.92	180	1350	95V	290	300					
11	0.19	0.91	185	1400	100V	295	300					
12	0.17	0.88	165	1450	90V	285	300					
13	0.18	0.89	185	1400	90V	290	300					
14	0.18	0.90	165	1500	95V	290	300					
15	0.16	0.87	180	1400	90V	290	300					
16	0.18	0.88	185	1400	90V	280	300					
17	0.16	0.88	180	1450	90V	290	300					
18	0.17	0.89	185	1350	100V	280	300					
19	0.20	0.95	185	1350	90V	285	300					
20	0.18	0.89	185	1400	100V	280	300					

Solitron DEVICES, INC.
TRANSISTOR DIVISION
AC - PHONE
305 - 848-4311
77 BLUE HERON BLVD., RIVIERA BEACH, FLORIDA 33404

ORIGINAL

INVOICE

INVOICE TO
NASA
George C. Marshall Space Flight Center
Marshall Space Flight Center
Alabama 35812

SHIP TO
Same
Accountable Property Officer
Bldg. 4471

TERMS - ½% 10, NET 30 DAYS
F.O.B. RIVIERA BEACH, FLORIDA

ORDER NUMBER	CUSTOMER ORDER NUMBER	SHIPPED VIA	REPRESENTATIVE	INVOICE DATE	DATE PROMISED
		Hand Carried - R. Howard		6/2/71	

NUMBER	ORDERED	SHIPPED	DESCRIPTION	UNIT PRICE	AMOUNT
20		20	NASA Contract NA S8-25917 DCN 1 - 0 - 40 - 02692, & S1 Medium Power Transistors with read and record data (Exhibit A, Para. B 2b)		

WE CERTIFY THAT THESE GOODS WERE PRODUCED IN COMPLIANCE WITH ALL APPLICABLE REQUIREMENTS OF SECTIONS 6, 7 AND 12 OF THE FAIR LABOR STANDARDS ACT, AS AMENDED, AND OF REGULATIONS AND ORDERS OF THE UNITED STATES DEPARTMENT OF LABOR ISSUED UNDER SECTION 14 THEREOF.

GOODS SHIPPED BY US AT CONSIGNEE'S RISK AFTER WE HAVE DELIVERED TO TRANSPORTATION COMPANY AND TAKEN RECEIPT FOR SAME

NOTICE OF ANY SHIPMENT MUST BE RECEIVED WITHIN TEN (10) DAYS AFTER RECEIPT OF MATERIAL. THE ABOVE LISTED MERCHANDISE TO REMAIN THE PROPERTY OF SOLITRON DEVICES, INC. UNTIL THE INVOICE IS PAID

No. T 58732

C. 10 Ampere Rectifier.

A planar rectifier was designed for this project to provide a device capable of assembly with a hard eutectic mount and aluminum wire bonding. This device was designed for a 30 amp capability under normal operating conditions to insure the device operation at high temperature.

The first two diffusion runs yielded devices which would meet the reverse voltage characteristics but were too high in forward voltage characteristics. This problem was solved by diffusing an N+ layer into the back of the slice.

Twenty-five devices were assembled in DO-5 packages and tested at 300°C. The reverse leakage at 200V V_R and 300°C ranged between 11 MA and 25 MA. Twenty of these devices were delivered to NASA-MSFC on 7-12-71 to satisfy the requirements of exhibit A, para. B.2C of the contract.

CELITRON DEVICES, INC.
777 BLUE HERON BLVD.
RIVIERA BEACH, FLA. 33404
PHONE: (305) 848-3411

TEST DATA SHEET

TYPE RECTIFIER LOT NO. _____ LOT SIZE _____ SAMPLE SIZE _____ RELIABILITY ○ PAGE _____ OF _____

CUSTOMER NASA CUSTOMER P. O. NAS8-25917 TESTER _____ PRE-SHIP INSP. ○ FINAL INSP. ○ DATE _____

PARAMETER		VR	VF	IR
TEMP. 25°C unless noted				300°C
TEST EQUIPMENT NO.				
CONDITIONS		IR=10μa	IR=10A	VR=200V
LIMITS	MIN.			
	MAX.			
UNITS OF MEASURE				
NO.	DATE CODE			
1		330V	0.870V	14MA
2		430V	0.865V	19MA
3		405V	0.865V	17MA
4		375V	0.880V	18MA
5		360V	0.865V	18MA
6		405V	0.870V	11MA
7		350V	0.870	12MA
8		345V	0.870V	14MA
9		340V	0.870V	16MA
10		340V	0.870V	25MA
11		280V	0.875V	16MA
12		355V	0.870V	14MA
13		420V	0.870V	17MA
14		410V	0.865V	18MA
15		350V	0.870V	19MA
16		415V	0.865V	14MA
17		405V	0.870V	15MA
18		420V	0.870V	11MA
19		350V	0.865V	12MA
20		405V	0.870V	16MA

PACKING LIST

Solitron DEVICES, INC.
TRANSISTOR DIVISION

[redacted] HERON BLVD., RIVIERA BEACH, FLORIDA 33404
S[redacted]ER - CONTENTS MERCHANDISE - RETURN REQUESTED

Solitron DEVICES, INC.
TRANSISTOR DIVISION

1177 BLUE HERON BLVD., RIVIERA BEACH, FLORIDA 33404
POSTMASTER - CONTENTS MERCHANDISE - RETURN REQUESTED

NASA
GEO. C. MARSHALL SPACE FLT. CENTER
MARSHALL SPACE FLIGHT CENTER
ALABAMA 35812

SAME
ACCOUNTABLE PROPERTY OFFICER
BLDG. 4471

TOMER'S DER NO.

CUSTOMER'S ORDER NO.

R ORDER NUMBER	CUSTOMER ORDER NUMBER	SHIPPED VIA	REPRESENTATIVE	INVOICE DATE	DATE PROMISED
		UPS		7/13/71	

20		20	NAS8-25917 DCN 1-0-40-02692, & S1 MEDIUM POWER TRANSISTORS WITH READ AND DATA (EXHIBIT A, PARA. B 2C)

PACKING LIST

SOLITRON DEVICES, INC. TRANSISTOR DIVISION 1177 BLUE HERON BLVD., RIVIERA BEACH, FLORIDA 33404

No. T5[redacted]96

IV. DISCUSSION

For a semiconductor device, whether it be a rectifier or a transistor, it is usual practice to base the maximum power rating on the theoretical allowable temperature the junction can attain. For silicon this is about 250°C. Beyond this temperature, the conduction becomes predominantly intrinsic, and the junction loses its rectification properties.

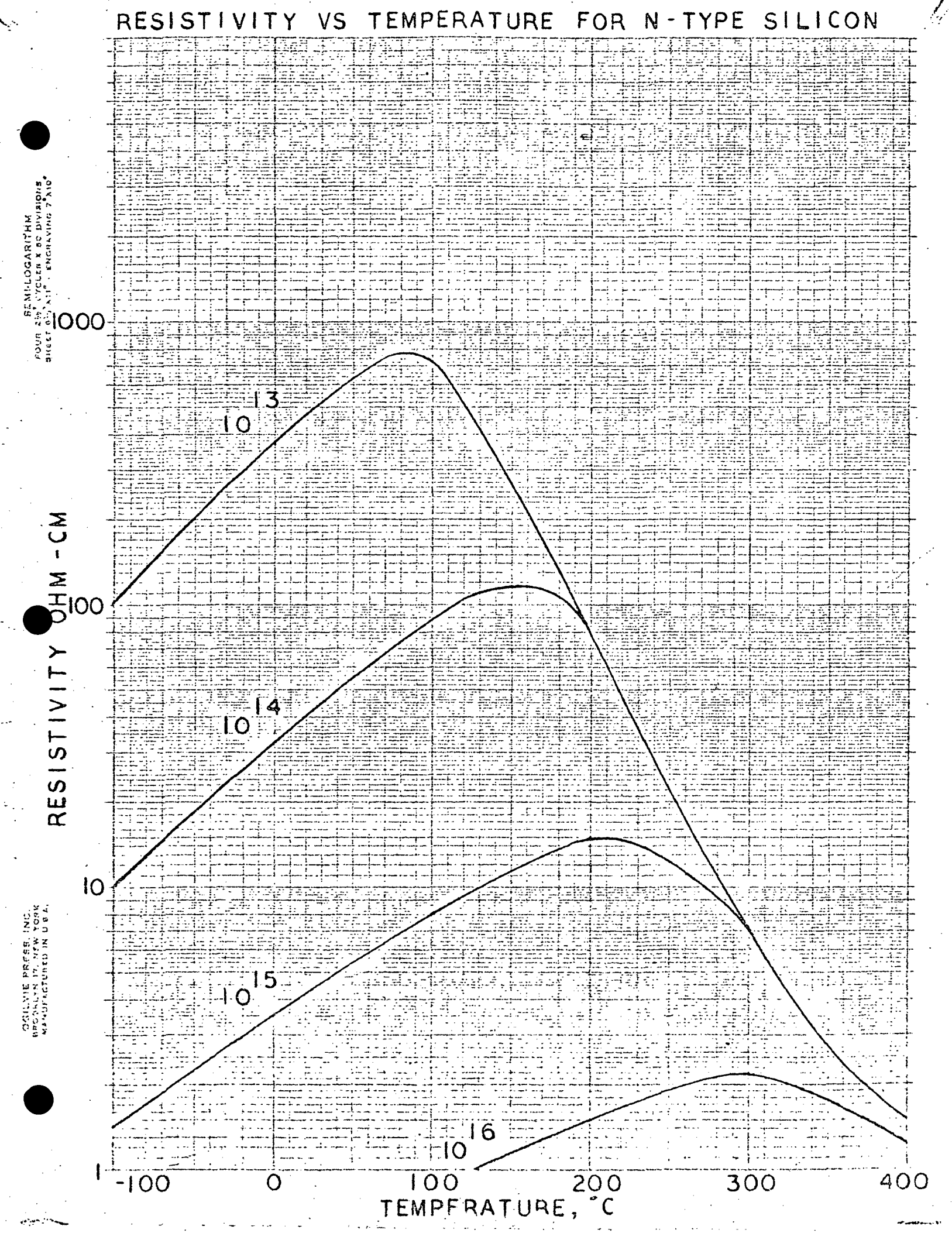
This is illustrated on a graph of resistivity versus temperature, for N-type silicon. This graph was reproduced in part from current literature. The 10^{15} doping curve is the nearest illustrated one to the doping level required to fabricate the six to eight ohm-cm material needed to sustain a 90 volt BVceo. The curves for the required material would fall between the 10^{14} and the 10^{15} curves but closer to the 10^{15} curve.

It can be seen that the 10^{15} curve peaks in resistivity at about 210°C. It becomes more conductive from this point until it meets the intrinsic curve at about 295°C. It is at the peak of the curve that the mobile carriers created by thermal ionization of the intrinsic semiconductor begin to outnumber the impurity-donated carriers and this continues until the semiconductor becomes completely intrinsic. The curves for the required material meet the intrinsic curve at lower temperatures than the 10^{15} curve.

This is the main problem encountered in attempting to fabricate a 300°C operating silicon device. Marginally successful operation was attained with the five ampere transistor and the power rectifier because these devices were made much larger than necessary for normal operation to allow for the increased power dissipation. The five ampere device would be normally rated as a twenty ampere device and the 10 ampere device would normally be a thirty ampere device.

The problem was greatly increased in attempting to fabricate a 100 ampere device to operate at 300°C. Experiments indicated that paralleling the devices was a reasonable approach up to a certain point for temperature up to 200°C. When attempting to increase the power dissipation, it was found that problems in oscillations occurred. The oscillation was probably due to the increase in wiring

RESISTIVITY VS TEMPERATURE FOR N-TYPE SILICON



necessary to connect the chips and possibly a mis-match of gain at high currents. Since gain can only be measured at low current (500 ma) in chip form, it is difficult to predict the match at high current (100 amp) within ten percent. A mis-match could cause one chip to pass more current than another chip leading to destruction. This coupled with thermal stress on the breakdown characteristics of the device leading to secondary breakdown virtually makes it impossible to fabricate the device.

The problem is further complicated by the radiation hardness specifications of the device. This limits the starting resistivity, the epitaxial thickness, diffusion depths, base width, and the physical size of the device that will support the shallow diffusions.

In view of the complications encountered, it is felt that functional reliable devices fabricated from silicon can not be expected to operate at 300°C and that radiation resistance may be enhanced if the voltage requirement could be lowered so that lower resistivity material be utilized.

V.

ENGINEERING DEVICE SPECIFICATIONS

ENGINEERING DEVICE SPECIFICATION

DOUBLE DIEFUSED EPITAXIAL
RADIATION HARDENED DEVICE

PROCESS FLOW	S.O.D.
1. Receive Slices	602111-1
2. Run Make Up and Clean Slices	669
3. Oxidize Slice	301
4. Base Photo Resist	
a) Coat & Bake	356
b) Mask & Expose	633
c) Develop	634
d) Inspect & Bake	350
e) Etch	358
5. Boron Deposition	660
6. Boron Deposition	670
7. Remove Boron Glass	304
8. Boron Diffusion (Base)	671
9. Emitter Photo Resist	
a) Coat & Bake	356
b) Mask & Expose	633
c) Develop	634
d) Inspect & Bake	350
e) Etch	358
10. Phosphorous Deposition Clean	660
11. Phosphorous Deposition & Diffusion (Emitter)	672

SOLITRON
RIVIERA BEACH, FLORIDA

FOR DOUBLE DIFFUSED EPITAXIAL
RADIATION HARDENED DEVICE

DATE 8-7-72 DRWN. KW
CHKD.
APPD.

NO.

REVISION DATE E.O.

PROCESS FLOW	S.O.D.
12. Low Temperature Oxide	673
13. Contact Photo Resist	
a) Coat & Bake	356
b) Mask & Expose	633
c) Develop	634
d) Inspect & Bake	350
e) Etch	358
14. Evaporation Clean	660
15. Aluminum Evaporation	355
16. Aluminum Removal Photo Resist	
a) Coat & Bake	356
b) Mask & Expose	633
c) Develop	634
d) Inspect & Bake	350
e) Etch and Photo Resist Removal	653
17. Sinter Aluminum Contacts	311
18. 300°C Vacuum Bake (Wafer)	662
19. Wafer Scribe	333
20. Dice Separation	313
21. Clean Dice	331
22. Test Dice Electrical	674
23. Visual Die Inspect	314
24. Clean Header	222

SOLITRON
RIVIERA BEACH, FLORIDA

FOR DOUBLE DIFFUSED EPITAXIAL
RADIATION HARDENED DEVICE

DATE 8-7-72 DRWN. KW
CHKD.
APPD.

NO.

REVISION DATE E.O.

PROCESS FLOW		S.O.D.
25.	Mount Die	260
26.	Ultrasonic Lead Attach (die)	257
27.	Lead Attach (Post)	258
28.	Clean Assembly	259
29.	Visual Inspection	276
30.	Clean Cap	222
31.	Vacuum Bake Assembly & Caps	240
32.	Encapsulate	262
33.	Fine Leak	261 or 561
34.	Heat Age	330
35.	Thermo Shock	555
36.	Bubble Test	559
37.	Electrical Test	

SOLITRON
RIVIERA BEACH, FLORIDA

FOR DOUBLE DIFFUSED EPITAXIAL
RADIATION HARDENED DEVICE

DATE 8-7-72 DRWN. KW
CHKD. Gal
APPD. Tan

NO. 3 of 4

REVISION DATE E.O.

TABLE OF PACKAGE TYPES

TYPE	BASE PART NO.	CAP PART NO.
(TO-61)	600941	600561
100 AMP	IT-A-525	IT-A-523
DIODE	TD-4587	TD-4591

REVISION	DATE	E.O.

SOLITRON
RIVIERA BEACH, FLORIDA

FOR
DOUBLE DIFFUSED EPITAXIAL
RADIATION HARDENED DEVICE

DATE 8-7-72 DRWN. KW
CHKD.
APPD.

NO. 4 of 4

OPTIMUM FABRICATION

PARAMETERS

DOUBLE DIFFUSED EPITAXIAL RADIATION HARDENED DEVICE

PROCESS PARAMETER	EPITAXIAL
Material Drawing Number	602111-1
Starting Resistivity	$7 \pm 1 \Omega$-cm
Epitaxial Thickness	25 ± 4 u
Boron Deposition Temperature	$940 \pm 2^{\circ}C$
Boron Deposition V/I	$13 \pm 1 \Omega$
Flow Rates N_2	2.5 L/MIN
O_2	85 CC/MIN
B_2H_6	475 CC/MIN
Boron Diffusion Time. DRY	25 MIN
Boron Diffusion Temperature DRY	$1125^{\circ}C$
Flow Rate O_2	1L/MIN
Boron Diffusion Time WET	35 MIN
Boron Diffusion Temperature WET	$1125^{\circ}C$
Water Temperature	$95^{\circ}C$
Anneal Time to Temperature	60 MIN to $800^{\circ}C$
Base Depth Xj	7 ± 1f
Emitter Deposition Temperature	$1050^{\circ}C$
Emitter Depostion Time	3 MIN
Emitter Diffusion Time	13 MIN
Flow R tes N_2	900 CC/MIN
O_2	900 CC/MIN
$POCL_3$	620 CC/MIN
Emitter V/I	$1.3 \pm .2 \Omega$
Base Width	$3 \pm .5$f
Aluminum Thickness	20 ± 5 KA$^{\circ}$

REV	REVISION RECORD	DATE	E.O.
B	REDRAWN & REVISED	4-4-72	F-1603

DRAWING NUMBER	REV
602111	B

RESISTIVITY	VOLT. BRK/DN	PART NO.
8Ω CM ± 20%	170 - 200	-1
5Ω CM ± 20%	150 - 170	-2

SUBSTRATE - SEE DRAWING 602298-1 REV. A

EXCEPT NOTE 5 DISLOCATION DENSITY LESS THAN 500 PER CM^2

EPITAXIAL LAYER:

1. EPITAXIAL LAYER - TYPE N (PHOSPHORUS DOPED) SEE TABLE.
2. LAYER THICKNESS - 25 + 4 μ. MEASURED BY IR METHOD IN 4 MICRON GROUPS OR INDIVIDUALLY MARKED.
3. STACKING FAULTS - 100 CM^{-2} MAXIMUM.
4. SURFACE - FREE FROM VISUAL DEFECTS IF POLISHED.
5. LESS THAN SIX (6) SURFACE DEFECTS IF NOT SURFACE POLISHED.
6. NO SURFACE SPIKES HIGHER THAN TWO (2) MICRONS.
7. BACK LAPPED TO 12 MICRONS FINISH IF EPITAXIAL BUILD UP ON BACK EDGE OF SLICE IS GREATER THAN 12 MICRONS.
8. NO INVERSION.

NOTE: VISUAL DEFECT AND STACKING FAULT COUNTS ARE NOT TO BE CHECKED WITHIN 1/8" OF OUTER EDGE, EXCEPT FOR EDGE CROWN.

NEXT ASSY	TOLERANCE	DRAWING TITLE			
	ONE PLACE (.0) ±.020 TWO PLACE (.00) ±.010 THREE PLACE (.000) ±.005	N/N+ 1 1/2" EPITAXIAL WAFER	DRAWN	LMS	4-4-72
	FRACTIONAL ±		DRAFTING	LMS	4-4-72
	ANGULAR ±		ENGINEER		
			APPROVED	RJB	4-[illegible]

SOLITRON DEVICES INC.
TRANSISTOR DIVISION
RIVIERA BEACH, FLORIDA

MATERIAL	SPE SPEC.	SCALE	FULL SIZE	DRAWING NUMBER	REV
SILICON		DEVICE	NPN	602111	B

ENGINEERING DEVICE SPECIFICATION
ZE, 30 AMPERE POWER DIODE (SILICON PLANAR)

PROCESS FLOW	STANDARD OPERATION DETAIL
1. Recieve Slices	600938-1
2. Clean	300 or 546
3. Oxidize Slice	286
4. Base Photo Resist	
a) Coat & Bake	214, 413, and 290
b) Mask & Expose	343
c) Develop	634
d) Inspect & Bake	350
e) Remove Oxide	358
5. Clean	550 or 660
6. Boron Deposition	282
7. Reflux	304
8. Boron Diffusion	287
9. Etch Photo Resist	
a) Coat & Bake	214, 413, and 290
b) Expose	343
c) Develop	634
d) Bake	350
e) Remove Oxide	358
10. Clean	550 or 660
11. Phosphorous Deposition	672
12. Contact Photo Resist	

SOLITRON
RIVIERA BEACH, FLORIDA

FOR
ZE, 30 AMPERE POWER DIODE (SILICON PLANAR)

DATE 8-8-72 DRWN KW
CHKD.
APPD.

NO. 1 of 4

REVISION DATE E.O.

PROCESS FLOW	STANDARD OPERATION DETAIL
a) Coat & Bake	214, 413, and 290
b) Mask & Expose	343
c) Develop	634
d) Bake	350
e) Remove Oxide	358
13. Aluminum Evaporation Clean	660 or 550
14. Aluminum Evaporation	309, 355, or 696
15. Metal Etch Photo Resist	
a) Coat & Bake	214, 413, and 290
b) Mask & Expose	343
c) Develop	634
d) Inspect & Bake	350
e) Metal Etch	683
16. Sinter Aluminum	311
17. Bake	318
18. Scribe	333
19. Dice Separation	313
20. Load Block	332
21. Electrical Test (TDE)	See TDE Sheet
22. Clean Dice	331
23. Mount Die	260
24. Ultrasonic Lead Attach	257
25. Resistance Weld	258

SOLITRON
RIVIERA BEACH, FLORIDA

FOR
ZE, 30 AMPERE POWER DIODE (SILICON PLANAR)

DATE 8-8-72 DRWN. KW
CHKD.
APPD.

REVISION DATE E.

PROCESS FLOW	STANDARD OPERATION DETAIL
26. Stamp Assembly	552
27. Vacuum Bake	240
28. Encapsulate	262
29. Crimp Weld	412
30. Therma Shock	555
31. Helium Leak Test	261 or 561
32. Heat Age	330
33. Pressure Bomb (Gross Leak)	559
34. Classify	

SOLITRON
RIVIERA BEACH, FLORIDA

FOR
ZE, 30 AMPERE POWER DIODE (SILICON PLANAR)

DATE 8-8-72 DRWN. KW
CHKD.
APPD.

NO. 3 of 4

REVISION DATE E. O.

OPTIMUM WAFER FABRICATION PARAMETER; TYPE DIODE

SUBSTRATE	602298-1
EPITAXIAL LAYER THICKNESS	21-29 u 4-6 cm
BASE DEPOSITON TEMP.	860°C
TIME	5' Dwell; 5' Source; 20' Soak
V/I	60-80
	B_2H_6 - 0.3 L/MIN; O_2 - 0.3 L/MIN; N_2 - 2.5 L/MIN
BASE DIFFUSION TEMP.	1200°C
TIME	0.5 Hr. Wet O_2; 4.5 Hr. Dry O_2 N_2
V/I	400-600
Flows N_2 O_2	1 L/MIN
Xj	25-35 f
EMITTER DEPOSITION TEMP.	1060°C
TIME	5' Dwell; 5' Source; 30 Min Soak in O_2
V/I	
	PCl_3 - 0.05 L/MIN; N_2 - 0.4 L/MIN; O_2 - 0.225 L/MIN
N+ DEPOSITION TEMP.	
TIME	
V/I	
FINAL DIFFUSION * TEMP.	
TIME	
SLOW COOL	
BASE WIDTH (W_b)	

* SPECIAL PROCESSING CONSIDERATIONS: See Past history for actual Final Diffusion Time.

SLICE PART NO. 600938-1

DIE CHARACTORISTICS: BVcbo _____ BVceo _____ GAIN _____

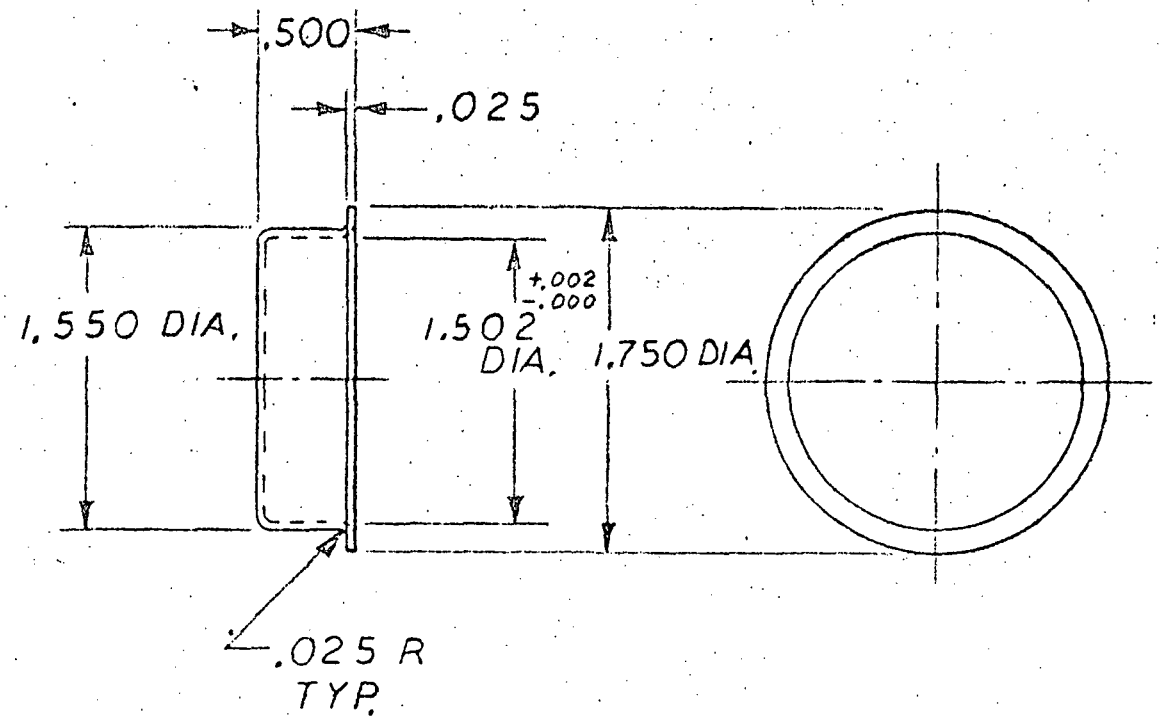
PRIME TYPE _____

VI.

DRAWINGS
(100 AMP)

REV	REVISION RECORD	DATE	E.O.

DRAWING NUMBER	REV
IT-A-523	



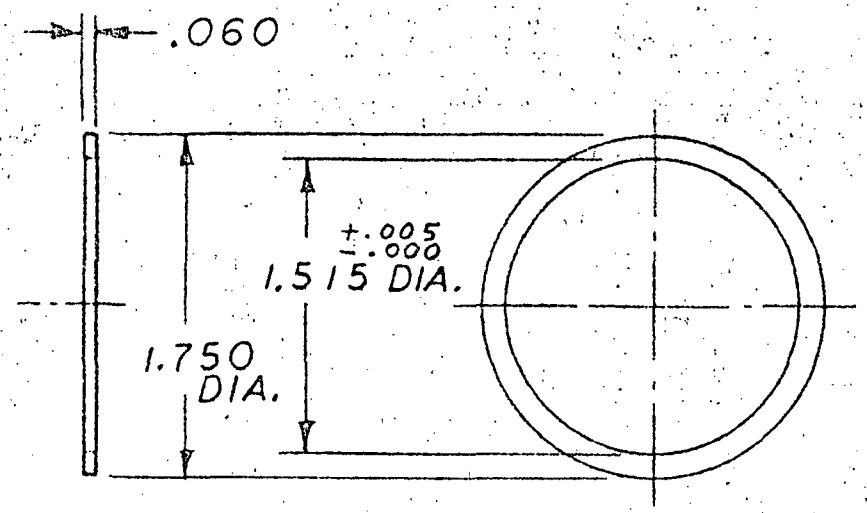
NEXT ASSY	TOLERANCE	DRAWING TITLE			
	ONE PLACE (.0) ±.020 TWO PLACE (.00) ±.010 THREE PLACE (.000) ±.005	CAP	DRAWN	LMS	6-16-72
			DRAFTING	LMS	6-16-72
	FRACTIONAL ±		ENGINEER	[illegible]	6-16-72
	ANGULAR ±		APPROVED	[illegible]	6-16-72

SOLITRON DEVICES INC.
TRANSISTOR DIVISION
RIVIERA BEACH, FLORIDA

MATERIAL	SPE SPEC.	SCALE	DRAWING NUMBER	REV
STN. STL.		FULL SIZE	IT-A-523	
		DEVICE: 100 AMP RAD.		

REV	REVISION RECORD	DATE	E.O.

DRAWING NUMBER	REV
IT-A-524	



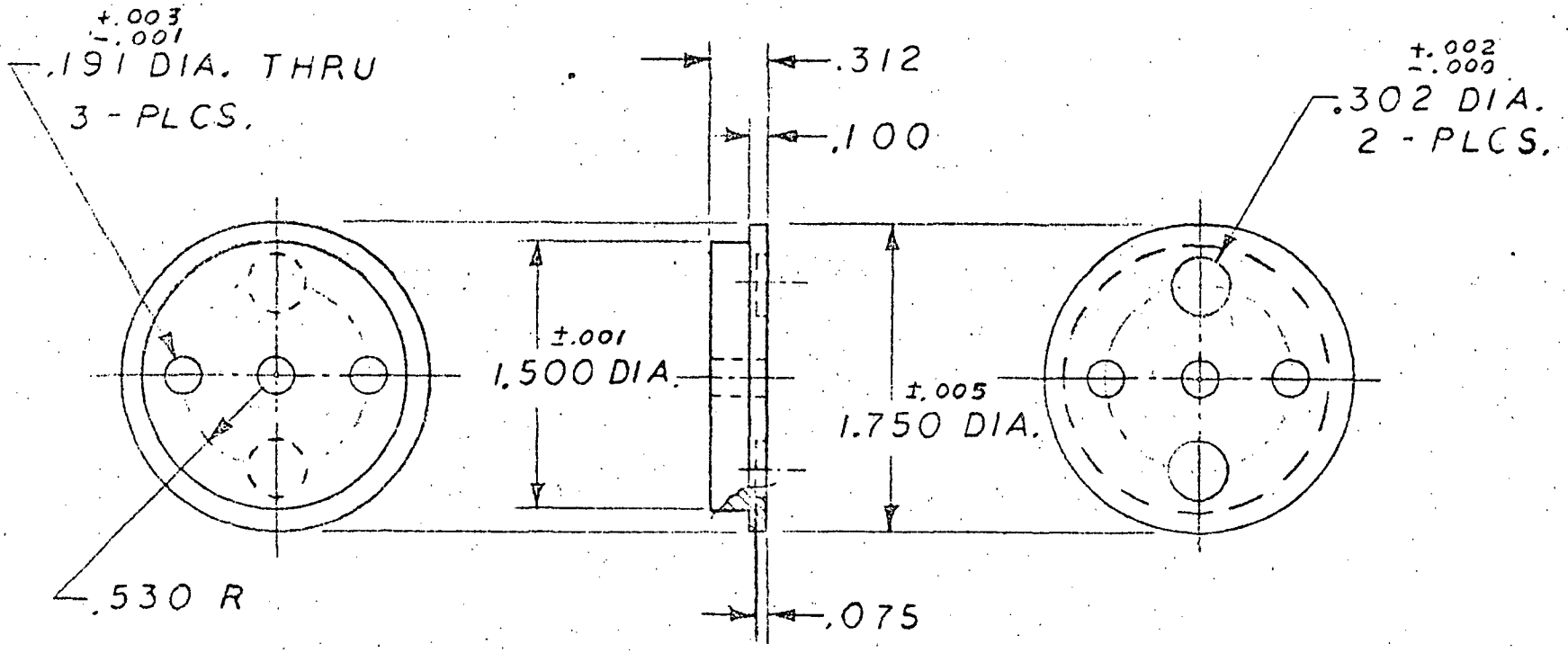
NEXT ASSY	TOLERANCE	DRAWING TITLE			
	ONE PLACE (.0) ±.020 TWO PLACE (.00) ±.010 THREE PLACE (.000) ±.005	WELD RING	DRAWN	LMS	6-16-72
	FRACTIONAL ±		DRAFTING	LMS	6-16-72
	ANGULAR ±		ENGINEER	RK	6-16-72
			APPROVED	RK	6-16-72

SOLITRON DEVICES INC.
TRANSISTOR DIVISION
RIVIERA BEACH, FLORIDA

MATERIAL	SPE SPEC.	SCALE	DRAWING NUMBER	REV
CRS		FULL SIZE	IT-A-524	
		DEVICE: 100 AMP RAD.		

REV	REVISION RECORD	DATE	E.O.

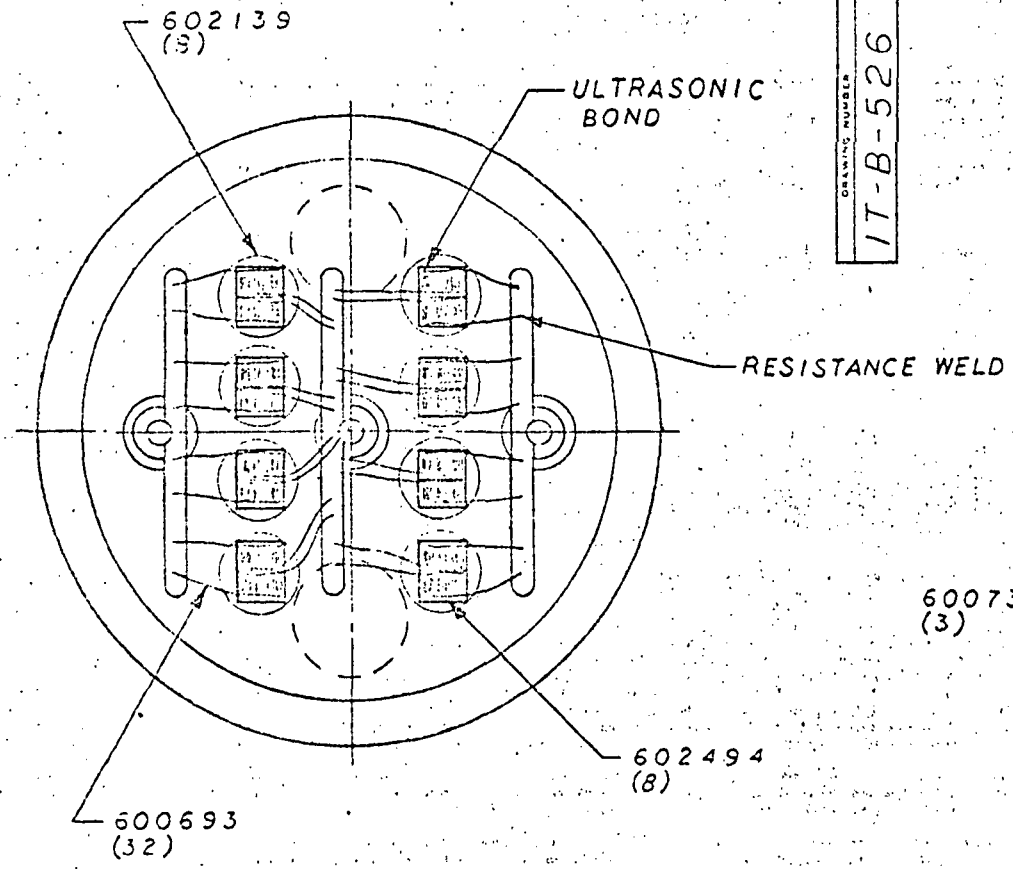
DRAWING NUMBER	REV
IT-A-525	



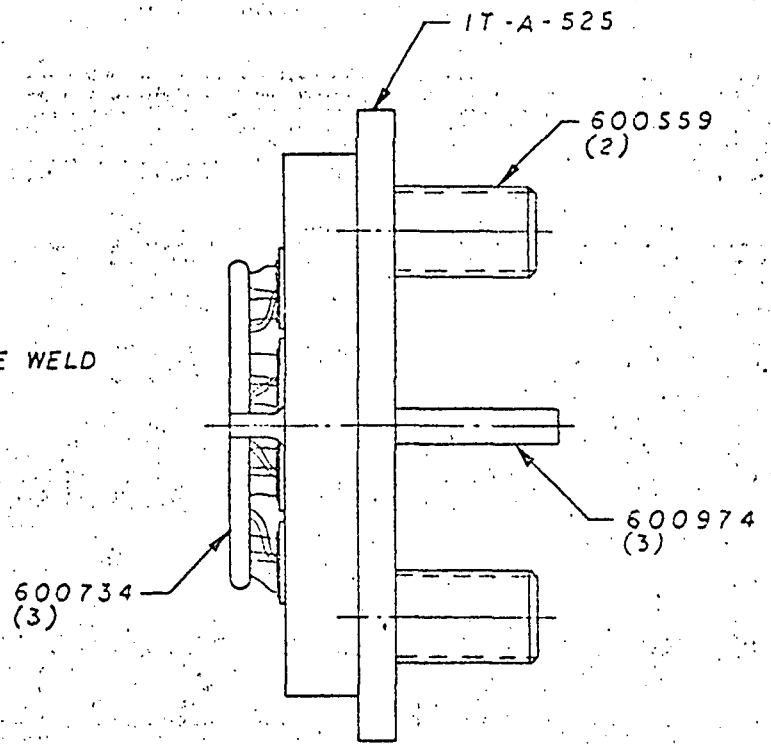
NEXT ASSY	TOLERANCE	DRAWING TITLE			
	ONE PLACE (.0) ±.020 TWO PLACE (.00) ±.010 THREE PLACE (.000) ±.005	BASE	DRAWN	LMS	6-16-72
			DRAFTING	LMS	6-16-72
	FRACTIONAL ±		ENGINEER	BJ	6-16-72
	ANGULAR ±		APPROVED	DC	6-16-72

SOLITRON DEVICES INC.
TRANSISTOR DIVISION
RIVIERA BEACH, FLORIDA

MATERIAL	SPE SPEC.	SCALE	DRAWING NUMBER	REV
OFHC COPPER		FULL SIZE	IT-A-525	
		DEVICE	100 AMP RAD.	



DRAWING NUMBER IT-B-526 REV



REV	REVISION RECORD	DATE	E.O.

NEXT ASSY

TOLERANCE
ONE PLACE ± .01 ± 020
TWO PLACE ± .001 ± 010
THREE PLACE ± .000 ± 005
FRACTIONAL ±
ANGULAR ±

DRAWING TITLE
TRANSISTOR & LEAD ASSY.

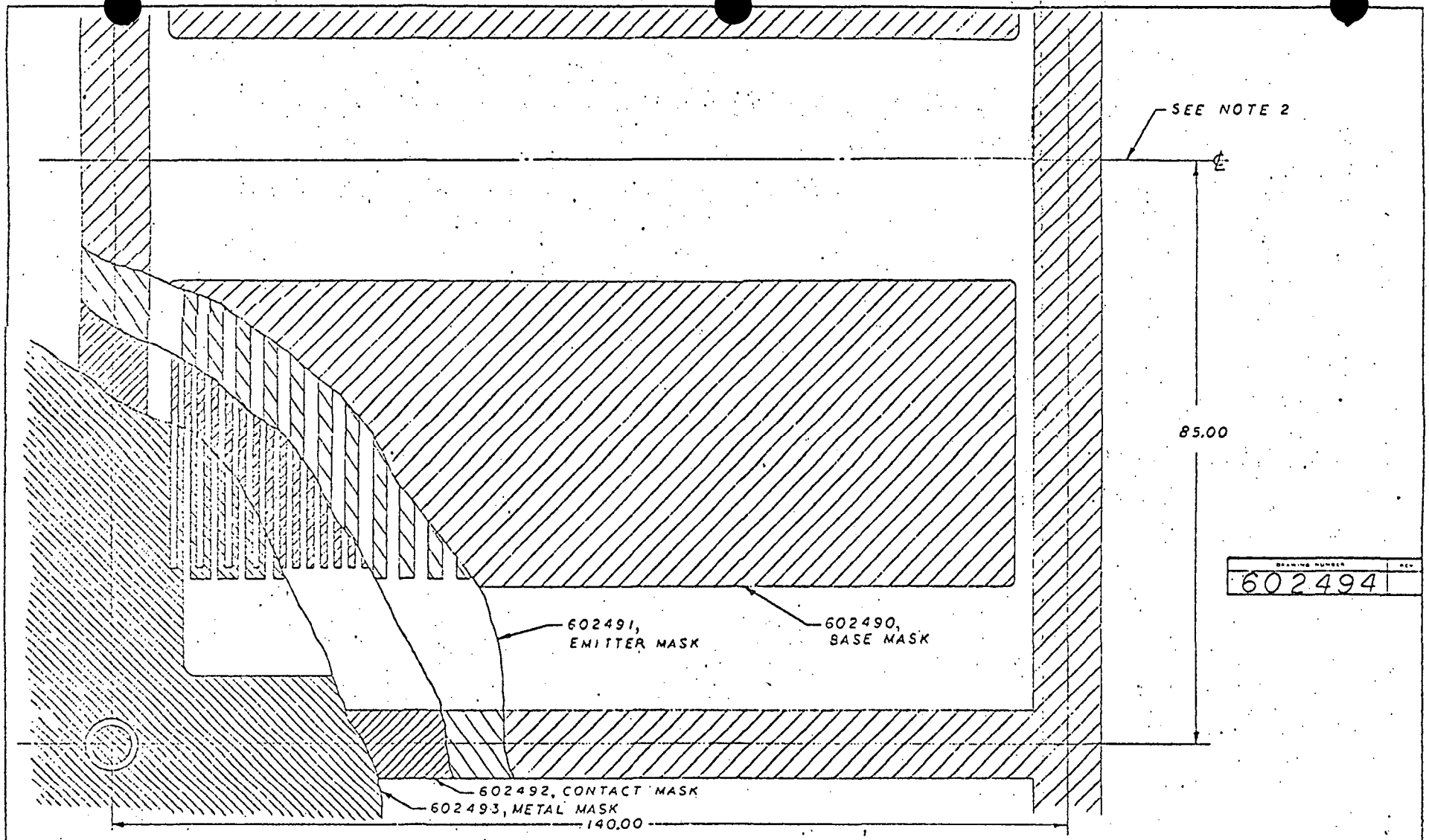
MATERIAL

BPE SPEC.

DRAWN	LMS	6-19-72
DRAFTING	LMS	6-19-72
ENGINEER		
APPROVED		
SCALE	3 X SIZE	
DEVICE	100 AMP RAD.	

SOLITRON DEVICES INC.
TRANSISTOR DIVISION
RIVIERA BEACH, FLORIDA

DRAWING NUMBER IT-B-526 REV



602494

NOTES:

1. ALL DIMENSIONS ARE IN MILS. (1 MIL=.001 INCH) & ARE FOR REFERENCE ONLY.
2. ONE HALF OF DETAIL ELEMENT SHOWN, GEOMETRY MUST BE SYMMETRICAL ABOUT CENTERLINE SHOWN. ALIGNMENT TARGETS NOT TO BE INCLUDED IN SYMMETRY, ONLY ONE TARGET PER ELEMENT.

NEXT ASSY	TOLERANCE	DRAWING TITLE	DRAWN	LMS 6-19-72	SOLITRON DEVICES INC.
	FRACTIONAL ±	COMPOSITE MASK	DRAFTING	LMS 6-19-72	TRANSISTOR DIVISION
	ANGULAR °		ENGINEER		RIVIERA BEACH, FLORIDA
			APPROVED		
MATERIAL		SPECIFIC	SCALE	100 X SIZE	DRAWING NUMBER 602494 REV
			DEVICE	7R MASK	

TC-21773-B

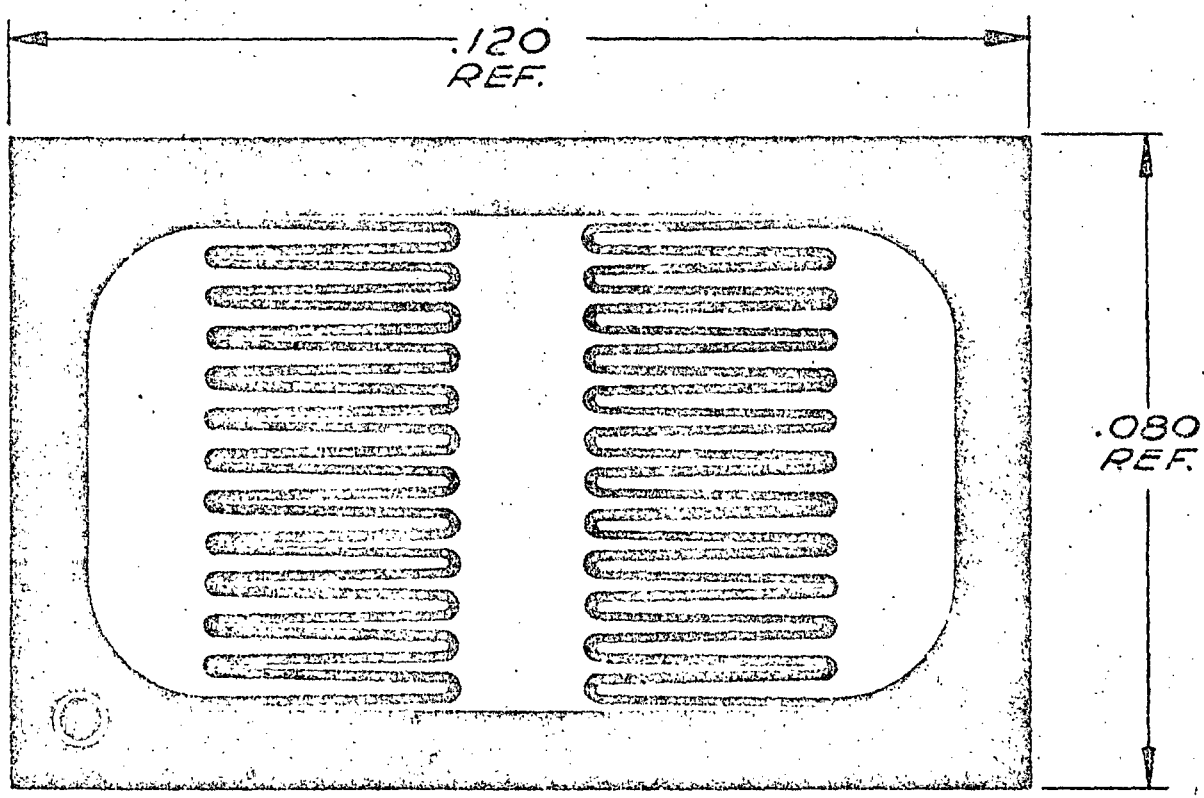
VII.

DRAWINGS

5 AMP

REV	REVISION RECORD	DATE	E.O.

DRAWING NUMBER	REV
602169	

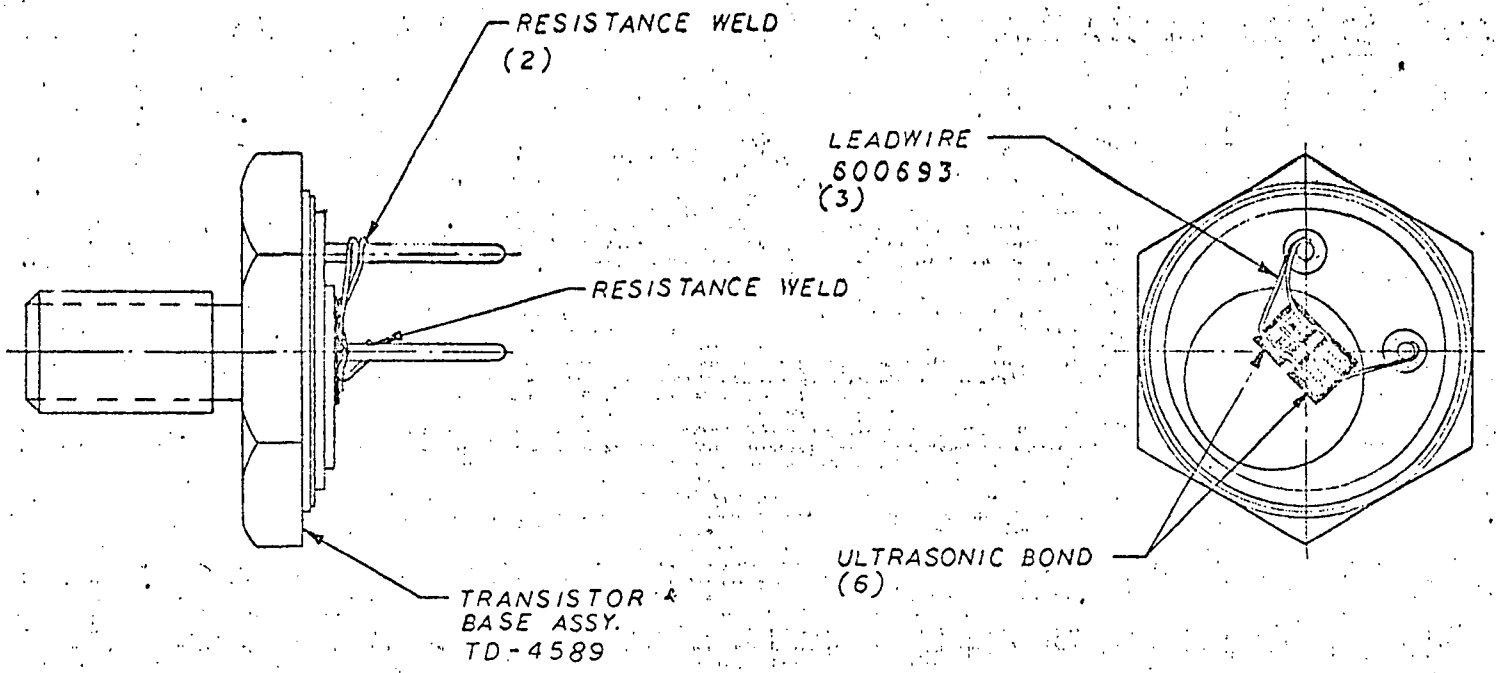


NEXT ASSY	TOLERANCE	DRAWING TITLE			
	ONE PLACE (.0) ±.020 TWO PLACE (.00) ±.010 THREE PLACE (.000) ±.005	COMPOSITE MASK	DRAWN	TAR	2-1-71
	FRACTIONAL ±		DRAFTING	RJR	2-1-71
	ANGULAR ±		ENGINEER		
			APPROVED		

SOLITRON DEVICES INC.
TRANSISTOR DIVISION
RIVIERA BEACH, FLORIDA

MATERIAL	SPE SPEC.	SCALE	42 X
		DEVICE	3R DIE

DRAWING NUMBER	REV
602169	



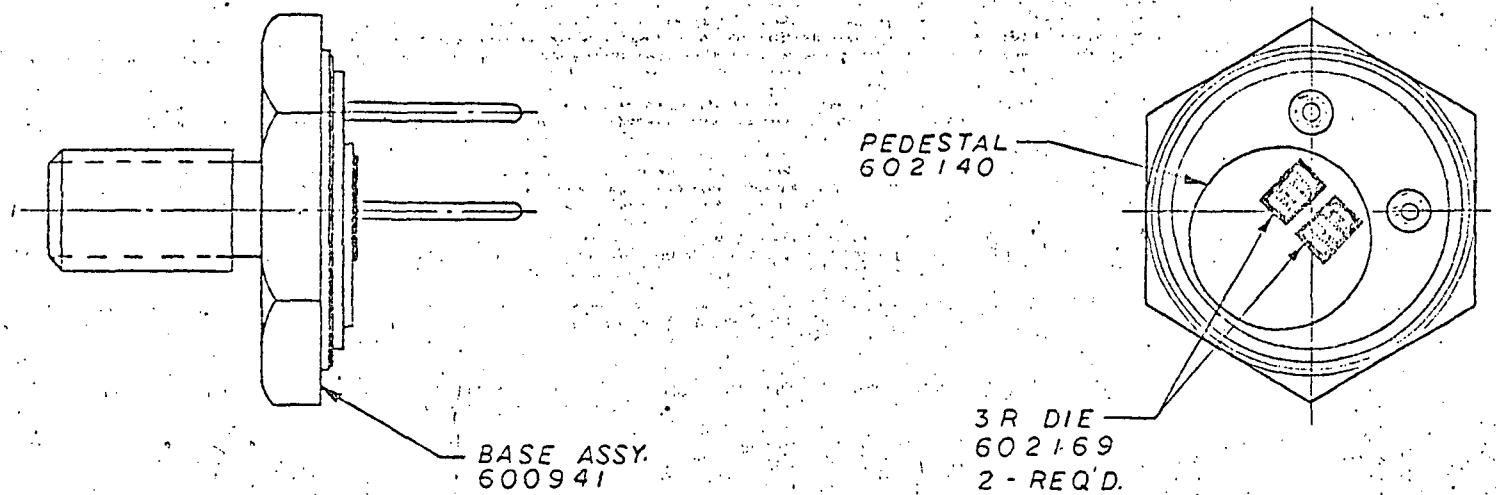
DRAWING NUMBER TD-4590 REV

NEXT ASSY	TOLERANCE	DRAWING TITLE			
	ONE PLACE ± .01 ± .030 TWO PLACE ± .001 ± .010 THREE PLACE ± .0005 ± .005	TRANSISTOR & LEAD ASSY.	DRAWN	LMS	7-31-72
	FRACTIONAL ±		DRAFTING	LMS	7-31-72
	ANGULAR ±		ENGINEER		7-31-72
			APPROVED		8-2-72

SOLITRON DEVICES INC.
TRANSISTOR DIVISION
RIVIERA BEACH, FLORIDA

REV	REVISION RECORD	DATE	E.O.

MATERIAL	SPEC SPEC.	SCALE	4 X SIZE	DRAWING NUMBER	REV
		DEVICE	6RSM	TD-4590	



DRAWING NUMBER TD-4589 REV

REV	REVISION RECORD	DATE	E. O.

NEXT ASSY	TOLERANCE	DRAWING TITLE	DRAWN	LMS	7-31-72	SOLITRON DEVICES INC.
TD-4590	ONE PLACE ±.01 ± .030 TWO PLACE ±.001 ± .010 THREE PLACE ±.0005 ± .005	TRANSISTOR & BASE ASSY.	DRAFTING	LMS	7-31-72	TRANSISTOR DIVISION RIVIERA BEACH, FLORIDA
	FRACTIONAL ±		ENGINEER		7-31-72	
	ANGULAR ±		APPROVED	BR	8-2-72	
MATERIAL		SPE SPEC.	SCALE	4 X SIZE		DRAWING NUMBER TD-4589 REV
			DEVICE	6RSM		

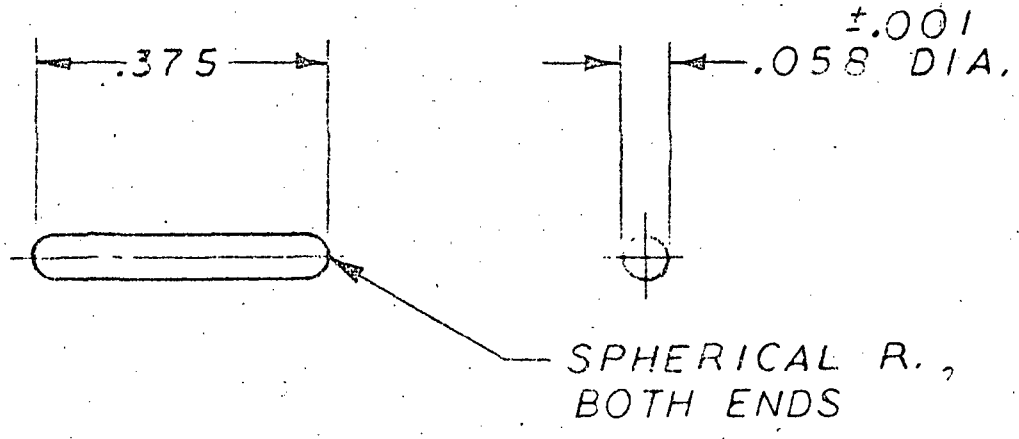
VIII.

DRAWINGS

RECTIFIERS

REV	REVISION RECORD	DATE	E.O.

DRAWING NUMBER	REV
602506	



NOTES:

1. MATERIAL: 3:1, 52 ALLOY, COPPER CORE.

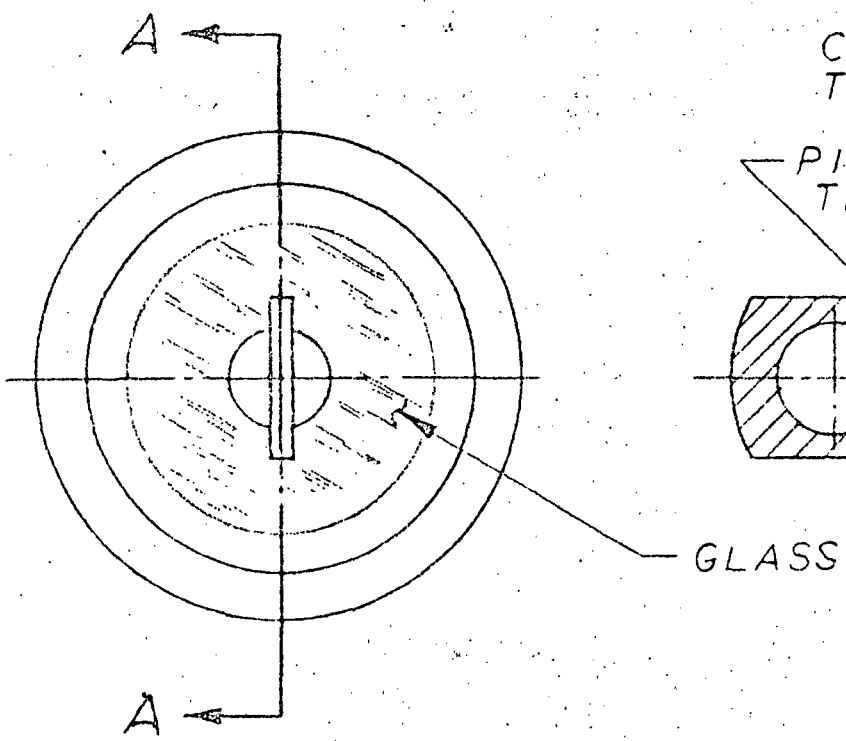
NEXT ASSY	TOLERANCE	DRAWING TITLE			
	ONE PLACE (.0) ±.020 TWO PLACE (.00) ±.010 THREE PLACE (.000) ±.005	STAND-OFF PIN	DRAWN	LMS	7-25-72
	FRACTIONAL ±		DRAFTING	LMS	7-25-72
	ANGULAR ±		ENGINEER	JCR	8-14-72
			APPROVED	[illegible]	8-14-72

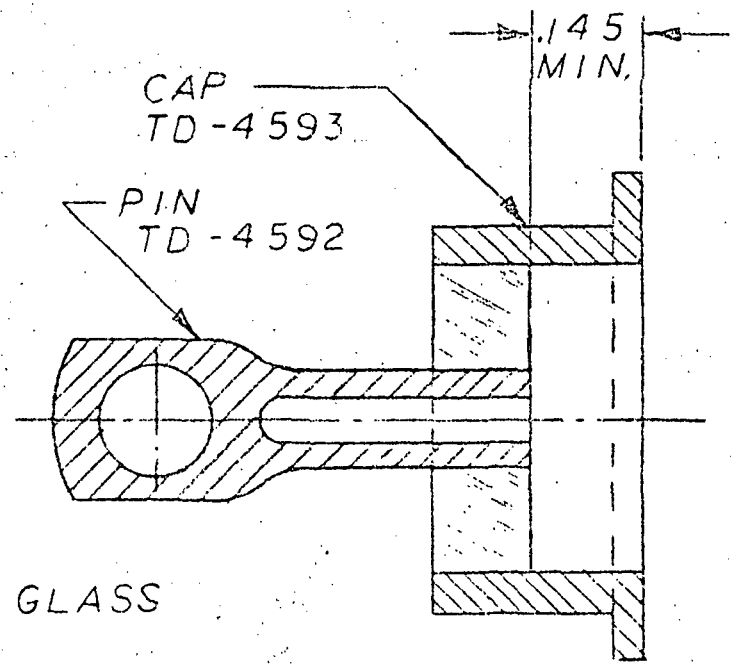
SOLITRON DEVICES INC.
TRANSISTOR DIVISION
RIVIERA BEACH, FLORIDA

MATERIAL	SPE SPEC.	SCALE	DRAWING NUMBER	REV
SEE NOTE 1		4 X SIZE	602506	
		DEVICE DO-5		

REV	REVISION RECORD	DATE	E.O.

DRAWING NUMBER	REV
TD-4591	





SECTION A-A

NEXT ASSY	TOLERANCE	DRAWING TITLE
	ONE PLACE (.0) ±.020 TWO PLACE (.00) ±.010 THREE PLACE (.000) ±.005	CAP ASSY.
	FRACTIONAL ±	
	ANGULAR ±	

DRAWN	LMS	8-11-72
DRAFTING	LMS	8-11-72
ENGINEER	JQ	8-11-72
APPROVED	BC	8-14-72

SOLITRON DEVICES INC.
TRANSISTOR DIVISION
RIVIERA BEACH, FLORIDA

MATERIAL	SPE SPEC.	SCALE	4 X SIZE	DRAWING NUMBER	REV
		DEVICE	DO-5	TD-4591	

REV	REVISION RECORD	DATE	E.O.

DRAWING NUMBER	REV
TD-4591	

1. FINISH: CLEAN WITH NO RESIDUE OR PARTICLES IN TUBES OR ON HEADER.

2. SEALS & TERMINALS MUST WITHSTAND HEATING TO 350°C AFTER WHICH LEAKAGE SHALL NOT EXCEED 1 X 10^{-9} ATM CC/SEC. RISE TIME 5 MIN. TIME AT TEMP ½ HR. MIN., ROOM AMBIENT COOL.

3. MINIMUM BREAKDOWN VOLTAGE ACROSS GLASS TO BE 500V 60~.

4. TERMINAL MUST WITHSTAND 20 LB PULL OR 20 IN. OZ TORQUE AFTER WHICH LEAKAGE SHALL NOT EXCEED 1 X 10^{-9} ATM CC/SEC.

5. GLASS TO BE OPAQUE.

6. PART MUST MEET CONDITION OF THERMAL SHOCK, MIL STD 202, METHOD 107A, TEST CONDITION C-10 CYCLES, AFTER WHICH LEAKAGE SHALL NOT EXCEED 1 X 10^{-9} ATM CC/SEC.

7. PART MUST MEET CONDITIONS OF THERMAL SHOCK (GLASS STRAIN), MIL STD 750, METHOD 1056 CONDITION A, 10 CYCLES, AFTER WHICH LEAKAGE SHALL NOT EXCEED 1 X 10^{-9} ATM CC/SEC.

8. EXTERIOR FINISH TO BE 63.

9. MAX LEAKAGE BETWEEN ISOLATED PIN & CASE TO BE 100 μA MEASURED BY APPLYING 100V.

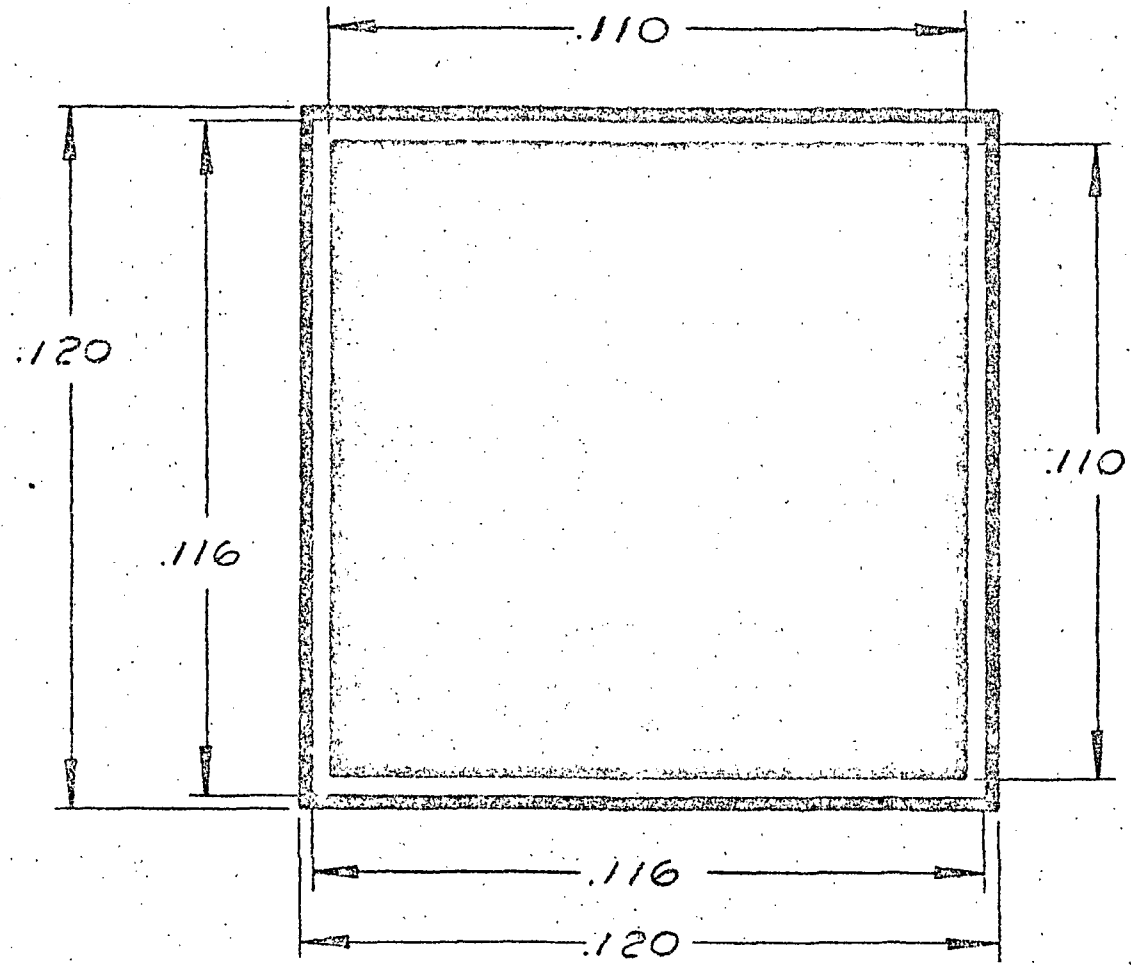
NEXT ASSY	TOLERANCE	DRAWING TITLE			
	ONE PLACE (.0) ±.020 TWO PLACE (.00) ±.010 THREE PLACE (.000) ±.005	CAP ASSY.	DRAWN	LMS	8-11-72
	FRACTIONAL ±		DRAFTING	LMS	8-11-72
	ANGULAR ±		ENGINEER	BC	8-14-72
			APPROVED	BC	8-14-72

SOLITRON DEVICES INC.
TRANSISTOR DIVISION
RIVIERA BEACH, FLORIDA

MATERIAL	SPE SPEC.	SCALE	4 X SIZE	DRAWING NUMBER	REV
		DEVICE	DO-5	TD-4591	

REV	REVISION RECORD	DATE	E.O.

DRAWING NUMBER	REV
602358	

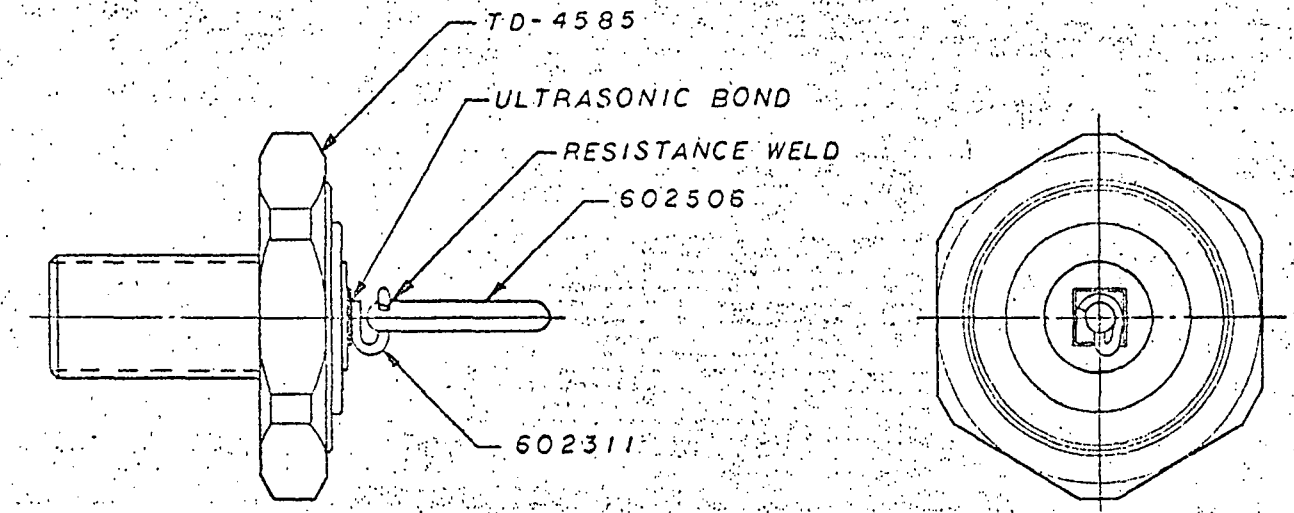


NEXT ASSY	TOLERANCE	DRAWING TITLE			
	ONE PLACE (.0) ±.020 TWO PLACE (.00) ±.010 THREE PLACE (.000) ±.005	COMPOSITE MASK	DRAWN	R	8-4-71
	FRACTIONAL ±		DRAFTING	R	8-4-71
	ANGULAR ±		ENGINEER		
			APPROVED		

SOLITRON DEVICES INC.
TRANSISTOR DIVISION
RIVIERA BEACH, FLORIDA

MATERIAL	SPE SPEC.	SCALE	30X
		DEVICE	ZE DIODE

DRAWING NUMBER	REV
602358	



TD-4586

REV	REVISION RECORD	DATE	E.O.

NEXT ASSY

TOLERANCE
ONE PLACE .01 ±.020
TWO PLACE .001 ±.010
THREE PLACE .0001 ±.005
FRACTIONAL ±
ANGULAR ±

DRAWING TITLE
DIODE & LEAD ASSY.

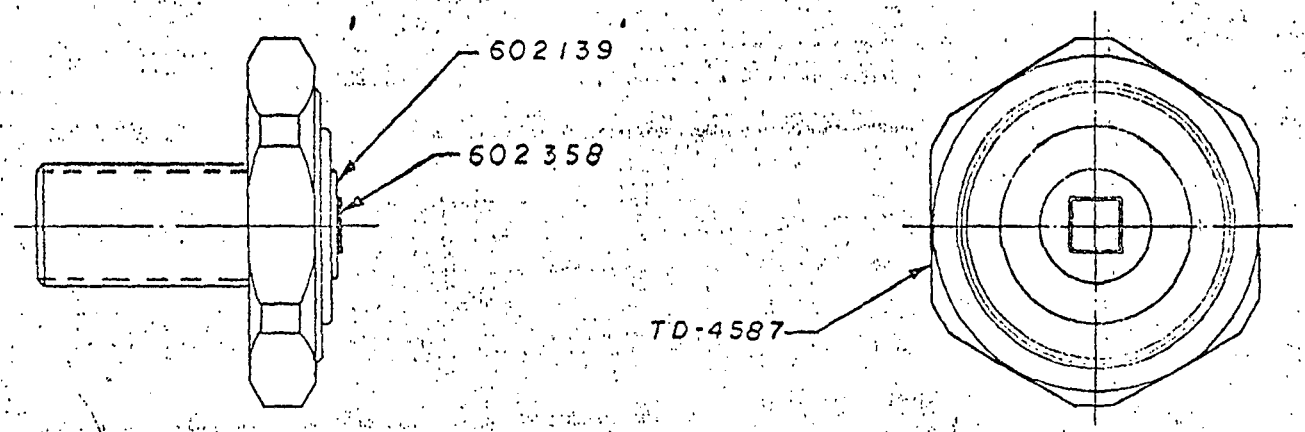
MATERIAL

SPEC SPEC.

DRAWN	LMS	7-25-72
DRAFTING	LMS	7-25-72
ENGINEER	BR	8-14-72
APPROVED	BR	8-14-72
SCALE	4 X SIZE	
DEVICE	DO-5	

SOLITRON DEVICES INC.
TRANSISTOR DIVISION
RIVIERA BEACH, FLORIDA

DRAWING NUMBER: TD-4586
REV.



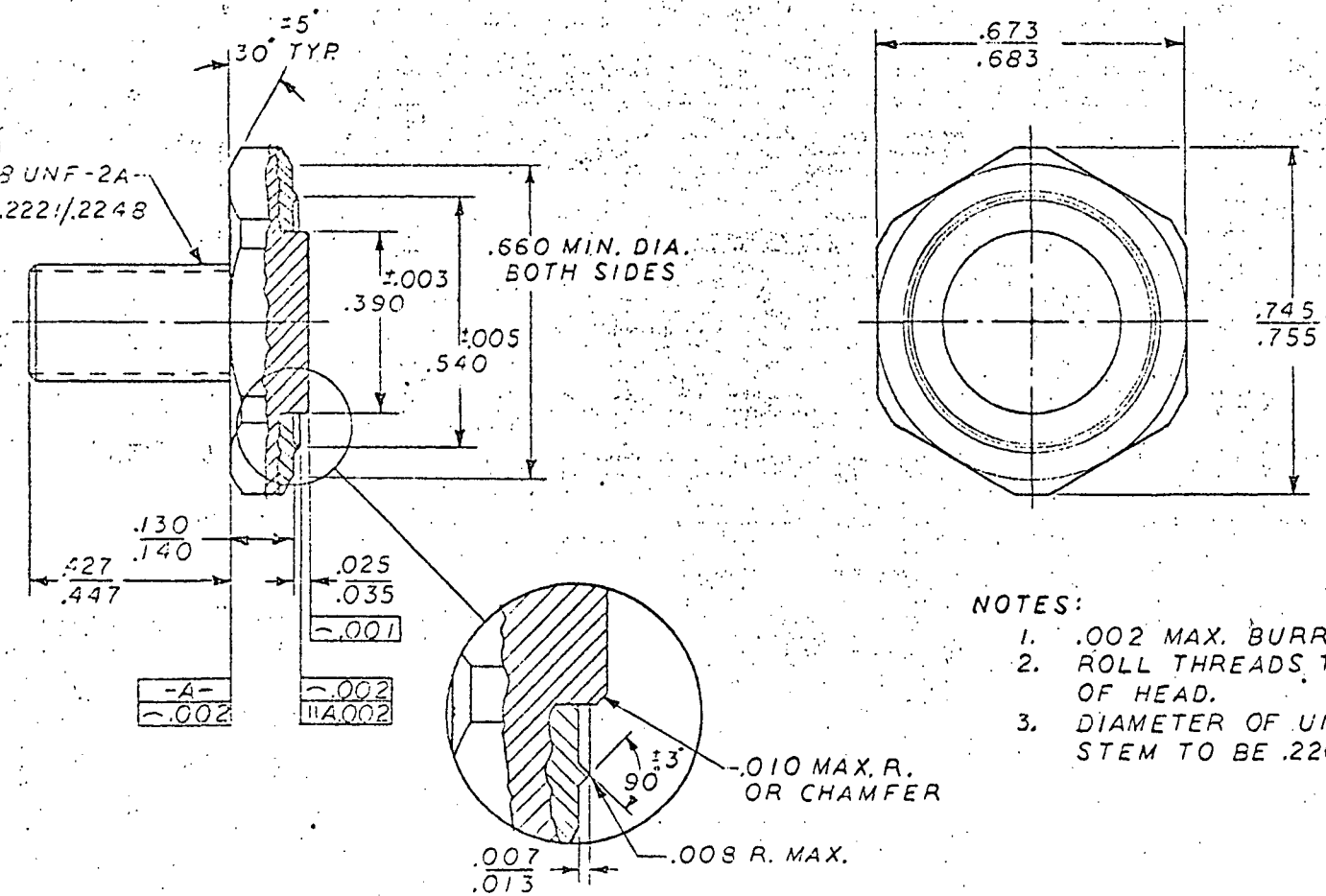
DRAWING NUMBER TD-4585 REV

NEXT ASSY	TOLERANCE	DRAWING TITLE			
	ONE PLACE 1.0 ± .030 TWO PLACE 1.00 ± .010 THREE PLACE 1.000 ± .005	DIODE & BASE ASSY.	DRAWN	LMS	7-25-72
	FRACTIONAL ±		DRAFTING	LMS	7-25-72
	ANGULAR ±		ENGINEER	BR	8-14-72
			APPROVED	EP	8-14-72
MATERIAL	SPEC.		SCALE	4 X SIZE	
			DEVICE	DO - 5	

SOLITRON DEVICES INC.
TRANSISTOR DIVISION
RIVIERA BEACH, FLORIDA

DRAWING NUMBER TD-4585 REV

REV	REVISION RECORD	DATE	E.O.



NOTES:

1. .002 MAX. BURR ALLOWED.
2. ROLL THREADS TO WITHIN 2 1/2 THREADS OF HEAD.
3. DIAMETER OF UNTHREADED PORTION OF STEM TO BE .220/.235.

NEXT ASSY	TOLERANCE	DRAWING TITLE			
	ONE PLACE ± .01 ± .030 TWO PLACE ± .001 ± .010 THREE PLACE ± .000 ± .005	BASE	DRAWN	L M S	1-14-72
	FRACTIONAL ±		DRAFTING	L M S	1-14-72
	ANGULAR ±		ENGINEER	FQ	2-14-72
			APPROVED	BB	2-14-72

SOLITRON DEVICES INC.
TRANSISTOR DIVISION
RIVIERA BEACH, FLORIDA

REV.	REVISION RECORD	DATE	E. O.

MATERIAL — SPEC SPEC.

SCALE: 4 X SIZE

DEVICE: DO-5

DRAWING NUMBER: TD-4587

REV.

TD-4587

(REF. DWG. SK-61966-1)

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