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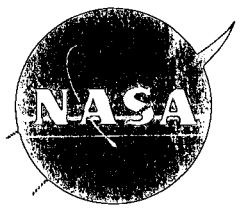

STUDY OF FEASIBILITY OF SOLID-STATE ELECTRIC SWITCH GEAR FOR AIRCRAFT AND SPACECRAFT

By

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Gale Sundberg, Project Manager

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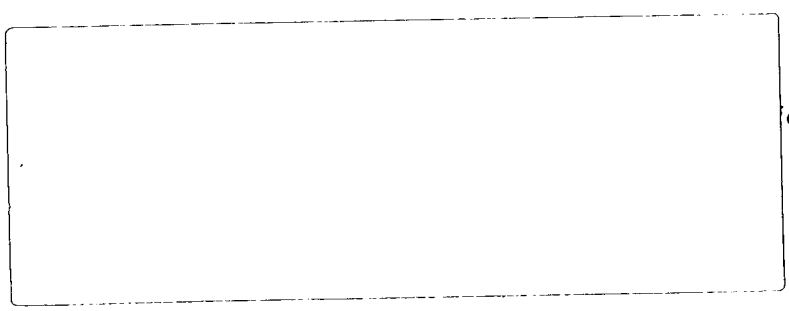

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16. Abstract

The design of a solid-state circuit breaker that can be interconnected to a second breaker to form a transfer switch is presented. The breaker operates on a nominal 270-V dc circuit and controls power to loads of up to 15 A. Automatic overload trip is provided as a function of excess energy measured through the breaker and/or excess current through the breaker. After an overload trip, up to nine preprogrammable attempts to reclose may be tried with programmable delays between each attempt. The breaker or switch is remotely controllable. Test data on performance in the laboratory over temperatures from -45 to 100°C are provided. The feasibility of solid-state switch gear has been established.

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FOREWORD

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Claudia Knox	for Parts Procurement and Accountability
Ed Buchanan	for System Engineering and Technical Direction

and many others for technical and administrative support.

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STUDY OF FEASIBILITY OF SOLID STATE ELECTRIC SWITCH GEAR FOR AIR AND SPACECRAFT

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SUMMARY

This final report defines the work accomplished to establish the feasibility of a solid-state circuit breaker and transfer switch for aircraft and spacecraft utilizing 270-volt dc power systems.

The effort was divided into three separate tasks. Task 1 was to perform a theoretical and experimental study with the objective of establishing and demonstrating the feasibility of a solid-state circuit breaker and a solid-state transfer switch. Task 2 required the detailed design of the breakers and switch; and Task 3 included the construction, test, and final delivery of breakers, switches, and test equipment.

The basic design requirements for both the breaker and the transfer switch are identified as follows.

1) To operate in a 270 ± 27 Vdc circuit with a nominal load current of 15 A;

2) To provide an automatic trip for overloads if the current I in excess of 15 amperes lasts over 10 ms and the value of I^2t exceeds 5 A^2-s. The circuit has to be open before I^2t = 30 A^2-s and a current of 18 A has to be interrupted before 92.6 ms;

3) The equipment must withstand a 300-V peak overvoltage above line voltage of 10 μs duration;

4) The breaker is required to have a "try again" capability. This requires it to reclose a programmable number of times (from zero to nine attempts) with a programmable time delay between attempts from 1 to 100 ms;

5) Forward voltage drop is defined as 2.5 V;

6) Life is defined as 1000 cycles of overload interruption;

7) External control is limited to 1 mJ of energy and the control is ohmically isolation from the power circuit;

8) The transfer switch is required to open one circuit before closing into the other.

Test requirements included:

1) Determination of the I^2t rating with respect to the ratio of overcurrent to nominal current;

2) Response to voltage variations from 3 to 300 V;

3) Variations of action thresholds and delays as a function of temperature from 0 to 50°C and down to -55°C and up to 100°C;

4) Effects of number of operations at temperatures of 0, 25, and 50°C.

The report is divided into three sections to correspond with the three phases of the contract. Section I identifies the major area studied and leads up to the design of the final circuitry, which is presented in Section II. Section III presents the results of the test program conducted on the breakers and transfer switch.

The conclusion reached as a result of this effort is that the design, development, construction, and operation of a high-voltage circuit breaker and transfer switch using completely solid-state components is technically feasible. Hardware is now in existence to substantiate this conclusion.

INTRODUCTION

Currently available conventional electric switch gear suffers from limited reliability and from functional limitations. The limited reliability stems from ingrained traditions of low-cost mass production of electromechanical devices such as breakers and power transfer switches. Inadequate quality control and reluctance of production crews to adhere to rigorous precautionary measures, such as continued maintenance of a clean room environment during the fabrication process, appear as one of the leading causes of the limited reliability of these components. The functional limitation consists primarily in the relatively slow response time of circuit breakers--on the order of milliseconds and more--and the need for manual operation of power transfer switches. The latter entails unnecessary routing of power cables to a central control point such as the cockpit of an aircraft.

Breakers should protect both the power transmission cables and the solid-state circuits and their components that are associated with the power system. To obtain this protection, the breaker must interrupt the flow of excessive current before it can damage critical elements in such associated circuits as semiconductor components.

The objective of this contractual effort was to establish the feasibility of solid-state switch gear in the form of circuit breakers and power transfer switches. The switch gear is to protect all parts of an electrical system by sensing overloads and opening the circuit before currents can rise to destructive values. The switch gear must provide remote control for open, close, or transfer actions and must provide programmable reclosure attempts in the event of an overload trip.

The scope of this effort included a study program and the design, development, construction, and delivery of three circuit breakers and one transfer switch for operation in a nominal 270-Volt 15-ampere dc circuit. Equipment tests were required to verify that the operational requirements were achieved and to determine performance variance with changes in voltage and temperature. Test equipment design and construction was also required.

The continued and increasing complexity of modern aircraft and the advent of manned spacecraft demand more attention to safety of electrical circuitry than has been practiced in the past. At the same time, costs in terms of weight and volume as well as dollars must be minimized. These requirements are

demanding consideration of higher voltages to minimize wire size, remote control to minimize wire length, and faster detection and reaction to protect equipment. The development of solid-state switch gear provides a means of protection that will operate many orders of magnitude faster than conventional mechanical breakers. Solid-state breakers will perform thousands of times more load current interruptions without requiring maintenance, and they do not create arcing or hot gas during operation. The development has potential application to such programs as Shuttle, Large Space Station, and advanced performance aircraft.

This work establishes the feasibility of solid-state switch gear and defines a basic design with which system type tests can be performed. System test can then determine those parameters of greatest importance for inclusion in a subsequent design for air and/or space testing. Electrical performance tests have been performed only in laboratory environments to date.

SECTION I

STUDY PHASE

The first phase of this effort involved a study program to determine limits and capabilities of both system requirements and some of the elements of component selection and circuit performance that would be needed in the subsequent design. Major portions of the study are presented.

System Considerations for Circuit Breaker Operation

A solid-state circuit breaker has the ability to open on overload in microseconds as contrasted to seconds or milliseconds for conventional magnetic or thermal circuit breakers. The specific requirements of this breaker development contract are reclosure within milliseconds after opening on overload and attempting to reclose as many as nine more times. This places specific requirements on the power source as well as the load. The breaker can be made to operate with any power source, but only those with fast response to changes in load current will permit the capabilities specified for the breaker to be used. A battery, or a source with a battery riding on it, meets this criterion as does a fuel cell. Both of these are high-current sources that offer a source impedance similar to that of a charged capacitor. For high-frequency changes in current, such as a current step function that might be caused by closing the breaker into a direct short, the main current limiting is by the series impedance of the current source.

In the case of a battery or fuel cell, this impedance will appear more inductive for higher frequency components, but the source will still be capable of almost unlimited current. Operation of a breaker with an inductive source such as an alternator rectifier or a dc generator imposes other restrictions on the breaker design. The current flowing in the source cannot rise quickly in the event of a short circuit; therefore, it will allow plenty of time for a breaker to open before current can rise to destructive levels. However, with an inductive source, the current will tend to flow even if the breaker does open, resulting in a transient voltage which the breaker must be designed to handle.

Although the power source with which the breaker was intended to operate was not specified, the fast response time indicated the use of a hard source such as a battery. This also appeared to be the most demanding, with respect to opening before current rise to destructive proportions, so a battery was used as the design source for the breaker.

Irrespective of the impedance of the power source, there will always be some inductance in the leads between the power source and the breaker. In an effort to predict these inductance values, an arbitrary length of 10 ft of wire of sizes that could most likely be used to feed a 15 A breaker was chosen. The wire data were computed for lightweight Kapton-insulated wire as used for our space programs. The values computed are shown in table I.

TABLE I.- INDUCATNCE, 10-FOOT WIRE LENGTHS

Wire size, AWG	Inductance, μH
0	3.82
2	3.96
4	4.08
8	4.36
12	4.78
16	5.08
18	5.15

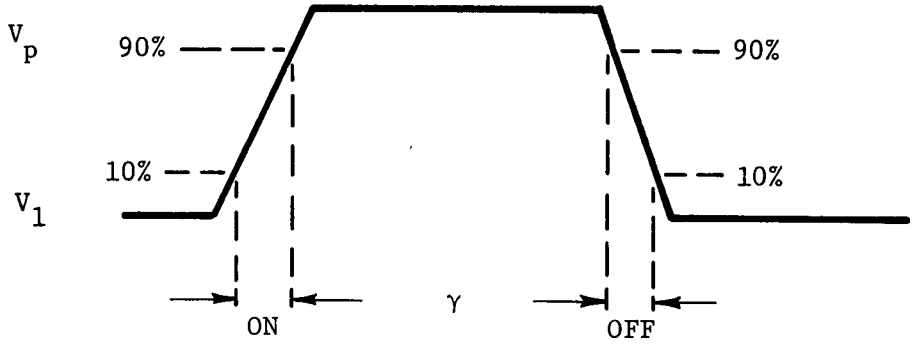
The inductances of two-wire distribution systems were also calculated for several wire sizes, since this wiring configuration would produce the lowest inductance and thus the highest rate of increase of fault current. These inductance values are shown in table II.

TABLE II.- INDUCTANCE, 10-FOOT LONG WIRE PARIS

Wire size, AWG	Inductance, μH
0	0.996
4	1.130
12	1.580

The calculated inductance of a pair of 12-gage wires was compared with the measured value of 3.2 μH for two hand-twisted 12-gage wires. This is in close agreement since the increase in separation required to change the inductance from 1.58 to 3.2 μH is only 0.06 in.

System Command Control.- The complexity and number of circuits that must be controlled in present-day aircraft and, conceivably in future manned spacecraft dictate the necessity of an automatic sequencer or possible computer control of circuit breakers. This need is reflected by the specification for ohmically-isolated commands of less than 1 mJ total command energy. It is possible that any data bus providing command signals from a sequencer will contain these commands in a data word of coded pulses or bits. This word will have to be decoded and a discrete command then transmitted to the breaker from the decoder. The 1 mJ command appears to be adequate, but should also be fully used. An arbitrary pulse input chosen for this development was a 15-V signal with time duration of 10 to 100 μs. This pulse is shown in figure 1. Its power level, defined as the "design goal," is shown in the curve of figure 2. This curve also shows the loci of both power and current values to provide 1 mJ of energy. Indicated on this curve is the present operating area for turn-on of the breaker in terms of power. It is obvious from the location of this point that redesign could maintain the input signal below the specified value and still decrease the sensitivity to noise and spurious signal turn-on by some orders of magnitude. Indicated in the figure are cross-hatched areas for both power and current-voltage which would be recommended design goals for future development.



$13.5 \leq V_p \leq 16.5$ V

$-0.5 \leq V_1 \leq 1.0$ V

$t_{ON} \leq 1.0$ μs

$t_{OFF} \leq 1.0$ μs

$10.0 \leq \gamma \leq 100.0$ μs

Note: The current delivered at V_p = 15.0 V shall be greater than 50 mA.

Figure 1.- Input Command Pulse

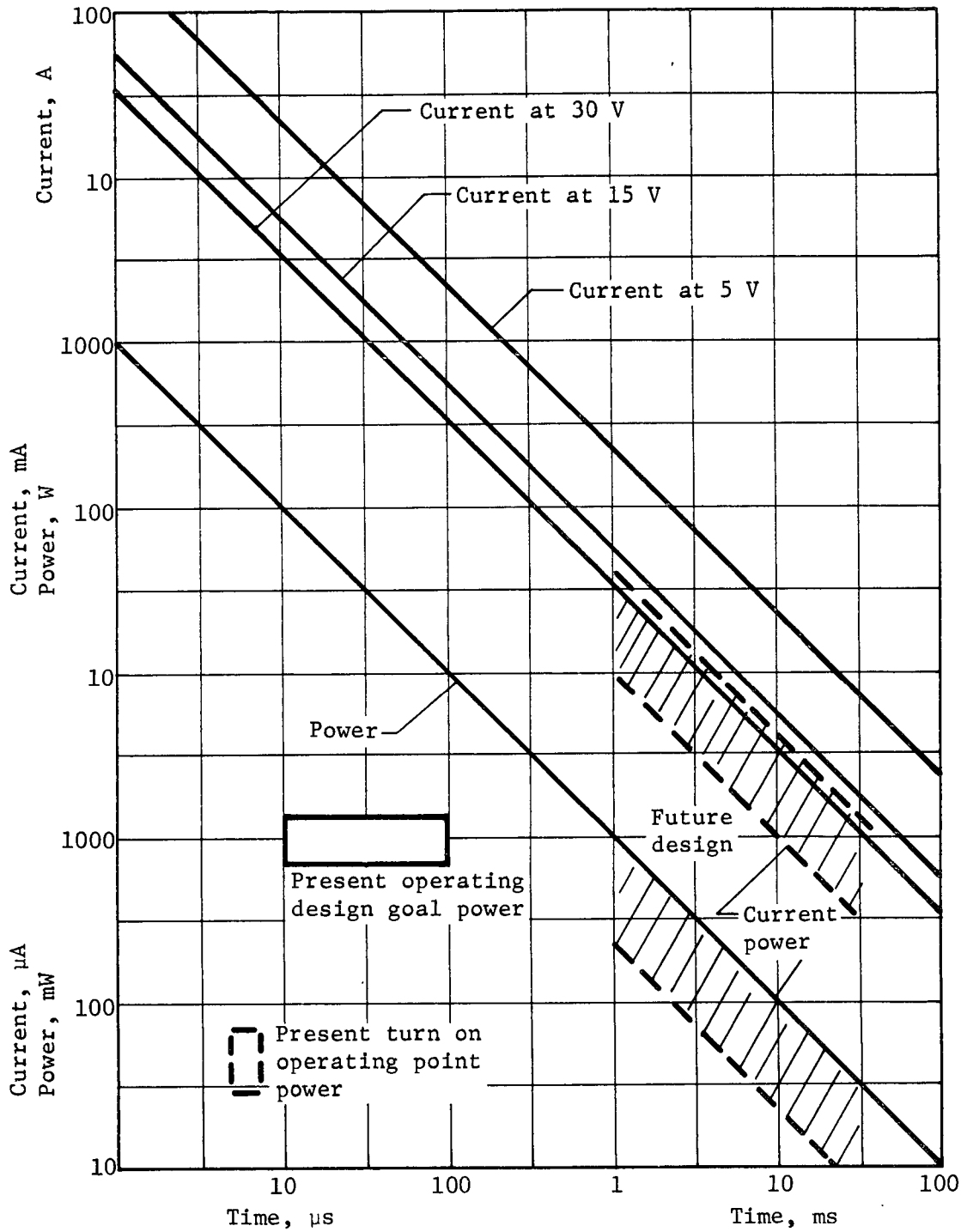


Figure 2.- Loci of 1-mJ Energy

Commutation Circuits

Due to the high voltage requirements (270 ± 27 V) and the nominal current of 15 A with overloads up to 45 A specified, it was determined that a Silicon-Controlled-Rectifier (SCR) must be used as the solid-state switching element. Selection of the main-switching SCR involved a number of requirements which had to be considered collectively. Comparison of capabilities was not aided by the limited number of characterization tests performed by the manufacturers and the broad tolerances reported or neglected in their literature. Some of these are discussed.

High voltage was an initial requirement, as any conceivable switching operation involved transients that were on the order of three to five times the source voltage. Fast recovery devices were essential to insure turn-off. This had to be accomplished with a minimum of energy storage and/or loss. Fast recovery devices were also necessary to comply with the fast recycle requirement.

A minimum forward voltage drop was defined, but it was further found that the voltage drop varied with current and temperature, as well as value of gate current and physical size of the chip within the device. Figure 3 shows voltage changes both with increasing and decreasing current for a General Electric SCR, C154M. It can be seen from this figure that a device of this type could appear as a noise source on a line if the load current were fluctuating near a current level associated with a considerable step in voltage drop.

The di/dt rating had to be considered as well as the impulse current rating. The SCR capability must reflect the requirements of the overall circuit in which the rate of current rise is mainly a function of the series inductance. The dv/dt rating was also a required consideration as both the transients of commutation and those possibly occurring due to other switching on the circuit, or from other external sources, must not be capable of gating the SCR on.

Finally, the thermal conductivity of the device--not only from the case to a heat sink, but also from the chip to the case--had to be evaluated to insure that up to ten overloads could be accepted at a nominal ms rate. The General Electric SCR, C156M, was finally chosen for the main switching application.

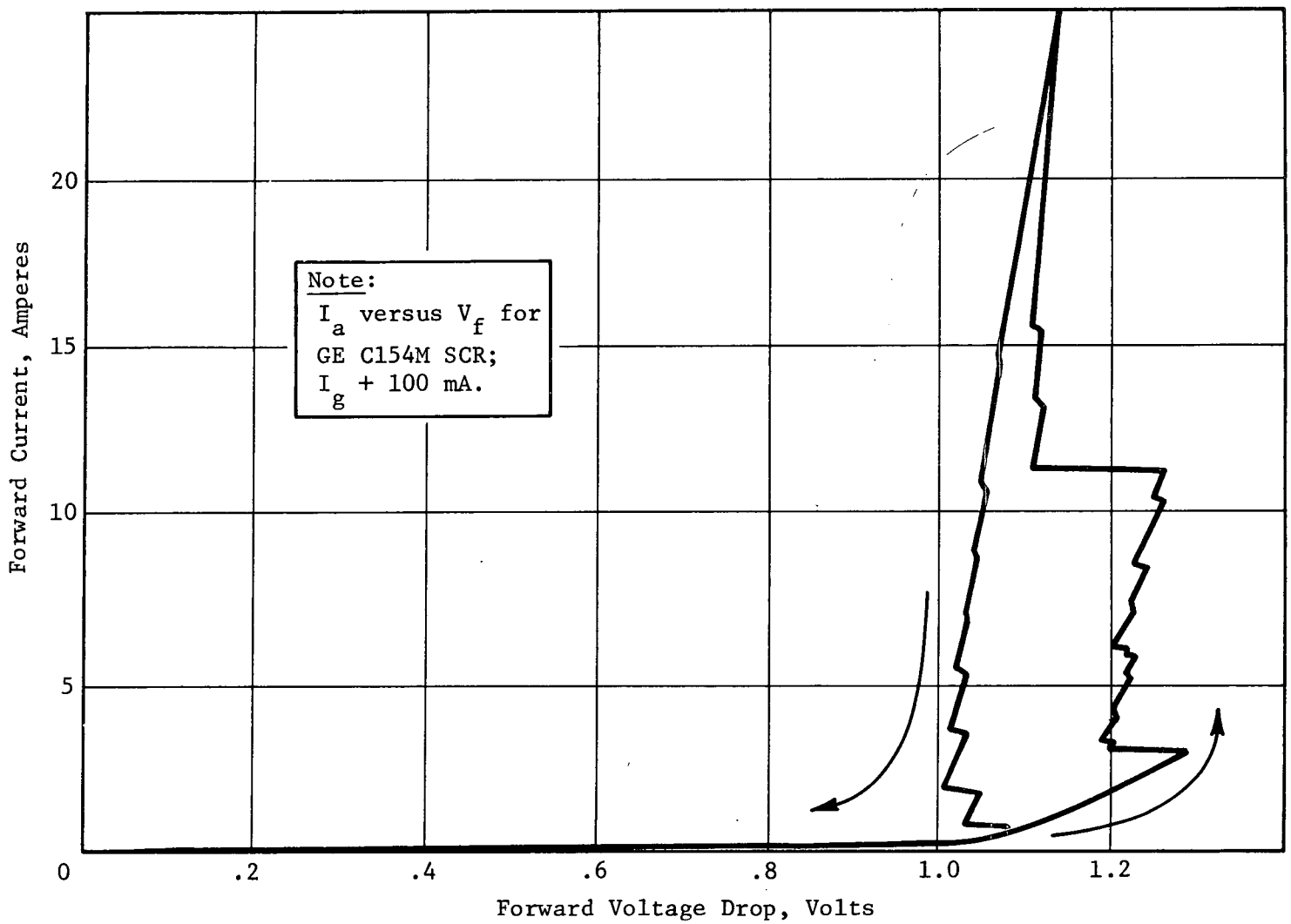


Figure 3.- Typical SCR Voltage Characteristics

In order to turn off an SCR, it is necessary to reduce the current flowing through it to a low value (sub-holding current), or more preferably to a zero-current condition. This can be conventionally achieved by applying a reverse potential for a time sufficiently long to allow the device to recover its blocking capability. The basic circuit for forced-commutation is shown in figure 4.

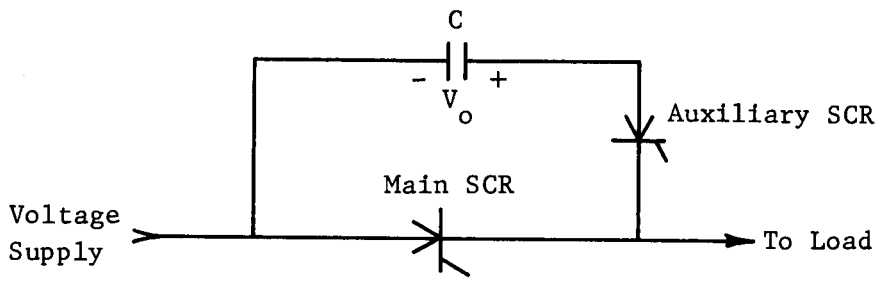


Figure 4.- Direct-Coupled Forced Commutation Circuit

The commutating capacitor is initially charged to V_o. When the main SCR is to be turned off, the auxiliary SCR is gated on. This applied a reverse potential to the main SCR. At first the capacitor provides the reverse bias across the SCR and simultaneously absorbs the load current. After the SCR current effectively ceases to flow, the capacitor carries load current only until it is charged through the load to source potential.

Figure 5 is a sketch of the SCR voltage and current Waveforms during the turn-off intervals. The capacitor is discharged from the initial value of V_o and charges to the supply voltage. In essence, the required time for the main SCR to recover is the minimum permissible time for the capacitor to discharge from V_o to zero. A mathematical expression for this criterion can be expressed as:

$$v_c = V_o - \frac{(I + I_{re})t_{re}}{C} - \frac{It_r}{C}$$

where I = load current, A

I_{re} = SCR reverse current

C = Capacitance, F

V_o = Initial capacitor voltage, V

v_c = Capacitor voltage, V

t_r = minimum SCR recovery time, s

t_{re} = SCR reverse conduction time, s

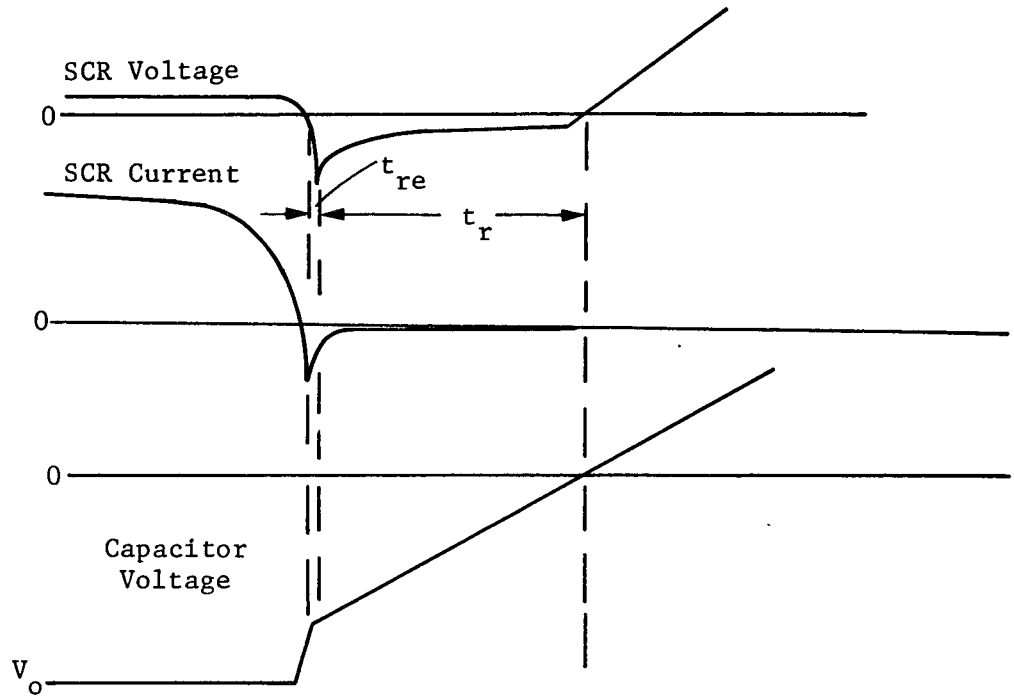


Figure 5.- Typical SCR Wave Forms during Forced Commutation

Because the maximum reverse blocking voltage capability of an SCR is very close to the forward blocking voltage, initial capacitor voltage may be of the same order of magnitude as that of the supply voltage. The minimum capacitance considered necessary for forced commutation is expressed by

$$C = \frac{I\left(t_r + t_{re}\right) + \left(I_{re}\ t_{re}\right)}{V_s}$$

where V_s = supply voltage, V.

For the solid-state switch gear, the maximum current under worst-case conditions would be 50 A and the lowest supply voltage would be 220 Vdc. For a maximum recovery time of 15 μs, the commutating capacitor would be 3.41 μf.

This neglects the effects of the SCR reverse current, and the condition that during the commutation interval, the load voltage is the sum of the supply voltage and the capacitor voltage. To overcome both of these problems an inductor could be used to absorb the voltage difference between supply and load and to limit the current during the reverse current interval.

Figure 6 shows a classical circuit employing a series inductor-capacitor network to turn off the main SCR.

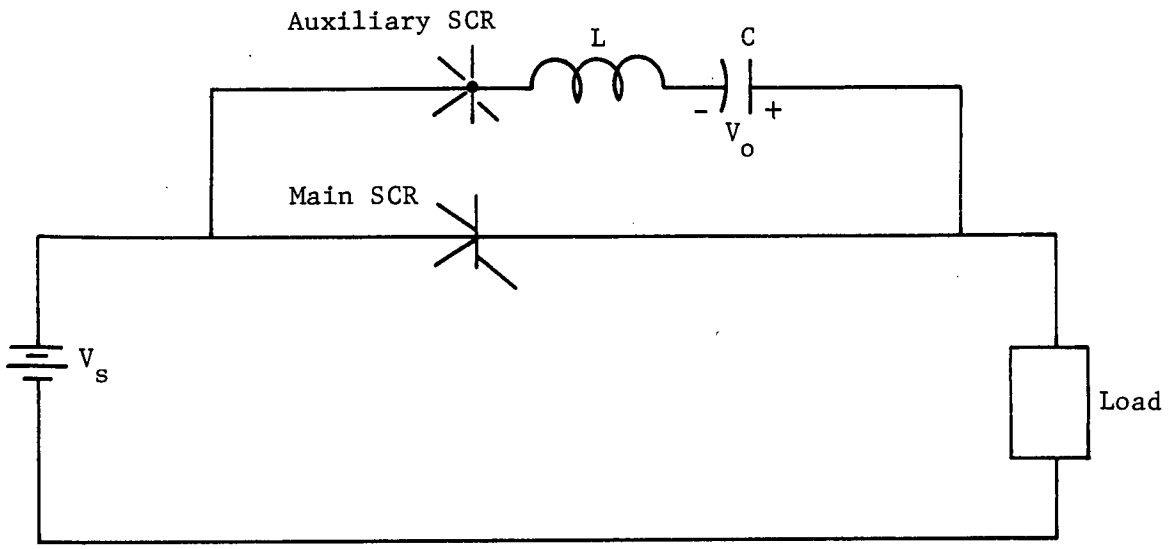


Figure 6.- Classical Method for Forced Commutation of an SCR

The response after the SCR reverse current ceases to flow is taken as

$$i = \frac{V_s + V_o}{\sqrt{L/C}} \sin \omega t + I_o \cos \omega t$$

where $\omega = \frac{1}{\sqrt{LC}}$,

and I_o is the load current at the time of gating the auxiliary SCR.

The optimum values[1] of capacitance and inductance for this type of circuit are:

---

[1]For a complete analysis of this circuit see *Principles of Inverter Circuits*, Bedford and Hoft.

$$C = 0.893 \frac{I_o t_r}{V_o},$$

$$L = 0.397 \frac{V_o t_r}{I_o}.$$

For the same conditions stated previously

$$C = 3.04 \ \mu F,$$

$$L = 26.2 \ \mu H.$$

This classical approach has the disadvantage of producing a voltage spike at the output equal to the supply voltage, since the load is in series with the L-C commutating network. Because any commutating circuit, which utilizes a network in parallel with the main SCR, will produce unacceptable voltage transients at the load, it was considered necessary to use impluse commutation as the means for turning off the main SCR.

The basic approach to the impulse commutating circuit uses a transformer to obtain reversal of potential as shown in figure 7.

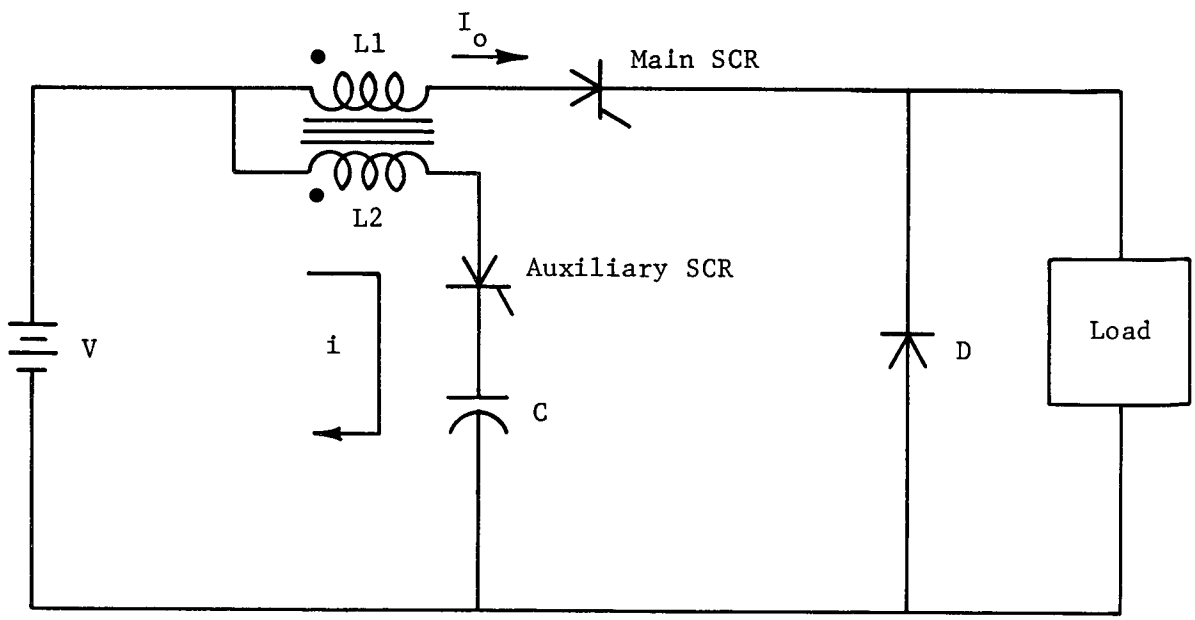


Figure 7.- Impulse Commutating Circuit with Transformer

This impulse commutating circuit derives the commutation pulses from the power source on gating the auxiliary SCR with Capacitor C discharged, and, through transformer action, induces a voltage in the circuit to oppose the supply voltage. The induced voltage, in this case, is the transformed inductor voltage of the L-C network. This inductor voltage is the difference between the supply and capacitor voltages. Because the capacitor voltage increases as the capacitor charges, the induced commutation voltage pulse will decrease with time. When the capacitor charges to where the commutation voltage pulse is zero, the commutation effort is complete. During the remaining interval of time, forward voltage is reapplied to the main SCR. The basic design criterion of this circuit is to maintain a reverse potential on the main SCR until it recovers blocking capability. Following this period of time, the commutation circuit is permitted to continue its cycle in order to "naturally commutate" the auxiliary SCR off. At the end of such a cycle, the capacitor voltage will be greater than the supply voltage. Therefore, it is necessary to employ accessory circuits to discharge the capacitor. Because the capacitor can charge to a potential, which can exceed the SCR blocking capability, it is also necessary to limit the capacitor voltage by clamping the capacitor voltage to supply voltage or to parallel the capacitor with a resistor late in the commutation cycle.

These secondary circuits can impose requirements as stringent as those of the principle main-SCR circuit because it is necessary to observe the same design criteria in assuring that the auxiliary SCR will have sufficient recovery time. It should be noted that the auxiliary SCR has to conduct a commutation current that is greater than the load current of the main SCR. This requirement is due not only to response of the commutation circuit, but also to transformation of the load current from the main SCR circuit to the commutation circuit at the onset of the commutation cycle.

For the following analysis of the impulse commutating circuit, all circuit parameters are considered to be ideal; the passive elements are considered linear and lossless, and the remaining elements are considered perfect switches. At the instant the auxiliary SCR is gated on, the circuit response is:

$$I = \frac{V}{L_2\left(S^2 + \frac{1}{L_2\ C}\right)} + \frac{I_o\ MS}{L_2\left(S^2 + \frac{1}{L_2\ C}\right)} \qquad (1)$$

where I_o = load current in amperes, prior to gating the auxiliary SCR

S = complex Laplacian variable

$M = L_1/L_2$.

In real time,

$$i = \frac{V}{Z_o} \sin \omega t + I_o \frac{N_1}{N_2} \cos \omega t \tag{2}$$

where $\omega = \frac{1}{\sqrt{L_2 C}}$,

$Z_o = \sqrt{\frac{L_2}{C}}$,

$\frac{N_1}{N_2} = \frac{M}{L_2}$.

also

$$V_c = V - V \cos \omega t + I_o Z_o \left(\frac{N_1}{N_2}\right) \sin \omega t \tag{3}$$

$$V_a = V - V\left(\frac{N_1}{N_2}\right) \cos \quad t + I_o Z_o \left(\frac{N_1}{N_2}\right)^2 \sin \omega t \tag{4}$$

where V_c = capacitor voltage,

V_a = Main SCR anode voltage.

The value of t giving a maximum value for I (t_m) can be found by differentiating equation (2) and setting the results equal to zero. This gives

$$\frac{V}{Z_o I_o} \left(\frac{N_2}{N_1}\right) \cos wt_m = \sin wt_m.$$

Letting $x = \frac{V}{Z_o I_o}\left(\frac{N_2}{N_1}\right)$ and defining $\theta = wt_m$ gives the following results:

$$\tan \theta = x$$

$$\sin \theta = \frac{x}{x^2+1}$$

$$\cos \theta = \frac{x}{x^2+1} .$$

Substituting these values back into equation (2) gives

$$I_{max} = \frac{V}{Z_o} \sin \theta + I_o \frac{N_1}{N_2} \cos \theta$$

$$= I_o \frac{N_1}{N_2} [x^2 \cos \theta + \cos\theta]$$

$$= I_o \frac{N_1}{N_2} \sqrt{x^2 + 1} . \qquad (5)$$

Similarly, equations (3) and (4) can be differentiated to find their maximum values. These do not occur at the t_m defined above. It is found from the differentiation that both occur at some t_n such that

$$x \sin wt_n = -\cos wt_n .$$

Defining $\phi = wt_n$ gives $\tan \phi = -1/x$, which implies that $\phi = \theta + \pi/2$ (as expected in a pure reactive circuit), and

$$\sin \phi = \frac{1}{\sqrt{1 + x^2}}$$

$$\cos \phi = \frac{-x}{\sqrt{1 + x^2}} .$$

Substituting these back into equations (3) and (4) gives maximum values for V_a and V_c:

$$V_a \text{ (max)} = V + I_o Z_o \sqrt{x^2 + 1}$$

$$V_c \text{ (max)} = V + I_o Z_o \left(\frac{N_1}{N_2}\right) \sqrt{x^2 + 1} \ .$$

Minimum values would occur at $\phi + \pi$ if no switching intervened. They are:

$$V_a \text{ (min)} = V - I_o Z_o \sqrt{x^2 + 1}$$

$$V_c \text{ (min)} = V - I_o Z_o \left(\frac{N_1}{N_2}\right) \sqrt{x^2 + 1} \ .$$

The potential across the main SCR is essentially V_a because the cathode of the SCR is held to zero when the SCR is reverse-biased and the SCR is assumed to have regained its blocking state when it is forward-biased. Also the reverse voltage at the start of the commutating cycle is

$$V_a \text{ (initial - reversed)} = V \left(\frac{N_1}{N_2} - 1\right) .$$

As the capacitor charges, the main SCR voltage reaches 0 V. This occurs at some $t_q < t_n$. At this instant, $V_a = 0$, giving [from equation (4)]

$$V + V\left(\frac{N_1}{N_2}\right) \cos wt_q - I_o Z_o \left(\frac{N_1}{N_2}\right) \sin wt_q \ .$$

This can be manipulated to give

$$\frac{x}{\sqrt{x^2+1}} \left(\frac{N_1}{N_2}\right) = \frac{x}{\sqrt{x^2+1}} \cos wt_q - \frac{1}{\sqrt{x^2+1}} \sin wt_q$$

or
$$\sin \theta \left(\frac{N_1}{N_2}\right) = \sin \theta \cos wt_q - \cos \theta \sin wt_q$$

$$= \sin (\theta - wt_q) \ .$$

Solving for t_q,

$$t_q = \sqrt{LC}\left\{\sin^{-1}\left(\frac{x}{\sqrt{x^2+1}}\right) - \sin^{-1}\left[\frac{\frac{N_2}{N_1}}{\sqrt{x^2+1}}\right]\right\}$$

$$t_q = \sqrt{LC}\left\{\sin^{-1}\left(\frac{x}{\sqrt{x^2+1}}\right) - \sin^{-1}\left[\frac{I_o x}{I_{max}}\right]\right\} . \qquad (6)$$

[The last step is from substitution of equation (5).]

In terms of the same parameters,

$$I = I(max) = I_o\left(\frac{N_1}{N_2}\right)\sqrt{x^2 + 1} , \qquad (7)$$

$$V_a\ (max) = V + I_o Z_o\ \sqrt{x^2 + 1} , \qquad (8)$$

and $$V_c(max) = V + I_o Z_o \left(\frac{N_1}{N_2}\right)\sqrt{x^2 + 1} . \qquad (9)$$

The design criteria for the circuit are based on limiting the peak current in the auxiliary SCR to the rated value of the SCR and insuring the minimum allowable recovery time for the main SCR. The procedure for this approach utilizes the ratio of the load impedance to the commutation circuit impedance as defined below.

Using the maximum current rating for the SCR as a limitation, the critical turnoff time, t_q, can be derived from equation (6)

$$\frac{t_q}{LC} = \sin^{-1}\left(\frac{x}{\sqrt{x^2 + 1}}\right) - \sin^{-1}\left(\frac{I_o x}{I_{max}}\right).$$

This expression is plotted in figure 8 as a function of x for a ratio of

$$\frac{I_o}{I_{max}} = 0.5 .$$

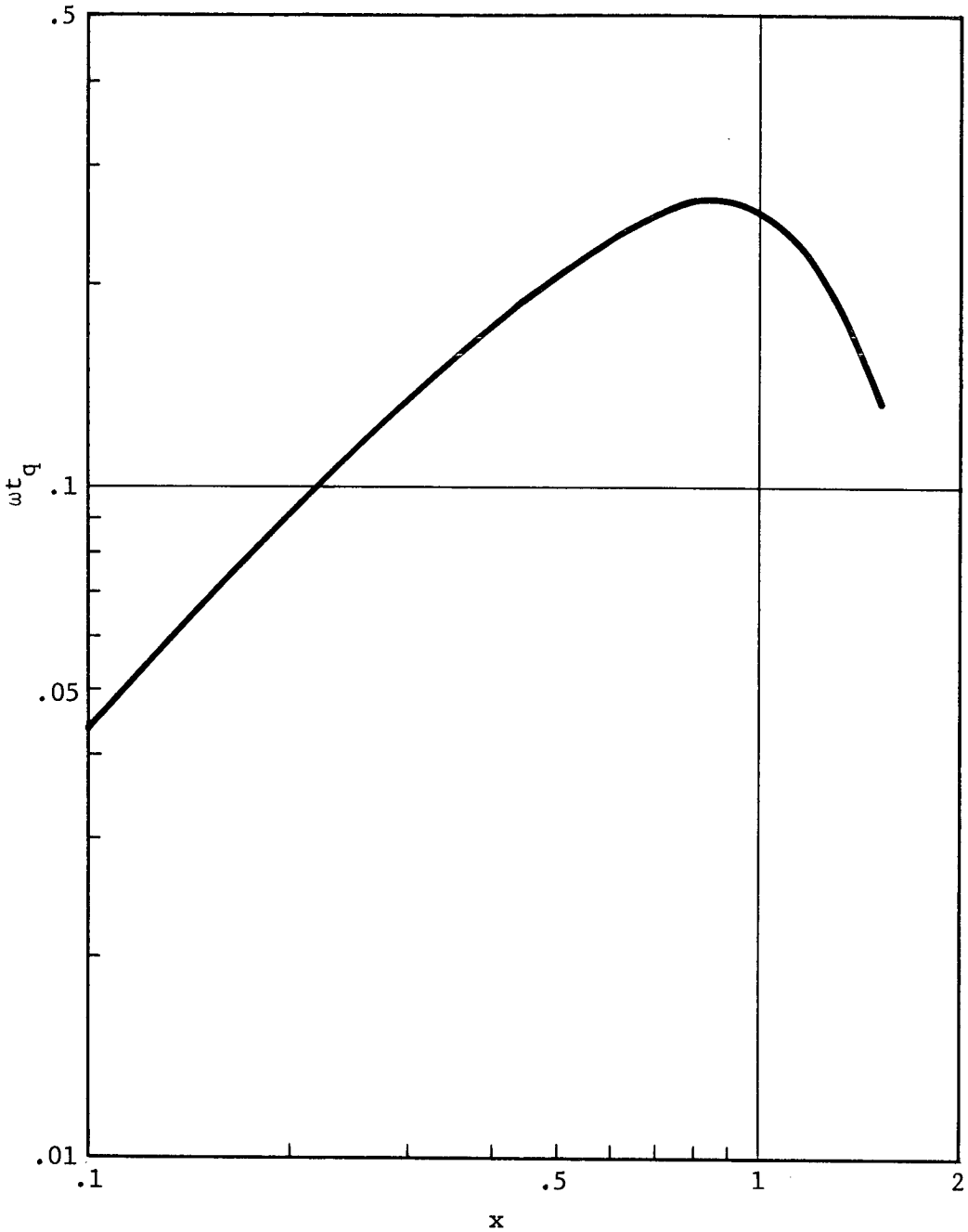


Figure 8.- Optimizing Function for Critical Turn Off Time for a Transformed Impulse Commutating Circuit

From this figure it can be seen that the maximum t_q for a given LC produce is for x = 0.88 and $t_q = 0.266 \sqrt{LC}$.

For the operating voltage levels and currents

$N_1/N_2 = 1.5$

$L = 226\ \mu H$

$C = 12.4\ \mu F.$

The current at time, t_q, is at maximum; therefore, the inductor must be designed to assure the derived value as a minimum for a current of 100 A. Further analysis reveals that the capacitor would see a maximum voltage of 1,307 V. For this reason, it is necessary to modify the basic circuit by utilizing a clamping network on the transformer in order to limit the capacitor voltage overshoot to a value less than the capacitor rating.

Figure 9 shows the basic commutating circuit with modifications to meet the various design restrictions. The circuit functions to limit the extent of the capacitor charge by clamping the capacitor voltage to the supply voltage. When the capacitor voltage exceeds the supply voltage by the breakdown potential of the zener, SCR-3 is gated on, affectively clamping the capacitor to the supply voltage. The inductor voltage will thus be limited to the forward voltage drop across SCR-3.

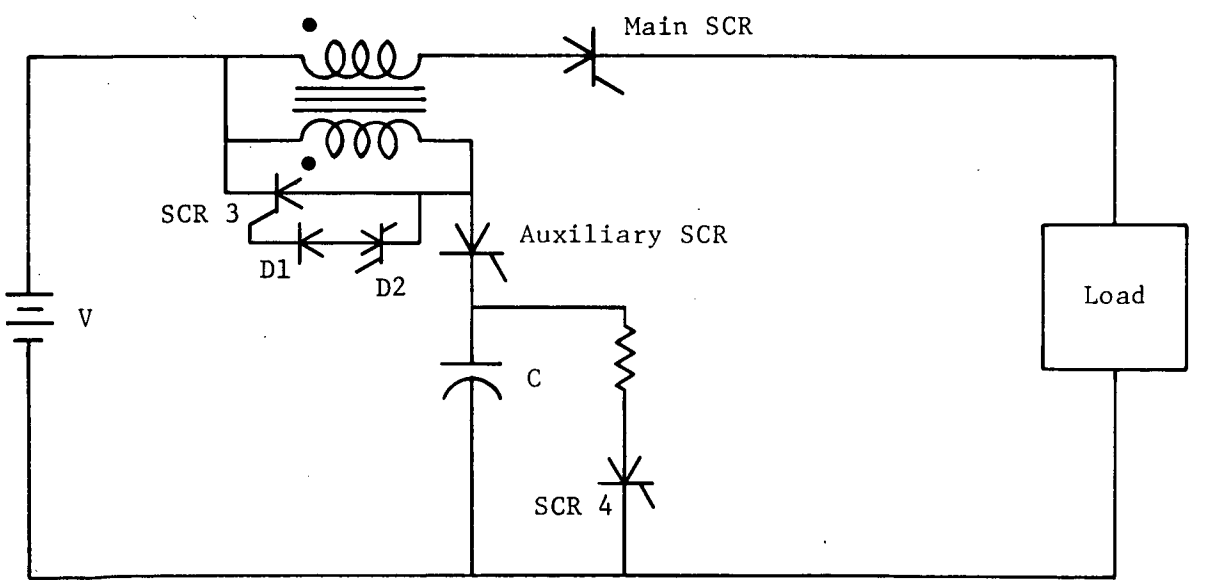


Figure 9.- SCR Commutation Circuit with Auxiliary Circuitry to Control Capacitor Voltages

The Auxiliary SCR is reverse biased by the potential difference between the supply voltage and the voltage across the commutation capacitor; this is essentially the Zener diode voltage. After a period of time sufficient to insure that the Auxiliary SCR has recovered, SCR-4 is gated on in order to discharge the commutation capacitor. This consideration imposes the requirement for additional auxiliary circuitry as the time for the capacitor to discharge will be short in comparison to the time required for current flow to cease within the inductor.

In the further effort to reduce the size and weight of the commutation circuit, it was noted that a precharged capacitor would have considerable effect on commutation and, if charged negatively at the onset of commutation, the reverse voltage available to reverse-bias the main SCR would be the transformed sum of the supply voltage and the initial capacitor voltage. As a result, the length of time that the main SCR is reverse-biased could be increased in comparison to the length of reverse-bias time available with no precharging of the capacitor. Therefore, for a fixed main SCR recovery time, it is possible to use a precharged capacitor which has the advantage of requiring less capacitance. Precharging the capacitor would additionally reduce the required inductance value by permitting a more rapid change in the current. This approach is analyzed below.

The resulting impulse commutation network is shown in figure 10. As in the previous analysis, all circuit parameters are considered to be ideal.

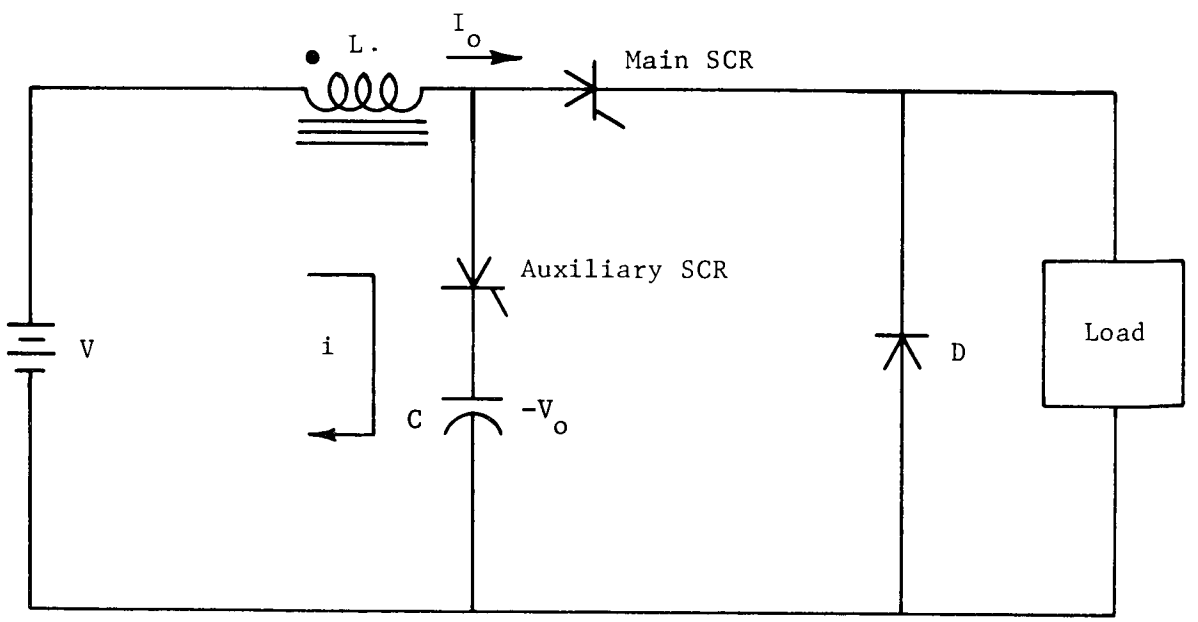


Figure 10.- Impulse Commutated Circuit using a Precharged Capacitor

The initial charge on the capacitor is negative, $-V_o$, as shown. After gating the auxiliary SCR, the current response is

$$I = \frac{V + V_o}{L\left(S^2 + \frac{1}{LC}\right)} + \frac{I_o S}{\left(S^2 + \frac{1}{LC}\right)} \tag{10}$$

where I_o = load current before gating the auxiliary SCR, A

S = complex Laplacian variable.

In real time,

$$I = \left(\frac{V + V_o}{Z_o}\right)\sin \omega t + I_o \cos \omega t, \tag{11}$$

where $\omega = \sqrt{\frac{1}{LC}}$,

$Z_o = \sqrt{L/C}$.

Also $V_c = V - (V + V_o) \cos \omega t + I_o Z_o \sin \omega t$

where V_c = the capacitor voltage.

The potential across the main SCR is V_c because the cathode is clamped to zero during the reverse voltage interval and the SCR is assumed to have recovered its blocking ability during the forward voltage interval. The maximum reverse voltage at the onset of commutation is

$$V_{c(\text{max reversed})} = V + V_o .$$

As the capacitor charges, the main SCR voltage rises to zero. When it reaches zero,

$t = t_q$

$V_c = 0$

or $V = -(V + V_o) \cos \omega t_q + I_o Z_o \sin \omega t_q .$ (12)

Let $$x = \frac{V + V_o}{I_o Z_o},$$

$$\sin \theta = \frac{x}{\sqrt{x^2 + 1}},$$

$$\cos \theta = \frac{1}{\sqrt{x^2 + 1}},$$

$$P = \frac{V}{V + V_o}.$$

Making the above substitutions yields

$$\sin \left(\theta - \omega t_q\right) = P \sin \theta. \tag{13}$$

Solving for t_q

$$t_q = \sqrt{LC} \left[\sin^{-1} \frac{x}{\sqrt{x^2 + 1}} - \sin^{-1} \frac{Px}{\sqrt{x^2 + 1}}\right] \tag{14}$$

in terms of the same parameters:

$$I_{max} = I_o \sqrt{x^2 + 1} \tag{15}$$

$$V_{c(max)} = V + \left(V + V_o\right)\frac{\sqrt{x^2 + 1}}{x} \tag{16}$$

$$V_{c(min)} = V - \left(V + V_o\right)\frac{\sqrt{x^2 + 1}}{x} \tag{17}$$

$$\frac{V_{c(min)}}{V} = 1 - \frac{\sqrt{x^2 + 1}}{Px} \tag{18}$$

If the critical turn-off time is expressed from equation (14) as a function of this criterion, the critical turn-off time is

$$\frac{t_q}{\sqrt{LC}} = \sin^{-1}\left(\frac{x}{\sqrt{1 + x^2}}\right) - \sin^{-1}\left(\frac{V}{V - V_{c(min)}}\right). \tag{19}$$

Because the second term in this equation is a fixed value, the maximum critical turn-off time would be obtained by using a large value of x. However, the maximum value of current imposes the limit of $I_{max}/I_o = 2.0$.

Thus, $x = \sqrt{3}$

and for $V_{c(min)} = 500$,

$$V_o = 395 \text{ V.}$$

Solving for the critical time

$$t_q = (0.685)\sqrt{LC} .$$

For the operating voltages and currents:

$$L = 175 \ \mu H,$$

$$C = 2.74 \ \mu F.$$

The current at time, t_q, is 94.7 A. This is the maximum current value at which the inductance of 175 μH must be specified. $V_{c(max)}$ is not 1,104 V.

Both of the commutation circuits described above had the disadvantage of imposing commutation transients between the high and low sides of the line so these would appear across any other loads that might be connected to the same source. In order to avoid this transient generation effect, another commutation circuit was developed. This new circuit performed the commutation function with respect to a separate commutation bus, which was only referred to power supply common for purposes of initial charge of the commutation capacitor. This circuit was the one finally used, and is described within Section II.

Inductor Design

Considering both system parameters and operational factors of commutation circuits, we find that an inductor is essential both to limit the rate of current rise due to a fault and, also, to store energy during the commutation cycle. The inductor design required special consideration because of the minimum weight requirement. Therefore, a significant effort was put forth to optimize the design. The technical objective was to have a minimum weight inductor with at least 175 μH inductance at a current of 95.0 A, and a dc resistance of less than 0.0333 ohms.

Various types of core materials and core configurations were considered. From a weight consideration only, it has been found that the cut "C" core provides the lowest weight for the given inductance and resistance required. To facilitate the design, the iron losses were considered to contribute negligible resistance effects and the acoustical problems normally encountered with laminated cores at the frequency of this application were not considered relevant.

The technical approach was to select a core, calculate the turns required for the inductance, and then ascertain the amount of copper conductor that could be fit into that core. The losses and weight were then calculated for the complete design. The results of the effort are shown graphically in figure 11 for various cores that would closely fulfill design requirements. Off-designs are also shown to display the trend.

The inductor used for the breadboard circuit is also shown. This inductor was not the minimum weight because the bobbin used for the core was oversized. This did not permit full window-area utilization, and the mean length of the turns was excessive. The core used for the final design was one manufactured by Arnold Engineering.

Current Sensing

It is generally desirable to perform current sensing in a lead at or near ground potential. In the development of a circuit breaker, there is no previous knowledge of whether the breaker will be used in a system that uses return wires, either grounded or floating, or even in a system using a structural return. For this reason, it was considered essential that the current sensing be accomplished in the high-potential lead.

A first approach used a Hall effect device for current sensing. The Hall device has a number of particular advantages. First, it operates by means of magnetic field so it could be electrically isolated from the 270 Vdc power circuit. Second, such devices have fast response times, so they could conceivably be used to sense fast-rise currents. Third, the operational principle is that of transferring a bias current or exciting current, which is proportional to the magnetic field in which it is placed, thereby acting as a multiplier. If two Hall devices were used, and the first had its output suitably amplified so it could be used as the bias-current source for the second, the I^2t fault sensing could be accomplished automatically. Figure 12 depicts this approach.

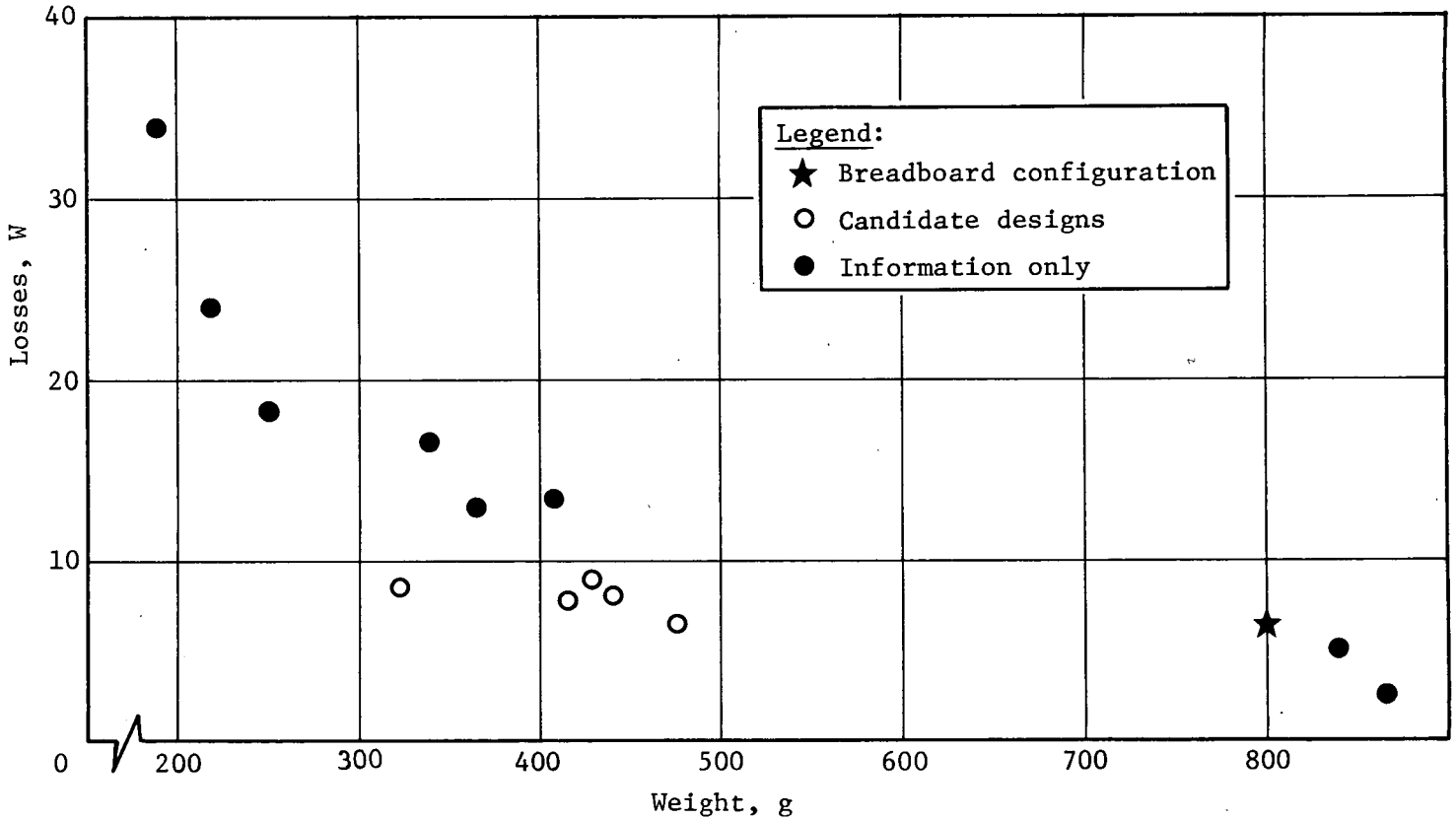


Figure 11.- Direct Current Losses versus Weight for Various Cut "C" Core Designs

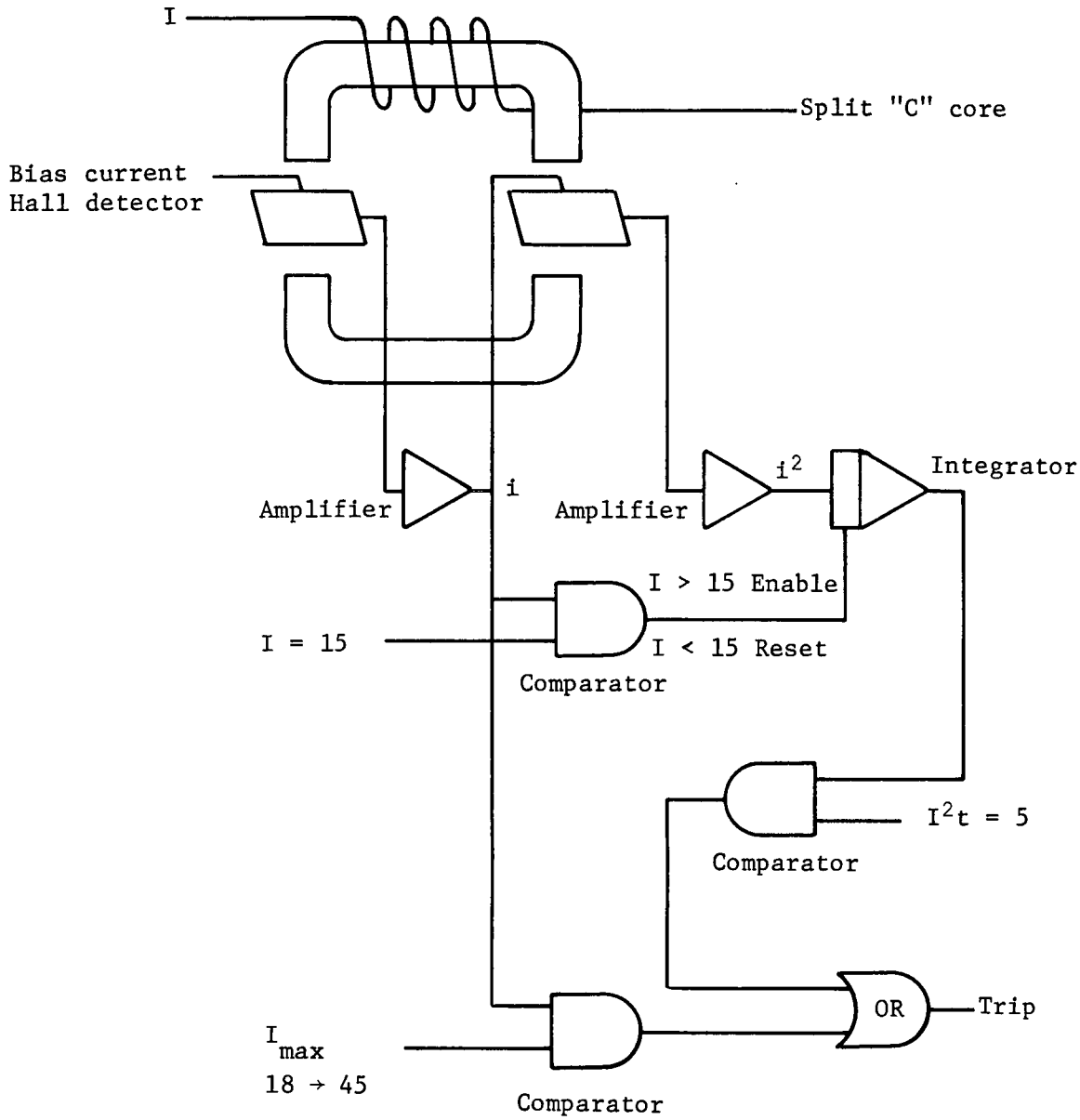


Figure 12.- Hall Effect Detector with Overcurrent Trip Circuits

The first portion of this circuit was built in breadboard form using a commercially available Hall device; the detector was mounted in the air gap of a split "C" core, which also served as the core for the commutation inductor previously discussed. The requirement for operation over the temperature range from -55 to +100°C demanded that the bias current be compensated since both the gain of the device and the residual offset voltage vary as a function of temperature. The breadboard then incorporated a current control and a temperature sensing feedback circuit to control the current. This circuit, shown in figure 13, was built and tested over the temperature range and proved to be an adequate current detector.

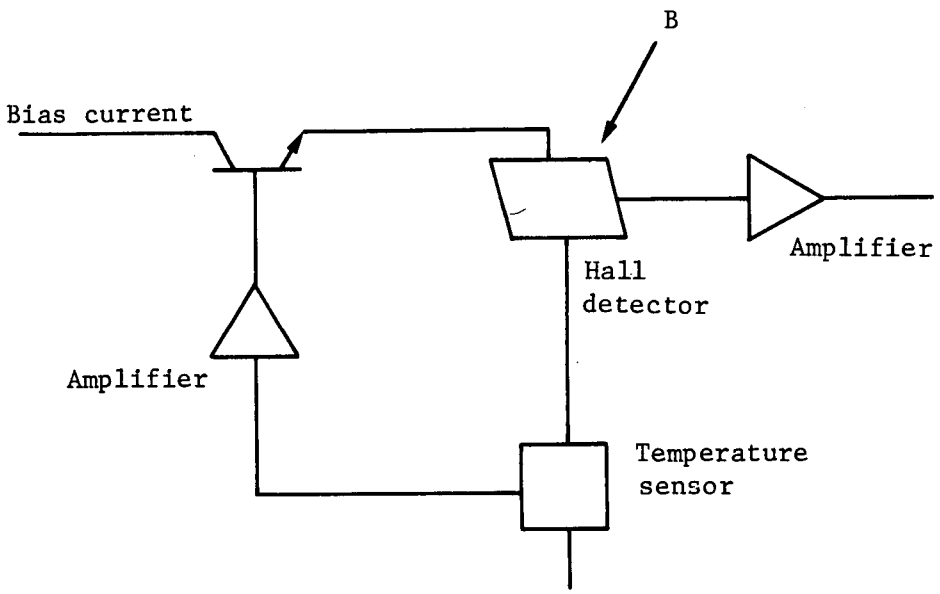


Figure 13.- Temperature-Compensated Hall Detector

Tests were then made on a second Hall detector, which directed the approach toward the current squaring technique. At this time it was found that in standard production of Hall devices, the units varied considerably in gain, offset voltage, and temperature coefficient. Consultation with the manufacturer indicated that the cost of procuring detectors to more rigorous specifications was prohibitive. On the other hand, the cost in both time and parts for calibrating each detector and then custom building compensation networks and amplifying circuits for each detector was also prohibitive. The plan to use a Hall effect current sensor was, therefore, dropped.

Conventional shunts have been used to measure current for years. However, when a shunt is to be used to measure a fast-rising current, consideration must be given to the inductance associated with the shunt or the current-sense indication will be in considerable error. The voltage across a shunt is effectively represented by

$$V_s = I\left(R + X_L\right) .$$

Because the reactance term is frequency-dependent, particular care must be given to finding a shunt with low inductance. A shunt has the disadvantage of providing resistive losses. Since, as previously outlined, the current-sensing had to be accomplished in the high voltage lead, the shunt offered a further disadvantage. Connecting the shunt directly in series with the high voltage lead necessitated operating all associated circuitry at a nominal 270 V above ground potential. If the shunt were to be operated ahead of the main SCR, it would have to measure all currents and transients caused by commutation. If the shunt were to be operated on the load side of the main SCR, it would be at the 270-V potential when the breaker is closed and would essentially drop in potential to that of the return lead when the circuit breaker was open.

A shunt was found that provided characteristics considered suitable for use with the breaker. The shunt, maunfactured by T and M Research of Albuquerque, New Mexico, had been developed by the manufacturer for the AEC. The coaxial shunt construction minimized inductance. The tubular resistance element is of a manganin-type alloy to minimize temperature changes; a change of 0.3% is experienced over the entire military temperature range (-50 to 100°C). This shunt, procured at a nominal resistance of 5 mΩ with an inductance of approximately 2.65×10^{-6} μH, is used in the final design of the solid-state breaker described in Section II.

The change from the Hall device to a current-sensing shunt necessitated design of new circuitry to achieve squaring of the current sense voltage in order to achieve the I^2t function. Monolithic and hybrid transconductance multipliers were considered. These are relatively expensive and do not possess particularly stable temperature characteristics. The requirement for fast response to a current transient also appeared to be a limitation. Other squaring circuits that were considered used the following types of multipliers--diode logarithmic, photocell, pulse height/pulse width, magnetostrictive, and piecewise linear multipliers. Simultaneous with the evaluation of

squaring methods, consideration was directed toward the true meaning of the specification for the I^2t function. I is defined as the current through the breaker and t as the time after nominal current is exceeded. This specification stated that the breaker should not open before the I^2t value = 5 A^2-s, the breaker should be fully open before an I^2t value of 30 A^2-s is reached. It was obvious that the I^2 value could not be integrated indefinitely, but that this value must be integrated only for that time interval when I exceeded 15 A or some slightly greater value. This condition has been indicated in figure 12, in conjunction with the Hall device. Further consideration indicated that the I^2t (in reality the integral of I^2 dt) was directly related to the I^2R dissipation in conductors over the integration time interval. R represents the resistive loss in the conductor. For operation with a 15-A breaker, it must be assumed that the wiring is designed to adequately dissipate $(15\ A)^2$ R Watts, continuously. The circuit must, therefore, be able to dissipate this amount of heat as a minimum, during any period of overload where excess thermal energy is being accumulated.

This approach toward current sensing involved the expression $\int (I^2 - 15^2)\ dt$. This integral provides for the exptected normal cooling and also permits the electronic integrator to discharge back to zero following an overload without imposing the requirement for additional reset circuitry. The actual circuit used prevents negative integration when the actual load current is less than 15 A.

It was apparent that the above integral expression, which provided for heat dissipation, could not arbitrarily be equated directly to the 5 and 30 A^2-s limits as the critical times of 10 and 92.6 ms required in the specification could not be satisfied. Nor could this integral expression be arbitrarily solved for the critical times and equated to new I^2t limits without moving out of the required response range. As an example, curves showing the response of $(I^2 - 15^2)t$ = 2.75 and 9.16 A^2-s are shown in figure 14. The area bounded by the heavy solid lines defines the limits of response defined by the contractual requirements.

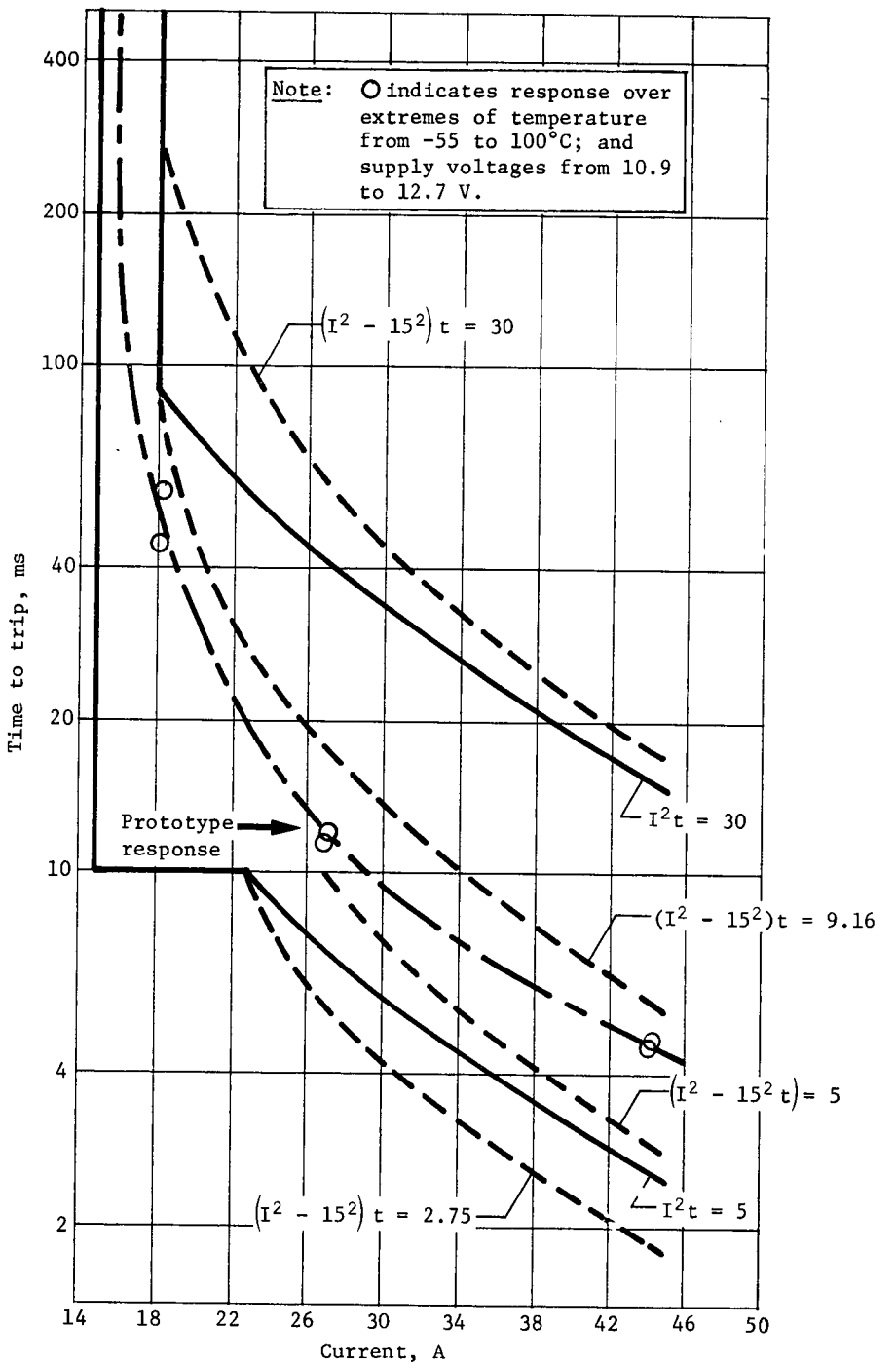


Figure 14.- I^2t Limits and Prototype Response

The final sensing and integration was evolved by relating the desired thermal protection to the intent of the contract specification. Additional factors relating the overall component weight and total circuit complexity were considered strongly. Thus, the final circuit for current sensing used a linear offset integrator that provided an approximation of the squaring function. This provided a response well within the limits of any of the curves of figure 14. As a verification, the response of the later prototype circuit breaker is also indicated in figure 14. This final circuit as used in the breaker is described in greater detail in Section II.

Logic Circuitry

The originally conceived logic requirements for the circuit breaker were minimal in supporting the requirement of counting from zero to nine recycles and inhibiting turn on of the circuit breaker if the recycle count were exceeded. Likewise, the provision of a variable time interval between trip and reclosure of the circuit breaker was conceived to be a simple requirement. The possible necessity of inhibiting turn on until completion of commutation capacitor precharge was anticipated.

When the complete breaker operation was evaluated, it was found that the logic functions were much more complex and involved. Logic provisions had to be included to--

1) Provide the singal to turn on the main SCR subsequent to an ON command. This had to be delayed until functions (2) and (3) had been completed.

2) Sense that the power supply was operating, that it had attained full operating voltage, and that it had remained at full operating voltage long enough to precharge the commutation capacitor.

3) Send a reset signal to all logic to insure initial state of the logic.

4) Provide a programmable recycle count from zero to nine recycles.

5) Provide a cycle timer programmable from 1 to 100 ms.

6) Provide a recycle count reset for logic clearance in the event a transient overload occurred and cleared.

7) Provide a time delay prior to counter reset. (2 minutes were estimated as being a suitable time interval for ensuring circuit cooling following an overload.)

8) Receive a manual open command and, subsequently, initiate the functions outlined in (9) and (10) following.

9) Initiate the commutation cycle following an open command.

10) Turn off the power supply following either an open command or the programmed number of reclosure attempts, resulting in an automatic lock-open of the circuit breaker.

11) Send a signal to the power supply to turn on a continuous gate to the main SCR following the close command, and to similarly turn off this continuous gate on initiation of a commutation cycle by either an overload or open command.

Capacitor Precharge and Recharge

It has been previously noted that the commutation capacitor must be fully precharged before turning on the main SCR and, thus, closing the circuit breaker into a load. The possibility exists that the main SCR might close into a short-circuit or other load fault condition; as a consequence, all necessary conditions for assuring commutation must exist before the main SCR is gated on. Since the commutation capacitor must be precharged using negative voltage, the logical solution is to provide an isolated output from the internal power supply of the circuit breaker for this purpose.

Charging circuitry for the commutation capacitor must be capable of withstanding the high voltage occurring between the commutation capacitor and the charging source during the commutation cycle. Various LC filter approaches were investigated for allowing precharge and at the same time keeping high voltage commutation transients out of the breaker power supply. All such approaches were found to be impractical. The most satisfactory approach to this problem is shown in figure 15 and is the one used in the final breaker design. This incorporates the following considerations.

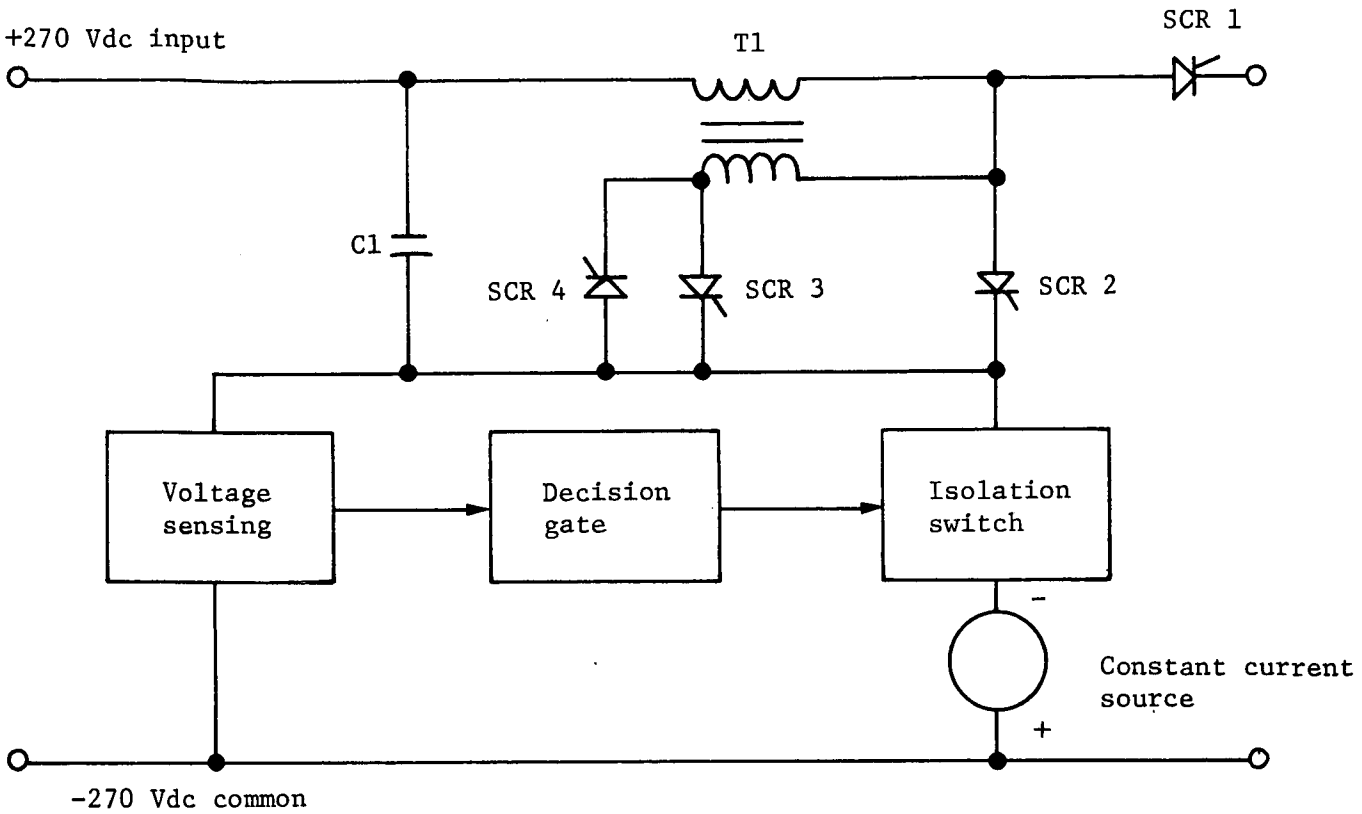


Figure 15.- Recharge Isolation Circuit Functional Diagram

1) Sensing of commutation capacitor voltage is accomplished by sensing the voltage appearing on the COMMUTATION BUS (the common connection of one terminal of the commutation capacitor to SCR2 cathode, SCR3 cathode, and SCR4 anode), essentially with respect to 270 Vdc COMMON.

2) The negative charging output of the breaker power supply is used with additional circuitry as a constant-current source for precharging the commutation capacitor. A switch used in the negative output of this constant current source is effectively opened during the commutation cycle, isolating the charging source from the commutation bus during the high voltage portion of the commutation cycle.

3) The isolation switch is driven by the voltage sensing network through a gate that closes the isolation switch during the precharge interval, opens the isolation shortly after the onset of a commutation cycle, and recloses the isolation switch after commutation is accomplished and toward the end of the commutation cycle.

A Delco DTS-804 transistor was selected to serve as both current source and isolation switch. Driving circuitry for the DTS-804 serves to sense voltage as described above, and provides appropriate base bias for the DTS-804. The operation of this circuit is described in greater detail within Section II.

Precharging of the commutation capacitor is one of three considerations that must be directed toward capacitor charging. After this capacitor has been charged, circuit leakage principally through SCR2, SCR3, and SCR4 provides a discharge path. The precharge circuit described in figure 15 was also used to provide sustained charging compensation for leakage losses during intervals of no commutation. The precharge circuit (now the *recharge* circuit) accomplished the provisions for the above two considerations simultaneously. The third consideration posed a problem somewhat different in nature.

Additional energy losses are sustained within the commutation circuit during the commutation cycle. Although these losses can be controlled to the extent that commutation for one cycle will not be jeopardized, consideration of a sustained number of rapidly recurring commutation recycles revealed that these losses could become rather excessive, to the point that commutation circuit energy decay would inhibit further commutation capability.

This consideration imposes the problem of rapid recharge of the commutation capacitor following each commutation cycle. This limited time-interval recovery places a considerable power demand upon the recharge power supply in order to sustain peak power requirements during recharge. Rather than build a circuit breaker power supply possessing this power capability, an alternate approach was attempted. This approach, shown schematically in figure 16, imposes no requirement for power upon the breaker power supply.

The description of the circuit shown in figure 16 follows. When SCR2 is gated on, initiating commutation, diode D_2 is reverse-biased until the SCR2 cathode voltage reaches zero with respect to 270 Vdc COMMON. In the interval between achievement of zero voltage on SCR2 cathode and the gating of SCR3, capacitor C2 charges through diode D2, causing extra current to be drawn through the commutation transformer primary. SCR3 is gated on at the time the commutation capacitor voltage is zero (commutation bus voltage with respect to 270 Vdc COMMON is at source voltage) and the commutation transformer (primary) current is at maximum. Leakage inductance in the commutation transformer causes SCR2 to become reverse-biased for a brief period of time, after which SCR2 remains OFF, for the remainder of the commutation cycle. As a result, diode D_1 isolates capacitor C_2 from the commutation circuit.

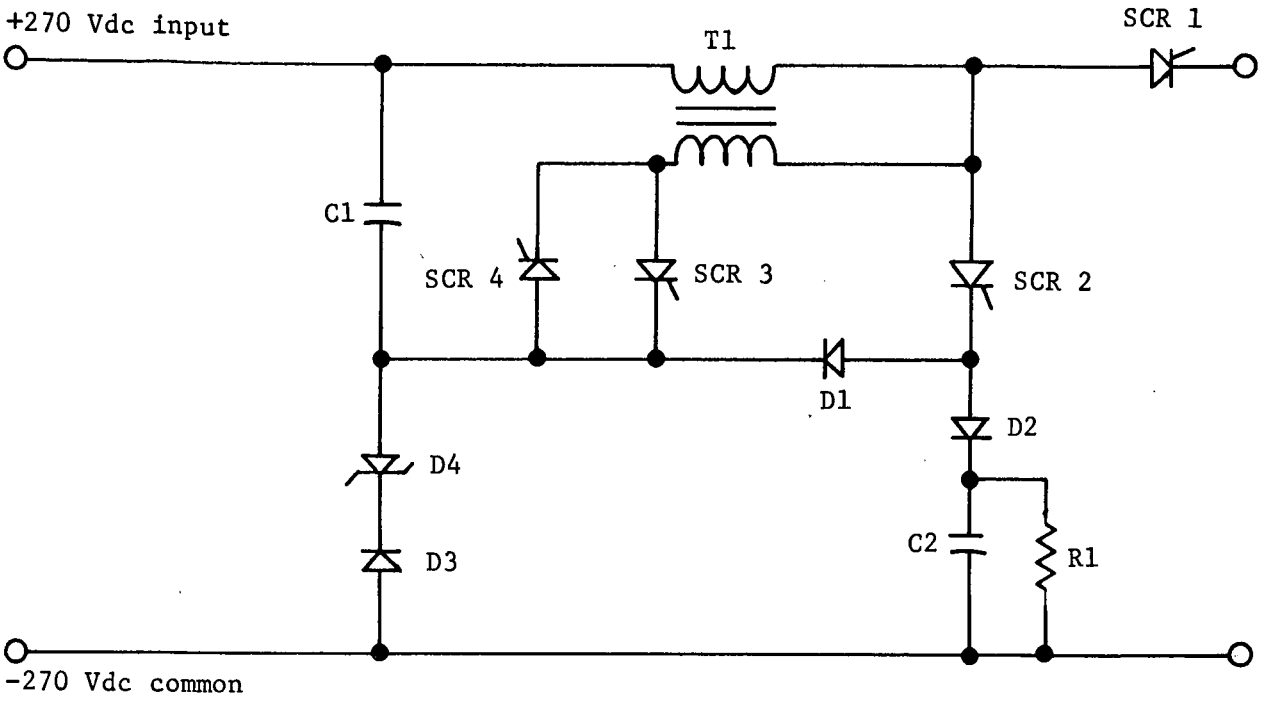


Figure 16.- Commutation Circuit with Auxiliary Capacitor Quick Charge Approach

The extra current in the commutation transformer, caused by C_1 charging, has stored sufficient additional energy in the inductor to offset circuit losses. The inductor current charges the commutation capacitor through SCR3 to a maximum voltage. At this point, SCR4 is gated on and the oscillation continues until the capacitor voltage reaches a peak voltage of the opposite polarity. (Zener surge suppressor D_4 is included to insure that multiple commutations do not result in raising the peak voltage on the commutation capacitor above the voltage rating.) C_2 then discharges through R_1 in time for the next commutation cycle.

This circuit was tested, with performance similar to that expected. There were found to be several disadvantages to this type circuit:

1) The length of time during which SCR2 is reverse-biased is dependent on the size of C_2. If this capacitor is made large enough to compensate for worst-case circuit losses at -50°C, the reverse-bias time available for SCR2 is very close to worst-case minimum. Hence, SCR2 may not reliably turn off. Attempting to increase this reverse bias time through increase of leakage inductance in the commutation transformer increases circuit losses and imposes a requirement for a large value for capacitor C_2. The net result is that the reverse-bias time available for SCR2 is not appreciable affected.

2) Because operation of this circuit depends upon leakage inductance as a parameter, and because source impedance characteristics cannot be generally defined, it was impossible to predict the effect of unknown source impedance upon the operation of the commutation circuit.

3) Energy losses cannot be entirely compensated because the compensation circuitry itself added energy losses to the commutation circuit, in the process of increasing the inductor current during commutation.

Considering the above disadvantages led to the decision to terminate further effort involving this quick-recharge scheme. Attention was again directed toward deriving the necessary recharge energy directly from the source through the power supply of the circuit breaker.

The next approach was to design a high-current version of the previously discussed precharge circuit. However, the required charging speed and resultant charging currents involved indicated that six of the DTS804 transistors would have to be operated in parallel. Circuit complexities for stable operation, together with the increase in power dissipation which could create problems when the circuit breaker would be operated at elevated temperatures indicated this approach to be impractical. In any event, the circuit breaker power supply would have to possess much greater power capability, necessitating either a redesign of the circuit breaker power supply or the incorporation of an auxiliary power supply for driving the fast recharge circuitry.

The third approach to the fast recharge circuit appeared to be the most practical, and is shown in figure 17. It will be noted from this functional diagram that the voltage sensing and decision circuitry close S_1, S_2, and S_3 in sequence at different voltages in order to approximate a constant current source of 1.5 A, operating similarly to the precharge circuit described previously. The DTS-804 transistors are used as switches, rather than as current sources, reducing the amount of thermal dissipation. This allows the use of three DTS-804 transistors instead of the previous six.

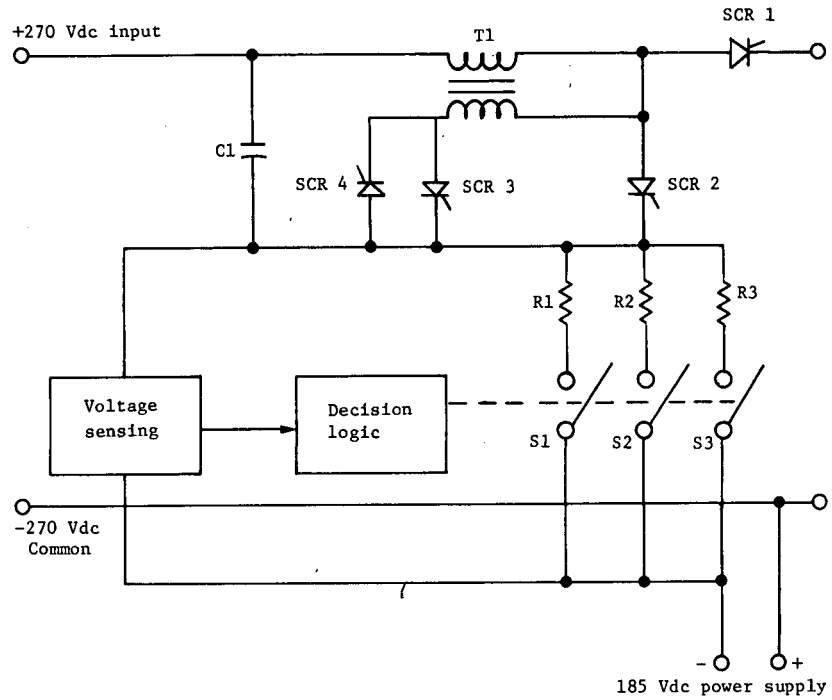
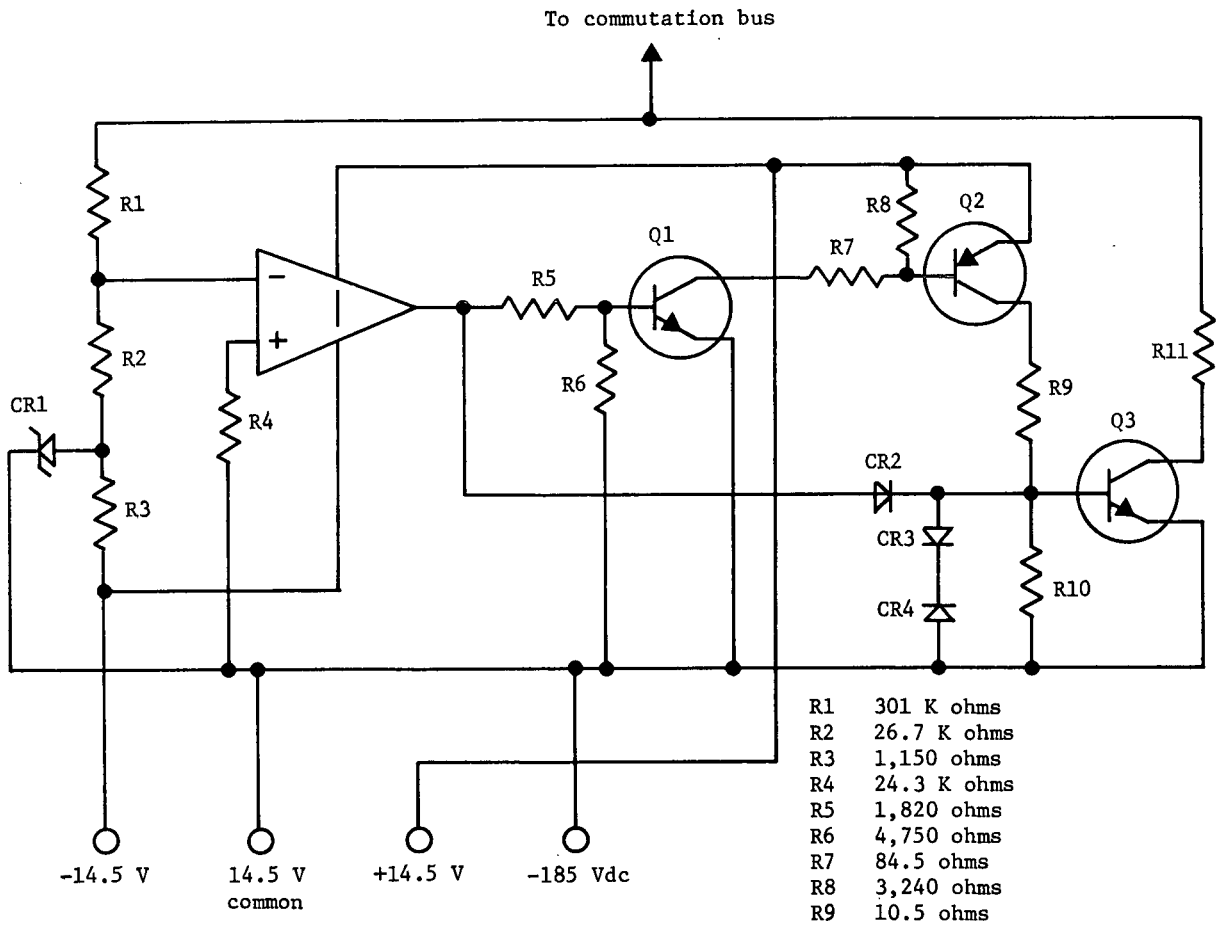


Figure 17.- Functional Diagram, Quick Recharge Circuit

Three steps are required to allow recovery of worst-case losses with peak currents in the safe operating region of the transistors. Switch S_1 closes when the commutation capacitor is within 150 V of full charge. S_2 closes at 75 V, and S_3 closes when the commutation capacitor is similarly within 21 V of full charge. R_1 is 100 ohms, R_2 is 88.7 ohms, while R_3 is 20 ohms. A schematic diagram of S_2 with voltage sensing and decision circuitry is shown in figure 18.

With the exception of resistance values, S_1 and S_3 are identical to S_2. This circuit requires a power supply capable of delivering 1.5 A at 185 Vdc, and bias supplies capable of delivering +14.5 V ± 41% at zero to 0.78 A and -14.5 V ± 41% at zero to 150 mA. This approach requires the redesign of the breaker power supply, or the incorporation of an auxiliary power supply to provide operating power for this circuit.

Only one section of this circuit was breadboarded and tested to confirm its operation. Although this circuit offered the complete solution to the commutation capacitor recharge problem, it was decided not to incorporate it in the final design as the construction schedule did not permit the power supply, heat sink, and case redesign that was required. The circuit provided was adequate to demonstrate feasibility although with some reclosure rate limitation.



Note: +185 Vdc return connected to 270 Vdc Common.

R1	301 K ohms
R2	26.7 K ohms
R3	1,150 ohms
R4	24.3 K ohms
R5	1,820 ohms
R6	4,750 ohms
R7	84.5 ohms
R8	3,240 ohms
R9	10.5 ohms
R10	2,100 ohms
R11	88.7 ohms (Dale RH-50)
CR1	1N823A
CR2	1N4148
CR3	3.3 V Zener
CR4	1N4148
A1	μA741
Q1	2N2222A
Q2	PNP
Q3	DTS-804

Figure 18.- Electrical Schematic for Switch

SECTION II

DESIGN PHASE

During this phase of the effort, the final design of the breaker configuration was accomplished. The important design details used in fabricating the breakers that were tested and delivered are outlined.

The following drawings are referenced during the course of this discussion and are included in Appendix A.

Figure No.	Title
42	Assembly - Solid State Circuit Breaker
43	SSCB System Block Diagram
44	SSCB System Functional Diagram
45	SSCB System Wiring Diagram
46	SSCB Analog and Logic Schematic Diagram
47	SSCB Gate & Recharge Isolation Schematic Diagram
48	SSCB Power Supply Schematic Diagram

General Description

The logic-controlled solid-state circuit breaker (SSCB) is mechanically composed of a main frame assembly, and the three etched-circuit board assemblies that follow--

1) Power Supply Circuit Board,

2) Gate and Recharge Isolation Circuit Board,

3) Analog and logic Circuit Board.

The Main Frame Assembly contains the discrete elements of the commutation circuit, including commutation capacitor C1, commutation transformer T1, main SCR1, and auxiliary commutation SCRs--SCR2, SCR3, and SCR4. The power supply circuit board, Part No. 042, contains the power supply elements necessary to provide operating bias for the transistors and integrated circuits used in the SSCB, and also contains circuitry to provide power for commutation capacitor C1 recharge circuitry. This circuit board is nearest the main frame assembly.

The gate and recharge isolation circuit board, Part No. 043, is mounted above power supply circuit board on four spacers. The analog and logic circuit board, Part No. 035, is, in turn, mounted on spacers; and is located above the gate and recharge isolation board. Shielding, in the form of a full-size circuit board shield, is located between the analog and logic board and the gate and recharge isolation circuit board. Figures 19, 20, and 21 are photographs of the solid-state circuit breaker. A detailed theory of operation for each of the above elements of the SSCB follows in the above outlined order, with an overall description of the functional operation of the entire SSCB subsequently provided.

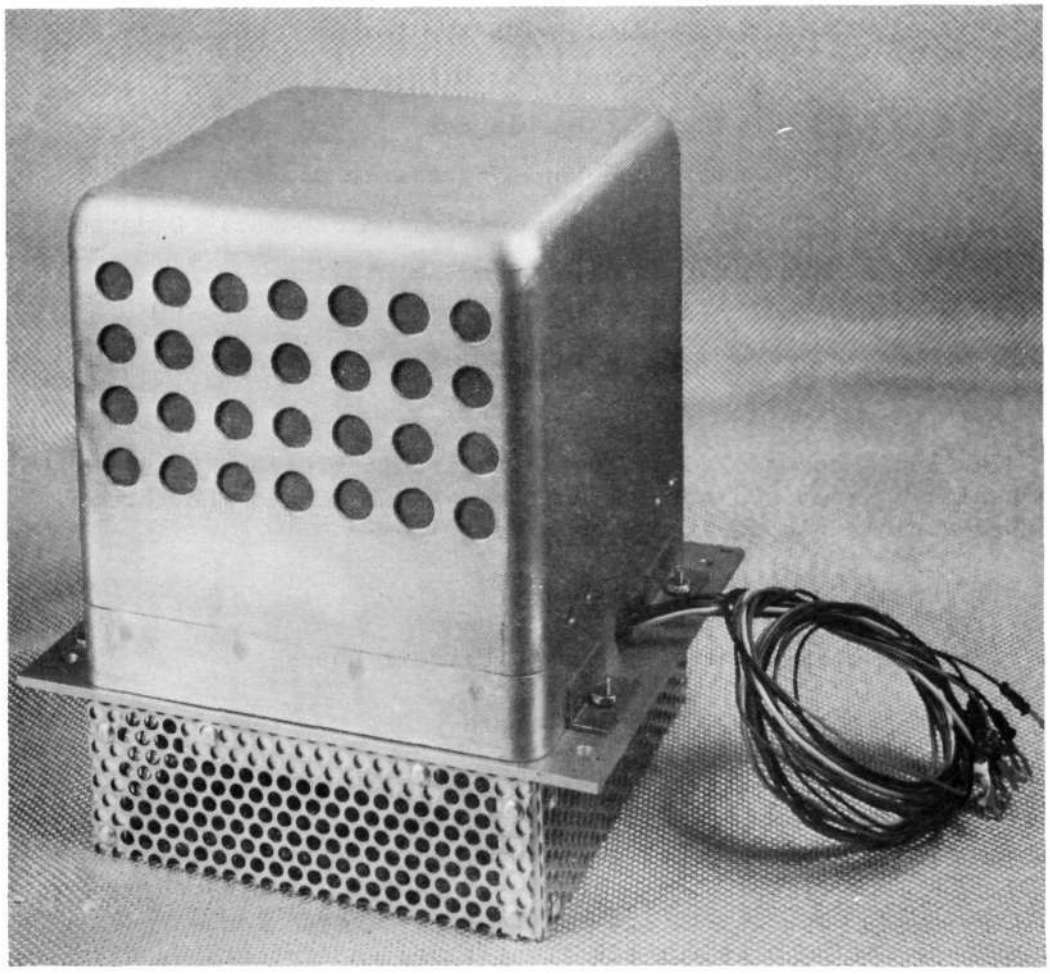


Figure 19.- Logic Controlled Solid-State Circuit Breaker

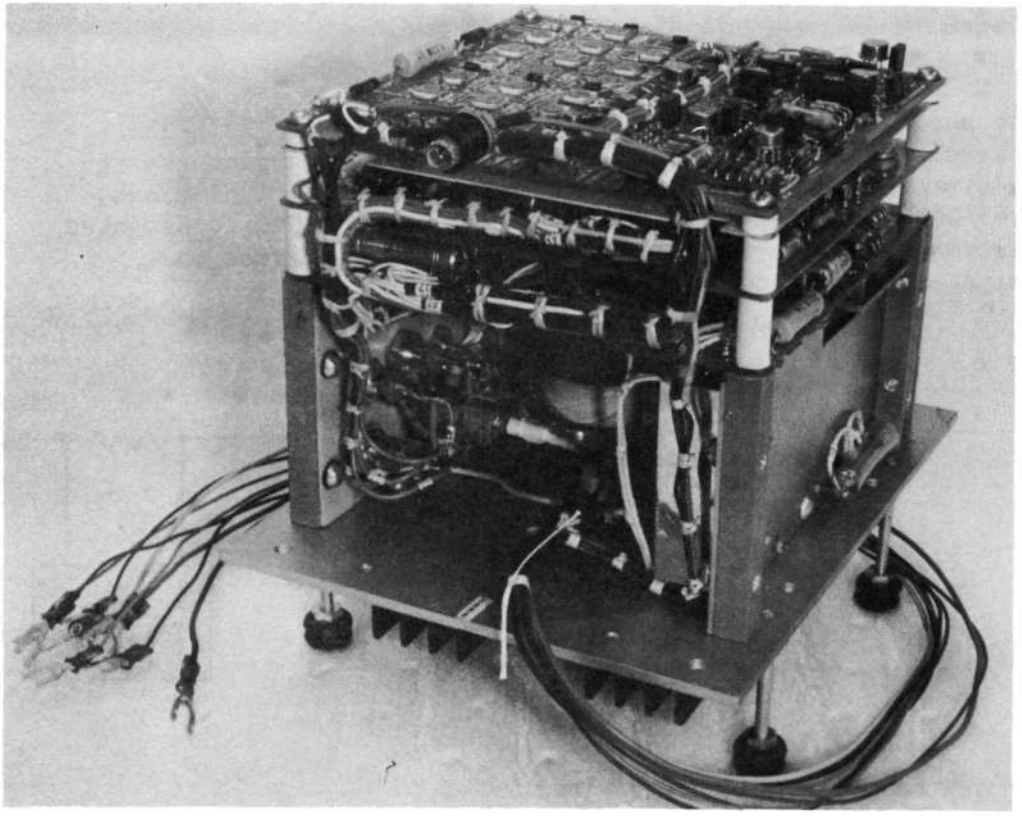


Figure 20.- Solid-State Circuit Breaker, Covers Removed

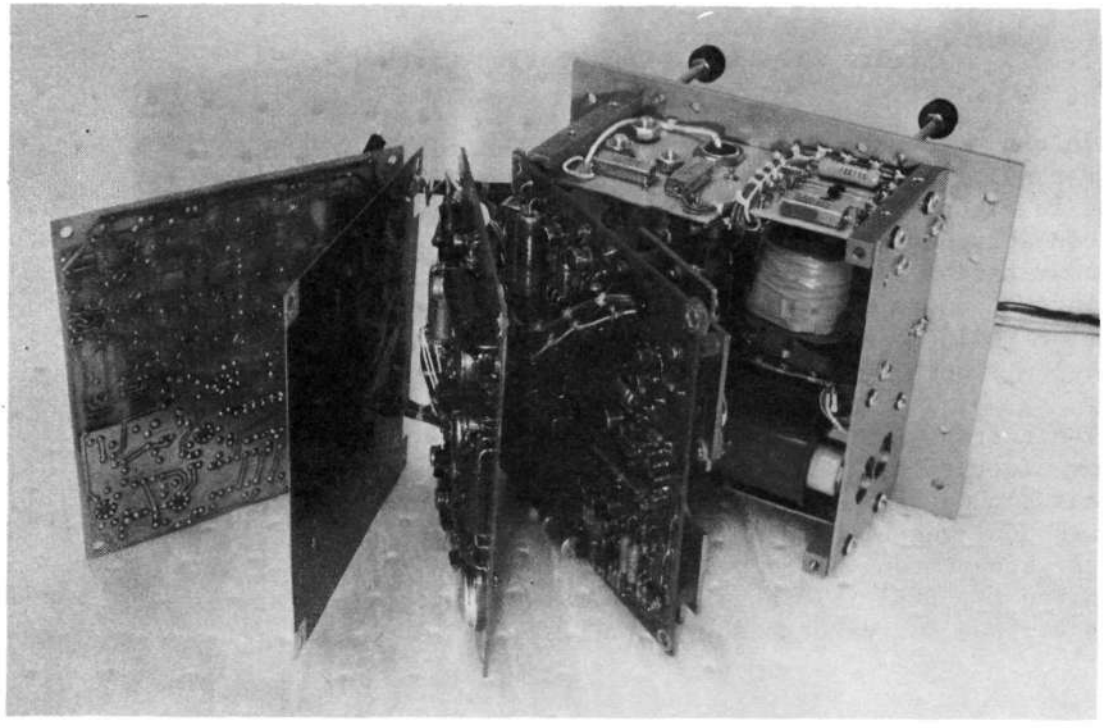


Figure 21.- Solid-State Circuit Breaker, Open Assembly

The basic commutation circuit is shown in figure 22. This same circuit can also be seen in relation to the complete system in the system block diagram and the system functional diagrams, (fig. 43 and 44 in App A), respectively. Assume SCR1 to be gated on, carrying load current, with capacitor C1 precharged to approximately 450 volts in the polarity indicated.

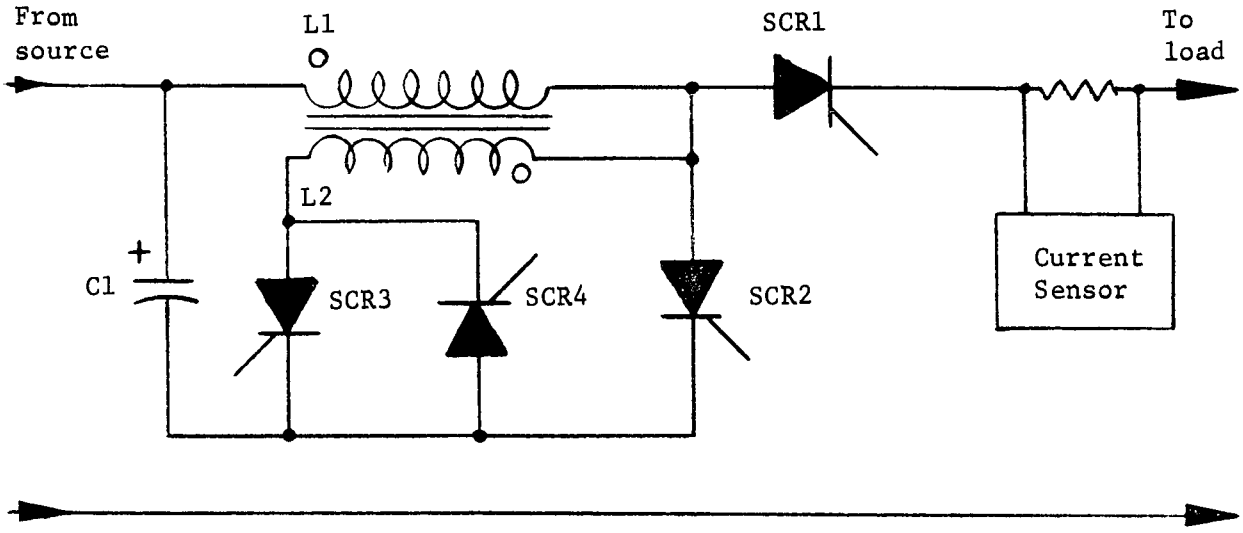


Figure 22.- Basic Commutating Circuit

In the event the SSCB receives a MANUAL OPEN COMMAND or a fault condition is sensed, SCR2 is gated on at time, t_0, as shown in figure 23. This gating of SCR2 causes SCR2 to conduct, subsequently dumping the charge on commutation capacitor C1 across the commutation transformer, T1, primary winding (L1). As a result, the anode of SCR1 is driven rapidly negative, thus terminating SCR1 conduction. This breaks the SSCB load current, effectively opening the SSCB.

The current flowing through L1 immediately prior to time, t_0, is now diverted by SCR2 conduction, as is shown in the capacitor, C1, current waveform of figure 23. As capacitor C1 discharges through SCR2 and L1, the negative anode voltage applied to SCR1 decays going through zero voltage at time t_1. In the period following t_1, SCR1 is biased in the forward blocking state as SCR1 anode voltage increases positively.

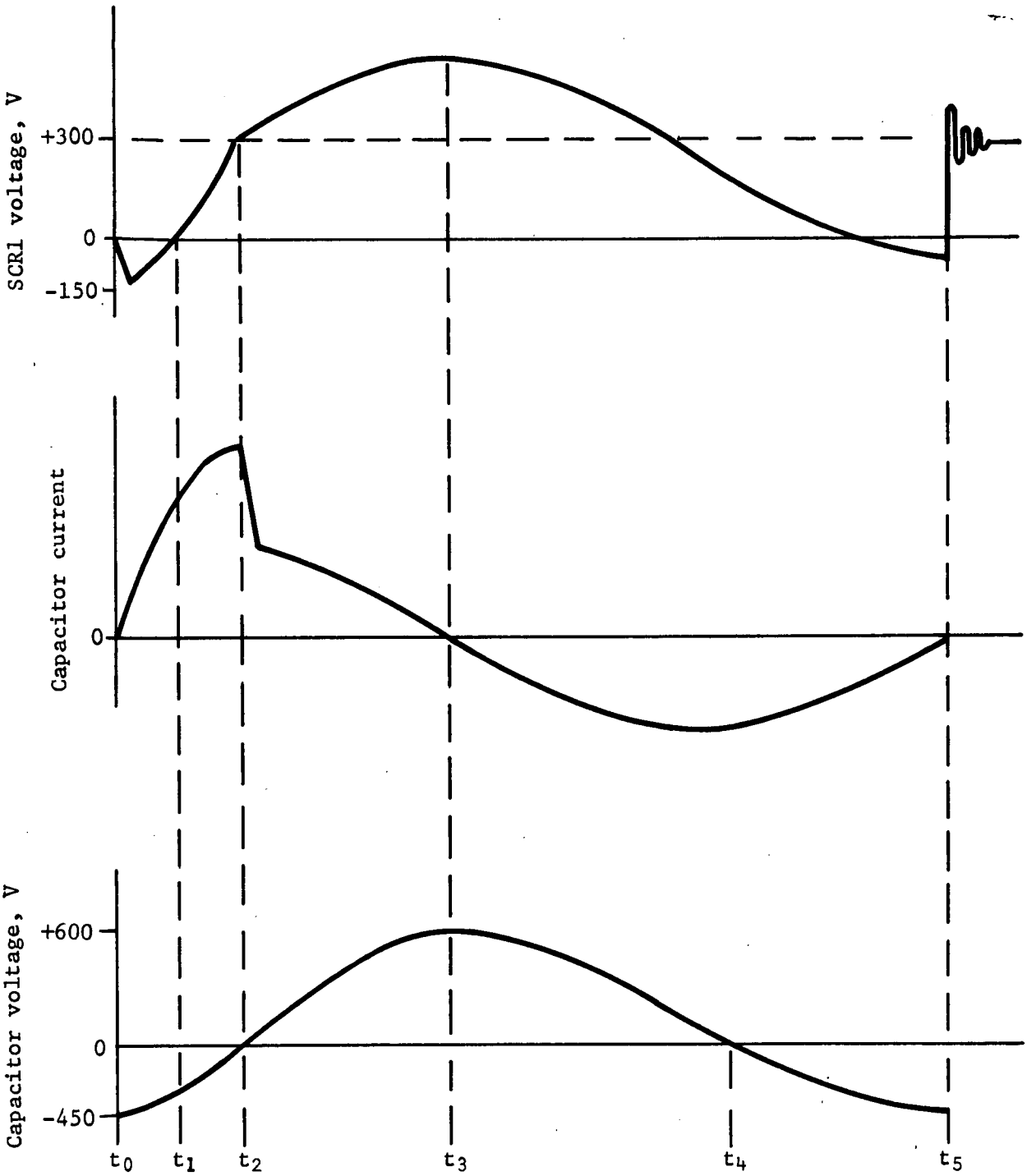


Figure 23.- Principal Waveforms of Commutating Circuit

At time t_1 the commutation capacitor C1 voltage has been decreasing from maximum negative value (at time t_o) and continues to decrease until C1 voltage goes through zero at time t_2. Inductor current in L1 is now at maximum value. SCR3 is gated on at this point, enabling current flow through commutation transformer winding, L2. L1 and L2 have essentially the same number of turns, so that, with the same magnetic field, the current rapidly drops to approximately one-half the peak value of current. The period of oscillation for the commutation circuit (C1, L1, L2) is now approximately doubled, beginning with time t_2. C1 voltage, rising in the positive-going direction, now appears across L1 and L2 in series. Half of this voltage appears across SCR2 as reverse bias, turning SCR2 off. This voltage is approximately equal to the voltage across SCR1. Note that this SCR1 voltage is approximately half the value it would have reached if SCR3 did not conduct. This conduction of SCR3 thus permits lower voltage ratings for SCR1.

As oscillation continues, the commutation current (capacitor C1 current) goes through zero and SCR4 is gated on at time, t_3, capacitor C1 is charged to a voltage that represents the energy of the initial C1 charge, plus the energy stored in the commutation inductor L1 at time, t_0, neglecting circuit losses.

At time t_4, the capacitor C1 voltage is again going through zero in the negative direction, the voltage across SCR1 is back down below source voltage, and SCR4 is carrying maximum current. By time t_5, capacitor C1 is nearly recharged (neglecting circuit losses), SCR4 is turned off, and SCR1 anode voltage returns to source voltage.

Circuit loss compensation during commutation is accomplished by recharging capacitor C1 during the latter portion of the commutation cycle, beginning this recharge following time t_4 and continuing recharge until C1 is fully recharged. The entire commutation cycle requires less than 0.5 ms, neglecting some additional recharge time required, and occures with minimum reference to the return circuit of the power source (with exception of recharge), in order to create minimum transient disturbances.

Gate circuitry, for operating SCR1, SCR2, and SCR3, together with commutation capacitor C1 recharge circuitry is located on the gate and recharge isolation circuit board. The SCR4 gate circuit components are located on an epoxy-glass panel structure within the main frame assembly. This panel structure also provides mounting and connection facilities for the auxiliary commutation SCRs, as well as for the current sensing shunt, R.

Power Supply Assembly

The power supply for the SSCB provides the following outputs.

1) Regulated outputs of +12 Vdc and -12Vdc for operating all analog and logic circuitry;

2) 200 Vdc unregulated output for operation of commutation capacitor C1 recharge circuits;

3) SCR1 continuous gate output voltage, for providing continuous gate drive to SCR1, enabling SCR1 to remain in the conduction state, even with application or interruption of small-value load currents.

Refer to figure 48 in Appendix A.

It should be noted that all power supply designators are in the 101 through 199 series although the schematic shows only the significant digits under 100. When 270 Vdc input is applied to the SSCB, the power supply starting circuits, consisting of transistors Q101 through Q105 and Q115, are energized from approximately 6 V bias derived from Zener diode CR101 and associated circuitry. The power supply switching transistors Q106 and Q107 are simultaneously supplied with 270 Vdc.

Application of MANUAL CLOSE COMMAND to terminals E102 and E103 causes switching of the single-shot multivibrator (Q101 and Q102) which, in turn, through Q103, drives Q115 to the on state, enabling the power supply starting circuit composed of transistors Q104 and Q105. The resultant switching of transistors Q104 and Q105 is coupled to the main switching circuit (Q106 and Q107) of the power supply through timing transformer T102, maintaining drive for this main switching circuit during the startup interval until adequate feedback drive is attained for transistors Q106 and Q107 to continue switching.

The outputs of transformer T103 are fed to rectifier circuits which derive each of the dc outputs. Approximately 18-V unregulated dc is fed to each of the 12-V regulators (Q108-Q109 and Q110-Q111) for providing +12 Vdc and -12 Vdc outputs, respectively.

Continuous gate output is derived from rectifiers CR19 and CR20, and is controlled by external logic input (SCR1 continuous gate command) fed to terminal E112. This external logic input, in high state, enables continuous gate output from the SSCB power supply. Transistors Q112 and Q114, controlled by external logic input, provide enabling/disabling switching for the continuous gate output.

The recharge voltage (approximately 200 Vdc) for the recharge isolation circuit, derived from bridge rectifiers CR21 through CR24, is fed directly to the power supply output terminals, E106 and E107.

The SSCB power supply is disabled by an external logic signal fed to terminal E113 (POWER SUPPLY OFF COMMAND). Transistor Q113, driven by Q116, provides saturation current to the control winding of transformer T102. When the logic input is in the high state, transformer T102 core is saturated, disabling the switching of transistors Q106 and Q107, until the SSCB power supply output voltages decay and no further switching can occur.

SCR Gate and Recharge Isolation Circuits

Reference is made to figure 47 in Appendix A. As mentioned previously, all gate circuit designators are in the 200 series although only the significant digits are shown on the schematic.

The operation of the SCR1 and SCR2 gate circuits is nearly identical, with the exception of the respective comparator inputs, A201 and A202. SCR1 GATE ENABLE signal, derived from the logic, is fed to terminal E202. (This is the same logic signal that controls the SCR1 continuous gate output from the SSCB power supply.) This gate enable logic signal, fed to the inverting input of comparator A201, enables the firing of SCR1 gate when switched from low to high state. The resultant output of comparator A201 switches to the low state, producing base drive to transistor Q201. The firing pulse generated in the Q201 collector circuit is coupled to SCR1 gate through transformer T203.

Three separate input signals are fed to comparator A202 through terminals E205, E206, and E217 (I_L trip input, I^2 trip input, and OPEN COMMAND, respectively). The two TRIP INPUT commands are logic signals derived directly from the analog fault current sensing circuitry. The OPEN COMMAND INPUT signal is derived directly from the logic portion of the analog and logic circuitry. The switching of either of these three inputs to high state causes the output of the A202 comparator to switch to low state, producing a gate firing pulse for SCR2 in the same manner as outlined above for generation of the SCR1 firing pulse. The gate firing pulse coupled to SCR2 causes SCR2 conduction, which initiates the SSCB commutation cycle.

Magnetic core reset for transformers T201 and T202, which are square law responses, is accomplished by deriving a small reset current from the 270 Vdc input through resistor R214, and applying this current to the reset windings of transformers T201 and T202. This bias tends to prevent undesired triggering due to noise.

The SCR3 gate circuit is somewhat more complex in operation. A secondary winding on the main commutation transformer, T1, is connected to terminals E212 and E213, providing driving voltage for the SCR3 gate circuit. When SCR2 is fired, a single gate pulse is simultaneously fed to the gates of SCR201 and Q203 [a programmable unijunction transistor (PUT)]. The conduction of SCR201 enables charging of capacitor C206, the charging current being supplied by the positive voltage developed across the commutation transformer secondary upon initiation of the commutation cycle. The same pulse which enables conduction of SCR201 also serves to inhibit premature gating of the PUT (Q203), this gate is being initially held at a higher positive potential than the Q203 anode. The decaying sinusoidal voltage applied to the gate of Q203 causes firing of the PUT following the time at which the voltage of terminal E213 (with respect to E212) has decayed to zero and is going negative. This corresponds to the time immediately following the point where the voltage across the commutation capacitor C1 has decayed to zero (at time t_2, fig. 23) and SCR3 forward conduction can be enabled by a gate pulse. This conduction of SCR3 sustains the commutation cycle as previously described. SCR202, enabled by the PUT (Q203), serves to enhance the SCR3 gate firing pulse.

Components for the SCR4 gate circuit are located within the main frame assembly, as described previously. SCR4 gate drive is obtained in the correct sense from a secondary winding on the main commutation transformer T1, which produces a sustained drive for the SCR4 gate at the time it is desirable for SCR4 to conduct (corresponding with time t_3, fig. 23).

The recharge isolation circuit is effectively a self-gated current source, in series between the SSCB power supply -200 Vdc output and the commutation bus (lower terminal of commutation capacitor C1, on the schematic). Gating of the recharge isolation circuit (RIC) is accomplished by sensing the voltage between the -200 Vdc power supply output and the commutation bus. Normally, the RIC is in the on state until the commutation bus voltage (with respect to 270 Vdc COMMON) rises to approximately +130 V (during the commutation cycle) at which time the RIC is

gated off. The RIC then effectively isolates the -200 Vdc power supply output from the commutation bus during the remainder of the commutation cycle, until the commutation bus voltage drops below the approximate value of +130 V toward the end of the commutation cycle. The RIC thus provides a threefold function.

1) Precharge of the commutation bus (commutation capacitor C1) before the commutation cycle.

2) Recharge of the commutation bus following the commutation cycle, to compensate for energy losses within the commutation circuit during the commutation cycle.

3) Sustained charging of the commutation bus (commutation capacitor C1) to compensate for leakage currents, during intervals between commutation cycles, when the SSCB is on, closed into a load.

Transistors Q204 and Q205, shown in Drawing 15824-042 together with associated circuitry, comprise the RIC portion of the gate and recharge isolation circuit.

Analog and Logic Circuits

Reference is made to figure 46 in Appendix A. Again, all logic circuit designators are in the 300 series although only significant digits are indicated on the schematic.

The voltage output of current sensing shunt, R, is connected to the input of the analog sensing circuitry at terminals D301 and D302 on the analog and logic circuit board. The input amplifier, A326, is a Harris HA2620 integrated circuit operational amplifier connected in inverting mode for a gain of -25.7. This amplifier was selected because of good high-frequency response and relatively low offset voltage drift. Consideration of good high-frequency response is essential because the circuit response time is inversely proportional to bandwidth; for a fast-rising fault current, it is important that the main SCR be commutated off before the load current becomes uncontrollable. Offset drift is an important consideration, since at a 15-A load the shunt provides only approximately 75 mV to the input analog amplifier. The gain of this amplifier was selected as being the maximum value that would not cause output clipping under worst-case conditions.

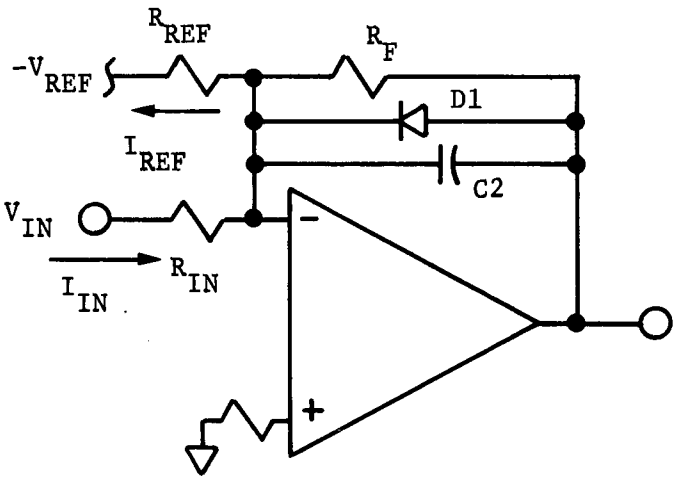
The I_L comparator, A330, is an LM106 integrated circuit. This type of comparator was selected on the basis of fast response, no requirement for a special power supply, and compatibility with COS/MOS logic circuitry. The input to this comparator stage is diode protected to prevent differential input voltage excursions from exceeding rated maximum under worst-case conditions. Near the switching point the voltage across these diodes is small, resulting in a high impedance; consequently, the effect on circuit operation is negligible.

Reference level for the I_L comparator is provided by A328, a μA741 integrated circuit. Calibration for this reference stage is provided by the resistor network R337 through R341. Trip level set is provided by taps in the resistance network R327 through R334.

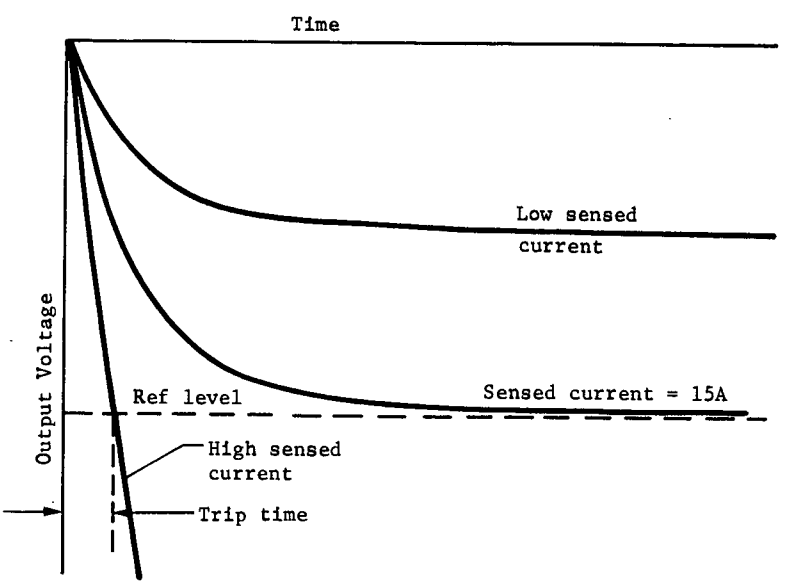
The I^2t comparator, A329, is also located on the Analog and Logic circuit board. This integrated circuit, an LM111, was selected from the standpoint of power supply considerations and compatibility with COS/MOS logic. Fast response in this comparator is of small relative importance since the I^2t output minimum delay is on the order of 3 ms.

Comparator A329 is driven by the A327 stage, an LM101A, which performs the squaring and integration functions for I^2t fault sensing. The squaring function is accomplished at the input, with capacitor C320 in the feedback circuit performing the integration. Diodes CR301, CR304, CR305, and CR306 turn the integrator off when the output reaches zero volts and the sensed current is less than 15 A. This circuit has the advantage of simplicity, relatively low cost, and tolerance of termperature extremes.

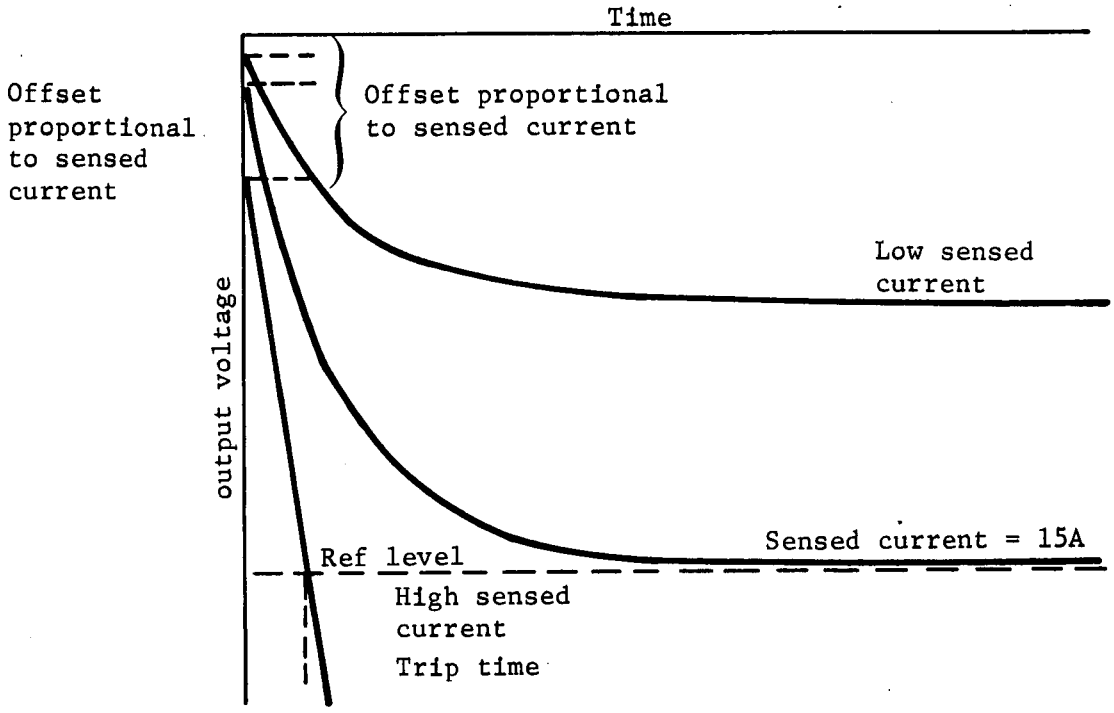
Since no single voltage or current is proportional to the square of the sensed current and since integration is approximated by an R-C circuit with relatively long time constant, analysis of the integrator circuit is simplified by viewing the overall circuit, rather than by separating the two functions of squaring and integration. Consider the following simplified circuit. (Reference designators used throughout this discussion of analog circuitry will pertain to those used in the accompanying illustrations, and will not refer, at this point, to reference designators actually used in the SSCB system.)



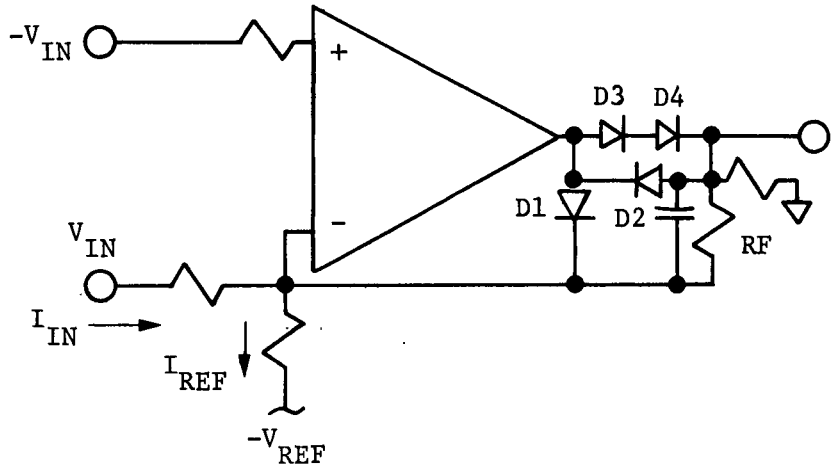
With reference to the above simplified integrator diagram, when the input voltage, V_{IN}, is low so that I_{IN} is less than I_{REF}, the net input to the operational amplifier is negative. The output of this amplifier, attempting to go positive, is clamped at approximately 0.5 V by diode D1; the circuit is now in the off state. When V_{IN} is raised by an increase in sensed current, I_{IN} can exceed I_{REF}, with the result that the output starts going negative as capacitor C2 charges toward the $R_F\left(I_{REF} - I_{IN}\right)$ with a time constant R_FC2. This operation is shown graphically in the following illustration. Note that, thus far, this circuit integrates, but does not square, the input voltage.



The effect of directly squaring the integrator input voltage would be to cause higher current-analog voltages to produce a faster trip than the simplified integrator circuit provides. This same effect is indirectly prodiced by starting the feedback capacitor charging with the output already offset in the negative direction by a value of voltage proportional to the sensed current as shown in the following graph.



This is accomplished by application of the voltage from the current-sensing shunt directly to the noninverting input of the operational amplifier, as shown in the following schematic.



Approximation of the desired response time versus sensed current is accomplished through appropriate selection of reference voltages, resistance, gains, and time constant. The fastest allowable response is used, considering component tolerances and drift. Long delays cause unnecessary heating of the main SCR; particularly, when multiple resets and reclosures of the SSCB occur. In the preceding discussion of the integrator circuit, the charging of the feedback capacitor to approximately +0.5 V in the off condition has been ignored. The three diodes D2, D3, and D4 provide compensation for this occurrence.

In the off condition, the output terminal of the operational amplifier is still at +0.5 V, but D3 and D4 have insufficient voltage applied across them to reach the knee of their voltage-current characteristic. This blocking state leaves a negligible charge on the feedback capacitor C2, making the output voltage essentially zero.

When I_{IN} exceeds I_{REF}, diode D2 conducts and the feedback capacitor begins to charge. In this case, diode D1 becomes reverse-biased. Diode D2, in the feedback loop, has a negligible effect on circuit performance. When I_{IN} is again reduced to less than I_{REF}, the output voltage returns toward zero due to discharge of the feedback capacitor through diodes D3 and D4 until the output voltage approaches zero. Because these two diodes are in the feedback loop until diode D1 clamps the output, diodes D3 and D4 likewise have a negligible effect on circuit performance.

The response of the prototype of this circuit followed the theoretically predicted curve as shown in figure 24. Subsequent testing of the production units as reported in Section III substantiated this response. The complete squarer-integrator circuit as described above is shown with reference designators and assigned component values in the SSCB analog and logic schematic diagram, figure 46, in Appendix A.

The logic circuitry utilizing COS/MOS flatpack integrated circuits is included on the other half of the analog and logic printed circuit board. The logic circuit operation is portrayed by the block diagram shown in figure 25 and is discussed in the operating sequence.

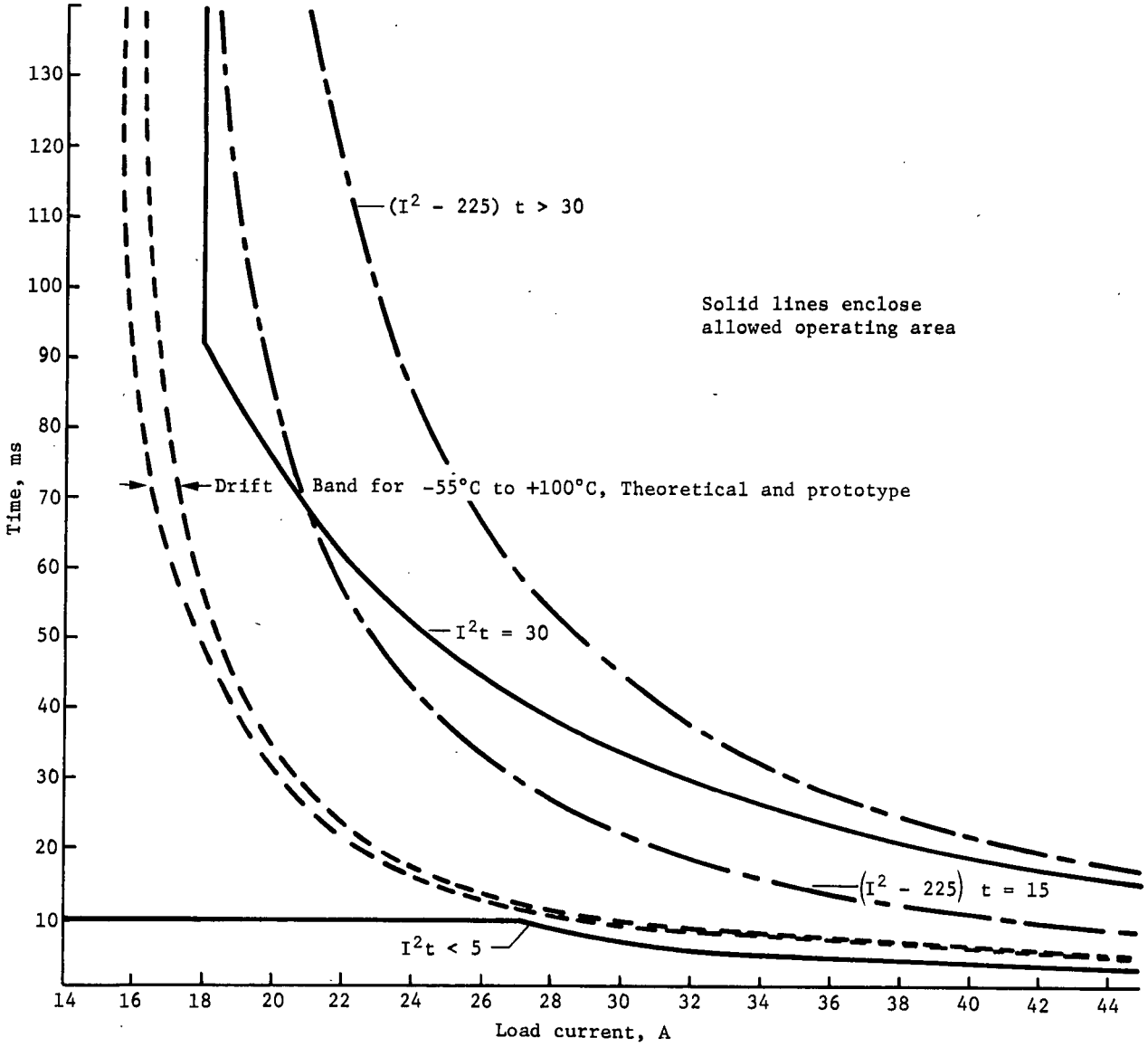


Figure 24.- Analog I^2t Trip, Theoretical and Prototype SSCB

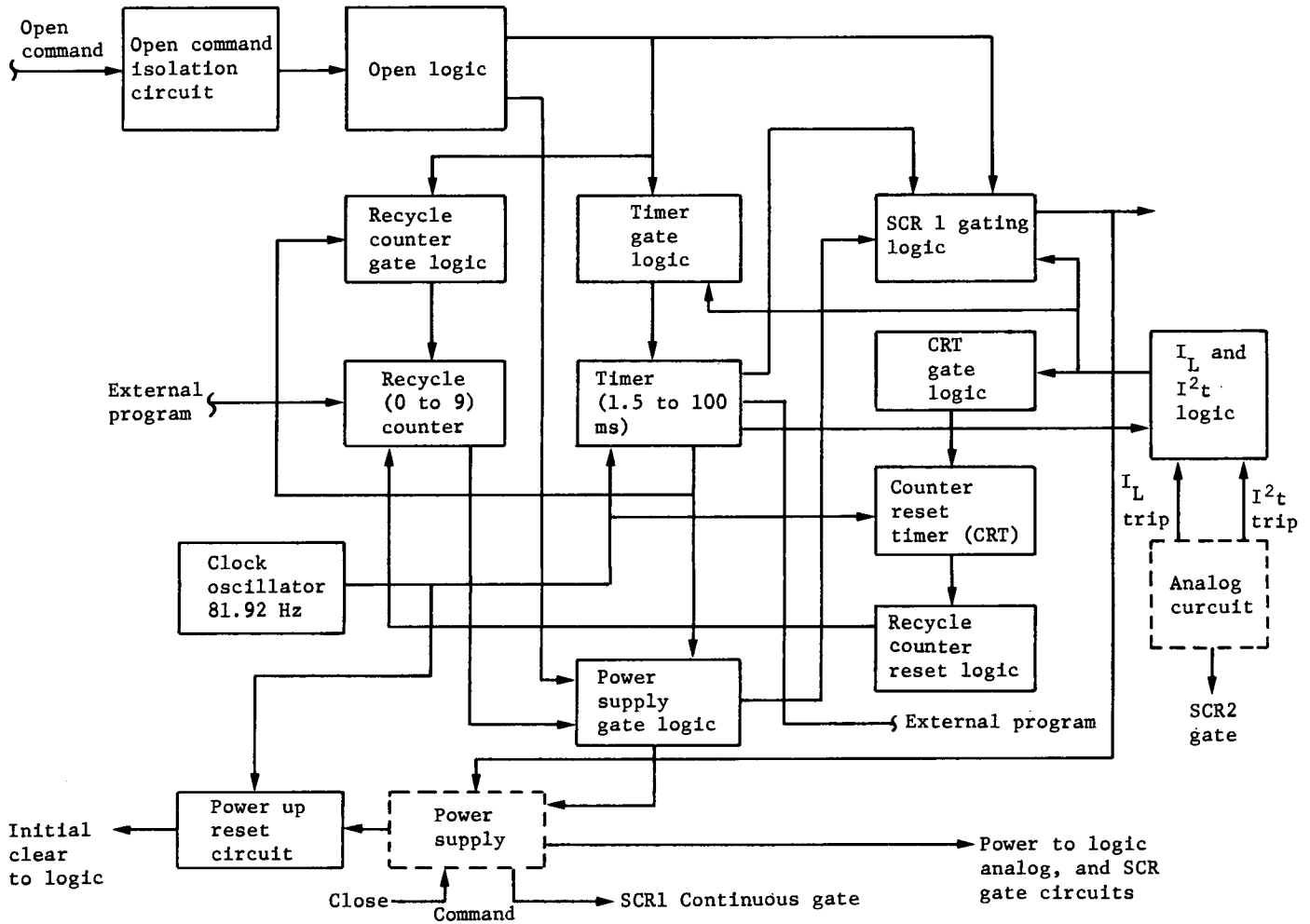


Figure 25.- Solid-State Circuit Breaker Logic Block Diagram

SSCB Operational Sequence

Upon application of the MANUAL CLOSE COMMAND to the SSCB, the power supply begins switching. A 12-V output from the power supply is fed to POWER UP RESET circuitry (on the logic board). An INITIAL CLEAR signal from the POWER UP RESET circuit sets all logic to the initial state, and also prevents SCR1 from being gated to the on state. Integration circuitry within the POWER UP RESET portion of the logic is designed so that the POWER UP RESET changes the logic state of the INITIAL CLEAR signal in approximately 100 ms following application of the MANUAL CLOSE COMMAND. When the INITIAL CLEAR signal changes the logic state, SCR1 is gated on, closing the SSCB into the load.

When SCR1 is fired, the SSCB must be prepared to open under fault-trip conditions, in the event that SCR1 closes into a short circuit or other overload condition. As a result, several conditions have to be established during the POWER UP RESET interval. These conditions are listed.

1) All power supply output voltages should be stabilized at operational levels.

2) Analog circuitry must be capable of identifying and responding to sensed overload conditions.

3) Logic circuitry must be capable of responding correctly to analog fault-trip output signals.

4) The SSCB must be capable of commutation when the analog circuitry senses overload conditions, fires SCR2 to initiate TURN OFF commutation, and sends a fault-trip signal to the logic. This means that commutation capacitor C1 must be precharged as described previously.

When the SSCB is closed into a load, and the I_L or I^2t fault condition is sensed by the analog circuitry for the first time, the following functions occur simultaneously.

1) The analog TRIP signal is fed to SCR2 comparator circuit, A202, on the gate board; this signal switches the output state of A202, which subsequently fires the SCR2 gate, initiating the commutation cycle.

2) The analog TRIP signal, also fed to the I_L and I^2t logic to feed a CONTINUOUS GATE DISABLE COMMAND to the power supply, removing the continuous gate from SCR1.

3) The programmable timer within the logic starts counting time.

4) The counter reset timer within the logic starts counting time.

SCR1 is now commutated off. When the programmable timer count ends, the following functions occur simultaneously.

1) The CONTINUOUS GATE COMMAND, fed by the logic to the power supply, changes from DISABLE to ENABLE state, with the result that the continuous gate drive is reapplied to SCR1.

2) This same signal, applied to SCR1 comparator circuit on the gate board as SCR1 GATE ENABLE signal, switches the output state of comparator A201; this results in subsequent application of a firing pulse to the gate of SCR1. SCR1 is now in the on (closed) state, sustained by continued application of the continuous gate drive to maintain conduction for low values of load current.

3) The recycle counter within the logic counts one.

In the event the fault is still present on the load, the cycle repeats until either the fault clears or the recycle counter reaches its programmed count setting.

If the fault clears, SCR1 remains in the on state. After approximately 102 s, the counter reset timer resets the recycle counter to zero count. In case a later fault occurs, the complete cycle is again initiated.

If the fault persists and the recycle counter reaches its full programmed count, SCR1 is not gated on and thus remains in the off state. the SSCB is now OPEN, remaining in this state until an external MANUAL CLOSE COMMAND is again applied to the SSCB. With the SSCB in the OPEN state, logic command disables the SSCB power supply as described in the preceding paragraphs.

SECTION III

FABRICATION AND TEST PHASE

This phase of the contract effort included fabricating circuit breakers and transfer switches in accordance with the design previously discussed. The testing that was accomplished both during the course of fabrication and on the completed units is described. Final testing to establish that the requirements had been achieved and to determine and relate the characteristics of performance was accomplished in accordance with a test plan that was approved prior to testing. These tests and their results are described under Operational Tests and Characterization Tests.

Breadboard Testing

Testing and performance verification was an integral part of this circuit breaker development program. Initial tests were performed on the breadboard analog circuits to verify performance of the Hall device detector and, subsequently, of the shunt detector and its associated overload detection, integration comparison, and trip circuitry. These tests verified operation and performance over the voltage and temperature extremes defined. The breadboard circuitry of the commutation circuit was also tested over the temperature range of -55 to +100°C. This test was particularly necessary early in the program because of the minimal data available on SCR performance. The breadboard of the power supply also was subjected to this same voltage and temperature regime.

Prototype Testing

After the breadboard tests and modification, in some cases, the developed circuits were built up on printed circuit boards. Each of these boards was individually bench-tested for operation over the voltage range and then installed in the environmental chamber and again tested over its voltage operating range at the extremes of -55 and +100°C and a number of temperatures in between. The complete prototype circuit breaker was then assembled and tested as a unit through many thousands of trip cycles for these same voltage and temperature ranges. Testing performed on the prototype and its components served to establish the test requirements and procuedure to be used on the production models. Unfortunately, the schedule for the timely completion of this program defined that the production units were following the prototype by only one month so it was not always possible to incorporate all the improvements that were indicated by the prototype evaluation.

Fabrication and Operational Tests

Operational tests were performed on each production unit in accordance with an approved test plan. The tests performed and results follow.

1) During checkout of the analog and logic printed circuit board prior to assembly, the automatic recycle operation was verified for each setting of 0 to 9 recycles. The recycle time adjustments and the programmable timer were also verified for both normal and high voltage operation of the dc power supply plus a small overvoltage. Table III shows the data recorded for each unit during these tests, which were all made at room temperature. The recycle counter was then set for two resets.

2) During bench checkout of the printed circuit board, the calibration of the ultimate trip levels for each programmable level setting was accomplished. A number of tests were made at voltages 0.9 V above and below nominal. The maximum and minimum current levels to trip at room temperature were recorded. These showed variations from a maximum of about 25% at 18 A to a maximum of 5% at 45A. Levels were adjusted so the average trip levels were at or below the nominal values. Table IV shows the average data values recorded for each unit for the defined trip level settings. Each circuit was then set for a 45 A ultimate trip setting. I^2t threshold settings were initially made at 18 A for testing and were, subsequently, readjusted to a threshold value of 15.85 A for operation.

3) Inspections were accomplished during the breaker assembly after each major step. The main frame and its wiring were verified against the wiring diagram. The system wiring diagram is shown in Figure 45 (App A). The power supply printed circuit board was then installed and connected and the new wiring again verified. This procedure was repeated for the gate circuit board and again verified. This procedure was repeated for the gate circuit board and again for the analog and logic board. Final touch-up of conformal coating on terminals was accomplished and cured. The complete assembly was then installed in the test assembly for system tests. The test equipment assembly is shown in figure 26 with one of the circuit breakers in the open temperature control chamber. System operational tests were then performed as follows. (Test procedures by which these tests were performed are included in Appendix B.)

Table III.- Programmable Timer Calibration

Serial number	Voltage dc supply	Time set, ms							Osc frequency, kHz	Pulse width, μs
		1.5	3	6	12	25	50	100		
1	11.5	1.65*	3.25	6.25	13.0	26	52	104	78.2	12.4
	13.0	1.65	3.25	6.25	12.5	26	52	104	78.2	12.4
2	11.5	1.64	3.25	6.5	13.0	26	52	104	78.2	13.0
	13.0	1.66	3.25	6.5	13.0	26	52	104	78.0	13.0
3	11.5	1.66	3.3	6.6	13.2	26	52	104	77.92	12.8
	13.0	1.66	3.3	6.5	13.2	26	52	104	78.0	12.8
4	11.5	1.64	3.25	6.5	13.0	26	52	104	78.2	12.6
	13.0	1.64	3.25	6.5	13.0	26	52	104	78.2	12.6
5	11.5	1.66	3.15	6.6	13.0	26	52	104	76.8	13.1
	13.0	1.66	3.3	6.6	13.2	26.5	53	106	77.0	13.0

*Actual time readout in ms.

Table IV.- Calibration of Ultimate Trip Current Levels

Serial number	Voltage dc supply	Current set, A						
		18	20	25	30	35	40	45
1	10.9	17.6*	19.2	24.4	29.3	34	29.8	44.6
	12.7	17.5	19.0	24.1	29.4	34.6	39.6	44.8
2	10.9	17.7	19.3	24.4	29.5	34.8	39.8	44.9
	12.7	17.8	19.2	24.3	29.4	34.7	40.0	44.7
3	10.9	17.1	18.7	23.6	29.2	34.3	39.5	43.4
	12.7	17.1	18.7	23.6	28.5	33.6	39.5	44.2
4	10.9	18.1	19.3	24.3	29.5	34.8	40.1	45.1
	12.7	18.2	19.7	24.8	29.4	34.8	39.3	44.7
5	10.9	17.9	19.6	24.4	29.2	33.4	38.9	43.5
	12.7	18.6	19.6	24.6	29.0	33.0	37.9	44.0

*Actual trip level in amperes.

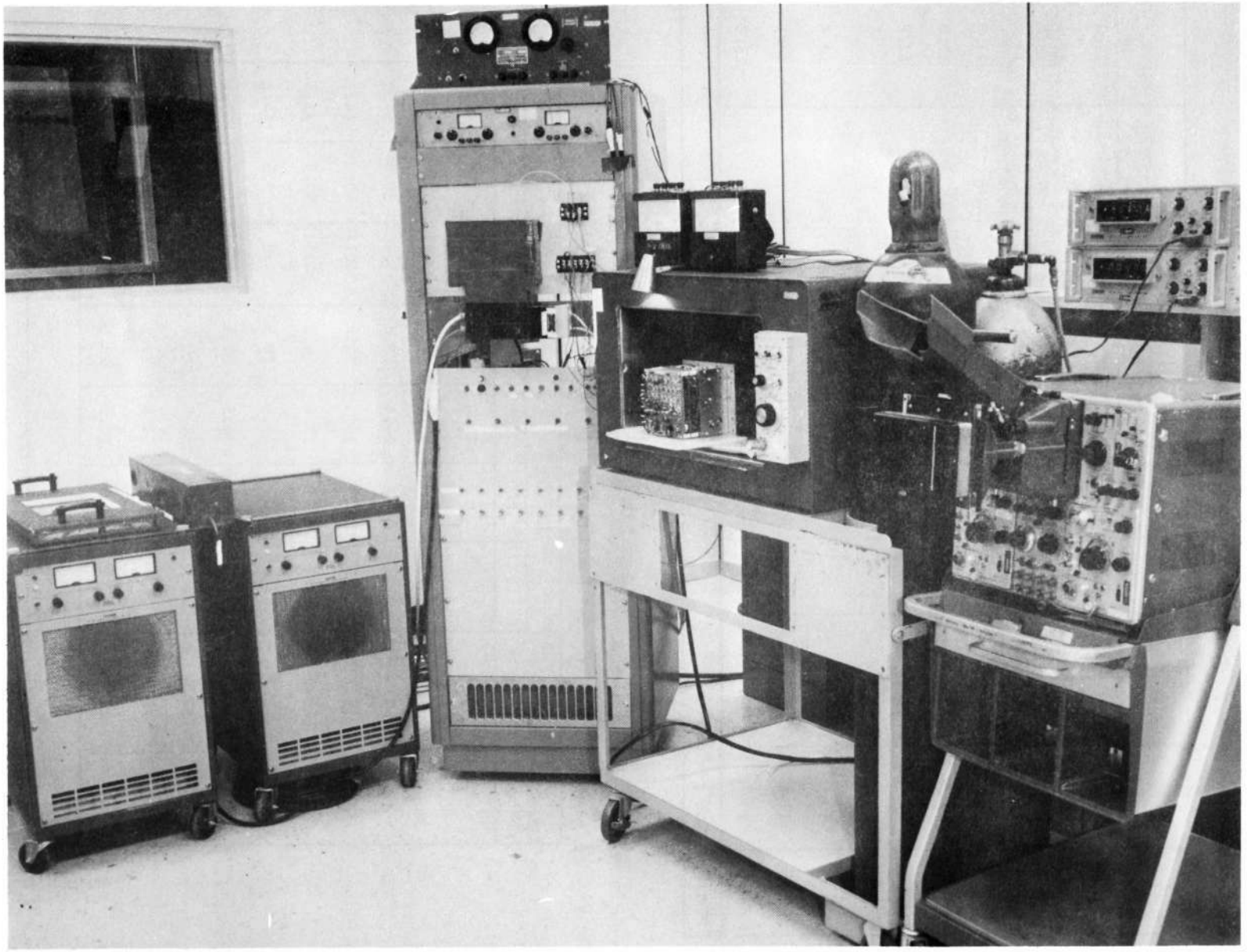


Figure 26.- Circuit Breaker Test Assembly

a) Each unit was first verified to respond to the manual CLOSE and OPEN commands.

b) A voltage drop test was made in which the voltage across the closed breaker was measured while the breaker was conducting the specified 15 A.

c) Tests were then performed to establish the time to trip for an 18-A I^2t at 270 V and a 35-A I^2t trip at 243 V. Recycle time was also determined for the 35-A I^2t trip. Photographs of typical data for these three tests are shown in figures 27, 28, and 29, respectively.

d) Although it was not a contractual obligation, tests were performed to verify that the breaker could be subjected to a short duration overcurrent and would not trip if the I^2t value did not reach the trip value. A steady-state load of 10 A was imposed and then, by a circuit in the test tool, a transient load with a peak above 30 A was added. This test was performed at both 243 and 270 V. Figure 30 shows the waveform used for this test and figure 31 is a photograph of the typical data.

e) An ultimate trip test was then performed at a 45-A setting with 243 V on the breaker. The ultimate trip setting was then changed to 18 A and a second ultimate trip test was performed at 297 V. Data were also recorded for an 18-A ultimate trip recycle time determination. Figures 32 through 34 show typical oscilloscope photographs of these ultimate trip tests.

A compilation of the data obtained in the operational tests is shown in table V. This table also shows the mean value determined for each parameter and the deviation of each discrete value from the mean. The maximum deviation from the mean is also indicated. A sample size of five units is not large enough to predict statistical probabilities, but the maximum deviations indicate the worst-case conditions for the sample. Figure 35 portrays the values for each breaker so that easy comparisons can be made.

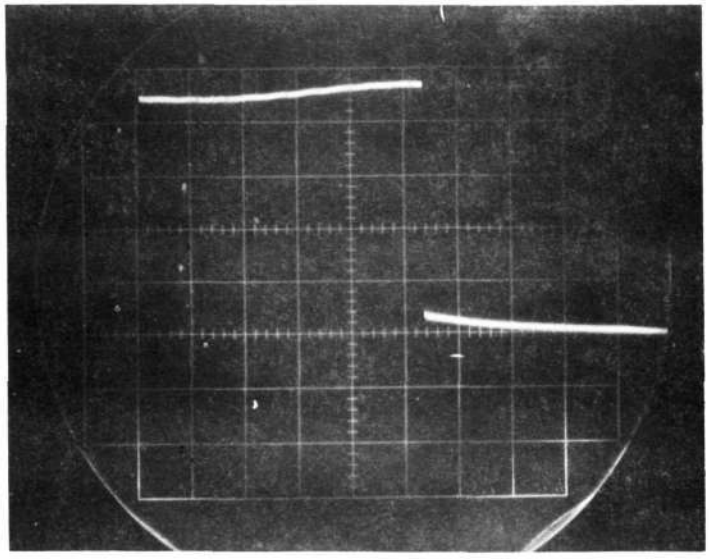


Figure 27.- 18-A I^2t Operational Test
(Vertical 4 A/division;
Horizontal 10 ms/division)

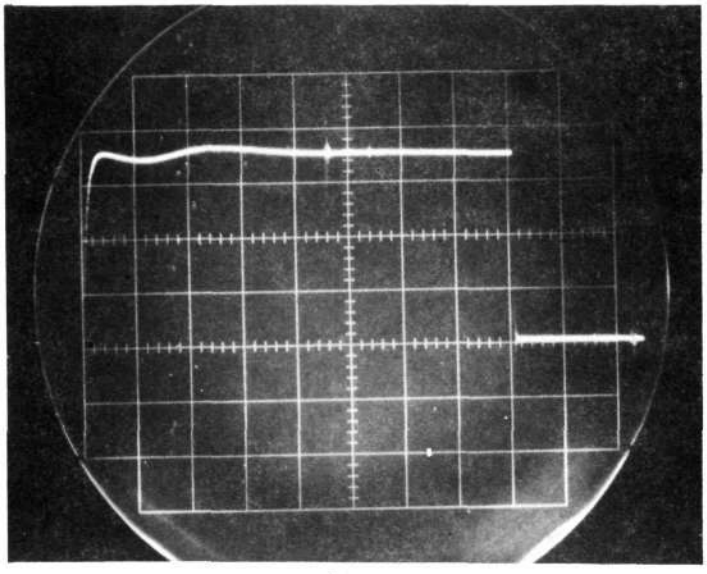


Figure 28.- 35-A I^2t Operational Test
(Vertical, 10 A/division;
Horizontal 1 ms/division)

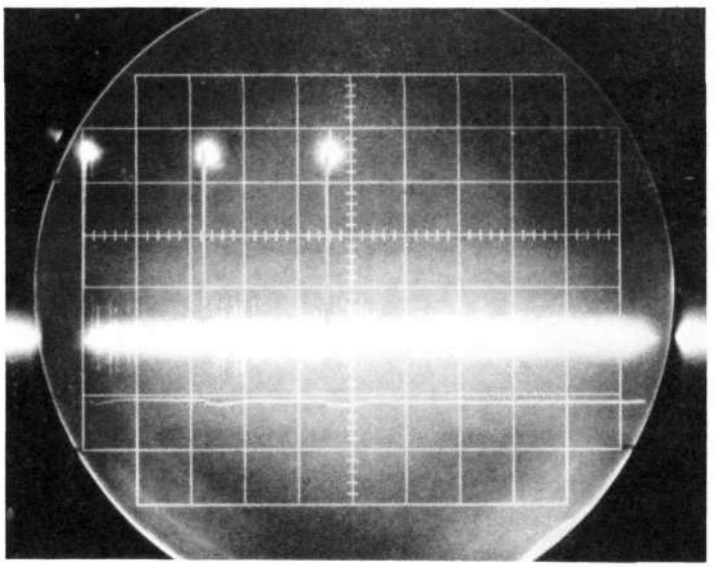


Figure 29.- 35-A I^2t Recycle Operational Test (Vertical, 10 A/division; Horizontal, 50 ms/division)

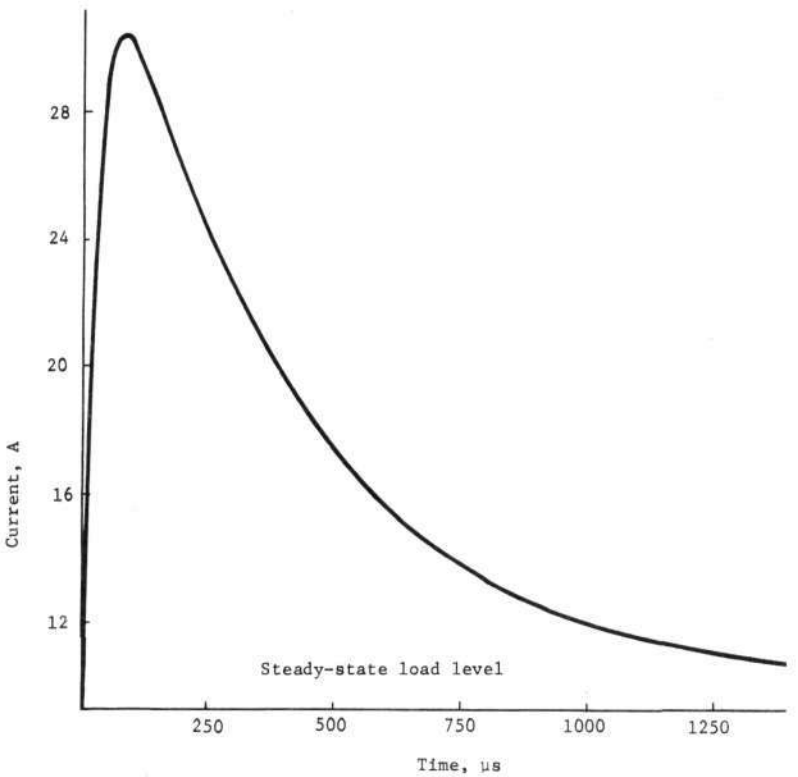


Figure 30.- Transient Load for No-Trip Test

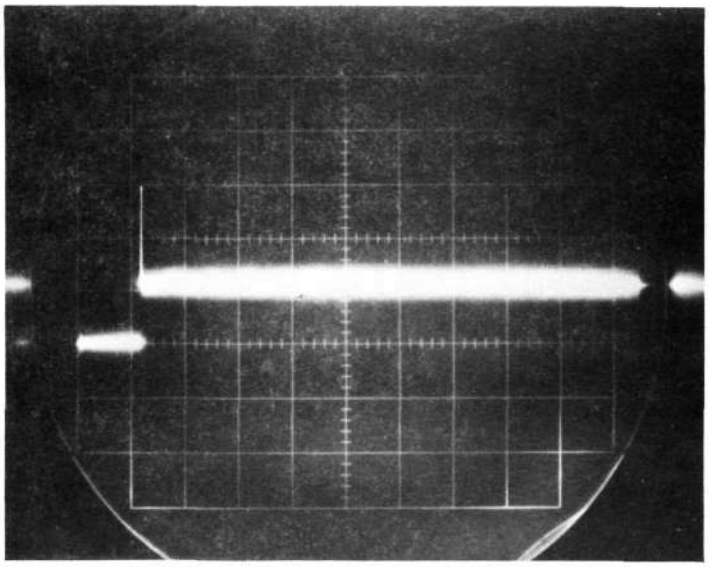


Figure 31.- Transient No-Trip Special Test
(Vertical, 10 A/division;
Horizontal, 100 ms/division)

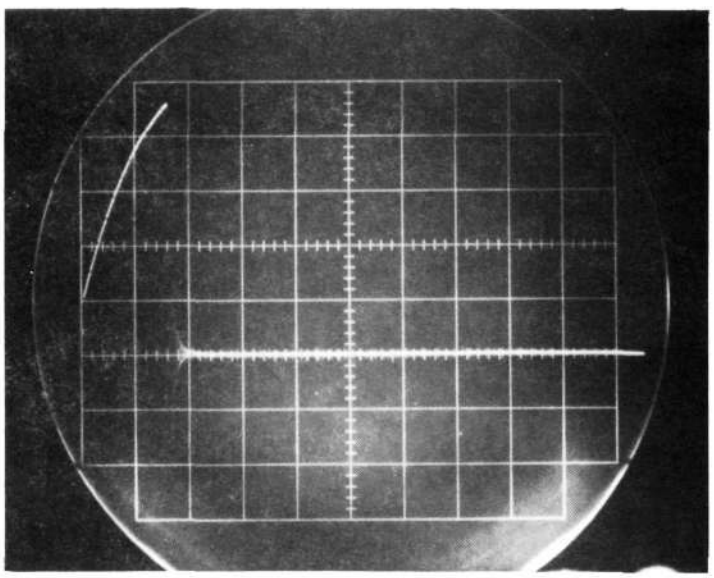


Figure 32.- 45-A Ultimate Operational Test
(Vertical, 10 A/division;
Horizontal, 100 μs/division)

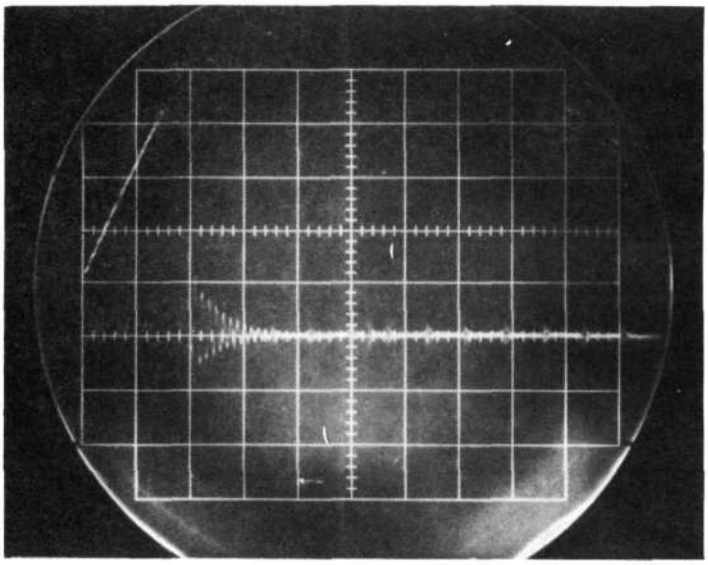


Figure 33.- 19-A Ultimate Operational Test (Vertical, 4 A/division; Horizontal, 20 μs/division)

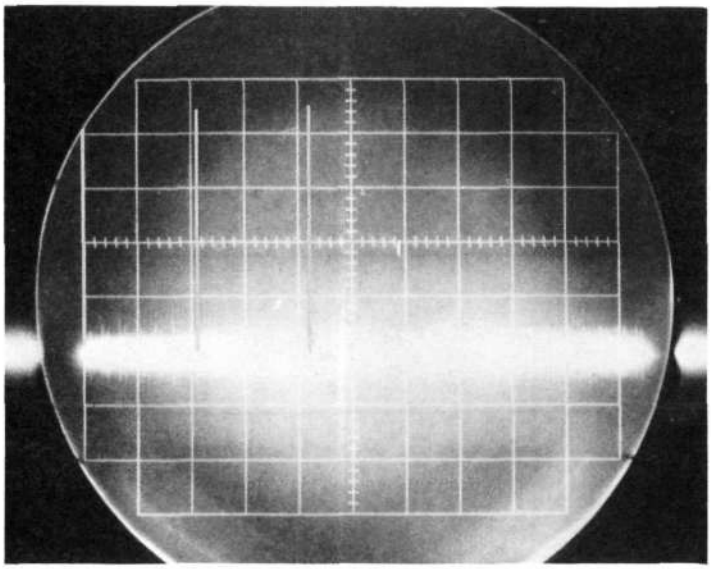


Figure 34.- 18-A Ultimate Recycle Operational Test (Vertical, 4 A/division; Horizontal, 50 ms/division)

TABLE V.- OPERATIONAL TEST DATA

Serial number	Voltage drop, V	18 A I^2t time to open, ms	35 A I^2t time to open, ms	35 A I^2t recycle time, ms	45 A ultimate time to open, μs	18 A ultimate time to open, μs	18 A ultimate time to open, ms
1	3.06	52	7.4	110	180	34	110
	+0.15†	-4.6†	-0.5†	-1.2†	-8†	+0.4†	+2.9†
2	2.95	86/62*	8.2	110	200	34	105
	+0.04†	+5.4†	+0.3†	-1.2†	+8†	+0.4†	-2.1†
3	2.77	55	8.1	112	170	30	105
	-0.14†	-1.6†	+0.2†	+0.8†	-22†	-3.6†	-2.1†
4	2.98	50	8.1	112	200	36	105
	+0.07†	-6.6†	+0.2†	+0.8†	+8†	+2.4†	-2.1†
5	2.81	64	7.8	112	210	34	117
	-0.1†	+7.4†	-0.1†	+0.8†	+18†	+0.4†	+9.9†
Mean	2.914	56.6	7.92	111.2	192	33.6	107.1
Maximum Deviation	5.15%	+13.09%	-6.31%	-1.01%	-11.4%	-7.14%	+9.24%

*Unit 2 trip setting was initially set to the 86 ms setting, which is within specified values, but was subsequently adjusted to provide an 18 A I^2t in a nominal 60 ms period.

†Deviation from the mean.

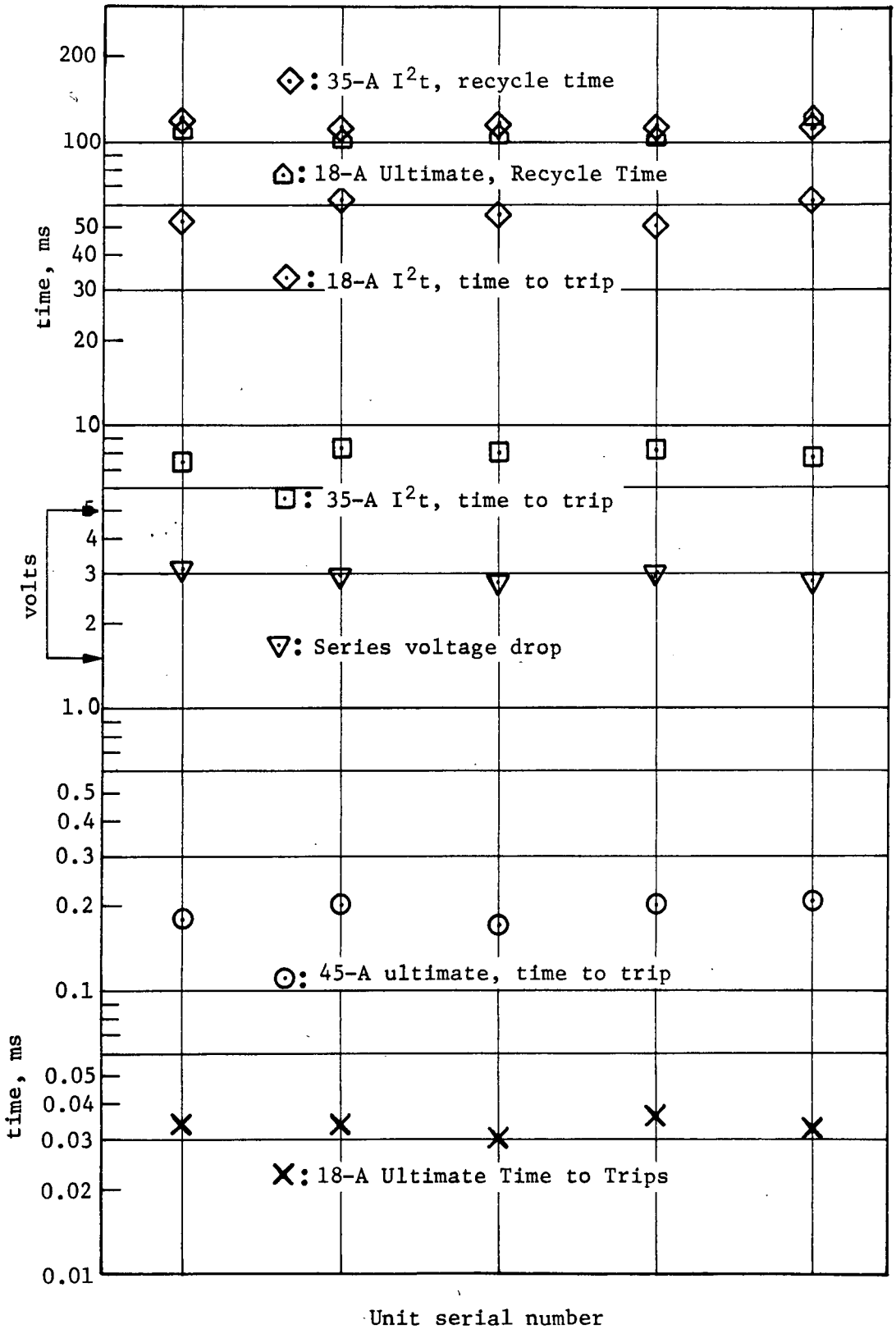


Figure 35.- Comparison of Operational Test Data

4) Two breakers were connected together as a transfer switch with an auxiliary control unit as shown in figure 36. This connection automatically ensured that the CLOSE command for either breaker resulted in an OPEN command for the other prior to the time the CLOSE command became effective. It was verified that breaker A could be turned on by manual command; the load could be transferred to breaker B and breaker B could be turned off. Breaker B could be turned on by manual command; the load could be transferred to breaker A and breaker A could be turned off. Either breaker could be turned on and off without transferring the load to the other. An overload on either breaker would result in opening the breaker without transfer to the other. All five of the breakers were designed and built so that any pair could be connected together to serve as a break-before-make transfer switch.

Characterization Tests

Characterization tests were performed on specific breakers as follows.

1) A transient susceptibility test was performed on both an open and closed breaker. The test was first performed using a 300-V peak overvoltage triangular pulse 10-μs long in series with the 270-V input line. When the breaker was open, and the control leads were connected into the test tool, which also contained the pulse-forming network, the breaker turned on and closed. When the breaker was closed, application of the pulse caused it to commutate once. To eliminate the possibility of coupling within the test tool, the control leads were disconnected from the tool and connected together to eliminate stray electrostatic pickup. The test was then repeated using only a 150-V pulse. With this condition, the breaker remained open when tested in the open condition, and remained closed when tested in the closed condition. The test was not repeated at 300 V by customer direction not to take a chance on over-stressing any of the circuitry.

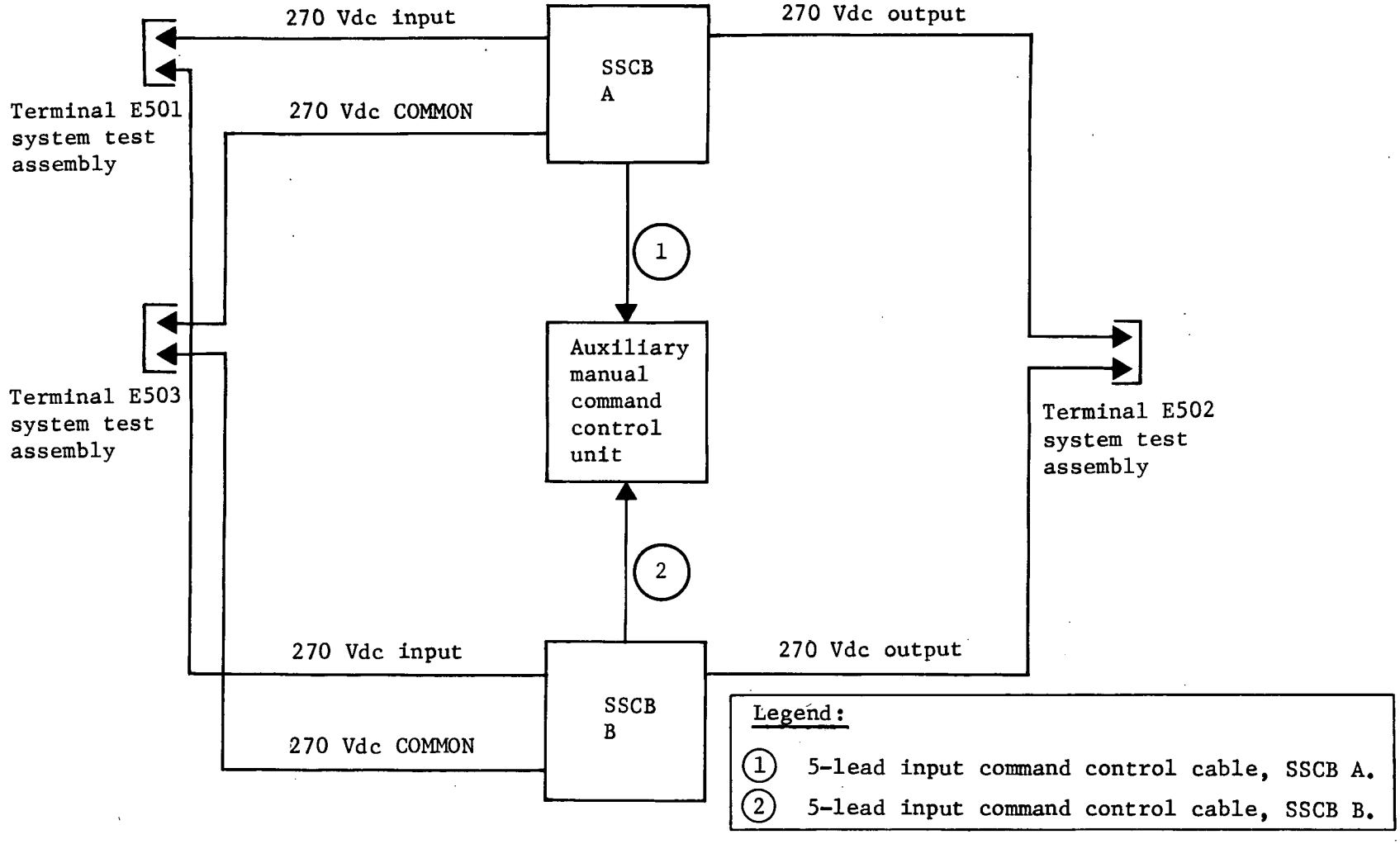


Figure 36.- Operation of Two SSCB Units, Transfer Switch Configuration Common Source and Common Load

2) Thermal tests were performed by mounting a breaker in a thermal test chamber and controlling the temperature to 25, 50, 0, -45, and +100°C, in that order. It was desired to test to -55°C; however, after results of operation on a previous test, it was decided to limit the low temperature to -45°C. The previous test was terminated at -55°C, due to a scrap of metal being dislodged from some recess in the environmental chamber, which caused a short on the power supply circuit board. The ensuing arc necessitated rebuilding the unit. After this, all the power supply and gate circuit boards were conformal coated to minimize any future contamination problems that might result in a high voltage breakdown. After conformal coating, tests performed on another program indicated that thermal stresses were causing broken connections at low temperature. The low temperature limit was therefore established at -45°C.

For each temperature, the unit was stabilized for a period of about an hour. The temperature on the main frame also was monitored by means of a thermocouple. An operational test sequence, consisting of a series voltage drop, an 18-A I^2t trip, a 35-A I^2t trip and 35-A I^2t recycle time, a 45-A ultimate trip and 45-A ultimate trip recycle time, was then performed. The unit was then stabilized at the next temperature and the test sequence repeated. Data from these thermal tests are shown in Table VI and are portrayed graphically in Figure 37.

3) A life test was performed where each of three units was operated for 1000 cycles, one at each temperature of 0, 25, and 50°C. The units were set for zero recycle and were operated automatically by the test tool in a sequence of about 4 cycles per minute during which the breaker was closed for about 12 s with a 15-A load. An overload, between 3 and 5 A, was then connected resulting in an automatic trip and shutdown of the breaker. After a nominal 2-s delay, the breaker was again commanded to CLOSE and the cycle was repeated. After 10, 100, 200, 500 and the complete 1000 cycles of operation a modified operational test was performed. Thes test consisted of a forward voltage drop, an 18-A I^2t, a 35-A I^2t and a 45-A ultimate trip test. Data from these tests are tabulated in Table VII and are portrayed in Figure 38.

TABLE VI.- CHARACTERIZATION TEST (SERIAL NO. 5 THERMAL TEST DATA)

Temperature, °C	Voltage drop, V	18 A I^2t time to trip, ms	35 A I^2t time to trip, ms	35 A I^2t recycle time, ms	45 A ultimate time to trip, μs	45 A ultimate recycle time, ms
-45	2.95	54	8.0	115	180	107
0	2.9	62	8.0	115	160	105
25	2.8	57	8.0	115	170	107
50	2.77	64	7.8	115	155	105
100	2.85	56	7.8	115	170	110

TABLE VII.- CHARACTERIZATION TEST (LIFE TEST DATA)

Serial number at temperature	No of cycles	V_f, V	18 A I^2t time to trip, ms	35-A I^2t time to trip, ms	45-A ultimate time to trip, μs
5 at 0°C	10	2.73	52	8.1	160
	100	2.88	50	7.8	160
	200	2.81	51	6.6	120
	500	2.85	49	7.9	160
	1000	2.93	51	7.9	150
2 at 25°C	10	3.04	52	8.3	160
	100	3.11	62	8.2	150
	200	3.28	62	8.3	170
	500	3.2	64	8.4	190
	1000	3.29	64	8.0	170
1 at 50°C	10	2.83	51	8.0	170
	100	3.31	49	7.0	150
	200	3.28	49	7.0	150
	500	3.07	49	8.0	150
	1000	3.28	50	8.0	150

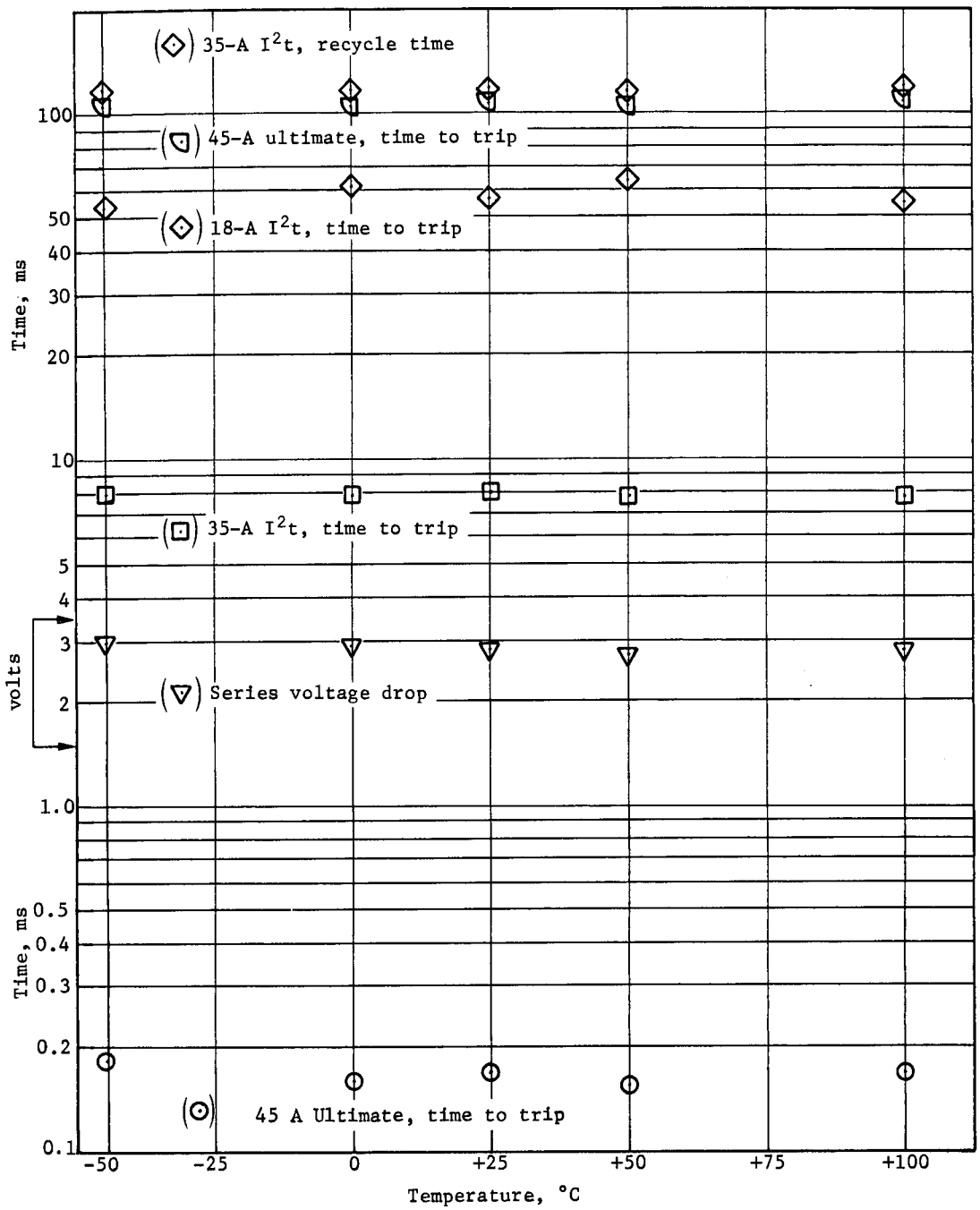


Figure 37.- Variations with Temperature, Serial Number 5 Characterization Test

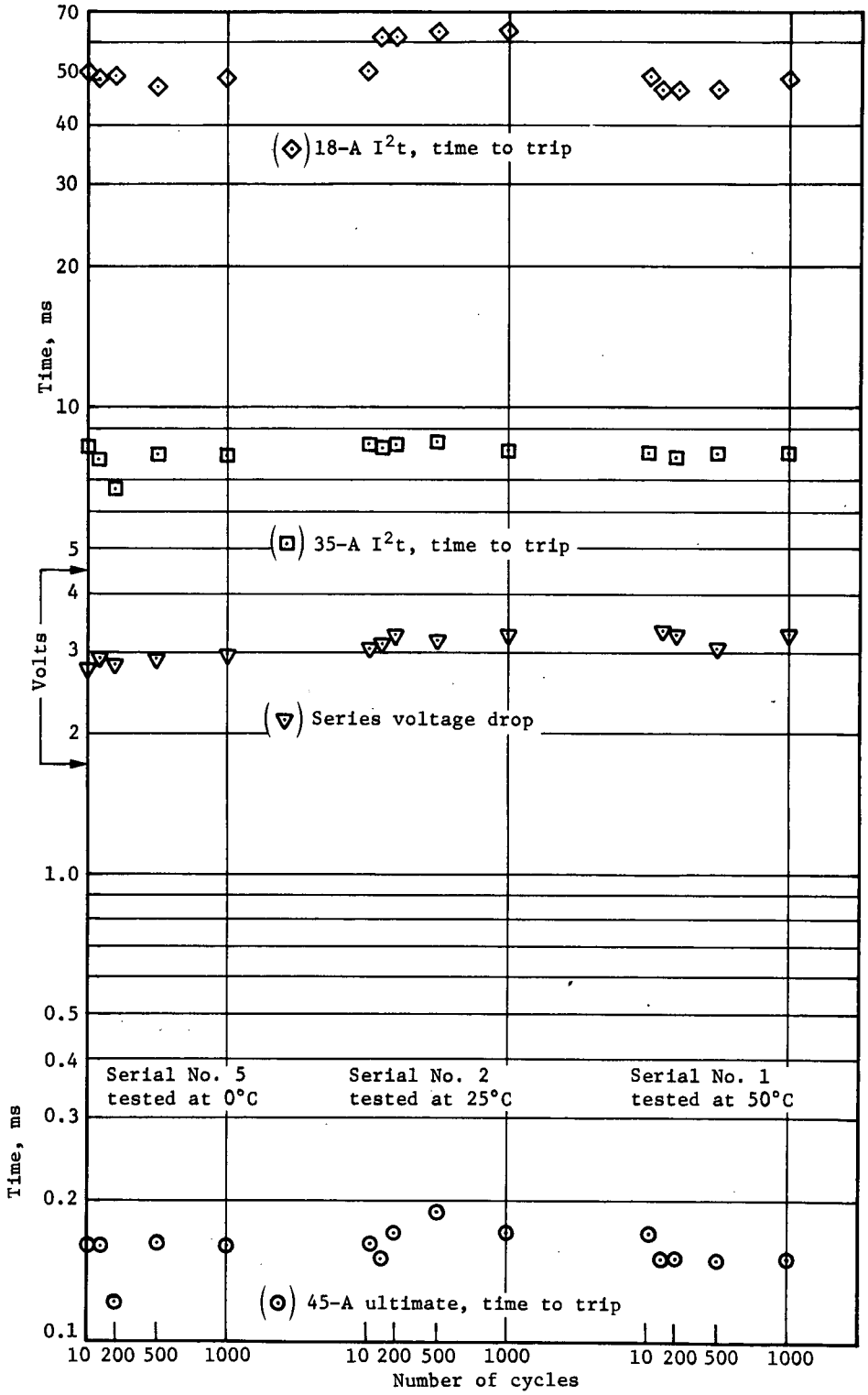


Figure 38.- Life Test Data Comparison for Characterization Test of Three Breakers at 0, 25, and 50°C

4) To compare the I^2t values obtained from these tests, data on the prototype performance were used to compute I^2t values; these are shown on table VIII. These values are then plotted on figure 39. The I^2t test data on the five production breakers for tests at 18 and 35 A are then listed in table IX together with the computed I^2t values. These values, including those from the comparable points on the prototype, are then shown on figure 40 for easy comparison.

TABLE VIII.- PROTOTYPE I^2t RATING

Current, A	Time to Trip, ms	I^2t, A^2-s	I/I_o
16	110	28.16	1.06
17	70	20.23	1.13
18	54	17.49	1.2
20	33	13.2	1.33
22	23	11.13	1.46
27	14	10.21	1.8
35	7.5	9.18	2.33
42	5	8.82	2.8
45	4.3	8.70	3.0

5) A test was performed to determine the voltage range over which the breaker would operate. Beginning at 243 V, the lowest specification value, the voltage was dropped in increments and operations CLOSE, OPEN, and 18-A I^2t trip were verified. It was found that consistent and reliable operation could be achieved down to a voltage of 170 V. This test was performed at room temperature only.

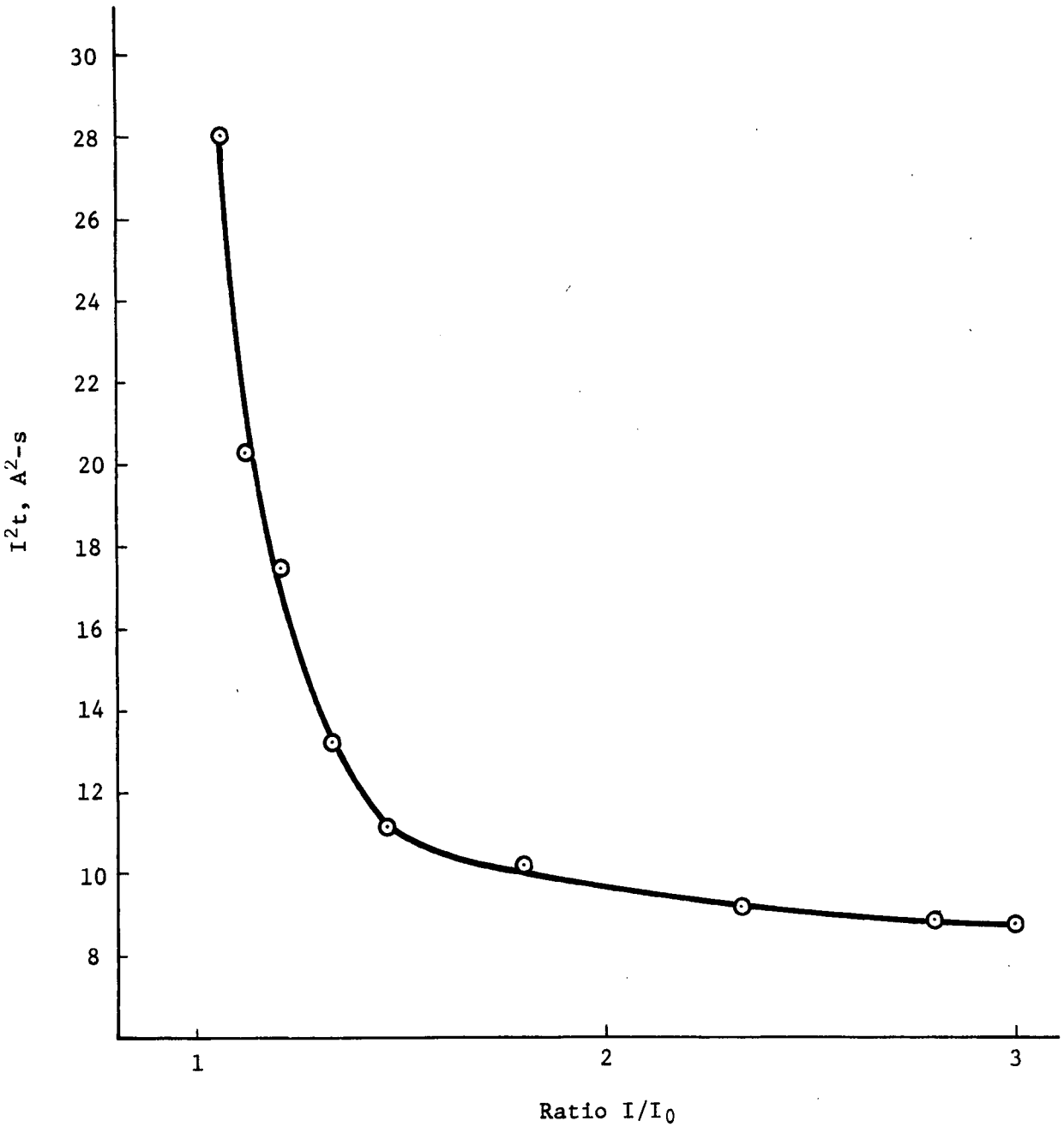


Figure 39.- I^2t Rating, Where I_o = 15 A

TABLE IX.- COMPILATION OF I^2t RATINGS

Test identification		18-A time to trip, ms	I^2t, A^2-s	35-A time to trip, ms	I^2t, A^2-s
Operational test, serial number	1	52	16.85	7.4	9.06
	2	62	20.09	8.2	10.04
	3	55	17.82	8.1	9.92
	4	50	16.2	8.1	9.92
	5	64	20.74	7.8	9.56
Thermal test serial number 5, °C	-45	54	17.50	8	9.8
	0	62	20.09	8	9.8
	25	57	18.47	8	9.8
	50	64	20.74	7.8	9.56
	100	56	18.04	7.8	9.56
Life test, 0°C, serial number 5, No. of cycles	10	52	16.85	8.1	9.92
	100	50	16.2	7.8	9.56
	200	51	16.52	6.6	8.08
	500	49	15.88	7.9	6.68
	1000	51	16.52	7.9	9.68
Life test, 25°C serial number 2, No. of cycles	10	52	16.8	8.3	10.17
	100	62	20.08	8.2	10.04
	200	62	20.08	8.3	10.17
	500	64	20.7	8.4	10.29
	1000	64	20.7	8.0	9.8
Life test, 50°C, serial number 1, No. of cycles	10	51	16.52	8.0	9.8
	100	49	15.88	7.0	8.58
	200	49	15.88	7.8	9.56
	500	49	15.88	8.0	9.8
	1000	50	16.2	8.0	9.8

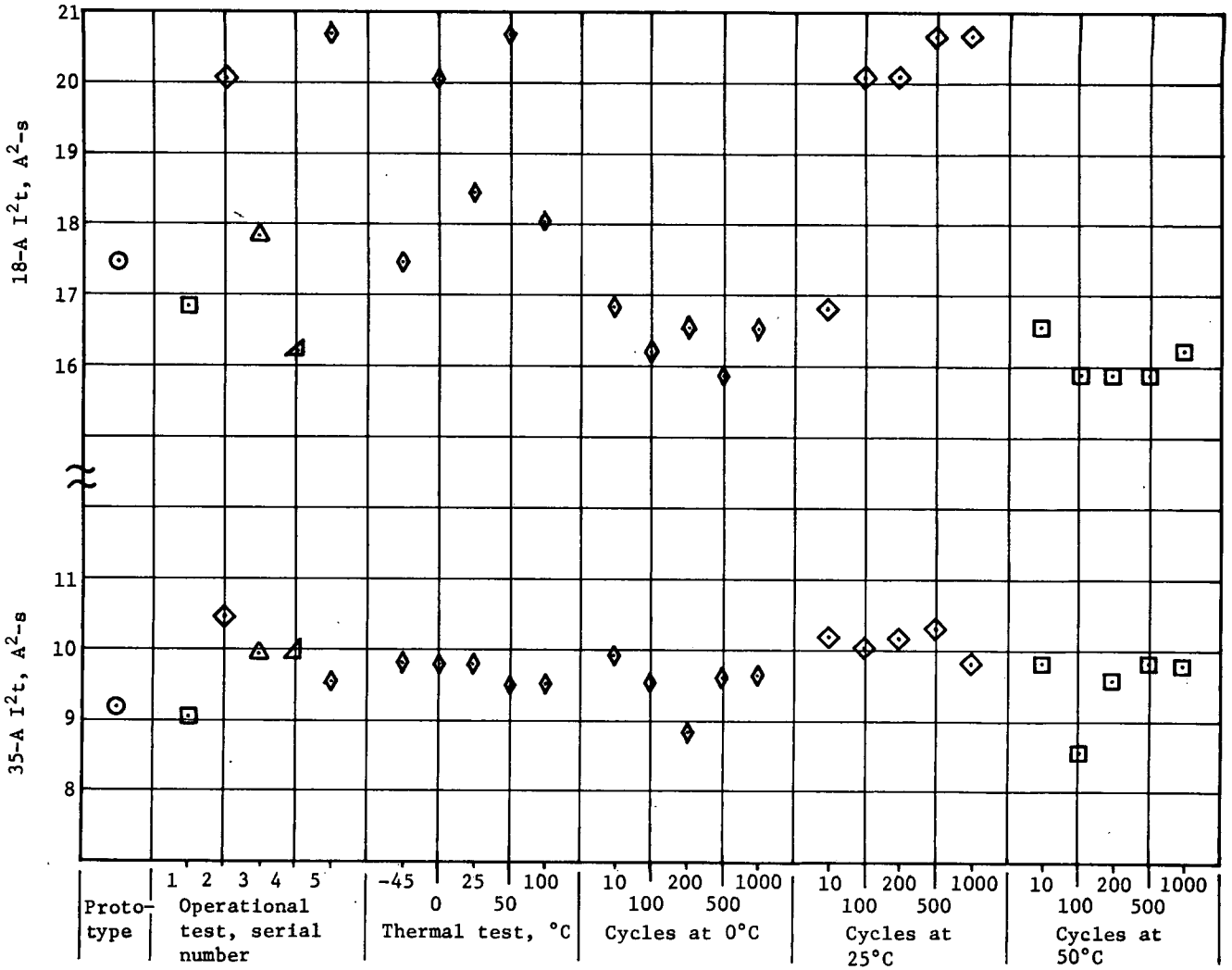


Figure 40.- Distribution of I^2t Rating

6) All the testing involving thermal control was accomplished in a thermal control chamber with the main cover removed and air or dry nitrogen being forcibly circulated to ensure that the desired temperature was maintained. In order to evaluate the effect of the covers, one unit with the cover installed was mounted on the test fixture on the front of the test tool. The vent holes were oriented to the bottom and top of the cover. The fins of the heat sink were horizontal and the cover over them was about 1/4-in. from the face of the panel. The unit was instrumented by a thermocouple mounted in free space near the anode of SCR1. The unit was closed into a 15-A load and operated continuously. The temperature was monitored at 1-min intervals until it reached a value of 51°C, at which point the test was arbitrarily concluded. Data from this test are shown in table X and are plotted on figure 41.

Problems and Recommendations

1) One of the greatest complexities created in the design of the breaker was that of making a commutating circuit to turn OFF the main SCR. The SCR, in contrast to a transistor, has the advantage of not requiring a power source to keep it conducting at low loss. However, due to the complexities of developing reliable commutation circuits, a tradeoff study should be made relating new transistor developments, SCRs, and gate control switches before a second-generation breaker development is undertaken. Of course, electrical power system requirements for any breaker must enter into this trade study.

2) The electrical system operational requirements for a breaker should be well established before the breaker design is undertaken. Every effort should be made to incorporate the maximum logic into the control system and not into the breaker. For example, if the breaker is to be controlled by an automatic sequencer or a computer, the computer should make the "try again" decision, after an overload trip, rather than incorporating this logic into the breaker. Similarly, breaker power on and breaker CLOSE could be two separate commands and logic within the breaker could be limited to some internal fault protection and a summation sending a "breaker ready" signal to the computer.

TABLE X.- TIME AND TEMPERATURE DATA, ENCLOSED BREAKER

Time	Temperature, °C	Time	Temperature, °C
0825	23.5	0851	44.0
0827	25.7	0852	44.6
0828	27.2	0853	45.2
0829	28.5	0854	46.0
0830	29.5	0855	46.7
0831	30.3	0856	47.2
0832	31.0	0857	47.9
0833	31.7	0858	48.5
0834	32.5	0859	48.9
0835	33.2	0860	49.7
0836	33.9	0901	50.0
0837	34.6	0902	50.8
0838	35.2	0903	51.0*
0839	36.0		
0840	36.7		
0841	37.3		
0842	38.2		
0843	38.9	Cooling Data	
0844	39.5	0904	50.5
0845	40.1	0905	49.7
0846	40.7	0910	46.5
0847	41.5	0920	43.0
0848	42.0	0940	36.0
0849	42.7	1000	32.3
0850	43.5	1040	27.5

*Breaker commanded open.

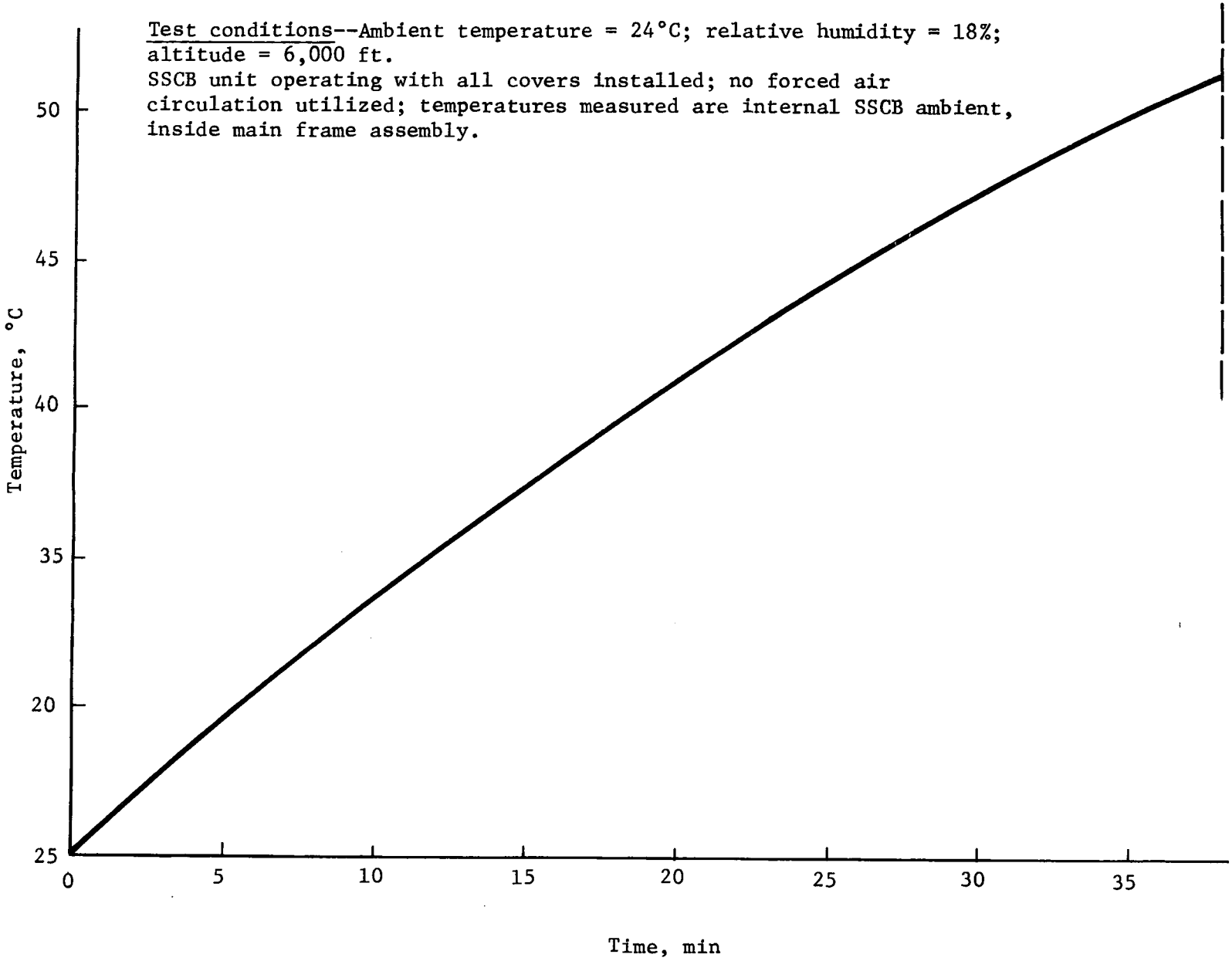


Figure 41.- Temperature Rise, Prototype SSCB, 243-Vdc Input, 15-A Load Current

3) This contract established a weight goal for the development circuit to establish feasibility of design. In attempting to meet or approach this goal construction techniques were used which are not consistent with ease or economy of change necessary to a development-type effort. For a future feasibility development-type of circuit construction, it is recommended that--

   a) PC board connectors be used instead of terminals and point-to-point wiring;

   b) dual-in-line packaging be used for logic instead of flatpacks;

   c) no weight limitation be imposed until the circuitry is developed and flight-packaging is required.

   With respect to the above recommendations, it should be noted that a larger and, therefore, heavier core in the main inductor would have allowed larger gage wire with a lower IR drop and consequently, complete compliance with the voltage drop requirement as well as a lower heat dissipation within the unit.

4) Deletion of the Hall-effect sensor and use of a shunt entailed operation of most of the logic and analog circuitry at the high voltage potential. It is recommended that any future breaker development reevaluate sensors such as the Hall effect device to see if manufacturing tolerances will permit their use, as the isolation they can afford would be a major advantage. It is also possible that analog response electro-optic isolators may be developed with sufficient linearity to permit their use to isolate a small sensor circuit and yet permit the majority of the control circuitry to operate at or near ground potential.

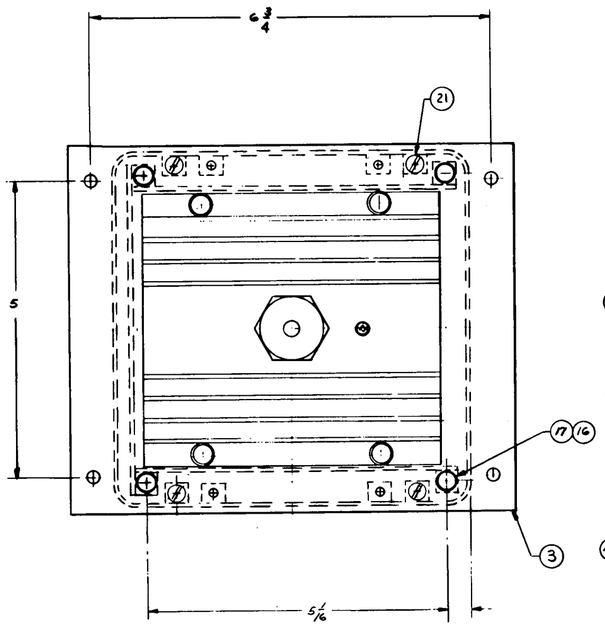
CONCLUSIONS

The feasibility of developing a solid-state circuit breaker and transfer switch to operate in a 270-V 15-A dc circuit has been established. The technology of SCR construction and circuit design to utilize these devices exists. Circuit breakers incorporating SCR switching elements have been built and tested and have performed the majority of the requirements imposed on them. The circuit breakers with their automatic trip and recycle capability as well as remote control can be interconnected to provide remote control transfer switches with overload protection.

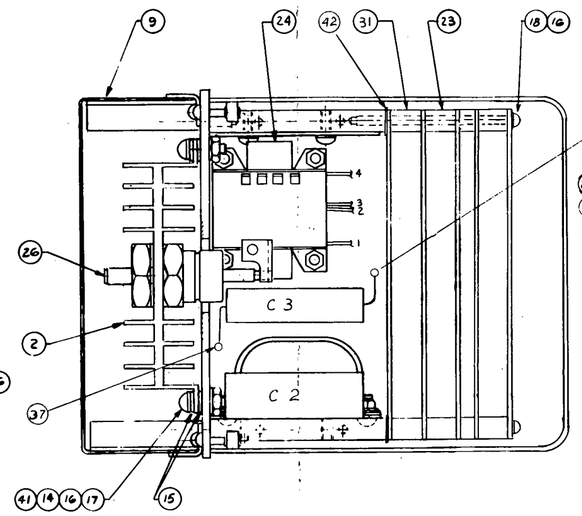
Solid-state switch gear having different current or voltage requirements as determined by aircraft or spacecraft electrical power systems analysis can be built within the capabilities of present-day SCR and transistor switching elements. If and when further advancements are made in power transistors or fully gate-controlled SCRs, simplified circuits can be built to achieve circuit breaker performance with less complexity and higher reliability. Improvements in the stability of Hall-effect devices or linear analog photoisolators could have significant advantages to offer to future solid-state circuit breaker improvement. Remote control by means of a computer can serve to replace much of the logic circuitry developed in this program and will, thereby, simplify the breaker design.

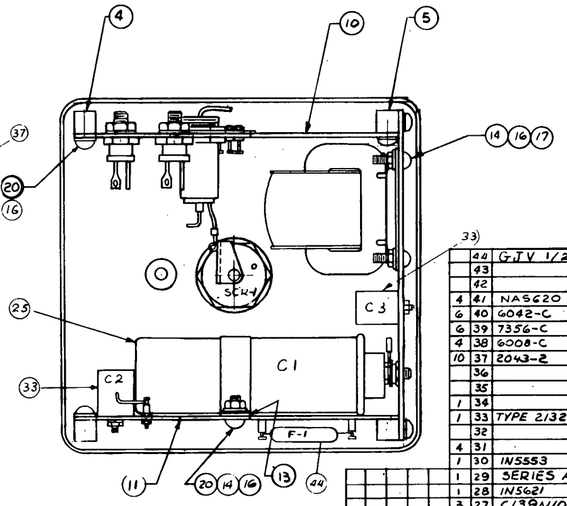
APPENDIX A

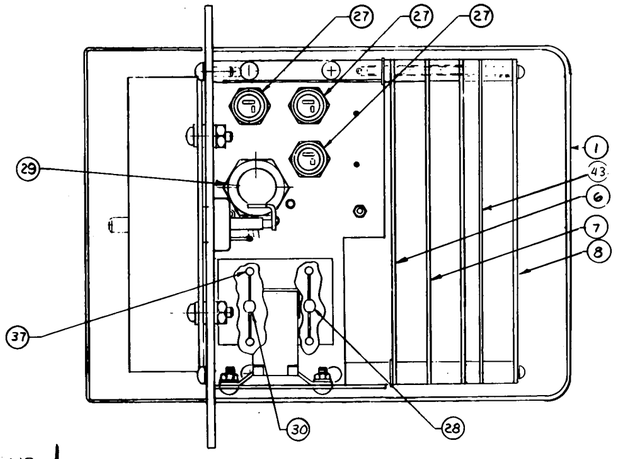
Figure	Title
42	Assembly, Solid-State Circuit Breaker
43	SSCB System Block Diagram
44	SSCB System Functional Diagram
45	SSCB System Wiring Diagram
46	SSCB Analog and Logic Schematic
47	SSCB Gate and Recharge Isolation Schematic Diagram
48	SSCB Power Supply Schematic Diagram



FRONT VIEW
COVER REMOVED







QUANTITY/DASH NO.	ITEM	PART NO.	SOME	DESCRIPTION	STOCK SIZE	MATERIAL OR VENDOR	MATERIAL SPECIFICATION	FINISH OR MFG CODE	CMS
	44	GJV 1/2		FUSE F1		BUSMAN			
	43			COPPER CLAD FIBRE	0.032				
	42			WASHER, FIAT FIBRE	#8, .50D				
4	41	NAS620		WASHER, FLAT	#8, .31 O.D. MAX				
6	40	6042-C		NUT, HEX	#6	GC ELECTRONICS			
6	39	7356-C		WASHER, LOCK, EXT.	#6	GC ELECTRONICS			
4	38	6008-C		SCREW, RD HD MACH	6-32 X 1/4 LG	GC ELECTRONICS			
10	37	2043-2		TERMINAL		CAMBION			
	36								
	35								
1	34								
1	33	TYPE 2/32		CAPACITOR C2,C3		SFEI			
	32								
4	31			SPACER					
1	30	IN5553		DIODE		SEMTECH			
1	29	SERIES A		SHUNT		T&M RESEARCH			
1	28	IN5621		DIODE		SEMTECH			
3	27	C130N/0M		SCR		GE			
1	26	C156M		SCR		GE			
1	25	28F5122		CAPACITOR C1		GE			
1	24			TRANSFORMER		MMC			
4	23	2117		SPACERS		W.H. SMITH			
1	22	K982706SP21		MTG STRAP		G.E.			
4	21	ZSP 10-1003		SCREW, CAPTIVE		ZERO MFG. CO.			
8	20	6014-C		SCREW, RD HD MACH	8-32 x 3/8 LG				
	19								
4	18			SCREW, RD HD MACH	8-32 x 1 1/2 LG				
12	17	6015-C		SCREW, RD HD MACH	8-32 x 1/2 LG	GC ELECTRONICS			
16	16	7358-C		WASHER, LOCK, EXT.	#8	GC ELECTRONICS			
8	15	2685		WASHER, SHOULDER		H.N. SMITH (NYLON)			
8	14	6043-C		NUT, HEX		GC ELECTRONICS			
1	13	15824003-003		PLATE, SPACER					
1	12	15824003-004		PLATE, MTG, TRANS.					
1	11	15824003-003		PLATE, MTG, CAP.					
1	10	15824003-002		PLATE, MTG, SHUNT					
1	9	15824002-009		COVER ASSY					
1	8	15824-035		COMPONENT BD ASSY					
1	7	15824-043		COMPONENT BD ASSY					
1	6	15824-046		COMPONENT BD ASSY					
2	5	15824003-007		ROD, SUPPORT					
2	4	15824003-006		ROD, SUPPORT					
1	3	15824003-001		MTG PLATE		.125 THK ALUM ALLOY			
1	2	15824003-008		HEAT SINK		THERMALLOY 6123			
1	1	Z9696 5 IN. DEEP		CASE		ZERO MFG. Co			

Figure 42.- Assembly, Solid-State Circuit Breaker

FOLDOUT FRAME 1

FOLDOUT FRAME 2

FOLDOUT FRAME 3

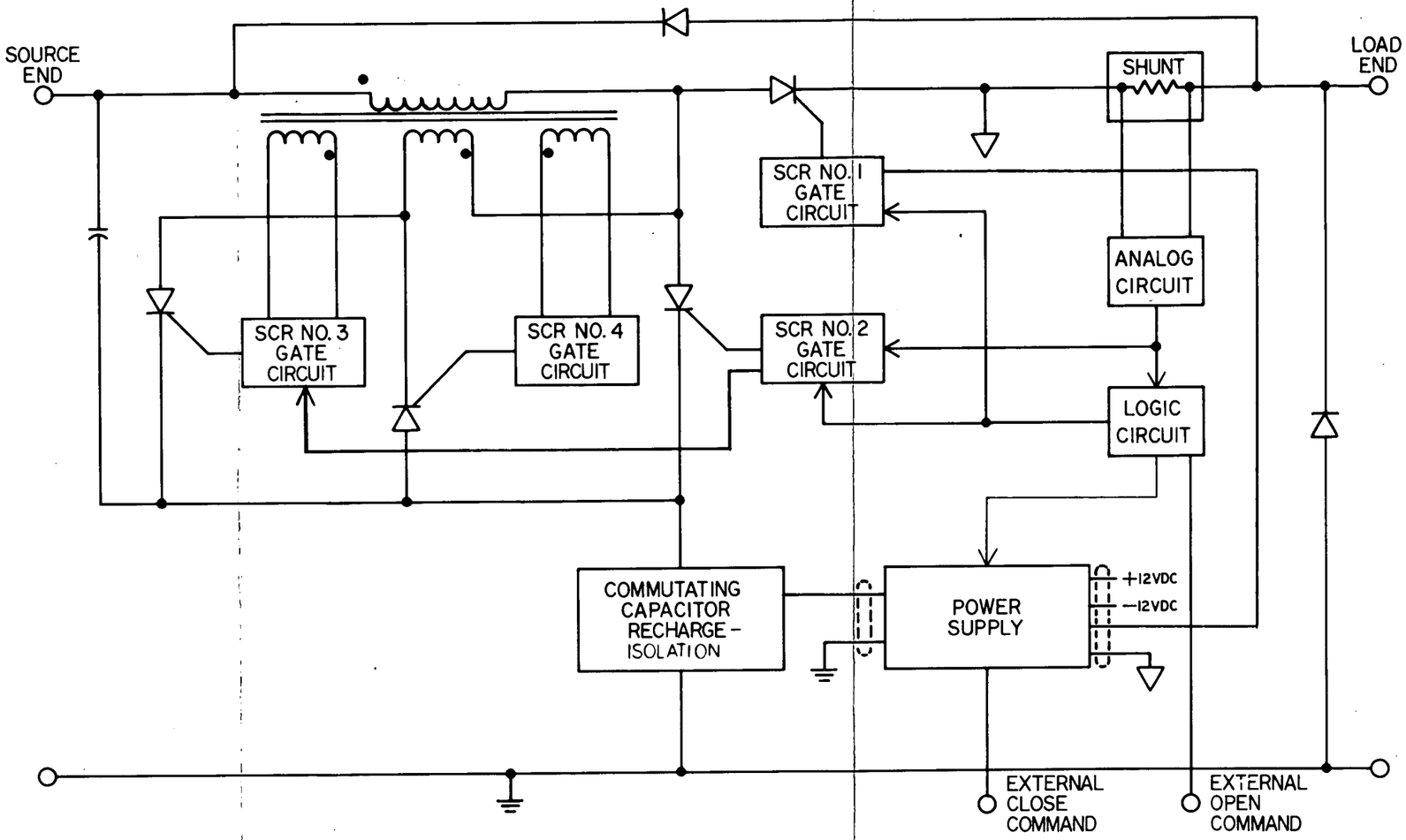
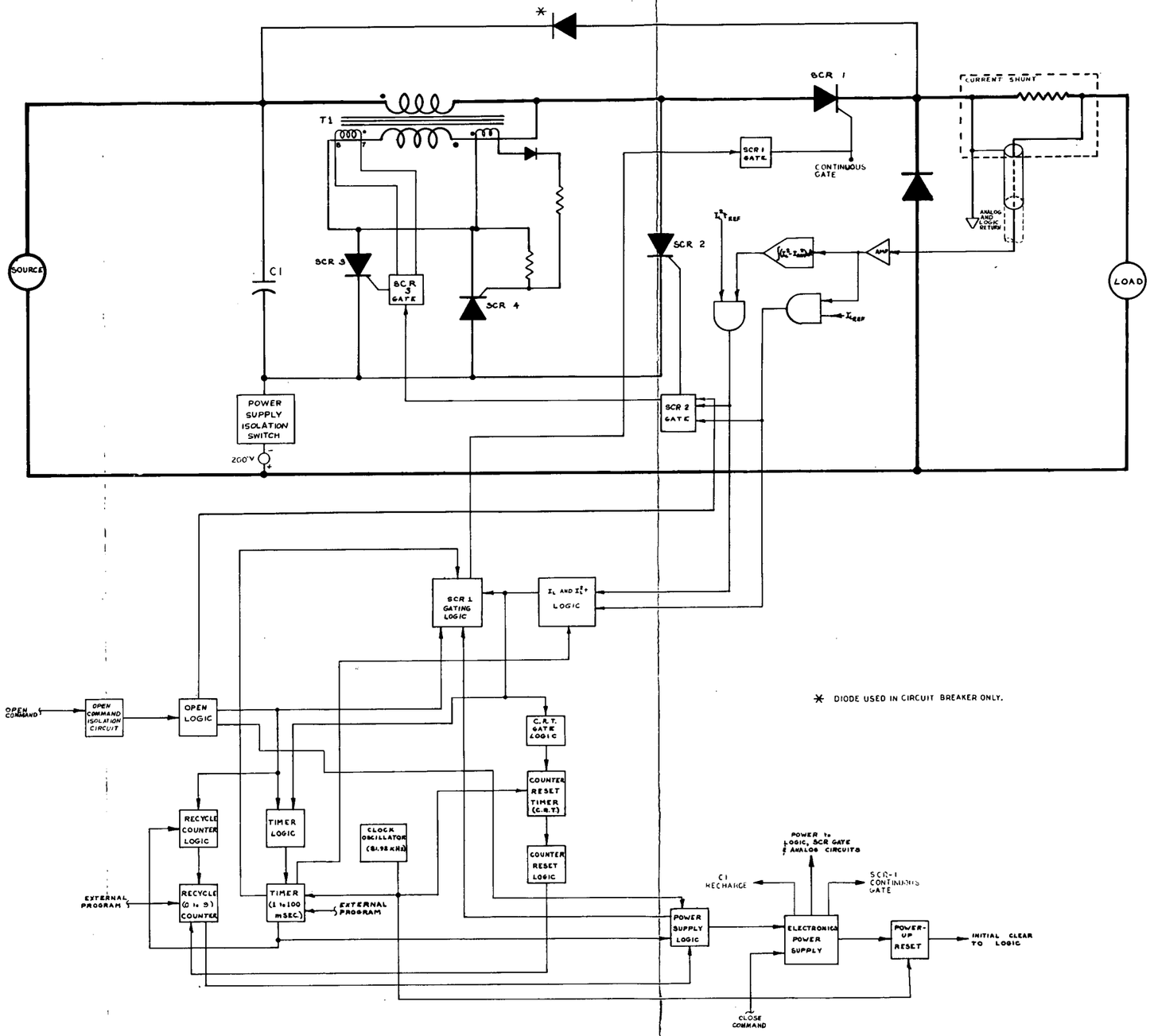


Figure 43.- Solid-State Circuit Breaker System Block Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

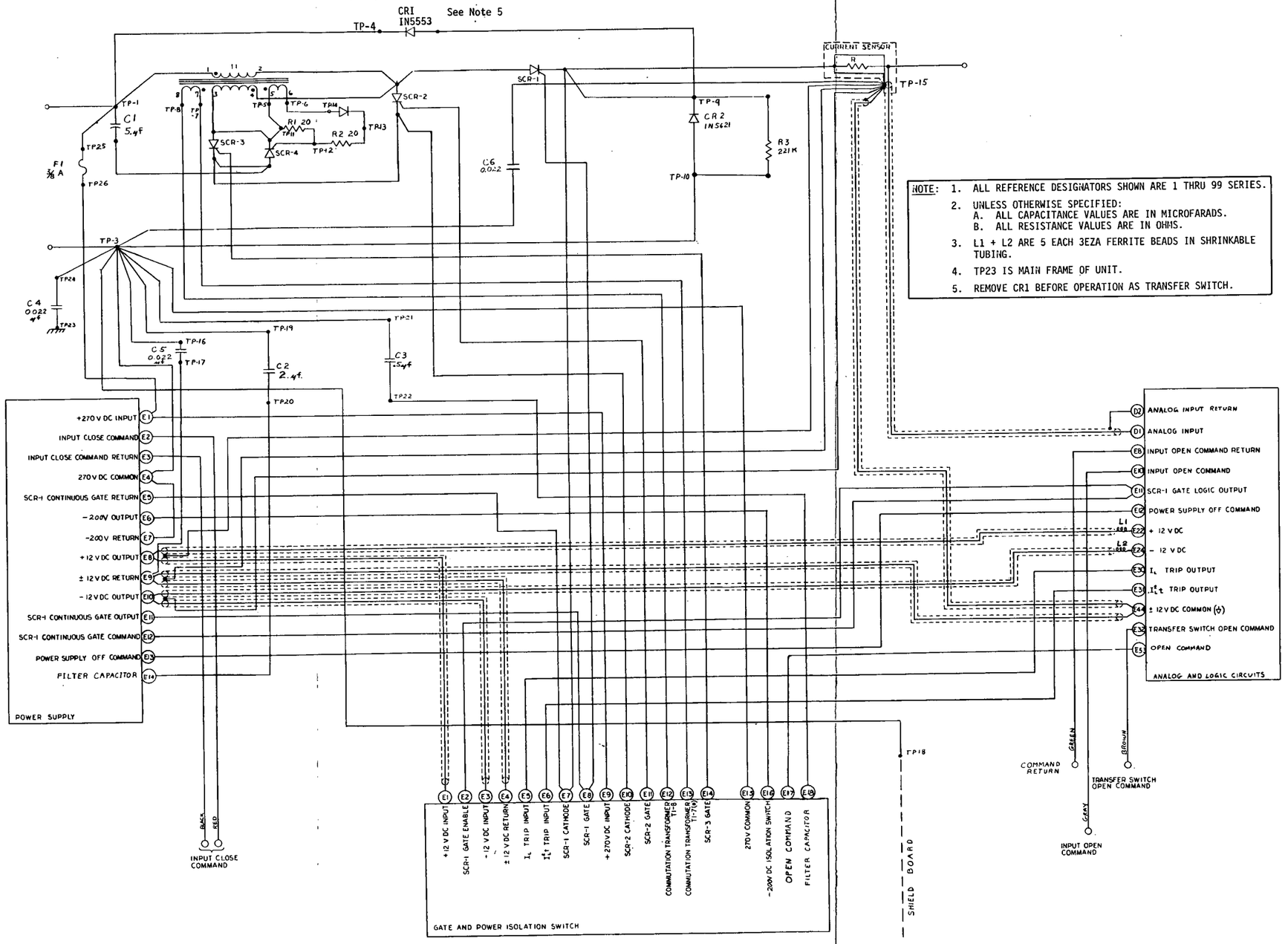


* DIODE USED IN CIRCUIT BREAKER ONLY.

Figure 44.- Solid-State Circuit Breaker Functional Diagram

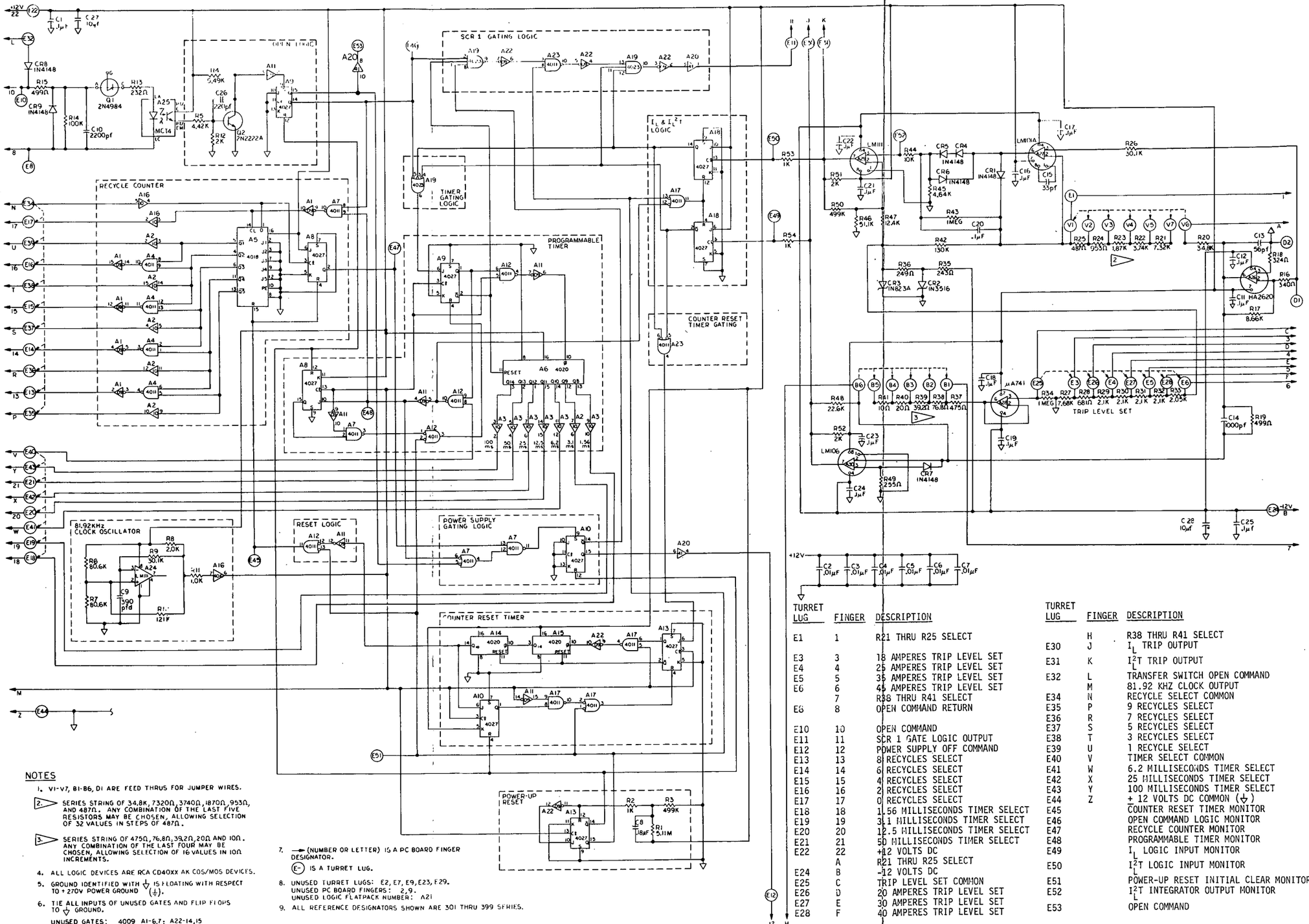
FOLDOUT FRAME 1

FOLDOUT FRAME 2



NOTE:
1. ALL REFERENCE DESIGNATORS SHOWN ARE 1 THRU 99 SERIES.
2. UNLESS OTHERWISE SPECIFIED:
   A. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
   B. ALL RESISTANCE VALUES ARE IN OHMS.
3. L1 + L2 ARE 5 EACH 3EZA FERRITE BEADS IN SHRINKABLE TUBING.
4. TP23 IS MAIN FRAME OF UNIT.
5. REMOVE CR1 BEFORE OPERATION AS TRANSFER SWITCH.

Figure 45.- Solid-State Circuit Breaker System Wiring Diagram



NOTES

1. V1-V7, B1-B6, D1 ARE FEED THRUS FOR JUMPER WIRES.
2. SERIES STRING OF 34.8K, 7320Ω, 3740Ω, 1870Ω, 953Ω, AND 487Ω. ANY COMBINATION OF THE LAST FIVE RESISTORS MAY BE CHOSEN, ALLOWING SELECTION OF 32 VALUES IN STEPS OF 487Ω.
3. SERIES STRING OF 475Ω, 76.8Ω, 39.2Ω, 20Ω AND 10Ω. ANY COMBINATION OF THE LAST FOUR MAY BE CHOSEN, ALLOWING SELECTION OF 16 VALUES IN 10Ω INCREMENTS.
4. ALL LOGIC DEVICES ARE RCA CD40XX AK COS/MOS DEVICES.
5. GROUND IDENTIFIED WITH ⏚ IS FLOATING WITH RESPECT TO +270V POWER GROUND (⏚).
6. TIE ALL INPUTS OF UNUSED GATES AND FLIP FLOPS TO ⏚ GROUND.

   UNUSED GATES: 4009 A1-6,7; A22-14,15
   4010 A16 9,10,11,12,14,15
   4011 A23-1,2,3,11,12,13
   4041 A20 11,12,13

7. —(NUMBER OR LETTER) IS A PC BOARD FINGER DESIGNATOR.
   (E-) IS A TURRET LUG.
8. UNUSED TURRET LUGS: E2, E7, E9, E23, E29.
   UNUSED PC BOARD FINGERS: 2, 9.
   UNUSED LOGIC FLATPACK NUMBER: A21
9. ALL REFERENCE DESIGNATORS SHOWN ARE 301 THRU 399 SERIES.

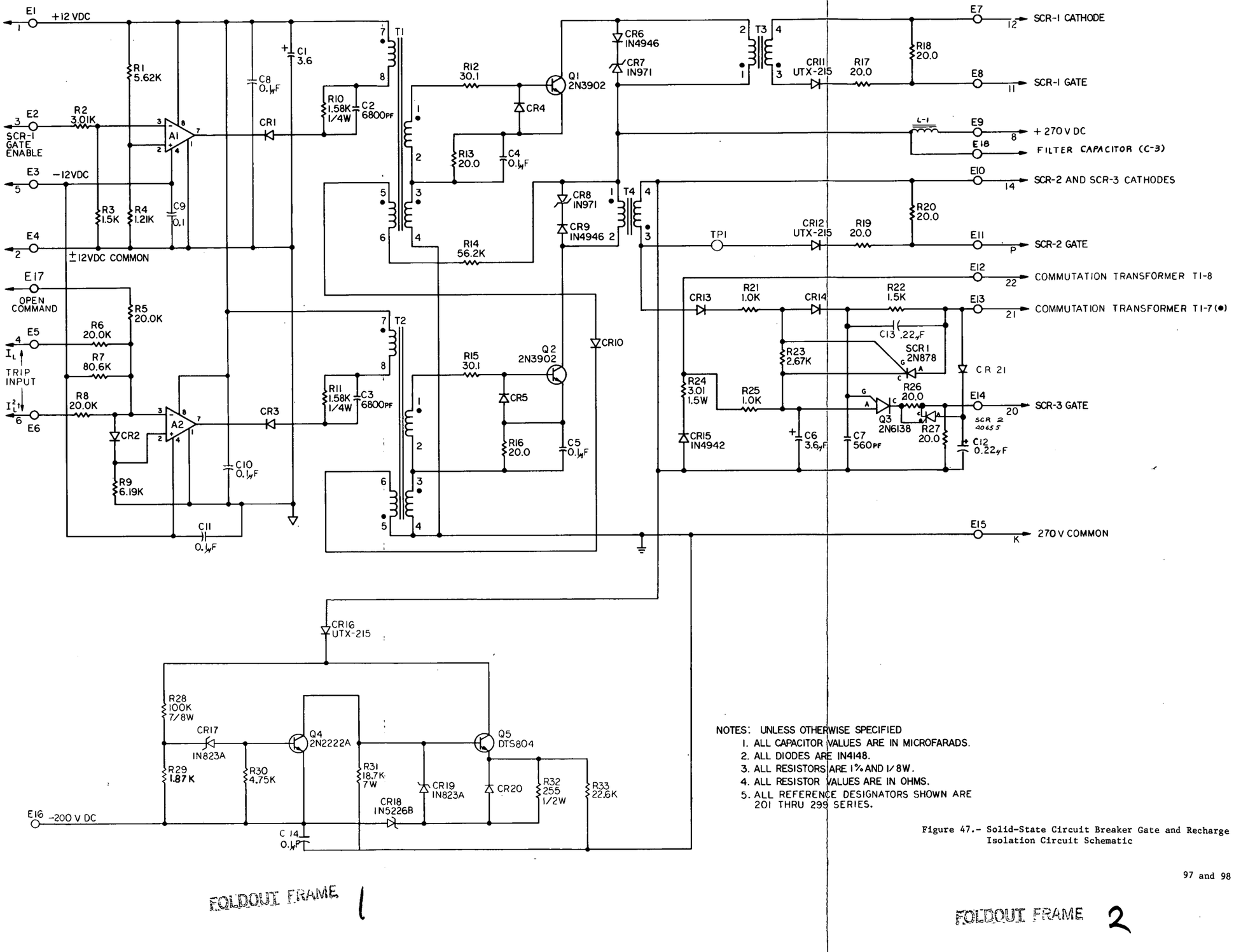
TURRET LUG	FINGER	DESCRIPTION
E1	1	R21 THRU R25 SELECT
E3	3	18 AMPERES TRIP LEVEL SET
E4	4	25 AMPERES TRIP LEVEL SET
E5	5	35 AMPERES TRIP LEVEL SET
E6	6	45 AMPERES TRIP LEVEL SET
	7	R38 THRU R41 SELECT
E8	8	OPEN COMMAND RETURN
E10	10	OPEN COMMAND
E11	11	SCR 1 GATE LOGIC OUTPUT
E12	12	POWER SUPPLY OFF COMMAND
E13	13	8 RECYCLES SELECT
E14	14	6 RECYCLES SELECT
E15	15	4 RECYCLES SELECT
E16	16	2 RECYCLES SELECT
E17	17	0 RECYCLES SELECT
E18	18	1.56 MILLISECONDS TIMER SELECT
E19	19	3.1 MILLISECONDS TIMER SELECT
E20	20	12.5 MILLISECONDS TIMER SELECT
E21	21	50 MILLISECONDS TIMER SELECT
E22	22	+12 VOLTS DC
	A	R21 THRU R25 SELECT
E24	B	-12 VOLTS DC
E25	C	TRIP LEVEL SET COMMON
E26	D	20 AMPERES TRIP LEVEL SET
E27	E	30 AMPERES TRIP LEVEL SET
E28	F	40 AMPERES TRIP LEVEL SET

TURRET LUG	FINGER	DESCRIPTION
	H	R38 THRU R41 SELECT
E30	J	I_L TRIP OUTPUT
E31	K	$I^2_L T$ TRIP OUTPUT
E32	L	TRANSFER SWITCH OPEN COMMAND
	M	81.92 KHZ CLOCK OUTPUT
E34	N	RECYCLE SELECT COMMON
E35	P	9 RECYCLES SELECT
E36	R	7 RECYCLES SELECT
E37	S	5 RECYCLES SELECT
E38	T	3 RECYCLES SELECT
E39	U	1 RECYCLE SELECT
E40	V	TIMER SELECT COMMON
E41	W	6.2 MILLISECONDS TIMER SELECT
E42	X	25 MILLISECONDS TIMER SELECT
E43	Y	100 MILLISECONDS TIMER SELECT
E44	Z	+ 12 VOLTS DC COMMON (⏚)
E45		COUNTER RESET TIMER MONITOR
E46		OPEN COMMAND LOGIC MONITOR
E47		RECYCLE COUNTER MONITOR
E48		PROGRAMMABLE TIMER MONITOR
E49		I_L LOGIC INPUT MONITOR
E50		$I^2_L T$ LOGIC INPUT MONITOR
E51		POWER-UP RESET INITIAL CLEAR MONITOR
E52		$I^2_L T$ INTEGRATOR OUTPUT MONITOR
E53		OPEN COMMAND

Figure 46.- Solid State Circuit Breaker Analog and Logic Schematic

FOLDOUT FRAME 1

FOLDOUT FRAME 2

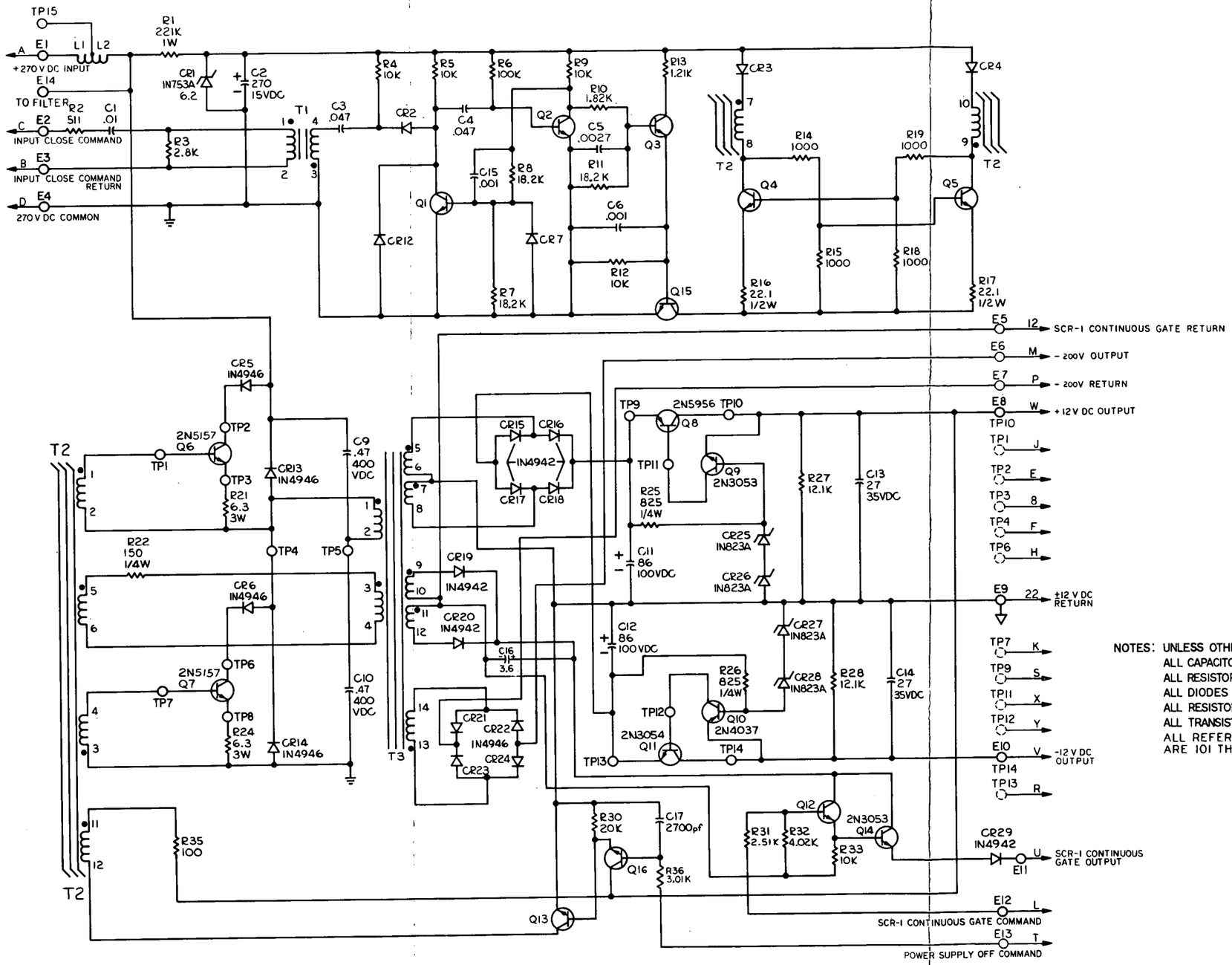


NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL CAPACITOR VALUES ARE IN MICROFARADS.
2. ALL DIODES ARE IN4148.
3. ALL RESISTORS ARE 1% AND 1/8W.
4. ALL RESISTOR VALUES ARE IN OHMS.
5. ALL REFERENCE DESIGNATORS SHOWN ARE 201 THRU 299 SERIES.

Figure 47.- Solid-State Circuit Breaker Gate and Recharge Isolation Circuit Schematic

FOLDOUT FRAME 1

FOLDOUT FRAME 2



NOTES: UNLESS OTHERWISE SPECIFIED.
ALL CAPACITOR VALUES ARE IN MICROFARADS.
ALL RESISTOR VALUES ARE IN OHMS.
ALL DIODES ARE IN4148.
ALL RESISTORS ARE 1/8W.
ALL TRANSISTORS ARE 2N2222A.
ALL REFERENCE DESIGNATORS SHOWN ARE 101 THRU 199 SERIES.

Figure 48.- Solid-State Circuit Breaker Power Supply Schematic

APPENDIX B

A copy of the test procedures, MCR-72-207, used in the formal test program performed under this contract is contained in Appendix B. Copies of the data sheets have been deleted.

TEST PROCEDURE

FOR

LOGIC CONTROLLED SOLID STATE CIRCUIT BREAKER

NASA CONTRACT NAS3-15824

Prepared by: E. Buchanan

Approved by: D. Waddington,
Program Manager

MARTIN MARIETTA AEROSPACE
DENVER DIVISION
DENVER, COLORADO 80201

Prepared for:

NASA LEWIS RESEARCH CENTER
CLEVELAND, OHIO 44135

CONTENTS

PART I
INTRODUCTION

A. TEST EQUIPMENT REQUIRED

Main dc Power Supplies	HP 6483C	2 each*
RF Interference Filter	Filtron FSR 202 or equivalent	1 each
Regulated dc Power Supply	EMC 200R or equivalent	1 each
Differential Digital Voltmeter	DANA 5600 or equivalent	1 each
DC Voltmeter, 0 to 500 V	Weston 901 or equivalent	1 each
DC Ammeter, 0 to 50 A	Weston 901 or equivalent	1 each
Oscilloscope	Tektroni 556 with Type 1A5 differential plug-in units	1 each
System Test Equipment	Solid-state circuit breaker system test tool	1 each*
Auxiliary Load Bank	2.5-A, 250-V	1 each
Dual dc Power Supply	HP 6255 A or equivalent	1 each

B. DRAWING REFERENCES

Drawing title	Figure
System Schematic, Test Tool	53
Life Test Schematic, Test Tool	54
Load Bank Schemtaic, Test Tool	55
SSCB System Wiring Diagram	45

*Indicates supplied equipment.

C. DESCRIPTION, SYSTEM TEST ASSEMBLY (Figures 53 thru 55)

The system test assembly is composed of the following front-panel units housed within a six-foot enclosed cabinet:

1. Load Bank Assembly: Group 1 and Group 2 load banks are housed within this unit. Additionally, a resistance of approximately 100 ohms is also included for providing a static load to the main dc power supply input of approximately 2.5-A for the purpose of providing a minimum load to the main dc power supplies.

2. Load Select Panel: This unit contains Switches S301 through S307 (Load Group 1 Select switches), Switches S401 through S406 (Load Group 2 Select switches), and Transient Load Switches S407 and S408. The transient loads associated with S407 and S408 are incorporated within the Group 2 load bank.

   Load Group 1 is used for continuous-duty load while Load Group 2 resistors are used for intermittent duty loads to simulate selectable overload conditions. The transient loads associated with S407 and S408 are included for the purpose of providing short duration higher current loads to simul8te high current conditions for certain ultimate trip tests.

3. SSCB Mounting Panel: This panel provides for mounting and connecting one test circuit breaker. Front panel Terminals E501, E503, and E502 provide connection points for the power leads to the test breaker (+270-Vdc Input, 270-Vdc Common, and +270-Vdc Output, respectively). Five additional front panel terminals provide connection points for the command leads to the test breaker.

   The test breaker is inserted into the retaining guides with connecting leads to the right, as the operator faces the test assembly cabinet. Test breaker leads, grouped in two cables, are connected to front panel terminals as follows. TRANSFER FUNCTION RETURN is common with OPEN COMMAND RETURN, within the test breaker.

Lead function	Wire size	Wire color	Terminal No.
+270-Vdc Input	16	Yellow	E501
270-Vdc Common	16	Green	E503
270-Vdc Output	16	Black	E502
CLOSE Command (+)	22	Red	E505
CLOSE Command Return (-)	22	Black	E504
OPEN Command (+)	22	Gray	E506
OPEN Command Return (-)	22	Green	E508
Transfer Function	22	Brown	E507

Switch S514 on the SSCB mounting panel provides the means for connecting the capacitor bank mounted on the same panel to Terminals E501 and E503 (+270-Vdc Input and 270-Vdc Common, respectively). This switch should remain closed for all testing except the overvoltage transient tests, during which this switch should be opened.

4. Auxiliary Power Supplies: Two blank panels are provided to cover positions for auxiliary power supplies, which are not supplied. One power supply provides 150-Vdc for overvoltage transient tests and may be connected to the (+) and (-) 150-V terminals inside the SYSTEM TEST ASSEMBLY cabinet. These terminals are colored red and black, respectively.

   The other power supply provides ±12 Vdc for operation of control circuits within the SYSTEM TEST ASSEMBLY. Connections are provided within the cabinet and are identified. Utility receptacles for 115-Vac power for the auxiliary power supplies are also provided within the SYSTEM TEST ASSEMBLY cabinet.

5. Main Control Panel: This unit, containing control and switching circuitry, is equipped with the following controls and indicators.

   115 Vac Power Switch S505: This switch controls 115 Vac, 60 Hz power to the SYSTEM TEST ASSEMBLY cabinet, enabling utility outlets, blowers, and other 60-Hz circuitry. The associated fuse and indicator lamp are mounted adjacent to this switch.

±12-Vdc Power Switch S506: This switch is used for application of 12 Vdc power from the associated auxiliary power supply to logic and other control circuitry within the SYSTEM TEST ASSEMBLY cabinet.

Manual CLOSE Command Switch S507: This switch applies manual close command signal to the test breaker through front panel Terminals E504 and E505.

Manual OPEN Command Switch S508: This switch applies manual open command signal to the test breaker through front panel Terminals E508 and E506.

Life Cycle Select Switch S509: Three positions are utilized for selection of 100, 200, or 500 cycles of overload operation at the approximate rate of four cycles/minute. Associated logic is reset for reinitiation of count cycle by opening and reclosing ±12-Vdc Power Switch S506.

AUTO Cycle Enable Switch S510: Closure of this switch activates the 1/3-rpm Cam Drive Motor. Resultant cam operation provides the following sequence of events.

a. Approximately 600 msec following cam closure, overload SCR 501 is fired, connecting Group 2 loads to the test breaker output.

b. Approximately 1800 msec following the firing of overload SCR501, a Close Command is generated which appears at front panel Terminals E504 and E505. The test breaker is thus closed and remains in this state until overload SCR501 is again fired during the following cam cycle.

Internal logic provides cycle count and automatic suspension of close command and SCR501 gate signals as determined by Life Cycle Select Switch S509.

Single-Cycle Enable Switch S511: This switch provides for single cycle overload operation for the test breaker as follows:

a. The test breaker is closed by closing Manual CLOSE Command Switch S507.

b. Single Cycle Enable Switch S511 is placed to CLOSED position.

c. Approximately 600 msec later, overload SCR501 is fired, applying Group 2 load to the test breaker.

d. Approximately 1800 msec following overload, a close command is again applied to the test breaker through front panel Terminals E504 and E505.

e. The test breaker is now opened with Manual OPEN Command Switch S508.

f. Single Cycle Enable Switch S511 is now opened, completing the CLOSE-OVERLOAD-TRIP AUTO-RECLOSE MANUAL-REOPEN cycle

SSCB Bypass-Load Group 1 Switch S502: The function of this switch is to connect Load Group 1 loads (Switches S301 through S307) directly to the +270 Vdc main power, principally for load bank dc current calibration with the test breaker disconnected.

SSCB Bypass-Load Group 2 Switch S501: The function of this switch is to connect Load Group 2 loads (Switches S401 through S408) directly to the +270 Vdc main power, principally for dc current calibration of Load Group 2 static loads, with the test breaker disconnected.

SSCB Connect-Load Group 1 Switch S504: Closure of this siwtch connects all Group 1 loads (selected by Switches S301 through S307) directly to the output terminals of the test breaker.

SSCB Connect-Load Group 2 Switch S503: Closure of this switch connects all selected group 2 loads (Switches S401 through S408) directly to the output terminals of the test breaker.

Note: Switches S501, S502, S503, and S504 discussed above should not be used to make or break Group 1 or Group 2 load bank loads while the system test equipment is energized with 270-V main dc power.

Transient Enable Switch S201: This switch is for the purpose of providing overvoltage transient pulse to the test breaker. This switch should normally be maintained in the Left-Hand (Disabled) position. For overvoltage transient tests of the test breaker, the following sequence of operations is used.

a. The auxiliary 150-Vdc power supply output is connected to Terminals E204 (black) and E205 (red), in the inside rear of the system test cabinet. These terminals are marked 150 Vdc, and are color coded, black being negative (-), and red being positive (+).

b. The 150-Vdc auxiliary supply may be energized from one of the utility receptacles within the system test cabinet. With the 115-Vac Power Switch S505 in the ON position, and with the 150-Vdc auxiliary supply energized, the voltage output of this power supply is set to the desired transient pulse voltage, nominally 150 Vdc.

c. With the test breaker installed, with the main dc power supplies energized, and with 270-Vdc main power applied to the Power Input terminals to the test breaker, Capacitor C201 is charged to the auxiliary dc power supply voltage.

d. Operation of TRANSIENT ENABLE SWITCH S201 to the Right-Hand (Fire) position causes SCR201 to fire, effectively connecting Capacitor C201 voltage across Diode CR202 and in series with the main dc voltage applied to the input power terminals to the test breaker.

e. Subsequent operation of switch S201 to the Left-Hand (Disabled) position bypasses the overvoltage transient circuitry and allows Capacitor C201 to recharge to the auxiliary power supply voltage.

Note: Switch S514, located on the SSCB mounting panel, should be opened as described in Paragraph C.3, during overvoltage transient tests, and should remain closed at all other times.

D. INITIAL CHECKOUT, SYSTEM TEST ASSEMBLY

1. Install the utility ac power cable provided, connecting the cable to J505 ac power connector located on the connector panel mounted on the rear of the equipment cabinet. Install auxiliary power supplies as described in Paragraph C.4.

2. Prior to connection of the auxiliary power supplies, energize the 150-Vdc power supply, setting the voltage control of the 150-Vdc supply to 150 V. It is suggested that this control be locked in position. Deenergize the 150-Vdc power supply and connect to the system test assembly, as described above.

3. Following the procedure of Paragraph 2, energize the ±12-Vdc dual auxiliary power supply, setting both channels to 12-Vdc output. Set the current limit of the positive supply to allow for approximately 50-mA load. Set the current limit of the negative supply to allow for approximately 5-mA load. Deenergize this auxiliary power supply and connect to the system test assembly, as described. It is recommended that the controls for this power supply also be locked in set position.

4. Set all front panel switches on the System Test Assembly to OPEN or DISABLED position. Connect the 115-Vac power cable to an appropriate source of 60-Hz power. Energize ac Power Switch S505. Check operation of all cabinet blowers. The ac Power indicator lamp should be illuminated.

5. Close 12-Vdc Power Switch S506. Observe (+) and (-) 12-Vdc voltage and current. The +12-V supply should be negligible, about 3 mA.

6. Connect the vertical input of an oscilloscope to Front Panel Terminals E504 (-) and E505 (+). Close Manual CLOSE Command Switch S507. The CLOSE Command signal should rise to approximately +12 V. Return S507 to OPEN position.

7. Connect the vertical input of an oscilloscope to Front Panel Terminals E506 (-) and E508 (+). Depress OPEN Command Switch S508. The OPEN Command signal should rise to approximately +10 V. Allow S508 to return to OPEN position.

8. Set Life Cycle Select Switch S509 to 100-cycle position. Reconnect the oscilloscope vertical input to Front Panel Terminals E504 and E505 as in paragraph 6. Close Auto Cycle Enable Switch S510. Observe the red indicator lamp, which should become illuminated several seconds following closure of S510. This lamp indicates cam switch operation, which should cycle at the rate of approximately 4 cycles per minute. Approximately 2.4 s following cam closure, a +12-V ON Command pulse should be observed between Terminals E504 and E505. Return S510 to OPEN position.

9. Close Single Cycle Enable Switch S511. Approximately 2.4 s following this closure, a single CLOSE Command pulse should again be observed between Terminals E504 and E505 as outlined in paragraph 8. Return S511 to OPEN position.

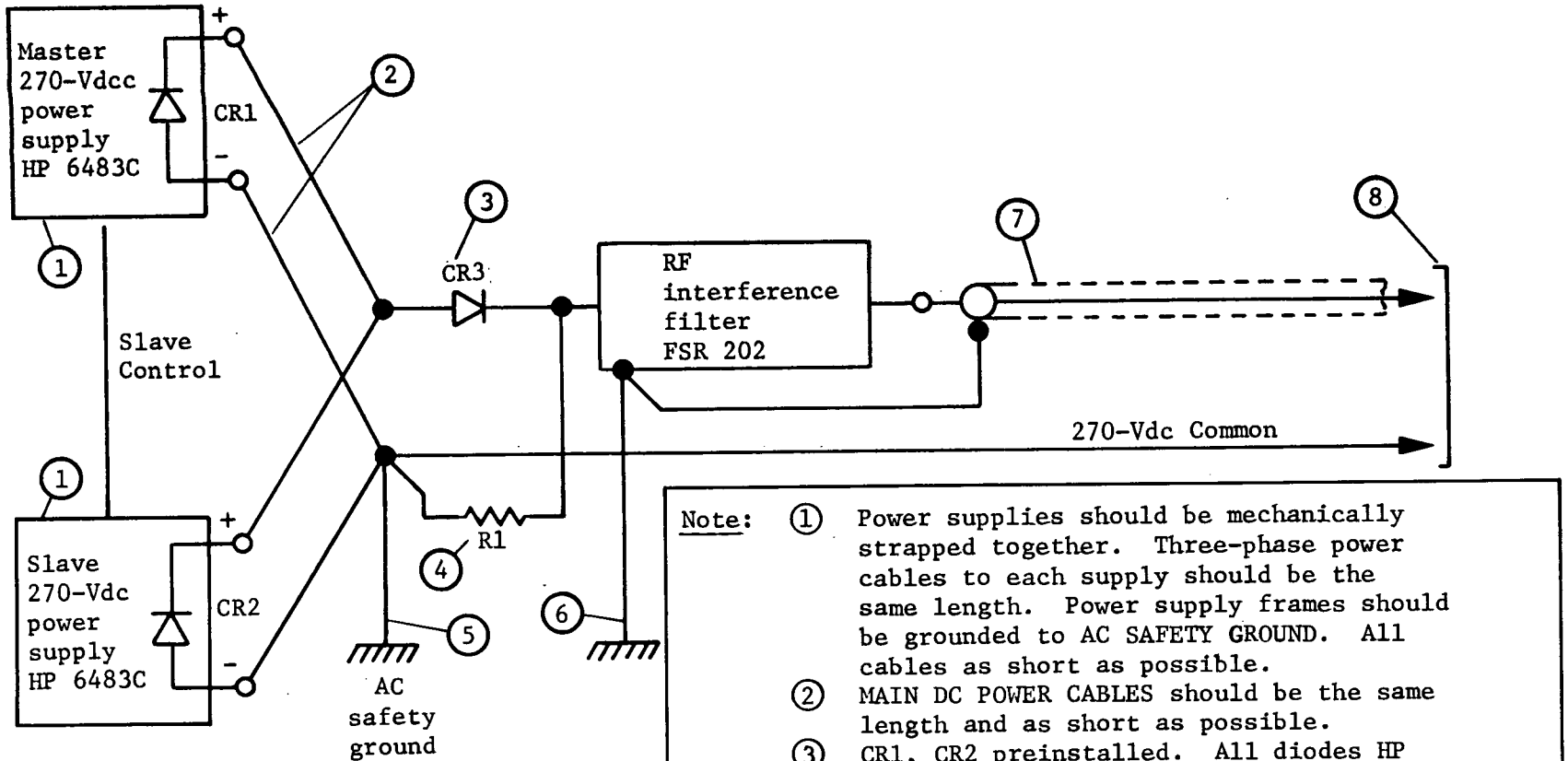
E. INITIAL CHECKOUT, MAIN DC POWER SUPPLIES

Connect the HP 6483C power supplies to an appropriate source of three-phase power as described in the respective equipment manuals. Follow individual installation and checkout precedures for these power supplies thoroughly and carefully prior to interconnection with the Logic Controlled Solid-State Circuit Breaker System Test Assembly. Particular attention should be directed toward correct phase balance settings for these supplies. It is recommended that complete familiarization with the equipment manuals be effected prior to installation and initial tests.

It is additionally important that close attention be directed toward transient damping control settings of these supplies prior to slaving together, to reduce the tendency toward mutual self-oscillation and undue output voltage ringing when these supplies are slaved together under conditions of application and interruption of higher current loads.

Following initial checkout of the unslaved power supplies, slave these supplies together as recommended in the equipment manuals. It is recommended that periodic monitoring of the phase balance of these supplies be accomplished within at least weekly intervals following initial adjustment. Install isolation diode assembly and the RF interference filter for decoupling purposes as described in figure 49. Conduct operational checkouts of these slaved power supplies in accordance with the procedures outlined in the equipment manuals.

Set the current limit control of the slaved power supplies to approximately 40 A (approximately 20 A each) after foregoing tests have been completed, to retard tendency toward mutual self-oscillation at higher current loads. Disconnect main power to these supplies in preparation for overall system integration.



Note:

① Power supplies should be mechanically strapped together. Three-phase power cables to each supply should be the same length. Power supply frames should be grounded to AC SAFETY GROUND. All cables as short as possible.

② MAIN DC POWER CABLES should be the same length and as short as possible.

③ CR1, CR2 preinstalled. All diodes HP supplied. CR3, furnished on heat sink, should be installed close to and at mid-point between supplies. Insulate heat sink.

④ Install auxiliary load bank: 100 ohms, 1 kW.

⑤ DC GROUND should be connected directly to AC SAFETY GROUND, cable as short as possible.

⑥ RFI FILTER should be mounted on mechanical strapping between supplies, case grounded to power supply frames.

⑦ Use RG-8/U coaxial cable, 29 to 50 foot length.

⑧ 270 V DC MAIN POWER OUTPUT to Auxiliary Mechanical Circuit Breaker, S513.

Figure 49.- Interconnection of Main Power Supplies

F. INTEGRATION AND CHECKOUT, COMPLETE TEST SYSTEM

Install auxiliary circuit breaker or disconnect, S513, if desired, at the System Test Assembly cabinet as shown in figure 50. This disconnect is used principally as a means to remove 270-Vdc main power from the system test cabinet, if such is desired for reasons of safety. Operation of this disconnect is not otherwise referred to within the System Test Procedure.

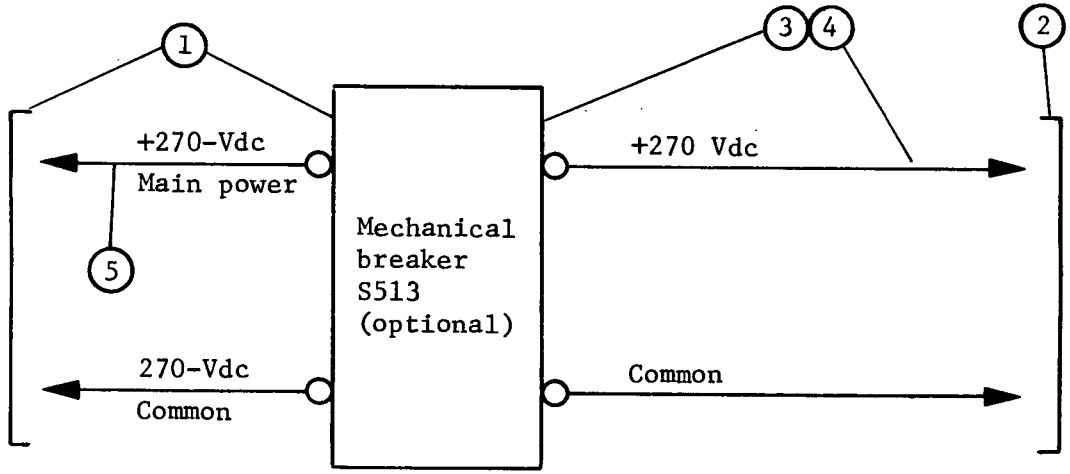
Using appropriate cables, connect the output side of this disconnect to the System Test Assembly, connecting this cable to Connector J504 located on the rear connector panel of the test assembly cabinet.

Connect the input side of the disconnect S513 to the output of the RF Interference Filter as described in figure 50. Particular attention should be directed toward appropriate grounding as shown in figure 49, and toward minimization of ground loops. Connect an auxiliary 100 ohm load bank (not supplied) as shown in figure 49.

Connect the 115 Vac Input of the System Test Assembly cabinet to one phase of the three-phase power source at the input to the main dc power supplies, using cables as provided. Refer to figure 51 and 52 for this connection. Ascertain that all disconnects, power switches on the main dc power supplies, power switches on the auxiliary power supplies, and front panel switches on the System Test Assembly are in the DISABLED or DEENERGIZED position. Initial checkout of the integrated test system will now follow.

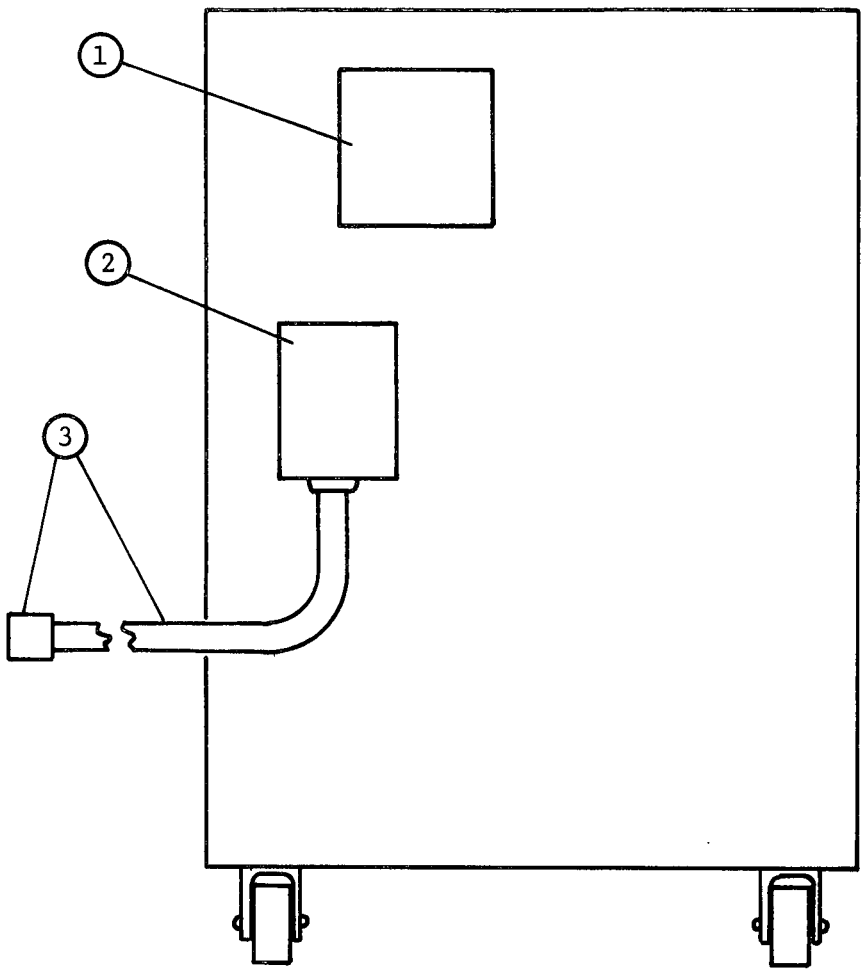
> WARNING: LARGE CAPACITOR BANKS EXIST ACROSS THE MAIN DC POWER BUS, BOTH WITHIN THE MAIN DC POWER SUPPLIES AND WITHIN THE SYSTEM TEST ASSEMBLY CABINET. DUE SAFETY PRECAUTIONS SHOULD BE EXERCISED TO MAKE CERTAIN THAT ALL EQUIPMENT IS DEENERGIZED AND THAT ALL CAPACITORS ARE DISCHARGED PRIOR TO MAKING CONNECTIONS, REMOVING CONNECTIONS, OR OTHERWISE PHYSICALLY WORKING WITHIN THE TEST SYSTEM.

Using the SHUNT SIGNAL OUTPUT CABLE provided, connect this cable to J503 within the System Test Cabinet. Route this cable around to the front of the test cabinet to provide differential current signals to the oscilloscope and other measuring equipment. (Refer to figure 55.) Note that the R509 shunt is used for measuring both Group 1 and Group 2 load currents, combined; the R510 shunt is used for measuring Group 2 load bank current only. THESE SHUNTS MUST BE READ WITH DIFFERENTIAL INPUT EQUIPMENT in order to minimize ground loop errors in measurements. Table XI and XII provide shunt calibration data for R509 and R510.



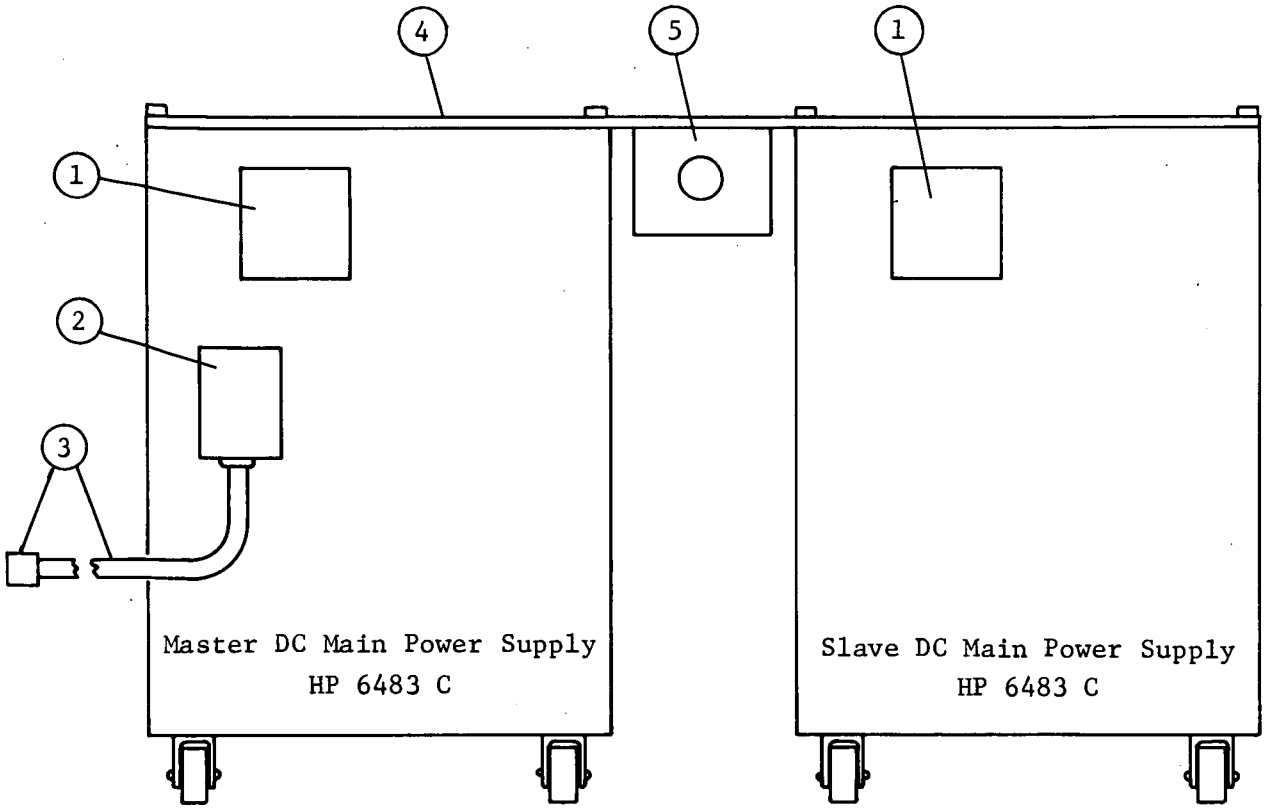
NOTE:
1. 270 MAIN DC POWER CABLE FROM MAIN DC POWER SUPPLIES (See figure 49). Positive lead should be RG-8/U coaxial cable, or equivalent, 20 to 50 ft leng. S513 Auxiliary Circiut Breaker, or equivalent disconnect rated to handle 50 A minimum, 300 Vdc minimum. See figure 49 for grounding instructions, shielded dc cable.
2. 270 VDC CABLE to SYSTEM TEST ASSEMBLY CABINET. Cable should be as short as possible, with S513, if used, as close to SYSTEM TEST ASSEMBLY CABINET as possible.
3. Every effort should be made to prevent AC and DC GROUND LOOPS in primary power system.
4. Avoid bypass coupling of power leads around decoupling circuits of figure 49.
5. 270 VDC SHIELDED CABLE TO BE GROUNDED AT RFI FILTER END ONLY, see figure 49.

Figure 50.- Connection of Auxiliary Circuit Breaker for Personnel Safety



Note: ① Rear panel connection point, 208-Vac, 3-phase power.
② Auxiliary instrument fuse box, 115-Vac utility power
③ Auxiliary 115-Vac power cable for connection, system test assembly cabinet 115-Vac, 60-Hz power.

Figure 51.- Undetailed Sketch, HP 6483C Master Power Supply, Location of Auxiliary 115-Vac Outlet



Note:
(1) See figure 51.
(2) See figure 51.
(3) See figure 51.
(4) Mechanical strapping bar, typical, two places.
(5) Recommended location, EMI filter.

Figure 52.- Sketch, Rear View Main DC Power Supply Assembly

TABLE XI.- SHUNT CALIBRATION DATA, R509
RESISTANCE = 0.005212 OHMS

Load current, A	Output, mV	Load current, A	Output, mV
1	5.212	26	135.512
2	10.424	27	140.724
3	15.636	28	145.936
4	20.848	29	151.148
5	26.060	30	156.360
6	31.272	31	161.572
7	36.484	32	166.784
8	41.696	33	171.996
9	46.908	34	177.208
10	52.120	35	182.420
11	57.332	36	187.632
12	62.544	37	192.844
13	67.756	38	198.056
14	72.968	39	203.668
15	78.180	40	208.480
16	83.392	41	213.692
17	88.604	42	218.904
18	93.816	43	224.116
19	99.028	44	229.328
20	104.240	45	234.540
21	109.452	46	239.752
22	114.664	47	244.964
23	119.876	48	250.176
24	125.088	49	255.388
25	130.300	50	260.600

TABLE XII.- SHUNT CALIBRATION DATA, R510
RESISTANCT = 0.004966 OHMS

Load current, A	Output, mV	Load current, A	Output, mV
1	4.966	26	129.116
2	9.932	27	134.082
3	14,898	28	139.048
4	19,864	29	144.014
5	24.830	30	148.980
6	29.796		
7	34.762		
8	39.728		
9	44.694		
10	49.660		
11	54.626		
12	59.592		
13	64.558		
14	69.524		
15	74.490		
16	79.456		
17	84.422		
18	89.388		
19	94.354		
20	99.320		
21	104.286		
22	109.252		
23	114.218		
24	119.184		
25	124.150		

The BNC connectors on the output end of the above signal cable are marked in two pairs, PAIR 1 corresponding with shunt R509 and PAIR 2 corresponding with shunt R510. The low (negative) sides of these shunt outputs are marked with blue-banded BNC connectors. It is to be noted that these leads are SHIELDED leads, shields being connected to the shells of the BNC connectors.

With no test breaker mounted on the TEST BREAKER MOUNTING PANEL, connect an external voltmeter to front panel Terminals E501 (+270 Vdc) and E503 (270 Vdc COMMON). Connect an external ammeter (0 to 50 A dc) to front panel Terminals E501 (+) and E502 (-). Note that this ammeter will be at main dc power bus potential. Make certain that the output voltage control for the slaved main dc power supplies is set to the extreme CCW (minimum voltage) position.

CAUTION: THE MAIN DC POWER SUPPLIES ARE CAPABLE OF FRONT PANEL VOLTAGE CONTROL SETTINGS UP TO 500 VDC. VOLTAGES IN EXCESS OF 300 V MAY BE CAPABLE OF UNDUE STRESS UPON COMPONENTS WITHIN THE SYSTEM TEST ASSEMBLY. WHENEVER SYSTEM DC MAIN POWER IS TO BE ENERGIZED OR DEENERGIZED, IT IS RECOMMENDED THAT THE FOLLOWING PROCEDURE BE UTILIZED.

ENERGIZE: Make certain that the output voltage control for the slaved main dc power supplies is set to the extreme CCW (minimum voltage) position. Switch both power supplies ON. Allow several seconds to elapse, then begin increasing output voltage control setting, observing the power supply panel meters. Increase output voltage to approximately 100 Vdc and then to approximately 150 Vdc, allowing both supplies time to stabilize and ascertaining that both supplies are sharing static load current (approximately 5 A total, as determined by the 100-ohm static bank in the system test assembly, and by the auxiliary 100-ohm load bank installed prior to initial system checkout). Following this stabilization, carefully increase the output voltage control setting to the desired operating voltage.

DEENERGIZE: Decrease the output voltage control setting until extreme CCW (minimum voltage) setting is attained. Deenergize the main dc power supplies by setting both ac power switches on the power supply front panels to the OFF position.

The following numbered steps pertain to operational checkout of the integrated test system. The test system is to be operated without a Test Breaker installed during this checkout phase.

1. Close auxiliary disconnect S513 if installed. Make certain that ALL other switches and disconnects are in OPEN, DE-ENERGIZED, or DISABLED position.

2. Close primary 3-phase ac power disconnects in preparation for energizing the main dc power supplies.

3. Close 115-Vac POWER SWITCH S505. System Test cabinet blowers should be energized.

4. Close 12-Vdc POWER SWITCH S506.

5. Connect the R509 shunt cables from J503 to either the differential input of an oscilloscope or DVM set to read 0 to 100 mV dc. This will allow shunt calibration comparison with the 0 to 50 A dc ammeter.

6. Set the following switches as indicated:

SSCB Bypass-Load Group 1	Switch S502	OPEN
SSCB Bypass-Load Group 2	Switch S501	OPEN
SSCB Connect-Load Group 1	Switch S504	CLOSED
SSCM Connect-Load Group 2	Switch S503	CLOSED
Auxiliary Capacitor Bank	Switch S514	CLOSED

7. Group 1 and Group 2 individual loads may now be selected (Switches S301 through S307 and S401 through S406, respectively) for individual load calibration at the desired main dc power voltage. The following steps are examples of the operational sequence used for this purpose.

   a. Select one or more individual Group 1 and/or Group 2 loads as determined by Switches S301 through S307 and Switches S401 through S406, respectively.

   b. ENERGIZE MAIN DC POWER SUPPLIES. Set output voltage to desired value, following procedure recommended in Section F.

   c. Group 1 and Group 2 combined load currents may now be read with both ammeter and Shunt R509.

   d. Using procedure recommended above, DEENERGIZE MAIN DC POWER SUPPLIES.

8. The same procedure, outlined in Section F.7, may be used for comparison of Load Group 2 shunt calibration (R510) with the dc ammeter. In this case, the other pair of leads from connector J503 can be used to read the shunt current (No. 2 pair of leads), in the same manner that R509 shunt current was previously read. R510 shunt is provided as an auxiliary shunt for monitoring Load Group 2 currents, and is not ordinarily used during operational tests of Solid-State Circuit Breakers.

9. The following sequence of operations is used to check the firing of Overload SCR501.

   a. With the MAIN DC POWER SUPPLIES DEENERGIZED, set the following switches as indicated--

SSCB Bypass-Load Group 1	Switch S502	OPEN
SSCB Bypass-Load Group 2	Switch S501	OPEN
SSCB Connect-Load Group 1	Switch S504	CLOSED
SSCB Connect-Load Group 2	Switch S503	OPEN

   b. Set Group 1 LOAD SELECT SWITCHES (S301 through S307) to provide approximately 10-A load at 243 Vdc as ascertained during load calibration outlined in Section F.7.

   c. Select one of the Load Group 2 LOAD SELECT SWITCHES S401 through S406 to provide a Group 2 load of approximately 3.5 A, in the same manner as outlined in paragraph b, above.

   d. Use Shunt R509 to monitor load current, as well as the 0 to 50 A dc ammeter.

   e. ENERGIZE MAIN DC POWER SUPPLIES. Adjust output voltage to approximately 243 Vdc. Load current as measured with the 0 to 50 A dc ammeter and with Shunt R509 should be at the level selected by GROUP 1 LOAD SELECT SWITCHES.

   f. CLOSE the SINGLE CYCLE ENABLE SWITCH S511. Approximately 600 ms following this closure, OVERLOAD SCR501 should fire, thus connecting Group 2 load.

   g. DEENERGIZE MAIN DC POWER SUPPLIES. Return SINGLE CYCLE ENABLE SWITCH S511 to DISABLED position.

h. ENERGIZE MAIN DC POWER SUPPLIES. Adjust output voltage to approximately 243 Vdc. Load current as measured with the 0 to 50-A dc ammeter and with Shunt R509 should again be at the level selected by GROUP 1 LOAD SELECT SWITCHES.

i. CLOSE the AUTO CYCLE ENABLE SWITCH S510. Approximately 600 ms following cam closure, OVERLOAD SCR501 should fire, thus connecting Group 2 load.

j. DEENERGIZE MAIN DC POWER SUPPLIES. Return AUTO CYCLE ENABLE SWITCH S510 to DISABLED position.

10. The following sequence of operations is used to check TRANSIENT OVERVOLTAGE FIRING test.

a. Connect the vertical input of an oscilloscope to front panel Terminals E501 (+270 Vdc) and E503 (270 Vdc COMMON).

b. Set the following switches as indicated:

SSCB Bypass-Load Group 1	Switch S502	OPEN
SSCB Bypass-Load Group 2	Switch S501	OPEN
SSCB Connect-Load Group 1	Switch S504	CLOSED
SSCB Connect-Load Group 2	Switch S503	OPEN
Auxiliary Capacitor Bank	Switch S514	OPEN
All Group 2 Load Select Switches		OPEN

c. Select GROUP 1 LOAD SELECT switches S301 through S307 to provide an approximate 10-A load at 270 VOLTS DC MAIN POWER SUPPLY VOLTAGE.

d. Energize the AUXILIARY 150-Vdc power supply, and set the output voltage to 150 Vdc.

e. Set the oscilloscope controls to monitor the 150-V transient across front panel Terminals E501 and E503. Remember that these terminals will be energized at the 270-Vdc level.

f. ENERGIZE THE MAIN DC POWER SUPPLIES. ADJUST OUTPUT VOLTAGE TO approximately 270 Vdc.

g. Set TRANSIENT ENABLE SWITCH S201 to RIGHT HAND (FIRE) position. Observe the 150-V transient occurrence on the 270-V front panel terminals.

h. Return SWITCH S201 to LEFT HAND (DISABLED) position.

i. DEENERGIZE the MAIN DC POWER SUPPLIES.

j. Close Switch S514 (Auxiliary Capacitor Bank).

11. The following sequence of steps will be utilized for PRE-OPERATIONAL TEST checkout of an installed TEST SOLID-STATE CIRCUIT BREAKER.

12. Set all switches on the SYSTEM TEST ASSEMBLY to OPEN or DISABLED position.

13. Make certain that ALL CAPACITOR BANKS have had ample time to discharge.

14. Install a TEST BREAKER on the SSCB MOUNTING PANEL as outlined in Section C.3. Reconnect an external voltmeter, for measuring the main dc power supply voltage input to the Test Breaker, between front panel Terminals E501 (+270 Vdc) and E503 (270 Vdc COMMON). MAKE CERTAIN THAT LEAD CONNECTIONS BETWEEN THE TEST BREAKER AND THE FRONT PANEL CONNECTION TERMINALS ARE CORRECT; INCORRECT CONNECTION COULD RESULT IN SEVERE DAMAGE TO THE TEST BREAKER.

15. In the event that it is desirable to use the external 0 to 50 A dc ammeter in series with the load output of the Test Breaker, this may be accomplished by connecting the +270 Vdc OUTPUT LEAD from the TEST BREAKER to the positive ammeter terminal. The negative terminal of the ammeter can now be connected to the front panel Terminal E502. Make certain that all connections are secure and well insulated from each other. WARNING: Meter is at +270 V.

16. Connect the leads corresponding to R509 shunt output (from Connector J503) to the differential input of an oscilloscope. Set the oscilloscope vertical gain to 20 mV/cm.

17. Set the following switches as indicated--

SSCB Bypass-Load Group 1	Switch S502	OPEN
SSCB Bypass-Load Group 2	Switch S501	OPEN
SSCB Connect-Load Group 1	Switch S504	CLOSED
SSCB Connect-Load Group 2	Switch S503	OPEN

18. In preparation for energizing the system, operate the following switches as indicated--

12 Vdc Power	Switch S506	CLOSED
115 Vac Power	Switch S505	CLOSED
Auxiliary Capacitor Bank	Switch S514	CLOSED

One individual load from Load Group 1 will now be selected for initial SSCB test--

Group 1 Load Select	Switch S301	CLOSED

19. ENERGIZE MAIN DC POWER SUPPLIES. CAREFULLY INCREASE OUTPUT VOLTAGE TO APPROXIMATELY 170 VDC.

20. CLOSE the CLOSE COMMAND SWITCH S507. A load current appropriate to the load selected should be read through Shunt R509 and the auxiliary 0 to 50 A ammeter, if used. Open the Test Breaker by depressing MANUAL OPEN COMMAND SWITCH S508. Indicated load current should cease.

21. CAREFULLY INCREASE MAIN DC POWER SUPPLY VOLTAGE TO APPROXIMATELY 200 V.

22. OPEN SWITCH S301.

23. CLOSE the MANUAL CLOSE COMMAND SWITCH S507. There should be no indicated load current. CLOSE SWITCH S301. Load current should be indicated, appropriate to the individual load selected by Switch S301.

24. OPEN SWITCH S301. Indicated load current should drop to zero. This test is to verify the existence of CONTINUOUS GATE applied to SCR1 of the Test Breaker.

25. CLOSE SWITCH S301. The load should be again indicated as before. OPEN the TEST BREAKER by depressing MANUAL OPEN COMMAND SWITCH S508.

26. DEENERGIZE MAIN DC POWER SUPPLIES.

27. CLOSE GROUP 1 LOAD SELECT SWITCHES S301 through S307, to provide a load of approximately 10 A at 243 V.

28. ENERGIZE MAIN DC POWER SUPPLIES. CAREFULLY INCREASE OUTPUT VOLTAGE TO APPROXIMATELY 243 V.

29. CLOSE MANUAL CLOSE COMMAND SWITCH S507. The Test Breaker should close, with a load current of approximately 10 A indicated. OPEN THE TEST BREAKER BY DEPRESSING MANUAL OPEN COMMAND SWITCH S508. Indicated load current should cease.

30. CLOSE ADDITIONAL GROUP 1 LOAD SELECT SWITCHES S301 through S307 to provide approximately 18-A load at 243 V. Use the S301 through S307 load calibration tables prepared in Section F, for determining desired S301 through S307 loads.

31. CLOSE MANUAL CLOSE COMMAND SWITCH S507. DO NOT RETURN THIS MANUAL CLOSE COMMAND SWITCH TO THE OPEN POSITION. The TEST BREAKER should trip at an I^2t rate, as determined by the load and by the number of reclosure cycles preset within the TEST BREAKER. The TEST BREAKER should remain open at the end of this recycle sequence.

32. DEENERGIZE THE MAIN DC POWER SUPPLIES. This completes the initial checkout of the TEST BREAKER prior to actual operational tests.

PART II
OPERATIONAL TEST PROCEDURE

1.0 INITIAL CONDITIONS FOR ALL TESTS, LIFE TESTS EXCLUDED

1.1 Set all switches, disconnects, and manual circuit breakers in OPEN or DISABLED position. Connect TEST SOLID-STATE CIRCUIT BREAKER as outlined in PART I, Paragraphs F.11 through F.15.

1.2 Set the following switches to the indicated positions--

12 Vdc Power	Switch S506	CLOSED
115 Vac Power	Switch S505	CLOSED

1.3 Calibrate the TRIP TIME INDICATOR integration circuit by injecting a pulse of at least +10 V amplitude and lengths of 50, 75, and 100 ms into Terminals E11 and E12 located on the front panel of the SYSTEM TEST ASSEMBLY. (Refer to figure 53). Record the voltage output of the integrator (OUTPUT TERMINAL "P", CONNECTOR J502) with a digital voltmeter. Fifty milliseconds should provide a nominal 2.5-V output. A nominal 5.0 V output should be provided by 100 ms.

1.4 Deenergize 115 Vac POWER SWITCH S505.

Note: Paragraphs 1.2, 1.3, 1.4 above should be omitted if no DATA ACQUISITION SYSTEM is used to record data during life tests. Switch S506 (12 VDC POWER) can be placed in CLOSED position throughout remainder of testing.

2.0 VOLTAGE DROP TEST

2.1 Set the following switches as indicated:

SSCB Bypass-Load Group 1	Switch S505	CLOSED
SSCB Bypass-Load Group 2	Switch S501	CLOSED
SSCB Connect-Load Group 1	Switch S504	OPEN
SSCB Connect-Load Group 2	Switch S503	OPEN

CAUTION: OPERATE THESE ABOVE LOAD GROUP SELECT SWITCHES ONLY WHEN THE MAIN DC POWER SUPPLIES ARE DE-ENERGIZED. NO FURTHER REFERENCE TO THIS PRE-CAUTION WILL BE MADE THROUGHOUT THIS TEST PROCEDURE.

2.2 Connect a differential dc voltmeter input to the current shunt output (R509) using the auxiliary test cable provided. Use the table provided for conversion of voltage readings to current values.

2.3 Connect the dc voltmeter between E501 and E503 to measure dc input voltage to the Test Breaker. Set voltmeter on appropriate range for measuring 270 Vdc.

2.4 Connect a differential dc voltmeter between E501 and E502 for measuring voltage drop across the Test Breaker. WARNING: These terminals will both be at 270-Vdc potential. An instrument with at least 300-V common mode capability must be utilized.

2.5

Switch	S513	Auxiliary Circuit Breaker	ON
Switch	S505	AC Power	ON

The System Test Equipment should be energized.

Switch	Main dc Power Supplies	OFF

Carefully increase the dc main power voltage to 270-Vdc.

2.6 Close GROUP 1 and GROUP 2 LOAD SELECT SWITCHES (S301 through S307 and S401 through S406, respectively) until a load current of approximately 15 A is obtained.

2.7

Switch	Main dc Power Supplies	OFF

Allow the 270-V main dc bus voltage to decay.

Switch	S502	SSCB Bypass-Load Group 1	OPEN
Switch	S501	SSCB Bypass-Load Group 2	OPEN
Switch	S504	SSCB Connect-Load Group 1	CLOSED
Switch	S503	SSCB Connect-Load Group 2	CLOSED

2.8 ENERGIZE THE MAIN DC POWER SUPPLIES. CAREFULLY INCREASE THE OUTPUT VOLTAGE TO 270 V.

2.9 CLOSE the MANUAL CLOSE COMMAND SWITCH S507. Verify that the TEST BREAKER has closed by observing load current. Readjust MAIN DC POWER SUPPLY VOLTAGE slightly to obtain 15-A load current.

2.10 Measure voltage drop between front panel Terminals E501 and E502. Record this forward voltage drop across TEST BREAKER.

2.11 OPEN the Test Breaker by depressing MANUAL OPEN COMMAND SWITCH S508. Verify that the Test Breaker has opened by observing load current.

2.12 DEENERGIZE MAIN DC POWER SUPPLIES. After all capacitors have discharged, disconnect test equipment defined in Paragraph 2.4 above.

3.0 I^2t TRIP TEST (TEST BREAKER SHOULD BE SET FOR 45-A ULTIMATE TRIP)

3.1 INITIAL CONDITIONS: All switches in OPEN or DISABLED position. MAIN DC POWER SUPPLIES DEENERGIZED. Set the following switches as indicated--

12 Vdc Power	Switch S506	CLOSED
115 Vac Power	Switch S505	CLOSED
SSCB Bypass-Load Group 1	Switch S502	CLOSED
SSCB Bypass-Load Group 2	Switch S501	CLOSED
SSCB Connect-Load Group 1	Switch S504	OPEN
SSCB Connect-Load Group 2	Switch S503	OPEN

3.2 REENERGIZE MAIN DC POWER SUPPLIES. Carefully increase the MAIN DC voltage to 270-V.

3.2.1 Maintaining input voltage at 270Vdc, select Group 1 and Group 2 loads (Switches S301 through S307 and S401 through S406, respectively) to obtain a load current of 18 A. Make certain that TRANSIENT LOAD SWITCHES S407 and S408 are in the OPEN position.

3.2.2 DEENERGIZE MAIN DC POWER SUPPLIES.

3.3 Remove R509 SHUNT OUTPUT from the differential voltmeter and reconnect these leads to the differential input of the oscilloscope. Set oscilloscope controls as follows--

Vertical	20 mV/cm
Horizontal	10 ms/cm
Trigger	Internal
Sweep Mode	Single Sweep

Prepare to photograph current waveform.

3.4 Set the following switches as indicated--

SSCB Bypass-Load Group 1	Switch S502	OPEN
SSCB Bypass-Load Group 2	Switch S501	OPEN
SSCB Connect-Load Group 1	Switch S504	CLOSED
SSCB Connect-Load Group 2	Switch S503	CLOSED

3.5 REENERGIZE MAIN DC POWER SUPPLIES. Carefully increase the MAIN DC output voltage to 270 V, and ascertain that both supplies have stabilized with respect to current. CLOSE TEST BREAKER by CLOSING the MANUAL CLOSE COMMAND SWITCH S507. DO NOT RETURN THIS SWITCH TO OPEN (DOWNWARD) POSITION. The TEST BREAKER should close and automatically reopen, repeating this sequence depending on the number of recycle closures as set within the TEST BREAKER. Photograph waveform. Record data. DE-ENERGIZE THE MAIN DC POWER SUPPLIES. Return SWITCH S507 to DOWNWARD position.

3.6 Prepare for I^2t TRIP TEST, 243-V input, 35-A load current, as follows.

3.6.1 Set following switches as indicated--

SSCB Bypass-Load Group 1	Switch S502	OPEN
SSCB Bypass-Load Group 2	Switch S501	OPEN
SSCB Connect-Load Group 1	Switch S504	CLOSED
SSCB Connect-Load Group 2	Switch S503	CLOSED
Manual Close Command	Switch S507	DOWNWARD (DISABLED)

Make certain that TRANSIENT LOAD SWITCHES S407 and S408 are in OPEN position.

3.6.2 Using LOAD BANK CALIBRATION data as obtained in Part 1, Section F, operate GROUP 1 and GROUP 2 LOAD SELECT SWITCHES S301 through S307 and S401 through S406 to obtain a 35-A load for 243-V input.

3.7 Set oscilloscope controls as follow for current measurement:

Vertical	50 mV/cm
Horizontal	1.0 ms/cm
Trigger	Internal
Sweep Mode	Repetitive

3.8 REENERGIZE MAIN DC POWER SUPPLIES. CAREFULLY INCREASE MAIN DC VOLTAGE to 423 V.

3.9 Observing oscilloscope waveform, CLOSE the MANUAL CLOSE COMMAND SWITCH S507. DO NOT RETURN THIS SWITCH TO THE DOWNWARD POSITION. Test Breaker should close and open automatically as outlined in Paragraph 3.5. Ascertain transient load current of 35 A as observed on the oscilloscope. Following the complete sequence of recycles, return SWITCH S507 to the DOWNWARD (DISABLED) position. If necessary, readjust load by operating GROUP 1 and GROUP 2 LOAD SELECT SWITCHES (S301 through S307 and S401 through S406, respectively) to provide a 35 A transient load.

3.9.1 Reset OSCILLOSCOPE SWEEP MODE for SINGLE SWEEP. Prepare to photograph waveform.

3.9.2 RECLOSE the MANUAL CLOSE COMMAND SWITCH S507. DO NOT RETURN THIS SWITCH TO THE DOWNWARD POSITION. Photograph waveform. Record data.

3.9.3 Return MANUAL CLOSE COMMAND SWITCH S507 to DOWNWARD position.

3.10 Prepare to record recycle data as follows.

3.10.1 Change oscilloscope sweep rate to 50 ms/cm. Prepare to photograph waveform.

3.10.2 CLOSE the MANUAL CLOSE COMMAND SWITCH S507. DO NOT RETURN THIS SWITCH TO DOWNWARD POSITION. Photograph waveform. Record data.

3.11 DEENERGIZE MAIN DC POWER SUPPLIES. Return SWITCH S507 to DOWNWARD (DISABLED) position.

4.0 TRANSIENT NO-TRIP TEST (Note: This test is not a contractual obligation.)

4.1 Set initial conditions as defined in Paragraph 3.1 with the following exceptions--

SSCB Bypass-Load Group 1	Switch S502	OPEN
SSCB Bypass-Load Group 2	Switch S501	OPEN
SSCB Connect-Load Group 1	Switch S504	CLOSED
SSCB Connect-Load Group 2	Switch S503	CLOSED

4.2 Set oscilloscope controls as follows--

Vertical	50 mV/cm
Horizontal	100 ms/cm
Sweep Mode	Single Trace
Trigger	External

Connect oscilloscope EXTERNAL TRIGGER INPUT to CLOSE COMMAND terminals E504 and E505, with E504 (CLOSE COMMAND RETURN) connected to oscilloscope ground.

4.3 Using the load bank claibration data obtained in Part I, Section F, operate GROUP 1 LOAD SELECT SWITCHES (S301 through S307) to select a load current of approximately 10 A at 243 V. ALL GROUP 2 LOAD SELECT SWITCHES S401 through S406 SHOULD BE IN OPEN POSITION. CLOSE TRANSIENT LOAD SWITCH S407. Maintain TRANSIENT LOAD SWITCH S408 in OPEN position.

4.4 Set oscilloscope to trigger from the CLOSE COMMAND signal. Prepare to photograph waveform.

4.5 CLOSE the CLOSE COMMAND SWITCH S507. Photograph waveform. TEST BREAKER should close and remain closed. Record data.

4.6 OPEN the Test Breaker by depressing MANUAL OPEN COMMAND SWITCH S508.

4.7 INCREASE MAIN DC POWER SUPPLY VOLTAGE TO 270 V. Repeat steps outlined in Paragraphs 4.4 through 4.6, photographing the waveform, and recording data.

4.8 DEENERGIZE THE MAIN DC POWER SUPPLIES.

5.0 ULTIMATE TRIP TEST - Prepare for ULTIMATE TRIP TEST, 243 V, 45 A, as follows.

5.1 Set all switches in OPEN or DISABLED position, with MAIN DC POWER SUPPLIES DEENERGIZED. Set the following switches as indicated--

12 Vdc Power	Switch S506	CLOSED
115 Vac Power	Switch S505	CLOSED
SSCB Bypass-Load Group 1	Switch S502	OPEN
SSCB Bypass-Load Group 2	Switch S501	OPEN

SSCB Connect-Load Group 1	Switch S504	CLOSED
SSCB Connect-Load Group 2	Switch S503	CLOSED

In addition, set oscilloscope controls as follows--

Vertical	50 mV/cm
Horizontal	100 μs/cm
Trigger	Internal
Sweep Mode	Single Sweep

5.2 Using LOAD BANK CALIBRATION DATA as obtained in Part I, Section F, operate GROUP 1 and GROUP 2 LOAD SELECT SWITCHES (S301 through S307 and S401 through S406, respectively) for a load current of approximately 25 A at 243 V. Now CLOSE TRANSIENT LOAD SWITCHES S407 and S408.

5.3 ENERGIZE MAIN DC POWER SUPPLIES. Carefully increase output voltage to 243 V. Prepare to photograph oscilloscope waveform.

5.4 CLOSE the MANUAL CLOSE COMMAND SWITCH S507. DO NOT RETURN THIS SWITCH TO THE DOWNWARD (DISABLED) POSITION. Photograph waveform. Record data.
DEENERGIZE MAIN DC POWER SUPPLIES. Return SWITCH S507 to DOWNWARD (DISABLED) position.

5.5 Prepare for ULTIMATE TRIP TEST, 18-A, 297-V, as follows.

WARNING: Allow all capacitors, including the commutation capacitor within the TEST BREAKER to COMPLETELY DEENERGIZE as a safety precaution and as a precaution to prevent accidental damage to INTERNAL COMPONENTS OF THE Test Breaker. For +25°C temperature, as least 10 min is recommended for this purpose.

5.5.1 Readjust Test Breaker for 18-A ultimate trip setting. This is accomplished by removing the Test Breaker cover and transferring the jumper that exists between Terminals E325 and E306 (located on the LOGIC BOARD) to run instead from Terminal E325 to Terminal E303. Insure that NO SOLDER OR OTHER DEBRIS is dropped onto circuit boards or other components, or into the breaker cover. Clean off all solder flux with an alcohol moistened swab.

5.5.2 Make careful visual inspection of Test Breaker to insure that the conditions of Paragraph 5.5.1, above, are satisfied. Replace cover.

5.6 Set up oscilloscope controls as follows.

Vertical	20 mV/cm
Horizontal	20 μs/cm
Trigger	Internal
Sweep Mode	Single Sweep

5.7 Establish initial conditions as defined in Paragraph 5.1 for all switch settings. Utilizing LOAD BANK CALIBRATION DATA as obtained in Part I, Section F, operate GROUP 1 LOAD SELECT SWITCHES S301 through S307 for approximately 10-A load at 297 V. CLOSE TRANSIENT LOAD SWITCHES S407 and S408. Prepare to photograph waveform.

5.8 ENERGIZE MAIN DC POWER SUPPLIES. Carefully adjust output voltage to 297 Vdc. CLOSE the TEST BREAKER by CLOSING the MANUAL CLOSE COMMAND SWITCH S507. DO NOT RETURN THIS SWITCH TO THE DOWNWARD (DISABLED) POSITION. The TEST BREAKER should close and open automatically, with number of recycles determined by internal setting within the Test Breaker. Photograph waveform. Record data.

5.9 Return MANUAL CLOSE COMMAND SWITCH S507 to DOWNWARD position. Change oscilloscope sweep rate to 50 ms/cm. Prepare to photograph recycle data.

5.10 Repeat steps outlined in Paragraph 5.8 above to record recycle data. Photograph waveform. Record data.

5.11 DEENERGIZE THE MAIN DC POWER SUPPLIES.

5.12 Following the procedures outlined in Paragraphs 5.5, 5.5.1, and 5.5.2 above, reset TEST BREAKER for 45 ampere ultimate trip.

(Nine Sample Data Sheets, as used in the test program, are omitted from this report.)

PART III
OVERVOLTAGE TRANSIENT TEST PROCEDURE

6.0 Install TEST BREAKER as outlined in Part I, Paragraphs F.11 through F.15, with the following exception: Connect. the 5 INPUT COMMAND LEADS to the TEST BREAKER together Insulate this connection and position this cable away from the 3 POWER LEADS to the TEST BREAKER. Refer to color code and wire size listed in Part I, Paragraph C.3 for identification of these cables.

6.1 Set the following switches as indicated--

Auxiliary Capacitor Bank	Switch S514	OPEN
12 Vdc Power	Switch S506	CLOSED
115 Vac Power	Switch S505	CLOSED
SSCB Bypass-Load Group 1	Switch S502	OPEN
SSCB Bypass-Load Group 2	Switch S501	CLOSED
SSCB Connect-Load Group 1	Switch S504	CLOSED
SSCB Connect-Load Group 2	Switch S503	OPEN

6.2 Referring to the LOAD BANK CALIBRATION DATA obtained in Part I, Section F, operate GROUP 1 LOAD SELECT SWITCHES S301 through S307 to provide a load of approximately 10 A at 270 V.

6.3 In the same manner as outlined in Paragraph 6.2 above, operate GROUP 2 LOAD SELECT SWITCHES S401 through S406 to provide a second load of approximately 10 A at 270 V. GROUP 2 loads are now applied across the INPUT 270 Vdc to the TEST BREAKER, while GROUP 1 loads are now applied to the TEST BREAKER OUTPUT.

6.4 Use a 0 to 50 A dc ammeter for TEST BREAKER load current monitoring, as described in Part I, Paragraph F.15.

6.5 Energize the 150-Vdc auxiliary power supply, setting the output voltage to 150 V.

6.6 ENERGIZE THE MAIN DC POWER SUPPLIES. Carefully adjust the output voltage to 270 V.

6.7 Set TRANSIENT ENABLE SWITCH S201 to the RIGHT-HAND (FIRE) position. The TEST BREAKER should remain open, as verified by monitoring of the load current on the dc ammeter.

6.8 DEENERGIZE THE MAIN DC POWER SUPPLIES.

6.9 Return TRANSIENT ENABLE SWITCH S201 to the LEFT-HAND (DISABLED) position. Deenergize the auxiliary 150-Vdc power supply.

6.10 Referring to Paragraph 6.0, connect these five TEST BREAKER INPUT COMMAND LEADS to System Test Assembly front panel Terminals E504 through E508 as described in Part I, Paragraph C.3.

6.11 Set the following switches as indicated--

SSCB Bypass-Load Group 1	Switch S502	OPEN
SSCB Bypass-Load Group 2	Switch S501	OPEN
SSCB Connect-Load Group 1	Switch S504	CLOSED
SSCB Connect-Load Group 2	Switch S503	OPEN

This now removes GROUP 2 loads from the TEST BREAKER INPUT, and leaves GROUP 1 loads connected to the TEST BREAKER OUTPUT. Return all GROUP 2 LOAD SELECT SWITCHES S401 through S406 to OPEN position.

6.12 Energize the 150-Vdc auxiliary power supply. Set the output voltage to 150 V.

6.13 ENERGIZE THE MAIN DC POWER SUPPLIES. Carefully adjust the output voltage to 270 V.

6.14 CLOSE TEST BREAKER by CLOSING the MANUAL CLOSE COMMAND SWITCH S507. Verify the TEST BREAKER to be closed by observing load current indication on the dc ammeter.

6.15 Set TRANSIENT ENABLE SWITCH S201 to RIGHT-HAND (FIRE) position. The TEST BREAKER should either remain closed without commutation, or remain closed after one single commutation, as determined by the RECYCLE COUNT setting within the Test Breaker.

6.16 OPEN the TEST BREAKER by depressing the MANUAL OPEN COMMAND SWITCH S508.

6.17 DEENERGIZE THE MAIN DC POWER SUPPLIES.

6.18 Deenergize the auxiliary 150-Vdc power supply.

PART IV
THERMAL TEST PROCEDURE

7.0 With all switches in OPEN or DISABLED position, install TEST BREAKER in an appropriate temperature chamber Carefully remove Test Breaker cover. Referring to Part I, Paragraph C.3, connect TEST BREAKER to the System Test Assembly.

7.1 Adjust thermal chamber temperature to +25°C and allow 1 hr for stabilization. Record the temperature.

7.2 Refer to Part II, Paragraph 1.0 through 5.12, OPERATIONAL TEST PROCEDURE. Portions of this test procedure will be used during thermal tests.

7.3 Perform a voltage drop test at 15 A, 270 Vdc, in accordance with Part II, Paragraphs 2.0 through 2.12.

7.4 Perform an I^2t TRIP TEST at 18 A, 270 Vdc, in accordance with Part II, Paragraphs, 3.0 through 3.5.

7.5 Perform an I^2t TRIP TEST at 35 A, 243 Vdc, in accordance with Part II, Paragraphs 3.6 through 3.11.

7.6 Perform an ULTIMATE TRIP TEST at 45 A, 243 Vdc, in accordance with Part II, Paragraph 5.0 through 5.4. Test Breaker ULTIMATE TRIP setting must be at 45 A.

7.7 Repeat steps outlined in Paragraphs 7.1 through 7.6, above, at +50°C.

7.8 Repeat steps outlined in Paragraphs 7.1 through 7.6, above, at 0°C.

7.9 Repeat steps outlined in Paragraphs 7.1 through 7.6, above, at +100°C.

9.10 Repeat steps outlined in Paragraphs 7.1 through 7.6, above, at -45°C.

PART V
LIFE TEST PROCEDURE

8.0 Install TEST BREAKER in appropriate thermal chamber as outlined in Part IV, Paragraph 7.0.

8.1 Stabilize chamber temperature at 0°C, +25°C, or +50°C, as desired, in the same manner as for Part IV, Paragraph 7.1.

8.2 Set the following switches as indicated--

12 Vdc Power	Switch S506	CLOSED
115 Vac Power	Switch S505	CLOSED
SSCB Bypass-Load Group 1	Switch S502	OPEN
SSCB Bypass-Load Group 2	Switch S501	OPEN
SSCB Connect-Load Group 1	Switch S504	CLOSED
SSCB Connect-Load Group 2	Switch S503	OPEN
Life Cycle Select	Switch S509	100 Cycles

All other switches should be in OPEN or DISABLED position.

8.3 Referring to LOAD BANK CALIBRATION DATA as obtained in Part I, Section F, set GROUP 1 LOAD SELECT SWITCHES S301 through S307 to obtain a load current of 15 A at 270 Vdc. Select one GROUP 2 load (SWITCHES S401 through S406) for a second load of approximately 3.0 A at 270 Vdc.

8.4 Refer to Part I, Sections C and D for descriptions of life test operation.

8.5 Refer to Part II, Paragraphs 1.0 through 5.12, OPERATIONAL TEST PROCEDURE. Portions of this test procedure will be used during life tests.

8.6 ENERGIZE MAIN DC POWER SUPPLIES. Carefully adjust output voltage to 270 Vdc.

8.7 Set AUTO CYCLE ENABLE SWITCH S510 to UPWARD (ENABLE) position. After a brief period, the TEST BREAKER should close, as indicated by load current monitioring. The LIFE TEST CYCLE should begin, as described in Part I Paragraphs C.4 and D.8.

8.8 Following ten cycles of operation, set AUTO CYCLE ENABLE SWITCH S510 to DISABLED (DOWNWARD) position.

8.9 Perform the following operational tests:

8.9.1 VOLTAGE DROP TEST in accordance with Part II, Paragraphs 2.0 through 2.12.

8.9.2 I^2t TEST at 18 A in accordance with Part II, Paragraphs 3.0 through 3.5.

8.9.3 ULTIMATE TRIP TEST at 45 A in accordance with Part II, Paragraphs 5.0 through 5.4. The internal TRIP SETTING of the TEST BREAKER must be at 45 A.

8.10 Restore conditions as outlined in Paragraphs 8.1 through 8.7. Continue life cycle operation until a total of 100 cycles of operation is attained.

8.11 Using the procedures outlined in Paragraphs 8.1 through 8.10, conduct life test for 1000 cycles of operation, performing operational tests outlined in Paragraph 8.10 above at the successive intervals:

8.11.1 Following 10 cycles of operation.

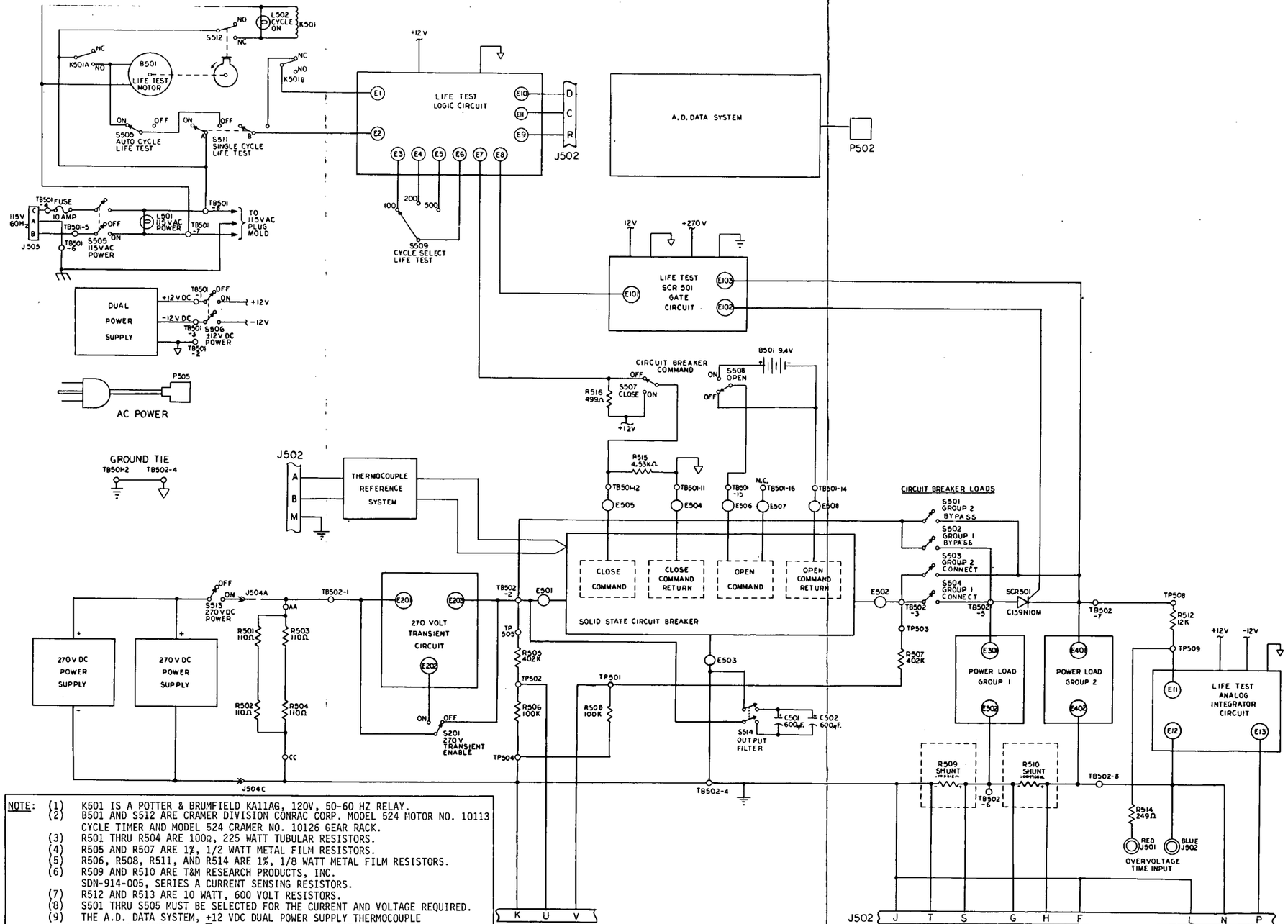
8.11.2 Following 100 cycles of operation.

8.11.3 Following 200 cycles of operation.

8.11.4 Following 500 cycles of operation.

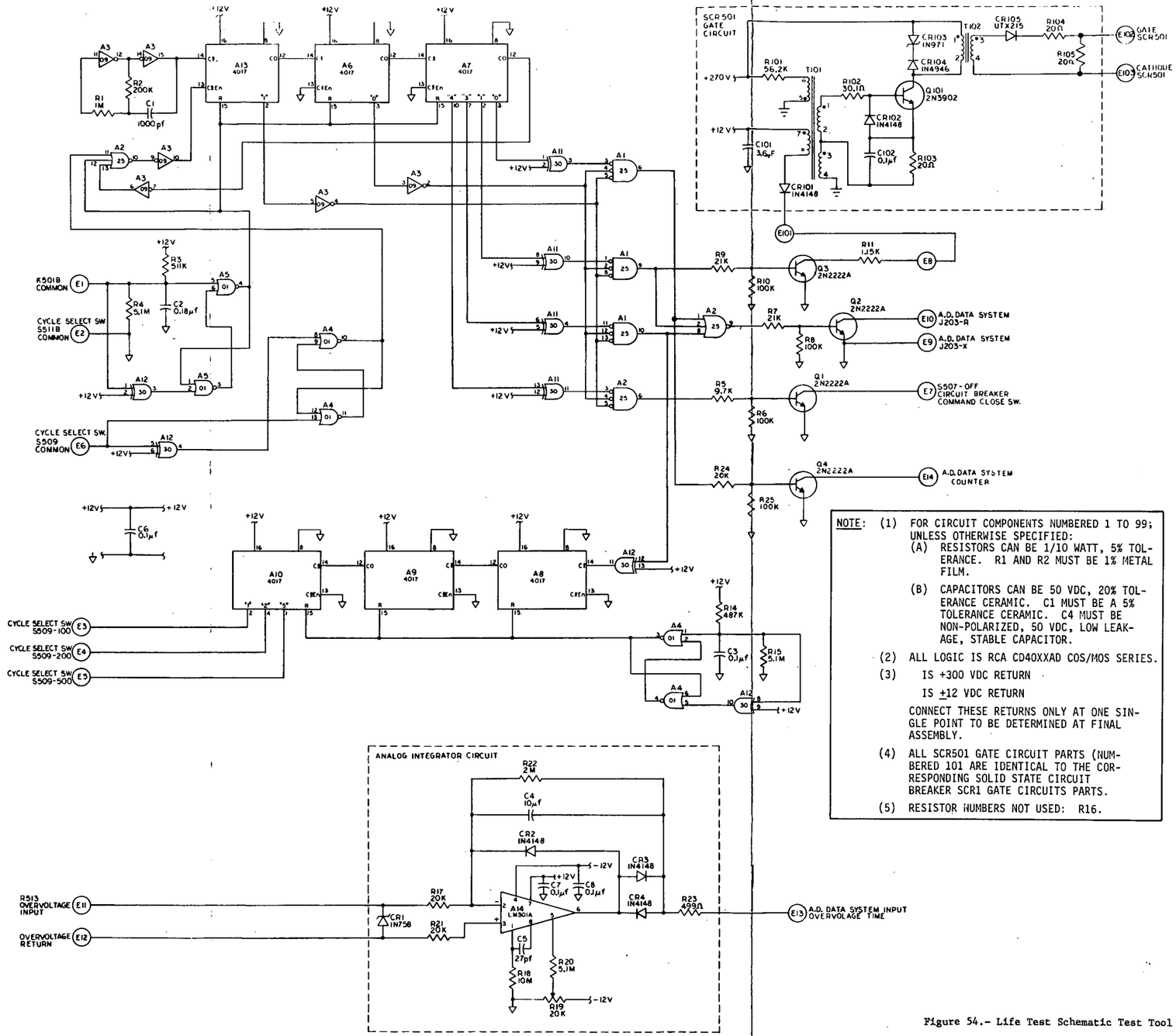
8.11.5 Following 1000 cycles of operation.

8.12 After life tests have been completed, DEENERGIZE MAIN DC POWER SUPPLIES. Return all switches to OPEN or DISABLED positions.



NOTE:
(1) K501 IS A POTTER & BRUMFIELD KA11AG, 120V, 50-60 HZ RELAY.
(2) B501 AND S512 ARE CRAMER DIVISION CONRAC CORP. MODEL 524 MOTOR NO. 10113 CYCLE TIMER AND MODEL 524 CRAMER NO. 10126 GEAR RACK.
(3) R501 THRU R504 ARE 100Ω, 225 WATT TUBULAR RESISTORS.
(4) R505 AND R507 ARE 1%, 1/2 WATT METAL FILM RESISTORS.
(5) R506, R508, R511, AND R514 ARE 1%, 1/8 WATT METAL FILM RESISTORS.
(6) R509 AND R510 ARE T&M RESEARCH PRODUCTS, INC. SDN-914-005, SERIES A CURRENT SENSING RESISTORS.
(7) R512 AND R513 ARE 10 WATT, 600 VOLT RESISTORS.
(8) S501 THRU S505 MUST BE SELECTED FOR THE CURRENT AND VOLTAGE REQUIRED.
(9) THE A.D. DATA SYSTEM, +12 VDC DUAL POWER SUPPLY THERMOCOUPLE REFERENCE SYSTEM AND S513 ARE NOT DELIVERABLE ITEMS.
(10) SWITCH POSITIONS DESIGNATED BY * ARE MOMENTARY POSITIONS.
(11) ALL A.D. DATA SYSTEM DATA INPUTS ARE DIFFERENTIAL.
(12) B501 IS A DURACELL #302905

Figure 53.- System Schematic Test Tool



NOTE: (1) FOR CIRCUIT COMPONENTS NUMBERED 1 TO 99; UNLESS OTHERWISE SPECIFIED:
(A) RESISTORS CAN BE 1/10 WATT, 5% TOLERANCE. R1 AND R2 MUST BE 1% METAL FILM.
(B) CAPACITORS CAN BE 50 VDC, 20% TOLERANCE CERAMIC. C1 MUST BE A 5% TOLERANCE CERAMIC. C4 MUST BE NON-POLARIZED, 50 VDC, LOW LEAKAGE, STABLE CAPACITOR.

(2) ALL LOGIC IS RCA CD40XXAD COS/MOS SERIES.

(3) IS +300 VDC RETURN

IS ±12 VDC RETURN

CONNECT THESE RETURNS ONLY AT ONE SINGLE POINT TO BE DETERMINED AT FINAL ASSEMBLY.

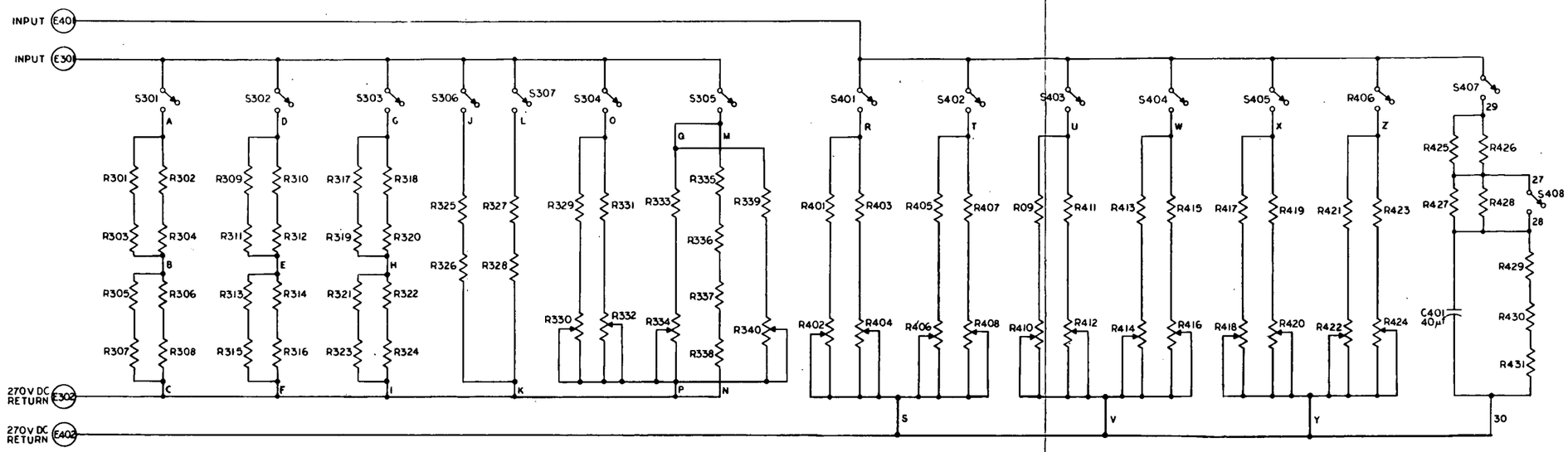
(4) ALL SCR501 GATE CIRCUIT PARTS (NUMBERED 101 ARE IDENTICAL TO THE CORRESPONDING SOLID STATE CIRCUIT BREAKER SCR1 GATE CIRCUITS PARTS.

(5) RESISTOR NUMBERS NOT USED: R16.

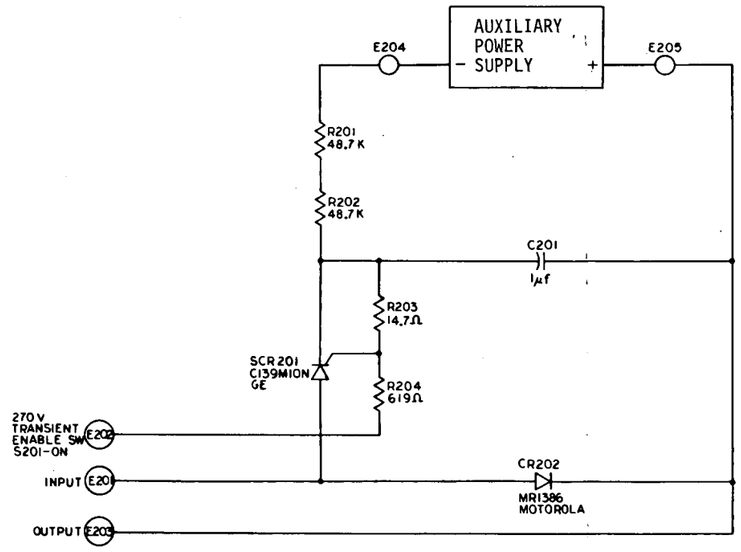
Figure 54.- Life Test Schematic Test Tool

FOLDOUT FRAME 1

FOLDOUT FRAME 2



150-VOLT TRANSIENT CIRCUIT



NOTE:
(1) R301 THRU R328 ARE 50Ω, 225 WATT, NON-INDUCTIVE TUBULAR RESISTORS.
(2) R329-R340 & R401 THRU R424 ARE 110Ω, 225 WATT, TUBULAR RESISTORS.
(3) R425 THRU R428 ARE 10Ω, 25 WATT, TUBULAR RESISTORS.
(4) R429 THRU R431 ARE 100KΩ, 1/8 WATT, >200V RESISTORS.
(5) C401 IS A 600 VDC, NON-POLARIZED CAPACITOR.
(6) ALL SWITCHES ARE ARROW-HART 80600-BJ.
(7) R201 THRU R204 ARE 1 WATT, 300 VOLT RESISTORS.
(8) 300 VDC POWER SUPPLY MUST SUPPLY AT LEAST 10 MA.

Figure 55.- Load Bank Schematic Test Tool

FOLDOUT FRAME 1

FOLDOUT FRAME 2