DESIGN STUDY REPORT
VOLUME II
ELECTRONIC UNIT

CONTRACT NO: NAS5-11643 AND NAS5-11288

GODDARD SPACE FLIGHT CENTER

PREPARED BY:

RCA/GOVERNMENT COMMUNICATIONS SYSTEMS
COMMUNICATIONS SYSTEMS DIVISION
CAMDEN, NEW JERSEY

FOR:

GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

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GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

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1.0 INTRODUCTION

The wideband recorder development covered by Contracts NAS5-11643 and NAS5-11288 has goals which are typical for a satellite equipment program; long life, high reliability, minimum power consumption and minimum weight. This report documents the efforts toward these goals on the Electronic Unit portion of the recording system. The analyses and tests conducted on the other portion of the recording system, the Transport Unit, were covered in Volume I of the Design Study Report, issued earlier.

Since issuance of the initial report, a significant number of changes have been incurred in the recorder specification. These were primarily due to changes in the spacecraft system design, yet covered only minor changes in the Transport Unit. Those changes that were required because of design changes are included in this report, although the major portion of this report covers only the Electronic Unit.

The recording system is required to record and reproduce wideband data from either of the two primary ERTS sensors. Return Beam Vidicon (RBV) camera or Multi-Spectral Scanner (MSS). The camera input is an analog signal with a bandwidth from dc to 3.5 MHz; this signal is accommodated through FM recording techniques which provide a recorder signal-to-noise ratio in excess of 39 dB, black-to-white signal/rms noise, over the specified bandwidth.

The MSS provides, as initial output, twenty-six narrowband channels. These channels are multiplexed prior to transmission, or recording, into a single 15 Megabit/second digital data stream. Within the recorder, the 15 Megabit/second NRZL signal is processed through the same FM electronics as the RBV signal, but the basic FM standards are modified to provide an internal, 10.5 MHz baseband response with S/N ratio of about 25 dB. Following FM demodulation, however, the MSS signal is digitally re-shaped and re-clocked so that good bit stability and signal-to-noise exist at the recorder output.

Two additional, longitudinally-recorded channels are also included in the recording system. One of these channels (Auxiliary Channel) is available for recording of housekeeping or audio data and is capable of recording and reproducing a 5 kilobit NRZ data stream. (Because of historical reasons this is basically an analog channel with a bandwidth of approximately 100 to 5000 Hz).

The second longitudinal track (Search Track) is a pre-recorded digital channel which outputs a discrete word for every 6 inches of tape movement. The output bit rate is 1.0 kb/s or 4.0 kb/s for the low or high tape reeling modes, respectively.

A completely automatic control system cycles the recorder from one operating mode to another, obviating the need for any intermediate commands. Memory functions are also incorporated, so that the choices between RBV/MSS and Record/Playback are stored even if primary power is removed from the system.

The division of the recording system into two discrete packages is a requirement of NASA Specification S-731-P-79, which calls for a minimum of electronics in the hermetically-sealed enclosure which houses the tape transport. Hence, the major elements of the Transport Unit are a transverse scan headwheel panel; a negator-spring reeling system; a urethane coated, mylar-belt coupled, hysteresis motor driven capstan assembly; and 2,000 feet of special two-inch wide video recording tape. Miscellaneous guides, auxiliary heads, $I\omega$ balancing elements, end-of-tape sensors, pressure and temperature sensors and electronics are also contained in the Transport Unit.

The electronics within the Transport Unit consist primarily of record amplifiers for the wide band channels, and playback preamplifiers for all three channels. In addition, portions of the control elements for motor switching are also located in the Transport Unit. To minimize the possibilities of tape path contamination, the electronics and most of the transport wiring are located on the side of the motor-board opposite to the tape path.

The balance of the electronic circuitry is contained in the Electronics Unit. This unit is a compartmentalized sheet metal structure properly reinforced to house 29 printed circuit boards and one hard wired structure containing the larger components which do not readily mount on printed circuit boards. This structure contains 12 connectors, of which four interconnect with the Transport Unit and seven with the spacecraft. Each of these connectors contain related functions and are thus arranged to facilitate the spacecraft harness wiring. One additional connector, the test point connector, is used to evaluate the performance margin of the recorder system under test conditions. This connector should be covered with an RFI shield in flight configuration.

The specification for the recorder life requires "one year in orbit after considerable ground testing" with a design goal of "4,000 full length record and playback cycles". In the studies and tests conducted during the design phase of the program, drift during three years was considered for the electronics and 4,000 record/playback cycles (5,000 operating hours) was the minimum goal for all limited life mechanical components except for the head-to-tape interface. In this latter area, a goal of 1,000 hours was established by RCA's proposal and this goal represented a two-to-one improvement over the best previous results. Two tests of the most recent head/tape configuration have now exceeded this goal without failure and the wear rates experienced do not preclude an extension of life to beyond 4,000 record/playback cycles.

Realization of this life, however, will depend on the ability to:

1) Minimize the build-up of contaminants on the video heads,

2) Prevent the occurrence of premature component failures. Design efforts in these areas for the Transport Unit are described in this report, together with the other related analyses and tests.

2.0 FLIGHT RECORDER ELECTRONIC UNIT

2.1 Mechanical Design

The function of the Electronic Unit (EU) enclosure is to accommodate all Video Tape Recorder (VTR) circuitry with the exception of the preamplifiers and wideband record circuits, in a manner consistent with the electronic design needs, the operational environment and specification requirements. Pursuant to this end the factors to be considered are configuration and structure, heat removal, RFI, weight, spacecraft integration, and selection of proper finishes and materials.

2.1.1 Configuration. - The configuration of the EU is based upon development of the printed circuit board (PCB) form factor, the interconnection requirements, and the space and weight allowances of the spcification.

a. Printed circuit board form factor. - The development of the internal configuration of the enclosure and the PCB form factor necessarily proceed together, because both electronic and mechanical requirements must be considered at the same time.

The mechanical design of the printed circuit boards is shown in Figure 2-2. This design was selected to allow good electrical signal flow, separation where necessary of various signals or functions, a reasonably good conductive path for thermal considerations and the required structural integrity.

This PCB for factor is compatible with the interconnection philosophy and the allowable enclosure dimensions.

The physical location of each printed circuit board with its appropriate unit designator and title is shown in Figures 2-1 and 2-3. These revised locations are in accordance with the latest design of the MSS and control circuitry.

b. Interconnect Approach (Figures 2-4 and 2-5). - Concurrent with the development of the PCB configuration is the development of the PCB connector, and a means of interconnecting these PCB's one to another and to the outside world (external) connectors.

Printed interconnect boards (IB's) were selected as the means of performing the routine PCB interconnections, to obtain the advantages of weight and bulk reduction, plus increased resistance to vibration damage due to the minimal number of wires required. In addition, wiring errors are minimized during assembly and test.

A1 1-2 Buffer/MSS Out A2 2-4 Buffer A3 Decoder A4 Master Clock A5 1-2 Variable Clock	A16 FM Equalizer A17 2-4 Limiter/Demod A18 1-3 Limiter/Demod A19 RBV Out/Rec Adj. A20 MSS/RBV Input A21 Modulator
A6 2-4 Variable Clock A7 Aux Rec./Search Play A8 Aux Playback A9 Sync Speed Detector	A22 Telemetry A23 Capstan Servo A24 Ref. Generator A25 T.W. Processor
A10 Volt Protect./Shoe Sol. SW A11 Control A12 Cycler A13 Command	A26 Iω Bridge A27 H.W. Bridge A28 Headwheel/Iω Driver
A14 DC/DC Converter A15 Motor Aux	A29 Capstan Driver/Damper A30 Capstan Bridge A31 Spare B

Figure 2-1. Electronic Unit PCB Locations

The final selection of the printed interconnect board is based upon the fact that 90% of the actual board to board connections can be made via IB trace. The balance of board to board interconnections are largely shielded leads. External connectors must connect via wire in any case. The approximate breakdown of connections is:

PCB Connections via IB trace	1,676
PCB Connections via wire	188
External Connections via wire at IB	248
External Connections via wire at Connectors	248
Approximate total Mo. of Connections in EU	2,360

2.1.2 Structure. - The enclosure is a stressed skin design of riveted construction and provides mounting supports for all components, electrical shielding between PCB's, and thermal conduction paths via Bircher Springs, connectors and PBC handles. The "egg crate" internal configuration provides structural rigidity and thermal conduction paths from internal to external surfaces and to the enclosure mounting feet.

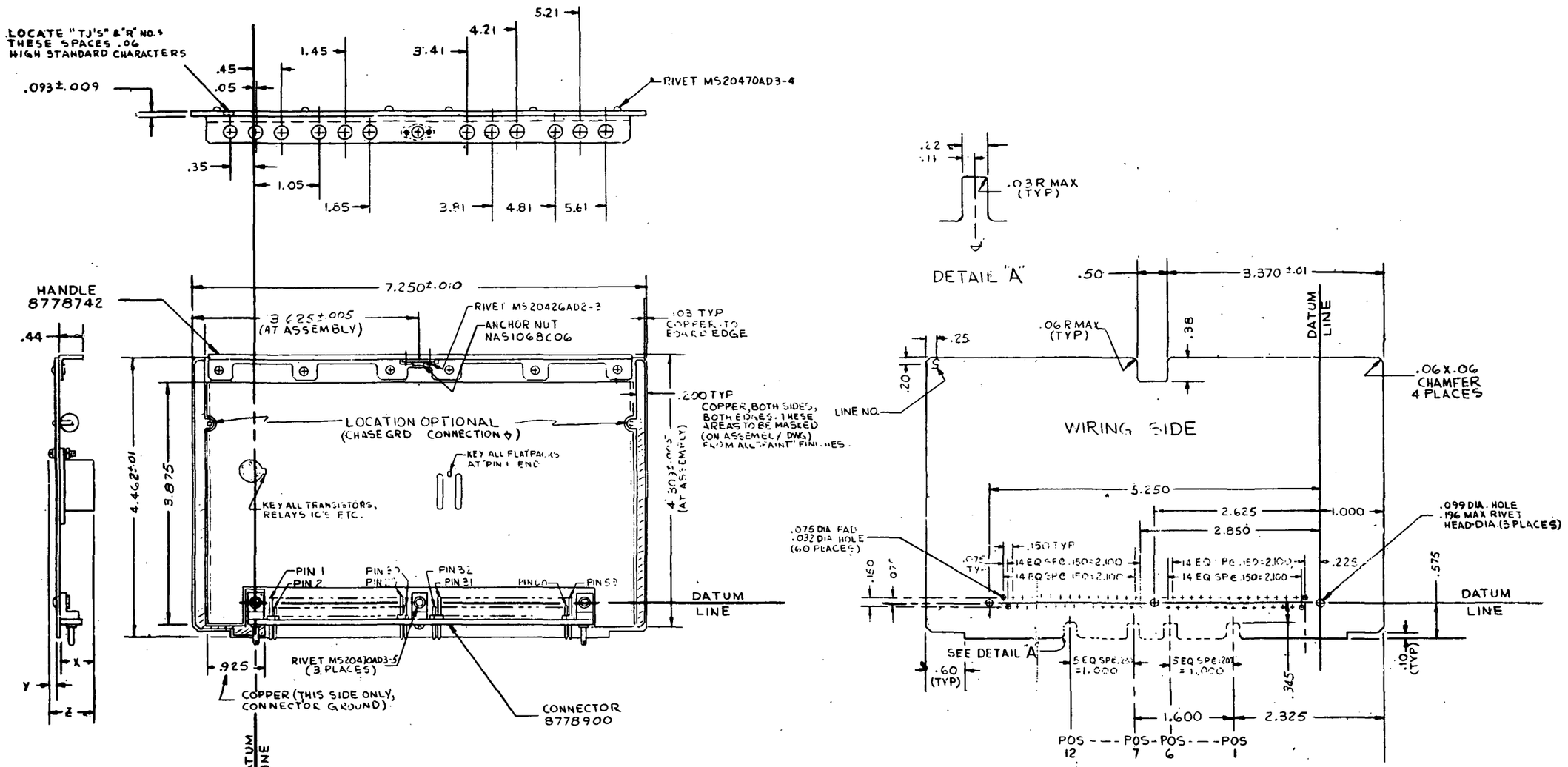


Figure 2-2. Printed Board Mechanical Layout

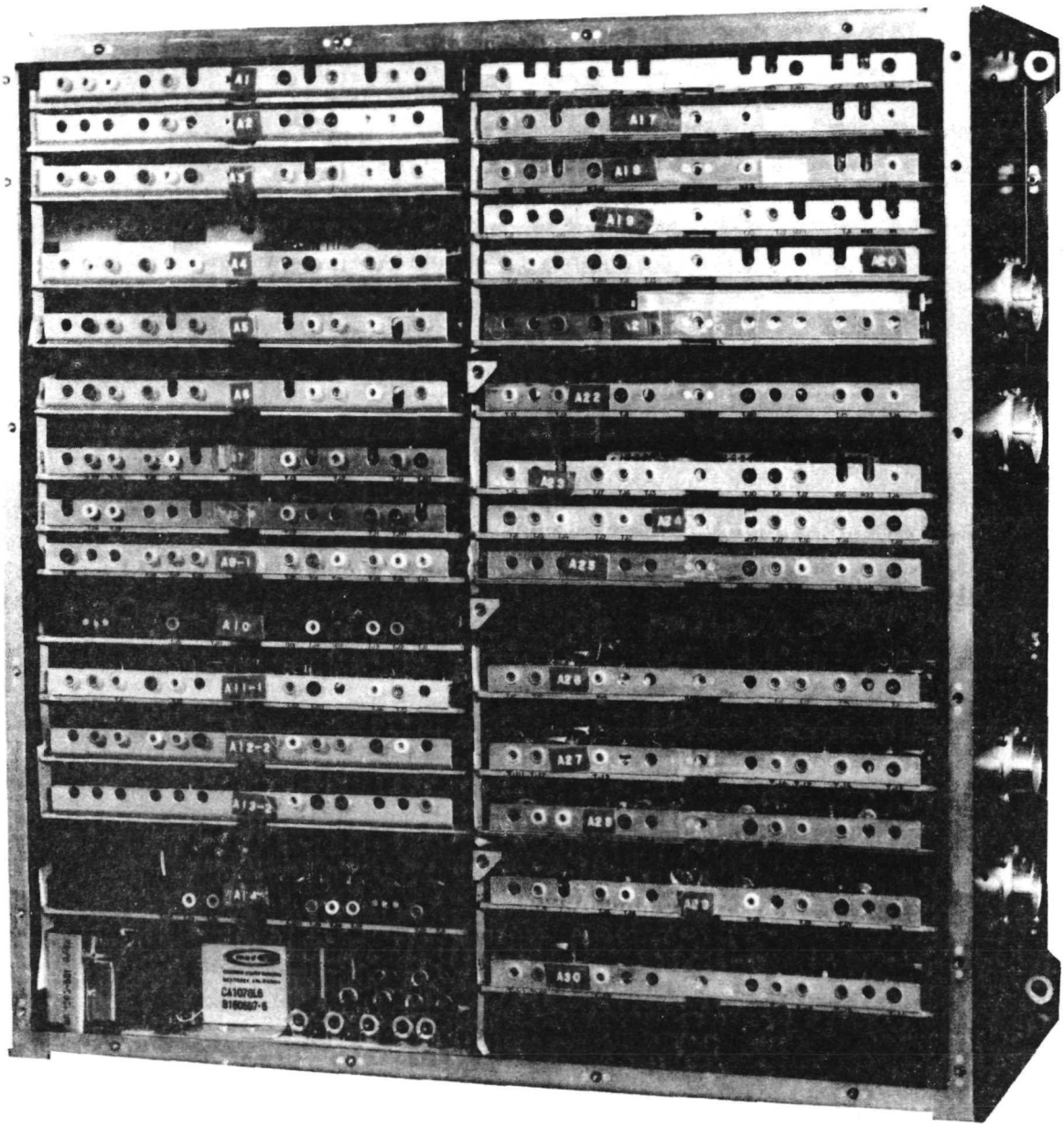


Figure 2-3. Printed Circuit Boards in EU Enclosure

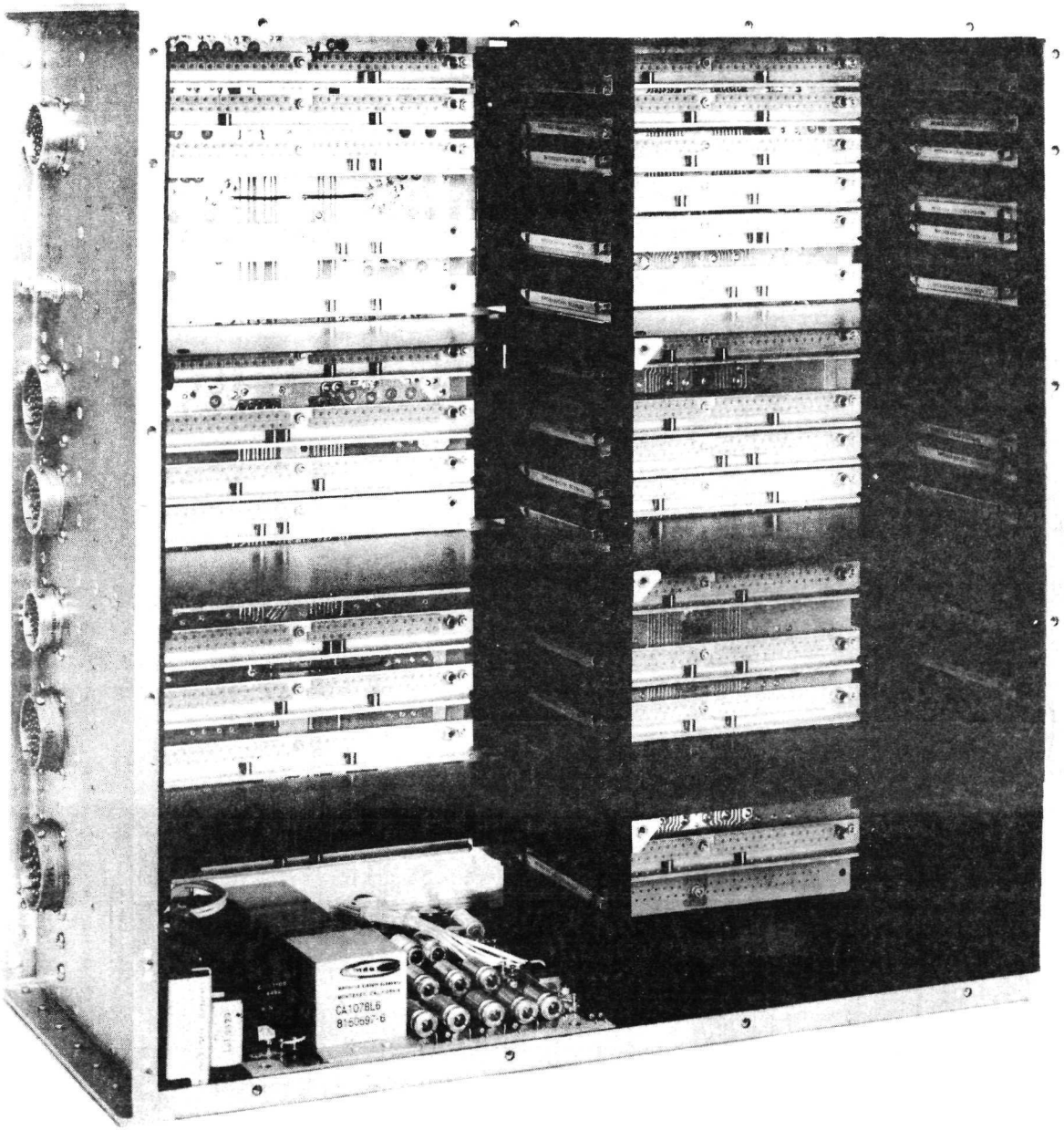


Figure 2-4. EU Enclosure (Front View)

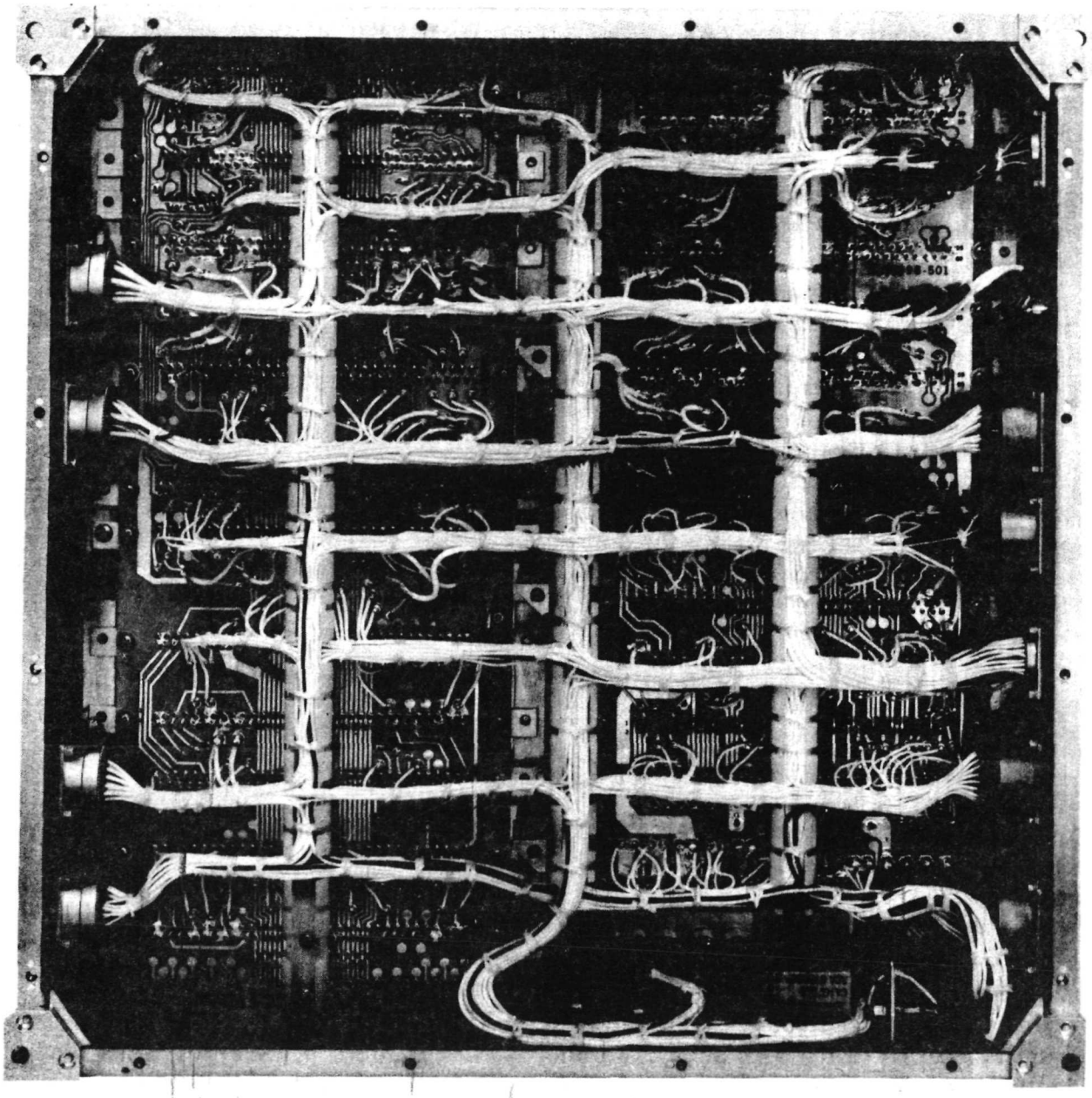


Figure 2-5. EU Enclosure (Wiring Side)

2.2 Thermal Analysis

The first attempt to solve for the heat flow and temperature rise of the Electronics Unit was a steady state analysis using Thermal II, a computer program written by RCA-AED. This program related the power dissipation of each board during the MSS playback mode with the radiation and conductive couplings between printed circuit boards, interconnect boards, and wall sections to yield the heat flow and temperature of each node or section of the unit. The heat sink for this case was defined to be the mounting surface which conducted and radiated to a 45° C sink. The program was abandoned when a transient analysis appeared to be indicated.

The new transient analysis uses another computer program developed by RCA-AED called Thermal I. It uses board dissipations and the same radiation and conductive couplings, but also accommodates the specific heat of the nodes, and the variation of board power dissipation as the function of the VTR changes.

The transient analysis serves two purposes. The first is to see if the EU is viable; that is, whether the transistor junction temperatures are less than 110° C (230° F). The other is to define a suitable thermal-vacuum test procedure which might be easily implemented in the test chamber that simulates or makes slightly worse the temperatures predicted in the nominal orbit.

As previously mentioned, one of the major changes between this and the previous program is the ability to go into different recording functions rather than a 100%, steady state, duty cycle. Table 2-1 contains a description of what is considered a nominal orbit load, a peak load in orbit, a thermal-vacuum test condition, and a 100% duty cycle. Also listed with these various power conditions is the worst case sink temperature. Table 2-2 is a listing of the assumed power dissipation of each of the boards during each of the record functions; the table also lists the peak board temperatures after many orbits for both heat sink configurations.

The heat sink position has been the other major change since the Thermal II analysis. Previously, the sink was described as the entire mounting surface. It is now described as an emissive "window" on the end of the unit that is "looking" at space. Because of the two units being mounted differently on the spacecraft, the sink was taken to be on the skin outside either board A1 or A15. This space window will be maintained at 20 ±10° C by means of its radiation loss to space and heaters located near the window.

The nominal orbital power condition is our primary interest. The other power modes are just an interesting sidelight at this point. Also because of the different sink positions, two separate studies are required. When the sink is on the end near board A1, the highest board temperatures are created. That case will be discussed first.

TABLE 2-1. THERMAL ANALYSIS, VARIOUS CONDITIONS

Nominal Orbit		Peak Load Orbit		Thermal Vac Test		Max. Duty Cycle	
Mode	Operating Time Minutes	Mode	Operating Time Minutes	Mode	Operating Time Minutes	Mode	Operating Time Minutes
Standby	10.0	Standby	10.0	Standby	20.0	Record	30.0
Record	10.0	Record	20.0	Record	10.0	Rewind	7.5
Rewind	2.5	Rewind	5.0	Rewind	2.5		
MSS PB	10.0	MSS PB	15.0	MSS PB	10.0		
Rewind	2.5	Rewind	3.75	Rewind	2.5		
Stop	75.0	Stop	56.25	Stop	65.0		
Recycle		Recycle		Recycle		Recycle	
Sink Temp	30° C	Sink Temp	30° C	Sink Temp	45° C	Sink Temp	45° C

TABLE 2-2. BOARD POWER DISSIPATION AND MAXIMUM TEMPERATURE IN NOMINAL ORBIT

BOARD		MODE DISSIPATION (WATTS)				TEMPERATURE (°F)		
NUMBER	NAME	STANDBY	RECORD	REWIND	MSS PB	NEAR A1	NEAR A15	THERMAL-VACUUM
A1	Buffer	0	0	0	2.2	111.3	119.2	127.8
A2	Buffer	0	0	0	2.1	113.6	120.3	128.2
A3	Decoder	0	0	0	2.3	114.1	120.9	128.4
A4	Master Clock	0	0	0	2.4	113.9	120.4	128.2
A5	Variable Clock	0	0	0	1.7	113.4	118.7	127.2
A6	Variable Clock	0	0	0	1.7	121.1	118.6	129.0
A7	Aux. Rec./Search Play	1.3	2.6	1.3	1.3	123.0	120.0	130.5
A8	Aux. Playback	0	0	0	2.1	122.8	119.8	130.4
A9	Sync. Speed Dector	2.2	2.2	2.2	2.2	125.1	121.6	132.4
A10	Volt. Prot./SSS	.8	.8	.8	.8	125.4	114.4	128.7
A11	Control	.4	1.6	1.6	1.6	126.1	115.6	130.5
A12	Cycler	.7	.7	.7	.7	124.4	113.7	128.4
A13	Command	.32	.32	.32	.32	124.4	113.0	128.2
A14	DC/DC Converter	4.0	11.0	5.5	12.0	145.4	127.4	148.4
A15	Motor Aux.	2.0	2.0	2.0	2.0	128.6	109.2	132.2
A16	FM Equalizer	0	0	0	1.8	119.4	120.2	127.6
A17	Limiter/Demod.	0	0	0	4.5	124.3	125.2	132.5
A18	Limiter/Demod.	0	0	0	4.5	124.3	125.1	132.4
A19	RBV Out/Rec. Adj.	0	.5	0	0	118.1	119.0	126.2
A20	MSS/RBV In	0	3.5	0	0	118.1	119.8	126.1
A21	Modulator	0	4.5	0	0	118.4	119.8	126.1
A22	Telemetry	1.0	1.0	1.0	1.0	123.4	119.9	128.6
A23	Capstan Servo	0	0	0	4.0	127.6	123.7	132.4
A24	Ref. Generator	1.7	1.7	1.7	1.7	126.4	121.5	131.2
A25	TW Processor	1.5	1.5	1.5	1.5	125.3	121.0	130.0
A26	Iω Bridge	.2	.2	.2	.2	123.9	114.7	125.6
A27	HW Bridge	.4	.4	.4	.4	124.5	115.0	126.0
A28	HW/Iω Driver	1.3	2.5	2.5	2.5	128.7	119.4	131.3
A29	Capstan Driver/ Damper	0	2.3	2.3	2.3	128.6	115.8	130.4
A30	Capstan Bridge	0	.2	.2	.2	124.9	111.3	125.5
	TOTAL	17.82	39.52	24.22	60.02			

Figure 2-6 shows the temperature of the DC/DC Converter board during the first five orbits. Because of the considerable cost of computer time, a calculation of many orbits to find what the maximum board temperatures approached was undesirable for every case studied. However, a curve based on the first few orbits could be made to fit the peak temperatures very well. A curve of the form:

$$T_n = \Delta T (1 - e^{-\lambda (n-1)}) + T_1$$

where:

T_n = peak temperature of the n^{th} orbit.

T_1 = peak temperature of the first orbit.

ΔT and λ are unknowns.

was assumed. Based on a single Thermal I program of 15 orbits, which confirmed the assumed curve's accuracy, the boards' peak temperature at any orbit or infinity was predicted for all conditions. This curve and the peak temperature at infinity is also shown on Figure 2-6 by the dashed lines.

Our other interest is to find a suitable thermal-vacuum test. With the DC/DC Converter board at one end of the unit and the sink at the other, a large temperature gradient resulted. The sink was 86° F (30° C) and the skin where the handle of the Converter board is attached reached 132.8° F at its peak. Because of this severe gradient, a simple thermal-vacuum test procedure has not yet been established, however, work in this area has just recently been started. It is hoped that blanketing portions of the unit during the test, and accounting for other possible heat losses in the spacecraft will yield a good test procedure.

As shown by Figure 2-7, when the sink has changed positions, the DC/DC Converter board temperature is substantially lower as well as some of the other board temperatures. Also, the skin outside the DC/DC Converter board handle is now 112.1° F at its peak. Defining a test procedure for this condition is also underway.

The Thermal I analysis yields only a board's temperature. The criteria for a transistor's viability is whether its junction temperature remains less than 230° F (110° C). Now that the board temperatures are known, the temperature rise from the board to the junction will determine if a transistor needs further heat sinking. This study of junction temperatures is also underway now. When a transistor junction temperature is excessive, some thermal conductive epoxy will be necessary to create a sufficient heat path to the board. It is hoped that relatively few transistors will require this epoxy so that any additional weight will be minimal. There is also a special heat-sinking handle on the DC/DC Converter board and the voltage protect board. A separate analysis of these boards is required.

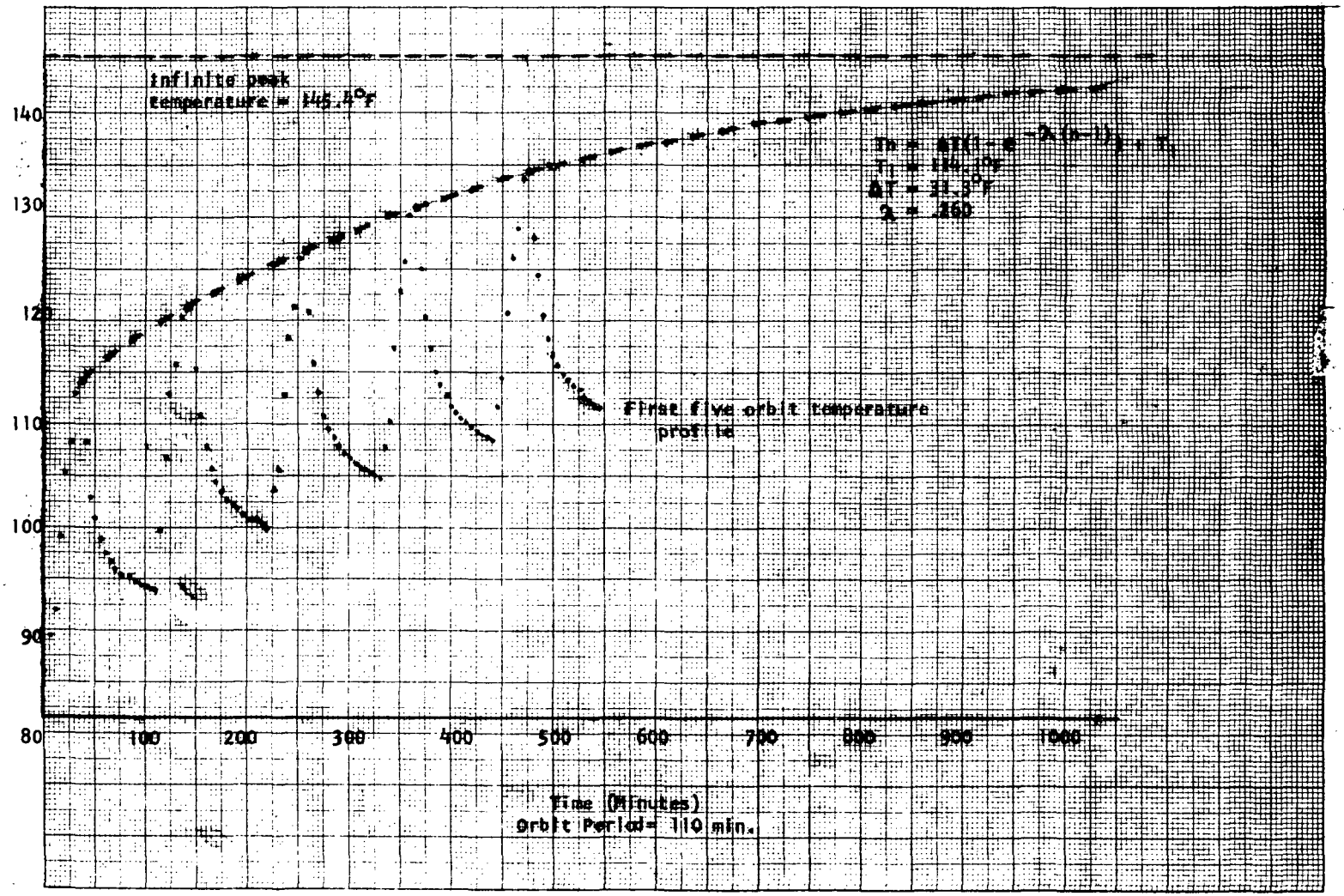


Figure 2-6. DC/DC Converter Board Temperature
(Nominal Orbit Conditions, sink at 86°F (30°C) near board A1)

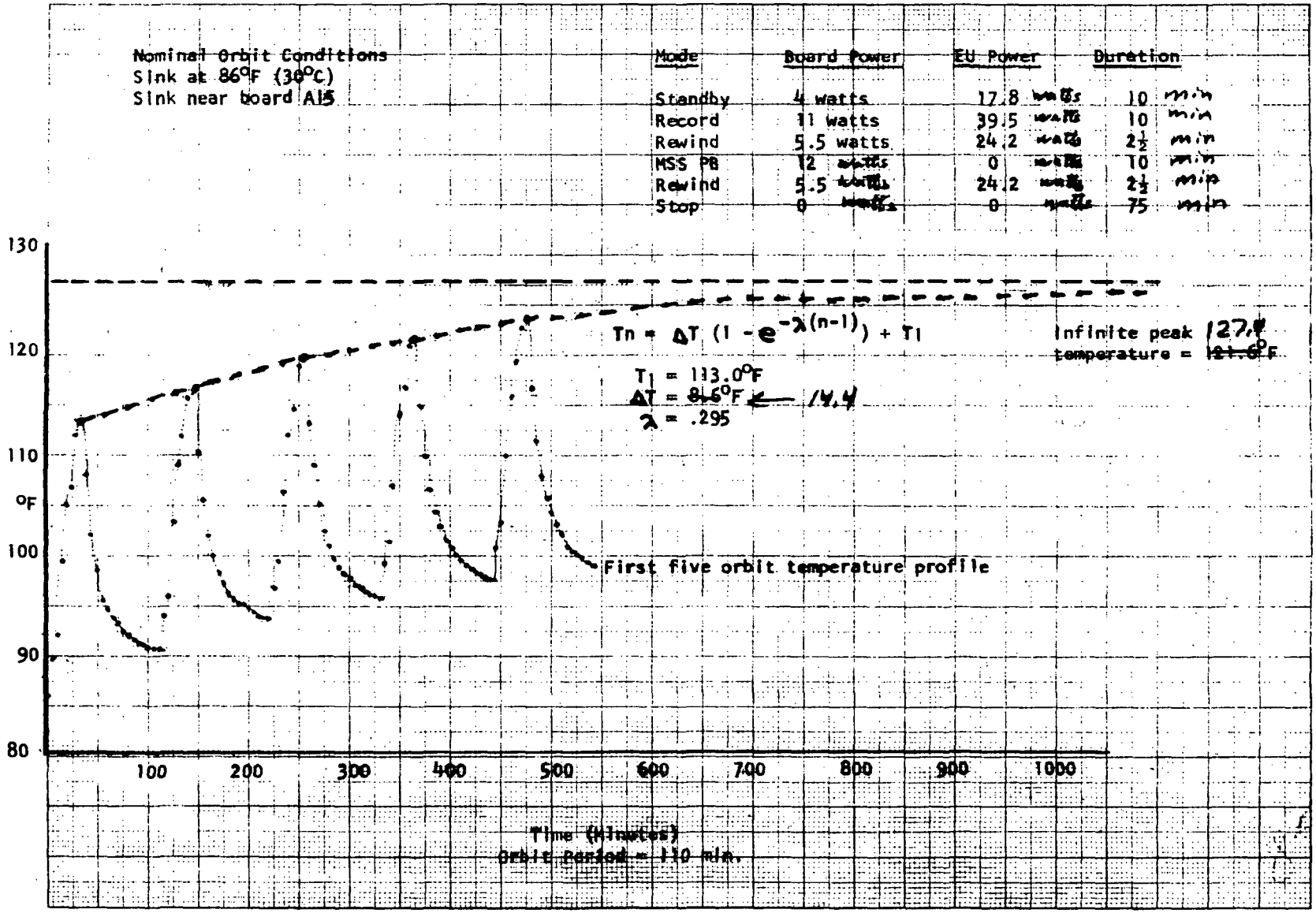


Figure 2-7. DC/DC Converter Board Temperature (Sink near Board A15)

2.3 RFI Considerations

The requirement to seal the EU against RFI resulted in relatively few design changes from the original non-sealed EU except in the area of the external connectors.

2.4 Enclosure Changes

The basic enclosure was modified to include continuous mounting flanges for the top and bottom covers, and a maximum cover fastener spacing of four inches. RFI gaskets were also added between the flanges and covers. The top cover, originally designed to allow test jack access without cover removal was redesigned to include the test jacks within the sealed enclosure.

2.5 Filtering

Filter pin connectors were added to all telemetry, external signal, command and power leads connecting the EU with the spacecraft. Additional filtering for the primary power leads is provided within the enclosure. The test point connector, not used during flight, is to be sealed using a standard (or modified if required) metalic protective cap.

2.6 EU Weight Summary

The EU weight control report (Table 2-3) presents the current weight forecast for the electronic unit of 31.392 pounds, which is 4.186 pounds below the December 1970 forecast. This weight reduction resulted from the implementation of the weight reduction program set forth in the Fifth Quarterly Report. This plan included reduction of selected panel thicknesses of the EU enclosure, reduction of selected PCB thicknesses and a review of EU interconnection wire sizes.

The method used in arriving at the PCB weights is presented in Table 2-4 and is based upon the actual weights of the PCB's currently generating in the engineering model. Several of these boards are still subject to some design changes (especially in the MSS area); most are of 0.093 thickness, and none have been coated (MFP). Small deviations from the weights presented are therefore still to be expected. Further, the finalized system weight may vary slightly due to allowable tolerances in board thickness, MFP thickness, quantity of solder used, etc.

2.7 Integration

Prior to the selection of a spacecraft supplier, RCA proceeded with design under the ground rules layed down by the equipment specification and the Nimbus D environmental handbook. Compatability between these requirements and the actual requirements set forth following selection of GE as the spacecraft supply is good; the only exception of note being in the thermal area, discussed elsewhere in this report.

TABLE 2-3. ELECTRONICS UNIT WEIGHT CONTROL REPORT

ASSEMBLY NAME	ESTIMATED/ACTUAL WEIGHTS					
	SEE NOTE	21 MAY 1969	15 JULY RWC EST	10 NOV BB WT.	12 DEC 1970	2 FEB 1970
1. HEADWHEEL BRIDGE		.78E	1.03E	.87A	.87A	.87A
2. CAPSTAN BRIDGE		.78E	1.28E	1.18A	1.12A	1.12A
3. IW BRIDGE		.78E	1.28E	1.18A	1.12A	1.12A
4. HEADWHEEL/IW DRIVER		1.0E	.77E	.5A	.5A	.50A
5. SYNC DECT./DAMPER	1	.56E	.57E	.44A	.37A	.37A
6. DC/DC CONVERTER		.87E	1.21E	1.21E	1.06A	1.06A
7. T. M.		.50E	.57E	.57E	.57E	.57A
8. CAPSTAN DRIVER/SERVO	2	.56E	.77E	.37A	.43A	.43A
9. AUX CHANNEL		.56E	.57E	.57E	.31A	.31A
10. SEARCH TRACK		.56E	.57E	.57E	.31A	.56A
11. VIDEO IN		.56E	.67E	.32E	.32A	.32A
12. MODULATOR		.56E	.74E	.38A	.38A	.38A
13. LIMITER/DEMOD (QTY. 2)		.5E	.62E .62E	.38A .38A	.38A .38A	.38A .38A
13A SERVO (TEMP)					.5A	.50A
14. VIDEO OUT		.56E	.62E			.38A
15. EQUALIZER		.50E	.67E			.43A
16. REC ADJ T.W. PROC	3	.50E	.57E			.38A

FOLLOWING INTRODUCTION OF MSS CAPABILITY, NEW CONTROLS, ADDITIONAL TELEMETRY & RFI FILTERING ASSEMBLY NAME	SEE NOTE	ESTIMATED/ACTUAL WEIGHTS	
		DEC '70 RWC	RWC
HEADWHEEL BRIDGE		.905A	.874
CAPSTAN BRIDGE		1.196A	1.216
IW BRIDGE		1.196A	1.216
HEADWHEEL/IW DRIVER		.624A	.562
SYNC SPEED DETECTOR		.409A	1.405
DC/DC CONVERTER		1.290A	.405
TELEMETRY		.498A	.452
CAPSTAN DRIVER/DAMPER		.592A	.500
AUX REC./SEARCH-PLAY	9	.409A	.405
AUX PLAYBACK		.466A	.373
MSS REV IN	4	.627A	.530
MODULATOR	4	.717A	.655
LIMITER/DEMOD	4	.530A	.500
LIMITER/DEMOD	4	.530A	.500
CAPSTAN SERVO		.561A	.500
BUFFER/MSS OUT	5,9	.405A	.374
EQUALIZER		.561A	.500
REC ADJ/REV OUT	4	.409A	.468

TABLE 2-3. ELECTRONICS UNIT WEIGHT CONTROL REPORT (Continued)

ASSEMBLY NAME	SEE NOTE #	ESTIMATED/ACTUAL WEIGHTS 21 MAY 69 EST	15 JULY RWC EST	10 NOV BB WT.	12 DEC 1970	2 FEB 1970
17. REFERENCE GENERATOR		.87E	.57E	.44A	.38A	.38A
18. COMMAND MATRIX		.56E	.63E	.63E	.31A	.31A
19. OUTPUT MATRIX (CONTROL)		.56E	.73E	.73E	.62A	.62A
20. CONNECTORS } PLACED AT						
21. CASE END OF BREAKDOWN						
22. NEST ASSEMBLY FOR CLARITY						
23. DAMPER/VOLT. PROT.	1		1.22E	1.22E	1.22E	1.22E
24. MOTOR AUX						1.10E
SUB TOTAL #1 PCB'S BEFORE MSS			(21 PCE'S)		(23 PCB'S)	13.69
25. ADDITIONAL BOARDS FOR MSS & CONTROLS CHANGES						1.52E
SUB TOTAL #2 PCB'S DUE TO MSS CHANGE						1.52E

FOLLOWING INTRODUCTION OF MSS CAPABILITY, NEW CONTROLS, ADDITIONAL TELEMETRY & RFI FILTERING ASSEMBLY NAME	SEE NOTE #	ESTIMATED/ACTUAL WEIGHTS DEC '70 RWC	Mar '71 RCW
REFERENCE GENERATOR		.467A	.405
COMMAND	9,4	.530A	.405
CONTROL	9	.717A	.624
VOLTAGE PROTECT/SHOE SOLENOID SWITCH		.467A	.374
MOTOR AUX		2.70A	
	(23 PCB'S)	17.026	
A. BUFFER 2-4	5,9	.405E	.374
B. VARIABLE CLOCK	5,9	.483A	.467
C. VARIABLE CLOCK	5,9	.483A	.467
D. MASTER CLOCK	5,9	.517A	.624
E. TONE WHEEL PROCESSOR	6	.467A	.405
F. CYCLER	7,9	.717E	.467
G. DECODER	5.9	.430A	.494
		3.49	
TOTAL WT-PCB'S		17.828*	16.542

*Excluding Motor Aux.

TABLE 2-3. ELECTRONICS UNIT WEIGHT CONTROL REPORT (Continued)

ASSEMBLY NAME	ESTIMATED/ACTUAL WEIGHTS					
	SEE NOTE #	21 MAY 69 EST	15 JULY RWC EST	10 NOV BB WT.	12 DEC 1970	2 FEB 1970
20. CONNECTORS		1.E	1.E	1.E	1.E	3.37E
21. CASE		5.E	5.E	10.5E	10.5E	-----
22. NEST ASSY (COVERS INCLUDED)		5.E	3.E	3.E	3.E	6.5E
26. MISCELLANEOUS						1.0E
SUB TOTAL#3		11.0E	9.0E	14.5E	14.5E	10.87
GRAND TOTAL - E.U.			25.23			26.08

FOLLOWING INTRODUCTION OF MSS CAPABILITY, NEW CONTROLS, ADDITIONAL TELEMETRY & RFI FILTERING ASSEMBLY NAME	ESTIMATED/ACTUAL WEIGHTS					
	SEE NOTE #	DEC'70 RWC	MAR 71 RWC			
CONNECTORS	10	3.50A	↑			
CASE - PART OF NEST ASSY						
NEST ASSY (EXCLUDING COVERS)		6.31A				
MISCELLANEOUS			N/A			
COVERS, TOP & BOTTOM		1.15E	SEE			
"CLOSE-UP" HARDWARE & GASKETS		.50E	BELOW			
WIRE, SOLDER, ETC.		2.59A*	↓			
INTERCONNECT BOARDS		1.00A				
		15.05				
COMPLETE WIRED ENCLOSURE INCLUDING MOTOR AUX, FILTERS, AND RELAY		35.57				
ACTUAL WEIGHT OF ENCLOSURE INCLUDING MOTOR AUX @ 2.70, 18's @ 1.0, WIRE, SOLDER, ETC. @ 2.59		16.10A	13.00			
PCB'S LESS MOTOR AUX & INTERCONNECT BOARDS		17.82A	16.542			
MISCELLANEOUS: COVERS		1.15E	0.35			
HARDWARE		.50E	.50			
TOTAL		35.57				
*WEIGHT OF WIRE, SOLDER, ETC. DERIVED FROM ACTUALS.						
TOTAL WT-EU		35.578	31.392			

TABLE 2-4. PCB WEIGHTS

Ref. Desig.	Board Name	Weights (lbs)			
		Wired, Uncoated Board (Actual)	Adjusted for Board Thickness	Coating (MFP) and Cement (Estimate)	Total Weight
A1	Buffer 1-3	0.406	0.344	0.03	0.374
A2	Buffer 2-4	0.406	0.344	0.03	0.374
A3	Decoder	0.468	0.468	0.03	0.494
A4	Master Clock	0.594	0.594	0.03	0.624
A5	Variable Clock	0.437	0.437	0.03	0.467
A6	Variable Clock	0.437	0.437	0.03	0.467
A7	Aux. Rec/Search Play	0.437	0.375	0.03	0.405
A8	Aux. Playback	0.406	0.344	0.03	0.374
A9	Sync Speed Detector	0.437	0.375	0.03	0.405
A10	Voltage Protect/SSS	0.406	0.344	0.03	0.374
A11	Control	0.656	0.594	0.03	0.624
A12	Cycler	0.437	0.437	0.03	0.467
A13	Command	0.375	0.375	0.03	0.405
A14	DC/DC Converter	1.375	1.375	0.03	1.405
A16	Equalizer	0.532	0.470	0.03	0.500
A17	Limiter/Demod	0.532	0.470	0.03	0.500
A18	Limiter/Demod	0.532	0.470	0.03	0.500
A19	Record Adj/RBV out	0.500	0.438	0.03	0.468
A20	MSS/RBV IN	0.562	0.500	0.03	0.530
A21	Modulator	0.687	0.625	0.03	0.655
A22	Telemetry	0.454	0.422	0.03	0.452
A23	Capstan Servo	0.532	0.470	0.03	0.500
A24	Ref. Generator	0.437	0.375	0.03	0.405
A25	Tone Wheel Processor	0.437	0.375	0.03	0.405
A26	Iω Bridge	1.186	1.186	0.03	1.216
A27	Head Wheel Bridge	0.844	0.844	0.03	0.874
A28	Head Wheel/Iω Driver	0.594	0.532	0.03	0.562
A29	Capstan Driver/Damper	0.532	0.470	0.03	0.500
A30	Capstan Bridge	1.186	1.186	0.03	1.216
TOTAL					16.542

Several meetings have been held between GE, RCA and NASA for the purpose of clarifying interface requirements with regards to equipment finishes and thermal requirements, mechanical mounting, cabling and connectors, and the definition of open areas.

Presently the mechanical mounting interface is well defined, RCA and GE having agreed upon the use of drill templates to assure proper fit. In addition, drill template drawings have been approved by both RCA and GE, and these templates fabricated.

The definition of cabling and connectors is all but complete. Recent changes to the cabling drawings have been agreed to and implemented by RCA, while connector interfaces have also been recently clarified.

2.8 Materials

All materials and finishes used in the Electronic Unit, with the exception of aluminum, magnesium and steel, are listed in Table 2-5.

TABLE 2-5. ELECTRONIC UNIT MATERIALS AND FINISHES

Material	Mil Spec or RCA Drawing No.	Where Used
Silicone	Mil-R-5847, Cl. II, gr. 50	RFI Gasket
Epoxy formulation	8533343-11	Elec. Component Cement
Glass-Epoxy Sheet	MIL-P-13949	PCB base Material
Mylar (Polyester)	2010817-10	Component Spacers
Brass (annealed)	2010020	PCB terminals
Brass	2010553	PCB terminals
Brass	2010019	Coax PCB Terminals
Nylon	2010798 (L-P41D a (2))	Cable Ducts (IB)
Insulation, Wire	2010909-812 (847)	Shield for Wires
Glass Epoxy	2010896	Spacer, Insulator
Solder	SN 63-W-RA-P2 (QQ-S-571)	General Use
Loctite	8954869	Staking of screws
Glyptol	2010156	Elec. Comp. (Coils) Locking
Tin Plating	MIL-T-10727	PCB Terminals
Iridite	1980135-1	Aluminum Finish
Dow 23	2021060	Mag. Finish
MFP	2016185-1	PCB Coating
Hard Coating for A1	1980041	Heat Sink Coating
Paint, Black Velvet	2020787	Enclosure Surfaces
Paint, epoxy (White)	8909949-1	PCB Marking
Paint, epoxy (Black)	8909949-3	PCB Marking

3.0 FLIGHT RECORDER/REPRODUCER TRANSPORT UNIT DESIGN

The discussion in this section will be limited to reporting of technical developments subsequent to the design status described in the Design Study Report, Vol. I. On this basis then, the new design areas to be discussed are: the new reel transmission, the new deck design, updating of the enclosure design. The new study areas to be described are: the analog study of the transport, an updated thermal discussion, tape active length and coasting measurements, and the vibration survey of the Engineering Model.

3.1 Transport Mechanism

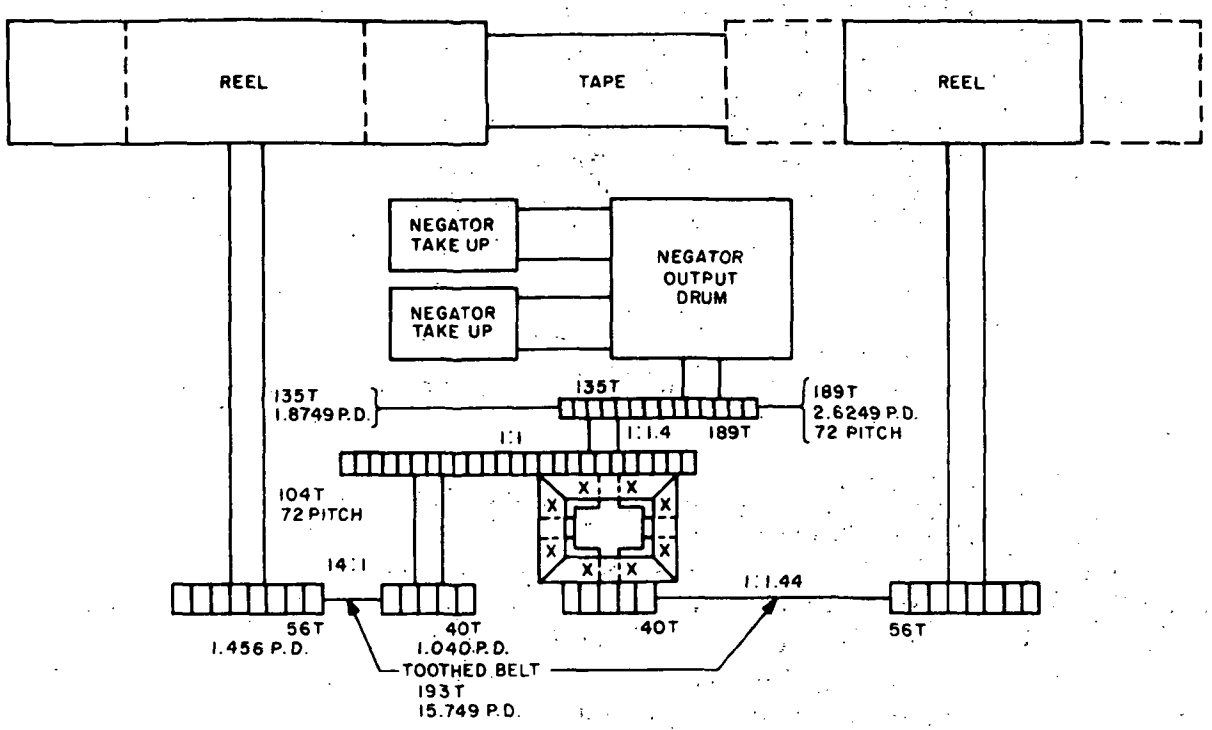
3.1.1 Redesign of Reel Torquing Transmission. - The transmission has been redesigned to improve the tooth loading parameters; however, the overall reduction ratio between the reels and negators remains unchanged. A schematic of the new system is shown in Figure 3-1(a), and a schematic of the previous system in Figure 3-1(b). An idler shaft stage has been added to reverse the motion of the takeup reel "seen" at the differential. This permits both toothed belts to be coupled to the end bevel gears of the differential, and the negators to be coupled to the spider shaft. In the previous design the takeup-reel toothed belt was coupled to the spider shaft, and the negators were coupled to one end of the bevel gear. There has been a modification in the number of teeth on the various sprockets and gears, resulting in the following improvements:

a. The torque load on the spider shaft and the bevel gear tooth loads has been decreased 28.5%.

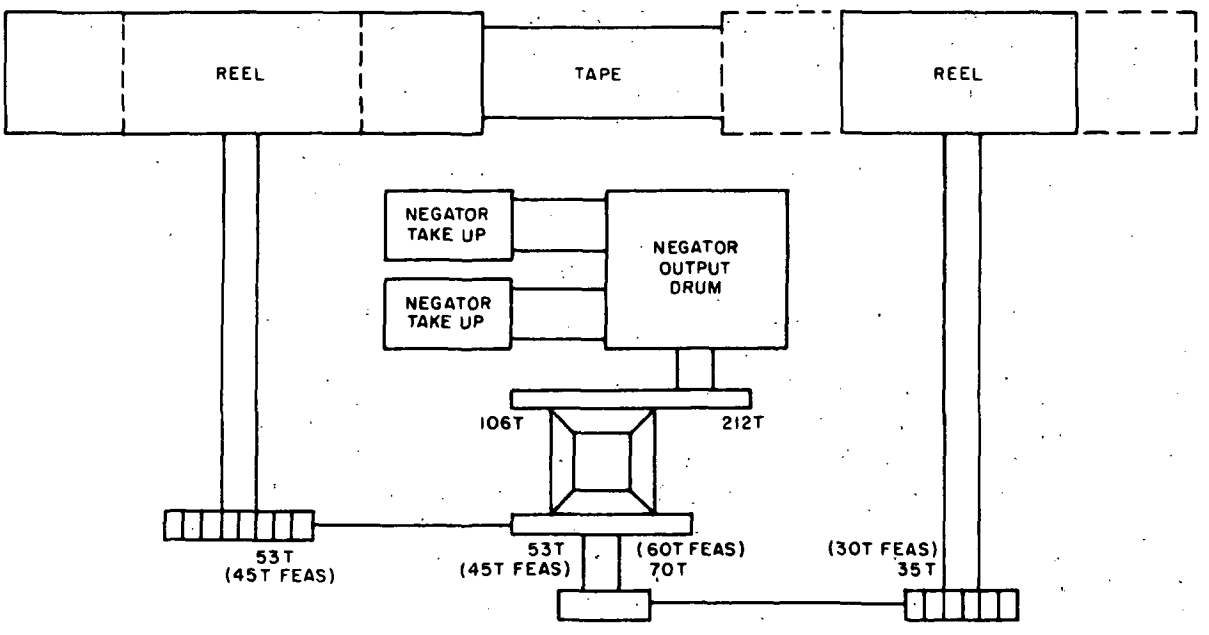
b. The tooth loads of the sprocket-belt drives have been reduced. Replacement of the 45-tooth sprocket on the supply reel shaft by a 56-tooth sprocket reduces its tooth load by 36%. Replacement of the 30-tooth sprocket on the takeup-reel shaft by a 56 tooth-sprocket reduces its tooth load by 71.5%.

c. Only one belt side load is now applied to the spider shaft. Previously, two belt side loads were present.

d. The bevel gear tooth frequencies have been changed to reduce possible effects of transport resonance between 15 Hz and 18 Hz. In the previous design the bevel gear tooth frequency varied from 7.5 Hz at BOT (Beginning of Tape) to 25 Hz at EOT (End of Tape). In the new design the tooth frequency varies from 42.1 Hz (BOT) to 44.5 Hz (EOT).



(a). Revised Configuration



(b). Previous Configuration

Figure 3-1. Reel Torquing Transmission

e. The bevel gear teeth will be Electrolyzed to improve the surface hardness, friction and wear characteristics. The gear tooth lubricant has been changed from Lehigh L-793 (G-8), in the previous design, to Andok C (G-6), in the new design. This was done to eliminate potential incompatibility between bearing grease and gear grease. There is also some indication that Andok C may be more effective at higher tooth pressures.

The first opportunity to evaluate the new design will occur when the breadboard transport is retrofitted with the new components. The present schedule for this event is the second half of December.

3.1.2 Transport Deck Design. - The transport deck design of the Engineering Model has been modified from that of the Feasibility Model in accordance with Technical Direction No. 1 (10/20/69). The modification replaces the printed circuit distribution board by a standard wiring harness, and eliminates the blind mating connectors. The new deck has ribbing to facilitate routing of the wiring and also to provide increased deck stiffness. The stress analysis of this deck was presented Vol I of the Design Study Report and is still applicable.

In the course of vibration testing of the Engineering Model, a simple vibration damper was added to the deck assembly. The damper consists of a strip of 0.090" aluminum sheet, 1" wide, and 19.6" long. The aluminum strip is clamped by cleats to the flange of the central stiffener rib with a thin viscoelastic layer (3M adhesive transfer tape #466) between the two clamped surfaces. The damping action reduced the amplification from 8.0 to 3.7 at the lowest resonant frequency. Based upon these results, it was decided to incorporate the damper in the design.

3.1.3 Analog Study of Transport Dynamics. - An electrical analog circuit of the tape transport was designed for computer application. The original purpose was to investigate mechanical resonances; however, its usefulness was extended to an optimization study of the capstan servo. One type of computer run was used to explore the possible effects of excitation by the differential gear teeth. This was done by assuming a constant amplitude torque disturbance at the negators, and varying the disturbing frequency. The velocity response at various points in the transport were obtained. This was done for tape-reel parameters corresponding to BOT, COT, and EOT (Beginning of Tape, Center of Tape and End of Tape, respectively). The dominant lower resonant frequencies derived were: 15 Hz at BOT, 18 Hz at COT, and 18 Hz at EOT.

It is planned to update this study with minor changes, consistent with the new transmission. The input disturbance will be changed from a nominal constant torque input to a nominal constant relative velocity between the two end level gears.

3.1.4 Tape Active Length and Coasting Measurements. - Tape footage parameters, based on measurements of both the Feasibility Model and the Engineering Model, are presented in Figure 3-2. The primary end-of-tape switches limit the normal active tape length to 1800 feet, minimum. At the beginning of tape there is a nominal tape length of 45 feet between the true start of tape and activation of the primary switch (BOTP); the secondary switch is activated (BOTS) 30 feet from the true start of tape. At the end of tape there is 110 feet of tape between the true end of tape and activation of the primary switch (EOTP); the secondary switch is activated (EOTS) 30 feet from the true end of tape. Between EOTP and EOTS there is 80 feet of tape, of which 65 feet is treated with cleaning compound.

Measurements of tape coasting length at high speed were made with and without the capstan brake. These values are given in Table 3-1.

3.2 Transport Enclosure

The enclosure was redesigned to correct a high stress problem existing in the original design. A sketch of the new configuration is shown in Figure 3-3. The stress analysis presented in the final version of the Design Study Report, Vol. I, is an up-to-date treatment of the new design. A summary of these calculations are shown in Figure 3-4. The enclosures will be machined from forged blocks of Magnesium Alloy ZK60A-T6; some of the properties of this alloy are also shown in Figure 3-4. In conjunction with RCA metallurgists, it was decided to heat treat to the final T-6 condition before machining. This condition results in good machinability, with no problem in obtaining uniform heat treatment throughout the block thickness.

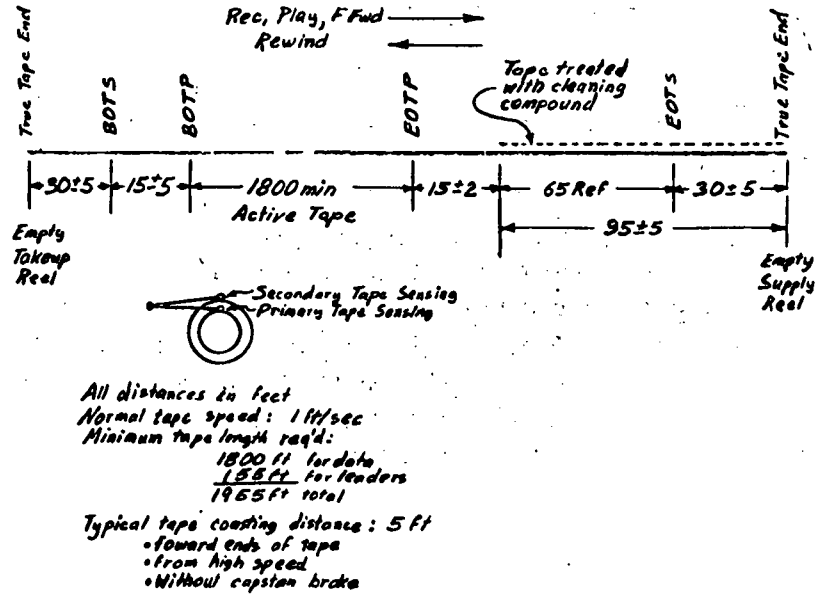


Figure 3-2. Tape Footage Parameters

TABLE 3-1. HIGH SPEED TAPE COASTING LENGTH DATA

	Coast Length (Inches)					
	BOT		COT		EOT	
	Rewind	Wind	Rewind	Wind	Rewind	Wind
With brake	24	34	30	30	39	28
Without brake	60	148	63	63	104	54

3.3 Transport Thermal Considerations

3.3.1 Background. - The thermal design of the Recorder System was based upon The Nimbus D, Revision 1 Handbook, which outlines the Thermal/Vacuum test profile for Electro-Mechanical Subsystems. Upon this basis, an analytical steady state thermal evaluation was presented in Vol. I of the Design Study Report. Following selection of a spacecraft contractor, RCA Installation Drawing 8370948, 3 August 1970, was submitted. Both documents define essentially the same requirements for thermal sinks — both radiant and conductive. Recent communications indicate that the planned spacecraft installation is compatible with these sink requirements, although some questions as to Recorder duty cycle remain open.

The Design Study Report was reviewed at the Design Review Meeting of October 20, 21 and 22, 1970. During the review, NASA questioned the value of thermal conductivity through a silicone rubber material, which RCA had given as 23 BTU/hr/ft^2/in/°F. This, in fact, is incorrect; published values of conductivity through such materials vary approximately from 1 to 3 BTU/hr/ft^2/in/°F.

3.3.2 Present Status. - As a result of the error found to exist in the steady state analytical evaluation presented in the Design Study Report, three avenues of investigation were opened:

(1) The steady state program was re-run using a Thermal conductivity value for silicone rubber of 2 BTU/hr/ft^2/in/°F. The results of this evaluation versus the values of Δt and Q reported in the Design Study Report are given in Figure 3-5. For this change, note that the temperature rise above sink for the motor board went from $\Delta t = 17.0°F$ to $\Delta t = 24.8$, an additional rise of approximately 8°F. (Other minor differences are also shown in the Figure.)

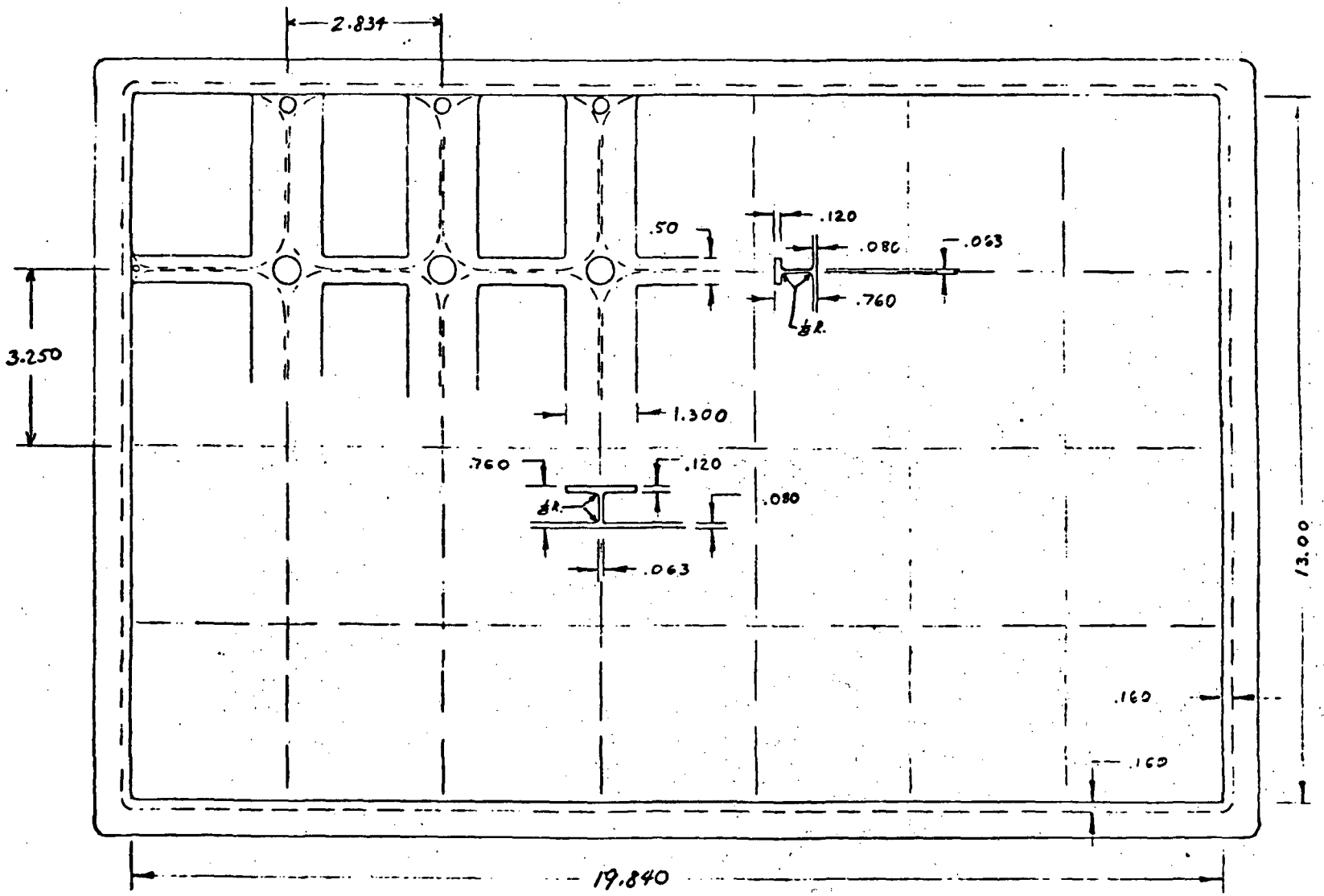
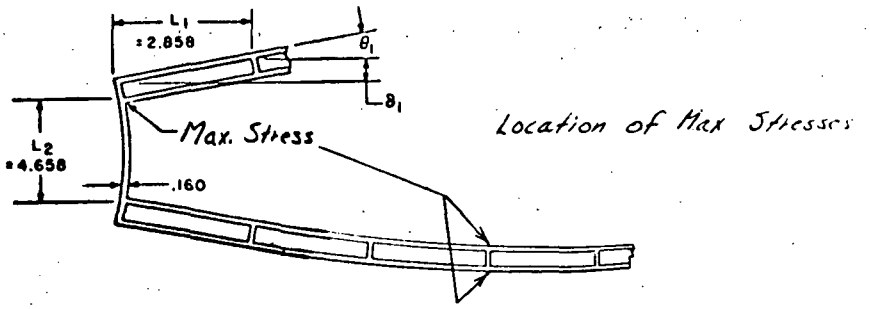


Figure 3-3. ERTS Enclosure Integral Design Constructional Sketch (Second Revision)

CALCULATED MAXIMUM STRESSES

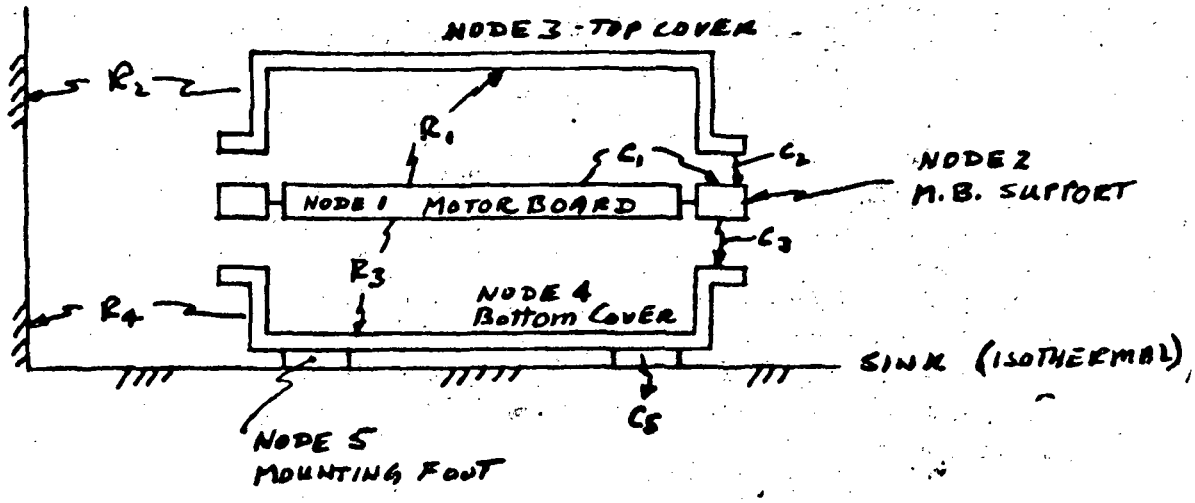


Parameter	Nominal Value	Comments on Deviation from Nominal Value
1. Upper and Lower Wall Stress		
a) Outer Skin	+14.2 KPSI	Small stress raisers due to corner radii (10-20%) and treatment of shear lag.
b) Flange	-10.2 KPSI	
2. Side Wall Stress	±10.2 KPSI	Moderate stress raisers due to discontinuities at rib-side wall junction, stress reductions due to neglect of flanges.
3. End Wall Stress	±10.7 KPSI	
4. Deflection of Upper and Lower Walls	.080"	Small ± errors due to assumed edge conditions, neglect of flange, and shear lag

Minimum: Mechanical Properties of ZK60A-T6 Magnesium Forging

	Max Strength Axis	Min Strength Axis
Tensile Strength, KPSI	46	40
Tensile Yield Strength, KPSI	28	22
Compressive Yield Strength, KPSI	25	21

Figure 3-4. ERTS Enclosure Stress Calculations



R_1, R_2, etc. - Radiant Transfer Paths

C_1, C_2, etc. - Conductive Transfer Paths

			Δt (above sink) °F		Q-BTU/hr.	
			K=23	K=2	K=23	K=2
Node	1	Motor Board	17.0	24.8		
Node	2	Motor Board Support	10.7	7.0		
Node	3	Top Enclosure Cover	10.0	8.6		
Node	4	Bottom Enclosure Cover	6.8	4.3		
Path	R_1	Motor Board to Top Cover			31.7	73.5
Path	R_2	Top Cover to Sink			45.6	39.1
Path	R_3	Motor Board to Bottom Cover			37.6	76.0
Path	R_4	Bottom Cover to Sink			25.4	15.7
Path	C_1	Motor Board to MB Mount			95.7	23.4
Path	C_2	Motor Board Mount to Top Cover			13.9	34.45
Path	C_3	Motor Board Mount to Bottom Cover			81.7	57.8
Path	C_4	Bottom Cover to Mounting Feet			93.9	118.1
Path	C_5	Mounting Feet to Sink			93.9	118.1

NOTE: The analyses contain the following differences:

In analysis where K=23: Total Heat Load is 165 BTU/hr.
In analysis where K=2 : Total Heat Load is 173 BTU/hr.
In analysis where K=2 : Mounting Foot, Node 5 and bottom cover, Node 4 are Isothermal, whereas the analysis wherein K=23, a low resistance between nodes 4 and 5 was used.

Figure 3-5. Transport Thermal Chart

(2) A search was initiated for methods of increasing the thermal conductivity between the motor board and the surrounding structure while retaining the electrical isolation and mount compliance requirements. Working through the existing mounting system, various electrically isolated spring systems were evaluated. Additionally, the use of electrically-isolated "ground strap" thermal conductors to fit with the present configuration was tentatively explored, with inconclusive results. A search is in progress for an alternate material, specifically formulated for thermal conductivity, to directly replace the silicone rubber isolators. To date, an RCA developed formulation of alumina-filled urethane, used on space programs dating back to Ranger, appears promising.

(3) A test series designed to evaluate the actual temperature distribution of an operating transport unit has been initiated on a "unit availability" basis. These tests are being conducted on the Engineering Model Transport Unit with the test results intended as verification of analytical data.

In light of the now marginal temperature condition shown by the latest steady state evaluations, it is thought advisable to enter into a transient analysis based upon an actual recorder duty cycle. Recent interface meetings indicate that maximum operate time for the recorder appears to be only 20 minutes per 103 minute orbit.

3.4 EM Transport Vibration Test

Engineering level vibration tests were performed on the EM transport, mounted in the original lower enclosure. The upper enclosure was omitted for purposes of visibility and instrumentation. However, its flange stiffening effect was roughly simulated by the addition of lengths of angle iron. Accelerometers were mounted on three points on the deck, on the headwheel motor and on one tab of the "picture frame."

Initially, a low-level survey was made with a constant ±1g sinusoidal excitation normal to the tape deck (a lateral plane). This was done for three types of deck mounting:

a. The deck "hard-mounted" (without rubber isolators) to the frame.

b. The deck "soft-mounted" (with rubber isolators) to the frame.

c. The deck "soft-mounted", plus a damper strip.

Sample X-Y plots, showing the accelerometer reading at the center of the deck, are given for these three types of mountings in Figures 3-6 through 3-8.

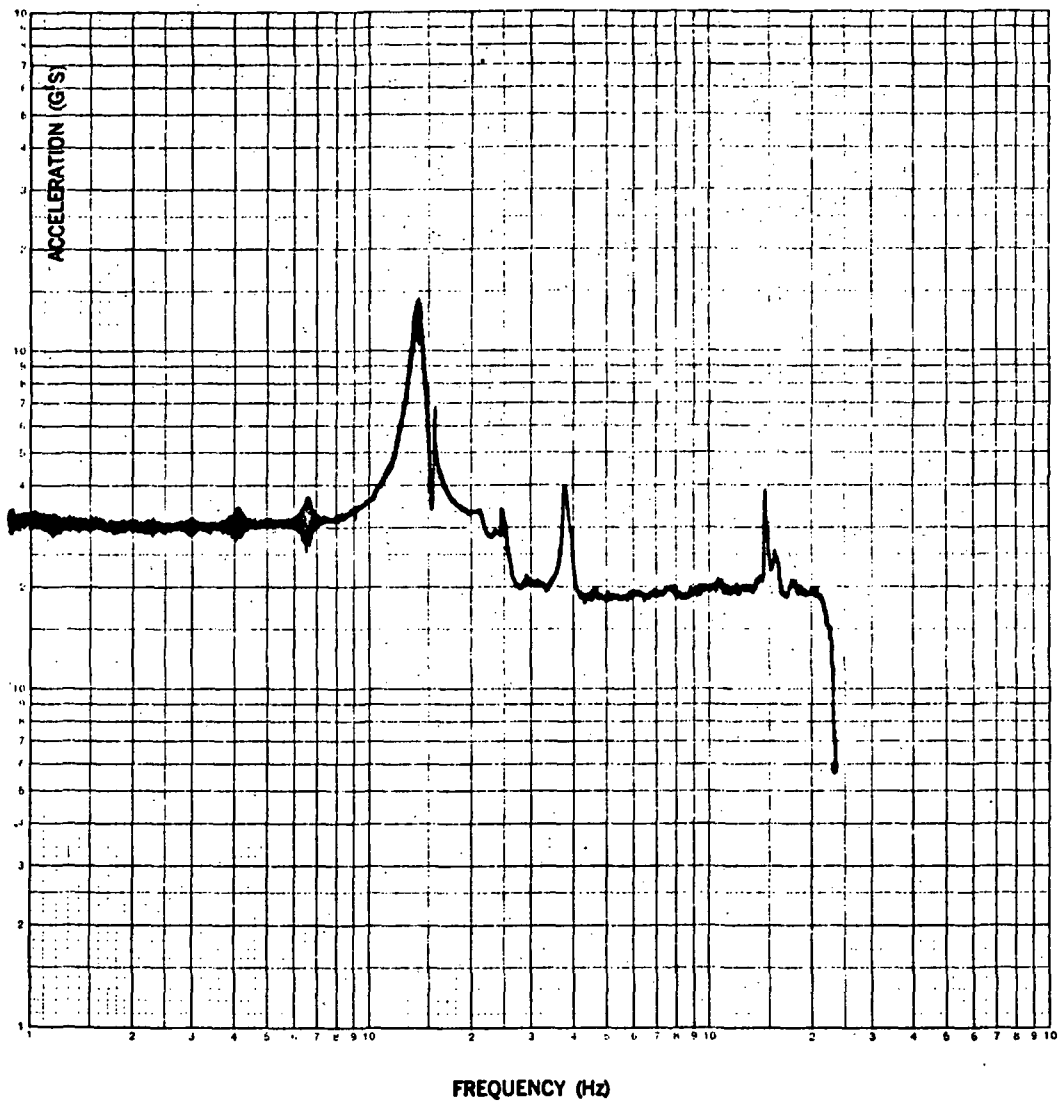


Figure 3-6. EM Transport Vibration Test (Hard-Mounted)

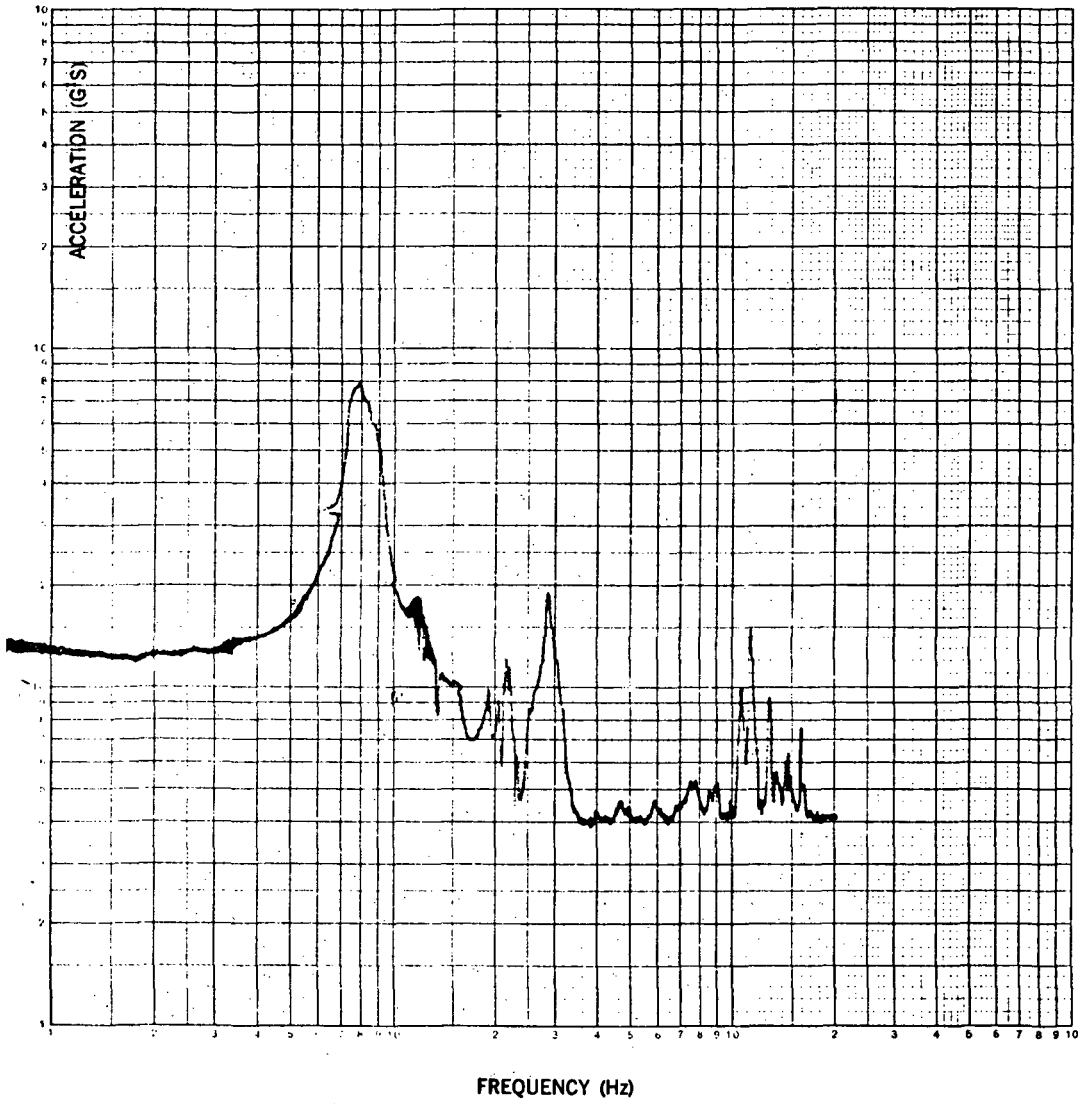


Figure 3-7. EM Transport Vibration Test (Soft-Mounted)

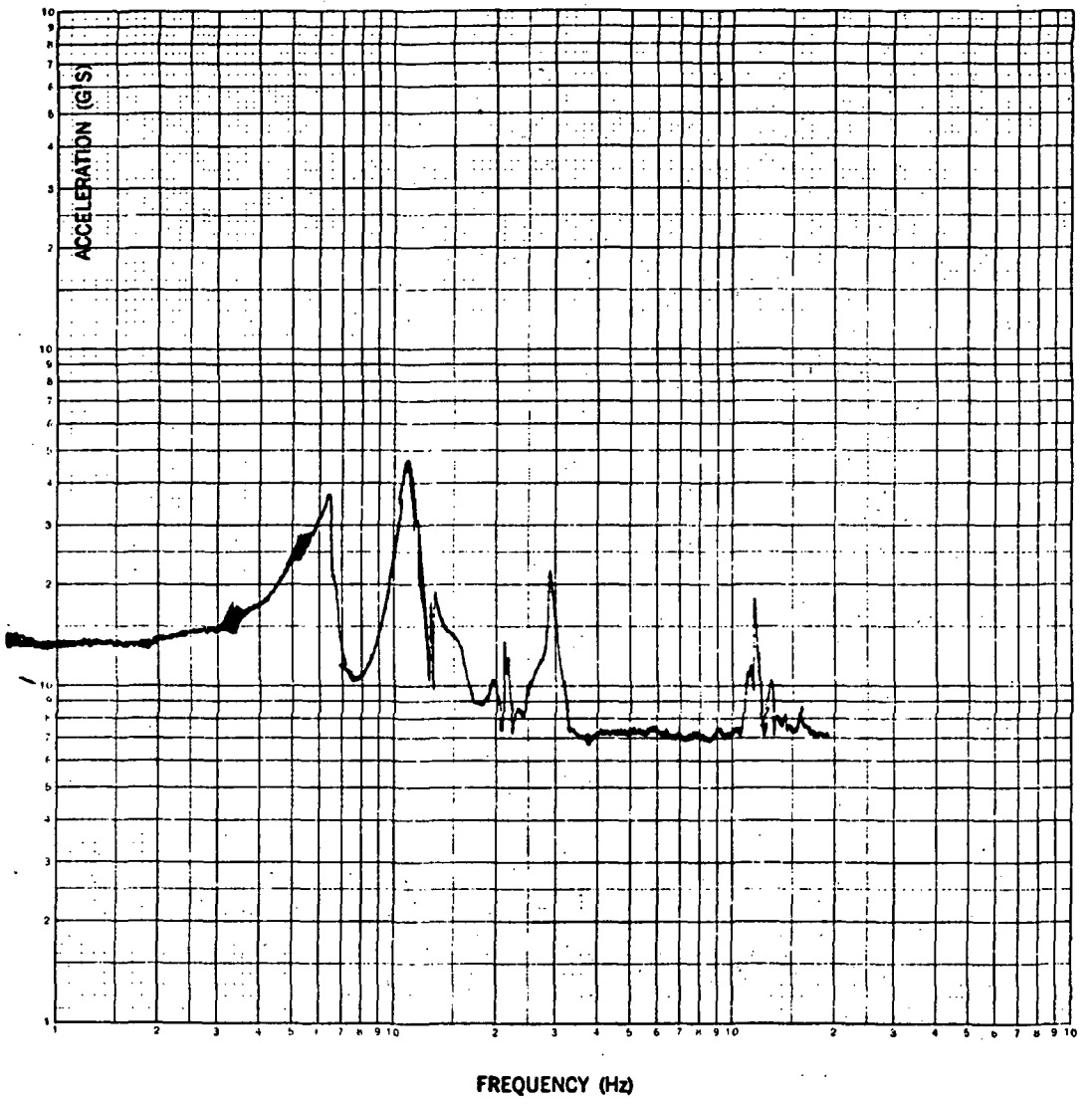


Figure 3-8. EM Transport Vibration Test (Soft-Mounted, with Damper)

The transport was then given full qualification level sine sweep and random excitation in all three planes. Due to the obvious improvement effects of the damper strip, it was retained for these tests. X-Y plots of the accelerometers were obtained for each run. At the end of each run the transport was operated mechanically to check for gross malfunctions.

Two failures occurred, both of which are not considered to be associated with a design problem. At the end of the first sine sweep, three full tape passes were made and, during the third pass, the tape caught and tore in the shoe. This is believed to have been caused by a small particle which entered the tape path, due to the absence of the top cover, during testing or transportation. In any event, no repetition of this occurred during the five subsequent runs.

The second failure, a sudden stop of the headwheel, was observed when the transport was being operated after completion of all vibration testing. It was found that one of the balancing screws had worked its way out sufficiently to hit the shoe. This occurred because a standard set screw had been installed by engineering personnel during the strike, instead of the required self-locking type of screw. Subsequently, it was found that a shoe flexure had cracked. It appeared, fairly conclusively, that this had been caused by impingement of the protruding balancing screw. The reasons for this conclusion were gouging marks, on a screw head and corner of the guide, which were in the rotational path of the protruding screw. An examination by our Materials Laboratory showed no abnormal material property or surface condition present in the vicinity of the crack.

3.5 Transport Unit Weight Summary

The updated Weight Control Report (Figure 3-9) shows an increase of 1.7 lbs in the TU (since February 1970) to a total weight of 45.13 lbs. This weight was verified by the actual weighing of the Engineering Model Transport Unit and adding the differential weights of those components which will change in the final configuration. These differential weights are the re-designed enclosure ($\Delta W = +0.9$ lbs) and the Differential/Negator Assembly ($\Delta W = +0.55$ lbs). The Differential/Negator Assembly weight increase results from improvements in the reel drive transmission system. The increase in enclosure weight is based upon actual measurement of a nearly complete upper enclosure of the new design. This item will be reviewed when dimensional inspection of the enclosure is complete.

ASSEMBLY NAME	DRAWING NUMBER / SERIAL NUMBER	UNIT WHT TARGET	QTY PER EQUIP	TOTAL TARGET EQUIP WHT	ESTIMATED/ACTUAL WEIGHTS					
					7 AUG 1969	10 SEPT 1969	15 NOV 1969	2 FEB 1970		DEC. 1970
REEL ASSEMBLY			QTY	(2)	4.0E	4.0A	4.0A	4.00A		4.00A
DIA SENSING			QTY	(2)	.60E	.60A	.60	.60A		0.60A
TAPE GUIDES			QTY	(5)	.90E	.80A	.80A	.80A		0.80A
ERASE HEAD					.25E	.25E	.25E	.25E		0.25E
H. W. PANEL					2.60E	2.60E	2.35A	2.35A		2.35A
AUX HD.					.25 E	.25 E	.25 E	.25 E		0.25E
CAPSTAN					.50 E	.47 A	.47 A	.47 A		0.47A
CAPSTAN MTR					1.80E	1.40A	1.40A	1.40A		1.40A
DIFF/NEG ASSY.					5.00E	5.00E	4.35A	4.35A		4.900A
H. W. IW					2.60E	2.00A	2.00A	2.00A		2.00A
REEL IW					1.50E	1.70A	1.70A	1.70A		1.70A
TAPE DECK					4.60E	ALUMIN 8.50A	ALUMIN 8.50A	MAG 6.00A		MAG 4.80A
TAPE					2.90E	2.90E	2.90E	2.90E		2.90E
CASE & FRAME					10.3E	10.3E	10.9E	11.10E		13.29E*
CONNECTORS					.50E	.50E	.50E	.50E		.50E
MODULES, WIRING					3.70E	3.70E	3.70E	3.70E		SEE BELOW
MISC.					1.0E	1.0E	1.0E	1.00E		1.00E
MODULES										
VIDEO RECORD/PREAMP			QTY	(2)						1.33A
VIDEO PLAYBACK AMP										0.29A
AUX/SEARCH/PREAMP										0.25A
CONTROL TRACK/TACH PREAMP										0.20E
MOTOR SWITCH										0.85E
WIRE										1.00E
					43.00	45.97	45.67	43.37		45.13

*INCLUDES DECK MOUNT FRAME @ 1.3, 8 DECK MOUNTS @0.11, & CLOSE UP HARDWARE @0.33

Figure 3-9. Weight Control Report

4.0 FLIGHT RECORDER/REPRODUCER ELECTRONIC UNIT, ELECTRICAL DESIGN

4.1 WIDEBAND CHANNELS

The wideband channels of the ERTS recorder system are handled by means of a transverse scan recording system. A headwheel containing four magnetic heads scans the tape at high speed and at right angles to the tape motion. In order to permit the recording and reproduction of a continuous channel of information, the signal processing shown in Figure 4-1 is performed. The video input information generates a continuous flow of FM information. The signal is then subdivided into two channels; one covering information going to scanning heads 1 and 3, the other to scanning heads 2 and 4. This information is switched electronically so that recording power is applied only to the scanning head that is in contact with the tape. The bottom of the figure shows diagrammatically the sequential sections of information recorded on the tape. Note that there is some overlap in the stored information during the recording process.

On playback, the individual heads play back the transversely recorded information (Figure 4-2). The individual output signals are combined into 1-3 and 2-4 FM channels. Since the information in each of these channels would be discontinuous, a fill-in operation is performed so that, in fact, each information channel in the FM domain will have a continuous flow of information. (Note again the overlap period between the primary information channels.) The FM signal is subsequently demodulated by two separate circuits. Note, however, that any timing discontinuity in the FM information channel (such as may be caused by slight playback tape scanning errors) will result in a switching spike in each of the two separate output channels. To remove the switching spikes, the baseband information is combined into a single channel by switching the video signal from one head to the next toward the end of the overlap period. The video switch is extremely fast and will not cause output spikes that extend beyond the normal system noise level.

In handling the RBV (Return Beam Vidicon) signals, the head switching occurs synchronously with the scanning rate of the raster. In this manner, any playback scanning error will only modify the horizontal line length, but will not cause timing errors within the picture display. In the MSS mode, any playback scanning error is removed by use of a digital buffering system.

Figure 4-3 shows, in block diagram form, the manner in which the RBV and MSS signals are handled in the Electronic Unit of the recording chain. The 3.5 MHz RBV signal is amplified, pre-emphasized and dc level shifted to give the proper frequency deviation to the FM modulator. This signal is then transmitted to the record current adjust module where, by remote command, the recording level can be adjusted to compensate for wear of the video heads.

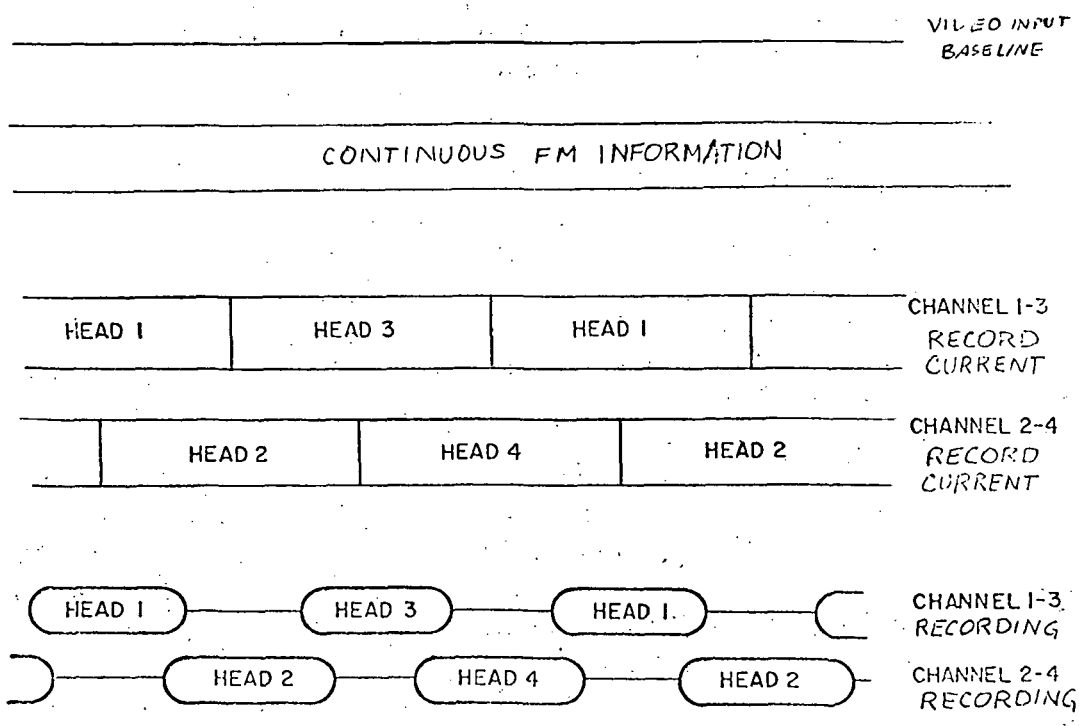


Figure 4-1. Basic Transverse Scan Recording Process

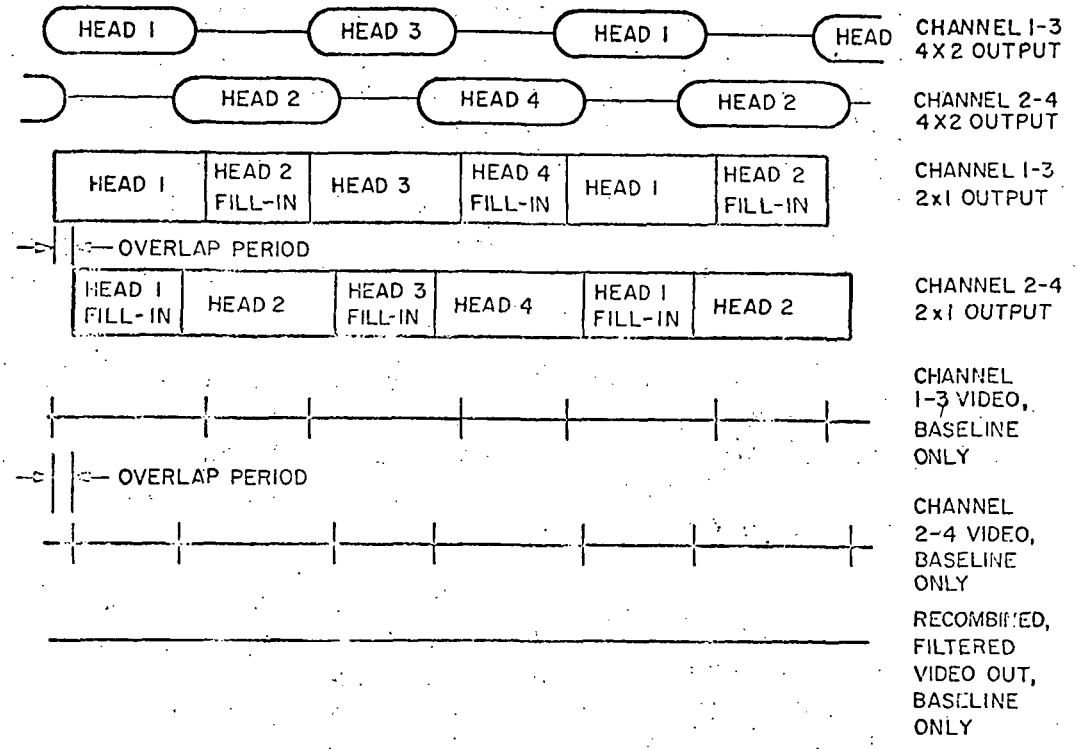


Figure 4-2. Basic Transverse Scan Playback Process

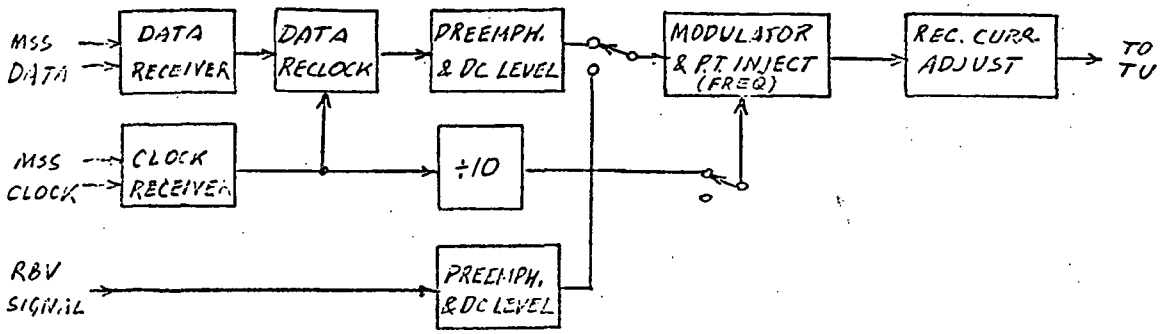


Figure 4-3. Electronic Unit Wideband Record

The 15 Mb/s MSS data and clock signals are received by balanced line receivers. The data is re-clocked to establish a controlled phase relationship between these two signal channels. The data is then pre-emphasized and dc level shifted to give the proper frequency deviation to the FM modulator. The clock signal is divided by 10, yielding a 1.5 MHz sine wave. This signal is added to the modulator and constitutes a pilot tone signal which is required for proper decoding of the MSS information. These two signals are then introduced to the record current adjust module, from which they go to the Transport Unit.

Figure 4-4 shows the manner in which the RBV or MSS FM signals are handled in the Transport Unit. The circuits to be described have to be housed in this unit, as these signals must be in close proximity to the video record/playback heads.

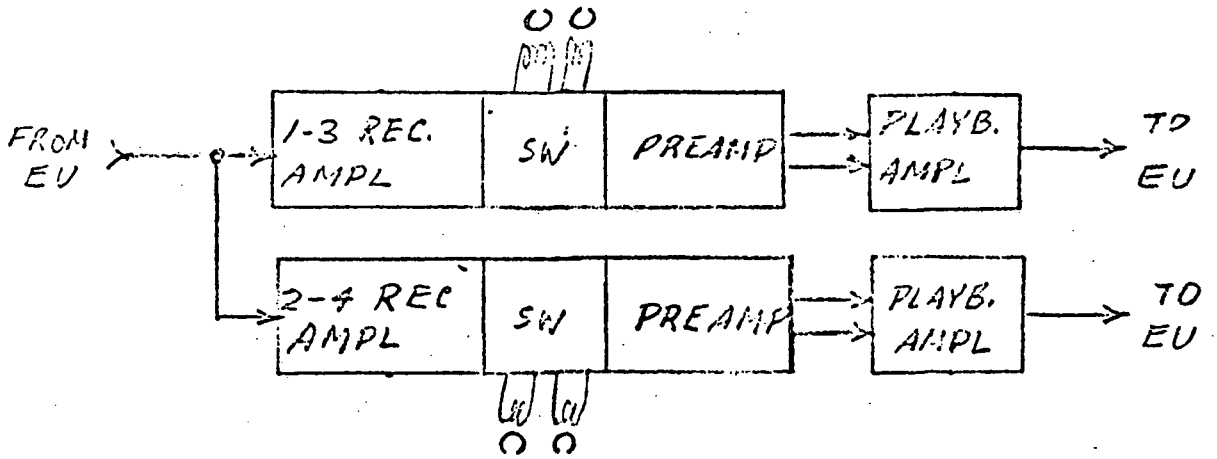


Figure 4-4. Transport Unit Wideband Channels

The incoming FM signal is divided into the 1-3 and 2-4 recording chains. These signals are then amplified to a sufficient level for recording on the magnetic tape. Specifically, the output from the record amplifiers goes through a record/playback relay to the headwheel panel assembly. There, the signal is transferred through a rotary transformer assembly to the video heads proper.

Upon playback, the signals induced in the video heads pass through the rotary transformers and the record/playback relays to four individual preamplifiers. From there, the signals go to two playback amplifiers: one for channels 1-3, the other for channels 2-4. The playback amplifiers provide some aperture (cosine) equalization for the signal, and generate enough signal level for transmission to the Electronic Unit.

Figure 4-5 shows the wideband signal processing in the Electronic Unit. For the RBV mode, the 1-3 and 2-4 playback signals are introduced to two equalizers which further equalize the high frequency response of the playback signal. These units also contain a linear roll-off circuit which improves the overall signal to noise performance of the recorder system. The two FM output signals are then introduced to two limiter/-demodulators to recover two baseband information channels. In these circuits the video pre-emphasis is also removed and a sharp cut-off, low-pass filter separates the baseband information from the FM carrier signal. The resultant video signals chain is finally combined into a continuous RBV signal by means of the video switch and driver circuitry.

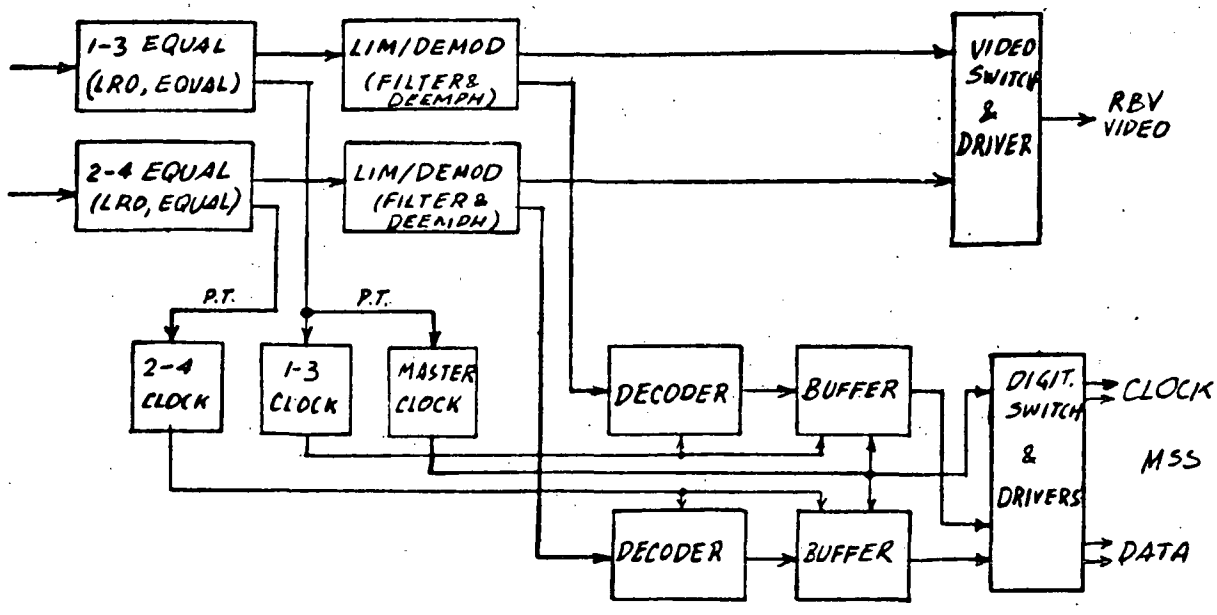


Figure 4-5. Electronic Unit Wideband Playback Channels

The recovery of the MSS information proceeds, in part, in a manner similar to that of the RBV signals. However, the equalizers are also used to extract the pilot tone information that was initially added to the FM information channel. From the pilot tone signals, two variable clock signals are developed: a 1-3 and a 2-4 clock signal. These clocks follow the exact timing of the video playback signals. A master clock signal, which follows only the long term average of the pilot information, is also developed.

The variable clock signals are used to operate the decoders where the baseband video information derived from the limiter/demodulators are strobed to recover the original digital information. The variable clocks are also used to strobe the recovered digital data into the buffers. Read out of both buffers is accomplished by means of the single master clock so that the data output of the buffers will contain a continuous flow of information compensating for any playback scanning (shoe) errors. The data channels thus derived are combined by a digital switch into a single output signal. A final reclocking operation takes place and the data and clock output signals are made to conform to the desired format.

For proper operation of the buffer, proper timing operations are required. This timing is derived directly from the pilot tone signals. In particular the zero-crossings of the 1.5 MHz pilot tone result in a unique phase relationship of the 15 MHz clock signals. The information thus available can be used to assure proper read-in and read-out of the buffer. (A more detailed discussion of the buffer phasing operation is covered in Paragraph 4.1.3.3).

4.1.1 RBV System Circuit Description. - The circuits used in the RBV system sometimes share the same boards used in the MSS system. Moreover, the required functions are frequently performed by the same board. For this reason, the boards required for the simpler (RBV) system are discussed first. Commonality will be covered during the discussion of the MSS system.

Presentation of circuits is in the order of signal flow.

4.1.1.1 Input Network (Figure 4-6). - The MSS input and RBV input networks are built on a single board. The RBV source impedance is a 75-ohm shielded line. A potentiometer across the input is used to adjust the signal range. After a slight amount of high frequency pre-emphasis, the signal feeds U8, a balanced input differential amplifier with a dc gain of approximately 10 dB. The output of U8 is then attenuated by about 3 dB and fed to a matched transistor pair (U9) connected as an emitter follower. Potentiometer R47 is used to fix the RBV dc level at the modulator input to approximately -0.75V to +0.75V.

4.1.1.2 FM Modulator (Figure 4-7). - The FM Modulator converts the base-band video signal into the required FM format. The same device is used for RBV and MSS; however, the quiescent frequency and the deviation is switched in the RBV/MSS Input module to obtain optimum system performance for either service.

The FM Modulator is a balanced direct modulator. The required input signal 180° phase shift is provided by complementary emitter followers. Two emitter follower stages and a 6.2-volt Zener diode in series with each input generate the nominal oscillator bias.

Both the high frequency (HF) and low frequency (LF) oscillators are variations of the standard Colpitts variable frequency oscillator. The tank circuit of each oscillator contains a voltage-variable capacitance diode (Varicap) with a nominal capacitance of 47 pF. In general, as the reverse voltage across the varicap increases the capacitance decreases, which results in an increase in oscillator frequency. The nominal operating point (100 MHz) provides an oscillator sensitivity of approximately 1.5 Khz/mV, or a difference frequency deviation of 3 kHz/mV. This sensitivity results in a RBV and MSS deviation of 8.35 ± 2.25 MHz and 12.75 ± 0.75 MHz respectively.

Emitter followers at each of the oscillator outputs feed a transformer-coupled, diode-bridge mixer (see Figure 4-8). The output of the mixer feeds a notch filter which rejects the unwanted sidebands and extracts the oscillator difference frequency.

The filtered FM signal is combined with the 1.5 MHz pilot tone in the FM Amplifier (Figure 4-9), before being fed to the record current attenuator and record amplifiers.

The FM and pilot tone signals are combined in a differential amplifier with a gain of about 30 dB. This stage is followed by a wideband current amplifier with a maximum output impedance of 10 ohms.

4.1.1.3 Record Current Adjust. - The Record Adjust Circuit provides a means for remote adjustment of the record current to compensate for normal record head and tape wear. A 0 to 7 dB attenuation range is available in 1 dB increments; also, during the Return Beam Vidicon (RBV) mode of operation, an additional 8 dB of attenuation results. (Exact attenuation values will be determined after Life Tests.) Ground station monitoring of each of the three attenuator states is available through three binary coded telemetry signals; 1 dB, 2 dB and 4 dB.

The Record Adjust Schematic is shown in Figure 4-10. FM input attenuation is provided by grounding capacitors C1, C2 and C3. Emitter follower, Q1, is used for isolation and to buffer the RBV control switch, Q2. Latching relays K2 through K4 are connected as a three stage binary counter controlling attenuator switches SK2

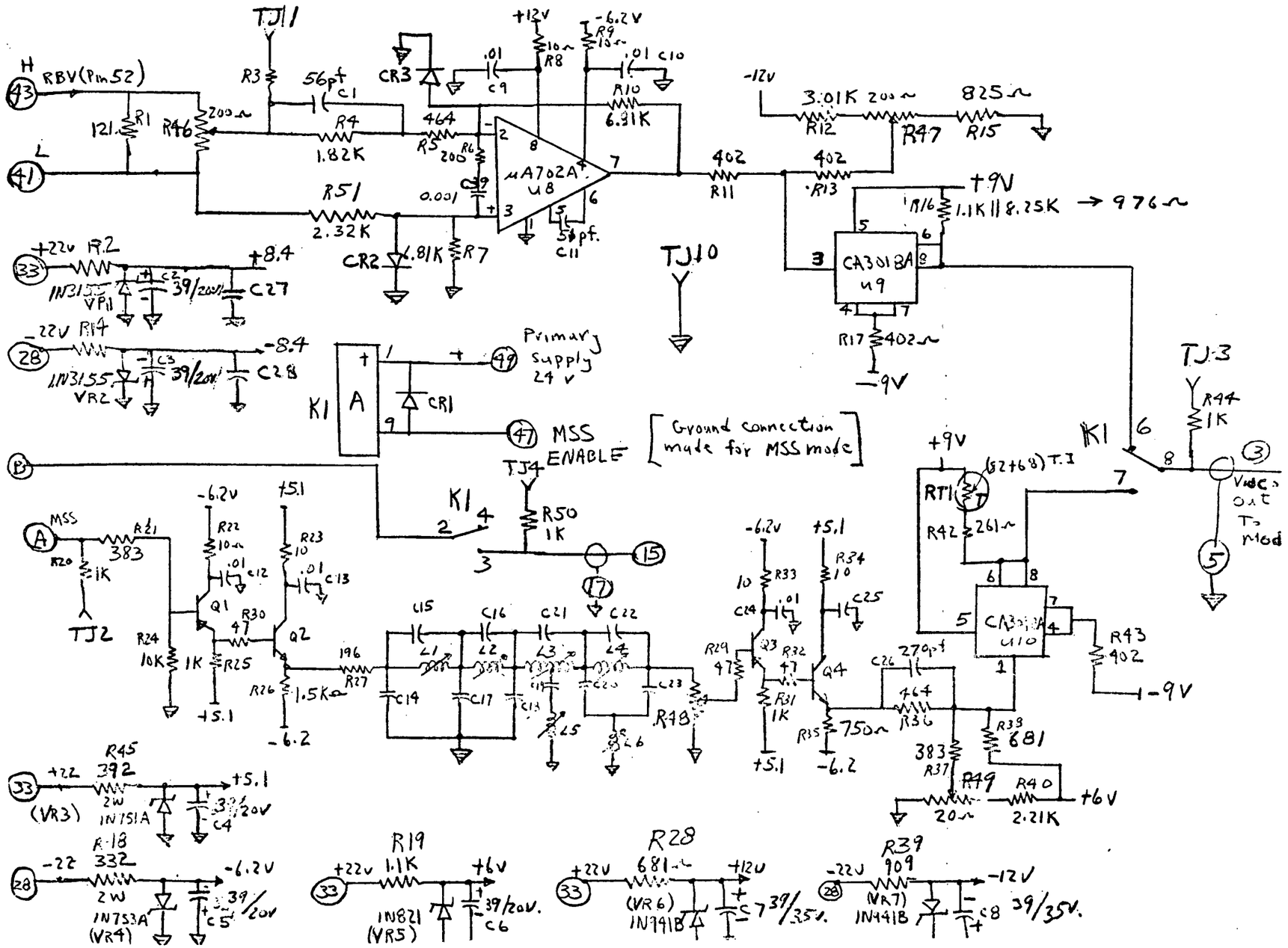


Figure 4-6. MSS/RBV Input Circuit Schematic Diagram

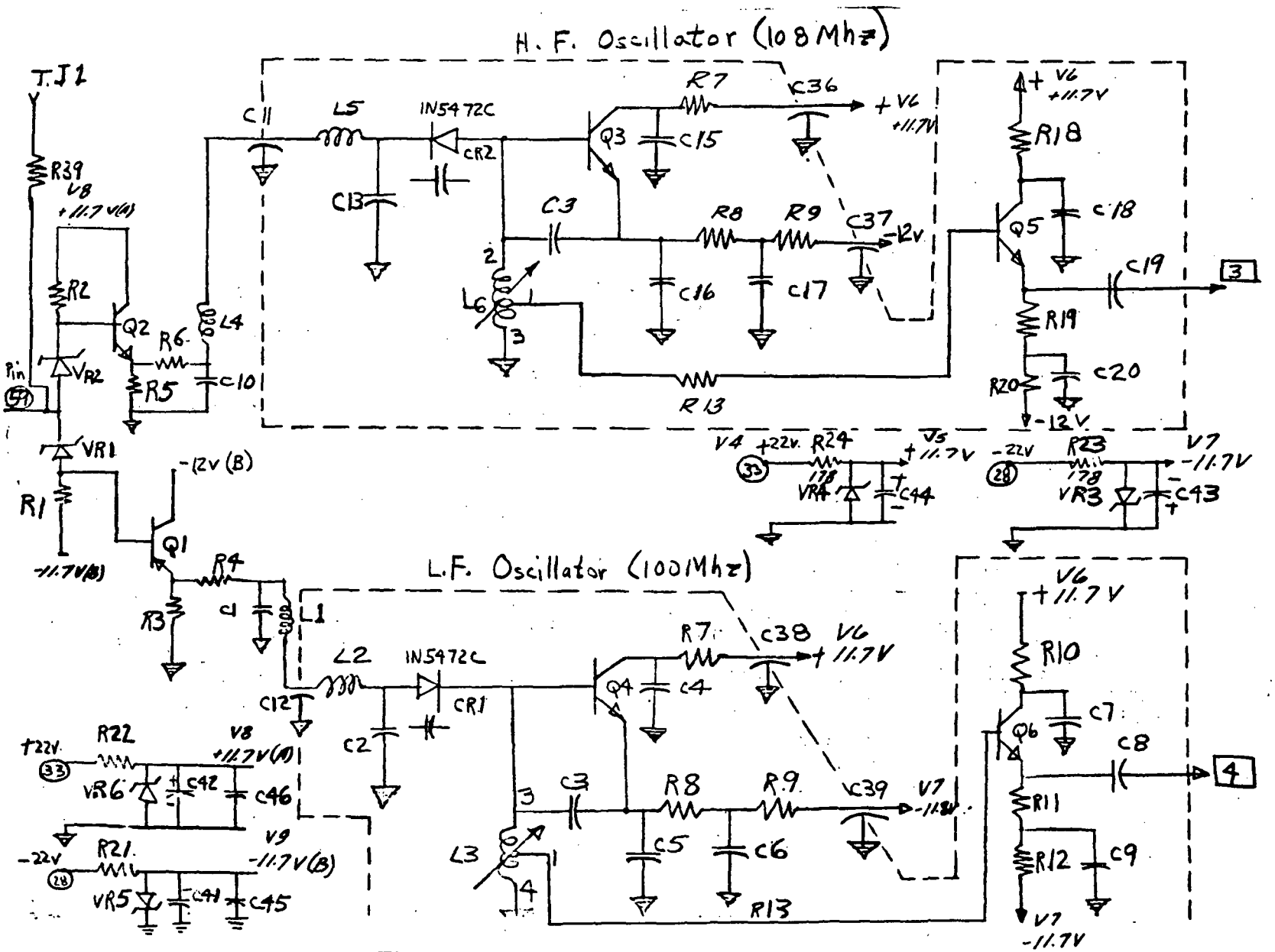
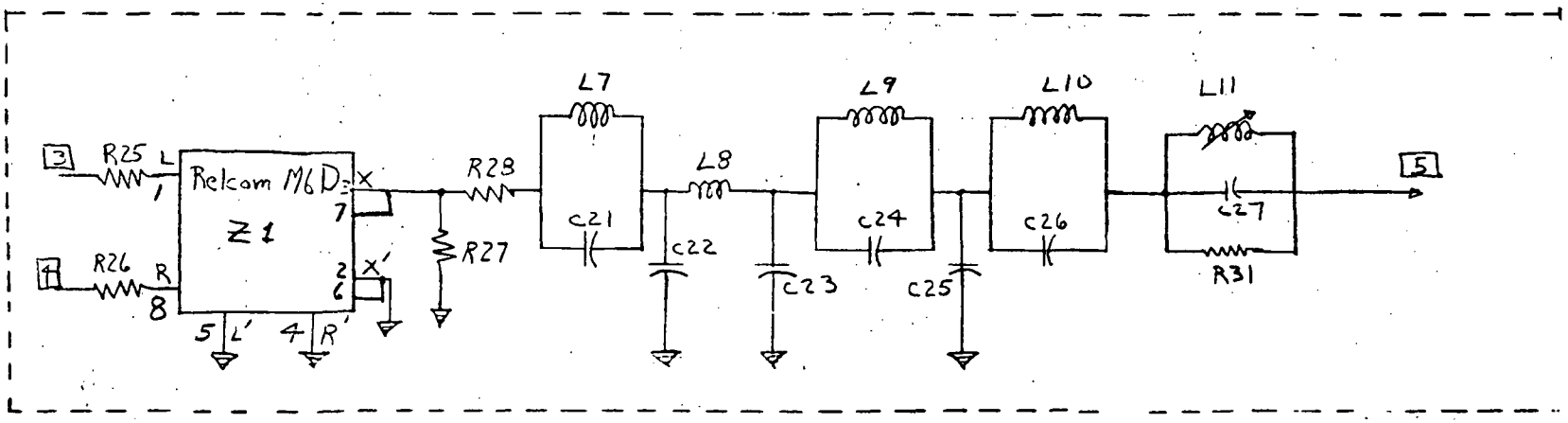


Figure 4-7. FM Modulator Schematic Diagram



Notes:

1) All inductors - shielded Miller coils
2) All capacitors - eric
3) All resistors 1/4 watt, 5%

Figure 4-8. Mixer/Band Pass Filter/Notch Filter Schematic Diagram

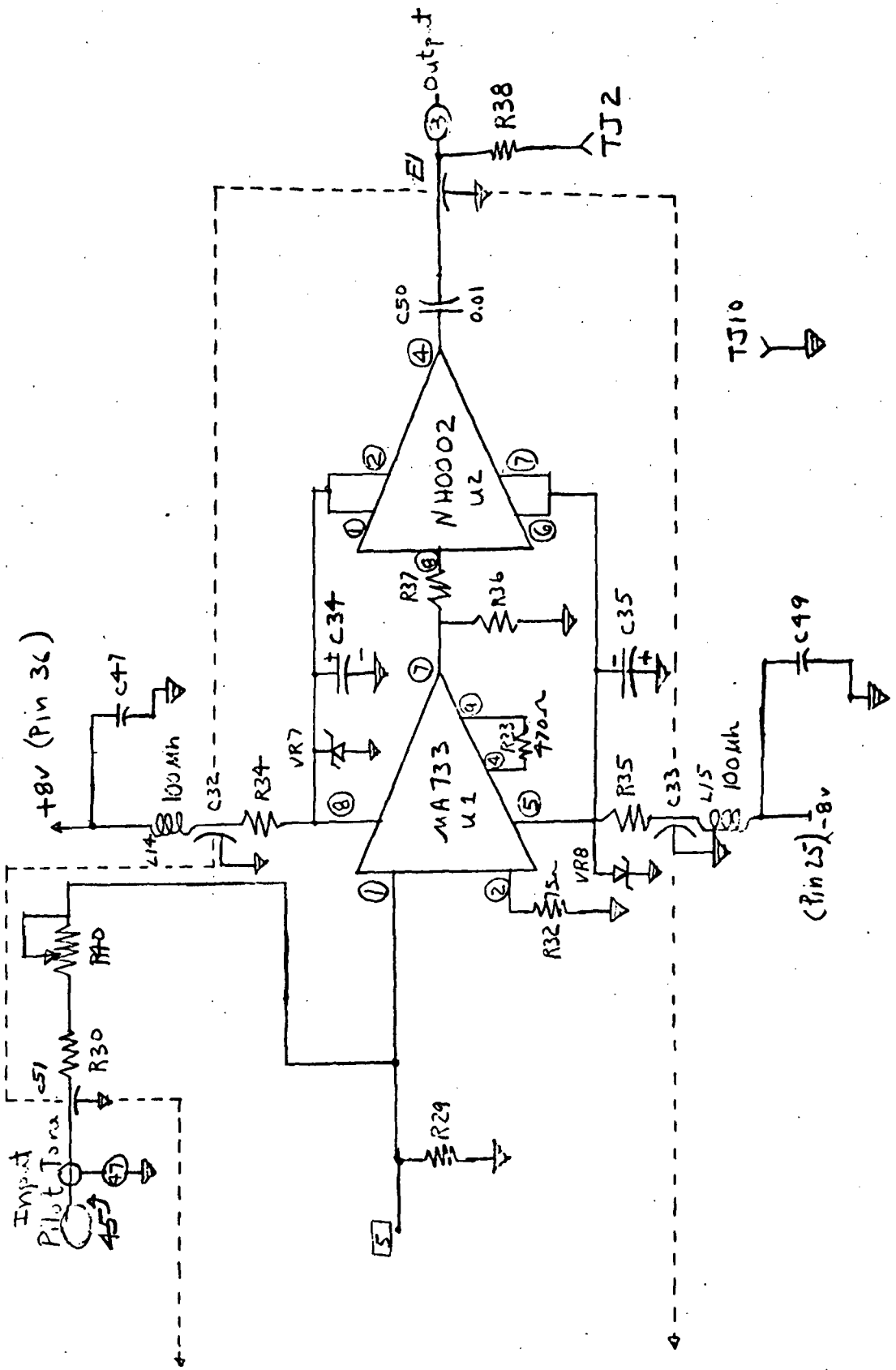
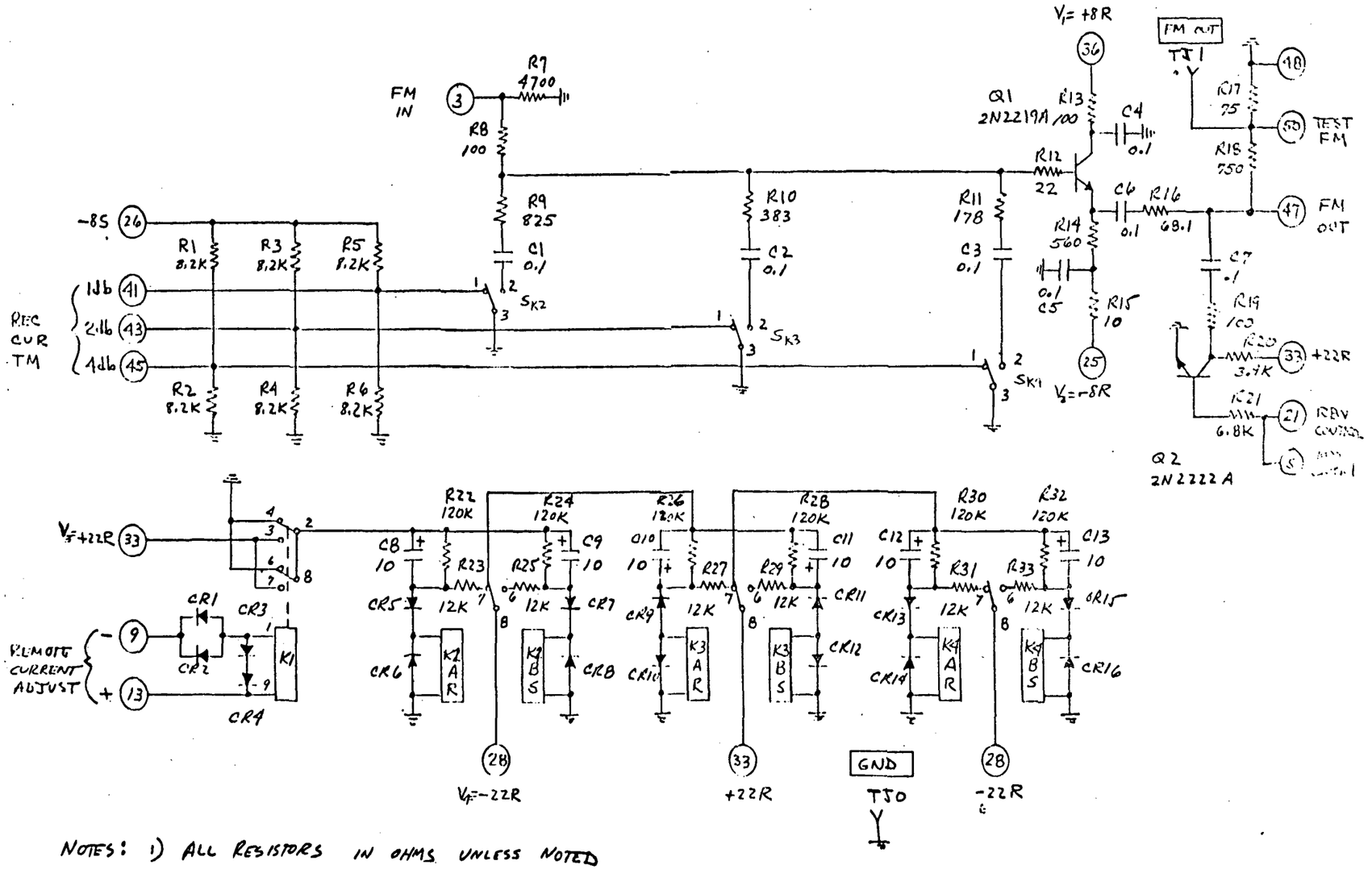


Figure 4-9 FM Amplifier and Line Driver Schematic Diagram



NOTES: 1) ALL RESISTORS IN OHMS UNLESS NOTED

2) ALL CAPACITORS IN UF " "

3) ALL CR IN645

Figure 4-10. Record Adjust Schematic Diagram

(2^0), SK3 (2^1), and SK4 (2^2) respectively. The serial remote control pulses switch relay K1 which in turn triggers the binary counter. Table I shows the counter truth table versus the number of input pulses.

TABLE 4-1. REMOTE CURRENT ADJUST COUNTER TRUTH TABLE

Pulse	Attenuation	Latching Relay State		
		K2	K3	K4
1	1	1	0	0
2	2	0	1	0
3	3	1	1	0
4	4	0	0	1
5	5	1	0	1
6	6	0	1	1
7	7	1	1	1
8	0	0	0	0

4.1.1.4 Record Amplifier, Preamplifier and Playback Amplifier. - These three circuits are housed in the transport unit. As their functions and physical arrangement have not changed since the initial design effort, the circuit descriptions covered in the Design Study Report, Vol. I, are still valid.

4.1.1.5 FM Equalizer. - Since the high frequency response of the playback heads falls off approximately as the cosine squared, signal equalization is required to compensate for the response variations prior to FM limiting and demodulation. Also, sufficient equalization is provided to compensate for signal-line capacitance. The FM signal to noise is improved by utilizing a two stage linear roll-off filter. The equalizer also provides the circuitry required to extract the pilot tone signal used in the MSS mode.

The FM Equalizer (Figure 4-11) consists of two identical channels; one half responds to the inputs from playback heads 1 and 3, and the other half is for the inputs from playback heads 2 and 4. Considering only the 1-3 inputs for descriptive purposes, a gate provides the fill-in signal between the 1 and 3 head signals by sampling the 2-4 input every 1.6 ms. The next stage feeds three networks, the RBV equalizer, the MSS equalizer, and the pilot tone extractor. Differential amplifiers are used to provide high frequency emphasis by taking the difference between two signals which exhibit a phase shift due to delay lines DL1 and DL4. To compensate for manufacturing tolerances, individual head equalization control is achieved

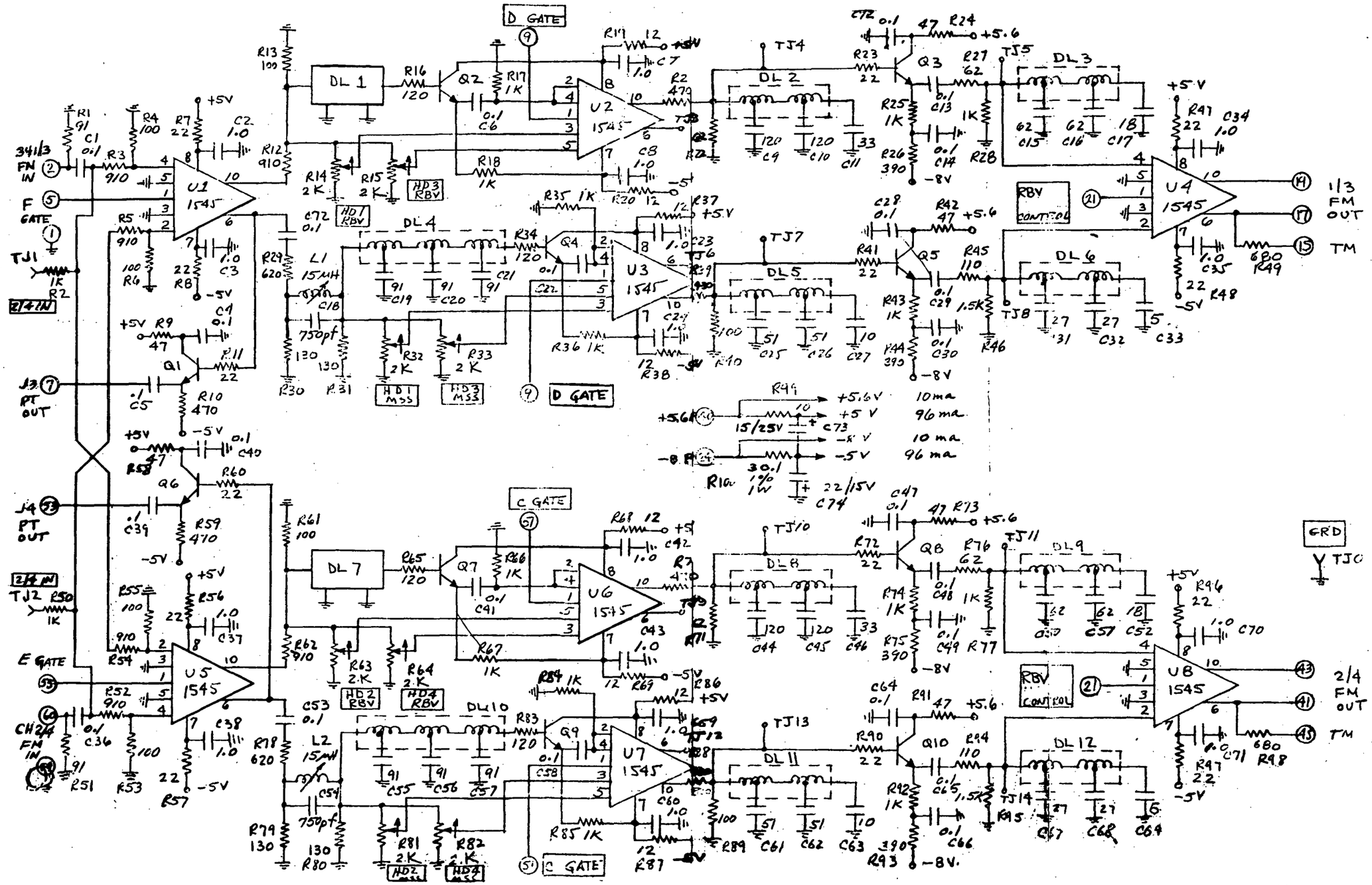


Figure 4-11. FM Equalizer Schematic Diagram

by adjustment of potentiometers for heads 1 and 3, respectively. The D gate signal, which is high (+3.5 V to +4 V) during the head 3 signal, switches the potentiometer reference level between heads 1 and 3.

Following equalization, the FM signal to noise ratio is improved with a two stage linear roll-off (LRO) filter. The filters are T sections of an m-derived, low-pass filter, which is characterized by a linear phase (constant group delay) response up to approximately 25% of cut-off frequency. For the RBV mode, the LRO filter null frequencies are 14 MHz at DL2 and 19.6 MHz at DL3. In the MSS mode, the null frequencies are 21 MHz at DL5 and 29 MHz at DL6. An output gate is used for RBV or MSS mode selection. When the gate level is 0, the system is in the MSS mode; when +4.5 V, the system is in the RBV mode.

4.1.1.6 Limiter/Demodulator. - The system requires two limiter/demodulators, one for heads 1-3 and the second for heads 2-4. Each of these circuits converts the FM waveform back to the original modulating signal. Prior to demodulation, the FM input is amplified in three differential amplifiers (Figure 4-12). This amplification and limiting removes amplitude variations which may be introduced by the transmission path, tape dropouts and bandwidth restrictions. After limiting, both phases of the FM signal are applied to a pulse shaper where a constant pulse width of approximately 23 ns is generated at each zero crossing. These pulses are applied to a diode detector bridge and the resultant dc output is integrated by an RC network and then amplified by an integrated circuit. The output of this stage feeds two parallel low pass filters; one path is for RBV video signals and the other path is for the MSS data. An operational amplifier in the MSS channel provides a dc offset for extraction of the carrier, and an emitter follower drives the MSS decoder.

4.1.1.7 RBV Video Output. - The two limiter/demodulators feed the Video Output circuit where the information is time-multiplexed into a signal channel, (See Figure 4-13.) In order to be compatible with the FET switch, the amplifier outputs are offset so that a negative level appears at the 2 x 1 switch inputs. Reference generator timing levels are level shifted through appropriate transistors to provide a negative triggering level to a high speed flip-flop which , in turn, gates the 2 x 1 switches. The multiplexed video is then fed to an amplifier which includes provisions for compensating for any remaining dc offset.

A 3-volt clamp is provided at the output of one of the amplifiers to limit the maximum signal swing that can occur on the output lines. A double emitter follower drives the RBV output filter (Figure 4-14).

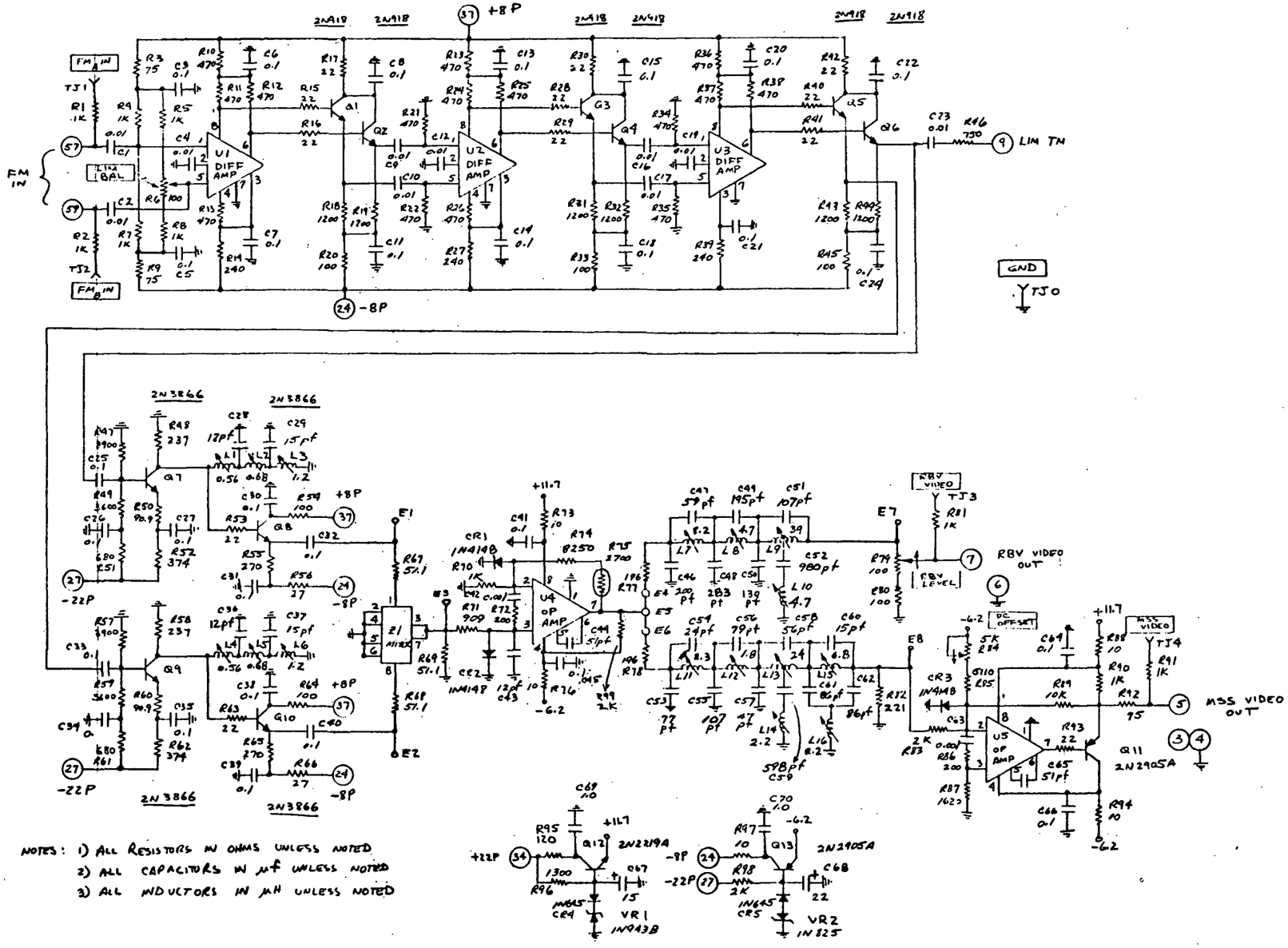
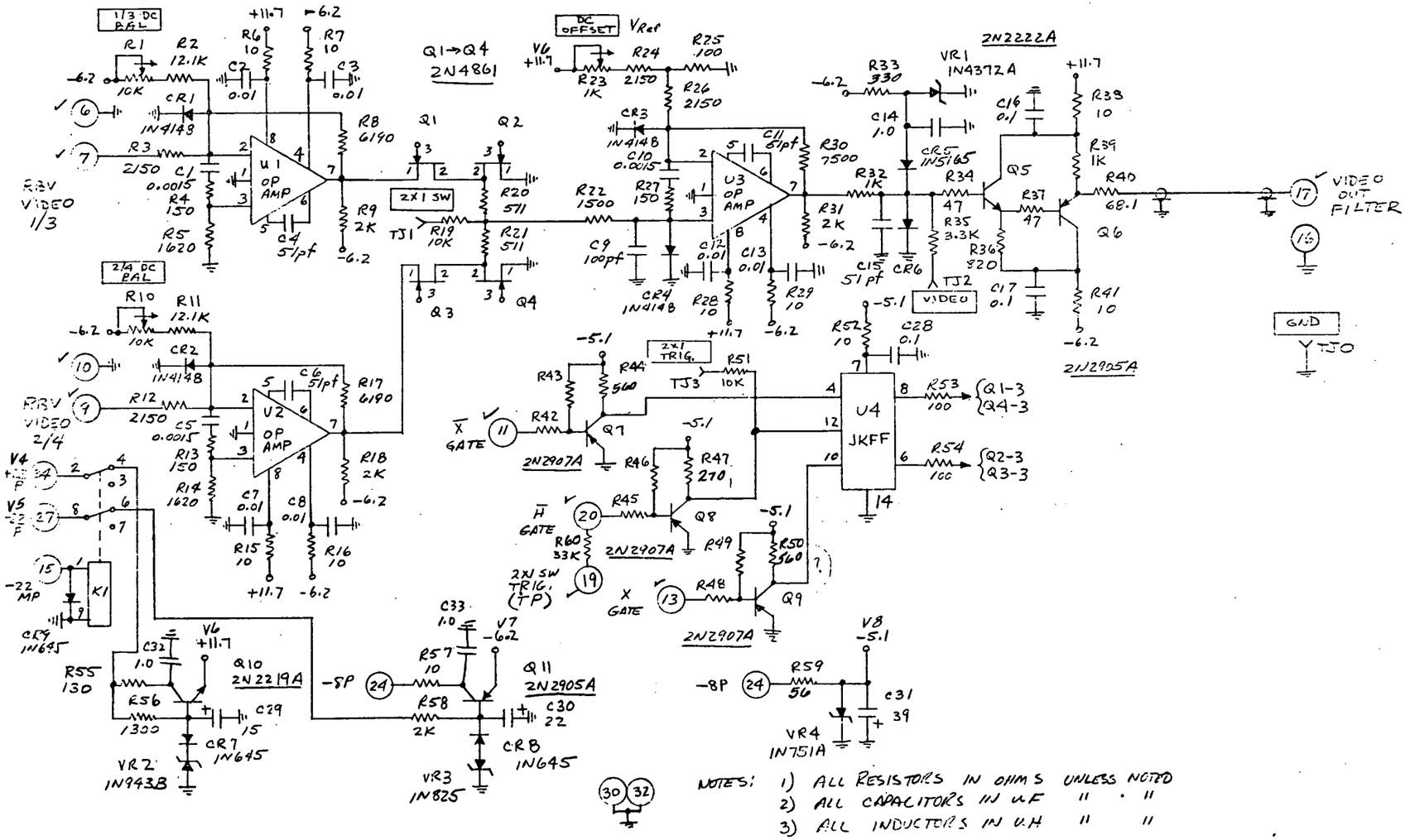


Figure 4-12. Limiter/Demodulator Schematic Diagram

TO BE REVISED



TO BE REVISED

Figure 4-13. RBV Video Out Schematic Diagram

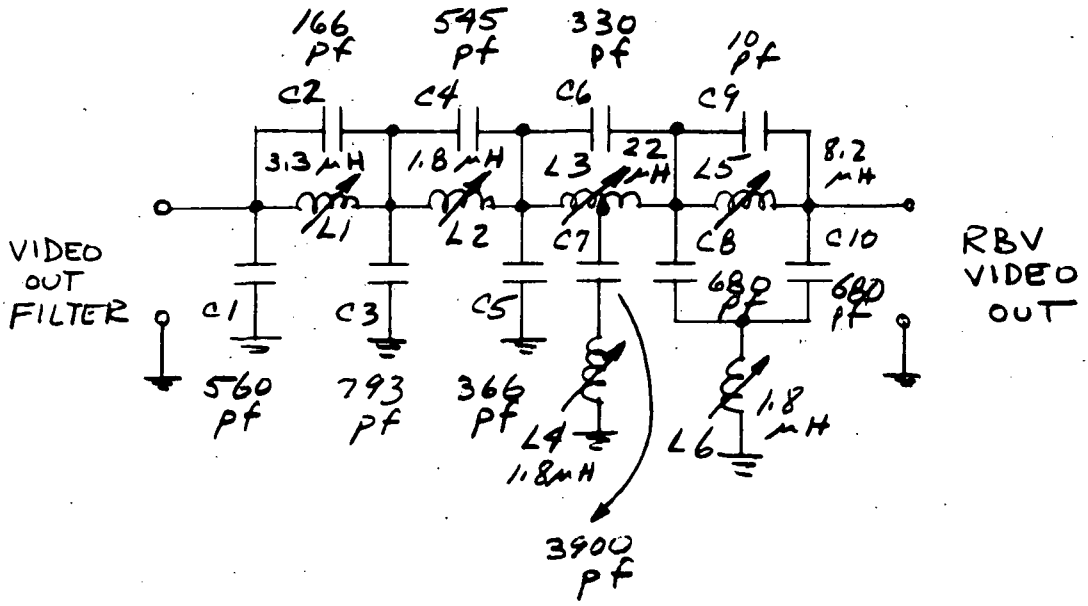


Figure 4-14. RBV Video Out Filter

4.1.2 Summary of RBV/MSS Input/Output Drift Analysis. - The RBV and MSS signal dc offset and gain variations have been summarized from the worst case analysis of the FM input/output networks in order to project the maximum input to output dc offset and gain drift due to temperature and aging. The RBV path consists of the RBV Input, Modulator, Limiter/Demodulator, and RBV Output circuits. During MSS operation the signal path is identical to the RBV path except for the MSS Input and Output networks.

4.1.2.1 Summary. - Detailed amplifier and component drift factors, as a result of temperature and aging, are given in the worst case analysis of each network. The total dc offset drift and percent gain variation for the MSS/RBV input and output stages are summarized in Table 4-2; as shown in the table, the resulting dc offset drift in millivolts for each network has been converted to percent of maximum signal range and referenced to the appropriate RBV or MSS output.

The total RBV dc offset drift is +11, -10.8 percent due to temperature and +17.1, -13.2 percent to aging. The record to playback gain variation is ±1.25 and ±10.7 percent due to temperature and aging, respectively. Clearly, the RBV dc offset drift design goal of ±5% will be exceeded under worst case conditions. However, the maximum allowable gain variation of ±1 dB has been met.

Since the MSS signal level is relatively low compared to the RBV level, the percentage dc offset is much greater. The MSS dc offset drift is +34.9, -39.2 percent due to temperature and +47.7, -38.4 percent due to aging. Gain variation is ±1.22% due to temperature and ±5.8 percent due to aging. Since the MSS signal is not a square wave, the dc offset results in unsymmetrical triggering of the dual line receiver gates. The maximum allowable dc offser which will not cause excessive data lott has yet to be specified.

4.1.2.2 Conclusions and Recommendations. - As discussed above, the RBV dc offset drift exceeds the design specifications. However, referring to Table 4-2, it can be seen that a major portion of the drift (approximately 75%) may be attributed to the modulator. This is due primarily to the sensitivity of the oscillator resonant circuit capacitors and varicap. Additional modulator temperature and aging drift is possible as a result of the variable inducators (L3, L6), which contribute a frequency sensitivity of -3.6 MHz/nH. The effects of inductor variation have not been included in the results of Table 4-2, because their drift coefficients had not yet been established.*

As a precaution against excessive modulator temperature drift, each network should be temperature cycled, and any marginal components replaced prior to installation into the system.

*A more recent analysis (Appendix I) using statistical methods includes inductor variations.

TABLE 4-2. SUMMARY OF RBV AND MSS INPUT/OUTPUT DRIFT

Network	Network Drift				Drift[1] Referenced to Video Output				Drift[1] Referenced to MSS Receiver Input			
	dc offset (mv)		Gain (%)		dc offset (%)		Gain (%)		dc offset (%)		Gain (%)	
	Temp.	Aging	Temp.	Aging	Temp.	Aging	Temp.	Aging	Temp.	Aging	Temp.	Aging
RBV Input	+ 15 - 13	± 31.6	±0.35	±5.8	+ 1 - 0.86	± 2.1	±0.35	± 5.8	—	—	—	—
MSS Input	+ 23.1 - 16.6	+ 5 - 11	±0.87	±4	—	—	—	—	+ 4.6 - 3.3	+ 1 - 2	±0.87	±4
Modulator[2]	+129 -111	± 71	—	—	+ 8.6 - 7.4	± 4.8	—	—	+26 -22.2	±14.2	—	—
Lim/Demod RBV	± 2.5	± 4	±0.2	±1	± 0.5	± 0.8	±0.2	± 1	—	—	—	—
Lim/Demod MSS	± 21.5 - 68.5	+162.5 -111.5	±0.35	±1.8	—	—	—	—	+ 4.3 -13.7	+32.5 -22.2	±0.35	±1.8
RBV Out	+ 14.7 - 32.2	+141 - 82	±0.7	±3.9	+ 1 - 2.1	+ 9.4 - 5.5	±0.7	± 3.9	—	—	—	—
Totals					+11.1 -10.8	+17.1 -13.2	±1.25	±10.7	+34.9 -39.2	+47.7 -38.4	±1.2	±5.8

Notes:

1. Percent dc drift is based on a nominal of 1.5 volts for RBV and 500 millivolts pp for MSS.
2. Modulator frequency drift has been converted to input voltage deviation using a 3 KHz/mV ratio. The effects of variable inductor (L3, L6) drift have not been included.

The bulk of both the dc offset and gain aging drift is due to the characteristics of potentiometers. Therefore, even though an effort has been made to minimize potentiometer drift effects, critical potentiometers should be further desensitized, or completely eliminated from the circuits where possible, if additional stability is required.

It should be noted that when temperature compensation was incorporated into the circuit design — such as sensistors in the MSS Input and Limiter/Demodulator — for analysis purposes, the resulting temperature drift was assumed to be negligible.

4.1.2.3 MSS/RBV Input Worst Case Analysis. - The MSS/RBV Input Network has been analyzed to ensure reliable operation under ERTS system environmental requirements. MSS and RBV signal Input drifts due to temperature and aging effects were determined along with the overall gain variation, and maximum and minimum MSS signal -sync reclocking delays were computed.

4.1.2.3.1 Design Considerations. - Circuit time delays between the MSS data and sync signals must be within the required limits to ensure reliable reclocking. Since the MSS/RBV signals are dc coupled to the modulator, dc drift due to temperature and aging must be minimized. Also, the RBV channel voltage gain must be stabilized against long term drift. Amplifier bandwidth must be compatible with signal requirements.

Internal voltage regulator stability should be adequate and diode dissipation within allowable limits.

4.1.2.3.2 Summary. - Individual component and amplifier worst case drift factors are tabulated in Table 4-3 for the RBV channel and Table 4-4 for the MSS channel. The magnitude of drift when reflected to the modulator input is also shown in the tables.

Assuming the complementary pair emitter follower transistors are matched, dc drift in the input channels is very low. Actually, in order to compensate for modulator temperature drift, some dc drift has been introduced into both the RBV and MSS channels by unbalancing the output emitter follower pairs. Signal voltage gain variation is primarily due to the aging characteristics of the level control potentiometers.

The MSS TTL output level variation is a major source of drift in the MSS channel. The "high" level drift is -10, +70 mV due to temperature and -55 mV due to aging, and the "low" level variation is +10 mV due to temperature and +20 mV due to aging. However, as shown in Table 4-4, the above drifts are attenuated by approximately 1/6 when reflected to the modulator input.

TABLE 4-3. RBV INPUT COMPONENT DRIFT SUMMARY

Component or Parameter	Component Drift		Drift Reflected to Modulator Input	
	Temperature (25-61° C)	Aging	Temperature (25-61° C)	Aging
R46 (200 ohm potentiometer)	Negligable	±4% of level	—	±4% of level
U8 (μA702A dc)	±1 mV	±2 mV	±0.7 mV	±1.5 mV
U8 (Gain)	±0.35%	±1.8%	±0.35%	±1.8%
R47 (200 ohm potentiometer)	±0.57 mV	±2.6 mV	±0.26 mV	±1.3 mV
-11.7 (IN943B) at U9 Input	±6 mV	—	±6 mV	—
±8.4 at U9	±1 mV	—	±1 mV	—
R47, R12, R15	±0.35%	±1.0%	±5.2 mV max	±27 mV max
U9 Unbalance	±1.7 mV	—	±1.7 mV	—
Total (dc)			+15, -13 mV	±31.6 mV
Total (gain)			±0.35%	±5.8%

In order to minimize zener diode temperature drift, the voltage regulator outputs were assumed to be within 2% of their nominal breakdown voltages. As a result, they are operating near the recommended reverse current required for optimum temperature stability.

4.1.2.3.3 Worst Case Analysis. - The MSS/RBV Input Network has been analyzed to determine overall circuit operating capability and dc stability. Worst case dc drifts due to temperature and aging have been calculated and the drifts were referenced to the modulator input to determine the effect on FM deviation. Component drift limits are summarized in Appendix A and the derating guidelines are given in Appendix H.

The MSS/RBV Input Network consists of two separate channels; the MSS channel and the RBV channel. After a slight amount of high frequency preemphasis, the RBV signal is amplified then fed to an emitter follower stage where the modulator input bias is set for the desired RBV carrier frequency.

a. MSS Input.- The MSS channel reclocks and filters the MSS binary NRZ signal. A potentiometer is used to adjust the modulator input bias for the MSS carrier frequency. A dual output transmitter generates the MSS signal level which when terminated by 50 ohms, is approximately 200 mV pp at the receiver input.

TABLE 4-4. MSS INPUT COMPONENT DRIFT SUMMARY

Component or Parameter	Component Drift		Drift Reflected to Modulator Input	
	Temperature (25-61° C)	Aging	Temperature (25-61° C)	Aging
TTL "High"	-10, +70 mV	-55 mV	-2, +12 mV	-9 mV
TTL "Low"	+10 mV	+20 mV	+2 mV	+3 mV
Q1 and Q2	Assumed to be matched	—	—	—
Q3 and Q4	Assumed to be matched	—	—	—
R49 (200 ohm potentiometer)	Negligable	±1 mV	—	±1 mV
R48 (200 ohm potentiometer)	±0.87%	±4%	±0.87% level	±4% level
±6.2 V (IN825) Drfit at U10	±3.6 mV	±1 mV	±3.6 mV	±1 mV
±8.4 V at U10	±2 mV	—	±2 mV	—
U10 - Unbalance	+3.5 mV	—	+3.5 mV	—
U10 - Sensistor	-5 to -9 mV	—	-5 to -9 mV	—
Total (dc)			+23.1, -16.6 mV 0 with Sensistor	+5, -11 mV
Total (gain)			±0.87%	±4%

1. Line Receiver/Clocking.- The MSS data and sync input signals feed Dual Line Receivers which are capable of detecting a differential input of 25 millivolts (or greater) and converting the level into a TTL-compatible output logic level.

   The delay of MSS Data transitions with respect to negative Bit Sync transitions (Logic 1 to Logic 0) is nominally 14 ms at the receiver inputs. In order to ensure sufficient flip-flop set-up and hold times prior to clocking, a pair of TTL inverters are used to delay the MSS data. The MSS Data reclocking timing relationships, using manufacturers delay limits are shown in Figure 4-15. If the set-up and hold time requirements have been met, information at the input of

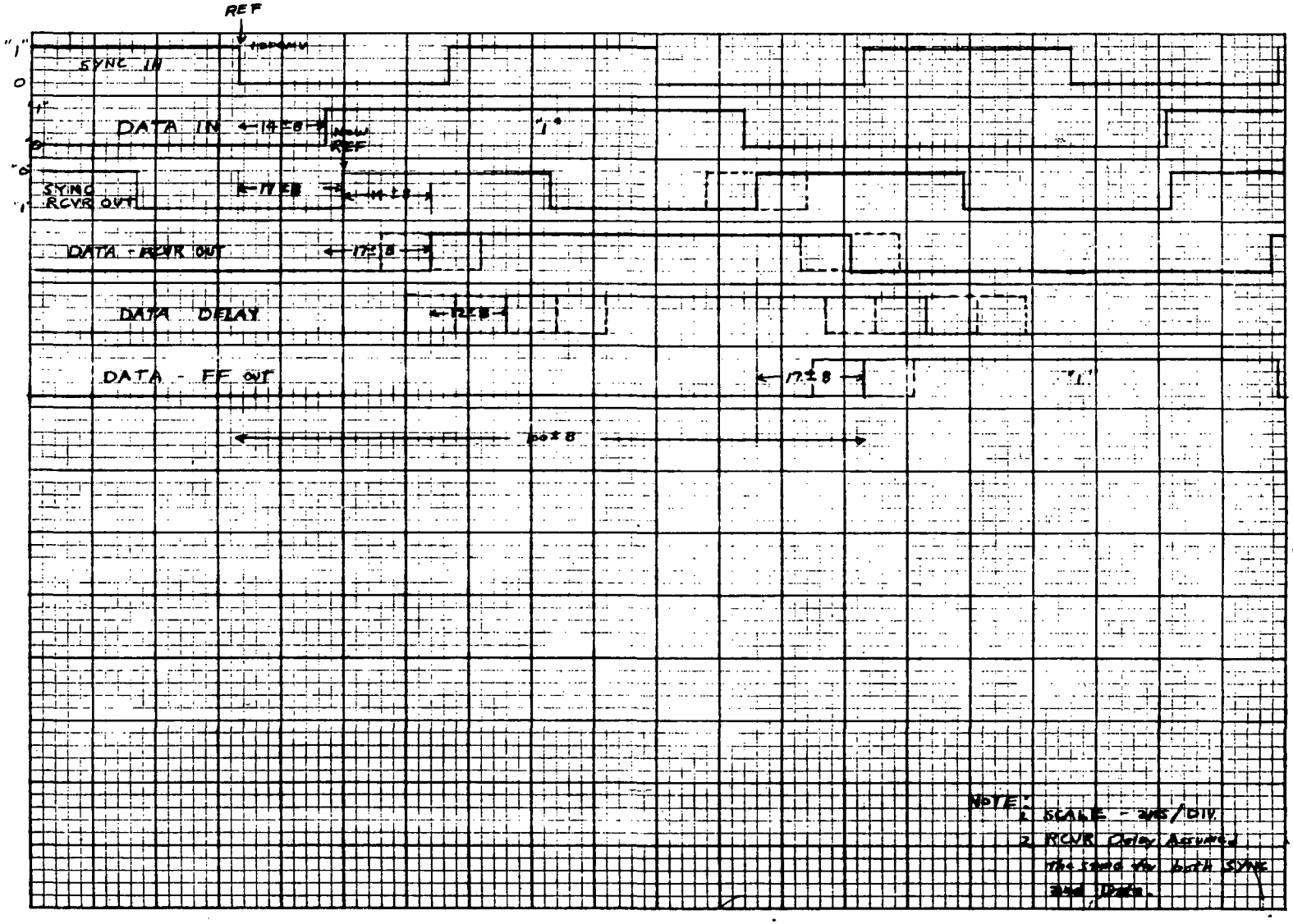


Figure 4-15. MSS Input Reclocking Timing Diagram

flip-flops U3 is transferred to the output on the positive edge of the clock pulse (sync input). From the figure, worst case set-up and hold times are 16 to 64 ns and 3 - 51 ns respectively. The reclocked MSS data (flip-flop output) is delayed a nominal of 100 ±8 ns with respect to the input sync pulse reference.

2. Emitter Followers. - Complementary transistors have been used for the MSS filter emitter follower buffers to minimize offset drift. Since the transistors are opposite in polarity, any drift in parameters will be nullified. In order to ensure equal drift coefficients the transistor collector currents should be approximately equal.

Input Emitter Followers (Q1, Q2). - The input emitter followers are driven by a TTL level (clocking flip-flop U3). Assuming the base of Q1 is at 0 volts, the emitter current is

$$I_{E1} = \frac{V_8 - V_{BE}}{R_{25}} \tag{1}$$

Similarly, assuming the output is at 0 volts, the emitter current for Q2 is,

$$I_{E2} = \frac{V_9}{R_{26}} \tag{2}$$

Using nominal component values, from the above equations,

$$I_{E1} = 4.4 \text{ mA and } I_{E2} = 4.15 \text{ mA}$$

Neglecting the voltage drop across the collector resistors, for the above nominal currents, the transistor power dissipations are $P_{d1} = 30$ mW and $P_{d2} = 21$ mW. These dissipation levels are within the allowable heat radiation capabilities of the transistor case size.

Emitter Followers Q3 and Q4. - These are driven from the low pass filter output level adjustment potentiometer, R48. Assuming the base of Q3 is at 0 volts, the emitter current is

$$I_{E3} = \frac{V_8 - V_{BE}}{R_{31}} \tag{3}$$

For Q4, the emitter current is

$$I_{E4} = \frac{V_9}{R_{35}} \qquad (4)$$

Using nominal values, and R31 = 560 ohms, I_{E3} = 8 mA, and I_{E4} = 8.3 mA.

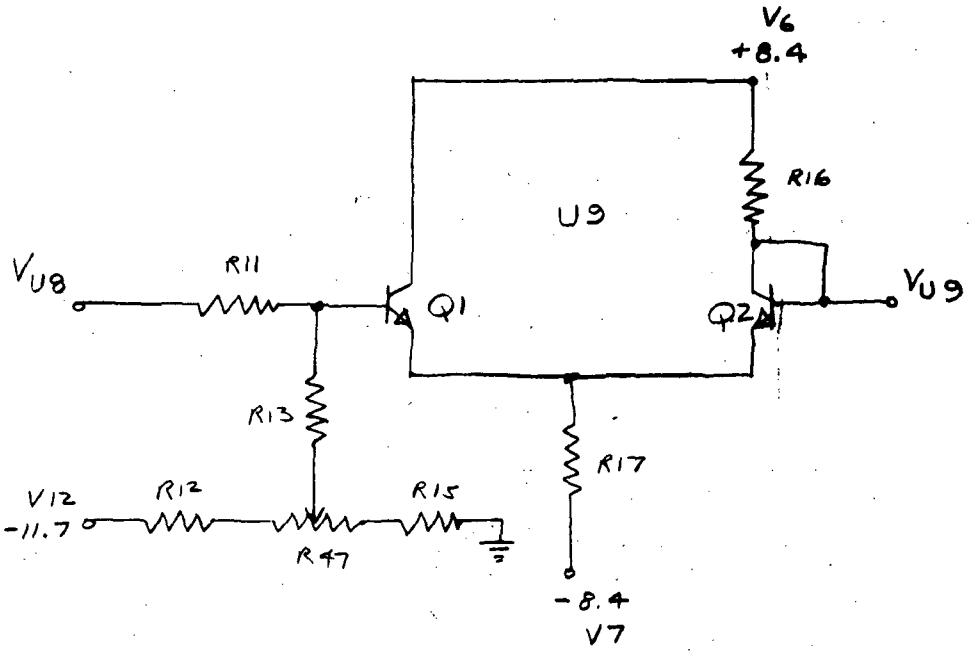
Neglecting the voltage drop across the collector resistors, for the above nominal currents, the transistor power dissipations are P_{d3} = 55 mW and P_{d4} = 41 mW. The above transistor dissipation levels are slightly higher than the maximum heat dissipation possible through radiation, and a path for heat conduction should be provided.

MSS Level Control (R48).- The MSS signal maximum FM deviation is controlled by potentiometer R48. The maximum temperature drift is ±0.87% of the potentiometer voltage level and the aging drift is ±4% of the potentiometer voltage level. Using a maximum MSS level of 0.5V into the modulator, and a sensitivity of 3 kHz/mV, the worst case change in modulator deviation due to potentiometer drift is ±13 kHz due to temperature and ±60 kHz due to aging.

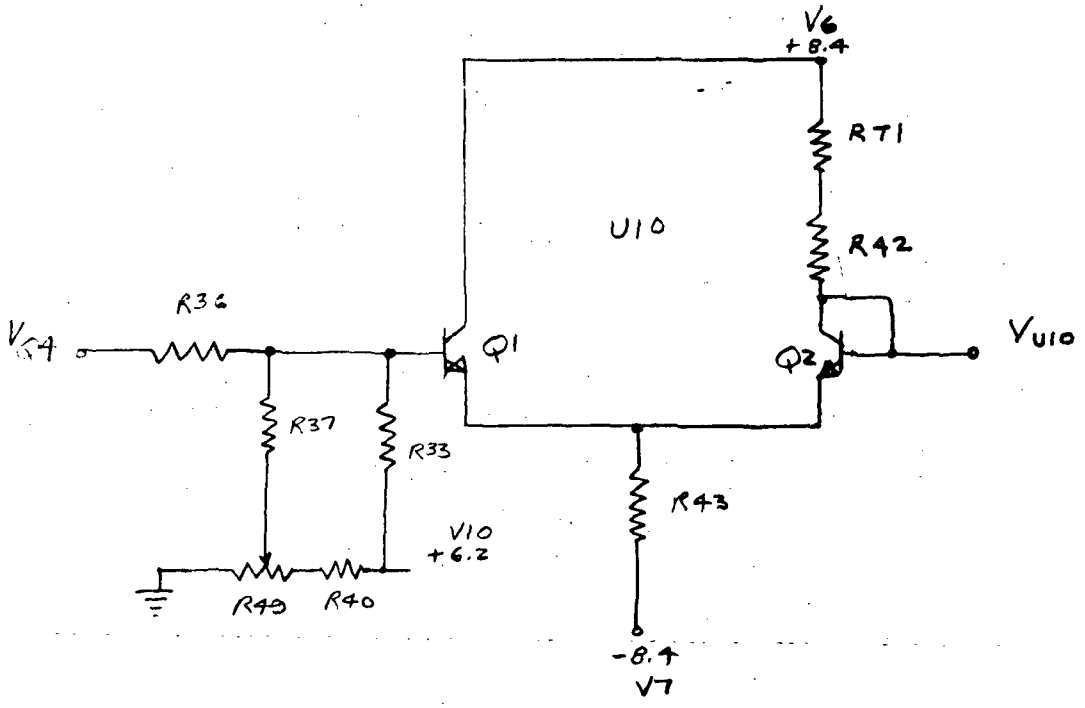
TTL Level Drift.- Although integrated circuit temperature and aging drift coefficients are not generally specified, the output level drift may be projected from what is known about the output circuit and the nature of semiconductor parameters. Since the low level of a TTL gate is an "ON" transistor, V_{CE} temperature and aging characteristics may be used. Thus the TTL low level drift is approximately +10 mV due to temperature and +10% or +20 mV due to aging. Similarly, the high level is an "ON" transistor plus a series diode. If the diode forward voltage drift is -70 mV due to temperature and +35 mV due to aging, the accumulated "high" level drift is -10, +70 mV due to temperature and -55 mV due to aging.

3. Low Pass Filter.- Since the capacitors (mica) and inductors used in the MSS low pass filter are inherently stable, filter characteristics drift due to temperature and aging will be negligible.

4. Output Emitter Follower (U10).- U10 is a matched monolithic pair of NPN transistors. As shown in Figure 4-16, the input stage (Q1) is connected as a conventional emitter follower, and the output stage (Q2) is connected as a series diode to offset the input base-to-emitter voltage drop. If the transistors operate at the same collector current, then, since they are matched $V_{BE1} = V_{BE2}$, the parameter drifts will track each other.



A. RBV



B. MSS

Figure 4-16. RBV and MSS Output Emitter Follower Circuits

Transistor Bias.- The output of U10 is biased to provide the desired MSS carrier frequency. Neglecting the 20 ohm potentiometer (R49), the dc output at U10 is given by

$$V_{U10} = \frac{\frac{R_{36}\,R_{37}}{R_{36}+R_{37}}}{\frac{R_{36}\,R_{37}}{R_{36}+R_{37}} + R_{38}} V_{10} \qquad (5)$$

For nominal component values, $V_{U10} = 1.46$ V, which is equivalent to a modulator output frequency of approximately 12.75 MHz.

The combined current flowing through the two transistors of U10 is

$$I_E = \frac{V_{IN} - V_{BE} + V_7}{R_{43}} \qquad (6)$$

Again using nominal values, $I_E = 22.7$ mA.

Assuming negligible load current, transistor Q2 current is controlled by the output level, or

$$I_{E2} = \frac{V_6 - V_{U10}}{R_{42} + RT_1} \qquad (7)$$

and for nominal values and RT1 = 150 ohms at 25° C, $I_{E2} = 17$ mA. Then, $I_{E1} = I_E = I_{E2} = 5.7$ mA.

Temperature Compensation. - Emitter follower U10 has been unbalanced in order to provide compensation for temperature drift in the MSS input and also in the modulator immediately following U10.

Since, $I_{E2} > I_{E1}$, then $V_{BE2}(T) < V_{BE1}(T)$, resulting in a differential positive output drift with increasing temperature of about 0.1 mV/0C. On the other hand, as temperature increases, the sensistor (RT1) resistance increases, causing I_{E2} to decrease. The effect of V_{BE} temperature coefficient is negligible, and the result is a decrease in V_{BE2} due to a current change of approximately 3-8 mV/mA. The net result is that U10 output dc level decreases approximately 5-9 mV as temperature increases.

Reference Drift. - Potentiometer R49 is used to set the MSS initial carrier frequency. Since the potentiometer resistance (20 ohms) is much smaller than the resistance in series with it (2.21k ohms), reference drift due to any change in potentiometer characteristics will be negligible.

The +6.2V regulator is connected to the input of U10 through a resistor divider, therefore any variation in the +6.2V regulator output will appear at the output of U10, attenuated by approximately 0.2 due to the input impedance. For a maximum voltage variation of ±19 mV (1N825) due to temperature, U10 output drift is ±3.6 mV; U10 aging drift is approximately ±1 mV.

b. RBV Input. - The RBV input is a 75 ohm balanced line. A potentiometer is used to adjust the signal level, which then is pre-emphasized and feeds a differential amplifier, U8. The output of U8 goes to a matched transistor pair emitter follower which contains a potentiometer for fixing the RBV carrier frequency.

1. Level Control. - Since the level control potentiometer is directly across the input signal, level variation depends on the potentiometer drift characteristics. Therefore, temperature drift will be negligible, but drift due to aging is ±4% of the tap voltage.

2. Difference Amplifier (U8). - U8 is a wideband operational amplifier connected in the inverting mode. The differential voltage gain is

$$A_V = \frac{R_{10}}{R_4+R_5} \tag{8}$$

For nominal resistor values, $A_V = 3$, and voltage gain drift as a result of resistor variation is ±0.35% due to temperature and ±1.8% due to aging.

DC offset drift will be caused by the operational amplifier offset voltage and offset current. However, since the input source resistances are balanced, drift due to offset current may be neglected. The offset voltage drift is given by

$$\Delta V_o = \Delta e_{os} A_{V8} \tag{9}$$

where the temperature drift, $\Delta e_{os} = \pm 350$ uV. Then, substituting into equation 9, $\Delta V_o = \pm 1$ mV. Assuming 0.65 mV/10,000 hr drift due to aging, from equation 9 $\Delta V_o = \pm 2$ mV.

3. Output Emitter Follower (U9). - U9 is a matched monolithic pair of NPN transistors. As was pointed out above (emitter follower U10), V_{BE} drift will be a minimum when the two transistor collector currents are equal.

Transistor Bias. - The output of U9 is biased to provide the desired RBV carrier frequency. Neglecting the 200 ohm potentiometer (R47), the dc output at U9 is given by

$$V_{U9} = \frac{\dfrac{R_{15}(R_{11}+R_{13})}{R_{15}+R_{11}+R_{13}}}{R_{12}+\dfrac{R_{15}(R_{11}+R_{13})}{R_{15}+R_{11}+R_{13}}} \left(\frac{V_{12}}{2}\right) \qquad (10)$$

For nominal component values $V_{U9} = -0.7$ V.

The total emitter current (Q1 + Q2) is given by

$$I_E = \frac{V_B - V_{BE} + V_7}{R_{17}} \qquad (11)$$

For nominal values, and $V_B = 1.2$ (RBV in = 0V), $I_E = 16.2$ mA. Assuming negligible load current, transistor Q2 current is limited by R16, or

$$I_{E2} = \frac{V_6 - V_{U9}}{R_{16}} \qquad (12)$$

and for nominal values, $I_{E2} = 9.8$ mA. Thus,

$$I_{E1} = I_E - I_{E2} = 6.4 \text{ mA}.$$

Temperature Compensation. - Emitter follower U9 has been unbalanced in order to provide temperature compensation for both the RBV input drift and modulator drift. Since $I_{E2} > I_{E1}$, then $V_{BE2}(T) < V_{BE1}(T)$, and the differential drift for increasing temperatures will be positive going at a 0.05 mV/° C rate.

Reference Drift. - Potentiometer R47 is used to set the RBV carrier reference frequency. DC drift will be caused by resistor and potentiometer drift and variation in the reference regulator (-11.7V). Voltage drift due to resistance change is approximately ±0.35% due to temperature and ±1.8% due to aging.

For a type 1N943B Zener diode, the temperature drift is ±47 mV. Thus, reflected to the emitter follower output, the drift is ±6 mV. In this case, the effect of Zener diode aging drift is negligible.

c. Voltage Regulators. - The MSS/RBV Input circuit contains eight Zener diode regulators. The regulator output voltages have been designated by their nominal voltages as: V6 = +8.4V, V7 = -8.4V, V8 = +5.1V, V9 = -6.2V, V10 = +6.2V, V11 = +11.7V, V12 = -11.7V and V13 = -5.1V. Since the current limiting resistors and diode parameters are relatively stable, nominal values have been used in the following analysis to conserve power requirements. In addition, optimum temperature stability is achieved when the Zener diodes operate at their recommended currents.

+8.4V Regulator (V6). - The initial 8.4V tolerance is 8.0 to 8.8V and the maximum drift is ±65 mV due to temperature and ±4 mV due to aging. Regulator dissipation is given by

$$P_d = V_6 I_Z \tag{13}$$

where

$$I_Z = I_{in} - I_{Load} \tag{14}$$

and,

$$I_{in} = \frac{V_{in} - V_8}{R2} \tag{15}$$

The V6 load current is

$$I_L = U_9 + U_{10} \tag{16}$$

From equation 15, for R2 = 287 ohms, I_{in} = 47.3 mA, and from the previous analysis, I_L = 38.9 mA. Then, I_Z = 8.4 mA and P_d = 70 mW.

-8.4V Regulator (V7). - The -8.4V Regulator loading is identical to the +8.4V Regulator, therefore, the analysis and drift parameters are the same. For R14 = 287 ohms and I_L = 38.9 mA, P_d = 70 mW.

+5.1V Regulator (V8). - The initial +5.1V tolerance is 4.85 to 5.35V and the maximum drift is ±50 mV due to temperature and ±300 mV due to aging. V8 loading is given by

$$I_L = Q1 + Q2 + Q3 + Q4 \tag{17}$$

From the MSS input analysis, I_L = 24.8 mA. For R45 = 510 ohms, I_L = 33 mA, thus I_Z = 8.2 mA and Zener dissipation is P_d = 42 mW.

-6.2V Regulator (V9). - The initial -6.2V tolerance is 5.89 to 6.51V and the maximum drift is ±100 mV due to temperature and ±370 mV due to aging. V9 loading is given by

$$I_L = U8 + Q1 + Q2 + Q3 + Q4 \quad (18)$$

For a U8 current of 7 mA, and a combined transistor current of 24.8 mA, I_L = 31.8 mA. Then for R18 = 392 ohms, the available input current is 40.4 mA, resulting in I_Z = 8.6 mA, and a Zener power dissipation of P_d = 53 mW.

+6.2V Regulator (V10). - The initial +6.2V tolerance is 6.0 to 6.22V and the maximum drift (1N825) is ±19 mV due to temperature and ±4 mV due to aging. V10 loading is given by

$$I_L = \text{U10 reference} \approx 12 \text{ mA} \quad (19)$$

For R19 = 825 ohms, the available input current is I_{in} = 19.2 mA. Thus, I_2 = 7.2 mA and the Zener power dissipation is P_d = 45 mW.

+11.7V Regulator (V11). - The initial +11.7V tolerance is 11.12 to 12.28V and the maximum drift is ±239 mV due to temperature and ±4 mV due to aging. V11 loading is operational amplifier U8 and is approximately 5 mA. For R28 = 681 ohms, the available input current is I_{in} = 15 mA. Thus, I_2 = 10 mA and the Zener power dissipation is P_d = 117 mA.

-11.7 Regulator (V12). - The initial -11.7V tolerance is 11.12 to 12.28V and the maximum drift is ±47 mV due to temperature and ±4 mV due to aging. V12 is used for the RBV input dc reference, and $I_L \approx$ 3.5 mA. Thus, for R39 = 909 ohms, the available input current is I_{in} = 11.3 mA, I_Z = 7.8 mA, and the Zener power dissipation is P_d = 91 mW.

-5.1 Regulator (V13). - The initial -5.1V tolerance is 4.85 to 5.35V and the maximum drift is ±50 mV due to temperature and ±300 mV due to aging. The regulator load is a line receiver, which draws approximately 5 mA. Thus, for a series resistance of 120 ohms, the available current is I_{in} = 24 mA, I_Z = 19 mA and the Zener power dissipation is P_d = 95 mW.

4.1.2.3.4 Conclusions and Recommendations. - Worst case analysis of the MSS/RBV Input circuit has shown that most of the drift is due to the potentiometer characteristics. The RBV level variation may be reduced by using a lower value potentiometer (R46) in conjunction with a fixed resistor across the input. Similarly, the MSS level control potentiometer (R48) is a major source of aging drift, and should be desenitized with a series fixed resistor.

Since emitter-follower pairs U9 and U10 were unbalanced to provide temperature compensation for both the input circuit and modulator, the two boards should be temperature cycled together, and the collector balancing resistors may have to be selected for each new combination. The MSS input dc stability depends a great deal on how well the emitter follower transistors (Q1-Q4) V_{BE} temperature coefficients are matched. The above analysis is based on the use of closely matched emitter follower transistors. As a result, any differential drift will be reflected at the modulator input.

Sufficient delays have been incorporated into the MSS input to provide reliable reclocking.

Since the above analysis is based on nominal Zener regulator voltages in order to save power and provide optimum temperature stability, the initial value should be measured. In order to support the projected drift calculations, the measured regulator levels should be within ±2% of nominal.

Any future printed board layout change should incorporate a matched complementary transistor pair (single package) for the Q1, Q2 and Q3, Q4 emitter followers. Such a device eliminates the possibility of a poor match of two individual transistors and reduces the effects of temperature gradients between separate units. In addition, it may be possible to consolidate the number of Zener regulators presently being used. Also, in some cases, using a lower source voltage would result in a significant reduction in network power consumption.

The power dissipation of emitter follower transistors Q3 and Q4 is slightly higher than permitted for radiation cooling alone, therefore, conductive urethane beads should be added to provide a path for heat conduction.

4.1.2.4 Modulator Worst Case Analysis. - The Modulator (Oscillator, Mixer and FM Amplifier) network has been analyzed to ensure reliable operation under ERTS System environmental requirements. Modulator carrier drift and amplifier gain variation due to temperature and aging were determined.

4.1.2.4.1 Design Considerations. - Of prime importance in the modulator design is the minimization of dc and component drifts which contribute to a change

in carrier frequency. In addition, since the oscillator amplifier and output emitter followers operate near saturation, worst case V_{CE} drift due to temperature and aging should be very small.

FM amplifier bandwidth should be adequate.

4.1.2.4.2 Summary. - Individual component worst case drift factors are tabulated in Table 4-5 along with each resulting modulator deviation drift. Assuming the complementary emitter follower transistors are closely matched, input dc drift will be due to the level shifting Zener diodes. Each diode may drift ±5 mV due to temperature and ±3 mV due to aging. Oscillator frequency variation is primarily due to the resonant circuit component drifts. Modulator deviation sensitivity as a function of component drifts is -0.88 MHz/pF due to the varicaps, -0.197 MHz/pF due to C2 and C13, and -3.6 MHz/nH due to the inductor.

4.1.2.4.3 Worst Case Analysis. - The Modulator network has been analyzed to determine overall circuit performance and dc bias and frequency stability. Worst case dc level and oscillator frequency drifts due to temperature and aging have been calculated.

a. Input Emitter Followers. - Input emitter followers Q1 and Q2 (Figure 4-7) are complementary transistors. Assuming the base-to-emitter junction parameters are closely matched. Then, although the two oscillators will drift due to temperature and aging, the modulator difference frequency will remain constant because the drift rate will be the same and in the same direction.

1. Transistor Bias. - In order to provide the required oscillator input bias, a Zener diode has been incorporated in series with each emitter follower base. Therefore, for Q2, the base voltage is given by:

$$V_{B2} = V_{in} + V_{R2} \tag{1}$$

similarly for Q1,

$$V_{B1} = V_{in} - V_{R1} \tag{2}$$

The oscillator input voltage for the high frequency oscillator (HF) is

$$V_{E2} = V_{B2} - |V_{BE}| \tag{3}$$

and for the low frequency oscillator (LF)

$$V_{E1} = V_{B1} + |V_{BE}| \tag{4}$$

TABLE 4-5. FM MODULATOR COMPONENT DRIFT SUMMARY

Component or Parameter	Component Drift		Drift Reflected to Modulator Deviation	
	Temperature (25-61° C)	Aging	Temperature (25-61° C)	Aging
VR1, VR2 (1N829)	±5 mV	±3 mV	±30 kHz	±18 kHz
Q1, Q2 (V_{BE})	Neglig. for matched characteristics	Neglig. for matched characteristics	—	—
1N54726 Varicap (-0.88 MHz/pF)	+0.33 pF	—	±290 kHz	—
C2, C13 (-0.195 MHz/pF)	-0.07 pF +0.35 pF	±0.5 pF	-13.6, +68 kHz	±195 kHz
L3, L6 (-3.6 MHz/nH)	Assume ±0.5% ±0.9 MHz	Assume ±0.5% ±0.9 MHz	±1.8 MHz	±1.8 MHz
Total			-333.6, +388 kHz, plus L3, L6	±213 kHz, plus L3, L6
Total Reflected to Mod. Input			-111, +129 mV, plus L3, L6	±71 mV, plus L3, L6

For nominal parameter values, Q1 and Q2 base and emitter voltages for the maximum and minimum input levels are given in Table 4-6.

2. Zener Diode Reverse Bias. - The input reference diodes are temperature compensated Zener diodes with a nominal breakdown voltage of 6.2V. Optimum temperature stability will result for a reverse current of 7.5 mA. Neglecting transistor base current, the diode reverse current is equal to the current through the series resistor. Or for V_{R2},

$$I_{R2} = \frac{V_8 - V_{B2}}{R_2} \tag{5}$$

and for V_{R1},

$$I_{R1} = \frac{V_9 - V_{B1}}{R_1} \tag{6}$$

For the projected MSS/RBV signal range, the corresponding diode reverse currents are shown in Table 4-6. During RBV operation the average Zener current is approximately equal to 7.5 mA, the specified optimum value, with a drift of ±5 mV due to temperature and ±3 mV due to aging. However, for MSS operation, the reverse currents for both V_{R1} and V_{R2} deviate from nominal by about 25%, which will result in a somewhat greater temperature drift than normal, depending upon the resulting polarity of the diode temperature coefficients.

3. Regulator Loading. - Regulator Loading. - Regulators V_{R5} and V_{R6} drive the input emitter followers and reference diodes. The +11.7V (V8) load is,

$$I_8 = I_{E2} + I_{R2} \tag{7}$$

and the -11.7V (V9) load is,

$$I_9 = I_{E1} + I_{R1} \tag{8}$$

Again, for various MSS/RBV input levels, the regulator loads are shown in Table 4-6. As is clear from the above tabulation, the regulator load currents are relatively constant, thereby eliminating voltage regulation effects.

4. Transistor Power Dissipation. - The transistor power dissipation is approximately,

$$P_d = I_E V_{CE} \tag{9}$$

where, for Q1, $V_{CE1} = 11.7 - V_{E1}$ and for Q2, $V_{CE2} = 11.7 - V_{E2}$. Using the results given in Table 4-6, typical $P_{d1} = P_{d2} = 76$ mW.

The input transistors are complementary. If they are assumed to be matched, and if the modulator oscillators are linear, then the effect of transistor drift may be neglected.

b. Oscillators. - The modulator oscillators are single transistor stages which use a voltage-variable capacitance diode (VARICAP) as the frequency control element.

1. Amplifier Bias. - Since the transistor operating point is near the saturation region, sufficient collector-emitter voltage must be available to prevent saturation under worst case conditions.

Using HF oscillator Q3 as the example, the collector-emitter voltage is,

$$V_{CE3} = V_{C3} - V_{E3} \tag{10}$$

where, $V_{E3} \approx V_{BE}$, and,

$$V_{C3} = V_6 - I_{C3} R_7 \tag{11}$$

Since $I_E \approx I_C$, then combining the above equations and solving for V_{CE},

$$V_{CE} = V_6 - \left(\frac{V_7 - V_{BE3}}{R_8 + R_9}\right) R_7 \tag{12}$$

Assuming the regulators (V6 and V7) are initially at approximately their nominal values (11.7V), from equation 12, drift due to temperature and aging results in a minimum $V_{CE3} = 1.7$V, at a collector current of $I_C \approx 3$ mA. Thus, the oscillator will remain in the active region throughout system environmental conditions.

TABLE 4-6. OSCILLATOR INPUT LEVEL VS MSS/RBV INPUT

Mode of Operation	Input Level V	Zener Vol. V	Zener Current		I_{in} mA	V_B		V_E		I_E		Regulator Load (mA)	
			I_{R2}	I_{R1}		V_{B2}	V_{B1}	V_{E2}	V_{E1}	I_{E2}	I_{E1}	-11.7	+11.7
MSS	1.2	6.2	5.75	8.9	3.2	7.4	-5	6.7	-4.3	15.6	10	18.9	21.3
	1.45	6.2	5.4	9.25	3.85	7.65	-4.75	6.95	-4.05	16.2	9.4	18.6	21.6
	1.7	6.2	5.1	9.6	4.5	7.9	-4.5	7.2	-3.8	16.8	8.8	18.4	21.9
RBV	-0.75	6.2	8.4	6.4	-2	5.45	-6.95	4.75	-6.25	10.8	14.5	20.9	19.2
	0	6.2	7.35	7.35	0	6.2	-6.2	5.5	-5.5	12.8	12.8	20.2	20.2
	0.75	6.2	6.4	8.4	2	6.95	-5.45	6.25	-4.75	14.5	10.8	19.2	20.9

2. Resonant Circuit. - The oscillator is a variation of the standard Colpitts oscillator. Again, using the HF oscillator as the example, as shown in Figure 4-17, the oscillator resonant circuit consists of C2 plus the diode capacitance, Cd, in parallel with inductor L3 along with capacitors C3 plus C5. Thus, the tank circuit resonant frequency is given by,

$$\omega^2 = \frac{1}{L\left(\frac{C_2 C_d}{C_2+C_d} + \frac{C_3 C_5}{C_3+C_5}\right)} \tag{13}$$

where C_d, the diode junction capacitance as a function of reverse voltage is,

$$C_d = \frac{k}{(V_R + V_O)\, n} \tag{14}$$

and, using the diode specifications at the projected operating point,

$$C_d = \frac{94}{(0.6 + V_R)\, 0.44}\ \text{pF} \tag{15}$$

Since the C3 and C5 branch is much smaller than the C2 and Cd branch, C3 and C5 may be neglected. Then,

$$\omega = \left[\frac{C_2\ (0.6 + V_R)\ 0.44 + 94\ \text{pF}}{L\ (C_2\ 94\ \text{pF})}\right]^{1/2} \tag{16}$$

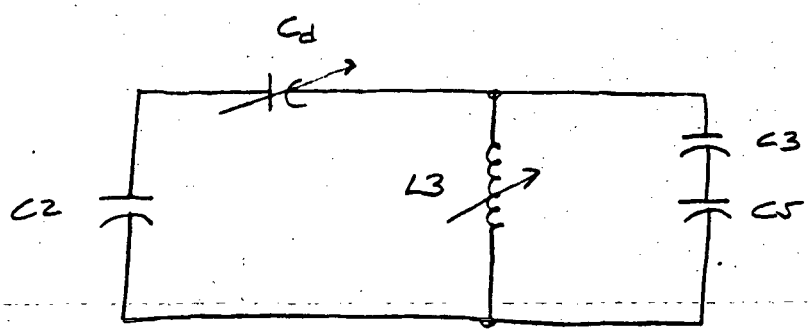


Figure 4-17. Oscillator Resonant Circuit

By taking the derivative of equation 16, the frequency sensitivity with respect to input voltage change is,

$$\frac{df}{dV_R} = \frac{1}{4\pi}\left[\frac{C_2\,(0.6 + V_R)\,0.44 + 94\ pF}{94\ pF\ L\ C_2}\right]^{-1/2} \left[\frac{0.44\,(0.6 + V_R) - 0.56}{94\ pF\ L}\right] \tag{17}$$

Depending on the value of inductance, the oscillator sensitivity varies from 1 to 2 MHz/volt; resulting in a modulator deviation of 2 to 4 MHz/volt.

Capacitor Drift (C2, C13). - Neglecting C3 and C5, which are comparatively small, the oscillator resonant frequency is,

$$f = \frac{1}{2\pi\left(L\,\frac{C_2\,C_d}{C_2 + C_d}\right)^{1/2}} \tag{18}$$

Taking the derivative of equation 18 with respect to C2, the oscillator frequency variation as a function of capacitor C2 is,

$$\frac{df}{dC2} = -\frac{C_d}{4\pi\ C_2\left(L\,\frac{C_2\,C_d}{C_2 + C_d}\right)^{1/2}\ (C_2 + C_d)} \tag{19}$$

And, for nominal values, equation 19 is $df/dC_2 = -0.195$ MHz/pF. Using mica capacitor parameters, the oscillator drift will be ±97 kHz due to aging and +13.6, -68 kHz due to temperature. Worst case modulator drift results when the two oscillators drift in opposite directions. Therefore, worst case modulator drift is ±195 kHz due to aging and -13.6, +68 kHz due to temperature.

Inductance Drift (L3, L6). - Taking the derivative of equation 18 with respect to L, the oscillator frequency sensitivity to inductance variation is,

$$\frac{df}{dL} = -\frac{1}{4\pi\,(C)^{1/2}\,(L)^{3/2}} \tag{20}$$

And, for nominal values, $df/dL = 3.6$ MHz/nH.

Since the inductor drift characteristics have not been established, the frequency deviation can not be determined accurately. However, assuming a maximum drift of ±1%, the oscillator frequency drift is ±1.8 MHz and the modulator deviation is ±3.6 MHz.

Varicap (CR1, CR2). - The voltage-variable capacitance diode junction capacitance as a function of reverse voltage is,

$$C_j = \frac{C_O}{1 + \left(\frac{V_R}{\phi}\right)^n} \tag{21}$$

where,

$C_O = C_j$ at $V_R = 0 = 110$ pF

$\phi = 0.6V$

$n = 0.44$

or, for the above constants,

$$C_j = \frac{94}{(V_R + 0.6)\ 0.44} \text{ pF} \tag{22}$$

Oscillator frequency variation as a function of diode reverse voltage is given by equation 17. The effect of diode capacitance (C_d) drift is given by interchanging C2 and Cd in equation 19, or,

$$\frac{df}{dc_d} = -\frac{1}{4\pi} \frac{C_2}{C_d \left(\frac{LC_2\ C_d}{C_2 + C_d}\right)^{1/2} (C_2 + C_d)} \tag{23}$$

and, for nominal parameter values,

$$\frac{df}{dC_d} = -\frac{0.88 \text{ MHz}}{\text{pF}} \tag{24}$$

Varicap capacitance temperature drift is given as 0.02%/° C to 0.04%/° C. Worst case modulator drift results when the LF oscillator and HF oscillator diodes drift at different rates. Thus, since the maximum differential drift is 0.02% from 25° C to 61° C, C_d = 0.33 pF, and from equation 24, f = ±290 kHz. Even if the diode temperature coefficients are perfectly matched, a slight amount of temperature drift will result due to the effects of reverse voltage unbalance on the junction capacitance temperature coefficients, particularly in the MSS mode (see Table 4-6, when $V_E \approx V_R$).

c. Output Emitter Followers (Q5 and Q6). - The output emitter followers are operated near the saturation level in order to minimize transistor power dissipation.

1. DC Bias. - The analysis of the emitter follower bias is similar to that of the oscillator amplifier (Q3), and minimum V_{CE} is given by

$$V_{CE5} = V_6 - \left(\frac{V_7 - V_{BE5}}{R_{11} + R_{12}}\right) R_{10} \tag{25}$$

Assuming the regulator voltages are initially at their nominal values, from equation (25), worst case V_{CE5} = 0.8V.

2. Power Dissipation. - The output emitter follower power dissipation is given by

$$P_{d5} = I_{E5} V_{CE5} \tag{26}$$

where,

$$I_{E5} = \frac{V_7 - V_{BE5}}{R_{11} + R_{12}} \tag{27}$$

and,

$$V_{CE5} = V_6 - I_{C5} R10 - V_{E5} \tag{28}$$

Using nominal values, I_{E5} = 21 mA, V_{CE} = 2V, and P_d = 42 mW.

d. Zener Regulators. - Two sets of ±11.7V voltage regulators are used in the modulator. VR5 and VR6 are temperature compensated, and are used on the input emitter followers and bias diodes. VR3 and VR4 supply the oscillators and output emitter followers.

1. +11.7V (V8, VR6). - The initial V8 tolerance is 11.12 to 12.28V and the maximum drift is ±24 mV due to temperature and ±3 mV due to aging. Regulator current is

$$I_Z = I_{in} - I_{load} \tag{29}$$

where,

$$I_{in} = \frac{V_{in} - V_C}{R_{22}} \tag{30}$$

and, the load current is

$$I_L = VR2 + Q2 \tag{31}$$

Using the results of Table 4-6, I_L = 20 mA. From equation (30), minimum available I_{in} = 23.5 mA, and nominal I_{in} = 31 mA. Thus, typical regulator power dissipation is 128 mW.

2. -11.7V (V9, VR5). - Since the VR5 and VR6 circuits and loading are the same, the analyses are identical.

3. +11.7V (V6, VR4). - The initial V6 (IN941B) tolerance is 11.12 to 12.28V and the maximum drift is ±239 mV due to temperature and ±4 mV due to aging. V6 load current is

$$I_L = Q3 + Q4 + Q5 + Q6 \tag{32}$$

Using previous results, required I_L = 48 mA and, for worst case parameters, minimum available I_L = 48 mA. Nominal I_{in} = 55 mA, then I_2 = 7 mA, and regulator power dissipation is P_d = 82 mW.

4. -11.7V (V7, VR3). - The VR3 and VR4 regulator circuits and loading are the same, thus the analyses are identical.

e. Mixer/Filter. - The mixer (Z1) and FM filters are shown in Figure 4-8.

1. Mixer. - The mixer is a hermetically sealed module, which consists of a transformer coupled diode bridge. Mixer drift characteristics have not been specified, and are not very critical in this application.

To improve isolation and reduce intermodulation products, the low frequency (LF) input has been attenuated with respect to the high frequency (HF) input by adding a series resistor. Minimum conversion loss results for a +10 dBm local oscillator level, which is slightly higher than is available from the modulator. This lower signal level, however, does not appear to affect system performance.

2. FM Filter. - The mixer output feeds a bandpass-notch filter, which has an upper cut-off frequency of approximately 25 MHz, and is designed to reject the unwanted mixer sidebands. Since the components used are relatively stable, drift of the filter characteristics will be insignificant.

f. FM Amplifier. - The FM amplifier consists of a video amplifier followed by a line driver.

1. Video Amplifier. - The video amplifier is an integrated circuit (uA733) differential amplifier, which has an adjustable voltage gain fixed by external wiring. With R33 = 470 ohms, the voltage gain is approximately 30 dB. Since the input signal is FM and the output is ac coupled, normal gain variation and dc drift are not critical.

2. Line Driver. - The line driver is a wide band, integrated circuit (NH0002) current amplifier. Again, since the input signal is FM and the output is ac coupled, normal gain variation and dc drift are not critical.

3. Voltage Regulators. - The dc supply voltage for U1 and U2 is provided by two 6.2V Zener regulators, VR7 and VR8. Using manufacturer's specifications, typical load current is 24 mA and the maximum is 34 mA. For a series resistance of 51 ohms, minimum available current is 24 mA at 6.2V. Typical input current is I_{1n} = 35 mA, then for nominal load I_2 = 11 mA, and regulator dissipation is P_d = 68 mW.

4.1.2.4.4 Conclusions and Recommendations. - Worst-case analysis of the Modulator circuit has shown that the greatest source of drift is due to the oscillator resonant circuit components. The major source of potential drift is the variable inductor, which contributes a frequency sensitivity of -3.6 MHz/nH. Therefore, since inductor drift coefficients are not specified, the drift characteristics should be established through laboratory tests.

The analysis assumes that the drift parameters of complementary transistors Q1 and Q2 will be closely matched. In addition, the capacitance tracking characteristics of the Varicap diodes are assumed to be similar.

Any future printed board layout change should incorporate a matched complementary transistor pair (single package) for input emitter followers Q1 and Q2. Such a device eliminates the possibility of a poor match of two individual transistors and reduces the effects of temperature gradients between separate units. In addition, since two sets of ±11.7V regulators are used in the modulator, it may be possible to consolidate the two without significantly affecting overall circuit performance.

4.1.2.5 Record Current Adjust Worst Case Analysis. - The Record Current Adjust Circuit has been analyzed to ensure reliable operation under the ERTS system environmental requirements. Performance limitations of all critical functions due to component and semiconductor parameter manufacturing tolerances and aging effects were determined.

4.1.2.5.1 Design Considerations. - Attenuator temperature and aging stability should be acceptable and the design must ensure against the possibility of the additional RBV attenuation during MSS operation. To avoid delays in record current adjustment during equipment check-out, it is desirable to minimize circuit time constants, thereby permitting rapid remote pulsing. Coincidentally, the minimum allowable pulse width and the maximum rate should be determined. Also, the limitations to the FM signal linearity should be analyzed.

4.1.2.5.2 Summary - Worst case overall attenuation drift due to temperature and aging from full attenuation (7 dB) is $\pm$ 1/2 dB. The maximum possible undistorted FM amplitude is 7Vpp, which exceeds the normal operating signal level of 3 Vpp. Cut-off stability of the RBV control stage is adequate and the minimum available drive current is sufficient to ensure transistor turn-on. The minimum allowable remote trigger pulse width is 5 ms at a maximum rate of about one pulse every 2 seconds.

4.1.2.5.3 Worst Case Analysis - The following analysis is based on the component specifications shown in Appendix A. An ambient temperature range of 0°C to 60°C over a 10,000 hour life was used for component and parameter derating.

a. FM Output Buffer (Q_1). - For the circuit configuration shown in Figure 4-10, the collector to emitter voltage and collector current of Q1 are dependent on the transistor h_{FE} and thus are subject to both the initial tolerance and subsequent drift due to temperature and aging. From the equivalent circuit shown in Figure 4-18, minimum V_{CE} is,

$$V_{CE1} = V_1 - I_{C1}\overline{R_{13}} - V_{E1} \qquad (1)$$

To evaluate V_{CE1} as a function of h_{FE1}, assume

$$I_E = h_{FE}I_B \qquad (2)$$

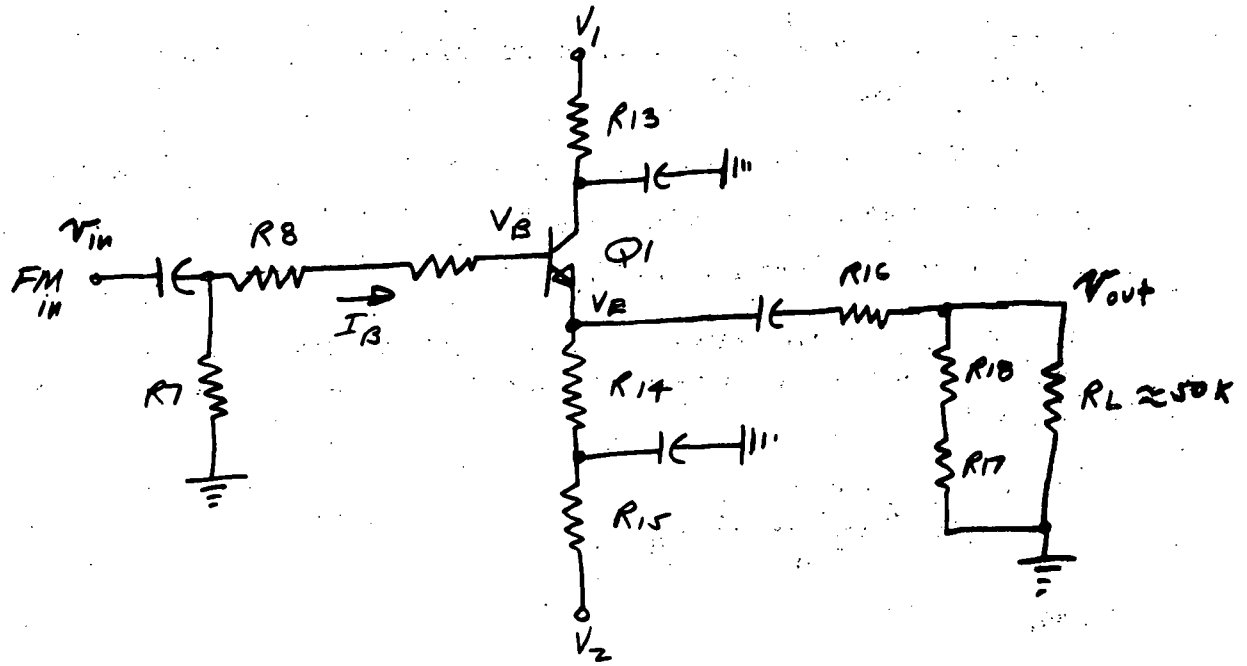


Figure 4-18. FM Output Buffer

And since,

$$I_{B1} = \frac{-V_{B1}}{R_7 + R_8 + R_{12}} \tag{3}$$

Also, assuming operation in the active region,

$$I_{E1} = \frac{V_{E1} - V_2}{R_{14} + R_{15}} \tag{4}$$

And since,

$$V_B = V_E + V_{BE} \tag{5}$$

Then, by solving the above equations for V_{E1} and since minimum V_{CE1} results for minimum V_{E1},

$$V_{E1} = \frac{\dfrac{V_2}{h_{FE}(R_{14}+R_{15})} - \dfrac{V_{BE2}}{R_7+R_8+R_{12}}}{\dfrac{1}{h_{FE}(R_{14}+R_{15})} + \dfrac{1}{R_7+R_8+R_{12}}} \tag{6}$$

At 60°C, where h_{FE} is maximum, substituting worst case values into equation 6, $V_{E1} = -0.96V$.

For the above condition, $I_{E1} = 9.5$ mA and since $I_{C1} = I_{E1}$ for $h_{FE} \gg 0$, substituting into equation 1, minimum $V_{CE1} = 7.25$ V, which is sufficient for linear operation with the normal 2 - 3 Vpp FM signal.

Since Q1 is a common collector stage, the voltage gain is less than one. Further attenuation results from input and output loading. From Figure 4-18,

$$V_{in} = \frac{Z_{in} + R_8 + R_{12}}{Z_{in}} V_B \tag{7}$$

and,

$$V_{out} = \frac{R_{17} + R_{18}}{R_{16} + R_{17} + R_{18}} V_E \tag{8}$$

For $R_L \gg 0$ $V_E = V_B$, then combining the above equations, overall circuit gain is,

$$A_v = \frac{V_{out}}{v_{in}} = \frac{\frac{R_{17} + R_{18}}{R_{16} + R_{17} + R_{18}}}{\frac{Z_{in} + R_8 + R_{12}}{Z_{in}}} \tag{9}$$

and for worst case values, $A_v = 0.925$; or, loading efforts may be neglected.

b. RBV Control (Q2). - The RBV Control Circuit, shown in Figure 4-19, is a saturating switch which is ON in the RBV mode, providing additional FM signal attenuation, and OFF during MSS operation, with negligible attenuation.

To ensure reliable turn-on, maximum required current gain must be less than the minimum available h_{FE}

or,

$$A_I \leq h_{FE} \tag{10}$$

where,

$$\overline{A_I} = \frac{\overline{I_c}}{\overline{I_B}} \tag{11}$$

From the figure, minimum available base current is

$$\overline{I_B} = \frac{V_{RBV}}{R_{21}} \tag{12}$$

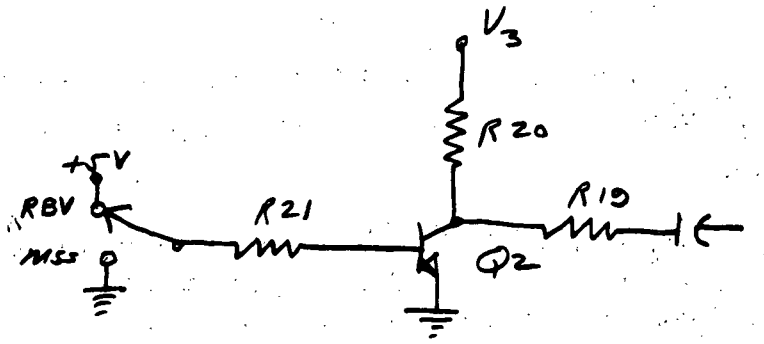


Figure 4-19. RBV Attenuation Control

and maximum collector current is

$$I_c = \frac{V_3 - V_{CE3}}{R_{20}} \tag{13}$$

Substituting worst case values into equations 12 and 13, at 0°C, I_c = 7.2mA and I_B = 0.63mA. Then, from equation 11, maximum required current gain is $\overline{A_I}$ = 11.4, and since h_{FE2} = 54 at 0°C, the requirement of equation 10 is fulfilled.

Q2 is OFF when the RBV control is in the MSS mode, and base current flow is due to I_{CB0}. Thus, the maximum base voltage is given by

$$\overline{V_{BE}} = \overline{I_{CB0}}\ \overline{R_{21}} \tag{14}$$

At 60°C, I_{CBO} = 0.2 uA, and substituting worst case values into equation 14, $\overline{V_{BE}}$ = 1.6 mV, which is sufficient to reliably maintain transistor cut-off.

c. FM Signal Attenuation. - The FM input signal level may be changed by grounding capacitors C1, C2 and C3 through relay contacts which are individually controlled by latching relays K2, K3 and K4.

1. Remote Adjust. - Since the relays are connected to operate as a 3 stage binary counter, the attenuation may be varied in eight 1 dB steps, from 0 to 7 dB.

Attenuation Tolerances. - Signal attenuation is given by:

for C1 grounded

$$V_{B0} = \frac{R_9}{R_8 + R_9} v_{in} \tag{15}$$

for C2 grounded

$$V_{B1} = \frac{R_{10}}{R_8 + R_{10}} v_{in} \tag{16}$$

for C3 grounded

$$V_{B2} = \frac{R_{11}}{R_8 + R_{11}} \, v \text{ in} \tag{17}$$

Using nominal values, from equations 15, 16, and 17, V_{B0} = -1 dB, V_{B1} = -2 dB and V_{B2} = -4 dB. Limits due to initial component tolerances are V_{B0} = -1 dB ± 2%, V_{B1} = -2 dB ± 4.5%, and V_{B2} = -4 dB ± 6%. Attenuation drift due to temperature and aging is V_{B0} = -1 dB ± 1%, V_{B1} = -2 dB ± 2.5%, and V_{B2} = -4 dB ± 4.5%.

Worst case overall drift with full attenuation is ± 1/2 dB.

Relay Activation Times. - The worst case relay delay time occurs when all four remote current adjust relays (K1 - K4) must be energized. This condition results when switching from 3 dB to 4 dB and 7 dB to 0 dB attenuation. The maximum overall accumulated relay activation time is given by

$$\overline{T}_K = \overline{T}_{K1} + 3\,\overline{T}_{K2} \tag{18}$$

Substituting worst case tolerances into equation 18, $\overline{T}_K$ = 6.5 ms.

Triggering Pulse Rate. - The remote current adjust pulse rate is limited by the discharge times of the relay triggering coupling capacitors. Maximum delay occurs immediately following the second trigger pulse (activation of K3B), which charges C13 to approximately -22V at the input to coil K4B. With contacts K3-7 and K4-6 open, the C13 discharge path is as shown in Figure 4-20. Thus, the maximum time constant is given by,

$$\overline{T}_{K4B} = \overline{R}_{32}\,\overline{C}_{13} \ln \frac{Eo}{Ef} \tag{19}$$

Since the minimum allowable relay activation voltage is 13.5V, assuming a trigger pulse of +22V, the maximum permissible negative charge is Ef = 22 -13.5 = 8.5V. Now substituting worst case values into equation 19, maximum discharge time is T_{K43} = 1.7 seconds; or, the maximum allowable pulse rate is 1 pulse/1.7 seconds.

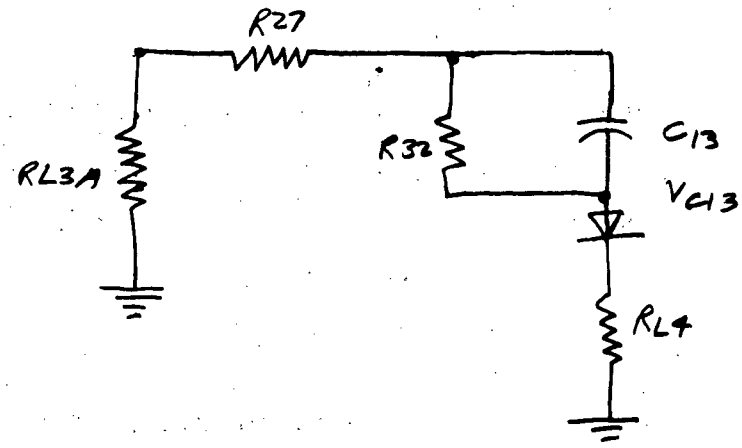


Figure 4-20. Relay K4B Capacitor Discharge Circuit

Current Adjust Pulse Width. - The current adjust pulse width may be written as,

$$T_{pw} = T_{K1} + T_{KL} \tag{20}$$

where,

T_{K1} = Remote current adjust relay activation time

and,

T_{KL} = Latching relay activation time (K2-K4).

Since the minimum latching relay pulse width is dependent on the coupling capacitor discharge time, the minimum decay is

$$T_{\underline{KL}} = R_{\underline{KL}}\, \underline{C}\, \ln \frac{Eo}{Ef} \tag{21}$$

where, R_{KL} = the relay coil resistance. Thus, for Eo = 20.8V, and minimum allowable relay activation voltage Ef = 13.5V, substituting worst case values into equation 21, at 0°C, $T_{\underline{KL}} = 2.8$ ms. And, since $\overline{T_{K1}} = 2$ ms, from equation 20, the minimum allowable current adjust pulse width is $T_{pw} = 4.8$ ms.

2. RBV Control Attenuation. - In the RBV mode transistor Q2 is in saturation, shunting the FM output signal to ground through a low impedance. Assuming the output impedance of Q1 is low (Q1 is a common collector stage), the ON equivalent circuit for Q2 is as shown in Figure 4-21. The FM signal level during MSS operation, S1 open, is

$$V_{MSS} = \frac{R_{17} + R_{18}}{R_{16} + R_{17} + R_{18}} V_{in} \qquad (22)$$

Similarly, in the RBV mode, S1 closed,

$$V_{RBV} = \frac{\frac{R_{19}(R_{17} + R_{18})}{R_{17} + R_{18} + R_{19}}}{\frac{R_{19}(R_{17} + R_{18})}{R_{17} + R_{18} + R_{19}} + R_{16}} V_{in}$$

Using nomimal values for comparative purposes, from equation 22, $V_{MSS} = 0.925\ V_{in}$ and, from equation 23, $V_{RBV} = 0.57\ V_{in}$. Thus, the added FM attenuation during RBV operation is $0.36\ V_{in}$, or

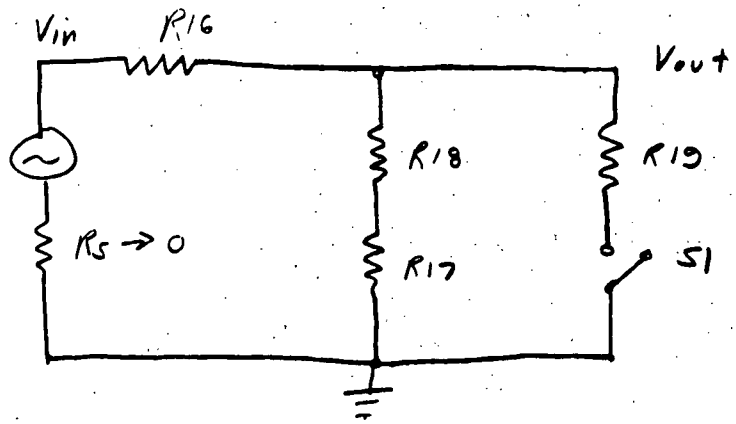


Figure 4-21. RBV Record Current Attenuation

approximately -8 dB. Since equations 22 and 23 involve identical parameters, and R19 is a stable resistor, output level drift due to temperature and aging is negligible between the MSS and RBV modes.

4.1.2.5.4 Conclusions and Recommendations. - The Record Adjust Circuit worst case analysis has shown that all operating requirements of the original design have been satisfied over the temperature range of 0°C - 60°C for a life of 10,000 hours. However, a possible drawback in the current adjust circuit is the relatively long pulsing period required. Due to the large capacitor values utilized to ensure reliable relay triggering, the resulting time constants limit the remote current adjust serial pulse rate to a maximum of 1 pulse per 1.7 seconds. In general, since changes in record current should be infrequent, and adjustment of the original setting may never be required, the specified pulse rate is not objectionable. On the other hand, if a record current adjust test is incorporated into the regular check-out procedure, timing the pulsing period may be an inconvenience. In this event, to avoid incorporation of a more sophisticated design in the airborne equipment and possibly decreasing the overall system reliability, a 3 stage shift register may be added to the ground equipment to automatically time the record current control pulses. Thus, the desired attenuation would be selected with 3 binary switches and the telemetry return compared to each switch position.

4.1.2.6 FM Equalizer Worst Case Analysis. - The FM Equalizer circuit has been analyzed to ensure reliable operation under the ERTS system environmental requirements. Performance limitations due to component and semiconductor parameter manufacturing tolerances and aging effects were determined.

4.1.2.6.1 Design Considerations. - In order to provide reliable playback signal equalization over the required temperature range and operating lifetime, a number of important design factors must be considered:

(1) to maintain sufficient isolation between head signals, the gating level OFF period of the gate controlled two-channel input amplifiers (U1 through U8) must approach 0 volts under worst case loading conditions;

(2) amplifier bandwidth should meet network frequency requirements; and

(3) delay line and linear roll-off filter components should be selected to minimize drift due to temperature and aging, thereby ensuring overall phase and frequency stability.

4.1.2.6.2 Summary. - The gate controlled, two-channel-input amplifiers were found to be very sensitive to the control signal low (0 volt) level. For

example, below 0 dB the single-ended voltage gain varies approximately 1 dB/10 mV. As a result, each gate control signal series resistance (located on the reference generator network) must be adjusted according to the maximum current load requirements. For the D and C gate outputs, which drive 4 loads, the maximum permissible series resistance is approximately 30 ohms. Both the MC 1545 amplifier and the 2N2369A transistor exhibit sufficient bandwidth under worst case conditions. Since the delay lines and low pass filters utilize highly stable mica capacitors and coils which are wound on fiber rods, there is negligible degradation in the equalizer frequency and phase characteristics.

Individual component specifications used in the analysis are shown in Appendix A.

4.1.2.6.3 Worst Case Analysis. -

a. Gate Controlled Amplifier (MC 1545). -

1. Gate Voltage Level Variation. - In Figure 4-22, the gate control level, V_G, depends on the voltage drop across R_1. Or,

$$V_G = V_O + I_{R1} R_1 \tag{1}$$

where V_O = TTL Output Level

and, $$I_{R1} = 3I_G + I_{RC} \tag{2}$$

Where 1_{RC} is the record channel gate current, which for $V_G \longrightarrow 0$, is given by:

$$I_{RC} = \frac{V_{CC} - V_{D1}}{R_2} \tag{3}$$

Assuming $V_{D1} = 0.7V$, $V_{CC} = 20V$, nominal I_{RC} is:

$$I_{RC} = \frac{20-0.7}{4.3K} = 4.5 \text{ mA}$$

From the manufacturer's specifications, for $V_G = 0$, at 25°C, $\overline{I_G} = 2.5$ Vma. The typical gate current requirements may be

calculated from the equivalent circuit shown in Figure 4-22, which was derived from the MC 1545 circuit schematic. Assuming $V_G \rightarrow 0$ and $V_{D2} = 0.7V$, then $V_1 = 0.7V$. And,

$$I_1 = \frac{5-0.7}{2.5K} = 1.71 \text{ mA}$$

Assuming that the transistor base current is negligible,

$$I_2 = \frac{5.7}{11.6K} = 0.49\text{mA}$$

Since,

$$I_G = I_1 - I_2 \tag{4}$$

Then, for nominal values,

$$I_G = 1.71 - 0.49 = 1.22 \text{ mA}$$

Using the above nominal values, and assuming the playback mode is the worst case ($I_{RC} = 0$) equation 2 becomes,

$$I_{R1} = 3\ (1.22) + 0 = 3.66 \text{ mA}$$

Then, from equation 1, the gate signal series resistance for a given V_G and TTL output level is:

$$R_1 = \frac{V_G - V_o}{I_{R1}} \tag{5}$$

For a nominal value of $V_o = 0.22V$, $I_{R1} = 3.66$ mA, and assuming $A_V = 25$ dB (single-ended voltage gain), from the MC 1545 gate characteristic, $V_G = 0.5V$. Then, from equation 5, allowable R_1 is:

$$R_1 = \frac{0.5 - 0.22}{3.66 \text{ mA}} = 76 \text{ ohm}$$

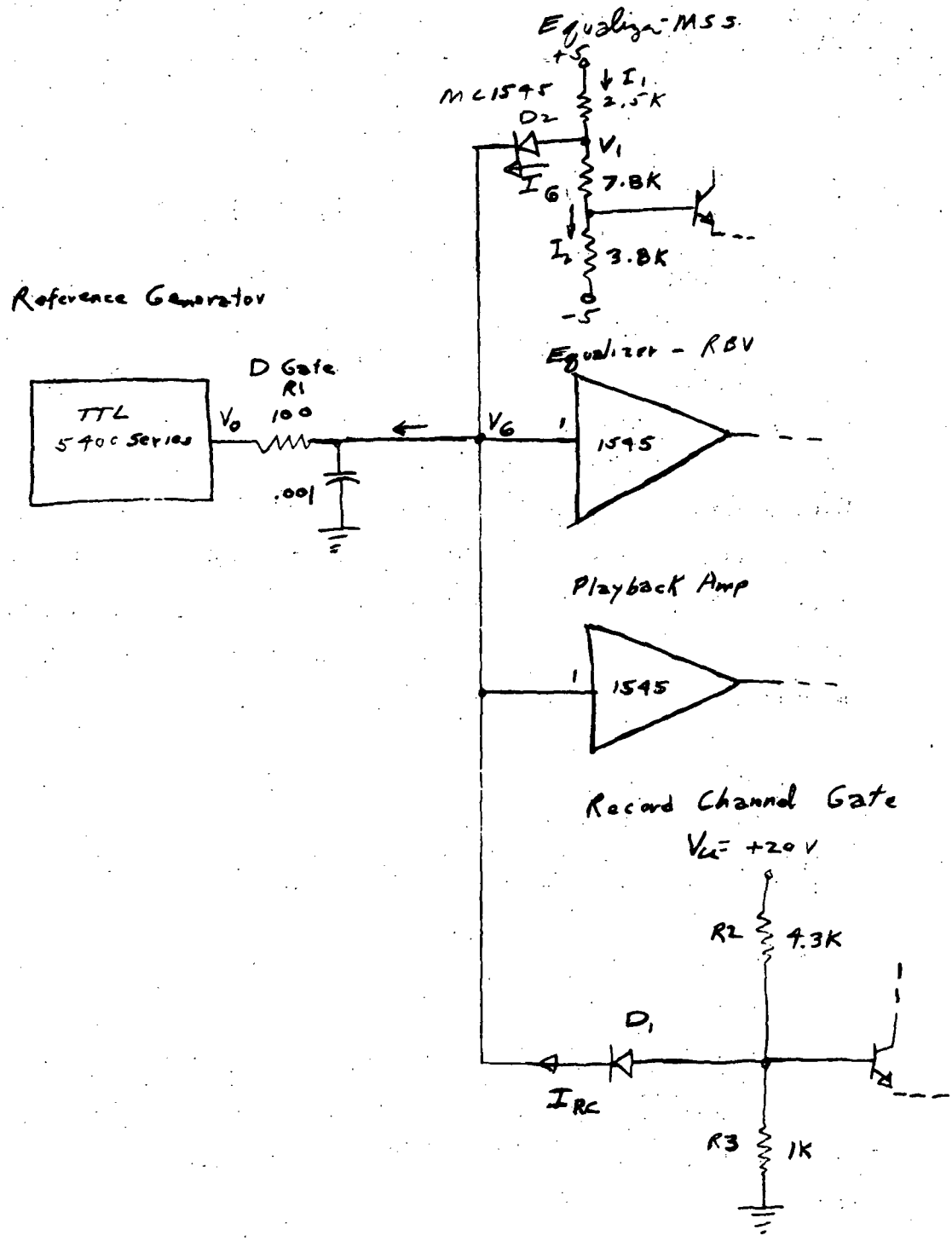


Figure 4-22. C/D Gate Loading

Under worst case conditions, however, from equation 1, maximum gate voltage is:

$$\overline{V}_G = \overline{V}_o + \overline{I}_{R1}\,\overline{R}_1 \tag{6}$$

where,

$$\overline{I}_{R1} = \overline{3I}_G + \overline{I}_{RC} \tag{7}$$

and,

$$\overline{I}_{RC} = \frac{V_{cc} - V_{D1}}{\underline{R_2}} \tag{8}$$

Using worst case component values, at 25°C, $\overline{I}_{RC}$ = 5.2 mA. Thus, with maximum I_G given as 2.5 mA, fom equation 7 for the playback mode, I_{R1} = 7.5 mA. For TTL logic, $\overline{V}_o$ = 0.27V at I_L = 7.5 mA. Again, assuming V_G = 0.5V, and substituting the above values into equation 5, worst case allowable R1 is:

$$\overline{R}_1 = \frac{0.5 - 0.27}{7.5\text{ mA}} = 30.6\text{ ohm}$$

Pilot Tone Extractor/Fill-in Gates (U1, U5). - The E and F gate signals each drive two loads, 1 MC 1545 and 1 TTL gate. And, for worst case conditions,

$$I_{R1} = I_G + I_{TTL} \tag{9}$$

From the manufacturer's specifications, $\overline{I}_G$ = 2.5 mA, I_{TTL} = 1.6 mA, and $\overline{V}_o$ = 0.27V. Now from equation 9, I_{R1} = 4.1 mA; assuming A_V = -25 dB and $\overline{V}_G$ = 0.5V, then from equation 5, maximum allowable R_1 is:

$$R_1 = \frac{0.5 - 0.27}{4.1\text{ mA}} = 56\text{ ohm}$$

MSS Command (U4, U8). - The MSS command signal is controlled by a relay, one side of which is connected to ground; therefore, gate voltage variation due to loading is negligible.

2. Gain Stability. - The nominal single-ended voltage gain is 18 dB and is virtually independent of temperature variation over the 0°C to 60°C range.

   From the MC 1545 specifications; the single-ended voltage gain variation, A_V, is 0.69 dB/volt. The +5 and -5 volt supplies are derived from the +5.6 and -8 volt sources, respectively. Overall allowable drift due to regulator and temperature for these supplies is +5.6 ±0.4V and -8 ± 0.6V. Using the specified gain variation, in terms of percentage change, ΔA_V = 0.69 dB/18 dB = 3.8%/V.

   Thus, the gain variation due to supply drift is:

   +5.6V, ΔA_V = 3.8% (0.4) = ±1.6%, or ±0.29 dB

   -8V, ΔA_V = 3.8% (0.6) = ±2.3%, or ±0.42 dB

3. Output Signal Drift Due to Potentiometer Drift. - Since the MC 1545 operates as a difference amplifier, the output with respect to the two input signals is given by:

$$E_o = A_V (E_1 - E_2) \tag{10}$$

   where,

   E_o = output signal

   E_1 = delayed input signal

   E_2 = potentiometer controlled signal

For the RT22C type potentiometer, the overall drift due to aging and temperature is ±4.2% of the center tap voltage. Thus, the worst case condition is when the center tap is full ON, or the amplitude of $E_2 = E_1$ at a 180° phase shift. The result is an output variation of:

$$E_o = A_V \left[2E_1 \pm 4.2\% E_1\right] \quad (11)$$

b. Delay Line (Technitrol LD101D330A). - No aging specifications are given for the Technitrol delay line. However, since mica capacitors are used in the network, variation of delay due to aging is projected at less than ±0.5%. The delay temperature coefficient is ±0.015%/°C, or a maximum of ±0.124 ns at 0°C and ±0.173 ns at 60°C. The effect on playback equalization due to delay variation is negligible compared to the variation in playback signal resulting from normal head and tape wear and changes in the head-to-tape interface.

c. Linear Roll-Off Filter - A two stage Linear Roll-Off Filter (LRO) with emitter follower isolation is used in each of the RBV and MSS channels. For the 1/3 head input, the LRO filters consist of tapped coils, DL2 and DL3 for the RBV mode and DL5 and DL6 for the MSS mode, along with their associated capacitors. The 2/4 head input network is identical to the 1/3 input.

The coils used in the LRO filter are wound on fiber rods; thus, coil inductance degradation due to temperature and aging is not measurable. Mica capacitors with a combined temperature and aging deviation of +0.4% and -0.15% are used. As a result, since L, C and mutual inductance M, are relatively unaffected by temperature and aging, drift of the LRO filter cut-off frequency and phase shift can be neglected.

d. Amplifier Bandwidth. - The FM Equalizer contains two types of amplifiers, gate controlled two-channel-input wideband integrated circuit amplifiers and single transistor emitter followers. The minimum derated bandwidth of the gate controlled amplifier (MC 1545) is 37.5 MHz and the minimum derated transistor (2N2369A) Gain Bandwidth Product (ft) is 450 MHz. Since the highest cutoff frequency of the LRO filters is 29 MHz, the Equalizer contains sufficient bandwidth.

e. Power Dissipation.

1. Gate Controlled Amplifier. - Since the maximum power supply and gate voltage levels are less than the specified maximums, and the typical load

is much less than the maximum allowable of 25 mA, amplifier power dissipation of the Gate Controlled Amplifier (MC 1545) is well within allowable limits.

2. Emitter Followers. - The quiescent transistor power dissipation of the emitter fillowers is given by:

$$P = V_{CE} I_C \tag{12}$$

Using Q3 of Figure 4-11 as a typical example, the collector current is:

$$I_C = \frac{^8V - V_E}{R_{25} + R_{26}} \tag{13}$$

Or, using nominal values, $I_C = 5.7$ mA,

and

$$V_{CE} = V_{CC} - I_C R24 \tag{14}$$

Using the above value of I_C,

$$V_{CE} = 5.6 - 0.27 = 5.33V$$

As a result, the nominal power dissipation is:

$$P = 5.33\ (5.7) = 30\ mW$$

which conforms with the specified maximum allowable junction temperature.

4.1.2.6.4 Conclusions and Recommendations. - Worst case analysis of the FM Equalizer has shown that the components utilized in the network have the required bandwidth and exhibit sufficient frequency and phase stability. Although the channel voltage gain is sensitive to power supply voltage fluctuations, the fact that the equalizer is immediately followed by a limiter nullifies this factor.

It should be noted that the Gate Controlled Amplifiers (MC 1545) are very sensitive to gate voltage level. To maintain the 4-5 input single-ended voltage gain below -25 dB, the gate voltage low level must not be greater than 0.5V. This level has been achieved by limiting the gate driver (Reference Generator) series impedance to 33 ohms.

4.1.2.7 Limiter/Demodulator Worst Case Analysis. - The Limiter/Demodulator network has been analyzed to ensure reliable operation under ERTS system environmental requirements. RBV and MSS output drift due to temperature and aging effects were determined along with the overall gain variation.

4.1.2.7.1 Design Considerations. - The limiter amplifier stages (Figure 4-12) must provide sufficient gain to accurately preserve the FM signal zero crossings under worst case amplitude variations, while at the same time maintaining an acceptable signal-to-noise ratio. Generally, a minimum of 60 dB of limiting is required. To minimize signal distortion, due to lack of symmetry, the reference level of each limiting stage must be stable. In addition, drift in the input balance will result in carrier feed-thru. Since differential amplifiers are used, limiter balance is relatively independent of power supply regulation. However, any variation in the +8V supply will be reflected on the output amplitude.

The pulse generator output amplitude and pulse width must be constant to minimize carrier feed-thru. Because all the stages following the discriminator are dc coupled, any variation in dc level will be reflected at the RBV and MSS outputs, therefore the dc drift of the discriminator is critical. Also, any drift in the MSS dc offset results in a reduction in the signal-to-noise ratio at the decoder input.

4.1.2.7.2 Summary. - In general, maximum allowable drift limits for individual network stages have not been specified. Since absolute drift data is meaningless, a composite summary of the overall FM chain input/output drift with interstage variations referenced to the Video/MSS output is given at the end of this section.

The limiter contains a minimum of 75 dB gain, which provides reliable limiting with low noise and negligible phase shift. Since the inputs are balanced, the amplifiers are relatively insensitive to power supply variations. Assuming opposite drift coefficients for the input bias resistors, worst case balance drift at each input is ±12 mV due to temperature and ± 80 mV due to aging. A slight amount of additional unbalance may result with aging of the balance adjustment potentiometer.

Laboratory tests have shown that the demodulator pulse generator output is stable with temperature variation. Delay line characteristic variation due to aging is approximately ±1.4%.

Discriminator drift characteristics are not specified; however, laboratory tests indicate a decrease in output signal level with increasing temperature. Consequently, a temperature sensitive resistor (sensistor) has been incorporated into the following amplifier stage to compensate for the discriminator output variation.

Operational amplifier offset current and voltage drift is generally negligible. Laboratory temperature tests of the RBV and MSS low pass filters showed them to be stable.

RBV and MSS output level aging drift is primarily due to the RBV level control and MSS dc offset adjustment potentimeters. Worst case MSS dc level drift due to potentimeter aging is ±217 mV at the output of U5.

A summary of individual component drifts is given in Table 4-7.

4.1.2.7.3 Worst Case Analysis. - The Limiter/Demodulator has been analyzed to determine overall circuit performance and dc stability. Worst case dc drift referenced to the RBV and MSS outputs due to temperature and aging have been calculated.

a. Limiter. - The Limiter consists of three stages of differential amplifiers, each followed by an emitter-follow buffer: A balance control is provided to adjust for any initial dc offset.

1. Difference Amplifiers (U1, U2, and U3). - The Limiter amplifiers are balanced differential input (RCA CA3028B) driven from a constant current source. The gain is fixed primarily by the collector resistor and output loading. Since the amplifiers are self-limiting, nonsaturating, there is no phase shift.

Gain. - The differential amplifier is essentially a common collector stage driving a common-base stage, therefore the voltage gain is proportional to the load impedance. From the manufactuer's specifications, the minimum differential voltage gain for R1=1.6 k ohm is 40 dB, when derated for R1=470 ohm, the minimum gain is approximately 25 dB, which is sufficient to provide reliable limiting.

Symmetry. - The Limiter symmetry is initially optimized for minimum carrier feed-thru by adjusting limiter balance potentimeter R6. Any drift of this setting will result from resistor and potentimeter variation due to temperature and aging. Neglecting the potentimeter variation, the bias input to either side of U1 is given by:

$$V_{in\ 1} = \frac{R_7}{R_7+R_4}\ (V_2+V_3)-V_3 \qquad (1)$$

Assuming V2 and V3 are nominal and any variation will be due to converter regulation, therefore $\Delta V2 = \Delta V3$. Then, substituting ±0.9% drift due to resistor aging into equation 1, worst case ΔV_{in} = ±80 mV or worst case differential input drift is ±160 mV.

TABLE 4-7. LIMITER/DEMODULATOR COMPONENT DRIFT

Component or Parameter	Component Drift		Drift Reflected to Signal Output	
	Temp. 25-61° C	Aging	Temp. 25-61° C	Aging
R4, R5, R7, R8	±24 mV diff. at U1 input	±160 mV diff. at U1 input	Carrier feed-thru	
R6 (100Ω Pot)	Negligible	±28 mV at U1 input	Carrier feed-thru	
±8V at U1	0.5 mV/mV at U1 in.		Negligible if ±8 Track. Sensitive to regulation	
+8V at U3			+8 reflected directly on V3 output	
-8V at U3			-8 Variation results in slight change of constant current.	
Pulse Gen. Amplitude	±0.34% Gain	±1.8% Gain		
Delay line delay	+0.62%, -0.34%	±1.4%		
Z1 Mixer	-70 mV (diode drop)	+30 mV (diode drop)	Mixer output increases	Mixer output decreases
U4	±5 mV	±8 mV	±2.5 mV at R73 ±12 mV at Q11	±4 mV at R73 ±20 mV at Q11
RT1			Increase U4 gain by +5.9%,-4.6%	
R79 (100Ω Pot)	+0.2% of Signal level	±1% of Signal level		

TABLE 4-7. LIMITER/DECODULATOR COMPONENT DRIFT (Continued)

Component or Parameter	Component Drift		Drift Reflected to Signal Output	
	Temp. 25-61°	Aging	Temp. 25-61°	Aging
U5 gain	±0.35%	±1.8%		
U5 offset	±2 mV	±3 mV		
U5 dc level out	±50 mV	±320 mV	±25 mV at receiver	±160 mV at receiver
R84 (SK pot)	±24 mV at U5 out	±217 mV max at U5 out	±12 mV at receiver	±108 mV max at receiver
6.2V at U5 in.	+33 mV	-35 mV	-33 to -66 mV at U5 out	35 to 70 mV at U5 out

Similarly, for a worst case temperature drift of ±0.175%, substituting into equation 1, ΔVin 1 = ±12 mV; or, worst case differential input drift is ±24 mV.

Additional balance drift is contributed by balance adjust potentiometer R6, which exhibits a ±4% variation in tap voltage due to aging. Since the nominal voltage across the potentiometer is approximately 700 mV, worst case drift due to aging is ±28 mV. Using ±0.87% resistance change due to temperature, the maximum potentiometer resistance variation is ±0.87 ohm, which will result in a negligible effect on the balance when the wiper is near the center and will be worst case when the wiper is near either end of the resistance element. Or, worst case potentiometer temperature variation for a drain current of 7 mA is 6 mV, with the wiper at either end.

Power Supply Variation Sensitivity. - Limiter power supplies, V2 and V3 are generated from a common converter and, as a result, any drift in the supplies will generally be in phase. Therefore since the differential amplifiers are balanced, the effect of power supply variation on U1 and U2 is negligible. However, the limiter output level is a function of the available bias current, and thus proportional to the supply voltage. From Figure 4-23, U3 output level is given by

$$V_{out} = V_2 - I_{E3} R_4 - (I_{E3} - I_{E1}) R_5 \qquad (2)$$

where I_{E3}, the constant current source, is

$$I_{E3} = \frac{V_b - (V_{B3} + V_{BE3})}{R_3} \qquad (3)$$

Since I_{E3} is relatively constant, as shown by equation 2, V_{out} is directly proportional to the positive supply voltage variation, V2. The result is a modulation of the limiter output peak-to-peak signal.

By solving equation 3, it can be shown that the constant current, I_{E3} is relatively insensitive to power supply variations.

Where, from Figure 4-23,

$$V_b = \frac{V_3 - I_{E3} R_{39}}{1 + \frac{R_{39}}{R_1 + R_2}} \qquad (4)$$

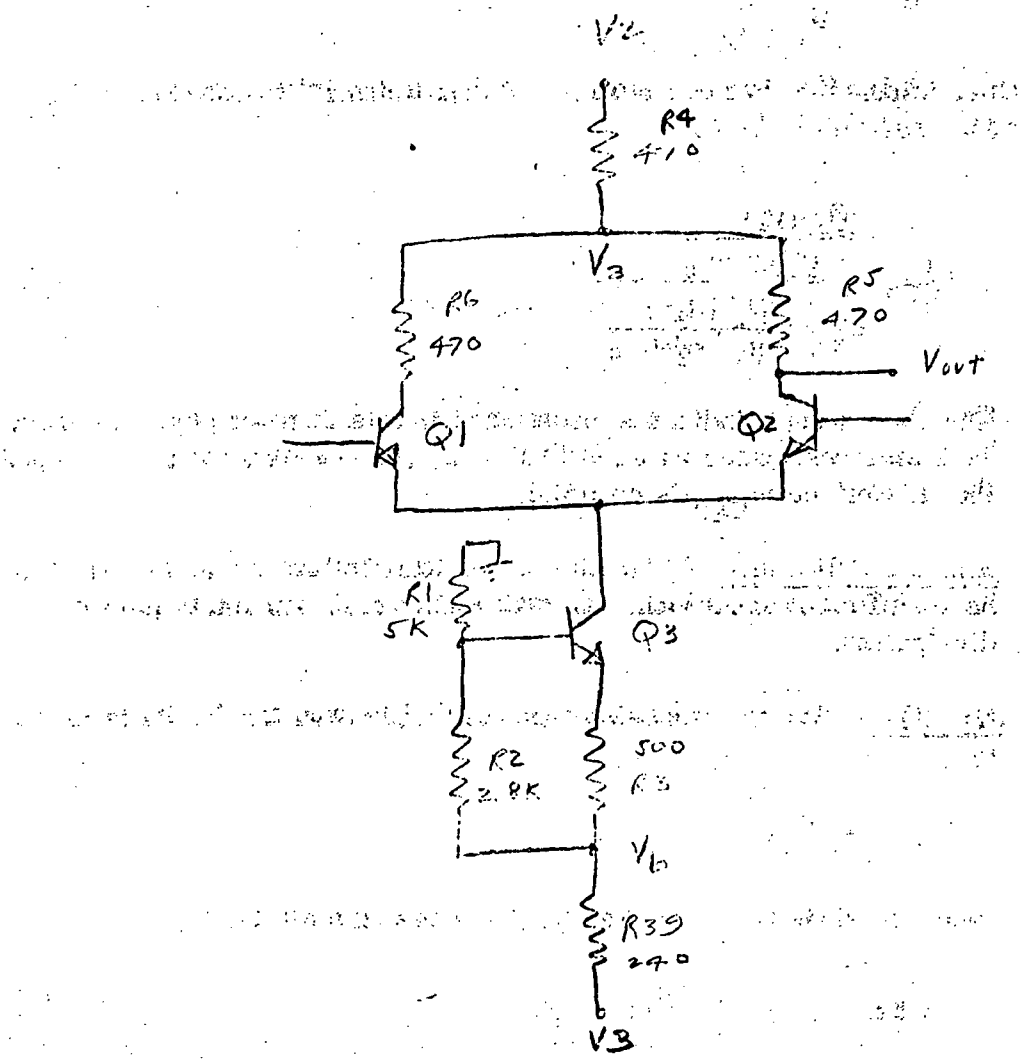


Figure 4-23. Limiter Amplifier U3

and,

$$V_{B3} = \frac{R_1 V_b}{R_1 + R_2} \tag{5}$$

Combining the above equations and substituting into equation 3, I_{E3} as a function of V3 is

$$I_{E3} = \frac{\frac{R_2 (V_3)}{R_1+R_2+R_{39}} - V_{BE}}{R_3 + \frac{R_2 (R_{39})}{R_1+R_2+R_{39}}} \tag{6}$$

The above result indicates any change in V3 is damped by the network base bias resistance ratio. In this case, the resistance ratio ≈ 0.35, thus the effect on I_{E3} is minimal.

Emitter Followers. - The Limiter emitter follower transistors (2N918) have sufficient bandwidth. An additional consideration is power dissipation.

Q1 - Q4. - Average transistor power dissipation for Q1-Q4 is given by

$$P_d = I_C V_{CE} \tag{7}$$

Where, using Q1 as the example, and assuming IC1=IC2,

$$V_{CE} = V_2 - 2 I_{C1} R_{17} - V_{E1} \tag{8}$$

and,

$$I_{C1} \approx I_{E1} = \frac{V_{B1} - V_{BE} + V3}{R_{18} + 2R_{20}} \tag{9}$$

Since $V_B = U_1$ out, then from equation 2, average maximum Vout is

$$\overline{Vout}_{av} = \overline{V2} - I_{E3} R_{10} - (\frac{IE3}{2}) R_{11} \tag{10}$$

Analysis of the Differential Amplifier results in a constant current source of 5.4 ±20% mA. Using the minimum value, I_{E3}=4.4 mA, and from equation 10, $\overline{V_{out}}$ = 5.4 V. From equation 9, I_{E1} = 9.4 mA, and from equation 8, V_{CE} = 3.38 V; thus, the average power dissipation is P_d = 33 mW.

Q5, Q6. - Except for the lower signal level at the input to Q5 and Q6, the power dissipation analysis is identical to that for Q1-Q4. For U3, minimum $I_{E3} \approx 2.2$ mA. Therefore, V_{out} = 7 V, I_{E5} = 10.6 mA, V_{CE} = 1.7 V and P_d = 18 mW.

b. Demodulator. - Basically, the demodulator is a wideband, direct demodulator consisting of an analog pulse generator for each phase of the limiter output. The pulse generator, which converts the limiter output to a series of uniform pulses, is followed by a diode bridge discriminator. After detection and amplification, the carrier is extracted by the introduction of a dc offset in each of the output channels (RBV and MSS).

The critical factors to be considered in the demodulator design are harmonic distortion, linearity, frequency response, signal-to-noise ratio, temperature and time, and dc and linear stability.

1. Pulse Generator. - The pulse generator is a class A amplifier driving a shorted delay line which extracts the leading and trailing edges of the limiter square wave output. The signal output is approximately a 23ns pulse, positive going for the input leading edge and negative going for the input trailing edge. Extracting both leading and trailing edges effectively doubles the discriminator frequency, which facilitates filtering of the undesirable sidebands.

Amplifiers (Q7, Q9). - The demodulator input are class A transistor amplifiers. Base bias current is much greater than the transistor base current, therefore the operating point is independent of the dc current gain. The voltage gain is relatively independent of transistor parameters and is fixed by external components. For Q7, assuming the delay line is a high impedance, the voltage gain is given by

$$A_v = \frac{R48}{R50} \tag{11}$$

Substituting resistance values into equation 11, nominal gain is 2.61 with a ±1.8% variation due to aging and a maximum of ±0.34% variation with temperature.

Since the amplifier's operating point is in the linear region, transistor power dissipation is of importance and, neglecting the output pulses which are of short duration, average power dissipation is given by

$$P_d = I_{C7} V_{CE7} \tag{12}$$

Where quiescently,

$$V_{CE7} = V_{C7} - (V_{B7} - V_{BE7}) \tag{13}$$

and,

$$I_{C7} \approx I_{E7} = \frac{V_{B7} - V_{BE7}}{R_{50} + R_{52}} \tag{14}$$

From Figure 4-12,

$$V_{B7} = \frac{R_{47} (V_5)}{R_{47} + R_{49} + R_{51}} \tag{15}$$

Substituting nominal values into the above equations, $V_{B7} = 10.5$ V, and $I_E = 23.2$ mA. For $V_{C7} \approx 0$, from equation 13, $V_{CE7} = 11.2$ V, and amplifier quiesent power dissipation is $P_d = 260$ mW.

Emitter Followers (Q8, Q10). - Since the base of each transistor is essentially clamped to ground, operating point drift for emitter follows Q8 and Q10 will be negligible.

To determine the power dissipation, and using Q8 as an example, let $V_{B8} = V_{C7} \approx 0$. Then, $V_E = V_{BE}$ and,

$$I_{E8} = \frac{V_3 - V_{BE}}{R_{55} + R_{56}} \tag{16}$$

$$V_{C8} = V_2 - I_C R_{54} \tag{17}$$

Substituting network values into the above equations, $I_{E8} = 24.7$ mA, $V_{CE8} = 6.23$ V and the quiescent power dissipation is $P_d = 154$ mW.

Delay Line. - The delay line is an LC network which simulates a shorted transmission line. The design equations are:

$$L_o = T_d R_o \tag{18}$$

$$C_o = T_d/R_o \tag{19}$$

where,

T_d = Line delay

R_o = Nominal terminating resistance

For R_o = 240 ohms and T_d = 12 ns, L_o = 2.88 uH and C_o = 50 pF.

Assuming inductor aging drift is negligible and temperature drift is ±0.1%; and capacitor drift is given as ±0.5% due to aging and +0.35%, -0.07% due to temperature. Using an RNR resistor for R_o, the cumulative drift is ±1.4% and +0.62%, -0.34% due to aging and temperature respectively. Any change in delay time directly effects the pulse generator pulse width and, ultimately, the demodulator gain.

2. Discriminator. - Discriminator, Z1, an hermetically sealed module, is a balanced-input, transformer-coupled diode bridge. The dc peak output is approximately equal to the peak input signal minus the diode forward voltage drop of about 0.6 V. The specified bandwidth of 0.05 to 200 MHz is sufficient for ERTS system requirements, but overall temperature and aging drift is not specified. However, assuming no change in transformer impedance, diode forward voltage drift may be projected as +5% due to aging and -2 mV/^oC due to temperature. The resulting effect on the discriminator output is a maximum decrease of 30 mV in the signal level due to aging and a maximum increase of 70 mV to temperature.

3. Discriminator Output Amplifier (U4). - U4 is an integrated circuit wideband operational amplifier connected in the non-inverting configuration.

Gain Drift. - The voltage gain is fixed by the external resistor ratio, thus

$$A_V = \frac{R_{70} + R_{74} + RT_1}{R_{70}} \tag{20}$$

where RT1 is a solid-state temperature-sensing resistor which exhibits a temperature coefficient of approximately +0.7%/° C. Using nominal values, A_V = 12 at 25° C. The worst case drift again at 25° C, is A_V ±1%.

The maximum change in voltage gain due to temperature, using 25 °C as a reference, is +5.9% at 61 °C and -4.6% at 0° C. This variation in U4 voltage gain with temperature is tailored to compensate for the change in gain in the pulse generator/discriminator due to temperature.

DC Drift. - The amplifier dc drift due to input offset voltage and current variation with temperature, referred to this output is given by

$$\Delta V_o = \Delta e_{os} \frac{R_i + R_t}{R_i} + \Delta i_{os} R \text{ source} \quad (21)$$

where

$$\Delta e_{os} = e_{os} (T) \Delta T \quad (22)$$

and

$$\Delta i_{os} = i_{os} (T) \Delta T \quad (23)$$

For balanced input source impedances, offset current drift can be neglected. Then, substituting into equation 21, maximum ΔV_O = ±4.8 mV. Since both the positive and negative supply voltage are regulated and temperature compensated, dc output drift due to supply variation will be negligible.

Offset voltage drift due to aging has been assumed to be about 2uV/day, or 0.65 mV/10,000 hours referred to the amplifier input. When referred to the amplifier output, maximum ΔV_O = 8 mV.

4. RBV Low Pass Filter. - The RBV Filter is a Cauer low pass with a cut-off frequency of 4.2 MHz. Laboratory temperature tests have shown negligible drift in phase and frequency response, and, since stable mica capacitor are used, the characteristics should not be effected by aging. Additional RBV signal level drift will be contributed by RBV level control potentimeter R79. Worst case aging drift is ±2% of maximum signal level at R79 maximum, and temperature drift is ±0.43%.

5. MSS Low Pass Filter. - The MSS Filter is a Cauer Low Pass with a cut-off frequency of 11 MHz. As was the case for the RBV filter, the MSS filter has been laboratory temperature tested and shown to exhibit excellent frequency and phase stability over the system temperature range. Also, due to component stability, filter characteristics should not be affected by aging.

6. MSS Output. - The MSS output consists of operational amplifier U5, which extracts the carrier level in addition to providing signal gain, followed by emitter follower stage Q11. In order to minimize the effects of transistor base-emitter nonlinearity and drift, the base-emitter junction of Q11 is included in the output amplifier feedback loop.

   Amplifier (U5). - U5 is an integrated circuit operational amplifier used here in the inverting mode. Closed loop voltage gain is relatively low compared to the open loop gain so that any variation in open loop gain does not affect closed loop gain.

   The MSS signal voltage gain is given by,

$$A_V = \frac{R_{89}}{R_{83}} \tag{24}$$

   Using nominal values at 25° C, $A_V = 5$. Maximum voltage gain temperature drift is ±0.35% and maximum aging drift is ±1.8%.

   Since the source impedances are balanced, output dc drift is due primarily to input offset voltage change and the carrier offset adjustment potentiometer drift. For U5, offset voltage drift due to temperature referred to the output is $\Delta V_{OS} = \pm 2$ mV. Drift due to aging is ±3 mV, and drift due to supply voltage variation is negligible.

   Variation in the MSS dc reference level is primarily affected by drift in dc offset adjustment potentiometer R84. Reflected to the operational amplifier output, the offset level is given by,

$$V_o = \frac{R_{89}\,(V_7)}{R_{84} + R_{85}} \tag{25}$$

Worst case drift will occur when the potentiometer is all the way in the circuit. Using nominal values, the offset level is $V_o = 7.95$ V. Worst case temperature drift (potentiometer all the way in) is $\Delta V_o = \pm 20$ mV, and maximum aging drift is ±130 mV, including the change in closed loop gain. The portion of drift attributed to the potentiometer is given by

$$\Delta V_o = \frac{R_{84}\,(R_{89})\,V_7\,R_{84}}{(R_{84} + R_{85})^2} \qquad (26)$$

Or, for worst case aging, $\Delta V_o = 71$ mV as a result of potentiometer aging. Additional MSS dc output drift results from drift of the offset bias supply voltage (-6.2). As shown by equation 25, the output level is directly proportional to V7, the dc supply. Maximum gain occurs for R84=0. Then, $\Delta V_o = 1.5\ \Delta V_7$ and, using the results of the Regulator Analysis given below, worst case $\Delta V_o = -47$ mV due to temperature and +51 mV due to aging.

Emitter Follower (Q11). - Since the base-to-emitter junction of emitter follower Q11 is incorporated into the operational amplifier (U5) feedback loop, the MSS output level is virtually independent of drift of transistor characteristics.

The power dissipation for Q11 is given by,

$$P_{d11} = I_{C11} V_{CE11} \qquad (27)$$

Where,

$$I_{C11} \approx I_{E11} = \frac{V_6}{R_{90}} = 11.7 \text{ mA},\ V_{CE11} \approx V7 = 6.2 \text{ V},$$

and worst case $P_{d11} = 73$ mW, neglecting the ac signal which is small compared to V_{CE}.

Voltage Regulators. - To ensure supply voltage stability, each Limiter/Demodulator board contains a voltage regulator for the +11.7 V and -6.2 V supplies. Each regulator is a series voltage regulator utilizing temperature compensated reference diodes.

1. +11.7 Vdc (V6). - Referring to Figure 4-12, the regulator output is given by,

$$V_6 = V_{VR1} + V_{CR4} - V_{BE12} \quad (28)$$

For worst case component tolerances the initial range of output voltage is $10.52 \leq V6 \leq 12.68$ V.

Worst case diode and transistor temperature drifts are given as CR4 - 35 mV, VR1 ±47 mV, and V_{BE12} - 60 mV. Substituting into equation 28, maximum $\Delta V6 = -72$ mV due to temperature. Worst case diode and transistor aging drift is given as CR4 +35 mV, V_{BE12} + 70 mV and $\Delta VR1 \approx 0$. Again from equation 28, maximum $\Delta V6 = -35$ mV due to aging.

Q12 power dissipation is given by

$$P_{d12} = I_{C12} V_{CE12} \quad (29)$$

where,

$$V_{CE12} = V4 - I_{C12}\ R95 - V6 \quad (30)$$

For $I_{C12} \approx I_{Load} = 45$ mA, $V_{CE12} = 4.8$ V and $P_{d12} = 216$ mW,

2. -6.2 Vdc (V7). - From Figure 4-12, the -6.2 V regulator output is given by,

$$V_7 = V_{VR2} + V_{CR5} - V_{BE13} \quad (31)$$

For worst case component tolerances, the initial range of output voltage is $5.4 \leq V7 \leq 6.9$.

Worst case diode and transistor temperature drifts are given as VR2 ±19 mV, CR5 - 35 mV, and V_{BE13} - 49 mV. Substituting into equation 31, maximum $\Delta V_C = +33$ mV due to temperature. Worst case diode and transistor aging drift is given as CR5 + 35 mV, V_{BE13} + 70 mV and $\Delta VR2 \approx 0$. Again from equation 31, maximum $\Delta V7 = -35$ mV due to aging.

Q13 power dissipation is given by

$$P_{d13} = I_{C13} V_{CE13} \tag{32}$$

where

$$V_{CE13} = V3 - I_{C13} R_{98} - V_7 \tag{33}$$

For $I_{C13} \approx I_{Load} = 45$ mA, $V_{CEB} = 1.3$ V and $P_{d13} = 58$ mW.

4.1.2.7.4 Conclusions and Recommendations. - Analysis of the Limiter/Demodulator has shown that the Limiter has sufficient gain to provide reliable limiting and both Limiter and Demodulator are inherently temperature stable. However, when utilizing worst case resistor and potentiometer aging specifications in the analysis, the network approaches marginal performance at the end of 10,000 hours of operation. A critical area is in the Limiter balance, where opposite bias resistor aging coefficients result in a differential input level of ±160 mV. The resulting unsymmetrical limiting would result in carrier feed-thru. It should be noted, though, that the type resistor (RNR) presently used for the balance input is very stable and, if manufacturer average aging coefficients are applied, the balance drift becomes negligible.

Since potentiometer aging specifications include vibration effects, the drift coefficients are quite large, particularly in rheostat applications (typically ±7% resistance charge over a 10,000 hour operating period). Therefore, increased network stability can be achieved by reducing the proportionate range of a potentiometer where practical or, if possible, by replacing it with a fixed resistor once final network alignment has been set.

If considerable variation in the +8 V supply is anticipated, a regulated supply should be used on U3 to prevent power supply modulation of the Limiter output.

Some consideration should be given to the establishment of temperature and aging specifications for the variable inductors used throughout the network, and also for discriminator module Z1.

The power dissipation of Q7 through Q10, and Q12, is much higher than can be dissipated through radiation alone; thus, an appropriate amount of thermally conductive adhesive should be applied between the transistor cases and the printed board to provide a path for heat conduction.

4.1.2.8 RBV Video Out Worst Case Analysis. - The RBV Video Output Network has been analyzed to ensure reliable operation under ERTS system environmental requirements. RBV output drift due to temperature and aging effects were determined along with the overall gain variation.

4.1.2.8.1 Design Considerations. - Of primary concern in the Video Out design is the cumulative drift due to temperature and aging effects, and signal gain variation. In addition, transistor switch ON/OFF stability must be assumed and logic gate worst case triggering requirements fulfilled. Since the "LOW" level input to gating flip-flop U4 comes from an OFF transistor, the source inpedance should be such that the TTL gate input voltage is satisfied under worst case input current requirements.

The maximum allowable signal level into the 2 X 1 switches should be determined for the specified FET gating levels. Also, the Video Out signal range and dc reference level must meet system specifications.

4.1.2.8.2 Summary. - Individual component and amplifier worst case drift factors are tabulated in Table 4-8, along with the magnitude of drift when reflected to the network output.

Since operational amplifiers with low closed loop gains are used, the video-output network voltage gain is relatively stable. DC reference drift is primarily due to the adjustment potentiometer aging characteristics and internal voltage regulator dc output variation.

Worst case dc level drift at the input to the 2 X 1 switches as a result of resistor and potentiometer variation is ± 0.5% due to temperature and ± 5% due to aging. -6.2V regulator drift contributes an additional +2, -17mV due to temperature, and -50mV due to aging at the switch inputs. A similar amount of drift due to resistor and potentiometer variation occurs at the output of amplifier U3. Also, at the U3 output, the +11.7V regulator drift adds +5, -10mV due to temperature and +17mV due to aging.

In order to meet the worst case drive requirements of the FET switch gating flip-flop, the maximum allowable source impedances of the triggering stages (Q7, Q8, and Q9) were computed. The resistances are: R44 = R49 = 560 ohms and R47 = 270 ohms. Furthermore, since the FET switching criteria is based on the magnitude of the gate-to-source voltage, the allowable signal range for a TTL gating level and FET's with a maximum pinch-off voltage of -0.8V, is -2.6 to -4.1V. These limits result in a maximum signal range of 1.5V.

TABLE 4-8. RBV OUTPUT COMPONENT DRIFT SUMMARY

Component or Parameter	Component Drift		Drift Reflected to RBV Output	
	Temp 25-61°c	Aging	Temp. 25-61°c	Aging
R1 (10K Pot)	± 7mV at U1 out	±52mV at U1 out	± 7mV	± 52mV
U1 and U2	± 1mV dc ± 0.35% gain at U1 out	± 1.9mV dc ± 1.8% gain at U1 out	± 1mV dc ± 0.35% level	± 1.9 mV dc ± 1.8% level
Q1, Q2 Q3, Q4 (R_{DS})	0.4% level		Negligible for matched FET's	
U3	± 1.5mV dc ± 0.35% gain at U3 out	± 3mV dc ±1.8% gain at U3 out	±0.75mV dc ±0.35% level	± 1.5mV dc ± 1.8% level
R23 (1K Pot)	± 3mV dc at U3 out	± 54mV dc at U3 out	± 1.5mV	± 27mV
Q5 and Q6	negligible when matched	negligible when matched		
-6.2V Supply	-4, +34mV	-100mV	-17mV, +2mV	+50mV
+11.7V Supply	+63, -32mV	-100mV	-5, +2.5mV	+8.50mV
Total - dc			+14.7, -32.2mV	+140.9, -82.4mV
Total - gain			± 0.7%	± 3.9%
RBV Clamp (Zener + diode (-3.4V)	-118mV	± 180mV	-59mV	± 90mV
RBV Clamp (+.4V)	-30mV	-	-19mV	-

4.1.2.8.3 Worst Case Analysis. - The RBV Video Output circuit has been analyzed to determine overall circuit performance and dc stability. Worst case dc drift and gain variation due to temperature and aging have been calculated. Transistor switch stability has been verified, and the worst case allowable switching signal level determined.

a. Amplifiers - (U1 and U2). - U1 and U2 are identical wideband operational amplifiers which are connected in the inverting mode. Gain variation will be due primarily to drift in the external resistors, and dc output level variation is caused by amplifier input offset voltage drift and the balance control and reference voltage supply drift.

1. Gain Drift. - For a large open loop gain, the closed loop voltage gain for U1 is given by

$$A_V = \frac{R_8}{R_3} \qquad (1)$$

Using nominal values, $A_V = 2.87$, and maximum temperature and aging drift are ± 0.35% and ±1.8% respectively.

2. Offset Drift. - Since the input source resistances are balanced, drift due to offset current may be neglected. The offset voltage drift is given by

$$\Delta V_O = \Delta e_{os} \frac{R_8}{R_3} \qquad (2)$$

where the temperature drift $\Delta e_{os} = \pm 350$ uV. Substituting into equation 2, $\Delta V_O = \pm 1$mV.

Offset voltage drift due to aging is assumed to be ±0.65mV/10,000 hours. Referred to the amplifier output, $\Delta V_O = \pm 1.9$mV.

3. Balance Drift. - The balance drift consists of two components: drift in the output due to resistor and potentiometer variation, and drift due to reference voltage variation (-6.2V). From Figure 4-13, the balance offset at the output of V1 is given by

$$V_O = \frac{R_8}{R_1 + R_2} V_7 \qquad (3)$$

Since the potentiometer drift coefficient is considerable, the worst case balance drift occurs with potentiometer R1 all the way in the

circuit. Substituting into the above equation, nominal offset is 1.735V and worst case drift is ±0.5% due to temperature and ±5% due to aging.

From the voltage regulator analysis given at the end of this section, the -6.2 reference voltage drift, neglecting load regulation effects, is -4, +34mV due to temperature and -100 mV due to aging. When reflected to the output of U1, reference voltage drift with the potentiometer all the way out, is -17, +2mV due to temperature and +50mV due to aging.

The combined balance drift at the output of U1, including U1 offset voltage drift is +11, -26mV for temperature and +132, -82mV due to aging.

b. 2 X 1 Switches. - The 2 X 1 switches consist of two pairs of field effect transistor (FET) stages which are triggered by a flip-flop. The flip-flop is clocked by the Reference Generator X, $\overline{X}$, and $\overline{H}$ gates, through a set of transistor level shifters.

1. FET Switch. - Q1 through Q4 are N-Channel field-effect transistors. The switch is gated OFF when $V_{GS} \geq V_{GS}$ (OFF), and appears as an open circuit. (V_{GS} (OFF) is the gate to source voltage required to cut off channel current.)

   For $V_{GS} = 0$, the switch is ON, with R_{DS} (ON), the drain-source on-state resistance, appearing in the signal line. Since R_{DS} increases with temperature, signal transfer will be affected.

   Using manufacturer's characteristics, typical $R_{DS} = 16$ ohms, and the temperature coefficient is 0.13 ohm/°C. Or, worst case drift is +4 ohms at 60°C, which is approximately 0.4% of the switching level. Since there is a FET switch in each side of the voltage divider feeding U3, it may be assumed the two R_{DS} drifts will be similar; thus, the effect on signal level is negligible.

   Due to the effects of interelectrode capacitances, switching transients are characteristic of FET switches. Generally, however, these transients may be filtered and appear as a constant level which may be offset by an out of phase dc level.

2. Switch Driver. - The FET switches are driven by the complementary outputs of a TTL flip-flop. When the series switch of each pair is OFF, the shunt switch is ON, grounding the output of the series switch.

Since the flip-flop is referenced to -5.1 volts, the triggering signals were required to be generated by a set of transistor switch level shifters, where a "1" input is equivalent to -5V.

Switch Ouput Level. - The maximum allowable input to the flip-flop to ensure a logical 0 is 0.8V. Therefore, since the flip-flop is referenced to -5.1V, the minimum "0" level is -4.3V. Thus, for Q7 and Q9, which drive 1 unit load, the maximum allowable collector resistance is:

$$R_C = \frac{V_8 - V_{in}(0)}{I_{in}(0)} \qquad (4)$$

Since the drivers and flip-flop use the same supply voltage, nominal voltage may be used. For V8 = 5.1V, and worst case TTL input levels, from equation 4, $\overline{R_C}$ = 500 ohms. Similarly for Q8, which drives 2 unit loads, $\overline{R_C}$ = 250 ohms. The driver "high" level is governed by maximum transistor V_{CE}, which is approximately 0.2V. This "high" level exceeds TTL input requirements.

Drive Requirements. - During the ON condition, the transistor collector current is given by:

$$I_C = \frac{V_8 - V_{CE}}{R_C} \qquad (5)$$

Letting R44 = R49 = 560 ohms and R47 = 270 ohms, and solving equation 5, $I_{C7} = I_{C9}$ = 8.9 mA and I_{C8} = 18.5mA. Maximum required base current is given by:

$$I_B = \frac{I_C}{h_{FE}} \qquad (6)$$

Or, for h_{FE} = 60 at 0°C, maximum required $I_{B7} = I_{B9}$ = 0.15mA and I_{B8} = 0.31mA.

From Figure 4-13, the available base current for Q7 is:

$$\underline{I_B} = \frac{V_8 - \overline{V_{BE}}}{R_{43}} - \frac{\overline{V_{BE}} + \overline{V_{in}}}{R_{42}} \qquad (7)$$

For R42 = 12k, R43 = 6.8k and V_{in} = 0.45V, from equation 7, I_B = 0.15mA. Similarly, for Q8, R45 = 3.3k, R46 = 5.6k and V_{in} = 0.5V then, from equation 7, I_B = 0.33mA. Both the above results are sufficient to insure the drivers will turn ON under minimum h_{FE} conditions.

Flip-Flop Output Level (U4). - From the manufacturers specifications, the nominal flip-flop (U4) levels are "0" = 0.1V and "1" = 3.3V, and the minimum range is given as 0.2 to 2.4V. When the output is referenced to -5.1V, the nominal range is "0" = -5V and "1" = -1.7V, and the minimum range is -4.9 to -2.6V.

Signal Range. - Since the FET switch switching requirements are

Switch OFF: $V_{GS} \geq V_{GS}$ (off) or V_P

Switch ON: $V_{GS} = 0.$

The maximum signal level that can be accurately switched depends on the FET pinch-off voltage (V_P or V_{GS} off) and the minimum available gate Voltage.

or, $$V_S = V_G - V_P \qquad (8)$$

For minimum V_P = -0.8, from equation 8 maximum signal voltage is -4.1V. To satisfy the FET ON condition, minimum V_S = -2.6V. Thus, the allowable signal range for V_P = -0.8, is 4.1 - 2.6 = 1.5V. As the FET V_P increases in magnitude, the switchable signal range decreases; therefore, the FETs should be selected to be compatible with the desired signal level and TTL gating range. Clearly, since the 2N4861 has a maximum V_P = -4 V, and if turn-ON conditions are met, the switch may never be turned OFF under TTL output worst case levels.

c. Amplifier (U3). - U3 is a wideband operational amplifier connected in the non-inverting mode. Since the open loop gain is relatively high, gain variation will be due primarily to drift of the external bias resistors. DC output level variation is caused by amplifier offset voltage drift, the dc offset control potentiometer and the offset reference power supply.

1. Amplifier Drift. - Neglecting the effects of the OFFSET bias divider, the closed loop gain for U3 is given by:

$$A_V = \frac{R_{26} + R_3}{R_{26}} \tag{9}$$

Using nominal values, $A_V = 4.48$ and maximum temperature and aging drift are approximately ±0.35% and ±1.8% respectively.

Since the input source resistances are balanced, drift due to offset current may be neglected. The offset voltage drift is given by:

$$\Delta V_O = \Delta e_{os} \quad A_V \tag{10}$$

Due to temperature, $\Delta e_{os} = \pm 350\,\mu V$ and, substituting into equation 10, $\Delta V_O = \pm 1.5mV$. Offset voltage drift at the amplifier input due to aging is assumed to be ±0.65mV/10,000 hours. Referred to the output of U3, $\Delta V_O = \pm 3mV$.

2. DC Offset Adjustment Drift. - DC offset drift is a combination of Potentiometer drift and dc reference supply drift.

Potentiometer (R23). - From Figure 4-13, the adjusted dc offset at the amplifier output is given by:

$$V_o = \frac{R_{30}}{R_{26}} \quad V_{REF} = 3.5 \; V_{REF} \tag{11}$$

where,

$$V_{REF} = \frac{R_{25}}{R_{23}+R_{24}+R_{25}} \; V_6 \tag{12}$$

Assuming V6 is constant, and the potentiometer resistance is completely in the circuit, from equation 12 the reference voltage temperature drift is ± 1mV and the aging drift is ±18mV. Due to the amplifier gain, the offset voltage drifts at the amplifier output are ±3mV and ±54mV due to temperature and aging respectively. It should be noted that the bulk of the aging drift can be attributed to the potentiometer, which has a ±7% aging coefficient.

-11.7V DC Reference. - From the regulator analysis (Paragraph 4.1.2.8.3.e) the +11.7 voltage drift, neglecting load regulation effects, is +63, -32 mV due to temperature and -100mV due to

aging. When reflected to the output of U3, the maximum dc drift (potentiometer all the way out) is approximately:

$$V_o = \frac{A_V \Delta V_6}{22.5} \quad (13)$$

Thus, from equation 13, the offset variation due to the supply voltage drift is -10, +5 V due to temperature and +17mV due to aging.

3. Zener Clamp (VR1). - The peak output of operational amplifier U3 is regulated by Zener diode VR1. The clipping level is given by:

$$V_{RBV} = V_{CR5} + V_{VRI} \quad (14)$$

Using component initial tolerances, the clipping range at 25°C is 3.22 to 3.56V. Temperature drift is approximately -2.7% at 60°C and aging drift is ±6%.

d. Emitter Follower (Q5 and Q6). - Q5 and Q6 are complementing transistors connected as an emitter follower. Since the nominal temperature coefficients are similar, the differential dc drift will be negligible. The power dissipation is given as:

$$P_d = I_C V_{CE} \quad (15)$$

For Q5, I_C = 6.7mA, V_{CE} = 11.7V and average P_{d5} = 79 mW. Similarly, for Q6, I_C = 11.7mA, V_{CE} = 6.2V and P_{d6} = 72mW.

e. Voltage Regulators. - The RBV output circuit is powered by three internal voltage regulators; +11.7V (V6), -6.2V (V7) and -5.1 (V8).

1. +11.7V Supply (V6). - The +11.7V supply is derived from the +22V converter output through a series regulator. The regulated output voltage is given by:

$$V_6 = V_{VR2} + V_F - V_{BE} \quad (16)$$

Using initial tolerances, the output voltage range at 25°C is 10.77 to 12.58V. Temperature drift (25° - 60°C, neglecting Zener regulation) is +63, -32mV, and aging drift is -100mV. A slight amount of

additional drift is possible due to series resistor (R56) variations, resulting in Zener voltage regulation effects. The series transistor power dissipation may be written as:

$$P_d = V_{CE} I_L \tag{17}$$

where,

$$I_L = U1 + U2 + U3 + dc\ offset + Q5 + Q6 \tag{18}$$

and,

$$V_{CE} = V_4 - I_L R_{55} - V_6 \tag{19}$$

Using nominal values, I_L = 43mA. Then, from equation 19, V_{CE} = 4.7V and the power dissipation is P_{d10} = 207mW.

2. -6.2V Supply (V7). - Q11 is also a transistor series regulator. The output voltage is given by:

$$V_7 = V_{VR3} + V_F - V_{BE} \tag{20}$$

Using initial tolerances, the output voltage range at 25°C is 5.55 to 6.8V. Temperautre drift (25° - 60°C, neglecting Zener regulation) is -4, +34mV, and aging drift is -100 mV. Additional regulation variations may result from resistor R58 aging. Q11 power dissipation is given by equation 17

where,

$$I_L = U1 + U2 + U3 + Q_5 + Q_6 + V_{bias} = VR_1 \tag{21}$$

and,

$$V_{CE} = V_3 - I_L R_{57} - V_7 \tag{22}$$

For nominal values, I_L = 54mA. Then, from equation 22, V_{CE} = 1.3V, and P_{d11} = 70mW.

3. -5.1V Supply. - The -5.1V supply is a Zener Shunt regulator. The initial tolerance is 5.32 to 5.88V and drift is ±6% due to aging and a maximum of ±0.1% due to temperature.

Regulator dissipation is

$$P_d = V_8 \ (I_Z) \tag{23}$$

where,

$$I_Z = I_{in} - I_{Load} \tag{24}$$

and,

$$I_{in} = \frac{V_3 - V_8}{R_{59}} \tag{25}$$

and the load current is

$$I_L = Q7 + Q8 + Q9 + U4 \tag{26}$$

For the transistor bias resistors specified above, I_L = 38 mA.

Using maximum converter voltage and R59 = 56 ohms, $\overline{I_{in}}$ = 61mA, and $\overline{I_Z}$ = 23mA, which is sufficient to maintain regulation. Substituting into equation 23, worst case Zener dissipation is P_d = 118 mW.

4.1.2.8.4 Conclusions and Recommendations. - Worst Case Analysis of the Video Output Network has shown that most of the temperature and aging drift is due to the characteristics of the balance and offset adjustment potentiometers. Therefore, added circuit stability may be achieved by using lower range potentiometers or, where possible, by replacing the potentiometer with a fixed resistor once final signal alignment has been completed.

Since the FET switch gating pulse is limited by worst case TTL logic output requirements, the maximum allowable input signal is restricted by the FET pinch-off voltage (V_{GS} off). As a result, the FETs used in the 2 X 1 switch should be selected for a V_{GS} off which is compatible with the maximum signal to be switched (approximately -0.8 to -1V). In addition, to ensure the ON condition, the minimum switch input level should be set for the gating signal (flip-flop output) worst case "1" level (-2.6V).

The effects of Zener diode voltage regulation on the internal dc regulators due to resistor aging may be minimized by using RLR type resistors (R56 and R58) in series with the Zener diodes.

Any future printed board layout change should incorporate a matched complementary transistor pair (single package) for the Q5 and Q6 emitter follower. Such a device eliminates the possibility of a poor match of two individual transistors and reduces the effects of temperature gradients between separate units.

The power dissipation of series regulator transistor Q10 is much higher than permitted for radiation cooling alone, therefore urethane beads should be added to provide a path for heat conduction.

4.1.3 MSS System Circuit Description. - As stated before, the MSS system requires circuits that are common to the RBV channel; for detailed circuit descriptions of the common elements, see the corresponding paragraphs in the RBV section.

4.1.3.1 Input Network (Figure 4-24). - The MSS data along with the 15 MHz sync signal feed a pair of dual input line receivers through 50-ohm shielded lines. The signal level at the receiver inputs is approximately 150 mV p-p measured across 50 ohms. A TTL compatible output level is developed at the receiver output when the differential input exceeds 25 mV. The receiver outputs trigger a D type flip-flop which provides the desired MSS data levels. In order to ensure sufficient SET/RESET setup and hold times for the flip-flop, the MSS data is delayed approximately 12 ns through two "NAND" gates (U2).

In addition to clocking the MSS data flip-flop, the sync feeds a gate (U4) which, in turn, drives a modulo-10 counter. The counter divides the 15 MHz sync signal to a 1.5 MHz square wave, which, after being low pass filtered, provides the system pilot tone.

After the MSS data is re-clocked, it then feeds a low-pass filter which has its input and output isolated by complementary transistor pair emitter followers. The emitter follower transistors are matched in order to minimize dc drift. Potentiometer R48 is used to control the signal level. The filter output then goes through a high frequency pre-emphasis network which feeds a matched transistor pair connected as an emitter follower. A second potentiometer is connected to the emitter follower and is provided to adjust the MSS dc level into the modulator to approximately +1.2 to +1.7 V.

A change in the exact frequency of the timing standard has been made by NASA; instead of 15 MHz, it has now been determined as 15.062630 MHz. All circuit designs and components are being adjusted to comply with this new standard.

From the MSS input circuitry the signal proceeds to the modulator where it is processed in a manner similar to the RBV signal (paragraph 4.1.2.4). The pilot tone signal is added to the modulator output after the mixer, where its absolute level can be adjusted as required. From there the combined signals go to the following boards, which are described in the RBV section: Record Current Adjust, Record Amplifier, Preamplifier, Playback Amplifier, and Equalizer. The circuits exclusively devoted to the MSS system are the decoder and buffering systems, which are described in the following paragraph.

4.1.3.2 Decoder and Variable Clock Phase Correction Loop. - The MSS data from the 1-3 Limiter/Demodulator and the 2-4 Limiter/Demodulator are fed through the corresponding filter equalizers before application to a pair of dual line receivers (Figure 4-25). By cross connection of the dual line receivers, two TTL

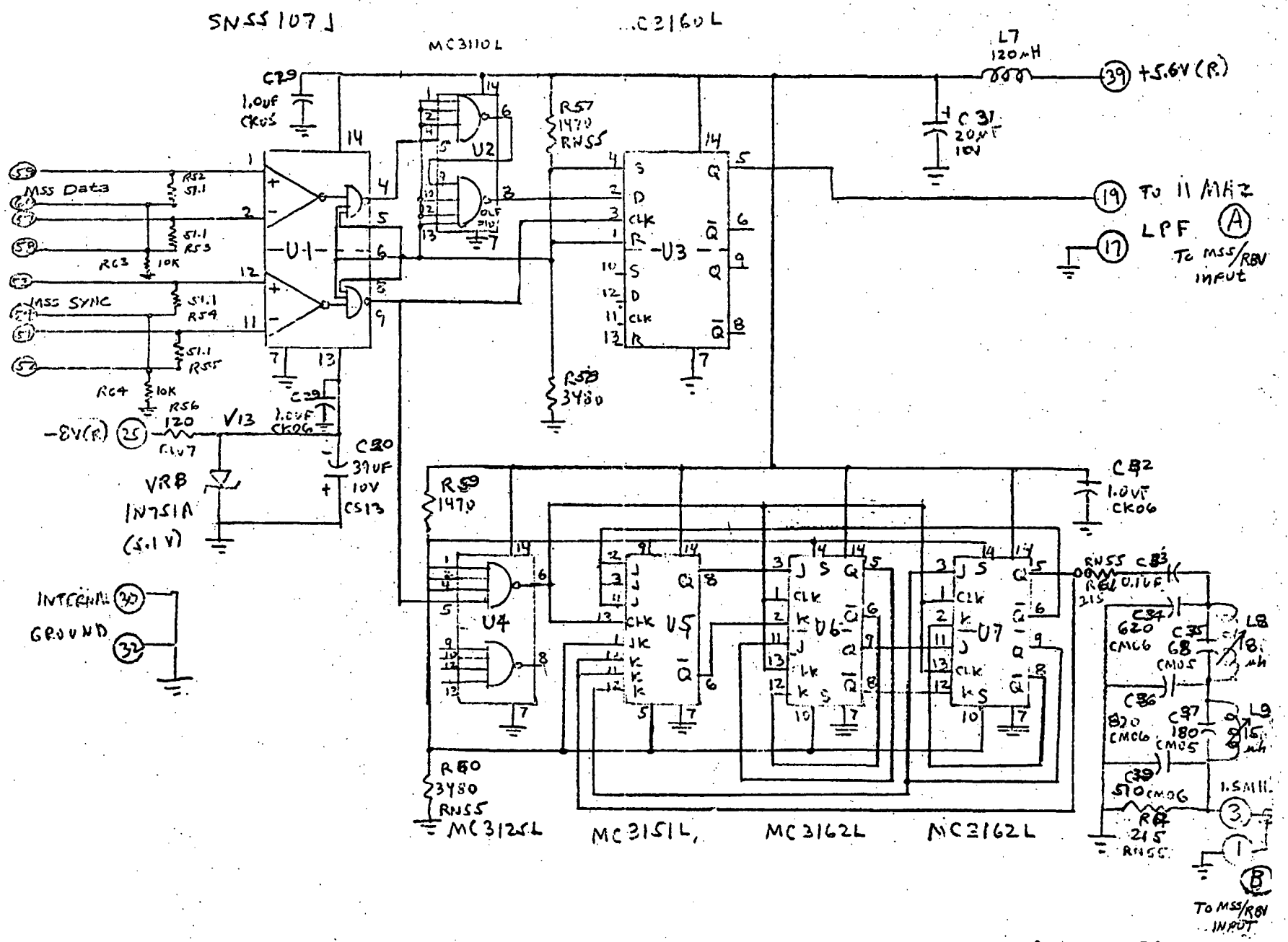


Figure 4-24. MSS Input Network

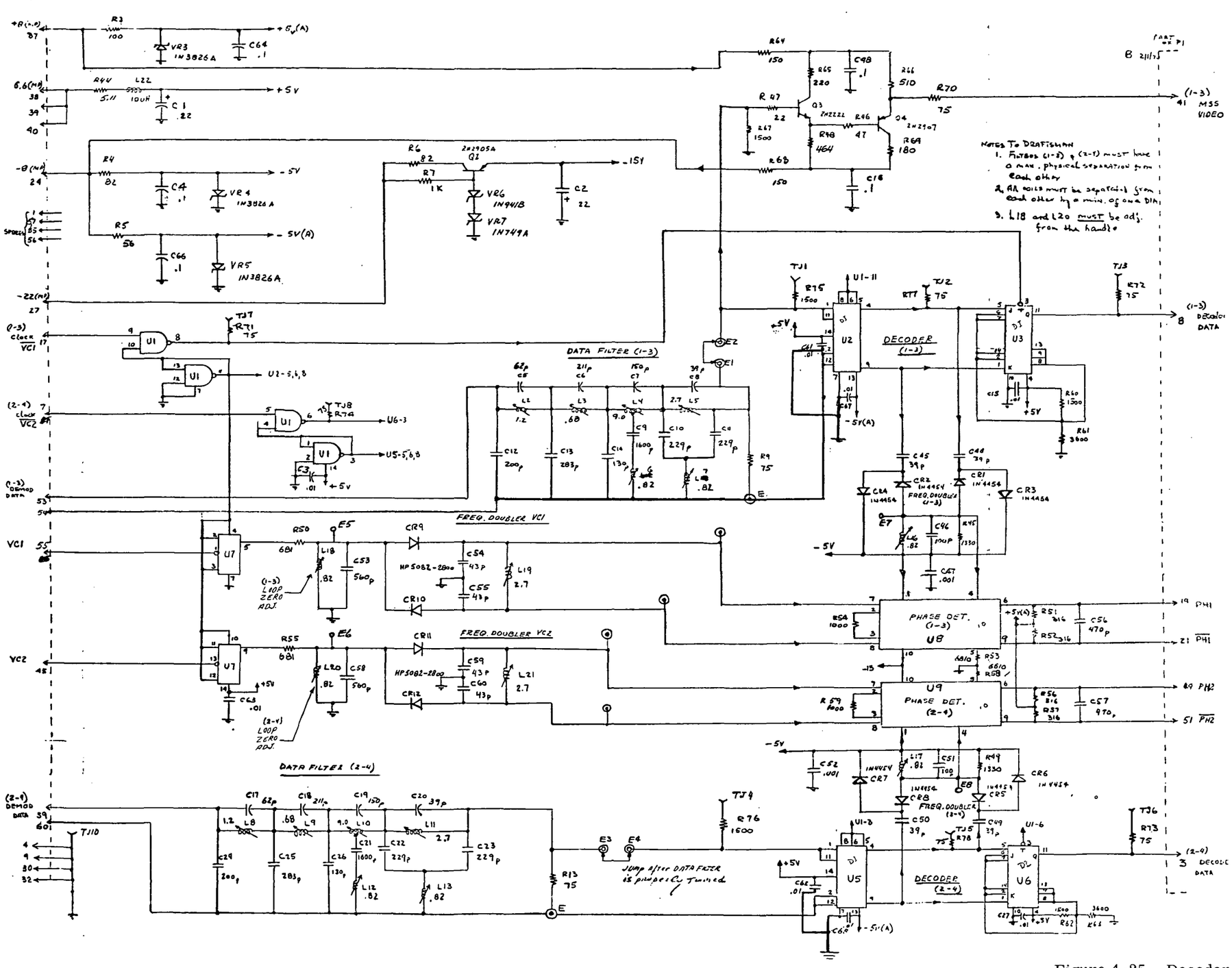


Figure 4-25. Decoder and Variable Clock Phase Correction Loop

compatible outputs are developed for each signal in quasi push-pull. The pair of outputs are connected as the J and K input of J-K flip-flops, which are triggered by the 1-3 and 2-4 clock. The result is a re-clocking of the limiter/demodulator MSS output signals before they are sent to the buffering system.

In addition, the MSS data is used to provide a reference for the variable clock phase correction loop, which includes a frequency doubler and phase detector. The phase correction loop compares the phase of the clipped MSS data directly with that of the variable clock and, if necessary, performs a correction on the variable clock phase. Since the phase correction is performed at a high frequency, it has greater phase stability than the variable clock circuitry which compares phase at a low frequency. It can correct for phase drifts between the data and pilot tone which might occur due to circuit drifts or head wear. In addition, the phase correction loop contains circuitry for effecting a differential phase adjustment to compensate for differential phase errors between heads.

The variable clock (VC) phase correction loop block diagram is shown in Figure 4-26 and the schematic is shown in Figure 4-27. The MSS data and VC frequency doublers and the phase detector are located on the decoder board while the dc amplifiers, loop filter and voltage controlled phase shifter are located on the variable clock board.

The loop receives MSS data from the data clipper and frequency multiplies the signal to 15 MHz; the frequency multiplication removes polarity information from the data transitions. The signal is compared with the variable clock signal in a phase detector and an error signal is generated proportional to the phase difference between them. This error is amplified and applied to an electronically variable phase shifter in the variable clock which corrects the phase to a degree determined by the position constant of the feedback loop (zero order feedback loop).

The differential phase signal is generated by using the tonewheel switching signal and a differential amplifier to superimpose the head to head correction on the dc phase correction. The differential phase adjustment has no dc component, and therefore does not affect the static phase.

4.1.3.3 Buffering System. - The basic operation of the buffer system is shown in Figure 4-28A. The incoming digital data is sequentially placed into various buffer registers; here, six units are shown and are labeled A through F. Depending upon the phase of the variable clock, any one particular data bit may be read into any one of the six storage devices shown. Read out of the stored information is accomplished by means of the master clock, which sequentially interrogates the state of the storage register. The phase relationship shown in the figure shows maximum buffering capability; that is, the read out is in opposite phase with respect to read in.

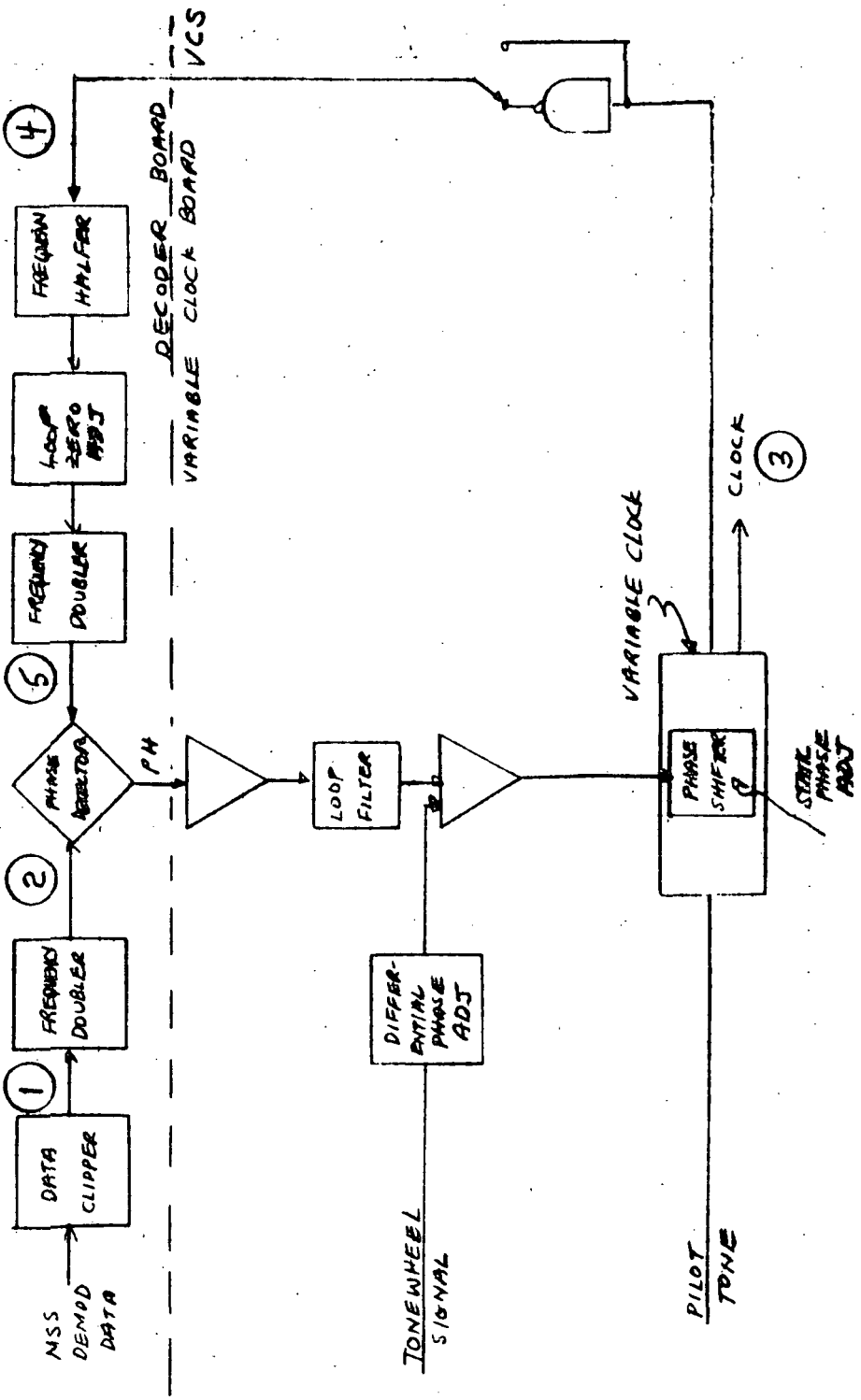


Figure 4-26. Phase Correction Loop Block Diagram

TO BE REVISED

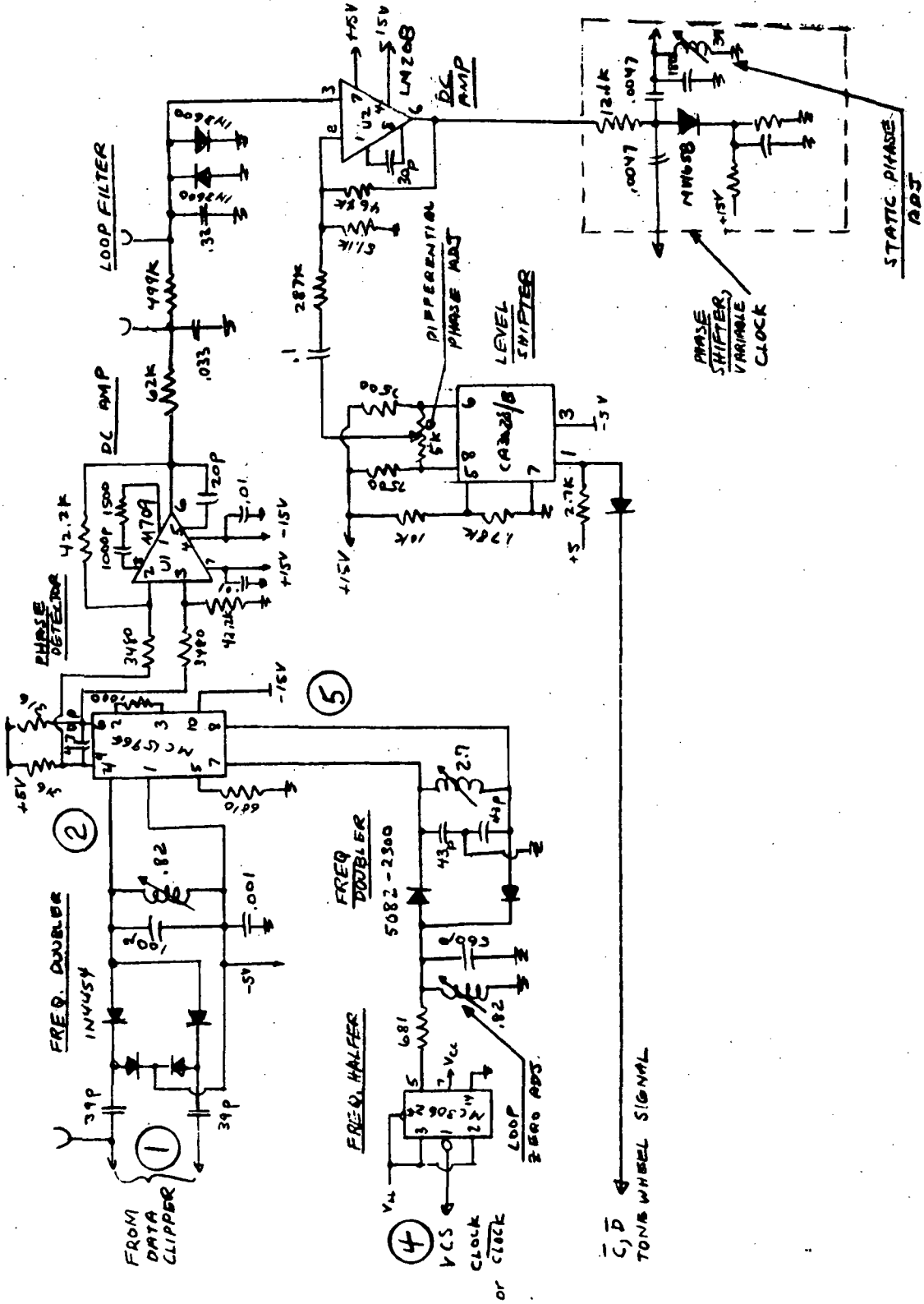
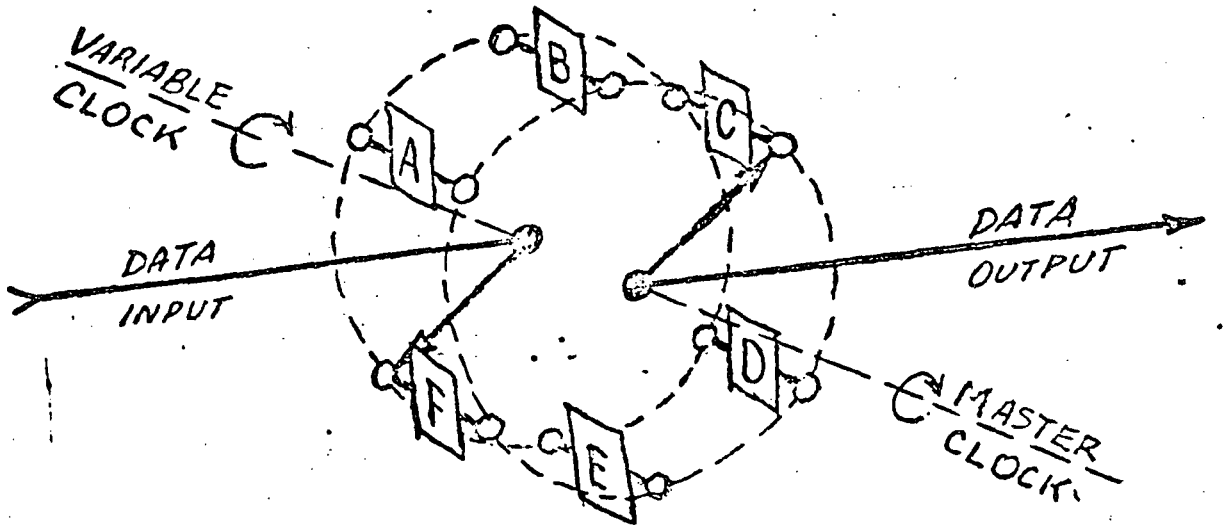
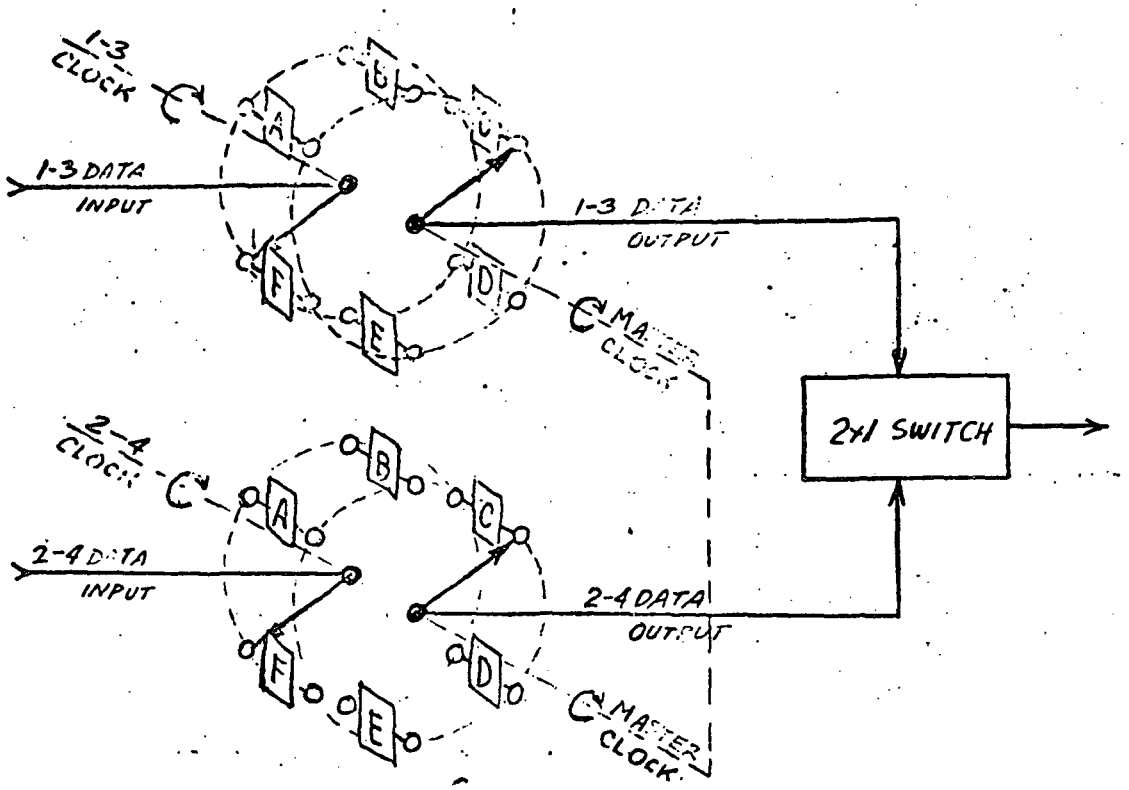


Figure 4-27. Phase Correction Loop Schematic (One Channel)

TO BE REVISED



A. Basic Operation



B. Functional Diagram

Figure 4-28. Buffer System

In other words, the variable clocks can be advanced or retarded by two bits before the data output signal will be garbled.

Figure 4-28B shows a more complete buffering system. The two halves of the buffer are shown; one for the data derived from heads 1 and 3 and the corresponding clocks, and one for the data derived from heads 2 and 4 and the corresponding clocks. The readout is derived by one single master clock system. From this diagram, it should become apparent that the variable clocks and their respective input data can assume various phase relationships and still achieve good output data as long as two requirements are not violated:

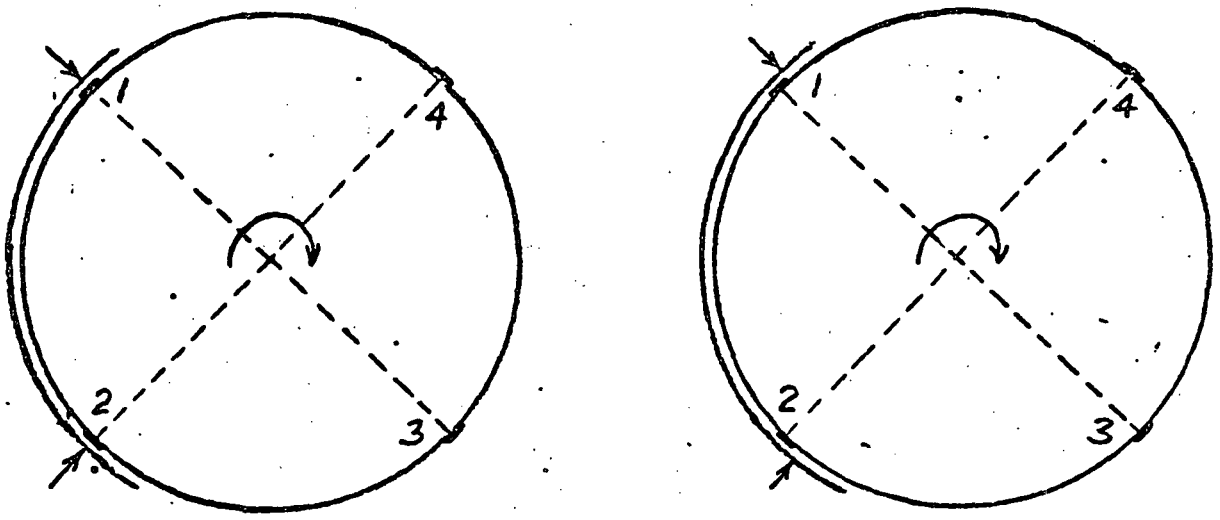
1. Neither of the variable clocks must ever cross the instantaneous phase of the master read-out clock.

2. The information stored in any like-designated storage register by the 1-3 or 2-4 channel must be identical even though the time of storing this information may be variable.

If both of these requirements are observed, the information derived from the 1-3 channel will be identical to that from the 2-4 channel, so that a switch-over can be achieved by use of a simple digital switch.

The first requirement can be easily met by knowing the amount of shoe error that can be expected in the system and providing sufficient storage elements in the buffering system. The second requirement will be met automatically as explained by Figure 4-29. If, on playback, the tape is stretched more than it was during record, the data and pilot tone (and hence the clock) frequencies will all be slightly reduced. This means that, toward the end of the head scan, the 1-3 clock will have fallen behind its nominal position. Under these conditions, a particular information bit will also be played back late. Thus, the information that nominally would have been store in Position F will still be stored there, although the time of storage will be late. Similarly, in the stretched tape condition, the head will establish an early clock relationship with respect to the master clock as it enters the tape. In other words, it will have advanced with respect to the master clock. Note, however, that under these conditions a particular information bit will have been played back early so that it, too, will have been placed into storage register F.

From the above discussion, it is obvious that any particular information bit will be stored into the proper storage element, though the actual storage operation may have occurred at slightly different times. Thus, by having the identical information bit in like-designated storage devices, the read out information read by the master clock from either storage register will be identical.



(a) Playback under normal conditions

(b) Playback under stretched tape conditions

The arrows indicate a redundant bit of information that is stored near the two edges of the tape. It is read out by heads 1 and 2 during the overlap period.

Figure 4-29. Effect of Transverse Tape Stretch

The actual manner in which the buffering is accomplished and the phases of the clocks are controlled is shown in Figure 4-30.[1] The clocks of the data buffers are directly controlled by the timing waveforms extracted from within the phase locked loop of the individual clocks. In this manner the phase of each variable clock is permanently linked to the phase of the pilot tone; during start up, tape dropout, or rest-out between short recordings, there is always a known phase relationship between the variable clock and pilot tone. And, since the pilot tone was recorded concurrently with the data, there is always a known phase relationship between the variable clock and the data.

A similar situation is present in the master clock system. There are, however, two differences: first, the bandwidth of the master clock system is much narrower than that of the variable clocks which results in an essentially fixed MSS output frequency; secondly, the phase of the data read-out vector is connected oppositely to that of the read-in vector which allows for maximum data buffering capability.

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[1] This system is based upon suggestions made by NASA Engineering (M. Maxwell).

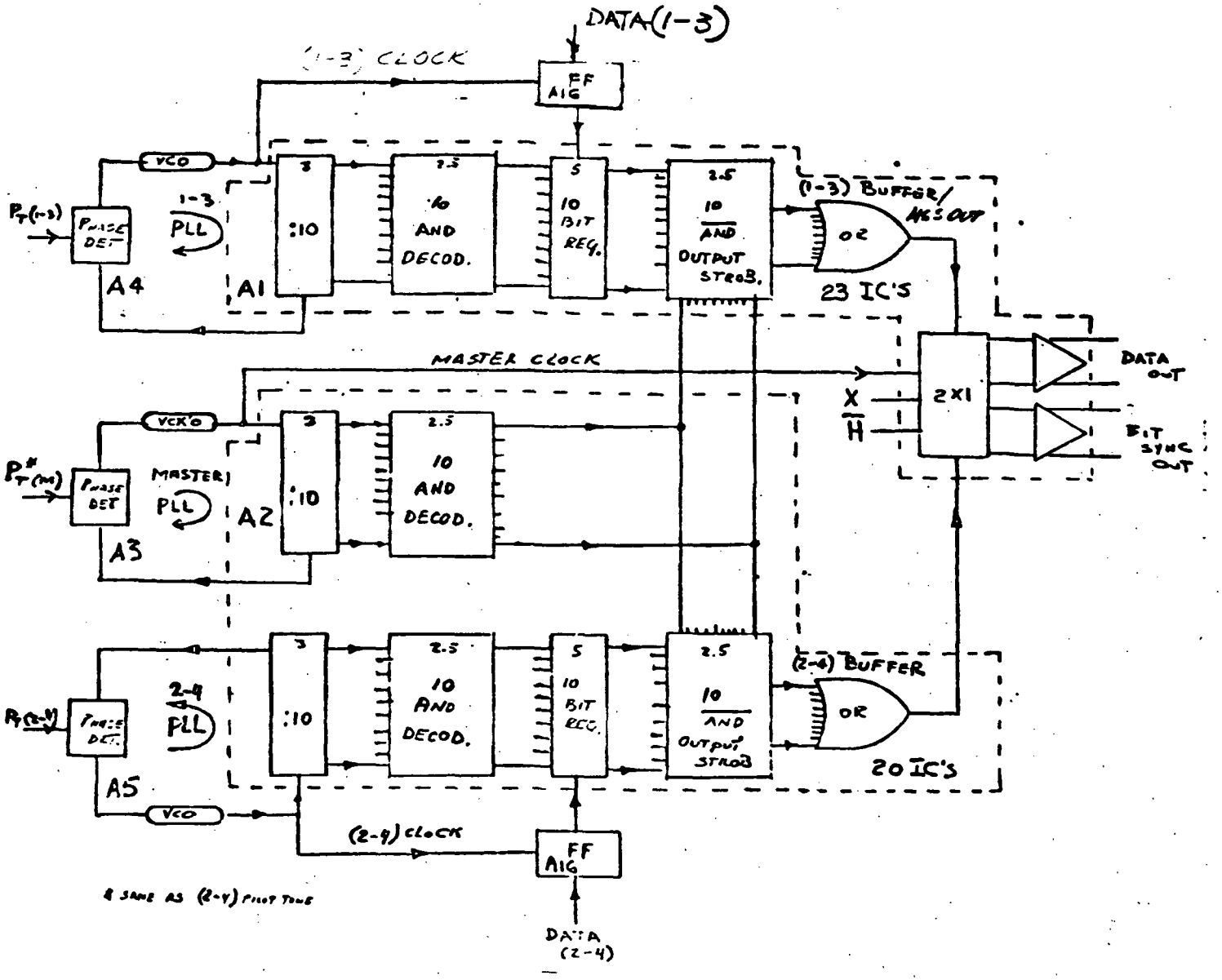


Figure 4-30. MSS System Concept

4.1.3.4 1-3 and 2-4 Buffer Circuits. - The buffers are designed using MTTL integrated circuits. Buffer I (Figure 4-31) processes the 1-3 decoder output and Buffer II (Figure 4-32) processes the 2-4 decoder output.

Basically, the buffer network transfers MSS data sync from the variable clock (VC) to the master clock (MC), and then gates the 1-3 and 2-4 channels into a single output.

As shown in Figure 4-31, the 1-3 variable clock is divided down by a ring counter (U1-U3). The counter outputs clock-in the decoder data, which are then stored in a 10 bit register, flip-flops U8-U12. Master clock signals, generated in Buffer II, shift the stored data out of the register and into OR gates U15-U17. X and H gate signals, which are referenced to the recorder headwheel, are used to gate reclocked channels 1-3 and 2-4 into a single channel. The serial MSS output, along with the master clock signal, feeds balanced input/output line transmitters for distribution to the system.

In general, the operation of Buffers I and II are identical. In addition the Buffer II board contains the master clock ring counter and decoding gates.

Figure 4-33 shows the buffer logic basic timing diagram. For purposes of clarity, all network delays have been neglected.

4.1.3.5 Master Clock. - The master clock is principally a phased locked oscillator and frequency multiplier, the input of which is the 1.5 MHz pilot tone and the output, the 15 MHz master playback clock (bit sync.). A block diagram of the master clock is shown in Figure 4-34 and a complete schematic shown in Figure 4-35.

The composite FM 1-3 signal is applied to the pilot tone extraction filter, which separates the pilot tone from the FM signal, and subsequently to two limiter stages in which amplitude variations due to head to head variations are removed. The 1.5 MHz pilot tone is then applied to the PLO phase detector which generates the error signal used to control the VCXO. The output of the VCXO operating at 15 MHz is applied to a squaring circuit and is then counted down in a divide by 10 synchronous counter in order to achieve the desired frequency multiplication in the PLO. The bit sync signal (master clock playback signal) is taken from the squaring circuit via a high speed gate.

4.1.3.6 Variable Clock. - The variable clock is essentially a phase locked oscillator and frequency multiplier. A block diagram of the variable clock is shown in Figure 4-36 and a complete schematic in Figure 4-37.

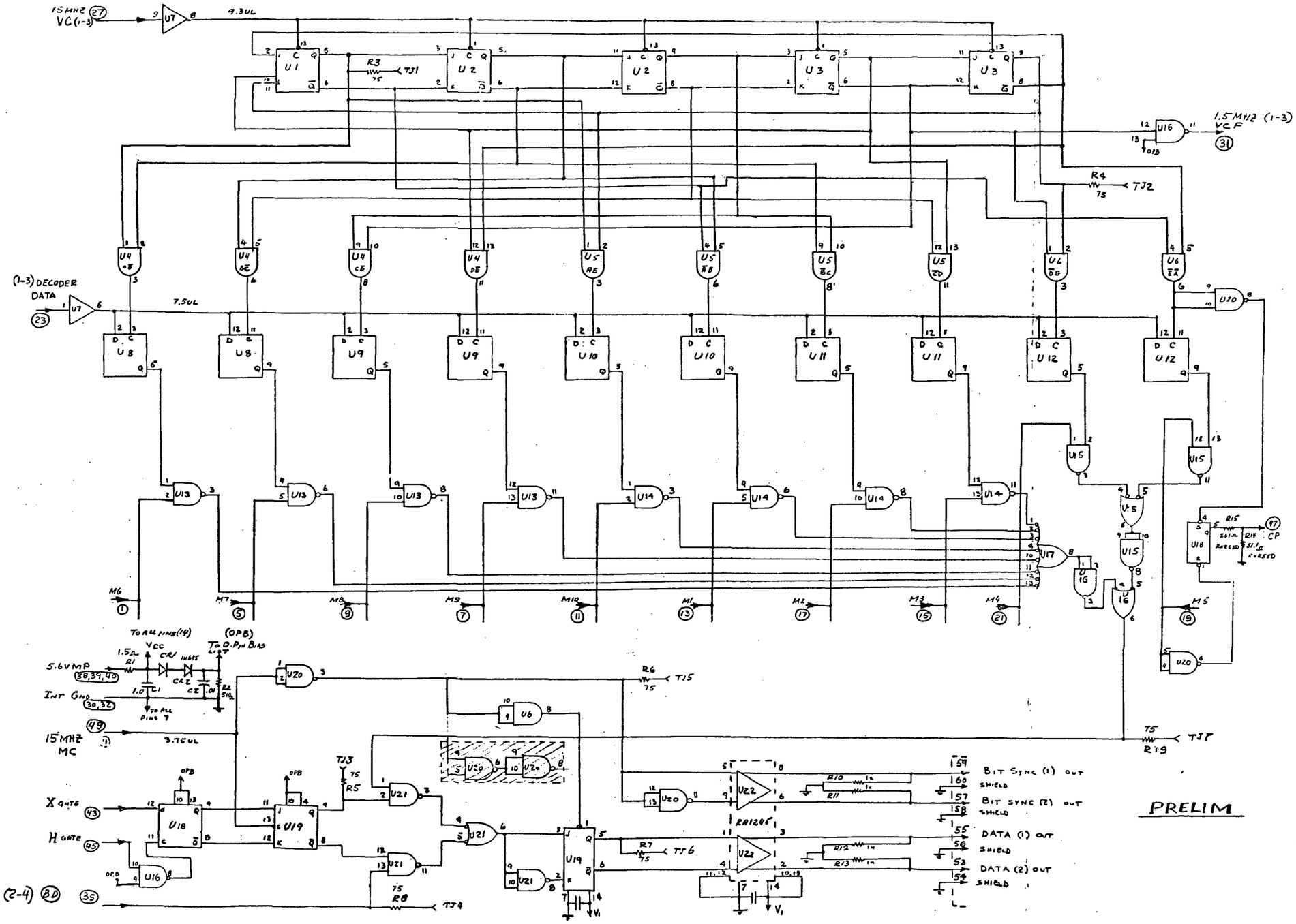
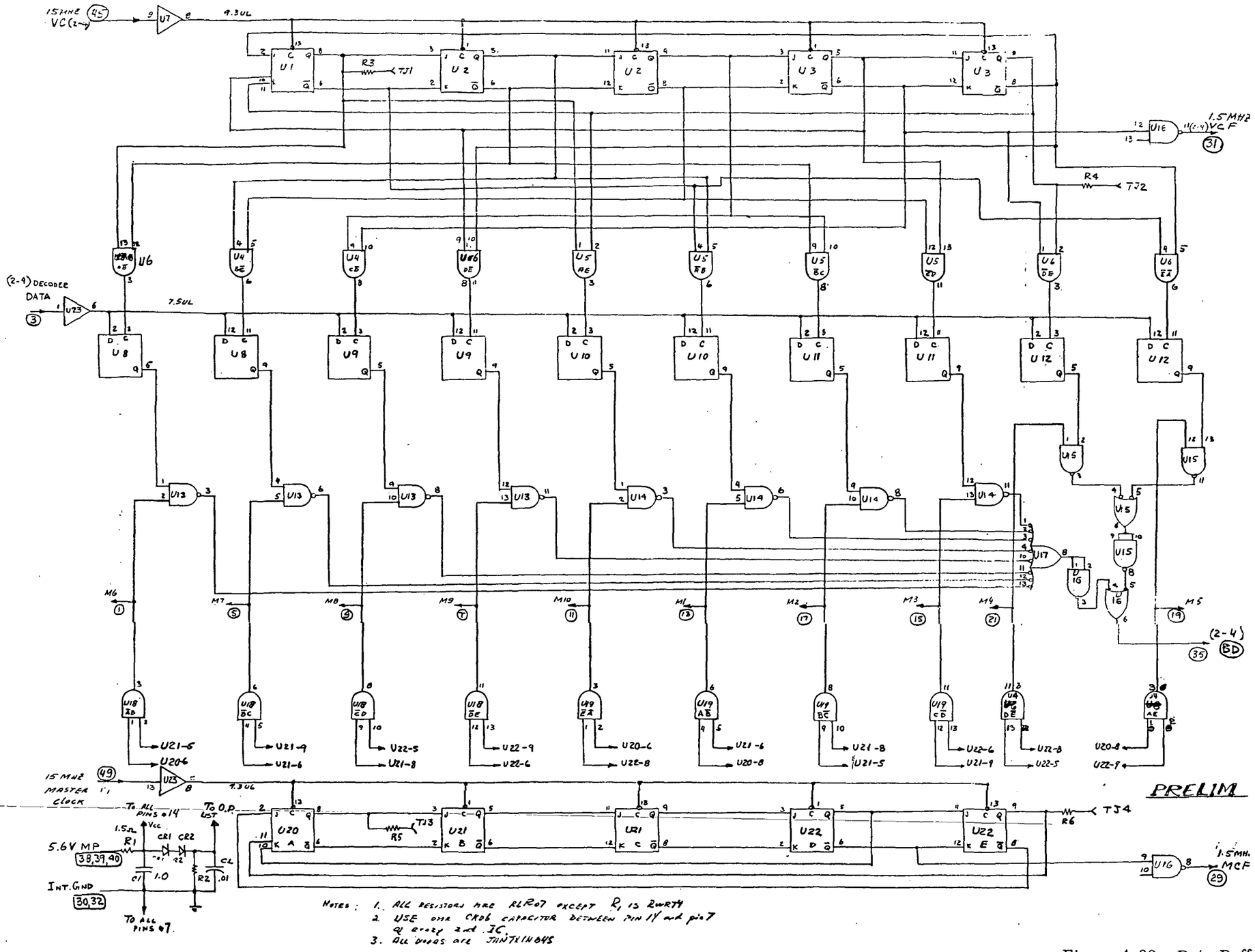


Figure 4-31. Data Buffer I Schematic Diagram



Notes:
1. ALL RESISTORS ARE RLR07 EXCEPT R1 IS 2WRT4
2. USE ONE CK06 CAPACITOR BETWEEN PIN 14 and pin 7 of every 2nd IC.
3. ALL DIODES ARE JAN1N645

Figure 4-32. Data Buffer II Schematic Diagram

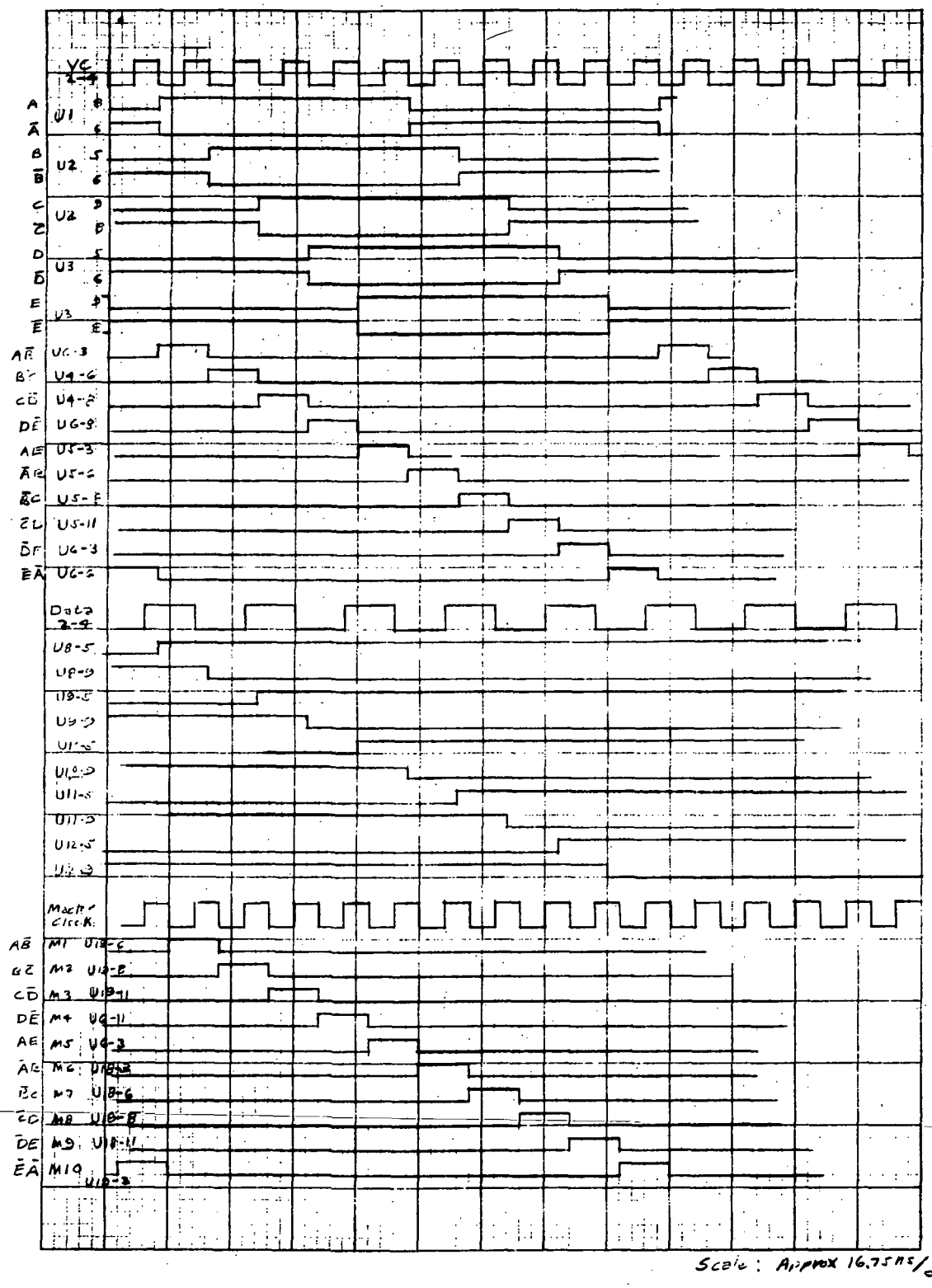


Figure 4-33. MSS Data Buffer Timing Diagram (Sheet 1 of 2)

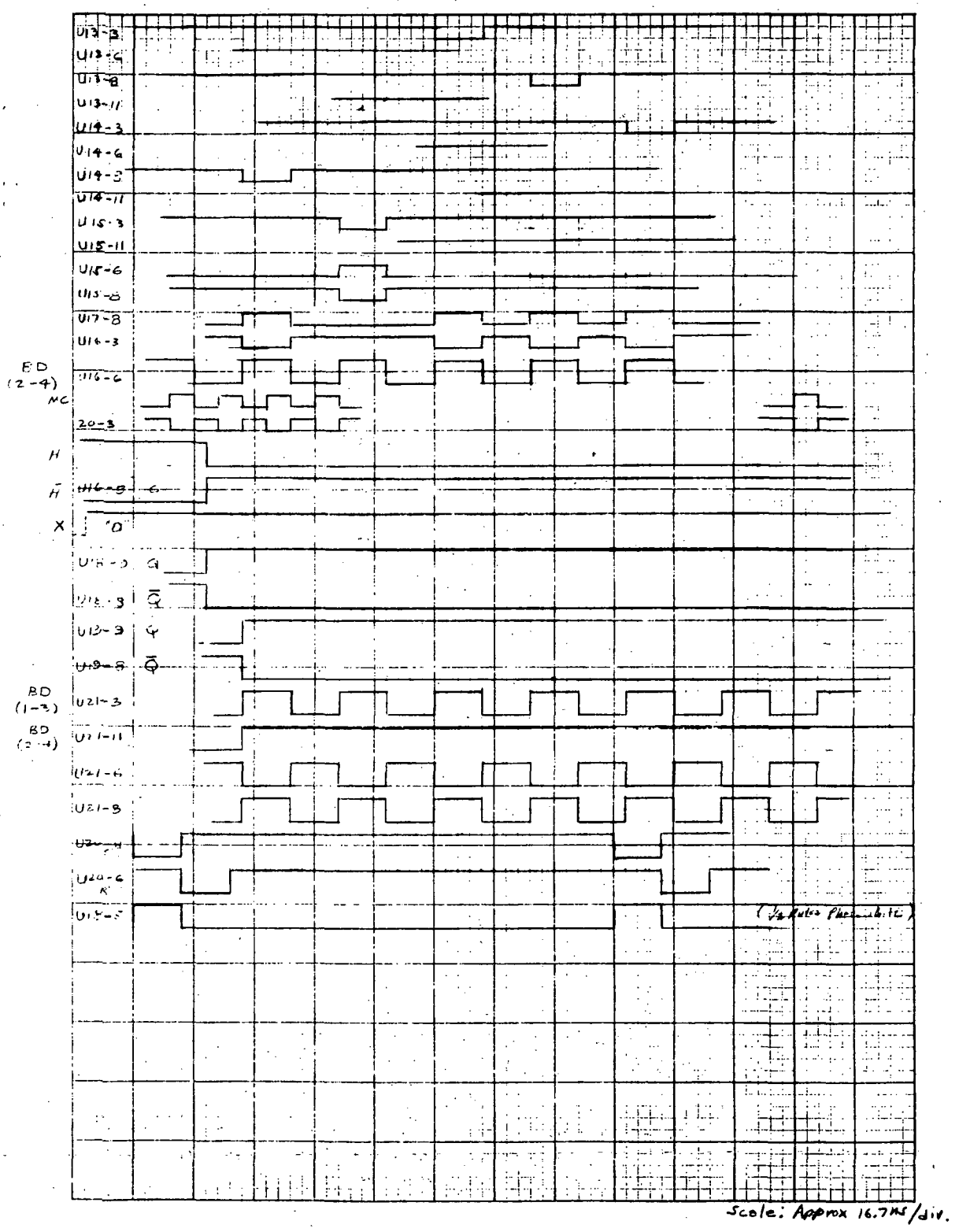


Figure 4-33. MSS Data Buffer Timing Diagram (Sheet 2 of 2)

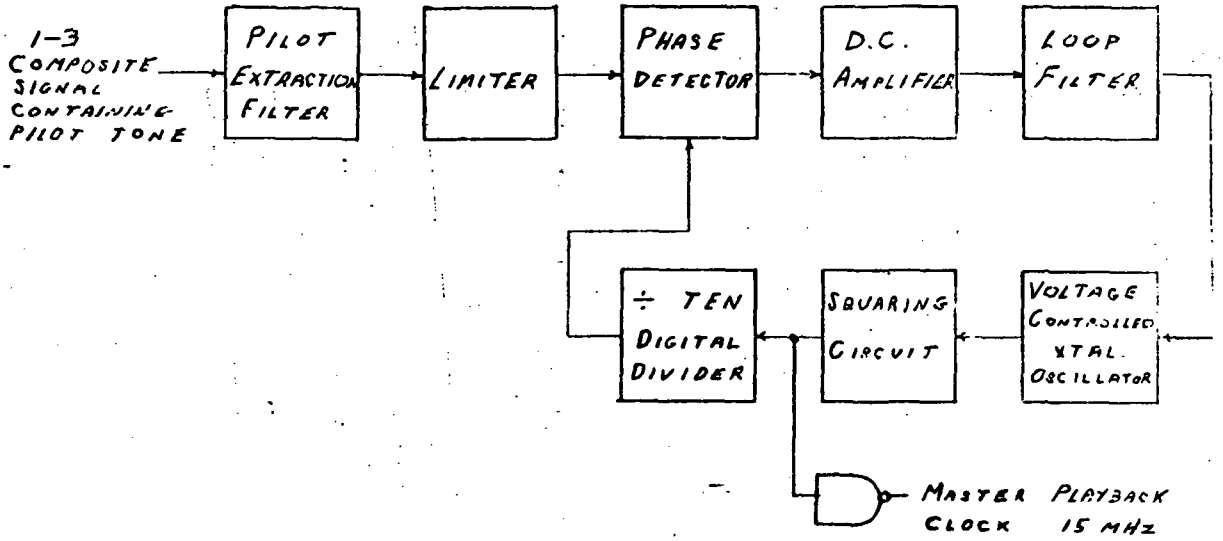


Figure 4-34. Master Clock Block Diagram

The composite FM signal (1-3 or 2-4 pilot tone) is applied to the pilot tone extraction filter, where the pilot tone is separated from the FM signal and subsequently fed to two limiter stages in which amplitude variations are removed. The limiter 1.5 MHz pilot tone is then applied to a phase shifter (discussed with the phase correction loop) and to the phase detector, which compares it to the variable clock output phase (divided by 10) and generates the error signal used to control the VCO frequency. The VCO output at 15 MHz is converted to TTL logic level by a voltage comparator and the variable clock output is taken via a high speed gate.

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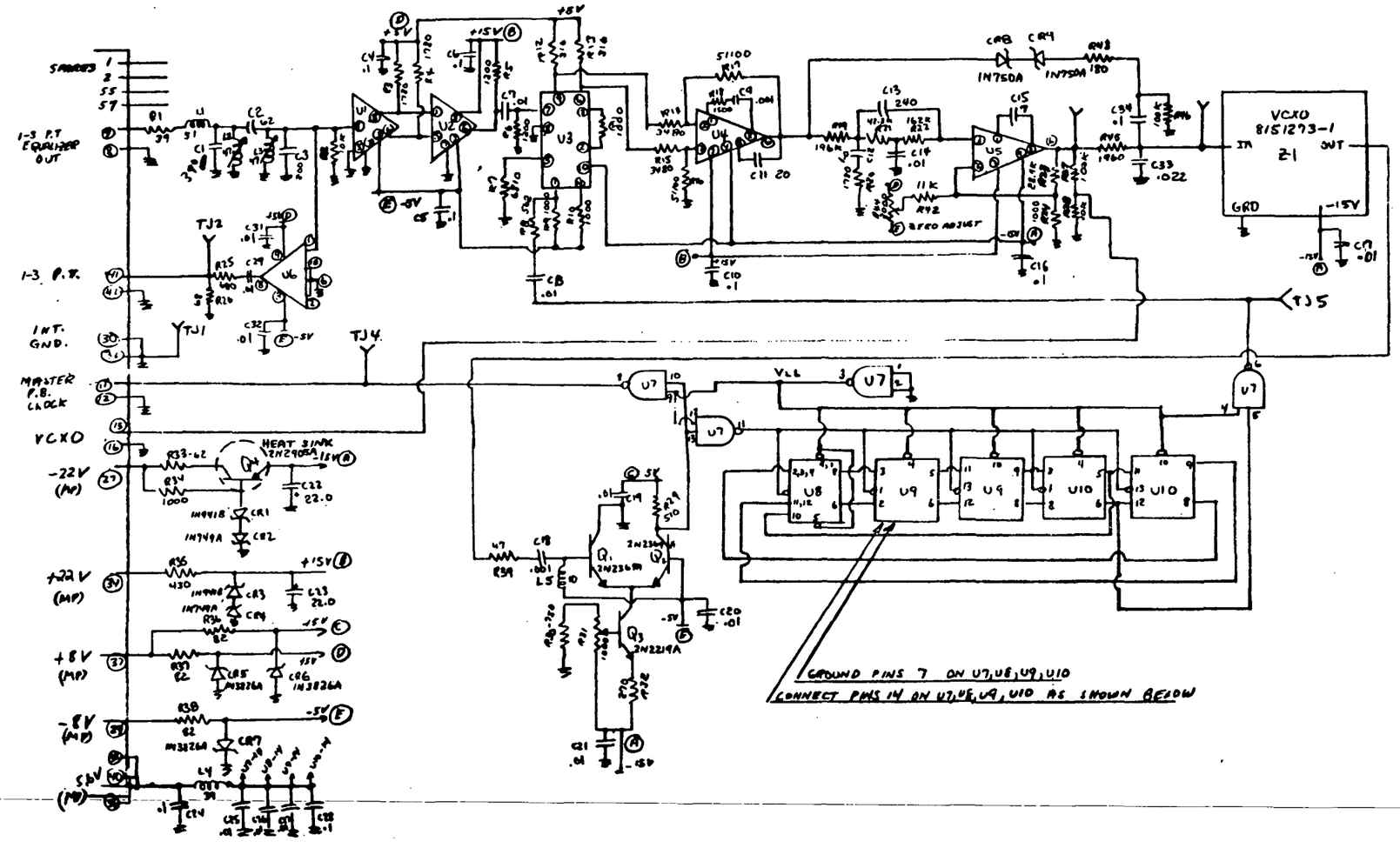

Figure 4-35. Master Clock Schematic Diagram

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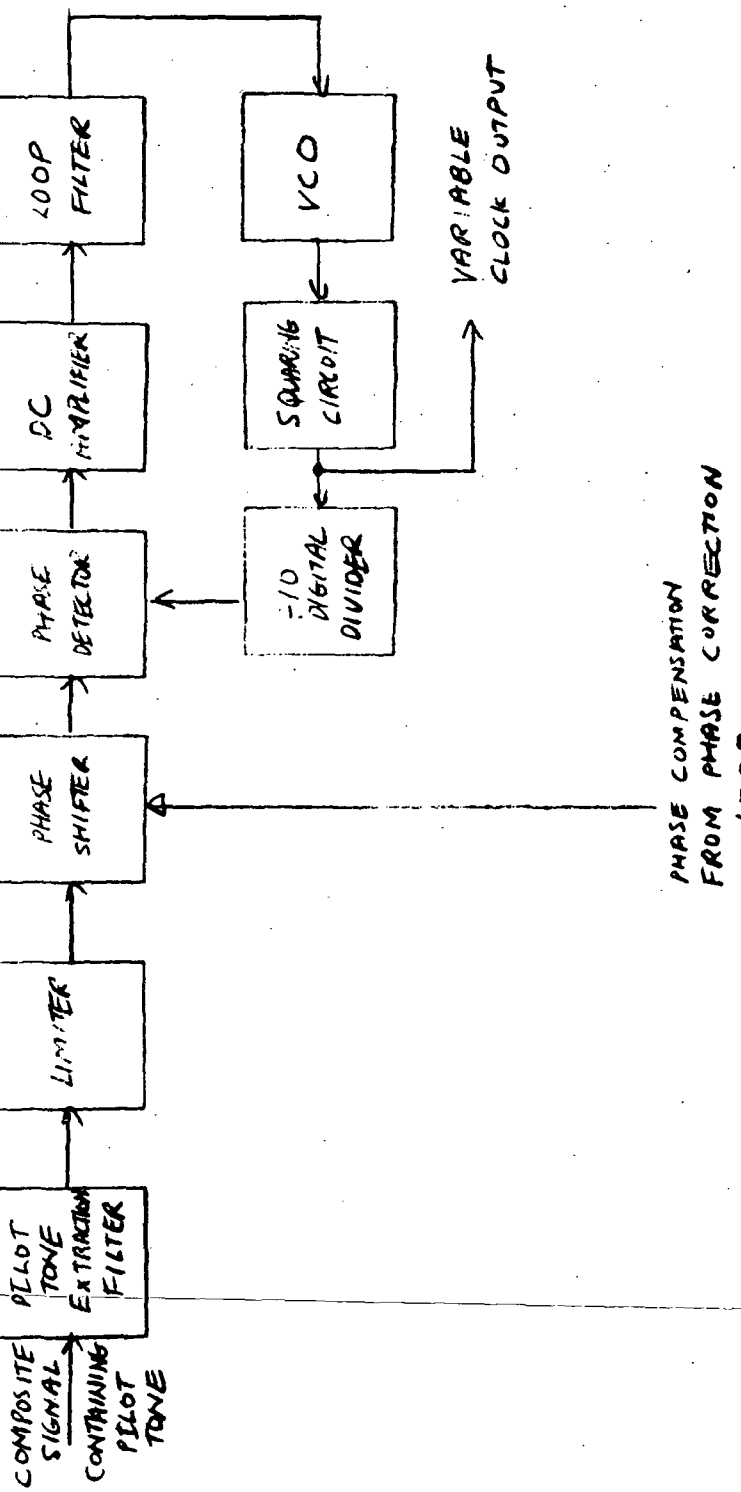

Figure 4-36. Variable Clock Block Diagram

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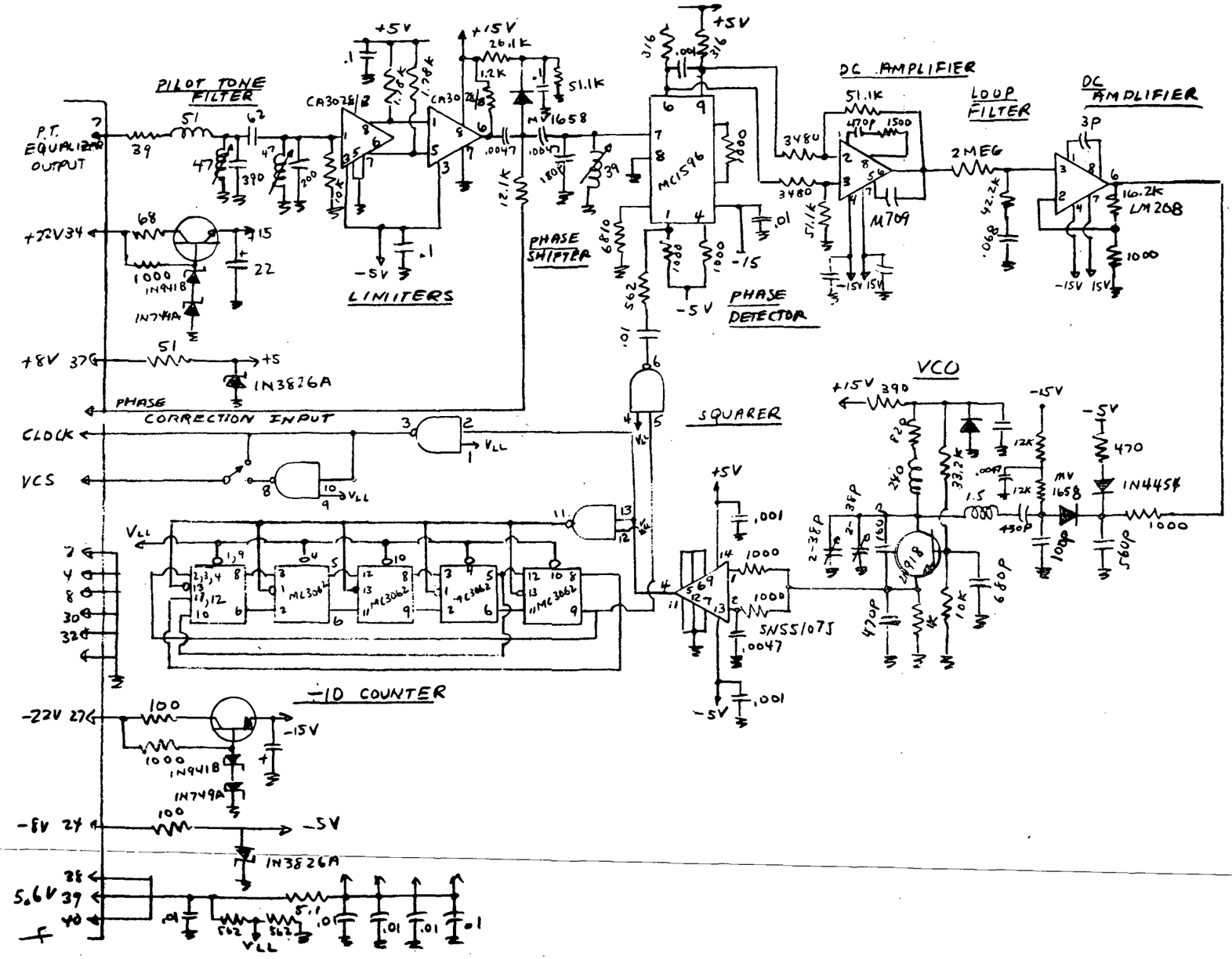

Figure 4-37. Variable Clock Schematic Diagram

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a. Decoder. - The decoder network (Figure 4-25) consists of a lowpass filter, line receiver and reclocking J-K flip-flop.

1. Lowpass Filter. - The lowpass filter has a cut-off frequency of 11.5 MHz and a 75 ohm characteristic impedance. Since the capacitors and inductors used in the design are relatively stable, drift in the filter characteristics will be negligible.

2. Line Receiver (U2). - The line receiver is a differential amplifier with a TTL compatible output level. The maximum differential threshold is 25 mV. Since a single input signal is used, one side of the amplifier is referenced to ground. Therefore, depending on whether the positive or negative input is grounded, any dc offset at the signal input acts as an additional threshold. As a result, since the MSS signal is not a square wave at this point in the processing, a dc offset causes unsymmetrical triggering of the dual input gates. In the event the dc offset exceeds the peak input signal level, one of the gates will remain ON continuously and the other will be OFF. During initial turn-on, there is a possibility of an instantaneous short circuit on the line receiver output due to charging of the frequency doubler capacitors. However, an output short is permitted by the manufacturer's specifications as long as both outputs are not shorted simultaneously.

3. Reclocking Flip-Flop (U3). - The output of the line receiver is reclocked in J-K flip-flop U3. The clock signal is inverted and slightly delayed by TTL gate U1. The flip-flop has no set-up or hold time requirement; therefore, the J-K inputs and the clock pulse transitions may be simultaneous.

4. MSS Test Jack Buffer. - A complementary transistor pair emitter follower has been provided to drive the MSS test line. The emitter currents are:

$$I_{E3} = \frac{V_3 - V_{BE}}{R_{48} + \frac{R_{68}}{2}} \qquad (1)$$

and

$$I_{E4} = \frac{V_3 - V_{BE}}{R_{69} + \frac{R_{68}}{2}} \qquad (2)$$

4.1.4 MSS System Worst Case Analysis

4.1.4.1 Decoder and Variable Clock Phase Correction Loop Worst Case Analysis. - The Decoder and Variable Clock Phase Correction Loop have been analyzed to ensure reliable operation under ERTS system environmental requirements. DC offset effects on the decoder line receiver triggering have been discussed, and maximum delays due to drift have been computed for the phase correction loop.

4.1.4.2.1 Summary. - The reliability of the MSS data decoding depends on the input signal-to-noise ratio and the initial phasing of the reclocking function. Correction loop phase shift is primarily due to the LC circuit characteristics. A summary of the network drift coefficients is given in Table 4-9. As shown, worst case offset is ±6 ns due to temperature and ±12.7 ns due to aging.

TABLE 4-9. PHASE CORRECTION LOOP DRIFT SUMMARY

Parameter		Temperature		Aging	
		% or mV	ns	% or mV	ns
Data Freq. Doubler			+.9, -0.6		±2.5
VC Freq. Doubler			+.28, -1.8		±0.63
Zero Adjust			+1.8, -1.2		±4.2
Phase Detector		±2.2 mV	±0.1	±11.4 mV	±0.5
μ709	dc	±4.2 mV		±6 mV	
	gain	±0.35%		±1.8%	
LM208	dc	±4.5 mV		±1.8%	
	gain	±0.35%		±1.8%	
Differential Phase	gain	±3.2%		±8.8%	
Phase Shifter			±3		±5.5
Cumulative	Offset		±6		±12.7
	Gain	±3.9%		±12.4%	

4.1.4.2.2 Worst Case Analysis. - The decoder network input and output signal and loading requirements were analyzed to ensure reliable operation under worst case conditions. Phase correction loop stability and overall phase drift were determined.

For nominal parameter values, from the above equations $I_{E3} = 13.5$ mA and $I_{E4} = 12.5$ mA. These current levels result in a $V_{CE3} = 4.4V$ and $V_{CE4} = 4.8V$, which are compatible with the MSS signal level. Using the above operating points, the power dissipations are $P_{d3} = 59$ mW and $P_{d4} = 60$ mW.

b. Variable Clock Phase Correction Loop. -

1. Loop Equation. - The phase correction loop equations are derived using the model shown in Figure 4-38. Thus,

$$\psi_a = \frac{\psi_i}{N} + n(t) + K_3 V_3 \quad (1)$$

$$\psi_o = \psi_a H(s) \quad (2)$$

$$V_3 = K_1 K_2 \left(\frac{\psi_i}{M} - \frac{\psi_o}{M} \right) \quad (3)$$

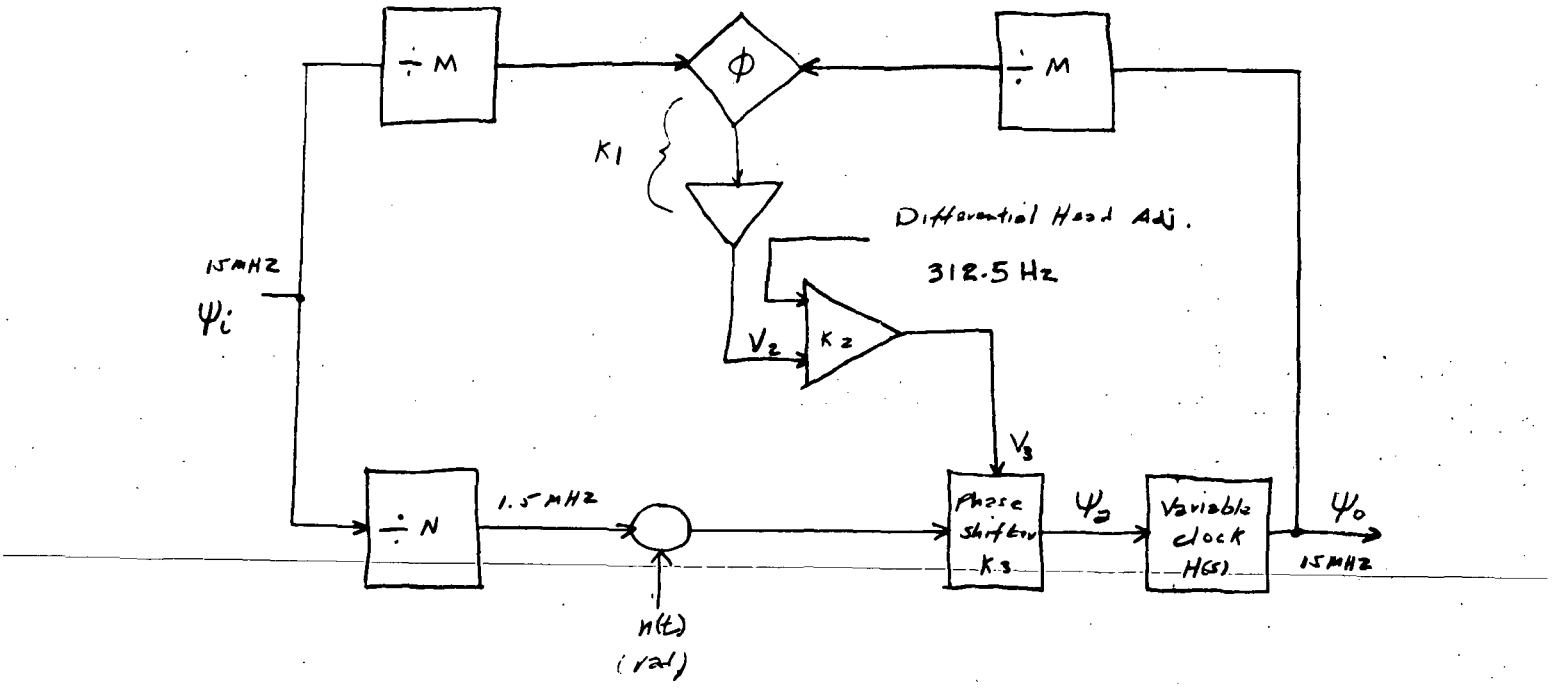

Figure 4-38. Phase Correction Loop System Model

Then combining the above equations:

$$\psi_o = H(s)\left[\frac{\psi_i}{N} + n(t) + K\left(\frac{\psi_i}{M} - \frac{\psi_o}{M}\right)\right] \quad (4)$$

where:

$$K = K_1 K_2 K_3$$

upon further reduction, and solving for phase delay,

$$t_d = t_i \frac{\left(\frac{1}{N} + \frac{K}{M}\right) H(s)}{1 + H(s)\frac{K}{M}} + \frac{t_n}{N} \cdot \frac{H(s)}{1 + H(s)\frac{K}{M}} \quad (5)$$

2. Loop Bandwidth and Gain. - The closed loop bandwidth is determined by the requirement that the differential phase shift signal must be passed to the output unattenuated. The loop gain, H(S)K/M, must be less than 0.1 at 625 Hz* to achieve this, or,

$$H(S)K/M < 0.1$$

Since H(S) = 10 at low frequencies and M = 1, the value of K at 625 Hz is:

$$K < 0.01$$

The dc open loop gain is determined by the accuracy requirements and the expected gain changes. Assume ±15 ns static errors are possible; held to ±1.5 nanosecond. Then from equation 5:

$$\frac{t_d}{t_n} = \frac{1}{N} \cdot \frac{H(S)}{1 + H(S)\frac{K}{M}} \leq 0.1$$

For H(S) = 10 and M = 1, the minimum value of the forward gain K at dc is:

$$K \geq 1$$

*The present phase correction loop open loop gain has been extended so that H(S)K/M<0.1 at 312.5 Hz.

Specifications call for a data transition at least once in every 10 bits. This is equivalent to one excitation every 10 cycles at 15 MHz. A single tuned circuit of quality factor Q has an envelope decay equal to:

$$\frac{E}{E_o} = e^{-\frac{\omega_o t}{2Q}} \qquad (6)$$

For 10 cycles and a Q of 10:

$$\frac{E}{E_o} = e^{-\frac{20\pi}{20}} = 0.045$$

Thus, in order that the loop gain exceed 1 under all conditions, excess loop gain of 26 dB must be built into the loop. Considering further that internal tolerances will effect the gain, the forward gain should be greater than 30 dB for nominal signal levels. Furthermore, the loop should be unconditionally stable so that this range of gain changes can be accommodated.

The open loop response of the phase correction loop satisfying the preceding criteria is shown in Figure 4-39. The single time constant loop results in an excessively high capacitor value. Therefore, the double time constant loop has been implemented with the corner frequencies shown in the figure. The closed loop bandwidth is approximately 30 Hz.

3. Phase Shifter. - The phase shifter circuit is used to: (1) manually phase the variable clock to the clipped data by adjustment of a coil (static phase adjustment), which necessitates a minimum adjustment range of ±34 ns; (2) electronically adjust the phase of the variable clock with a range of ±15 ns by action of the phase correction loop; and (3) superimpose phase variations of ±10 nsec upon the static phase by action of the differential phase compensation circuitry. These requirements will be examined individually.

Static Phase Adjustment. - The required static adjustment range is ±34 ns, which corresponds to a phase shift of $\phi = W_o t_d$ or $\phi = 18.4^\circ = \pm 0.32$ radian. The coil can be adjusted ±10% from its nominal value. If,

$$\tan \phi = -QX \qquad (7)$$

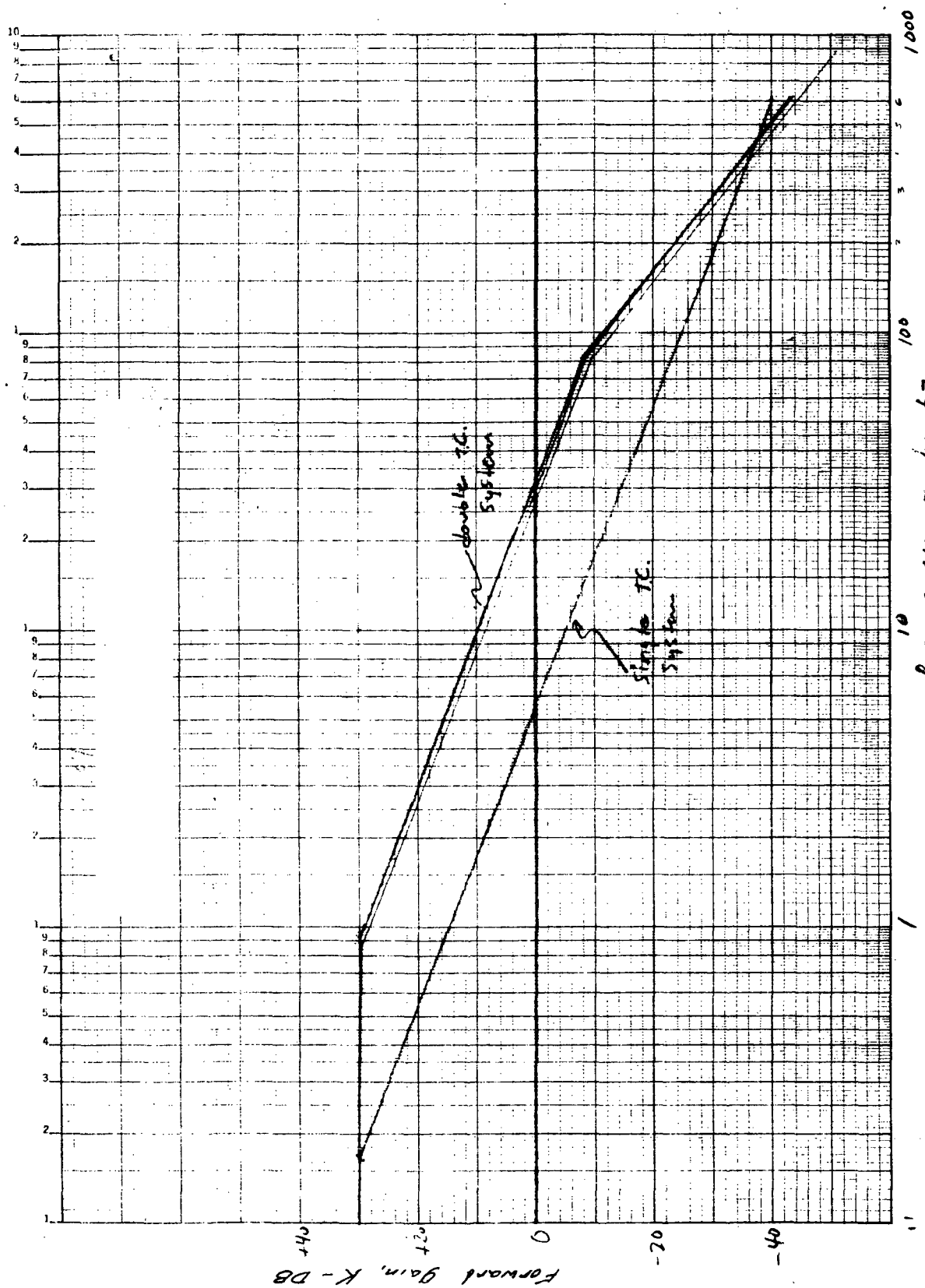

Figure 4-39. Phase Correction Loop, Open Loop Gain

where,

$$X = \frac{\omega}{\omega_o} - \frac{\omega_o}{\omega} = \frac{2\Delta\omega_o}{\omega_o} \tag{8}$$

Then,

$$\frac{\Delta\omega_o}{\omega_o} = -\frac{1}{2}\frac{dL}{L} \tag{9}$$

and, for small dL,

$$\tan\phi = Q\frac{dL}{L} \tag{10}$$

In order to have the required adjustment range:

$$Q \geq \frac{\tan\phi}{\frac{dL}{L}} = 3.3$$

Electronic Phase Control. - Allow a ±3V swing on varactor MV1658, which is biased at -10V (see Figure 4-25) to effect a ±15 ns phase correction. The average capacitance change is 22pF/3V.

$$\frac{\Delta C}{C_T} Q \geq \tan\phi \tag{11}$$

$$C_T = \frac{Q}{\omega_o R} \tag{12}$$

$$\omega_o R \Delta C \geq \tan\phi \tag{13}$$

or

$$R \geq \frac{\tan\phi}{\omega_o \Delta C} \tag{14}$$

and for nominal values,

$$R \geq 680 \text{ ohms}$$

Assuming a ±2V swing on MV1658 biased at -13V (worst case), for a ±10 ns differential head compensation, C = 8pF/2V, and,

$$R \geq 1230 \text{ ohms}$$

Assuming a tank load of 1200 ohm, the coil required for a tank Q of 3.3 is:

$$L = \frac{R}{\omega_o Q} = 39\ \mu H$$

and assuming a diode capacitance of 115pF, the additional tank capacitance is 175pF.

Worst Case Phase Shifter Phase Adjustability. - In order to determine that sufficient range of delay was available for all possible tolerance variations, an ECAP simulation of the phase shifter was run. Coil inductance was varied between 35 and 43 μH. Capacitance diode capacity was varied ±10% and bias voltage ±1V. The curves of Figure 4-40 show that adequate phase variation may be had for any combination of capacitance and inductance in the tank.

Worst Case Phase Shifter Phase Drift. - Assumed variations of tank capacitance and inductance due to voltage, temperature and time variations are tabulated in Table 4-10. The worst case time shift is found from:

$$\Delta t_d = \frac{\Delta \phi}{\omega_o} = \pm 8.5 \text{ ns}$$

4. Loop Zero Adjust. - The loop zero adjust circuit is an LC circuit with a variable inductance. Its function is to compensate for any data-to-VC phase shift caused by loop delays. The range of delay variation is approximately ±15 ns.

The resonant circuit is initially tuned to 7.5 MHz. Temperature and aging drift depends on the inductor and capacitor tolerances and the circuit Q. Using the relationships which were derived for the phase shifter drift analysis, the phase angle in radians is:

$$\Delta \phi = Q \frac{\Delta L}{L} \qquad (15)$$

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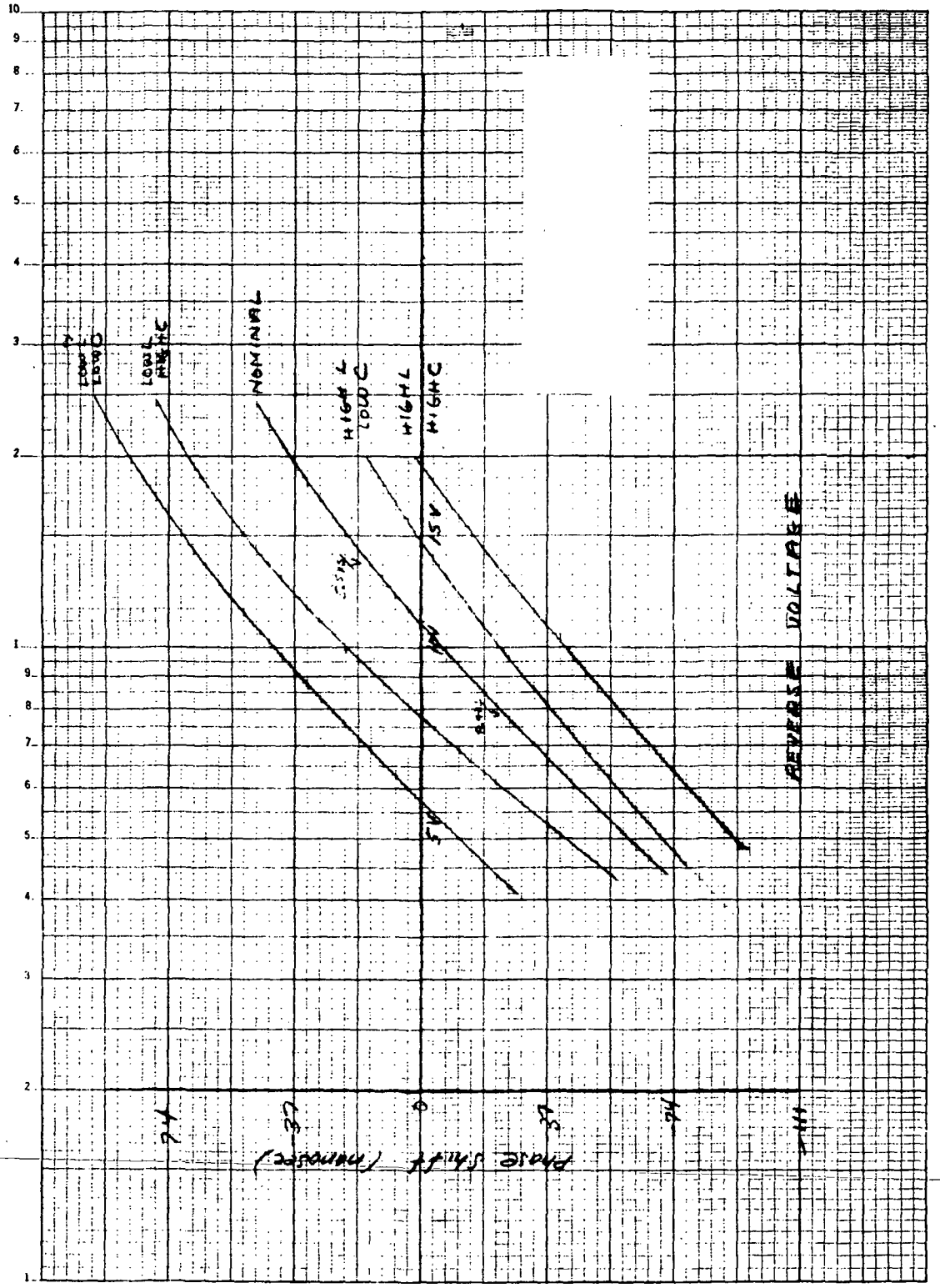

Figure 4-40. Phase Shifter Transfer Characteristic as a Function of Initial Tolerances

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TABLE 4-10. WORST CASE PHASE SHIFTER DRIFT

Parameter	Inductance	Capacitance	$\Delta\phi = Q\frac{dX}{X}$
Bias Voltage	0	±2.6pF ±0.9%	
Time/Temp. 0 - 61° C	±1.5%	±0.78pF ±0.27%	
Total	±1.5%	±1.17%	±0.080 radian

and the delay is:

$$\Delta t_d = \frac{\Delta\phi}{\omega_o} \tag{16}$$

Thus, using a capacitor tolerance of ±0.5% due to aging and -0.07, +0.35% due to temperature, and an inductor tolerance of ±1.5% due to aging and ±0.5% due to temperature, the overall worst case delay drift is +1.8, -1.2 ns due to temperature and ±4.2 ns due to aging.

5. MSS Data Frequency Doubler. - The MSS data frequency doubler is a full wave rectifier feeding an underdamped LC circuit. The LC circuit is tuned to 15 MHz and has a Q of about 10. Network excitation occurs for each data transition, and the minimum rate will be one transition every 667 ns (every 10 data bits). The MSS data resonant circuit envelope damping factor is:

$$t \approx \frac{2Q}{\omega_o} \tag{17}$$

Or, the amplitude decay over a 10 bit sequence will be about 95%.

The delay drift due to temperature and aging may be computed using the relationships which were derived for the phase shifter drift analysis. Thus, using the same component tolerances, the overall worst case delay drift is +0.9, -0.6 ns due to temperature and ±2.5 ns due to aging.

6. VC Frequency Doubler. - The variable clock frequency doubler is a full wave rectifier driving an LC resonant circuit. The LC circuit is tuned to 15 MHz and has a Q of about 3. Using the relationships developed for the phase shifter drift analysis and the same component tolerances, the delay drift is +0.28, -0.18 ns due to temperature and ±0.63 ns due to aging.

7. Phase Detector. - The phase detector is a monolithic circuit consisting of an input differential amplifier driving a pair of synchronized, single-pole, double-throw switches. Since the output is dc coupled, offset drift is critical.

   Output voltage drift due to offset current is 2mV due to temperature. In addition, a differential mode voltage will be developed at the output due to load resistor unbalance. Resistor drift is ±0.9% due to aging and ±0.175% due to temperature. This results in a worst case output voltage differential drift of ±11.4 mV due to aging and ±2.2 mV due to temperature.

   The maximum output voltage change is restricted by the difference circuit constant current source. Since the available current is 2 mA, the maximum output voltage change is:

   $$\Delta V_o = I_L R_L = 620 \text{ mV}$$

   Laboratory tests show that the phase detector output voltage sensitivity is approximately 20-25 mV/ns phase shift.

8. DC Amplifiers. - The output of the phase detector is amplified in operational amplifier U1, integrated, then combined with the differential phase correction in amplifier U2.

   U1 is an integrated circuit operational amplifier connected in the differential mode. The voltage gain is approximately 12 and the variation in gain due to bias resistor drift is ±1.8% due to aging and ±0.35% due to temperature. Input offset voltage drift reflected to the amplifier output is ±4.2 mV due to temperature. Additional output voltage drift due to aging is projected as approximately 6 mV.

   The output of U1 is integrated with a time constant of approximately 300 ms and clamped at the input of U2 to prevent excessive correction. The diode clamping level is shown in Figure 4-41.

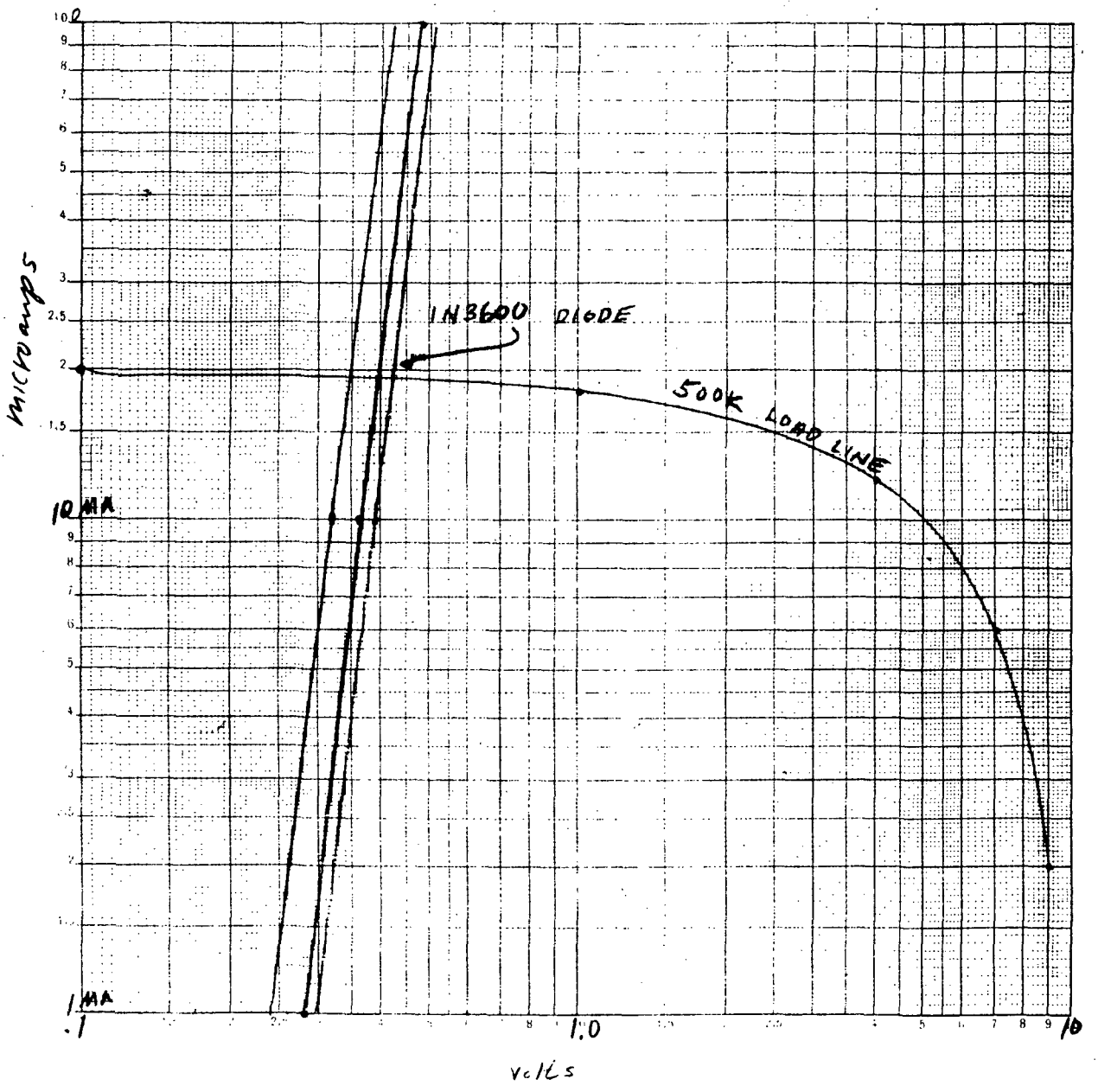


Figure 4-41. Long Term Phase Correction Level Diode Clamp Characteristic

Operational amplifier U2 is used to combine the tonewheel differential phase correction with the long term loop correction error. The amplifier is connected in the differential mode with a non-inverting input voltage gain of 10. Offset voltage drift reflected to the amplifier output is ±4.5 mV due to temperature and is projected as ±3 mV due to aging. Voltage gain drift due to bias resistor variation is ±1.8% due to aging and ±0.35% due to temperature. Since the tonewheel differential phase correction signal is ac coupled, the square wave trailing edge will have about a 2% drop with respect to the leading edge.

U2 output sensitivity is approximately 150 mV/ns phase correction.

9. Differential Phase Control. - The differential phase control circuit is an emitter coupled differential amplifier with one input referenced to approximately +2.3V. The signal input is diode coupled to the C gate for heads 2-4 and to the D gate for heads 1-3, which are referenced to the tonewheel speed. An adjustment potentiometer is connected between the balanced outputs in order that both the desired amplitude and proper phase correction may be selected for the specific head combination (1-3 or 2-4). Based on a constant current source of 2 mA, the maximum output signal change is 3.75 Vpp. For an amplifier gain of 1.5 (inverting input of U2), the phase shifter input level is 5.6V, resulting in an available phase correction range of ±28 ns.

   Possible sources of differential phase correction drift are variations in the internal constant current source, the input reference bias, adjustment potentiometer, and load resistors. Since the output level is ac coupled, the input reference bias drift may be neglected. The potentiometer output level drift is ±4% due to aging and ±0.8% due to temperature. Level drift due to load resistor drift is slightly less than ±1.8% due to aging and ±0.35% due to temperature. Constant current drift depends primarily on the internal emitter resistance variation, which may be assumed to drift approximately ±2% due to temperature and ±3% due to aging.

10. Cumulative Phase Drift. - A summary of the phase correction loop temperature and aging drifts is shown in Table 4-12. The cumulative worst case offset drift is ±6 ns due to temperature and ±12.7 ns due to aging. Signal level variation as a result of gain changes is approximately ±3.9% due to temperature and ±12.4% due to aging.

c. Voltage Regulators. - Analysis of the +5A, -5A, -5, and -15 Volt power supplies is given in paragraph 4.1.4.6, the "Master Clock, Variable Clock and Decoder Power Supply Regulator Worst Case Design". The +5V supply, which is used to supply the digital logic circuits, is decoupled from the +5.6V supply through an RLC network. The typical load current is 108 mA and the maximum is 176 mA. These currents result in a voltage drop with respect to the 5.6V supply of 0.5V and 0.86V, respectively.

4.1.4.2.3 Conclusions and Recommendations. - Worst case analysis of the MSS data decoder and variable clock phase correction loop has shown that both circuits should operate reliably over the ERTS system requirements. However, since the phase correction loop requires a number of phase adjustments, a systematic alignment procedure should be adhered to when initially setting-up the loop. Otherwise, it is possible to operate near the non-linear region and subsequently drift into saturation.

In order to conserve power, it may be desirable to review the MSS data test point requirements. The complementary pair emitter follower buffer (Q3 and Q4) uses about 400 mW.

4.1.4.3 MSS Data Buffer Worst Case Analysis. - MSS Data Buffer I and II have been analyzed to ensure reliable operation under worst case logic circuit variations. Gate loading was tabulated and critical accumulated propagation delays were determined.

4.1.4.3.1 Design Considerations. - Worst case accumulative propagation delays must be taken into account for all clocking functions. Logic gate output loading and fan-in requirements should be met, and manufacturer's recommendations for biasing unused inputs followed. Worst case power supply decoupling network voltage drops should not restrict logic gate minimum power supply requirements.

4.1.4.3.2 Summary. - Minimum data input setup and hold time requirements are within the logic circuit operating specifications, and gate output loading restrictions have been met. The worst case dc supply load is 418 mA typical, 692 mA maximum for Buffer I, and 342 mA typical, 640 mA maximum for Buffer II. The resulting gate supply voltage range under the above loading conditions is 4.2 to 5.4V for Buffer I and 4.2V to 5.5V for Buffer II.

4.1.4.3.3 Worst Case Analysis. - The Buffer Logic has been analyzed to determine clocking reliability and maximum gate input and output loading. Two boards have been used for the buffer network: Buffer I processes the 1-3 channel and contains the logic for multiplexing the two buffer outputs; Buffer II processes channel 2-4 and contains the master clock reference counter.

TO BE REVISED

Buffer II has been analyzed first since the master clock gating levels, required for the operation of both buffers, are generated on that board.

a. Buffer II (2-4). - For purposes of analysis, Buffer II has been broken down into the variable clock counter, storage register, master clock counter and logic gate loading requirements.

1. Variable Clock Counter. - The variable clock counter (U1-U3) is a recirculating shift register (ring counter) that inverts the data as it is recirculated from the low order to the high order stage. Five JK flip-flops are used in the counter, resulting in a 1.5 MHz, or divide by ten output. Since only one bit changes with each clock pulse, the possibility of false or transitional counts are eliminated.

   The counter outputs are decoded by AND gates U4-U6 to provide ten sequential clock pulses, 1 bit in duration, at a 1.5 MHz rate. These clock pulses are used to clock the decoder data into the buffer storage register.

2. Storage Register. - The decoder data is stored in a 10 bit register, U8 to U12. D type flip-flops connected in the clocked mode of operation are used in the register. When operated in the clocked mode, the flip-flop will assume the state present on its D input with application of the leading edge of the clock pulse. In general, to insure reliable clocking, the D input is required to be present for some specified minimum setup and hold time.

   Figure 4-42 shows the storage register clocking timing relationships for the 1-3 decoder data input. The dashed extensions indicate maximum accumulative propagation delays. In order to provide a sufficient clocking safety margin, the variable clock triggering the buffer registers is 180° out of phase with the decoder sync. As shown in the figure, the decoder data at the D inputs precede the clock pulse (in this case the U4-3 output, AB) by a minimum setup time of 33 ns and a hold time of 13 ns under worst case conditions. This may be compared to the maximum specified setup and hold times of 10 and 5 ns, respectively.

3. Master Clock Counter. - The master clock counter is identical to the variable clock counter except that it is triggered by the master clock. The five stages used are flip-flops U20-U22.

4. MSS Data (2-4). - The channel (2-4) reclocked MSS Data is combined in gates U15 to U17. Eight bits feed OR gate U17 and two bits feed pins 4 and 5 of OR gate U15. The outputs of these gates are inverted and further combined in gates U16 to provide the 2-4 MSS Data.

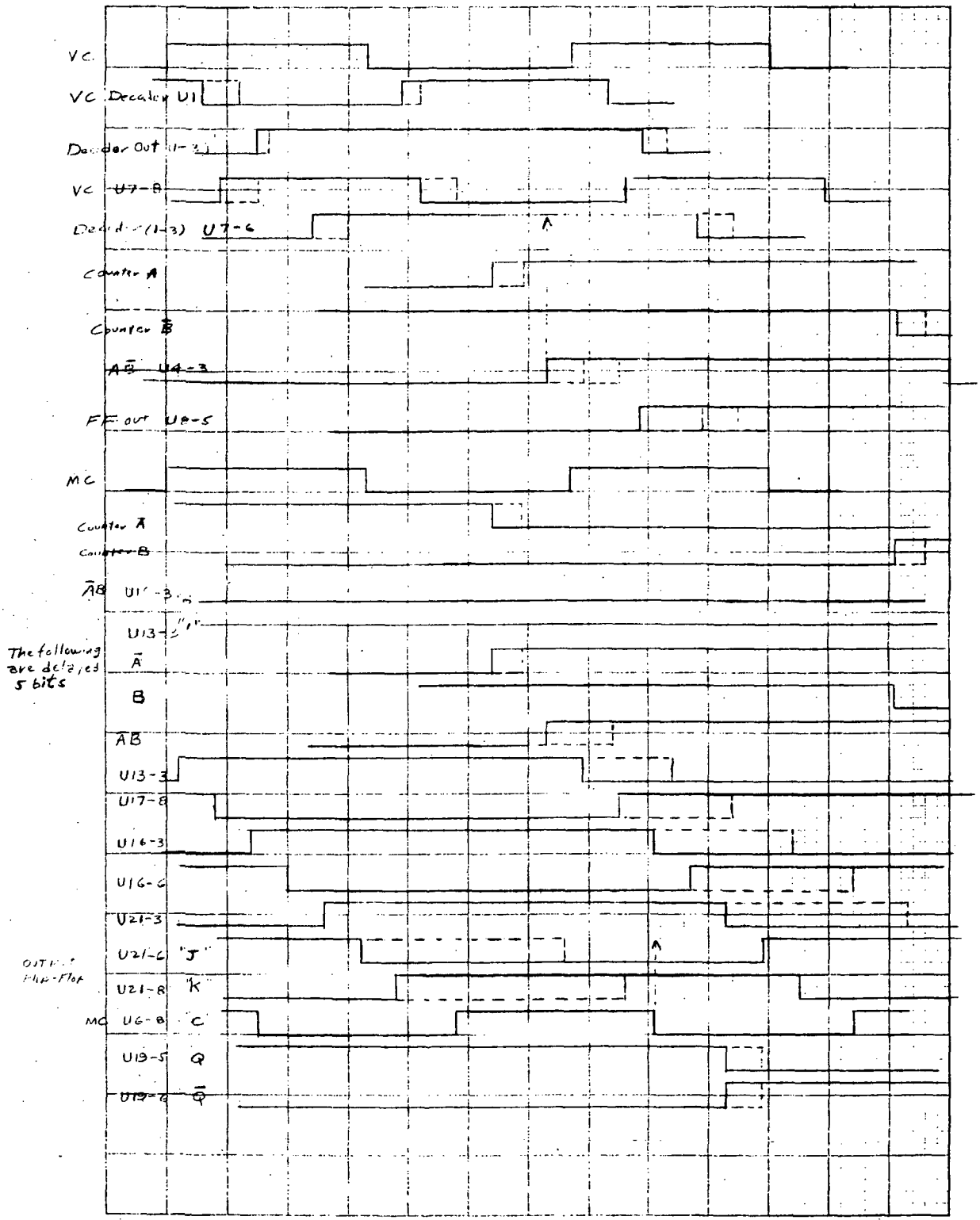


Figure 4-42. Decoder Data Storage Register and Output FF Clocking

5. Gate Output Loading. - Logic gate output loads have been tabulated in Table 4-11 for comparison with the maximum allowable Unit Loads (UL) specification for each element. Since both buffers are similar, only those gates unique to Buffer II are shown in the table. Loading for the gates performing identical functions in both buffers is shown in Table 4-12, the tabulation of Buffer I gate loading. As shown in the tables, all gates are loaded below the maximum allowable of 60%.

6. Unused Inputs. - In order to minimize the effects of external noise, the integrated circuit manufacture recommends that the unused inputs of any MTTL logic circuit should not be left open, but should either be tied to the used inputs or returned to a voltage between 2.0 and 5.5 Vdc. The above requirements have been fulfilled for the buffer logic by tying all unused inputs to a dc bias tapped-off the 5.6 Vdc supply. This bias level range is 2.8 to 4 Vdc at approximately 5 mA of current.

7. Power Supply Loading. - The logic gate power supply current requirements for Buffer II are summarized in Table 4-13. Total load current is 342 mA typical and 640 mA maximum. The typical gate voltage resulting from the voltage drop due to the decoupling network is 5.1V. The minimum voltage under worst case loading conditions is 4.2V and the maximum is 5.5V.

b. Buffer I (1-3). - The 1-3 buffer variable clock counter, storage register and output gates are identical to the 2-4 buffer. The master clock reference is derived from the 2-4 buffer board. Additional functions on the Buffer I board are the channel 1-3 plus 2-4 gating, MSS output reclocking, and data transmitters. A VC/MC phase monitor is also provided.

TABLE 4-11. BUFFER II GATE LOADING

Output No.	Type	Load		Load		Max Allow. UL	Total UL
		Type	UL	Type	UL		
U23-8	MC3126	3151-C	1 x 2.3	3162-C	4 x 1.75	20	9.3
U18-3,6,8,11	MC3101	3100	2 x 1			10	2
U19-3,8,11	MC3101	3100	2 x 1			10	2
U6-11	MC3101	3100	2 x 1			10	2
U16-8	MC3100	TTL	1			10	1

TABLE 4-12. BUFFER I GATE LOADING

Output No.	Type	Load		Load		Max Allow. UL	Total UL
		Type	UL	Type	UL		
U1-6,8	MC3151	3162-K	1x.75	3151-K	2 x .75	10	2.25
U2-5,6,8,9	MC3162	3162-K	1x.75	3151-K	2 x .75	10	2.25
U3-5,9	MC3162	3162-K	1x.75	3151-K	2 x .75	10	2.25
U3-6,8	MC3162	3162-K	1x.75	3151-K	2 x .75	10	2.25
U4-3,6,8,11	MC3101	3160-C	1x1.5			10	1.5
U5-3,6,8,11	MC3101	3160-C	1x1.5			10	1.5
U6-3	MC3101	3160-C	1x1.5			10	1.5
U6-6	MC3101	3160-C	1x1.5	3100	2 x 1	10	3.5
U8-U12	MC3160	3100	1x1			10	1
U13-U14	MC3100	3115	1x1			10	1
U15-3,11	MC3100	3100	1x1			10	1
U15-6	MC3100	3100	2x1			10	2
U15-8,U16-3 U16-6	MC3100	3100	1x1			10	1
U17-8	MC3115	3100	2x1			10	2
U7-8	MC3126	3151-C	1x2.3	3162-C	4 x 1.75	20	9.3
U7-6	MC3126	3160-D	10x.75			20	7.5
U16-8	MC3126	3160-C	1x1.5			20	1.5
U18-8,9	MC3160	3162-J	1x.75			10	.75
U19,8,9	MC3162	3100	1x1			10	1
U21-3,11	MC3100	3100	1x1			10	1
U21-6	MC3100	3162-J	1x.75	3100	2 x .75	10	2.25
U21-8	MC3100	3162-K	1x.75			10	.75
U20-6,8	MC3100	3160-S	1x1.15			10	1.15
U20-11	MC3100	1245	1x 1.25 UL 2.5 mA			10	1.25

TABLE 4-12. BUFFER I GATE LOADING (Continued)

Output No.	Type	Load		Load		Max Allow. UL	Total UL
		Type	UL	Type	UL		
U19-5, 6	3162	1245	1 x 1.25 / 2.5 mA			10	1.25
U20-3	3100	1245	1 x 1.25 / 2.5 mA	3100	2 x .75	10	1.25
U18-5	3160	310	10 mA (5UL)			10	5

TABLE 4-13. BUFFER II POWER SUPPLY LOAD

TTL Gate Type	Supply Current (mA)		Circuit Number	Total Current (mA)	
	Typical	Max		Typical	Max
MC3151	10	15	U1, U20	20	30
MC3162	20	29	U2, U3, U21, U22	80	116
MC3160	24	29	U8, U9, U10, U11, U12	120	145
MC3100	17.6	H-36	U13, U14, U15, U16	70	144
MC3101	22.5	H-24	U4, U5, U6, U18, U19	112	120
MC3115	4	H-9	U17	4	9
MC3126	18	L-38	U7, U23	36	76
Total				342	640

1. MSS Data Gating. - The two buffer outputs (1-3 and 2-4) are gated together by the X and H gate signals, which are referenced to the recorder headwheel. The timing sequence for the gating operation is shown in Figure 4-43. Since there is considerable delay (60 us) between the D input transition and the clock pulse of U18, the setup and hold timing requirements, which are in the ns range, have been met. Resyncing the gating levels to the master clock is accomplished in U19.

2. Data Output. - The MSS data is reclocked in JK flip-flop U19, then it feeds a differential input line transmitter.

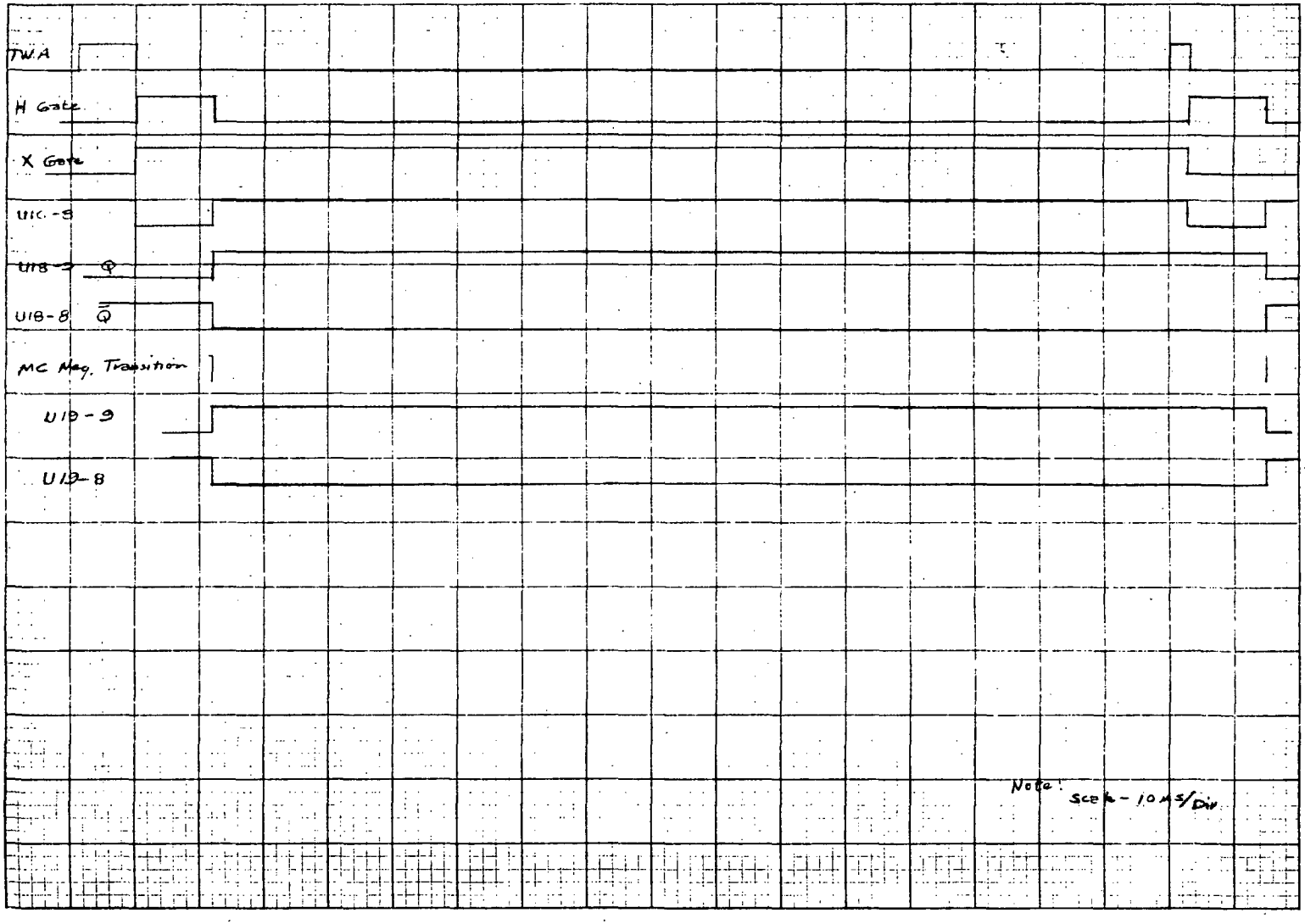


Figure 4-43. Buffer Output Gating, 1-3 plus 2-4

Reclocking. - The output flip-flop reclocking timing relationships are shown in the lower half of Figure 4-42. Triggering is accomplished at the master clock negative going transition and an 8 ns setup time is required. As shown in the figure, the worst case setup times are 15 ns for the "J" input and 5 ns for the "K" input.

Line Transmitter. - The line transmitter is an emitter coupled differential amplifier with a balanced output. The typical available "on" current at 25° C is 4.5 mA and the maximum is 5.2 mA. Off current is a maximum of 100 uA. When driving a 50 ohm load, the nominal output signal level is 225 mVpp.

3. Clock Phase Monitor. - Outputs of the VC and MC ring counters are used to trigger the set and reset inputs of flip-flop U18. The resulting output pulse width is proportional to the difference in phase between the two clocks.

4. Gate Output Loading. - Logic gate output loads for Buffer I have been tabulated in Table 4-12. As may be seen from this tabulation, all gates are loaded at less than the maximum allowable of 60%.

5. Unused Input Bias. - As was the case for Buffer II, all unused inputs have been tied to a dc bias or an active input to minimize the effects of external noise.

6. Power Supply Loading. - The logic gate power supply current requirements for Buffer I are summarized in Table 4-14. The total load current is 418 mA typical and 692 mA maximum. The typical gate voltage resulting from the voltage drop due to the decoupling network is 5V. The minimum supply voltage under worst case loading conditions is 4.2V and the maximum is 5.4V.

4.1.4.3.4 Conclusions and Recommendations. - Worst case analysis of the Buffer Network has shown that reliable operation should be maintained throughout system operating requirements. Clock phasing is adequate to accommodate data maximum accumulative propagation delays. Logic gate fan-in and output loading restrictions have been satisfied. Switching transient suppression has been provided by distributing 0.01 uF capacitors from the power supply to ground throughout the printed circuit board.

Although all unused inputs appear to have been accounted for, all IC pin functions should be verified in the final printed board layout.

TABLE 4-14. BUFFER I POWER SUPPLY LOAD

TTL Gate Type	Supply Current (mA)		Number	Total Current (mA)	
	Typical	Max		Typical	Max
MC3151	10	I_{max}/I_{pd} 21/15	U1	10	15
MC3162	20	41/29	U2, U3, U19	60	87
MC3160	24	42/29	U8, U9, U10, U11, U12, U18	144	172
MC3100	17.6	25/H-36 L-17.5	U13, U14, U15, U16, U20, U21	105	215
MC3101	22.5	34/H-24 L-48	U4, U5, U6	67	144
MC3115	4	6.5/H-9 L-4.25	U17	4	9
MC3126	18	L-38	U7	18	38
RA1245	5	6	U22/2	10	12
Total				418	692

Under worst case supply current requirements and a low converter voltage, the logic power supply voltage will fall below the recommended minimum of 4.5V. Therefore, if laboratory tests result is an average buffer operating current approaching the worst case maximum, the power supply decoupling network should be adjusted to be compatible with the full load converter output voltage.

It should be noted that distortion will be introduced into the line transmitter output transition due to any phase delay between the complementary inputs and also the difference in the line transmitter switching delays. The result of this distortion is a shortening of the output difference current pulse width during alternate "1's" and "0's".

4.1.4.4 Master Clock Worst Case Analysis. - The master clock input is the 1.5 MHz pilot tone recorded simultaneously with the MSS data; the output is the 15.0 MHz master clock playback signal used subsequently to read out the MSS Buffer and to be transmitted as the bit sync. The purpose of the master clock is to generate this signal so that its average frequency is exactly ten times the pilot tone frequency, with a spectral purity meeting design specifications.

The design of the master clock assures that the output conforms to the following specifications for the environmental conditions listed in the worst case analysis criteria:

1. Output frequency - 15.0 MHz.

1.1 Output Long term stability - Sum of MSS clock and spacecraft clock.

1.2 Output Medium term stability - equal to extracted pilot tone.

1.3 Output Medium term accuracy - less than 60 ns (pp) phase error with respect to pilot tone up to 10 Hz, for pilot tone time base instability of ±2.5 us.

1.4 Short term stability - less than 20 ns (pp) jitter for shoe errors less than 100 ns for all spectral components above 100 Hz.

2.0 Output format - square wave.

2.1 Output asymmetry - ±3.5 ns.

3. Output loading - TTL compatible; 10 unit loads.

Implicit in these specifications is that the master clock be frequency locked to the pilot tone under all conditions.

4.1.4.4.1 Design Criteria. -

a. Introduction. - The basic PLO is synthesized as a second order feedback loop employing a compensated lag network to obtain independent control of bandwidth and low frequency gain. The design is constrained by: (1) the necessity for a minimum velocity constant to achieve the required timing accuracy at low frequencies; and (2) the necessity to sharply attenuate shoe error components in the pilot tone at 1250 Hz.

In order to achieve the best possible performance and still meet servo stability and frequency lock requirements, the basic loop has been enhanced with a bridged tee filter at 1250 Hz to suppress the shoe error components, and nonlinear acquisition circuitry to increase the pull-in range to the maximum permitted by the oscillator. A voltage controlled crystal oscillator was found necessary to meet the frequency lock requirements.

b. Low Frequency Phase Accuracy. -

1. Description. - The extracted pilot tone contains a low frequency flutter component with peak timing errors of ±2.5 us. The master clock playback signal must track the input phase to within an accuracy of 60 ns (pp) for all frequencies up to 10 Hz.

2. Analysis. - The pilot tone with low frequency timing error can be represented by

$$f(t) = E \sin (\omega pt + T_f \omega p \sin \omega_f t) \qquad (1)$$

where

T_f is the peak timing error

ω_f is the flutter frequency

ω_p is the pilot tone frequency.

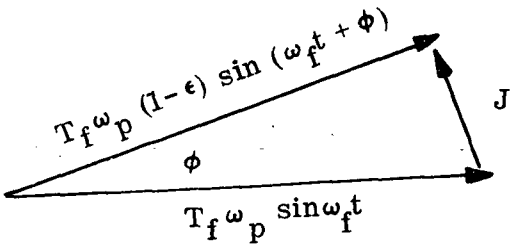
The argument of equation 1 expresses the phase of the pilot tone signal.

The phase of the master clock output (referred to the input) with respect to the phase of the pilot tone is

$$\frac{\psi_o}{N} - \psi_{in} = T_f \omega_p \left[(1-\epsilon) \sin (\omega_f t + \phi) - \sin \omega_f t\right]$$

where $(1-\epsilon)$ and ϕ are the amplitude and phase respectively of the PLO transfer function.

The difference in phase between input and output represents a timing error. The total error can be found by representing the phases as vectors:



Using the law of cosines

$$J = T_f \omega_p \left[1 + (1-\epsilon)^2 - 2(1-\epsilon)\cos\phi\right]^{1/2}$$

For small ϕ and ϵ,

$$J = T_f \omega_p \sqrt{\epsilon^2 + \phi^2}$$

J represents the peak phase error between input and output.

ϵ is the amplitude error of the PLO transfer function. In the region of interest, this can be accurately approximated as the reciprocal of the loop gain AB (see Appendix B).

$$AB = \frac{K}{N\omega_f} \cdot \frac{1}{\sqrt{1+\omega^2 T_1^2}} \cong \frac{K}{N\omega_f^2 T_1}$$

$$\therefore \epsilon = \frac{N\omega_f^2 T_1}{K}$$

ϕ is the phase of the PLO transfer function which for small angles is:

$$\phi = -2\xi \left(\omega_f^2 \frac{T_1 N}{K}\right)^{3/2} = -2\xi\epsilon^{3/2}$$

Thus

$$J = T_f \omega_p \epsilon \left[1 + 4\xi^2 \epsilon\right]^{1/2}$$

and since $J = \Delta t \omega_p$, where Δt is the peak jitter

$$\Delta t = T_f \epsilon \left[1 + 2\epsilon\xi^2\right]$$

where

$$\epsilon = N\omega_f^2 T_1/K$$

The small ϵ and with the nyquist stability constraints placed on the PLO, the timing error is principly due to amplitude error, and to a close approximation is

$$\Delta t = T_f \frac{N\omega_f^2 T_1}{K}$$

This expression determines the velocity constant of the loop based on the peak acceptable phase tracking inaccuracy at low frequencies.

3. Results. - The master clock was synthesized to maximize $\frac{K}{NT_1}$ for frequencies out to 10 Hz and still maintain adequate performance with respect to high frequency jitter and Nyquist stability. The results are shown in Figure 4-44.

c. Short Term Phase Stability. -

1. Introduction. - The short term phase stability of the master clock is governed principly by the shoe error component in the pilot tone. The effects of random noise in the pilot tone on the short term stability are negligible because of the narrowness of the loop.

2. Analysis. - The shoe error appears in the pilot tone as a periodic instantaneous phase change occurring at a 1250 Hz rate as shown in Figure 4-45a. This signal may be decomposed into a steady frequency offset and a periodic phase disturbance which appears as an error in the master clock loop (Figure 4-45b). A Fourier analysis of this signal yields the amplitude of each frequency component of this signal, enabling the optimum PLO transfer function to be synthesized. The Fourier series representation of the pilot tone phase with shoe error is:

$$d(t) = \Delta t \sum_{n=1}^{\infty} \frac{1}{\pi n} \cos \pi n \cos^2 \pi n f_s t$$

where $\Delta t = 100$ ns, the maximum specified shoe error, and $f_s = 1250$ Hz.

The peak phase jitter at each harmonic of the head switching rate can be computed and is shown in Table 4-15.

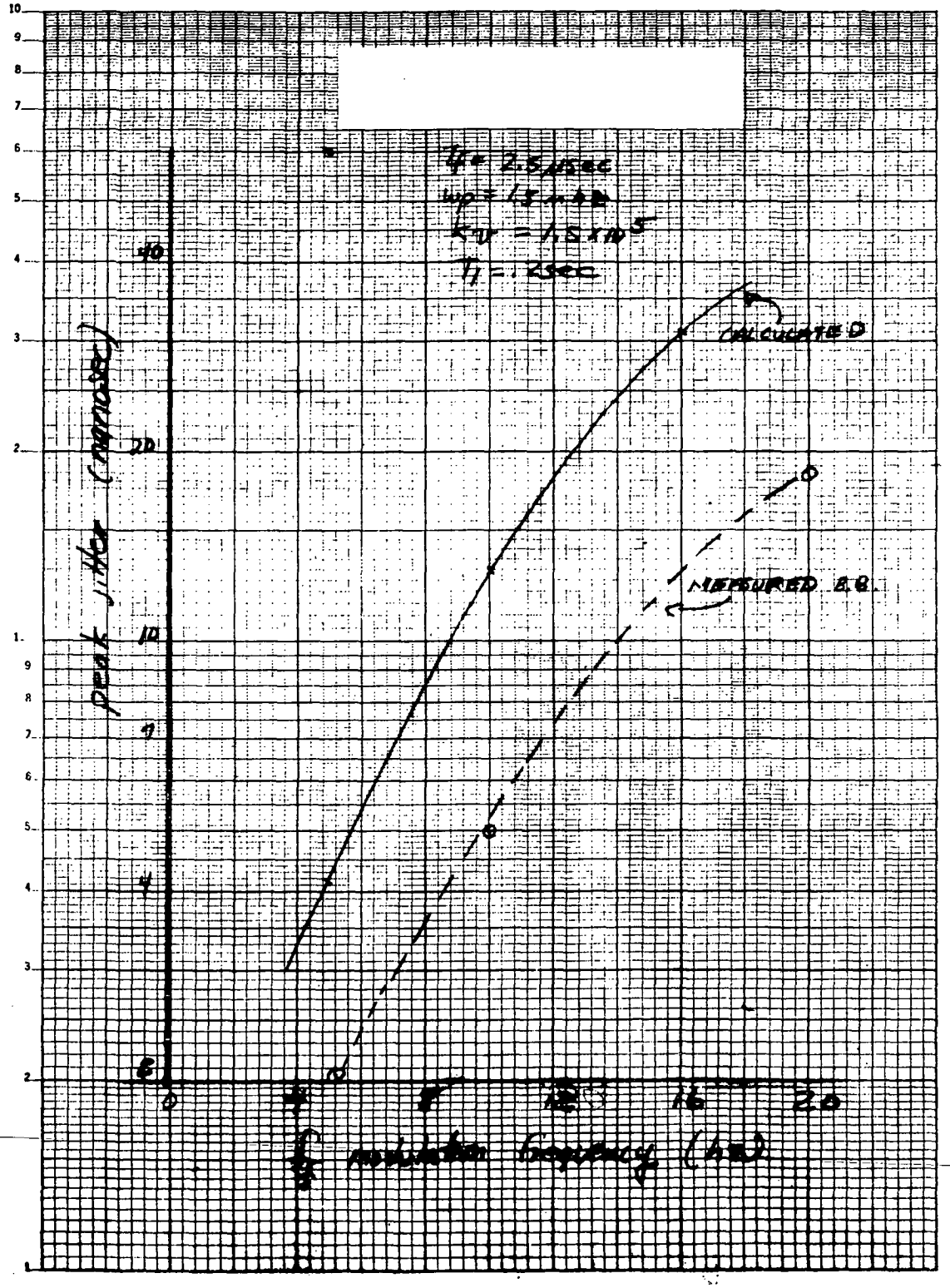
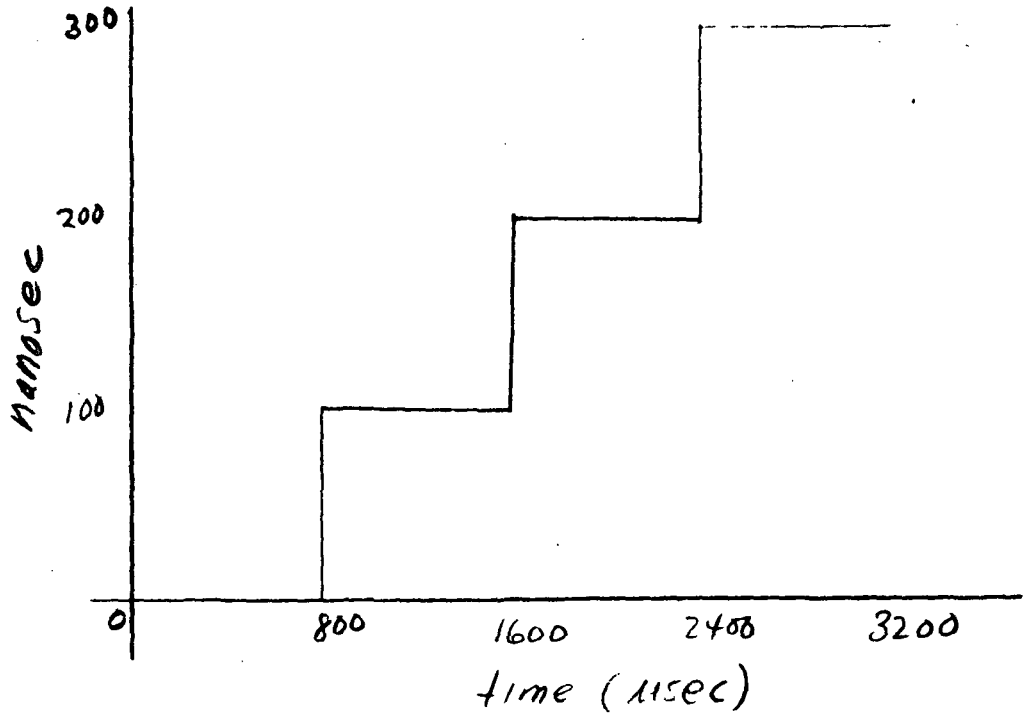
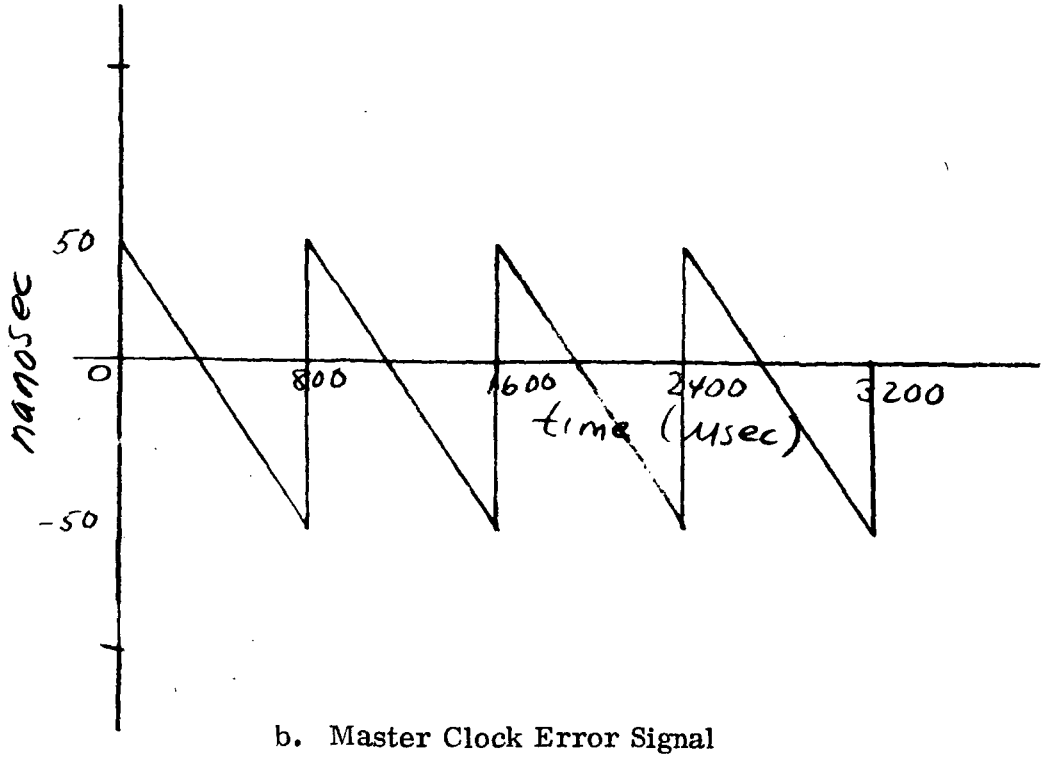


Figure 4-44. Master Clock Low Frequency Accuracy



a. Pilot Zone Cumulative Phase



b. Master Clock Error Signal

Figure 4-45. Shoe Error

TABLE 4-15. MASTER CLOCK PEAK PHASE JITTER

Frequency (Hz)	Peak Pilot Tone Jitter (ns)	Calculated Peak Master Clock Jitter (ns)
1250	32	0.55
2500	16	0.48
3750	11	0.27
5000	8	—

3. Results. - The open loop transfer function of the PLO is shaped to attenuate the jitter components to acceptable levels. The final configuration chosen utilizes a bridged tee filter resonant at the jitter frequency to obtain the greatest possible jitter reduction consistent with adequate phase margin. The bridged Tee yields a 3:1 reduction in jitter over the best possible design using a compensated lag network realizing the same phase margin. The calculated jitter components are shown in Table 4-15.

   The master clock jitter was measured on a wideband oscilloscope as follows: the oscilloscope main sweep was adjusted for 100 us/cm internally triggered; the delayed sweep for 100 ns/cm free running; the X10 multiplier was activated to yield a 10 ns/cm resolution. The master clock waveform now displayed is the result of triggering on the waveform and looking at a single cycle 100 us after being triggered; since the triggering is asynchronous with the jitter source, the jitter shows up as time jitter on the waveform edge.

   Utilizing this technique, the peak to peak jitter was measured to be less than 4 ns, which agrees with the analysis.

d. PLO Transfer Function. - The PLO open loop and closed loop transfer functions are shown in Figure 4-46. A summary of pertinent parameters utilizing the model of Appendix B is given below.

$$T_1 = 0.2 \text{ second}$$

$$T_2 = 1.78 \times 10^{-3} \text{ second}$$

$$K_v = 1.5 \times 10^5 = \frac{K}{N}$$

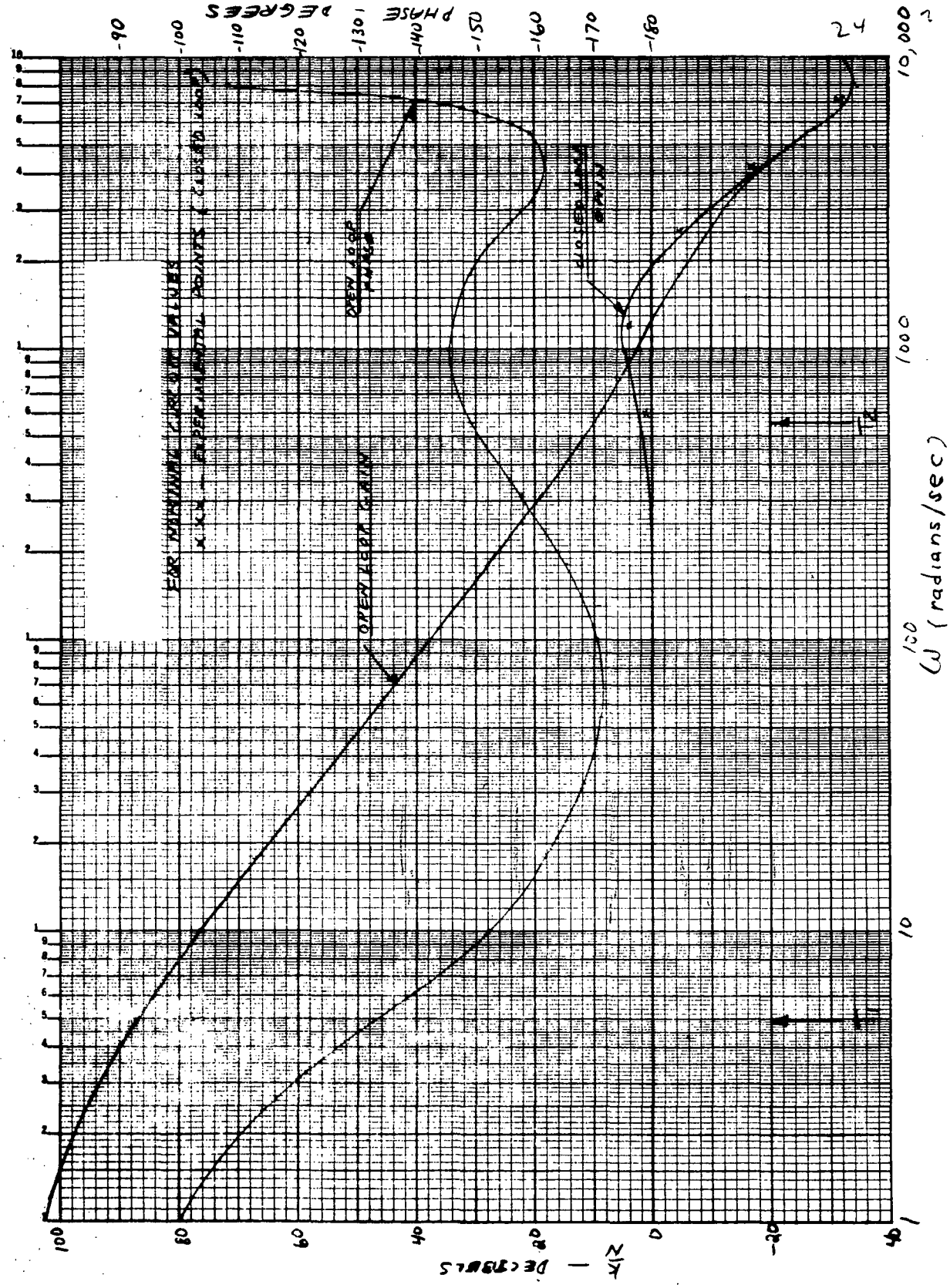


Figure 4-46. Computed Master Clock Transfer Functions for Nominal Circuit Values

$\xi = 0.5$

3 dB bandwidth = 360 Hz

e. Frequency Lock. - The pull-in range of a second order PLO with sinusoidal phase detector is given by[1] (see Appendix C).

$$\omega_p \leqq N\sqrt{4\frac{K}{N}\xi\,\omega_n}$$

The Master Clock loop, with parameters chosen to achieve the desired dynamic performance has a calculated pull-in range of ±28000 Hz. However, because of the non-minimum phase response of the bridged Tee filter, the pull in range is reduced to about ±15000 Hz. This was not deemed adequate (see worst case analysis).

Furthermore, specific conditions could result in a time to lock as long as 5 to 8 seconds. In order to alleviate this condition, acquisition circuitry was added to the PLO.

Frequency lock range is enhanced by a feed forward path through zener diodes, which circumvented the filter networks. An out of lock condition results in a triangular waveform at the output of the phase detector amplifier U4, with an amplitude of 8.5 volts peak. The zener diodes conduct signals above 5.5 volts peak around the compensated lag filter and twin Tee, effectively increasing the loop gain at high frequencies, and resulting in a PLO pull in range equal to the PLO hold in range. Normal disturbances entering the loop do not cause the diodes to conduct or are attenuated by the high pass filter following the diodes. Thus, the feed forward is inactive when the PLO is locked up. The acquisition time also is reduced to less than 0.1 second.

f. Cycle Slipping. - In order for the master clock to slip a cycle, a phase disturbance must be injected into the PLO greater than $\frac{\pi}{2}$ radians and lasting for greater than the response time of the PLO.

In ordinary operation the PLO input is a sinusoid and additive gaussian noise. Viterbi[1] computes the frequency of skipping cycles for this input as

$$f_s = \frac{4B_L}{\pi} e^{-2\alpha}$$

[1] Vilerbi, A.J. "Phase Locked Loop Dynamics in the Presence of Noise by Fokker-Planck Techniques" JPL TR #32-427.

where B_L is the PLO bandwidth and α is the input S/N ratio measured in the PLO bandwidth.

In the case of the master clock, the input signal to noise ratio measured in the PLO bandwidth (360 Hz) is greater than 50 dB, $\therefore \alpha > 10^5$. The time between cycle slips is the reciprocal of f_s or

$$T_s = \frac{\pi}{4 B_L} e^{2\alpha} \cong 2 \times 10^{40} \text{ seconds.}$$

Therefore, the probability of skipping a cycle in normal operation is very small.

In the presence of a complete signal dropout, a bound for the worst possible situation can be established by assuming an instantaneous 180° phase reversal of the input signal and noting the time required for the PLO phase (referred to the input) to reach 90°. The time is found from the 50% point on the step response input, an ECAP calculation of which is shown in Figure 4-47. The dropout bound turns out to be 750 μs, much longer than any conceivable tape dropout.

In practice, experiments indicate unlimited periods are tolerated since the phase detector output tends to remain stationary at the 90° point.

4.1.4.4.2 Worst Case Analysis. -

a. Nyquist Stability. - The design at the PLO must be such that Nyquist stability is assured under all operating conditions. The stability of the PLO is determined from a Bode Diagram of the open loop response.

The calculated nominal open loop response taken from the circuit constants is shown in Figure 4-46, along with the calculated and measured closed loop response.

Principal causes of deviation from the nominal closed loop characteristic result from component drift and initial tolerances:

1. Drift of dominant time constant due to C12 drift = ±15%.

2. Variation at loop gain due to

   a. Phase detector input voltage variation = ± 8%.

   b. U3 gain tolerance = ±3%

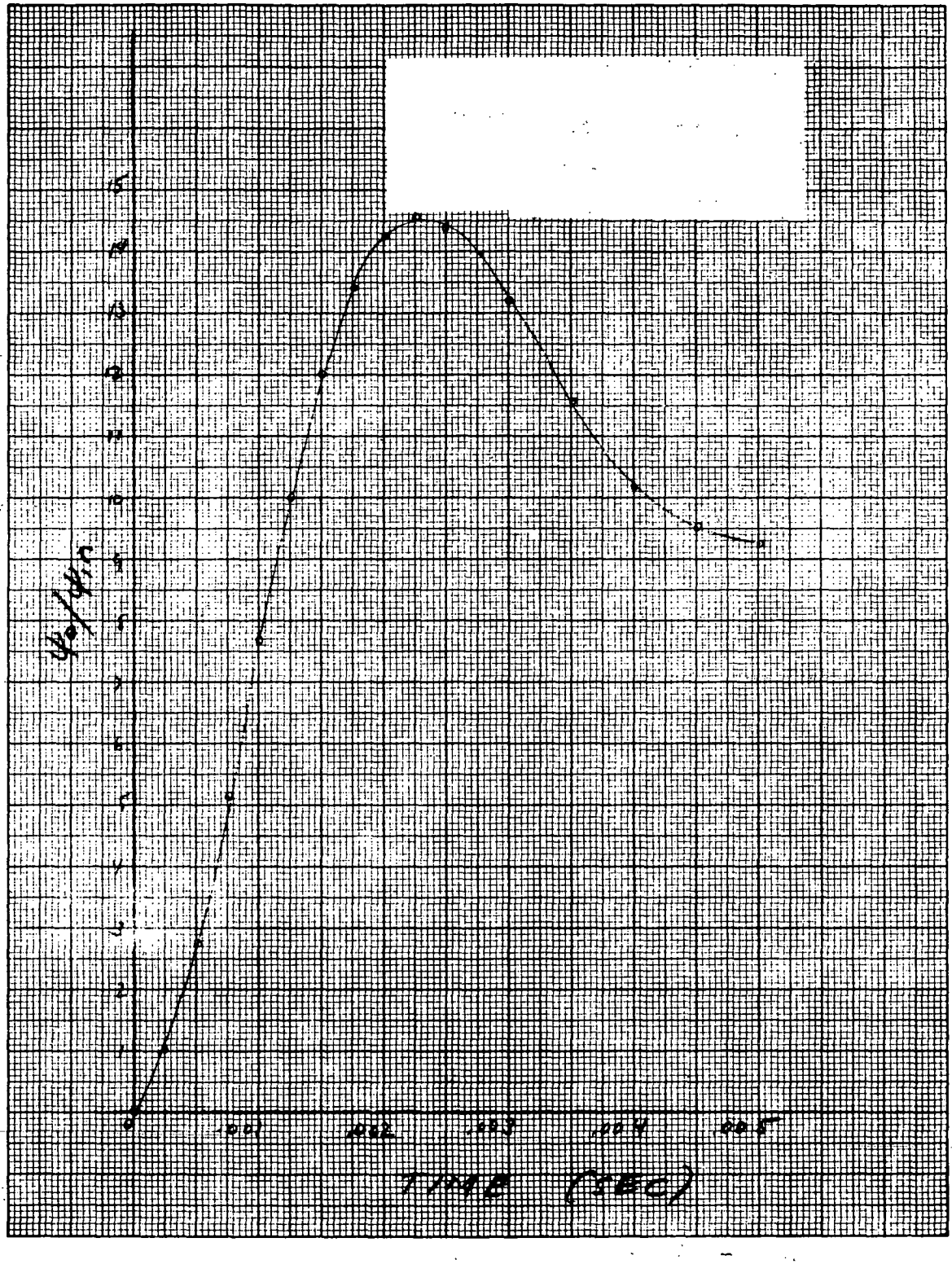


Figure 4-47. Master Clock Response to a Unit Phase Step

c. U4 gain tolerance = ±4%

d. U5 gain tolerance = ±4%

e. VCXO sensitivity tolerance = $^{+20\%}_{-\ 0\%}$

Total = $^{+39\%}_{-19\%}$

The result of a 100% reduction in the dominant time constant and 4 dB increase in gain is a severe test of Nyquist stability. The result of Figure 4-48 indicates a worst case phase margin of 18° with attendant response peaking of 9 dB; the peaking is of no consequence in the design. Under these conditions the short term phase jitter will increase 3 dB.

b. Master Clock Frequency Lock. - The master clock is required to frequency lock to the pilot tone under all conditions. Uncertainty in the pilot tone frequency and drift in the VCXO in the master clock require that a specific pull-in range be available in the master clock.

The frequency uncertainty in the pilot tone is the sum of

1. Spacecraft clock = $\pm 2 \times 10^{-5}$
2. MSS clock = $\pm 4 \times 10^{-5}$
3. Low frequency hunting = $\pm 16 \times 10^{-5}$
4. Shoe error — rejected by VCXO.

Total = $\pm 21 \times 10^{-5}$

This represents a worst case frequency deviation of the pilot tone of ±3300 Hz.

Sources of drift in the PLO arise in the phase detector, dc differential amplifier and VCXO.

1. Phase Detector. - A differential mode voltage can be developed at the phase detector output due to load resistor unbalance. The total unbalance is that due to initial tolerance (0% since initial zeroing is assumed), aging (±0.7%) and temperature (±0.03%).

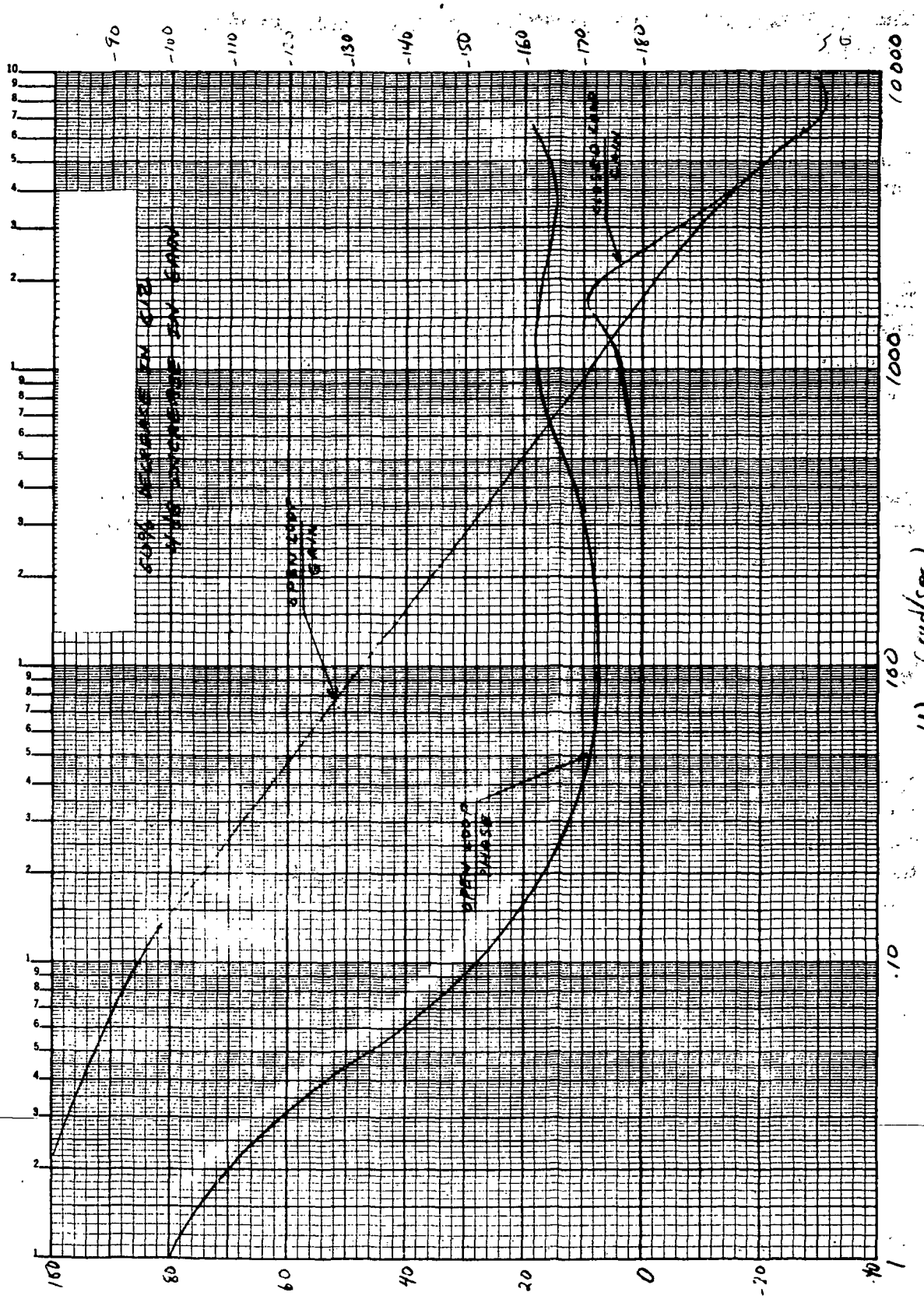


Figure 4-48. Master Clock Computed Transfer Characteristics

The resulting input voltage across the input differential amplifier U4 is

$$\Delta V = 2 \cdot I_C \cdot \Delta R = \pm 9.2 \text{ mV}$$

The other source of drift is that due to temperature coefficient of the output offset current in the phase detector. This voltage is

$$\Delta V = \Delta I \cdot \Delta T \cdot R = \pm 1.7 \text{ mV}$$

2. Differential Amplifier. - Resistor drift in the differential amplifier affects the common mode rejection ratio. The drift is the sum of aging (0.9%) and temperature (0.15%). The offset referred to the input as found from an ECAP simulation is

$$\Delta V = \pm 1.75 \text{ mV}$$

Temperature coefficient of the input offset voltage of the differential amplifier amounting to $\pm 20\ \mu V/^\circ C$ results in an equivalent net offset over temperature of

$$\Delta V = 20 \times 10^{-6} \times 30 = \pm 0.6 \text{ mV}$$

3. VCXO. - The specified drift of the VCXO is the sum of temperature (1×10^{-4}), power supply (0.5×10^{-4}) and aging (1×10^{-4} for one year). This is equivalent to ±3750 Hz.

4. Summary. - The VCXO is specified to have a minimum swing of ±19 kHz with ±14 V applied to its input. Transforming the equivalent voltage drifts to output frequency swing, using the actual amplifier and VCXO sensitivities (14.6 V/V, 28.7 V/V and 1600Hz/volt), we find that the drifts are

1.	Pilot tone uncertainty =	± 3150 Hz
2.	Phase detector drift =	± 8450 Hz
3.	Differential amplifier drift =	± 1540 Hz
4.	VCXO Drift =	± 3750 Hz
	Total =	±16890 Hz

This is within the minimum pull-in range of 19000 Hz.

c. Master Playback Clock Symmetry. - The master playback clock signal is derived from the master clock VCXO, whose output is a sinusoid of amplitude 1.0 Vpp (minimum). This waveform is applied to a long tailed pair (Q_1, Q_2, Q_3) for conversion to a square wave suitable for driving a TTL gate. The symmetry of the master clock playback signal is specified to be $\pm$5 ns (maximum). This symmetry is adjusted by controlling the current through the tail in the differential amplifier.

The model chosen for analysis of the variation in switching times at the output of the gate is shown in Figure 4-49.

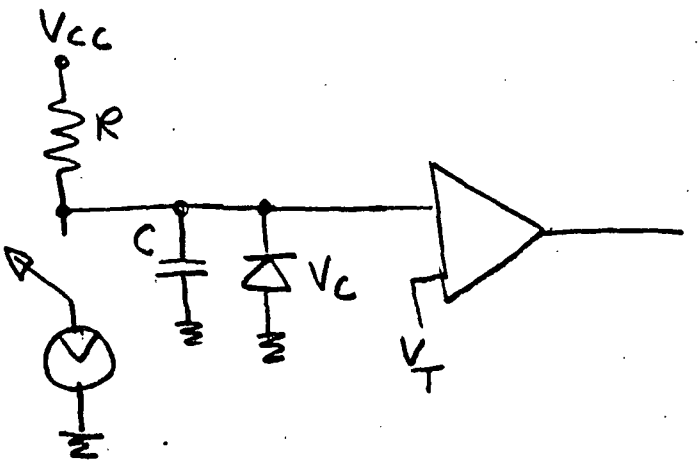


Figure 4-49. Squaring Circuit Model

where I is the tail current, R the load resistor, C the interstage capacitance, V_C the clamp diode voltage and V_T the gate threshold voltage.

Then, the transient equations are

$$V_{on} = (V_{cc} + V_c)\,(1 - e^{-t/RC}) - V_c$$

$$V_{off} = V_{cc} - IR\,(1 - e^{-t/RC})$$

where V_{on} and V_{off} refer to the gate turn on and turn off transients. Now, assuming a linear transient we find that

$$t_{on} = \frac{V_T + V_c}{V_{cc} + V_c} RC$$

$$t_{off} = (V_{cc} - V_T) \frac{C}{I}$$

and

$$\left| dt_{on} \right| = \left| \frac{\partial t_{on}}{\partial V_t} \right| dV_T + \left| \frac{\partial t_{on}}{\partial V_c} \right| dV_c + \left| \frac{\partial t_{on}}{\partial V_{cc}} \right| dV_{cc}$$

$$\left| dt_{off} \right| = \left| \frac{\partial t_{off}}{\partial V_{cc}} \right| dV_{cc} + \left| \frac{\partial t_{off}}{\partial V_T} \right| dV_{cc} + \left| \frac{\partial t_{off}}{\partial I} \right| dI$$

The worst case is found with the following circuit parameters:

$V_T = 1.45 \pm 0.15$ V

$V_{cc} = 5 \pm 0.05$ V

$V_c = 0.6$ V ± 0.06 V

$R = 510$

$C = 20$ pF

$I = 12$ mA ± 0.6 mA

$dt_{on} = \pm 0.39$ ns

$dt_{off} = \pm 0.86$ ns

To these figures must be added the propagation delay variation of the output gate which is ± 1 ns. The sum is well within the specifications and has been verified experimentally.

4.1.4.4.3 Conclusions. - The analysis has verified the ability of the master clock to conform to specifications over extended periods of time and temperature. Analysis of several components of the master clock, namely the power supply, pilot tone extraction filter, and limiter are not included herein, since they are more directly related to the variable clock performance and as such will be reported upon there.

4.1.4.5 Variable Clock Worst Case Analysis. - The input to the variable clock is the 1.5 MHz pilot tone recorded simultaneously with the MSS clock. The variable clock output, (1-3, 2-4 clock) is a 15 MHz signal used to strobe the MSS data as it comes from the data decoder.

The design of the variable clock insures that the variable clock output conforms to the following specifications for the environmental conditions listed in the worst case analysis criteria.

1.0 Output Long Term Stability — Sum of MSS clock and Spacecraft clock.

2.0 Phase accuracy — ±10 ns, DC to 5000 hz, ≥ 100 us subsequent to head switching, with ±100 ns input phase transient, pilot tone S/N ratio ≥ 41 dB rms/rms (5 kHz bw).

3.0 Output loading — TTL compatible, 10 unit loads.

4.1.4.5.1 Design Criteria and Performance. -

a. Introduction. - The variable clock is designed to track, within prescribed limits, the phase of the playback pilot tone. The pilot tone undergoes rapid phase transients (as large as ±100 ns) at a 1250 Hz rate due primarily to shoe errors in the headwheel panel. Following the transients, 120 us are allowed in the MSS system for settling time (overlap period). The variable clocks utilize this time to re-adjust their output phase to that of the pilot tone. The noise bandwidth of the variable clocks are carefully tailored to be the minimum required to achieve the desired phase accuracy, since the pilot tone noise adds significantly to the variable clock output phase uncertainty.

The phase instability of the variable clock arises from the following sources:

1. Pilot tone random noise.
2. Transients introduced in head switching
3. Low frequency phase and amplitude flutter in the pilot tone.
4. Static circuit drifts.

The design of the variable clock is such as to minimize the sum of the transient inaccuracy and random noise while maintaining the DC drifts below a level which can be corrected by the phase correction loop (see Paragraph 4.1.4.1).

b. Pilot Tone Frequency Selection. - The upper limit on the pilot tone frequency is imposed by the requirement that phase error in the variable clock PLO should never exceed $\pi/2$ radians, or a skipped cycle might result. If a 100 ns maximum shoe error is assumed, the resulting pilot tone maximum frequency is 2.5 MHz. A second consideration is intermodulation of the data by the pilot tone. From this standpoint, the pilot tone should be as low a frequency as possible but 1.0 to 1.5 MHz is reasonable.

A third consideration is the phase jitter on the variable clock resulting from the finite signal to noise ratio of the pilot tone. The output phase jitter is inversely proportional to the pilot tone frequency, assuming pilot tone signal to noise ratio indicating that the maximum pilot tone frequency is most desirable. Consideration of all these factors led to a choice of 1.5 MHz for the pilot tone frequency.

c. Pilot Tone Extraction. -

1. Attenuation Characteristics. - The pilot tone is present at the equalizer output with the FM MSS signal. The pilot tone extraction filter is used to separate the pilot tone from this composite signal and to suppress components of the FM signal so that jitter cannot be introduced into the clocks by the FM signal.

   The relative level of the pilot tone to the FM signal at the equalizer output is shown in Figure 4-50.

   Jitter can be introduced into the PLO around spurious response frequencies of the phase detector. The most important frequencies are noted on Figure 4-50 and constitute the 3rd, 5th and 7th order spurious responses of the phase detector.

   Experimental data on the phase detector indicates 30 dB rejection of 3rd order, 36 dB rejection of 5th order, and 40 dB rejection of 7th order intermodulation.

   Considering the FM signal as random noise and assuming a 30 kHz noise bandwidth for the variable clock PLO, an input signal to noise ratio of 48 dB is required to achieve one ns peak jitter in the PLO output. Thus, each intermodulation component should be attenuated so that the sum of the filter attenuator and phase detector spurious rejection exceeds 48 dB.

   The pilot tone extraction filter attenuation characteristics shown in Figure 4-51 were synthesized using the foregoing reasoning. Its attenuation is ample to reject every spurious at least 55 dB.

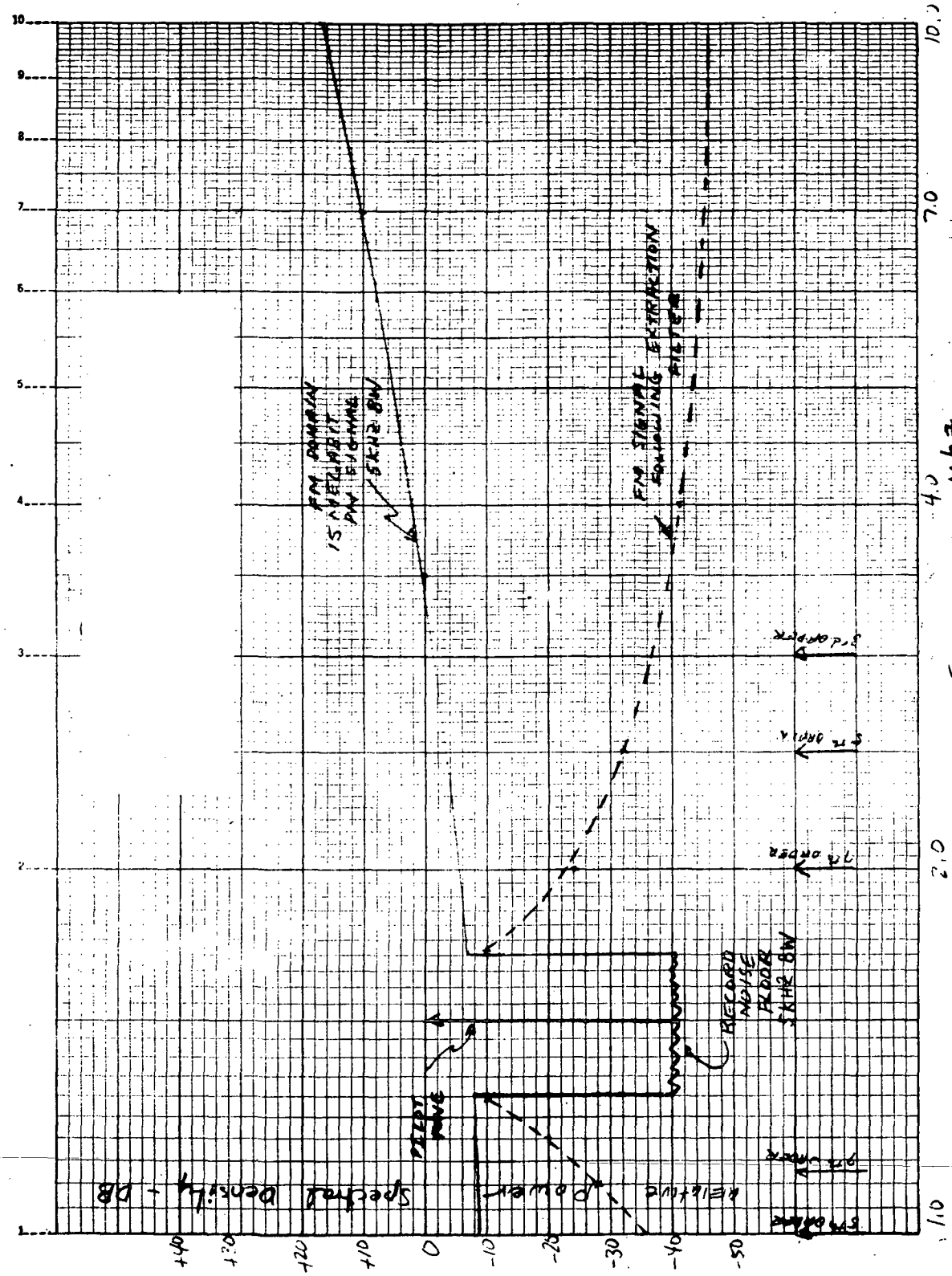


Figure 4-50. Power Spectral Density of FM Composite Signal at Equalizer Output

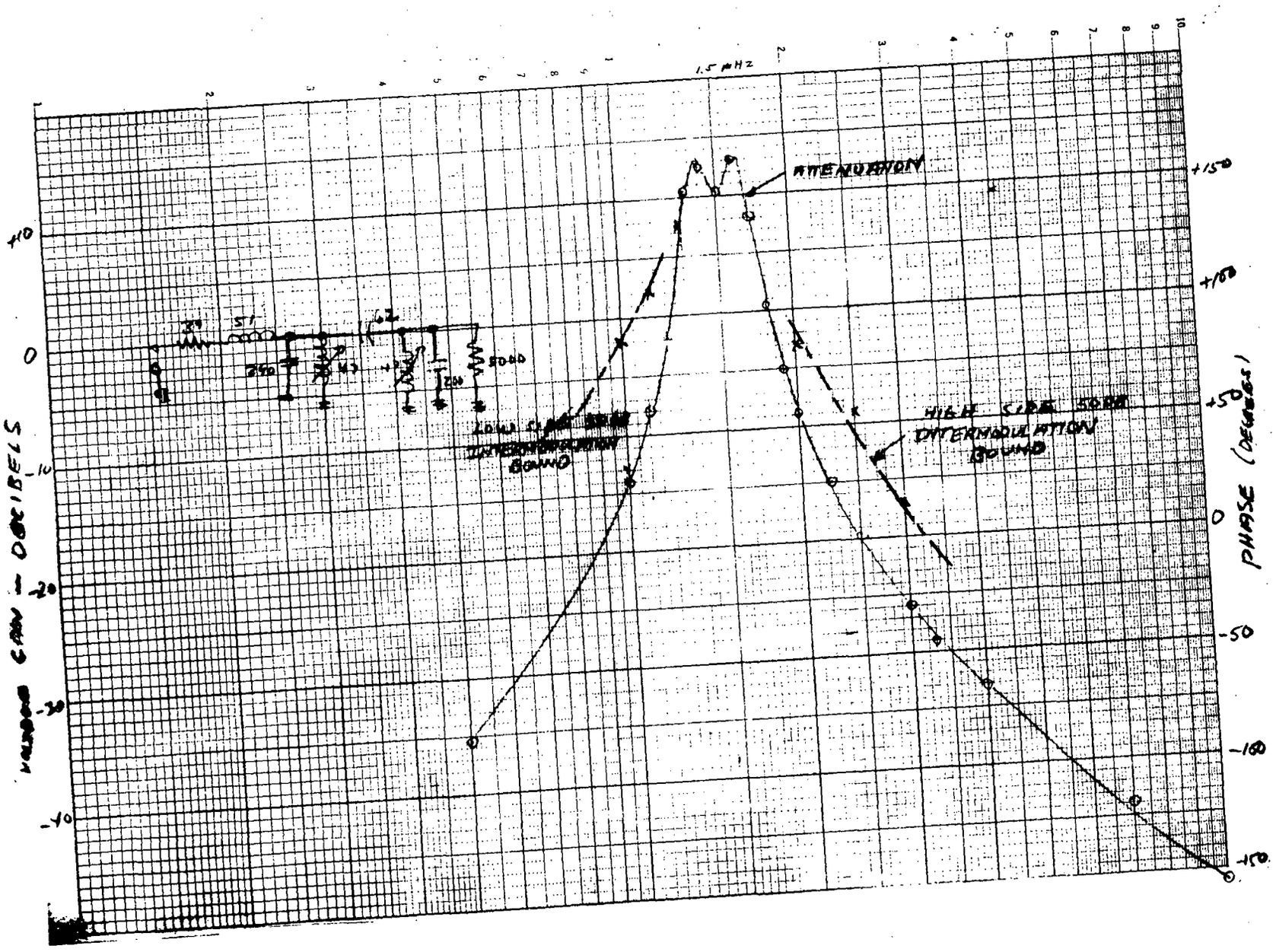


Figure 4-51. Pilot Tone Extraction Filter Attenuation Characteristics

2. Input Impedance. - The pilot tone filters are driven by emitter followers with an output impedance on the order of 10 ohms. In one instance, two filters are driven in parallel by one driver. The input impedance of the pilot tone filters is of interest to assure that undue loading of the drivers does not take place. (See Figure 4-52.)

3. Transient Response. - The lower limit on bandwidth of the pilot extraction filter was selected on the basis of transient phase response. In order to establish a feel for the result, a two pole bandpass filter was analyzed. The response of the four pole filter was extrapolated from this result due to the difficulty of an exact analysis of the more complex filter structure.

The excitation to the filter was assumed to be of the form:

$$f(t) = \sin \omega pt - \mu (t-T) \sin \omega pt + \mu (t-T) \sin (\omega pt + \phi_p) \quad (1)$$

This is a step change in phase at time T. The form of the output of a two pole bandpass filter of center frequency ω_o and half bandwidth $\alpha = \omega o/2Q$ is

$$\begin{aligned} Fo(t) = {} & Be^{-\alpha(t-T)} \sin \left[\beta (t-T) + \beta T + \psi_2\right] \\ & + A \sin \left[\omega_p (t - T) + \beta T + \psi_1 + \phi_p\right] \\ & - Be^{-\alpha(t - T)} \sin \left[\beta (t - T) + \psi_2 + \beta T + \phi_p\right] \end{aligned} \quad (2)$$

for $t>T$, let $\tau = t - T$ and collecting terms

$$\begin{aligned} fo(\tau) = {} & A \sin (\omega_p \tau + \psi_1 + \phi_p) \\ & - 2B e^{-\alpha 7} \sin\left(\frac{\phi_p}{Z}\right) \cos\left(B\tau + \psi_2 + \frac{\phi_p}{2}\right) \end{aligned} \quad (3)$$

The desired output is $\sin (\omega_p \tau + \phi_p)$. In order to see the phase error in $fo(\tau)$, multiply by $2 \cos (\omega_p t + \phi_p + \psi_1)$ and examine the low frequency terms. This is equivalent to examining the output of a phase detector with a characteristic $V_{out} = \sin (\phi_1 - \phi_2)$

$$\begin{aligned} V_{out} = {} & A \sin\left(\psi_1 - \psi_2\right) - Z Be^{-\alpha\tau} \sin \frac{\phi_p}{2}\Big) \\ & \cos \left[(\omega_p - \beta) \tau + \psi_1 - \psi_2 + \frac{\phi_p}{2}\right] \end{aligned} \quad (4)$$

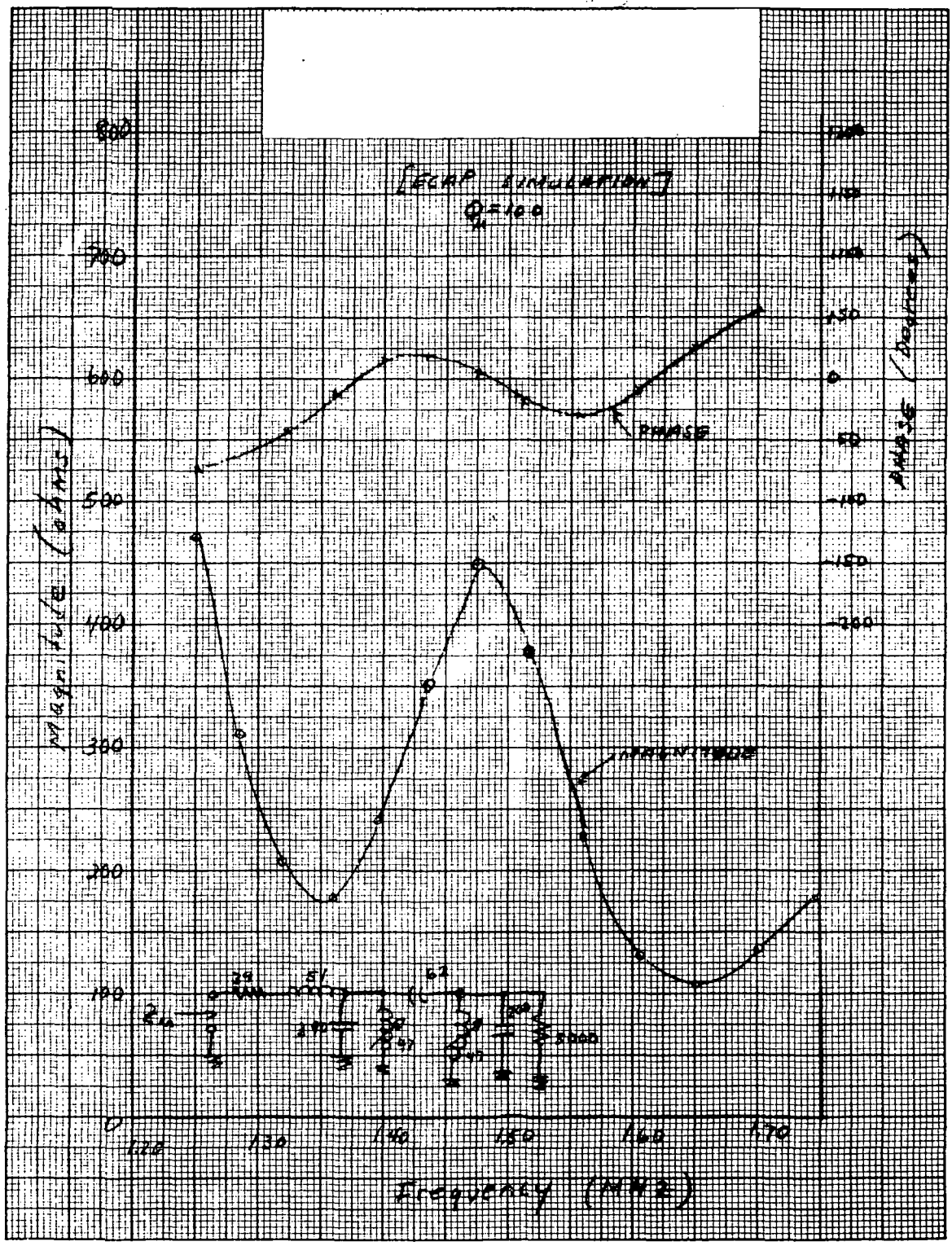


Figure 4-52. Pilot Tone Extraction Filter Input Impedance

If ω_p is within 10% of ω_o, $\psi_1 - \psi_2$ is negligible and A = B = 1.

Then

$$\text{Sin}\,(\phi_1 - \phi_2) = 2e^{-\alpha\tau} \sin\left(\frac{\phi_p}{2}\right) \cos\left[(\omega_p - \omega_o)\,\tau + \frac{\phi_p}{2}\right] \quad (5)$$

Now substituting time displacement for phase since

$$\phi_p = \omega_p T_s$$

$$\phi_1 - \phi_2 = \omega_p te$$

and letting

$$\Delta_\omega = \omega_p - \omega_o$$

The time displacement error is found to be

$$te = \frac{1}{\omega_p} \sin^{-1}\left\{-2e^{-\alpha\tau} \sin\left(\frac{\omega_p T_s}{2}\right) \cos\left(\Delta\omega\tau + \frac{\omega_p T_s}{2}\right)\right\} \quad (6)$$

Equation 6 is shown plotted for several pilot tone frequencies in Figure 4-53. From this we see that in order for the phase to settle to within 1% we must satisfy

$$2\alpha T \geq 8$$

If 20 us is allocated to the filter for settling time, then

$$\frac{\omega_o}{Q} \geq 400 \text{ kHz.}$$

The four pole pilot tone extraction filter which was constructed has approximately this bandwidth. The phase transient response was measured using a phase modulator and wide band phase detector, and was seen to agree reasonably well with the analytic results for the two pole filter. (See Figure 4-54.)

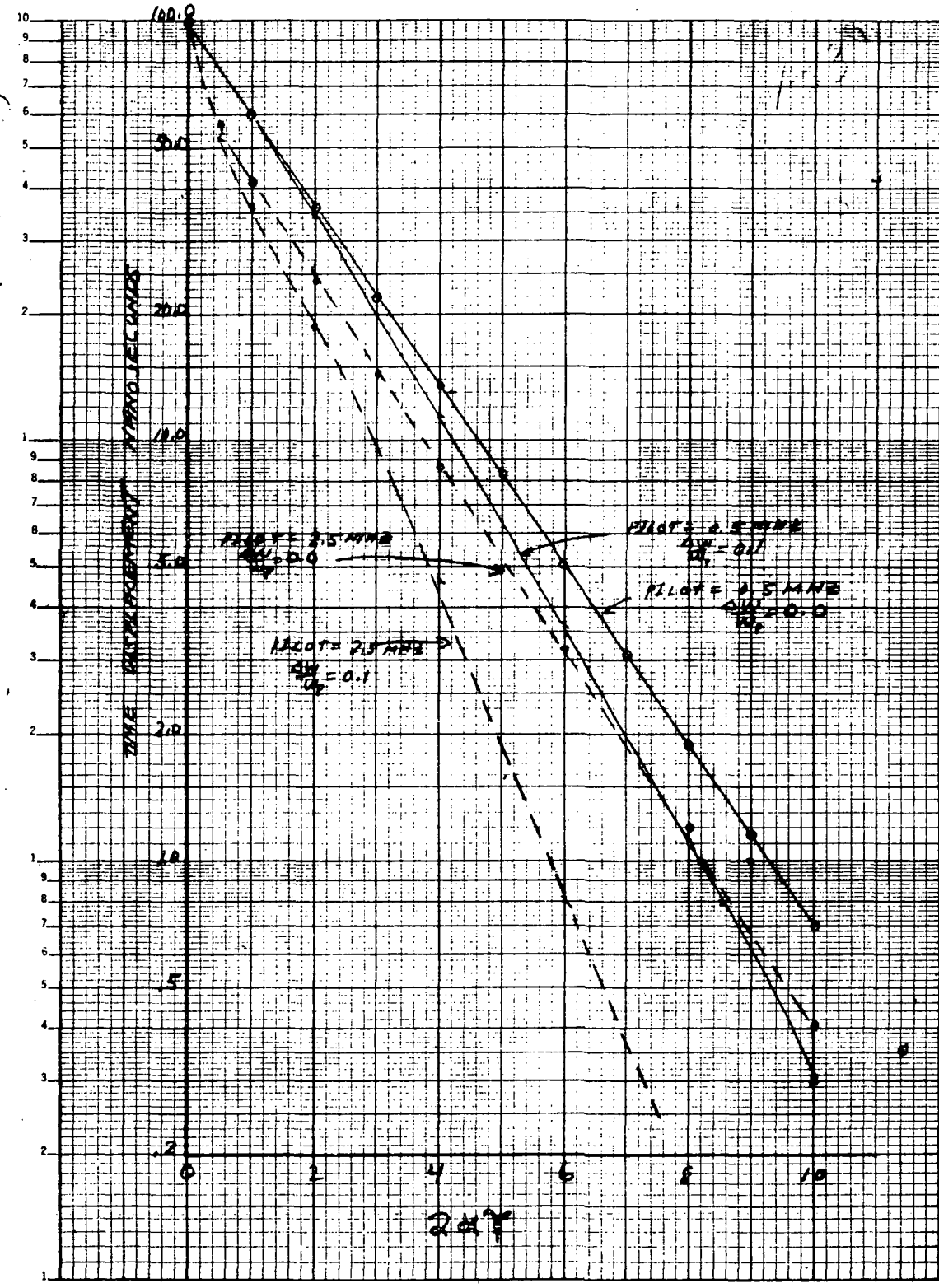


Figure 4-53. Settling Time Through a 2 Pole Filter to a Step Change in Phase ($T_S = 100 \times 10^{-9}$)

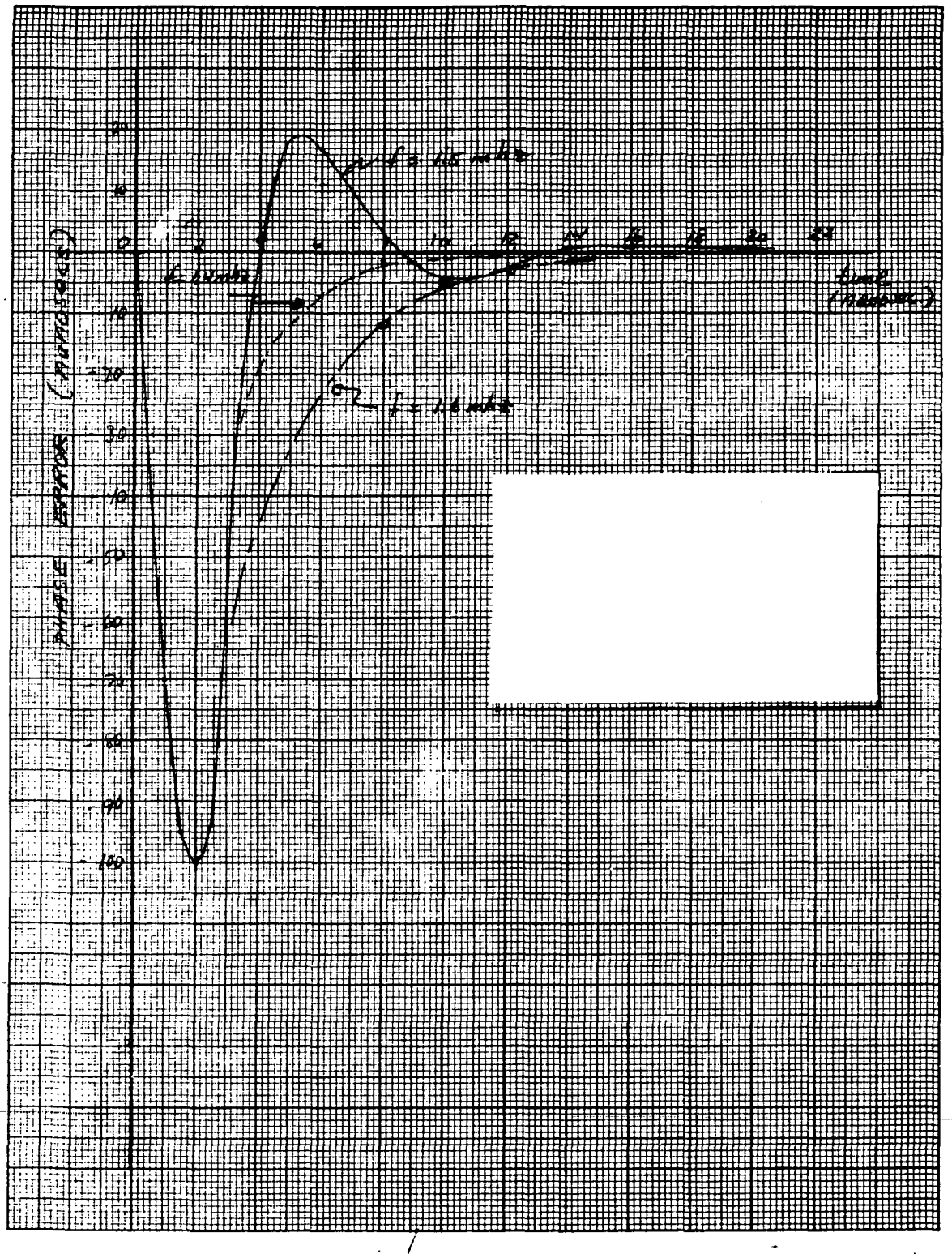


Figure 4-54. Pilot Tone Extraction Filter, Transient Phase Response to a 100 Microsecond Step

d. Limiter. - The limiter serves to remove AM fluctuations from the pilot tone which, if allowed to enter the phase detector, might introduce phase jitter in the variable clock signal.

The limiter static transfer function is shown in Figure 4-55. The limiter provides at least 20 dB of full limiting to the nominal pilot level of 100 mVpp.

AM to PM conversion was tested by amplitude modulating a 1.5 MHz signal generator with an audio tone. The measured jitter on the variable clock output was less than 1 ns (peak) for modulating frequencies up to 100 Hz with 50% modulation and a carrier level of 60 mVpp. Phase jitter was too small to measure below 30 Hz.

e. Phase Locked Oscillator. -

1. PLO Bandwidth. - The dynamic time base stability of the variable clock is primarily a function of the PLO transfer function. Jitter contribution from pilot tone noise is reduced with decreasing bandwidth while settling time from shoe error excitation is reduced with increasing bandwidth.

The frequency response of the PLO is determined by the parameter ω_n (see Appendix C) and optimum performance is obtained by choosing these parameters to yield minimum time base error following the overlap period.

In order to determine the optimum parameters, an analysis of contributory factors was made and the design optimized as discussed in the succeeding sections.

Additive Noise. - Additive random noise E_{np} associated with the playback pilot tone, E_{sp} causes a perturbation of the pilot tone zero crossings resulting in short term phase jitter of the pilot tone and of the variable clock output. A simple model for this phenomenon is shown in Figure 4-56.

If the ratio E_{sp}/E_{np} is high (the case of interest), the phase jitter of E_{sp} can be simply written as:

$$\Delta\theta = \frac{E_{np}}{E_{sp}} \qquad (1)$$

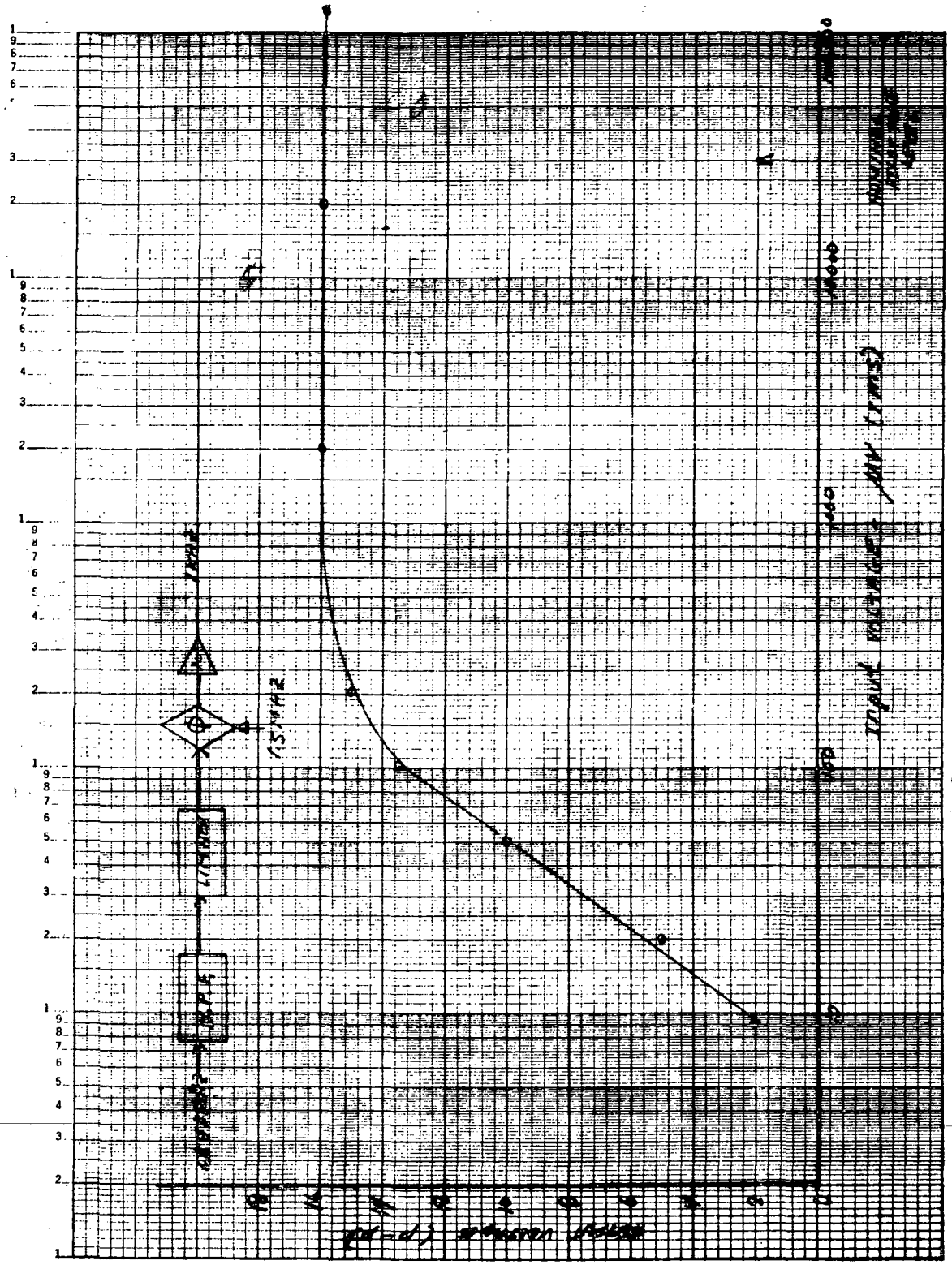


Figure 4-55. Limiter Transfer Function

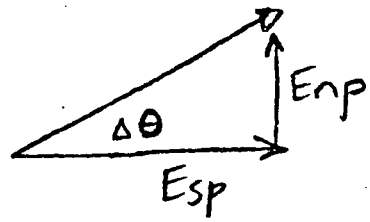


Figure 4-56. Phase Jitter Model

where Esp is the signal peak amplitude and Enp is the noise peak amplitude. This can be converted to time jitter by noting that

$$\Delta\theta = \frac{t_n}{T_p} \times 2\pi \tag{2}$$

where tn is the time jitter and Tp is the period of the carrier.

Combining (1) and (2), the required peak signal to peak noise ratio to achieve a peak time jitter is

$$\frac{E_{sp}}{E_{np}} = \frac{1}{\omega_p t_n} \tag{3}$$

Since signal to noise ratio is frequently measured as peak signal to RMS noise, and considering narrowband noise, the RMS noise amplitude is

$$E_n = E_{np}/\sqrt{2}$$

and

$$t_n = \frac{\sqrt{2}}{\omega_p \left(\frac{E_{sp}}{E_n}\right)} \tag{4}$$

This equation is shown plotted in Figure 4-57 for a 1.5 MHz pilot tone frequency.

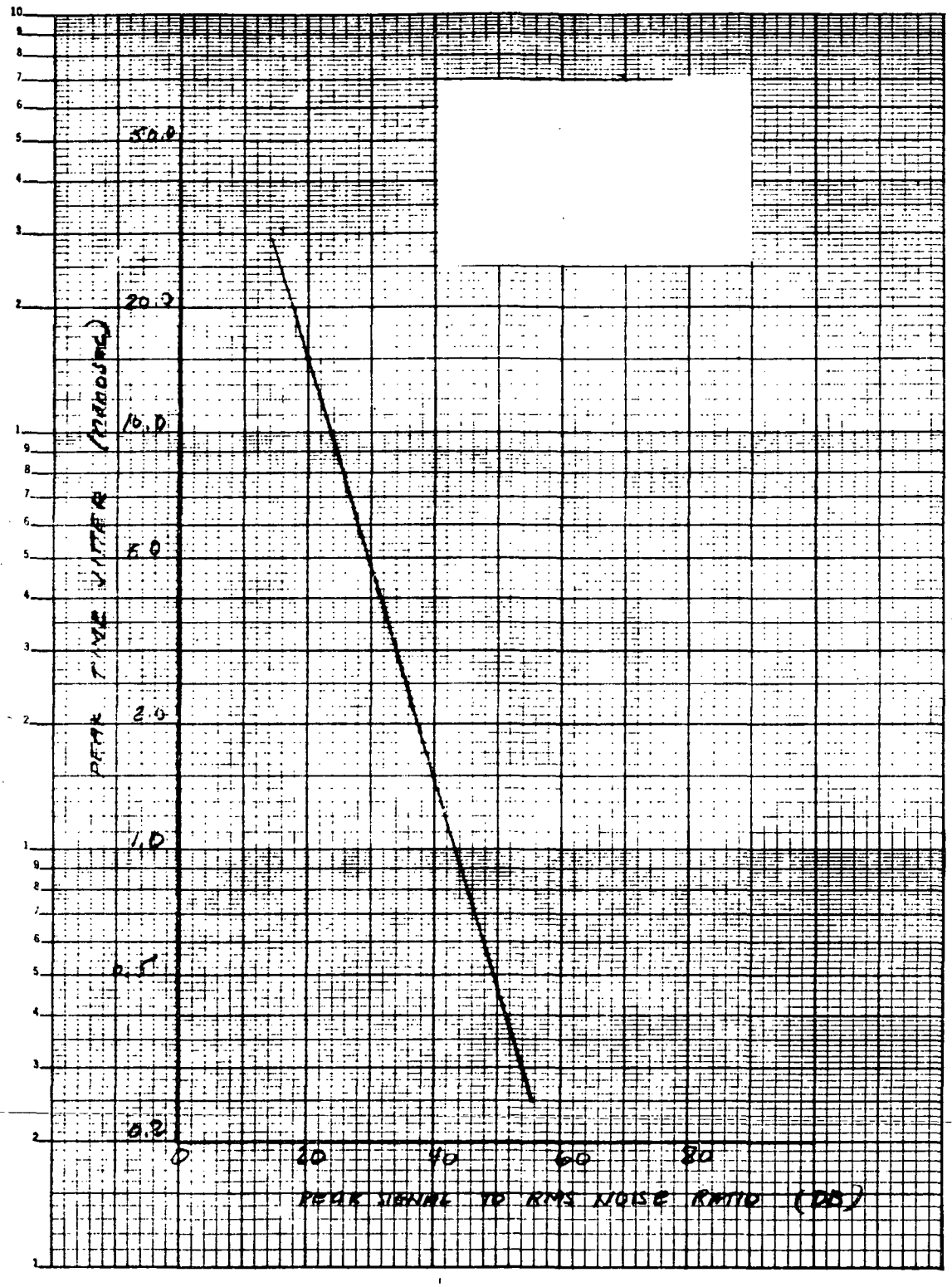


Figure 4-57. Signal to Noise Ratio vs Induced Time Jitter

The effect of the PLO on the signal to noise ratio is found with the assumption that the input noise spectrum is flat within the PLO bandpass. The PLO noise bandwidth is given by

$$B_n = \frac{1}{2}\,\omega_n\left[2\xi + \frac{1}{2\xi}\right] \text{Hz} \tag{5}$$

The pilot tone signal to noise ratio is commonly calculated from a slot noise measurement. Assume that the noise is measured in a slot Bs Hz wide. Then, combining (4) and (5), peak time base jitter tn' at the PLO output is given by:

$$t_n' = \frac{\sqrt{\omega_n\left(2\xi + \frac{1}{2\xi}\right)}}{\omega_p\left(\frac{E_{sp}}{E_n}\right)\sqrt{B_s}} = \sqrt{\frac{B_n}{B_s}}\,t_n \tag{6}$$

where Esp/En is the peak signal to rms noise ratio in a slot Bs Hz wide. This equation is plotted in Figure 4-58.

Note that the PLO output phase jitter can be reduced to arbitrarily low values independent of the input S/N ratio providing the bandwidth of the PLO is reduced to zero. The PLO bandwidth, however, cannot be reduced without limit because the PLO must follow the phase transients introduced by head switching. This is discussed in the following section.

Transient Response. - Each time a playback head comes in contact with the tape, a step phase discontinuity as large as ±100 ns may be introduced into the pilot tone and data. Since the variable clocks, of necessity, have a much lower bandwidth than the data channels, a phase disturbance is generated which advances or retards the variable clocks with respect to the data.

The head overlap time which follows the transient is utilized by the variable clocks as settling time. The overlap time is 120 us. The variable clock has been allowed a settling time to 1% of 100 us to allow for tolerances in the variable clocks and overlap time.

The PLO response to a step change in phase is derived in Appendix C, and some typical normalized responses are shown in Figure 4-59. Of

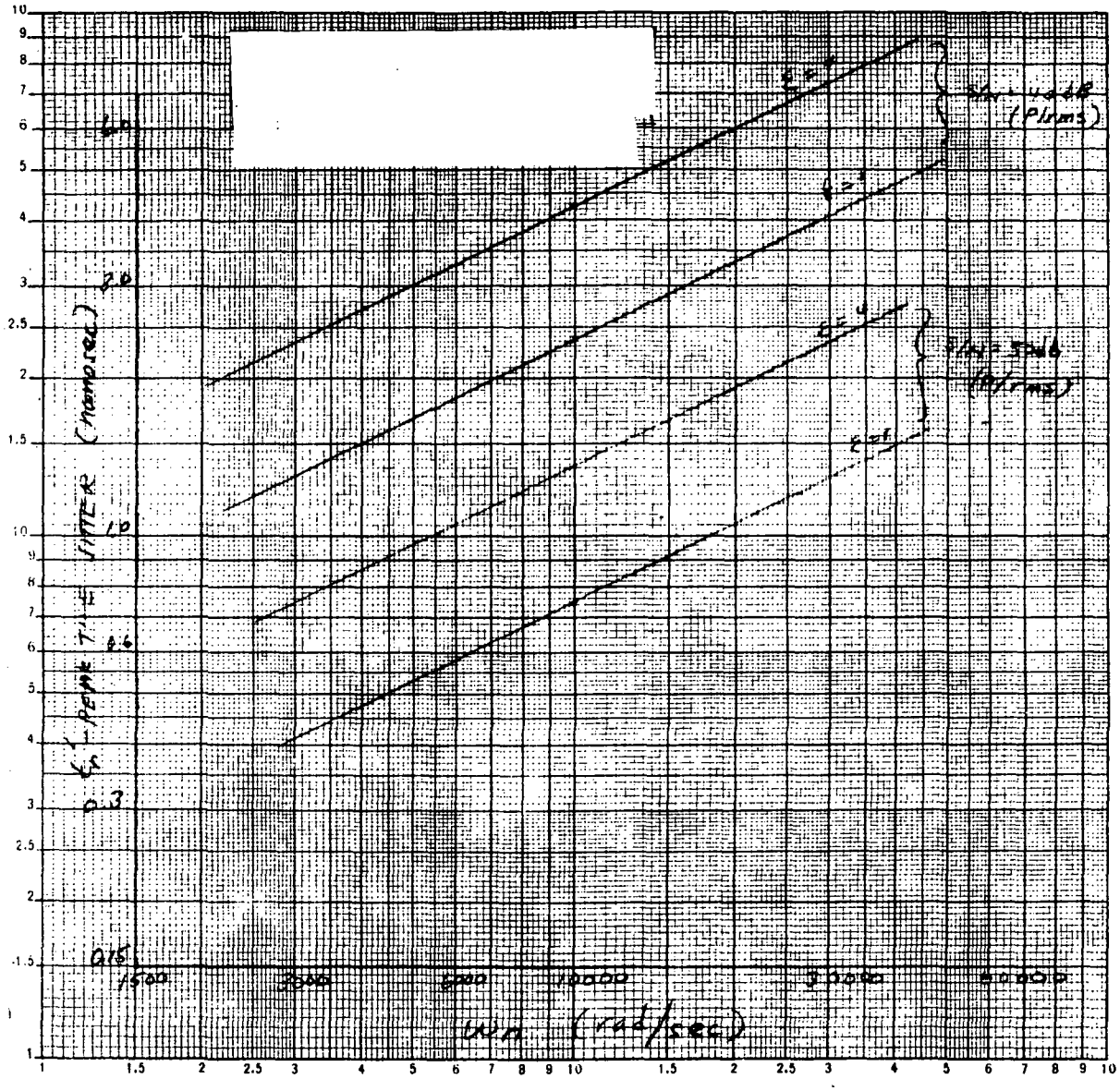


Figure 4-58. PLO Output Peak Jitter

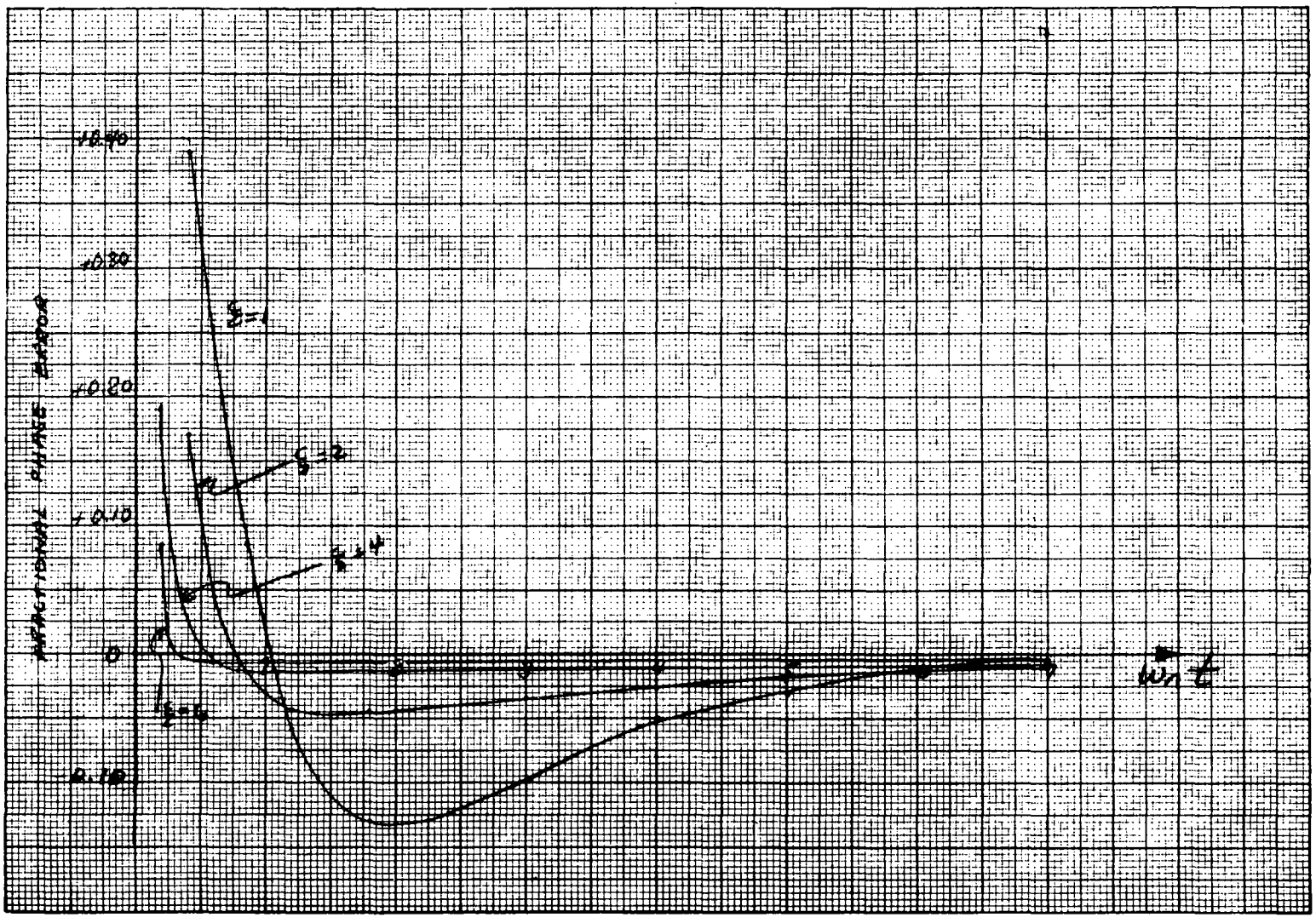


Figure 4-59. Fractional Phase Error for a Step Change in Input Phase

significance is that the normalized settling time to 1% is much smaller for large values of ξ (damping factor) although for very small errors, low damping factors are desirable.

Optimization. - Optimization of the variable clock involves choosing ω_n and ξ in such a way that the PLO noise bandwidth is minimized while insuring that the settling time is sufficiently short.

The optimization was carried out by using calculations of normalized settling time as a function ξ and assuming a specific accuracy requirement 100 us following the phase excitation. Figure 4-60 is the outcome of this calculation, indicating a preference for an overdamped system for the case where a finite but small inaccuracy in the response can be tolerated.

With Figure 4-60 as a guideline, a worst case analysis was conducted to determine the transient response as a function of component tolerances and drifts. This analysis resulted in the selection of $\omega_n = 4000$ rad/s and $\xi = 6$ for the nominal case. The noise bandwidth is 24 kHz for these parameters, resulting in a peak phase jitter (44 dB peak/rms pilot tone signal to noise ratios) of

$$t_n = \frac{\sqrt{2}}{\omega_p \left(\frac{E_{sp}}{E_n}\right)} \sqrt{\frac{B_n}{B_s}} = 2.13 \text{ ns.}$$

The transient phase error as a function of time is shown in Figure 4-61 for an assumed input phase transient of 100 ns. These curves were experimentally verified.

2. PLO Velocity Constant. - The velocity constant (Appendix C) of the PLO is the open loop gain of the loop at a frequency of 1 rad/s. It is found from an analysis of the PLO drift (see Paragraph 4.1.4.5.2) that the velocity constant of the loop controls the phase accuracy of the variable clock if VCO drift should occur. The expression for the phase drift is

$$t = \frac{1}{K_v} \left(\frac{\Delta \omega_c}{\omega_c}\right)$$

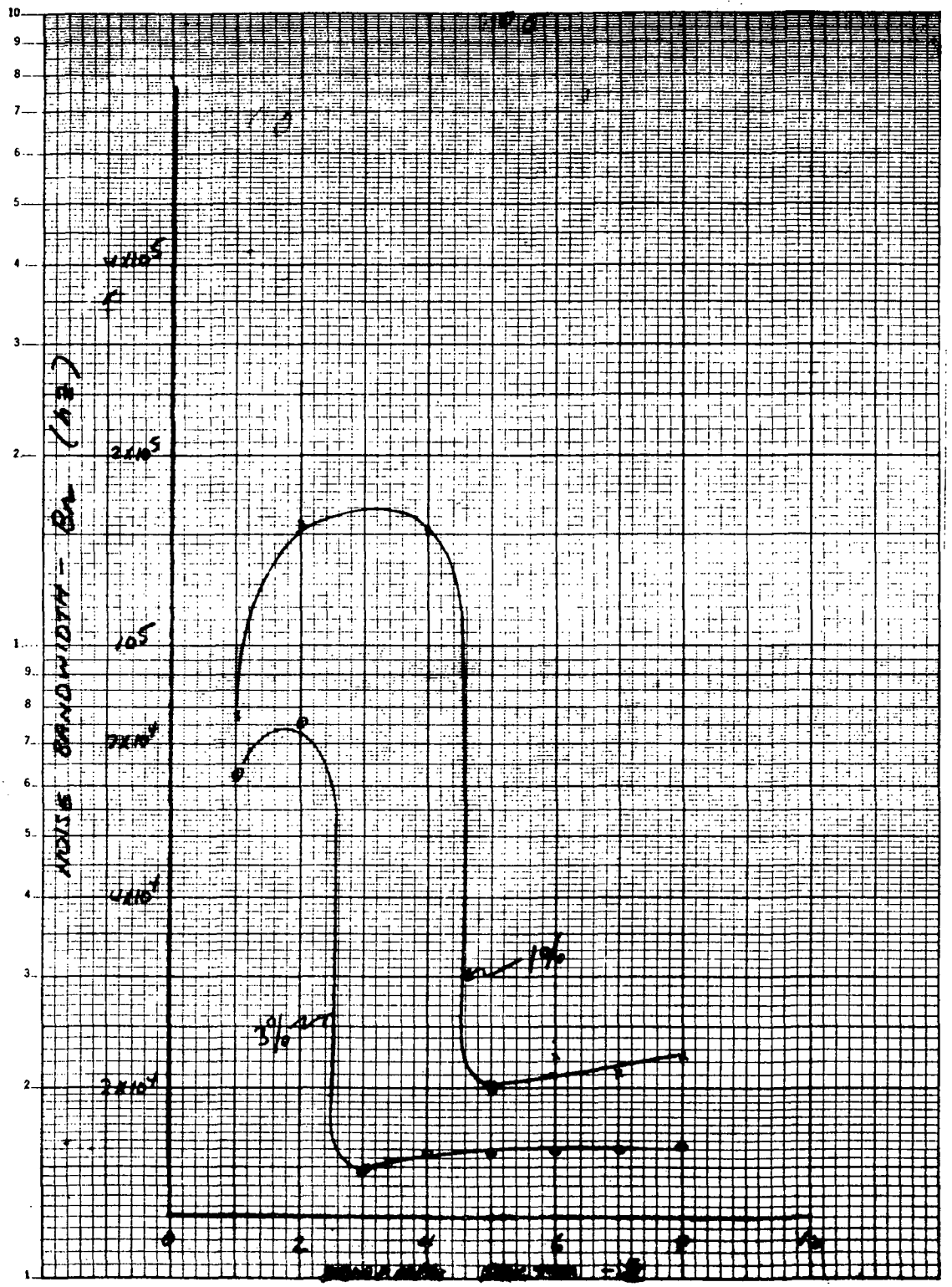


Figure 4-60. Locus of Points Satisfying Transient Accuracy for 100 Microsecond Settling Time

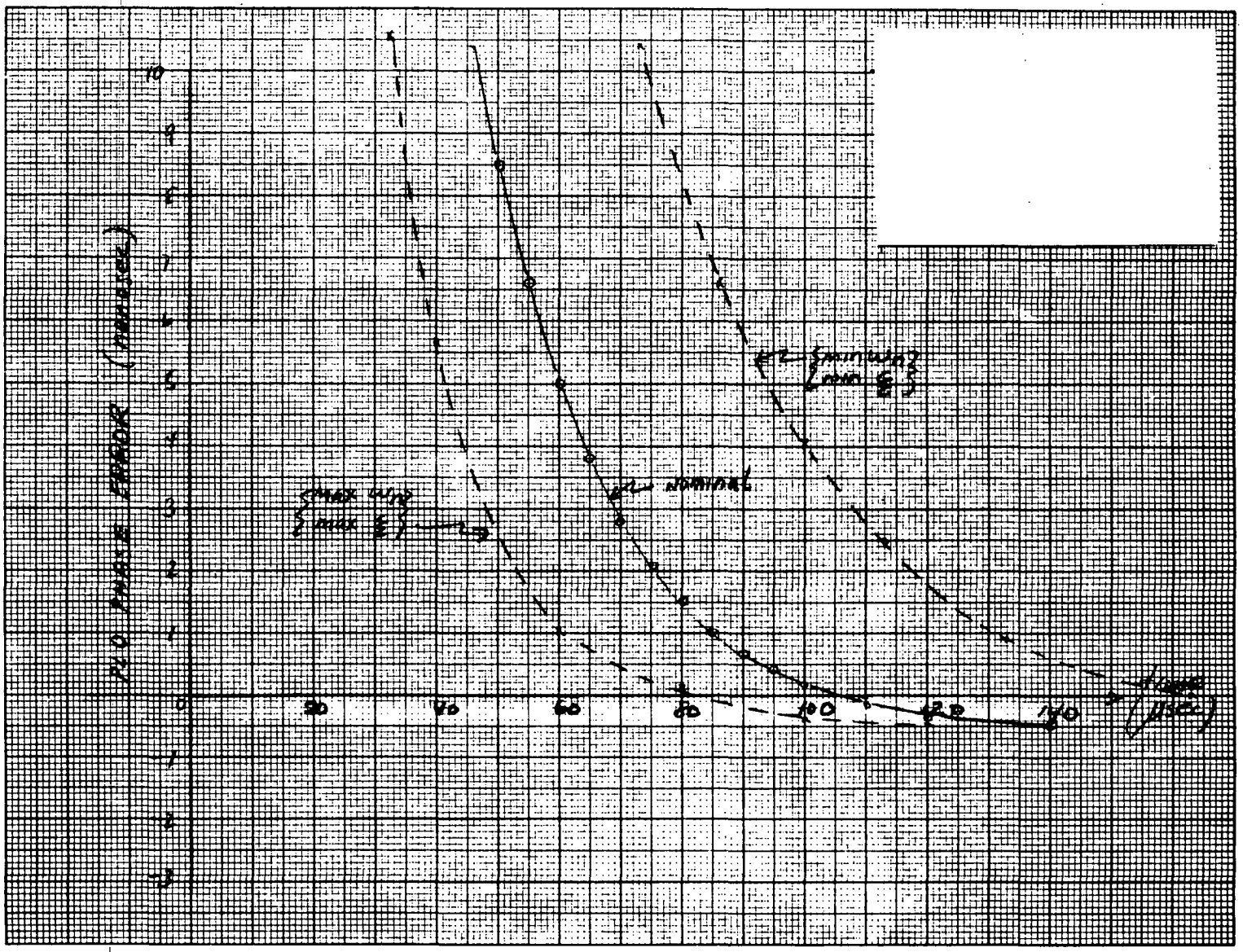


Figure 4-61. Transient Phase Error to a 100 Nanosecond Phase Discontinuity (Calculated)

It has been determined that a drift of 1.325% should be ascribed to the VCO (long term and temperature). Therefore, in order that the phase drift be held to within that which can be corrected by the third loop a bound on K_v is established. It is

$$K_v \geq \frac{\left(\frac{\Delta \omega_c}{\omega_c}\right)}{\Delta t}$$

choosing $\Delta t = 6$ ns, we have

$$K_v \geq \frac{0.01325}{6 \times 10^{-9}} = 2.2 \times 10^6$$

3. Low Frequency Accuracy. - The phase accuracy at low frequencies was found previously to be (see Paragraph 4.1.4.4.1.b)

$$\Delta t = T_f \left(\frac{\omega_f}{\omega_n}\right)^2$$

where

$$\omega_n = \left(\frac{K}{NT_1}\right)^{1/2}$$

The variable clock parameters yield

$$\Delta t = 2.5 \times 10^{-6} \left(\frac{10 \times 6.28}{4000}\right)^2 = \pm 0.615 \text{ ns}$$

therefore the selection of ω_n is compatible with the low frequency accuracy requirements.

4. PLO Transfer Function. - The PLO open and closed loop transfer functions are shown in Figure 4-62. A summary of the pertinent parameters utilizing the model of Appendix A is given below.

$T_1 = 0.153$ seconds

$T_2 = 0.003$ seconds

$K_V = 2.45 \times 10^6$

$\omega_n = 4000$ rad/s

$\xi = 6$

The pull in range is:

$$f_p \approx \frac{1}{2\pi} (4\xi KN\omega_n)^{1/2} \approx 770 \text{ kHz}$$

It is actually limited by the VCO swing to ±400 kHz.

Gain margin = 20 dB

Phase margin = 80°

4.1.4.5.2 Worst Case Analysis. -

a. Variable Clock Phase Stability. -

1. Pilot Tone Extraction Filter. - The nominal phase shift through the pilot tone extraction filter is zero degrees. Drift in the inductor or capacitor values will cause a change in the phase shift which will result in a phase inaccuracy in the variable clock output. The worst case phase shift was computed using a stability of ±1.5% for the inductors and 0.25% for the mica capacitors. The ECAP simulation indicated a worst case phase instability due to aging and temperature of ±6 ns due primarily to the three coils in the filter.

2. PLO Static Phase Stability. - The variable clock outputs are adjusted to the desired phase with respect to the data at system test. Drift of these settings will take place due to temperature and aging of the components in the PLO circuits. The relationship between the component drifts and the variable clock phase inaccuracy is developed here.

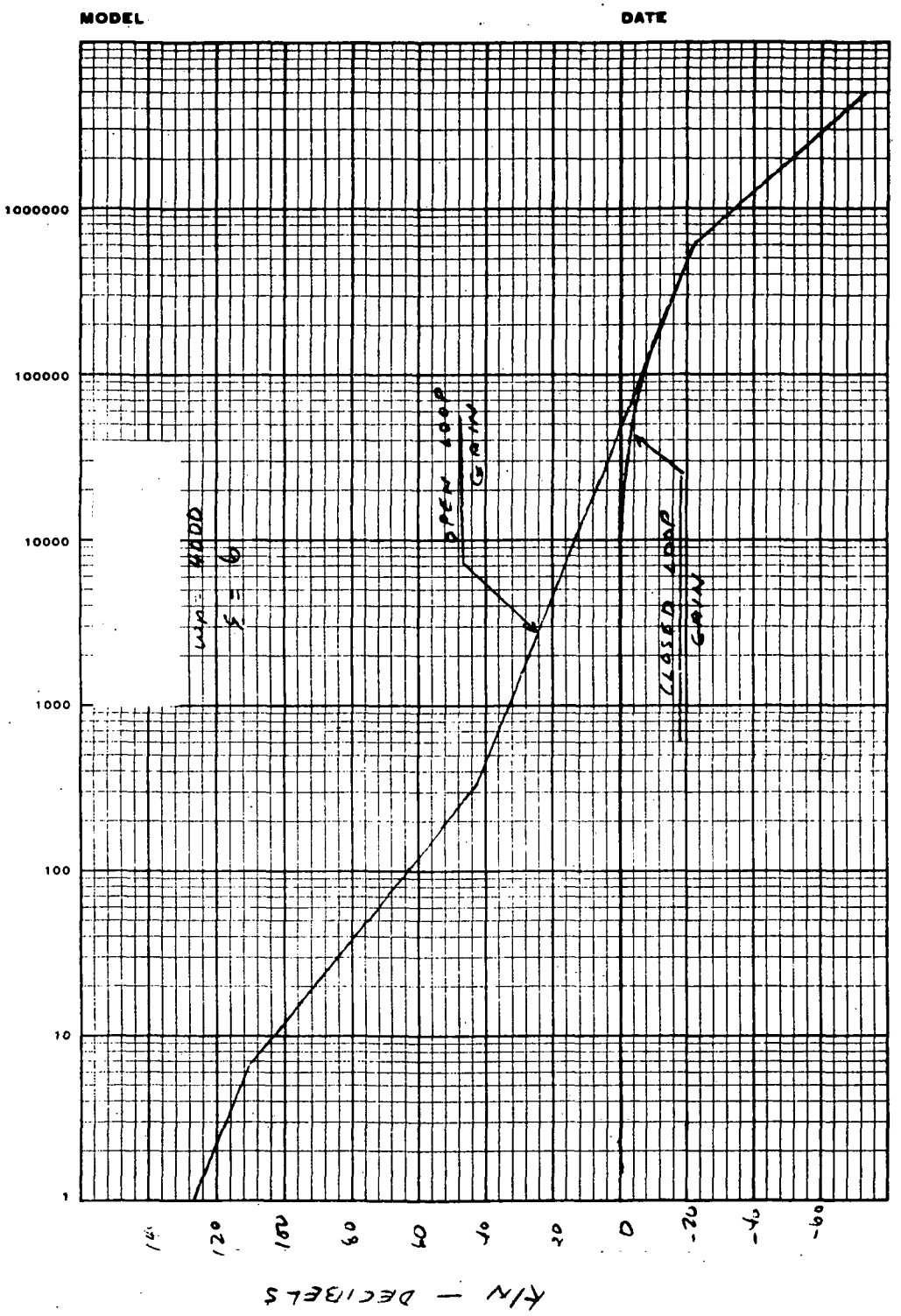


Figure 4-62. PLO Open and Closed Loop Transfer Functions

Let ω_o be the variable clock output frequency and ω_c the center frequency of the VCO. Using the model of Figure 4-63 we have:

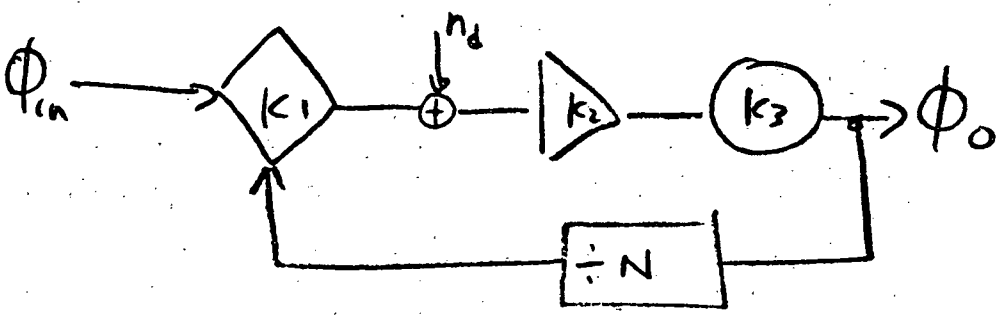


Figure 4-63. PLO Model

$$\omega_o = \omega_c + \Delta\omega_o = \frac{d\varphi_o}{dt}$$

but

$$\Delta\omega_o = \left(\varphi_{in} - \frac{\varphi_o}{N}\right) K + n_d K_2 K_3 + \Delta\omega_c$$

$$\therefore \omega_o = \omega_c + o\omega_c + \left(\varphi_{in} - \frac{\varphi_o}{N}\right) K + n_d K_2 K_3$$

$$\frac{d\varphi_o}{dt} + \varphi_o \frac{K}{N} = \omega_c + o\omega_c + \varphi_{in} K + n_d K_2 K_3$$

In the steady state $d\varphi_o/dt \rightarrow 0$ and ignoring the steady state phase we have

$$\Delta\varphi_o = \frac{\Delta\omega_c}{K/N} + \frac{n_d}{K_1/N}$$

but

$$\Delta\varphi_o = \omega_o t_d$$

where t_d is the timing error.

$$\therefore t_d = \left(\frac{\Delta\omega_c}{\omega_c}\right)\frac{N}{K} + \frac{n_d N}{\omega_c k_1}$$

Thus, the timing error drift is related to the component drift and broken down into that due to the VCO drift and that due to the PLO drift referred to the phase detector output.

Voltage Controlled Oscillator. - The VCO is a clapp oscillator using a varactor diode for frequency control. The oscillator has been extensively tested for reliable starting and frequency stability over the temperature range.

The transfer characteristics of the oscillator are shown in Figure 4-64. Curve A is the basic sensitivity characteristic. The sensitivity of the VCO varies over a considerable range and, at large negative input voltages, actually increases by a factor of 2 to 3. This increase in sensitivity reduces the Nyquist stability of the PLO and interferes with frequency lock. The addition of a diode shaping circuit alters the transfer characteristic to that shown in Curve B, eliminating the problem.

Drift of the VCO center frequency results in a compensating phase drift in the PLO. Also, the drift places restrictions on the PLO pull in range. For these reasons, the VCO drift must be minimized. Extensive temperature testing of the VCO indicates a worst case temperature drift of ± 0.35% over the ERTS temperature range. To this figure the aging characteristics of the frequency determining elements must be added. This is developed in Table 4-16.

TABLE 4-16. VCO WORST CASE DRIFT SUMMARY

Frequency Determining Element	Aging Tolerance (in %)	Resulting VCO Frequency Drift (in %)
Mica Capacitors	± 0.25	±0.1
Tubular Capacitors	±2	±0.125
Coil	±1.5	±0.75
Temperature		±0.35
Total		±1.325

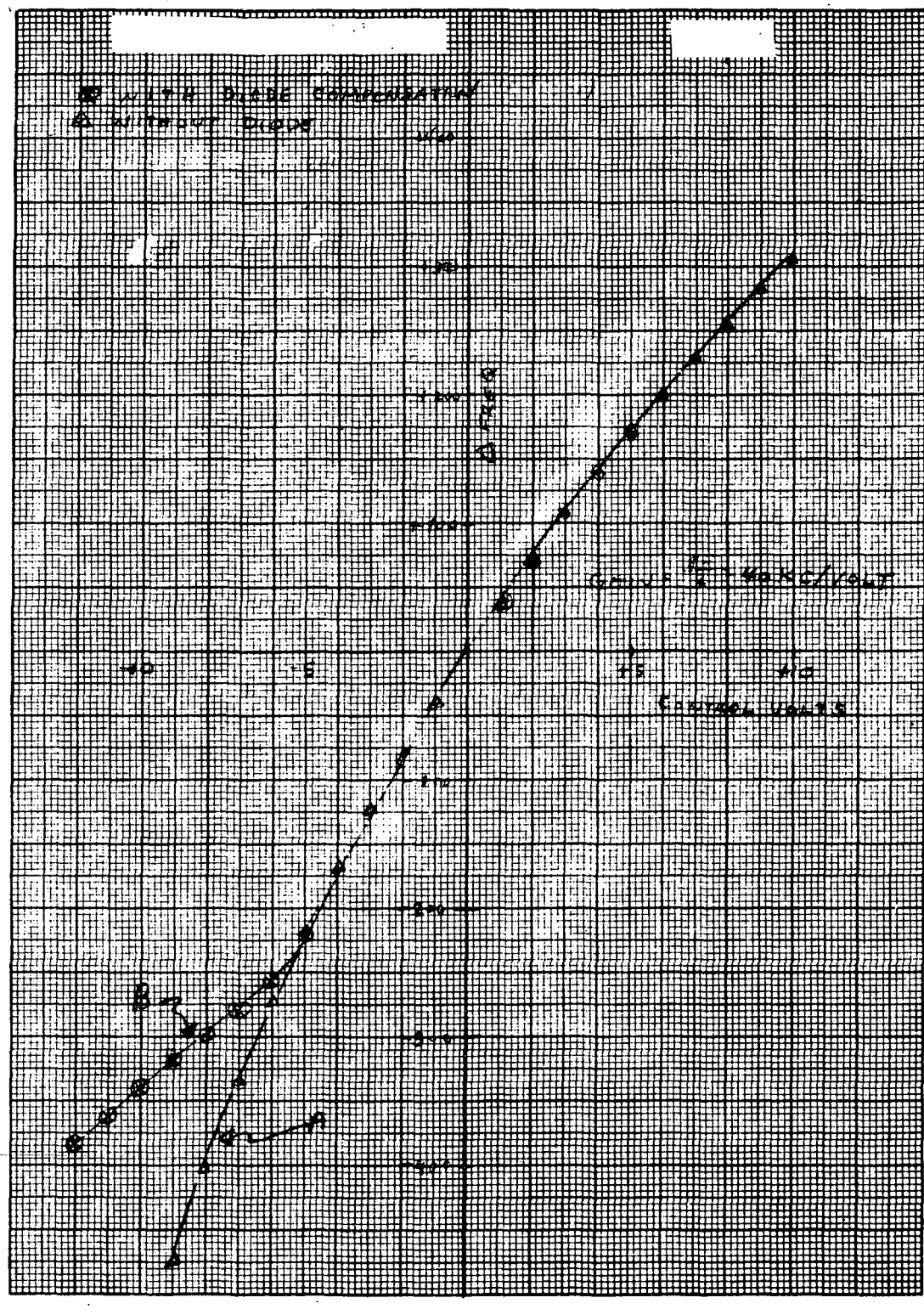


Figure 4-64. Oscillator Transfer Characteristics

PLO Drift. - The PLO long term drift including temperature is computed in a manner identical to that employed in the master clock. The four principle sources of drift are identified in Table 4-17.

TABLE 4-17. PLO WORST CASE DRIFT SUMMARY

Parameter	n_d (in mV)
Phase Detector Offset Current Temp coefficient (±180 nA/°C)	±1.7
Phase detector load resistor aging and temperature (±1.2%)	±15
Differential amplifier resistor aging and temperature	±1.75
Differential amplifier temperature coefficient of offset voltage (±20 mV/°C)	±0.6
Total	±19.1 mV

3. Summary Phase Drift. - The contributions of independent sources of variable clock phase uncertainty are tabulated in Table 4-18. Since these contributions are statistically independent and are themselves generally composed of several independent contributions, the rms phase uncertainty is probably a better measure of worst case phase uncertainty than the absolute sum of contributions. Both figures are included in the tabulation.

TABLE 4-18.

Source	Peak Phase Uncertainty Worst Case (in nanoseconds)
Phase Extraction Filter	±6.0
AM to PM Conversion	±0.5
Pilot tone noise	±2.13
Transient Error (120 usec.)	±1.5
Low Frequency Flutter Inaccuracy	±0.6
PLO Drift	±5.2
VCO Drift	±5.5
Total Absolute Worst Case	±21.4 nanoseconds
Total RMS Worst Case	±10.3 nanoseconds

b. Worst Case Transient Response. - Minimization of the PLO noise bandwidth implies that the PLO settling time is adjusted to the greatest that is tolerable. The worst case settling time is calculated so that the nominal values can be chosen with assurance that the worst case settling time does not exceed tolerable levels.

Transient response will change due to gain changes and time constant changes:

Loop Gain Changes - Initial tolerance and aging

Phase detector drive voltage -	±8%
Phase detector gain	±3%
DC Amplifier	±4%
DC Amplifier	±4%
VCO Sensitivity	±15%
Total	±34%

Time Constant Changes - Initial and aging

Resistors	each ±1.9%
Capacitor C	±15%

The above information can be used to calculate the changes in parameters ω_n and ξ. These are shown in Table 4-19 assuming nominal values of $\omega_n = 4000$, $\xi = 6$ and $K_V = 2.45 \times 10^6$

TABLE 4-19. TRANSIENT RESPONSE SUMMARY

Parameter	Nominal	Deviation	
		+	-
K_V	3.3×10^6	2.45×10^6	1.6×10^6
n	4950 rad/s.	4000 rad/s.	3040
6	7	ξ	5
1% settling time	60 ns	85 ns	131 ns.
B_n	34500 Hz	24000 Hz	15500 Hz
t_n (44 dB P/rms)	2.58	2.13 ns.	1.7 ns

It can be seen that the choice of the nominal values assures proper operation in the extreme worst case.

c. Frequency Lock. - The PLO must be designed so that frequency lock is achieved under all conditions.

For this calculation we assume the maximum VCO and PLO drifts and include the initial tolerances on the components. These are tabulated in Table 4-20.

TABLE 4-20. WORST CASE FREQUENCY LOCKS CONDITIONS

Source	VCO Δf (kHz)
VCO Drift	±200
PLO Drift	±180
Initial Tolerance	±330

The pull in range of the variable clock is ±400 kHz. With the addition of frequency offset due to initial tolerances, the sum of the frequency offsets exceeds the pull-in range. Therefore, correction of the initial offsets is necessary and has been provided with a potentiometer adjustment. The resulting sum worst case drift is less than the pull-in range.

4.1.4.6 Worst Case Analysis for Mater Clock, Variable Clock and Decoder Power Supply Regulator. - Worst case analyses of the series pass and shunt voltage regulators used on the Master Clock, Variable Clock and Decoder Boards are covered in this report.

A conventional series pass transistor regulator type is used to derive ±15 volts from the ±22 unregulated input voltage, with the exception of the +15 volts on the Master Clock. Shunt regulators are not used since zener diodes larger than one watt would be required. Further, the temperature coefficient of 15 volt zener diodes is much higher than zeners in the 6-8 volt range. Extremely tight voltage regulation is not considered necessary; therefore no voltage reference amplifiers are included in the regulators.

Shunt zener regulators are used for all five volt supplies and one +15 volt regulator; the regulation provided is considered adequate for the circuitry involved.

4.1.4.6.1 15 Volt Series Regulator Worst Case Analysis. -

Introduction. - The 15 volt regulator of Figure 4-65 is used to derive +15 or -15 volts from the +22 volt and -22 volt system supplies. Each regulator consists of two zener diodes, series connected, as a voltage reference source for the base of the series pass transistor Q. Quiescent current for the zener reference is derived by connecting a resistor R_B to the 22 volt unregulated input. A second resistor, R_C, is used in series with the collector of Q to reduce dissipation in Q.

1. Design Considerations. - The same basic regulator is used for both +15 volts and -15 volts; a 2N2219A is used for the +15 volt series pass transistor and a 2N2905A for the -15 volt regulator. Two zener diodes are used in series as the voltage reference to minimize the voltage temperature coefficient. The 2N2219A and 2N2905A are high beta transistors to minimize the effects of current changes in the zener reference due to base current changes.

2. Summary. - The worst case analyses include worst case dissipations of Q, R_C, R_B, CR1, and CR2 since these are the limiting items.

b. Worst Case Analysis. - A typical schematic is shown in Figure 4-65. All parameters of interest are indicated by two values separated by a bar, the upper value being the maximum and the lower the minimum. All limits include the worst combination of aging, temperature and tolerances. Specifically, the limits for V_L include temperature variations of $^{+0.22}_{-0.35}$ volt.

Maximum dissipation in R_B must be less than 125 mW and will occur when the reference voltage is a minimum, V_{IN} is a maximum and R_B is minimum (assuming I_b negligible)

$$\overline{I} = \frac{\overline{V}_{IN} - V_{Z1} + V_{Z2}}{R_B} = \frac{23 - 13.9}{800} = \frac{9.1}{800} = 11.4 \text{ mA}$$

$$P_{RB} = (11.4)^2 \times 10^{-6} \times 8 \times 10^2 = 103 \text{ mW} < 125 \text{ mW}$$

which checks.

CR2 is limited to a dissipation of 200 mW under the same conditions, while the dissipation of CR1 may be 250 mW.

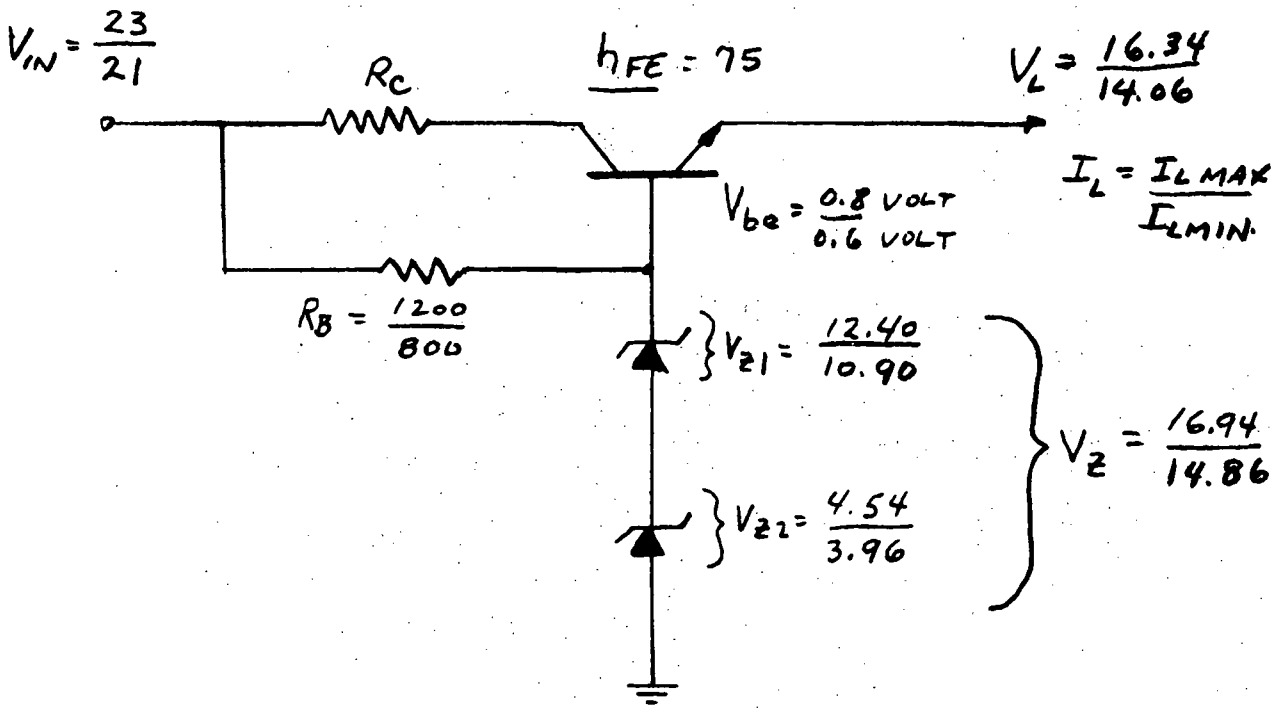


Figure 4-65. 15 Volt Series Regulator Schematic Diagram

$$\overline{P_{CR1}} = \overline{I}\ V_{\underline{Z1}} = 11.4 \times 10^{-3} \times 10.66 = 121\ mW < 250\ mW$$

$$\overline{P_{CR2}} = \overline{I}\ V_{\underline{Z2}} = 11.4 \times 10^{-3} \times 3.19 = 36\ mW < 200\ mW$$

The dissipation in R_C and Q has been calculated for the specific values of $\overline{I}_L$ and $I_{\underline{L}}$ and R_C used on each module, as tabulated in Table 4-21. All stress values are within the required limits.

TABLE 4-21. SERIES REGULATOR DISSIPATION

Module and Voltage	R_C(tol) Ohms	R_C(type)	$\overline{I}_L$ (mA)	$I_{\underline{L}}$ (mA)	$\overline{P}_Q$(mW)	$\overline{P}_{RC}$(mW)
Decoder +15		Not Used				
-15	90 74	RLR07	27	14	215	66
Variable Clock +15	75 61	RLR20	28	14	230	59
-15	110 90	RLR07	9	3	82	9

TABLE 4-21. SERIES REGULATOR DISSIPATION (Continued)

Module and Voltage	R_C(tol) Ohms	R_C(type)	$\overline{I_L}$ (mA)	I_L (mA)	$\overline{P_Q}$(mW)	$\overline{P_{RC}}$(mW)
Master Clock +15			Not Used			
-15(C)	69 55	RLR20	25	20	212	43
-15(D)	75 61	RLR20	30	20	243	68

Maximum dissipation in Q occurs when V_L and R_C are minimum and I_L and V_{IN} are maximum.

The voltage across R_C under these conditions is

$$V_{RC} = \overline{I}_L R_{\underline{C}}$$

The collector to emitter voltage of Q is then:

$$\overline{V}_{CE} = \overline{V}_{IN} - V_{RC} - V_{\underline{L}}$$

$$\overline{P}_Q = \overline{V}_{CE}\,\overline{I}_L$$

Maximum dissipation in R_C occurs for $\overline{I}_L$ and $\overline{R_C}$ as noted in the table.

The maximum value of R_C is a function of $V_{\underline{IN}}$, $\overline{V_L}$, $\overline{I_L}$, and $V_{\underline{CE}}$ as follows.

$$V_{\underline{IN}} - \overline{I_L}\,\overline{R_C} - V_{\underline{CE}} - \overline{V_L} = 0$$

$$\overline{R_C} = \frac{V_{\underline{CE}} + \overline{V_L} - V_{\underline{IN}}}{\overline{I_L}}$$

Using the appropriate values of $V_{\underline{IN}}$, $V_{\underline{CE}}$, and $\overline{V_L}$

$$21 - \overline{I}_L\overline{R_C} - 1.5 - 16.2 = V_{\underline{IN}} - \overline{I_L}\,\overline{R_C} - V_{\underline{CE}} - \overline{V_L}$$

or

$$\overline{I_L}\,\overline{R_C} = 3.3,$$

and

$$\overline{R_C} = \frac{3.3}{\overline{I_L}}$$

For the Decoder -15 V Regulator,

$$\overline{R_C} = \frac{3.3 \times 10^3}{27} = 122 > 90$$

For the Variable Clock +15 V Regulator,

$$\overline{R_C} = \frac{3.3 \times 10^3}{28} = 177 > 75$$

For the Variable Clock -15 V Regulator,

$$\overline{R_C} = \frac{3.3}{9} = 366 > 110$$

and for the Master Clock (-15 Regulators),

$$-15(C);\ \overline{R_C} = \frac{3.3}{25} = 132 > 69$$

$$-15(D);\ \overline{R_C} = \frac{3.3}{30} = 110 > 75$$

All values check for the inequality shown.

4.1.4.6.2 5 Volt Shunt Regulator. -

a. Introduction. - The +5 volt and -5 volt supplies are derived from the +8 volt and -8 volt system supplies. Total power requirements are small enough to allow the use of a less complicated shunt regulator rather than a series transistor type used in the ±15 volt supplies.

1. Design Considerations. - A schematic of a typical regulator is shown in Figure 4-66 along with maximum and minimum parameter values. R_S, V_L and I_L values are a function of a specific regulator design.

   Worst case design requires that two sets of conditions be met. One condition is that the zener diode current never be zero. Another is that all components be within the maximum power ratings required for reliability. Since maximum power dissipation is involved in the calculations the design problem could not be handled by ECAP analysis. However, a FORTRAN program was written which performed calculations for the nine shunt regulators involved in the three board types. A flow chart of this program is presented in Figure 4-67. A summary of critical regulator parameters is shown in Table 4-22.

2. Summary. - *Worst case analysis was performed to determine* minimum zener current, maximum dissipation in R_S and the zener diode and maximum and minimum load voltage V_L.

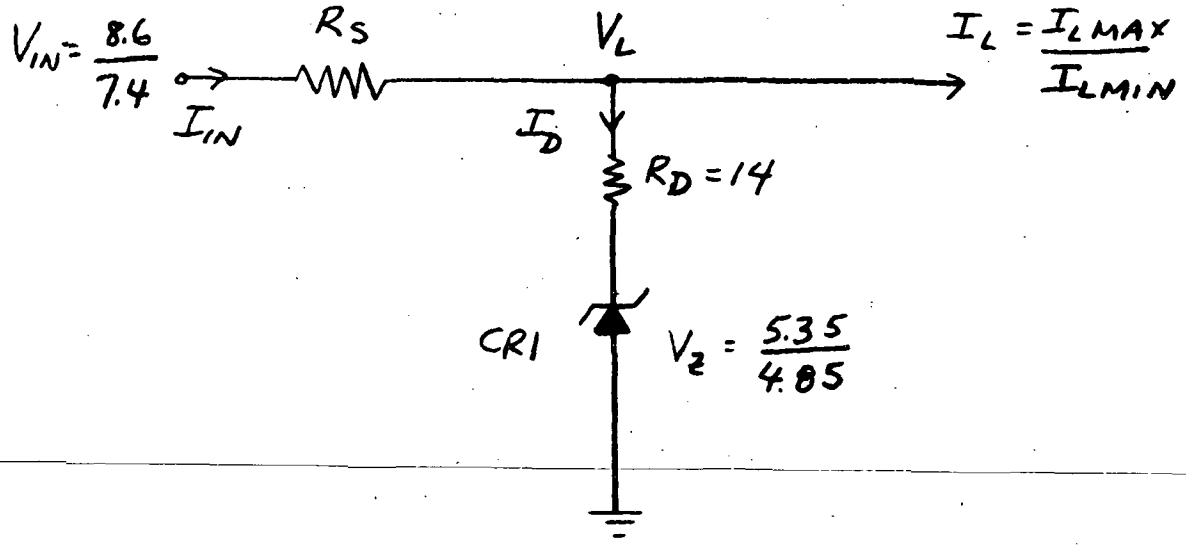


Figure 4-66. 5 Volt Regulator Equivalent Circuit

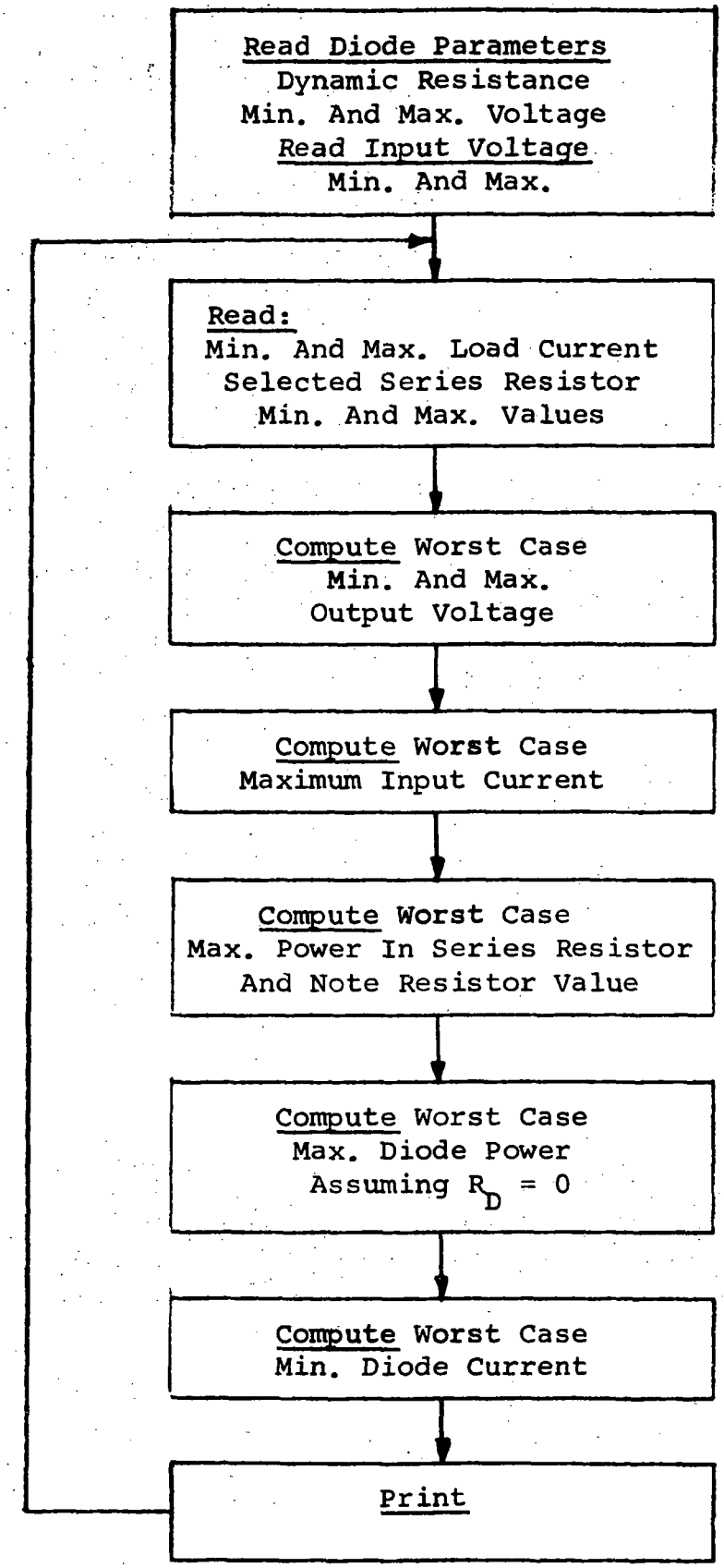


Figure 4-67. Flow Chart, Regulator Analysis Program

TABLE 4-22. SHUNT REGULATOR DISSIPATION

Module	R_S Ohms	R_S(type)	Rating (mW)	I_D	$\overline{I_C}$	I_C	$\overline{P_D}$	P_D Rated	$\overline{P_{RS}}$
Decoder +5A	90 73	RLR20	250	2	22	13	224	500	159
-5	90 73	RLR20	250	3	18	15	222	500	157
-5A	62 50	RLR20	250	3	30	16	330	500	212
Variable Clock +5	56 46	RLR32	500	14	23	11	366	500	212
-5	110 90	RLR20	250	7	12	5	187	500	127
Master Clock +5A	90 73	RLR20	250	3	20	15	222	500	157
+5B	90 73	RLR20	250	1	23	13	224	500	159
-5	90 73	RLR20	250	3	20	12	225	500	157

4.1.4.6.3 +15 Volt Shunt Regulator

a. Introduction. - This regulator is used to supply load currents of 3 to 9 mA on the Master Clock board at +15 volts which is derived from the +22 volt system voltage. The small amount of current required permitted the use of a shunt regulator rather than a more complicated series regulator.

1. Design Considerations. - The regulator uses a series resistor and a series combination of a 1N749A and a 1N941B as the regulator elements. These diodes are also used as a reference in the 15 volt series regulators. The equivalent schematic is shown in Figure 4-68.

Worst case dissipation of components was calculated by modifying the program used for the 5 volt shunt regulator design. Worst case power for R_S = 430 ohms nominal is 190 milliwatts. R_S is a type RLR32 with a rating of 500 milliwatts.

Maximum dissipation in the composite zener diode is 265 milliwatts at a diode voltage of 14. Subtracting the minimum voltage of the 1N749A from 14 volts gives a maximum value of the 1N941B voltage as 10.7. The 1N941B dissipation is then 19 x 10.7 = 204 milliwatts and the 1N749A dissipation is 61 milliwatts.

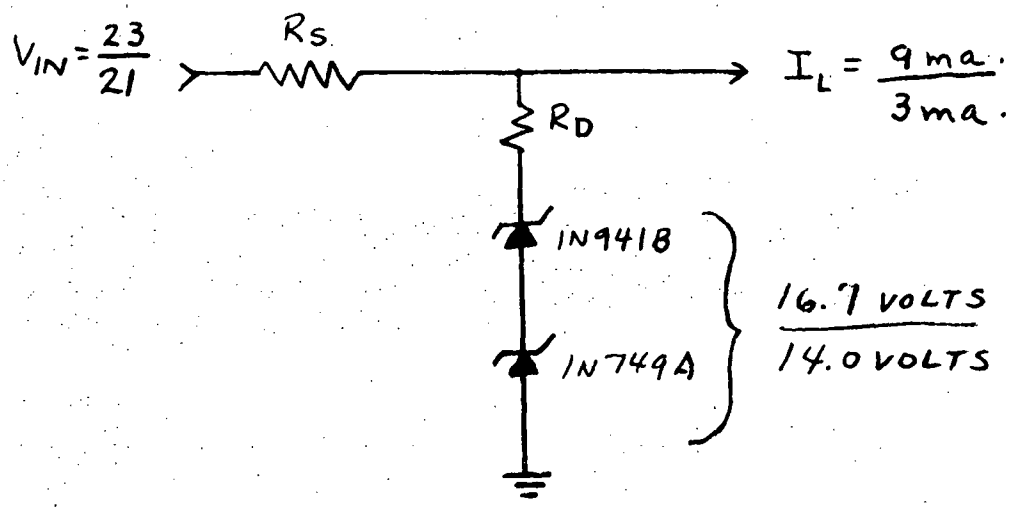


Figure 4-68. +15 Volt Shunt Regulator

4.2 Narrowband Channels

The design of the narrowband channels has not changed materially since the definition of the original performance specifications. However the specific uses and detailed formats have recently been identified. The paragraphs that follow delineate the final system configurations and uses.

4.2.1 Auxiliary Track. - This channel will now be used to record a 1 kb digital data encoded in a split phase format. For this reason it has been decided to ac couple the input and output amplifiers of the system, thus eliminating any danger of accumulating dc drifts that might be present in the record/playback system. Some slight changes in signal levels/impedances were also incurred, which would enhance system compatibility. (See Figure 4-69.)

The Auxiliary Channel amplifier is a linear channel using an FM carrier system. The input signal at a level of 6.0 volts peak-to-peak is ac coupled through an emitter follower to the frequency deviable multivibrator, which has a nominal frequency set at 32 kHz. A signal level of +3.0 V will decrease the frequency to 22 kHz, while a level of -3.0 V will increase the frequency to 42 kHz.

The output of the multivibrator is coupled through an emitter follower to an IC flip-flop which divides the frequency of the signal in half and insures a symmetrical square wave output. This square wave is applied to an amplifier and gating circuit which controls the bi-directional recording current of +2 mA, -2 mA which is applied to the head. The current drives the head into magnetic saturation in both directions on alternate cycles so as to erase any previous magnetization history and provide new recorded information.

The signal thus generated is then transmitted to the Transport Unit. The purpose of the auxiliary channel preamplifier is to switch the auxiliary head to its record amplifier when the circuits is in the record mode, and to the preamplifier when in the playback mode. The preamplifier proper amplifies the playback signal from the head sufficiently for retransmittal to the Electronic Unit. The amplifier bandwidth is also adjusted to minimize spurious noises that may be coupled into this channel. The preamplifier circuit was reviewed in the Design Study Report, Vol. 1.

The Auxiliary Channel playback circuit comprises subassembly A8 of the Electronics Unit. (See Figure 4-70.) The signal from the preamp with a level of 0.5 to 2.0 V peak-to-peak is applied to a two stage limiter with 50 to 60 dB of limiting. The two phased outputs of the limiting circuit, operating at a nominal frequency of 16 kHz, is applied to two inputs of an IC one shot multivibrator whose output pulse width is approximately 10.6 us at twice the frequency. The fixed pulse with signal frequency varying at the information rate, is dc coupled through RC filters and two IC operational amplifiers to retrieve the modulating signal at a 1.5 V peak-to-peak signal level. The external load is ac coupled to eliminate possible dc signal drifts.

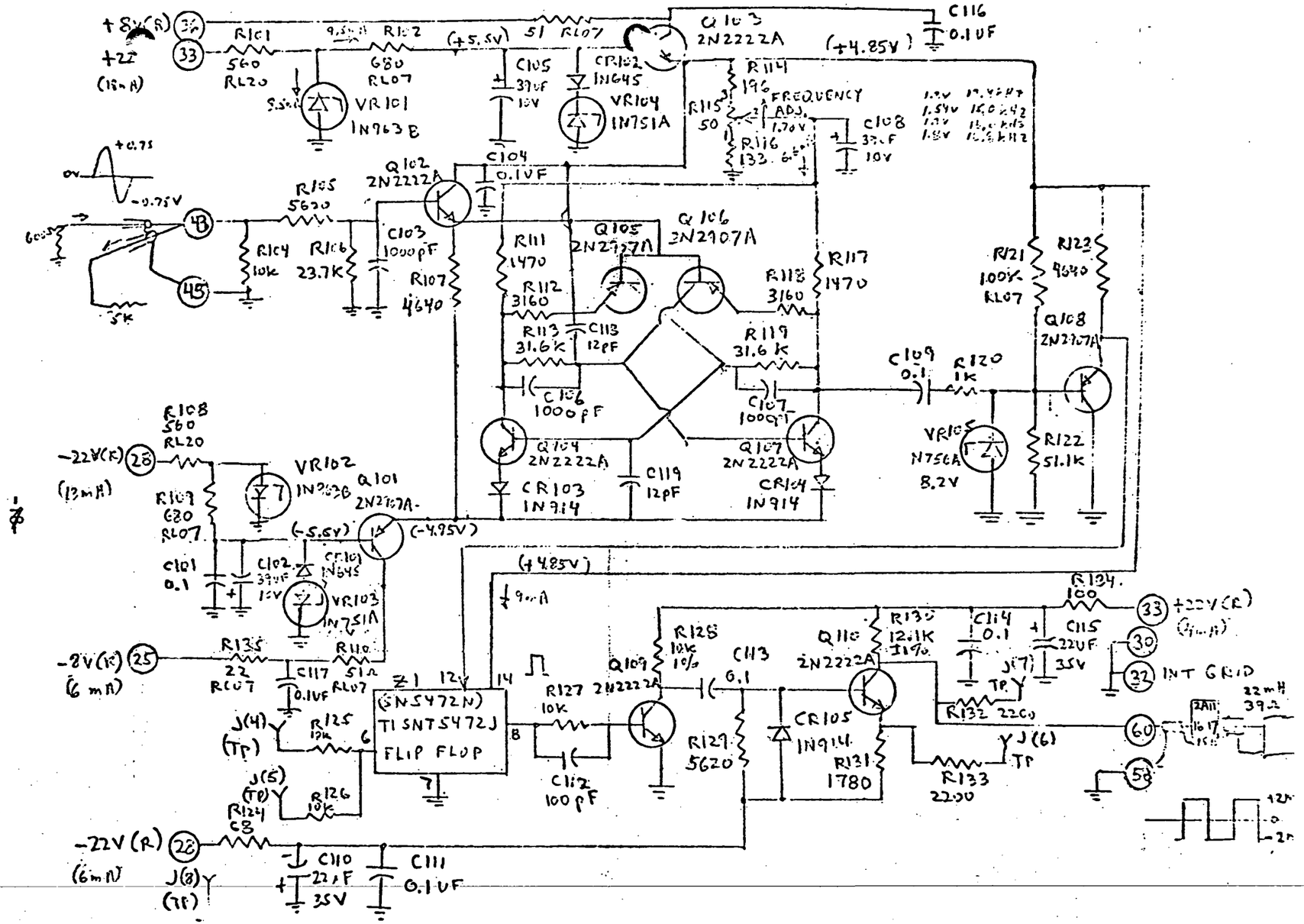


Figure 4-69. Auxiliary Channel (Record)

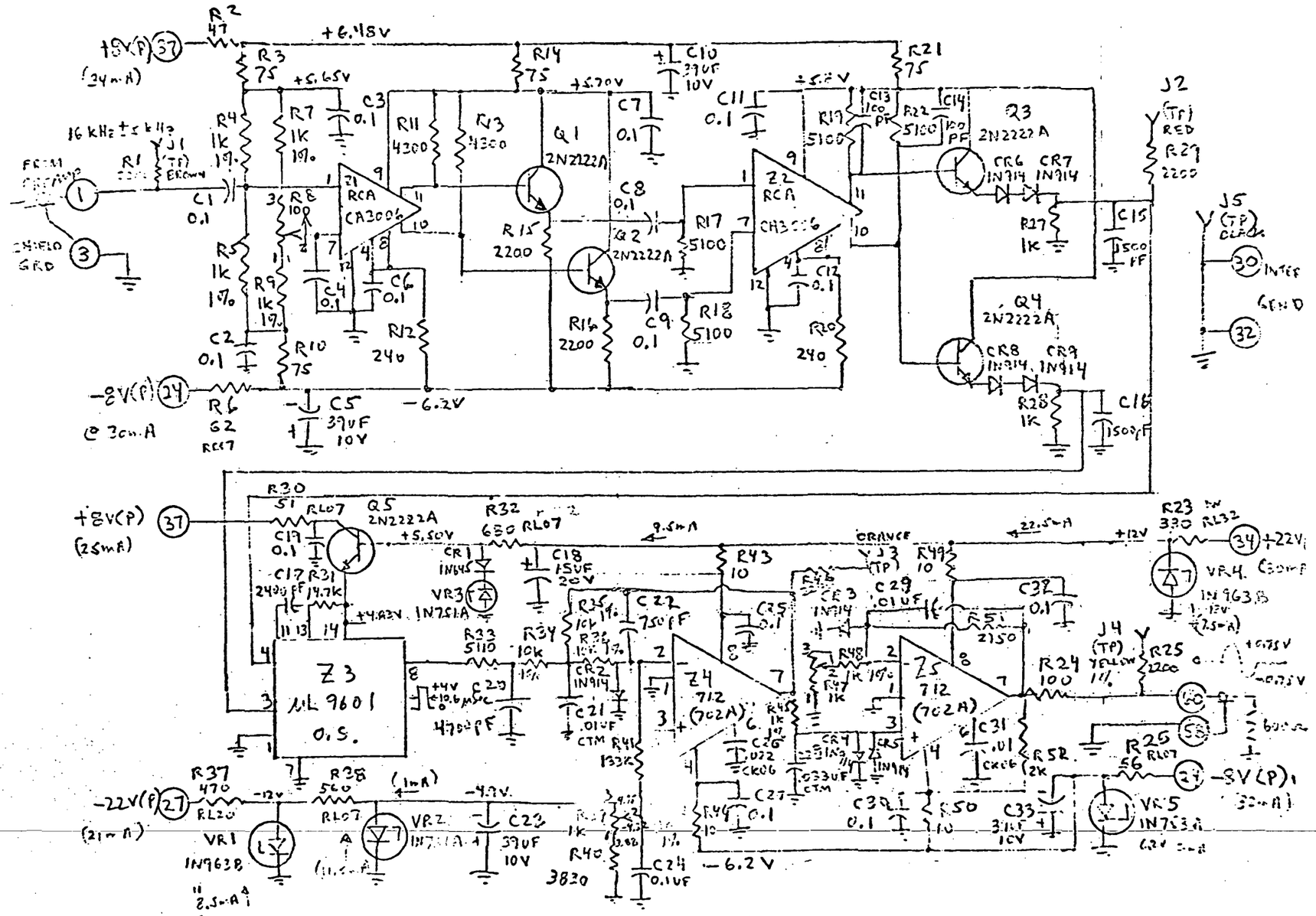
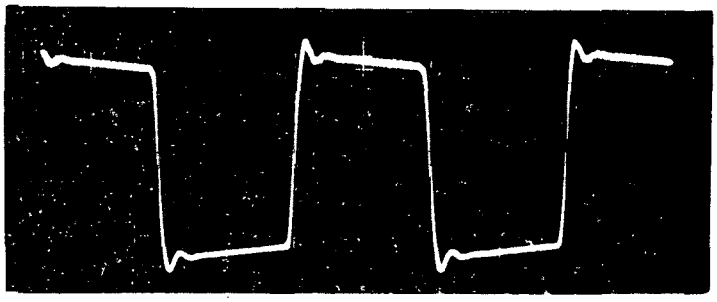


Figure 4-70. Auxiliary Channel (Playback)

Since the Auxiliary Channel will be used exclusively for digital signals, it is planned to test this channel with typical signals. It should, however, be re-emphasized that this channel is basically an analog channel and thus contains no re-clocking or re-generating facilities. Therefore, any deviations in the input signal will be correspondingly reproduced in the output signal. Digital signal circuit performance is shown in Figure 4-71.

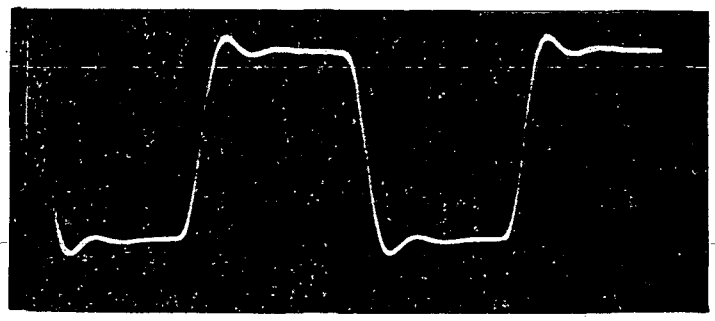
4.2.2 Search Track. - The purpose of the Search Track is to permit the location of the tape within the recorder system.

The design of the Search Track playback circuit is based on two pre-recorded tracks, one carrying logical 1's and the adjacent track carrying logical 0's. A pulse repetition rate of 1000 bps has been determined for the ERTS recorder system when operating at low tape speed. The output signal will be in form of a three level RZ format to allow self-clocking of the intermittent data when operating at both speeds. The word format will be a binary coded decimal word repeated in a mirror image so that simple decoding equipment can be designed that will identify the location of the tape irrespective of the direction of tape motion. A 15 bit word (30 bit total) is used so that an unambiguous word can be recorded at every six inches of tape length. A detailed description of the coding and word format is given in Figures 4-72 and 4-73.



V = 0.5 V/cm
H = 500 s/cm

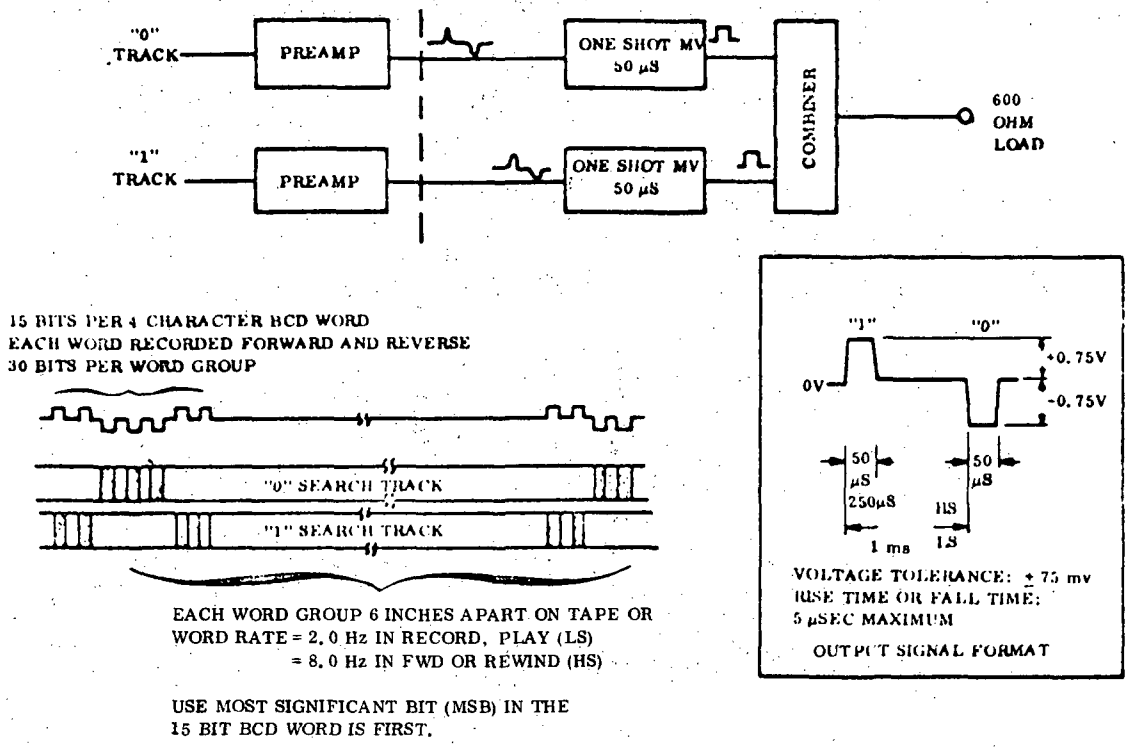
500 Hz SQUARE WAVE



V = 0.5 V/cm
H = 200 s/cm

1 KHz SQUARE WAVE

Figure 4-71. Auxiliary Track Circuit Performance (Back to Back)



a. Coding

BCD	
1	000000000000011000000000000000
2	000000000000010010000000000000
3	000000000000011110000000000000
4	000000000001000010000000000000
5	000000000001011010000000000000
6	000000000001100110000000000000
7	000000000001111110000000000000
8	000000000010000010000000000000
9	000000000010011001000000000000
10	000000000010000000010000000000
11	000000000010001100010000000000
.	
200	000001000000000000000000100000
.	
5999	101100110011001100110011001101

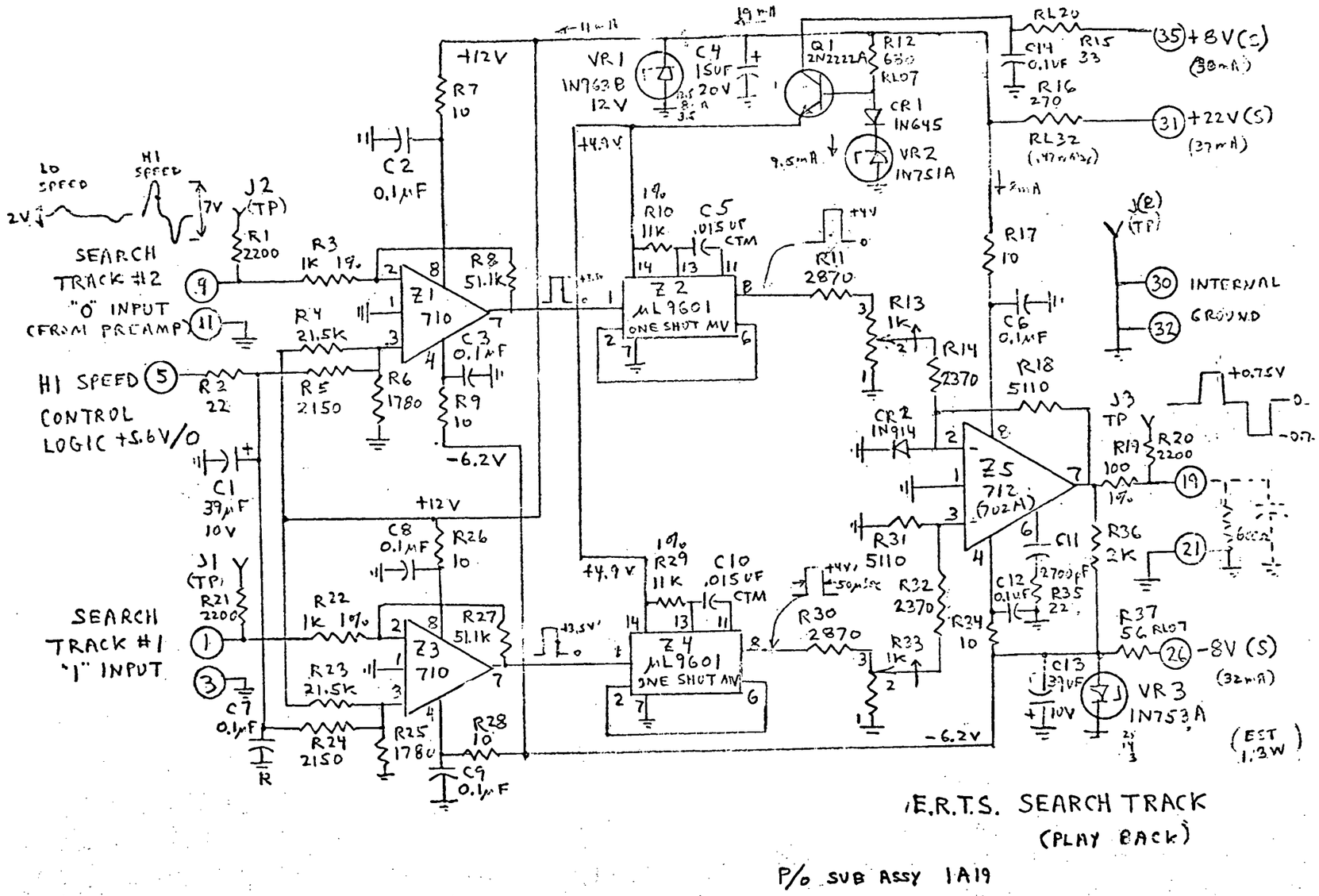
NOTES

1. Low BCD numbers will appear near the beginning of tape. High BCD numbers will appear near end of tape.

2. BCD No. 1 will occur ahead of the secondary beginning of tape. Thus, under normal operating conditions, the BCD code will start at some low BCD number other than 1.

b. Format

Figure 4-72. Coding and Format



E.R.T.S. SEARCH TRACK (PLAY BACK)

P/O SUB ASSY 1A19

Figure 4-73. Search Track System Schematic Diagram

The playback signals derived from the magnetic heads are amplified in two preamplifiers. Here the signals are band limited to minimize noise interference and amplified for transmission from the Transport Unit to the Electronic Unit.

The playback signal pulses are then applied to two one-shot multivibrators set for 50 us duration pulses. The outputs of the 1's track one-shot and the 0's track one-shot are combined to obtain an output which is a 1.5 V peak-to-peak, three level RZ format.

4.2.3 Auxiliary Track Worst Case Analysis. -

NOTE: This analysis was made on the subsystem shown in Figures 4-69 and 4-70, which has since been redesigned to incorporate dc coupling. Although the results of the analysis are still generally applicable, values given here may differ from those in Paragraph 4.2.1.

The auxiliary track subsystem in the recording equipment consists of the following functions: (a) FM Modulator; (b) Head Driver; (c) Playback Preamplifier; (d) FM Limiter; (e) FM Discriminator; and (f) Output Filter Amplifier. Each of these functions, plus the supporting power supply regulator filters, etc. are an integral part of the two subassemblies comprising the subsystem. The analysis of the input and the output circuits was made in reference to the functional diagram (Figure 4-74).

The main task of the analysis, using the criteria of Appendix H, was to show that the auxiliary track circuits will satisfy the performance requirements, which are summarized in Table 4-23.

4.2.3.1 Record Assembly Analysis

a. Auxiliary Track Input Buffer (Q102). - The purpose of this stage (Figure 4-75) is to provide a high input impedance to the input line and to supply a signal drive to the FM modulator.

Assuming $\underline{B} \geq 50$

Input impedance at the base of Q2

$$Z_{iQ2} = 4.64\text{k ohms}\,(1+\underline{B}) \cong 235\text{k ohms}$$

$$Z_{in} = R_4 \,||\, (R_5+R_6) \,||\, Z_{iQ2}$$

$$= \frac{10\,(5.62+21.5)}{37.12} = 7.3\text{k ohms}$$

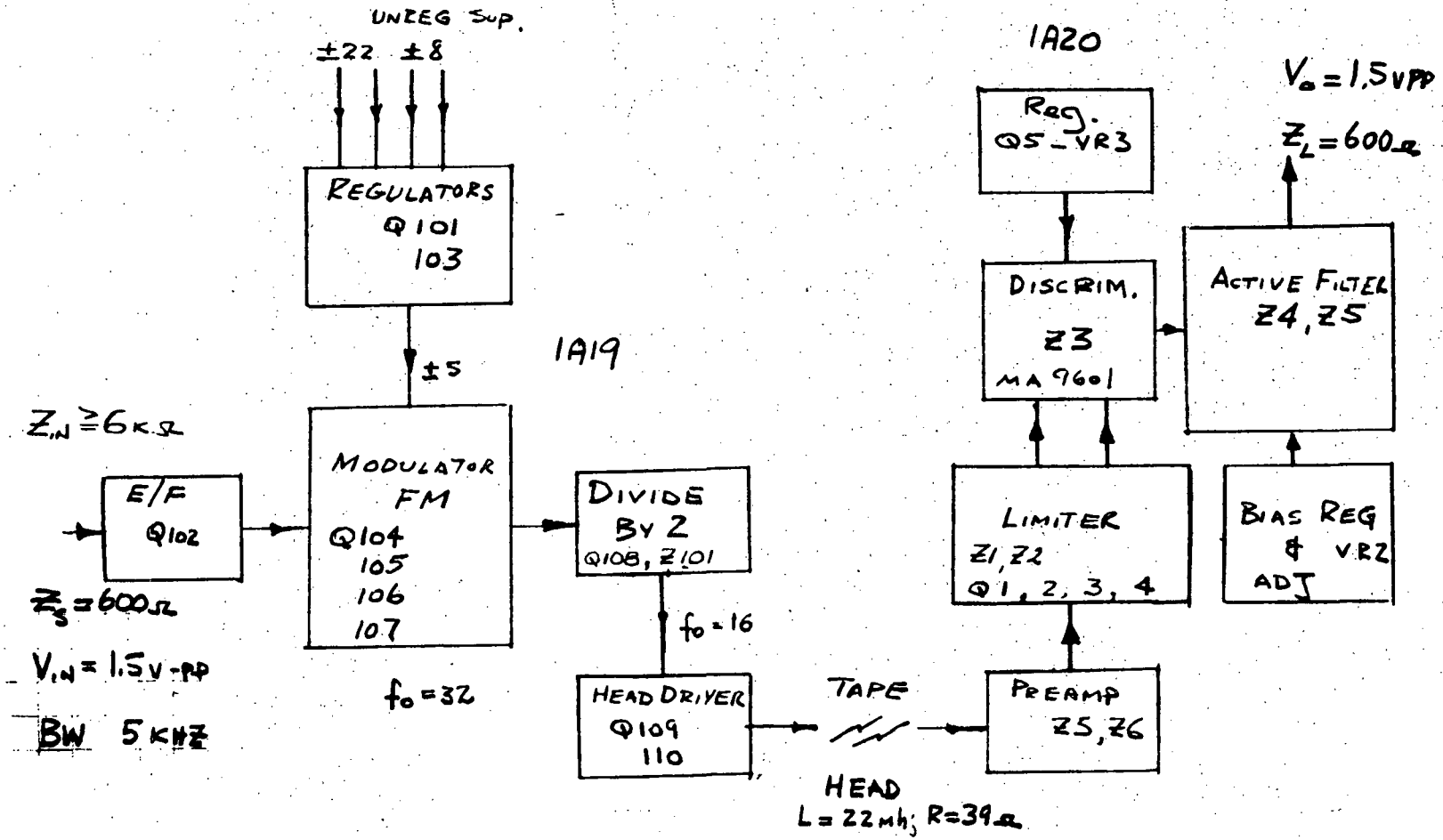


Figure 4-74. Auxiliary Track Subsystem Functional Diagram

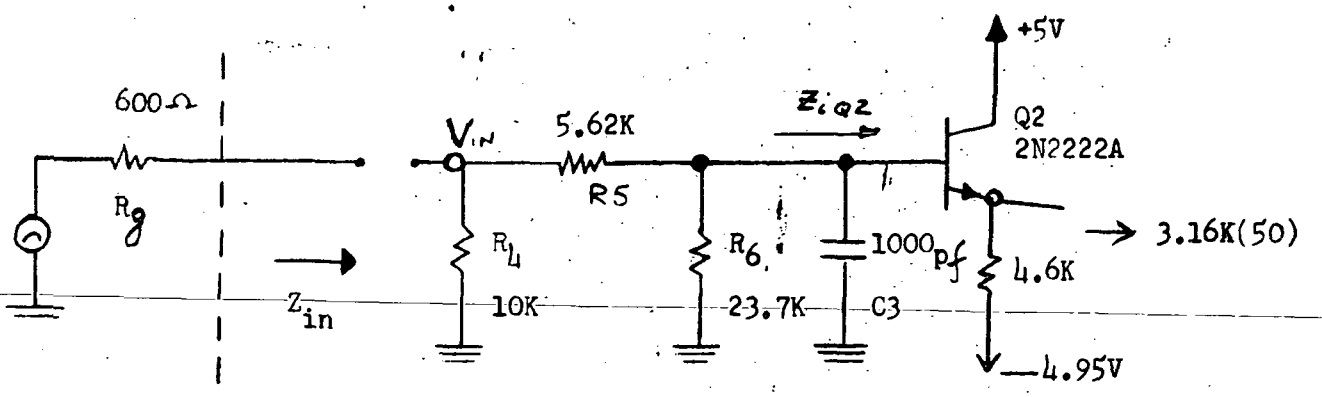
TABLE 4-23. AUXILIARY TRACK PERFORMANCE SUMMARY

Parameter	Specified Value	Calculated Value	Measured Value
Input Impedance	6 k (min.)	7.3 k (min.)	---
Input Amplitude (Z_S = 600)	1.5 V pp (max.)	1.5 V pp (max.)	1.5 V pp
Signal (BW)	5 kHz (max.)	5.1 kHz	5.0 kHz
FM Carrier (Nom.)	---	15.9 kHz	16.0 kHz (adj.)
Carrier Deviation	---	±5.5 kHz	±5 kHz
Worst Case Drift (Input to Output)		±203 mV	

Thus, if the available open circuit source signal is 1.5 V pp, the resulting input

$$V_{in} = \frac{1.5\ (7.3)}{0.6 + 7.3} = 1.39 \text{ V pp.}$$

The loading does not constitute any difficulties because the FM modulator was designed to absorb effects of nominal loading. The worst case load variations are primarily those of R_4, R_5 and R_6, all RNR55C type with a combined EOL tolerance of 0.24 ±0.175% which will contribute a negligible drift in the overall consideration of the Auxiliary Channel output.



Note: Reference designators have been reduced by 100.

Figure 4-75. Input Buffer Circuit

Capacitor C3 is used to filter out an occasional high frequency disturbance. The effective pole which it introduces in conjunction with the resistive components of source resistance R_g, R_4, R_5 and R_6 is at:

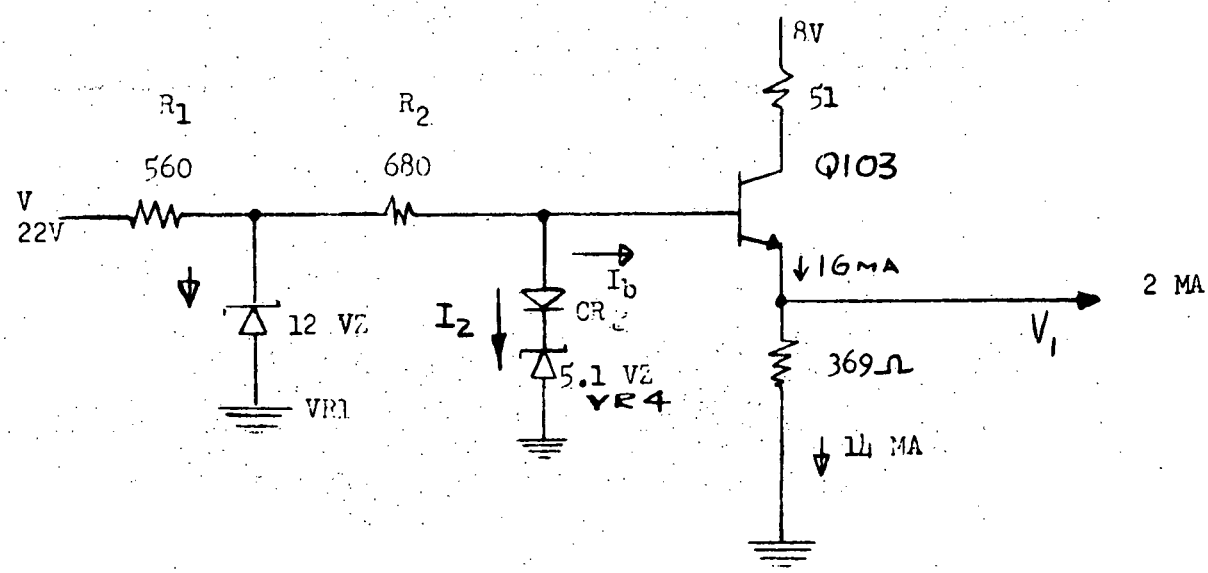
$$f = \frac{1}{2\pi \text{Reg. } C_3} = \frac{1}{2\pi (R_4 // R_g + R_5) C_3}$$

$$= \frac{1}{2\pi (5.2)\, 10^3 (10^{-9})} \cong 30 \text{ kHz}$$

Which is sufficiently beyond the required high frequency response of the Auxiliary Channel.

b. Power Supply Regulators (Q103, Q101). - The two power supply regulators are identical in design, except for output polarity; therefore, only Q103 shall be considered (see Figure 4-76).

$$\therefore \bar{I}_b = \frac{16 \text{ mA}}{(\underline{B} + 1)} = 0.32 \text{ mA} \quad \text{For } \underline{B} = 50$$



Note: Reference designators have been reduced by 100.

Figure 4-76. Power Supply Regulator

Input to reference diode VR4 is preregulated by the 12 Vdc VR1; thus, the worst case current through the VR4 branch can be calculated as follows:

$$I_2 = \frac{V_{R1} - V_{R4} - V_{CR2}}{R_2} - Ib$$

If

$$\overline{B} = 150$$

$$I_2 = \frac{(12.6 - 4.85 - 0.6)}{0.68\ (1 - 0.03)} - 0.107 = \frac{Ib}{11.5} = 0.107 \text{ mA}$$

$$I_2 = \frac{11.4 - 5.35 - 0.8}{0.68\ (1 + 0.030)} - 0.35 = 7.10 \text{ mA}$$

Thus, the total change of current through VR103 is 11.5 - 7.1 = 4.4 mA.

The degradation of regulated output V_1 for the 4.4 mA change of I_2 was estimated as negligible by measurements. The effects of the initial tolerances upon the regulator's output, and its influence on the modulated frequency of the auxiliary track channel are adjusted out by R115 (see Figure 4-69) on the 1A19 subassembly. A factor which may cause a frequency drift is the characteristic tracking with temperature between the CR102 and the V_{BE} of Q103 with temperature. Laboratory data, however, substantiates that the bias variation supplied to the modulator does not degrade performance of the overall subsystem below the specified limits.

c. Frequency Modulator (Q104 through Q107). - The auxiliary track modulator is presented schematically in Figure 4-77 for the purpose of discussion and analysis. Several ECAP attempts were made using three different transient models to prove that the modulator will start upon the application of power supplies. These have failed because of complexities associated with the modeling, and deficiencies in specified parameters required in the transient semiconductor modeling.

As a result of the computer transient analysis, however, a need for a starting device to cause oscillation became apparent and a 12 picofarad starting capacitor has been added to force Q4 and Q7 to ON and OFF states respectively.

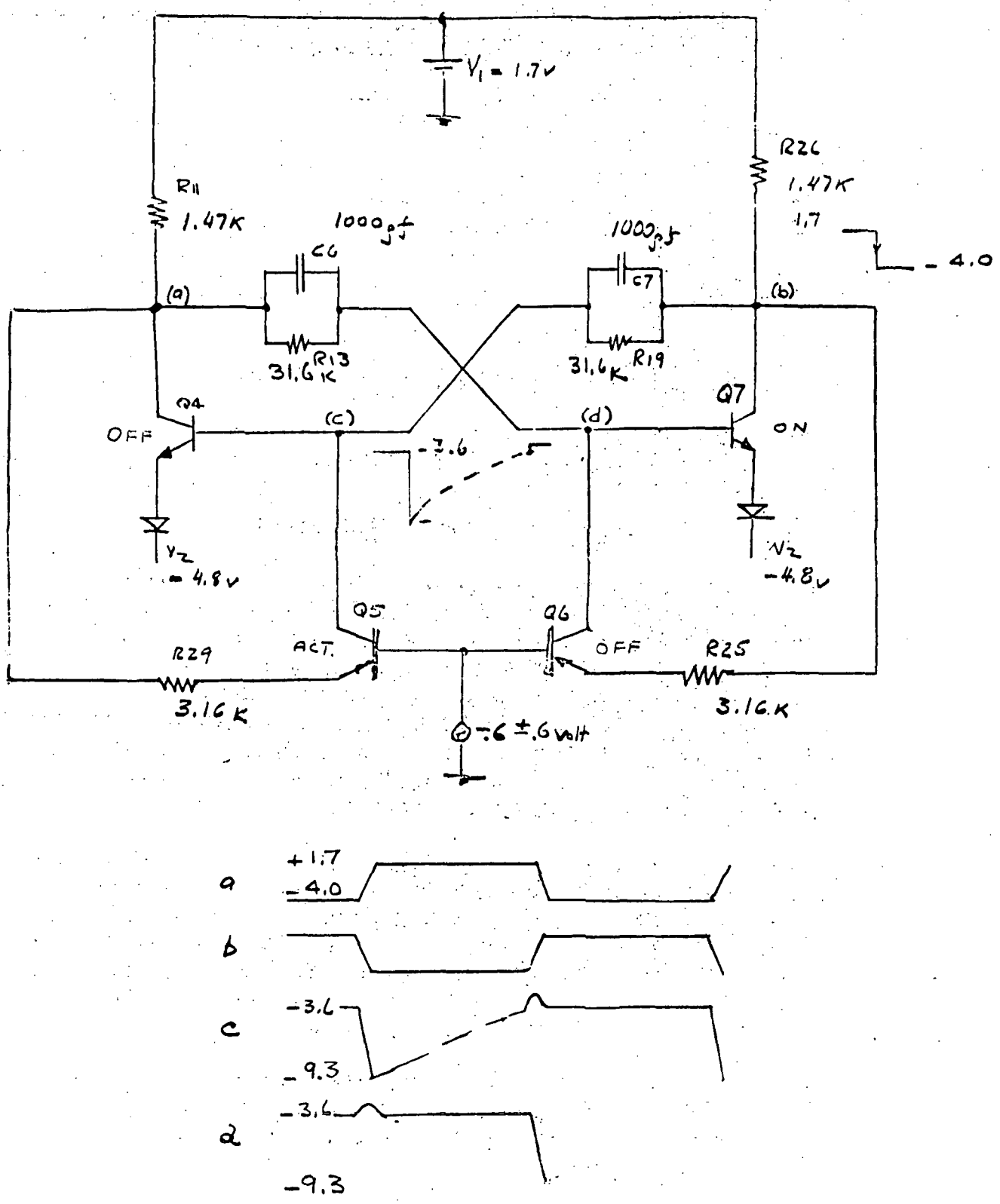


Figure 4-77. Auxiliary Track Modulator

The frequency deviation analysis of the FM modulator due to the input signal and the drift of its components is given in reference to Figures 4-77 and 4-78.

In summary, the ON-OFF intervals of Q4 and Q7 determine the output frequency of the modulator. Transistors Q4 and Q7 are operating in the astable multivibrator mode between cutoff and saturation by means of regeneration via C6 and C7. Q6 and Q5 of the modulator are used as current control devices operating between cutoff and the active region to supply charging currents and the base drives during the OFF intervals of Q7 and Q4 respectively.

The turn OFF action is affected by a negative base current supplied to Q7 by Q4 and vice-versa, and through the degeneration of the positive base current provided by the controlling Q6 and Q7. Using the equivalent circuit model of Figure 4-78, an equation may be derived to describe the instantaneous frequency of the modulated auxiliary track.

The derivation of one half of the period is undertaken with the assumption that the other half of the period is negligibly different. To compute the overall frequency drift, equation 1 was differentiated to determine the drift contribution by each parameter in the equation.

Thus, by partially differentiating equation 1 for the modulating frequency, an estimate of the drift contribution can be summarized as follows:

Nominally

$$2\,C_7(R_{25} + R_{26}) = 2(10^{-9})(3.16 + 1.47)\,10^3 = 9.21 \text{ us}$$

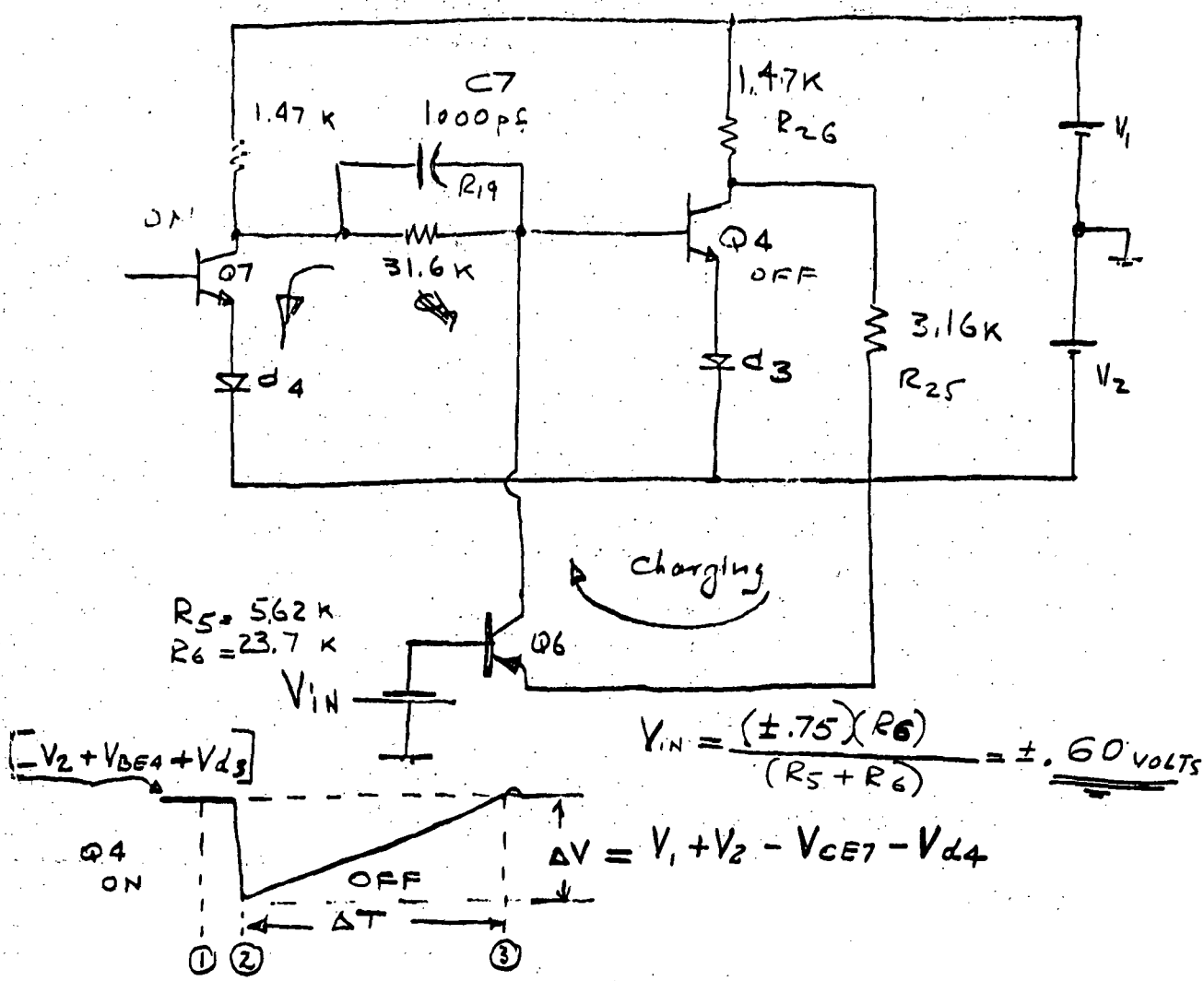
Center Frequency (Equation 1)

$$f_o = \frac{10^6}{9.21}\left\{\frac{1.7 + 0.7 - 0.7}{1.7 + 5.0 - 0.2 - 0.7}\right\} = \frac{10^6}{9.21}\,\frac{1.7}{(5.8)} = 31.8 \text{ kHz}$$

Frequency Deviation

$$\Delta V_{in} = \pm 0.6 \text{ volts}$$

$$\Delta f = \frac{10^6}{9.21}\,\frac{\Delta V_{in}}{5.8} = \pm\frac{0.6 \times 10^6}{53.5} = 11 \text{ kHz}$$



$$V_{IN} = \frac{(\pm .75)(R_6)}{(R_5 + R_6)} = \pm .60 \text{ VOLTS}$$

$$\Delta V = V_1 + V_2 - V_{CE7} - V_{d4}$$

$$\Delta T = C_7 \frac{\Delta V}{\Delta I} \qquad f = \frac{1}{2\Delta T} = \frac{\Delta I}{2C\Delta V}$$

$$\Delta I = \frac{V_1 + V_{IN} - V_{BE6}}{R_{25} + R_{26}}$$

Eq. 1

$$f = \frac{1}{2C_7(R_{25} + R_{26})} \left\{ \frac{V_1 + V_{IN} - V_{BE6}}{V_1 + V_2 - V_{CE7} - V_{d4}} \right\}$$

Figure 4-78. Auxiliary Track Modulator Drift Model

Drift Derivatives

1. $f_0 = 0.585 \frac{1}{C_7(R_{25} + R_{26})} = 0.585 \frac{1}{RC}$

$$\frac{D_F}{D(RC)} = 0.585 \left\{ \frac{CDR + RDC}{RC^2} \right\}$$

$$\Delta f_0 = \frac{0.585}{RC} \left\{ \frac{\Delta R}{R} + \frac{\Delta C}{C} \right\} = f_0 \left\{ \frac{\Delta R}{R} + \frac{\Delta C}{C} \right\}$$

EOL and TEMP

$$\frac{\Delta R}{R} \cong \pm 0.005 \Rightarrow \pm 0.5\% \qquad \frac{\Delta C}{C} \cong \pm 0.005 = \pm 0.5\%$$

$$\Delta f_0 = 31.8\ (\pm 0.01) = \pm 318\ \text{Hz}$$

Nominally

V_{in}	= 0.6	V_d4	= 0.7
V_1	= 1.7	C_7	= 1000 pF
V_2	= 5.0	R_{25}	= 3.16 kohms
V_CE	= 0.2	R_{26}	= 1.47 kohms

2. Drift component due to ΔV_{BE}

Specified temperature coeff. -1.8 mV/°C

for $\Delta T = \pm 30$°C from 25°C $\quad \Delta V_{BE_b} = 54$ mV

$$\Delta f_0 = \frac{10^6}{9.21} \frac{\pm \Delta V_{BE_b}}{5.8} = \frac{\pm 0.054 \times 10^6}{53.6} = -(\pm 1.0\ \text{kHz})$$

3. Drift components due to ΔV_2

Temperature 1N751A 5.1V ±0.03%/° C ⇒ ±0.045V

Assume compensating of Q101 by CR101 (see Figure 4-69)

Track within ±0.005 volts over temperature ⇒ ±0.005V

Tot ΔV_2 = ±0.05

$$\Delta f_0 = \frac{10^6}{9.21}\left\{\frac{1.7\ \Delta V_2}{[V_1 + V_2 - V_{CE7} - V_{d4}]^2}\right\} = \frac{10^6(1.7)(0.5}{9.21\ (33.8)} = \pm 274\text{Hz}$$

4. Drift due to ΔV_{d4} can be excluded from consideration because ΔV_{d4} ΔV_{d3}. This may be concluded from steady state conditions of ON/OFF regions. (See Figure 4-78.)

5. Drift due to ΔV_1 is negligible since V_1 controls both ΔV and ΔI and appears in either denominator and the numerator of equation 1.

6. Drift component due to ΔV_{CE} at 0.1 mV/° C = ±3.5 mV

$$\Delta f_0 = \frac{10^6(1.7)(\pm 0.0035)}{9.21\ (33.8)} = \pm 38.5\text{Hz}$$

Total Worst Case Δf_o = ±1.63kHz.

Referred to the output via the discriminator and output active filter:

Discriminator Output (V_1)

ΔV_1 = A (Δt) (Δf_o) = 65 millivolts

where A ⇒ pulse amplitude

= 4.0 volts peak (meas.)

Δt ⇒ pulse width

= 10 ms nom. (meas.)

Δf_0 ⇒ FM carrier drift

= ±1.63kHz

From the ECAP sensitivity computations (Figure 4-79, sheet 5, output Node 9) of the active output filter relative to input Branch #1 is:

$$\frac{\partial V_9}{\partial V_1}\frac{V_1}{100} = 17.5 \text{ mV/1\%}$$

Thus: $V_1 = 1.28V \Rightarrow$ Voltage source in Branch #1 (see Figure 4-79, sheets 1 and 3)

$$\Delta V_9 = \frac{17.5\ (\pm 65)\ (100)}{1280} = \pm 89 \text{ mV}$$

d. Divide by two Driver (Q108). - This stage (Figure 4-80) is used as a non-inverting buffer to prevent loading upon the modulator and to affect a drive capability of the SN5472J multivibrator. A limiting zener diode (VR105) which appears on the schematic drawing has been deleted as superfluous.

$$T = \{R20 + [R21 \,||\, R22]\} \cdot 09 = 34.8 \text{ X } 10^3(10^{-7}) = 3.48 \text{ ms}$$

$$F_L = \frac{1}{2\pi T} = 45.6\text{Hz}$$

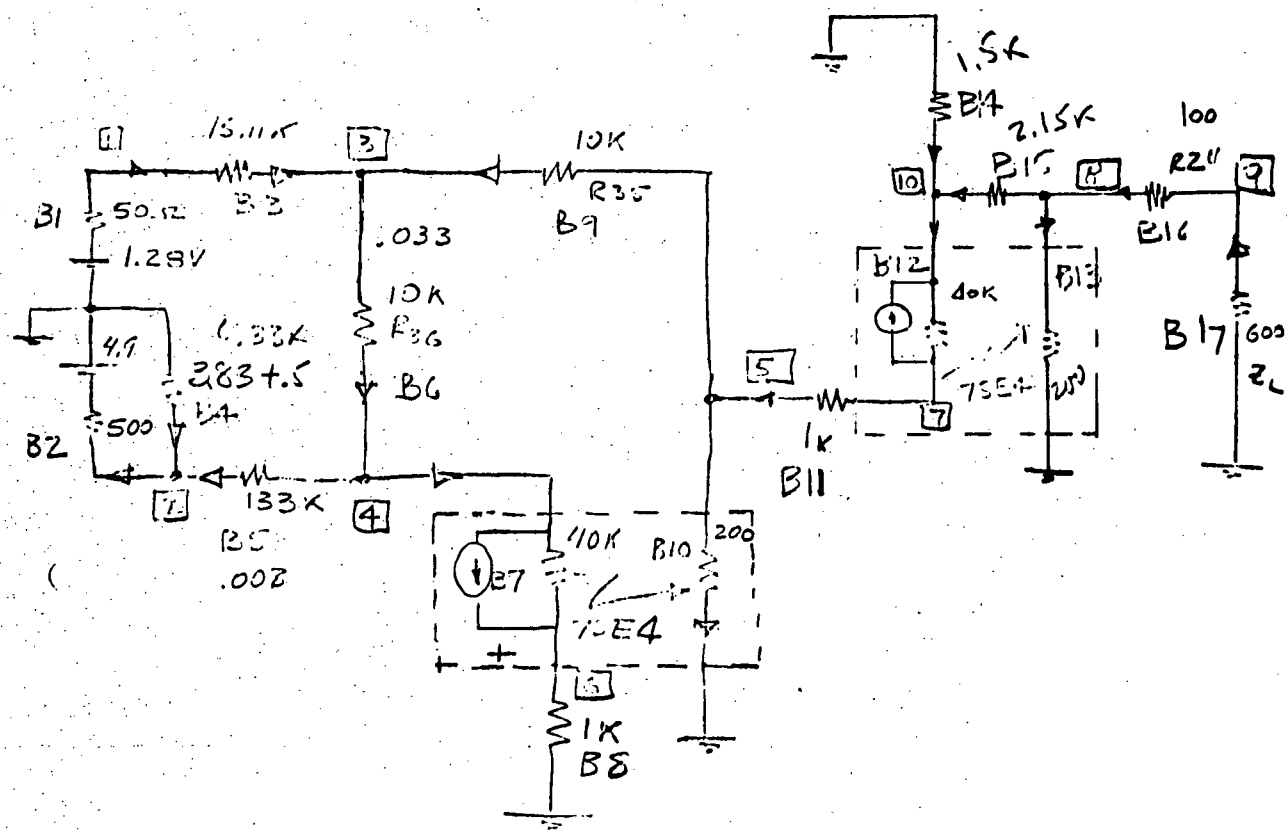
$$V_{B8} = \frac{5\ (51)}{151} \pm \frac{1}{2}\ \Delta V = \boxed{1.7 \pm 2.8}$$

For $V_{B8} = 4.5$ volts Q8 is OFF and a sufficient I_2 is supplied to affect a "high" input state of SN5472J.

But for $V_{B8} = 1.7 - 2.8 = 1.1$ volt, Q8 is saturated, essentially clamping its emitter to ground. Trigger ON or a low state current I_1 is now supplied in excess of the required worst case 3.5 mA margin.

e. Divide by two Flip-Flop (Z1-1A19). - Z1 is a J-K master-slave flip-flop whose function in this case is to divide the frequency of the resulting FM signal. The output of the SN5472 is quite capable of supplying 10 unit loads or approximately 10 mA, which is more than sufficient to drive its 10k load.

f. Head Driver (Q109, Q110). - The head driver of the ERTS aux track supplies bi-directionally ±2.0 mA to a 22 millihenry load. (See Figure 4-69.) From laboratory performance data, it seems that variation of the current




```
        MODIFY
R2      R=1
R4      R=5340  → 4.83 K
        EX

NODE VOLTAGES

NODES                VOLTAGES

  1- 4     0.12769928D 01   -0.48990454D 01   0.36830122D 00   -0.36435041
  5- 6     0.13525469D 00   -0.88865914D-06
```

Figure 4-79. Auxiliary Track Playback Filter DC Analysis (Sheet 1 of 7)

```
C      [illegible] FILT CONTRIBUTION BY PARTIAL
C      RELATIVE ANALYSIS OF BITS AUX.TRACK
C      14-20(74 AND 75)
       R(0 ,1 ),      R=50.      E=1.28(.02)
R2     R(2 ,0 ),      R=500(.01),     E=4.9(.01)
R3     R(1 ,3 ),      R=1511(.005)
R4     R(0 ,2 ),      R=4330(.01)
R5     R(4 ,2 ),      R=133E3(.005)
R6     R(3 ,4 ),      R=1E4(.005)
R7     R(4 ,6 ),      R=4E4,     T=0(-5E-7,5E-7)
R8     R(6 ,0 ),      R=1E3(.005)
R9     R(5 ,3 ),      R=1E4(.005)
R10    R(5 ,0 ),      R=200
R11    R(7 ,5 ),      R=1E3(.005)
R12    R(10,7 ),      R=4E4,     T=0(-5E-7,5E-7)
R13    R(8 ,0 ),      R=200
R14    R(0 ,10),      R=1500(.005)
R15    R(8 ,10),      R=2150(.005)
R16    R(9 ,8 ),      R=102(.005)
R17    R(0 ,9 ),      R=600(.01)
T1     R(7 ,10),      BETA=75E4
T2     R(12,13),      BETA=75E4
       SENSITIVITY
       WORST CASE, 5, 0
       PRINT,DV,SE,WORST CASE
       EXECUTE
```

NODE VOLTAGES

NODES	VOLTAGES			
1- 4	0.12765637D 01	-0.43779983D 01	0.32916373D 00	-0.68807391D-05
5- 8	0.31133883D-01	-0.16782283D-06	0.31133207D-01	0.75690173D-01
9- 10	0.64877290D-01	0.31106150D-01		

PARTIAL DERIVATIVES AND SENSITIVITIES OF NODE VOLTAGES

WITH RESPECT TO RESISTANCES $\frac{\partial V_j}{\partial R_i} \cdot \frac{R_i}{100}$ (volts) / 1%

BRANCH	NODE	PARTIALS	SENSITIVITIES
1	1	-0.62513491D-04	-0.31256728E-04
1	2	-0.38716964D-10	-0.19358473E-10
1	3	-0.15201791D-07	-0.76008924E-08
1	4	-0.11526658D-07	-0.57633258E-08
1	5	0.41343230D-04	0.20671650E-04
1	6	-0.28113786D-09	-0.14056889E-09
1	7	0.41342425D-04	0.20671199E-04
1	8	0.10051054D-03	0.50255243E-04
1	9	0.86151867D-04	0.43075925E-04
1	10	0.41306495D-04	0.20653242E-04
2	1	-0.23108863D-06	-0.11554421E-05
2	2	0.93278930D-03	0.46639182E-02
2	3	-0.70066086D-04	-0.35033026E-03
2	4	0.51585958D-07	0.25792974E-06
2	5	-0.18640149D-03	-0.93200710E-03
2	6	0.12581936D-06	0.62900642E-06

Figure 4-79. Auxiliary Track Playback Filter DC Analysis (Sheet 2 of 7)

2	[illegible]	-0.[illegible]E-03	-0.22659203E-02
2	[illegible]	-0.[illegible]E-03	-0.19421317E-02
2	[illegible]	-0.[illegible]E-03	-0.93117692E-03
3	1	0.[illegible]E-06	0.31249972E-04
3	2	-0.[illegible]E-10	-0.58501008E-08
3	3	-0.15201712D-07	-0.22969780E-05
3	4	-0.11526598D-07	-0.17416087E-05
3	5	0.41343109D-04	0.62469430E-02
3	6	-0.28113640D-09	-0.42479705E-07
3	7	0.41342211D-04	0.62468052E-02
3	8	0.10051002D-03	0.15187062E-01
3	9	0.86151441D-04	0.13017479E-01
3	10	0.41304281D-04	0.62413774E-02
4	1	0.25843232D-07	0.11190114E-05
4	2	-0.10431561D-03	-0.45168623E-02
4	3	0.79356922D-05	0.33928431E-03
4	4	-0.57669395D-06	-0.24979715E-06
4	5	0.20845754D-04	0.90262084E-03
4	6	-0.14070700D-09	-0.60926091E-08
4	7	0.20845301D-04	0.90260128E-03
4	8	0.50678508D-04	0.21943788E-02
4	9	0.43438721D-04	0.18808960E-02
4	10	0.20827185D-04	0.90181665E-03
5	1	-0.81275456D-08	-0.10809633E-04
5	2	-0.11055974D-06	-0.14704441E-03
5	3	-0.24642722D-05	-0.32774613E-02
5	4	0.18143136D-08	0.24130359E-05
5	5	-0.65558680D-05	-0.87193027E-02
5	6	0.44251529D-10	0.58854521E-07
5	7	-0.65557256D-05	-0.87191127E-02
5	8	-0.15933095D-04	-0.21197662E-01
5	9	-0.13661224D-04	-0.18169422E-01
5	10	-0.65502830D-05	-0.87115355E-02
6	1	0.10850004D-06	0.10850003E-04
6	2	-0.50519989D-10	-0.50519979E-08
6	3	0.32897213E-04	0.32897212E-02
6	4	-0.15046060D-07	-0.15046596E-05
6	5	0.54592433D-04	0.54592416E-02
6	6	-0.36684388D-09	-0.36684380E-07
6	7	0.54591247D-04	0.54591224E-02
6	8	0.13272070D-03	0.13272066E-01
6	9	0.11376060D-03	0.11376057E-01
6	10	0.54543804D-04	0.54543763E-02
7	1	-0.59460867D-12	-0.23784330E-09
7	2	-0.56341246D-12	-0.22536498E-09
7	3	-0.18028538D-09	-0.72114119E-07
7	4	-0.16773687D-09	-0.67094732E-07
7	5	-0.31175563D-09	-0.12470224E-06
7	6	0.20924292D-14	0.83697166E-12
7	7	-0.31174586D-09	-0.12469951E-06
7	8	-0.75791502D-09	-0.30316596E-06
7	9	-0.64964144D-09	-0.25985656E-06
7	10	-0.31147793D-09	-0.12459117E-06
8	1	-0.59460816D-12	-0.59460804E-11
8	2	-0.56341208D-12	-0.56341190E-11
8	3	-0.18028522D-09	-0.18028519E-08
8	4	-0.16773676D-09	-0.16773671E-08
8	5	-0.31175533D-09	-0.31175527E-08
8	6	-0.16782059D-09	-0.16782056E-08
8	7	-0.31174856D-09	-0.31174849E-08
8	8	-0.75791429D-09	-0.75791391E-08
8	9	-0.64964081D-09	-0.64964034E-08
8	10	-0.31147763D-09	-0.31147755E-08
9	1	0.35409201D-10	0.35409193E-08
9	2	0.27343363D-10	0.27343359E-08

Figure 4-79. Auxiliary Track Playback Filter DC Analysis (Sheet 3 of 7)

9	4	0.91405531E-05	0.21405534E-06
9	5	-0.29782565E-04	-0.29782560E-02
9	6	0.13554003E-09	0.13354998E-07
9	7	-0.29731313E-04	-0.29731912E-02
9	8	-0.72404525E-04	-0.72404922E-02
9	9	-0.62061392E-04	-0.62061362E-02
9	10	-0.29756034E-04	-0.29756031E-02
10	1	0.18495144E-09	0.36990278E-09
10	2	0.14282148E-09	0.28562284E-09
10	3	0.56077285E-07	0.11215457E-06
10	4	0.42526230E-07	0.85046426E-07
10	5	0.10652263E-06	0.21324922E-06
10	6	0.10370783E-08	0.20741566E-08
10	7	0.10562231E-06	0.21324462E-06
10	8	0.25921716E-06	0.51843426E-06
10	9	0.22216613E-06	0.44437223E-06
10	10	0.10652965E-06	0.21305925E-06
11	1	0.34920994E-20	0.34920984E-19
11	2	0.26966363E-20	0.26966356E-19
11	3	0.10588047E-17	0.10588045E-16
11	4	0.80293161E-18	0.90283139E-17
11	5	0.20131377E-17	0.20131961E-16
11	6	0.19581250E-19	0.19581242E-18
11	7	-0.67646946E-09	-0.67640649E-08
11	8	-0.16446615E-08	-0.16446609E-07
11	9	-0.14095384E-08	-0.14095381E-07
11	10	-0.67581910E-09	-0.67581287E-08
12	1	0.34913705E-20	0.13965481E-17
12	2	0.26960732E-20	0.10784285E-17
12	3	0.10548837E-17	0.42343325E-15
12	4	0.80266396E-18	0.32106551E-15
12	5	0.20127772E-17	0.80511075E-15
12	6	0.19577161E-19	0.78306643E-17
12	7	0.14695039E-13	0.58780151E-11
12	8	-0.16446621E-08	-0.65778482E-06
12	9	-0.14095380E-08	-0.56381555E-06
12	10	-0.67581935E-09	-0.27032769E-06
13	1	0.50807275E-15	0.11979454E-14
13	2	0.46253316E-15	0.92506628E-15
13	3	0.16160657E-12	0.36321711E-12
13	4	0.13770349E-12	0.27540698E-12
13	5	0.34530820E-12	0.69061635E-12
13	6	0.33586203E-14	0.67172389E-14
13	7	0.25210527E-08	0.50421036E-08
13	8	0.25690304E-06	0.51380607E-06
13	9	0.22020260E-06	0.44040519E-06
13	10	0.10334940E-06	0.20669876E-06
14	1	0.64560674E-16	0.97299228E-15
14	2	0.50046104E-16	0.75129133E-15
14	3	0.19665750E-13	0.29498631E-12
14	4	0.14911432E-13	0.22367145E-12
14	5	0.37392225E-13	0.56088332E-12
14	6	0.36369329E-15	0.54553970E-14
14	7	0.27296020E-09	0.40940395E-08
14	8	-0.29695823E-04	-0.44543715E-03
14	9	-0.25453562E-04	-0.38180337E-03
14	10	-0.11191346E-07	-0.16787016E-06
15	1	-0.42197139E-16	-0.90723772E-15
15	2	-0.32585081E-16	-0.70057862E-15
15	3	-0.12734175E-13	-0.27507451E-12
15	4	-0.97010981E-14	-0.20857345E-12
15	5	-0.24326881E-13	-0.52302325E-12
15	6	-0.23661204E-15	-0.50871545E-14
15	7	-0.17760610E-09	-0.38185277E-08
15	8	0.20718652E-04	0.44545066E-03

Figure 4-79. Auxiliary Track Playback Filter DC Analysis (Sheet 4 of 7)

15	15	-0.7250 [illegible]E-09	-0.15653676E-06
16	1	0.4[illegible]E-16	0.43895731E-16
16	2	0.3775[illegible]E-16	0.37757804E-16
16	3	0.1[illegible]E-13	0.14825187E-13
16	4	0.11241102E-13	0.11241100E-13
16	5	0.2818[illegible]E-13	0.28188426E-13
16	6	0.27417311E-15	0.27417292E-15
16	7	0.20580241E-09	0.20580024E-09
16	8	0.20971678E-07	0.20971676E-07
16	9	-0.92663314E-04	-0.92663602E-04
16	10	0.84366861E-08	0.84366860E-08
17	1	0.43895749D-16	0.29337431E-15
17	2	0.37757820D-16	0.22654680E-15
17	3	0.14825194E-13	0.88951145E-13
17	4	0.11241105E-13	0.67446591E-13
17	5	0.2818[illegible]E-13	0.16913055E-12
17	6	0.27417317D-15	0.16450386E-14
17	7	0.20580241E-09	0.12348014E-08
17	8	0.20971683E-07	0.12583007E-06
17	9	0.15464946D-04	0.92789647E-04
17	10	0.84366879D-08	0.50620116E-07

WITH RESPECT TO BETAS

BETA	NODE	PARTIALS	SENSITIVITIES
1	1	0.39879209D-13	0.29906609E-09
1	2	0.30794379D-13	0.23095760E-09
1	3	0.12091075D-10	0.90682931E-07
1	4	0.91679775D-11	0.68759732E-07
1	5	0.22989815D-10	0.17242343E-06
1	6	0.22360911E-12	0.16770665E-08
1	7	0.22989315D-10	0.17241947E-06
1	8	0.55890974D-10	0.41918134E-06
1	9	0.47906549D-10	0.35929872E-06
1	10	0.22969336D-10	0.17226984E-06
2	1	0.21411421D-18	0.16058548E-14
2	2	0.16534128D-18	0.12400581E-14
2	3	0.64919440D-16	0.48689525E-12
2	4	0.49224736D-16	0.36918510E-12
2	5	0.12343699D-15	0.92577595E-12
2	6	0.12006028D-17	0.90045091E-14
2	7	0.90119830D-12	0.67589774E-08
2	8	0.91834883D-10	0.68876085E-06
2	9	0.78715613D-10	0.59036648E-06
2	10	0.36944209D-10	0.27708126E-06

WITH RESPECT TO VOLTAGE SOURCES

BRANCH	NODE	PARTIALS	SENSITIVITIES
1	1	0.99670265D 00	0.12757786E-01
1	2	0.61729557D-06	0.79013773E-08
1	3	0.24237433D-03	0.31023892E-05
1	4	0.18377873D-03	0.23523662E-05
1	5	-0.65916970D 00	-0.84373653E-02
1	6	0.44824060D-05	0.57374766E-07
1	7	-0.65915539D 00	-0.84371828E-02
1	8	-0.16025200D 01	-0.20512242E-01
1	9	-0.13735885D 01	-0.17581921E-01 ←
1	10	-0.65852534D 00	-0.84298514E-02
2	1	0.22134879D-03	0.10846087E-04
2	2	-0.89346930D 00	-0.43779980E-01
2	3	0.67112965D-01	0.32885340E-02
2	4	-0.49411732D-04	-0.24211740E-05

Figure 4-79. Auxiliary Track Playback Filter DC Analysis (Sheet 5 of 7)

2	6	-0.12051[illegible]70-05	-0.59052997E-07
2	7	0.17854[illegible]23E 00	0.87485164E-02
2	8	0.4[illegible]E 00	0.21269146E-01
2	9	0.[illegible]E 00	0.18230695E-01
2	10	0.17[illegible]E 00	0.87409131E-02

WITH RESPECT TO CURRENT SOURCES

BRANCH	NODE	PARTIALS	SENSITIVITIES
7	1	-0.36492600D 02	0.00000000E 00
7	2	-0.33324800D 01	0.00000000E 00
7	3	-0.11064551D 05	0.00000000E 00
7	4	-0.99213270E 03	0.00000000E 00
7	5	-0.28435511D 05	0.00000000E 00
7	6	-0.99980418D 03	0.00000000E 00
7	7	-0.29434893D 05	0.00000000E 00
7	8	-0.69136103D 05	0.00000000E 00
7	9	-0.59254370D 05	0.00000000E 00
7	10	-0.23410181D 05	0.00000000E 00
12	1	-0.23761106D-03	0.00000000E 00
12	2	-0.18348560D-03	0.00000000E 00
12	3	-0.72043684D-01	0.00000000E 00
12	4	-0.54626646D-01	0.00000000E 00
12	5	-0.13698294D 00	0.00000000E 00
12	6	-0.13323566D-02	0.00000000E 00
12	7	-0.10000056D 04	0.00000000E 00
12	8	-0.45704401E 04	0.00000000E 00
12	9	-0.39252343D 04	0.00000000E 00
12	10	-0.99843665D 03	0.00000000E 00

WORST CASE SOLUTIONS FOR NODE VOLTAGES

NODE	WCMIN	NOMINAL	WCMAX
5	PARTIAL W.R.T. R 7 HAS CHANGED SIGN AT MIN		
5	PARTIAL W.R.T. R 10 HAS CHANGED SIGN AT MIN		
5	PARTIAL W.R.T. R 12 HAS CHANGED SIGN AT MIN		
5	PARTIAL W.R.T. R 13 HAS CHANGED SIGN AT MIN		
5	PARTIAL W.R.T. R 14 HAS CHANGED SIGN AT MIN		
5	PARTIAL W.R.T. R 15 HAS CHANGED SIGN AT MIN		
5	PARTIAL W.R.T. R 16 HAS CHANGED SIGN AT MIN		
5	PARTIAL W.R.T. R 17 HAS CHANGED SIGN AT MIN		
5	PARTIAL W.R.T. T 1 HAS CHANGED SIGN AT MIN		

Figure 4-79. Auxiliary Track Playback Filter DC Analysis (Sheet 6 of 7)

```
 5  PARTIAL W.R.T.  T  2  HAS CHANGED SIGN AT MIN
 5  PARTIAL W.R.T.  R  8  HAS CHANGED SIGN AT MAX
 5  PARTIAL W.R.T.  R 11  HAS CHANGED SIGN AT MAX
 5      -0.2241796E-01      0.3113388E-01      0.8433867D-01
 9  PARTIAL W.R.T.  R  7  HAS CHANGED SIGN AT MIN
 9  PARTIAL W.R.T.  R 10  HAS CHANGED SIGN AT MIN
 9  PARTIAL W.R.T.  R 12  HAS CHANGED SIGN AT MIN
 9  PARTIAL W.R.T.  R 13  HAS CHANGED SIGN AT MIN
 9  PARTIAL W.R.T.  R 14  HAS CHANGED SIGN AT MIN
 9  PARTIAL W.R.T.  R 15  HAS CHANGED SIGN AT MIN
 9  PARTIAL W.R.T.  R 16  HAS CHANGED SIGN AT MIN
 9  PARTIAL W.R.T.  R 17  HAS CHANGED SIGN AT MIN
 9  PARTIAL W.R.T.  T  1  HAS CHANGED SIGN AT MIN
 9  PARTIAL W.R.T.  T  2  HAS CHANGED SIGN AT MIN
 9  PARTIAL W.R.T.  R  8  HAS CHANGED SIGN AT MAX
 9  PARTIAL W.R.T.  R 11  HAS CHANGED SIGN AT MAX
 9      -0.48293777E-01      0.64377272E-01      0.17913274D 00
```

WORST CASE OUTPUT DRIFT NODE # 9

$179 - 64.9 = 114.1$

$-(48.3 + 64.9) = 113.2$ $\Big\} \approx \pm 113.6 \Rightarrow 114_{MV}$

Figure 4-79. Auxiliary Track Playback Filter DC Analysis (Sheet 7 of 7)

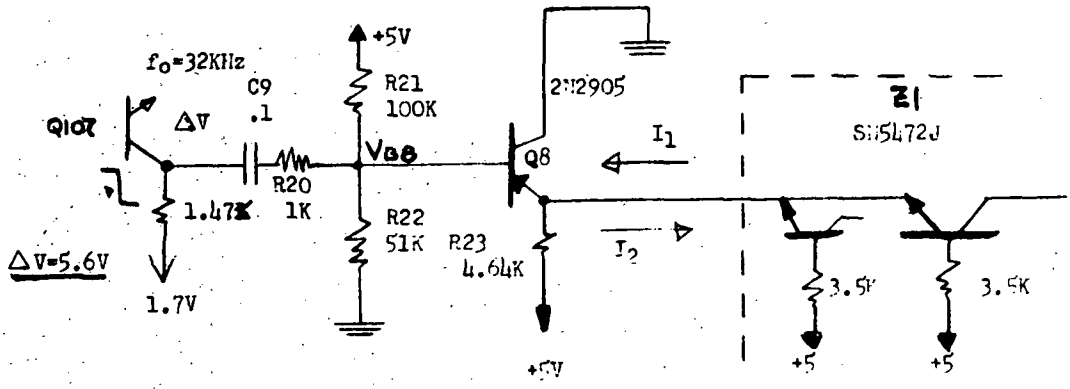


Figure 4-80. Divide By Two Driver

limits of 0.5 mA is acceptable for a faithful reproduction of the input signal and a proper self erasure requirement. The output transistor which drives the head operates between cutoff and the class "A" regions. The positive steady state current is thus a function of R_{30} and V_1. When Q10 is cut off (Figure 4-81), the head current is:

$$I_L = \frac{V1}{R30}(1 - E^{-t/T}) \text{ and } T = \frac{L}{R} = \frac{22 \times 10^{-3}}{12.1 \times 10^{3}} = 1.81 \text{ s}$$

Consider at t = 3T = 5.4 μs steady state

$$I_L = \frac{V1}{R30}$$

thus,

$$I_L = \frac{22\ (1 + 0.05)}{12.1\ (1-0.05)} = 2.0 \text{ mA}$$

$$I_L = \frac{22\ (1 - 0.05)}{12.1\ (1+0.05)} = 1.63 \text{ mA}$$

Diode CR6 clamps the base potential of the Q10 to -22.7 volts dc, thus assuring a cutoff condition.

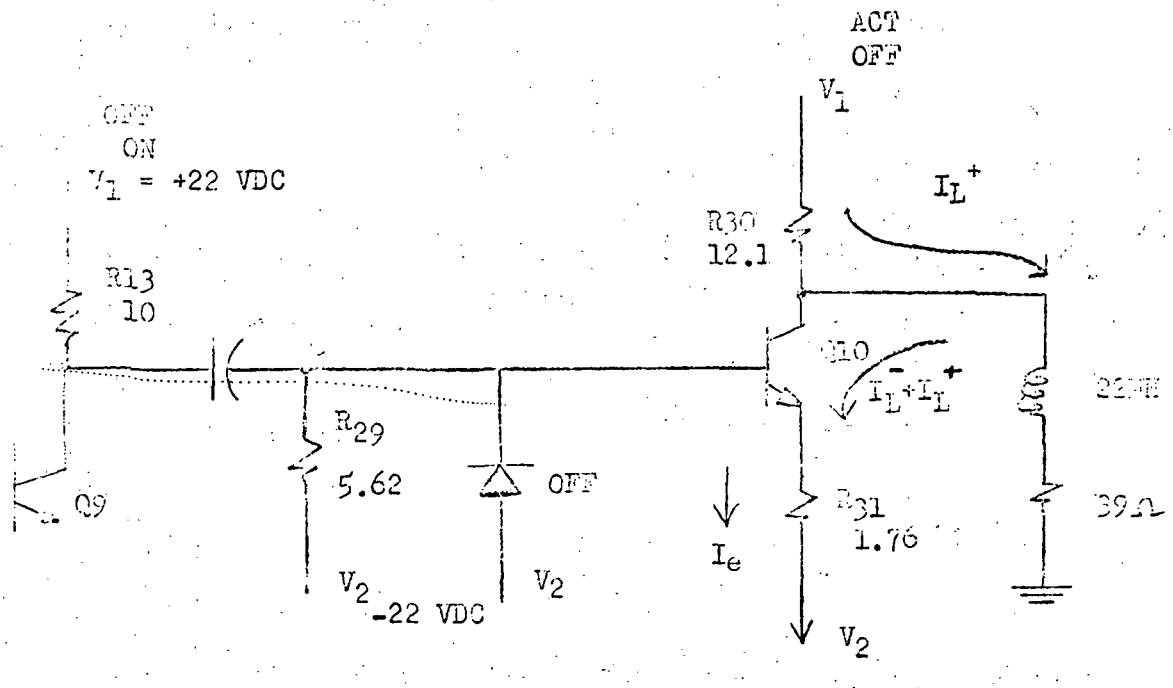


Figure 4-81. Auxiliary Track Head Driver

The negative current is delivered through Q10, and the governing parameters are:

$$I_e = \frac{\frac{V_1\,(R29)}{R_{13} + R_{29}} - V_{BE}}{R_{31}}$$

Since hfe $\simeq$ 1 + hfe

and hfe $\geq$ 50

$$I_e = I_L^- + I_L^+$$

$$I_L^- \cong \frac{V_1\,R_{29}}{(R_{13} + R_{29})\,R_{31}} - \frac{V_{BE}}{R_{31}} - I_L^+$$

Nominally

$$I_L^- = \frac{\frac{22\,(5.62)}{15.62} - 0.7}{1.78} - 1.81\text{mA} = \frac{7.2}{1.78} - 1.81$$

$$= 2.2\text{mA}$$

Max.

$$I_L^- = \frac{22\,(1 + 0.05)(0.358) - 0.6}{1.78\,(1 - 0.05)} - 1.63 = 2.9\ \text{mA}$$

4.2.3.2 Playback Analysis. - Playback circuits of the auxiliary track are primarily; (a) Playback preamplifier; (b) Amplifier Limiter; (c) discriminator; and (d) output amplifier and filter. (See Figure 4-82.)

a. Playback Preamplifier. - Worst Case Analysis of this circuit has been covered in the Design Report, Volume I.

b. Auxiliary Track Limiter (Z1 through Q3 and Q4, Figure 4-70). - The auxiliary track amplitude limiter consists of two integrated amplifiers Z_1 and Z_2 and two pairs of emitter followers (Q_1, Q_2) and Q_3, Q_4). The limiter accepts an FM input signal and converts it to two phase amplitude limited square waves. The output square waves are shaped to have a fast rise time and a slow fall time, the purpose of which will be explained in relation to the nature of the discrimination process.

A section of limiter Z_1 is shown in Figure 4-83. Rough calculations indicate no problems relative to bias or gain variation in the CA3006 element. Output emitter followers Q3 and Q4 of 1A20 conduct on alternate half cycles of the input signal. Capacitors C15 and C16 are charged through Q3 and Q4 respectively, and discharged through 1000 ohms each, thus allowing a fast rise and slow fall time for the resulting square wave.

The charging time constant $T_1 = (R_c + 2R_d)\ (1.5 \times 10^{-9})$, which is approximately 300 ns, whereas the discharging time constant $T_2 = 1.5$ us. The reasons for this unbalance is discussed subsequently.

c. Auxiliary Channel Discriminator (Z3, Figure 4-70). - As has been mentioned previously, the integrated circuit (uA9601) one shot is used as a discriminator. The output of the circuit generates a positive pulse during each phase transition at the FM input signal (Figure 4-84).

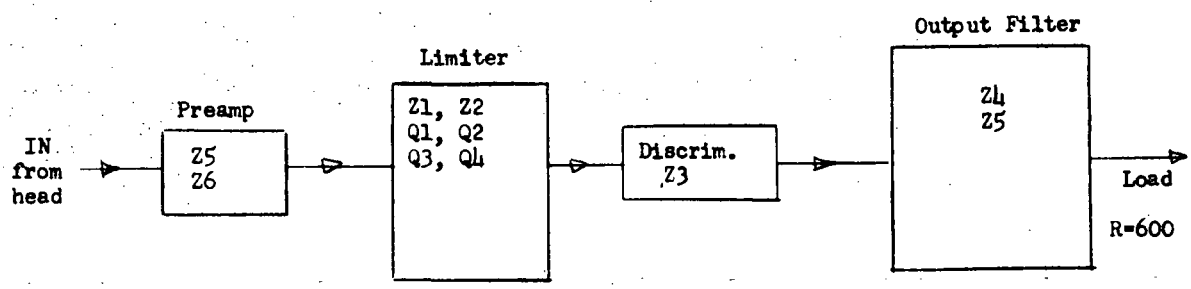
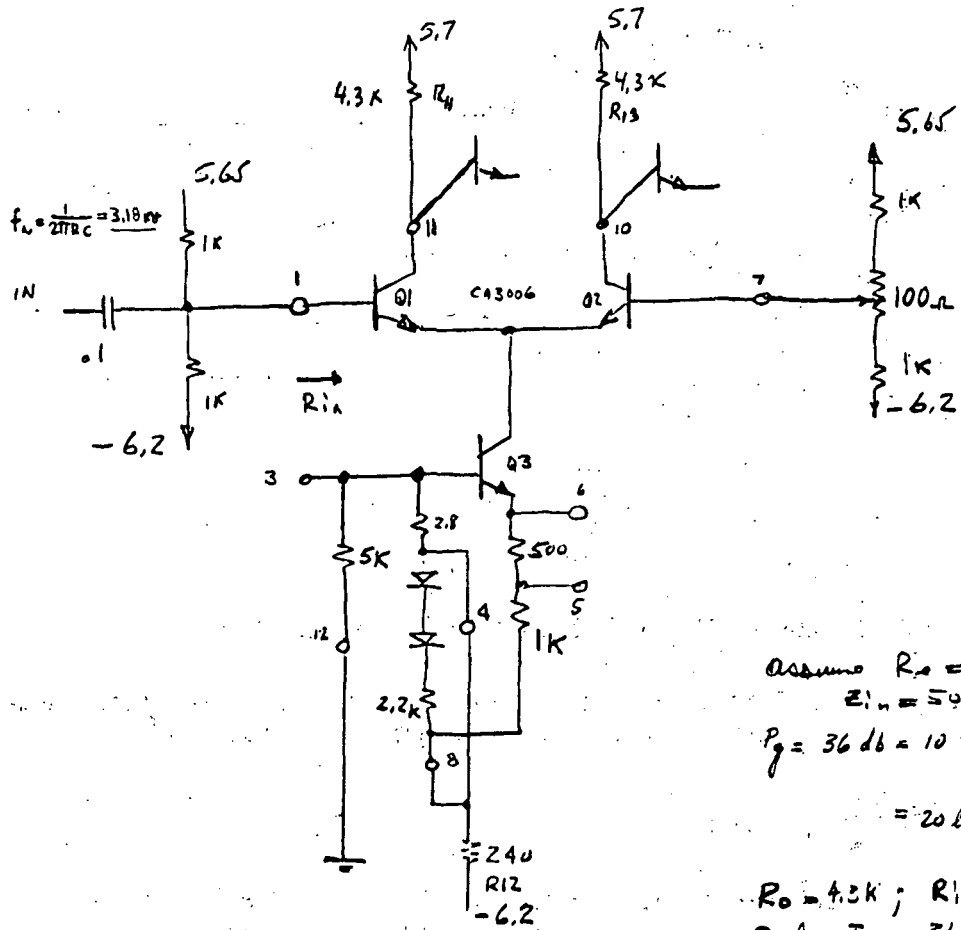


Figure 4-82. Playback Functional Diagram



$$V_5 = \frac{6.2\,(5.0)}{5 + 2.8 + .2V} = -3.87$$

$$V_c = -3.87 - .7 = -4.57\,v$$

$$I_c = \frac{6.2 - 4.57}{1.74\,k} = \frac{1.63}{1.7\,V} = .94\,ma$$

$$I_{c_1} = I_{c_2} = .45\,ma$$

$$\Delta V_{R11} = \Delta V_{R13} = .45(4.3) = 1.94v$$

$$V_{c_1} = V_{c_2} = 5.7 - 1.94 = 3.8V$$

Assume $R_o = 10\Omega$

$$Z_{in} = 500\Omega + 1000 = 1.5k$$

$$P_g = 36\,db = 10 \log \frac{I_o^2 R_o}{I_i^2 R_i}$$

$$= 20 \log \frac{I_o}{I_i} + 10 \log \frac{R_o}{R_i}$$

$R_o = 4.3K$; $R_{in} = 600\Omega$

$$\therefore 20 \log \frac{I_o}{\Delta I_i} = 36 - 10 \log \frac{4.3}{1.5} = 32db$$

$$\frac{\Delta I_o}{\Delta i} = \frac{45}{1}$$

or

$$20 \log \frac{\Delta V_o}{\Delta V_{in}} = 36 + 10 \log \frac{4.3}{1.5} = 40db$$

$$\frac{\Delta V_o}{\Delta V_{in}} = \frac{100}{1}$$

NEXT STAGE

$$20 \log \frac{\Delta V_o}{\Delta V_{in}} = 36 + 10 \log \frac{4.3K}{(5.1 \| 1.5)K}$$

$$= 34\,db$$

$\therefore$ OVERALL GAIN $\simeq$ 74 db $\Rightarrow \frac{5000}{1}$

Figure 4-83. Auxiliary Track Limiter Z1, Partial Schematic

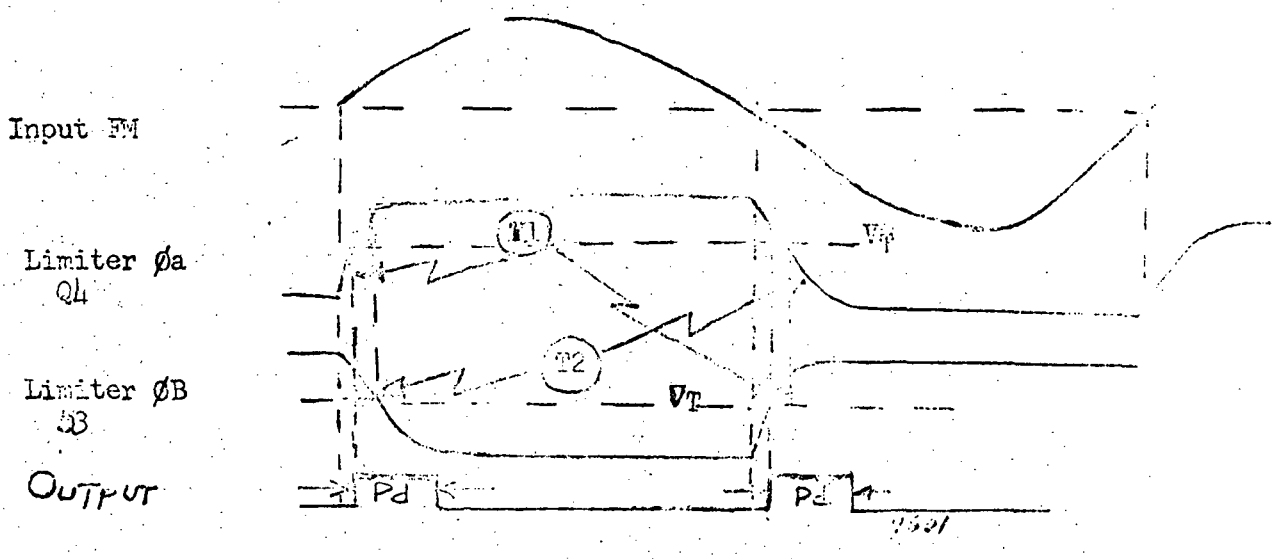


Figure 4-84. Auxiliary Channel Discriminator Waveforms

The two phases of the limiter are ANDed by the action of uA9601 and, when both signals are $>V_T = 1.5$ Volts, a positive pulse with duration[1]

$$Pd = 0.36 \left[R_{31}\, C_{17}\right]$$

is generated. These pulses correspond to each zero and 180° of the input sine wave. ANDing rather than ORing the two phases provides a better noise immunity.

Nominally: $Pd = 0.36 \left[14.7X10^{3}(2.4X10^{-9})\right] = 12.7$ us

$$Pd = 0.36\, \bar{R}\, \bar{C}$$

Assuming RNR55 EOL + Temp $\Delta R = \pm 0.5\%$

and CTM EOL + Temp $\Delta C = \pm 1\%$

$$Pd = 0.36 \left\{R(1 \pm 0.005)\ C\ (1.0 \pm 0.01)\right\}$$

$$= 0.36\ \ RC\ (1 \pm 0.005)\ (1.0 \pm 0.01) \cong 12.7\ (1 \pm 0.015)$$

$$\overline{Pd} = 12.9 \text{ us}$$

$$\underline{Pd} = 12.5 \text{ us}$$

[1] Fairchild Company

d. Output Filter. - The principal function of the output filter is to filter the FM carrier and its derivatives from the discriminated output. Since a dc to 5 kHz response is required, both ac and dc analyses of the output filter are given.

An equivalent ECAP circuit encompassing both Z_4 and Z_5 of the auxiliary track playback active filter is shown in Figure 4-85.

1. Output Filter AC Analysis. - The equivalent ECAP ac model (Figure 4-85) does not include open loop phase lag compensating capacitors C26 and C31. The exclusion is warranted by a prior analysis of frequency pole locations (Figure 4-86). Notice that the high frequency poles in both cases are beyond 211 kHz. The results of the ECAP ac program are shown in tabular computer form in Figure 4-87, reflecting the frequency response as a function of time constants. The results of phase shift and gain based on available power (GAV) from both the nominal and the minimum time constants are plotted in Figure 4-88.

2. Output Filter Bias Adjustment Range. - In addition to the ac response analysis, the output active filter has been analyzed for the adequacy of its output bias adjustment and its low frequency output drift due to worst case component tolerance shift during the mission. The former of the ECAP dc programs was primarily executed to see the output variation at Z4 when potentiometer R39 was adjusted from its center to minimum and maximum values. The analysis assumes that the discriminator puts out 1.28 volts average. The assumption is based on 12.8 us, 3.2 v peak pulse output at 32 kHz rate. The results of the program show (Figure 4-89) that the adjustment is sufficient for a range of -71.8 to +135 mVdc.

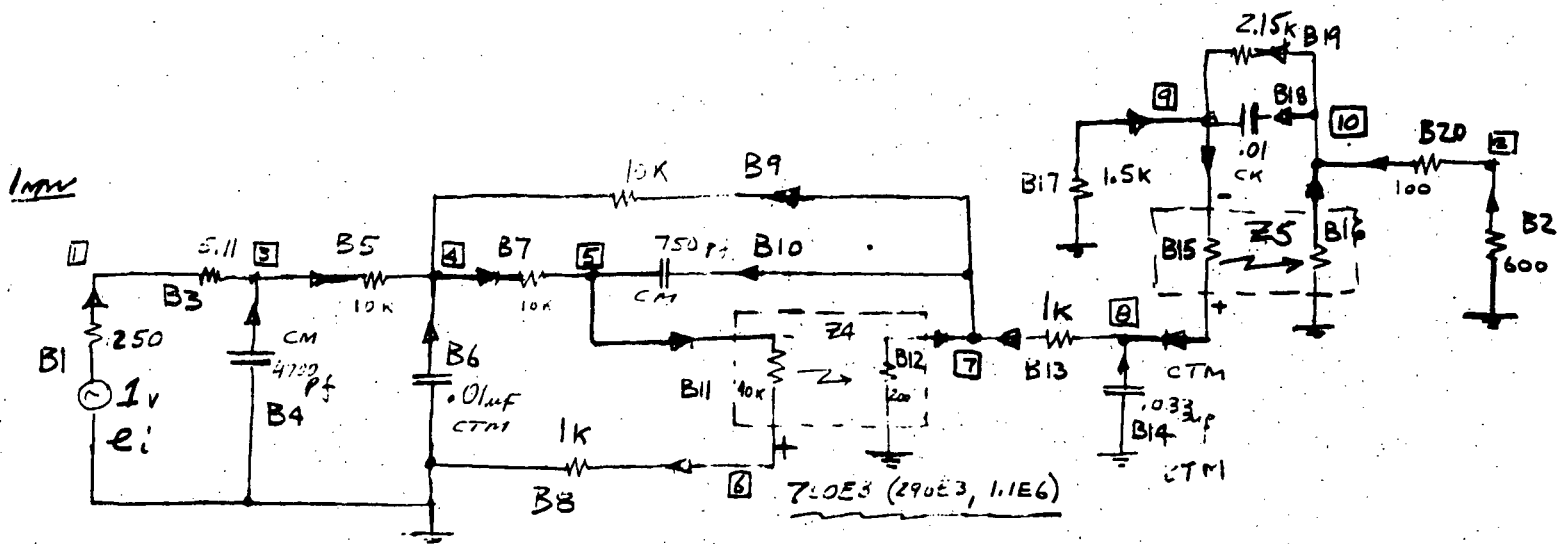
3. Output Drift Analysis. - The auxiliary track filter circuit, Z4 and Z5 with its bias adjustment at its center point, has been analyzed by an ECAP dc program to ascertain dc drift contributions of its four main sources, which are:

    a. Output bias adjust Zener diode VR2 (see Figure 4-70) at ±0.03%/°C or EOL ±1%.

    b. The uA702 input bias current variation due to Temperature and Life (allow ±0.5 uA).

    c. Resistor tolerances for RNR55 (allow EOL + Temp. ±0.5%).

    d. Input variation (primarily that of pulse width — allow 1%; and amplitude — allow 1%, of the discriminator output).



FREQ 1E3 (+36) 10E3

For GAV

$R_{B1\ 4P} = \frac{1}{\quad} = 50\Omega$

CAPACITORS	EOL ± %	Temp ± %
CTM	.5	.48
CM	.5	.29
CK	10.0*	4.5

* CHANGE TO CTM

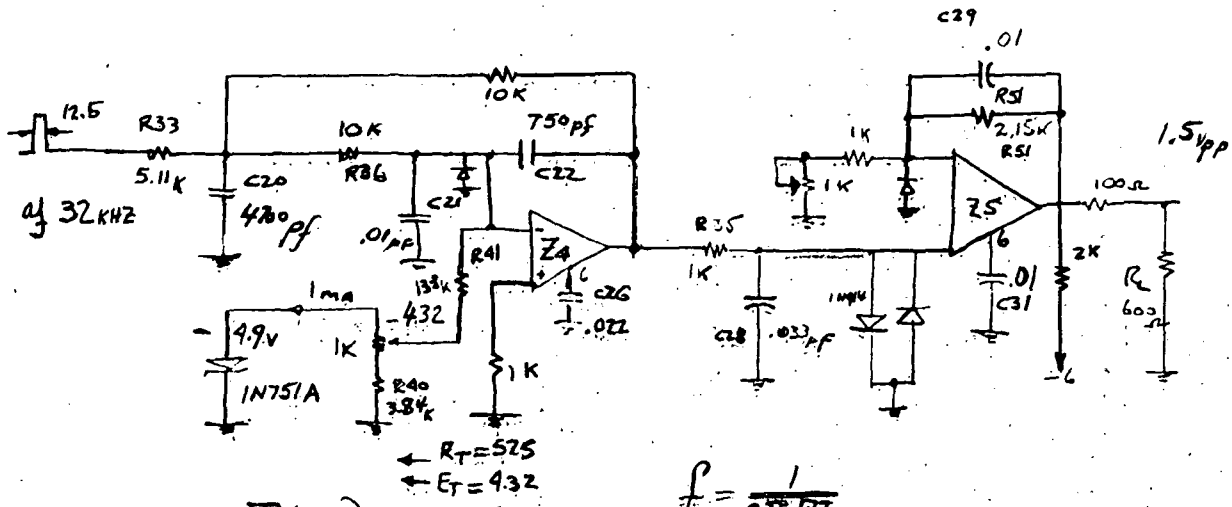
$20 \log \frac{E_2}{e_i} = GAV - 10 \log \frac{4(250)}{600}$

$= 4.8 - 2.2 = 2.6\ db$

$\frac{E_2}{e_i} = 1.35$

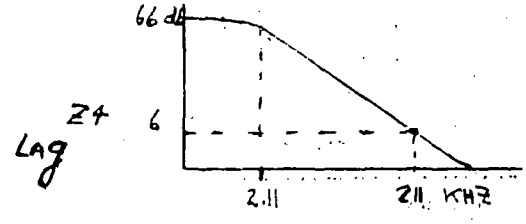
FIG 14 EMTS AUX. TRACK PLAY/BACK FILTER

Figure 4-85. Auxiliary Playback Filter

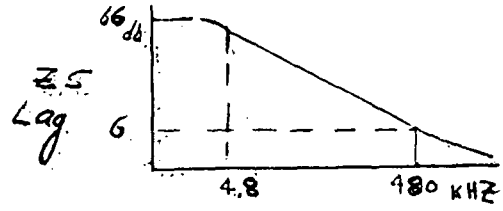


$f = \frac{1}{2\pi T}$

	T (μs)	f
$R_{33}\ C_{20}$	24	6.6 KHZ
$R_{36}\ C_{21}$	100.	1.59
$R_{36}\ C_{22}$	7.5	21.1
$R_{35}\ C_{28}$	33	4.8
$R_5\ C_{29}$	21.5	7.4
$(3.4K)^*\ C_{26}$	75	2.11
$(3.4K)\ C_{31}$	34	4.8



$G_L = 6$ db



$\bar{G}_L = 6$ dB

* Internal Values

Figure 4-86. Auxiliary Track Playback Output Filter Preliminary Pole Analysis

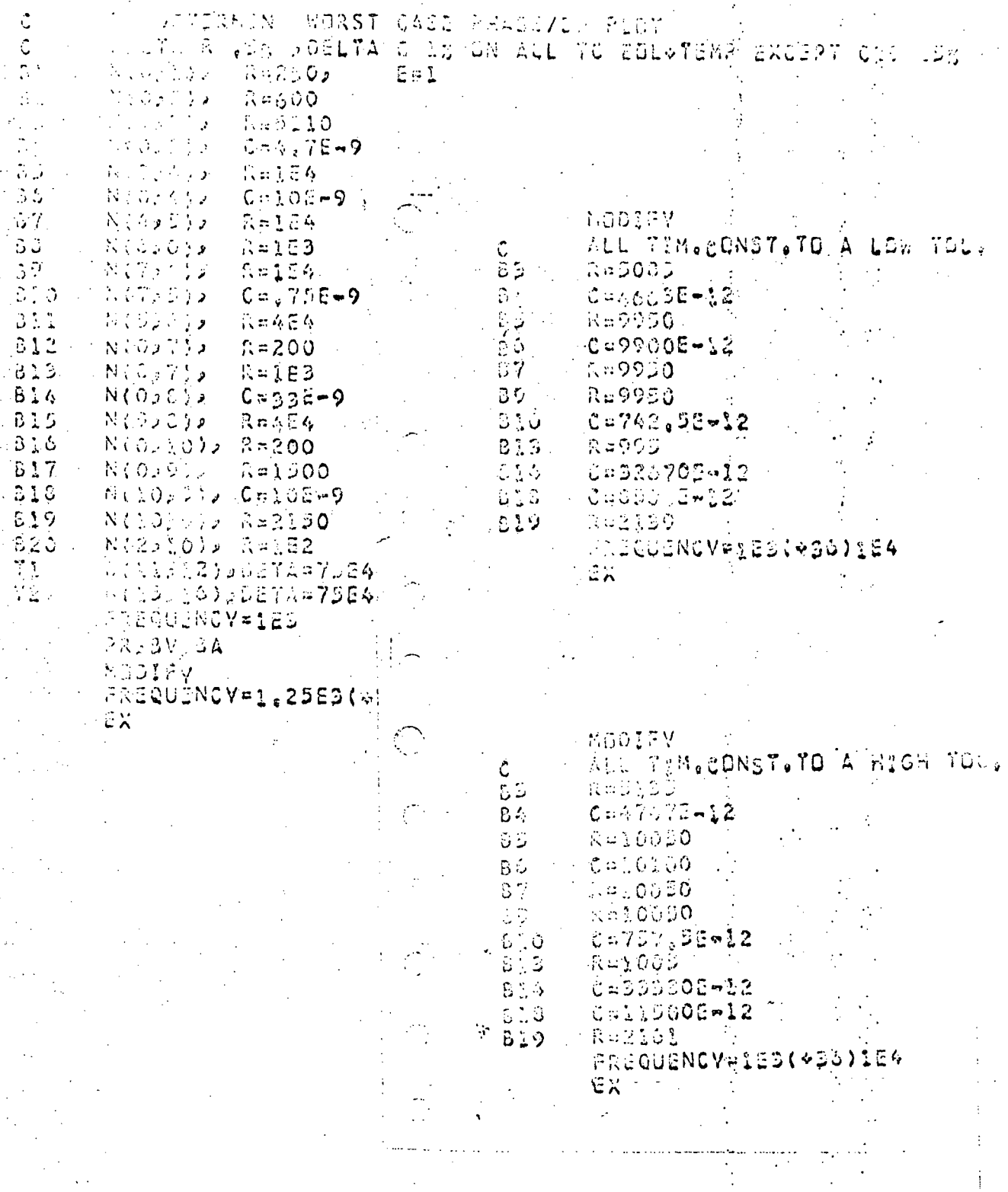


Figure 4-87 Auxiliary Track Output Filter ECAP Program (Sheet 1 of 3)

AUX,TRACK P/B FILTER (NOH, TUL)

GENERATOR RESIS,OHMS= 250.00 LOAD RESIS,OHMS= 600.00 PWR AVAIL,WATTS= 0.00
DIS,DISSIPATION LMMI,MISMATCH LOSS AT INPUT LIS,INSERTION LOSS
GPI,GAIN BASED ON INPUT PWR MAGNITUDE GAV,GAIN BASED ON AVAILABLE PWR

FREQ HERTZ	R INPUT OHMS	X INPUT OHMS	SHIFT DEGREES	INPUT VSWR	DIS WATTS	LIS DB	LMMI DB	GPI DB	GAV DB	
1.000E 03	1.459E 04	-2.363E 03	-209.31	59.88	-0.003	-5.61	11.90	16.70	4.80	-2
1.250E 03	1.432E 04	-2.879E 03	-216.63	59.59	-0.003	-5.56	11.88	16.63	4.75	
1.500E 03	1.401E 04	-3.354E 03	-223.95	59.25	-0.003	-5.51	11.85	16.55	4.70	
1.750E 03	1.367E 04	-3.784E 03	-231.28	58.86	-0.003	-5.45	11.82	16.47	4.64	
2.000E 03	1.330E 04	-4.171E 03	-238.65	58.45	-0.003	-5.39	11.79	16.38	4.58	-5
2.250E 03	1.292E 04	-4.517E 03	-246.07	58.00	-0.003	-5.33	11.76	16.28	4.52	
2.500E 03	1.253E 04	-4.823E 03	-253.57	57.53	-0.003	-5.26	11.73	16.19	4.46	
2.750E 03	1.212E 04	-5.094E 03	-261.19	57.05	-0.003	-5.20	11.69	16.09	4.39	
3.000E 03	1.171E 04	-5.332E 03	-268.97	56.54	-0.003	-5.14	11.66	15.98	4.33	-88
3.250E 03	1.128E 04	-5.539E 03	-276.95	56.01	-0.003	-5.06	11.62	15.87	4.26	
3.500E 03	1.085E 04	-5.714E 03	-285.19	55.43	-0.003	-4.98	11.57	15.75	4.18	
3.750E 03	1.040E 04	-5.855E 03	-293.74	54.78	-0.002	-4.88	11.52	15.60	4.07	
4.000E 03	9.932E 03	-5.953E 03	-302.63	54.01	-0.002	-4.75	11.45	15.41	3.94	-122
4.250E 03	9.456E 03	-6.001E 03	-311.90	53.06	-0.002	-4.57	11.39	15.15	3.76	
4.500E 03	8.983E 03	-5.989E 03	-321.52	51.90	-0.002	-4.32	11.30	14.81	3.52	
4.750E 03	8.518E 03	-5.912E 03	-331.45	50.49	-0.002	-3.99	11.18	14.36	3.18	
5.000E 03	8.068E 03	-5.772E 03	-341.58	48.84	-0.002	-3.55	11.04	13.79	2.74	-161
5.250E 03	7.710E 03	-5.583E 03	-351.75	47.02	-0.002	-2.99	10.89	13.07	2.18	-169
5.500E 03	7.390E 03	-5.360E 03	-1.77	45.12	-0.001	-2.31	10.71	12.22	1.50	+178
5.750E 03	7.131E 03	-5.123E 03	-11.48	43.26	-0.001	-1.51	10.54	11.24	0.70	
6.000E 03	6.927E 03	-4.888E 03	-20.70	41.52	-0.001	-0.61	10.37	10.17	-0.20	
6.250E 03	6.758E 03	-4.666E 03	-29.34	39.95	-0.001	0.37	10.21	9.03	-1.18	
6.500E 03	6.645E 03	-4.462E 03	-37.35	38.57	-0.001	1.41	10.06	7.85	-2.21	+143
6.750E 03	6.545E 03	-4.277E 03	-44.71	37.38	-0.000	2.48	9.93	6.65	-3.29	
7.000E 03	6.467E 03	-4.112E 03	-51.45	36.34	-0.000	3.58	9.82	5.43	-4.39	+129
7.250E 03	6.400E 03	-3.964E 03	-57.61	35.43	-0.000	4.68	9.72	4.23	-5.49	
7.500E 03	6.342E 03	-3.832E 03	-63.25	34.64	-0.000	5.78	9.62	3.03	-6.59	
7.750E 03	6.291E 03	-3.712E 03	-68.41	33.94	-0.000	6.87	9.54	1.86	-7.68	
8.000E 03	6.244E 03	-3.604E 03	-73.16	33.31	-0.000	7.95	9.46	0.71	-8.75	+107
8.250E 03	6.201E 03	-3.504E 03	-77.53	32.73	0.000	9.00	9.39	-0.42	-9.81	
8.500E 03	6.161E 03	-3.412E 03	-81.56	32.21	0.000	10.	9.33	-1.52	-10.8	
8.750E 03	6.123E 03	-3.327E 03	-85.31	31.73	0.000	11.	9.26	-2.59	-11.8	
9.000E 03	6.086E 03	-3.248E 03	-88.78	31.29	0.000	12.	9.21	-3.64	-12.8	-92
9.250E 03	6.052E 03	-3.173E 03	-92.03	30.87	0.000	13.	9.15	-4.66	-13.81	
9.500E 03	6.019E 03	-3.103E 03	-95.06	30.48	0.000	13.	9.10	-5.66	-14.76	
9.750E 03	5.987E 03	-3.036E 03	-97.90	30.12	0.000	14.	9.05	-6.63	-15.68	
1.000E 04	5.957E 03	-2.973E 03	-100.56	29.77	0.000	15.	9.00	-7.58	-16.59	+80

Figure 4-87. Auxiliary Track Output Filter ECAP Program (Sheet 2 of 3)

AUX.TRACK P/3 FILTER (LOW TOL)

FREQ HERTZ	R INPUT OHMS	X INPUT OHMS	SHIFT DEGREES	INPUT VSWR	DIS WATTS	LIS DB	LMMI DB	GPI DB	GAIN DB	
1,000E 03	1,453E 04	-2,324E 03	-208,26	59,59	-0,003	-5,60	11,83	16,67	4,79	-2
1,250E 03	1,426E 04	-2,834E 03	-215,32	59,31	-0,003	-5,56	11,85	16,61	4,76	
1,500E 03	1,396E 04	-3,303E 03	-222,39	58,98	-0,003	-5,52	11,83	16,55	4,72	
1,750E 03	1,363E 04	-3,729E 03	-229,49	58,60	-0,003	-5,48	11,81	16,48	4,67	
2,000E 03	1,327E 04	-4,113E 03	-236,62	58,19	-0,003	-5,43	11,78	16,40	4,63	-5
2,250E 03	1,290E 04	-4,456E 03	-243,81	57,75	-0,003	-5,39	11,74	16,32	4,58	
2,500E 03	1,251E 04	-4,761E 03	-251,08	57,30	-0,003	-5,34	11,71	16,24	4,53	
2,750E 03	1,212E 04	-5,031E 03	-258,47	56,82	-0,003	-5,30	11,68	16,16	4,49	
3,000E 03	1,171E 04	-5,266E 03	-266,02	56,32	-0,003	-5,25	11,64	16,08	4,44	-9
3,250E 03	1,130E 04	-5,475E 03	-273,78	55,80	-0,003	-5,20	11,60	15,99	4,39	
3,500E 03	1,087E 04	-5,652E 03	-281,78	55,24	-0,003	-5,14	11,56	15,89	4,33	
3,750E 03	1,043E 04	-5,795E 03	-290,08	54,62	-0,003	-5,07	11,51	15,77	4,26	
4,000E 03	9,980E 03	-5,901E 03	-298,72	53,88	-0,003	-4,96	11,45	15,61	4,16	-11
4,250E 03	9,516E 03	-5,960E 03	-307,73	53,00	-0,002	-4,82	11,38	15,40	4,01	
4,500E 03	9,049E 03	-5,952E 03	-317,10	51,92	-0,002	-4,61	11,30	15,10	3,81	
4,750E 03	8,592E 03	-5,904E 03	-326,80	50,60	-0,002	-4,33	11,19	14,71	3,52	
5,000E 03	8,161E 03	-5,783E 03	-336,73	49,05	-0,002	-3,95	11,06	14,20	3,14	-15
5,250E 03	7,774E 03	-5,611E 03	-346,76	47,30	-0,002	-3,45	10,91	13,56	2,64	
5,500E 03	7,443E 03	-5,400E 03	-356,72	45,46	-0,002	-2,84	10,74	12,77	2,03	
5,750E 03	7,170E 03	-5,171E 03	-6,43	43,61	-0,001	-2,11	10,57	11,87	1,30	+ 17
6,000E 03	6,953E 03	-4,939E 03	-15,72	41,86	-0,001	-1,27	10,40	10,86	0,46	
6,250E 03	6,783E 03	-4,716E 03	-24,49	40,26	-0,001	-0,35	10,24	9,78	-0,46	
6,500E 03	6,650E 03	-4,509E 03	-32,66	38,84	-0,001	0,64	10,09	8,65	-1,45	
6,750E 03	6,546E 03	-4,321E 03	-40,20	37,60	-0,000	1,67	9,96	7,48	-2,48	
7,000E 03	6,461E 03	-4,151E 03	-47,14	36,53	-0,000	2,73	9,84	6,30	-3,54	+ 13
7,250E 03	6,391E 03	-4,000E 03	-53,50	35,59	-0,000	3,81	9,73	5,12	-4,61	
7,500E 03	6,331E 03	-3,866E 03	-59,34	34,77	-0,000	4,88	9,64	3,95	-5,69	
7,750E 03	6,279E 03	-3,741E 03	-64,69	34,04	-0,000	5,95	9,55	2,80	-6,75	
8,000E 03	6,231E 03	-3,630E 03	-69,62	33,39	-0,000	7,00	9,47	1,66	-7,81	+ 11
8,250E 03	6,188E 03	-3,528E 03	-74,16	32,81	-0,000	8,04	9,40	0,55	-8,85	
8,500E 03	6,147E 03	-3,435E 03	-78,37	32,28	0,000	9,06	9,33	-0,53	-9,87	
8,750E 03	6,103E 03	-3,3[illegible]E 03	-82,27	31,79	0,000	10,06	9,27	-1,60	-10,87	
9,000E 03	6,072E 03	-3,[illegible]E 03	-85,90	31,33	0,000	11,04	9,21	-2,63	-11,85	-
9,250E 03	6,037E 03	-3,[illegible] 03	-89,29	30,91	0,000	12,00	9,16	-3,65	-12,8[illegible]	
9,500E 03	6,004E 03	-3,[illegible] 03	-92,46	30,52	0,000	12,93	9,10	-4,64	-13,74	
9,750E 03	5,972E 03	-3,[illegible] 03	-95,43	30,15	0,000	13,85	9,06	-5,60	-14,66	
1,000E 04	5,942E 03	-2,[illegible] 03	-98,23	29,80	0,000	14,75	9,01	-6,55	-15,56	

Figure 4-87. Auxiliary Track Output Filter ECAP Program (Sheet 3 of 3)

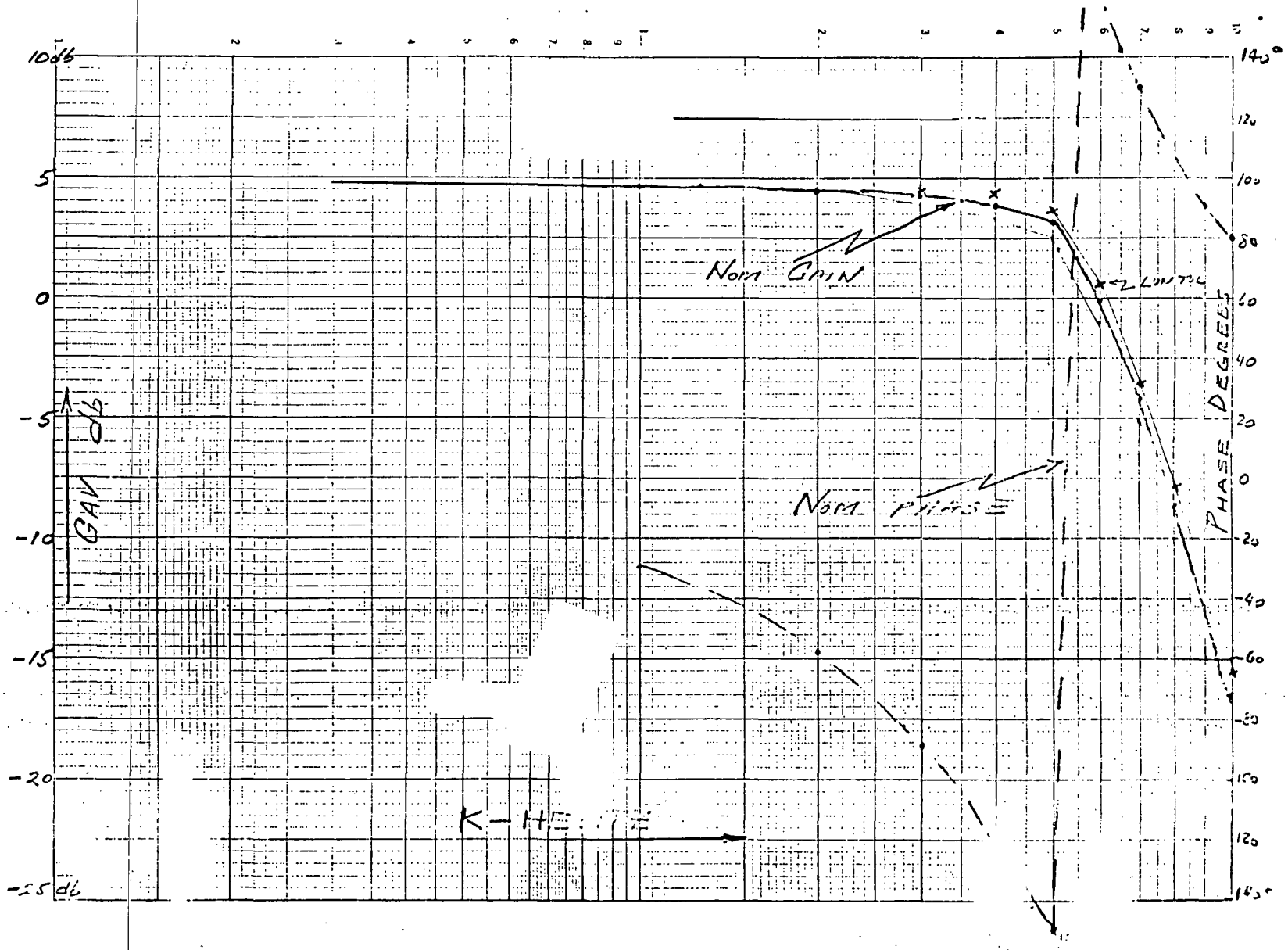


Figure 4-88. Auxiliary Track Output Filter Response

```
        DC
C       TO DETERMIN ADEQUACY OF BIAS ADJ.
C       ERTS AUX.TRACK OUTPUT STG Z4
B1      N(0,1),  R=50,      E=1.28
B2      N(2,0),  R=500,     E=4.9
B3      N(1,3),  R=15110
B4      N(0,2),  R=4.33E3
B5      N(4,2),  R=133E3
B6      N(3,4),  R=10E3
B7      N(4,6),  R=40E3
B8      N(6,0),  R=1E3
B9      N(5,3),  R=1E4
B10     N(5,0),  R=200
B11     N(0,5),  R=1E4
T1      B(7,10), BETA=75E4
        PR,NV
        EX

NODE VOLTAGES

NODES                    VOLTAGES

  1-  4      0.12768637D 01   -0.43779983D 01    0.32916351D 00   -0.70507808D-0
  5-  6      0.31133457D-01   -0.17197019D-06
                      21.1 MV

        MODIFY
B2      R=1E3
B4      R=3.83E3
        EX

NODE VOLTAGES

NODES                    VOLTAGES

  1-  4      0.12767360D 01   -0.38624769D 01    0.29044085D 00    0.22021863D-0
  5-  6     -0.71883581D-01    0.53711835D-06
                     -71.8 MV

        MODIFY
B2      R=1
B4      R=4.83E3
        EX

NODE VOLTAGES

NODES                    VOLTAGES

  1-  4      0.12769928D 01   -0.48989485D 01    0.36829394D 00   -0.36429579D-
  5-  6      0.13523534D 00   -0.88852592D-06
                      135MV
```

Figure 4-89. Worst Case Output Bias Drift

The results of the worst case analysis indicate an output drive of ±113.6 mV peak.

The contributions of drift in the output filter due to variation of the four parameters as depicted from the ECAP sensitivity analysis (Figure 4-90) are summarized in Table 4-24.

TABLE 4-24. AUXILIARY TRACK OUTPUT FILTER DRIFT SUMMARY

Parameter	Output Drift (peak mV)
Bias change of 1% (VR2)	18.2
Bias Current	
Z4 (uA702)	30.0
Z5 (uA702)	2.0
Resistor Tolerances	28.4
Input Drift	35.0
Total	113.6 mV peak

4.2.3.3 Summary. - Analysis of the Auxiliary Track has shown that the design of the circuit is basically sound after a few circuit corrections were made as a result of this review. The major caution to be noted is the amount of dc drift that could theoretically occur; referenced to the output signal the drift is 89 mV due to the record portion and 114 mV due to the playback portion of the equipment.

4.2.3.4 Test Results (Breadboard). - A point by point plot of the deviable multivibrator frequency vs. input dc voltage exhibits good linearity over the entire range. A test of frequency stability vs. temperature shows a possible shift of ±1% of the nominal frequency. A worst shift of ±0.4% in frequency by a possible change of one of the supply voltages was noted. A breadboard of the Auxliary Channel playback circuit was also temperature cycled while a signal from the recording circuit was applied to the input on a back-to-back basis (less head and preamplifier). A possible shift of the output DC base line of about 15 mV (1% of 1500 mV) was noted.

The frequency response of the low pass filter in the playback circuit which rejects the carrier frequencies is shown in Figure 4-91.

Resistor No. Branch	Comp. Tolerance Δ%	$\frac{\partial V_1}{\partial R_j}$ / 1% +	−	× Δ% +	−
1	0	0		0	
2	1		1.9		1.9
3	.5	13.0		6.5	
4	1	1.8		1.8	
5	.5		18.0		9.0
6	.5	11.3		5.7	
7	0		0		0
8	.5		0		0
9	.5		6.2		3.1
10	0	0		0	
11	.5		0		0
12	0	0		0	
13	0		0		0
14	.5		.4		.2
15	.5	.4		.2	
16	.5		0		0
17	1	0		0	
				14.2	14.2

$$\Sigma \left| \frac{\partial V_o}{\partial R_j} \right| \times \Delta\% = 28.4$$

$$\left| \frac{\partial V_o}{\partial V_1} \right| \times \Delta\% = 35.0$$

$$\left| \frac{\partial V_o}{\partial V_2} \right| \times \Delta\% = 18.2$$

Offset due Currents ΔI_o

$\partial V_o / Z_1 = .592 \times 10^5 (.5 \times 10^{-6}) = 30.0$

$\partial V_o / Z_2 = .392 \times 10^4 (.5 \times 10^{-6}) = 2.0$

$113.6 \Rightarrow 114_{mv}$

Figure 4-90. Output Drift Due to EOL Parameter Variation (from ECAP Sensitivity Analysis)

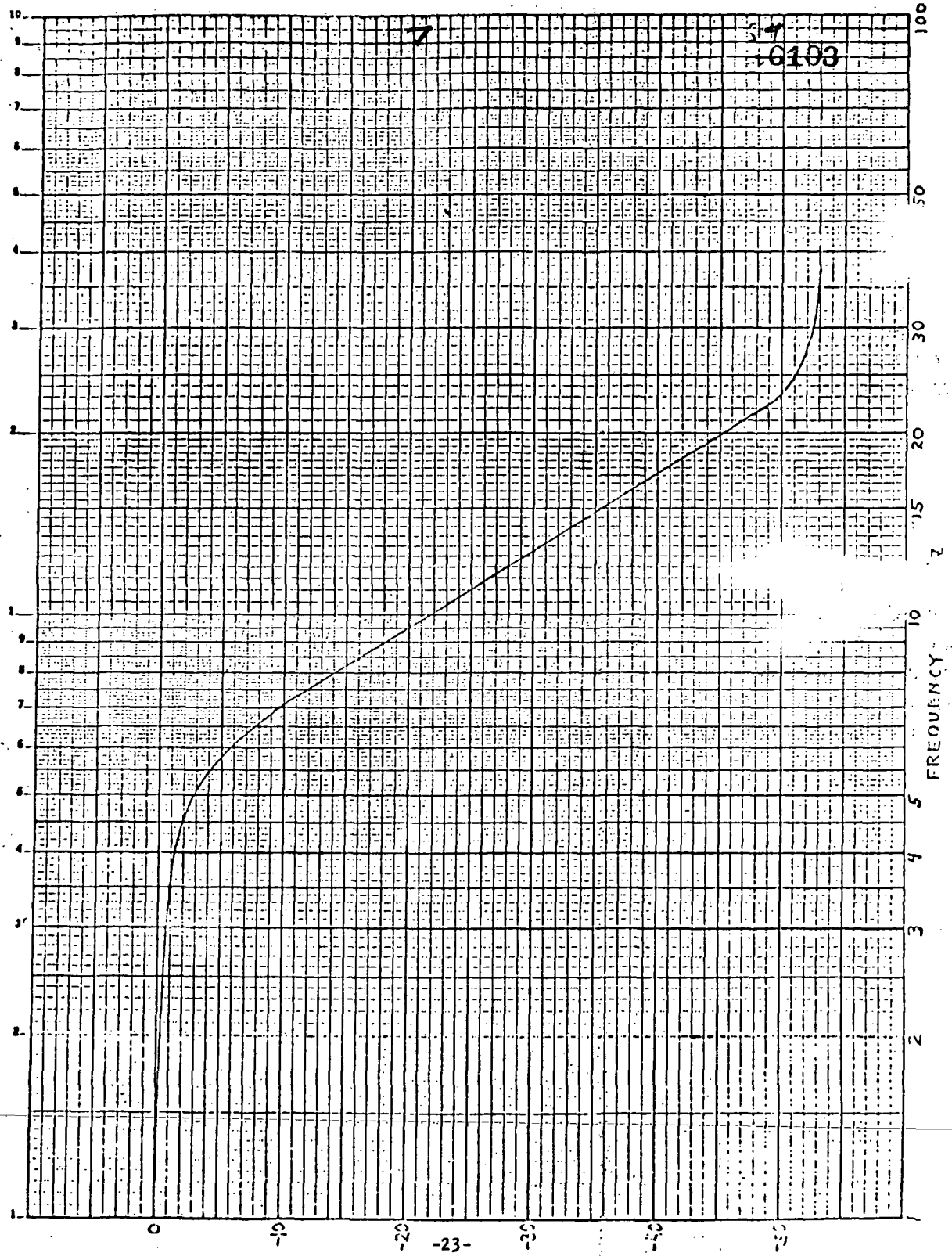


Figure 4-91. Low Pass Filter Frequency Response

A fixed head assembly head was made for the longitudinal tracks. One of the heads was made for the Auxiliary Channel and had the following characteristics:

Gap:	250 microinches
Track:	30 mils
Inductance:	22 ±3 mH at 1 kHz
DC Resistance:	39 ±5 ohms

By varying the bi-directional recording current at a 16 kHz rate, experimental tests showed the optimum record current for maximum playback signal was ±1 mA, as shown in Figure 4-92. However, a 0.5 mA current provided inadequate erasure capabilities; so it was felt that a ±2 mA record level would be a better choice.

4.2.4 Search Channel Worst Case Analysis. -

4.2.4.1 Preamplifier. - The performance of the preamplifier has been summarized in the Design Study Report, Volume I.

4.2.4.2 Threshold Detector. - A uA710 comparator, Z1 and Z3, subassembly are used as threshold detectors for the search track "0" and the search track "1" input signal respectively. The threshold "high" or "low" is preset by the command logic through a relay contact which is either 5.6 vdc or ground depending upon the speed of the tape. It has been estimated that the ratio of the signal amplitudes of the play-back high speed to low speed tape is approximately 3.5 to 1.

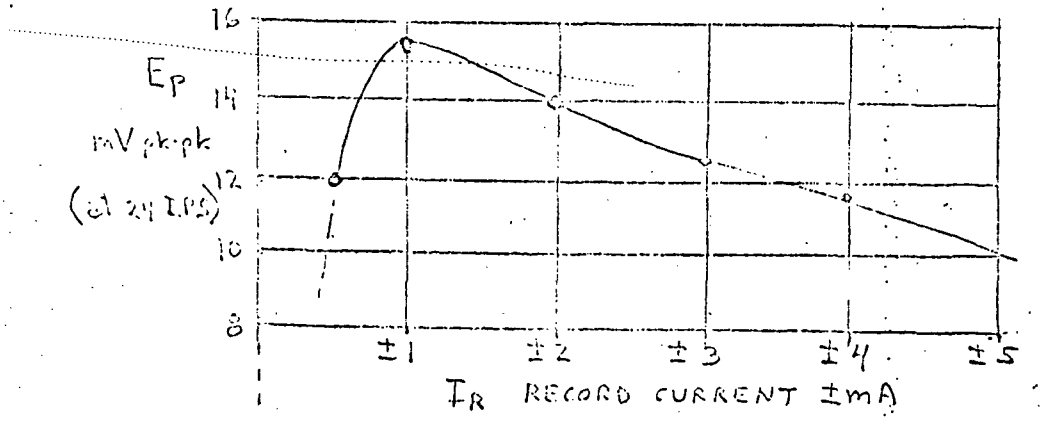


Figure 4-92. Record Head Current vs Playback Voltage

The schematic diagram of the search track threshold detector is shown on Figure 4-93.

When control signal V_2 is "low", the dc threshold:

$$V_{TL} \cong \frac{V_3 (R_5 \text{ 11 } R_6)}{R_4 + (R_5 \text{ 11 } R_6)} = \frac{12\ (0.97)}{21.5 + 0.97} = 0.51V$$

And when the control signal V_2 is "high," the dc threshold is calculated as follows:

$$\frac{(V_2 - V_{TH})}{R_5} + \frac{(V_3 - V_{TH}}{R_4} - \frac{V_{TH}}{R_6} = 0$$

$$V_{TH}\left[\frac{1}{R_5} + \frac{1}{R_4} + \frac{1}{R_6}\right] = \left[\frac{V_2}{R_5} + \frac{V_3}{R_4}\right] = 2.6 + 0.56 = 3.16 \text{ mA}$$

$$V_{TH} = \frac{3.16 \text{ mA}}{[0.464 + 0.046 + 0.562] \text{ millimhos}} = \frac{3.16}{1.072} = 2.95V$$

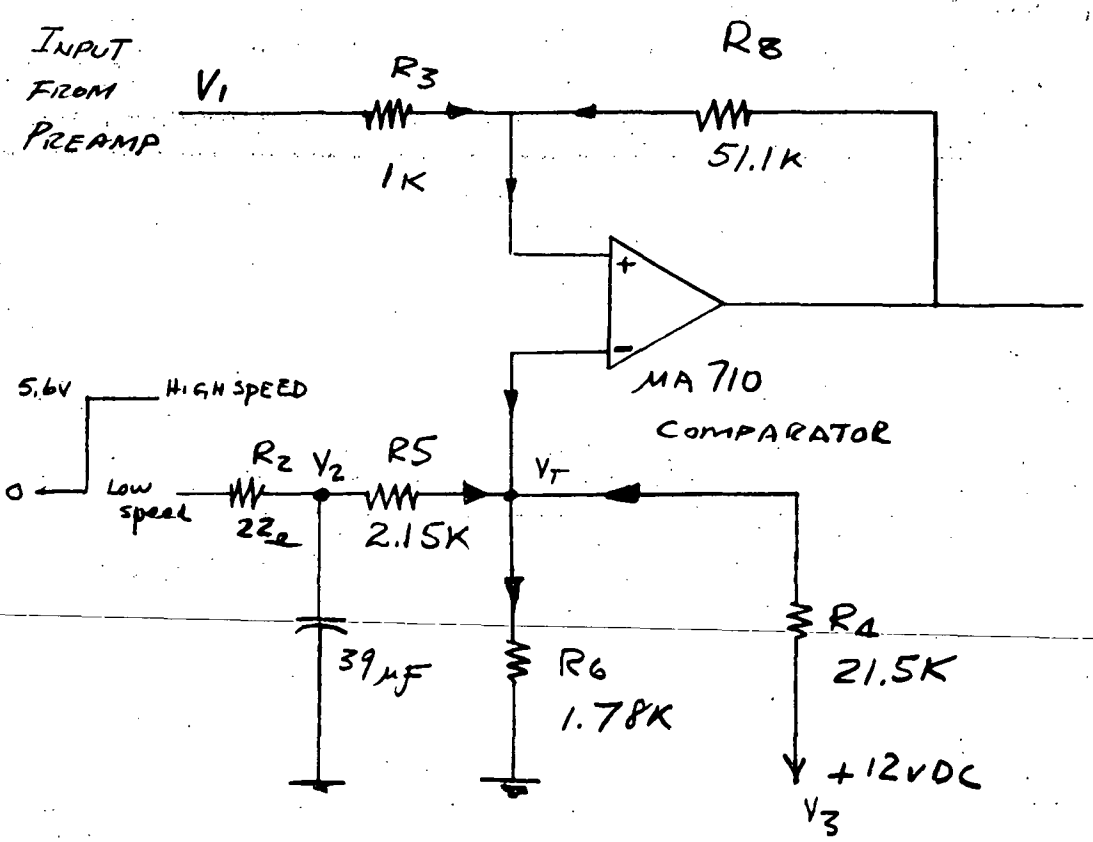


Figure 4-93. Search Track Variable Threshold Detector

The high speed threshold is thus only 0.55 volts below maximum peak input which is assumed to be 3.5 volts peak. Considering that the ΔV_{TH} may go up 10%, e.g. V_{TH} = 3.3 volts, and considering that the offset of the pre-amp stage and its gain is minimum, the V_{HT} may have to be reduced to:

$$V_{TH} \leqq \left[V_{IN}\, G - \Delta\overline{Vo}\right] \quad G \rightarrow 54 \text{ dB}$$

$$= \left[6.0 \times 10^{-3} (505)\ (1 - 0.1)\ -0.127\right]$$

$$= 2.59 \text{ Volts}$$

The low speed signal threshold seems to have a sufficient margin toward the peak input of 1.0 volt.

However, the reduction of V_{TH} should be done judiciously and in relation to V_{TL}. Reducing R6 to 1.2 k ohms is recommended.* The V_{TL} will, then, be reduced to approximately 0.415 Vdc, also improving the margin to the minimum low speed peak signal.

It is also advisable to increase R_2 to 100 ohms,* in order to reduce the surge through the relay contact which supplies high/low speed bias control.

To improve noise immunity, the threshold comparator utilizes a positive feedback via a 50 k ohm resistor. This creates a hysteresis which according to the application notes shall not be less than 5 millivolts in order to prevent oscillation thus:

$$H = \frac{R_1\,[Vo - Vo]}{R_1 + R_2} = \frac{1}{50}\,[4.0 - (-0.5)] = 90 \text{ mV}$$

which is adequate

4.2.4.3 Pulse Generators (Z2 and Z4). - Two one-shots, uA9601, are used in each "0" and "1" track of the search channel to generate a fixed pulse width after a negative transition of the threshold comparator output. The equivalent waveform analysis is as follows (see Figure 4-94):

The output pulse width is:

$$T = 0.32\, R_{10}\, C_5 \left[1 + \frac{0.7}{R_{10}}\right]$$

*The recommendations have subsequently been implemented.

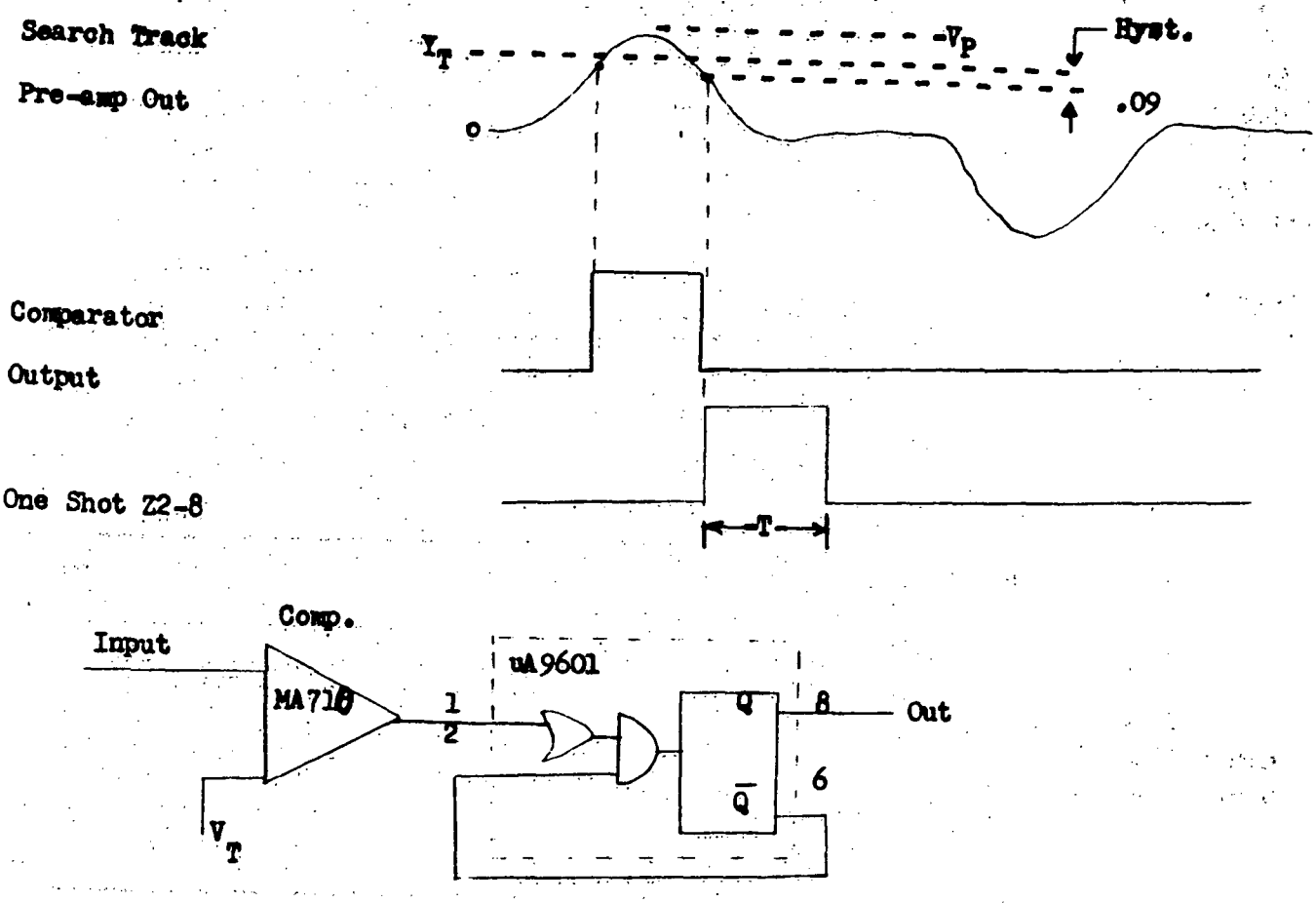


Figure 4-94. Search Track Detection Waveforms

where R_{10} = 11k ohms ±1%

C_5 = 15,000 pF

$T = 52.7 \times 10^3 [1 + 0.0635]_{us} = 56$ us

Since it is assumed that the maximum bit rate to be associated with the ERTS search track is 2.5 kb/s, corresponding to 400 microseconds per bit, it is sufficient to say that the pulse width variation of as much as ±10% is not critical in the performance of the search track; that is, including the mechanics of the output decoder, which is not a part of this equipment. It should be mentioned that a negative-feedback, pin 6 to pin 2 of the uA9601, is used primarily to prevent output pulse stretching due to the possibility of retriggering by an occasional noise source appearing at pin 1, the occurence of which is highly unlikely. The device, however, in no way relates itself to the reduction of error rates.

4.2.4.4 Output Combiner. - The purpose of the output stage on the playback search track subsystem is to combine binary "0" and "1", which are processed by two separate one-shots into a composite bipolar signal. The design approach assures that the logical "1" is represented by a positive excursion of 0.75 volts peak and the logical "0" is represented by a negative excursion of -0.75 volts peak nominal. The width of each excursion is determined by the time constants of the two one-shots. The output performance is as shown in Figure 4-95.

where:

V_R = 0 ±0.2 volts dc

A_1 = 0.75 volts peak ±20%

A_0 = 0.75 volts peak ±20%

Pw_2 = 56 microseconds ±10%

Pw_2 = 56 microseconds ±10%

Since the output information is in a digital format it seems that whatever the nature of the decoding device for the composite search track signal the decoder is provided with a comfortable threshold margin.

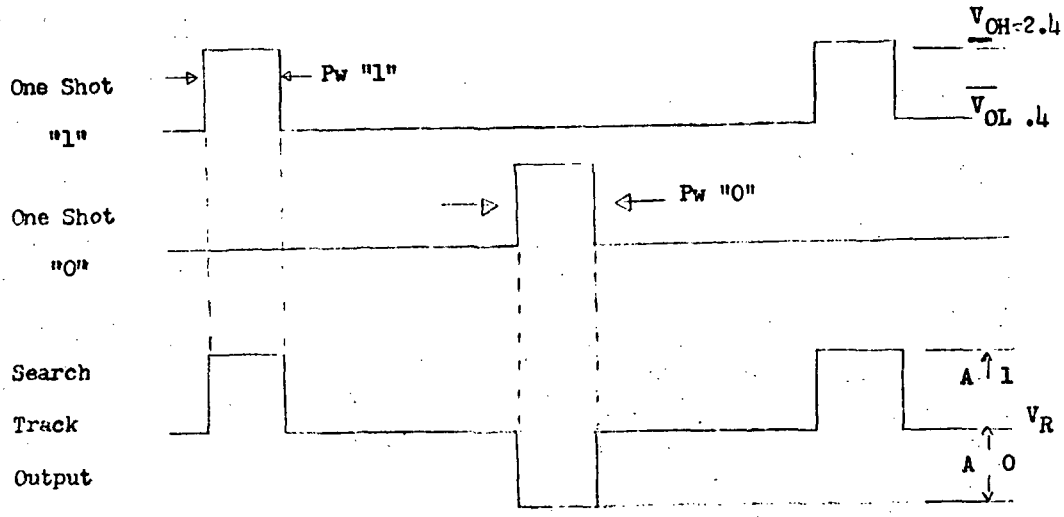


Figure 4-95. Output Combiner Waveforms

4.2.4.4.1 Modified Output Combiner. - If the output voltage range from ±0.2 volts minimum to ±0.95 volts maximum were allowable, the following circuit modification is suggested. The two potentiometers R13 and R33 used in the original design are excluded, and the output combining circuit is modified (see Figure 4-96).

The variation of the baseline at the output of the combining amplifier is a function of two basic parameters: (a) the differential bias current of the uA702C ΔI_d, which is ±3 uA; and (b) the difference between the V_{OL} of the two one-shot multivibrators ΔV_{OL}, which is 0.1 volt worst case.

Thus, the variation of the baseline:

$$\Delta V_3 = V_{OL}\,[G(1 \pm G)] \pm \Delta I_d\,(R_1)$$

$$= 0.1\ (2)\ (1 \pm 0.04) \pm 3 \times 10^{-6}\ (10^4)$$

$$= \pm 0.238 \text{ volts dc}$$

which transfers to the 600 ohms load as:

$$\Delta V_R = \pm 0.238 \left(\frac{R_L}{R_5 + R_L} \right) = \pm 0.238\ \frac{6}{7} = \pm 0.2V$$

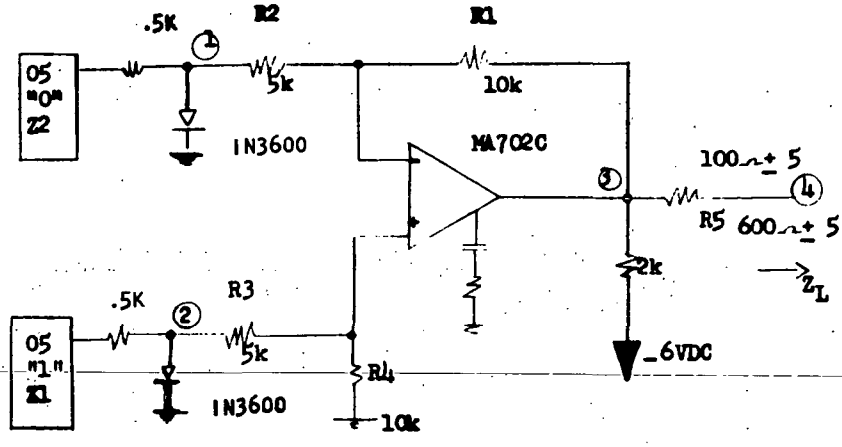


Figure 4-96. Modified Output Combiner

The variation of either of the information levels A_o or A_1 (see Figure 4-94) is primarily a function of the maximum and minimum differences between the clamping diode (V_d) IN3600 and its counterpart V_{OL} or the saturation level of the uA9601.

IN3600 Diode	uA9601
$\overline{V}_d = 0.63$ V	$V_{CE} = 0.2$V at 1.0 mA
$\underline{V}_d = 0.57$ V	$V_{CE} = 0.1$V

$$\overline{A}_1 = \overline{A}_o = [V_d - V_{OL}]\, G$$

$$= [0.63 - 0.1]\, 2\, (\tfrac{6}{7})\, (1 + 0.04)$$

$$= 0.53\ (1.78) = 0.95 \text{ volts}$$

and

$$\underline{A}_1 = \underline{A}_o = [V_d - V_{OL}]\ G$$

$$= [0.57 - 0.2]\ 2\ (\tfrac{6}{7})\ (1 - 0.04)$$

$$= 0.37\ (1.64) = 0.605 \text{ volts}$$

The gain from digital "1" one-shot and the gain from digital "0" one-shot as viewed from the output of the signal combiner are made to be equal; for example, the gain from digital "1" one-shot is:

$$G\ \text{"1"} = \left[\frac{R_1 + R_2}{R_2}\right] \cdot \left[\frac{R_4}{R_3 + R_4}\right] = 2$$

by choice of [R1 + R2] = [R3 + R4] to within ±2% EOL, and the gain from digital "0" one-shot is also:

$$G\ \text{"0"} = \frac{R_1}{R_2} = 2$$

Thus from the above analysis it seems feasible to eliminate two potentiometers. The amplitude clamping diodes assure a minimum output which is independent of V_{OH} parameter variation of the uA9601 retriggerable monostable multi-vibrator.

The variation of the differential gain of the circuit shown in Figure 4-96 is derived and calculated as follows:

$$G_{(1-4)} = G_{(2-4)} = G \left[\frac{R_1}{R_2} \quad \frac{R_L}{R_L + R_5} \right]$$

$$\frac{\partial G}{\partial R_1} = R_2 \frac{R_L}{(R_L + R_5)} = \frac{0.6}{2\,(0.6 + 0.1)} = 0.428$$

$$\frac{\partial G}{\partial R_2} = \frac{R_1}{R_2} \left(\frac{R_L}{R_L + R_5} \right) = \frac{10\,(0.6)}{25\,(0.7)} = 0.34$$

$$\frac{\partial G}{\partial R_5} = \frac{R_1}{R_2} \frac{R_L}{(R_L + R_5)^2} = \frac{10}{5} \frac{(0.6)}{0.49} = 2.45$$

$$\sum \frac{\partial G}{\partial R} = 3.22$$

Assuming EOL $\Delta R = \pm 1.25\%$

$$\overline{\Delta G} = \pm 1.25\,(3.22) = \pm 4.0\%$$

Thus the recommended design shall meet the limits of the original specification more reliably.

4.2.4.5 Summary. - The circuit design of the Search Track has been reviewed. After some suggested circuit changes, the performance of this signal channel has been found to give performance within the range of specifications.

4.3 Timing and Gating Circuits

The primary timing reference to the ERTS recorder system is the spacecraft clock signal. This signal, as indicated in Figure 4-97, is used to drive the headwheel and Iω motors in all operating modes. Since these are synchronous motors, their average speed will be completely synchronous to the spacecraft clock. However, synchronous motors do have a basic hunting frequency which, for the ERTS recorder, will be at about 5.5 Hz with a peak to peak amplitude of 5 us (record and playback). The phase relationship between the spacecraft clock and the headwheel itself will be completely random, so that a tone wheel system is required to accurately determine the position of the video heads with respect to the tape. A tonewheel processor is used to derive from the tonewheel all the internal timing and gating required to accommodate the transverse scanning system. The tonewheel processor also generates the camera re-phase signal which is required to synchronize the RBV camera beam scan with the recorder head scan.

During recording, the synchronous capstan motor is driven directly from the reference generator. However, during playback, the speed and phase of the capstan is controlled by a capstan servo system. The primary input to the servo is a signal derived from a control track, which had recorded a tonewheel signal on the tape during the record operation. These two signals determine the exact capstan phase and will assure that the information which was recorded by each transverse scanning head is played back by the identical head.

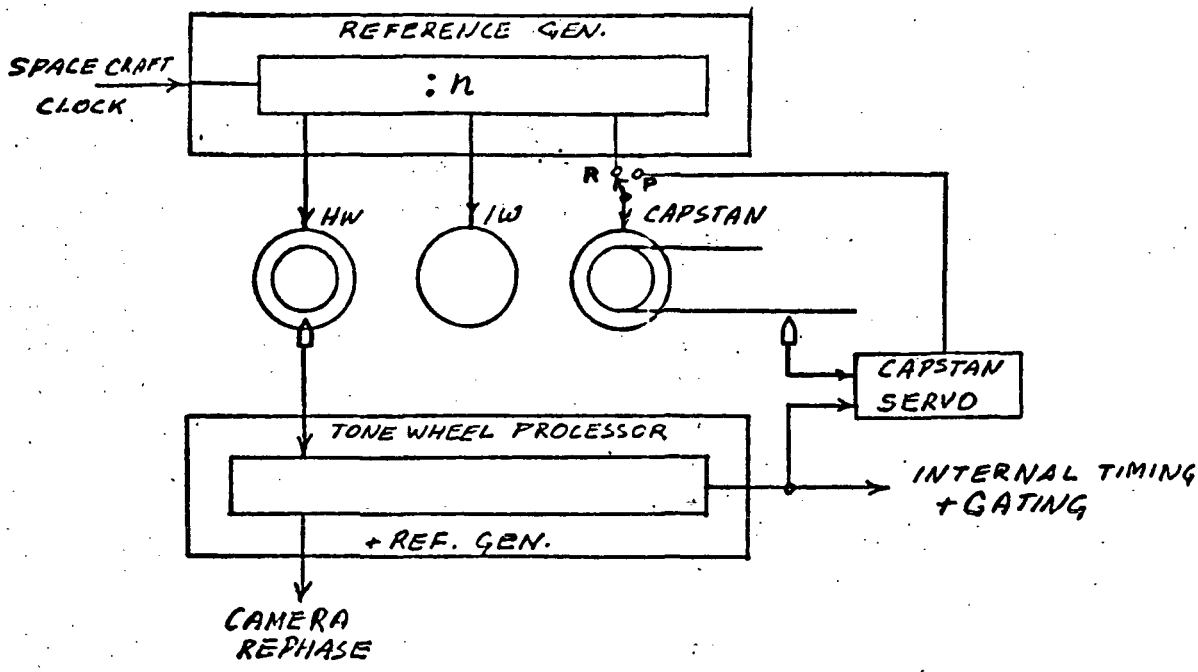


Figure 4-97. Basic Timing System

Operation of the reference generator and tonewheel processor is discussed in the following paragraphs. Figure 4-98 shows overall timing waveforms and their relationships to the wideband signals. The stability of the RBV and MSS output signals are summarized in Table 4-25.

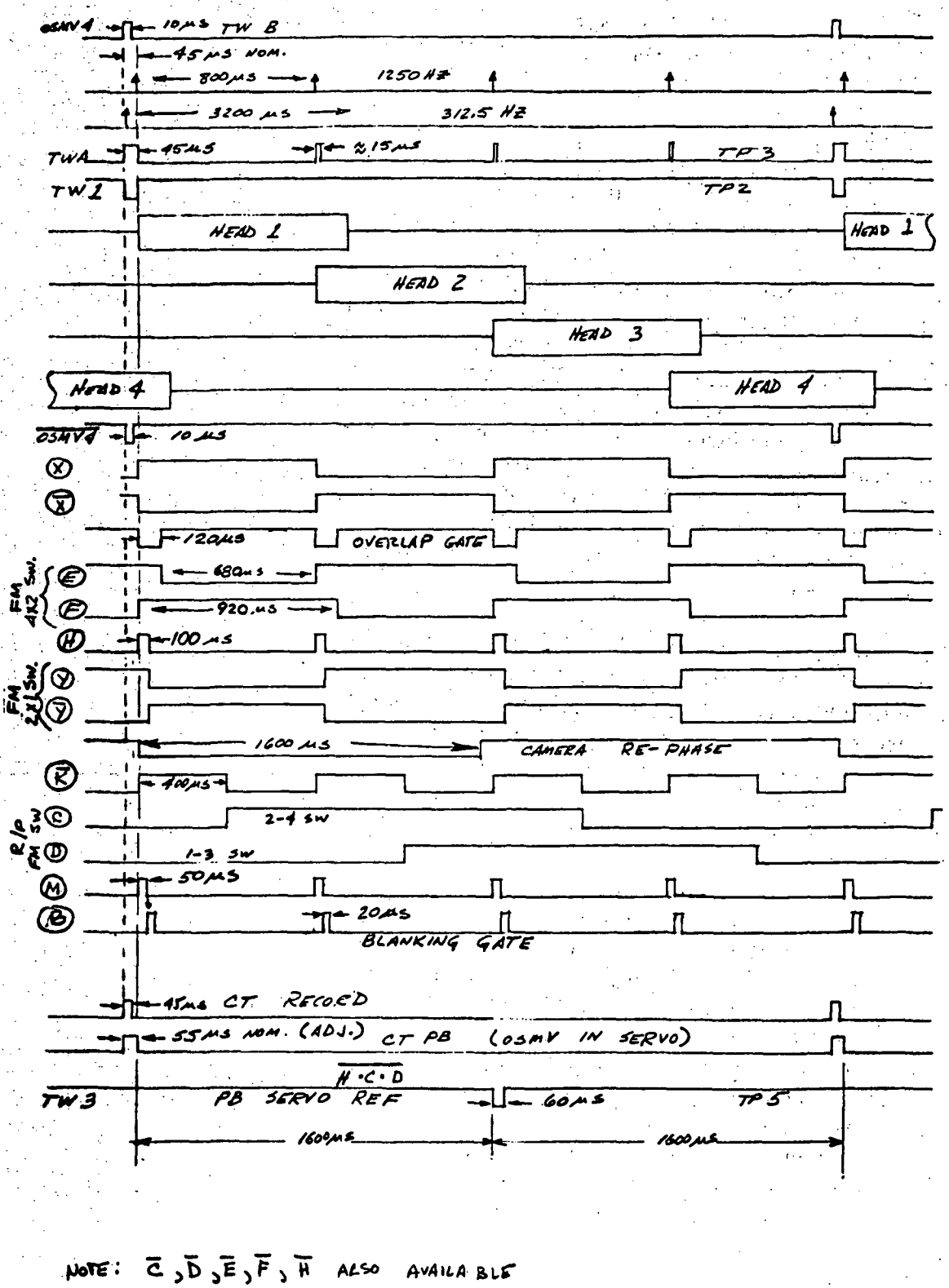
4.3.1 Reference Generator Circuit Description. - The Reference Generator may be divided into two separate functions. The first part consists of the generation of various timing waveforms which are derived from a 50 kHz signal obtained from the spacecraft clock (see Figure 4-99). This signal is transformer-coupled, bandpass filtered and then amplified. This output is low-pass filtered, buffered and fed to the Motor Auxiliary Circuit for the telemetry circuits measuring the currents. In addition, the output signal goes to a binary divider where it is divided by 10. The 5 kHz signal is further divided by 4 to generate a 1250 Hz signal for the headwheel driver. The 5 kHz signal is also applied to a divide by 5 stage, and the resulting 1 kHz signal is subjected to a gating function. This function selects the 1 kHz signal derived from the spacecraft clock in the record mode or the 1 kHz signal from the capstan servo in the playback mode. The selected 1 kHz signal is further divided by 4 to generate the 250 Hz output required by the capstan driver in record and playback. For the forward or wind tape speeds, the required 1 kHz signal is directed to the capstan without experiencing the last divide by 4 operation.

The second portion of the reference generator operates upon the processed TW (tonewheel) signals, TW1 and TWA, which are used to provide the required video/FM gating functions and to generate the camera re-phasing signal. TWA occurs at a 1250 Hz rate, corresponding to one pulse per quarter revolution of the headwheel; TW1 occurs once every revolution of the headwheel, or at a 312.5 Hz rate. The detailed timing functions required during record and playback are referenced to TWA, whereas TW1 is used for resetting the Reference Generator digital logic and to provide the camera re-phase signal.

Basically, the timing functions derived from TWA are of three types: first, the switching levels generated for multiplexing the FM channels during record and playback; second, the 4X2 FM switching signals used to perform the "fill-in" functions; and third, a playback reference signal, TW3, generated for the capstan servo.

4.3.2 Tonewheel Processor Circuit Description. - The Tonewheel Processor (Figure 4-100) is triggered by the TW pulse, which is generated by a tonewheel mounted on the rotating HW (headwheel) shaft. After processing, the signal is used to provide a pulse for synchronizing various timing functions during recording. In order to maintain a reference for use during playback, the TW pulse is recorded longitudinally on a separate control track. An additional function of the TW processor is to provide a HW speed monitoring level to the TM (telemetry) channels.

4.3.3 Reference Generator Worst Case Analysis. - The Reference Generator network has been analyzed to ensure reliable operation under ERTS system environmental requirements. Performance limitations due to component and semiconductor



NOTE: $\overline{C}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{H}$ ALSO AVAILABLE

Figure 4-98. ERTS Timing Diagram

TABLE 4-25. SUMMARY OF TIME BASE ERRORS AT VTR OUTPUT

Source	TIME BASE ERROR	
	RBV Mode	MSS Mode
1. 50 kHz Spacecraft	±1 in 10^5	±1 in 10^5
2. MSS Bit Clock		±4 in 10^5
3. Headwheel Hunting	±1 in 10^4	±1 in 10^4
4. Shoe Error	±50 nanosecond discontinuity @ 1250 Hz (synchronous)	
5. PLO Tracking Error		±10 nanoseconds @ 1250 Hz Rate
6. Output Clock Jitter		±3 nanoseconds/66.7 nanoseconds

parameter manufacturing tolerances and aging effects were determined. Worst case loading of the output signals was computer, and interfacing requirements were specified. (See Appendix H for analysis criteria.)

When the headwheel is running at normal speed, an ac tonewheel signal is produced every 800 us. As shown in the timing diagram of Figure 4-101, the beginning of each HW revolution is indicated by a change in TW signal phase.

In the processing circuit, the TW input signal is split into a positive-and a negative-going pulse. The negative-going pulse feeds one differential comparator and the positive-going signal feeds a second one. As shown in the timing diagram of Figure 4-101, each comparator output is then NANDed with a 200 us pulse in two NAND gates. The result is a negative-going pulse which occurs once very HW revolution (every 3200 us at normal speed) at one output, and a negative-going pulse for each TW signal (every 400 us at normal speed) at a second output. A 45 us negative pulse input to the control track record amplifier is provided by a multivibrator. The processor also provides analog telemetry circuits to indicate the speed of the headwheel motor.

4.3.3.1 Design Considerations. - In order to provide reliable record and playback timing signals over the required system temperature range and operating lifetime, a number of important design factors were considered.

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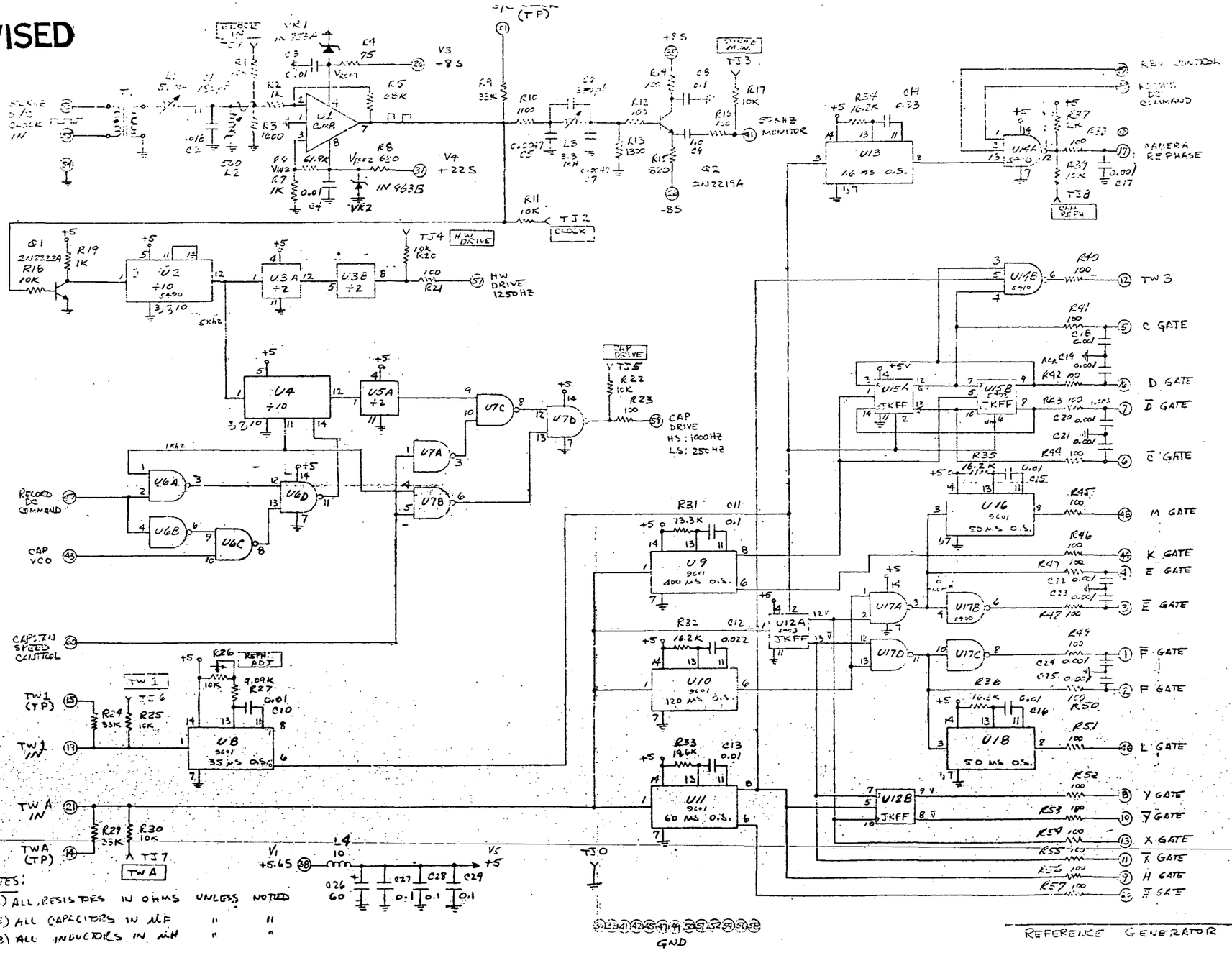

Figure 4-99. Reference Generator Schematic Diagram

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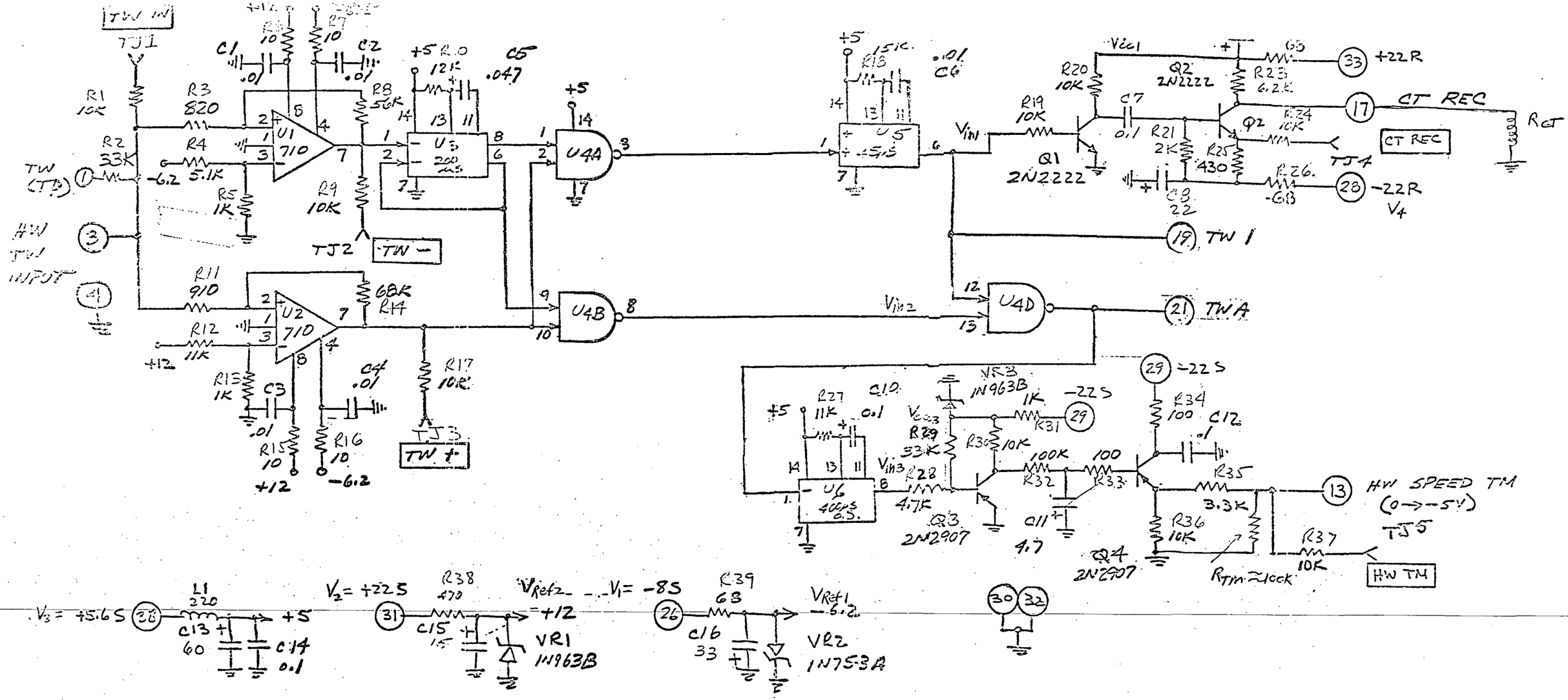

Figure 4-100. TW Processer Schematic Diagram

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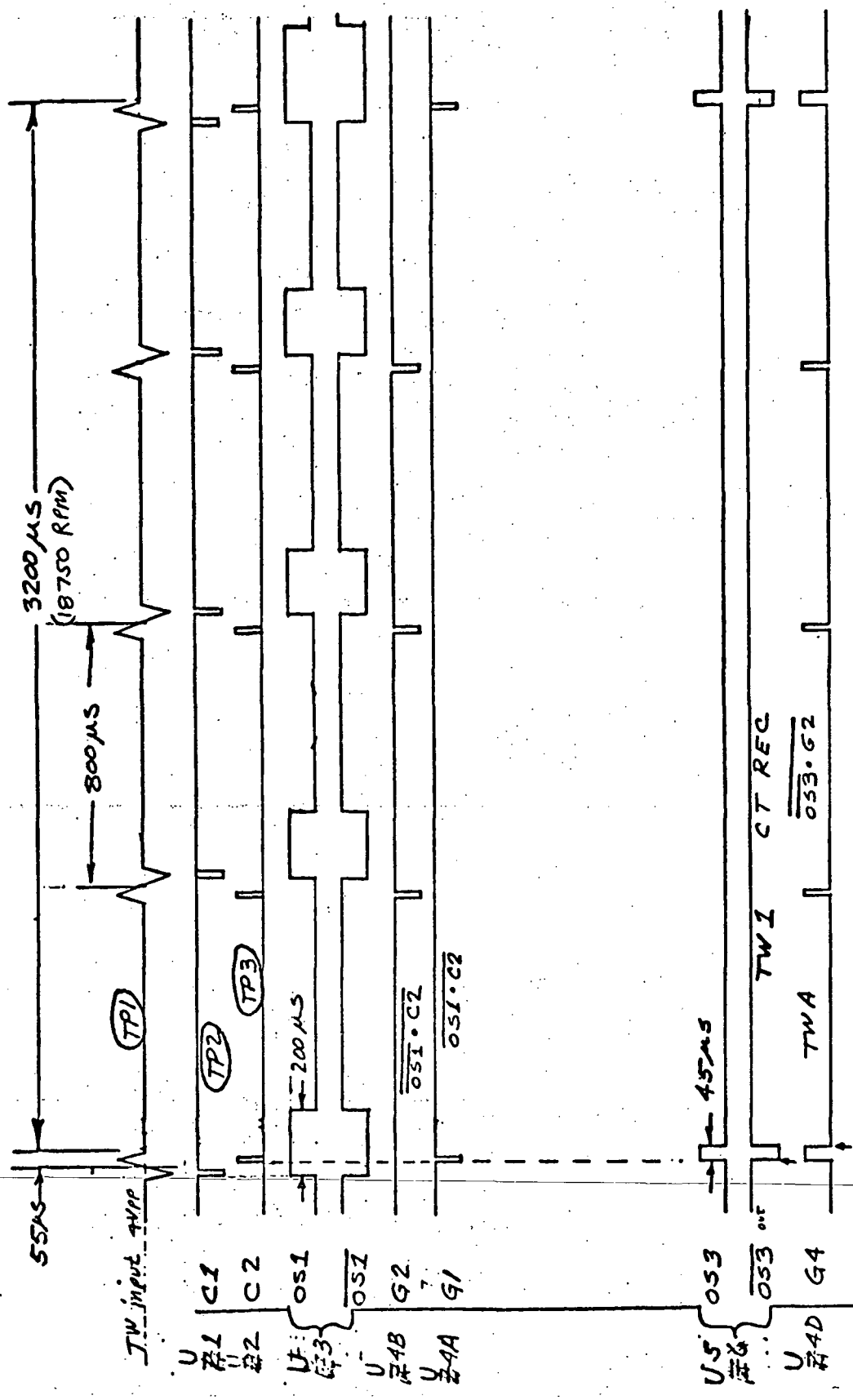

Figure 4-101. Tonewheel Processor Timing Diagram

In processing the 50 kHz space craft clock signal, the variation in filter characteristics, differential comparator reference level, and transistor buffer amplifier bias and on-off stability were determined. In addition, the TTL divider and gating logic input/output loading requirements were analyzed.

Although the timing signal pulse widths generated from the tonewheel reference (TWA and TW1), are not critical, the overall pulse width variation was calculated, along with the resulting effect on FM switching. Since each gating signal is terminated with an RC circuit, to minimize transmission line crosstalk, a critical analysis of all output loading was required. The effects of both the source gate current loading and the output circuit current loading and voltage threshold requirements were analyzed.

4.3.3.2 Summary. - Temperature and aging effects on the band pass and low pass filter characteristics were found to be negligible. The differential comparator reference level was stable and the current and voltage offsets were negligible compared to the magnitude of the reference level. The bias stability of buffer Q2, and the ON/OFF stability of saturating switch Q1 were found to be sufficient. Multivibrator pulse width drift due to temperature and aging averages ±7%; when initial component tolerances are included, the overall range is approximately +14, -13%. Since considerable record/play-back head overlap is designed into the system, and the heads are 800 us apart, gate signal pulse widths are not critical; thus, the above pulse width tolerances are acceptable. Gate loading was found to be critical due to the 100 ohm series resistance in each output. The calculated maximum allowable series resistance for each gate is shown in Table 4-26. As shown in the table, the lowest allowable series resistance is for the C and D gates in the playback mode, where the maximum permissible resistance is 30 ohms.

The camera rephase output source impedance is approximately 2 k ohms when the output voltage is high (2.4V) and 300 ohms when the output is low (0.6V). These limits meet the present system interface requirements. Initial pulse symmetry is ±7.3% from nominal, with a worst case drift of ±4.8% as compared to an overall allowable range of ±20%. The negative going transition time is approximately one us into a resistance-capacitance load. This value will be slightly higher when driving the added capacitance of the system transmission line, but the switching time may be improved by adjustment of the output shunt capacitor (C17=0.001 UF). Camera rephase pulse jitter is projected as 5 us at a 5 Hz rate.

4.3.3.3 Worst Case Analysis. - The Reference Generator circuit has been analyzed for an operating temperature range of 0°C to 60°C. A 10,000 hour lifetime was used for component and semiconductor parameter derating.

a. 50 kHz Monitor/Motor Drive. - The 50 kHz space craft clock (SCC) input is transformer coupled (T1) into a band pass filter which feeds differential comparator U1. The output of the differential comparator, a 50 kHz square wave, is then low pass filtered and buffered in Q2.

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TABLE 4-26. REFERENCE GENERATOR OUTPUT LOADING

Signal	Pin No.	Location Type	Max Cur (mA)	Location Type	Max Cur (mA)	Location Type	Max Cur (mA)	Total Current (mA)	Voltage Drop (max.)	V_{out} Max "Low"	V_{in} Max. "Low" Allow.	Series RS Max. Allow.
F	2	Equalizer MC1545	2.5					2.5	0.29	0.52	0.5	92
E	4	Equalizer MC1545	2.5					2.5	0.29	0.52	0.5	92
C	5	Rec Amp CA3026	5.2	PB Amp MC1545	2.5	Equalizer 2-MC1545	5	R-Mode 5.2 PB Mode 7.5	0.6 0.86	0.83 1.09	0.5 0.5	44.3 30.6
$\overline{C}$	6	Decoder	1.6					1.6	0.19	0.59	No Require.	Use 115
$\overline{D}$	7	Decoder	1.6					1.6	0.19	0.59	No Require.	Use 115
$\overline{X}$	11	Video Out Q7	+.1 "0" +.17 "1"					+0.1 "0" +0.17 "1"	0.01	0.41	No Require.	Use 115
TW3	12	Cap. Servo TTL Gate	1.6	Cap. Servo SN5495-SR	1.6			3.2	0.32	0.52	0.8	190
X	13	Video Out Q9	+.1 "0" +.17 "1"	Video Out MC3160-Set	2.3			2.2	0.25	0.45	0.8	270
D	16	Rec Amp CA3026	5.2	PB Amp MC1545	2.5	Equalizer 2-MC1545	5	R-Mode 5.2 PB Mode 7.5	0.6 0.86	0.83 1.09	0.5 0.5	44.3 30.6
Cam Re-phase	17	AED-CCC DTTL 9040 FF	.4 "0" 0 "1"	2K 70 Gnd	.4 "0" 1.34 "1"			0.8 "0" 1.34 "1"	.08 "0" 0.15	0.41 0.15	0.8	Use 115
$\overline{H}$	20	Video Out Q8	+.1 "0" +.17 "1"	Video Out MC3160 (CL)	-3			2. +0.17	0.33	0.53	0.8	196
50 kHz Mon	41	Motor Aux 8150596-1	237 rms					237 rms				$\frac{V_{out}}{V_{in}} = 0.1$
K	44	Video Out MC3100	2					2	0.23	0.43	1.1	450
HW Drive	57	Cycler 9601	1.6	Cap. Dr./ Dem SN5472	3.2			4.8	0.55	0.75	0.8	119
Cap Drive	59	Cap. Dr./Dem SN5472	3.2					3.2	0.37	0.57	0.8	178

Notes: 1. R = 115 ohms
2. TTL V_{out} = 0.27v at 7.5 MHz
3. Currents are sink (negative) unless otherwise noted

TO BE REVISED

1. Band Pass Filter. - The band pass filter is a constant K, half-section with a center frequency fo = 50 kHz. Circuit design is based on the following relationships:

$$R^2 = \frac{L_1}{C_2} = \frac{L_2}{C_1} \tag{1}$$

$$C_1 = \frac{1}{\omega_o^2 L_1} \tag{2}$$

and,

$$L_2 = \frac{1}{\omega_o^2 C_2} \tag{3}$$

where,

ω_o is the angular resonant frequency

R is the nominal terminating resistance

Since both inductors are adjustable, deviation from the nominal center frequency will be due to component aging and temperature drift. Inductance drift is negligible. In addition, variation in C1, which is a mica capacitor, may be neglected. Therefore, from equation 3,

$$\omega_o = \frac{1}{\sqrt{C_2 L_2}} \tag{4}$$

Using component variations due to temperature and aging, fo = 50 ±3 kHz, which results in less than 1 DB attenuation.

2. Differential Comparator. - Differential voltage comparator U1 is a high gain differential input, single-ended output amplifier which exhibits rapid recovery from saturation. External positive feedback is used with the amplifier to improve the rise time and also provide some hysteresis in the transfer characteristic for added noise immunity. The signal level at which the comparator fires depends upon the input threshold level. Any change in input offset voltage or current causes a change in the threshold level.

Zener Regulation. - Since the Zener reference voltage stability depends upon the magnitude of its reverse current, the range of reverse current variation will be determined. As shown in Figure 4-99, Zener reverse current may be written as

$$I_{VR2} = I_{R8} - I_{U1} - I_{R6} \tag{5}$$

where,

$$I_{R8} = \frac{V_4 - V_{Ref1}}{R_8} \tag{6}$$

$$I_{R6} = \frac{V_{Ref1}}{R_6+R_7} \tag{7}$$

and, I_{U1} = Comparator Positive Supply Current

Substituting into equation 5,

$$I_{VR2} = \frac{V_4 - V_{Ref2}}{R_8} - I_{U1} - \frac{V_{Ref2}}{R_6+R_7} \tag{8}$$

Now, substituting worst case component values into equation 8 at 60°C $\overline{I_{VR2}}$ = 15.62 mA and at 0°C $\underline{I_{VR2}}$ = 1mA. For a dynamic impedance of 10 ohms, the voltage regulation is approximately ±0.75%.

The comparator threshold level is given by,

$$V_{in2} = \frac{R_7}{R_6+R_7} V_{Ref2} \tag{9}$$

Neglecting load regulation, and substituting worst case values into equation 9, the threshold limits are: at 60°C $\overline{V_{in}}$ = 0.207V, and at 0°C $\underline{V_{in}}$ = 0.172V, which are well below the minimum clock signal of 0.85V peak.

Similarly, the regulator stability of VR1 may be determined. From Figure 4-99, Zener reverse current is,

$$I_{VR1} = \frac{V_3 - V_{Ref1}}{R_4} - I_{U1} \qquad (10)$$

Substituting worse case values into equation 10, the reverse current limits are: at 0°C I_{RV1} = 40.4 mA, and at 60°C I_{VR1} = 2.1 mA. From the manufacturer's specifications, VR1 regulation for the above reverse current range is ±5%.

Input Offset. - A differential voltage results between the comparator input terminals due to the offset voltage and current. The maximum input offset voltage is 3.35mV, which is negligible compared to the nominal value of reference threshold, V_{in2} = 0.19V. Maximum offset current is specified as 4.8 uA. For a source resistance of 2,600 ohms, this current results in an offset voltage of ΔV = 12.5mV, which is also negligible compared to the reference threshold of V_{in2} = 0.19V.

3. Low Pass Filter. - Filter L3, C5, C6 and C7 is a low pass filter with characteristics based on the following relationships:

$$L_o = \frac{R_o}{\omega_o} \qquad (11)$$

$$C_o = \frac{L_o}{R_o^2} \qquad (12)$$

$$\omega_o = \frac{1}{C_o R_o} \qquad (13)$$

$$C_5 = C_7 = 2.08\, C_o \qquad (14)$$

$$C_6 = 0.159\, C_o \qquad (15)$$

$$L_3 = 0.861\, L_o \qquad (16)$$

For terminating $R_o = 1,300$, $L_o = 3.73$mH, and $C_o = 2,200$ pF, from equation 13 fo = 55.7 kHz. Since drift in the inductor and capacitor C6 (mylar) is very small, the drift of f_o will be negligible.

4. Buffer (Q2). - Transistor Q2 is an emitter follower amplifier with the output ac coupled. The dc bias (and, as a result, the collector to emitter voltage) is dependent on the transistor h_{FE}, and therefore subject to both the initial h_{FE}, tolerances and subsequent drift due to temperature and aging. From Figure 4-99, transistor V_{CE} is given by,

$$V_{CE} = V_2 - I_C R_{14} - (I_E R_{15} + V_3) \tag{17}$$

and emitter voltage is,

$$V_E = V_3 - I_E R_{15} \tag{18}$$

Assuming a large current gain, then

$$h_{FE} \approx \frac{I_E}{I_B} \tag{19}$$

Now, from Figure 4-99,

$$I_B = \frac{V_B}{R_{13} + R_{L3} + R_{10} + R_{U1}} \tag{20}$$

where, RU1 ≈ 200, the output impedance of U1. Combining the above equations and solving for V_E,

$$V_E = \frac{V_3 (R_{13} + R_{L3} + R_{10} + R_{U1}) - h_{FE} R_{15} V_{BE}}{R_{13} + R_{L3} + R_{10} + R_{U1} + h_{FE} R_{15}} \tag{21}$$

Minimum V_{CE} occurs for maximum collector current; thus, h_{FE} would be a maximum, and V_E is minimum (V_E negative). Substituting worst case values into equation 20, $V_E = 0.89$V for $h_{FE} = 375$. Also, $I_C \approx I_E = 6.8$ mA, and from equation 17 $V_{CE} = 7.49$V. Worst case power dissipation in the quiescent mode, for $I_C = 12$mA, $V_{CE} = 8.1$V, is PQ2 = 97mW.

5. Inverter (Q1). - Transistor Q1 is a common emitter amplifier used as an inverter for triggering TTL divider U2. The maximum required base drive depends on the transistor minimum current gain. Thus,

$$\overline{I_B} = \frac{\overline{I_C}}{h_{FE}} \tag{22}$$

From Figure 4-99, the collector current is given by,

$$I_C = \frac{V_1 - V_{CE}}{R_{19}} + I_{U2} \tag{23}$$

and the base current is given by,

$$I_B = \frac{V_{in} - V_{BE}}{R_{18}} \tag{24}$$

At 0°C, where h_{FE} is minimum, substituting worse case values, from equations 23 and 24, $\overline{I_C}$ = 13.15mA and $\overline{I_B}$ = 0.425mA. Now from equation 22, minimum required h_{FE} = 31, which is much less than the minimum available h_{FE} = 53. Q1 OFF stability is ensured due to the fact that the maximum low level differential comparator output is 0V, and as a result the base-emitter junction of Q1 is reverse biased.

6. Binary Divider— Headwheel Drive. - U2 and U3 are TTL decade counters internally interconnected to provide a divide-by-two counter and a divide-by-five counter. The maximum required drive current is -6.4mA, and the input voltage threshold is 0.8V, which are compatible with the output of inverter Q1 and the associated logic gates.

As shown in Table 4-26, the worst case headwheel drive current is 4.8mA for a maximum allowable series resistance of R21 = 83 ohms.

7. Divider/Gating—CAP Drive. - U4 and U5 are TTL decade counters and U6 and U7 are TTL gates, and thus the input and output requirements are compatible. The CAP VCO input is a TTL gate and the CAP drive load is a TTL flip-flop. The record dc command is also a TTL gate.

b. Camera Re-Phase/TW Reference Gating. - The camera rephase signal is referenced to tonewheel output TW1 and the gating levels are referenced to TWA. Figure 4-102 shows the various signal timing relationships.

1. Multivibrator Pulse Variations. - The multivibrators (U8, U13, U16 and U18) are connected in the retriggerable configuration. Since the input trigger pulse is dc coupled, triggering is independent of the input signal transition time. For the range of component values used below, the output pulse width is defined as,

$$T = 0.32\, R_X\, C_X \left[1 + \frac{0.7}{R_X} \right] \tag{25}$$

where,

R_X is in k ohms

C_X is in pF

T is in ns

Due to component variations, the maximum pulse width is:

$$\overline{T} = 0.32\, \overline{R_X}\, \overline{C_X} \left[1 + \frac{0.7}{\overline{R_X}} \right] \tag{26}$$

And, the minimum pulse width is,

$$\underline{T} = 0.32\, \underline{R_X}\, \underline{C_X} \left[1 + \frac{0.7}{\underline{R_X}} \right] \tag{27}$$

Multivibrator U8. - Using nominal component values and assuming potentiometer R26 is centered, at 25°C, the nominal pulse width for multivibrator U8 is T = 47 us. As a result of drift due to temperature and aging, the maximum pulse width is $\overline{T}$ = 52 us at 60°C and the minimum pulse width is $\underline{T}$ = 43 us at 0°C. The percentage overall drift is +10, -8.5%.

Multivibrator U9. - The nominal time constant of multivibrator U9 is T = 445 us. The initial range is $\overline{T}$ = 473 us and $\underline{T}$ = 420 us, and the overall range including drift due to temperature and aging is $\overline{T}$ = 510 us at 60°C and $\underline{T}$ = 390 us at 0°C. Or, worst case drift is ±7%.

TO BE REVISED

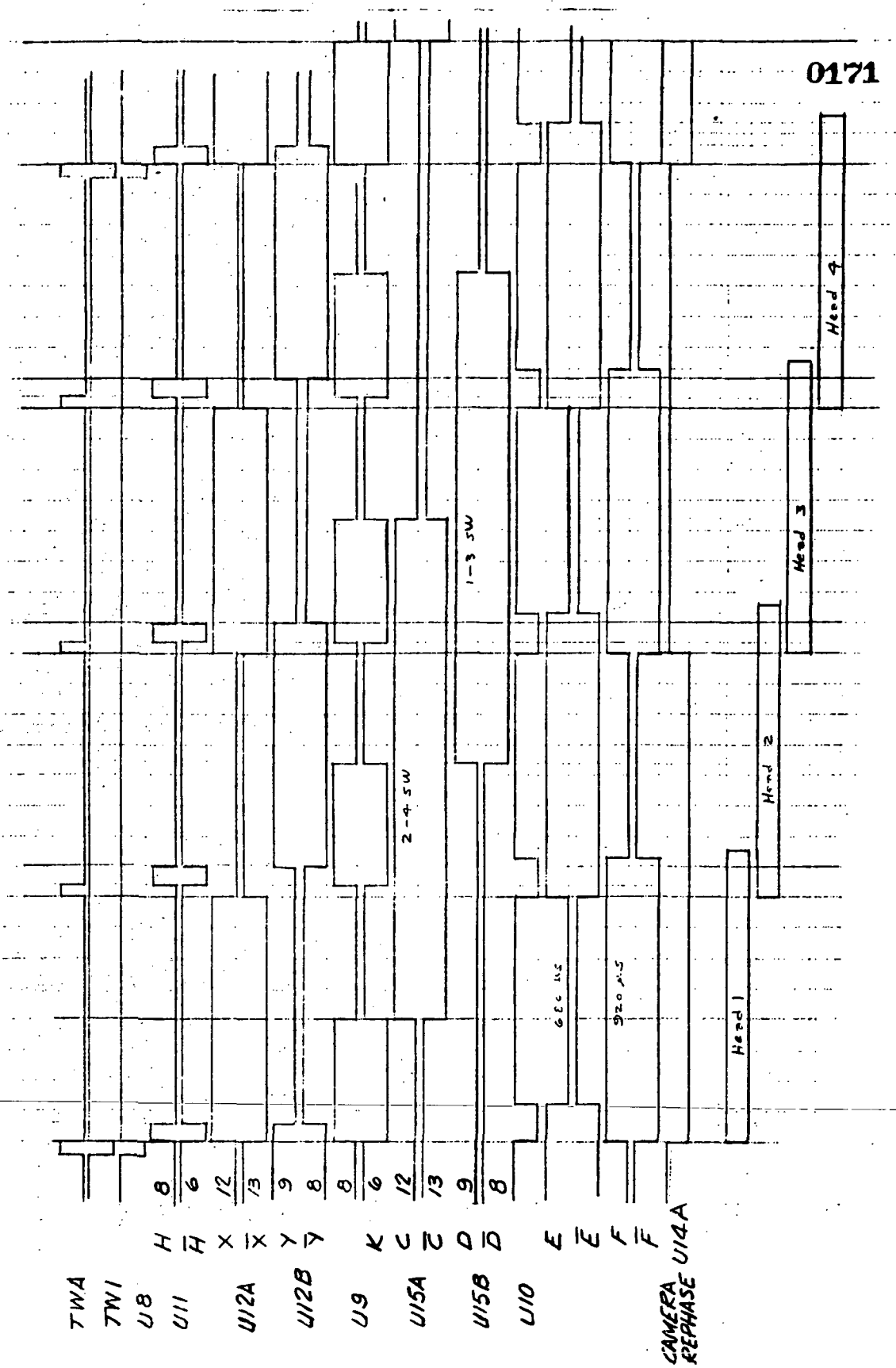

Figure 4-102. Reference Generator Timing Diagram

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Multivibrator U10. - The nominal time constant of multivibrator U10 is T = 120 us. The initial range is $\overline{T}$ = 120 us and $\underline{T}$ = 113 us, and the overall time constant range including drift due to temperature and aging is $\overline{T}$ = 134 us at 60°C and $\underline{T}$ = 104 us at 0°C. Or, worst case drift is ±7%.

Multivibrator U11. - The nominal time constant of multivibrator U11 is T = 64.8 us. The initial range is $\overline{T}$ = 68.8 us and $\underline{T}$ = 60.8 us, and the overall range including drift due to temperature and aging is $\overline{T}$ = 74 us at 60°C and $\underline{T}$ = 56.5 us at 0°C. Or, worst case drift is ±7%.

Multivibrator U13. - The nominal time constant of multivibrator U13 is T = 1780 us. The initial range is $\overline{T}$ = 1910 us and $\underline{T}$ = 1650 us, and the overall range including drift due to temperature and aging is $\overline{T}$ = 2000 us at 60°C and $\underline{T}$ = 1570 us at 0°C. Or, worst case drift is approximately ±5%.

Multivibrators U16 and U18. - The nominal time constant of multivibrators U16 and U18 is T = 54 us. The initial range is $\overline{T}$ = 57.5 us and $\underline{T}$ = 51 us, and the overall range including drift due to temperature and aging is $\overline{T}$ = 62 us at 60°C and $\underline{T}$ = 47.5 us at 0°C. Or, worst case drift is approximately ±7%.

2. Signal Timing. - Since both reference signals, TW1 and TWA, are in phase, and relatively large time constants are involved in the pulse delays, there are no race conditions in the reference generator logic.

3. Output Gate Loading. - A number of the circuits driven by the reference generator are sensitive to input voltage level, therefore gate signal loading is critical and all load requirements were analyzed.

C, D, E and F Gates. - The C, D, E and F gates drive two-channel-input amplifiers which are very sensitive to control signal level. For example, below 0 dB the single-ended voltage gain varies approximately 1 dB/10 mV input level. Detailed current calculations for these gate signals are given in paragraph 4.1.2.6.3. Output impedance requirements are summarized in Table 4-26.

X, $\overline{X}$ and $\overline{H}$ Gates. - X, $\overline{X}$ and $\overline{H}$ Gates drive several TTL circuits; in addition, each gate drives a transistor buffer on the Video Out Board. Voltage drop due to the 100 ohm resistor in series with the gate outputs is negligible compared to the drop across the 10 k ohms in series with the Video Out buffers (on the Video Out Board).

Thus, the X, $\overline{X}$ and $\overline{H}$ Gate outputs meet system requirements.

$\overline{C}$, $\overline{D}$ and K Gates. - The $\overline{C}$, $\overline{D}$ and K gate loads are relatively low and thus drive capability is more than adequate.

4. Camera Re-Phase. - The camera rephase output is a square wave with a period of 3.2 ms. This signal drives a shielded line and an LP DTuL flip-flop in the RBV camera subsystem (camera controller and combiner).

Load Requirements. - From Figure 4-103, the available load current is,

$$I_{R38} = I_{U14} + I_{R37} \tag{28}$$

Also, since

$$I_{R38} = \frac{V_{U14}}{R_{38} + R_L} - I_6 \tag{29}$$

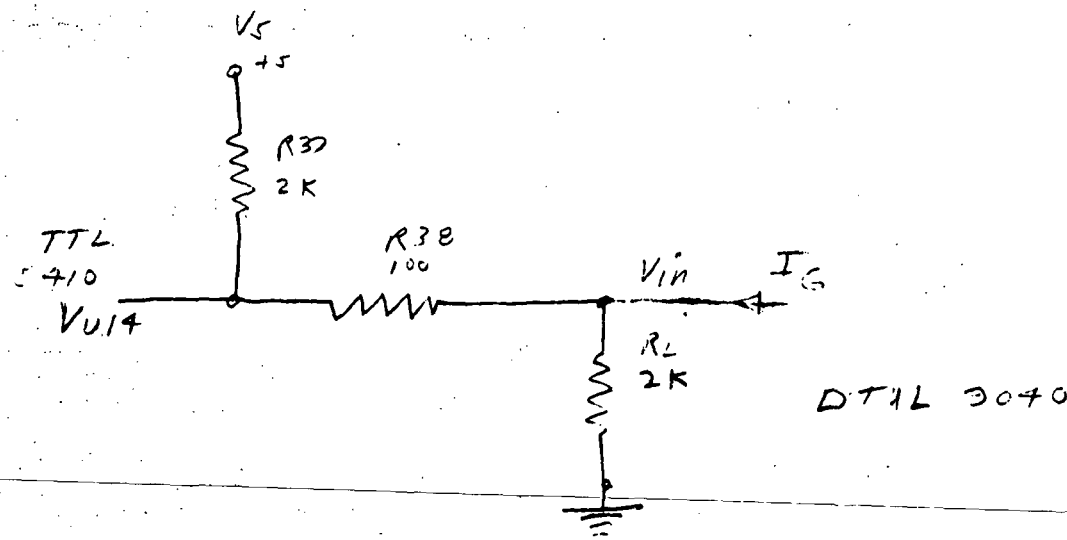


Figure 4-103. Camera Rephase Interface

Then for V_{U14} high, $I_G \approx 0$, and assuming V_{U14} is at its minimum high level, or I_{R37} is maximum, then substituting worst case values into equation 29, available $I_{R38} = 1.34$ mA. Under the above conditions, the current supplied by R_{37} is $I_{R37} = 0.9$ mA. Thus, substituting into equation 28, the current required from U14 is $I_{U1} = 0.44$ mA, which is within the TTL gate high level drive specifications.

When the camera rephase signal is low, maximum DTuL current required is, $\overline{I_G} = 0.4$ mA. From Figure 4-103,

$$V_{in} = \frac{R_L}{R_L + R_{38}} V_{U14} - I_G R_{38} \qquad (30)$$

Substituting worst case values into equation 30, for $\overline{V_{U14}} = 0.4$, maximum camera rephase low level is $\overline{V_{in}} = 0.35$V, which is within the allowable threshold of 0.8V.

Worst Case Specifications. - The camera rephase signal rise time depends on C17, a 0.001 uF capacitor at the Reference Generator output, the shielded interconnecting line, and the camera phasing control input impedance. Assuming that the transmission line capacitance is small compared to C17, and gate average output impedance is 1 k ohm, signal rise time is approximately one us.

Signal jitter is specified as 5 us peak to peak at a 5 Hz rate.

The TTL gate output impedance with the +5V supply open, is greater than 10 k ohms.

The source impedance for the output high is approximately 2 k ohms, and for the low level Z out $\approx$ 300 ohms, including the 100 ohm series resistance.

At $V_{out} = 2.4$V, the available current is $I_{out} = 1.3$ mA, and at $V_{out} = 0.6$V, $I_{sink} = 2$ mA.

The worst case low output level is $\overline{V_{out}} = 0.6$V at a load of 300 ohms, and the high level is $\underline{V_{out}} = 2.4$V at a 1,700 ohm load.

Power Supply Decoupling Load. - The +5.6 voltage supply decoupling network is shown in Figure 4-99, where $R_{L4} = 1.8$ ohms. From the manufacturers specifications, the Reference Generator worst case +5 load requirement is 457 mA. Thus, $\Delta V = 0.83$V and the gate supply voltage is $V_5 = 4.6 \pm 0.2$V.

4.3.3.4 Conclusion and Recommendation. - Worst case analysis of the Reference Generator has shown that reliable operation will be maintained over the required temperature range of 0°C to 60°C for a lifetime of 10,000 hours. Considerable gate signal pulse width variation is possible due to capacitance initial tolerances and drift. However, since the record/playback heads overlap, system gating requirements are not critical.

The input signal specifications were found to be compatible with the network input gates. Analysis of the output gate loads showed that a number of the gate loads are sensitive to the magnitude of the low level input voltage. Therefore, worst case maximum resistance allowable in series with the TTL gate outputs were specified, and any necessary circuit modifications were incorporated into the design. Due to the additional power derating required in a vacuum environment, Q2 should be painted to increase its dissipation capability.

4.3.4 TW Processor Worst Case Analysis. - The TW Processor has been analyzed to ensure reliable operation under ERTS System environmental requirements. Performance limitations of all critical functions due to component and semiconductor parameter manufacturing tolerances and aging effects were determined. (See Appendix H for analysis criteria.)

4.3.4.1 Design Considerations. - The minimum differential comparator reference levels must be great enough to discriminate against TW noise spikes. Since signal processing depends on the leading edges of pulses, multivibrator pulse widths are not critical. However, gross pulse width variation should be avoided, to prevent erroneous HW speed indications and to ensure a reliable control track record signal. Sufficient transistor drive capability must be provided, while simultaneously ensuring reliable cutoff stability. Semiconductor maximum dissipation limits must not be exceeded under maximum load high temperature operation.

4.3.4.2 Summary. - In general, since the TW processor circuit operation is basically digital, component tolerances and drift factors are not critical. As a result, even though the range of pulse width and reference level variations is considerable, no network revisions were required.

The differential comparator reference levels have a temperature and aging drift of -16% and +23% from their initial values. Worst case comparator input offset voltage and current are negligible compared to the magnitude of the reference levels, which have a nominal value of one volt.

Multivibrator pulse width variation due to temperature and aging is as follows: U3 ±27.5%; U5 +15, -11%; U6 +43, -36%. Multivibrator trigger delay is of the order of 35ns, which is negligible compared to the pulse widths.

Switching stages Q1 and Q3 were found to exhibit adequate gain for minimum h_{FE} and are stable during the high temperature cut-off condition. The minimum control track record current is 5 mA which is equal to the allowable minimum. Also, the maximum possible is 14.7 mA, which is below the limit of excessive tape saturation and head damage. The HW speed TM signal variation as a result of amplifier signal drift due to temperature and aging is +2.6, -3.9%. The bulk of the HW speed TM signal level change will result from the U6 multivibrator pulse width variation given above.

4.3.4.3 Worst Case Analysis. - The following analysis is based on the component specifications listed in Appendix H. An ambient temperature range of 0° C to 60° C over a 10,000 hour lifetime was used for component and parameter derating, when derated transistor parameters were not defined in manufacture specifications, the derating criteria shown in the appendix were applied. These parameter derating guidelines are considered to be applicable to the ERTS system worst case requirements.

a. Differential Comparator. - Differential voltage comparators U1 and U2 are high gain, differential input, single-ended output amplifiers which exhibit rapid recovery from saturation and are compatable with low-level logic circuits. External positive feedback is used with the amplifier to improve the rise times and also provide some hystersis in the transfer characteristics for added noise immunity. The signal level at which the comparator fires depends on the input reference level, and on any drift in reference level resulting from a change in input offset voltage or current.

1. Zener Regulation. - As shown in Figure 4-100, the reference level for the negative input comparator (U1) is derived from the -8V supply, and the reference level for the positive input comparator (U2) is derived from the +22V supply.

Negative Input (U1). - Comparator U1 reference level (V_{Refl}) is generated by the regulator shown in Figure 4-104. V_{Refl} also serves as the negative power supply for both U1 and U2. The regulator load may be represented by,

$$I_{L1} = I_{R4} + I_{U1} + I_{U2} \tag{1}$$

where,

$$I_{R_4} = \frac{V_{Refl}}{R_4+R_5} \tag{2}$$

and, $I_{U1} = I_{U2}$ = comparator negative supply current. It may be assumed that I_{L1} is relatively constant, since the change in I_{U1} and I_{U2} are approximately out of phase, and their transition transient is filtered by C16. Then, the maximum load current is,

$$I_{L1} = \frac{V_{\overline{Refl}}}{\underline{R_4}+\underline{R_5}} + 2\,\bar{I}_U \tag{3}$$

For worst case component value at 60° C, $\bar{I}_{L1} = 15.3$ mA. To determine the variation in Zener current, I_{Z2}, assuming I_L constant, from the figure,

$$\Delta I_{R39} = \Delta I_{Z2} \tag{4}$$

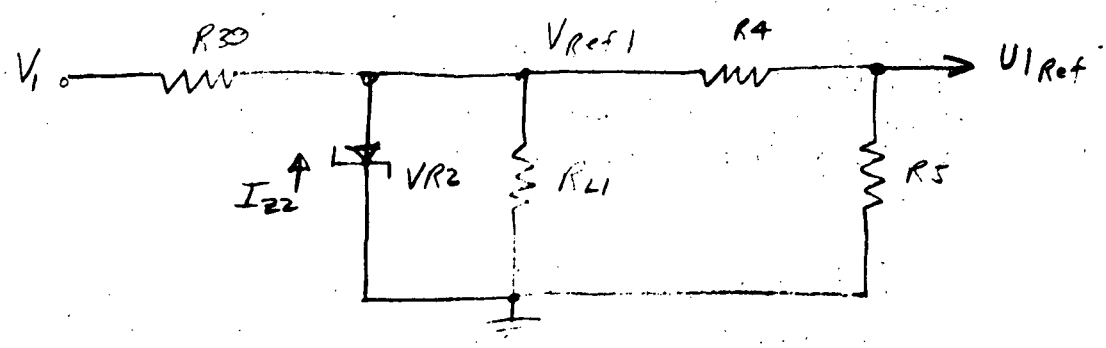


Figure 4-104. Comparator U1 Reference Level

where,

$$I_{R39} = \frac{V_1 - V_{Refl}}{R_{39}} \tag{5}$$

and maximum I_{R39} is,

$$\overline{I_{R39}} = \frac{\overline{V_1} - V_{\underline{Refl}}}{\underline{R_{39}}} \tag{6}$$

For worst case values, at 60° C, $\overline{I_{R39}} = 48.5$ mA.

Similarly, minimum I_{R39} is,

$$\underline{I_{R39}} = \frac{V_1 - \overline{V}_{Refl}}{\overline{R}_{39}} \tag{7}$$

and for worst case values at 60° C, $\underline{I_{R39}} = 10$ mA.

Since,

$$I_{R39} = I_{Z2} + I_{L1} \tag{8}$$

and $I_{\underline{R39}} < I_{L1}$, then $I_{Z2} = 0$ and $V_{\underline{Refl}}$ is dependent entirely on I_{L1} R_{39}. Or,

$$V_{\underline{Refl}} = \underline{V_1} - \overline{I_{L1}}\ \overline{R_{39}} \tag{9}$$

And, for $I_{L1} = 15.3$ mA, $V_{\underline{Refl}} = 6.2$V, which is equal to the regulator nominal value, thus avoiding any degradation in the negative reference level.

The worst case Zener power dissipation occurs at maximum input voltage, V1, and minimum load current, which results in maximum Zener current. Or,

$$\overline{P_d} = \overline{I_{Z2}}\ V_{Refl} \tag{10}$$

where, $V_{Refl} = 5.83$V, the value used in the computation of $\overline{I_{R39}}$. Then, for $I_{L1} = 10.2$ mA and the above value of $\overline{I_{Z2}}$, at 60° C, $\overline{P_d}$ = 223 mW, which is within the maximum allowable dissipation of 275 mW.

Positive Input (U2). - The reference level for comparator U2 is derived from the circuit shown in Figure 4-105. Except for polarity, this network is identical to that of Figure 4-103 and, therefore, the equations used in the above analysis may be used by simply interchanging parameter designations. For the positive voltage supply, $I_U = 9$ mA; then, for equation 3, $\overline{I_{L2}} = 19.3$ mA. And from equations 6 and 7, $\overline{I_{R38}} = 29$ mA and $I_{\underline{R38}} = 14.5$ mA. Again, since $I_{\underline{R38}} < I_{L2}$, Zener regulation ceases and $V_{\underline{Refl2}}$ is dependent on I_{L2} R_{38}. Or, from equation 9, $V_{\underline{Refl2}} = 10.1$V, which is slightly less than the Zener regulator worst case value of 11.3V.

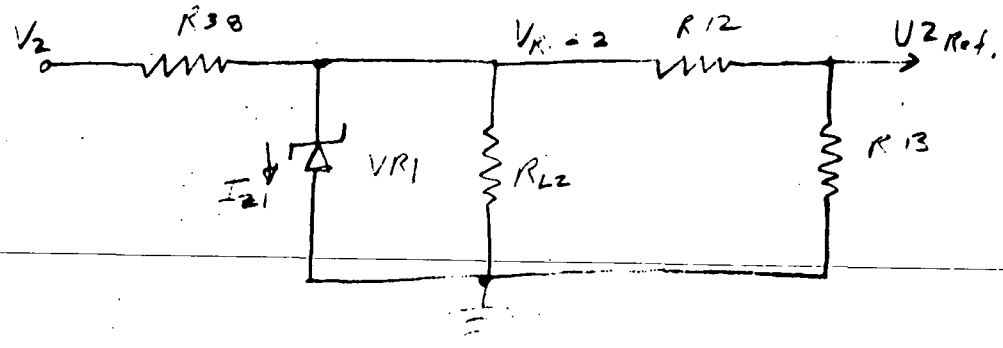


Figure 4-105. Comparator U2 Reference Level

Using equation 10, the worst case VR1 power dissipation for I_{L2} = 11.4 mA is $\overline{P}_d$ = 200 mW, which is less than the maximum allowable dissipation of 220 mW.

Regulator Drift. - Zener regulator drift due to temperature and aging may be determined from the manufacturer's specification. Neglecting the Zener reverse current change due to resistor aging, Zener reverse voltage variation for the ERTS system environmental requirements is as follows: (1) due to temperature, V_{Ref1} = +0.16, -0.1% and V_{Ref2} = +0.27, -0.2%; (2) drift due to gaing is the same for both references, ±1%. Thus, the overall worst case drift from their initial levels is V_{Ref1} +1.16, -1.1% and V_{Ref2} + 1.27, =1.2%.

Comparator Input Level Variation. - The comparator input levels, $U1_{Ref}$ and $U2_{Ref}$, depend on the variation in regulator reference and the resistor divider temperature and aging characteristics.

For comparator U1, neglecting the input current, the minimum input reference level is,

$$\underline{U1}_{Ref} = \frac{\underline{R_5}}{R_4 + \underline{R_5}} \underline{V_{Ref1}} \tag{11}$$

and, the maximum level is,

$$\overline{U1}_{Ref} = \frac{\overline{R}_5}{\underline{R_4} + \overline{R_5}} \overline{V}_{Ref1} \tag{12}$$

Using initial tolerances at 25° C, the nominal value of $U1_{Ref}$ = 1.02V, $\underline{U1_{Ref}}$ = 0.89V and $\overline{U1}_{Ref}$ = 1.16V. The resulting drift due to temperature and aging at 0° C is: $\underline{U1_{Ref}}$ = 0.743V and at 60° C, $\overline{U1}_{Ref}$ = 1.43V. Thus, the worst case possible U_{1Ref} drift from its initial value is U_{1Ref} + 23, -16%.

Similarly, for comparator U2, the input reference level is,

$$U_{2Ref} = \frac{R13}{R_{12} + R_{13}} V_{Ref2} \tag{13}$$

and the initial range at 25° C is: nominal $U2_{Ref}$ = 1V, $\underline{U2_{Ref}}$ = 0.865V and $\overline{U2}_{Ref}$ = 1.15V.

The resulting drift due to temperature and aging is, assuming a regulated reference, at 0° C, $\underline{U2}_{Ref} = 0.73V$, and at 60° C, $\overline{U2}_{Ref} = 1.45V$. For the condition where reference regulation ceases, or $V_{Ref2} = 10.1V$, the worst case comparator input level variation is $\underline{U2}_{Ref} = 0.65V$ at 0° C and $\underline{U2}_{Ref} = 1.16V$ at 60° C. The worst case drift from the initial $U2_{Ref}$ value for the regulated condition is $U2_{Ref}$ +26, -15%.

2. Input Offset. - Due to the comparator inherent offset voltage and current characteristics, a differential voltage results between the input terminals. The maximum input offset voltage is 3.35 mV, which is negligible compared to the nominal value of reference threshold of 1V.

   To minimize the effects of the bias currents, the dc source resistance is approximately equal to the source resistance of the reference. From the comparator specifications, the maximum offset current is 4.8 μA, which, for a source resistance of 820 ohms, results in an offset voltage of $\Delta V = 3.9$ mV. As a result, the effect of offset current is also negligible compared to the reference threshold of one volt.

   Thus, the worst case threshold range is 0.73V to 1.45V, which is within the tonewheel signal limits of 1.5 to 2V peak.

3. Output Loading. - The differential comparator typical output sink current is 1.7 mA. This is sufficient to drive the required one TTL load of a maximum of 1.6 mA.

   The minimum positive output level is 2.5V, which exceeds the minimum allowable multivibrator trigger level of 1.8V.

   The maximum output "low" level is 0 volts, which is within the maximum allowable multivibrator low voltage trigger level of 0.85V.

b. Multivibrator Pulse Variation. - The multivibrator inputs are dc coupled and, therefore, independent of the input signal transition times. The output pulse width is given by,

$$T = 0.32\ Rx\ Cx \left[1 + \frac{0.7}{Rx}\right] \qquad (13)$$

where,

Rx = k ohms

Cx = pF

T = ns

From equation 13, the maximum pulse width is

$$\overline{T} = 0.32\,\overline{Rx}\,\overline{Cx}\quad 1+\left[\frac{0.7}{Rx}\right] \tag{14}$$

And the minimum pulse width is

$$\underline{T} = 0.32\,\underline{Rx}\,\underline{Cx}\quad 1+\left[\frac{0.7}{\underline{Rx}}\right] \tag{15}$$

1. U3 Pulse Width Drift. - U3 is connected in the non-retriggerable configuration to minimize the possibility of extraneous pulses. From equation 13, for nominal component values at 25° C, T = 190 μs. Using initial tolerances, equations 14 and 15 yield $\overline{T}$ = 210 μs and $\overline{T}$ = 153 μs. Pulse width drift due to temperature and aging result in a maximum width of $\overline{T}$ = 270 μs at 60° C and a minimum pulse width of $\underline{T}$ = 112 μs at 0° C. The worst case drift from the initial values is +28.5, -27%.

2. U5 Pulse Width Drift. - U5 is connected in the retriggerable mode. From equation 13, for nominal component values at 25° C, T = 50 μs. Using initial tolerances, equations 14 and 15 yield $\overline{T}$ = 54 μs and $\underline{T}$ = 45 μs. Pulse width drifts due to temperature and aging results in a maximum width of $\overline{T}$ = 62 μs at 60° C and a minimum width of $\underline{T}$ = 40 μs at 0° C. Therefore, worst case drift from the initial values is +15, -11%.

3. U6 Pulse Width Drift. - U6 is also connected in the retriggerable mode. And, from equation 13, for nominal component values at 25° C, T = 372 μs. Using initial tolerances, equations 14 and 15 yield $\overline{T}$ = 413 μs and $\underline{T}$ = 340 μs. Pulse width drift due to temperature and aging result in a maximum width of $\overline{T}$ = 590 μs and a minimum width of $\underline{T}$ = 217 μs. Therefore, worst case drift from the initial value is +43, -36%.

c. Control Track Record Amplifier. - The control track record amplifier consists of transistors Q1 and Q2. Q1 is normally ON and Q2 is normally OFF.

1. Q1 Analysis.

Drive Requirements. - To ensure reliable worst case switching,

$$\text{minimum available } h_{FE} \geq \text{maximum available } h_{FE} \tag{16}$$

The maximum required transistor current gain is given by,

$$\overline{h_{FE1}} = \frac{\overline{I_{C1}}}{\underline{I_{B1}}} \tag{17}$$

From Figure 4-100, maximum collector current is,

$$\overline{I_{C1}} = \frac{\overline{V_2} - \underline{V_{CE1}}}{R_{20} + R_{22}} \tag{18}$$

And, minimum base current is

$$\underline{I_{B1}} = \frac{\underline{V_{in1}} - \overline{V_{BE1}}}{R_{19}} \tag{19}$$

Substituting worst case component values into the above equations, at 0° C, where transistor h_{FE} is minimum, $\overline{I_{C1}} = 2.8$ mA, $\underline{I_{B1}} = 0.132$ mA. Then, from equation 17, maximum required $h_{FE1} = 21$, which is less than the minimum available h_{FE1} at 0° C of 53, and the requirement of equation 16 is fulfilled.

OFF Stability. - In the cut-off condition, the transistor maximum base current must be of the order of the high temperature value of I_{CBO}. Using equation 19, maximum base current is,

$$\overline{I_{B1}} = \frac{\overline{V_{in1}} - \underline{V_{BE1}}}{\underline{R_{19}}} \tag{20}$$

And for worst case component values at 60° C, $I_{B1} = 13\,\mu A$, which places Q1 well within its cut-off region.

2. Q2 Analysis.

Drive Requirement. - Basically, Q2 operates as a current source and is normally in the cut-off region. When Q1 is turned off, a pulse is coupled through C7 and amplified by Q2. Assuming C7 is a low impedance, and that Q2 input impedance is much greater than R21, the signal at the input to Q2 is,

$$V_{B2} = \frac{R_{21}}{R_{20} + R_{21}} V_{CC1} \tag{21}$$

Letting $V_{CC1} = 21.5V$ and using nominal component values, $V_{B2} = 3.6V$. For worst case component values, $\overline{V_{B2}} = 4.73V$ at 60° C and $\underline{V_{B2}} = 3V$ at 0° C.

Q2 OFF Stability. - Neglecting capacitor leakage current, when Q2 is cut-off the base current is equal to the reverse saturation current, I_{CBO}. Assuming I_{E2} is negligible, then from Figure 4-100,

$$\overline{V_{BE}} = \overline{I_{CBO2}}\,\overline{R_{21}} \tag{22}$$

$I_{CBO} = 0.34$ mA at 60° C and, for the worst case R21, substituting into equation 22, $V_{BE} = 0.74\ \mu V$; this is sufficient to maintain cut-off.

Q2 Voltage Gain. - Since Q2 acts as a current source, the control track record head time constant is small and therefore, the coil inductance can be neglected. Then, assuming that the transistor base resistance is small, and h_{FE} is large, the common emitter voltage gain is approximately,

$$A_v \approx \frac{R_L}{R_E} \approx \frac{R_{23}\,RCT}{(R_{23} + RCT)\,R_{25}} \tag{23}$$

Using worst case component values at 0° C, minimum gain is $\underline{A_V} = 0.052$. Maximum gain at 60° C is $\overline{A_V} = 0.095$.

CT Head Current. - When Q2 is OFF, the quiesent control track bias voltage is,

$$V_{CT} = \frac{R_{CT}}{R_{23} + R_{CT}}\ V_{CC1} \tag{24}$$

Resulting in a quiesent head current of,

$$I_{CTO} = \frac{V_{CC1}}{R_{23} + R_{CT}} \tag{25}$$

Substituting worst case values into equation 25, $I_{CTO} = 4$ mA at 0° C and $I_{CTO} = 3$ mA at 60° C.

The control track record head current change is given by,

$$\Delta I_{CT} = \frac{\Delta V_{CT}}{R_{CT}} \tag{26}$$

where,

$$\Delta V_{CT} = A_v = \Delta V_{B2} \tag{27}$$

Thus, substituting the above worst case values of gain and base voltage change into equation 27, $\Delta V_{CT} = 0.15V$ at 0° C and $\Delta V_{CT} = 0.45V$ at 60° C. Then, substituting the calculated values of ΔV_{CT} into equation 26, $\Delta I_{CT} = 5$ mA at 0° C and $\Delta I_{CT} = 14.7$ mA at 60° C. These record currents are within the minimum required control track current of 5 mA and the maximum allowable current of 25 mA. In addition, to prevent excessive tape saturation, the maximum recommended record current is 15 mA, a requirement, which is also fulfilled.

d. Head Wheel Speed Telemetry. - The headwheel speed monitor circuit consists of transistors Q3 and Q4, and an RC integrator. Q3 is a saturating switch which is normally ON, and Q4 is an emitter follower which drives the HW speed telemetry channel.

1. Zener Bias Current. - The output of Q3 is clamped by Zener diode VR3. Neglecting transistor current, which is approximately 1 mA, the diode current is,

$$I_Z = \frac{V_4 - V_{CC3}}{R31} \tag{27}$$

Substituting nominal values into equation 27, $I_Z = 10$ mA, which is the recommended value for optimum diode regulation.

2. Q3 Analysis.

Q3 Drive. - When multivibrator U6 is "low" ($V_{in3} = 0$), Q3 is ON and the maximum required h_{FE3} is,

$$\overline{h_{FE3}} = \frac{\overline{I_{c3}}}{I_{B3}} \tag{28}$$

Since R32 >> R30, IR32 may be neglected; then, from Figure 4-100, Q3 collector current is,

$$\overline{I}_{c3} = \frac{\overline{V}_{cc3} - \underline{V_{CE3}}}{\underline{R30}} \tag{29}$$

The base current is given by

$$I_{B3} = I_{R29} + I_{R28} \tag{30}$$

or, minimum available I_{B3} is,

$$I_{B3} = \frac{\underline{V_{cc3}} - \overline{V_{BE3}}}{\overline{R_{29}}} + \frac{\overline{V_{BE3}} - \overline{V_{in3}}}{\overline{R_{28}}} \tag{31}$$

Substituting worst case parameters into equations 29 and 31, at 0° C where h_{FE} is minimum, I_{c3} = 1.54 mA and I_{B3} = 0.34 mA. Then from equation 28, maximum required current gain is h_{FE} = 4.7. Since minimum available h_{FE3} is 57, the requirement of equation 16 is fulfilled.

OFF Stability. - When multivibrator U6 is high ($V_{in3} \approx 3.5V$), Q3 turns off. Neglecting reverse saturation current and assuming the base-emitter junction of Q3 is reverse biased, the minimum positive base voltage is,

$$\underline{V_{B3}} = \underline{V_{in3}} - \left[\frac{\overline{R_{28}}}{\overline{R_{28}} + R_{29}} \left(\overline{V_{cc3}} + \underline{V_{in3}}\right)\right] \tag{32}$$

Substituting worst case values into the above equation, $\underline{V_{B3}}$ = +0.4V at 0° C, which is sufficient to ensure reliable cut off.

Since the maximum allowable reverse V_{BE} is 5V, there is no possibility of Q3 base-emitter junction breakdown.

Output Level (ΔV_{c3}). - The HW speed telemetry signal magnitude is dependent on the tolerances of the components associated with Q3. Assuming C11 is a low impedance, for Q3 OFF, maximum V_{c3} is,

$$\overline{V}_{c3} = \frac{\overline{R_{32}}}{\underline{R_{30}} + \overline{R_{32}}} \overline{V_{cc3}} \tag{33}$$

Using initial tolerances at 25° C and substituting into equation 33, $\overline{V}_{c3}$ = 11.3V and $\underline{V_{c3}}$ = 9.84V. Drift due to temperature and aging results in $\overline{V_{c3}}$ = 11.61V at 60° C and $\underline{V_{c3}}$ = 10.2V at 0° C. Or, the overall worst case variation of the HW speed level from its initial value is +2.7, -3.5%. The output of Q3 is integrated by C11, which then drives the TM output stage, Q4. Since the time constant, R32 C11, is much greater than the headwheel period, the output signal level is equal to the average height of the pulse over one period. When the headwheel is running at normal speed, V_{c3} is a 400 μs square wave, and the HW speed telemetry signal = $V_{c3}/2V - V_{BE}$. Or, using the above worst case values of V_{c3}, the TM maximum output range is 4.30V to 5.33V.

4.3.4.4 Conclusions and Recommendations. - Worst case analysis of the tonewheel processor circuit has shown that reliable operation will be maintained over the temperature range of 0° C to 60° C for a lifetime of 10,000 hours. Although the above calculations indicate a considerable range of differential comparator input reference levels and multivibrator pulse widths, no degradation in network performance results.

4.4 Motors and Power

4.4.1 Introduction. - The basic circuits used for driving the motors and generating the internal dc voltages have remained unchanged for an appreciable length of time. However, associated with the changes in the command structure, there has been a significant modification of the power flow system. The new interface is summarized in block diagram form in Figure 4-106.

The major power flow changes are as follows:

1. Switching of the power to the DC/DC Converter is accomplished external to the recorder.

2. Voltage protection sensing is accomplished external to the recorder.

3. V.P. (Voltage Protection) reset is accomplished by a non-standard external command.

The changes in the command structure are delineated in the appropriate section.

4.4.2 DC/DC Converter Circuit Description. - The DC/DC Converter (Figure 4-107) is a dual-transformer converter with a common collector, push-pull chopper. Transistor switching is accomplished by a saturating toroidal transformer, and a

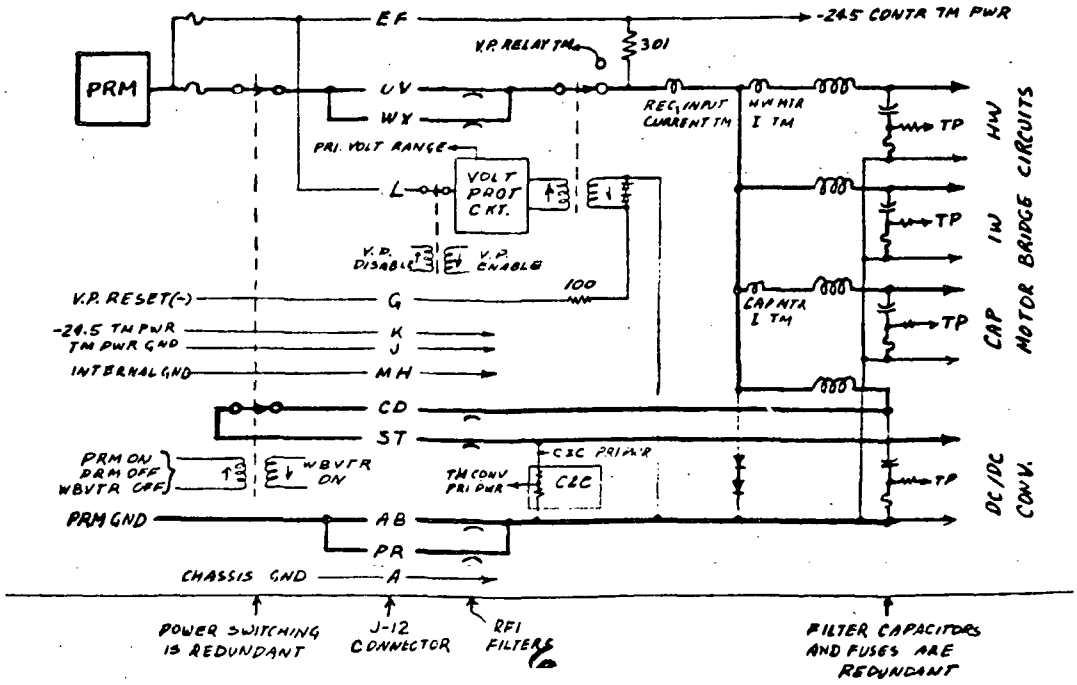


Figure 4-106. Power Flow System

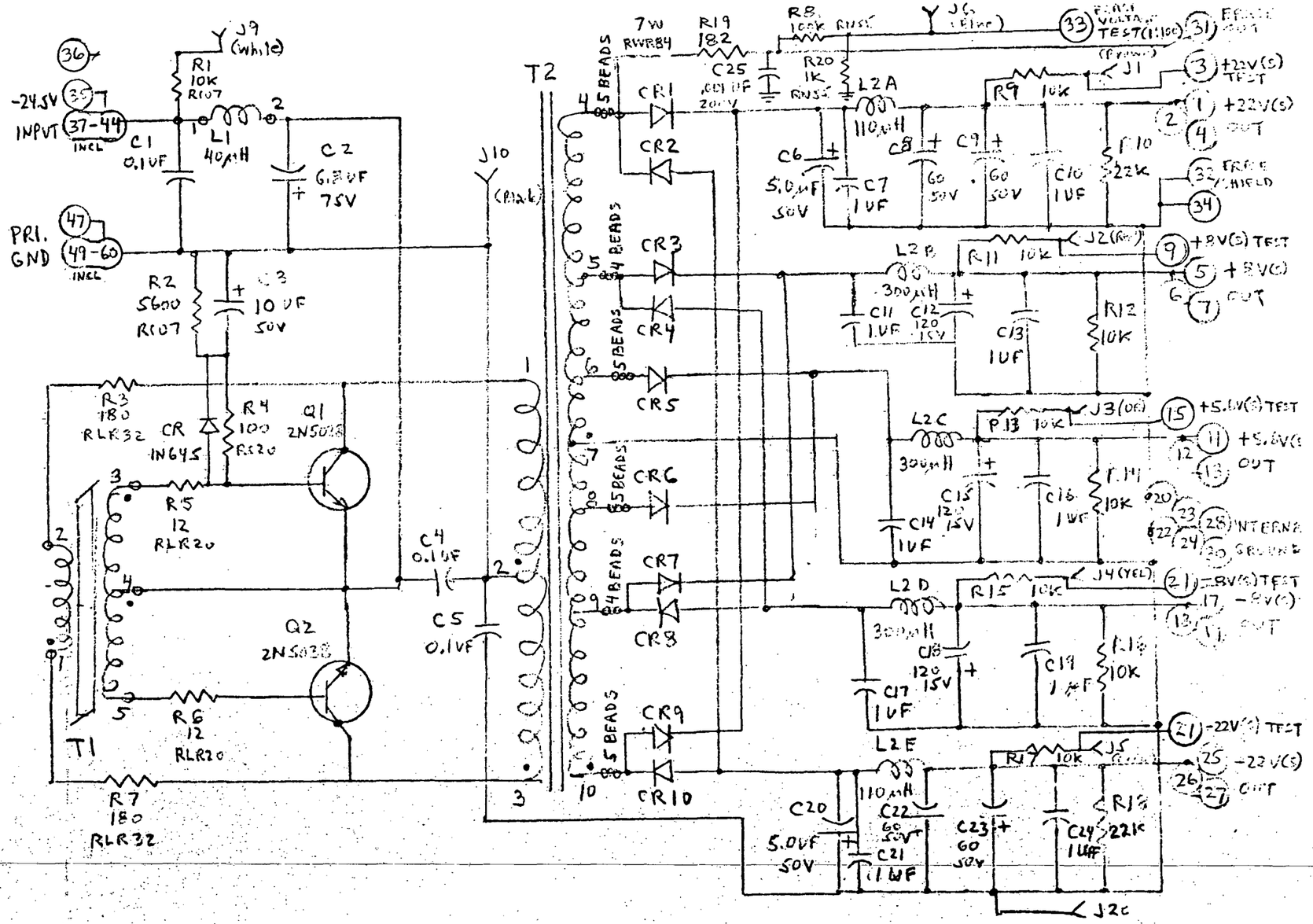


Figure 4-107. DC/DC Converter Schematic Diagram

linearly operating transformer provides the output power transformation. Transistor switching occurs when the "on" transistor is cut off by the decrease in base current which occurs when the toroidal transformer saturates. As the core reaches saturation, the increasing magnetizing current causes an additional voltage drop across the two feedback resistors. Thus, the primary winding of the saturated transformer has less voltage dropped across it, effecting the decrease in secondary or base-drive voltage. The frequency of oscillation is determined primarily by the saturating transformer peak square-wave voltage, number of primary turns, core maximum flux density and cross sectional area.

The secondary of the power transformer is tapped to provide five full-wave rectified voltage levels: ±22, ±8 and +5.6 volts nominal. Each supply is filtered by an LC network, and an output bleeder resistor is incorporated into the circuits to discharge the filter capacitance under no load conditions.

4.4.3 Voltage Protection Circuit Description. - The allowable system primary voltage variation is relatively large (18 to 39 V transient and 20-34.5 V continuous). In order to avoid component degradation within the recorder, it is necessary to limit this range to 24.5 V ±5%. Overvoltage protection prevents damage to electronic components, while undervoltage protection avoids excessive heating of motors and motor drive circuits which could eventually result in an increase in component failure rates.

The voltage protection circuit responds as follows. (See Figure 4-108). When the primary voltage supply rises above 26 volts, the voltage protection circuit immediately disconnects the recorder from the power source; the only delay is caused by relay activation times. In order to protect the TTL integrated circuits from overvoltage stress during relay activation, a separate fast-response circuit has been developed for the 5.6 V supply.

To avoid unnecessary shut-down due to brief undervoltage transients, a minimum delay of 41 ms is permitted when the voltage decreases below 23V, before the recorder is disconnected from the primary supply. In either case, once the recorder is shut down appropriate re-start commands will be required to resume operation.

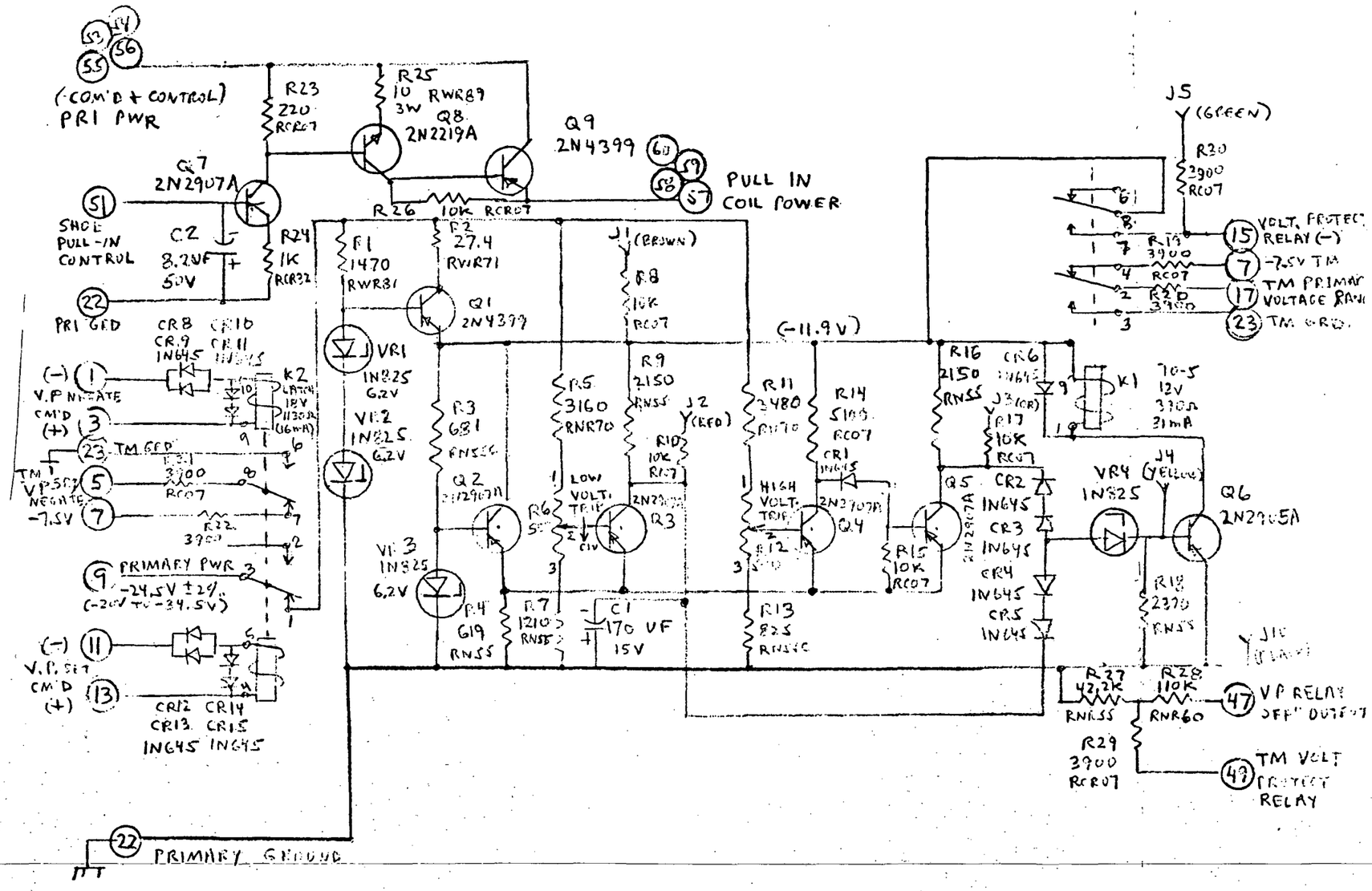
Zener diodes VR1 and VR2 provide a nominal 12.4 volts reference for series regulator Q1. Thus the emitter of Q1 maintains a relatively constant voltage across the basic detection circuit. The trip point references V_{B3} and V_{B4} are provided by zener VR3 and emitter follower Q2. It may be noted that since transistors Q2, Q3, Q4 and Q5 are of the same type, the effects on the reference level of V_{BE} variations due to temperature and aging are minimized. The low voltage trip level is sensed by Q3 through R5, R6 and R7. Q3, which is normally ON, is turned off when the primary voltage drops, turning on relay driver Q6, which in turn activates the voltage

protection relay. Q6 turn-on is delayed by the R9C1 time constant. Diodes CR4, CR5 and VR4 provide the necessary level shift to ensure that Q6 remains OFF during normal non-protect operation.

Similarly, Q4 senses a high primary voltage through resistor divider R11, R12 and R13. At the high trip level, Q4, which is normally OFF, turns on, driving Q5 OFF. Unlike the low voltage protection case which permits a delay for transients, Q6 is turned on immediately, activating the voltage protection relay.

4.4.4 Motor Drivers and Bridges. - The ERTS recorder system contains three motors (Headwheel, $I\omega$ balancing and Capstan) each requiring its own drive circuitry. The circuit configuration for each motor is identical, the only difference being the individual frequency of operation.

There has been no change in the design of these circuits. Hence, the description given in the Second Quarterly Report is still correct.



A10

31 mA at -24.5 V = 0.76 W
74+80 mA at -24.5 V = (2.5+2.75 W)
~300 mA at -24.5 V Failure Mode (Est)

Figure 4-108. Voltage Protection Circuit Schematic Diagram

4.4.5 DC/DC Converter Worst Case Analysis. - The DC/DC Converter has been analyzed to ensure reliable operation under the ERTS system environmental requirements. Performance limitations of all critical functions due to component and semiconductor parameter manufacturing tolerances and aging effects were determined. (See Appendix H for analysis criteria.)

4.4.5.1 Design Considerations. - Since the converter outputs are unregulated, the worst case primary supply input level and the output loading requirements must be determined accurately in order that the output transformer turns ratio can be specified high enough to compensate for series losses.

In designing the transformers, cores should be chosen with a high flux density to minimize the iron and copper mass. Wire size should be compatible with the load current and, in order to reduce copper loss and interwinding capacitance effects, the number of turns should not be excessive.

The transistor selection is based on the operating frequency, with the storage time being made less than the switching period. The peak value of the collector-to-emitter voltage breakdown rating of each transistor must be equal to twice the supply voltage plus the amplitude of any voltage spikes. The saturation voltage should be as low as possible to reduce collector dissipation and the collector current rating must be greater than the worst case turn-on surge. Conditions which may result in secondary-breakdown should be analyzed to ensure that the transistor specifications are not exceeded.

Worst case primary power turn-on and turn-off transients should be measured to determine the effects on associated subsystems.

4.4.5.2 Summary. - The converter input voltage (-24.5 Vdc primary) drops approximately 0.37V due to series losses under worst case steady state (MSS Playback) and approximately 0.65V during initial converter turn-on. Output regulation results are shown in Table 4-27, with the worst case deviation being +7.2, -2.3% for the +5.6 Volt supply, including the primary supply operating limits. Output ripple results are shown in Table 4-28. The overall range is 10 mVpp in the standby mode to 40 mVpp in the MSS playback mode, both measured at the 5.6V supply. The tentative maximum output power requirements is 47.2 watts, including the erase current, and the calculated efficiency is approximately 83% at maximum load.

The push-pull transistor current and voltage specifications exceed the circuit operating requirements, and base drive is sufficient for minimum gain under worst case temperature and loading conditions. A starting circuit is included in the design to ensure turn-on under worst case current surges.

TABLE 4-27. DC/DC CONVERTER REGULATION VS PRIMARY VOLTAGE AND OUTPUT LOAD VARIATION

	Primary Input = 24V			Primary Input = 24.5V			Primary Input = 25V		
Nominal Output (Volts)	Standby	Record	MSS Playback	Standby	Record[3]	MSS Playback	Standby	Record	MSS Playback
+22	21.8	21.2	21.1	22.24	21.56	21.55	22.7	22.1	22.0
+ 8	7.88	7.63	7.45	8.08	7.79	7.64	8.25	7.99	7.80
+ 5.6	5.77	5.67	5.47	5.92	5.79	5.62	6.03	5.95	5.74
- 8	7.80	7.63	7.43	7.99	7.79	7.62	8.11	7.99	7.78
-22	21.7	21.2	21.0	22.20	21.59	21.53	22.7	22.1	21.9

Notes:
1. T2 turns ratio: Np = 30, Ns = 23, 3, 11
2. Primary input voltage was measured at the command control relay outputs.
3. Erase output grounded.
4. Measurements are at 25°C ambient.

TABLE 4-28. DC/DC CONVERTER OUTPUT RIPPLE

Nominal Output Volts	Peak-to-Peak Ripple (MV)	
	Standby Mode	MSS Playback Mode
+22	10	25
+8	10	20
+5.6	15	40
-8	10	20
-22	10	25

Notes: 1. Peak-to-Peak measurements taken across a resistive load.
2. The above measurements do not include switching spikes.

The turn-on current surge on the primary input line is 5A peak, with a rise time of 0.7 ms, a fall time of 2 ms and a duration of 3.0 ms. The maximum output voltage rise time is 1.5 ms for all supplies, and the maximum fall time is 50 ms for the ±22V supply in the standby mode.

4.4.5.3 Worst Case Analysis. - The following analysis is based on the revised DC/DC Converter schematic shown in Figure 4-107. An ambient temperature range of 0° C to 60° C over a 10,000 hour lifetime was used for component and parameter derating. Individual component specifications used in the computations are given in Appendix A.

The converter circuit was analyzed with respect to converter input voltage variation, maximum power requirements, starting reliability and maximum power dissipation. In addition, laboratory measurements were performed of the turn-on current surge, turn-off transient, output ripple and load regulation.

a. Converter Supply Voltage Variation. - As shown in Figure 4-109, the converter input voltage depends on the current flow through the Command/Control relays and the input choke, LG. During normal operation, the input current is relatively constant but increases when the tape transport motors are started.

Using the notation of the figure, the converter voltage is given by:

$$V_1 = V_{in} - I_{in} (R_F + R_{K1}) - I_1 (R_{LG} + R_{K2} + R_{L1}) \quad (1)$$

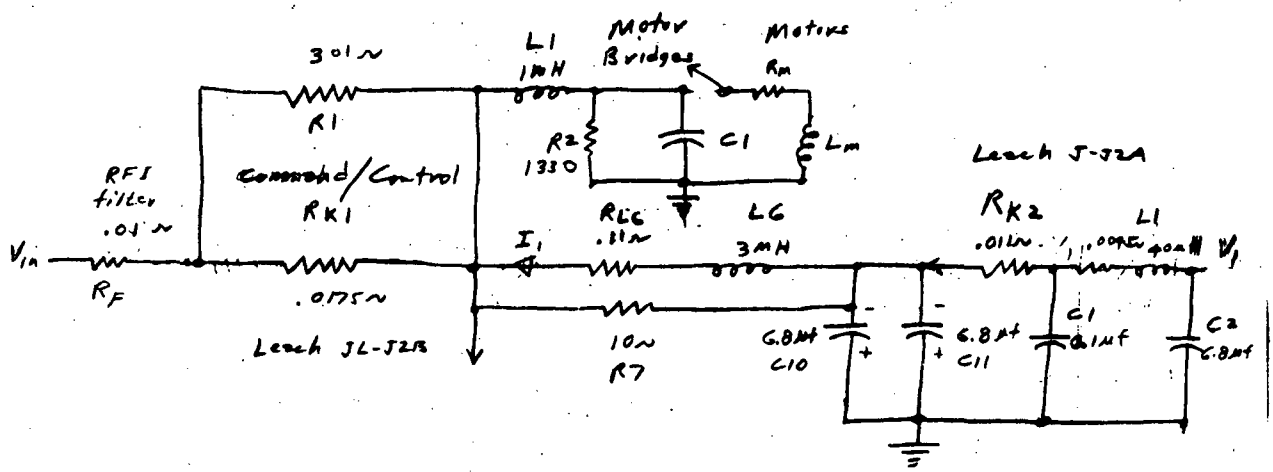


Figure 4-109. Converter Input Interface Equivalent Circuits

1. Steady State Operation. - During steady state operation, with the motor running, and assuming $I_{in} = 4.5A$ and $I_1 = 2A$, from equation 1, the converter input voltage is:

$$V_1 = V_{in} - 0.376V$$

Motor Starting. - When the headwheel and I_W motor are in their starting cycle, the peak input current is approximately $I_{in} = 14.5A$. Assuming little change in I_1, then from equation 1, the converter input voltage is:

$$V_1 = V_{in} - 0.65V$$

b. Output Transformer Ratio. - The output transformer, T2, is shown in Figure 4-107. The primary-to-secondary turns ratios are based on the projected voltage drops in each of the output circuits. Therefore,

to compensate for output losses, the open circuit output voltages as shown in Table 4-29 are somewhat higher than the desired nominal output dc levels. The required number of turns between transformer taps is as follows:

Tap Numbers	Number of Turns
1-2, 2-3	39
6-7, 7-8	11
5-6, 8-9	3
4-5, 9-10	23

c. Power Requirements. - The converter efficiency may be written as:

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} \tag{2}$$

Where the output power, P_{out}, is the system loading requirement, and, P_{loss} is due to converter internal dissipation.

TABLE 4-29. OUTPUT TRANSFORMER VOLTAGE AS A FUNCTION OF INPUT LEVEL

Primary Voltage	Secondary Voltage		
Taps 1-2	Taps 6-7	Taps 5-7	Taps 4-7
25	7.05	8.95	23.7
24.5	6.9	8.79	23.2
24.0	6.77	8.6	22.8
23.6	6.65	8.45	22.4
23.1	6.5	8.30	22
Turns Ratio	0.282	0.358	0.95

Notes:
1. T2 Turns Ratio: Np = 39, Ns = 23, 3, 11
2. Secondary Voltages are calculated, assuming no transformer losses.

1. Converter Loading. - The DC/DC Converter load requirements are shown in Table 4-30. Minimum total output power is 14.9 watts in the standby mode and maximum power output is 47.2 watts in MSS playback mode.

2. Internal Dissipation. - Neglecting output filter choke losses, internal dissipation is primarily due to discharge resistor drain, P_{RC}, rectifier drops, P_D, output transformer core loss, P_{core}, and magnetizing current leakage, P_{IM}, and transistor collector dissipation P_Q. Thus, converter internal dissipation may be written as:

$$P_{loss} = P_{RC} + P_D + P_{core} + P_{IM} + P_Q \quad (3)$$

From Figure 4-107, the discharge resistor loss is:

$$P_{RC} = 2\frac{V_{22}^2}{R_{10}} + 2\frac{V_8^2}{R_{12}} + \frac{V_{5.6}^2}{R_{14}} \quad (4)$$

Using nominal voltage and resistor values, and substituting into equation 4, $P_{RC} = 0.06W$.

TABLE 4-30. DC/DC CONVERTER LOAD REQUIREMENTS

Nominal Output Voltage	Standby		Record		MSS Playback	
	ma	Watts	ma	Watts	ma	Watts
+22	187	4.12	820	18.0	530	11.65
+8	52	.415	168	1.35	557	4.46
+5.6	775	4.35	1000	5.6	2090	11.70
-8	162	1.30	292	2.3	882	7.10
-22	214	4.70	665	14.6	559	12.30
Erase	-	-	130 peak	2.95	-	-
TOTALS		14.9		44.8		47.2

Since each diode conducts for 1/2 cycle, the total diode dissipation is equivalent to considering one diode in continuous conduction. Then,

$$P_D = I_{+22} V_{CR1} + I_{+8} V_{CR3} + I_{+5.6} V_{CR5} + I_{-8} V_{CR7} + I_{-22} V_{CR9} \quad (5)$$

Again using nominal values, and substituting into equation 5,

$P_D = 3.88W$

Core loss depends on the flux density of the core material, B, the frequency of oscillation, and the volume of core material; or:

$$P_{core} = P_{fB} A \, ml \, D \quad (6)$$

where,

P_{fB} = core loss at the operating frequency and nominal flux density - watts/lb.

A = Effective core cross sectional area - cm^2

ml = Mean length of the magnetic path - cm

D = Magnetic alloy density (8.7 gms/cm^3 for nickel-iron)

For the square permalloy 80 core, nominal B = 7.4 kilogausses, and at a frequency of 22 kHz, from the manufacturers core loss characteristics, P_{fB} = 35 watts/lb. Then substituting the core specifications into equation 6, $P_{core} = 0.91W$.

Power loss due to magnetizing current leakage, I_M, is:

$$P_{IM} = V_P I_M \quad (7)$$

where, V_p = the transformer primary voltage, and the magnetizing current is given by:

$$I_M = \frac{0.794 \, H \, ml}{N_p} \quad (8)$$

where,

H = the magnetizing force - oersteds

Np = number of primary turns

ml = mean length of the magnetic path - cm

From the manufacturer core characteristics, $H \approx 0.3$, and substituting into equation 8, $I_M = 53.4$ mA. Assuming the converter input voltage is approximately equal to the primary supply, or $V_p \approx V_1 = 24.5V$, then substituting into equation 7, $P_{IM} = 1.3W$.

Neglecting base dissipation and switching losses, and due to symmetry, assuming one transistor is always ON, the push-pull transistor dissipation may be approximated by:

$$P_Q = I_C V_{CE} \tag{9}$$

Q1 and Q2 collector current, I_c, may be approximated by assuming a converter efficiency of $\eta = 80\%$, then:

$$P'_{in} = \frac{P_{out}}{0.80} = 59 \text{ watts}$$

and,

$$I'_c = \frac{P'_{in}}{V_1} = 2.4A$$

For $V_{CE} = 0.5V$, then from equation 9, $P_Q = 0.96W$.

Now, substituting the above results into equation 3, $P_{loss} = 7$ watts. Assuming 2-1/2 watts of other losses (switching, resistor, choke, etc.), $P_{in} = 47.2 + 9.5 = 56.7$ watts. Then, from equation 2, projected converter efficiency is $\eta = 83.5\%$.

d. Transformer Efficiency. - By using the previously calculated transformer losses, the output transformer efficiency, $\eta 2$, may be determined. Or:

$$\eta 2 = \frac{P_{1\ out}}{P_{1\ in}} \tag{10}$$

where,

$$P_{1\ loss} = P_{core} + P_{IM} \tag{11}$$

From previous calculations, $P_{in} = 56.7$ watts and P_1 loss = 2.21 watts, then from equation 10, $\eta 2 = 96.5\%$.

e. Push-Pull Transistor Amplifier. - Push-pull transistors Q1 and Q2 are driven by a saturable basedrive transformer T1. Power is transferred to the load through the linearly operating output transformer T2.

1. Base Drive.

Maximum Load. - The maximum base drive requirement is based on the maximum converter load. Using a maximum load of P_{out} = 50W, and an efficiency of η = 83%, then P_{in} = 60 watts. The maximum base drive requirement is given by:

$$\overline{I_B} = \frac{\overline{I_C}}{h_{FE}} \tag{12}$$

where maximum collector current is:

$$\overline{I_C} = \frac{P_{in}}{V_1 - \overline{V_{CE}}} \tag{13}$$

At 0°C, where h_{FE} is a minimum, h_{FE} = 26, $\overline{V_{CE}}$ = 0.49. For V_{in} = 24V, V_1 = 23.6V and substituting into the above equations, $\overline{I_C}$ = 2.6A and I_B = 100 mA. Total base input power may be written as,

$$\overline{P_B} = \overline{I_B}\,\overline{V_{BE}} + \overline{I_B^2}\,\overline{R_B} \tag{14}$$

Substituting 0°C worst case values into equation 14, $\overline{P_B}$ = 0.26 watts. T1 secondary voltage, V_{S1} is given by:

$$V_{S1} = \frac{P_B}{I_B} \tag{15}$$

Or, V_{S1} = 2.5 volts. For a turns ratio of 14 (1/2 the secondary), V_{P1} = 2.6 x 14 = 36.5V. Assuming a transformer efficiency of η_1 = 97%, then T1 primary power is, P_{in1} = 0.268W, from which the primary current is I_{P1} = 7.35 mA. The available primary voltage is:

$$2V_1 = 47.26V$$

The drop across the feedback resistors is:

$$I_{P1} R_{fb} = 2V_1 - V_{P1} \quad (16)$$

or, $I_{P1}R_{fb} = 10.76V$, and solving for the allowable feedback resistor, $R_{fb} = 1470$ ohms. Since $R_{fb} = R3 + R7 = 360$ ohms, sufficient base drive is available for reliable switching under worst case conditions.

Available Base Drive. - Assuming a T_1 primary current of approximately 8 mA, from equation 16, $V_{P1} = 44.39V$, and $V_{S1} = 3.13V$. Since the base input voltage is:

$$V_{S1} = V_{BE} + I_B R_B \quad (17)$$

Substituting worst case values into equation 17, and solving I_B:

$$I_B = \frac{V_{S1} - V_{BE}}{R_B} \quad (18)$$

and, at 0°C, available $I_B = 142$ mA, and the corresponding allowable $I_c = 3.90A$. When translated to output power capability, the input power is $P_{in} = 93W$ and for 80% efficiency, allowable $P_{out} = 75W$.

2. Transistor Turn-On Surge. - When the converter is turned on, both Q1 and Q2 initially saturate due to the turn-on surge current. The peak collector current surge is 8A with a rise time of 0.9 ms and an overall duration of 1.8ms. As the surge decays, the converter begins to oscillate after approximately one ms. The above peak collector current is well within the transistor maximum limit of 30A.

3. Starting Circuit. - To ensure converter oscillation at initial power application, especially under load, an ac coupled resistor voltage divider network has been used to supply the necessary starting current. Using an RC circuit requires a large turn-on pulse; however, the advantage of this technique is that dc power loss is minimized. At turn-on, C3 appears as a short and the transistor base current is supplied through R4. The recorder will be in the standby mode during turn-on and the required base current is given by:

$$I_B = \frac{I_c}{h_{FE}} \quad (19)$$

Where I_c is the steady state standby collector current, which may be derived from the standby output power of approximately 20 watts. For a light load converter efficiency of 70%, the input power is 28.5 watts and $I_c = 1.2A$. And from equation 19, for $h_{FE} = 27$, assuming a 24 volt turn-on pulse with sufficient duration to overcome the turn-on surge, maximum required $I_B = 45$ mA. Therefore maximum allowable R4 is:

$$\overline{R_4} = \frac{V_P}{I_B}$$

Or for a turn-on pulse $V_P = 24V$, and $I_B = 45$ mA, maximum allowable R4 = 530 ohms, which is greater than the design value of R4 = 200 ohms, thus ensuring reliable turn-on.

The duration of the turn-on pulse is governed by the R4C3 time constant. Nominal R4C3 = 1 ms, which is approximately equal to the turn-on surge duration and results in only a slight decay in available base current prior to turn-on.

4. Power Dissipation. - Maximum power dissipation will be calculated to determine whether the converter transistors are operating within their specified maximum dissipation ratings. In addition, their maximum junction temperatures must be estimated for purposes of reliability evaluation and to determine heat sink requirements.

Collector Dissipation. - Since the switching period is small compared to the transistor thermal time constant, average power may be used for purposes of analysis. Neglecting base dissipation, average collector circuit power over a complete cycle is given as,

$$P_{avg} = \frac{V_{CE}(ON)\,\overline{I}_c\,t_{on} + \overline{V_{CE}}(OFF)\,\overline{I_{cbo}}\,t_{off}}{T} + \frac{V_{CE}(OFF)\,I_c\,t_{sw}}{3T} \qquad (20)$$

where,

T = switching period $= \frac{1}{22\text{ kHz}} = 45.5$ us

$t_{sw} = t_r + t_f$ (rise time + fall time)

Worst case power dissipation occurs at 60°C in the MSS playback mode. Assuming little variation in system power requirements due to temperature, then from previous calculations, $\overline{I_c} = 2.6A$. For a switching time of $t_{sw} = 1$ us, substituting worst case values into equation 20, $\overline{P}_{avg} = 1.37W$ for one transistor, or 2.74W for both Q1 and Q2.

Heat Sink Requirements. - Presently available heat sink area is approximately 4 in^2, and is limited to radiation. Radiant heat transfer is given by:

$$Q = A_1 e_1 \sigma (T_1^4 - T_2^4) \text{ BTU/hr.} \qquad (21)$$

where,

A_1 = heatsink area (ft^2)

e_1 = emissivity (1 for black body)

σ = Stefan-Boltzman constant (0.173×10^{-8} BTU/hr-ft^3 R4)

T_1 = temperature of heat sink (°Rankine)

T_2 = temperature of surrounding surface (°Rankine)

For a uniform heat sink temperature, equation 21 may be solved for the required radiation area. Or,

$$A_1 = \frac{Q}{e_1 \sigma (T_1^4 - T_2^4)} \qquad (22)$$

Since maximum allowable junction temperature is 110°C, $T_1 = 690°R$. For $T_2 = 60°C = 600°R$ and Q = 2.74 watts = 9.35 BTU/hr., solving equation 22, the minimum allowable radiant heat sink area is $A_1 = 7.9$ in^2. Therefore, the present heat sink area must be increased or some means of heat conduction should be provided.

In a failure mode, the input voltage may increase to about 27V before the Voltage Protection circuit will activate. The resulting Q1 and Q2 worst case power dissipation will be approximately 3 watts. However, manufacturer's allowable junction temperature is 175°C and, if the heat sink requirements for normal operation are fulfilled, the transistors will not be damaged.

5. Breakdown Voltages. - Due to push-pull operation, the converter transistor reverse voltage is twice the input supply voltage plus switching transients. Or, minimum allowable collector-emitter breakdown voltage is given by:

$$V_{CEO} \geq 2\, V_1\, (1 + 0.20) \qquad (23)$$

The minimum allowable V_{CEO} = 60V. From the manufacturer's specifications, maximum V_{CEO} = 90V, which exceeds the converter requirements.

Manufacturer's specifications for secondary-breakdown with the base-emitter junction forward biased are: 30A at 25°C, derated by 25% at 60°C (22.5A), which is much greater than converter circuit transients.

The allowable base-emitter junction reverse votlage is 7 volts, which is less than the peak base input reverse voltage of approximately 3 Volts.

f. Converter Output. - The connector output circuit consists of the full wave rectifiers, LC filters, and square wave erase signal.

1. Rectifiers. - Due to their forward voltage drop, rectifier power dissipation is substantial and considerable heat dissipation is required.

Power Dissipation. - Since all the rectifiers are mounted on a common heat sink, worst case heating occurs for maximum total power dissipation, or in the MSS playback mode. Diode average power dissipation may be written as:

$$P_{avg} = \frac{V_f\, I_f\, t_{ON} + V_R\, I_R\, t_{OFF}}{T} + \frac{V_{sw}\, I_f\, t_{sw}}{3T} \qquad (24)$$

where,

$t_{sw} = t_r + t_f$ (diode rise and fall times)

For t_{sw} = 0.4 us, $t_{on}/T = 0.494$ and $t_{sw}/3T = 2.93 \times 10^{-3}$, equation 24 reduces to,

$$P_{avg} = V_f\, I_f\, (0.494) + V_R\, I_R\, (0.494) + V_{sw}\, I_f\, (2.93 \times 10^{-3}) \qquad (25)$$

Substituting worst case values into equation 25, at 60°C, the diode dissipations are as follows:

CR1/CR2 - 2 P_{avg} = 0.514W

CR3/CR4 - 2 P_{avg} = 0.506W

CR5/CR6 - 2 P_{avg} = 2.128W

CR7/CR8 - 2 P_{avg} = 0.812W

CR9/CR10 - 2 P_{avg} = 0.542W

Total rectifier dissipation = 4.5W

Heat Sink Requirements. - The diode heat sink has been designed such that a low thermal resistance contact will be maintained between the heat sink and the Electronic Unit chassis, resulting in what is considered an infinite heat sink. Therefore, the maximum case temperature will be approximately 60°C; and for a thermal resistance of θJ-C = 9°C/A, the maximum diode junction temperatures will be as follows:

CR1/CR2 - 64.8°C

CR3/CR4 - 65°C

CR5/CR6 - 78°C

CR7/CR8 - 67.9°C

CR9/CR10 - 65°C

which are well within the maximum allowable diode junction temperatures of 110°C.

2. Filters. - Each of the full wave rectified outputs is filtered by an LC filter. Since the input signal is a square wave, the filter dc output is equal to the peak square wave input. The only ripple is due to unsymmetrical levels resulting from component tolerances. In addition, switching spikes of 300-400 mV peak-to-peak, which are not completely suppressed by the LC filter, appear on the output. These spikes have been suppressed considerably with the addition of ferrite beads on the transformer output leads.

g. Erase Output. - The 46 Vpp square wave erase current signal is tapped off the +22V winding (tap no. 4) through a 180 ohm resistor. Since the erase current is used only in the Record mode, it does not add to the worst case converter load, which is MSS playback mode.

The erase head impedance is given as L = 0.75 mH and R_L = 0.55 ohms. Thus, assuming the erase output approaches a current source, the minimum peak erase current is given by:

$$I_x = \frac{V_{secondary}}{R_{19}} \quad (26)$$

Or, $\overline{I_x}$ = 125 mA peak. Neglecting the coil resistance, the current rise time is given by:

$$T_r = \frac{L}{R_{19}} \quad (27)$$

Using nominal values, T_r = 4.2 us, which is approximately one-fifth of the current pulse width.

The series resistor (R19) power dissipation may be calculated from:

$$P_E = \frac{V^2}{R_{19}} \quad (28)$$

Using nominal values, P_E = 3W.

4.4.5.4 Laboratory Test Results.

a. Primary Power Switching. - Since the dc/dc converter represents a RLC load, when the primary power is turned on or off, both current and voltage transients result at the input and output.

1. Input Transients. - The primary power input turn-on/off current surge is shown in Figure 4-110. The turn-on surge is about 5.5A, with a rise time of 0.7 ms, fall time of 20 ms, and a transient duration of 3.0 ms. (measured at the 50% level)* A turn-off current surge of about 1.5A was measured. Since the input choke is shunted with a damping resistor and a diode clamp is used, turn-on/off voltage transients were negligible.

*Subsequent measurements on a second model have shown a lesser turn-on transient, which may be attributed to component tolerances.

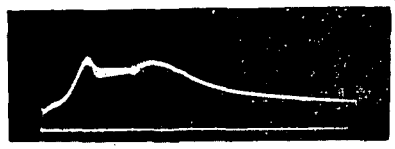


Figure 4-110. Primary Voltage Turn On Current Transient

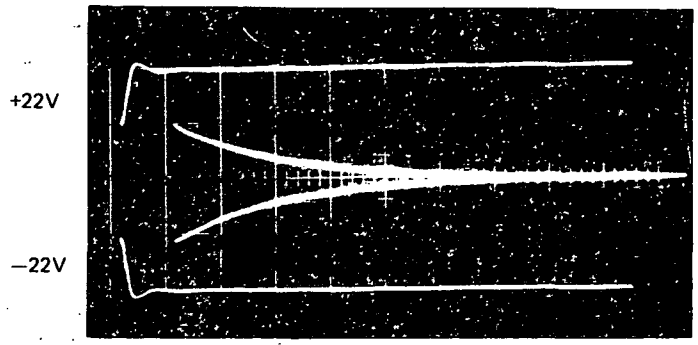
2. Output Voltage Transients. - The output voltage turn-on/off transients are shown in Figure 4-111. A 5% overshoot of about one ms duration occurs during turn-on for all five outputs driving a resistive load, at the standby power level. Again, using standby power loading, the output rise time is 1.5 ms for all supplies and the fall times are 50 ms for ±22V, 30 ms for ±8V and 2 ms for +5.6V.

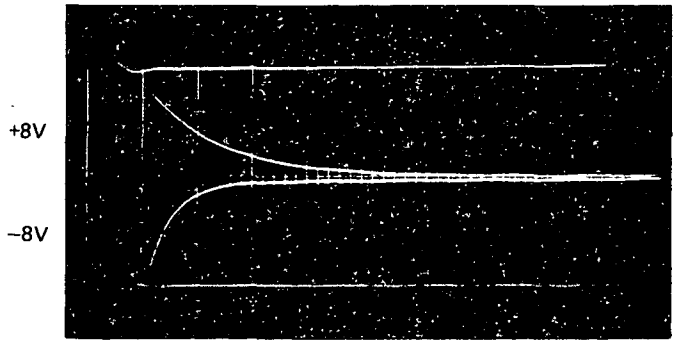
   No significant transients occur on the converter outputs when switching between standby and MSS playback power levels.

b. Converter Regulation Data. - Converter regulation test results are shown in Table 4-27. Data were taken for three primary power levels -24.5 and -24.5 ±2% under standby, record and MSS playback load requirements. The overall voltage variations are: +22V +3.2, -4.1%; -22V, -3.2, +4.5%; +8V, +3.1, -4.5%; -8V, -1.4, +4.8%; +5.6V, +7.2, -2.3%. The above voltage ranges are all within the original specifications except for the +5.6V high level, which is about 2% too high. However, the higher 5.6V level is required, since it decreases considerably with loading, relay contact and line losses.

4.4.5.5 Conclusions and Recommendations. - Worst case analysis of the DC/DC converter has shown that the circuit will operate reliably over the temperature range of 0°C - 60°C for a lifetime of 10,000 hours under a projected maximum load of 50 watts. In order to meet system maximum transistor junction temperature requirements for Q1 and Q2, either a large heat sink will be used to increase the radiation area, or additional dissipation will be provided by utilizing heat conduction techniques.* Since the starting circuit is ac coupled, a turn-on pulse of at least 12

*Design of the transistor heat sink has not been finalized due to collector capacitance considerations with regard to switching transients.





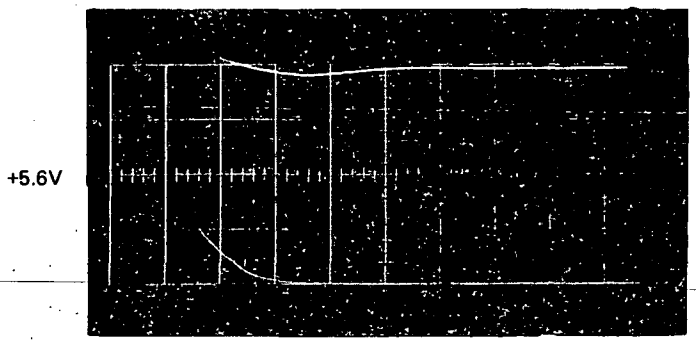


Figure 4-111. Converter Output Voltage Turn ON/OFF Voltage Transients

volts is required to start the converter. In addition, due to the turn-on current surge, the start is delayed approximately one ms until the surge subsides. It should be recognized that since there is no internal regulation in the converter, the dc output levels are sensitive to both primary input voltage changes and output load variations. Thus any revision of the present converter input/output specifications may require modifications of the output transformer turns ratio to compensate for a corresponding increase or decrease in dc supply level.

The measured converter turn-on current surge rise time of 0.7 ms is much faster than ERTS system specifications allow. However, the peak surge is a short transient which may not be detrimental to the primary power supply operation. To increase the turn-on time would require a larger input choke to suppress the current surge, or a reduction in the amount of output filter capacitance to decrease the charging current. A larger choke would add considerable size and weight to the system, and less filter capacitance would increase the output ripple. Thus, neither of the above solutions is entirely satisfactory and some other compromise should be considered if the present turn-on current transient is undesirable.

4.4.6 Voltage Protection Circuit Worst Case Analysis. - The Voltage Protection Circuit has been analyzed to ensure reliable operation under the ERTS system environmental requirements, using the criteria of Appendix H. Performance limitations of all critical functions due to component and semiconductor parameter manufacturing tolerances and aging effects were determined.

4.4.6.1 Design Considerations. - Sufficient drive capability must be provided in order that the switching circuits may operate properly under maximum load, minimum gain conditions. At the same time, quiescent stability must be maintained under high gain, high leakage current conditions.

During an increase in primary voltage, recorder disconnect should be as fast as possible, preventing component degradation due to overstressing. On the other hand, for a decrease in primary voltage, recorder disconnect must be delayed a minimum of 35 ms to avoid shut down during the switching of the primary voltage regulators in the event of regulator malfunctions. Since a number of components, particularly motors, begin to overheat under low voltage operation, maximum low voltage disconnect delay should not be excessive.

Components directly related to the trip voltage adjustment should be selected to minimize trip point drift due to both temperature and aging. Trip point control potentiometer range must be great enough to allow trip point adjustment for worst case components.

4.4.6.2 Summary. - Following a preliminary analysis, several changes in component types and values were incorporated into the voltage protection network to improve both performance and stability. Changes are shown in the component list, Appendix A, and Figure 4-108 reflects the revised circuit. In addition, the analysis and results discussed below pertain to the revised network.

The voltage protection circuit series voltage regulator was found to be stable throughout the primary supply range of 18-39 volts. Overall output variation, V_{E1}, was approximately +1, -4% of nominal. Load regulation and temperature stability were also adequate. In addition, reliable circuit operation is possible for transients as low as 12.6V and a continuous low voltage level of 13.8V.

At continuous voltage levels of less than 13.8V, the voltage protection circuit will be inoperative. However, such a failure mode of the primary voltage supply is considered to be unlikely and would also leave the recorder inoperative.

The trip point reference voltage, V_{B2}, is virtually independent of load current, temperature variations and the effects of aging. Maximum reference drift is less than ±0.1%.

All switching stages exhibit adequate gain for minimum h_{FE}, maximum loading conditions, and are stable under maximum h_{FE}, high temperature conditions. The maximum continuous power dissipations of transistors Q2 through Q5 are well within allowable limits, but Q1 requires a small heat sink to maintain the permissible junction temperature of 110°C during continuous high Vcc operation.

The minimum low voltage turn-off delay is 41 ms, which exceeds the system maximum transient of 35 ms. Maximum turn-off delay is 321 ms which is compatible with power transistor thermal time constants and motor response times.

The high voltage turn-off delay is caused by the accumulation of relay activation times, resulting in a maximum delay of 12 ms.

Worst case trip point drift as a result of temperature and aging are Vcc + 0.58, -0.45% and Vcc ±1.6%, respectively.

4.4.6.3 Worst Case Analysis. - The revised Voltage Protection Circuit is shown in Figure 4-108. The following analysis is based on the recommended component changes listed in Appendix A. An ambient temperature range of 0°C to 60°C over a 10,000 hour lifetime was used for component and parameter derating. As given in the system specifications, the continuous primary power variation is -20 to -34.5 volts, with 35 ms transients of -18 or -39 volts peak. Relay coil resistance variations as a function of temperature were determined linearly using the temperature coefficient of copper. When derated transistor parameters were not defined in

manufacturer's specifications, the derating criteria shown in Appendix H were applied. These parameter derating guidelines are considered to be applicable to the ERTS system worst case requirements. Appendix H also contains a summary of resistor and capacitor derating factors as specified by Mil Standards.

a. Regulator Stability. - Q1 output voltage variation has been determined as a function of primary voltage change, loading and temperature.

1. Regulator Load Variation. - The regulator load is essentially constant during normal operation, but increases due to relay energizing current when the circuit is activated. Thus load current is given by:

$$I_L = I_{Quiescent} + I_{Relays} \quad (1)$$

From Figure 4-108, the quiescent current, assuming Q4 and Q6 cut off and neglecting leakage current, is

$$I_{Quiescent} = I_{E1} = I_{R3} + I_{C2} + I_{C3} + I_{C5} \quad (2)$$

and,

$$I_{Relays} = I_{C6} + I_{VP} \quad (3)$$

where,

VP = Voltage Protection Relay

Using nominal component values at 25°C; quiescently, $I_{E1} = 17.5$ mA. Since the relay coil resistance decreases with temperature, relay currents were computed at 0°C. Adding the currents for L_1 and L_{VP}, $I_{Relays} = 138.8$ mA. Substituting the above results into equation 1, at the trip point $I_L = 156.3$ mA. However, the base current change of Q1 is small due to loading compared to the nominal reference diode reverse current and, as a result, reference variation is primarily dependent on the change of reverse current resulting from the primary voltage, Vcc variation.

2. Primary Voltage Variation. - As the primary voltage varies over the range -18 to -39 volts, the current through the reference diodes VR1 and VR2 changes due to both Vcc and the increased loading resulting when either the high or low voltage trip levels are exceeded.

From Figure 4-108, diode reverse current is:

$$I_Z = I_{R1} - I_{B1} \tag{4}$$

Since,

$$V_{cc} = I_{R1} R_1 + V_{B1} \tag{5}$$

Then I_2 as a function of both Vcc and Q1 base current is:

$$I_Z = \frac{V_{cc} - V_{B1}}{R_1} \tag{6}$$

Assuming V_{B1} relatively constant, I_Z may be determined at various levels of Vcc. Thus using the diode reverse current vs breakdown voltage characteristics, as shown in Table 4-31, V_{B1} may be determined as a function of Vcc. Also, as shown in Table 4-31, the variation in breakdown voltage temperature coefficient has been obtained as a function of reverse current. Using the results of the table, V_{B1} variation is +0.64% with increasing Vcc and -0.96% with decreasing Vcc.

The value of Vcc continuous, as which zener regulation ceases, that is, $I_Z = 0$, may be computed from equation 6, letting $V_{B1} = 11.8$; then, Vcc = 18.6V. Similarly, the minimum transient value of Vcc at which zener regulation ceases is Vcc = 12.6V. If the regulated voltage, V_{E1}, is permitted to drop to 9.25V (the minimum relay activation voltage) continuous Vcc operation is limited by the saturation of Q1, and continuous minimum Vcc = 13.8V.

3. Temperature Stability. - As shown in Table 4-31, the zener diode temperature coefficient is related to the magnitude of reverse current. The mean value approaches 0 at the recommended breakdown current of 8 mA, and the maximum coefficient, -0.4%/°C, occurs at breakdown currents of less than one mA. In general, the variation of V_{B1} due to changes in temperature is negligible compared to the effects of breakdown current variation.

b. Trip Reference Level Stability. - Zener diode VR3 provides the trip reference level for both high and low voltage sensing. Thus since small changes in reference level are amplified by the sensing resistor dividers, load and temperature stability are critical.

TABLE 4-31. VARIATION OF BV VS. Vcc FOR 1N825

Vcc	I_Z (mA)	Typical BV	Max. Temperature Coef. (%/°C)		Typical V_{B1}
39 AT	12.9	6.32	+0.01	-0.005	12.64
34.5 AT	10.1	6.3	+0.01	-0.005	12.6
27 AT	5.2	6.27	+0.008	-0.02	12.54
27 BT	9.15	6.3	+0.01	-0.008	12.6
24.5 BT	7.55	6.28	+0.01	-0.01	12.56
22 BT	5.85	6.27	+0.01	-0.012	12.54
22 AT	1.80	6.18	+0.005	-0.03	12.36
20 BT	4.45	6.26	+0.008	-0.02	12.52
20 AT	0.5	6.1	0	-0.04	12.20
18 BT	3.2	6.22	+0.008	-0.02	12.44
18 AT	0				11.1

NOTES:
1. BT = Before Trip Condition
2. AT = After Trip Condition
3. Typical Values are at 25°C
4. V_{B1} = 12.4V, I_{B1} = 0.55 mA, I_{B1} AT = 4.6 mA

1. Load Variation. - The supply voltage, V_{E1}, is relatively stable; therefore, reference voltage V_{B2} variation is due mainly to the change in reverse current resulting from I_{B2} variation. Maximum change in I_{B2} results when Q3 turns off, causing I_{C2} to increase by 2.86 mA. Thus, for h_{FE2} = 57,

$$\Delta I_{B2} = 50 \text{ uA},$$

which is negligible compared to the nominal reverse current of 8.5 mA.

2. Temperature Variation. - By operating VR3 at its recommended reverse current, I_Z = 8.5 mA, the mean temperature coefficient is 0 and the maximum value is specified at ±0.008%/°C. In terms of breakdown voltage the variation is ±17 mV at 60°C and ±12 mV at 0°C.

The effect of reference level variation due to temperature on trip point stability is discussed further under a following section, "Trip Level Stability."

c. Circuit Drive Requirements. - The worst case drive requirements have been calculated for transistors Q5 and Q6, which operate as saturating switches with limited available current drive. On the other hand, detailed analysis of Q3 and Q4 is unnecessary since the available current drive through the resistor dividers is much greater than the typical base current flow.

1. Relay Driver (Q6). - The maximum base current required to activate relay K_1 is:

$$I_{B6} = \frac{\overline{I_{C6}}}{h_{FE6}} \qquad (7)$$

At 0°C, where coil resistance and h_{FE} are minimum, $\overline{I_{C6}}$ = 28.2 mA for the minimum relay activation voltage of 9V. Now for a minimum h_{FE} = 60, substituting into equation 7, maximum required I_{B6} = 0.47 mA. Similarly, the minimum base current which will produce turn-on is:

$$\underline{I_{B6}} = \frac{\underline{I_{C6}}}{h_{FE6}} \qquad (8)$$

At 60°C, where coil resistance and h_{FE} are maximum, $\underline{I_{C6}}$ = 18.7 mA. And, from equation 8, for h_{FE} = 375, $\underline{I_{B6}}$ = 50 uA. Thus, for reliable operation, the minimum available I_{B6} from either Q3 or Q5 must be sufficient to cause relay activation, while maximum leakage currents must be low enough so that Q6 remains OFF under worst case, normal primary voltage conditions.

Since both circuits (Q3 and Q5) driving Q6 are identical, the available drive current for the above conditions may be determined by considering only Q3.

OFF Stability. - When Q_3 is normally ON, Q_6 is OFF, and to insure that Q_6 remains OFF under worst case conditions, the following criteria must be fulfilled:

$$\overline{V_{C3}} \leq V_{\underline{BE6}} + V_{\underline{VR}} + 2V_{\underline{CR}} \tag{9}$$

At 60° C, where I_{B6} is minimum and V_{CE} is maximum, the left side of equation 9 is $\overline{V_{CB}} = 6.32V$. For solution of the right side of equation 9, the minimum Q_6 turn-on voltage at 60°C is given as $V_{BE6} = 0.58V$. To determine the diode voltage drops, their current flow must be known. Assuming I_{CR2} and $I_{CR3} = 0$, as V_{C3} increases the current through CR4, CR5 and VR4 will be:

$$I_D = I_{B6} + \frac{V_{BE6}}{R_{18}} \tag{10}$$

As calculated from equation 8, $I_{B6} = 50$ uA. Then, from equation 10, $I_D = 290$ uA. Using this value of current, from the diode transfer functions, $V_{VR} = 5.64V$ and $V_{CR} = 0.4V$. Or, $V_{BE6} + V_{VR} + 2V_{CR} = 7.02V$ and since $6.32 < 7.02$, the requirement of equation 9 is fulfilled.

Base Drive. - As determined from equation 7, the maximum Q_6 base current requirement is $\overline{I_{B6}} = 0.47$ mA. Thus, to ensure worst case relay activation, minimum available I_{B6} must meet the requirements,

$$I_{\underline{B6}} \geq 0.47 \text{ mA} \tag{11}$$

Neglecting leakage current at 0° C, and assuming Q_3 to be OFF, then the available drive current is:

$$I_{\underline{B6}} = \frac{\overline{V_{\underline{E1}}} - \overline{V_{CR3}} - \overline{V_{CR4}} - \overline{V_{VR3}} - \overline{V_{BE6}}}{R_9} - \frac{\overline{V_{\underline{BE6}}}}{R_{\underline{18}}} \tag{12}$$

For Vcc = 20V, $V_{\underline{E1}} = 10.77V$ at 0° C and, substituting worst case parameters into equation 12, $I_{\underline{B6}} = 0.49$ mA. Or, from equation 11, since $0.49 > 0.47$, the worst case base current requirement is fulfilled.

2. Q5 Drive. - Transistor Q_5 is driven by Q_4, with Q_5 normally ON and Q_4 normally OFF. The maximum base current required to turn-ON Q_5 is:

$$\overline{I_{B5}} = \frac{\overline{I_{C5}}}{h_{\underline{FE5}}} \tag{13}$$

Under worst case conditions, 0° C and Vcc = 39V, $\overline{I_{C5}}$ = 3.5 mA, and for h_{FE5} = 57, from equation 13, $\overline{I_{B5}}$ = 0.062 mA. Thus, for reliable turn-on, minimum available base current must meet the requirement:

$$\underline{I_{B5}} \geq 0.062 \text{ mA} \tag{14}$$

Neglecting leakage current, and letting V_E be equal for both the maximum and minimum conditions,

$$\underline{I_{B5}} = \frac{V_{E1} - \overline{V_{CR1}} - \overline{V_{BE5}} - V_{E2}}{\overline{R_{14}}} - \frac{\overline{V_{BE5}}}{\underline{R_{15}}} \tag{15}$$

and substituting worst case values into equation 15, I_{B5} = 0.99 mA, fulfilling the requirement of equation 14, 0.99 0.062.

With Q_4 ON, Q_5 OFF stability is given by:

$$\overline{V_{C4}} > \underline{V_{B5}} \tag{16}$$

where,

$$\overline{V_{C4}} = V_{E2} + \overline{V_{CE4}} \tag{17}$$

and, assuming diode leakage current is $\gg I_{CB05}$,

$$\overline{V_{B5}} = V_{E2} + \overline{I_D}\,\overline{R_{15}} \tag{18}$$

At 60° C, subtracting V_{E2}, equation 17 results in $\overline{V_{C4}}$ = 0.28V and equation 18 results in $\overline{V_{B5}}$ = 0.35V. Thus, since 0.28 < 0.35, the requirement of equation 16 is fulfilled, or CR1 is reverse biased.

d. Voltage Protection Trip Delay. - To avoid unnecessary recorder turn-off during brief low voltage transients, low voltage cut-out is delayed for a minimum of 35 ms. Any high voltage trip delay is due to inherent circuit and component delays.

1. Low Primary Voltage. - When Vcc drops below 22V, Q_3 cuts off and C_1 begins changing toward V_{E1}. The minimum charging time is given by:

$$\underline{t} = \underline{R_9 C_1} \text{ Ln} \frac{V_{E1} - \overline{V_{C3o}}}{V_{E1} - \underline{V_{C3f}}} \tag{19}$$

where,

$V_{C3o} = V_{C3}$ at $t = 0$

$V_{C3f} = V_{C3}$ when relay K1 reaches the minimum required turn-on voltage.

Using the results obtained for Relay Driver Q_6, $V_{C3o} = 6.32V$, $V_{C3f} = 7.02V$; letting $V_{E1} = 12.13V$, then, from equation 19, $\underline{t} = 41.5$ ms at 60° C. System specifications give the primary voltage transient maximum duration as 35 ms; thus, the calculated minimum delay is adequate.

The maximum delay occurs for maximum drive conditions, at 0° C with minimum h_{FE6}. Thus,

$$\overline{t} = \overline{R_9}\ \overline{C_1}\ \text{Ln}\frac{V_{E1} - V_{C3o}}{V_{E1} - V_{C3f}} \qquad (20)$$

For $V_{E1} = 10.8$, substituting worst case parameters into equation 20, $\overline{t} = 321$ ms.

2. High Primary Voltage. - When Vcc increases above the high voltage trip level, the transistor switching times, being less than a microsecond, are negligible. Thus the speed of high voltage protection is limited by the activation times of relays K1 and K_{VP}. Or, high voltage protection time delay is:

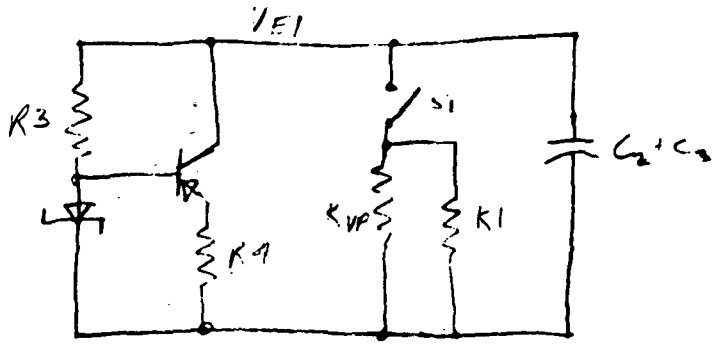
$$\overline{t} = \overline{t}_{K1} + \overline{t}_{KBV} \qquad (21)$$

From the manufacturer's specifications, $\overline{t}_{K1} = 2$ ms and $\overline{t}_{KBV} = 10$ ms, or substituting into equation 21, $\overline{t} = 12$ ms.

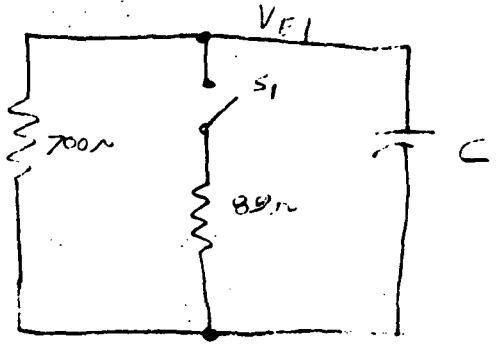
3. Power Turn-off. - When Vcc drops to 0, either by grounding or opening the input, Q_1 cuts off and, assuming C_2 and C_3 are charged to V_{E1}, the equivalent circuit shown in Figure 4-112 applies.

V_{E1} decay is given by:

$$t = RC\text{Ln}\frac{Eo}{Ef} \qquad (22)$$



a. Simplified Discharge Current Paths



b. Resistor Equivalent

Figure 4-112. Voltage Protection Circuit Equivalent Circuit for Vcc = 0

Since the capacitor discharge time will change when the trip relays activate (S_1 closes), the discharge time consists of two components, or,

$$t = t_1 + t_2 \qquad (23)$$

where,

t_1 = R9C1, decay time for relay activation

t_2 = 12 ms, the maximum relay activation time

Since the maximum low voltage delay time is 321 ms, then t_1 = 321 ms, and including the relay activation times t = 333 ms. Assuming E_{f1} = 9.6V and E_{F2} = 9.25V, required capacitance to ensure the voltage protection relay opens during primary power turn-off, is C = 4350 uF.

Since this value of capacitance is physically large and would add unnecessary weight, it has not been incorporated into the present design. Thus, the voltage protect relay will not be activated during complete power failure or normal turn-off.

e. Potentiometer Limits. - The worst case switching limits have been calculated for Q_3 and Q_4 to ensure that the trip point adjustment potentiometers, R_6 and R_{12}, exhibit the required setting range.

1. Low Voltage Trip (R6). - To ensure that Q_3 can be adjusted to cut off at the low voltage trip point, the requirement is:

$$\overline{V_{B3L}} \leq V_{\underline{B3T}} \tag{24}$$

where,

V_{B3T} = base voltage at the trip setting.

V_{B3L} = base voltage at the potentiometer low limit.

For Vcc = 22V, at 25° C, $\overline{V_{B3L}}$ = 5.65V and $V_{\underline{B3T}}$ = 5.7V, and since 5.65 < 5.70, the requirement of equation 24 is satisfied.

The potentiometer upper limit requirement is:

$$V_{\underline{B3H}} \geq \overline{V_{B3T}} \tag{25}$$

where,

V_{B3H} = base voltage at the potentiometer high limit.

For Vcc = 22V at 25° C, $V_{\underline{B3H}}$ = 7.5V and $\overline{V_{B3T}}$ = 6.3V, and since 7.50 > 6.30, the requirement of equation 25 is satisfied.

2. High Voltage Trip - (R12). - R12 is initially adjusted so that Q_4 turns on at the high voltage trip point, Vcc = 27. Thus the high limit requirement is:

$$\underline{V_{B4H}} \geq \overline{V_{B4}} \tag{27}$$

For Vcc = 27, at 25° C, $\underline{V_{B4H}} = 7.03V$, $\overline{V_{B4}} = 6.51V$, and since $7.03 > 6.51$, the requirement of equation 27 is satisfied.

The potentiometer lower limit requirement is:

$$\overline{V_{B4L}} \leq \underline{V_{B4}} \tag{28}$$

For Vcc = 27V, at 25° C, $\overline{V_{B4L}} = 4.82V$, $\underline{V_{B4}} = 5.89$, and since $4.82 < 5.89$, the requirement of equation 28 is satisfied.

f. Transistor Power Dissipation. -

1. Regulator Q_1

Power Dissipation. - Q_1 is a Class A amplifier which has a maximum power dissipation given by:

$$P_1 = \overline{V_{CE1}}\ \overline{I_{C1}} \tag{29}$$

The worst case power dissipation occurs at 60° C, with Vcc = 34.5V, and both relays K_1 and K_{VP} energized. From Figure 4-108, maximum collector current is:

$$\overline{I_{C1}} = \alpha_{N1} I_{E1} = \alpha_{N1} \left[\overline{I_{R3}} + \overline{I_{C2}} + \overline{I_{C3}} + \overline{I_{C4}} + \overline{I_{C6}} + \overline{I_{VP}}\right] \tag{30}$$

And for the above worst case condition, $\overline{I_{C1}} = 156$ mA.

Since,

$$\overline{V_{CE}} = \overline{Vcc} - V_{E1} - \overline{I_{C1}}\underline{R2} \tag{31}$$

Then for continuous operation, Vcc = 34.5, $V_{E1} = 12.67$ and $\overline{V_{CE}} = 18V$. Thus, substituting into equation 29, $\overline{P_1} = 2.8W$.

Heat Sink Requirements. - Transistor junction temperature for free air operation may be determined from,

$$T_J = T_A + \theta_{J-A} P \tag{32}$$

where,

T_A = ambient temperature (° C)

θ_{J-A} = thermal resistance from junction to free air (° C/W)

P = transistor power dissipation (watts)

For $T_A = 60°$ C, and $\theta_{J-A} = 34.875°$ C/W, the maximum junction temperature of Q_1 is $T_J = 158°$ C. Since the ERTS system maximum allowable transistor junction temperature is 110° C, a heat sink will be required by Q_1 to reduce its junction temperature.

If the heat sink is assumed to be isolated, preventing conduction, then heat transfer from the heat sink is entirely due to radiation. When the area of the heat sink is made smaller than the area of the surrounding surface, the radiant heat transfer in BTU/hr. is given by,

$$Q = A_1 e_1 \sigma (T_1^4 - T_2^4) \tag{33}$$

where,

A_1 = heat sink area (ft.^{2})

e_1 = emissivity (approximately 0.8 for unpolished copper)

σ = Stefan-Baltzman constant (0.173×10^{-8} BTU/hr.-ft.^{2}-R^4)

T_1 = temperature of heat sink (° RanKine)

T_2 = temperature of surrounding surface (° RanKine)

Since the heat sink is copper, which has a high conductivity, it may be assumed that the temperature of the heat sink is uniform, and that the required area may be calculated for a given heat transfer. Solving equation 33 for A_1,

$$A_1 = \frac{Q}{e_1 (T_1^4 - T_2^4)} \quad (34)$$

Then converting watts to BTU/hr., Q = 9.6 BTU/hr. And for T_1 = 690° R, T_2 = 600° R, solving equation 34, required heat sink area is $A_1 = 10 \text{ in}^2$.

2. Q2, Q3, Q4, Q5 and Q6 Dissipation. -

Q2 Dissipation. - For Q_2, which operates as a Class A amplifier, the dissipation is:

$$\overline{P_2} = \overline{V_{CE2}}\,\overline{I_{C2}} \quad (35)$$

Maximum I_{C2} results when Vcc is low and Q_3 is OFF. Or,

$$\overline{I_{C2}} = \overline{I_{R4}} - I_{C5} \quad (36)$$

Maximum V_{CE2} is given by:

$$\overline{V_{CE2}} = \overline{V_{E1}} - V_{E2} \quad (37)$$

At 60° C, for Vcc = 20V, substituting worst case values into the above equations, $\overline{I_{C2}}$ = 7.35 mA, $\overline{V_{CE2}}$ = 6.09V and $\overline{P_2}$ = 44.7 mW.

Q3 Dissipation. - Assuming Q_3 ON, the power dissipation is:

$$\overline{P_3} = \overline{V_{CE3}}\,\overline{I_{C3}} \quad (38)$$

Then for $\overline{I_{C3}}$ = 3.43 mA and $\overline{V_{CE3}}$ = 0.28V, $\overline{P_3}$ = 0.96 mW.

Q4 Dissipation. - Assuming Q_4 ON, the power dissipation is:

$$\overline{P_4} = \overline{V_{CE4}}\,\overline{I_{C4}} \quad (39)$$

Then for $\overline{I_{C4}}$ = 1.66 mA and $\overline{V_{CE4}}$ = 0.28V, $\overline{P_4}$ = 0.46 mW.

Q5 Dissipation. - Assuming Q_5 ON, the power dissipation is:

$$\overline{P_5} = \overline{V_{CE5}}\,\overline{I_{C5}} \quad (40)$$

Then for $\overline{I_{C5}}$ = 3.43 mA and $\overline{V_{CE5}}$ = 0.28V, $\overline{P_5}$ = 0.46 mW.

Q6 Dissipation. - Assuming Q_6 ON, the power dissipation is:

$$\overline{P_6} = \overline{V_{CE6}}\,\overline{I_{C6}} \tag{41}$$

Then, for $\overline{I_{C6}}$ = 31.6 mA and $\overline{V_{CE6}}$ = 0.43V, $\overline{P_6}$ = 13.6 mW.

g. Trip Level Stability. - The trip level variation is directly proportional to the change of Q_3 and Q_4 base reference voltage due to component temperature coefficients and aging.

1. Temperature Effects. - The reference level temperature stability depends on the temperature coefficients of both diode VR3 and the resistor divider sensing networks.

Low Voltage Trip. - Assuming potentiometer R_6 centered, Vcc constant, and the V_{BE} temperature coefficients of Q_2 and Q_3 approximately equal (transistors are of the same type with similar loading), V_{B3} drift due to resistor change as a function of temperature may be determined. Q_3 base voltage is given by:

$$V_{B3} = \frac{(R_7 + \frac{R_6}{2})\,Vcc}{R_5 + R_6 + R_7} \tag{42}$$

At 25° C, the nominal base voltage level V_{B3} = 0.2510 Vcc, and at 60° C V_{B3} = 0.2516 Vcc. Thus, the maximum change in V_{B3} due to resistor variation is ±0.0006 Vcc. In terms of Vcc trip point variations, since V_{B3} = 0.251 Vcc, the trip point drift from the 25° C setting is Vcc ±0.24%. The total drift due to temperature also includes the reference level variation of ±17 mV as determined above (Trip Reference Level Stability). In terms of Vcc, the drift is ±0.28%. Thus, the total worst case low voltage trip point drift due to temperature is Vcc ±0.52%.

High Voltage Trip. - Since Q_4 operates at a lower collector current than Q_2, the trip point drift due to the V_{BE} temperature coefficient must be included along with the drift due to the resistor divider and reference level change. The effects of V_{BE} drift on Vcc is:

$$\Delta V_{cc} = K\,\Delta V_{BE} \tag{43}$$

where nominal K = 4.

From the transistor specifications, $\Delta V_{BE} = -0.1$ mV/° C. Or, for a temperature change from 25° C to 60° C, $\Delta V_{BE} = -3.5$ mV; and, from equation 43, $\Delta Vcc = +14$ mV = +0.058%.

Now, using the results for low voltage trip, which are applicable due to the similarity of the resistor divider ratios, total high voltage trip point drift is Vcc +0.58, -0.46%.

2. Aging Drift. - The effect of aging on the zener reference breakdown voltage is negligible, and, assuming V_{BE} drift due to aging is identical for the transistors, the trip point drift as a result of component aging will be entirely due to resistor variation. As noted above, the resistor divider ratios are similar for both the low trip point and high trip point, resulting in approximately identical drift coefficients.

Analyzing the low voltage case, from equation 43,

$$\Delta V_{cc} = 4 \Delta V_{B3} \tag{44}$$

Substituting worst case values into equation 42, $V_{B3} = 0.255$ Vcc, and $\Delta V_{B3} = 0.004$ Vcc. Translated to the primary voltage level, aging results in a trip point variation of Vcc $\pm$1.6%.

4.4.6.4 Conclusions and Recommendations. - With the recommended component values incorporated into the Voltage Protection circuit, worst case analysis has shown that all operating requirements have been satisfied over the temperature range of 0°C - 60°C for a life-time of 10,000 hours. However, for reliable high temperature operation, a heat sink must be provided for Q_1. As shown in the previous analysis, if heat transfer is strictly due to radiation, a minimum surface area of 10 in^2 is required. It should be noted that the specified area may be reduced considerably if heat transfer due to conduction is also utilized.

For the T018 size transistors (Q2 thru Q5), the maximum allowable dissipation in a zero gravity environment is 27 mW for an unpainted surface and approximately 45 mW for a painted surface. Therefore, Q2 should be painted in order to conform with the maximum allowable junction temperature requirements.

As a matter of record, the analysis has shown that in the event of instantaneous primary power failure (Vcc = 0), the voltage protection relay will remain in its original state.

A summary of the voltage protect response to continuous and transient voltage changes is shown in Tables 4-32 and 4-33, respectively.

TABLE 4-32. VOLTAGE PROTECT RESPONSE FOR A DISCRETE LEVEL CHANGE

Voltage Level	Circuit Response
27-34.5	Drop-out after a maximum of 12 ms
22-27	No drop-out
13.8-22	Drop-out after a maximum of 333 ms
0-13.8	No drop-out for a fall time of less than 40 to 333 ms, depending on component tolerances.

TABLE 4-33. VOLTAGE PROTECT RESPONSE FOR TRANSIENT LEVELS

Transient Peak	Circuit Response		
	$t<12$	$12 \leq t \leq 40$	$40 \leq t \leq 333$
27-39	Drop-out depends on relay activation times	Drop-out	Drop-out
22-27	No drop-out	No drop-out	No drop-out
12.6-22	No drop-out	No drop-out	Drop-out depends on component tolerances
0-12.6	No drop-out	No drop-out	No drop-out

Note: t = transient duration in ms.

4.4.7 Motor Drive Circuits Worst Case Analysis. - The motor driver circuits reviewed are used for three separate motors: Capstan, Iω and headwheel. An identical drive circuit is used for ϕ_1 and ϕ_2 of a given motor, and the drive circuits for the three motors use identical configurations, differing only in the frequency of operation and transformer turns ratio.

The analysis results include principally worst case component stress levels and worst case drive levels. This assures that all components are operated within allowed stress operating factors and that transistors have sufficient drive levels to support their respective loads. Specifications for critical semiconductor components were reviewed to assure adequate controls over important design parameters.

In the process of initial calculations, certain component changes were found necessary or desirable. This report incorporates the latest changes, which are described in Appendix D.

4.4.7.1 Design Assumptions. - The basic review calculations were made for a temperature range of 0° C to +60° C, and for power supply variations of ±7% about nominal. Important design assumptions are tabulated in Appendices D and H. Certain of the more critical parameters are controlled by RCA specification control drawings, others are parameters used as guides for design calculations, usually obtained from device characterizations from manufacturer's data sheets. The appendix contains plots of certain important semiconductor characteristics.

4.4.7.2 Component Stress Analysis

a. Low Level Signal Drive Circuits. - The low level drive circuits have the same basic configuration with minor differences for the Headwheel, Capstan and Iω circuits. The basic configuration is shown on Figure 4-113.

   The motor reversing circuit, Z3, is used only by the capstan circuit. For the Headwheel and Iω circuits, transistor Q9 is shared by two switched return circuits, designated Q10 and Q10[1]. The results of the stress analysis for this group of circuits are shown in Table 4-34.

b. High Level Signal Drive Circuit. - The high level drive circuits (Figure 4-114) are comprised of the transformer and motor bridges transistors with associated components. Although the configuration is identical for the three motor types, the operating currents and resulting dissipations are different, and are shown separately in Table 4-35.

4.4.7.3 Graphical Calculation of Power Transistor Drive. - Since the method of base drive to the power transistors approximates a fixed base voltage type drive, the non-linear V_{BE} versus I_B characteristic of the transistor necessitates the use of graphical analysis methods to determine drive values. The equivalent circuit is shown in Figure 4-115.

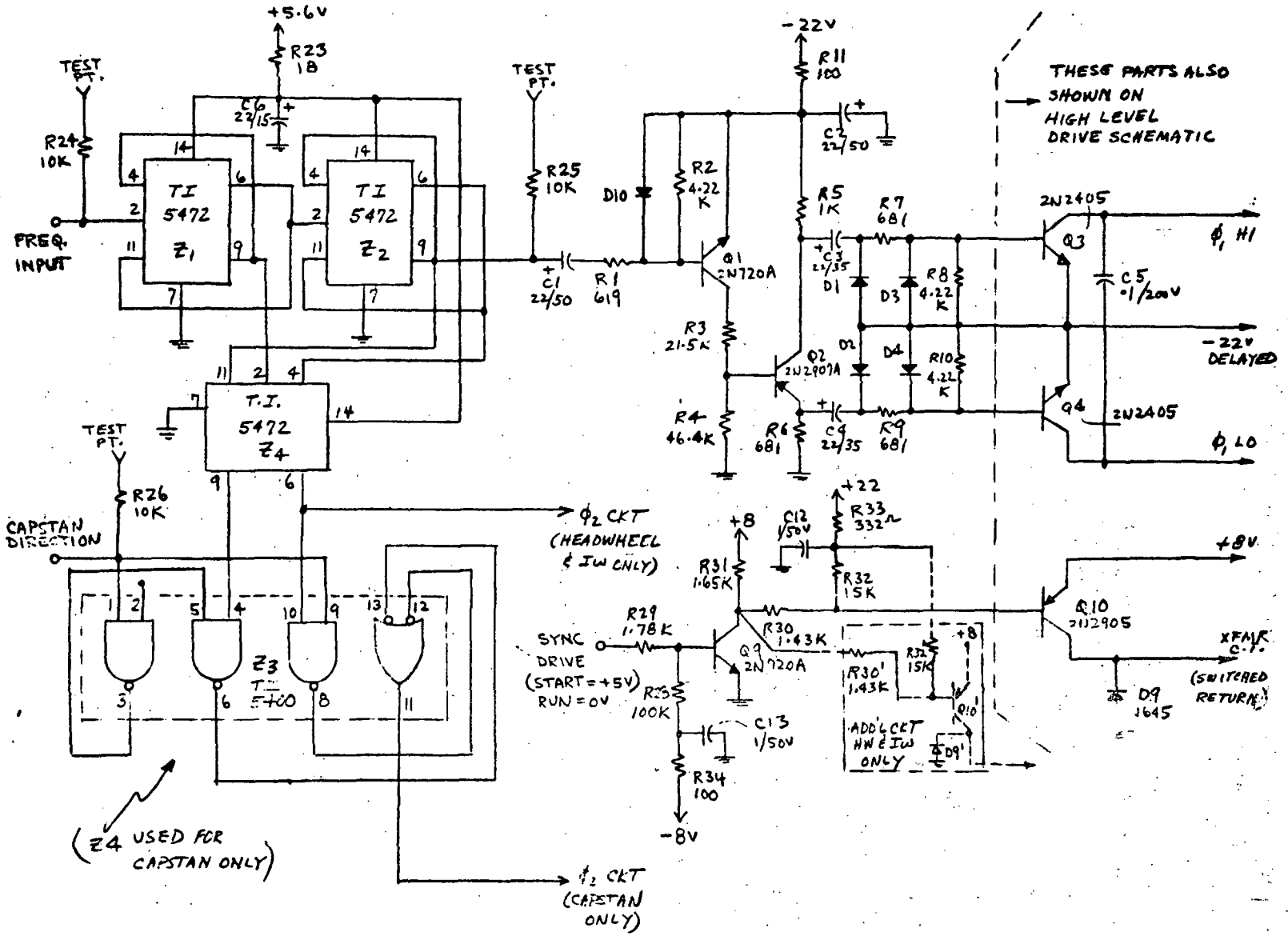


Figure 4-113. Low Level Drive Circuits, Schematic Diagram

TABLE 4-34. LOW LEVEL SIGNAL DRIVE CIRCUITS STRESS ANALYSIS

Symbol	Part No.	Nominal Value	Tolerance (%)		Rated Stress	Actual Stress (Nominal)	% of Rating	Max. Allowed % Rating	Remarks
			Initial	Design					
R1	RNR55C6190	619 ohms	1	2	100 mW	1.3 mW	1.3	50	
R2	RNR55C4221	4.22 K	1	2	100 mW	0.12 mW	0.12	50	
R3	RNR55C2152	21.5 K	1	2	100 mW	4.48 mW	4.48	50	
R4	RNR55C4642	46.4 K	1	2	100 mW	2.96 mW	2.96	50	
R5	RNR65C1001	1 K	1	2	250 mW	81.2 mW	32.5	50	
R6	RNR65C6810	681 ohms	1	2	250 mW	121 mW	48.4	50	
R7	RNR65C6810	681 ohms	1	2	250 mW	11.7 mW	4.68	50	
R8	RNR55C4221	4.22 K	1	2	100 mW	0.58 mW	0.58	50	
R9	RNR55C6810	681 ohms	1	2	100 mW	19.4 mW	19.4	50	
R10	RNR55C4221	4.22 K	1	2	100 mW	0.58 mW	0.58	50	
R11	RNR65C1000	100 ohms	1	2	250 mW	8.97 mW	3.59	50	
R23	RNR55C0180	18 ohms	1	2	100 mW	18.45 mW	18.45	50	
R24 to R26	RLR07C103J	10 K	5	10	250 mW	≈ 0	0	50	Test point a solution res.
R28	RNR55C1003	100 K	1	2	100 mW	0.76 mW	0.76	50	START Mode
R29	RNR55C1781	1.78 K	1	2	100 mW	3.8 mW	3.8	50	START Mode
R30	RNR55C1431	1.43 K	1	2	100 mW	36.3 mW	36.3	50	START Mode
R31	RNR60C1651	1.65 K	1	2	125 mW	36.9 mW	29.6	50	START Mode
R32	RNR55C1502	15 K	1	2	100 mW	14.4 mW	14.4	50	START Mode
R33	RNR55C3320	332 ohms	1	2	100 mW	0.32 mW	0.32	50	
R34	RNR55C1000	100 ohms	1	2	100 mW	0.34 μW	≈ 0	50	
C1	CSR13G226K	22 uF	10		50 V	22.25 V	44.4	60	3 ohms/V OK
C2	CSR13G226K	22 uF	10		50 V	22 V	44	60	3 ohms/V OK
C3	CSR13F226K	22 uF	10		35 V	6.63 V	19	60	3 ohms/V OK
C4	CSR13F226K	22 uF	10		35 V	9.6 V	27.4	60	3 ohms/V OK
C5	CKR06BX104KP	0.1 uF	10		200 V	60 V	30	60	
C6	CSR13D226K	22 uF	10		15 V	5.02 V	33.5	60	3 ohms/V OK
C12	8150546	1 uF	10		50 V	22 V	44	60	
C13	8150546	1 uF	10		50 V	8 V	16	60	
D1	1N645	—	—	—	V_R = 225 V	4.7 V	2.09	80	
		—	—	—	T_j = 200°C	60.8°C	30.4	55	T_j = 110°C max
D2	1N645	—	—	—	V_R = 225 V	5.15 V	2.29	80	
					T_j = 200°C	61.1°C	30.5	55	T_j = 110°C max
D3	1N645	—	—	—	V_R = 225 V	0.9 V	0.4	80	
					T_j = 200°C	60°C	30	55	D3 hardly conducts at all

TABLE 4-34. LOW LEVEL SIGNAL DRIVE CIRCUITS STRESS ANALYSIS (Continued)

Symbol	Part No.	Nominal Value	Tolerance (%)		Rated Stress	Actual Stress (Nominal)	% of Rating	Max. Allowed % Rating	Remarks
			Initial	Design					
D4	1N645	—	—	—	V_R = 225 V	0.9 V	0.4	80	D4 hardly conducts at all
					T_j = 200°C	60°C	30	55	
D9	1N645	—	—	—	V_R = 225 V	8 V	3.55	80	START Mode
					T_j = 200°C	89°C	44.5	55	RUN Mode, P_D = 92.8 mW, T_A = 60°C
Q1	2N720A	—	—	—	V_{CEO} = 80 V	22 V	27.5	80	
		—	—	—	V_{CBO} = 120 V	23.2 V	19.3	80	
		—	—	—	V_{EBO} = 7 V	1.19 V	17	80	
		—	—	—	T_j = 200°C	60.04°C	30	55	T_j = 110°C max.
Q2	2N2907A	—	—	—	V_{CEO} = 40 V	22 V	55	80	Slightly high.
		—	—	—	V_{CBO} = 60 V	22 V	36.7	80	
		—	—	—	V_{EBO} = 5 V	4.45 V	89	80	Slightly high.
		—	—	—	T_j = 200°C	78.5°C	39.3	55	T_j = 110°C max
Q3, Q4	2N2405	—	—	—	V_{CEO} = 90 V	63.5 V	70.5	80	
		—	—	—	V_{CBO} = 120 V	64.2 V	53.5	80	
		—	—	—	V_{EBO} = 7 V	0.7 V	10	80	
		—	—	—	T_j = 200°C	P_C = 39.2 mW, T_j = 66.9°C	33.4	55	START Mode, T_j = 110°C max
Q9	2N720A	—	—	—	V_{CEO} = 80 V	8 V	10	80	
		—	—	—	V_{CBO} = 120 V	9.03 V	7.52	80	
		—	—	—	V_{EBO} = 7 V	1.03 V	14.7	80	
		—	—	—	T_j = 200°C	60.6°C	30.3	55	T_j = 110°C max.
Q10	2N2905	—	—	—	V_{CEO} = 40 V	8.9 V	22.2	80	
		—	—	—	V_{CBO} = 60 V	11.53 V	19.2	80	
		—	—	—	V_{EBO} = 5 V	2.63 V	52.6	80	
		—	—	—	T_j = 200°C	76.6°C	38.4	55	T_j = 110°C max.
Z1, Z2, Z4	5472 (T.I.)	—	—	—	V_{CC} = 7 V	5 V	71.5	80	
		—	—	—	T_j = 150°C	*	*	73.3	T_j = 110°C max.
Z3	5400 (T.I.)	—	—	—	V_{CC} = 7 V	5 V	71.5	80	
		—	—	—	T_j = 150°C	*	*	73.3	T_j = 110°C max.

*Thermal Data Not Available

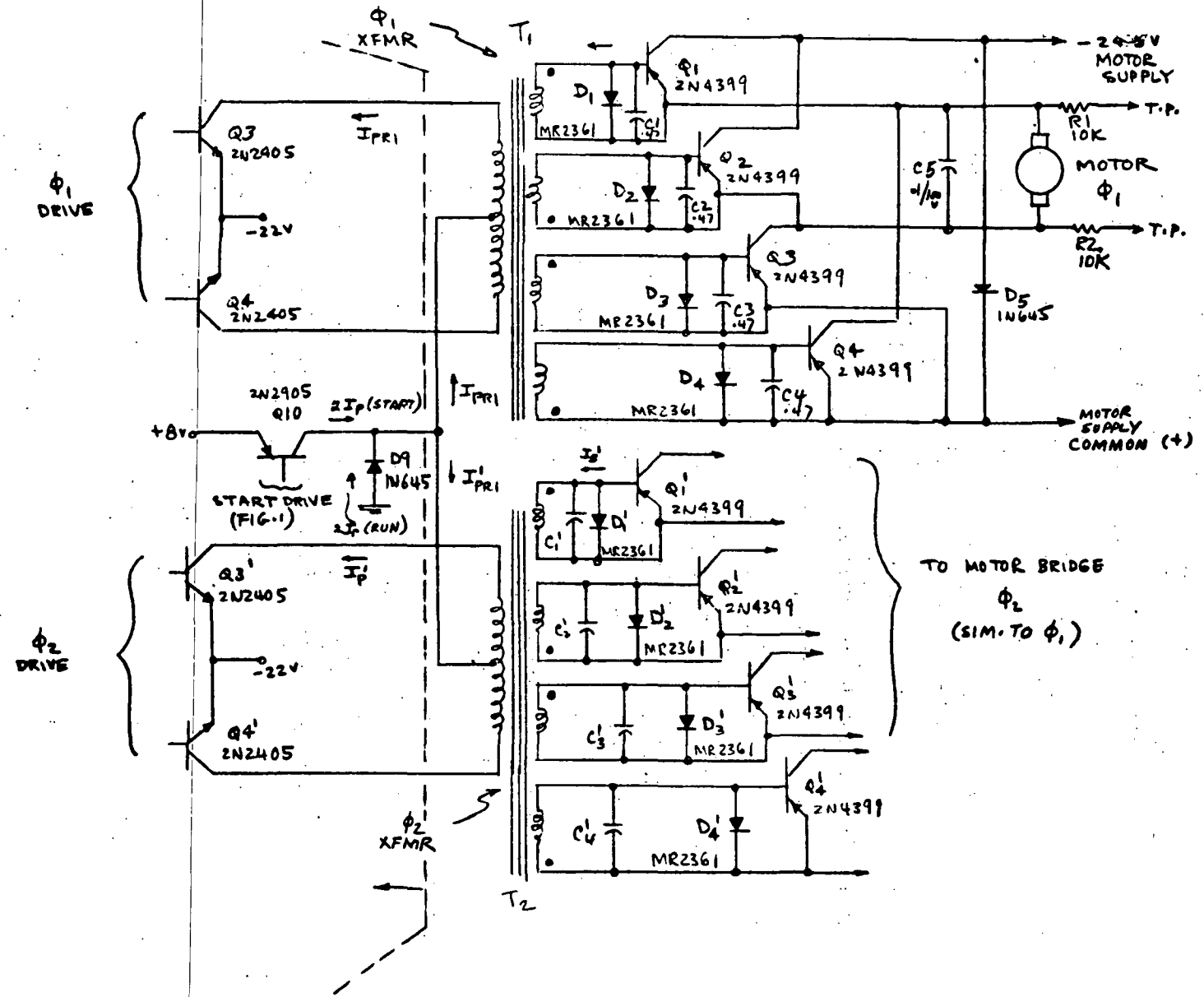


Figure 4-114. High Level Drive Circuits, Schematic Diagram

TABLE 4-35. HIGH LEVEL SIGNAL DRIVE CIRCUITS STRESS ANALYSIS

Symbol	Part No.	Nominal Value	Tolerance		Rated Stress	Actual Stress (Nominal)	% of Rating	Max. Allowed % Rating	Remarks
			Initial	Design					
D1, D2, D3, D4	MR-2361	—	—	—	1000 mW	≈ 0	0	—	RUN Mode only
D5	1N645	—	—	—	V_R = 225 V	24.5 V	10.9	80	Power stress negligible
Q1, Q2,	2N4399	—	—	—	V_{CEO} = 60 V	49 V	81.6	80	Slightly high.
Q3, Q4	Selected	—	—	—	V_{CBO} = 60 V	50.4	84	80	Slightly high.
					V_{EBO} = 5 V	1.4	28	80	—
T_1, T_2	8150568 (Special AFMR)	—	—	—	N/A	N/A	N/A	N/A	—
C1, C2, C3, C4	CKR060W474KP	0.47 uF	10 %	—	50 V	1.4 V	2.8	60	—
C5	CKR060W104KP	0.1 uF	10%	—	100 V	24.5	24.5	60	—
D1, D2,	MR-2361	—	—	—	1000 mW	Average 40.5 mW	0.05	—	START Mode (θ_M = 100°C/W)
D3, D4					T_j = 200°C	64°C	32	55	(T_j = 110°C max.)
Q1, Q2,	2N4399	—	—	—	T_j = 200°C				START Mode
Q3, Q4	(Selected)				T_j = 200°C				RUN Mode
D1, D2,	MR-2361	—	—	—	1000 mW	Average 37 mW	3.7	—	START Mode only θ_{jA} = 100°C/W
D3, D4					T_j = 200°C	63.7°C	31.8%	55	T_j = 110°C max allowed
Q1, Q2	2N4399	—	—	—	T_j = 200°C			55	START Mode
Q3, Q4	(Selected)				T_j = 200°C			55	RUN Mode
D1, D2,	MR-2361	—	—	—	1000 mW	Average 37 mW	3.7	—	START Mode only θ_{jA} = 100°C/W
D3, D4					T_j = 200°C	63.7°C	31.8	55	T_j = 110°C max allowed.
Q1, Q2,	2N14399	—	—	—	T_j = 200°C			55	START Mode
Q3, Q4	(Selected)				T_j = 200°C			55	RUN Mode

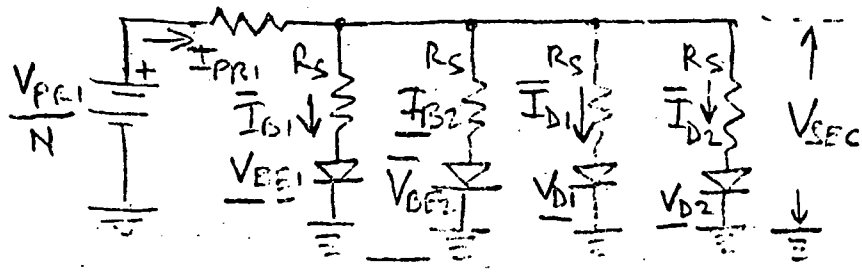


Figure 4-115. Equivalent Power Output Circuit

Where:

V_{PR1}	=	Voltage across 1/2 the transformer primary.
N	=	Transformer turns ratio, 1/2 primary to each secondary.
R_P	=	Transformer primary resistance (1/2 primary).
R_S	=	Transformer secondary resistance (each secondary).
$\underline{V}_{BE1}$	=	Minimum V-1 characteristic of power transistor V_{BE}.
$\overline{V}_{BE2}$	=	Maximum V-1 characteristic of power transistor V_{BE}.
$\underline{V}_{D1}$, $\underline{V}_{D2}$	=	Minimum V-1 characteristic of V_{BE} protective diode.
$\overline{I}_{D1}$, $\overline{I}_{D2}$	=	Maximum resulting current to V_{BE} protective diode.
$\overline{I}_{B1}$	=	Maximum resulting base current for given V_{PR1} applied.
$\underline{I}_{B2}$	=	Minimum resulting base current for given V_{PR1} applied.
$\overline{I}_{PR1}$	=	Resulting total reflected primary current.

The principal end items of interest are: (1) $\underline{I}_{B2}$ (minimum base drive); (2) $\overline{I}_{D1}$, $\overline{I}_{D2}$ (maximum current in protective diode); and (3) $\overline{I}_{PR1}$ (maximum reflected primary current to driver transistor) $\underline{I}_{B2}$ is of interest at low temperatures to assure adequate h_{FE} to support required motor currents. $\overline{I}_{D1}$, $\overline{I}_{D2}$ are of interest at high temperatures to assure that the protective diodes are not overstressed. $\overline{I}_{PR1}$ is of interest since it determines the load on the driver transistors. These parameters have been calculated for both START and RUN modes, over the operating temperature range from 0° C to +60° C, considering variations in the V_{PR1} input voltage. Detailed calculations and graphical worksheets are contained in the appendix; important results are tabulated in Table 4-36.

The general procedure used for graphical calculations is outlined as follows (reference Figures are contained in the appendix):

(1) Define typical V_{BE} vs I_B curve from manufacturer's data, and define limit V_{BE} curves from RCA-generated specification limits (see Figure D-1).

TABLE 4-36. RESULTS OF DRIVE CALCULATIONS

Motor Type	Mode		Power Transistor Drive			Protective Diode Stress		Req'd. Reflected Primary Current (min.)	Driver Transistor Required h_{FE} (min)
			I_B (min)	I_C (max)	Req'd. h_{FE} (min)	I_D (max) Peak*	Max. Power Stress (Average)		
Headwheel	Start	0° C	0.510 A	10.0 A	19.6	6.2 mA	4.22 mW	74.4 mA	28.0
		60° C	0.49 A	10.0 A	20.4	60 mA	40.5 mW	71.8 mA	27.0
	Run	0° C	76 mA	1000 mA	13.15	-	-	21.9 mA	8.24
		60° C	150 mA	1000 mA	6.67	-	-	25.8 mA	9.7
Capstan	Start	0° C	0.390 A	8.0 A	20.5	8.0 mA	5.55 mW	53.2 mA	20.0
		60° C	0.390 A	8.0 A	20.5	54 mA	37.0 mW	50.0 mA	18.8
	Run	0° C	88 mA	1130 mA	12.85	-	-	18.5 mA	6.95
		60° C	145 mA	1130 mA	7.8	-	-	22.0 mA	8.26
I_ω	Start	0° C	0.39 A	5.0 A	12.8	8.0 mA	5.55 mW	53.2 mA	20.0
		60° C	0.39 A	5.0 A	12.8	54 mA	37.0 mW	50.0 mA	18.8
	Run	0° C	88 mA	600 mA	6.82	-	-	18.5 mA	6.95
		60° C	145 mA	600 mA	4.14	-	-	22.0 mA	8.26

*Duty Cycle = 50%

(2) Define TC curve of V_{BE} from manufacturer's data. Construct limit V_{BE} curves at other temperatures (see Figure D-2).

(3) Construct ($V_{BE} + V_{RS}$) curves by adding V_{RS} drop on secondary resistance at corresponding current and temperature (see Figure D-3).

(4) Define limit curves for V_D at 25° C (see Figure D-4).

(5) Define TC curve of V_D from manufacturer's data (see Figure D-5).

(6) Calculate V_D at other temperatures, and corresponding secondary resistance drop V_{RS}, to get ($V_D + V_{RS}$) curves (see Figure D-6).

(7) Graphically construct total Z_{sec} curves by adding min I_B curve, max I_B curve, and max I_D curve at a corresponding secondary voltage and temperature (see Figure D-7).

(8) Graphically construct operating load lines by calculating limit V_{sec} open circuit, and using reflected primary resistance, R_{PR1}/N^2 (see Figure D-8).

(9) Operating points for a given mode of operation are determined by intersection of load lines with Z_{sec} curve at a corresponding temperature. Read resulting secondary load voltage, $V_{sec} = V_{BE} + V_{RS}$.

(10) From individual ($V_{BE} + V_{RS}$) or ($V_D + V_{RS}$) curves, read operating current in each device.

4.4.7.4 Conclusions. - All component parts were found to be operated within allowable ratings, as summarized in Tables 4-34 and 4-35 of the report. The minimum available base drive levels for transistors are found to be consistent with present h_{FE} specifications:

a. Drive (Selected 2N2405) h_{FE}. -

Minimum required (calculated):	28 at	I_C	= 75 mA
		V_{CE}	= 0.4V
		T_A	= 0° C
Minimum available (spec.):	40 at	I_C	= 100 mA
		V_{CE}	= 0.4V
		T_A	= 0° C

b. Power Transistor (selected 2N4399) h_{FE}. -

Minimum required (calculated):	19.6 at	I_C	= 10A
		V_{CE}	= 0.75V
		T_A	= 0° C
Minimum available (spec.):	15 at	I_C	= 15A
		V_{CE}	= 0.75V
		T_A	= 0° C

This is satisfactory because h_{FE} increases as collector current decreases. From an estimated curve (Figure D-2) an h_{FE} of 20.5 is available at I_C = 10A, which satisfies requirements.

In the course of preparing this report, certain changes in the driver transformer turns ratios were found necessary for correct drive levels. The changes have been incorporated, and are as follows:

1. Increase number of secondary turns for Headwheel transformer from 31 to 35. This decreases turns ratio from 25.85 to 22.85.

2. Decrease number of secondary turns for Capstan and I_ω transformer from 50 to 44. This increases turns ratio from 19 to 20.5.

It was also found necessary to characterize the V_{BE} drops for the power transistors at three current levels in order to guarantee proper base drive conditions. These are:

1.	V_{BE} = 1100 mV ±200 mV at	I_C	= 15A
		I_B	= 1A
2.	V_{BE} = 675 mV ±100 mV at	I_C	= 600 mA
		I_B	= 60 mA
3.	V_{BE} = 575 mV ± 100 mV at	I_C	= 80 mA
		I_B	= 8 mA

These V_{BE} specifications have been incorporated in the power transistor specifications.

4.4.8 Motor Auxiliary and Filter Assembly Worst Case Analysis. - The Motor Auxiliary and Filer Assembly networks have been analyzed to ensure reliable operation for the ERTS System motor drive and input current requirements, using the criteria of Appendix H.

4.4.8.1 Summary. - The various circuits which make up the Motor Auxiliary board have been analyzed with respect to critical component stress, and temperature and aging drift.

To limit the magnitude of the individual motor bridge capacitor ac currents, several smaller capacitors have been placed in parallel. In addition, low duty cycle ac current overload tests have been conducted to ensure that there is no degradation in the capacitor characteristics during the high starting currents.

The dc current monitoring telemetry transformers have been shown to exhibit considerable drift due to temperature variation. Laboratory measurements of sample transformers show an output level drift of +8.9 to -6.8% for the recorder current TM, +7.2 to -8.5% for the Headwheel motor current TM, and +13 to -6.2% for the capstan motor current TM.

Motor starting current surges are limited by two motor starting ramp generators. The Headwheel and Iω ramp rise time is 41ms and the fall time is 1 sec; minimum quiesent output voltage is -19V. The capstan ramp has a rise time of 19ms and a fall time of 530ms; minimum quiesent output voltage is -18.8V.

A review of the record current step loading transient measurements is given in Table 4-37. From this data, it is clear that the DC/DC converter turn-on surge is not within specifications.

The worst case trickle change power requirement is approximately 50mW. The 5.6V transient suppression circuit maximum output is 7.4V, but is further reduced by the various logic circuit decoupling networks to about 6.8V max at the actual IC's, which is within their maximum allowable Vcc. Worst case suppression diode leakage dissipation is 120mW, and typical dissipation is 20mW.

4.4.8.2 Worst Case Analysis. - The Motor Axuiliary and Filter Assembly networks were analyzed to ensure reliable operation under worst case current requirements. Particular attention was given to component stress limitiations.

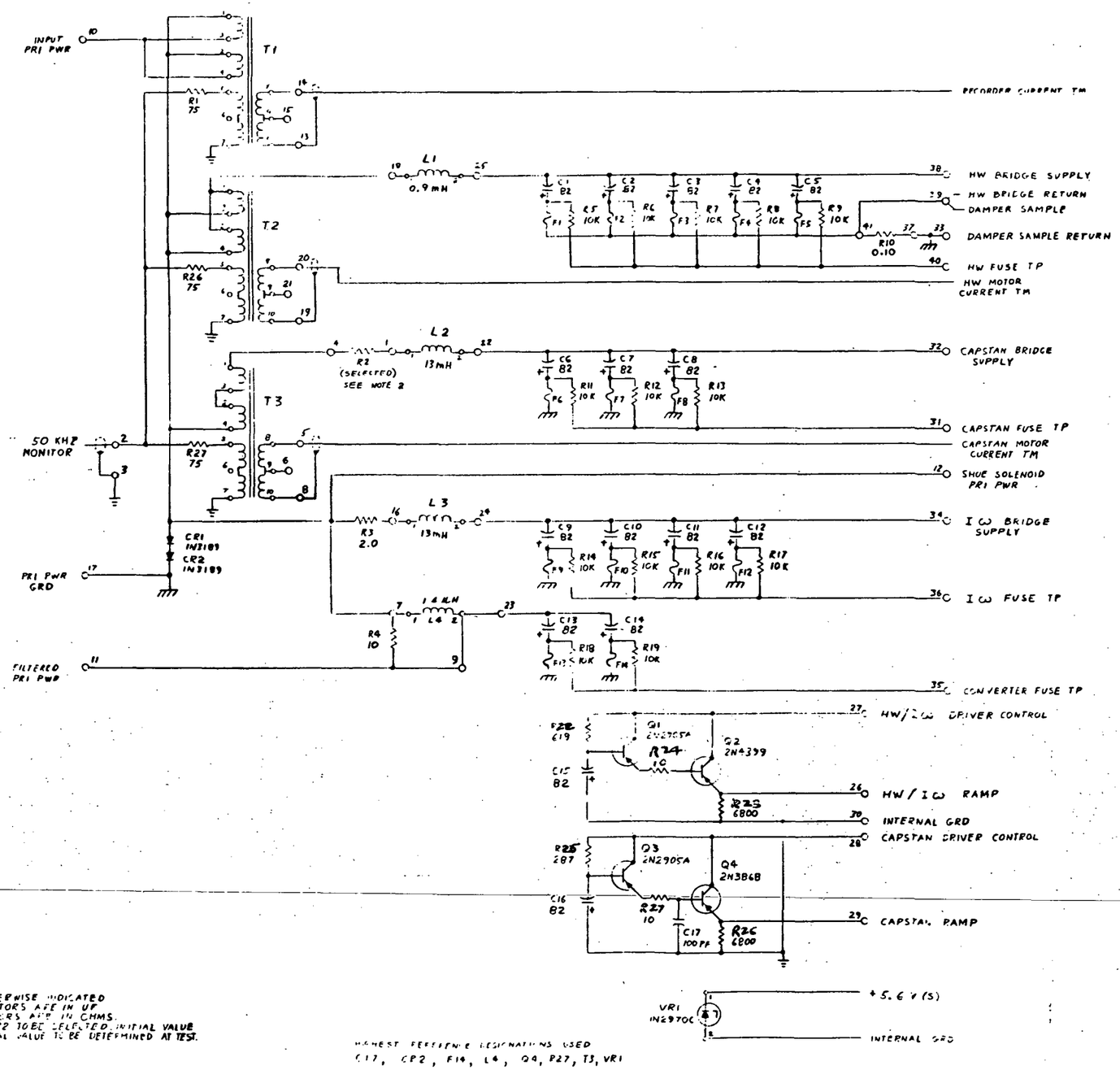
a. Motor Bridge Supplies. - An LC circuit has been provided for each of the recorder motors (Headwheel, Iω and Capstan) to isolate the motor bridges from the primary supply.

1. Headwheel Bridge Supply. - As shown in Figure 4-116, the Headwheel Bridge Supply consists of L1, and C1 through C5. Since the starting current is very high, capacitor ac current limitiations dictated the use of several smaller capacitors in parallel as opposed to a single large

TABLE 4-37. PRIMARY POWER SUPPLY CURRENT TRANSIENTS

Subsystem Operation	Maximum Increasing Step (A)	Risetime (ms)		Maximum Decreasing Step (A)	Falltime (ms)	
		Minimum Allowable	Measured		Minimum Allowable	Measured
Headwheel and I_ω						
Start-up	9	10	20	5	5	3 (seconds)
Start-run	-	-	-	6	5-6	2-3
DC/DC Converter	9.5	12	(1)	8.5	8	2
Shoe Solenoid	4	3.5	5-6	4	3.5	2-3
Capstan						
Standby	1	None	≈10	1	None	
MSS Standby To Fast Fwd	3	2	5	1	None	2

Note: Current steps do not include changes of less than 1A.



NOTES:
1. UNLESS OTHERWISE INDICATED
ALL CAPACITORS ARE IN UF
ALL RESISTORS ARE IN OHMS.
2. VALUE OF R2 TO BE SELECTED. INITIAL VALUE 1 OHM, FINAL VALUE TO BE DETERMINED AT TEST.

HIGHEST REFERENCE DESIGNATIONS USED
C17, CR2, F14, L4, Q4, R27, T3, VR1

Figure 4-116. Motor Auxiliary Circuits

capacitor. The Headwheel peak dc starting current is about 8A and decreases linearly to approximately 3A in the three to four seconds required for the motor to come up to speed. When the motor winding is switched from start to run, the required dc current is further decreased to about 0.5A.

The total Headwheel Motor ac current has been measured as approximately 4A rms during starting, assuming roughly a sine wave variation.

Capacitor current. - The motor bridge capacitors are wet slug, polar, tantalum. Maximum rated continuous ripple current is 400mA rms. However, the allowable ac current is related to the capacitor power dissipation capability; thus, the peak transient ac current capacity is much greater than the allowable continuous current. As a result, extensive tests have been conducted using a 3A peak to peak current at 312 Hz, for up to six seconds over a one minute duty cycle; no degradation in the capacitor's electrical specifications was noted. Specifically, the test was conducted using four 82μF capacitors in parallel and driving the headwheel motor.

In order to provide a safety factor, five 82μF capacitors are used in the actual Headwheel Bridge Supply. However, the minimum network capacitance due to temperature, aging and production tolerances is 300 μ F, which is equivalent to the four capacitors used in the ac current stress experiment, leaving no safety margin under worse case conditions. Thus, if there is a capacitor failure, - - that is, the leakage current increases enough to blow the series fuse, - - an additional ac starting current will be shifted to the remaining four capacitors (284 μ F minimum). As a result, test conditions described above will be exceeded and there is a possibility of capacitor degradation, which may eventually lead to failure of all five capacitors.

Fuse Loading. - Each of the motor bridge capacitors contains a subminiature 2A fuse in series with the primary ground in order to prevent a short circuit on the primary power bus in the event of capacitor failure. The fuse is derated to 1.8A for operation in space, and a 200% overload is permitted for up to 5 seconds before blowing.

Capstan Bridge Supply. - The Capstan Motor Bridge Supply consists of L2, and three parallel 82 μ F capacitors, C6, C7 and C8. In the record/playback modes (low speed), the dc starting current is 1A, and decreases to about 350 mA when running at 250 Hz. When a one ohm detorqueing resistor is placed in series with the input to the bridge supply, the start-up time is approximately 1.5 seconds.

In the high speed mode (Fast Forward or Rewind), the starting current is 4A and the running current is 0.5A at 1000 Hz. Since the Capstan Motor power requirement is greater in the High Speed Mode than in the Low Speed Mode, the bridge supply capacitor ac starting current will be most critical at high speed start. However, the worst case capstan current and starting time are less than one-half that of the Headwheel Motor which uses five capacitors, therefore, it may be assumed that the three capacitors used in the Capstan Bridge Supply will not be overstressed.

I_ω Bridge Supply. - The I_ω Bridge Supply consists of L3 and four parallel 82 μ F capacitors --C9, C10, C11 and C12. Since the dc starting current is only one-fourth as much as the Headwheel Motor current, and the running current is one-half as great, the four capacitors used result in considerable safety factor when compared to the Headwheel Bridge Supply, that is, assuming the ac starting current is somewhat proportional to the dc starting current.

b. Filtered Primary Power. - The primary voltage (-24.5 Vdc) is low-pass filtered prior to feeding the DC/DC Converter and the command and control circuits. The filter consists of L4 and two 6.8 μF capacitors C13 and C14, in parallel. Converter maximum steady state current is approximately 2A, which results in about a 0.18V drop due to inductor winding resistance.

Since the series inductance is relatively small, the converter current turn-on surge is directly proportional to the converter output filter capacitance and the loading capacitance. The present surge during converter turn-on is 6 to 8A peak.

The command and control load is primarily due to the shoe solenoid, which requires a 4.6A pulse during pull-in and 85 mA during hold. Since a ramp is used to control the pull-in switch, the current rise time is within system requirements.

c. Current Telemetry. - The Headwheel Motor, Capstan Motor and total recorder primary current are monitored by modulating a 50 kHz sine wave through a saturable transformer. The resulting sine wave is then amplified and rectified and the dc level is sent to the telemetry sub-system.

The 50 kHz signal is derived from the spacecraft clock and processed on the Reference Generator board. Typically, the Reference Generator output level is 1V rms. The initial level is primarily dependent on the differential voltage comparator output positive and negative limits, which have a +27% and -27% variation, respectively. The comparator output, which is typically 3.4V pp, has a worst case range of 2.3 to 4.6V pp.

In addition, the comparator output drifts with temperature, and the temperature drift will be reflected as a change in the 50 kHz reference level. Both positive and negative levels decrease as temperature increases. As a result, there will be a lower peak-to-peak signal at high temperatures and a higher signal as temperature decreases. The worst case temperature drift (25° - 60° C) is approximately -6%.

1. Recorder Current. - The recorder primary current is approximately 11A during motor start-up and decreases to 2.5A in steady-state standby, or 4.5A in steady-state MSS. The dc current vs. 50 kHz signal amplitude is non-linear up to about 2A input, and has a sensitivity of approximately 60mV/A thereafter.

   Due to the transformer core temperature characteristics the output signal level exhibits considerable drift over the ERTS system temperature range of operation. Laboratory tests have resulted in an output drift from the 25° C, 2.5A level of +8.9% at 60° C and -6.8% at 0° C. As the dc current level increases, the temperature drift becomes worse. Data shows the drift from the 25° C, 4.5A level is +10.8% at 60° C and -12% at 0° C.

2. Headwheel Motor Current. - The Headwheel current is 8A during start-up and drops to 0.5A when switched to the run winding. The transformer output voltage as a function of dc input current is linear up to about 0.8A, then begins to approach saturation. Output voltage sensitivity is approximately 1.4V/A.

   Laboratory temperature tests have shown an output level drift from the 25° C, 0.5A level of +7.2% at 60° C and -8.5% at 0° C.

3. Capstan Motor Current. - In the low speed mode (record or playback), the capstan motor current is 1A during start-up and 0.35A during run. In the high speed mode (fast forward or rewind), the starting current is 4A and the run current is 0.5A. The transformer output voltage as a function of dc current is linear up to about 0.55A, and the voltage sensitivity is 2.5V/A.

   Laboratory temperature tests have shown an output level drift from the 25° C, 0.3A level is +13% at 60° C and -6.2% at 0° C. At the 0.5A level, the drift is +6.7% at 60° C and -8.6% at 0° C.

d. Starting Ramp Circuits. - In order to comply with the Primary Power Supply transient loading requirements, the motor starting current surges have been limited by applying the supply voltage to the Motor Driver Control circuits in the form of a ramp function. Since the headwheel and $I\omega$ motors operate together, they use a common ramp generator. A separate, lower power circuit provides the capstan ramp.

1. Headwheel and Iω Ramp - The Headwheel and Iω ramp circuit consists of Q1 and Q2 connected in a Darlington configuration.

Rise Time - Since the transistor input impedance is very high, the output voltage rise time, T_r, is determined principally by the charging of C_{15} through R_{20}. Or,

$$T_r = R_{20} C_{15}$$

And for minimum component values, T_r = 41 ms.

Fall Time - The ramp circuit fall time, T_f, is a function of the motor driver circuit filter capacitors discharging through the output transistor emitter resistor, R_{22}. Since there are four drivers controlled by the HW/Iω ramp, each containing a 39 uF capacitor, the total capacitance is 159 uF. Or,

$$T_f = R_{22} (159 \text{ uF}) = 1 \text{ second}$$

Quiesent Output Voltage - The ramp generator output voltage level is limited by the driver transistor Base-to-Emitter drop and base circuit series impedances. Thus, from Figure 4-116, the output voltage is:

$$V_{E2} = V_5 - I_{B1} R_{20} - V_{BE1} - I_{C1} R_{21} - V_{BE2} \quad (1)$$

where V_5 = the -22V dc converter voltage.

Since, for a Darlington circuit,

$$I_{B1} = \frac{I_{C2}}{h_{FE1} h_{FE2}} \quad (2)$$

and, letting $I_{C2} = I_L$, and $V_{E2} = V_{out}$, then substituting into equation 1, the quiesent output voltage is

$$V_{out} = V_5 - \frac{I_L R_{20}}{h_{FE1} h_{FE2}} - V_{BE1} - \frac{I_L R_{21}}{h_{FE2}} - V_{BE2} \quad (3)$$

For large h_{FE} ($h_{FE} > 50$), base resistor losses are negligible and, from equation 3, and the output voltage reduces to

$$V_{out} = V_5 - V_{BE1} - V_{BE2} \tag{4}$$

Using nominal values, from equation 4, $V_{out} = 20.7V$. Maximum output voltage is given by

$$\overline{V_{out}} = \overline{V_5} - \underline{V_{BE1}} - \underline{V_{BE2}} \tag{5}$$

and substituting into equation 5, $V_{out} = 22.0V$. Similarly, the minimum level is

$$\underline{V_{out}} = \underline{V_5} - \overline{V_{BE1}} - \overline{V_{BE2}} \tag{6}$$

and for worst case values, $V_{out} = 19.0$

Power Dissipation - Since the transistor base, and therefore the emitter, are clamped to the driver control level (-22V) which is also the collector potential, complete saturation during turn-on is not possible. As a result, transistor power dissipation is relatively high.

Q1 dissipation. - Transistor power dissipation is given by

$$P_d = I_C V_{CE} \tag{7}$$

where, for the ramp circuit, $V_{CE} = V_5 - V_E$. Then for Q1,

$$V_{E1} \approx V_5 - V_{BE1} \tag{8}$$

and, since $I_{C1} \approx \frac{I_{C2}}{h_{FE2}}$, the power dissipation is

$$P_{d1} = \frac{I_L}{h_{FE2}} V_{CE1} = \frac{I_L}{h_{FE2}} V_{BE1} \tag{9}$$

From the above result, maximum power dissipation is

$$\overline{P_{d1}} = \frac{I_L}{h_{FE2}} \overline{V_{BE1}} \tag{10}$$

For I_L = 470 MA during starting, P_{d1} = 7.8 MW. During run,

I_L = 225 mA, and P_{d1} = 3.8 mW.

Since the power dissipation is very low, the increase in Q1 junction temperature will be insignificant.

Q2 dissipation - Using the above analysis as a guide, Q2 collector - emitter voltage is

$$V_{CE2} = V_5 - V_{E2} = V_5 - (V_{BE1} + V_{BE2}) \tag{11}$$

and from equation 7, Q2 power dissipation is

$$P_{d2} = I_L (V_{BE1} + V_{BE2}) \tag{12}$$

Maximum dissipation is given by

$$\overline{P}_{d2} = \overline{I}_L (\overline{V}_{BE1} + \overline{V}_{BE2}) \tag{13}$$

Again, for I_L = 470 mA during starting, $\overline{P}_{d2}$ = 0.86 W, and for I_L = 225 mA during run, $\overline{P}_{d2}$ = 0.4 W.

The transistor junction temperature as a function of power dissipation is

$$T_j = T_A + \theta_{J-A} P_T \tag{14}$$

where,

T_j = Ambient Temperature (°C)

and,

θ_{J-A} = Thermal resistance from junction to free air (°C/W).

Thus for, Q2 at T_A = 60°C and θ_{J-A} = 34°C/W, from equation 14,

$\overline{T_J}$ = 89°C at start-up and $\overline{T_J}$ = 75°C during run, both of which are below the system maximum allowable junction temperature of 110°C. In addition, since the starting time (approximately 5 seconds) is less than the transistor thermal time constant, the maximum junction temperature at start-up will be less than 89°C.

2. Capstan Ramp. — The Capstan motor ramp generator circuit consists of transistors Q3 and Q4 connected in a Darlington Pair. The circuit analysis is similar to the above analysis of the Headwheel and Iω Ramp Generator.

Rise and Fall Time. - The ramp rise time is given by

$$T_r = R_{23}\ C_{16} \tag{15}$$

For minimum component values, T_r = 19 ms.

The ramp turn-off time is determined by the discharge of two 39 μF capacitors through the output transistor emitter resistor, R_{25}. Or,

$$T_f = R_{25}\ (78\,\mu F) = 530\ ms$$

Quiesent Output Voltage - From the previous analysis, the Capstan ramp generator output voltage is

$$V_{out} = V_5 - V_{BE3} - V_{BE4} \tag{16}$$

For nominal values, V_{out} = 20.6V, and using worst case values, $\overline{V_{out}}$ = 21.9V and V_{out} = 18.8V.

Power Dissipation. - Q3 dissipation is given by

$$P_{d3} = \frac{I_L}{h_{FE4}}\ V_{BE3} \tag{17}$$

Where I_L = 215mA during the 1.5 second start up time and I_L = 97mA in the high speed run mode. For worst case values, during start-up, P_{d3} = 2.4mW, both of which are negligible compared to the transistor dissipation capacity.

Q4 dissipation is given by

$$P_{d4} = I_L (V_{BE3} + V_{BE4}) \tag{18}$$

The maximum Capstan motor duty cycle is 1.5 seconds in start-up and 10 to 15 seconds in run. Since the start time is much less than the transistor thermal time constant, the computation of average power dissipation is applicable. Thus, neglecting the switching interval,

$$P_{d4} = \frac{(I_{start}\ t_{start} + I_{run}\ t_{run})\ (V_{BE3} + V_{BE4})}{t_{start} + t_{run}} \tag{19}$$

and worst case average dissipation is $\overline{P_{d4}} = 217$ mW.

This value of power dissipation exceeds the heat radiation capacity of the transistor type used and, therefore, some means of heat conduction should be provided in order to meet the system maximum allowable junction temperature requirements.

Recorder Current Transients. - According to ERTS system requirements, peak current changes on the primary power supply (-24.5 Vdc) bus including both increasing and decreasing steps, must conform to the minimum allowable rise time vs current step shown in Figure 4-117. This curve indicates the minimum allowable rise time that can occur without a loss of voltage regulation on the -24.5 Vdc bus.

Laboratory measurements of primary current transients have been conducted for a number of functions requiring large current changes. The switching characteristics of several critical conditions are shown in Table 4-38. Current changes which are less than the minimum allowable specifications are shown in parentheses. Of particular interest is the DC/DC Converter turn-on current surge, which has a rise time of one ms and a fall time of two ms as compared to the minimum allowable rise and fall times of 12 and 8ms respectively. Efforts are presently being directed towards slowing down the converter turn-on surge.

Trickle Charge Current. - The motor bridge supplies, along with the motor bridges, are connected directly to the primary bus through a 301 ohm resistor in order to maintain a charge on the bridge supply capacitors and thereby minimizing the recorder turn-on current surge. Since both the bridge supply capacitors and the motor bridge transistors are characterized by a leakage current component when voltage is applied, a small trickle current will flow continuously during recorder shut down. The total leakage current may be written as

TABLE 4-38. PRIMARY POWER SUPPLY CURRENT TRANSIENTS

Subsystem Operation	Maximum Increasing Step (A)	Risetime (MS)		Maximum Decreasing Step (A)	Falltime (mS)	
		Minimum Allowable	Measured		Minimum Allowable	Measured
Headwheel and Iω Start-up	9	10	20	5	5	3 Sec
Start-run				6	5-6	(2-3)
DC/DC Converter	9.5	12	(1)	8.5	8	(2)
shoe solenoid	4	3.5	5-6	4	3.5	(2-3)
Capstan Standby	1	None	≈10			
MSS Standby to Fast Fwd	3	2	5	1	None	2

Note: Current Steps do not include changes of less than 1A.

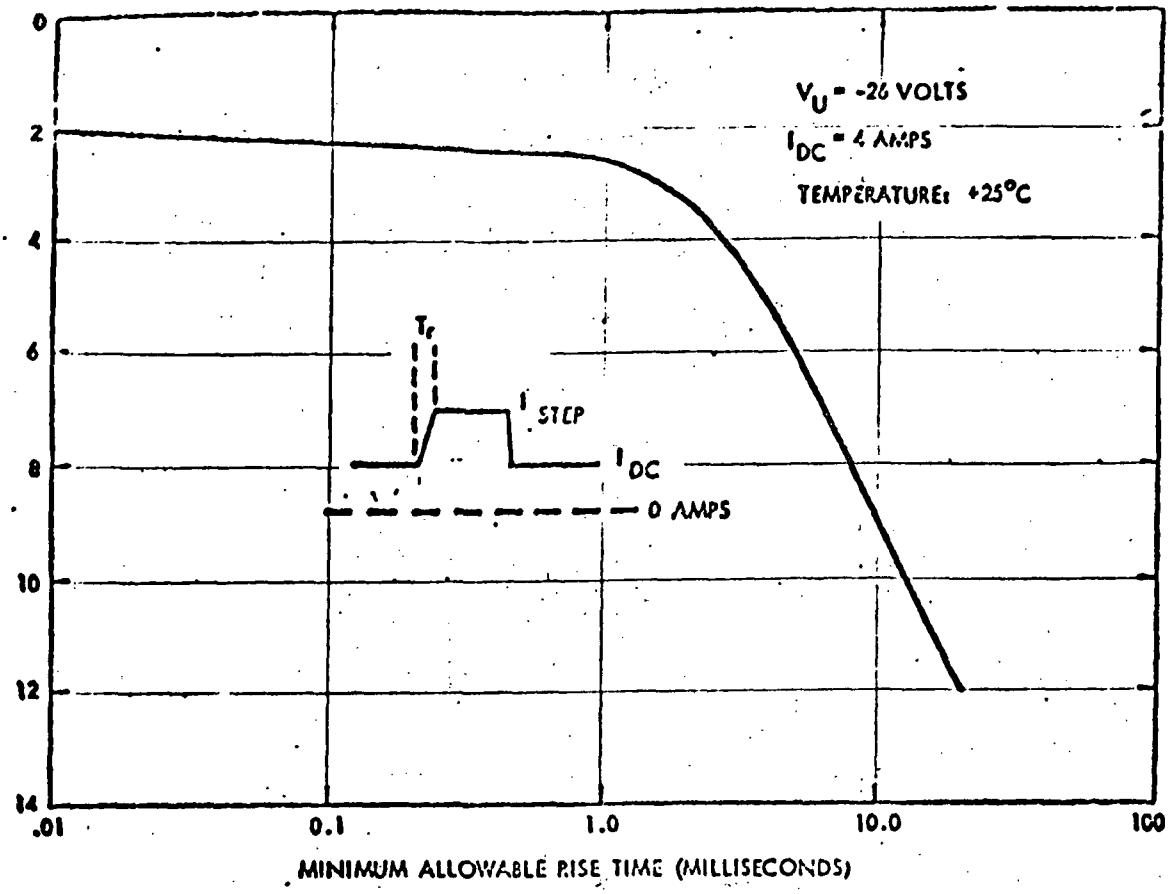


Figure 4-117. Minimum Allowable Current Rise Time

TABLE 4-39. IC LOGIC GATE SUPPLY VOLTAGE LIMITS

Circuit Type	Max $\frac{Vcc}{(Vcc)}$	Max $\frac{Vin}{Vin}$	$\frac{\Delta V}{(\approx Vcc - Vout)}$	Max Allowable System Vcc (Vcc = Vin + ΔV)
Motorola MTTL-MC3100	8	5.5	1.5	7
TI TTL-5400	7	5.5	1.5	7
Fairchild TTL-9000	8	5.5	1.5	7
Raytheon TTL-RF3200	7 to 12v for 1 sec	5.5	1.6 Typ	7.1

$$I_L = N_c I_c + N_T I_{CES} \quad (20)$$

Where,

N_c = Number of Capacitors

I_c = Capacitor leakage current

N_t = Number of transistors

I_{CES} = Transistor Cut-Off Current

1. Capacitor Leakage.- The motor bridge capacitors are 82 μF, CL67 tantalum electrolytics with a maximum leakage current of 16 μA each at 85°C. In addition, there are two 6.8 μF capacitors in the primary supply filter which have a maximum leakage of 2 μA. Summing up the 14 capacitors, the maximum leakage current at high temperatures is

$$\overline{I_{CT}} = 12\ (16\mu A) + 2\ (2\mu A) = 196\ A$$

Typically, at 25°C, the capacitor leakage is about 25 μA.

2. Transistor Leakage. - The motor bridge transistor base is connected to the emitter through a low resistance transformer winding, thus I_{CES} the collector cut-off current for the emitter shorted to the base, is applicable. Manufacturer's specifications for maximum leakage currents are given for reverse voltage levels, which are much greater than the levels experienced in the actual motor bridge application; as a result, the leakage current levels are several mA, which is unrealistic for trickle resistor design purposes.

If typical values, which are specified at a lower voltage, are used, then the leakage current at 100°C is 90 μA; or, for the 12 parallel transistor pairs, the maximum leakage current is about 1mA. If the leakage is allowed to double due to aging, then the worst case leakage current is 2mA. As a result, the charging resistor maximum voltage drop is 0.6 volts, and the leakage current worst case power dissipation is approximately 50mW.

Since two transistors are in series with 24 volts, the average reverse voltage is 12V and, as a result, the cut-off current is very low. Measurements of type 2N4398 transistor samples have resulted in I_{CES} readings of 1 to 2 μA, and a total system leakage current of less than 30 μA at room temperature.

5.6V Supply Transient Suppression. - As a result of relay activation times, there is a delay in the reaction of the voltage protection circuit, and a 9V transient of up to 12 ms in duration is possible on the 5.6 Vdc supply. In order to protect the integrated circuit logic elements from this overvoltage, a zener diode (VR1) which has a nominal breakdown voltage of 6.8V has been provided to instantaneously clamp the transient.

1. Diode Clamping Level. - Zener diode VR1 (1N2970C), has a nominal value of 6.8V with a ±2% initial tolerance. If a ±6% variation due to aging is permitted, neglecting temperature drift, the worst case limits are 6.3 to 7.4V. Maximum diode transient current is governed by the converter output impedance, Or,

$$\Delta I_z = \frac{\Delta V}{R_s} \tag{21}$$

and, for a source impedance of 0.22 ohms, I_Z = 12A, which is less than the maximum allowable nonrecurrent current, assuming an output system load of approximately 1A.

Depending upon the converter output level, a small amount of diode leakage current will flow continuously. Experimental leakage current measurements have shown that the leakage current at 61°C for a nominal output voltage of 5.6V and a nominal zener breakdown of 6.8V is about 3 mA; or, the typical power dissipation is about 20 mW.

Worst case diode power dissipation will occur for the minimum breakdown voltage in conjunction with the maximum converter 5.6V output level. For a minimum breakdown voltage of 6.3V, including the initial tolerance and aging characteristic and a high converter output of 6V, the worst case power dissipation is projected as about 120 mw.

2. Integrated Circuits Voltage Limits. - In general, the maximum allowable gate supply voltage, V_{cc}, is not the primary factor in determining the maximum V_{cc} which may be applied to a number of interconnected elements. Since the voltage at a high output is proportional to the V_{cc} voltage, the maximum allowable gate input voltage, V_{in}, to the following stage can be exceeded. Therefore, the primary limit on V_{cc} is that the voltage at any input may not go above the maximum allowable V_{in} unless the input current is limited.

The supply voltage limits for various types of logic gates used in the recorder are shown in Table 4-39. The maximum allowable supply voltage is 7V, which is less than the worst case clamping level of 7.4V. However, since all logic circuits are decoupled from the converter outputs through a series impedance, the maximum V_{cc} transient at the gates is less than 7V.

Voltage Protect Relay. - The voltage protection relay is a latching relay which is SET (opened) by the activation of the voltage protection circuit and RESET (closed) by a command from ground control. The minimum allowable operating voltage is 9V for a duration of at least 10ms. For the specified primary power supply limits, the voltage protection circuit worst case levels are 11.6V to 13.2V, which are above the minimum allowable relay coil voltage (9V), yet do not exceed the maximum allowable voltage of 14.5V. It may be noted that worst case analysis of the voltage protection circuit has shown that at continuous primary voltage levels of less than 13.8V, or at primary power shut down, the voltage protection circuit will be inoperative. As a result, the voltage protection relay will remain in its original state (closed).

The ground control reset signal is a 21V pulse with a 37ms duration. In order to limit the relay coil voltage below 14.5V, a 100 ohm resistor has been placed in series with the reset winding. Thus the minimum reset voltage, neglecting diode drops is given by

$$V_c = \frac{R_{coil}}{R_s + 100 + R_{coil}} (V_{in}) \qquad (22)$$

or the $V_{in} = 20.5V$, and $R_S = 70$ ohms (the reset signal source impedance), $V_c = 0.3$.

The maximum reset coil voltage is slightly greater than the maximum allowable but, since the reset pulse is of short duration compared to the deenergized period, the average coil power dissipation is negligible.

4.4.8.3 Conclusions and Recommendations. - Worst case analysis of the circuits which comprise the Motor Auxiliary Board has shown that they will perform reliably over the ERTS system requirements. However, a few of the large current surges, particularly during DC/DC Converter turn-on, do not meet allowable spacecraft power supply transient limits and are still being reviewed.

It may be noted that the ac current during motor start-up exceeds the motor bridge supply capacitor maximum allowable continuous ac current limit. Therefore, low duty cycle, overload tests have been conducted to ensure that no degradation of capacitor electrical characteristics will occur as a result of transient overloads.

The current telemetry transformers show considerable drift due to temperature. Since the temperature coefficients vary from unit to unit, individual calibration curves must be generated over the system temperature range of operation if a highly accurate telemetry indication is required.

Since the worst case average power dissipation of the capstan ramp output transistor, Q4, is greater than can be dissipated through radiation alone, some means of heat conduction should be provided in order to maintain a junction temperature below the maximum allowable of 110°C.

A simplified and more stable current telemetry system should be considered in any future circuit revision. It appears that since a small amount of series resistance due to coils, transformers and clamping resistors has been introduced into the system, the current telemetry functions may be performed by measuring the voltage drop across this resistance with a differential input operational amplifier. It should be recognized, however, that some resistor divider attenuation of the primary voltage level may be required, depending on the operational amplifier common mode voltage limit.

4.5 SERVO SYSTEM

4.5.1 Introduction. - The ERTS recorder system contains two servo systems: A Capstan Servo which is used only during playback and assures that the transversely (wideband) recorded information is properly reproduced; and a Headwheel Damper System which stabilizes the rotation of this component during the record and playback process.

4.5.2 Capstan Servo. - The purpose of the Capstan Servo is to assure proper tape speed and phasing to assure tracking of the transversely recorded information. During recording, the TWA signal is recorded longitudinally along the edge of the magnetic tape. This will make an indexing mark everytime the headwheel makes a full revolution; i.e., everytime four transverse video tracks have been recorded. Upon playback, this signal is compared to the phase of the TW signal so that a track-by-track scanning alignment can be achieved.

The basic operation of the Capstan Servo can best be shown by reference to Figure 4-118; a more detailed block diagram is shown in Figure 4-119 and the schematic diagram in Figure 4-120. The tonewheel timing reference is the TW3 signal derived from the reference generator. The processed control track signal forms the other input to the phase detector whose output drives a VCO (voltage controlled oscillator). This signal in turn determines the speed and phase of the capstan motor and, hence, the control track signal. By using only a once-around reference, the information recorded by a particular head will be reproduced by the same head, thus eliminating various assembly tolerances in the construction of the headwheel panel.

A computer program of the transient response of the servo system has been made, which includes all the electrical and mechanical aspects of the loop. Close correlation between the experimental data and the computer run-off has been noted. The computer run-off has been used to optimize loop performance, and the stability analysis of the system is in progress.

4.5.3 Headwheel Damper. - When the Headwheel of the ERTS recorder is perturbed in some manner it will oscillate at its resonant frequency (approximately 6.5 Hz). The damper circuit is used to dampen this oscillation, causing it to decay. The damping action is accomplished in a feedback loop by sensing changes in the dc supply current to the headwheel bridge circuit. Periodic changes in the supply current are directly related to the oscillatory condition, so that a change in this supply current can produce a control signal which will compensate for that change.

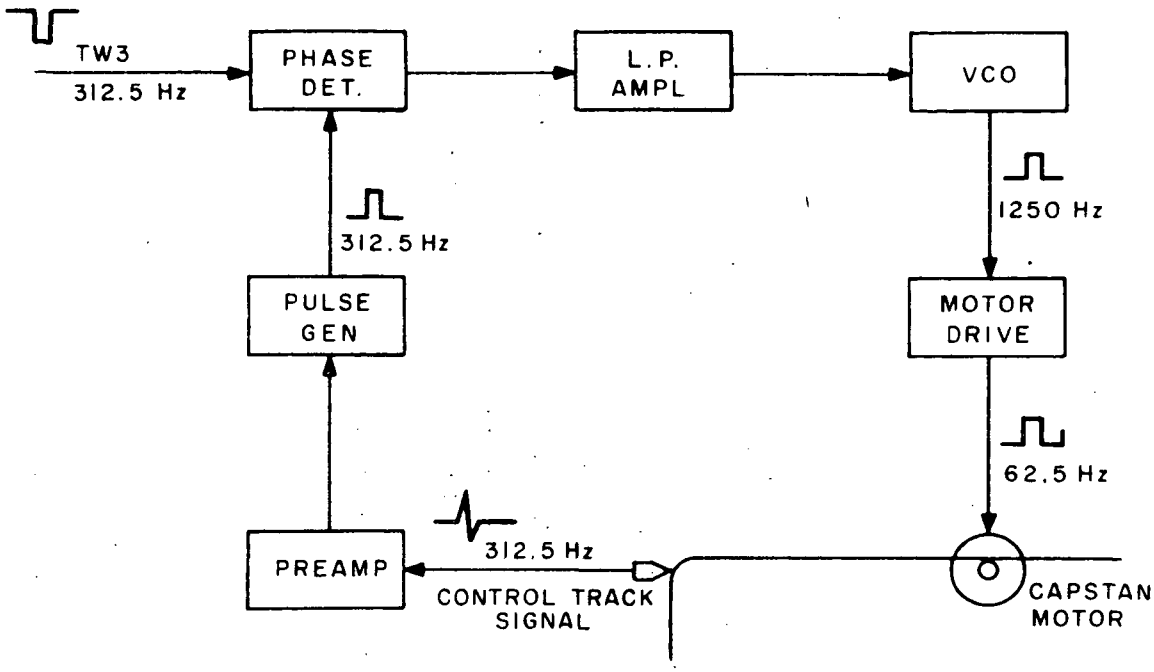


Figure 4-118. Capstan Servo Simplified Block Diagram

A block diagram of the Headwheel Damping Loop is shown in Figure 4-121, and the schematic diagram in Figure 4-122. This feedback circuit will become unstable if the loop gain, U, becomes greater than the low-pass filter time constant, T_1; i.e., instability occurs when $U/T_1 > 1$. $U/T_1 = 1$ represents the critically dampened condition; and, as U/T_1 increases, the effective damping increases. A computer stability analysis of the transfer function for the closed loop Headwheel Damping Circuit indicated that desirable damping occurs when $0.35 \leq U/T_1 \leq 0.9$. Therefore, it would be desirable to ensure that U/T_1 remains within these limits under worst case conditions.

Another consideration of the damper circuit concerns the high-pass filter time constant, T_2. The high-pass filter is used to obtain dc isolation between the amplifier and the delay circuits. If T_1 and T_2 are close in value, T_2, will tend to cancel the effects of T_1. Therefore, it is desirable to ensure that $T_1/T_2 \ll 1$ under worst case conditions.

4.5.4 Capstan Servo Error Amplifier Worst Case Analysis. - The performance characteristics of the Capstan Servo Amplifier and VCO are analyzed in the following paragraphs.

The basic approach is to provide a simplified analytical basis for performance and substantiate reliable operation with a worst case analysis where it has seemed appropriate. Emphasis is directed to the principal functional segments of the system

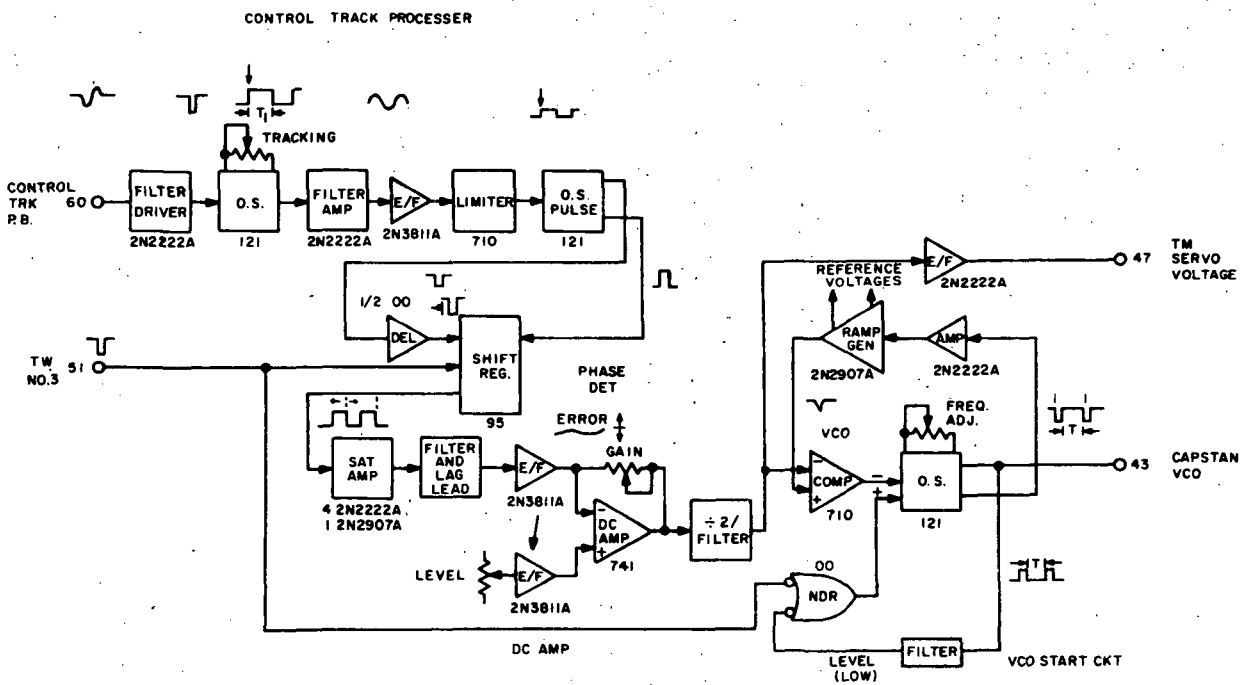


Figure 4-119. Capstan Servo Detailed Block Diagram ERTS

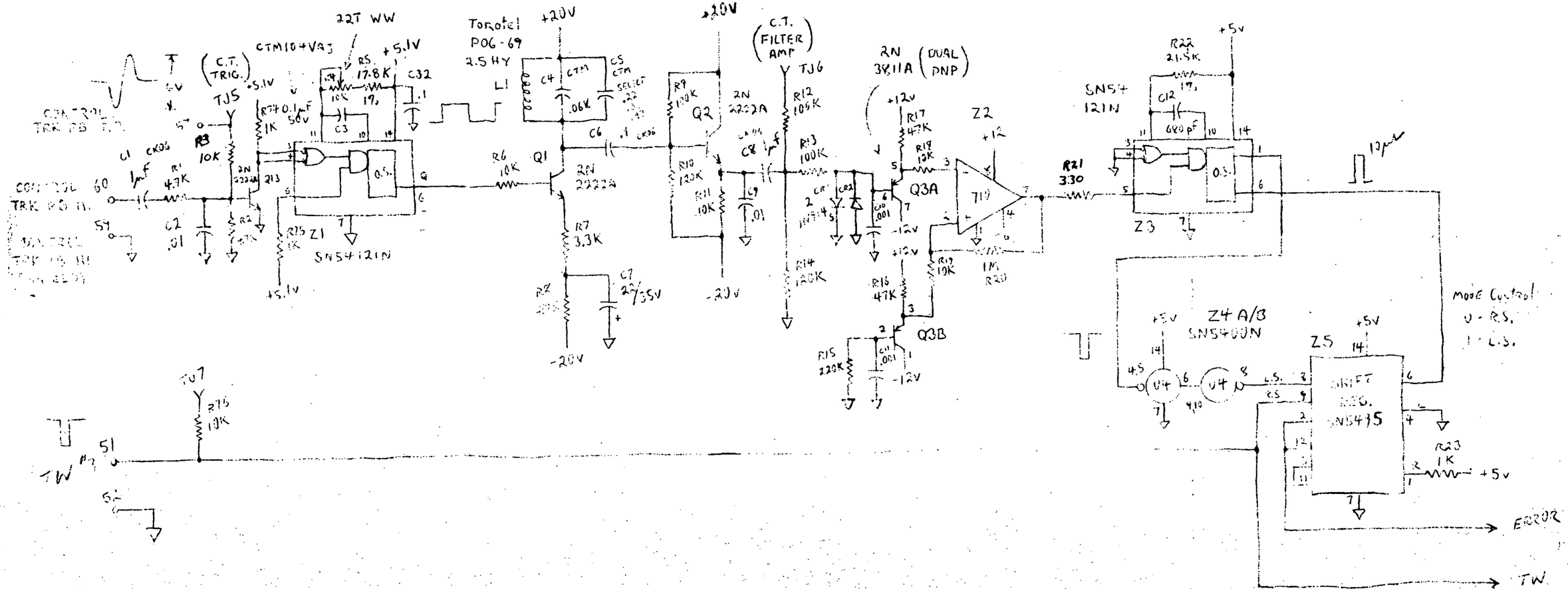


Figure 4-120. Capstan Error Detector, Servo Amplifier, and VCO Schematic Diagram (Sheet 1 of 2)

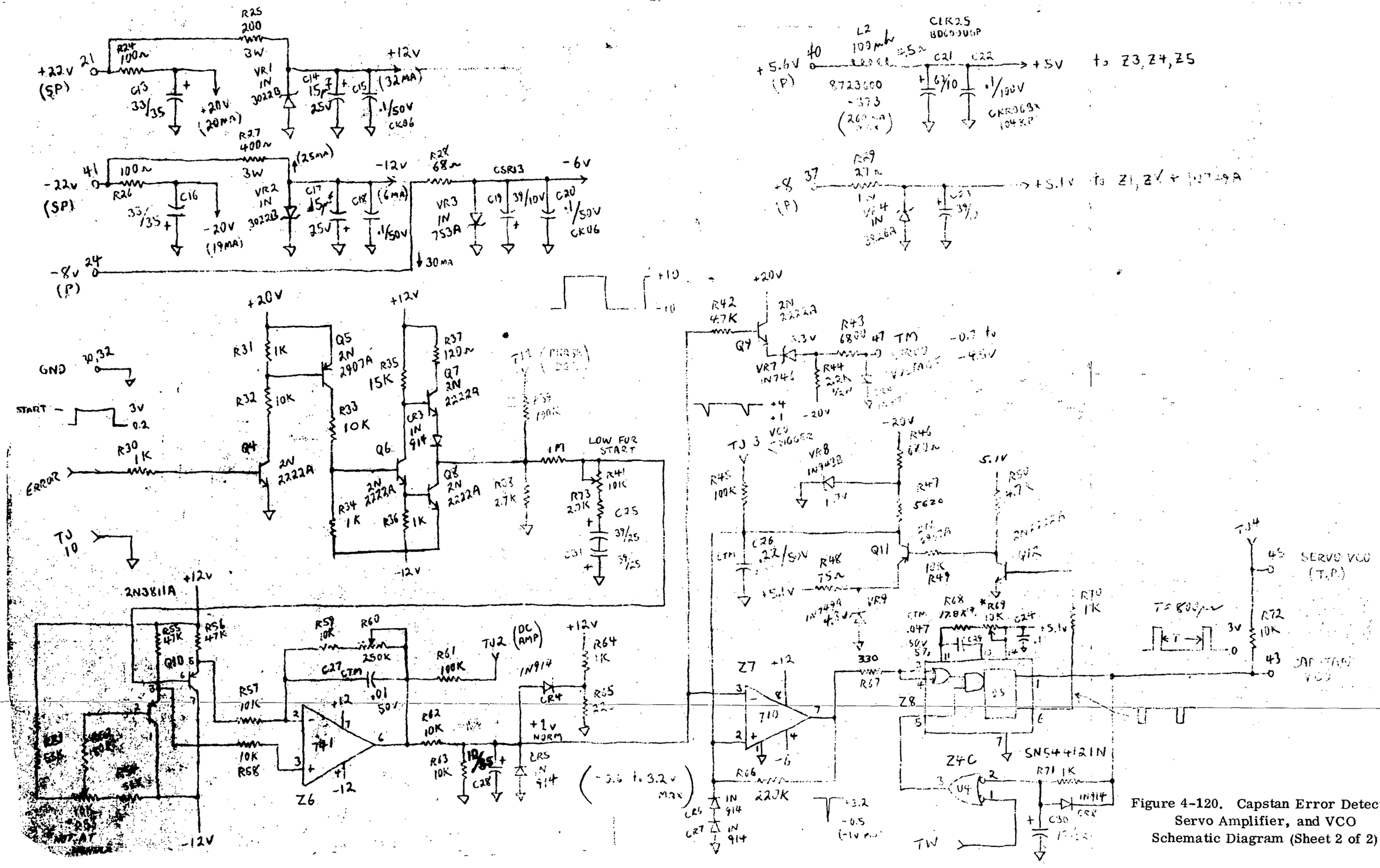


Figure 4-120. Capstan Error Detector, Servo Amplifier, and VCO Schematic Diagram (Sheet 2 of 2)

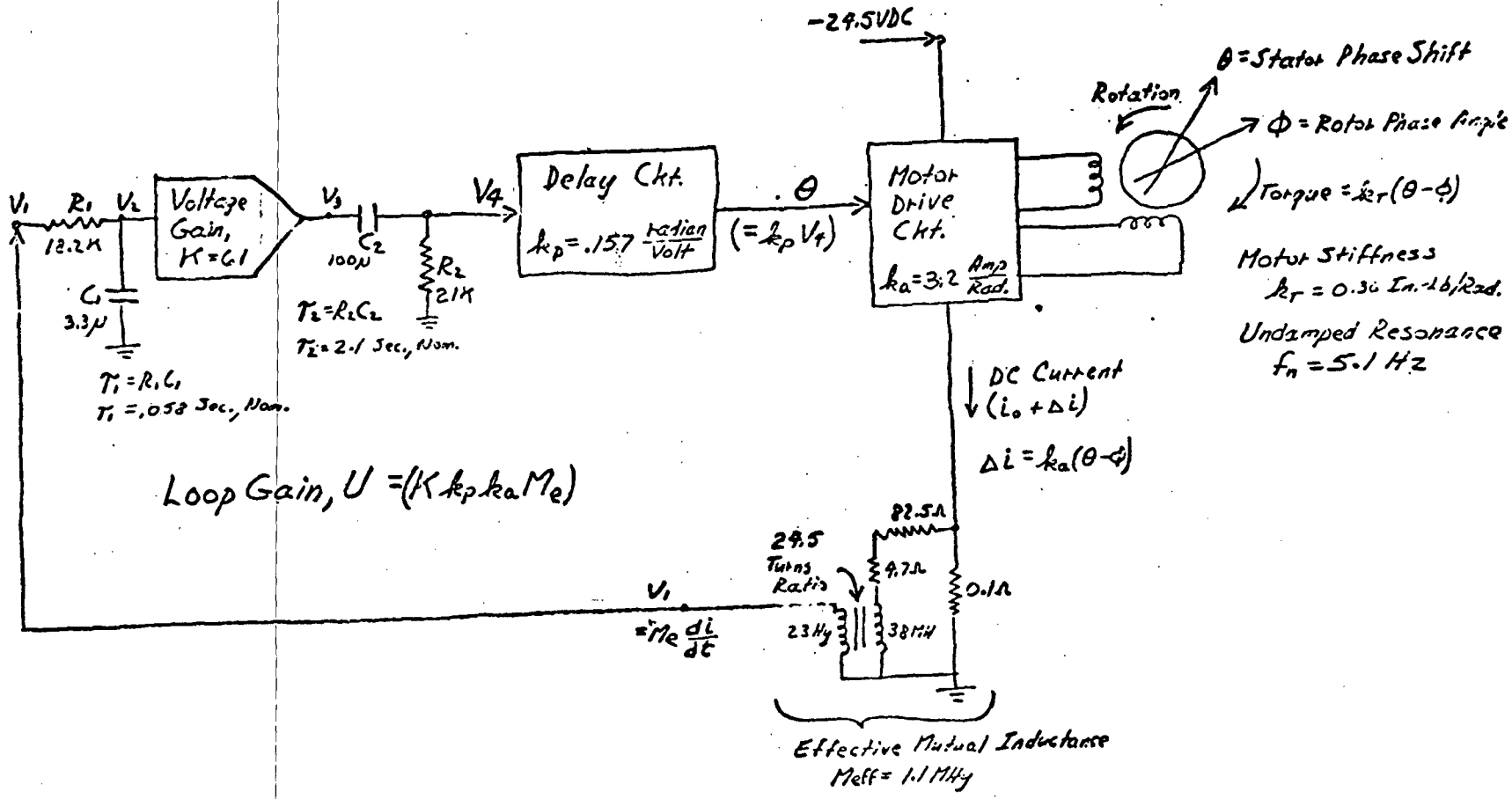
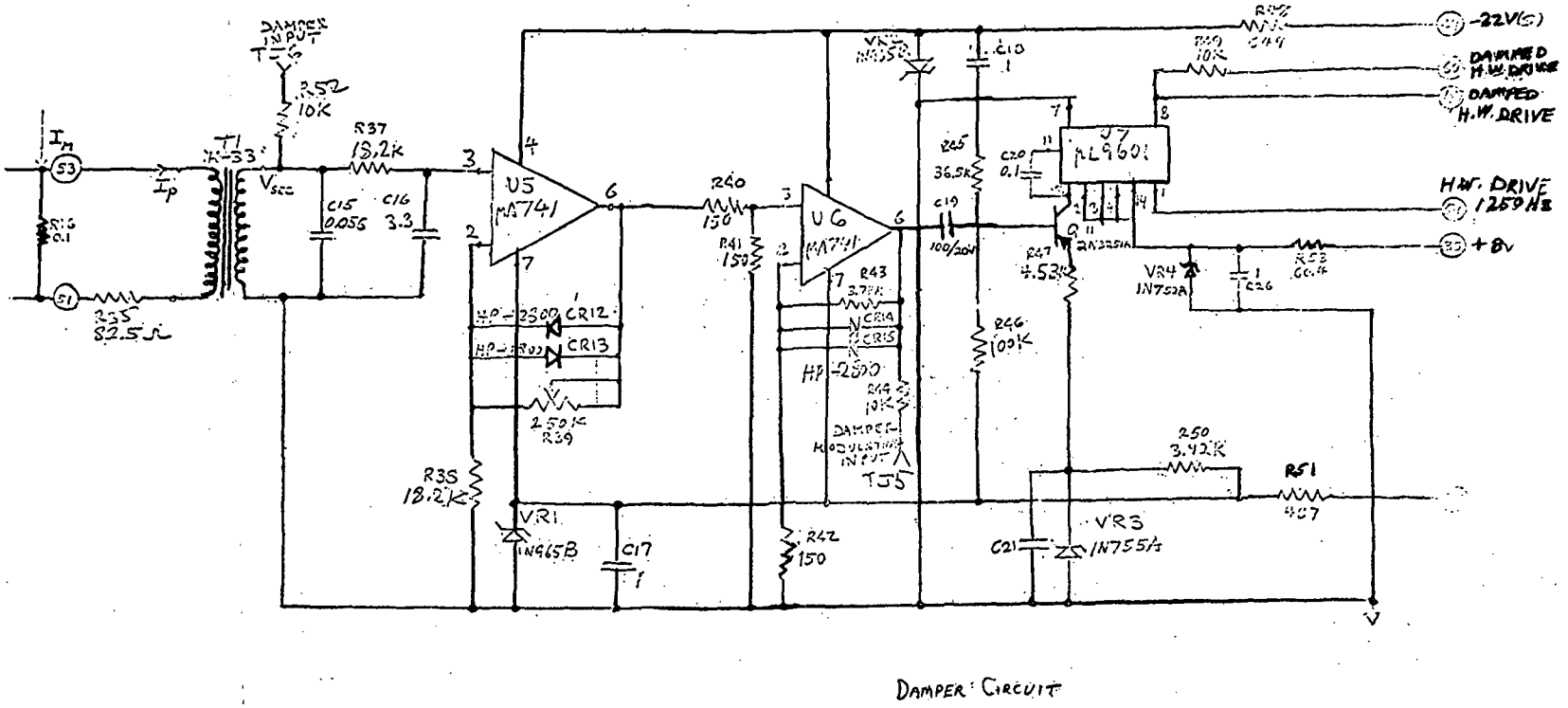


Figure 4-121. Headwheel Damper Block Diagram



DAMPER CIRCUIT

NOTE: ALL DIODES ARE JAN IN5711 UNLESS OTHERWISE SPECIFIED.

Figure 4-122. Headwheel Damper Schematic Diagram

and to an evaluation for the probable variations in loop gain and corner frequencies. Estimates for the bounds of these variations are developed with respect to initial component tolerances, variations in voltage, temperature and aging effects. (See Appendix H for analysis criteria.)

4.5.4.1 Scope of Analysis. - The Servo Amplifier is part of a larger complex which includes a capstan drive motor and a tape transport mechanism. As an integrated system involving closed-loop operation, specifically in its playback mode, conditions and criteria for stability must be established. However, the present analysis will be confined only to the amplifier and VCO; the drive motor and tape transport are described elsewhere. Figure 4-123 is a functional block diagram of the loop in the playback mode; the symbols used conform to those identified with the components of the schematic diagram (Figure 4-120).

4.5.4.2 Servo Functions. - The principal gain factors and frequency transfer functions for the Tape Transport Servo in the Playback mode are shown in Figure 4-124. Here, the purpose is to establish a phase-locked condition between an independent reference signal derived from a tonewheel and a dependent signal derived from magnetic tape. The dependent signal, having been previously recorded on the tape with stimulation by the same tonewheel and constant capstan drive by an accurate primary frequency source, now serves to establish a precise rate of transport when correlated with the tonewheel signal in a closed loop where the drive is now developed by a VCO. In addition to this, the relative displacement between the two signals is also adjustable (corresponding to a framing operation with a movie projector), so that some form of comparison or registration external to the loop is implied (station 11, Figure 4-123), without any reaction on the loop, itself, because of this adjustment.

4.5.4.3 Comparator

4.5.4.3.1 Functional Description. - Starting at station 1, a rectangular voltage wavefront is developed at the output of a phase comparator, which is stimulated by the independent and dependent reference frequencies, Ω_R and $m/n\,\Omega v$, respectively. A phase-lock is established when $\Omega_R = m/n\,\Omega v$ and the error voltage approaches a steady state value.

The phase comparator has a transfer dimension, conveniently expressed as

$\varphi \longrightarrow$ volts/radian

and is implemented as a three-stage, right-shift, left-shift register shown in Figure 4-125 (Z5, Figure 4-120).

An important feature of this design is the fact that the circuit is almost completely free of amplitude sensitivity associated with its input signals (except for non-critical

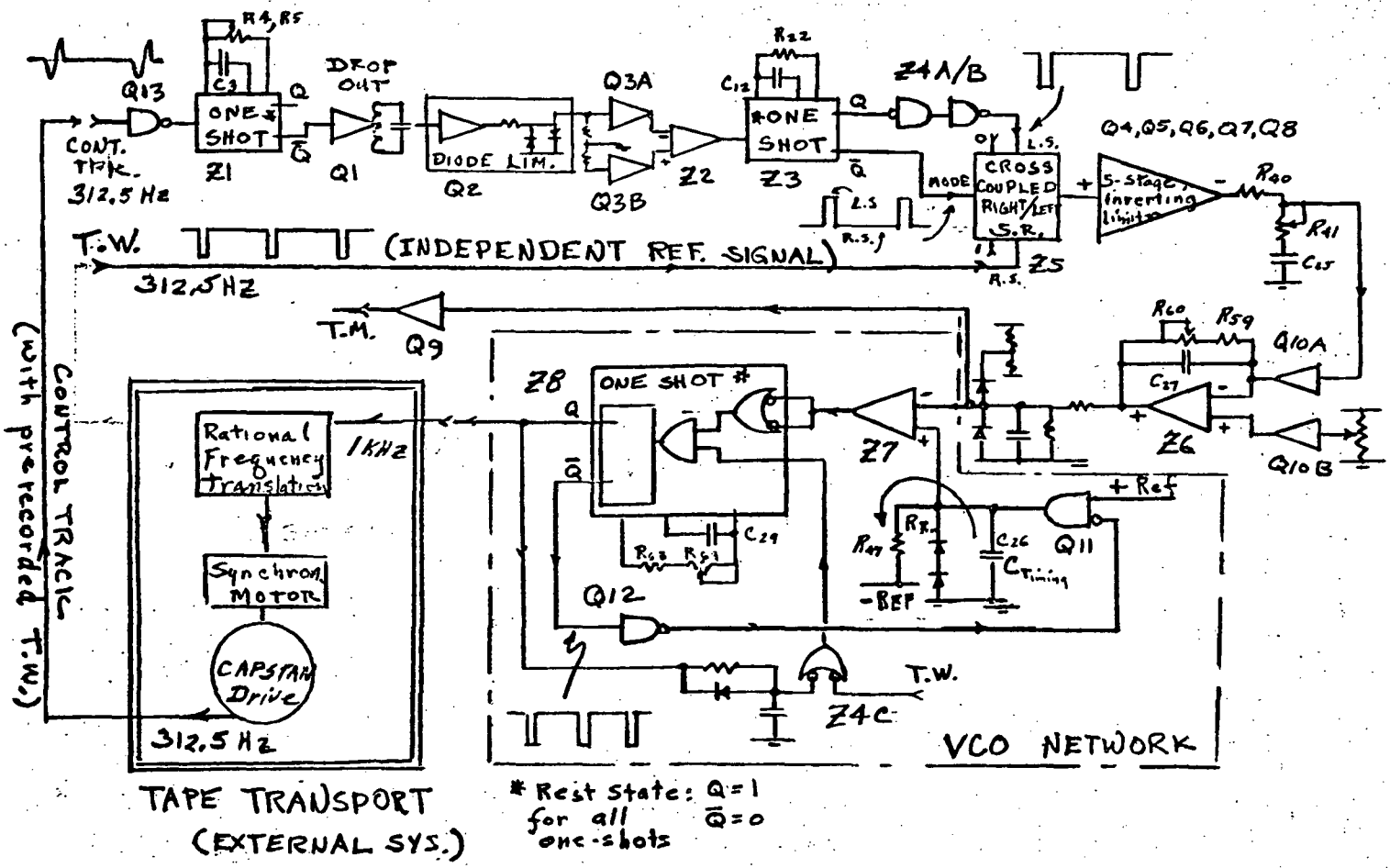


Figure 4-123. ERTS Capstan Error Detector and VCO Loop (Playback Mode)

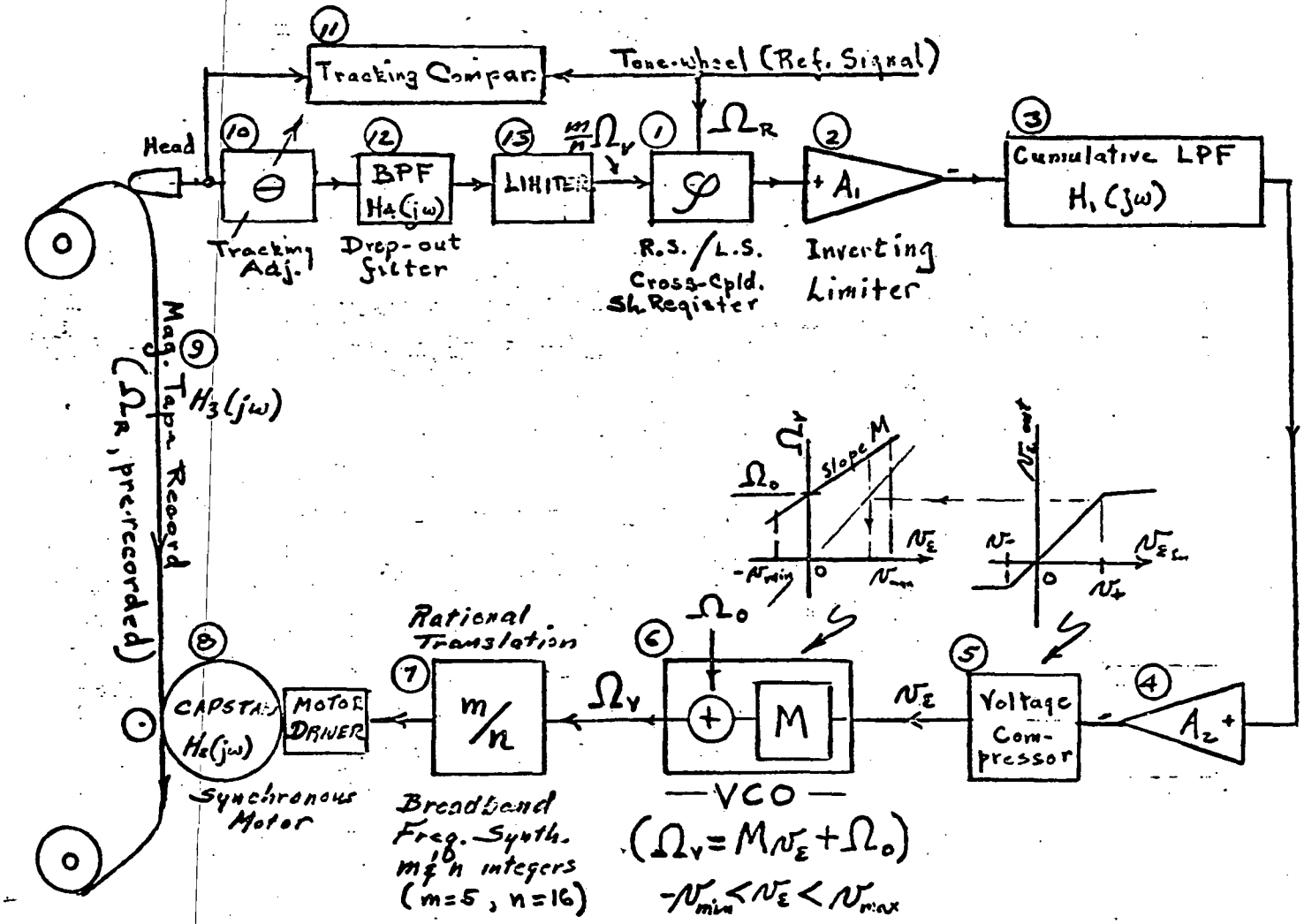


Figure 4-124. Symbolic Diagram Illustrating Principal Gain Factors and Frequency Transfer Functions (Playback Mode)

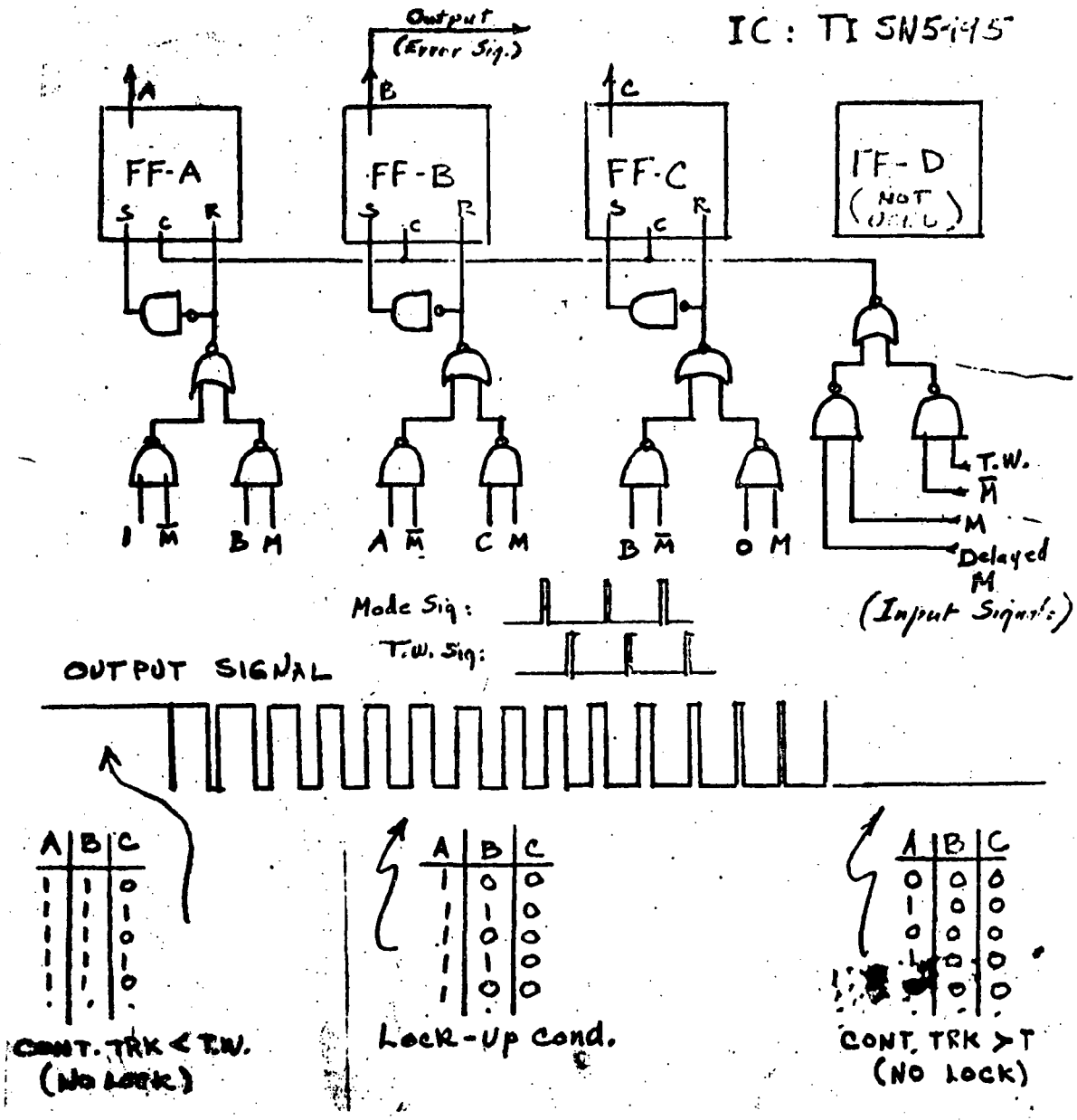


Figure 4-125. R-S, L-S, Three-Cell Phase Comparator

threshold conditions). Conceptually, this is an ideal approach for a comparator, not only inherent in the choice for a flip-flop register but also in the careful zero-crossing, limiter network designs which process the control-track signal.

The mode signal, ultimately derived from the control track, is regenerated as an asymmetrical rectangular signal having a positive-going duty cycle of

$$\frac{C_{12} \times R_{22} \times \ell n2}{\text{Period of C.T. Sig.}} = \frac{0.69 \times 680 \times 21.5 \times 10^{-9}}{(1/312.5)}$$

$$= 0.31\%$$

An auxiliary output developed as an inverted mode signal at stage Z3 and suitably delayed by successive inversions Z4 A/B, to assure proper triggering for the shift register, is also used in conjunction with the timing-wheel reference signal.

When the mode signal has a repetition rate which tends to be faster than that of the reference signal, the state of FF-C is (Figure 4-125) gated more frequently by its right-sided input, a logical zero. If this differential rate between the two input signals persists, the effect is such that FF-C transfers an output zero to FF-B, which in turn transfers an output zero to the input of A. The output states of B and C will then remain constant at logic zero and only the output of FF-A will change state. The error signal, developed at the output of FF-B, therefore remains low. One may think of this operation -- that of the dependent signal momentarily running at a higher rate than the reference -- as a right-shifting or zero-producing effect at the comparator. Conversely, when the control track (dependent signal) momentarily runs at a lower rate than the reference, the left-sided inputs to all three flip-flops tend to be gated more frequently than their right-sided inputs. Ultimately if this differential rate persists, the left-sided logical one input to FF-A is transferred to FF-B and then to FF-C, so that A and B outputs remain at logical one levels and only FF-C continues to change its state. Thus, a momentary decrease in the control track rate is accompanied by a left-shifting, or one-producing effect at the comparator.

Finally, with a proper phase-lock established, it is clear that only FF-B changes its state; FF-A output remains constant at a logical one level and FF-C remains constant at a logical zero level. The error signal, developed by the output of FF-B, is therefore a quasi square wave whose duty cycle will vary in accordance with the free-running error of the VCO.

4.5.4.3.2 VCO and Loop Relationships. - It is important to note that the free-running frequency of the VCO (with a design-center value of control voltage applied) must correspond closely to the reference frequency, and that its frequency range of

control must straddle the reference position in such a way that all anticipated variations due to environmental or aging influences can be accommodated. These properties may be regarded as a desirable "positional" characteristic of the VCO.

A "derivative" characteristic suggests that an arbitrarily small increment in the error voltage is accompanied by an opposing, or restoring effect, developed by the loop return to the same point (applies to any point of analysis in the loop). This condition is implied by the proper polarity associated with the right-shift, left-shift properties of the comparator, the slope of the modulator, and the number of inversions associated with amplifications for the error signal.

Finally, while the above characteristics are necessary they are not sufficient. It is also necessary to investigate the open-loop properties of the system to assure the condition that 180-degree phase shift is not accumulated within the spectral range for which the error-signal gain-factor may exceed unity (Nyquist criterion and Bode plots).

4.5.4.3.3 Transfer Function Evaluation. - To evaluate the transfer function for the phase comparator, one may determine the range of operation of the timing wheel pulse relative to the mode control signal as shown in Figure 4-126.

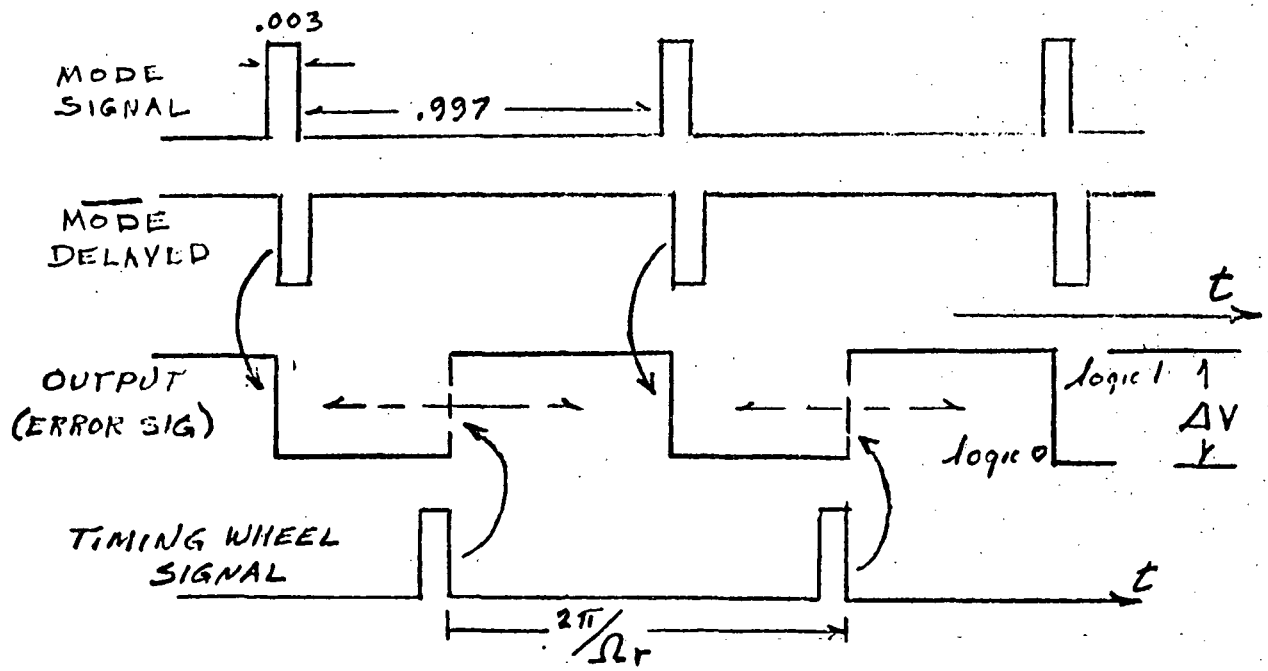


Figure 4-126. Range of Phase Comparison

It is clear that phase comparison is virtually possible over 2π radians, a particular feature of this type of network, so that the transfer function is

$$\Delta V/0.997 \times 2\pi \approx \frac{\Delta V}{2\pi} \quad \text{volts per radian}$$

where ΔV is the voltage difference between logic one and logic zero.

It is evident that even significant changes (10% to 20%) in pulse widths associated with the input signals do not affect the transfer function appreciably. However, the logical output levels, V_0 and V_1, corresponding to logical zero and logical one, respectively, for stage Z5 will vary[1]

V_1 minimum $\geqq$ +2.4 volts

V_0 maximum $\leqq$ +0.4 volt

$\Delta V = (V_1 - V_0) > 2.0$ volts

4.5.4.3.4 Limiting Amplifier. - To obviate substantial changes in the transfer function due to changes in ΔV, the Shift Register Comparator is followed by a five-stage, inverting, limiting amplifier which provides:

a. amplification for the rectangular wave while preserving only its zero-crossings,

b. transfer to a new neutral voltage reference, approximately zero, and

c. improved clamping to stabilized voltage references (±12.0 V zeners), so that the fractional variation of ΔV (and the transfer constant) is substantially reduced.

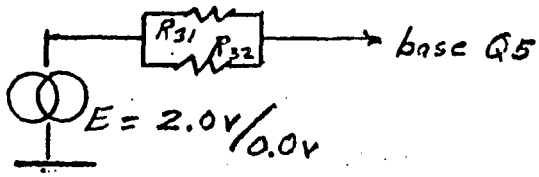
At the input to stage Q4, the limiting voltage thresholds derived from Z5 are adequate to saturate, or cut off, Q4 under worst case conditions. For a saturation collector current of

$$2 \text{ ma} = \frac{\text{20v supply (C13)}}{\text{10k collector load (R32)}}$$

a saturation collector potential less than 0.2 volt is assured when a base current exceeding 0.2 ma is available. The minimum logical one level is +2.4 volts behind

1 Specifications for SN5495 (-55° C to +125° C) (See Appendix E)

R30, 1k, a condition which exceeds these requirements for all operating temperatures[1]. Conversely, the maximum logical zero, +0.4 volt, will assure cut-off. Similar investigations for the characteristic of Q5 predict that the Thevenin's equivalent source,



is adequate for cut-off, or saturation, under worst-case conditions. Both Q4 and Q5 will conform to their desired operational characteristics with unregulated supply variations of ±25 percent (referred to positive and negative 22v sources with decoupling provided by C13 and C16).

Stage Q6 acts effectively as a limiting phase splitter to provide a positive-going, low-Z pull-up via Q7 and a negative-going, low-Z pull-down via Q8 with diode CR3 included to assure cut-off for Q7 during pull-down. These stages are relatively non-critical and effectively convert ΔV, the range of the comparator, to a nominal value of +12 - (-12) = 24 volts.

4.5.4.3.5 Worst Case Evaluations.

a. Maximum ΔV:

Maximum tolerance value VR1	+12.60 volts
Drop across R37	-0.53
CE drop across Q7	-0.20
Drop across CR3 (I = 4.4, T = 60°C)	-0.65
	+11.22 volts

[1] 2N2222A Characteristics. (Appendix E)

[2] 2N2907A Characteristics. (Appendix E)

Maximum tolerance value VR2	-12.60 volts
CE drop across Q8	+0.20
	-12.40 volts

ΔV maximum = 11.22 + 12.40 = 23.62 volts

b. Minimum ΔV:

Minimum tolerance value VR1	+11.40 volts
Drop across R37	-0.53
CE drop across Q7	-0.20
Drop across CR3 (I = 4.4, T = 0° C)	-0.78
	+10.09 volts
Minimum tolerance value VR2	-11.40 volts
CE drop across Q8	+0.20
	-11.20 volts

ΔV minimum = 10.09 + 11.20 = 21.29 volts

$$\varphi \text{ maximum} = \frac{V \text{ maximum}}{2\pi} = \frac{23.62}{2\pi} = 3.75 \text{ volts/radian} \quad (1)$$

$$\varphi \text{ minimum} = \frac{V \text{ minimum}}{2\pi} = \frac{21.29}{2\pi} = 3.40 \text{ volts/radian} \quad (2)$$

Summarizing the above, we have evaluated the limiting values for the phase comparator transfer function lumped together with the inverting limiter (corresponding to the transfer including stations 1 and 2 in Figure 4-124). The total anticipated variation is less than 0.9 dB for worst case limits for this section of the loop.

4.5.4.3.6 Incidental Drift. - Additionally, it is to be noted that if a small differential voltage develops as a result of unbalanced supply voltages, for example, and remains uncompensated because adjustments to R53 are no longer possible, the effect will be to reduce the dynamic range of the comparator -- the duty cycle will automatically adjust itself (at R38) to compensate for the fractional increment,

$$\frac{\Delta v}{\Delta V} = \frac{\text{unbalanced offset drift}}{24V}$$

Insofar as the useful range of control for the VCO involves a total increment of approximately 4 volts, or 16% of the total dynamic range associated with the phase comparator, there is a substantial margin for drift. Thus, small drift voltages will only contribute slightly to the asymmetry of the square wave at the comparator. These drift voltages are not nearly so significant as variations in the free-running frequency of the VCO -- at least, for the present configuration.

4.5.4.4 Voltage Controlled Oscillator (VCO)

4.5.4.4.1 Circuit Description. - The VCO, corresponding to station 6 in Figure 4-124, is devised as a self-triggering, one-shot network which includes an integrated circuit, Z8, with logic control levels; a feedback network including stages Q11 and Q12 to control an RC timing circuit; and a voltage comparator, Z7. An auxiliary loop around the one-shot, developed with stage Z4C, is included to assure a starting condition for the oscillator.

The period associated with the fundamental rate for the VCO is defined by two sub-intervals; thus,

$$T_{vco} = T_v + T_o$$

T_o is a quasi constant interval established by a stable combination of components (R_{68}, R_{69}, and C_{29}) used in conjunction with the one-shot network. T_v, on the other hand, is a variable interval of substantially shorter duration, which is effectively voltage-controlled by the error signal. This variable interval is defined by the time that it takes the voltage developed by C_{28} to decay (via R_{47}) to a level virtually equal to the error signal applied as a differential input to the comparator. At this instant the comparator senses equality, the one-shot is recycled, the interval, T_v, ends and the interval, T_o, begins.

4.5.4.4.2 Timing and Sensitivity Definitions. - Starting at a reference level of +4.1 volts and working to a negative reference of -11.7 volts, the timing waveform associated with the variable interval is

$$v(t) = E_\epsilon^{-t/R_{47}C_{28}} \qquad (1)$$

where $E = VR_9 - Q_{11}(\text{sat.}) - (-VR_8)$

Since this waveform is effectively intercepted by the error voltage soon after its start, we shall assume that its slope is linear with evaluation conveniently defined at t=0. Hence,

$$\left.\frac{dv(t)}{dt}\right]_{t=0} = -\frac{E}{R_{47}C_{28}} \tag{2}$$

The fundamental frequency component of the VCO is $\Omega v = 2\pi/T_{VCO} = 2\pi/T_V+T_O$ radians/second. A derivative function, $d\Omega v/dv_\epsilon$, is defined as the modulation sensitivity, M, in radians/second/volt; hence,

$$M = \frac{d\Omega v}{dv_\epsilon} = -\left[\frac{2\pi}{(T_V + T_O)^2}\right] \times \left[\frac{dT_V}{dV_\epsilon}\right] \tag{3}$$

It is clear that the second factor is simply the reciprocal expression of equation 2. Therefore,

$$M = \left[\frac{2\pi}{(T_V + T_O)^2}\right] \times \left[\frac{R_{47}C_{28}}{E}\right] \tag{4}$$

$$= 400 \text{ radians/second/volt (nominal)}$$

Once a phase lock is established, the denominator of the first factor is constant and equal to 0.001 second. With variations in T_O under worst-case analysis, T_V must compensate for these variations, and it is necessary to investigate the condition that T_O is properly bounded. Even so, the modulation sensitivity is evidently a function of limiting values for $R_{47}C_{28}$ and E.

This factor, M, provides a useful measure of VCO performance when the oscillator has reached its normal, unperturbed condition of operation. In this condition equilibrium implies that the fundamental frequency (1 kHz modified by a rational factor of 5/16) is precisely equal to that of the timing wheel over an indefinitely long period of time.

4.5.4.4.3 Positional Stability Factors. - The positional property of the VCO, previously described, is best illustrated by a graphical relationship shown in Figure 4-127. Here, the steady-state VCO frequency is related to its static control voltage,

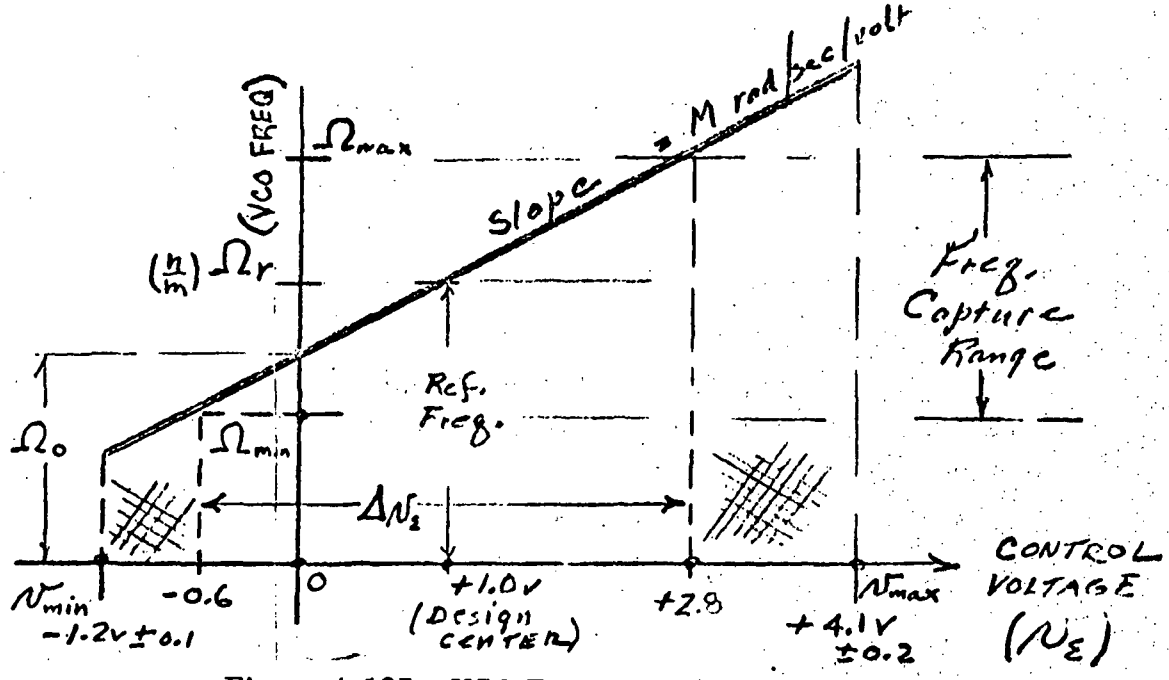


Figure 4-127. VCO Frequency as a Function of v_ϵ

v_ϵ, by simply integrating equation 3 to establish a linear relationship over a valid range of the error signal. Thus,

$$\frac{d\Omega v}{dv_\epsilon} = M \quad \text{and}$$

$$\Omega v = Mv_\epsilon + \Omega_o \qquad (5)$$

where V minimum < V < V maximum

Over a long term and under environmental influences, this characteristic may be expected to change, perhaps, in three respects: first, the sensitivity, slope M, may change; secondly, the limiting bounds for the control voltage (abscissa) may change; and finally, the characteristic may be translated in the direction of the ordinate. If the latter change occurs, for example, a free-running frequency drift is implied and is conveniently associated with variations in Ω_o; it is clear that the frequency capture range defined by Ωmaximum and Ωminimum may no longer straddle the desired reference frequency, Ω_{ref}, and may even exceed this value -- in which case a phase-lock is no longer possible.

The designer has provided stabilized, zener reference voltages committing the range of the error signal at the input to the comparator, Z7, (part of the VCO network) to v_{max} and v_{min}, as indicated in Figure 4-127. Worst case variations for these limits are dominately expressed by the initial tolerances for the zener voltages. A dead zone, indicated by the cross-hatched regions in the figure is also

provided to restrict the range of the error signal derived from Z6. Thus, a lower bound of -0.6 volt and an upper bound of +2.8 volts (correspondingly smaller than the limits v_{max} and v_{min} associated with the input to Z7) act in a compression network (diodes CR_4 and CR_5) to assure the condition that voltage comparison will always take place at the comparator, Z7. Hence, the VCO, once started, will not fail to operate for the lack of a recycling condition.

4.5.4.4.4 Worst-Case Analysis for Sensitivity. - With respect to the bounds for modulation sensitivity,

$$M = (2\pi)\ \frac{R_{47}C_{28}}{E} \times 10^6 \text{ radians/second/volt,}$$

we have the worst case for,

R_{47} 10,000 ppm (initial tolerance)

9,000 ppm (aging)

50 ppm x ΔT of 30° C 1,500 ppm (temperature)

20,500 ppm Δ_1

C_{28} 50,000 ppm (initial tolerance)

50,000 ppm (aging)

400 ppm x ΔT of 30° C 12,000 ppm (temperature range)

112,000 ppm Δ_2

simplifying with Δ_1 and Δ_2, the minimum value of the RC product is diminished by

$$(1.00 - 0.025)\ (1.000 - 0.112) = 0.87$$

Evaluation for the maximum (worst case) value of E (the timing voltage)

12.78 volts (maximum initial value VR_8)

$\frac{0.12 \text{ volt}}{12.90 \text{ volts}}$ (350 ppm x ΔT of 30° C)

4.51 volts (maximum initial value, VR_9)

$\frac{0.04 \text{ volt}}{4.55 \text{ volts}}$ (300 ppm x ΔT of 30° C)

Therefore, $E_{max} = 12.90 + 4.55 - 0.2$ (Q11 saturation)

$$E_{max} = 17.25 \text{ volts}$$

Hence, the worst case minimum value of M is

$$M_{min} = \frac{R_{47} \text{ min. x } C_{28} \text{ min.}}{E_{max}} (2\pi) \times 10^6 \text{ radians/second/volt}$$

$$M_{min} = \frac{2\pi \times 4640 \times 0.22 \times 0.87}{17.25}$$

$$M_{min} = 325 \text{ radians/second/volt}$$

4.5.4.4.5 Worst Case Analysis for Drift and Capture Range. - The free-running drift is evaluated by assuming that the uncontrolled segment of the VCO period is dominant. No assignments are made for initial tolerances with respect to the principal timing components, R_{68}, R_{69}, C_{29}, the reference bias developed by VR_4, or the initial activity of the IC one-shot (Z8). These variances are all compensated by an initial pre-set adjustment for R_{69}, and it is assumed that the design-center value for the steady-state error voltage (approximately +1.0 volt at TJ3) is developed.

However, aging and temperature variations remain effective; these are evaluated as follows:

R_{69} (as a rheostat):

75,000 ppm x (1/5) weighting ⟶ 15,000 ppm (aging)

R_{68}:

9,000 ppm x (4/5) weighting ⟶ 7,000 ppm (aging)
50 ppm x T = 30° C ⟶ 1,500 ppm (temp.)

$\Delta_1 = 23,500$ ppm

C_{29}:

400 ppm x ΔT = 30° C — 12,000 ppm (temp.)
50,000 ppm (aging)

$\Delta_2 = 62,000$ ppm

Hence, the minimum Capture Range is

$$\text{Capture Range}_{min} = 1.55 \times 325$$

$$= 500 \text{ radians/second}$$

The worst case frequency drift, therefore, exceeds the worst case capture range. However, the difference is not significant and can be easily remedied in a number of ways. For example, the sensitivity factor may be augmented by appropriate changes in R_{47}.

4.5.4.4.6 Summary of Positional Stability. - Summarizing the above discussions, we have examined the worst case conditions relating to the positional stability of the VCO from the standpoints of

a. free-running drift,

b. modulation sensitivity variations, and

c. control voltage variations.

One may conclude that the design for the VCO is inherently sound. While a deficiency has been discovered, an appropriate remedy is very simply implemented.

4.5.4.4.7 Dynamic Transfer Factor. - When the VCO is operating in the steady-state condition with a phase-lock established, one may conceive an arbitrarily small increment in the error voltage, v_ϵ. The immediate effect is to produce a phase transient in the VCO output, and a new sensitivity transfer factor, η, is defined; this has a dimensionality of radians/volt, and not radians/second/volt. The latter dimension is associated with M and the presumption for steady-state operation, but not for transient operation.

Thus, η is a useful coefficient which is identified with the transfer function of the VCO and used in loop analysis with a time-dependent error signal. It must be dimensionally reciprocal with φ, the transfer factor associated with the phase comparator, since all other transfer functions within the transport servo loop are defined as dimensionless ratios.

η is evaluated by the following expression,

$$\eta = \left(\frac{dt}{dv_\epsilon}\right)\left(\frac{2\pi}{T_v + T_o}\right) \quad \text{radians/volt}$$

Z8 activity[1]:	1,000 ppm x $\Delta T = 30^\circ C$	3,000 ppm (temp.)
		10,000 ppm (aging)
	(Variations with bias at VR_4 and 300 ppm/° C are not significant.)	--- ppm (VR_4)
	$\Delta_3 = 13{,}000$ ppm	

For simplification, add Δ's:

$$\Delta_1 + \Delta_2 + \Delta_3 = 9.8\%$$

Since the nominal operating frequency is 6,280 radians/second, the worst case drift is

$$0.098 \times 6280 = \underline{615} \text{ radians/second}$$

This value of frequency drift must remain less than the worst-case (minimum value in this instance) capture-range, expressed by

$$\left[\frac{\Delta v_\epsilon}{2}\right]_{min} \times M_{min} = \text{Capture Range (minimum)}$$

The quantity Δv_ϵ may be regarded as the available error voltage range present at the output of Z6 which is compressed by the action of diodes CR_4 and CR_5; the factor 1/2 assumes that the operator has preset the initial VCO frequency to its optimum design-center value (R69). With a minimum drop of 0.65 volt assumed for each diode (at $T_{max} = +60^\circ C$) and a worst case potential developed at R65 of +1.8 volts, we have

$$\frac{\Delta v_\epsilon}{2} = \frac{(2 \times 0.65 \times 1.8)}{2} = \underline{1.55} \text{ volts}$$

where

$$VR_{65_{min}} = VR_{1_{min}} \left(\frac{R_{65_{min}}}{R_{64_{min}} + R_{65_{min}}}\right) = 11.70 \left(\frac{200}{1100 \times 200}\right)$$

[1] See Appendix E (Figures J and K for SN54121N)

or,

$$\eta = (2\pi)\ \frac{R_{47}C_{28}}{E_{nom}} \times 10^{3} = 0.4 \text{ radian/volt (nominal)} \tag{6}$$

$$\eta_{max} = \frac{2\pi \times 4640 \times 0.22 \times (1.14)}{(11.00 + 4.05 - 0.20)} = 0.496 \text{ radian/volt} \tag{6a}$$

$$\text{WORST CASE} \begin{cases} \eta_{max} = 0.496 \text{ radian/volt;} \\ \eta_{max} = 0.325 \text{ radian/volt} \end{cases} \tag{6b}$$

4.5.4.4.7 Frequency Translation Factor. - The frequency of the VCO is effectively translated from 1,000 Hz (6288 radians/second) to 312.5 Hz (1965 radians/second) which corresponds to the fundamental component of the control-track signal. The ratio of these two frequencies is a rational fraction, 5/16, so that the translation is conceptually a simple problem either in frequency synthesis, or appropriate mechanical gearing associated with the capstan drive. The important points to note, however, are that:

a. the relationship between the VCO frequency and that of the timing wheel (or, equivalently, the control track signal) must be rational if a phase lock is to be established;* and

b. if this translation factor is less than unity (downward translation), the loop gain is diminished precisely by the same factor; the converse condition applies, of course, if the system had been designed differently.

The first point follows because of the intrinsic nature of a phase-lock, and the second point follows because the rate of digital information accumulated at the phase comparator is occurring more slowly than the epochal rate of the VCO signal. To appreciate this condition more fully, it is clearly evident with a hypothetical case that it requires ten times less correction if the correction is introduced ten times more frequently -- which is simply stating the condition for loop gain in another sense.

4.5.4.4.8 Worst Case Gain and Transfer Function Summary

$$H_0 = \eta \times \varphi \times \left(\frac{m}{n}\right) \tag{7}$$

$$H_{0_{max}} = 0.496 \times 3.75 \times \frac{5}{16} = 0.582 \tag{7a}$$

*True only if there is no tape-slippage at the capstan.

$$H_{0_{min}} = 0.325 \times 3.40 \times \frac{5}{16} = 0.346 \quad (7b)$$

The subscript, 0, is introduced to identify this gain factor with the other dimensionless transfer functions:

a. $H_1(j\omega)$ - (associated with the accumulated filter functions comprised of electrical circuit components in the servo amplifier)

b. $H_2(j\omega)$ - (associated with the transient phase response of the capstan drive motor)

c. $H_3(j\omega)$ - (associated with the transient phase response of the tape transport mechanism)

d. $H_4(j\omega)$ - (associated with the transient phase response of the drop-out BPF which precedes the comparator)

Thus, the overall, open-loop system function is:

$$G_{(j\omega)} = H_0 \cdot H_1(j\omega) \cdot H_2(j\omega) \cdot H_3(j\omega) \cdot H_4(j\omega) \quad (8)$$

for which only H_0, defined above, is <u>independent</u> of the error signal spectrum, $j\omega$.

The characteristics and a worst case analysis for $H_1(j\omega)$ and $H_4(j\omega)$ are developed in the following paragraphs. $H_2(j\omega)$ and $H_3(j\omega)$ are not considered, but have been thoroughly analyzed elsewhere.

4.5.4.5 <u>Cumulative Error Voltage Filter.</u> -

4.5.4.5.1 <u>Sub-factors of $H_1(j\omega)$.</u> - In the previous sections, a cumulative filter function expressed as an output/input dimensionless voltage ratio, has been described. This function relates to all of the intervening circuitry between the phase comparator and VCO functions, depicted as station 3 in Figure 4-127, and symbolized as $H_1(j\omega)$.

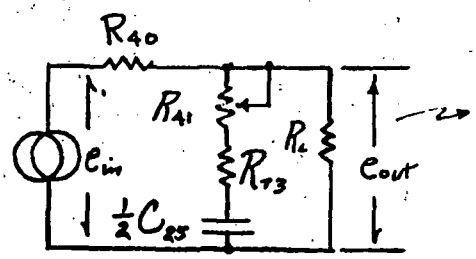
It is convenient to express

$$H_1(j\omega) = \left[A_1(\omega) \cdot \epsilon^{jx_1(\omega)}\right] \cdot \left[A_2(\omega) \cdot \epsilon^{jx_2(\omega)}\right] \cdot \left[A_3(\omega) \cdot \epsilon^{jx_3(\omega)}\right] \quad (1)$$

where the three factors on the right side are identifiable with particular circuit segments and are in the form for which the <u>magnitudes</u> and the lag <u>angle</u> arguments are explicit. The network is designed such that at particular nodes a substantial impedance mismatch exists. This condition validates the engineering approximation for

relatively simple cascaded functions implied by equation 1, rather than mutually coupled functions which would result in a more complex expression. Thus, the factor, $\left[A_1(\omega) \cdot \epsilon^{jx_1(\omega)}\right]$, is identified with the voltage transfer ratio relating the collector of Q8 to the emitter of Q10, as shown in Figure 4.-128.

The factor $\left[A_2(\omega) \cdot \epsilon^{jx_2(\omega)}\right]$ is identified with the transfer ratio relating the emitter of Q10 to the output node of the operational amplifier, Z6, as shown in Figure 4-129.



where $R_L = h_{FEQ10}\left(R_{56} /\!/ R_{57}\right)$

and $300 < h_{FE}Q10 < 900$

$$\frac{e_{out}}{e_{in}} = A_1 \frac{(S+S_{01})}{(S+S_{p1})} = \left[\frac{(R_{41}+R_{73})}{R_{40}}\right] \cdot \left[\frac{S + \left(\frac{1}{[R_{41}+R_{73}]\cdot\frac{1}{2}C_{25}}\right)}{S + \left(\frac{1}{\left(\frac{R_{40}R_L}{R_{40}+R_L}\right)\cdot\frac{1}{2}C_{25}}\right)}\right]$$

$S = j\omega$

Nom. Values:

$R_{40} = 10^6\,\Omega$

$R_{41(max)} = 10^4\,\Omega$

$R_{73} = 6.2\times10^3\,\Omega$

$\frac{1}{2}C_{25} = 19.5\times10^{-6}\,fd$

$2.5\times10^6\,\Omega < R_L < 7.5\times10^6\,\Omega$

Figure 4-128. Transfer Function, Q8 to Q10.

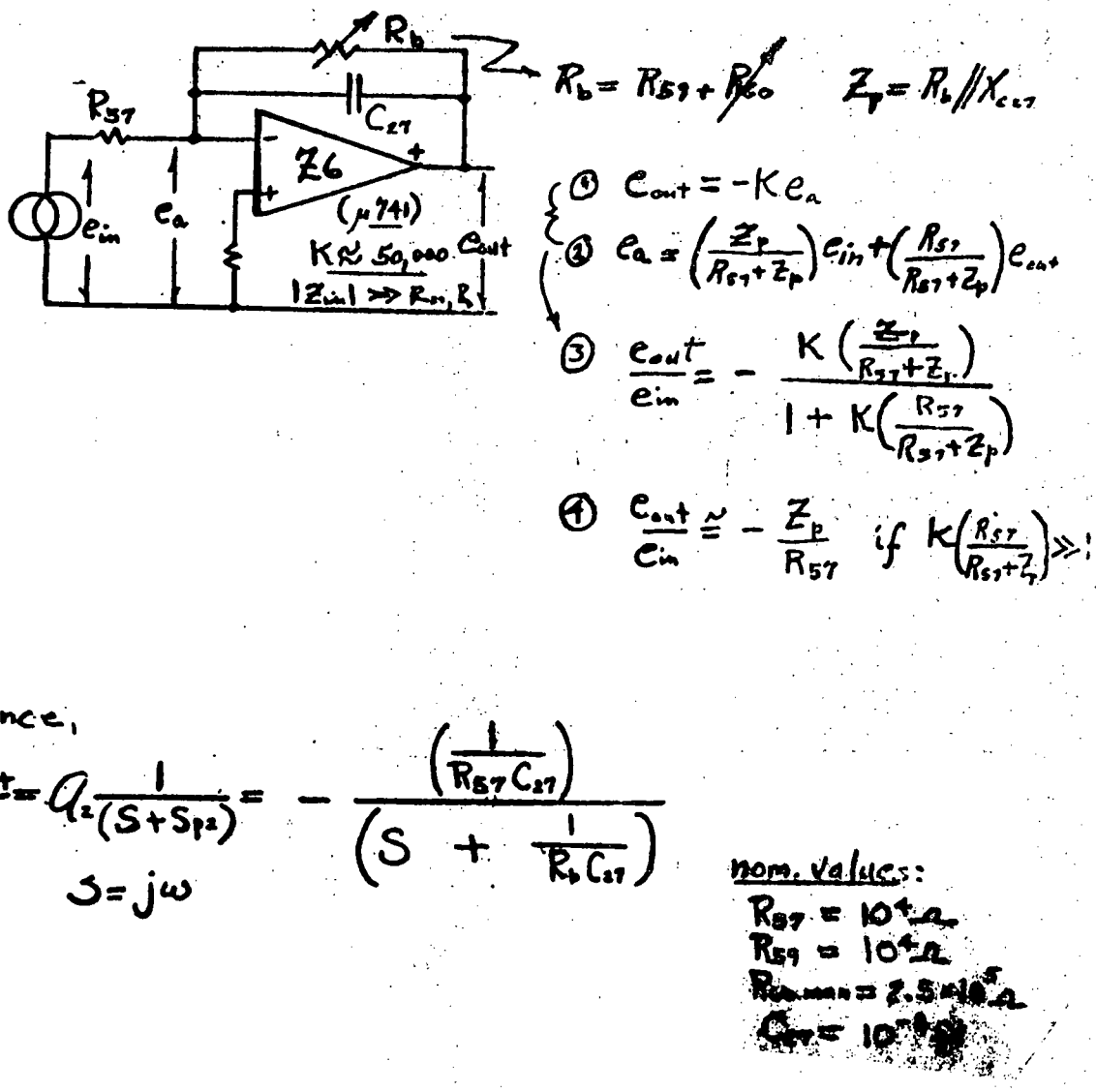


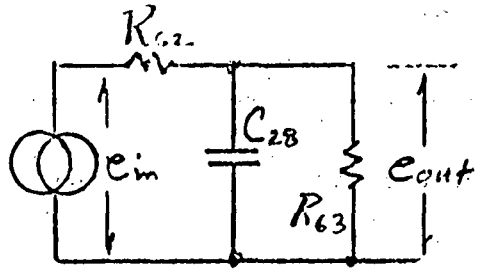
Figure 4-129. Transfer Function from Q10 to Z6

The factor $\left[A_3(\omega) \cdot \epsilon^{jx_3(\omega)}\right]$ is identified with the transfer ratio relating the output node of Z6 to the input of the VCO comparator, Z7, as shown in Figure 4-130. Terminal loading by Z7 and Q9 is not significant and may be absorbed in the assignment for R63.

4.5.4.5.2 Development of Magnitude Increments. - Returning to equation 1 of Paragraph 4.5.4.5.1, we may develop each of the magnitude factors, as follows:

$$A_1(s)\Big]_{s=j\omega} \longrightarrow A_1(\omega, X_i) = A_1(X_i) \left[\frac{(\omega^2 + S_{o1}^2(X_i))^{1/2}}{(\omega^2 + S_{p1}^2(X_i))^{1/2}}\right] = A_1\left(\frac{N_1^{1/2}}{D_1^{1/2}}\right) \quad (2)$$

$$\frac{\partial A_1(\omega, X_i)}{X_i} = \left(\frac{\partial A_1}{\partial X_i}\right)\left(\frac{N_1^{1/2}}{D_1^{1/2}}\right) + \left(\frac{A_1}{N_1^{1/2} D_1^{1/2}}\right)\left(S_{o1}\right)\left(\frac{\partial S_{o1}}{\partial X_i}\right) - \left(\frac{A_1 N_1^{1/2}}{D_1^{3/2}}\right)\left(S_{p1}\right)\left(\frac{\partial S_{p1}}{\partial X_i}\right) \quad (3)$$



$$\frac{e_{out}}{e_{in}} = q_3 \frac{1}{(S + S_{p3})} = \left(\frac{1}{R_{62} C_{28}}\right) \cdot \left[\frac{1}{\left(S + \frac{1}{\left(\frac{R_{62} R_{63}}{R_{62} + R_{63}}\right) C_{28}}\right)}\right]$$

$S = j\omega$

nom. values:

$R_{62} = 10^4 \Omega$

$R_{63} = 10^4 \Omega$

$C_{28} = 10^{-6}$ fd

Figure 4-130. Transfer Function Z6 to Z7

Let $$\frac{\partial A_1(\omega, X_i)}{\partial X_i} = \gamma_{i1} \tag{3a}$$

then, $$\Delta A_{i1} = (\gamma_{i1}) \cdot (\Delta X_{i1})$$

$$\Delta A_{i2} = (\gamma_{i2}) \cdot (\Delta X_{i2}) \tag{4}$$

$$\Delta A_{i3} = (\gamma_{i3}) \cdot (\Delta X_{i3})$$

or, in total

$$\Delta|H_1| = \sum_i \sum_j (\gamma_{ij})\,(\Delta X_{ij}) \tag{5}$$

where i is an index associated with each component, X_i, typically 3 or 4 resistors, or capacitors for each factor in equation 1; j is the index associated with each factor in equation 1 (j = 1, 2, and 3).

From the standpoint of worst case condition, each increment in the magnitude function due to an increment for any component will tend to augment this function if criterion for loop stability is to be determined. Thus, ΔX_i (the worst case increment ostensibly known for each component) will assume the same sign as the associated derivative function. This results in the condition that

$$\Delta A_{ij} > 0 \quad \text{for all} \quad X_{ij}$$

and, therefore, in the maximization of the total magnitude increment, $\Delta|H_1|$ (equations 4 and 5.

In the first iteration for the derivative, γ_{ij}, nominal values for X_{ij} are used to evaluate this quantity. With a second iteration, the worst-case values, $(X_{ij} + \Delta X_{ij})$, or $(X_{ij} - \Delta X_{ij})$ are now known and may be used to improve the accuracy for the determination of ΔA_{ij}.

The success of this approach depends not only on the knowledge of "nominal" component values, but also on the a priori determination of ω_θ, the frequency at which the total phase-lag angle has reached π radians for the total system function, $G(j\omega) = H_0 \cdot H_1(j\omega) \cdot H_2(j\omega) \cdot H_3(j\omega) \cdot H_4(j\omega)$, also determined with nominal values. Hence, the magnitude margin of stability for the worst case development of all components is established with a straightforward evaluation of numeric values, only, of equations 3, 4, and 5.

If the value for ω_θ were, otherwise, not determinable, each derivative function, $(\partial A_{ij}/\partial X_{ij})$, would be a variable function of ω, and the task for optimization would, indeed, be much more ponderable.

The same remarks apply to the worst-case development for the lag-angle function, examined in the next section. In this instance it is necessary to set $\omega = \omega_T$, or that frequency at which the total system develops a transmission magnitude of unity, to establish the worst-case conditions for phase margin stability.

4.5.4.5.3 Development of Lag-Angle Increments. - As in the previous section, we return to the expression for a particular factor of $H_1(j\omega)$ to establish the derivative function for the lag-angle with respect to a change in any component, X_i.

The lag-angle associated with the first factor is

$$\alpha_1 (\omega, Xi_1) = \theta_{01} (\omega, Xi) - \theta_{P1} (\omega, Xi) \tag{6}$$

in which θ_{01} is the angle associated with a zero vector and θ_{P1} is the angle associated with a pole vector. Defined in this context, the lag-angle accumulates with $\alpha < 0$, and in the worst case concept, negative increments, $\Delta\alpha$, are determined for each increment, ΔXi. The derivatives are now defined:

$$\frac{\partial \alpha_1}{\partial Xi_1} = \frac{\partial \theta_{01}}{\partial Xi_1} - \frac{\partial \theta_{p1}}{\partial Xi_1} \tag{7}$$

$$\frac{\partial \alpha_1}{\partial Xi_1} = \left[\cos^2 \left(\frac{\omega}{S_{01}}\right)\right] \cdot \left[\frac{\omega}{S_{01}^2}\right] \cdot \left[\frac{\partial S_{01}}{\partial Xi_1}\right] + \left[\cos^2 \left(\frac{\omega}{S_{P1}}\right)\right] \cdot \left[\frac{\omega}{S_{P1}^2}\right] \cdot \left[\frac{\partial S_{P1}}{\partial Xi_1}\right] \tag{8}$$

Let $$\frac{\partial \alpha_1}{\partial Xi_1} = \beta_{i1} \tag{8a}$$

then, $\Delta\alpha_{i1} = (\beta_{i1}) \cdot (\Delta X_{i1})$, etc.

and the total lag-angle increment for $H_1(j\omega)$ is

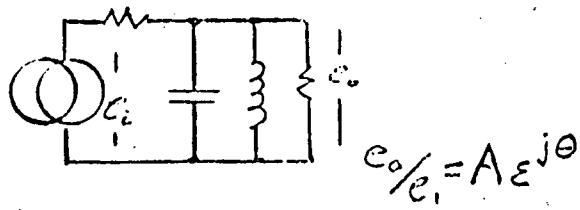
$$\sum_i \sum_j (\beta_{ij}) \cdot (\Delta X_{ij}) \tag{9}$$

4.5.4.5.4 Drop-Out Filter Evaluation. - When the control track signal, developed by the playback head, is injected into the servo amplifier, it is regenerated as a rectangular signal by a one-shot, stage Z1. The duty cycle may be modified by a timing adjustment at this stage so that the control track may be advanced or retarded with respect to the tone wheel signal. The registration between the two signals may be observed visually, or by means of an external comparison meter suggested by station 11, Figure 4-124, but there is no conceptual tie-in with the principal loop. Also, since there is no differential group delay associated with this adjustment, it has no effect whatever on the characteristics of the loop.

The same conditions do not apply, however, to the drop-out filter which succeeds stage Z1 (station 12, Figure 4-124). It is to be noted that at this point in the servo system, the error signal has effectively been transformed from deviations in the voltage domain to deviations in the frequency domain. Amplitude variations, therefore, have little direct meaning, unless they are so sizable that limiting and threshold deficiencies develop. However, the differential group delay characteristic is important. When properly tuned, this narrow band pass network may be expected not to compromise the stability of the system; but when detuned, its effect on the system must be investigated.

Our purpose is to convert this function, $H_4(j\omega)$, in such a way that it is effectively transformed to a low pass equivalent lag pole with unity transfer. In this context it is then directly associable with the vectors previously evaluated for $H_1(j\omega)$ on the negative axis of reals of the complex plane. Evidently, its relative proximity to the origin is an undesirable condition, affecting system stability; this is aggravated in some sense by high Q and the degree to which it is detuned.

For a single-pole resonator, the lag angle, θ, for the narrow band case is implicitly related to the loaded Q and resonant frequency, ω_o, as follows:



$$\tan\theta = Q\left[1 - \left(\frac{\omega_o}{\omega}\right)^2\right] \qquad (1)$$

in which Q for this approximation is not a function of ω, and ω does not differ substantially from ω_o. The group delay is

$$t_d = \frac{d\theta}{d\omega} = 2Q\frac{\omega_o^2}{\omega^3}\left[\frac{1}{1+\tan^2\theta}\right] \qquad (2)$$

and the differential group delay is

$$\Delta t_d = \left(\frac{d^2\theta}{d\omega^2}\right) \cdot \Delta\omega \quad \text{seconds} \tag{3}$$

where $\Delta\omega$ is regarded as a small tuning error. If the band pass network is to have a low pass transformation with unity transfer and a lag pole of the form, $S_o/S + S_o$, then this is equivalent to stating that

$$S_o = \frac{\pi}{4}\left(\frac{1}{\Delta t_d}\right) \quad \text{radians/second} \tag{4}$$

or,

$$S_o = \frac{\pi}{4}\left[\frac{1}{\Delta\omega \cdot \left(\frac{d^2\theta}{d\omega^2}\right)}\right]$$

Evaluating

$$\frac{d^2\theta}{d\omega^2},$$

$$\frac{d^2\theta}{d\omega^2} = -\frac{2Q}{\omega^2}\left(\frac{\left(\frac{\omega_o}{\omega}\right)^4}{1+\tan^2\theta}\right)\left(3\left(\frac{\omega}{\omega_o}\right)^2 + 4Q\,\frac{\tan\theta}{1+\tan^2\theta}\right) \tag{5}$$

$(\omega_o = 2\pi \times 312.5)$

From equations 4 and 5 we have, by a simple artifice, established a lag pole which is effectively variable with a tuning error implied by a selection for ω versus ω_o, or equivalently, $\Delta\omega = (\omega \pm \omega_o)$. The approximations in the development appear valid for the purposes of predicating a vector which may affect the stability of the system.

4.5.4.5.5 Tabulation of Components and Summary. - A tabulation of all components affecting $H_1(j\omega)$ is provided in Table 4-39. With the entry of nominal values in the expressions for the derivative functions developed for phase lag and magnitude in paragraphs 4.5.4.5.2 and 4.5.4.5.3, the increments by which phase margin and magnitude margin are diminished (correspondingly to the worst case

TABLE 4-39. COMPONENTS AFFECTING $H_i(j\omega)$

Symbol Number	Nominal Value (X_i)	Initial Tolerance (ppm)	Temperature Variable (for $\Delta T = 30^\circ$ C ppm)	Aging Variable (ppm)	ΔX_i*
R40	1 Meg.	50,000	30,000	100,000	120k
R41 (max.)	10k (max.)	50,000	1,500	70,000	1,100
R73	6,200	50,000	20,000	50,000	740
C25/C31	19.5 uF	100,000	100,000	50,000	5.2 uF
RL (h_{FE}Q10)	5 Meg.	¢ 2.5 Meg. h_{FE}(300-900)	10,000	50,000	2.5 Meg.
R57	10k	50,000	20,000	50,000	1,200
R59	10k	50,000	20,000	50,000	1,200
R60 (max.)	250k (max.)	50,000	7,500	70,000	35k
C27	10,000 pF	50,000	10,000	50,000	1,200 pF
R62	10k	50,000	20,000	50,000	1,200
R63	10k	50,000	20,000	50,000	1,200
C28	10 uF	100,000	50,000	50,000	2.6 uF

*¢Value which gives worst combination.

choice for the component increments) is now determinable at the critical frequencies. Iterations may be included to improve accuracy.

Appendix E determines the proper sign of the drift of the various components if the critical frequency is approximately 8 Hz, which is the lowest frequency at which the mechanical portion of the servo loop will tend to resonate. Using a computer simulation of the electrical and mechanical elements in the complete servo loop, the transient response of this system has been evaluated. This data is summarized in Figure 4-131. Plot 43 (sheet 1 of the figure) summarizes the response of the system under nominal operating conditions. Note that the system has some overshoot, but it has reached steady state values within 1 second. Plot 44 (sheet 2) shows the performance of the system assuming all components have drifted into the worst possible direction and by the maximum expected amount (drift, rather than misadjustments of potentiometers, has been assumed). Even under these conditions, the servo system is stable. Plot 45 (sheet 3) shows the performance when all components have drifted in the direction opposite to that shown in plot 44. The servo system is very well damped.

In summary, worst case drift problems will keep the servo system in satisfactory operating conditions. The major response characteristics of the servo are controlled by potentiometer R41 (branch 51 on the computer run-off) which sould normally be set to give a transient response falling between plots 43 and 45 (sheets 1 and 3, respectively).

4.5.5 Headwheel Damper Circuit Worst Case Analysis. - The Headwheel Damper Circuit has been analyzed to ensure satisfactory operation under the worst case operating conditions of the ERTS recorder. Circuit performance limitations due to changes in circuit components caused by manufacturer's tolerances, temperature changes and aging were determined.

4.5.5.1 Summary. - If no changes are made in the original components selected, Damper Circuit performance is questionable under worst case conditions. For example, T_1/T_2 is supposed to remain much less than one. However, using the original components, $T_1/T_2 = 0.175$ under worst case conditions. In addition, $(U/T_1)_{min.} = 0.312$ and $(U/T_1)_{max.} = 1.13$ under worst case conditions.

Using the recommended component values shown in Appendix A, the Damper Circuit will perform as intender under worst case conditions. With the recommended values, $(T_1/T_2)_{max.} = 0.052$ (worst case). Also, $(U/T_1)_{min.} = 0.372$ and $(U/T_1)_{max.} = 0.9$ under worst case conditions. These extremes are within the design requirements determined by the computer analysis of the closed loop system.

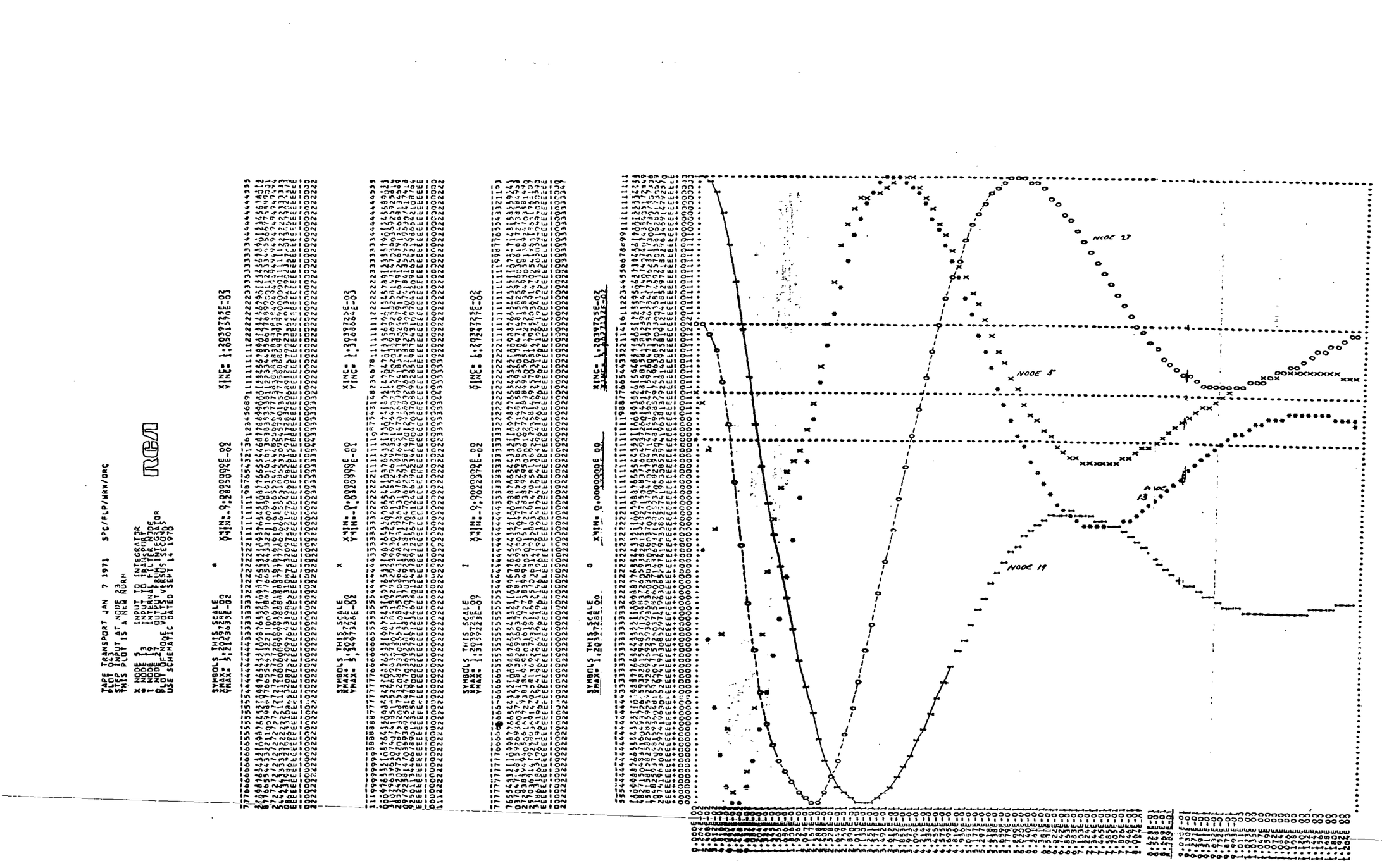


Figure 4-131. System Transient Response
(Sheet 1 of 3)

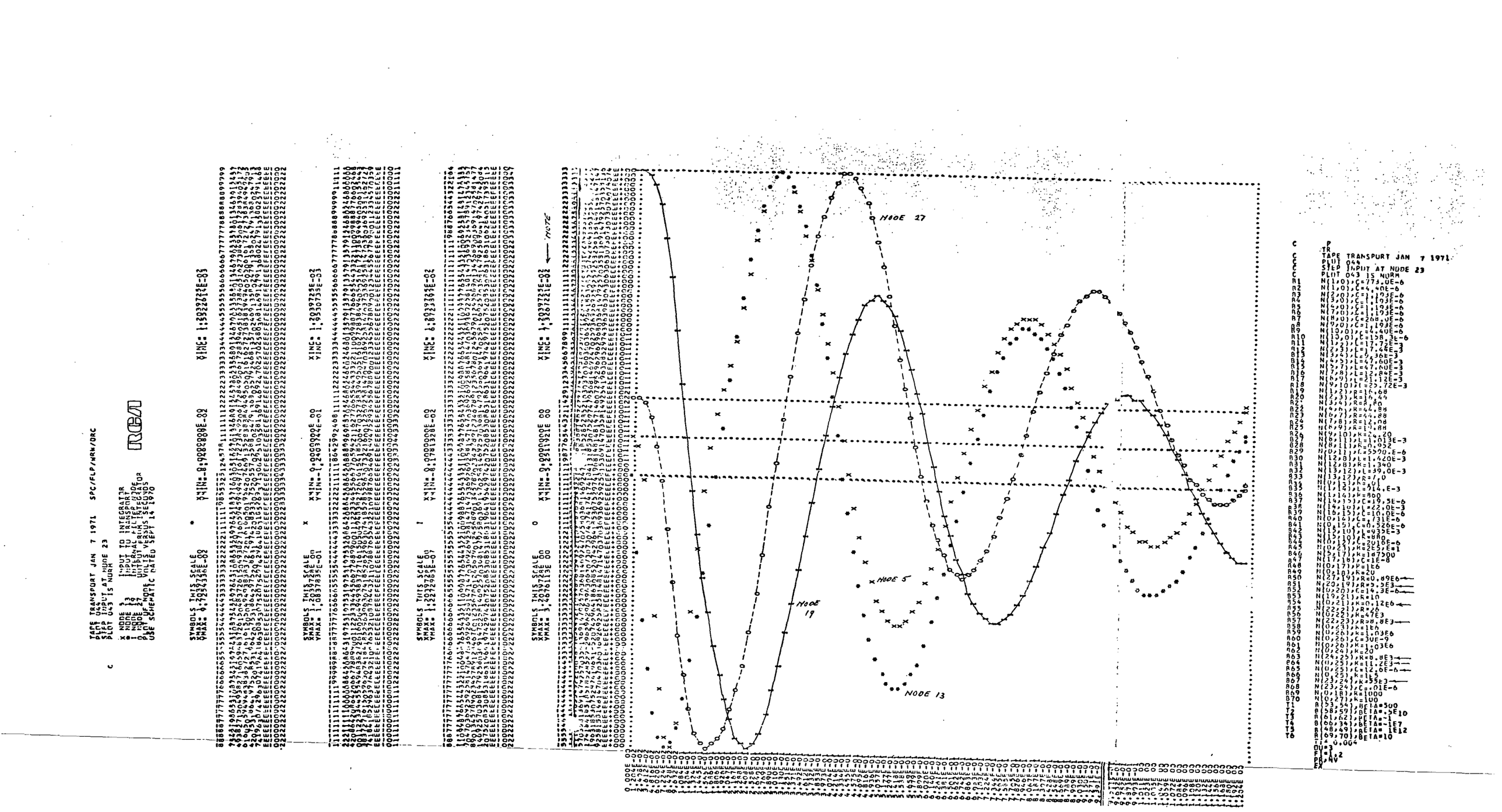


Figure 4-131. System Transient Response
(Sheet 2 of 3)

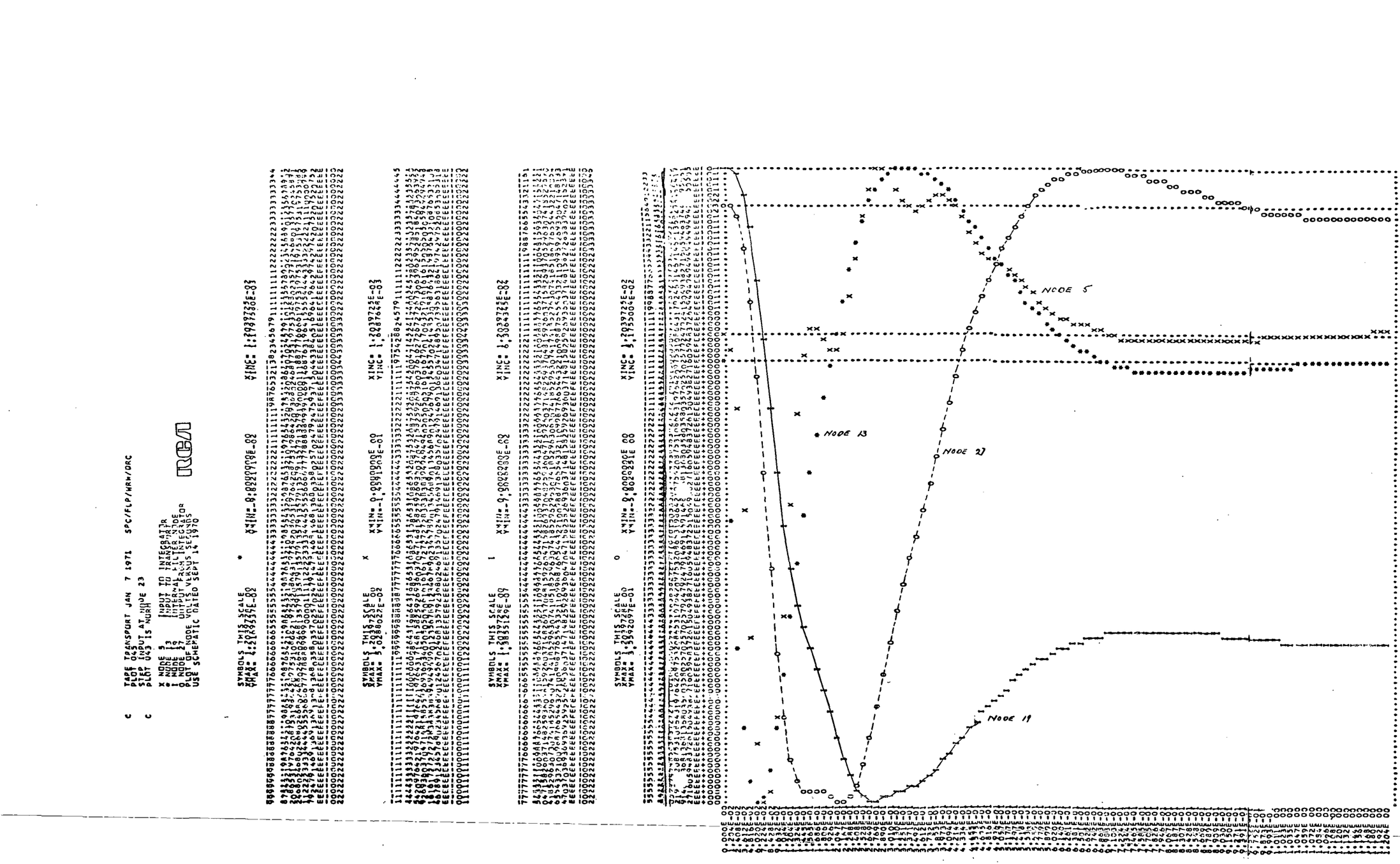


Figure 4-131. System Transient Response
(Sheet 3 of 3)

4.5.5.2 Symbols

a. Transistor Parameters. -

V_C, V_B, V_E - dc voltages at collector, base and emitter, respectively.

I_C, I_B, I_E - dc currents in collector, base and emitter, respectively.

$\beta (h_{fe})$ - small signal beta or current transfer ratio.

h_{ie} - intrinsic input impedance of transistor.

A_V - voltage amplification of transistor.

b. Headwheel Damping Loop Parameters

The parameters and their significance are given in Figure 4-121.

c. Diodes

V_{VRN} - breakdown voltage of zener diode n.

I_{VRN} - reverse dc current of zener diode n.

P_{DVRN} - power dissipation in zener diode n.

4.5.5.3 Worst Case Analysis. - The revised Damper Circuit is shown in Figure 4-122. The following analysis reflects circuit performance based on the recommended component changes listed in Appendix A. The component and parameter derating (Tables 4-40 and 4-41) applies to 10,000 hour aging over an ambient temperature range from 0°C to 60°C. Derating specified by Mil standards was applied when available; otherwise, derating information obtained from RCA Standards and device manufacturers was applied. These parameter derating guidelines are considered to be applicable to the worst case requirements of the ERTS recorder.

a. Circuit Elements. - Drift of the major circuit elements will have an effect on the two main Damper Circuit figures of merit, T_1/T_2 and U/T_1. The drift of each circuit element under worst case conditions will be computed in this section. Application of the circuit parameter variations to the figures of merit, T_1/T_2 and U/T_1, is contained in Paragraphs 4.5.5.3 a, b and c respectively.

TABLE 4-40. PASSIVE ELEMENT DERATING FACTORS

Type	Tolerance (%)		Temp. Char. (%)		Power Derating (%)
	Initial	Initial Plus 10,000 Hrs.	0°C	60°C	
RNR-XXC-FP -XXE-FP Resistors	±1 ±1	±1.9 ±1.9	±0.125 ±0.063	±0.175 ±0.088	50
RJ24CX Resistors	±10	Rheo. ±17	±0.625	±0.875	
RLRXXC-JP Resistors	±5	±9	±0.5	±0.7	
RER65FR Resistors	±1	±3	±0.25	±0.35	
CK06BX-K Capacitors -M	±10 ±20	+20, -30 +40, -50	+15 -55°C to 125°C		
CH09A3RA Capacitors J	±5	+5, -10	-2.7	+2.5 -1.5	
CQ09A1MC Capacitors J3	±5	±5.5	±2 (0°C to 70°C)		
CSR - Capacitors	±10	±30	-3.3	+4.7	

1. Transformer Circuit. - Variations in transformer parameters change the effective mutual inductance, M_{eff}, which affects the overall loop gain, U. The effective mutual inductance, M_{eff} = 1.1 mH was measured experimentally. M_{eff} in terms of the transformer circuit parameters of Figure 4-122 is defined as:

$$M_{eff} = \frac{V_{sec}}{\omega I_p}\left(\frac{I_p}{I_M}\right) = \frac{V_{sec}}{\omega I_M}$$

TABLE 4-41. TRANSISTOR PARAMETER DURATION

Parameter	Derating Factor
I_{CBO}	Double every 14°C rise in junction temperature for Germanium. Double every 10°C rise in junction temperature for Silicon. Derate 100% for aging.
V_{BE} (sat)	Decrease 2.5 mV/°C rise in junction temperature. Derate 10% for aging (increase maximum). Derate typical ±20%.
V_{CE} (sat)	Increase 0.2-0.5 mV/°C rise in junction temperature. Derate 10% for aging (increase maximum). Derate typical ±50%.
h_{FE}	Derate 50% of +25°C value for -55°C. $\frac{25}{80} \times 50 = \frac{125}{8} = 16\%$ Derate 25% for aging (power rating <1 watt). 16 + 25 = 41°6 Derate 30% for aging (power rating ≥1 watt).
f_t	Gain Bandwidth, Decrease minimum 25%

The current ratio,

$$\frac{I_p}{I_M} = \frac{R16}{R35 + R_{T1} + R16}$$

where R_{T1} is the dc resistance of the transformer.

R_{T1} (measured) = 4.7 ohms

Using nominal values, $M_{eff} = \frac{V_{sec}}{\omega I_p}\left(\frac{I_p}{I_M}\right)$

$$\frac{V_{sec}}{\omega I_p} = M_{eff}\left(\frac{I_M}{I_p}\right) = 1.1\left(\frac{8.25 + 4.7 + 0.1}{0.1}\right) = 0.96 \text{ H}$$

Under worst case conditions of aging and temperature,

$$(M_{eff})_{max.} = \left(\frac{V_{sec}}{\omega I_p}\right)^*_{max.} \left(\frac{I_p}{I_M}\right)_{max.}$$

$$= (0.98)\left(\frac{.1024}{81.61 + 4.28 + .1024}\right) = 1.17 \text{ mH}$$

$$(M_{eff})_{min.} = \left(\frac{V_{sec}}{\omega I_p}\right)^*_{min.} \left(\frac{I_p}{I_M}\right)_{min.} =$$

$$= (0.94)\left(\frac{.0976}{83.39 + 5.8 + .0976}\right) = 1.03 \text{ mH}$$

2. Amplifiers. - The gain, K, which is part of the loop gain, U, is defined from Figure 4-122 as the voltage gain from the input of amplifier U5 to the output of amplifier U6. Therefore,

$$K = (\text{Gain, U5})(\text{Loss of R40-R41})(\text{Gain, U6})$$

$$= \left(1 + \frac{R_{39}}{R_{38}}\right)\left(\frac{R_{41}}{R_{40} + R_{41}}\right)\left(1 + \frac{R_{43}}{R_{42}}\right)$$

Using nominal values,

$$K = \left(1 + \frac{67.5k}{18.2k}\right)\left(\frac{150}{150 + 150}\right)\left(1 + \frac{3.74k}{150}\right) = 61$$

Using worst case values,

$$K_{max.} = \left(1 + \frac{72.82k}{18.02k}\right)\left(\frac{151.6}{148.4 + 151.6}\right)\left(1 + \frac{3.78k}{148.4}\right) = 67.1$$

$$K_{min.} = \left(1 + \frac{62.18k}{18.38k}\right)\left(\frac{148.4}{151.6 + 148.4}\right)\left(1 + \frac{3.7k}{151.6}\right) = 55.1$$

3. Delay Circuit. - The delay circuit coefficient, k_p, is proportional to the voltage at the base of Q_{11}, V_B; i.e., $k_p = 80\ \mu s/V = 0.157$ rad/V. Variations in k_p will be caused by changes in supply voltage (V_{VR4}), and also changes in the resistor (Q11 acts as a variable resistive load to the 9601) and capacitor, C20, which

*A worst case change of ±2% was assumed for M based on data supplied by UTC; this is the approximate change of $V_{sec}/\omega I_p$.

determine the output pulse width. Drift in the effective resistance of Q11 manifests itself primarily in changes in the C20 charging current and voltage; i.e., the I_C and V_C of Q11. Changes in V_C are due to changes in the voltage gain, A_V, and changes in V_B since $V_C = A_V V_B$.

With the recommended changes in the Delay Circuit, $|A_V| \approx R_L/R_E$ since, as shown in Appendix F, $(1 + \beta) R_E \gg h_{ie}$. Therefore, using nominal values,

$$|V_C| = |A_V| V_B = \left(\frac{R_L}{R_E}\right)\left(\frac{V_{VR1}\, R_{45}}{R_{45} + R_{46}}\right) = \left(\frac{R_L}{4.53k}\right)\frac{15(36.5k)}{36.5k + 100k}$$

$$0.885\, R_L \text{ for } R_L \text{ in kohm}$$

Under worst case conditions,

$$|V_C|_{max.} = \left(\frac{R_L}{4.485k}\right)\left(\frac{15.75(36.89k)}{99k + 36.89k}\right) = 0.956 R_L$$

$$|V_C|_{min.} = \left(\frac{R_L}{4.575k}\right)\left(\frac{14.69(36.11k)}{36.11k + 101k}\right) = 0.844 R_L$$

$$\% \text{ increase in } V_C = \left(\frac{V_{C_{max.}}}{V_{C_{nom.}}} - 1\right) 100 = \left(\frac{0.956 R_L}{0.885 R_L} - 1\right) 100 = 8.0\%$$

$$\% \text{ decrease in } V_C = \left(1 - \frac{V_{C_{min.}}}{V_{C_{nom.}}}\right) 100 = \left(1 - \frac{0.844 R_L}{0.885 R_L}\right) 100 = 4.6\%$$

Changes in I_C will also affect k_p. Using nominal values:

$$I_C = \frac{I_F}{\left(1 + \frac{1}{\beta}\right)} = \frac{(7.5 - 4.51)/4.53k}{1 + \frac{1}{100}} = 0.655 \text{ mA}$$

Under worst case conditions:

$$I_{C_{max.}} = \frac{(7.65-4.36)/4.485k}{1.01} = 0.727 \text{ mA}$$

$$I_{C_{min.}} = \frac{(7.39-4.78)/4.575k}{1+\frac{1}{59}} = 0.561 \text{ mA}$$

$$\% \text{ increase in } I_C = \left(\frac{I_{C_{max.}}}{I_{C_{nom.}}} - 1\right) 100 = 11\%$$

$$\% \text{ decrease in } I_C = \left(1 - \frac{I_{C_{min.}}}{I_{C_{nom.}}}\right) 100 = 14.3\%$$

The equation given for the output pulse width, T, of the 9601 is:

$$T = 0.32\, R_X C_X \left[1 + \frac{0.7}{R_X}\right]$$

Using nominal values, T = 200 μs and C = 0.1 μF,

$$R_X = R_{eff}\,(Q11) = 5.55k$$

Since changes in R_X show up as changes in V_C and I_C, only C_X need be varied to complete the computation of ΔT and therefore Δk_p*.

Thus, for changes in C_X only,

$$T_{max.} = 0.32\,(5.55)\,(1.025 \times 10^5)\left[1 + \frac{0.7}{5.55}\right] = 205\ \mu s$$

$$T_{min.} = 0.32\,(5.55)\,(0.975 \times 10^5)\left[1 + \frac{0.7}{5.55}\right] = 195\ \mu s$$

*The effects of V_C and I_C on T will be included when the drift of k_p is calculated.

$$\% \text{ increase in } T = \left(\frac{T_{max.}}{T_{nom.}} - 1\right) 100 = \left(\frac{205}{200} - 1\right) 100 = 2.5\%$$

$$\% \text{ decrease in } T = \left(1 - \frac{T_{min.}}{T_{nom.}}\right) 100 = 2.5\%$$

As shown in Appendix F, an 8% increase in V_C results in a 6% increase in T, a 4.6% decrease in V_C results in a 3.5% decrease in T. Similarly, an 11% increase in I_C results in a 9.6% decrease in T and an 14.3% decrease in I_C results in a 13% increase in T. Also, changes in the zener voltage will result in a -.97% to +2.24% change in k_p.

$$k_{p_{nom.}} = 0.157 \text{ rad/V}$$

Under worst case conditions:

$$k_{p_{max}} = (k_{p_{nom.}}) (\%\ T_{V_C}) (\%\ T_{I_C}) (\%\ T_{C20}) (\%\ T_{VR4})$$

$$= (0.157)\ (1.06)\ (1.13)\ (1.025)\ (1.022) = 0.197$$

$$k_{p_{min.}} = (0.157)\ (0.965)\ (0.904)\ (0.975)\ (0.99) = 0.132$$

4. Zener Supplies. - It was necessary to change the zener supply configuration to permit Q11 to meet the requirement - $(1 - \beta)\ R_e >> h_{ie}$. This stabilized A_V and thereby reduced the k_p variation. The supply configuration shown in Figure 4-122 is recommended. The recommended configuration results in the following worst case results:

$$14.39V \leq V_{VR1} \leq 15.75V$$

$$-15.75V \leq V_{VR2} \leq -14.39V$$

$$7.24V \leq V_{VR3} \leq 7.80V$$

$$5.45V \leq V_{VR4} \leq 5.77V$$

$(I_{VR1})_{max.}$ = 15.4 mA; $(P_D\ VR1)_{max.}$

= 242 mW (60.5% rated power)

$(I_{VR2})_{max.}$ = 11.9 mA; $(P_D\ VR2)_{max.}$

= 187 mW (46.8% rated power)

$(I_{VR3})_{max.}$ = 1.65 mA; $(P_D\ VR3)_{max.}$

= 12.4 mW (3.1% rated power)

$(I_{VR3})_{max.}$ = 42 mA; $(P_D\ VR4)_{max.}$

= 242 mW (60.5% rated power)

b. T_1/T_2 Variations. - It is desirable that $T_1/T_2 << 1$ under worst case conditions. As this ratio approaches 1, T_1 which, in turn, cancels out the effectiveness of the Damper Circuit. If the recommended value of C19 is used, T_1/T_2 using nominal values becomes:

$$\frac{T_1}{T_2} = \frac{R_{37}C_{16}}{R_{eq}C_{19}} = \frac{(18.2 \times 10^{3})\ (3.3 \times 10^{-6})}{(21 \times 10^{3})\ (100 \times 10^{-6})} = 0.0286$$

where R_{eq} = R45//R46//R_{in} of Q11 = 21k

Under worst case conditions:

$$\frac{T_1}{T_2} = \frac{(18.56k)\ (3.68u)}{(19.8k)\ (66.7u)} = 0.0516$$

The ratio is quite acceptable since T_1/T_2 could probably get as high as 0.1 without appreciably impairing Damper Circuit performance.

c. U/T_1 Variations. - The ratio U/T_1 predicts the amount of damping and should lie between 0.35 and 0.9 for acceptable damping action.

Using nominal values of k = 61, k_a* = 3.2A/rad, k_p = 80 μs/V = 0.157 rad/V, M_{eff} = 1.10 mH, and T_1 = 58 ms,

$$\frac{U}{T_1} = \frac{K k_a k_p M_{eff}}{T_1} = \frac{61(3.2)\,(0.157)\,(1.1 \times 10^{-3})}{58 \times 10^{-3}} = 0.58$$

Under worst case conditions,

$$\frac{U}{T_1}_{max.} = \frac{6.71\,(3.2)\,(0.197)\,(1.17 \times 10^{-3})}{(18.02k)\,(3.045u)} = 0.9$$

$$\frac{U}{T_1}_{min.} = \frac{55.1\,(3.2)\,(0.132)\,(1.03 \times 10^{-3})}{(18.38k)\,(3.52u)} = 0.372$$

Thus, under worst case conditions, U/T_1 stays within the design limits of 0.35 and 0.9.

4.5.5.4 Conclusions and Recommendations. - Based on the calculations presented in the last paragraph U/T_1 could increase 55% or decrease 35.9% from its initial value. For the previous analysis, the value of U/T_1 selected for the Feasibility Model was used for the initial value of U/T_1. Care must be taken when potentiometer R39 is set initially to assure that, if the above variations are encountered, the ratio U/T_1 will remain in its useful region; i.e., $0.35 \leq U/T_1 \leq 0.9$.

In actual use in the flight recorders the system will be aligned as follows: R39 will be adjusted so that the damper will just reach the oscillatory state, this corresponding to $U/T_1 = 1.0$; the gain will then be reduced by 4.7 dB, corresponding to a U/T_1 of 0.58; under these conditions, the worst case drift variations will still assure a stable yet well damped headwheel system.

*Variations in the motor constant, k_a, were not considered since it only decreases; and, when it does decrease, less damping is needed.

4.6 COMMAND SYSTEM

4.6.1 Introduction. - The present command system is a completely revised system from the one initially considered. The major change was the implementation of a completely automatic system; i.e., in the new system it will be possible to go directly from one operating command to another without giving the required intervening commands. These are now generated internally and sequenced in such a manner that proper control of the transport is maintained.

A second change in the command system has been considered since it became apparent that it is necessary to store most operating commands in the recorder during a primary power turn-off turn-on cycle. This mode of operation became a requirement when it became known that the spacecraft has only a very limited stored command capability. To facilitate this change, certain modifications in the power flow system were also incorporated. (See Paragraph 4.4.1.) These necessitated changes in the power input connector and the Motor Auxiliary board which controls the distribution of power within the recorder system.

4.6.2 System Description. - The paragraphs that follow are a description of the new command system, which cover the combined operation of four individual boards: Command, Control, Cycler and Sync Speed Detector.

TABLE 4-42. OPERATING COMMANDS

Command No./Command Name	HW & TW Motor Speed	Shoe Position	Capstan Speed	Capstan Direction	WB Signal Capability
Rewind	normal	open	high	rewind	–
Forward	normal	open	high	forward	–
Record	normal	closed	normal	forward	MSS if previous command was 5 RBV if previous command was 6, 7 or 8
Play	normal	closed	normal	forward	MSS if previous command was 5 RBV if previous command was 6, 7 or 8
MSS Standby	normal	open	0	–	–
RBV Standby	normal	open	0	–	–
RBV Enable	normal	open	0	–	–
RBV Run Tape	normal	closed	normal	forward	RBV (command 7 is a prerequisite)

The ERTS recorder system has two types of commands, operating and special (Tables 4-42 and 4-43, respectively). The former commands cause the recorder to perform the record/play/winding functions and are generally mutually exclusive. The second group of commands are for special contingencies and adjustments and are generally stored until the issuance of a negating command.

Power is applied to the recorder by controls external to the recorder (Figure 4-106). Whenever the Spacecraft Power (PRM) is applied, the recorder is placed into the trickle charge mode. Subsequently the WBVTR ON command is given, which applies full power to the recorder and automatically places the unit into the standby mode. The WBVTR OFF command returns the recorder to the trickle charge mode. Stopping the recorder will not allow the capstan brake power to be available so that the tape will coast to stand-still in an uncontrolled, though safe, mode.

TABLE 4-43. SPECIAL COMMANDS

Command No./Command Name	Command Function
Voltage Protect Enable	Enable V.P. circuitry
Voltage Protect Disable	Disconnect V.P. circuitry
Voltage Protect Reset	Reset action of V.P. circuitry
Lap	Permit lapping of video heads
Record Current Adjust	Adjust level of record current

The manner in which the operating command and control system is accomplished is shown in block diagram form in Figure 4-132. All of the operating commands are received by a bank of latching relays. These relays afford the required signal isolation and provide the basic storage of the desired command. The receipt of any of these commands will cause a reset of all latching relays in the following manner. Any new command will generate a 12 ms reset pulse which will clear all previously stored information in the latching relays. The reset pulse is timed so that the 45 ms initiating-command pulse will still be present, to assure that this command remains latched in the relay bank. The latching relays are not reset when converter power is applied unless REWIND or FORWARD had been latched in the relay memory. All other commands can be remembered for "blind orbit" operation. Telemetry is also provided to indicate the commands given to the recorder system, both during WBVTR ON and PRIMARY POWER ON.

The outputs of the command latching relays are dc signal levels which operate the command processor and cycler. The exception to this is the RBV Run Tape signal, which is a dc signal and is directly applied to the processor. The processor circuitry interrogates the command levels and, by means of a clock signal (basically

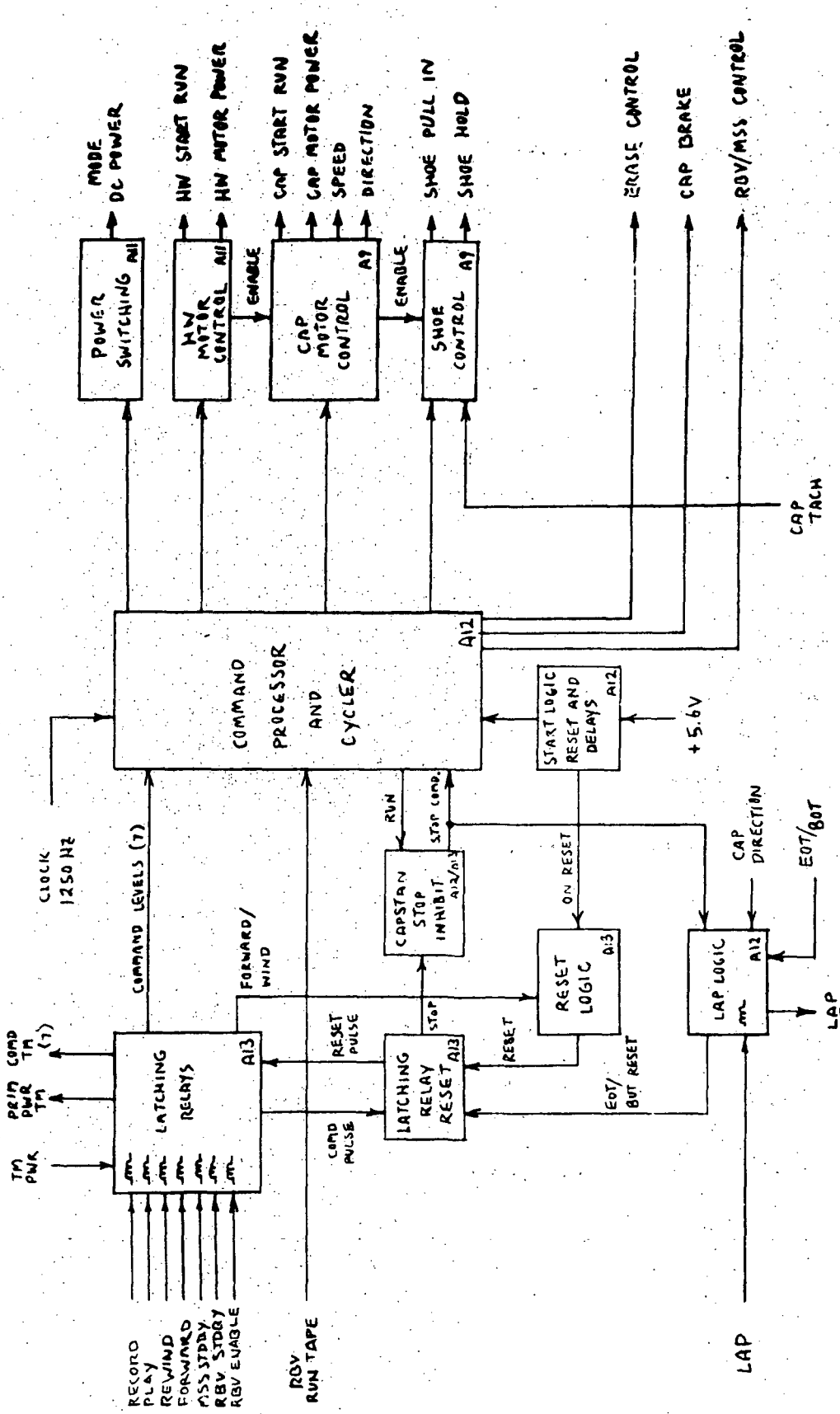


Figure 4-132. ERTS Control System Block Diagram

derived from spacecraft clock) and time delay circuits, assures the proper sequencing of the desired functions listed below:

1. Power is applied to various electronic circuitry only as required. Thus, there are four discrete power distribution conditions: Standby, Record, RBV Playback, MSS Playback.

2. Power is applied to the HW/1ω motors and they are cycled through their start-run modes.

3. Power is applied to the capstan motor to determine the capstan speed and direction. In the high speed modes, the capstan start-run cycling is accomplished.

4. The shoe of the headwheel panel is controlled; that is, the shoe pull-in coil is powered initially while the shoe hold coil is powered for the entire duration of the record/playback process.

5. Powering of the erase head is controlled in the RBV or MSS record modes.

6. Braking power to the capstan is applied for two seconds whenever it is desired to stop the tape.

7. RBV/MSS control signals are generated for various video circuitry to switch internal operating commands.

As part of the ERTS control system, certain interlocks are provided for the moving components of the system. Thus, the capstan motor can only operate after the headwheel is up to speed (exceptions to this rule are the high-speed wind modes). The shoe to the headwheel panel can only close when two conditions are satisfied: (1) the headwheel motor is powered; and (2), the tachometer on the capstan indicates this motor to be above a minimum speed. The above interlocks assure that no mechanical damage can be done to the recorder system.

In addition, beginning and end of tape signals are used to inhibit the capstan from operating when these conditions have been reached. This operation is, of course, also interlocked with the capstan direction control. Upon command, it is also possible to override the primary end of tape switch. This will allow an additional section of tape to be brought in contact with the video heads until the secondary end of tape is reached. This section of tape will have been impregnated with a mild abrasive which, in an emergency, can be used to remove any foreign material that may adhere to the video heads. The lap command is automatically rescinded every time an internal STOP command is generated within the recorder.

4.6.3 Control System Worst Case Analysis. - The worst case analysis of the ERTS Control System is divided into two major sections. The first section deals with system aspects such as input commands, machine modes, mode cycling and major machine sub-sequences; this section also includes detailed analyses of various special considerations which affect the performance of the control system as a whole. The analyses of the second section are presented on a module by module basis. The result is a detailed study of separable control functions.

Both sections of the worst case analysis include the restrictions imposed on the electronics package by the ERTS environmental and extended life requirements. The stressing of all discrete components including resistors, capacitors, inductors, relays and semiconductors is based on limitations specified in the ERTS Worst Case Analysis Criteria Summary (Appendix H) and/or appropriate military specifications. When analyzing the TTL family of integrated circuit logic which is extensively employed throughout the ERTS Control System, use is made of manufacturers specifications, laboratory testing and numerous verbal and written contacts with the vendor's engineering department. The results of every laboratory test are supported as far as possible with a vigorous analytical analysis.

The final section of this report summarizes the overall control system analysis and lists the recommended changes which have been discussed with, and adopted by, the control system design engineer.

4.6.3.1 System Analysis

4.6.3.1.1 Input Commands and Machine Modes - All commands to the ERTS Recorder are supplied from an external source and, with the exception of the RBV Run Tape command, interface with latching relays within the recorder (see Paragraph 4.6.3.2.1 and Paragraph 4.6.3.2.2 for interface analyses). The set coils of all command latching relays are electrically isolated from each other and from the recorder. Reset coils are, as a result, isolated from the set coils. With the exception of the Lap command reset coil they are also referenced to primary power ground.

Input commands are designated as either operating commands or special commands. Operating commands are those which initiate normal machine modes — MSS Standby, MSS Record, Play, RBV Standby, RBV Enable, RBV Run Tape, Rewind, Forward and OFF. Special commands are used to initiate a test sequence (Lap), power disconnect sequence (Emergency Off) and voltage protection circuitry toggling (Voltage Protect Negate and Voltage Protect Set).

Every input operating command initiates a corresponding machine mode or sequence. Operating commands, with the exception of RBV Run Tape, may be initiated in any sequence; the RBV Run Tape command must always be preceded by an RBV Enable command.

The control system will respond to operating command rates up to 10 commands per second; however, it is recommended that the restrictions discussed in Paragraph 4.6.3.1.4b be observed.

Special commands may be initiated at any time without affecting the latching relay store of the last operating command; however, all special commands (with the exception of Voltage Protect Negate and Voltage Protect Set) will reset the last operating command when appropriately negated. The appropriate negations for special commands are given in Table 4-44.

TABLE 4-44. NEGATIONS FOR SPECIAL COMMANDS

Special Command	Negation
Lap	Stop Sequence (see Para 2.2.2.1)
Emergency Off	Off Command
Voltage Protect Negate	Voltage Protect Set
Voltage Protect Set	Voltage Protect Negate

The Lap command may be given at any time except when a Stop Sequence is in progress (see Paragraph 4.6.3.1.3q); however, its insertion has no effect until the EOTS flag is set when the tape is moving in a forward direction with the headwheel shoe engaged.

When these conditions are satisfied the headwheel will be lapped on abrasive tape placed between the primary and secondary EOT positions. The Lap command is reset by the stop timer (see Paragraph 4.6.3.1.3a and Paragraph 4.6.3.1.3c for evaluation of stop timer sequence and Lap command reset).

All operating commands with the exception of Off are clocked into D-type mode flip-flops. Clocking is accomplished using a 1250 Hz reference derived from the spacecraft clock. The Clock, Data, Preset and Reset lines to the mode flip-flops are controlled by the control system logic. When a new external command is given the control system reacts by first comparing the requirements of the new command with the reality of the then existing machine mode. It then "decides" on the safest and most expeditious means for cycling the recorder to the new machine mode. The new command is never clocked into the appropriate mode flip-flop(s) until it is both safe and meaningful to do so.

4.6.3.1.2 Mode Cycling - As noted above, it is the function of the control system to apply the appropriate transitional timing sequences needed to assure both a smooth and, even more important, safe mode-to-mode transition. The time required to assure stable operation in a selected mode is a function not only of the mode selected, but of the previously active mode as well.

In the ERTS control system most of the transitional timing sequences are performed with the aid of TTL one-shot multi-vibrators.

Worst case times needed to assure stable operation in a selected mode are given in Table 4-45. The times shown are based on the assumption that stable operation in the existing mode is achieved before the new command is initiated; the means for effecting the transitions will become clear in the discussions to follow.

a. Operating Modes

1. MSS Standby - The operation of the ERTS Recorder in the MSS Standby mode will be examined with the aid of Figure 4-133, which is an abbreviated diagram of the control system logic as it relates to the MSS Standby, RBV Enable and RBV Standby modes. When the MSS Standby command is applied to the set coil of the MSS Standby latching relay (K5), the following occur:

   (a) K5A contacts open to generate the MSS Standby "ON" TM (see Paragraph 4.6.3.1.4d for analysis of mode telemetry).

   (b) K5B contacts close to set the MSS status (via K6 latching relay), and to energize the DC/DC Converter (via the DC Power On control).

   (c) K5C contacts close to energize the mode trigger circuit and to gate the MSS Standby command to the standby mode flip-flop.

   Closure of the K5B contacts generates the DC Power On control only if the MSS Standby command is preceded by an Off command. The K10 contacts can never be open when the MSS Standby command is given, since VP fault and Emergency Off conditions (which actuate K10) must be negated by an Off command before any other operating command is applied to the recorder. If this requirement is not met, no damage can occur. The recorder will merely accept the MSS Standby command, or any operating command for that matter, without acting on it. When the Off command is ultimately given, all previously stored commands will be immediately reset.

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TABLE 4-45. WORST CASE MODE CYCLING TIMES

FROM \ TO	MSS Standby	RBV Standby	Play	Record	RBV Enable	RBV Run Tape	Rewind	Forward	OFF	Lap	Emergency OFF	VP Set	VP Negate
MSS Standby		0.018 / 0.023	0.50 / 0.56	0.50 / 0.56	0.018 / 0.023		1.25 / 1.86	1.25 / 1.86	1.48 / 2.26		0.03 (5) / 0.06		
RBV Standby	0.018 / 0.023		0.50 / 0.56	0.50 / 0.56	0.018 / 0.020		1.25 / 1.86	1.25 / 1.86	1.48 / 2.26		0.03 (5) / 0.06		
Play	1.46 / 2.21	1.46 / 2.21		0.018 / 0.023	1.46 / 2.21		2.66 / 4.00	2.66 / 4.00	1.48 / 2.26		0.03 (5) / 0.06		
Record	1.46 / 2.21	1.46 / 2.21	0.018 / 0.023		1.46 / 2.21		2.66 / 4.00	2.66 / 4.00	1.48 / 2.26		0.03 (5) / 0.06		
RBV Enable	0.018 / 0.023	0.018 / 0.023	0.50 / 0.56	0.50 / 0.56		0.50 / 0.56	1.25 / 1.86	1.25 / 1.86	1.48 / 2.26		0.03 (5) / 0.06		
RBV Run Tape	1.46 / 2.21	1.46 / 2.21	0.018 / 0.023	0.018 / 0.023	1.46 / 2.21		2.66 / 4.00	2.66 / 4.00	1.48 / 2.26		0.03 (5) / 0.06		
Rewind	1.46 (4) / 2.21	1.46 (4) / 2.21	1.96 (4) / 2.77	1.96 (4) / 2.77	1.46 (4) / 2.21			2.71 / 4.07	1.48 / 2.26		0.03 (5) / 0.06		
Forward	1.46 (4) / 2.21	1.46 (4) / 2.21	1.96 (4) / 2.77	1.96 (4) / 2.77	1.46 (4) / 2.21		2.71 / 4.07		1.48 / 2.26		0.03 (5) / 0.06		
OFF (4)	4.32 / 6.53	4.32 / 6.53	4.80 / 7.07	4.80 / 7.07	4.32 / 6.53		1.23 / 1.84	1.23 / 1.84			0.01 Max.	0.01 Max.	0.01 Max.
Lap (6)							2.66 / 4.00		1.48 / 2.26		0.03 / 0.06		
Emergency OFF									0.01 Max.				
VP Set													0.01 Max.
VP Negate												0.01 Max.	

Notes:

1. All times given in seconds as Min/Max.
2. Add .04 seconds to maximum times shown if OFF relay is set.
3. Times omitted where transfer is impossible, not allowed or meaningless.
4. Times assume Headwheel & I_{ω} motors were running. If HW & I_{ω} motors were not running add 4.27/6.45 to Min./Max. times shown.
5. Does not include time for Capstan and/or HW & I_{ω} motors to coast to a stop.
6. Assumes lapping is in progress when new command is issued.

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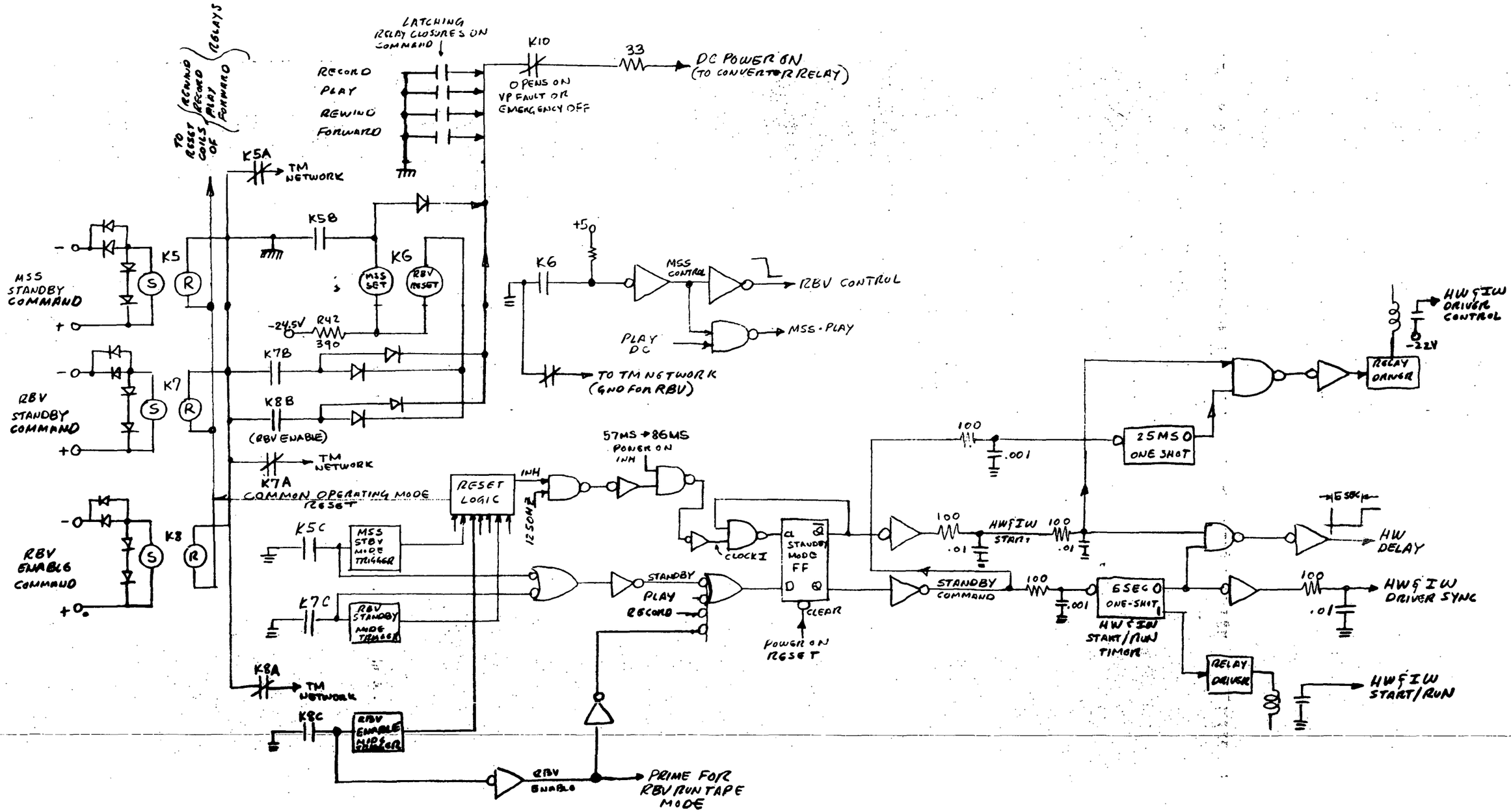

Figure 4-133. Standby Mode Partial Logic Diagram

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When the MSS status is set into the MSS/RBV latching relay (K6), the MSS TM is generated, as are various MSS commands and controls. These signals are employed for the most part to establish MSS status throughout the recorder. The singular exception is the MSS Control signal, which is used to prime the gating of MSS play voltages.

Grounding the input to the MSS Standby mode trigger circuit (via K5C contacts) generates a normal operating command reset sequence (see Paragraph 4.6.3.1.3b) when the MSS Standby command is preceded by an operating command other than Off. This sequence resets all operating command latching relays except MSS Standby. If the MSS Standby command is preceded by a normal Off command (i.e., one which resets all operating commands including Off) a reset sequence is not generated. If, however, the MSS Standby command is preceded by an Off command which leaves the Off relay set (i.e., an Off command used to negate Emergency Off or VP fault conditions), an extended reset sequence will be generated (see Paragraph 4.6.3.1.3b for a full description and analysis of this type of reset). The extended reset sequence is similar to the Normal reset sequence in that it resets all previous command latching relays.

If the previous machine mode required tape movement, the MSS Standby mode trigger circuit will also generate a stop sequence (see Paragraph 4.6.3.1.3c). The primary functions of the stop sequence are to disconnect the capstan motor drive (i.e., by "clearing" all the run tape mode flip-flops) and to energize the capstan motor brake circuit.

In addition to energizing the mode trigger circuit, closure of K5C contacts also gates the Standby command to the data input of the standby mode flip-flop. It will be noted that this input is enabled for all operating modes except Rewind, Forward and Off. Additional control is also maintained via the reset and clock inputs.

If the previous machine mode was Off (Assume first that the Off latching relay is not set), and MSS Standby, RBV Standby, RBV Enable, Play or Record mode is selected, the Power On sequencer applies an unconditional reset to the standby mode flip-flop by holding the reset input "low" on power turn-on (see Paragraph 4.6.3.1.3a for description and analysis of Power On sequences). The "O" output of the standby mode flip-flop is fed back to prime

one input of a mode clocking NAND gate. The second input to this gate is the Clock I signal. The Clock I signal comes up "low" on power turn-on, and remains "low" for approximately 71 milliseconds. The Clock I "low" may produce a positive-going edge at the clock input to the standby flip-flop, but the effect of this edge is negated by the over-riding "low" at the reset input. As a result the standby flip-flop always remains reset for approximately 71 milliseconds after power turn-on. This 71 millisecond delay is required to provide time for the HW/Iω start/run one-shot timing capacitor to charge (see Paragraph 4.6.3.1.3c for analysis of this requirement).

When the 71ms Power On timer expires, the Clock I signal goes "high" on the positive edge of the 1250Hz clock, and then "low" on the next edge. This second edge clocks the standby mode flip-flop to a set condition. When the flip-flop sets, it latches itself into an unconditional set via feedback from the $\overline{Q}$ output to the clock input. This feedback applies an unconditional and invariant "high" to the clock input. The constant "high" disables the clock and, as a result, the standby flip-flop can only be reset by a "low" applied to its reset input. Since it is only possible to generate a reset via a Power On sequence, the standby mode flip-flop, once set, will remain set for all operating modes except Off. The purpose of this feature is to shorten mode-to-mode cycling times and minimize power consumption, by allowing the headwheel and Iω motors to run continuously. Thus, if an Off-Record-Rewind-Play sequence is desired, the HW and Iω motors will each be accelerated to synchronous speed by the Record command, and then continue to run as the recorder is cycled first to Rewind and then to Play.

If a Rewind or Forward command is initiated following an Off mode (with the Off latching relay reset), the standby mode flip-flop will, of course, not be set. Only those modes which enable the data input can set the standby mode flip-flop.

If a standby command is initiated following an Off mode which has left the Off latching relay set (i.e., Off following Emergency Off, or VP Fault), a reset sequence will be generated to reset the Off mode latching relay. This sequence has no effect on the time it takes to set the standby mode flip-flop since, the Reset sequence is completed before the 71ms turn-on delay expires.

The standby mode flip-flop generates the HW and Iω Start and Standby Command signals. These signals are combined to generate

the HW and Iω motor Start/Run sequence, and to connect the input signal drive to the motor driver amplifiers. With reference to Figure 4-133, it will be noted that filtering is incorporated on both control lines. This filtering serves two purposes: first, it suppresses spiking; second, it delays the HW and Iω start signal with respect to the Standby command signal.

This delay is required to insure the proper generation of two delayed signals.

The signal employing the smaller delay incorporates a 25ms TTL one-shot. This signal is used to delay the HW and Iω motor drive signal until after the start windings are switched in. The second delayed signal (i.e., Headwheel Delay) is derived from a 5 second TTL one-shot. This signal is employed to unconditionally inhibit the capstan motor drive for 5 seconds or, until both the HW and Iω motors have reached synchronous speed. The 5 second TTL one-shot output is applied to relay contacts (via a relay driver) which control selection of both the HW and Iω motor start/run windings.

When the HW and Iω Start/Run timer expires, both motors are rotating at synchronous speed with power applied to their run windings. When this occurs the recorder has achieved a stable MSS Standby mode.

2. RBV Standby - When viewed with respect to the control system, the RBV Standby mode is very similar to the MSS Standby mode (see Figure 4-133). The main difference is one of MSS vs. RBV status TM's and controls.

3. Play - When in a Play mode, the ERTS recorder is moving tape at a normal speed via capstan servo control. The HW and Iω motors are rotating at synchronous speed with the headwheel shoe engaged.

   The MSS Play vs. RBV Play status of the recorder is not defined by the Play command alone. The correct MSS vs. RBV status must be established prior to the initiation of the Play command. Thus, if the MSS Play mode is desired, and the MSS vs. RBV status of the recorder is RBV, the Play command must be preceded by an MSS Standby command. Conversely, if RBV Play is desired and the MSS vs. RBV status of the recorder is MSS, the Play command must be preceded by an RBV Standby command.

Cycling of the recorder to a Play mode will be described with the aid of Figure 4-134. When the Play command is applied to the set coil of latching relay K2, one pole generates the Play TM and applies power to the DC/DC Converter via the DC Power On control. The latter function is, of course, only performed if the previous mode was Off.

The Play sequence is initiated by a third set of K2 contacts, which energize the mode trigger circuit and the mode flip-flop gating logic. The Play mode trigger initiates a Normal Reset sequence, unless the previous operating command was Off with the off latching relay reset. A Stop sequence is only generated when the Play command follows a high speed (i.e., Forward or Rewind) mode.

The mode flip-flop gating logic performs the following functions when the K2C latching relay contacts close:

(a) inhibits the gating logic to the Record mode flip-flop.

(b) enables the data input to both the Standby and Play mode flip-flops.

The Record mode inhibit is provided to insure a coincident mode flip-flop switchover whenever a Record command follows a Play mode. It does this by preventing the Record command from propagating to the data input of the Record mode flip-flop. When the Play command latching relay is reset during the Normal Reset sequence, the Record inhibit is removed. The Record mode flip-flop is not immediately set, however, because both the Record and Play mode flip-flop clocks are disabled by the Reset Clock inhibit. As a result, nothing happens until the Reset Clock inhibit is removed at the end of the normal reset sequence. When this occurs the first clock pulse will transfer control from the Play mode flip-flop to the Record mode flip-flop. (Note that the Play mode flip-flop assumes a logical "O" state when it stores the Play mode command.)

If the sequence of events is reversed (i.e., a Play command follows a record mode) the Play command is not inhibited, but rather delayed via a filter at the data input to the Play mode flip-flop. The time constant of the filter is long enough to insure that, in the worse case, the record inhibit propagates to the data input of the Record mode flip-flop before the data line input to the Play mode flip-flop goes "low." As a result it is impossible for both the Record and Play mode flip-flops to be "ON" at the same time.

TO BE REVISED

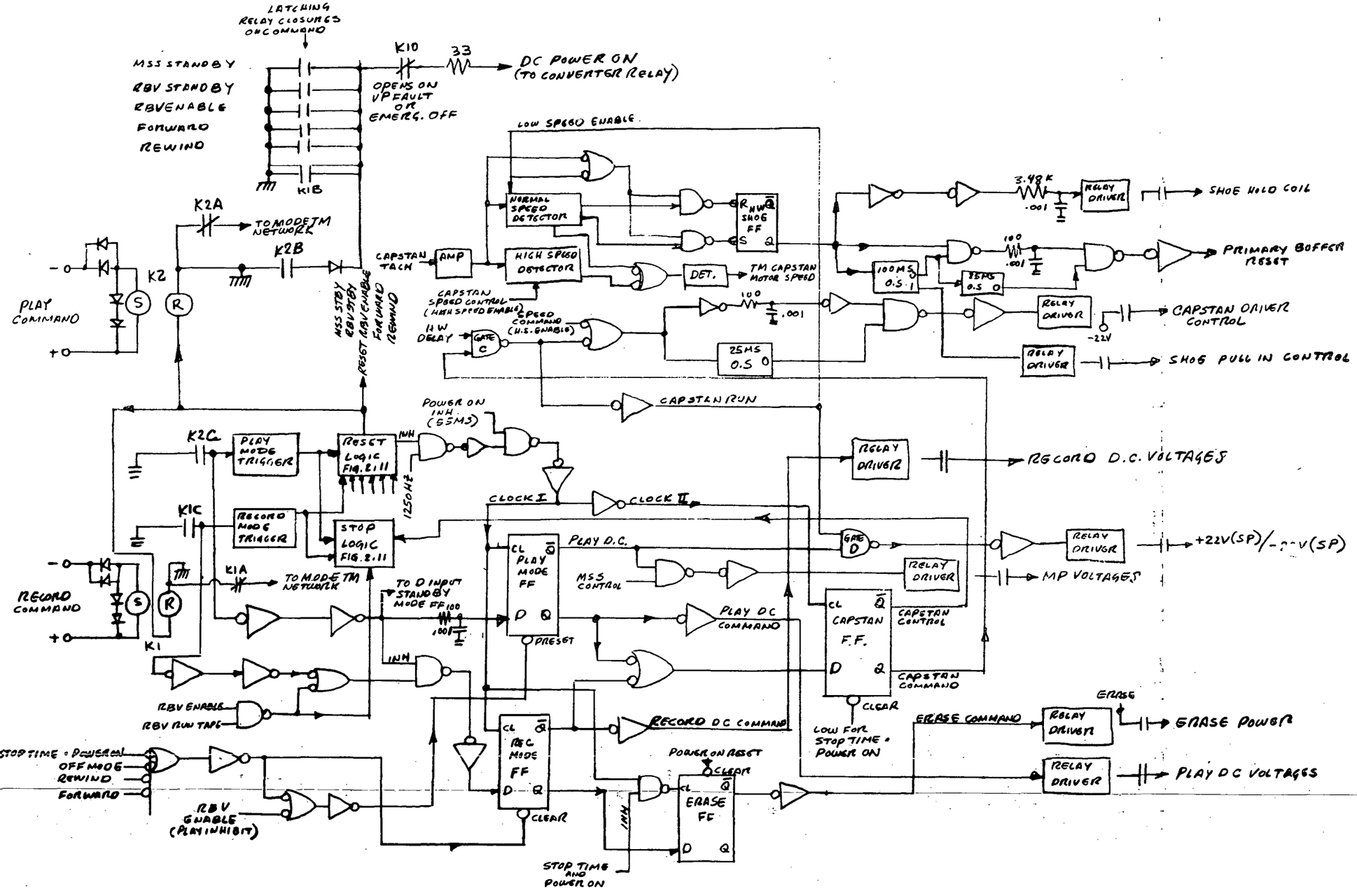

Figure 4-134. Record/Play Mode Partial Logic Diagram

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When the Play command is preceeded by an RBV or MSS Standby mode, the Play mode flip-flop may or may not be clocked to a "O" (i.e., "ON") state before the reset sequence mask inhibits the Clock I signal. There is a seven microsecond period from the time when the Play latching relay contacts close to the time when the reset sequence mask appears (see Paragraph 4.6.3.1.36 and Figure 4-135). If the clock edge occurs during this period, the Play flip-flop will be turned ON. If, one the other hand, there is no clock edge during this time, the Play mode flip-flop will not be turned ON until after the reset sequence mask is removed, following the reset sequence. It is really of little importance when the Play mode flip-flop turns ON following a Standby mode, because there is no control "back-tracking" to be done. In other words, the Play mode is merely an extension or enlargement of operation in a Standby mode. (Note that the Play command enables the standby mode flip-flop.)

When the Play command follows a high speed mode, a Stop sequence is required. The Stop sequence applies an unconditional preset to the Play mode flip-flop. As a result it is impossible to turn on the Play mode flip-flop until after the Stop sequence timer has expired. This is an important inhibit since it locks out Play mode cycling until after the capstan motor is stopped and all high speed controls are reset.

If reference is made to Figure 4-134, it will be noted that there are other preset inhibits which lock out the Play mode flip-flop; namely, Power ON sequence, Off command and RBV Enable.

The Power On inhibit is combined with the Stop timer inhibit. When a Play command follows an Off mode, the Power On preset insures that the Play flip-flop is powered on in a set (i.e., OFF) condition. It remains in this state for approximately 55 milliseconds, or until the extended Power On inhibit is removed from the clock input. When this occurs the Play flip-flop is clocked to a "O" (i.e., ON) state by the first positive-going edge of the Clock I signal.

The Off command preset serves two purposes: first, it inhibits the Play mode when the Play command is given with the Off latching relay set; second, it immediately interrupts the Play mode when an Off command is given following play.

Finally, it will be noted that a Play flip-flop preset is also generated by the RBV enable command. It will be remembered that the RBV Enable command is a precursor to the RBV Run Tape mode only. As

a result, it is not related in any way to operation of the recorder in a Play mode. Thus, if an RBV Enable to Play sequence is initiated, the Play mode flip-flop is unconditionally locked out until the RBV Enable latching relay is reset.

When the Play command is entered into the Play mode flip-flop, the flip-flop assumes a logical "O" state. The "low" appearing at the Q output is then gated to the capstan Record/Play flip-flop where it gates that flip-flop to a set condition. When the capstan Record/Play flip-flop sets, the Capstan command and Capstan Control signals are generated as shown in Figure 4-134.

The Capstan command is applied to gate C along with the HW delay signal. There it awaits completion of the HW and Iω Start/Run sequence (if initiated) before:

(a) enabling the capstan driver amplifier via the Capstan Driver control;

(b) enabling the Capstan Run signal.

It will be noted that the Capstan Driver control is delayed from the Capstan command by 25ms. This delay is required to allow time for relay selection of the appropriate capstan motor windings.

The Capstan Run signal is applied to two loads. The first load is Gate D. Gate D "ANDs" the Play dc signal (generated by the Play mode flip-flop) with Capstan Run, to generate special ±22Vdc power for the capstan servo module.

The Capstan Run signal is also applied to the capstan sync speed detector logic. Here it enables the normal speed detector circuit, while removing an unconditional reset on the headwheel shoe flip-flop. This reset is normally applied to unconditionally inhibit headwheel shoe pull-in for all modes except Record, Play and RBV Run Tape. The description and analysis of capstan sync speed detection and headwheel shoe control is presented in Paragraph 4.6.3.2.4 and will not be considered here.

The Capstan Control signal is applied to the Stop logic (see Paragraph 4.6.3.1.3C) to:

(a) inhibit the Stop sequence for a Record-to-Play or Play-to-Record mode transfer.

(b) enable the Stop sequence for transfer from Record or Play to any other operating mode.

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The Play dc command is generated by the Play mode flip-flop to enable all unconditional Play voltages throughout the recorder.

The Play dc signal is "ANDed" with an MSS status indicator (MSS Control) to enable MSS Play voltages.

The capstan motor is a two phase hysteresis synchronous motor with three sets of windings. One winding set is employed in the Record, Play and RBV Run Tape modes, while the other two sets are employed for Start/Run sequencing in the Rewind and Forward modes. The selection of the normal speed windings required by the Play, Record, and RBV Run Tape modes is simplified by the fact that there are no requirements for a Start/Run sequence, and/or direction control. Thus, in a normal state the capstan motor is connected to operate at normal speed. If a high speed mode (i.e., Rewind or Forward) is selected, the normal speed windings are switched out. The capstan motor will then accelerate via a Start/Run sequence similar to, but of much shorter duration than that employed by the HW and Iω motors. If the Rewind mode is selected the high speed winding phasing must also be reversed to produce tape motion in a reversed-from-normal direction. (See Paragraph 4.6.3.1.2a7 for a detailed analysis of capstan motor winding and direction controls.)

4. Record. - When in a Record mode, the ERTS recorder is moving tape at a normal speed controlled by a 250Hz reference source derived from the spacecraft clock. The headwheel and Iω motors are rotating at synchronous speed with the headwheel shoe engaged.

The Record command is similar to the Play command in that it does not implicitly define the MSS Vs RBV status of the recorder. Therefore, if the recorder is to achieve the required MSS Vs. RBV Record status, the Record command must be preceded by the appropriate MSS or RBV Standby mode. Operation of the recorder in the RBV Record mode is entirely analogous to operation in the RBV Run Tape mode. The major destinction is that, when the RBV Run Tape mode is selected, the actual recording time is directly (and therefore, accurately) controlled by the command level itself.

Cycling of the recorder to a Record mode will be described with the aid of Figure 4-134. When the Record command is applied to the set coil of latching relay K1, one pole generates the Record TM on status and connects the DC/DC Converter via the DC Power On control. A third pair of contacts, K1C, initiates the record sequence by energizing the Record mode trigger circuit and the Record mode flip-flop gating logic.

With reference to Figure 4-134, it will be noted that there are marked similarities between the Record and Play modes. For example, both the Record and Play mode flip-flops use the same clock input signal (i.e., Clock I) and very nearly identical (through reversed) preset inhibits. The reversal is required simply because the Play mode and Record mode flip-flop revert to logical "O" and logical "1" states, respectively, when turned ON.

The data input to the Record mode flip-flop is enabled by a properly executed RBV Run Tape command as well as the normal Record command. When the recorder is operating in a normal RBV Record mode the RBV Run Tape sequence is locked out by the absence of an RBV Enable command. If the recorder is operating in an RBV Run Tape mode and the Record command is given, the RBV Enable command will be disabled by a normal reset sequence. This in turn will override the RBV Run Tape command and the recorder will continue to operate in an RBV Record mode.

When the Record mode flip-flop is set, it in turn sets the capstan Record/Play and Erase flip-flops. The operation of the capstan Record/Play flip-flop was previously discussed. The erase flip-flop is employed to energize the master erase head in all Record modes.

The Erase flip-flop is controlled by a Power On inhibit and a clocking gate. The Power On reset is applied during a Power On sequence to insure that the Erase flip-flop will not be powered on in a set or ON state. The clocking gate is driven by the normal Clock I signal and a combined Power On/Stop timer input. The purpose of the Power On/Stop timer input is to disable data clocking during the Stop sequence interval. As a result of this input, Erase turn off will be delayed for approximately 1.7 seconds when cycling from a Record mode to all modes except Play. (Play is excluded because Record-to-Play and Play-to-Record cycling do not generate a stop sequence.) The effect is to produce a blank (i.e., unrecorded) section of tape following the recorded segment.

If a Play command follows a Record mode, the stop sequence is not generated and the Erase flip-flop is reset on the second clock edge following the normal reset sequence. The first edge is used to coincidently switch the Record mode flip-flop OFF and the Play mode flip-flop ON.

5. RBV Enable. - The RBV Enable mode is similar to the RBV Standby mode in that, when stabilized, it generates the RBV status and causes both the HW and Iω motor to accelerate and run at synchronous speed.

   In spite of these similarities however, RBV Enable is a logical precursor to the RBV Run Tape mode only. This fact will be clear if reference is made to Figures 4-134 and 4-135. With reference to Figure 4-135, it will be noted that the RBV Enable command is reset by all subsequent operating commands except the RBV Run Tape on command. Moreover, with reference to Figure 4-134 it is apparent that, for the RBV Run Tape command to be effective, it must be preceded by the RBV Enable mode.

6. RBV Run Tape. - The RBV Run Tape command initiates a controlled RBV Record mode when preceded by an RBV Enable command (see Figure 4-136.) The input RBV Run Tape command is unlike any other externally applied command in that it does not interface with a command latching relay. It is instead applied to the control logic directly, via a dual gate Schmitt trigger. When the RBV Run Tape input goes "high" (indicating RBV Run Tape ON) the Schmitt trigger generates both a TTL "low" and a TTL "high."

   The TTL "low" is applied to the RBV Tape TM detector. The TM detector converts the "low" input to a standard - 7.5 volt (nominal) TM output signal.

   The TTL "high" output is applied to a NAND gate, which inhibits the RBV Run Tape ON command unless it is preceded by an RBV Enable command. If both commands are present, then the output of the NAND gate goes "low" to enable the Record mode flip-flop gating logic. The output of the NAND gate is also applied to a 140-μsec TTL one-shot. When the RBV Run Tape signal goes "high" the one-shot is disabled.

   When the RBV Run Tape signal enables the Record mode flip-flop the recorder immediately cycles to a Record mode. It remains in this mode until the RBV Run Tape Command input goes "low". When this occurs the Record mode flip-flop gating input is disabled and the 140 us one-shot begins to time.

   When the one-shot fires it generates a pulse which, in turn, fires the Stop timer. The Stop timer immediately institutes a special Stop sequence (see Paragraph 4.6.3.1.3c), which resets the Record and Capstan Record/Play flip-flop and brakes the capstan motor to a stop.

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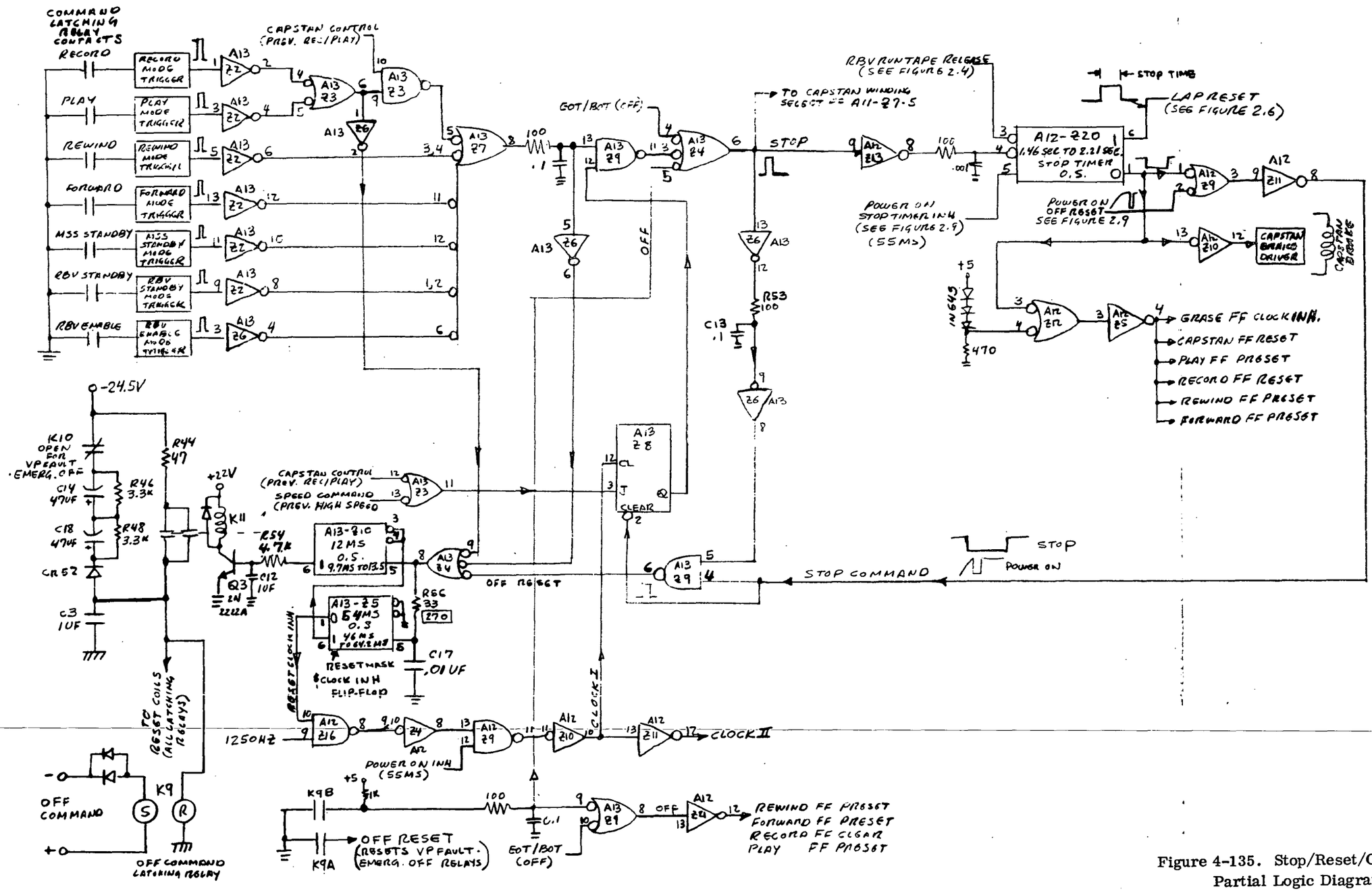

Figure 4-135. Stop/Reset/Off Control Partial Logic Diagram

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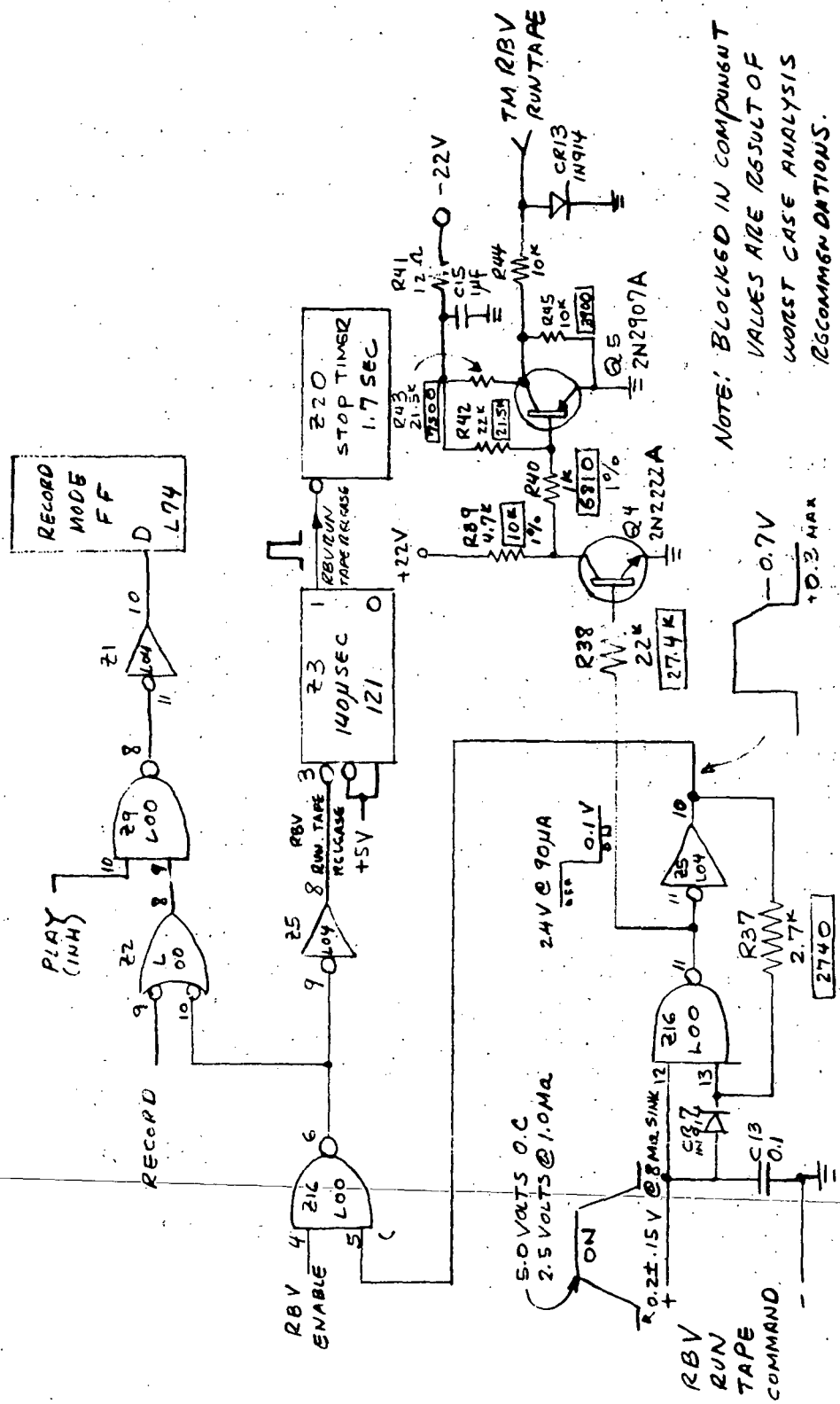

Figure 4-136. RBV Run Tape Mode Logic

Since a reset sequence is not initiated by an RBV Run Tape OFF command, the recorder will revert automatically to the RBV Enable mode when the special Stop sequence is completed. Actually, the recorder never really leaves the RBV Enable mode, since the headwheel drive is unaffected by a Stop sequence.

If the RBV Run Tape command is ON when another operating command is given, the control system will interrupt the RBV Run Tape mode by resetting the RBV Enable command via a normal reset sequence. The recorder will then cycle to the last mode selected.

7. Rewind. - When in a Rewind mode the ERTS recorder is moving tape in a reversed from normal direction at a speed four times the normal speed, or 40 ips. The headwheel and Iω motors may or may not be rotating, depending upon the nature of the previous machine mode (see Paragraph 4.6.3.1.2a1). Under no condition is the headwheel shoe ever engaged in the Rewind mode.

The operation of the control system in the rewind mode will be described with the aid of Figure 4-137. With reference to this figure it will be noted that, when the Rewind command is applied to the set coil of latching relay K3, the following occur:

(a) K3A contacts open to generate the Rewind TM ON signal.

(b) K3B contacts close to energize the DC/DC Converter via the DC Power On control.

(c) K3C contacts close to energize the Rewind mode trigger circuit, and generate the Rewind signal.

When the Rewind mode trigger circuit is energized, it generates a normal reset sequence unless logic power was disconnected by a prior off command which left the off relay reset. If the previous machine mode was OFF with the off latching relay remaining set (i.e., an Off following Emergency Off or VP fault), a modified extended reset sequence will be generated (see Paragraph 4.6.3.1.3b).

The Rewind mode trigger circuit generates a Stop sequence only if the previous operating mode required tape motion. The Stop sequence disconnects power from the capstan power amplifier and applies power to the capstan motor brake.

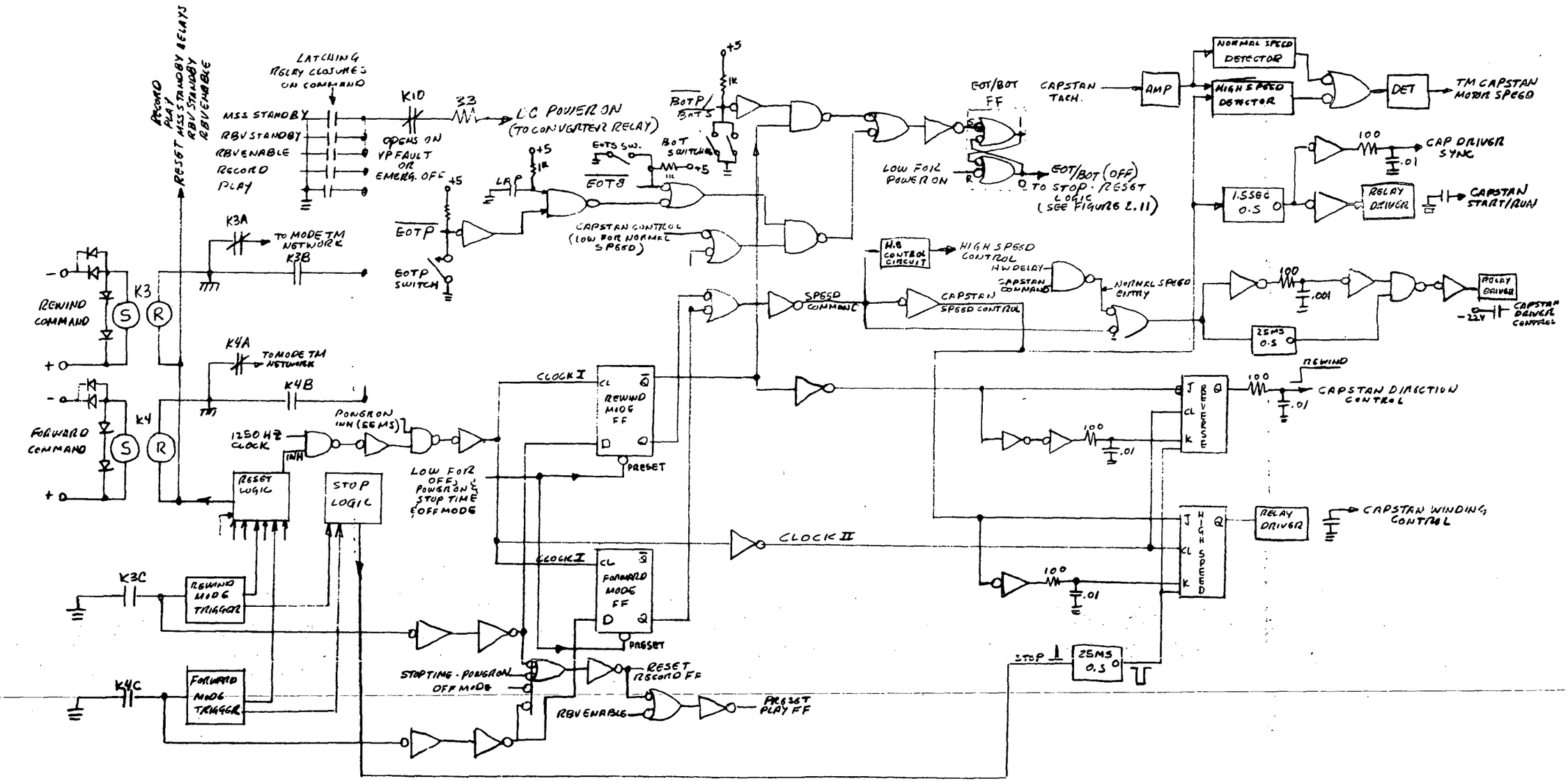

Figure 4-137. Rewind/Forward Mode Partial Logic Diagram

The Stop sequence has no effect on the HW and Iω motor drive. Therefore, if the HW and Iω motors are running before the Rewind command is initiated, their operation will not be interrupted. Conversely, if the HW and Iω motors are not running when the Rewind command is initiated they will not be energized by insertion of the Rewind command.

The Rewind signal unlatches or inhibits the Record and Play mode flip-flops, and is applied as a data input to the Rewind mode flip-flop. Before examining the effect of data line clocking, it will be necessary to first consider the effect of overriding presets.

With reference to Figure 4-137, it will be noted that the Rewind mode flip-flop is preset (i.e., held OFF) by the following:

(a) an Off command;

(b) Power On sequence;

(c) Stop sequence.

The Off command unlatch is provided to insure that:

(a) when the Off command is given, the Rewind mode will be immediately locked out;

(b) when Rewind follows Off with the Off relay set, the Rewind mode will be locked out until the Off latching relay is reset.

The Power On sequence preset is provided to insure that the Rewind mode flip-flop is always powered on in a "1" (i.e., OFF) state.

The Stop sequence inhibit is generated to either hold off rewind cycling until after the capstan motor has stopped (Rewind command following Forward, Record, Play or RBV Run Tape ON modes), or to disconnect rewind status from the capstan drive electronics (Forward, Record, Play, or RBV Run Tape ON commands following a Rewind mode).

When the Rewind mode flip-flop is clocked to an ON (i.e., reset) state, it primes the gating of the BOTP/BOTS indicators to the BOT/EOT Flip-flop, and generates the following capstan-oriented command levels:

(a) Speed command

(b) Direction command

(c) Capstan Speed control

When the Speed Command signal goes "low" in the Rewind mode it:

(a) enables a relay driver which, in turn, applies power to the capstan driver amplifier after the correct capstan motor winding configuration is selected (see Figure 4-137);

(b) primes a flip-flop in the Stop sequencer which will enable the Stop sequence when a new operating command is given (see Figure 4-135 and Paragraph 4.6.3.1.3c).

(c) increases the High Speed Control signal level which, in turn, increases the Search mode Off-Tape signal threshold.

The Direction Command signal goes "low" in the Rewind mode to enable a JK flip-flop which, in turn, selects the reversed from normal capstan motor winding phasing which is needed to rewind the tape.

The Capstan Speed Control signal goes "high" in either the Rewind or Forward modes to:

(a) enable the high speed JK flip-flop which selects the capstan motor high speed windings via a relay driver;

(b) fire the 1.5 second high speed Capstan Start/Run timer;

(c) enable logic which connects the high frequency (i.e., 1250Hz) reference source to the capstan driver amplifier.

Sequencing of the Rewind capstan commands is rather straightforward when the Rewind command is preceded by a mode which does not require tape motion. However, when the Rewind mode supercedes or is replaced by a Play, Record, Forward or RBV Run Tape ON mode, cycling is complicated by the need to first stop the capstan motor and then reorient its windings and drive before allowing it to accelerate to its new stable state.

With reference to Figures 4-135 and 4-137 it will be clear that, when the Rewind command is given following a Run Tape mode, it is theoretically possible to clock the Rewind flip-flop to an ON state before its Stop sequence preset goes "low". The width of this "window" can be calculated by subtracting the time it takes for the Rewind command to propagate to the D input of the Rewind flip-flop, from the time it takes for the Stop sequence preset to appear. This time

will vary from 16.5 μsec to 88.2 μsec. Thus, if the Clock I signal goes "high" during this time, the Rewind flip-flop will be turned on. Although the turn-on is only transitory in that the Stop sequence will turn off the Rewind mode flip-flop, the resultant pulse on the Capstan Speed Control line will fire the 1.5 second Start/Run timer.

Once the Start/Run timer fires, it times for a full timing period. If this time is longer than the Stop timer interval, the Start/Run timer will not be timed out when the Stop sequence expires. As a result, the Rewind flip-flop may turn on without restarting the Start/Run timer. Thus the capstan motor will be powered on via its high speed run windings. Consequently, it will not attain synchronous speed and, as a result, the tape will rewind at a slower than normal speed.

In calculating the worst case limits for both the high speed capstan Start/Run and Stop sequence timers, the following worst case results were obtained:

(a) Start/Run timer

@ 0°C, 1.29 seconds $\leq$ td $\leq$ 1.81 seconds
@ 60°C, 1.20 seconds $\leq$ td $\leq$ 1.70 seconds

(b) Stop sequence timer

@ 0°C, 1.56 seconds $\leq$ td $\leq$ 2.21 seconds
@ 60°C, 1.46 seconds $\leq$ td $\leq$ 2.07 seconds

With regard to these figures it is obvious that, in the worst case, the Start/Run interval can be longer than the Stop sequence interval. To insure that this does not occur in practice, one of three steps must be taken:

(a) reduce the Start/Run timer interval by changing the 26.1 kohm timing resistor to 21.5 kohms. This will alter the Start/Run timer interval to the following worst case extremes:

@ 0°C, 1.06 seconds $\leq$ td $\leq$ 1.49 seconds
@ 60°C, 0.99 seconds $\leq$ td $\leq$ 1.40 seconds

(b) increase the Stop sequence timing interval by increasing either C_T or R_T. (C_T and R_T refer to external timing components associated with the Stop timer one-shot.) If C_T is increased from 82 uF to 100uF the Stop timer interval will then be:

@ 0°C, 1.9 seconds $\leq$ td $\leq$ 2.7 seconds
@ 60°C, 1.78 seconds $\leq$ td $\leq$ 2.53 seconds

(c) specify initial tolerances on both the Start/Run and Stop sequence timers so as to minimize overlap. This can alter original time intervals to read as follows in the worst case:

Start/Run timer

@ 0°C, 1.29 seconds td $\leq$ 1.61 seconds
@ 60°C, 1.2 seconds td $\leq$ 1.56 seconds

Stop sequence timer

@ 0°C, 1.78 seconds $\leq$ td $\leq$ 2.21 seconds
@ 60°C, 1.65 seconds $\leq$ td $\leq$ 2.07 seconds

To reduce the Start/Run timer as suggested by step (a) is not advisable, since a minimum start time of 1.20 seconds is required to insure that the capstan motor achieves synchronous speed. With regard to step (b), the suggested change will insure that at all times there is virtually no overlap between the Start/Run and Stop timers. Step (c) is also a possible alternative since, if initial values are properly chosen, the overlap is eliminated.

With reference to Figure 4-137, it will be noted that the stop signal is applied as an inhibit to the capstan direction and high speed JK flip-flops. This inhibit is inserted to mask a transition when the Clock II signal is forced "high" by a clock inhibit at the beginning of a reset sequence. (See Paragraph 4.6.3.1.3b).

The Stop inhibit is selective in that it inhibits resetting of the Capstan Direction flip-flop on a Rewind-to-Forward, Rewind-to-Record or Rewind-to-Play transition. It also inhibits the resetting of the high speed flip-flop on a high speed-to-Record or high-speed-Play transition. This is done to preserve the overall Rewind or high speed status until after the high speed modes are reset by newly inserted Record or Play commands.

8. Forward. - Operation of the control system in the Forward mode is similar in many respects to that in the Rewind mode (see Figure 4-137). For example, both the Forward and Rewind mode flip-flops employ identical preset and clock input signals. Moreover, both modes require high speed capstan control and a Start/Run capstan motor sequence.

The major differences between the Rewind and Forward modes are two: first, whereas the Rewind mode flip-flop primes the BOTP/BOTS

gating, the Forward mode flip-flop is ORed with the Capstan flip-flop output to generate EOTP/EOTS gating; secondly, when the Forward mode is selected, the rewind JK flip-flop is not turned ON.

9. OFF. - When the recorder is in an Off mode, the DC/DC Converter is turned off and, as a result, all control logic is inoperative. The Off command may be initiated at any time and is required to negate either the Emergency Off command or a VP fault condition.

The response of the control system to an Off command will be examined with the aid of Figure 4-135. If the command is given while the recorder is in a mode other than Emergency Off, or VP fault, the K9B off latching relay contact closure will:

(a) generate the off signal,

(b) institute a special Stop sequence.

The Off signal is applied as an unlatch control to all mode flip-flops except Standby. The special Stop sequence performs all of the functions of a normal Stop sequence (i.e., disconnects power to the capstan motor driver and applies braking to the capstan motor).

It will be noted that the Off command, unlike all other operating commands has no mode trigger circuit and cannot as a result generate a normal mode reset sequence. This omission is intentional, since it would be unadvisable for the Off command to generate a mode reset and hence disconnect the DC/DC Converter before the capstan motor has been stopped. Still is a requirement that the Off command be capable of resetting the last operating mode command, so as to achieve its goal of disconnecting the DC/DC Converter.

To achieve this end the Off command generates an extended off reset sequence, which is extended in that it occurs at the end instead of at the beginning of a Stop sequence.

The means for effecting this reset will be clear if reference is made to Figure 4-135. When the Off command is given, the Stop timer is fired and propagates a "low" to pin 4 of "AND" gate A13-Z9 before the Off command is able to propagate a "high" to pin 5. The delay in pin 5 propagation is, produced by the filter network between the Stop signal and the pin 5 input. During the Stop sequence, pin 5 goes "high" while pin 4 is held "low" by the Stop timer. When the Stop timer "times out," it propagates a "high" to the pin 4 input of A13-Z9.

This forces the gate output to go "low". When this occurs the Reset one-shot is fired. The reset one-shot resets all command latching relays including that for the OFF command. This, inturn, removes the DC Power On signal from ground to disconnect power to the DC/DC Converter relay. This causes the converter to drop out. As a result, all power to the control system (with the exception of telemetry and primary power) is disconnected. The recorder will remain in this state until a new operating command (other than Off) is given.

If the Off command is initiated when the recorder is in an Emergency Off or VP Fault mode, the K9A contacts reset the Emergency Off and VP Fault relays. This causes the K10 relay contacts in the reset network to close. When this occurs the common mode reset line is pulsed to reset all operating commands latching relays except off (see Paragraph 4.6.3.1.3b for complete analysis of this type of reset). This, inturn, places the recorder is in an Off mode with the Off latching relay set. When a new operating command is given, the presence of the Off signal will generate a reset sequence. It is imperative that this sequence be completed before the new input command level is removed.

Analysis of the time it takes for this reset sequence was calculated using worst case delays, and found to be 39.1 ms maximum (see Table 4-46). Since this time is less then the minimum command level period (i.e., 40ms), the reset sequence will always terminate before the new input command level is removed (see Paragraphs 4.6.3.1.3b2 and 4.6.3.2.1c for supporting analysis).

TABLE 4-46. OFF RESET SEQUENCE TIMING

Step	Action	Time (In Milliseconds)
1	Operating command initiated	0
2	Input command latching relay contacts close	1.5/3.5
3	DC/DC Converter Relay contacts close and converter turns on	11.5/13.5
4	Logic voltage Stabilized	13.5/15.5
5	A13-Z9-4 goes "high" to fire reset timer	14.8/22.8
6	Q3 turns on (see Figure 4-135)	16.4/24.4
7	K11 picked up (voltage applied to reset coils of latching relays)	19.3/27.3
8	Off command latching relay resets	20.8/28.8
9	Reset timer expires (see Figure 4-135)	24.6/36.4
10	Q3 turns off	24.8/36.6
11	K11 drops out removing reset	27.3/39.1

4.6.3.1.3 Special Modes. -

a. Lap. - The Lap permits lapping of the video heads on special abrasive tape placed between the primary and secondary end of tape positions. When the Lap command is given, it unconditionally generates the TM Lap on signal and inhibits the EOTP flag (see Figure 4-138). The Lap mode is negated by any mode transition which requires a Stop sequence.

Since it is required that the recorder be in either a Record or a Play mode with the headwheel shoe engaged before lapping can occur, it is obvious that the Lap mode control logic is not all-inclusive; that is, insertion of the Lap command alone will not insure that the video heads will be lapped. It is generally not advisable to lap the video heads in the Record mode, because the heat produced at the pole tips by the record current adds to the frictional heat already produced by the lapping process itself. For the Lap command to be effective, it must be given when the recorder is either in a Play mode or some other mode from which Play can be reached without instituting a Stop sequence. This limits the choice of pre-play modes to Off, RBV Standby and Record.

Because of the simplicity of the Lap mode logic, the worst case analysis was limited to an evaluation of Q1 in the saturated state (see Figure 4-138). The maximum saturation current of Q1 is given by:

$$\overline{I_{C1}} = \frac{\overline{V_{+22}}}{\underline{R_{COIL}}} = \frac{23.2}{919} = 25.3 \text{ mA}$$

At this current the worst case $h_{FE} = 37$, and the maximum base current requirement is $25.3 \times 10^{-3}/37 = 683\ \mu A$. At 0° C, where R_{COIL} is minimum, $\overline{Vbe\ sat}$ is given as 0.84 volts.

Once again, at 0° C the worst case TTL logic drive capability is given by a linear approximation as:

$$V_{Drive} = -140\ I_b + 2.8$$

Using this equation, the maximum base drive resistance can be calculated from:

$$-140\ I_b + 2.8 = I_b R_B + \overline{Vbe}_{sat}$$

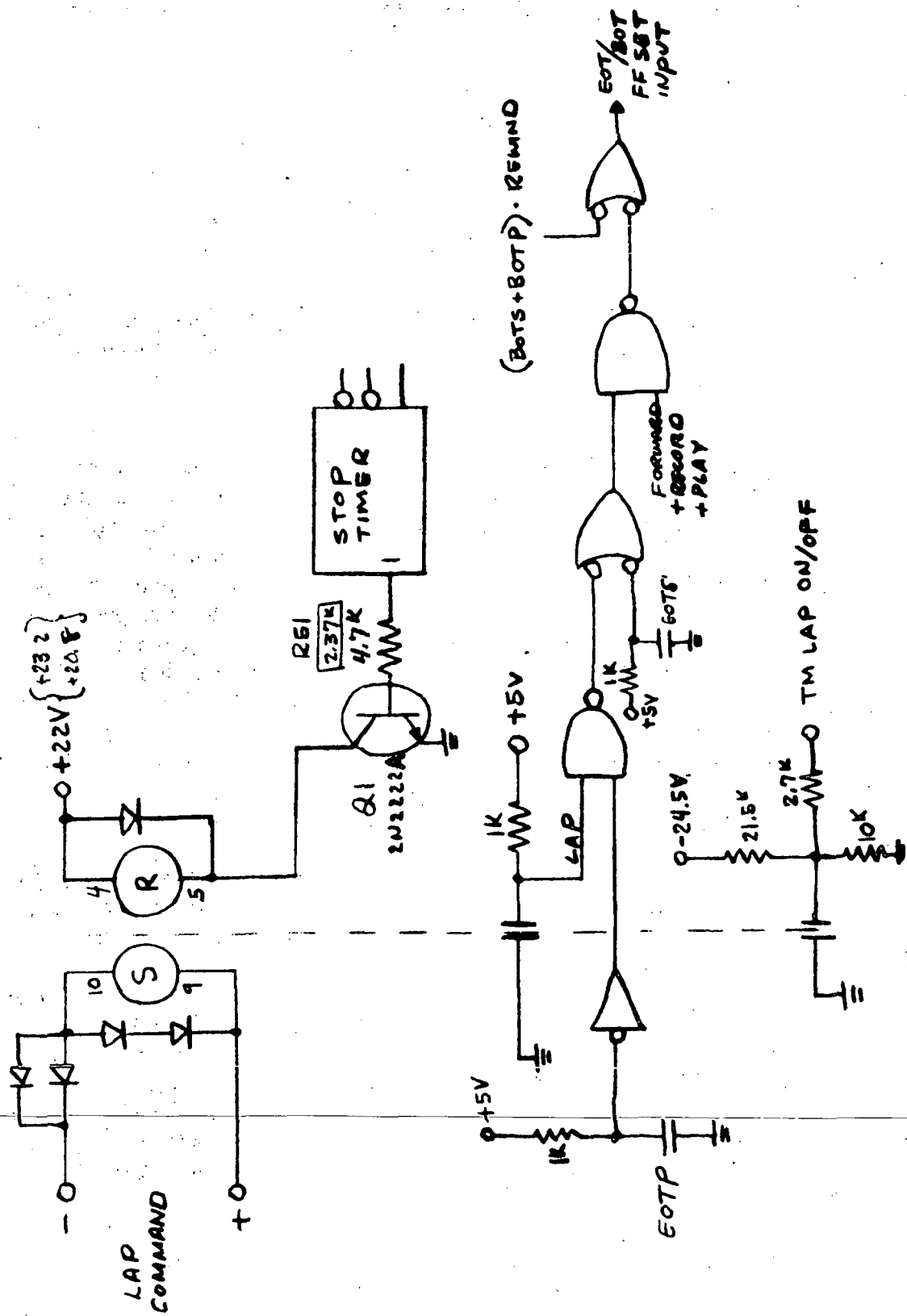

Figure 4-138. Lap Mode Logic Diagram

From which,

$$\overline{R_B} = \frac{-140\ \overline{I_b} + 2.8 - \overline{Vbe}_{sat}}{\overline{I_b}}$$

$$= \frac{-140 \times 683 \times 10^{-6} + 2.8 - 0.84}{683 \times 10^{-6}}$$

$$= 2700 \text{ ohms.}$$

The calculated value for R_B is less than that chosen in the original design. Thus, if Q1 is to be fully saturated in the on state, R51 must be reduced from 4700 ohms to 2430 ohms which is the nearest standard one percent preferred value.

b. Emergency Off and VP Fault. - Although the VP (Voltage Protect) Fault condition is not initiated by an external command, the effect which it has on the ERTS control system is wholly analagous to that produced by the externally applied Emergency Off command (see Figure 4-139). When either the Emergency Off command is given or a VP Fault condition exists, primary power is removed from the recorder, except for power to the voltage protection circuitry and a trickle charging network. This, in turn, causes the DC/DC Converter relay to drop out, both by virtue of the 301 ohm trickle charging resistor's inability to supply holding power, and by a disconnect from primary power ground. As a result, the control system is disabled and the recorder is forced to turn off.

With reference to Figure 4-139 it will be noted that, when either the Emergency Off or VP Fault latching relays are set, -24.5 volt primary power is applied to turn on relay A13-K10 within the control system. When energized, this relay disconnects both the DC/DC Converter relay ground return (via contacts K10B) and the accelerated reset network (via contacts K10A).

When an Off command is given to negate either an Emergency Off or VP Fault condition, the Off command latching relay (A13-K9) is set. When this occurs, the reset coils of both the Emergency Off and VP Fault latching relays are energized via the Off Reset signal. Primary power is immediately re-applied to the control system and relay A13-K10 is de-energized. When K10 is de-energized, the closure of contacts K10A pulses the common mode latching reset coils. The width of this reset pulse will vary between 2.16 ms and 4.63 ms (see Paragraph 4.6.3.1.3b for supporting analyses). Since the externally applied Off command is

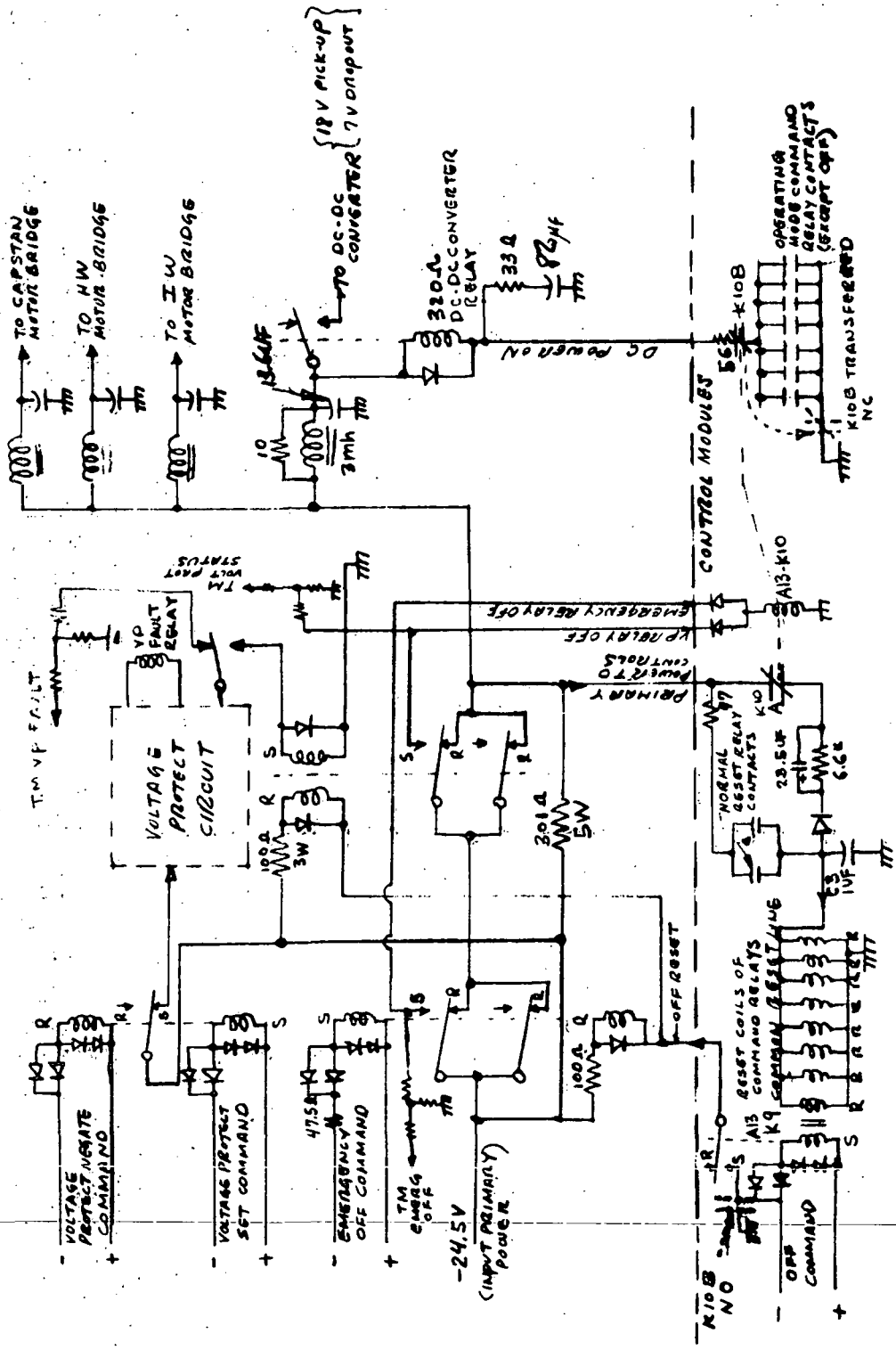

Figure 4-139. Power On/Off Logic Diagram

still active after the reset pulse disappears, all operating command latching relays (except Off) will be reset. The recorder will thus revert to an Off mode with the Off latching relay in a set condition. The Off relay will not be reset until another operating command is given (see paragraph 4.6.3.1.2a).

In the preceding discussion the purpose of the K10B contacts was not discussed. These contacts serve two purposes: First, in the Power Off cycle, they remove the DC/DC Converter relay load from the trickle charging network; this limits the primary power drain to normal capacitor leakage currents. Secondly, in the Power On cycle, the synchronous closure of K10A and K10B contacts allows the accelerated reset pulse to reset the previous operating command before the DC/DC Converter relay can be picked up. Of course, the DC/DC Converter would be turned off anyway in the process of resetting the previous operating command; however, the presence of the K10B contacts prevent the DC/DC Converter from being pulsed unnecessarily with primary power.

There are some inherent problems with the negation of the Emergency Off and VP Fault conditions. These problems are caused by the fact that the Off latching relay is not reset by the accelerated reset pulse. As a result, both the Emergency Off and VP Fault latching relays will have power applied to their reset coils until a new operating command is given. This could produce a potentially dangerous situation* if, for example, the primary power regulator fails while the Off latching relay is set. If this were to occur, the VP Fault latching relay would have power applied to both its set and reset coils.

The effect which this has on relay operation can be described with the aid of Figure 4-140 which is a cross-sectional view of the balanced armature latching relay. With reference to this figure, it will be noted that both the set and reset coils of the relay are wound to generate opposing flux in a common core. As a result, if the reset coil is energized, the armature will rotate from the solid line position to the dotted line position. If the reset voltage is then maintained while an equal voltage is applied to the set coil, the net coil produced flux will be reduced to zero. As a result, the armature and relay contacts will remain in the reset position, until the reset coil voltage is removed.

If these events are translated to the previously suggested case (i.e., a primary power regulator failure with the Off mode latching relay set), it is obvious that the VP Fault latching relay will not respond to the VP Fault condition. As a result, if the fault persists and a new operating command is given, the DC/DC Converter will be allowed to turn on and

*Subsequent external command system changes have resulted in a revision of the Voltage Protect controls. The only danger remaining is the fact that under VP Negate conditions, any primary supply over voltage is proportionately applied to the internally generated DC/DC Converter voltages and thus may over stress certain components.

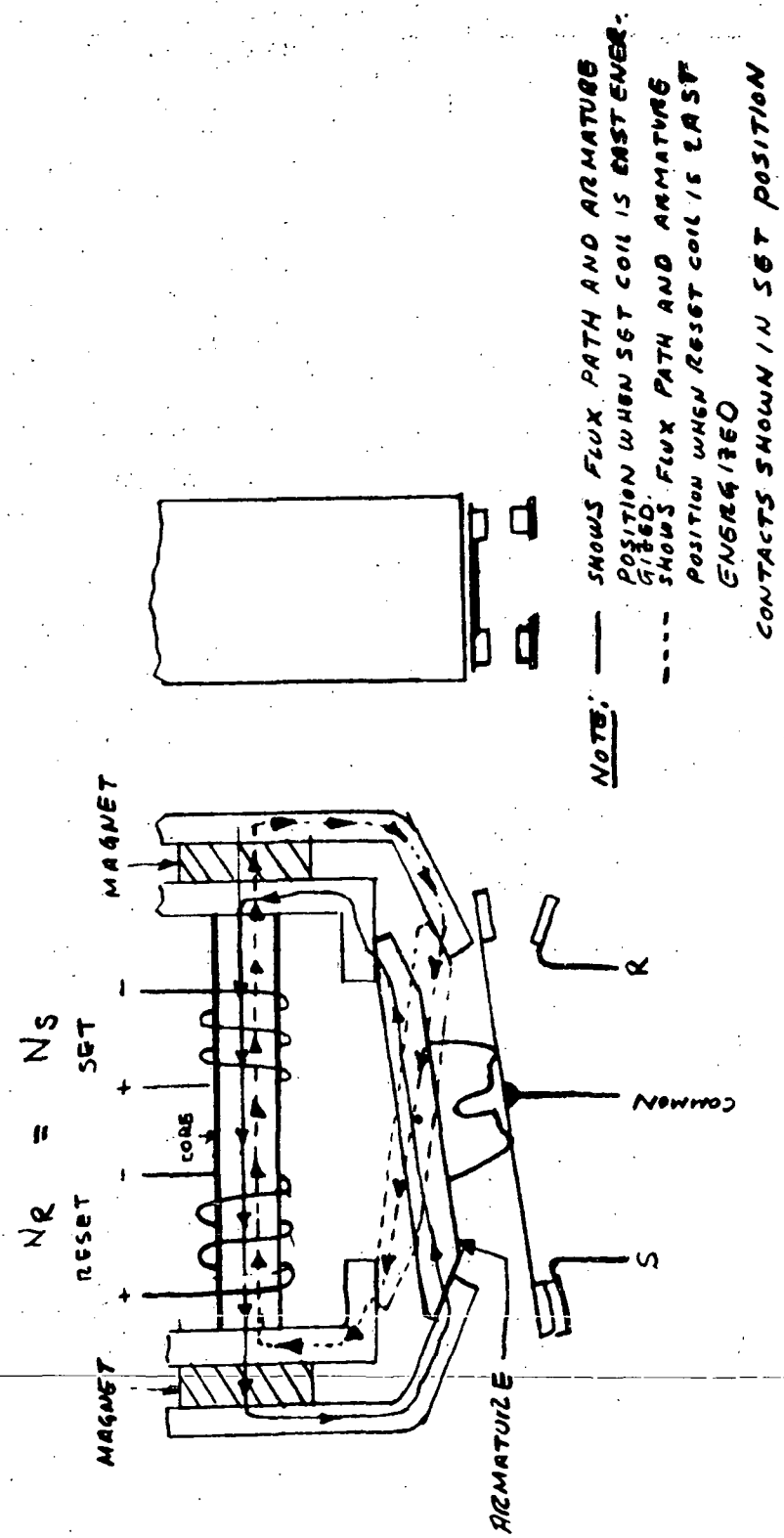

Figure 4-140. Emergency Off/VP Fault Latching Relay

remain on until the Off mode latching relay is reset. Fortunately the TTL control logic is protected against the -39 V to -18 V primary power extremes which can occur during a primary power regulator failure. However, since the false turn on is largely due to the continuous nature of the Off command reset, it would not occur if the Off Reset signal were transformed to a pulse. This can be accomplished quite readily by transferring the K10B normally closed contacts to the opposite side of the operating command relay contacts (see dashed lines in Figure 4-139). This would free the K10B -NO contacts to open the Off Reset signal ground as shown. Thus, when an Off command is given to negate either an Emergency Off or VP Fault condition, the Off Reset signal would only be active (i. e. , at ground potential) until the K10 relay is de-energized. Once the K10 contacts fall back to their de-energized position, the Off Reset signal would be disconnected. This would remove the reset from the Emergency Off and VP Fault latching relays and thereby enable the recorder to respond to either an Emergency Off command or a VP Fault condition.

c. Voltage Protect Negate and Voltage Protect Set. - The Voltage Protect Negate and Voltage Protect Set commands are toggling commands which either disconnect or connect the voltage protection circuitry (see Figure 4-139). When the Voltage Protect Negate command is given, all power is removed from the voltage protection circuitry. The VP Fault relay is not energized when this occurs and, as a result, the recorder will continue to operate in the then current mode.

With the voltage protection circuitry disconnected, the recorder is required to withstand continuous primary voltage extremes of -20 volts and -34. 5 volts at an ambient temperature of 35° C. Within the control system, only the reset function is directly affected by primary power voltage extremes. The analysis of both accelerated and normal resets (see Paragraph 4. 6. 3. 1. 3b), shows that the reset function is unaffected by voltage variations within the -20 to -34. 5 volt extremes.

Since the DC/DC Converter incorporates Zener diodes to limit overvoltage surges, the -20 volt to -34. 5 volt input variation translates to an output variation of only ±10% with respect to nominal, for each converter voltage. Thus, for example, the +5. 6 volt TTL logic voltage applied to the control system will vary from +5. 04 volts to +6. 16 volts.

This voltage is decoupled by an LC half-section filter within each control module such that, if worst case loading is assumed,[1] the voltage extremes applied directly to the logic within each control module would be

Module	V5.6 @ Logic
A9	+4.47 to +5.47
A11	+4.52 to +5.52
A12	+4.47 to +5.47
A13	+4.46 to +5.45

The recommended voltage range for TTL series 5400 logic is given by the manufacturer as +4.5 volts to +5.5 volts, when operating over a temperature range from -55° C to _125° C. From this, it is obvious that the above calculated extremes are close enough to the recommended extremes to insure satisfactory operation of the logic in the VP Negate mode.

It has thus been shown that, when the Voltage Protect Negate command is given and the primary voltage is allowed to vary from -20 volts to -34.5 volts, the control system logic will respond coherently.

4.6.3.1.3 System Sub-Sequences.

a. Power On. - When the ERTS Recorder is in an Off mode, the DC/DC Converter is turned off and, as a result, all power is removed from the control system logic. When a new operating command is given, the DC/DC converter is turned on and logic power is reapplied. Since the TTL logic has no permanent memory of its own, it is necessary to prime it to a safe and meaningful state when power is applied. This priming is accomplished via the Power On sequences. Power On sequencing is complicated by the fact that, due to interaction, different areas of the logic must be primed for different periods of time. Thus, there are three distinct sub-sequences within the major Power On sequence (see Figure 4-141).

The first of these sub-sequences (incorporating one shot Z18, gates Z12, Z5, Z13 and associated components) insures that all mode and mode-associated flip-flops are powered on in an Off state. The second

[1]Assumed worst case loading is based on maximum TTL logic current drains given at 35° C for Vcc = +5.0 volts. The maximum current drain at 5.0 volts is totaled for each module and converted to an equivalent resistance. The actual voltage extremes of +5.04 volts and +6.16 volts are then applied to the equivalent load resistance in series with the series resistance of the input LC filter.

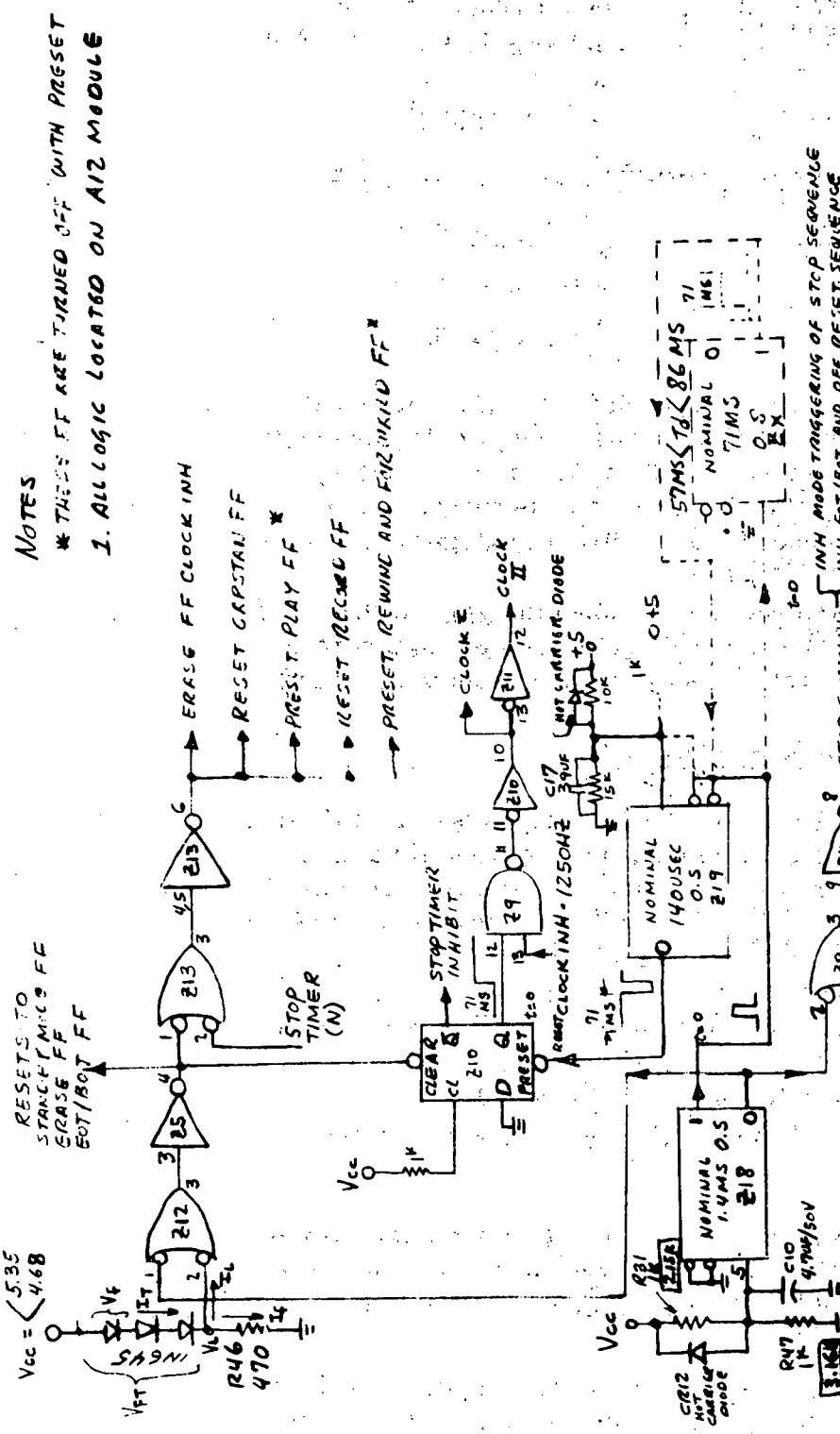

Figure 4-141. Power On Sub-Sequence Logic Diagram

sub-sequence, incorporating one shot Z18 and gates Z9 and Z11, locks out the Stop sequence trigger and enables an Off mode reset sequence. The third power on sub-sequence is of longer duration than the first two. Its purpose is to inhibit the clocking of mode flip-flops until all system one-shots are charged. A secondary function of the third sub-sequence is to provide a prolonged inhibit at the input to the Stop timer.

1. Sub-Sequence 1. - The first of the three Power On sub-sequences noted above is required to insure that every mode flip-flop is powered on in an OFF state. This is done by applying a power-on "low" to either the reset or preset input of each mode and mode-related flip-flop. The logic required to perform this conditioning includes one-shot multivibrator Z18, gates Z12, Z5, Z13 and associated components shown in Figure 4-141.

   With respect to one-shot Z18, it is obvious that the "0" output will power-on to a "high" and remain "high" until the voltage at the input capacitor (C10) is charged to a "1" level. When this occurs, the one-shot fires and the "0" output goes low for approximately 1.4 ms. (see Figure 4-142 waveform b). Analysis has shown (see Appendix G) that it is difficult to predict the turn on time of Z18 with any degree of accuracy. By using worst case parameters, the turn on time (as shown in Appendix G) will vary from 1.9 ms to 7.9 ms. It is for this reason that the Z18 "0" output is ORed with still another Power On reset at gate Z12.

   The diode Power On reset generated at Z12 is unlike the Z18 turn on reset, in that its duration and incidence is not directly related to time. As Vcc rises, Z12-2 remains at a logical "low" until Vcc is large enough to turn on the series diodes. This does not occur until after Vcc passes the "1" logical threshold for TTL logic (i.e., 1.0 to 1.8 volts over a 0° C to 60° C temperature range). As a result, Z13-6 is held "low" until after all logic has passed its threshold level. This "low" is used to either preset or reset each mode flip-flop to an OFF state (see Figure 4-142 for Power On waveforms).

   In the worst case analysis of the diode Power On reset, both minimum and maximum firing delay times were calculated. The maximum firing delay obviously occurs when VFT is maximum, Vcc is minimum and VL is maximum (see Figure 4-141). At the maximum firing point,

$$\overline{I_F} = \frac{\overline{V_L}}{R_{46}} = \frac{1.8}{385} = 4.67 \text{ mA.}$$

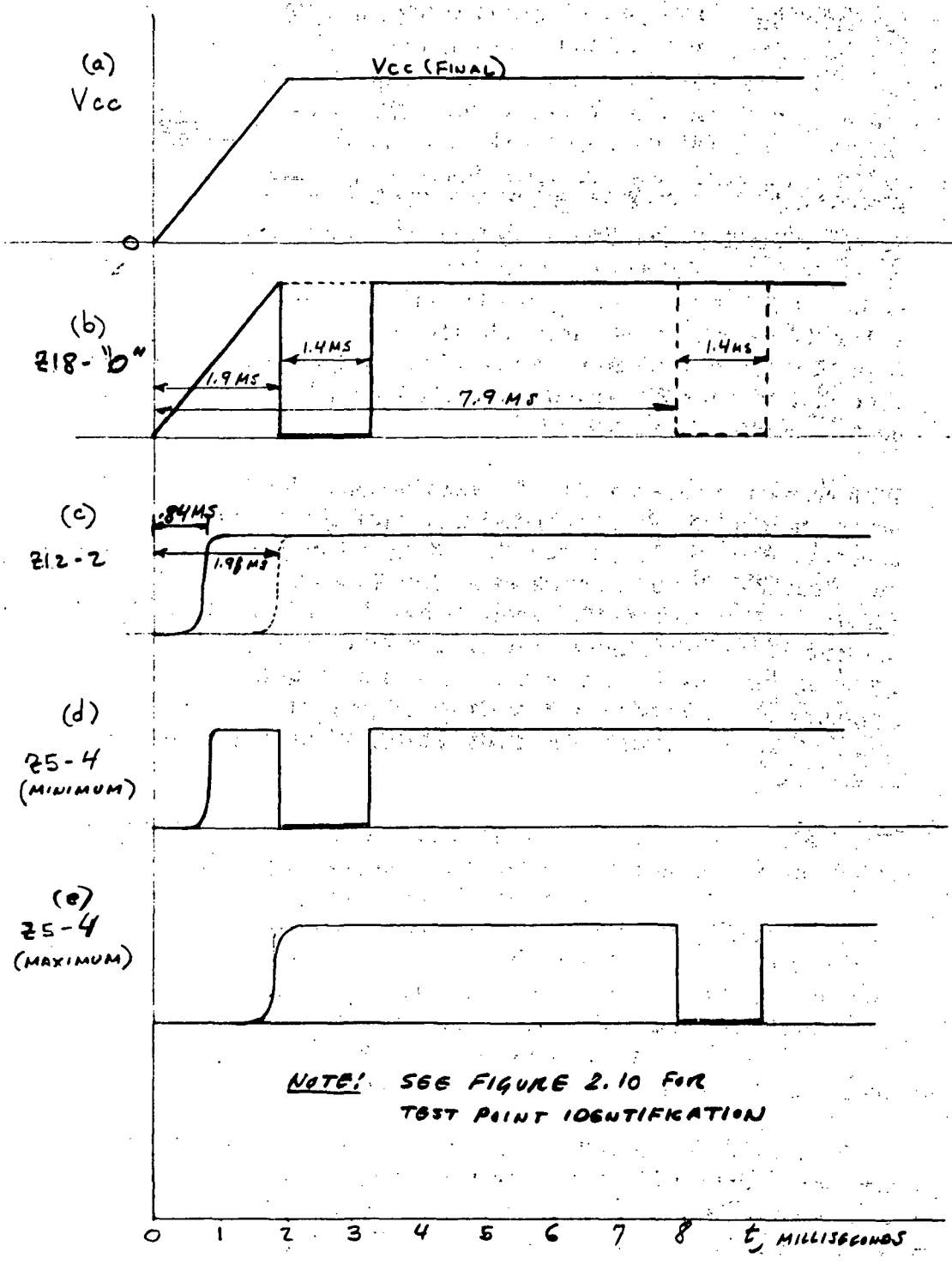

Figure 4-142. Mode Flip-Flop Power On Timing (Sub-Sequence 1)

and

$$\overline{I_T} = \overline{I_F} + \overline{I_L} = 4.71 \text{ mA.}$$

at 4.71 mA.,

$\overline{V_f}$ = 0.88 volt (from curves, assuming 0° C and TC = 2.2 mV/° C).

Thus,

$$\overline{V_{FT}} = 3 \times 0.88 = 2.64 \text{ volts.}$$

Therefore,

$$\begin{aligned} \overline{VL} \text{ (Final)} &= Vcc - \overline{V_{FT}} \\ &= 4.68 - 2.64 \\ &= 2.08 \text{ volts.} \end{aligned}$$

Thus it is seen that the maximum required firing level is exceeded under worst case conditions. As Vcc stabilizes in 2.0 milliseconds (substantiated by laboratory measurement), the maximum firing delay will then be 1.91 milliseconds.

The minimum firing delay requires that VFT be minimum, Vcc be maximum and VL be minimum (i.e., 1.0 volt). At the minimum firing point,

$$\underline{I_F} = \frac{\underline{VL}}{R_{46}} = \frac{1.0}{558} = 1.79 \text{ mA}$$

and,

$$\underline{I_T} = \underline{I_F} + \underline{I_L} = 1.82 \text{ mA}$$

at 1.82 mA,

$\underline{V_F}$ = 0.418 volt (from curves, assuming 60° C and TC = 2.2 mV/°C)

Thus,

$$\underline{V_{FT}} = 3 \times 0.418 = 1.254 \text{ volts}$$

The minimum firing delay can thus be calculated from:

$$t = \frac{2.254}{5.35} \times 2.02 \times 10^{-3} = 0.842 \text{ ms}$$

Thus, on power turn-on, the firing delay (Tp) of the diode reset will range from 0.84 ms to 1.91 ms.

When logic power is removed from the control system, it is imperative that all charging states be reduced to a quescent state before power is reapplied. If reference is made to Figure 4-141 (which shows the Power On sequence logic) it will be noted that there are two capacitors which must be fully discharged when logic power is removed (i.e., C10 and C17). When power is removed from the associated networks the guaranteed low input condition is restored to the one-shots via rapid discharge of the capacitors through a Schottky or hot carrier diode. The worst case or longest time discharge will obviously be associated with the largest capacitance; i.e., C17.

The curve of dynamic resistance Rd vs. diode current, I, is approximated from the data sheets by the relation,

$$Rd\ I = 63 \times 10^{-3}$$

This expression was obtained by approximating a typical curve given by the manufacturer.

With reference to Figure 4-141, the expression for the capacitor discharge current I as a function of time, t, after logic power is removed is:

$$I = \frac{Vcc}{Rd}\ e^{-t/2x10^{-3}} \cdot e^{-t/Rd\,C17} \qquad (1)$$

where Vcc = initial voltage on capacitor

$e^{-t/2x10^{-3}}$ assumes that logic power is reduced to zero with a time constant of 2×10^{-3} seconds after DC/DC Converter turn-off

The current through the diode after the supply voltage is reduced to zero can thus be determined by letting $t = 2 \times 10^{-3}$ in equation 1. The resultant current is 0.1 mA maximum. At this current the maximum worst case diode drop is +0.45 volts. Since 0.45 volts is less than

the minimum one-shot "1" threshold level of +0.8 volt, an input "low" is instantaneously guaranteed when logic power is removed from the control system. As a result, a normal Power On sequence will be generated when logic power is reapplied.

2. Sub-Sequence 2. - In a Power On sequence the "0" output of one-shot A12-Z18 is also employed to dub a 1.4 ms pulsed "Stop" Command signal (see Figures 4-135 and 4-141). This pseudo stop command performs two functions; namely,

   (a) forces J-K flip-flop A13-Z8 to power on in a reset condition;

   (b) pulses A13-Z9-4 "low" and then "high" to enable an Off mode reset.

   J-K flip-flop A13-Z8 is reset during the Power On sequence so as to unconditionally inhibit a mode generated Stop sequence. It does this by forcing a "low" at pin 12 of and gate A13-Z9. Since pin 13 is also held "low" during power turn on, it might therefore seem academic to hold pin 12 low as well. (The mode trigger circuits do not pulse on power turn-on.) However, in this regard, it should be realized that the only correct state for flip-flop A13-Z8 during Power On, is the reset state. The set state is only justifiable when Z8 is clocked there by a previous Run Tape mode (see Paragraph 4.6.1.3c).

   Sub-sequence 2 pulses pin 4 of AND gate A13-Z9 during power-on so as to enable a previous Off command to be reset (see Figure 4-135). It is imperative that a previous Off command be reset before the Stop timer inhibit (generated by power on sub-sequence 3) is removed. If the previous Off command is not reset during power turn-on, it will be reset later via an Off command instituted Stop sequence. However, if the Stop sequence is enabled, the reset which it produces will also reset the active command. As a result, the control system will not acknowledge the last operating command. The recorder will thus revert to an Off mode with the Off latching relay reset.

3. Sub-Sequence 3. - The third Power On sub-sequence (see Figure 4-141) is prolonged beyond that of either sub-sequence 1 or 2. Its direct purpose is to inhibit both the Stop timer and the mode flip-flop clock for approximately 55 ms after power turn-on.

The reason for inhibiting a Stop sequence during power turn-on was noted briefly in Paragraph 4.6.3.1.3b above, and is treated at length in Paragraph 4.6.3.1.3c.

The mode flip-flop clock I signal is inhibited in order to delay mode clocking until after all TTL logic one-shots have charged to a stable state. If the Power On clock inhibit were removed, the new operating command would be immediately clocked into the required mode flip-flop(s) as soon as the Power On sub-sequence 1 is terminated. This would, in turn, fire one-shots which had not yet charged to a stable state. The result would be greatly foreshortened one-shot period (see Appendix G for analysis). This would result in erratic performance which could conceivably damage the recorder.

The minimum duration of sub-sequence 3 is defined as the time required for the longest period one-shot to charge to a stable state after power turn-on. The longest period one-shot within the control system is the HW and Iω Start/Run timer. The period of this one-shot (as a function of power on charging time before firing) is plotted in Appendix G. With respect to this figure, it will be noted that the minimum worst case time required to assure HW and Iω motor acceleration to synchronous speed, is given as 3.5 seconds. This time was arrived at on the basis of laboratory test. If this minimum time is to be guaranteed in the worst case, the minimum worst case power on charging time must them be 52 milliseconds. This time defines the required minimum duration of Power On sub-sequence 3.

In order to achieve this relatively long power-on delay, it was at first decided to employ the same technique used to delay turn-on of A12-Z8 (see Figure 4-139). This required the addition of one-shot A12-Z19 with an associated input charging network which, on power turn-on, would delay turn on of Z19 for no less than 52 milliseconds. This would, in turn, delay turn on of flip-flop Z10 and, as a result, inhibit mode flip-flop clocking for a period of 52 ms.

By employing an analysis similar to that shown in Appendix G, it was shown (see Figure 4-143) that it is almost impossible to predict the turn-on delay of Z19 with any accuracy, if external RC charging is employed. With respect to the figure it will be noted that, if a minimum turn-on delay of 52 ms is to be guaranteed in worst case, an input charging capacitor of at least 140 uF would be required. This capacitor would unfortunately result in a ridiculously long turn-on delay if charging proceeded via the "$\bar{t}$ for maximum charging" curve.

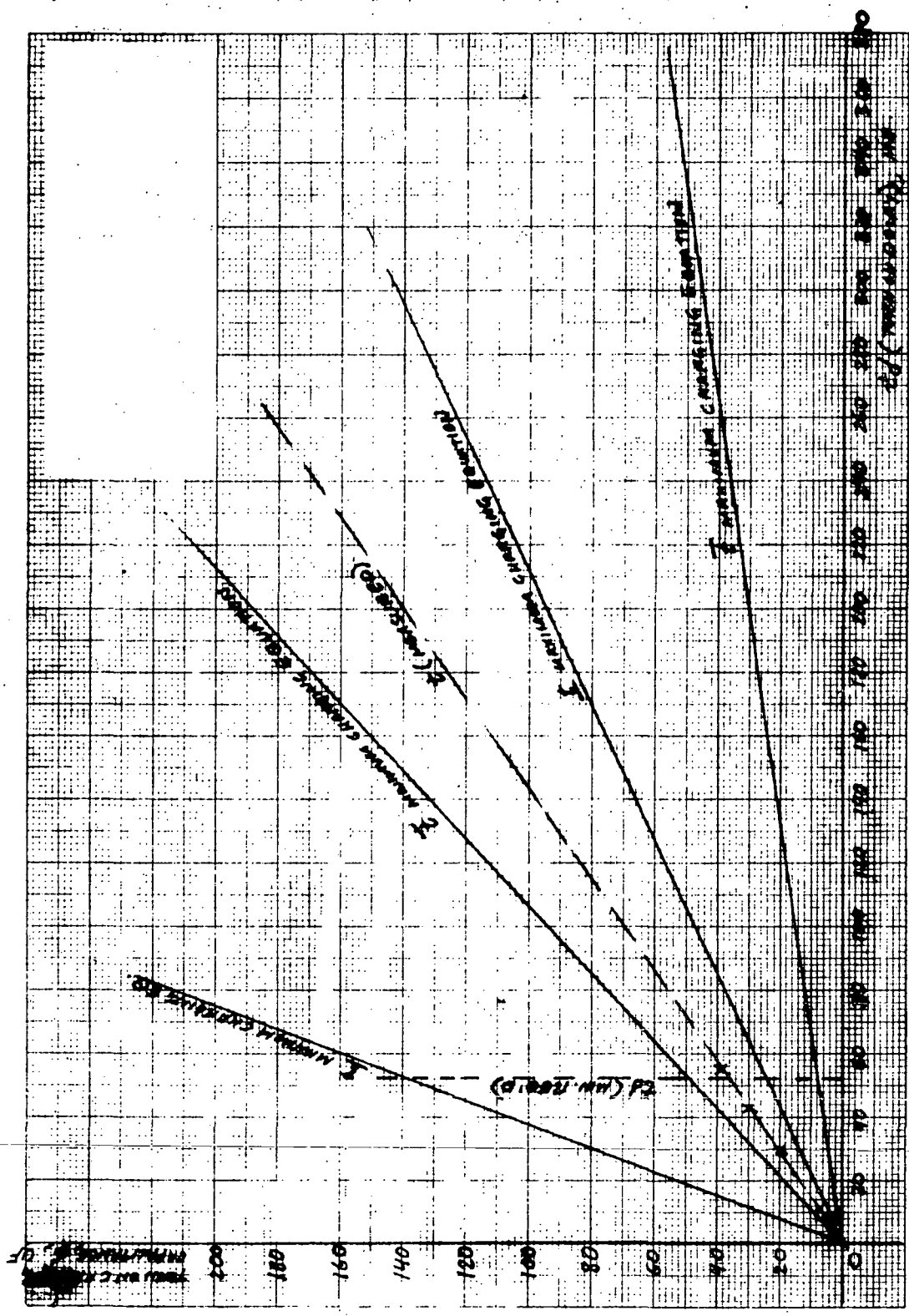

Figure 4-143. Delayed Turn On of SN54121 One-Shot Turn On Charging Capacitance vs. Turn On Delay

It was therefore recommended that the RC delayed turn on technique be abandoned in favor of one having a greater degree of delay certainty. A new technique was proposed which required the addition of still another one-shot, Z_X (see dotted signal path in Figure 4-141).

By adding Z_X the waveforms of Power On sub-sequence 3 will be as shown in Figure 4-144. With regard to this figure it should be noted that the resulting clock inhibit (curve d) during power turn-on, will vary from 59.9 to 94.4 milliseconds, assuming worst case conditions.

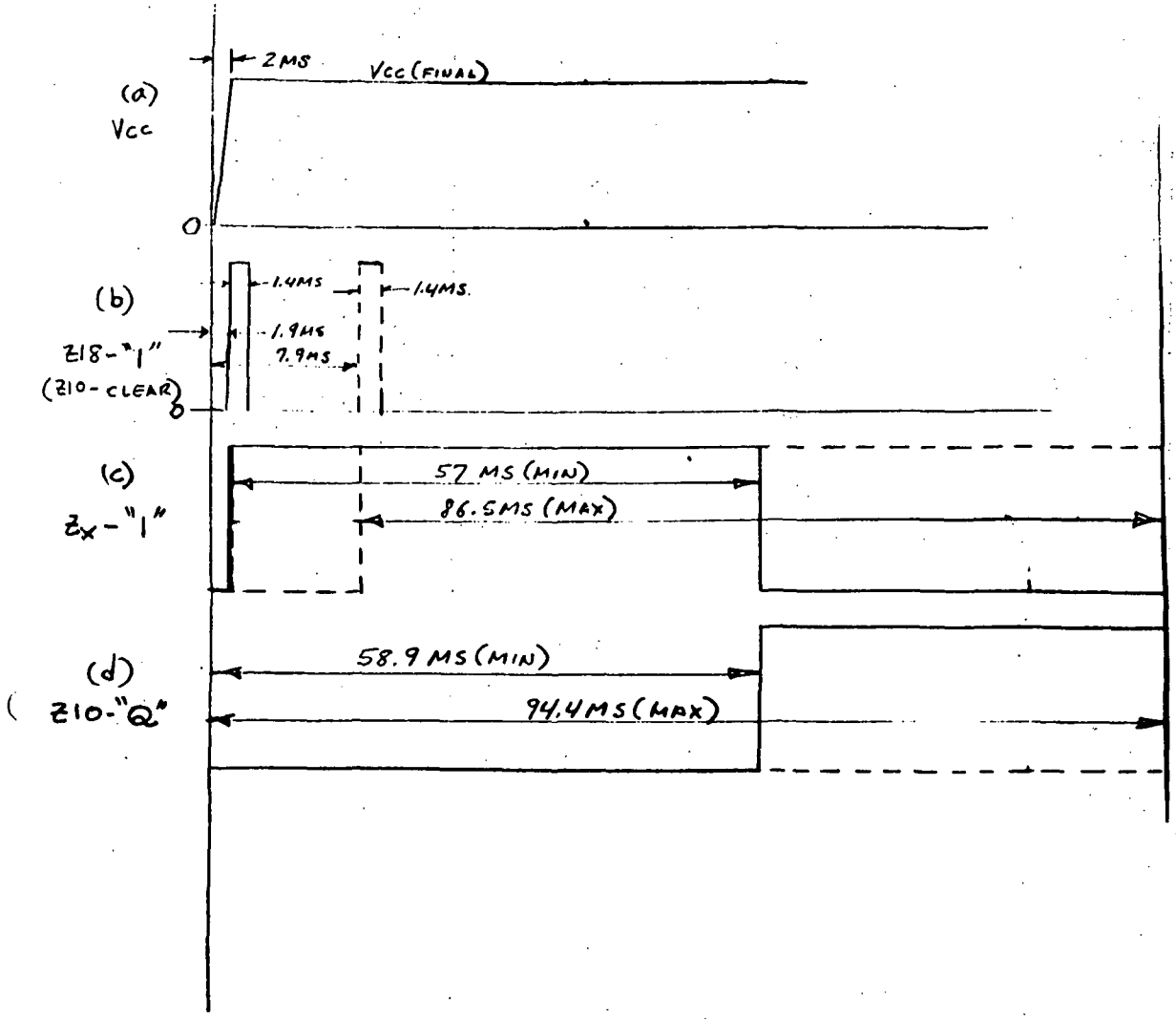

Figure 4-144. Power On Clock Inhibit Waveforms (Sub-Sequence 3)

b. Command Resets. - Since all input operating commands with the exception of RBV Run Tape interface with the recorder via latching relays, the control system must incorporate some means for resetting the previous command when a new command is given. This is accomplished via reset sequences which, when initiated, apply voltage to the reset coils of all command latching relays in common (see Figure 4-135). The duration of the reset sequences are timed to always fall within the active period of the last input command level. (The duration of the externally applied command level is specified as 45±5 milliseconds.) As a result, all command latching relays will be reset with the exception of that which is receiving the new operating command. Following the reset sequence the recorder will respond to the last operating command, and that command alone.

The reset sequence incorporates three distinct sub-sequences; namely,

(1) Normal mode reset sequence

(2) Off reset sequence

(3) Accelerated reset sequence

The normal mode reset sequence is the major sub-sequence, in that it is employed when cycling between operating modes other than off. The Off reset sequence is similar to the normal reset sequence, except that it is responsive only to an Off command or the EOT/BOT condition. The accelerated reset sequence is employed whenever primary power is removed and then re-applied to the control system (i.e., when an Off command is issued to negate a voltage protection fault or an Emergency Off mode).

1. Normal Mode Reset Sequence. -

Description. - The normal mode reset sequence is employed to reset the command latching relay of the previously active mode when cycling between operating modes other than Off (see Figure 4-135). It is initiated by any one of the seven mode trigger circuits. When a new operating command is given, the corresponding mode trigger circuit generates a positive-going pulse which propagates to A13-Z4-8, where it is applied to a reset timing network. The reset timing network consists of two one-shot multivibrators, A13-Z10 and A13-Z5. A13-Z10 is the main reset sequence timer, and fires as soon as A13-Z4-8 goes "high". This causes A13-Z10-6 to go "high" and remain "high" for approximately 12 milliseconds. When A13-Z10-6 goes "high",

transistor Q3 is turned on, thereby energizing relay K11. When the contacts of K11 close, voltage is applied to the reset coils of all command latching relays in common. When the 12 millisecond period of the main reset timer expires, Q3 is turned off, K11 is de-energized and its contacts open to terminate the reset sequence. When this occurs, the input command level is still applied to the last initiated operating command latching relay. As a result, this relay will remain in a set condition, and the recorder will cycle to a corresponding mode.

With reference to Figure 4-135, it will be noted that a second one-shot (A13-Z5), having a nominal delay of 54 milliseconds, is fired approximately 1.5 μs after the main reset timer. This one-shot serves two purposes: First, it disables the input circuitry of the main reset sequence timer, so as to enable only one reset sequence to be initiated per input command level period; secondly, it disables the mode flip-flop clock during the active period of the input command.

The inhibits generated by the A13-Z5 one-shot are needed because of the contact instability which results when, during the reset sequence, both the set and reset coils of the last initiated command latching relay are simultaneously energized. This phenomena can best be explained with the aid of a simple diagram showing the command latching relay mechanism (see Figure 4-145). With reference to the figure it will be noted that the command latching relay incorporates a permanent magnet and a balanced or floating armature. The armature is shown in the set position. If it is assumed that both the set and reset coils are not energized, then the armature will remain in the set position by virtue of the pulling force of the permanent magnet flux, $\emptyset C$. If voltage is applied to the set coil the armature will, of course, remain where it is. If, however, the reset coil is energized while the set coil is energized, the flux produced by the reset coil ($\emptyset_A$) will cancel that produced by the permanent magnet ($\emptyset_C$). As a result the armature will not experience a magnetic force and will be free to oscillate about its pivot point. When this condition exists, as it does during a normal reset sequence, the position of the contacts is uncertain.

As a result of this uncertainty it is possible for the input command latching relay to generate a second mode trigger pulse during reset. In the absence of the inhibit placed upon the main reset timer by the 54 ms mask timer, a second mode trigger

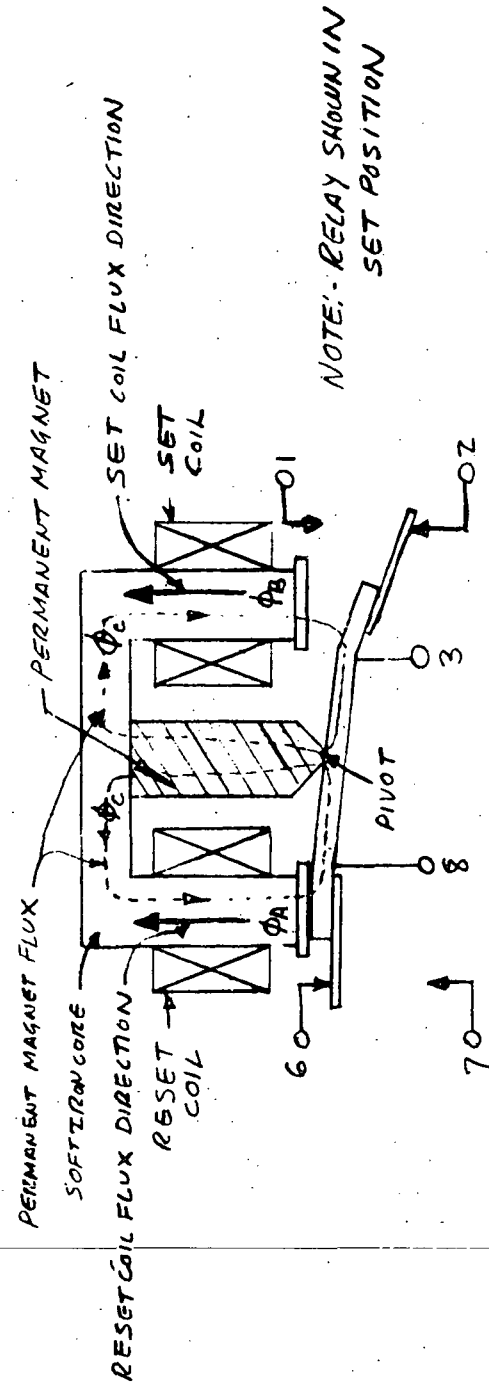

Figure 4-145. Command Latching Relay Mechanism

pulse could initiate a second reset sequence. A second reset sequence, in turn, would reset all operating commands and leave the recorder in an Off mode.

Analysis. - In analyzing the normal mode reset sequence, the following areas were investigated:

(a) Mask timer delayed turn on,

(b) Minimum and maximum reset times,

(c) Reset capability in worst case

When analyzing the delayed turn on of the mask timer, the equivalent circuit shown in Figure 4-146 was used. The voltage generator V (t) is employed to simulate the drive capability of the OR gate which pulses both the reset and mask one-shots. The expression for V (t) was obtained from manufacturers' data showing V out (1) Vs load current. The bracketed values for R56 and C17 show the extreme values which prevail over a temperature range from 0° C to 60° C. It should be noted that V_T(Z5) and V_T(Z10) refer to the input threshold voltages of one shots Z5 and Z10, respectively. When the expressions for time-to-threshold versus V_T(Z5) and time-to-threshold versus V_T(Z10) were derived and solved using worst case values, it was discovered that it was possible for the mask one-shot to fire before the reset one-shot. If this occurs, the mask will inhibit the reset one-shot, and a reset sequence will not be generated.

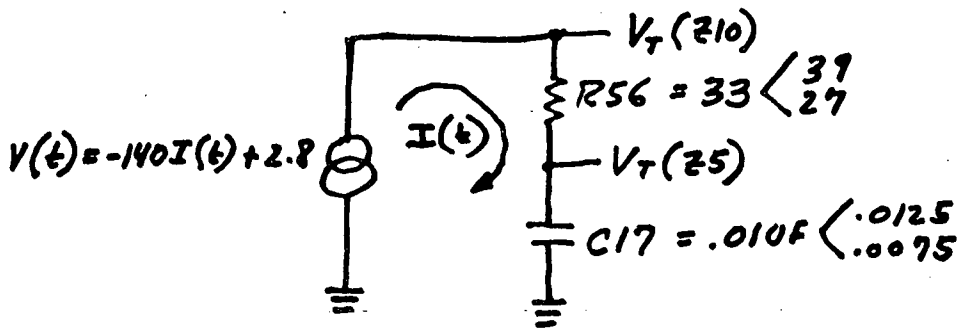

Figure 4-146. Reset Mask Timer Network

By increasing R56 from 33 ohms to 270 ohms the transient loading on the driver OR gate is reduced and, as a result, there will be no delay associated with the firing of the reset one-shot, Z10. As a consequence, Z10 will always fire before Z5.

Both the minimum and maximum reset times were calculated using worst case conditions. The minimum reset time was of interest, since it had to be long enough in the worst case to insure that the input command latching relays were always reset. The maximum reset time was of interest, since it had to be of shorter duration than the minimum input command level (i.e., less than 40 milliseconds). Table 4-47 shows the derivation of both the minimum and, maximum reset times.

With reference to the table, it is obvious that both the minimum and maximum reset time requirements are met. The minimum duration of the reset applied to the command latching relays is obtained as 11.5 ms, by subtracting the minimum time shown in step 5 from that shown in step 9. This time is more than adequate since the latching relays require an operate time of only 1.5 milliseconds. The maximum duration of the reset sequence is shown by step 9 of Table 4-47 to be 23.3 ms. This time is much shorter than the minimum input command period and, as a result, the new operating command will not be reset.

TABLE 4-47. NORMAL MODE RESET SEQUENCE TIMING

Event	Time (in milliseconds)
1. New mode command initiated	0
2. New mode contacts close	1.5/3.5
3. Reset timer fires	1.5/3.5 (Negligible Delay)
4. Q3 turns on	3.0/5.0
5. Relay K11 picks up (reset applied)	6.0/9.5
6. Previous command latching relay resets	7.5/11.0
7. Reset one-shot expires	11.3/17.1
8. Q11 turns off	11.5/17.3
9. K11 drops out (Reset removed)	17.5/23.3

With reference to Figure 4-135, it will be noted that the normal mode reset voltage is applied to all reset coils in parallel through a 47 ohm resistor in series with the primary supply voltage. The nominal resistance of each reset coil at 25° C is 1130 ohms ±10%. The minimum and maximum values of coil resistance over a 0° C to 60° C temperature range is determined by applying the equation,

$$R_f = R_i \left[1 + \alpha_i (t_f - t_i)\right]$$

where

R_f is the resistance at the temperature t_f

R_i is the resistance at the temperature t_i

αi is the temperature coefficient of copper at t_i.

Successive applications of this equation yield the resistance extremes for each reset coil of 919 ohms (at 0° C) to 1435 ohms (at 60° C). Since the reset voltage is applied to eight reset coils in parallel, the effective resistance will vary from 114.9 ohms to 178 ohms.

The pick-up voltage of the command latching relays is given by the manufacturer as 13.5 volts maximum at 125° C. At 125° C Rcoil = 1720 ohms. Thus Icoil (req'd) = 13.5/1720 = 7.84 mA. If it is assumed that relay pick-up is by ampere-turn requirement, then, for the per coil resistance extremes of 919 ohms and 1435 ohms, the pick-up voltage (V_{pu}) can be calculated as follows:

at 0° C $\quad V_{pu} = 919 \times 7.84 \times 10^{-3} = 7.2$ volts

at 60° C $\quad V_{pu} = 1435 \times 7.84 \times 10^{-3} = 11.25$ volts

If it is assumed that the "minimum" primary voltage is that which can occur in the VP Negate mode (i.e., -20 volts), the minimum available reset coil voltage can be calculated with the aid of Figure 4-147.

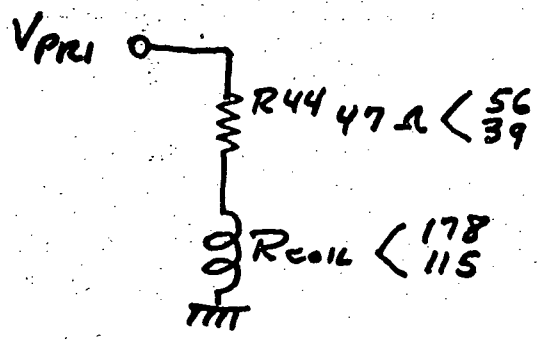

Figure 4-147. Normal Mode Reset Network

From the figure,

$$\underline{Vcoil} = \frac{\underline{Rcoil}}{\underline{Rcoil} + \overline{R}_{44}} \times 20.0$$

$$= \frac{115}{171} \times 20$$

$$= 13.4 \text{ volts}$$

Since $\underline{Vcoil} > V_{PU}$ (required), the reset capability is guaranteed in the worst case.

2. The Off Reset Sequence. - The Off Reset sequence is employed to:

   (a) Reset a previously set in Off command while a Power On sequence is in progress, following the initiation of an operating command other than Off.

   (b) Reset the previous operating command when an Off command is initiated. This sub-sequence will also reset the Off command latching relay.

   (c) Reset the previous operating command when the EOT/BOT flag is set.

The Off Reset sequences are unlike the normal reset sequences in that they are not initiated via a mode trigger circuit. Off Reset sequences are initiated via entrance through the Stop sequence loop, or via a Power On sequence (See Figure 4-135. With reference to the figure, it will be noted that both the Off command and the EOT/BOT flag gain entrance to the Stop sequence loop via OR gate A13-Z4.

The role of the Power On sequence in generating an Off reset sequence will become clear in the discussion to follow.

If it is assumed that the Off command latching relay is set when an operating command other than Off is given[1], a Power On sequence is generated (See Paragraph 4.6.3.1.3a). The Power On sequence pulses pin 4 of AND gate A13-Z9 "low" and then "high". While this is occurring the pin 5 input to the AND gate is powered on to a "high", and held "high" by the presence of an Off command "low" at pin 5 of OR gate Z13-Z4. Thus, when pin 4 of the AND gate goes "high", pin 6 of A13-9 goes "low" to fire the reset timer. The requirements for the Off reset sequence, so initiated, are that it be completed before the newly applied operating command level goes low. (The minimum time allowance is 40 milliseconds.) The maximum period of the Off reset sequence is shown in Table 4-46.

With regard to the table it will be noted that the maximum worst case time required to execute the reset sequence approaches, but does not exceed, the minimum duration of the externally applied operating command.

If an Off command is given while the recorder is in another operating mode, a reset sequence is not generated immediately (See Figure 4-135). The Off command forces a "high" at the pin 5 input of AND gate A13Z9, and also fires the Stop timer. The Stop timer enables the Stop sequence which disconnects tape drive, and applies braking to the capstan motor (See Paragraph 4.6.3.1.3c for analysis of Stop sequence).

When the Stop timer is fired, the pin 4 input of AND gate Z13-Z9 is driven "low" before the Off command input to pin 5 goes "high". At the end of the Stop sequence, pin 4 is driven high; this transition fires the reset timer. The reset timer resets not only the previous operating command, but the Off command as well. Then, in the absence of an active operating command, the DC/DC Converter is turned off and the recorder reverts to an Off mode with the Off latching relay reset.

If the EOT/BOT (Off) flag is set while the recorder is in an active operating mode, an Off reset sequence is generated. This sequence is identical to that produced when an Off command is given to negate a previous operating mode.

[1]The Off command latching relay is always left in a set condition when an Off command is given to negate either an Emergency Off command or a Voltage Protect Fault condition.

3. Accelerated Reset Sequence. - The Accelerated Reset sequence is employed to reset all previous operating commands whenever primary power is re-applied to the recorder (i. e., when an Off command is issued to negate either a Voltage Protection Fault or an Emergency Off mode). (Note that this sequence can also occur when the VP Negate command is active.) This sequence does not employ the reset timer or, for that matter, any of the control system TTL Logic. It instead employs an RC charging network which is connected in series with the reset coils of the command latching relays (See Figure 4-135). The equivalent circuit of the accelerated reset sequence network is shown in Figure 4-148. Analysis of this circuit shows that when V_{PRI} is re-applied to the network, the expression for the voltage across the reset coils is:

$$VR(t) = \frac{R2}{R_1+R_2} V_{PR1} + \left(\frac{C1}{C_1+C_2} - \frac{R1}{R_1+R_2}\right) V_{PR1} \epsilon^{-t \frac{R_1R_2}{R_1+R_2}(C_1+C_2)} \quad (1)$$

With reference to this equation the expression for $V_R(t)$ at t=o and $t=\infty$ can be shown to be:

$$V_r(t_o) = \frac{C1}{C_1+C_2} \times V_{PRI} \; V_{pri} \quad (2)$$

$$V_r(t\infty) = \frac{R2}{R_1+R_2} \times V_{PRI} \; V_{pri} \quad (3)$$

The curve for $V_R(t)$ as a function of time after primary power is re-applied, will then be as shown in Figure 4-149.

In analyzing the accelerated reset network, it was necessary to answer the following questions: (1) Does the network reset the previous command latching relay(s) in the worst case ?, and (2) Is the accelerated reset effectively removed from the reset coils when $V_R(t)$ equals $V_R(\infty)$?

Before either of these questions could be answered it was necessary to determine the worst case relay pick-up voltage requirements.

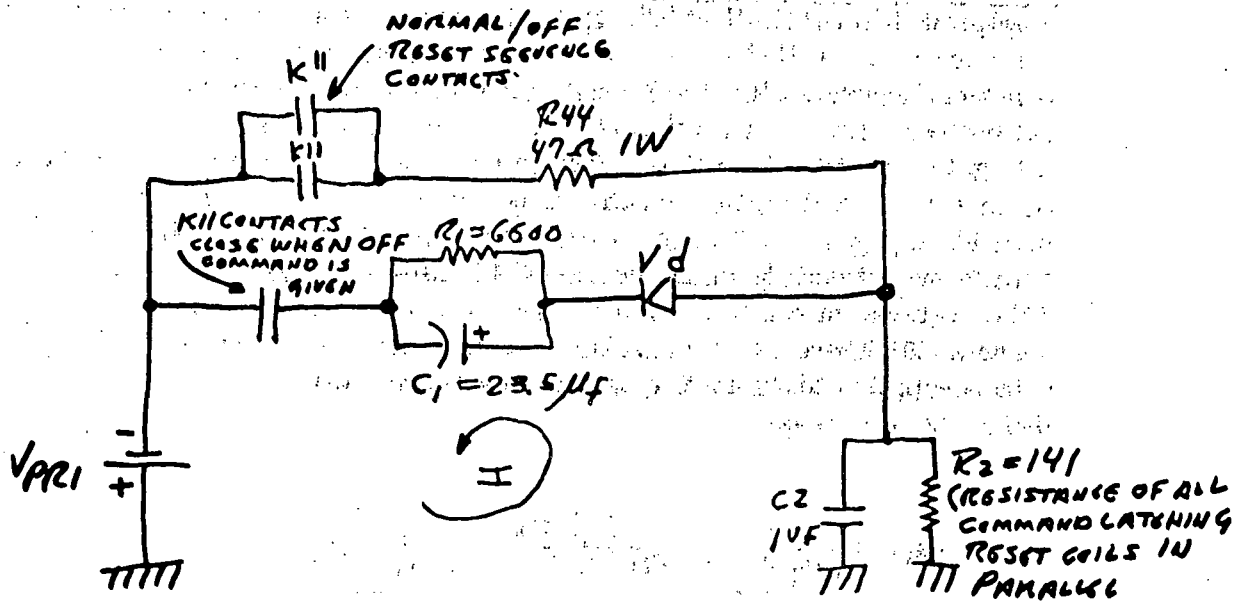

Figure 4-148. Accelerated Reset Network

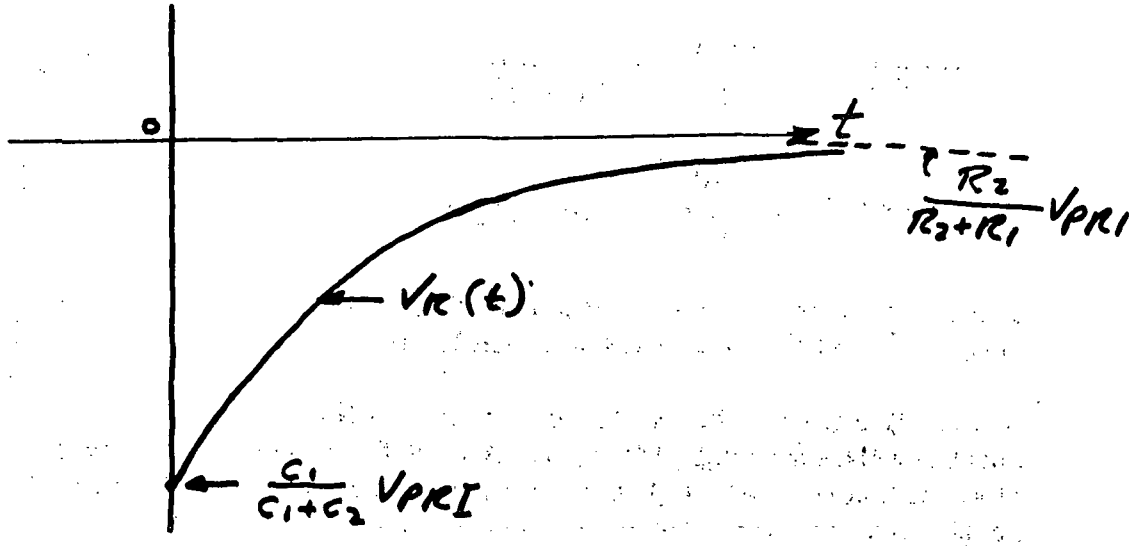

Figure 4-149. Accelerated Reset Pulse

MIL-R-5757/71 specifies a maximum pickup voltage of 13.5 volts at 125° C. Since this is a maximum value, it implies that the coil resistance is also maximum. The maximum coil resistance at 125° may be calculated from:

$$R_f = R_i \left[1 + \alpha i^{(T_f - T_i)}\right]$$

where

R_i = maximum coil resistance @25° C (Given as 1243 ohms)

R_f = maximum coil resistance @ 125° C

αi = temperature coefficient of copper

T_f = 125° C

T_i = 25° C

Substitution of values yields a maximum coil resistance of 1720 ohms @125° C. If it assumed that relay pick-up is by ampere-turn requirement, it is thus possible to calculate the current requirement at 125° C, and apply this value at any other temperature. If this is done for the 0° C and 60° C temperature extremes, the resultant pick-up voltages will be:

at 0° C $\quad 8.82 \text{ Volts} \geqq V_R \text{ (Pickup)} \geqq 7.20 \text{ Volts}$

at 60° C $\quad 11.25 \text{ Volts} \geqq V_R \text{ (Pickup)} \geqq 9.21 \text{ Volts}$ (4)

If equations (2) and (3) are solved using worst case values in modes other than V_P negate $V_R(t\infty)$ will assume the following values:

At 0° C, $\quad 24.25 \text{ Volts} > /V_R(t_o)/ > 22.65 \text{ Volts}$

At 60° C $\quad 24.4 \text{ Volts} > /VR(t)/ > 22.9 \text{ Volts}$ (5)

And,

At 0° C $\quad 0.64 \text{ Volt} > /VR(to)/ > 0.35 \text{ Volt}$ (6)

At 60° C $\quad 0.81 \text{ Volt} > /VR(t)/ > 0.44 \text{ Volt}$

Inspection of sets 4 and 5 will show that, in the worst case, the pick-up voltage is always achieved when primary power is re-applied to the accelerated reset network.

Comparison of sets 4 and 6 will show that, in the steady state condition, the pick-up voltage is effectively removed.

If the pick-up voltage values given in set 4 are substituted into equation 1, it is possible to solve for the total time that an effective pick-up voltage is applied to the reset coils. The minimum and maximum reset times arrived at in this way are 2.21 milliseconds and 4.63 milliseconds, respectively. Since 2.21 milliseconds is greater than the operate time of the command latching relay (i.e., 1.5 milliseconds) a reset is always guaranteed.

If equations 2 and 3 are solved using worst case values in the VP Negate mode, where the ambient temperature in the VP Negate mode is specified as 35° C, $V_R(to)$ and $V_R(t\infty)$ will assume the following values:

$$19.0 \text{ Volts} < /V_R\ (t_o) / < 33.6 \text{ Volts} \quad (7)$$

$$0.33 \text{ Volts} < /VR\ (t\ ) / < 1.0 \text{ Volt} \quad (8)$$

The required pick-up voltage V_{RPU} at 35° C is:

$$8.28 \text{ Volts} < V_{RPU} < 10.1 \text{ Volts} \quad (9)$$

Inspection of sets 7 and 9 will show that, in the VP Negate mode, the pick-up voltage is always exceeded when primary power is re-applied to the accelerated reset network.

Comparison of sets 8 and 9 will show that, in the steady state condition, the reset pick-up voltage is effectively removed.

Once again, if the pick-up voltage values given in set 9 are substituted into equation 1, it is possible to solve for the total time that an effective pick-up voltage is applied to the reset coils. The minimum reset time arrived at in this way is 1.75 milliseconds. Since 1.75 milliseconds is greater than the relay operate time (i.e., 1.5 ms), a reset is always guaranteed.

c. Stop Sequence. - The ERTS control system initiates a stop sequence whenever,

(1) A Run Tape mode is negated by another mode which requires a change in tape speed and/or direction.

(2) An Off command is given, except when it is given to negate an Emergency Off mode or a VP Fault condition.

(3) The EOT/BOT Off flag is set.

(4) The RBV Run Tape command is released.

The heart of the Stop sequence is the Stop timer (see Figure 4-135) which, when fired by one of the events listed above,

(1) Inhibits all Run Tape mode and Run Tape mode-related flip-flops.

(2) Resets the Lap command latching relay.

(3) Applies power to the capstan brake via the capstan brake driver.

(4) Generates an Off reset sequence whenever the EOT/BOT Off flag is set, or an Off command is initiated. (Note that a stop sequence is never generated when an Off command is given to negate either an Emergency Off mode or a VP fault condition. It is impossible to do so since logic power is not available when the Off command is given.)

When the ERTS recorder is in a Run Tape mode and another command is initiated which requires a change in tape speed and/or direction, the appropriate mode trigger circuit applies a 250 to 900 sec logical "low" to the input of OR gate A13-Z7 (see Figure 4-135). With reference to the figure, it will be noted that the Record or Play mode trigger is disabled if the previous operating mode was Record or Play.

When one of the inputs to A13-Z7 goes "low", it forces a "high" at pin 13 of AND gate A13-Z9. The second input to the AND gate is primed to a "high" by J-K flip-flop (A13-Z8), only if the previous mode required tape movement.

When both AND gate inputs go "high", a positive-going pulse appears on the Stop signal line. The Stop pulse is first sent out to fire a 25 ms one-shot in the capstan motor winding control logic (see Figure 4-137). The 25 ms

one-shot is incorporated to delay the transfer from high speed to normal speed windings, until after the capstan motor drive has been removed. When the Stop signal pulses "high", the Stop timer is fired.

In addition to performing the functions noted earlier, the Stop timer forces the Stop Command signal to a "low" for the duration of the Stop sequence. A "low" on the Stop Command line resets the Stop sequence enabling flip-flop A13-Z8, and inhibits the Off reset AND gate A13-Z9. The entire sequence of events is clarified if reference is made to Figure 4-150a.

If an Off command is given when the recorder is in a mode other than Off, Emergency Off or VP Fault, a Stop sequence is initiated by the Off command latching relay. Relay contacts force a "low" at pin 5 of OR gate A13-Z4 which, in turn, fires the Stop timer. While the Stop sequence is in progress, the Off reset AND gate A13-Z9 is inhibited as shown in Figure 4-150b. When the Stop timer expires, pin 4 input to AND gate A13-Z9 goes "high" to initiate a reset sequence (see Paragraph 4.6.3.1.3b2). The reset sequence disconnects logic power by resetting all operating command latching relays, including Off.

When the recorder is in a Run Tape mode and the EOT/BOT Off flag is set, the control system reacts by instituting a Stop sequence followed by a reset sequence which removes logic power from the control system. In short, the events are identical to those which occur when an Off command is initiated.

When the recorder is in a RBV Run Tape mode and the RBV Run Tape command is released, the pin 3 input to the Stop timer goes "low" to initiate a Stop sequence. When the Stop timer expires, the recorder reverts to an RBV Enable mode (see Paragraph 4.6.3.1.2a6).

With reference to Figure 4-135 it will be noted that the Stop timer is inhibited during a Power-On sequence. If it is assumed that an operating command is given with the Off command latching relay set, it is required that the Off command be reset before the new input command level is removed. It is therefore imperative that the pin 1 input to OR gate A12-Z9 be held "high". When pin 1 is held "high", the Power On/Off reset signal will effectively generate a reset sequence via AND gate A13-Z9 (output pin 6). If the Stop timer were not inhibited during Power On, it would be fired by the Stop signal. The Off command latching relay would not be reset then until the Stop timer had expired. If a reset sequence is generated at this time it would reset not only the Off command latching relay, but all other command latching relays as well.

TO BE REVISED

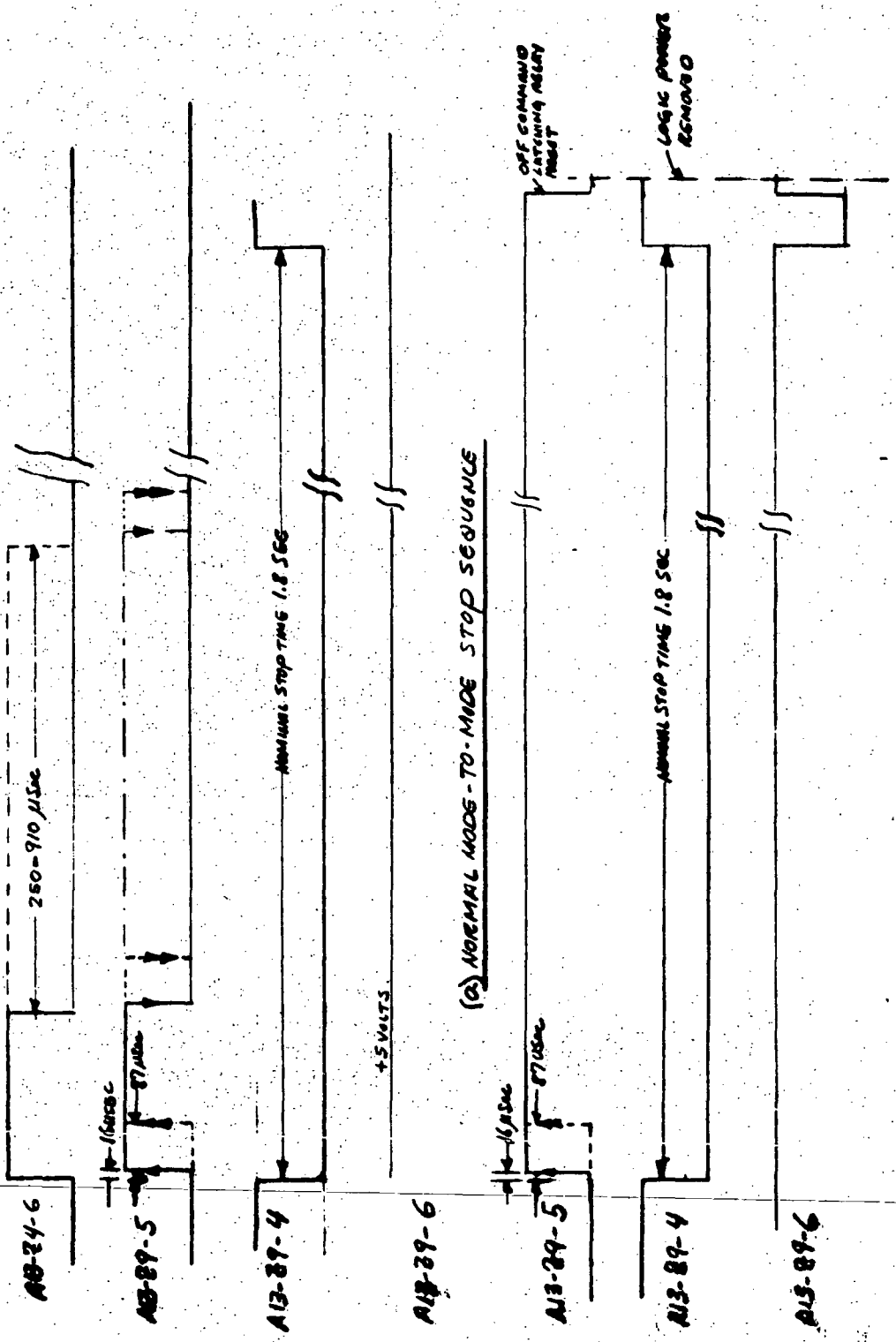

Figure 4-150. Timing Diagrams Stop Sequence

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d. EOT/BOT. -

1. Description. - The ERTS recorder incorporates four switches to signal the beginning and end of tape conditions, namely BOTP, BOTS, EOTP and EOTS (see Figure 4-137). As the end of tape is approached in a Forward Run mode, the EOTP (end of tape - primary) switch closes. This closure sets the EOT/BOT flip-flop, providing the Lap mode is not active. If the Lap mode is active, the EOTP signal is inhibited and tape movement continues until the EOTS (end of tape - secondary) switch closes. When this occurs, the EOT/BOT flip-flop will be unconditionally set.

   If the recorder is operating in a Rewind mode and the BOTP (beginning of tape - primary) switch closes, the EOT/BOT flip-flop will be unconditionally set. If, for any reason, the BOTP switch does not close, the tape will continue to rewind until the BOTS (beginning of tape - secondary) switch closes. When this occurs, the BOT/EOT flip-flop will be set.

   When the BOT/EOT flip-flop is set, the EOT/BOT (Off) signal line goes "low". This "low" is applied to the Stop/Reset/Off control logic (see Figure 4-135), where the effect is identical to that produced when an Off command is given. That is, a stop sequence is initiated and followed by a command reset and a DC/DC Converter disconnect.

   If the recorder was turned off by an EOT flag, and an operating command other than Off is given, the EOT/BOT flip-flop will be powered on in a reset condition via the Power On sequence. If the operating command is one which does not require forward tape motion, the EOT/BOT flip-flop will not be set and the recorder will achieve the mode selected. If, however, the selected operating mode is one which requires forward tape motion, (and assuming that the Lap mode is not active) the appropriate tape motion mode flip-flop will be turned on following the Power On sequence. When this occurs the EOT/BOT flip-flop will be set once again, and the cycle of Stop, Reset and DC/DC Converter disconnect will be repeated. There is no net forward motion of the tape during this time, since the Stop sequence automatically inhibits the Capstan and Forward mode flip-flops (see Figures 4-134 and 4-137).

   If the recorder is turned off by a BOT flag, and a Rewind mode is selected, the EOT/BOT flip-flop will be reset by the Power-On sequence; however, once the Rewind mode flip-flop is turned on (i.e., at the end of the Power-On sequence), the EOT/BOT flip-flop will be

set once again. The cycle of Stop, Reset and DC/DC Converter disconnect will then be repeated. Once again there will be no net tape movement, since the Rewind mode flip-flop is turned off by the Stop sequence. Although the Rewind mode flip-flop must be turned on before the Stop sequence can occur, the capstan motor driver turn-on is delayed by 25 milliseconds from Rewind flip-flop turn-on (see Figures 4-134 and 4-137). Since the Stop sequence is initiated long before the 25 ms one-shot expires, the capstan motor drive will be disabled before a connection is actually made.

2. Analysis. - The analysis of EOT/BOT turn off is similar in many respects to the turn off produced by insertion of an Off command. As a matter of fact, once the EOT/BOT flip-flop is set, the chain of events which occur is identical to that which takes place when an Off command is given. The logic required to set the EOT/BOT flip-flop while the recorder is running in a Forward tape mode is fairly straight-forward, inasmuch as there are no potential race conditions, and no ambiguities.

When the recorder is turned off by an EOT/BOT condition and an unallowed operating command is given, the resetting of the EOT/BOT flip-flop is straightforward. (Unallowed is used here to mean a mode which will reinstate either the EOT or BOT condition.)

If, for some reason, the EOT/BOT flip-flop were powered on in a set condition, the situation would be similar to the case which exists when an operating command is given with the Off command latching relay set. The main difference is that the EOT/BOT flip-flop, unlike the Off command latching relay, is not resettable. (Except, of course, by a Power On sequence.) The result is a Stop sequence generated at the end of the Power On sequence. This in turn, produces a reset sequence which disconnects the DC/DC Converter.

4.6.3.1.4 Special Considerations.

a. Primary Power Transients. - In Paragraph 4.6.3.1.3.c the operation of the ERTS control system was evaluated in the Voltage Protect Negate mode. A portion of the analysis of this paragraph dealt with the effects of primary power under-voltage and over-voltage extremes of -20 volts and -34.5 volts, respectively. The conclusion was reached at that time that the control system logic will respond coherently when these voltage extremes are applied to the recorder.

In addition to withstanding the primary power voltage extremes of -20 volts and -34.5 volts in the VP Negate mode, the ERTS recorder is also required to withstand primary power voltage transient extremes of -18 volts and -39 volts for a period of 35 milliseconds, when primary power regulators are switched.

With regard to the maximum limit of -39 volts, it is immediately apparent that thermal stress is insignificant because of the short duration of the transient. Direct breakdown is also remote since relays which operate from the primary power source are rated for maximum voltage on the basis of thermal considerations. With regard to over-stressing at the DC/DC Converter, it should be noted that the 5.6V converter output voltage is limited to +10% of its nominal voltage by a zener diode over-voltage suppressor.

If the magnitude of the primary power voltage drops to 18 volts, the reflected TTL logic voltage will fall below the minimum allowable limit of +4.5 volts. It is difficult to predict how the control system logic will react when this occurs. Because of this uncertainty, the DC/DC Converter has been designed to turn off when the primary power voltage falls to -18 volts. As a result, all power to the control system logic is removed approximately 70 milliseconds after the -18 volt step occurs. It remains off until the normal primary power voltage has been restored. When this occurs, the DC/DC Converter turns on and automatically re-applies logic power to the control system. The control system reacts by instituting a normal Power On sequence, followed by a return to the previous operating mode.

b. Command Rates. - The control system logic of the ERTS recorder will respond coherently to command rates up to 10 per second; however, it is not generally advisable to operate the recorder for long periods of time at rates which approach this maximum allowable figure.

To begin with, there is a real danger of overheating the headwheel, Iω and/or capstan motors if they are operated for long periods of time with power applied to their start (i.e., low impedance) windings. It is difficult to predict a maximum permissable command rate in this case, without just performing a thermal stress analysis on the motors in question. Such as analysis is beyond the scope of the control system worst case analysis.

Finally there is the deleterious effect which maximum command rates have on the life of electromechanical components in particular. Constant stressing of such components is an open invitation to fatigue and early failure.

c. Multiple Commands. - Whenever two distinct units interface via isolated parallel entry command lines, some priority must be established to protect the driven unit from the ambiguity of multiple input commands. Since the ERTS controller does not establish this priority, the control system of the ERTS recorder must. The control system establishes a protective priority by employing unconditional mode flip-flop inhibiting logic. If the mode and mode-related flip-flops shown in Figures 4-133, 4-134 and 4-137 are examined, it will be apparent that the following priority exists when multiple commands are received:

Mode	Priority Level
Off	1
RBV Enable	2
MSS/RBV Standby	2
Rewind	2
Forward	3
MSS/RBV Play	4
Record/RBV Run Tape	5

With reference to the priority list, it will be noted that the OFF command takes precedence over all other operating commands. The second level commands, consisting of Standby modes and Rewind, are autonomous with respect to each other, except insofar as MSS VS RBV status are concerned. Since the MSS and RBV status of the recorder is established via set and reset coils of a common latching relay (see Figure 4-133), it is impossible to establish an MSS vs RBV priority. The uncertainty which results when both the set and reset coils of the MSS/RBV relay are energized has been discussed in Paragraph 4.6.3.1.3b1.

With respect to the high speed modes, it will be noted that the Rewind mode takes precedence over the Forward mode. This precedence is established by the high speed mode-related flip-flops shown in Figure 4-137. With reference to this figure, it will be noted that the high speed flip-flop is set for both the Rewind and Forward modes, while the Rewind flip-flop is not. As a result, when Rewind and Forward commands are simultaneously applied to the recorder, the Rewind mode will take precedence.

With reference to Figure 4-134, it will be noted that all Record modes are inhibited by a Play command. As a result, the Play command will take precedence over a Record command when both are issued simultaneously.

It will be noted that both the Record and Play commands are autonomous with respect to Standby commands. A singular exception here is in the case of the RBV Enable command which, because of its record orientation, inhibits, and therefore takes precedence over a Play mode command.

So far we have only discussed the effects of operating command multiplicity, and here again only for the case when multiple commands are issued in a coincident fashion. If multiple operating commands are issued in a non-coincident (i.e., overlapping) fashion, it is possible, depending on the magnitude of overlap and command durations, for the recorder to ignore the leading command and coherently respond to the trailing command. For this to take place it is required, first of all, that a reset be initiated when the multiple commands are given. This restriction automatically excludes cycling from a Power Off status where the Off latching relay is reset (see Paragraph 4.6.3.1.2a9). Secondly, it is required that the leading edge of the trailing command be able to generate <u>its own</u> reset sequence. To do this, it must occur after the reset sequence produced by the leading operating command, has expired. All of these conditions reduce the maximum allowable overlap to 48% of the 45 ms nominal command period. This figure is arrived at with the aid of the times given in steps 2, 3 and 9 of Table 4-47.

The ability of the recorder to protect itself against the ambiguities of multiple operating command is of far greater importance than the mode status achieved. From the above it is apparent that, if two or more operating commands are received, the recorder will acknowledge receipt of the ambiguity (via telemetry returns), and then proceed to cycle to the mode with the highest priority.

If one of the multiple command inputs to the recorder is a special command, the condition is either allowed (as in the case of Voltage Protect Set, Lap and VP Negate commands), or employed to disconnect the recorder from the DC/DC Converter (as in the case of the Emergency Off command). In either case the recorder is protected, and no damage can occur.

If two or more special commands are applied to the recorder, there is no ambiguity unless those commands are VP Negate and VP Set (see Figure 4-139). If the VP Negate and VP Set commands are given in a coincident fashion, the recorder will respond to neither. If, however, they are given in an overlapping fashion, the recorder will respond to the trailing or last initiated command.

d. Repeated Commands. - The ERTS control system will ignore repeated commands for all modes except RBV Run Tape. This capability is an inherent outcome of latching relay command interface between the controller and the recorder.

In as much as the RBV Run Tape command is a continuous function (i.e., not pulsed), it must have continuous access to the control system of the recorder (see Paragraph 4.6.3.1.2a6).

e. Mode Telemetry. - The control system incorporates 10 digital mode telemetry drivers within control modules A9 thru A13 inclusive. The specifications for each telemetry output are as follows:

(1) Output Level

Absence of command ("0" state) = 0 to -1 volt
Presence of command ("1" state) = -5 to -10.0 volts

(2) Output Impedance

50,000 ohms maximum

Although the TM RBV Run Tape command conforms to these specifications it is not derived in common with the other mode telemetry. As a result, its analysis is treated in a separate section of this report (see Paragraph 4.6.3.2.2b).

In the original plan the mode telemetry circuits were powered from the primary power supply as shown in Figure 4-151. With reference to this figure it will be noted that in an Emergency Off mode or VP Fault condition, the 301 ohm trickle charging resistor was inserted between the

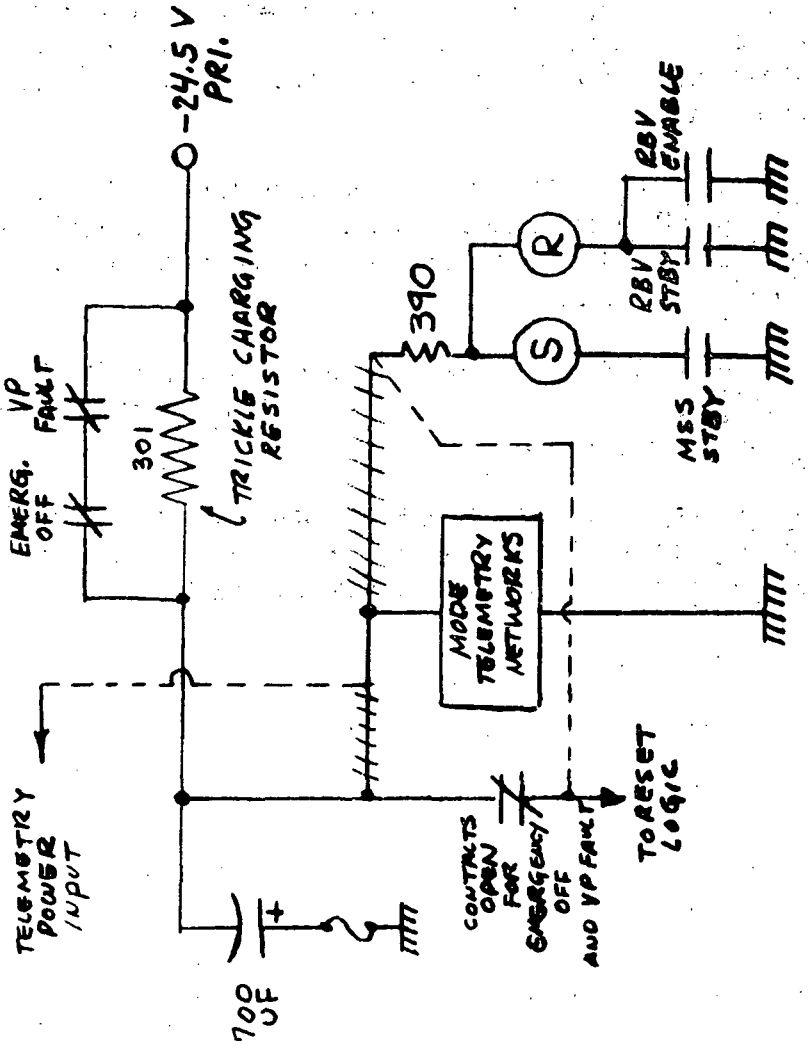


Figure 4-151. Power to Mode Telemetry

primary power input and the mode telemetry circuits. Moreover, it will be noted that, when an Emergency Off mode or VP Fault condition existed, the voltage at the mode telemetry circuits was much more positive than -24.5 volts ±2%. This was largely due to the current requirement of the set coil of the MSS/RBV status relay. As a result, it was impractical to contain the telemetry outputs within proscribed limits for both the normal condition (i.e., when the trickle charging resistor is shorted), and for the exceptional condition when it was not. As a result, two courses of action were suggested. Firstly, it was suggested that the MSS/RBV status set coil be returned to -24.5V primary power via the path shown dotted. This would remove the coil load from the -24.5 volt primary supply when Emergency Off or VP Fault were preset. Moreover, it was decided that the mode telemetry should be removed from the primary power supply and referenced instead to the telemetry power supply. This would dis-associate the trickle charging resistor from the mode telemetry circuitry. The worst case analysis of the mode telemetry was then pursued with the assumption that these changes would be implemented.

The mode telemetry circuits are shown in Figure 4-152. With reference to this figure it will be noted that, in general, the closure of Command relay contacts is an indication of the TM OFF state. With regard to the TM TBV/MSS status, the contact closure as shown indicates the RBV ON condition.

It is obvious from the figure that, in the absence of the requisite command, the associated mode telemetry output is held at ground potential.

In analyzing the worst case TM ON levels, there are two extreme conditions which must be examined. All other conditions will produce TM ON levels between these extremes. Thus, if the extremes are satisfied, all conditions will be satisfied.

The most negative TM ON output level exists when the telemetry voltage is at -25 volts, and when all commands are set in, with Emergency Off or VP Fault. Under these conditions it is impossible for the recorder to generate a reset, since the DC/DC Converter relay pick-up is inhibited. As a result each of the "tree" TM outputs can read a maximum negative level,

$$\overline{V_{TM}} = \frac{\overline{R_1}}{\overline{R_1} + \underline{R_{41}}} \times \overline{V_{PRI}}$$

$$= \frac{11845}{19187} \times -25$$

$$= -15.45 \text{ volts.}$$

This level is out of the -5 to -10 volt level required.

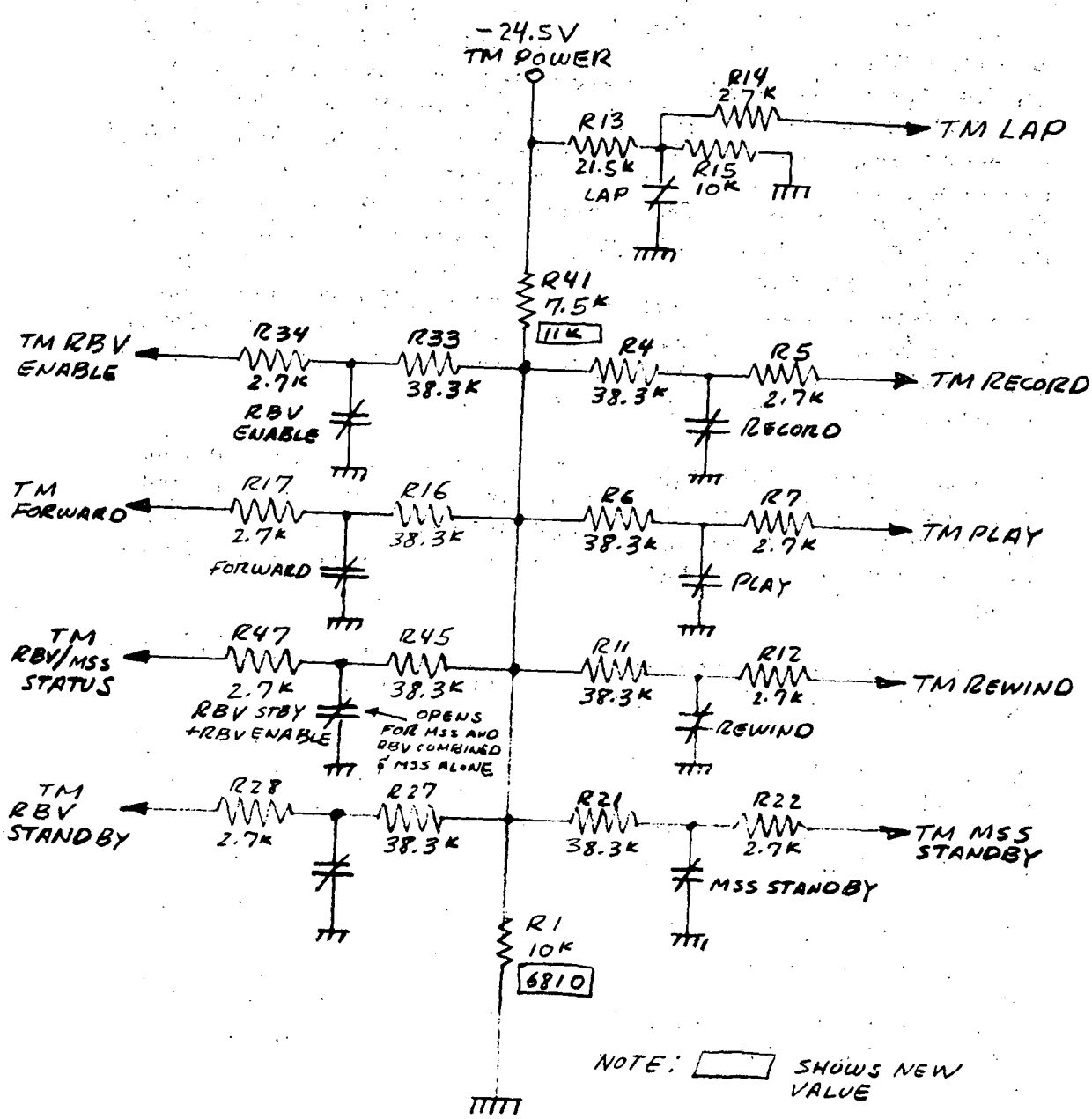
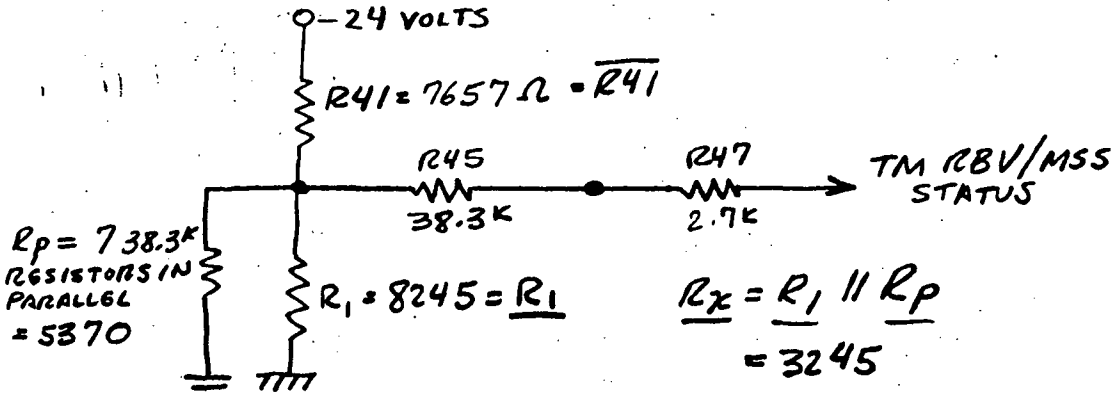


Figure 4-152. Mode Telemetry Circuits

In calculating the least negative TM ON output level, the telemetry power supply is assumed to be at -24 volts. Moreover, the recorder is assumed to be in an Off mode. With these conditions prevailing the TM MSS/RBV status is interrogated with MSS status set in. The "tree" circuit thus appears as shown below:



The least negative TM is then,

$$\underline{TM} = \frac{Rx}{\underline{Rx} + \overline{R_{41}}} \times -24.0$$

$$= -7.13 \text{ volts.}$$

This level is acceptable although the most negative TM ON extreme is not.

By changing R_1 and R_{41} to 6810 ohms and 11 k ohms respectively, the TM ON extremes were calculated and found to be -9.8 volts and -5.03 volts. Since all TM ON outputs will fall within these extremes the output level specification is satisfied.

The maximum TM output impedance can be calculated for that condition which gives the most negative TM ON output level as follows:

$$\overline{Z \text{ out}} = 3210 + 39{,}100 + \frac{\overline{R_1} + \overline{R_{41}}}{\overline{R_1} + \overline{R_{41}}}$$

$$= 42{,}310 + 4300$$

$$= 45{,}310 \text{ ohms}$$

Since $\overline{Z \text{ out}}$ is less than 50,000 ohms, the output impedance requirement is also satisfied.

f. TTL Logic. - The ERTS control system employs TTL integrated logic exclusively in performing the bookkeeping and decision making processes associated with control. When it is employed in this manner, the TTL integrated logic enjoys a degree of isolation from the outside world. On its input side it is buffered by the mode latching relays which, with the exception of RBV Run Tape, receive the input commands. On its output side it is buffered by relay drivers which, with but few exceptions, carry the mode and mode-oriented control signals to the recorder proper. It is important that this isolation be preserved if the relatively high speed capability of TTL logic is to be successfully degraded to perform the relatively low speed switching requirements of the ERTS control system.

It is equally important when employing TTL logic that a high degree of power line decoupling be employed, both internally and with respect to the outside world. Decoupling with respect to the outside world is provided by LC half-section filters which are capable of supressing both high frequency and low frequency disturbances. Every DC/DC Converter voltage to every control module is separately decoupled in this manner. Internal +5.6 volt power line decoupling is of equal importance and is incorporated within modules to minimize cross coupled disturbances between chips. Ceramic capacitors (0.1 uF) are employed as shunt filters for this purpose. The need for internal decoupling is apparent when it is realized that a single TTL logic gate will draw from 5 to 6 times its normal I_{CC} current while its output is switching from a "1" to a "0" state.

The ERTS control system employs 17 TTL integrated one-shots to generate the automated timing sequences which it requires. The problems associated with this usage have already been discussed (see Paragraph 2.3.1 and Appendix G).

When calculating the worst case minimum and maximum time delays associated with each one-shot, reference was made to the manufacturer's specifications. A listing of worst case delays is included in this report as Table 4-48.

All unused inputs within the control system logic are tied to a "high" through 1000 ohm resistors returned to the +5.6 volt supply. This is done to desensitize inputs which are not being used.

The TTL loading rates established by the manufacturers have been judiciously observed in the design of the control system logic. Steady state loading has been limited to 80% of the maximum drive capability, so as to provide an additional margin of safety.

TABLE 4-48. TTL ONE-SHOT DELAYS

Function	Function Performed	Nominal Period	Minimum Period	Maximum Period	Figure Reference
A9-Z2	Capstan Speed Detection (HS Modes)	490 μs	417 μs	549 μs	4-162
A9-Z3	Capstan Speed Detection (NS Modes)	2460 μs	2095 μs	2765 μs	4-162
A9-Z8	Capstan Speed Detection (NS Mode)	1740 μs	1478 μs	2540 μs	4-162
A9-Z11	Capstan HS Start/Run Timer	1.5 s	1.20 s	1.81 s	4-137
A9-Z13	Capstan Motor Driver Turn On Delay	25 ms	21.2 ms	29.7 ms	4-134 and 4-137
A9-Z14	HW & IW Motor Driver Turn On Delay	25 ms	21.2 ms	29.7 ms	4-133
A9-Z7	Primary Buffer Reset Delay	25 ms	21.2 ms	29.7 ms	4-134
A11-Z4	HW & IW Motor Start/Run Timer	5.0 s	4.27 ms	6.45 s	4-133
A11-Z7	Stop Seq. Low Speed Capstan Inhibit Timer	25 ms	21.2 ms	29.7 ms	4-137
A12-Z18	Pulser - Power On Sequence 1	1.4 ms	1.1 ms	1.73 ms	4-141
A12-Z19	Pulser - Power On Sequence 3	140 μs	110 μs	173 μs	4-141
ZX Proposed	Delay Gen. - Power On Sequence 3	71 ms	57 ms	86 ms	4-141
A12-Z20	Stop Timer	1.7 s	1.46 s	2.21 s	4-135
A12-Z3	Pulser - RBV Run Tape Off	140 μs	110 μs	173 μs	4-138
A13-Z5	Reset Clock Inh/Mask Timer	54 ms	46 ms	64 ms	4-135
A13-Z10	Reset Timer	11 ms	9.7 ms	13.5 ms	4-135
A9-Z10	HW Shoe Pull-In Timer	100 ms	84.2 ms	127 ms	4-162

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4.6.3.2 Module Analysis. - The control system logic is distributed over four modules in the electronics package. Distinct modules perform separable control functions as shown in Figure 4-153. With reference to this figure it is apparent that, in general:

(1) The A13 module (Command) is input oriented in that it forms an interface between the input commands and the TTL mode logic.

(2) The A12 module (Cycler) contains the mode recognition and storage logic.

(3) The A11 module (Control) is output oriented in that it provides an interface between the TTL mode logic and the recorder electronics.

(4) The A9 module (Sync Speed Detector) is output oriented in that it provides an interface between the TTL mode logic and the motor drive electronics.

In the analyses which follow, each module will be treated separately in an attempt to provide a detailed evaluation of separable control functions.

4.6.3.2.1 Command Module (A13).

a. Input Command Interface and Command Latching Relays. - As noted earlier, all input commands (with the exception of RBV Run Tape) are applied to the control system via latching relays. Analysis of latching relay command interface will be handled here, while analysis of the RBV Run Tape interface is deferred to paragraph 4.6.3.2.2b.

1. Setting the Command Latching Relays. - Input command interface with mode relays within the recorder as shown in Figure 4-154. When a command is initiated, the input command level is switched OFF state to the ON state for a period of 45 ± 5 milliseconds. During this time the input command line is capable of supplying a maximum current of 200 mA.

In analyzing the command relay interface it is required to show that:

(1) The command relay is not energized by the OFF condition.

(2) The command relay will always be set by the worst case ON condition.

(3) The current drawn by the command relay in the ON condition is less than 200 mA.

With regard to the first condition, it is apparent that current flow to the relay coil is blocked bythe series diodes during the OFF condition.

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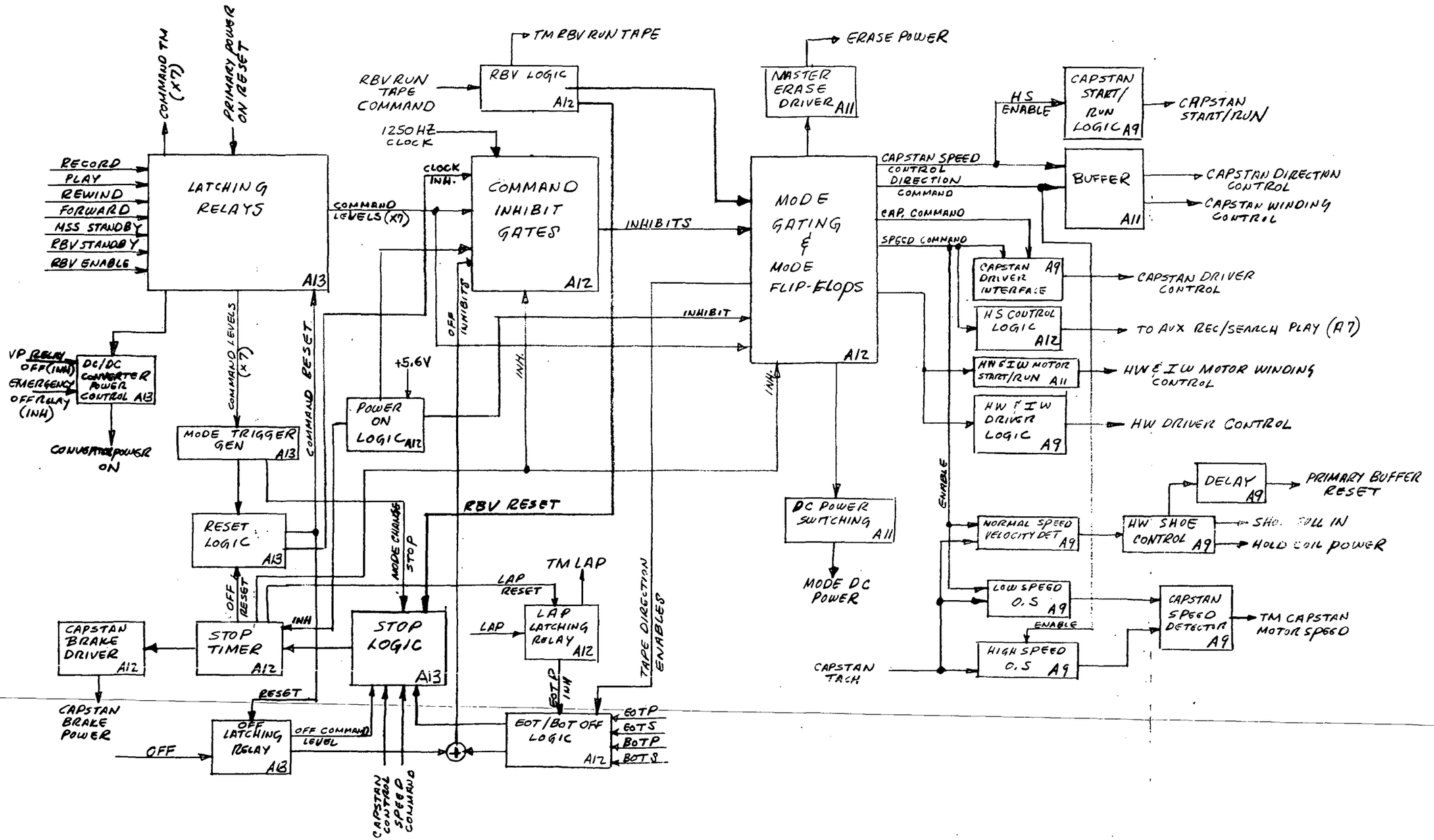

Figure 4-153. ERTS Control System Block Diagram

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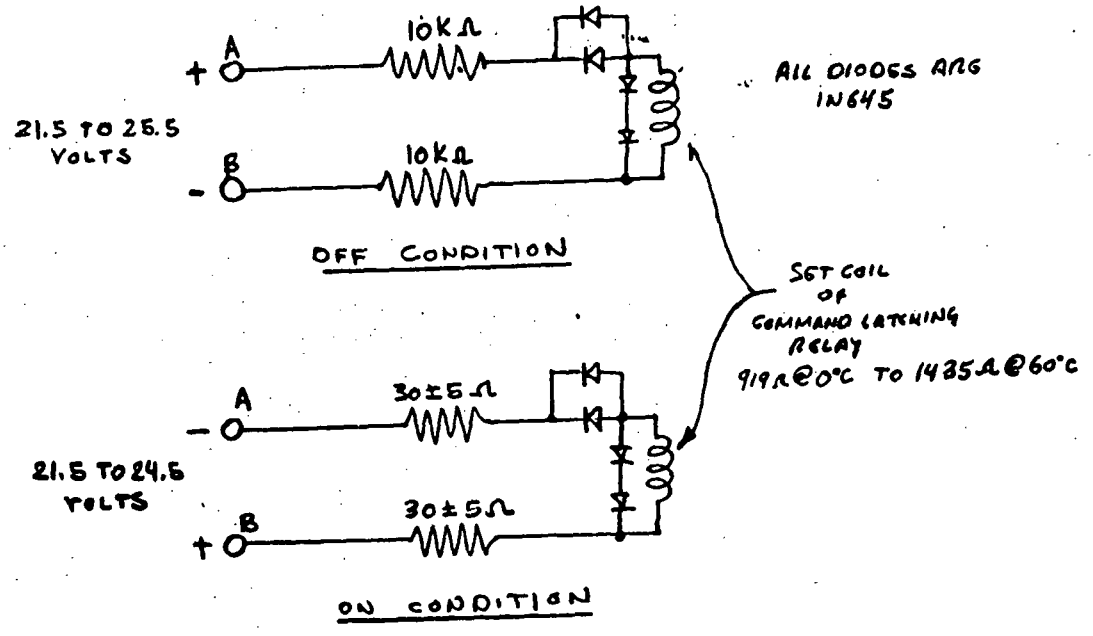

Figure 4-154. Command Relay Interface

In the ON condition the command relay coil requires a minimum current flow of 7.84 mA to guarantee relay pick-up (see Paragraph 4.6.3.1.3b1 for supporting analysis). The minimum current capability of the input command line can be determined as I_{CMD}, where, from Figure 4-154

$$I_{CMD} = \frac{21.5}{1505} = 14.3 \text{ mA}$$

Since 14.3 mA > 7.84 mA, the command relay will always be set in the command ON condition.

Again with regards to the ON condition it is apparent that the maximum input current capability of 200 mA is never exceeded.

2. Resetting the Command Latching Relays. - In Paragraph 4.6.3.1.3b1 it was shown that, when the K11 relay contacts close during a reset sequence (see Figure 4-135), the input operating command latching relays will always be reset. No attempt was made at that time to show that the Q3 relay driver transistor is capable of picking up K11. The Q3 driver circuit is redrawn in Figure 4-155 for the purpose of this analysis. If reference is made to this figure it will be noted that, when the reset one-shot output goes "high" during a reset sequence, Q3 must be driven into saturation. The worst case drive capability of the reset one-shot in the "1" state is 400 μA at ±2.6 volts over a 0°C to 60° temperature range. The base current required by Q3 to ensure saturation in the worst case can be determined with the aid of Figure 4-155, as follows:

$$\overline{I_L} = \frac{23.2}{1270} = 17.9 \text{ mA}$$

$$\overline{I_b} = \frac{\overline{I_L}}{h_{FE}} = \frac{17.9 \times 10^{-3}}{37} = 484 \ \mu\text{A}.$$

if

$$\overline{V_{BE\ SAT}} = 0.82 \text{ volts (from mfg's specifications)}$$

then

$$\overline{Ib}_{(REQ'D)} = 484 \times 10^{-6} = \frac{2.62 - 0.82}{\overline{R_B}} \qquad (1)$$

where $\overline{R_B}$ is the maximum allowed series base resistance.

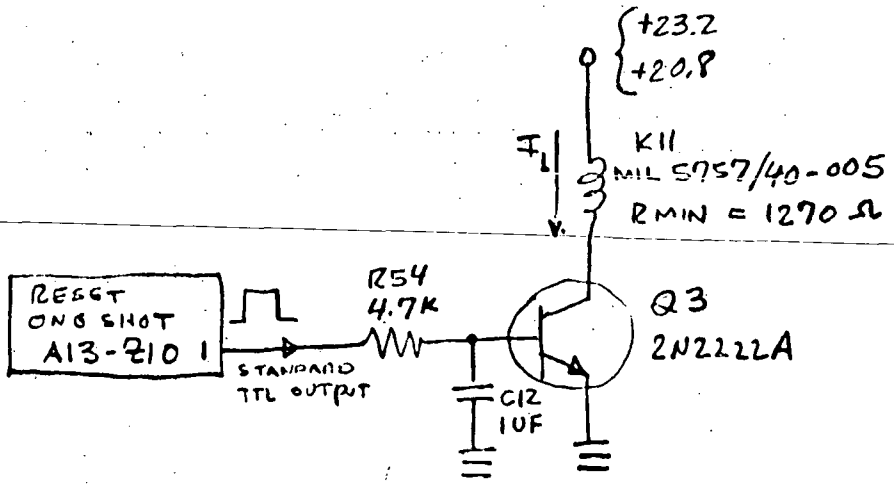

Figure 4-155. Normal Reset Driver

Solution of equation (1) yields R_B = 3600 ohms. Thus if the series base resistance shown in Figure 4-155 is reduced from 4700 ohms to a standard 1% plus resistance of 3480 ohms, Q3 will always be saturated during a reset sequence. The saturation current of Q3 is sufficient to ensure pick-up of relay K11 in the worst case.

b. Mode Trigger Circuits. - The mode trigger circuits (see Figures 4-135 and 4-156) generate a pulse when, in the course of normal operation, an operating command other than Off or RBV Run Tape is applied to the recorder. (Normal operation in this case excludes mode cycling from an Off, VP Fault, Emergency Off or other Power Off conditions. In such cases a mode trigger pulse is not generated.) The mode trigger pulse in turn initiates a normal reset sequence and a Stop sequence, when needed.

There is a single basic requirement which each mode trigger circuit must satisfy if it is to perform satisfactorily; the pulse which it produces must be of sufficient width to guarantee its propagation to both the Reset and Stop timers.

If all tolerances are taken into consideration, the mode trigger circuit shown in Figure 4-156 will produce a positive-going pulse with a width of from 250 μs, when the Command relay contacts close. Since the propagation time from the mode trigger circuit to the inputs of both the Reset and Stop timers is much less than 250 μs, the mode trigger pulse will always initiate a Reset sequence and a Stop sequence, when needed.

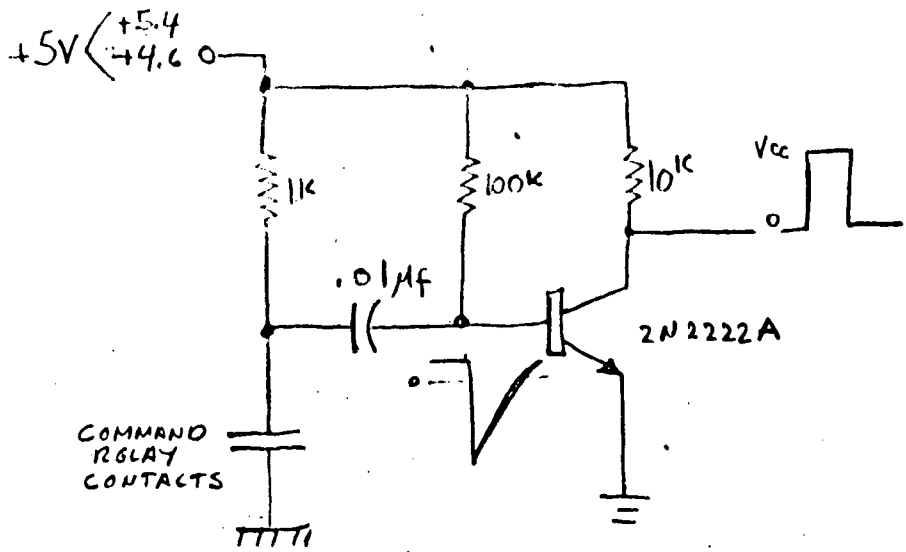

Figure 4-156. Mode Trigger Circuit

c. DC/DC Converter Power Control.- Because turn on and turn off of the DC/DC converter is controlled by the operating command mode latching relays (see Figure 4-139), the worst case turn on and turn off times of the DC/DC converter are directly related to the performance of the control system.

1. DC/DC Converter Turn On.- Worst case conditions for DC/DC Converter turn on occur when, with V_{PRI} = 20 volts in the VP Negate mode, an operating command (other than Off) is applied to the recorder with the Off command latching relay set. When this occurs, an Off reset sequence must be initiated and completed before the input command level is removed (see Table 4-4). To do this successfully requires that the time required to turn on the DC/DC Converter be no greater than the maximum operate time of the DC/DC Converter relay (i.e., 10 milliseconds).

Analysis has shown that, if the originally proposed network shown in Figure 4-139 is employed to turn on the DC/DC Converter, the response of the converter relay to the operating command relay contact closure will be delayed by 0.5 ms to 7.27 ms. This is an intolerable delay which will, in the worst case, increase the Off reset sequence period to 46.3 milliseconds (see table 4-46). As 46.3 ms is greater than the minimum external command level period of 40 ms, the new operating command will be reset in the process of resetting the previously set Off command. As a result, the recorder will not respond to the new operating command, and will revert instead to an Off mode with the Off latching relay reset.

There is a relatively simple way to correct the deficiency just noted. If the 56 ohm resistor in series with the Command latching relay contacts is replaced by a short circuit, and then relocated in series with the DC/DC Converter relay coil, the turn on response of the coil to a command relay contact closure will be instantaneous. As a result, the DC/DC Converter will be turned on 10 milliseconds after the command latching relay contacts close. This will produce an acceptable Off reset sequence as shown in Table 4-46.

The worst case conditions for DC/DC Converter relay pick-up will occur in the VP Negate mode when the primary voltage is reduced to 20 volts. The minimum primary voltage which is required to insure relay pick-up was determined by first determining the maximum coil current required. The manufacturer's specifications indicate that a minimum operate voltage of 19.8 volts is required to pick-up the relay in a 125°C environment. If the minimum coil resistance of 288

ohms at 25°C is translated to 125°C, a maximum coil current of 46.5 mA results. If it is assumed that relay pick up is by ampere-turn requirement, then the coil current which was determined at 125°C is invariant, and will be applicable at any temperature.

The minimum required operate voltage can thus be determined from:

$$V_{operate} = 46.5 \times 10^{-3} \left(\overline{R_{coil}} + 65 \right) \qquad (1)$$

where 65 is the maximum value of the nominal 56 ohm resistor which was placed in series with the relay coil

Substituting $\overline{R_{coil}}$ = 365 ohms (@ 35°C) into equation 1, and solving for $V_{operate}$, yields 20 volts. From this it is apparent that the converter relay will just pick-up under worst case conditions.

2. DC/DC Converter Turn Off. - As it was important for the DC/DC Converter relay to instantaneously respond to a turn-on command, it is just as important that its response to a turn-off command be delayed. This requirement is imposed because of the command latching relay contact instability which exists when, during a normal or Off reset sequence, voltages are applied to both the set and reset coils (see Paragraph 4.6.3.1.3b1). The period of contact instability can be determined by subtracting the times shown in step 5 of Table 4-47 from step 9. The result yields a contact instability period of 13.8 milliseconds. From this it can be inferred that, when the command relay contacts open for 13.8 ms, the DC/DC Converter relay must not drop out.

A circuit diagram of the proposed DC/DC Converter relay circuit is shown in Figure 4-157. If the loop equations are solved for I_1, we have,

$$I_1(t) = \frac{V_{PRI}}{R_1 + R_2 + R_3} \; e^{-t/(R_1 + R_2 + R_3) C} \qquad (2)$$

substituting $I_1(t) = V_{coil}(t)/R_3$ into equation 2 and solving for t, we have.

$$t = (R_1 + R_2 + R_3) C \, \mathrm{Ln} \left[\frac{R_3 V_{PRI}}{(R_1 + R_2 + R_3) V_{coil}(t)} \right] \qquad (3)$$

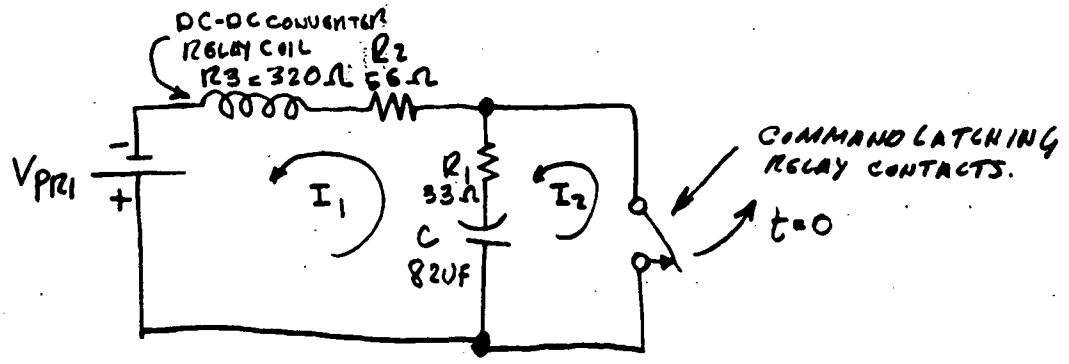

Figure 4-157. DC/DC Converter Relay Circuit

Solving for t requires C, V_{PR1}, $\overline{V_{coil}}$ (t), R_1, R_2 and R_3. When making these substitutions, V_{coil} is equal to the maximum specified dropout voltage of 7.0 volts. Solution of equation 2 using current values yields at 22.3 milliseconds. Since t is longer than the maximum command latching relay contact instability period of 13.8 milliseconds, the DC/DC converter will not drop out during a normal or Off reset sequence.

4.6.3.2.2 Cycler Module (A12). -

a. RBV Run Tape Logic. - The RBV Run Tape Logic (see Figure 4-136) includes the following:

(1) RBV Run Tape command interface.

(2) Stop timer enabling logic.

(3) RBV Run Tape mode gating logic.

(4) TM RBV Run Tape driver.

1. RBV Run Tape Command Interface. - The RBV Run Tape command interface employs one low power TTL NAND gate and an inverter in a Schmitt trigger configuration. The interface sharpens the command rise and fall times to produce the standard TTL transistions required by the command logic.

In the absence of the RBV Run Tape command, the input level is "low" (i.e., 0.2 ± 0.15 volt with a sink capability of 8 mA maximum). This level is well below the minimum TTL "1" input threshold of 0.8 volts and, as a result, is interpreted by the input logic as a "low".

When the input command is initiated, the input level begins to rise. At 2.0 volts (maximum), Z16-12 is primed. One diode drop later, or at 2.846 volts (maximum), Z16-13 reaches its maximum "1" state threshold level. At this instant the input level is required to supply a maximum current of:

$$\overline{I} = \frac{2.0}{R37} + \overline{I_{in}} \text{ (Z16-12)} + I_{in} \text{ (Z16-13)} \qquad (1)$$

$$= \frac{2.0}{2187} + 12 \times 10^{-6} + 12 \times 10^{-6}$$

$$= 939\ \mu A$$

Since the maximum source capability (arrived at by straight line extrapolation) is 860 μA, at 2.846 volts, it is apparent that the input "1" transition is not guaranteed.

If R37 is changed from a carbon composition ±5% resistor to a ±1% film resistor, the required maximum current will be, from equation 1.

$$I = \frac{2.0}{2682} + 24 \times 10^{-6}$$

$$= 769\ \mu A$$

This figure is below the 860 μA available from RBV Run Tape command source, and hence a "1" transition is guaranteed.

Once the input "1" threshold is exceeded, Z5-10 goes "high" thereby reducing the input current requirement. This allows the input level to rise until an equilibrium is reached between available source current, and feedback current supply and input logic demand.

When the RBV Run Tape Command is negated, the input voltage level starts to fall. The Z5-10 level falls volt for volt until Z16-13 reaches +0.7 volt (maximum). When this occurs Z5-10 switches to its "0" logic level of +0.3V (maximum). This in turn reinforces the RBV Run Tape OFF level by providing a current sink for the Z16-13 input. This guarantees an input "low" at that pin. Since CR7 disconnects, the only current which the source must sink is that required by A16-12.

This is typically 0.18 mA, or much less than the 8.0 mA sink capability of the source.

2. Stop Timer Enabling Logic. - The Stop timer enabling logic is provided to inject a Stop sequence whenever the RBV Run Tape command is turned off. Before the RBV Run Tape ON command is given the inputs to one-shot Z3 are enabled; however, the one-shot is in a "timed out" state. Application of the RBV Run Tape ON command disables the one-shot (provided of course that the RBV Run Tape command was preceded by an RBV Enable command), by putting a "high" at Z3-3. When the RBV Run Tape OFF command is given, one-shot Z3 is fired. Z3 produces a positive pulse of approximately 140 μs duration at its "1" output. The negative-going edge of this pulse triggers the Stop timer and restores the recorder to an RBV Enable mode.

3. RBV Run Tape Mode Gating Logic. - The RBV Run Tape ON signal is applied as a "low" input to Z2-10. This "low" enables the D input of the Record mode flip-flop.

4. TM RBV Run Tape Driver. - The TM RBV Run Tape signal is a digital telemetry output. In the absence of the RBV Run Tape ON command both Q4 and Q5 are saturated and the TM RBV Run Tape signal level is approximately -0.2 volts. When the RBV Run Tape ON command is given, the input to Q4 falls to +0.1 volt, causing Q4 to cut off. This, in turn, forces Q5 into cut-off, via a voltage divider consisting of R39, R40 and R42. With Q5 cut off, the TM RBV Run Tape signal level falls to -7.5 volts.

   The worst case analysis of the TM RBV Run Tape driver was directed toward an investigation of the following:

   (a) Q4 saturation and TTL input drive capability.

   (b) Q5 off biasing.

   (c) Q5 saturation.

   Q4 Saturation. - When the RBV Run Tape command is OFF, Q4 must be driven into saturation by Z16-11 output. The maximum drive capability of Z16-11 in the "1" state is 90 μA at 2.4 volts. When Q4 is saturated;

$$\frac{}{IC4} = \frac{23.2}{R\ 39} = \frac{23.2}{3.9} \times 10^{-3} \approx 6.0\ mA$$

The maximum base drive required to support saturation is then

$$\overline{I_{b_{req'd}}} = \frac{6.0}{h_{fE}} \times 10^{-3} \text{ A}$$

$$= \frac{6.0}{57} \times 10^{-3}$$

$$= 105 \ \mu\text{A}$$

The true base drive required of Z16-11 is:

$$\underline{I_{b_{drive}}} = \frac{2.4 - \overline{Vbe\ sat}}{R38}$$

$$= \frac{2.4 - 0.57}{18,900}$$

$$= 96.7 \ \mu\text{A}$$

Thus,

$$\underline{I_{b\ drive}} < \overline{I_{b\ req'd}}$$

It is to be noted that both exceed the worst case TTL drive capability. Thus $\overline{I_{C4}}$ must be reduced by increasing R39, and the base drive capability increased by increasing R38.

Increasing R39 to 10k (±5% carbon)

$$\overline{I_{C4}} = \frac{23.2}{8100} = 2.86 \text{ mA}$$

From which,

$$\overline{I_{b\ req'd}} = \frac{2.86}{\underline{hfe}} = \frac{2.86}{52} = 55 \text{ mA}$$

If R38 is changed to a 27.4k ±1% film resistor,

$$\underline{I_{b\ drive}} = \frac{2.4 - \overline{V_{be4\ sat}}}{\overline{R38}}$$

$$= \frac{2.4 - 0.5}{26.85k}$$

$$= 70.7\ \mu A$$

Since $\underline{I_{b\ drive}} > \overline{I_{b\ req'd}}$, the saturation of Q4 is now guaranteed.

Q5 Off Biasing. - Using given parameters, it was found that the OFF bias to Q5 could use as high as +12 volts. To bring this value within maximum recommended limits, it was suggested that R40 be changed from 1 kohm to 6810 ohms, and that R42 be changed from a 22 k ± 5% resistor to a 21.5k ± 1% film resistor. With these changes incorporated, the OFF bias to Q5 will always fall in the range from +0.9 volt to +4.55 volt.

Q5 Saturation. - With given parameters, Q5 is grossly oversaturated in the ON state. This has the effect of increasing the $V_{be\ sat}$ of Q5. This, in turn, increased the current drawn through R40 from Q4. To minimize this effect it was suggested that R43 be changed from 21.5k to 7.5k. If R43 is changed, it is also necessary to reduce R45 from 10k to 3.9k, so as to insure a nominal -7.5 volt output signal.

b. Capstan Brake Driver Logic.

1. Description. - The capstan brake is engerized whenever a Stop sequence is initiated (see Paragraph 4.6.3.1.3c). The capstan brake driver logic is provided as an interface between the Stop sequence timer and the capstan brake coil (see Figure 4-158). When a Stop sequence is initiated, Z10-12 goes "high" and remains "high" for the duration of the Stop sequence interval (i.e., 1.46 to 2.21 seconds). When this occurs, Q6 is turned ON. As the collector voltage of Q6 falls to V_{CE} (SAT), transistor Q7 is driven into saturation. Whe Q7 saturates, it acts as a current sink for capstan brake coil power.

The worst case analysis of the capstan brake driver logic was concerned with insuring that, in the worst case:

(a) Both Q6 and Q7 are absolutely cut off in the absence of a Stop sequence.

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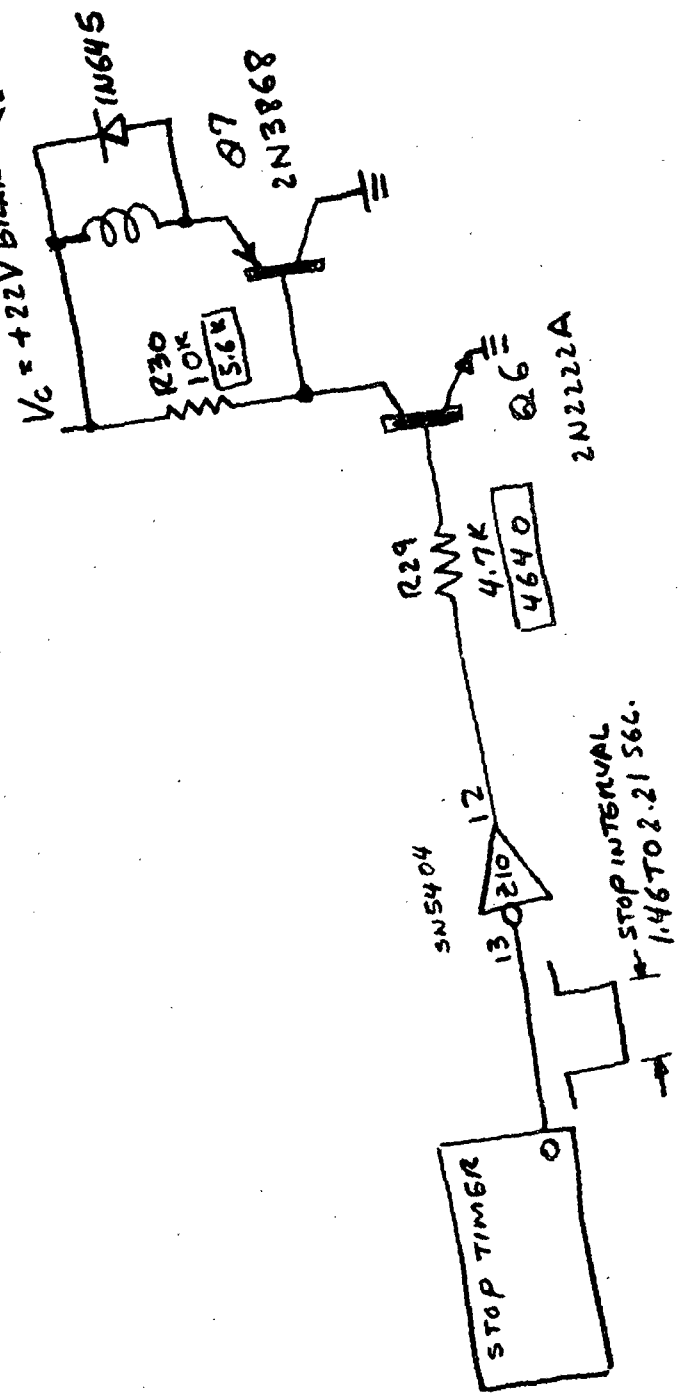

Figure 4-158. Capstan Brake Driver Logic

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(b) Both Q6 and Q7 are in saturation during the Stop timer interval.

(c) When Q7 is in saturation, its junction temperature does not exceed 110°C.

Before the worst case analysis could proceed, it was necessary to determine worst case minimum and maximum brake coil resistance. The resistance of the brake coil was found to be 46.5 ohms when measured in a de-energized state at an ambient free air temperature of 25°C. This value is equivalent to that which would prevail in the ERTS transport package when fully powered in an ambient environment at 0°C. It is assumed that the transport experiences a 15°C rise when fully powered, and that there is a 10°C rise in coil temperature. If it is assumed that the transport achieves the worst case minimum ambient of 0°C, a 10°C rise due to coil current will correct the minimum brake coil resistance to 43.9 ohms, using the well known relationship:

$$R_f = R_i \left[1 + \alpha_i \, (T_f - T_e)\right] \qquad (1)$$

where

R_i = initial resistance at temp. T_i

R_f = final resistance at temp. t_f

α_i = temperature coefficient of copper at 25°C = 0.00385

The maximum value of coil resistance was measured with the coil drawing a current of 0.5 A in a free air environment at 60°C. The measured value was 60.3 ohms.

2. Power Dissipation of Q7. - If it is assumed that Q7 must drive the minimum coil resistance of 43.9 ohms continuously (a somewhat absurd condition unless it is assumed that a command requiring a change in tape speed and/or direction is followed after 2.21 seconds by a new command requiring another change in tape speed and/or direction, and so on, continuously), and that V_{CE7} (SAT) = 0; then,

$$\overline{I_{C7}} = \frac{\overline{V_c}}{R_{coil}} = \frac{23.2}{43.9} = 0.528 \text{ A}$$

With I_{C7} = 0.528 A, and with a maximum allowed Q7 junction temperature of 110°C, V_{CE7} is 0.542 volt. The maximum worst case power to be dissipated by Q7 is then,

$$\overline{P} = 0.542 \times 0.528$$

$$= 0.286 \text{ Watt}$$

If Q7 is separated from the printed circuit board by an insulating spacer as was initially proposed, then, since true operation is in a vacuum, heat transfer will be via conduction from the junction to the case and thence by radiation to a black body sink at 61°C.

For transfer by conduction (junction to case),

$$T_C = T_J - \overline{P}\,\theta_{JC} \qquad (2)$$

where

θ_{JC} = 17.5°C/Watt (from transistor data sheets)

T_J = 110°C (maximum allowed)

$\overline{P}$ = 0.286 watt (from above)

T_C = Temperature of transistor case

Substituting given values and solving for T_C, yields T_C = 106°C.

Using this figure as a base, the radiation formula can be applied to determine the required radiating area. The radiation formula is given as:

$$Q = A_1 E_1 \sigma (T_1^4 - T_2^4) \qquad (3)$$

where,

Q = Heat Transfer, = 0.286 x 3.41 = 0.975 Btu/h

A_1 = Maximum Radiating Area Required (in ft^2)

E_1 = Emissivity of Transistor Case (0.8 assumed)

σ = Stefan-Boltzman Constant = $.173 \times 10^{-8}$ BTU/h ft^2 $(^\circ R)^4$

T_1 = Temperature of Radiating Area, = 682.7 °R

T_2 = Temperature of Blackbody Receptor, = 601.5 °R

Substituting given values and solving for A_1 yields a radiating surface area requirement of 1.2 in^2. Since the radiating surface area of Q7 is only 0.302 in^2, it is therefore impossible to insure sufficient heat transfer by radiation alone.

If, instead of depending on heat transfer by radiation, the transistor case is either (1) mounted on the printed board ground plane copper, or (2) affixed to the ground plane copper via a thermally conductive polyurethane adhesive, it would then be possible to achieve more efficient heat transfer via conduction. Both approaches were investigated in the worst case design analysis, making use of a measured maximum ground plane temperature of 68 °C (see Appendix G for analysis).

With reference to Appendix G, it will be noted that, of the two approaches to conduction heat transfer, the intimate case to ground plane contact approach is preferable; however, either approach will produce the desired result of limiting of Q7 junction temperature to a temperature less than 110 °C.

3. Saturation of Q6. - When the collector current of Q7 is maximum at 0 °C, $\underline{h_{FE}}$ = 22.3 (from curves). Therefore when Q6 saturates,

$$\overline{I_{C6}} = \overline{I_{b7}} = \frac{528}{22.3} = 23.7 \text{ mA}$$

This is a worst case sinking requirement for Q6.

If a maximum Q6 base drive capability of 400 μA at 2.4 volts is assumed with $\underline{h_{FE6}}$ = 32.5 (from curves), then,

$$\underline{I_{C6}} = 0.4 \times 10^{-3} \times 32.5$$

$$= 13 \text{ mA}$$

This current is large enough to insure that Q6 is driven well into saturation. As a matter of fact, the saturation current capability

is so great that it is possible to reduce R30 from 10kohms to 5.6-kohms without raising the required Q6 saturation current beyond 3.15 mA. There is an advantage to be gained in reducing R30 (i.e., a lower resistance will provide a lower impedance sink for the base-to-emitter junction of Q7 when it is cut off).

4. Cut-Off Conditions. - Under worst case conditions with an ambient temperature of 60°C, $I_{CB06} \approx 0.3\ \mu A$. Since there is insufficient drive on the base of Q6 to approach a minimum cut-in or turn-on voltage, it can be assumed that $h_{FE6} \approx 0$, and that $I_{E6} = 0$. Under these conditions, $Ib6 \approx I_{C6} \approx I_{CB06}$. As a result, the drop across the Q6 collector resistor, R30, is insignificant.

With regard to Q7, a worst case junction temperature of 110°C may be assumed. At this temperature, $I_{CB07} = 12\ \mu A$. This current will produce a forward base bias of only 67 mV. This "drive" is incapable of exceeding the cut-in voltage of Q7. As a result, there will be no emitter current flowing in Q7.

Thus, cut-off of both Q6 and Q7 is assured under worst case conditions with an input TTL logic "low".

c. High Speed Control Circuit. - The High Speed Control circuit (see Figure 4-137 and 4-159) generates a digital output level which is "low" in normal or low speed modes, and "high" in the high speed (i.e., Forward and Rewind) modes. The High Speed Control signal is applied to the Auxiliary Search Playback module (A7), where it is used to threshold the amplified Search signal off tape.

The worst case analysis investigated the following apsects of the high speed control circuit (see Figure 4-159):

Cut-off and saturation of Q2

Variations in output level for both high speed and normal speed conditions

Ability of the high speed control circuit to threshold worst case search track signals.

1. Saturation of Q2. - Q2 must be saturated in all modes except Rewind and Forward. The analysis showed that, under worst case conditions, the saturation of Q2 was not guaranteed. In order to improve the base drive capability, R34 was reduced from 47kohms to 10kohms, as shown in Figure 4-159. The resultant increased base drive more than offsets the increased collector saturation current increase, which was recommended so as to improve the collector voltage stability of transistor Q2. The result is insured saturation of Q2 in all modes except Rewind and Forward.

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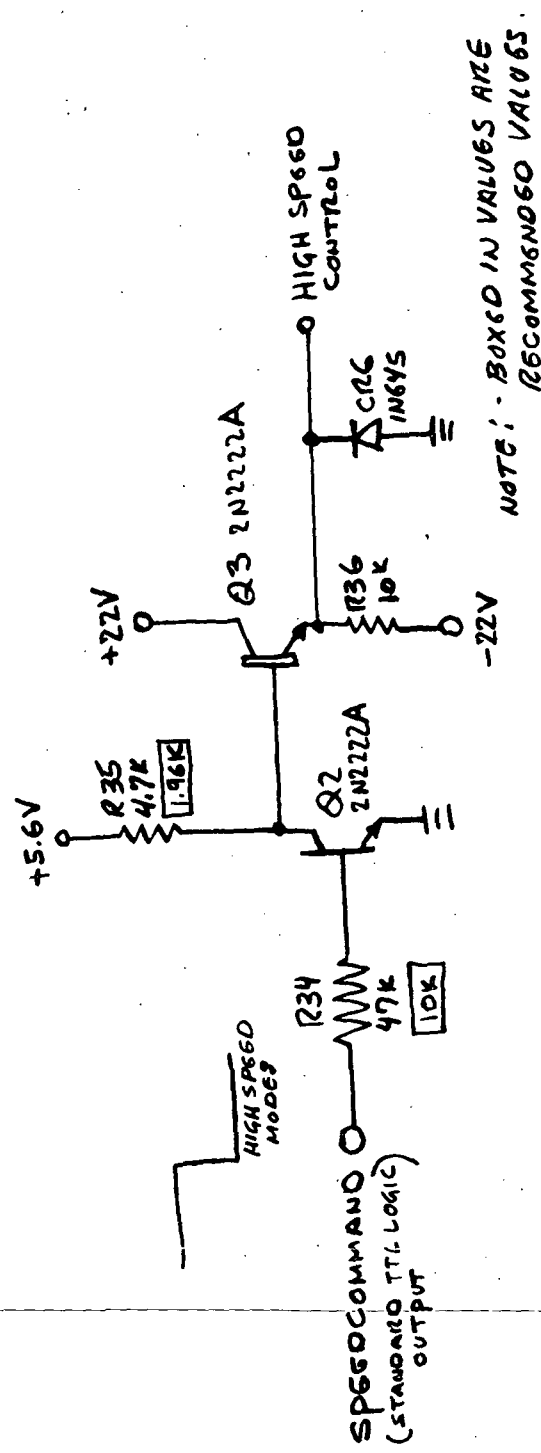

Figure 4-159. High Speed Control Circuit

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2. Cut-off of Q2. - In high speed modes, Q2 must be cut off. Since the worst case TTL logic "low" input to Q2 is a small positive (i.e., +0.218 volt maximum) voltage, and since there is no reverse bias at the emitter junction, there is a question as to whether Q2 is, in fact, cut off. If the base-to-emitter forward cut-in voltage $V\gamma$, is calculated, using worst case transistor values in the following EBERS-Moll equation,:

$$V_\gamma = N\ V_T\ L_n \left[1 - \frac{I_E - \alpha_I\ I_C}{I_{EO}} \right] \qquad (1)$$

a maximum value of +0.259 volts results. Since this voltage is greater than the worst case TTL logic input level, it was concluded that Q2 is truly cut off in all modes except Rewind and Forward.

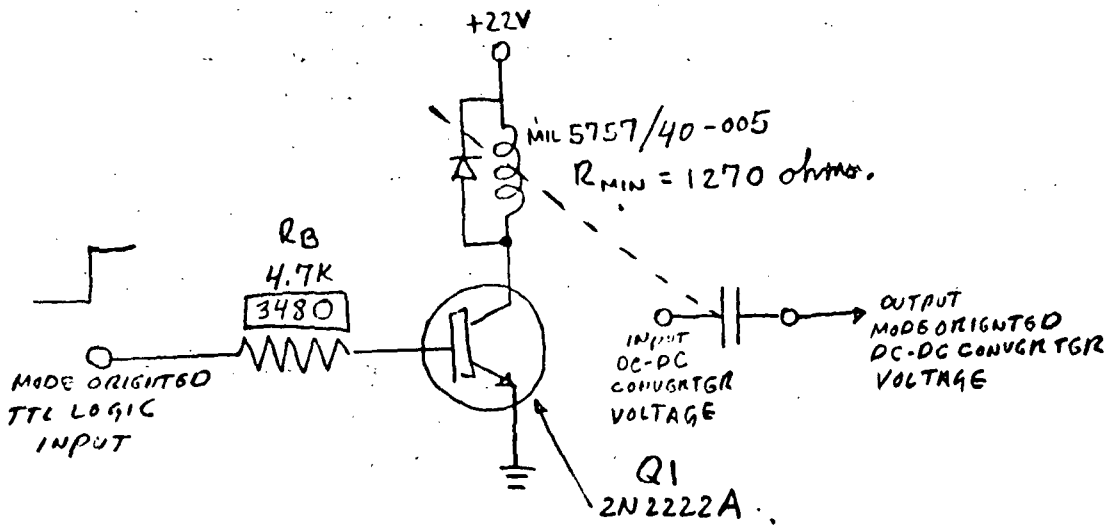
3. Variations in Output Level. - Utilizing worst case circuit parameters, an output variation of +4.3 volts to +5.7 volts was arrived at for operation in a high speed mode. For normal speed operation, the high speed control signal output variation of -0.45 volts to 0.62 volts was calculated. In the high speed modes, most of the output variation is due to variation in the +5.6 volt supply. In the normal speed modes the variation is due to changes in V_{CE} (SAT) of transistor Q2 and Vbe (SAT) of transistor Q3.

4. Threshold Capability of High Speed Control Signal. - In order to perform a satisfactory analysis of the threshold capability of the high speed control signal, it was first necessary to analyze the input circuit of the Auxiliary Search/Playback module (A7). The first disclosure of this analysis was that the High Speed Control signal could be considered as a voltage source in the face of minimum loading at the input of module A7.

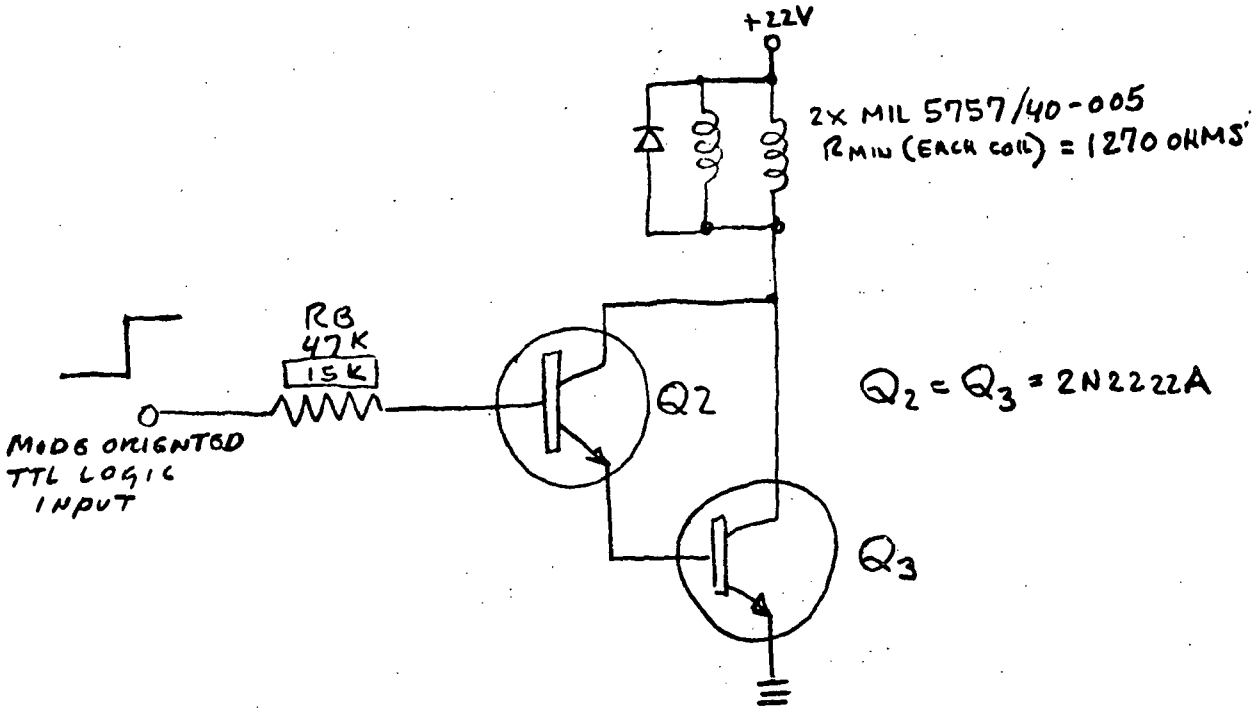
   The balance of the analysis consisted of first determining worst case required threshold voltages (by assuming minimum off-tape signal amplitudes in both high speed and low speed modes), and then of selecting voltage divider resistors (within the A7 module) which would guarantee the threshold conditions.

4.6.3.2.3 Control Module (A11).

a. DC Power Switching. - The ERTS control system employs relay driver logic, as shown in Figure 4-160, to couple mode oriented power voltages to the recoder electronics.



(a)



(b)

NOTE: SUGGESTED VALUE CHANGES ARE SHOWN IN BLOCKS.

Figure 4-160. DC Power Switching Circuits

The circuit shown in Figure 4-160a is intended to drive one power switching relay as indicated. The worst case minimum drive capability of the TTL logic input to Q1 is 484 μA at +2.6 volts. The maximum collector current required for saturation is I_C, where,

$$\overline{I_C} = \frac{23.2}{1270} = 18.3 \text{ mA}$$

For an h_{FE} of 37 then,

$$I_{b\ (req'd)} = \frac{18.3 \times 10^{-3}}{37} = 497\ \mu A$$

When saturated, $\overline{V_{be\ (SAT)}} = 0.82$ volt (from manufacturer's specs)

Thus,

$$I_{b\ (available)} = 500\ \mu A = \frac{2.62 - 0.82}{R_B}$$

Solving for $\overline{R_B}$ yields 3600 ohms. Thus, if a standard 3480 ohm ±1% film resistor is used, the saturation of Q1 is guaranteed in the worst case.

The circuit shown in Figure 4-160b must drive two power switching relay coils. The maximum collector current required to saturates Q3 is I_{C3}, where,

$$\overline{I_{C3}} = \frac{23.2}{635} = 36.5 \text{ mA}$$

for an h_{FE3} of 38 then,

$$I_{b3\ (req'd)} = \frac{36.5 \times 10^{-3}}{38} = 0.96 \text{ mA}$$

at $I_{E2} = 0.96$ mA, $h_{FE2} = 29$

Thus,

$$\overline{I_{b2\ (req'd)}} = \frac{960}{29} = 33.2\ \mu A$$

When saturated $\overline{V_{be2}}$ (SAT) = 0.62 volt (from manufacturers specs).

Thus,

$$I_{b\ (available)} = 33\ \mu A = \frac{2.62 - 0.62}{R_b}$$

Solving for R_b yields 60.6kohms. Thus, it would seem that the original selected value of 47 kohms is sufficiently low to ensure saturation of Q2. It is, however, suggested that R_b be reduced to 15kohms, so as to improve the cut-off condition.

b. Master Erase Driver. - The master erase head is powered via Record relay contacts as shown in Figure 4-161a. The Record relay driver is similar to the relay driver shown in Figure 4-160a.

The analysis of the master erase driver was limited to a determination of worst case relay contact stressing. For the purpose of this analysis, the circuit shown in Figure 4-161a can be reduced to that shown in 4-161b, since $X_c \gg X_L$. The equation for the current in the erase head when the relay contacts are closed is:

$$I = \frac{V_{in}}{Z} = \frac{23\ \mathrm{Sin}\ (2\pi \times 20 \times 10^3\ t)}{205}$$

$$= 0.112\ \text{A peak.}$$

The current carrying capability of each relay contact is given by the manufacturer as 0.2 A at 28 volts for a 0.32 H load. The contacts are thus capable of handling an inductive load energy

$$W = \frac{1}{2} LI^2 = \frac{1}{2} (0.32 \times 0.04) = 6.4\ (10^{-3})$$

The inductive load energy required by the master erase head is:

$$W = \frac{1}{2} (0.75 \times 10^{-3} \times 0.012) = 4.5\ (10^{-6})$$

Thus it is apparent that the erase head does not overstress the record relay contacts.

4.6.3.2.4 Sync Speed Detector (A9).

a. Capstan Speed Detector and Headwheel Shoe Control. -

1. Description. - The Sync Speed Detector module incorporates a capstan velocity detector which is driven by an amplified capstan tachometer

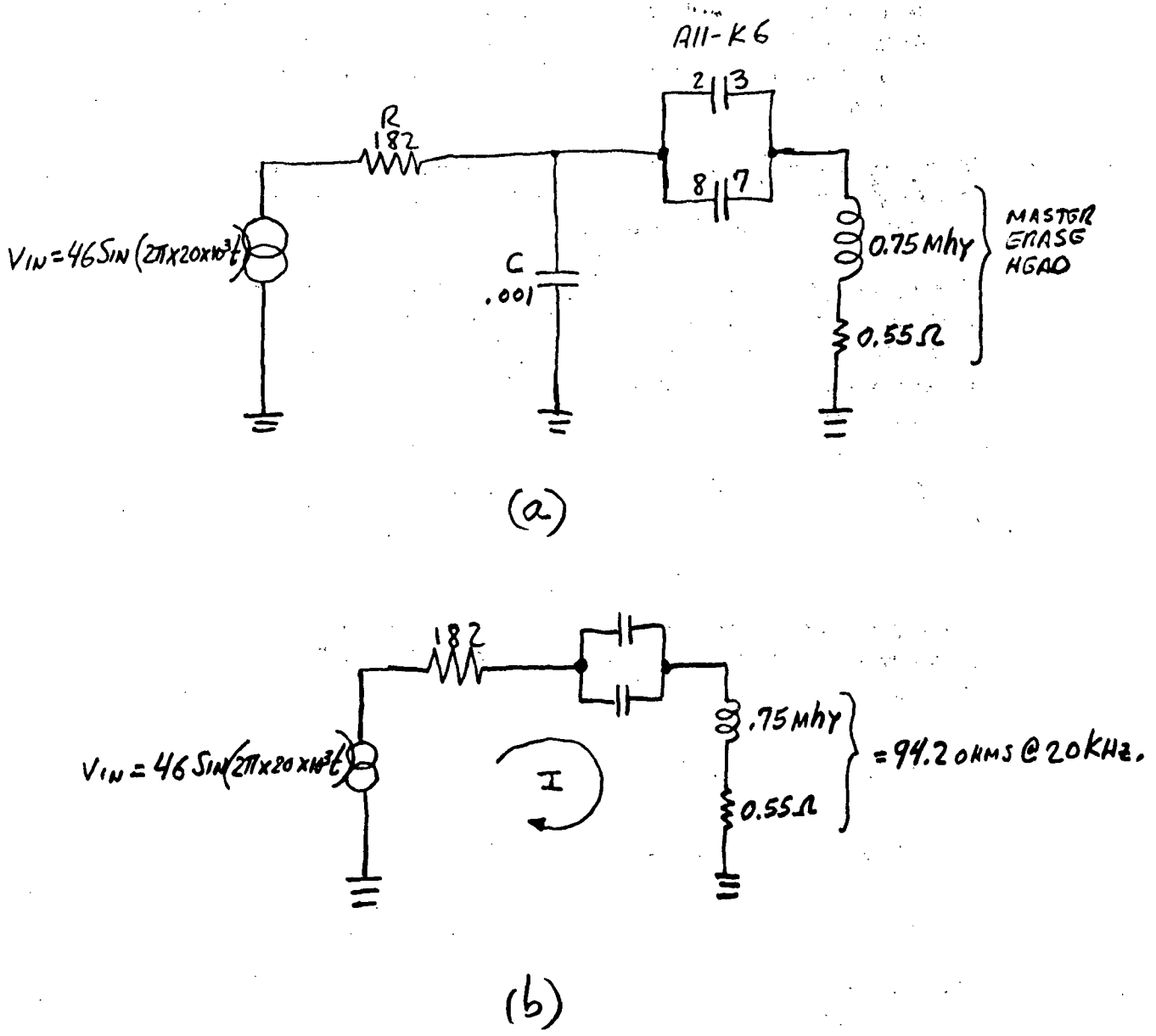


Figure 4-161. Master Erase Head Driver Circuit

signal as shown in Figure 4-162. When the correct capstan speed is attained in either a Record or Play mode, the velocity detector sets the Headwheel Shoe flip-flop. When this occurs, the Headwheel Shoe is energized to bring the tape into contact with the rotating video heads. If, for any reason, the capstan motor speed decreases, the velocity detector will reset the Headwheel Shoe flip-flop. The Headwheel Shoe will immediately disengage, and remain disengaged until the capstan motor accelerates to the correct speed.

2. Analysis. -

Capstan Tacholmeter Amplifier. - The Capstan Tachometer amplifier, Q3, is driven by the Capstan Tachometer signal. This signal is derived from a tonewheel pickup, attached to a shaft within the capstan motor assembly. In analyzing the Capstan Tachometer amplifier the output requirements were determined first. This determination was then used to specify the worst case input requirements. The actual Capstan Tachometer signal input was then analyzed to determine if, in the worst case, it met all input signal requirements.

The Capstan Tachometer amplifier is really a switching amplifier which is driven into saturation when a positive-going Capstan Tachometer signal pulse appears at its input. The Capstan Tachometer amplifier must drive the equivalent of 4.1 standard TTL logic loads. It must, therefore, be capable of supplying 180 μA at +2.4 volts when cut off, and of sinking 6.4 mA when saturated. The collector resistor of Q3 is sufficiently "low" to insure both the logical "1" and "0" conditions in the worst case.

The worst case collector current needed to saturate Q3 is $\overline{I_c}$ where,

$$\overline{I_c} = \frac{5.4}{810} = 6.7 \text{ mA} \qquad (1)$$

at 6.7 mA, $h_{FE} = 47$

The base current required to saturate Q3 is then $I_{b\ (req'd)}$ where,

$$\overline{I_{b\ (req'd)}} = \frac{\overline{I_c}}{47} \ 142\ \mu\text{A}. \qquad (2)$$

The maximum value of Vbe (SAT) under these conditions is 0.99 volts, based on manufacturer's specifications. If it is assumed that $I_{b\ (req'd)}$ is increased to 170 μA so as to allow a margin of safety, the equivalent peak input voltage required to saturate Q3 will be approximately +1.8 volts. This voltage specifies the minimum positive input requirement for the Capstan Tachometer signal.

The minimum Capstan Tachometer signal amplitude capability must be determined in the normal or low capstan speed modes, since the capstan tonewheel pick-up signal will be lower in those modes. Tests conducted on a typical breadboard tape transport have shown that the minimum capstan tonewheel signal in the Record or Play modes is 160 mVpp. This signal is applied to a pre-amplifier which, in turn, generates the Capstan Tachometer signal. The minimum gain of the Capstan Tachometer pre-amplifier is 7.38 in the low speed modes. As a result, the pre-amplifier is capable of supplying a Capstan Tachometer signal having a minimum amplitude of only 1.18 Vpp. This signal is obviously too small to guarantee saturation of the Q3 Capstan Tachometer amplifier.

This deficiency can be overcome by either increasing the tone-wheel output signal to 500 mVpp (i.e., by reducing the spacing between the tonewheel pickup and the tonewheel), or by increasing the tachometer pre-amplifier gain by a factor of 3.2.

Capstan Velocity Detector. - The Capstan Velocity detector consists of two TTL integrated one-shots in tandem, and associated gating (see Figure 4-162). With reference to the figure, it will be noted that the detector is disabled in high speed (i.e., Rewind and Forward) modes. This is done to prevent the Headwheel Shoe from engaging in those modes.

The Capstan Velocity detector is enabled in the low speed (i.e., Record/Play) modes by a logical "high" which appears on the Capstan Run bus. The Capstan Run bus is forced to a "high" only after the headwheel and Iω motors have been accelerated to synchronous speed in a Record or Play mode.

When the Capstan Velocity detector is enabled it compares the position of a current Capstan Tachometer pulse to that of the previous Capstan Tachometer pulse. It does this by delaying the Capstan Tachometer pulse by an equivalent "synchronous"

TO BE REVISED

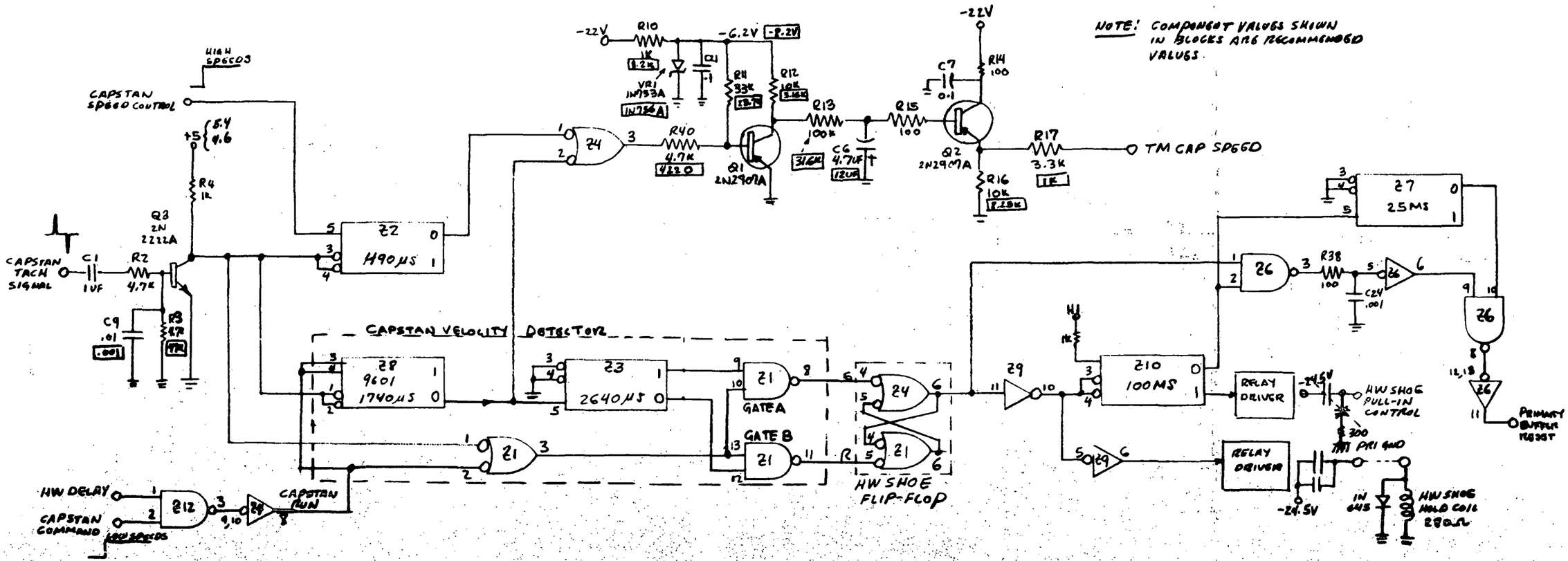


Figure 4-162. Capstan Sync Speed Detection/HW Shoe Control Logic

TO BE REVISED

pulse period. Thus if the capstan motor is rotating at the correct speed or above, the Velocity Detector will gate a set input to the Headwheel Shoe flip-flop. If, on the other hand, the capstan motor is rotating at a speed which is lower than the correct speed, the Velocity Detector will gate a reset input to the Headwheel Shoe flip-flop.

The worst case analysis of the Capstan Velocity detector was directed toward selecting appropriate delays for both the Z8 and Z3 one-shots. The requirement for tandem delay is that the minimum total delay be greater than the maximum "correct speed" period of the Capstan Tachometer signal.

When the capstan motor is being served in a Playback mode, its speed is controlled by a voltage controlled oscillator. The minimum frequency of the VCO drive is such that it will produce a Capstan Tachometer period of 3580 μs maximum. Thus, the tandem delay requirement may be expressed in equation form as follows:

$$\underline{T_D(Z8)} + \underline{T_D(Z3)} >> 3580\ \mu\text{sec.} \qquad (1)$$

In addition to the tandem delay requirement, there is a separate requirement which relates to Z8 alone. This requirement is imposed by the fact that the Z8 one-shot is re-triggerable. Because of this re-triggerable feature, the maximum delay of one-shot Z8 must be less than the maximum Capstan Tachometer period in an overspeed servo mode. The maximum frequency of the capstan servo-controlled oscillator is such that the following inequality must be observed.

$$\overline{T_{PZ8}} < 2655\ \mu\text{s.} \qquad (2)$$

As a final step, the worst case tolerances on the Z8 and Z3 one-shots (see Table 4-48) were adjusted to satisfy the conditions of equations 1 and 2 above.

Headwheel Shoe Control. - When the Headwheel Shoe is set by the Capstan Velocity Detector, both the pull-in and holding coils of the Headwheel Shoe solenoid are energized. After approximately 100 ms, the pull-in coil is de-energized.

With Reference to Figure 4-162, it will be noted that both the pull-in and holding coil circuits employ relay drivers. As a result, the analysis of the Headwheel Shoe control was primarily concerned with the stressing of relay contacts. The resistance and inductance of the shoe solenoid holding coil is such that, in the worst case, the relay contacts are never over-stressed.

The shoe pull-in control line is coupled to an amplifier (located outside of the control system) which, in turn, drives the shoe solenoid pull-in coil. The maximum current required by the amplifier is less than 5 mA. As a result, the relay contacts are virtually unstressed.

b. Primary Buffer Reset. - The Primary Buffer reset is a standard TTL logic signal output which goes "high" to enable the MSS data synchronizers once the Headwheel Shoe is engaged. The Primary Buffer reset signal interfaces with its load as shown in Figure 4-163.

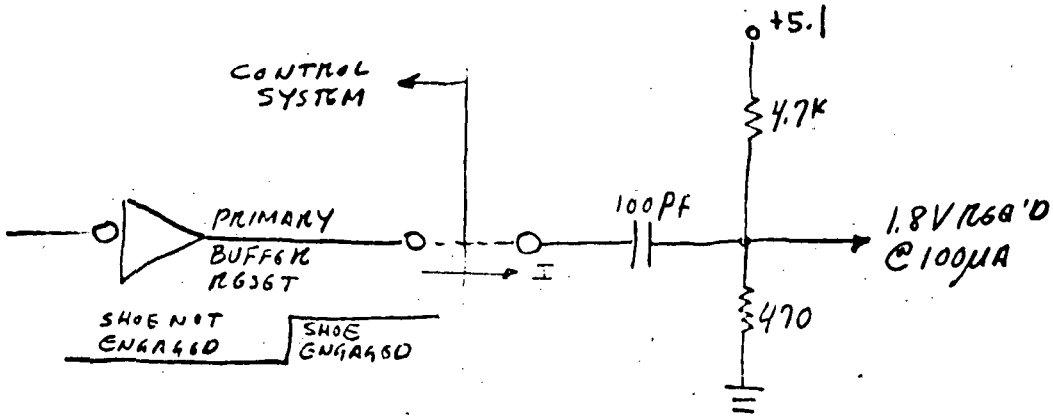


Figure 4-163. Primary Buffer Reset Interface

If reference is made to the figure, it is possible to calculate the maximum transient current loading when the Primary Buffer reset signal goes "high". From the figure,

$$I(\text{req'd}) = \frac{1.8}{420} + 100 \times 10^{-6} = 4.38 \text{ mA}$$

The current capability of a standard TTL output at 1.8 volts can be determined by extrapolating typical manufacturer's characteristics to worst case conditions. This extrapolation shows that, when in a logical

"1" state, standard TTL logic is capable of supplying 6 mA at +1.8 volts. As a result, the Primary Buffer reset signal is capable of driving a worst case load.

c. TM Capstan Motor Speed. - The TM Capstan Motor Speed signal is an analog telemetry return which must conform to the following specifications in both high speed and normal speed modes:

(1) Output voltage at capstan standstill = 0 volts

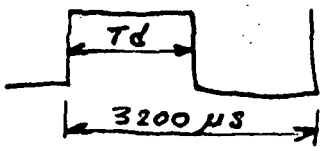
(2) Output voltage at maximum capstan speed = -5 volts

(3) Maximum output impedance = 10,000 ohms.

The TM Capstan Motor Speed circuit employs the Capstan Tachometer amplifier (Q3), delay one-shots Z2 and Z8, an OR gate, an amplifier (Q1), an integrator and a driver amplifier (Q2), as shown in Figure 4-162. In normal speed modes the output of the Z8 one-shot is fed to the amplifier/integrator network. In high speed modes, the Z2 one-shot is the driving source.

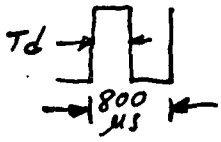
Since the TM Capstan Motor Speed signal is required to provide comparable speed indications in both high speed and normal speed modes, the duty cycle (or delay) of the Z2 one-shot must track that of the Z8 one-shot. Since the Capstan Tachometer frequency at high speeds is four times the average normal speed frequency, the delay of one-shot Z2 must be one fourth that of one-shot Z8. The delay of one-shot Z2 was adjusted to meet this requirement. Thus, as a starting point in the worst case analyses of the TM Capstan Motor Speed circuit, the "correct speed" waveforms shown in Figure 4-164 were established.

Before the TM Capstan Motor Speed circuit could be analyzed with the waveforms shown in the figure applied to its input, it was necessary to analyze the current with logic "1" and "0" inputs. In the course of this analysis it was necessary to constantly readjust parameters so as to produce an extreme output voltage swing which would accommodate the actual input waveforms shown in the figure. After all parameter adjustments had been made, the worst case maximum negative output signal levels were claculated. This resulted in an output deviation from -6.38 volts to -7.77 volts at 0° C, and from -6.98 volts to -8.22 volts at 60° C. If the duty cycles shown in Figure 4-164 are applied to these



where,
1640μs < Td < 2540μs @ 0°C
1478μs < Td < 1970μs @ 60°C

Z4-3 OUTPUT
(a) NORMAL SPEED MODES.



where
417μs < Td < 529μs @ 0°C
430μs < Td < 549μs @ 60°C

Z4-3 OUTPUT
(b) HIGH SPEED MODES.

Figure 4-164. High Speed/Low Speed Inputs to TM Capstan Motor Speed Circuit

limits, the true TM Capstan Speed output signal will vary, under worst case conditions, as follows:

At Normal speeds,

-6.17 volts < TM Capstan Speed < -3.27 volts @0° C

-5.07 volts < TM Capstan Speed < -3.22 volts @60° C

At High speeds,

-5.13 volts < TM Capstan Speed < -3.32 volts @0° C

-5.63 volts < TM Capstan Speed < -3.77 volts @60° C

If these figures are separately averaged for normal and high speed operation, the average "correct speed" TM Capstan Speed signal amplitude will be -4.43 volts at normal speed and -4.46 volts at high speed.

4.6.4 Conclusions and Recommendations. - The recommendations made within the body of this report have been reviewed with the control system design engineer and incorporated into the networks. Recommended changes in component values are listed on a module-by-module basis in Appendix G. The worst case analysis of the ERTS control system has shown that, with the addition of the recommended changes, all operating requirements are satisfied over a temperature range from 0°C to 60°C, for an projected lifetime of 10,000 hours. Recommendations made with regard to limitations in command rates based on motor history, though not substantiated by the analysis, should be investigated if the recorder is to be operated at high command rates for protracted periods of time. Operation of the recorder in a Record Lap mode is not recommended. Here again, there is an absence of definitive data to support this recommendation; however, it is advisable that laboratory tests and/or an analysis be performed. Finally it will be noted with reference to Appendix G, that most of the recommended changes involving tantelum capacitors simply request that the initial capacitance tolerance be reduced from $\pm$10% to $\pm$5%. This requirement is imposed in order to minimize worst case variations in the delay of critical one-shot timers.

4.7 Telemetry

4.7.1 Introduction. - Both analog and digital telemetry signals (Table 4-49) are generated within the ERTS recorder system. Many of these signals are generated right on the board where the function to be monitored is located; schematics of these networks (Limiter TM, Playback TM and Record TM) are shown in Figures 4-165 through 4-167. However, this approach is not convenient in several cases, and a special TM board has been set aside for this function; this board, which contains the circuitry for the Headwheel Motor Current TM, Capstan Motor Current TM and Total Current TM, is referred to as Current TM in this report. The schematic diagram of the Current TM is shown in Figure 4-168.

The Voltage Transfer Network (Figure 4-169) has the function of dropping the available -24.5 volt supply and regulating the result for auxiliary service to other recorder devices. It consists of VR1, the Zener regulator and an appropriate RC filter. The Electronic Unit Temperature TM also drops the supply, but is regulated by the temperature sensitive thermister located elsewhere.

The other TM circuits, while different in configuration, provide the same basic function of linearly amplifying the monitored ac signal, converting the ac to a dc level, and amplifying again. In the Current TM (Figure 4-168), Q1 performs the ac amplification and U6, a uA741 operational amplifier in the inverted configuration, provides the dc gain. The converter consists of Q2, C6, C7, and HP2807 diodes employed in a voltage rectifier-doubler arrangement. In all circuits the converter is enclosed by a dashed box and works into the load also enclosed. In the Limiter TM (Figure 4-165), Q7 combines with U1, an MC1545G integrated circuit

TABLE 4-49. TELEMETERED FUNCTIONS

	Recommended Sampling Rates (Note 1)	Ground Reference	Condition of Maximum Negative Voltage	Source Impedance
DIGITAL TM				
MSS STANDBY	B	POW	After command	
RBV STANDBY	B	POW	After command	
RECORD	B	POW	After command	
PLAY	B	POW	After command	
REWIND	A	POW	After command	
FORWARD	A	POW	After command	
RBV ENABLE	B	POW	After command	
RBV run tape	B	SIG	During receipt of signal	
LAP	A	POW	After command	
4 dB Rec. Adj. TM	A	SIG	Attenuator in	
2 dB Rec. Adj. TM	A	SIG	Attenuator in	
1 dB Rec. Adj. TM	A	SIG	Attenuator in	
Convert Primary Power	A	POW	After command	
VOLTAGE PROTECT ENABLE/DISABLE	A	TM	Enable condition	
Primary voltage range	A	TM	Input voltage acceptable	
Primary end of tape	A	SIG	At EOT	
Secondary end of tape	A	SIG	At EOT	
Primary beginning of tape	A	SIG	At BOT	
Secondary beginning of tape	A	SIG	At BOT	
Voltage protect relay	A	POW	When recorder disconnected	
MSS/RBV status	A	POW	When in MSS	
ANALOG TM				
TU pressure	A	TM	High pressure	
TU temperature	A	TM	Low temperature	
EU temperature	A	TM	Low temperature	
Tape footage (Note 2)	A	TM	At EOT	
Capstan motor speed	A	SIG	Maximum speed	
HWP motor speed	A	SIG	Maximum speed	
Capstan motor current	A	SIG	Maximum current	
HWP motor current	A	SIG	Maximum current	
Recorder input current	B	SIG	Maximum current	
Record current/playback voltage	A	SIG	Maximum current/voltage	
Limiter voltage	A	SIG	Maximum voltage	
Servo voltage	A	SIG	Capstan overspeed	
+5.6 V	A	SIG	Minimum Voltage	

NOTES:

1. A - 1 per 16 seconds; B = 1 per second; C - 5 per second
*The tape footage indicator can be used to measure tape position and tape motion.

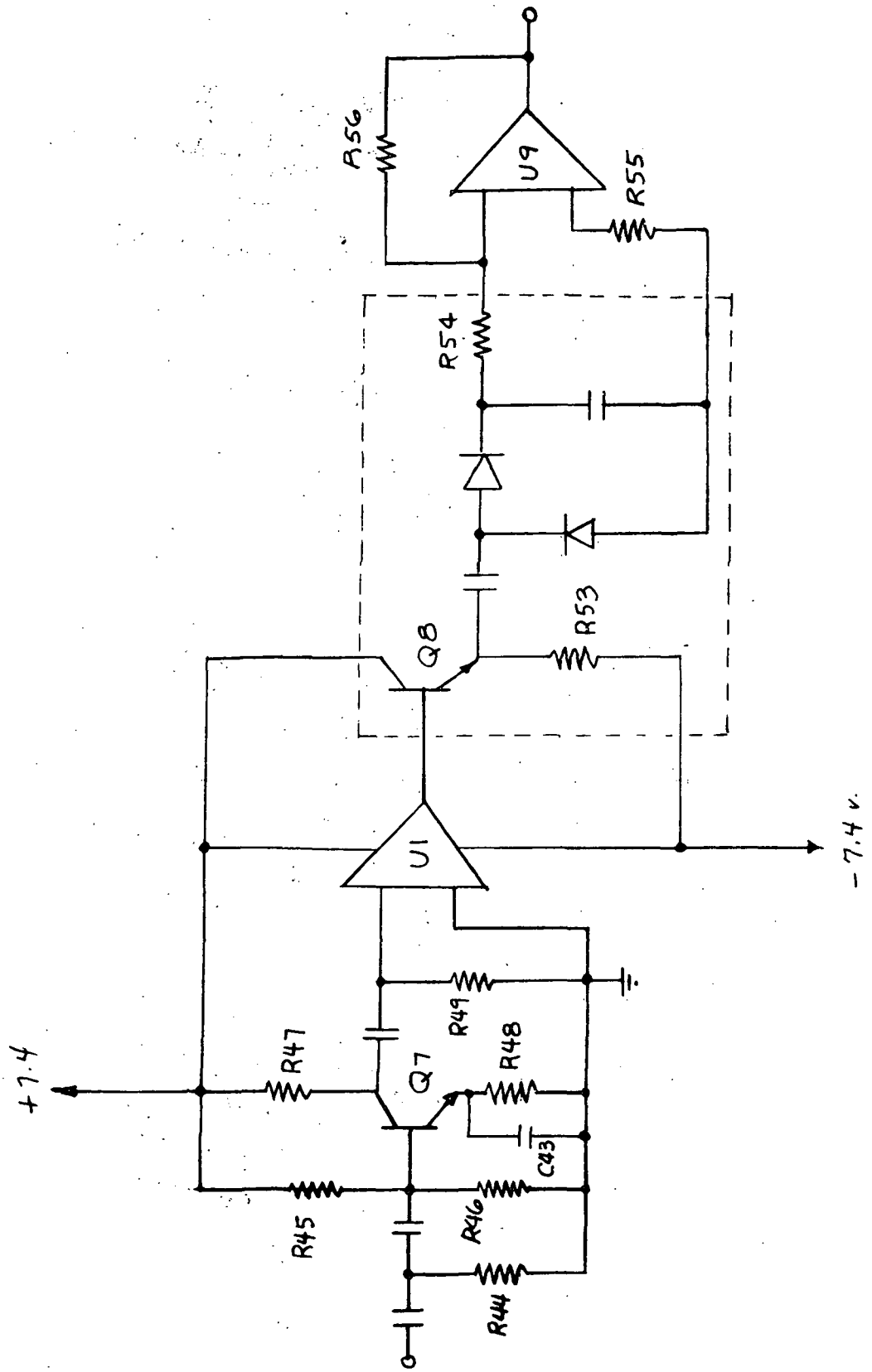


Figure 4-165. Limiter TM Schematic Diagram

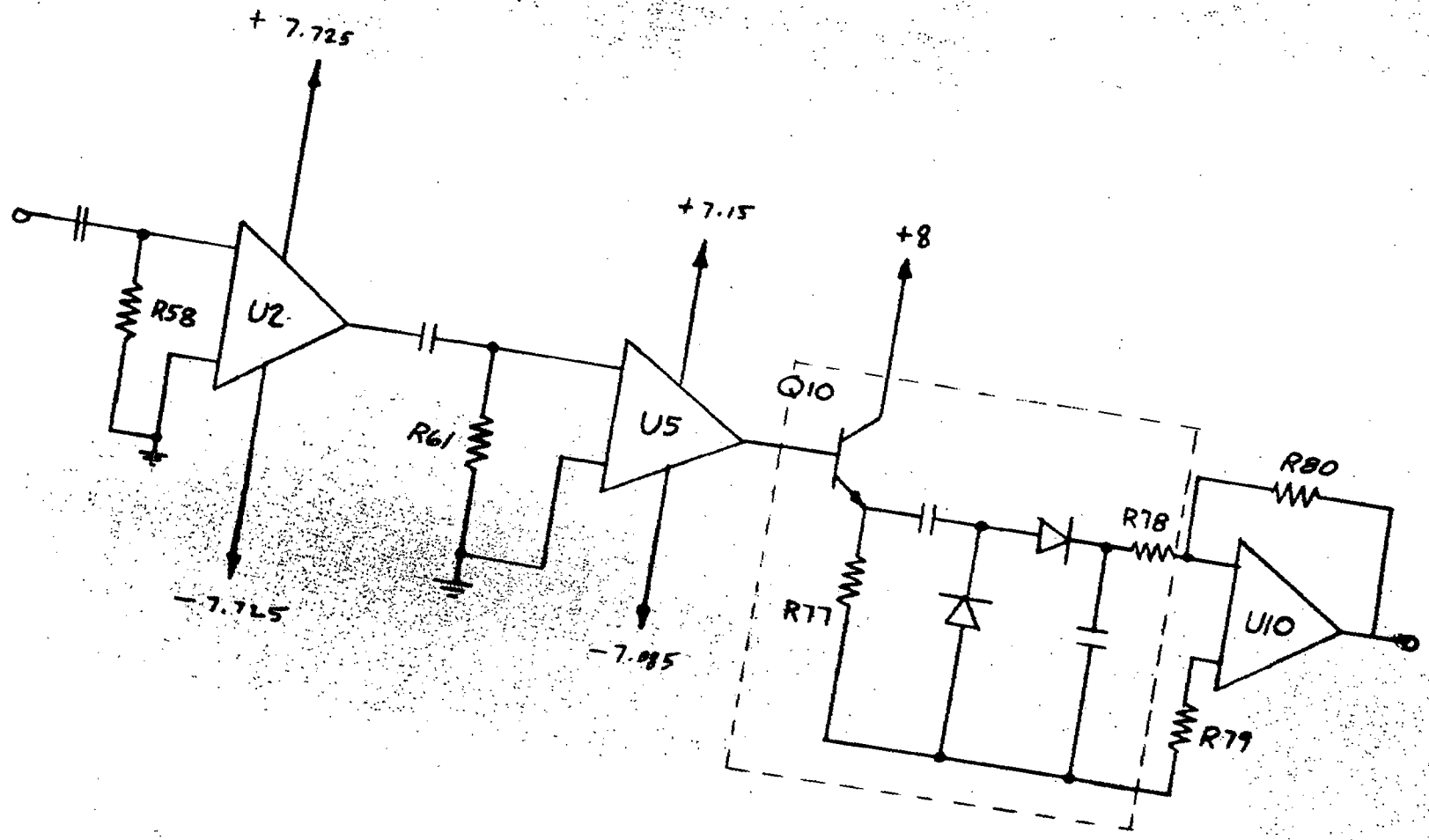


Figure 4-166. Playback TM Schematic Diagram

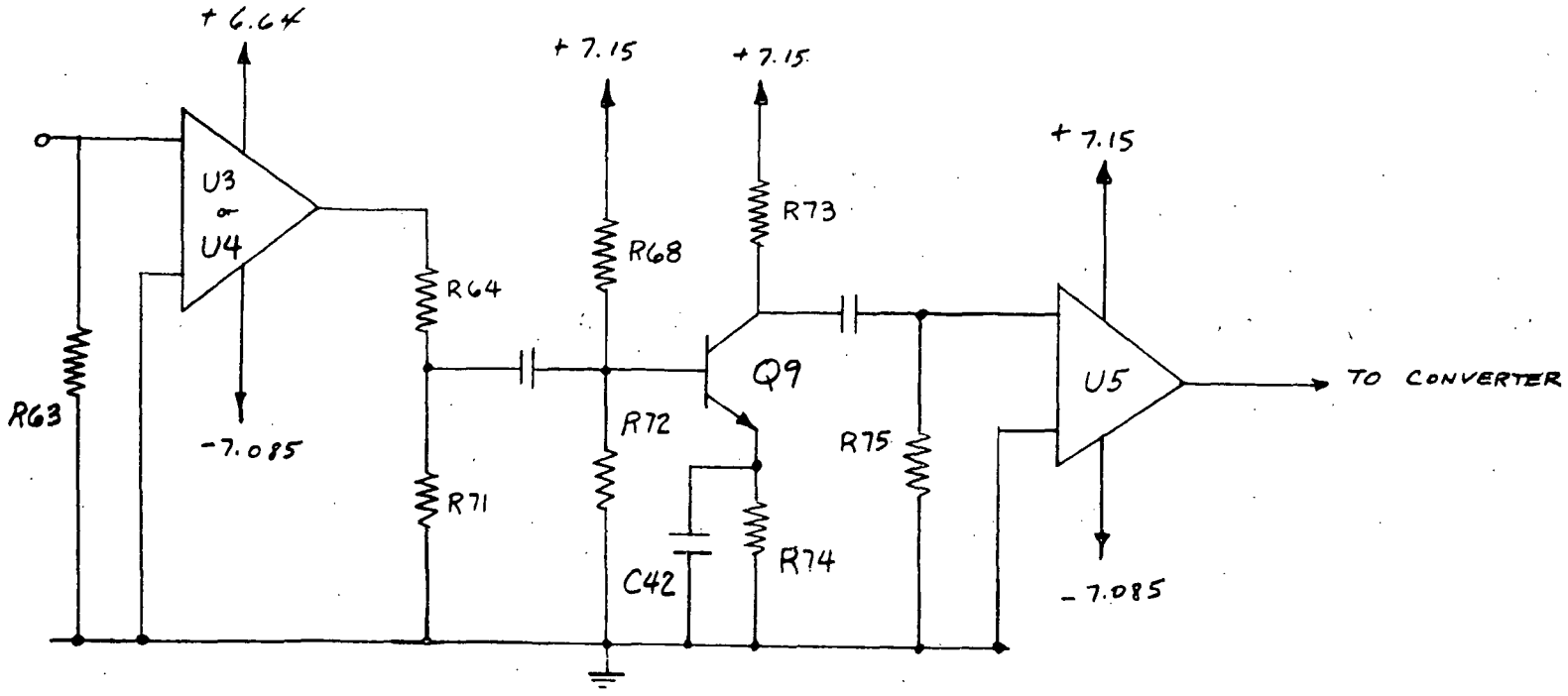


Figure 4-167. Record TM Schematic Diagram

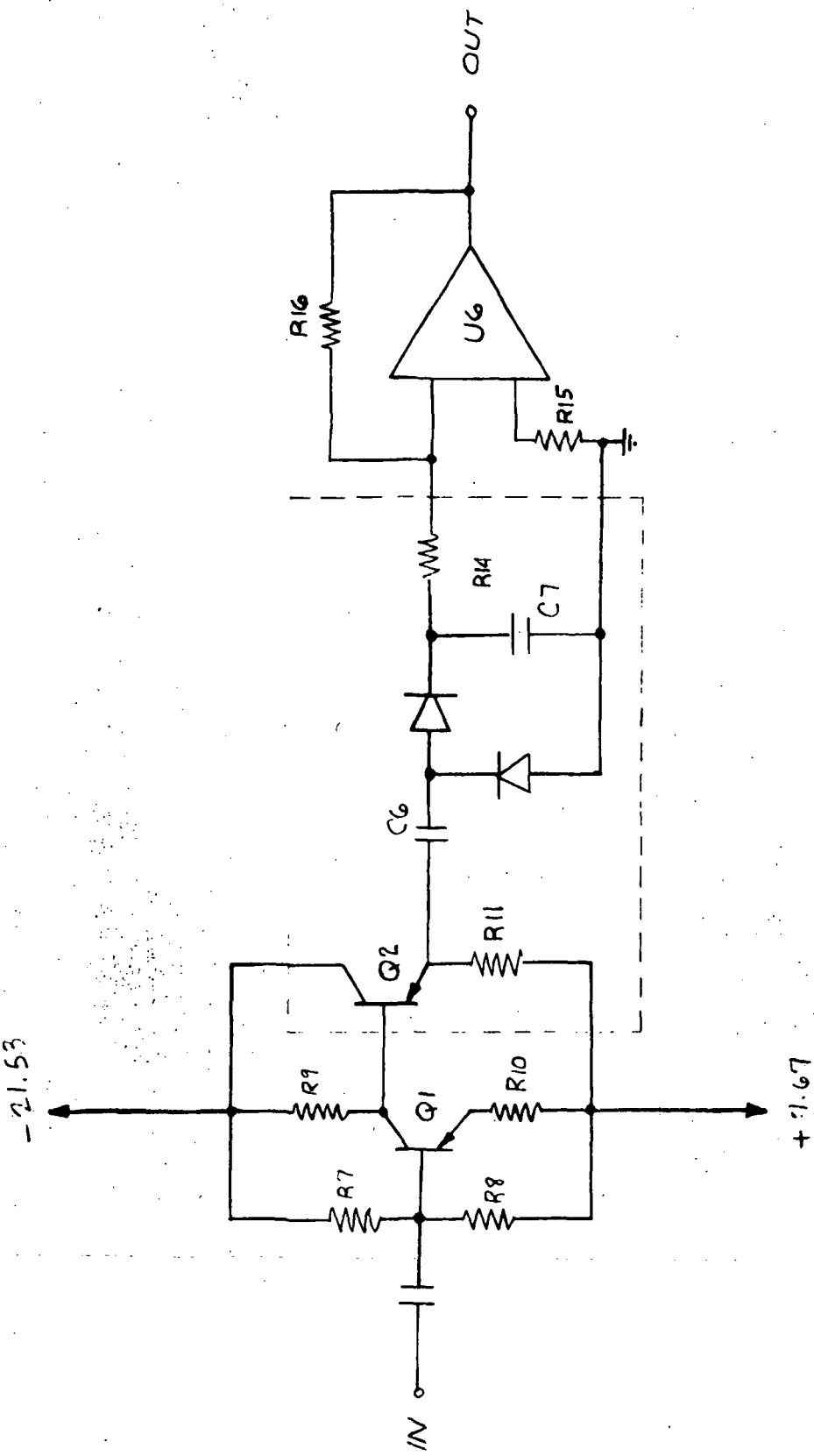


Figure 4-168. Current TM Schematic Diagram

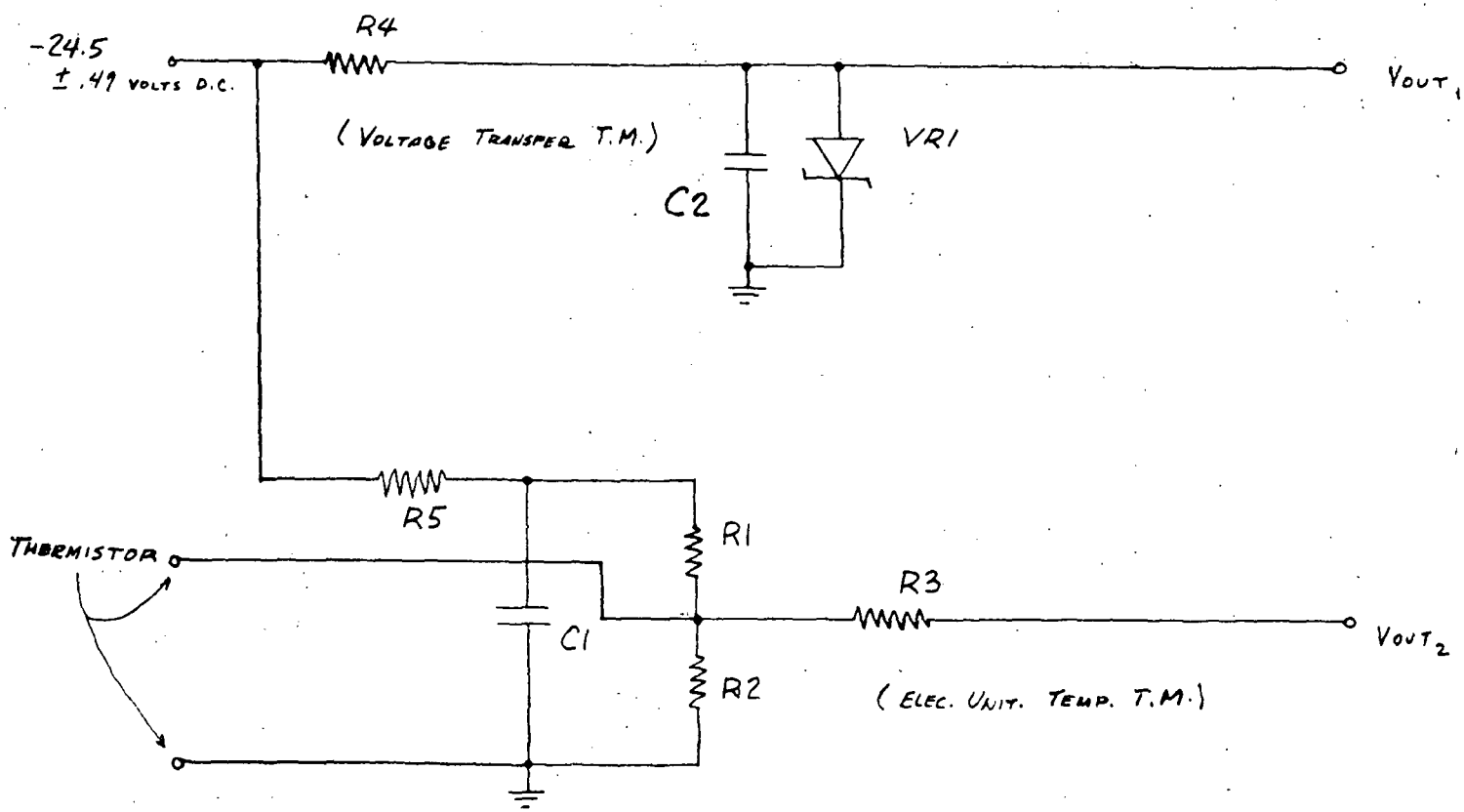


Figure 4-169. Voltage Transfer and Electronic Unit Temperature TM Schematic Diagram

amplifier, to provide ac amplification for the converter. U9, another uA741 inverter operational amplifier, performs the dc amplification. The Playback Voltage TM linear amplification (Figure 4-166) consists of U2 and one-half of U5, both MC1545G amplifiers; as shown in the figure, the converter delivers dc voltage to U10, a uA741 inverted operational amplifier. The Record TM (Figure 4-167) alternately monitors record currents from heads 1 and 3 via U3, MC1545G, and identically from heads 2 and 4. Q9 and the other half of U5 provide additional ac gain and from there the signal is delivered to the Playback TM converter and dc amplifier.

4.7.2 Telemetry Circuits Worst Case Analysis. - The telemetry board houses several circuits designed to yield a dc output related linearly to the output signal levels provided by various circuits in the recorder. In addition to these circuits, the temperature sensing network and a voltage transfer circuit are included. It is desired to describe the circuit performance at the temperature extremes of 0° and 60°C, and the effect of maximum and minimum component values. The maximum and minimum values are noted as a function of purchase, temperature and, where possible, aging tolerances. If the circuits fail as a result of the above, then values are reselected and the analysis is redone until satisfaction results. The changes are listed in the appendix and discussed in the conclusion. See Appendix H for worst case analysis criteria.

Transfer curves relating the dc output to the ac input will be provided so that a theoretical understanding of the problems that arise in the circuit is at hand.

4.7.2.1 Design Considerations. - In all cases (excluding Voltage Transfer and Electronic Unit Temperature TM) the incoming ac signal must be amplified without distortion at all levels. The quiescent operating points, then, must be selected for continued operation at the extremes. The criteria of converter design was found to be dependent upon the source impedance, load impedance and output time constant. For all converters of this sort the following condition must be met for reasonable efficiency:

$$\omega C R_L > 100$$

where

ω = angular frequency of input signal

C = the output shunt capacitor

R_L = load resistance

In addition, the source impedance (output impedance of emitter follower) must be very small while the load resistance kept high. Because of temperature variation of the diode forward voltage drops, the input signal should be kept comparatively high.

Specifications limit the output voltage range to 5 volts -- i.e., from 0 volts at minimum input voltage to -5 at maximum input. It is assumed that a reasonable error is allowed, for if the operational amplifier offset voltage is at one extreme it is possible to have a slight positive potential at the output when the input is non-existent. Operational amplifier drift due to temperature is so slight over the allowable temperature range that it can be neglected. Regardless, it is necessary to apply offset minimization principles where practical, and this was done.

Peculiar to the Limiter and Record TM is a frequency dependency due to the diminishing input impedance of the MC1545G (see Figure 4-170). Because this impedance is paralleled with the collector resistance of the preceding transistor stage, the gain of that stage diminishes proportionally and gives rise to the necessity of compensating at the emitter. The compensating capacity must be selected with care to provide the most flat response without increasing the gain beyond need. With compensation, response plots showed that at the worst case the fall of gain relative to the value at 5 MHz was no more than 0.7 dB, yet never less than zero. Further details will not be given in this report about this frequency nature.

The Record dc command, which turns off an alternate channel of U5, must be 5 volts or zero volts -- nothing in between -- or else both channels will suffer gain losses and render the whole circuit concept useless.

4.7.2.2 Feasibility. -

a. Inputs. - The signals to be monitored were not similar, nor could all of them be assigned tolerance. The Current TM input was given as 1.0 volt rms from a low source impedance, say 60 ohms; a tolerance was placed on this figure at ±5%. Since it drives a high input impedance of approximately 2000 ohms, the effect of source impedance is negligible.

This was not the case in the Limiter TM input. A known source impedance of 750 ohms delivers a constant feed of 1.4 Vpp to an infinite load but, because of the 70 ohm termination, the voltage drops are calculated and shown as the input to the transistor stage in Table 4-50.

Referring to the Playback TM input, the source impedance of 680 ohms delivers a range of 200 to 300 millivolts to an infinite load but because of the termination, the input to U2 is calculated and the results shown in Table 4-51.

A range of 20 to 70 millivolts was given as the input of U3 or U4 in the case of Record TM (Table 4-52).

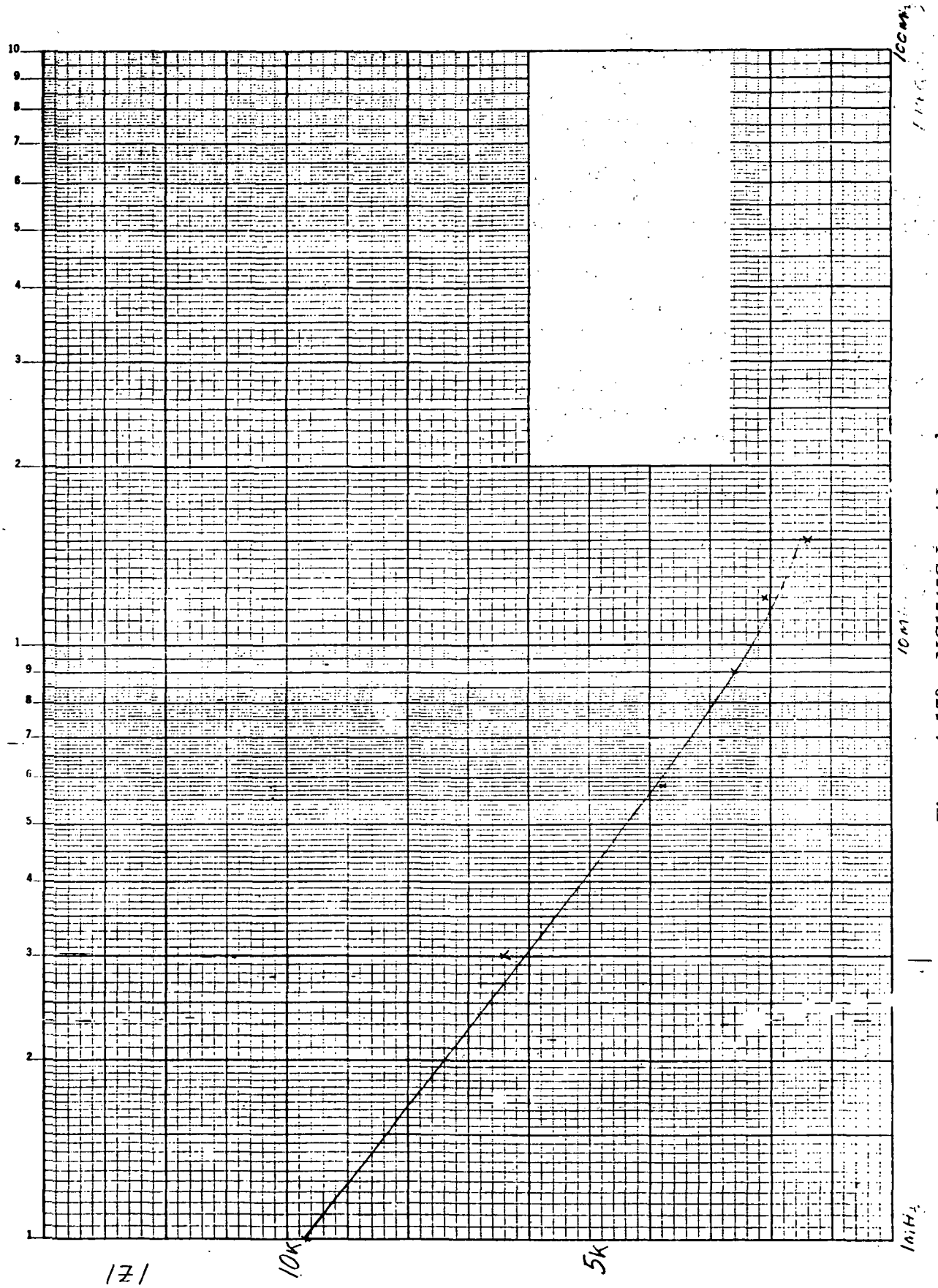


Figure 4-170. MC1545G Input Impedance

TABLE 4-50. LIMITER TM WORST CASE SUMMARY

Condition	Input (mV)	Av (Q7)	Av (U1)	Out (U1) (Volts)	κ (Conv)	Out (Conv) (Volts)	Av (U9)	Output (Volts)
0° Max	122	2.0883	9.7	2.458	54.33	1.335	-2.990	-4.141
0° Min	117	1.8521	9.7	2.095	44.86	1.04	-2.752	-2.72
60° Max	122	2.0883	9.7	2.461	63.13	1.554	-2.997	-4.808
60° Min	117	1.8521	9.7	2.095	54.69	1.23	-2.746	-3.97

TABLE 4-51. PLAYBACK TM WORST CASE SUMMARY

Condition	Input (mV)	Av (U2)	Av (U5)	Out (U5) (Volts)	κ (Conv)	Out (Conv) (Volts)	Av (U10)	Output (Volts)
0° Max	27.3	9.8	9.4	2.51	55.10	1.395	-2.990	-4.31
0° Min	26.2	9.8	9.4	2.41	53.83	1.292	-2.752	-3.42
60° Max	27.3	9.8	9.4	2.51	63.22	1.584	-2.997	-4.90
60° Min	26.2	9.8	9.4	2.41	62.16	1.496	-2.746	-3.97

TABLE 4-52. RECORD TM WORST CASE SUMMARY

Condition	Input (mV)	Av (U3)	Vin (Q9) (mV)	Av (Q9)	Av (U5)	Converter		Out (Conv)	Output (Volts)
						in.	χ		
0° Max	70	9.2	274	0.973	9.4	2.5	55.10	1.378	-4.270
0° Min	70	9.2	259	0.839	9.4	2.5	49.18	1.018	-2.664
60° Max	70	9.2	274	0.973	9.4	2.5	63.22	1.580	-4.888
60° Min	70	9.2	259	0.839	9.4	2.5	58.29	1.207	-3.177

b. Decoupling Drops. - The changes in the supply voltage itself have a negligible effect on the circuit, but drops across decoupling resistors are considerable and affect the gain of the MC1545G amplifier. This fact is taken into consideration when figuring the gain and also for establishing the maximum allowable input signal to the transistor amplifiers. Arrows indicated in the schematics of Figures 4-165 through 4-168 point to the available supply after decoupling drops.

c. Quiescent Point Variation. - As previously mentioned, the transistor amplifiers must remain linear at all times. Table 4-53 shows the worst case calculations of V_{CE}, the collector to emitter voltage; Ic, collector current; and the maximum signal allowed at the input of the transistor. This input is computed as follows:

$$\overline{V_i} = \left[\frac{(V_s - \overline{V_{CE}})}{\overline{A_V}} - V_{BE} \right] X\,2$$

where

$\underline{V_s}$ = the minimum absolute value of potential difference across the biasing network.

V_{BE} = forward voltage drop from base to emitter at the considered temperature.

$\overline{A_V}$ = the maximum voltage gain of the transistor stage.

or

$$V_i = \frac{V_{CE} - V_{CE}\,(SAT) \cdot 2}{A_V}$$

where

V_{CE} (SAT) = saturation voltage of the transistor at the given temperature.

whichever is the smaller.

TABLE 4-53. TRANSISTOR WORST CASE DATA

Transistor	Condition	I_c (mA)	V_{ce} (V)	Maximum Allowable Signal (V_{pp})	Available Supply Voltage (V)
Q1	0°-I_c Max	1.5	13.9	4.28	26.8
	0°-I_c Min	1.19	17.07	3.76	26.8
	60°-I_c Max	1.62	10.2	5.3	26.8
	60°-I_c Min	1.3	15.28	5.03	26.8
Q2	0°-I_c Max	6.05	11.2	20.4	26.8
	0°-I_c Min	6.75	8.5	18.1	26.8
	60°-I_c Max	6.10	11.34	20.7	26.8
	60°-I_c Min	6.12	9.2	17.6	26.8
Q3	0°-I_c Max	1.89	2.455	1.70	7.35
	0°-I_c Min	0.86	4.98	1.30	7.35
	60°-I_c Max	2.16	1.72	1.1	7.35
	60°-I_c Min	1.47	3.16	2.32	7.35
Q4	0°-I_c Max	0.623	4.76	4.12	7.15
	0°-I_c Min	0.254	6.185	0.72	7.15
	60°-I_c Max	0.635	4.775	3.48	7.15
	60°-I_c Min	0.255	6.190	1.30	7.15

A typical calculation of V_{CE} and I_C is as follows:

Referring to Figure 4-167,

$$V_B = \frac{\left[1 + h_{FE}) \text{ R74//R72} \right] \left[7.15 \right]}{\text{R68} + \left[(1 + h_{FE}) \text{ R74//R72} \right]}$$

$$V_E = V_E - V_{BE}$$

$$I_E \approx I_C = \frac{V_E}{\text{R74}}$$

$$V_C = I_C \text{ x (R73)}$$

$$V_{CE} = V_C - V_E$$

d. Power Dissipation. - Power dissipation for all the transistors at maximum worst case is very much lower than the manufacturers design maximum, which is lower than military specification requirements. Such conditions as leakage and thermal runaway are completely negligible. Typically,

$$P_{diss} = V_{CE} \cdot I_c + \frac{V_{cc} \text{ (peak)} \cdot i_c \text{ (peak)}}{2}$$

$$\cong 6 \text{ to } 50 \text{ milliwatts}$$

e. Converter Discussion. - The voltage rectifier-doubler (converter) used in the telemetry circuits is of a non-linear nature and was too complicated to analyze in depth. Laboratory measurements under conditions similar to those encountered in actual operation were relied upon in this report. Figures 4-171 through 4-175 show the results of the laboratory tests.

The converter efficiency (η), defined in this case as the percentage of dc voltage out relative to the applied peak to peak voltage in, is dependent upon three factors:

(1) Load Resistance (assuming always that the source impedance is lower than 50 ohms).

(2) Temperature.

(3) Input Signal Level.

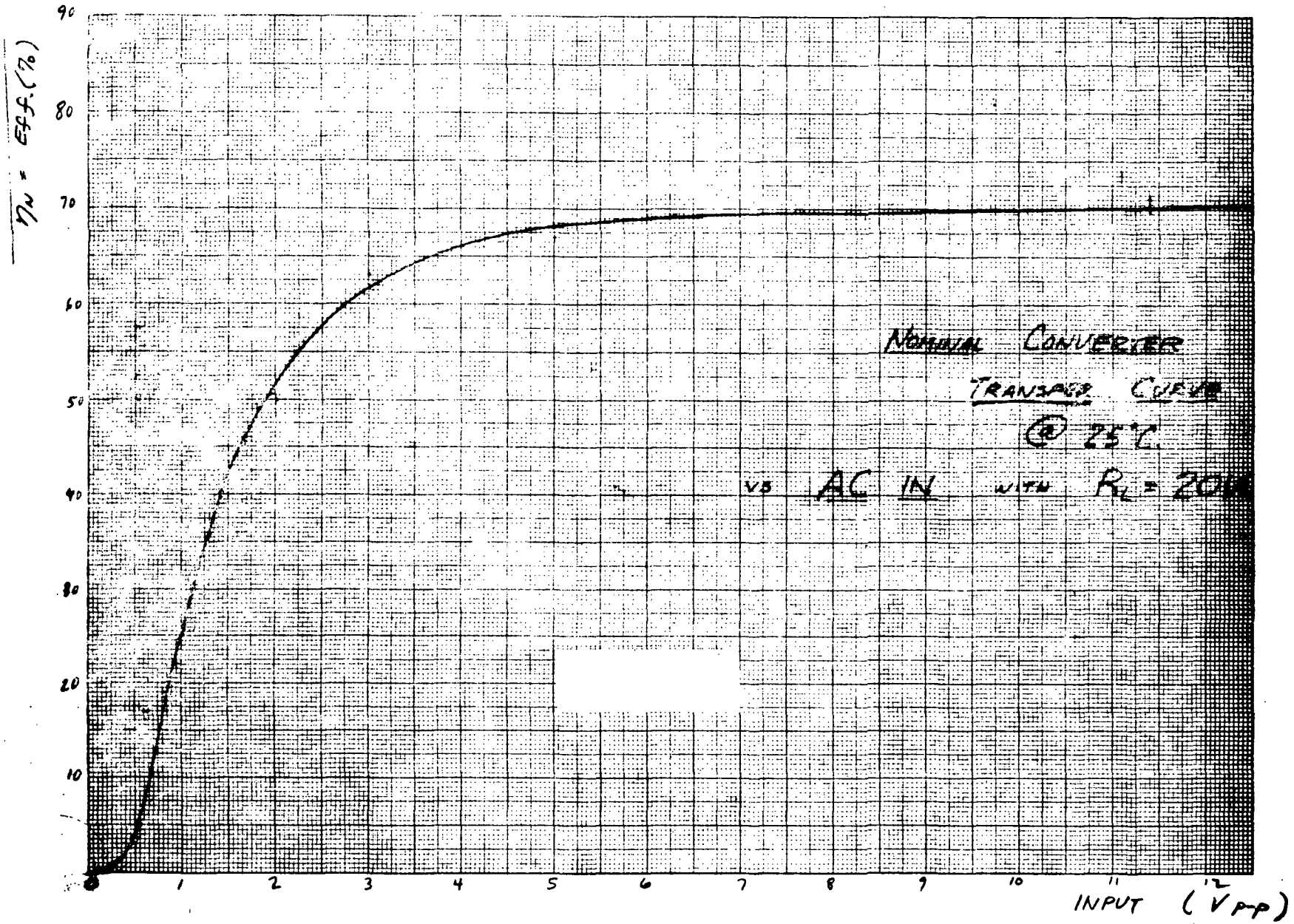


Figure 4-171. Nominal Converter Transfer Curve

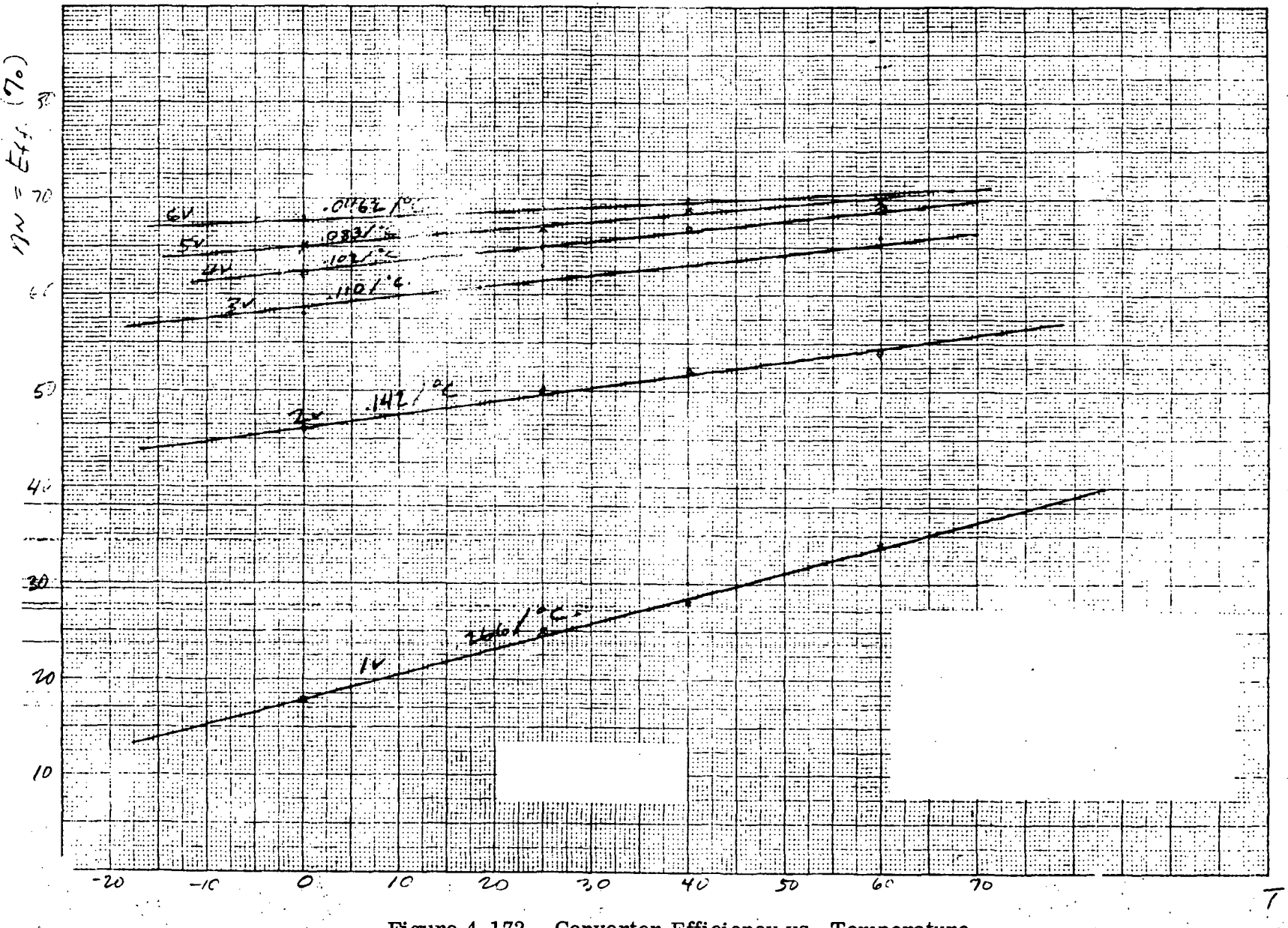


Figure 4-172. Converter Efficiency vs. Temperature

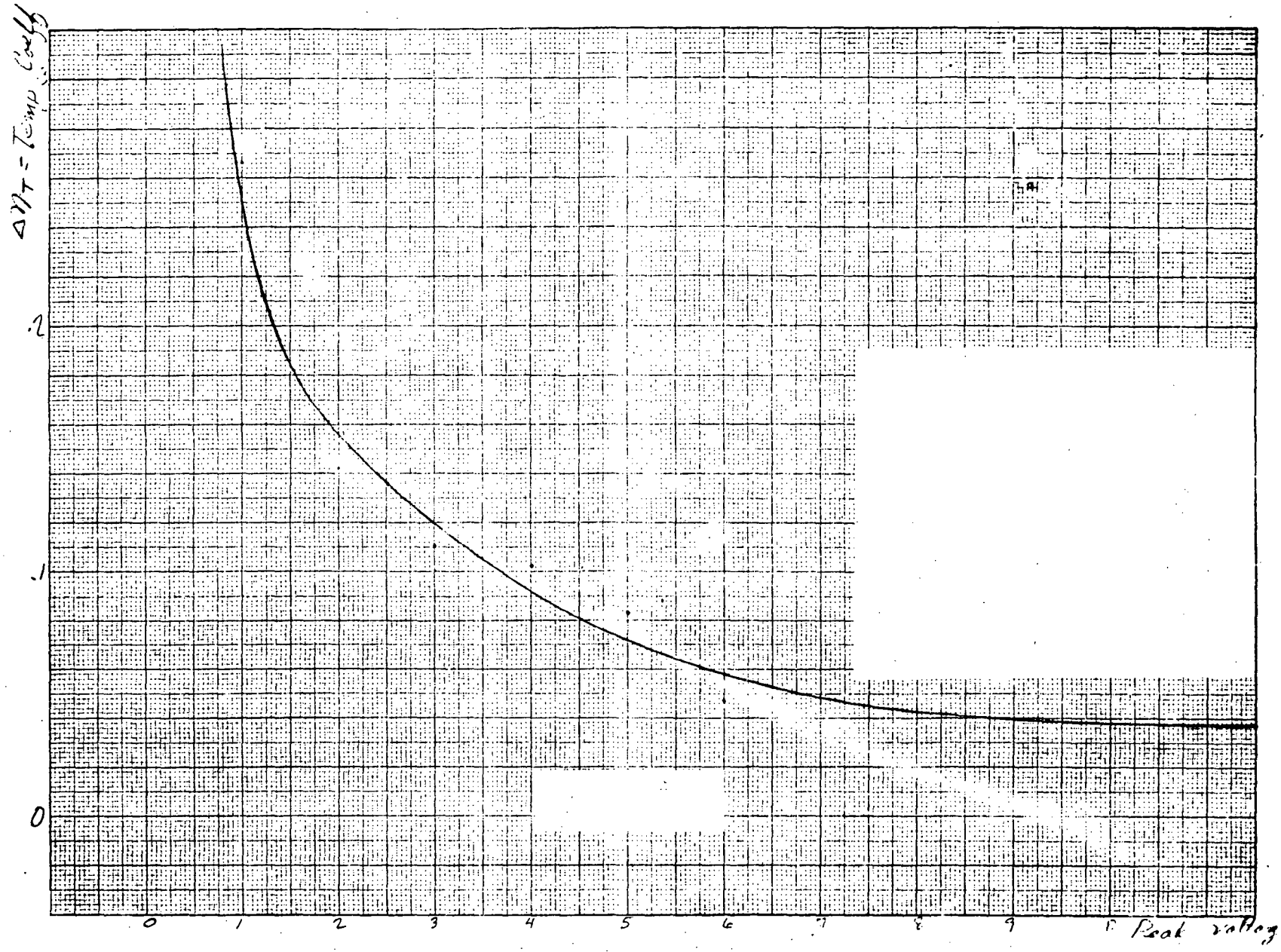


Figure 4-173. Converter Temperature Coefficient ($\Delta\eta_T$) vs. Max Voltage

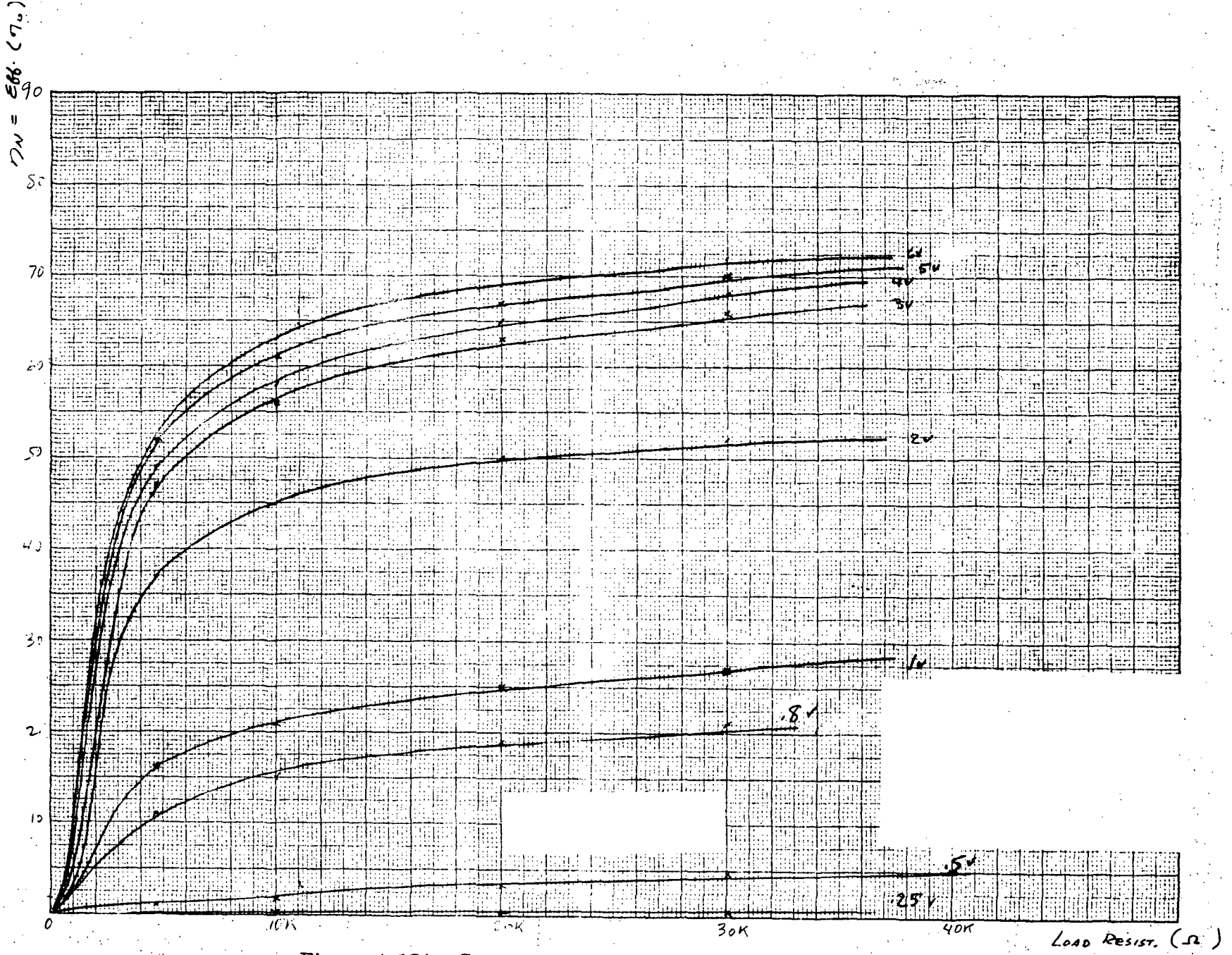


Figure 4-174. Converter Transfer Coefficient vs. Load Resistance

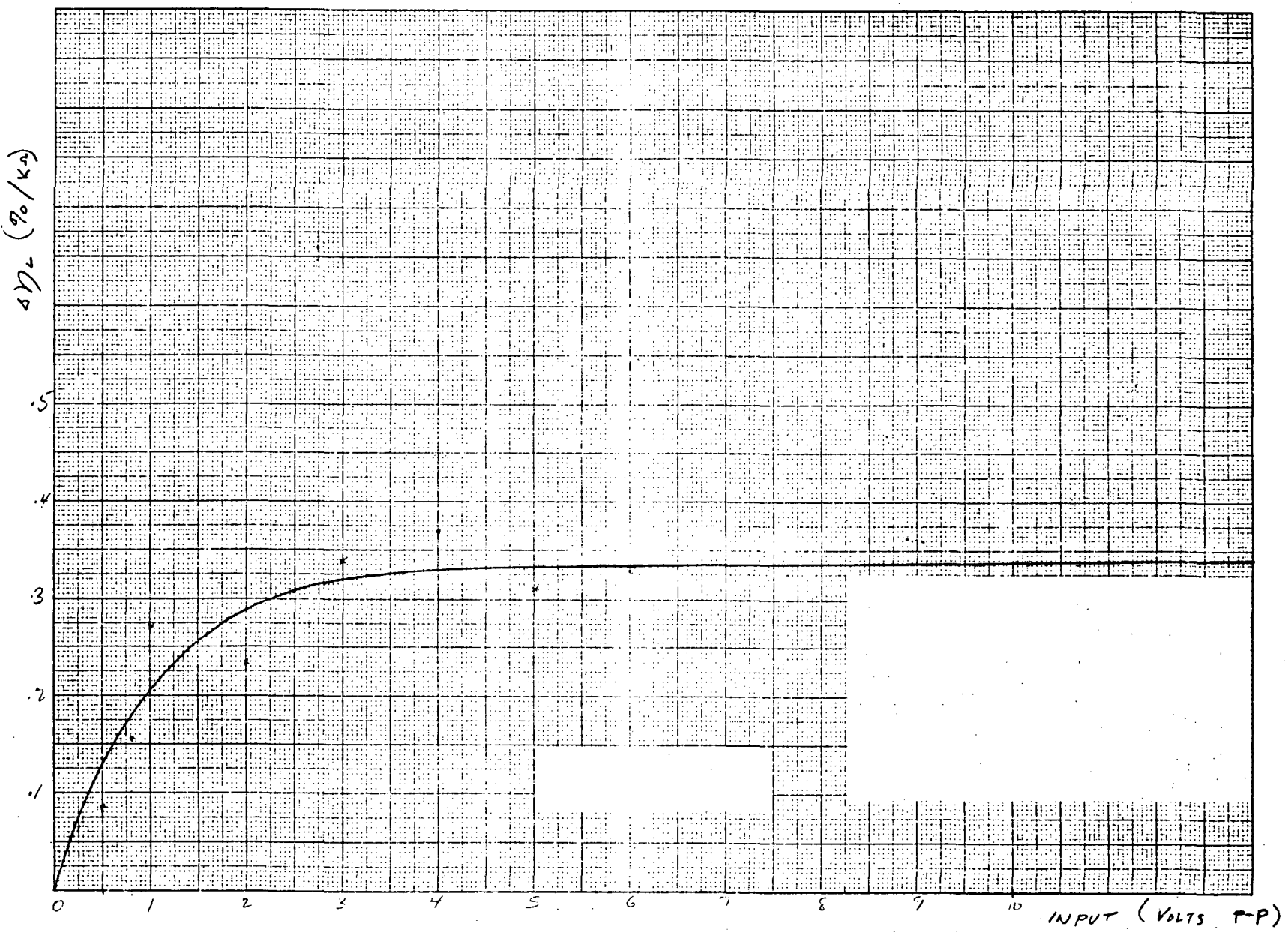


Figure 4-175. Loading Coefficient ($\Delta\eta_L$) vs. AC Input

The third factor is the crucial one, in that as input signal fades the converter proliferates the fading. It is easy to see why a perfectly linear telemetry transfer curve is impossible (see Figures 4-176 through 4-179). A whole family of curves of the type shown in Figure 4-171 could have been drawn with R_L as the variable, but it was chosen to establish a loading coefficient, $\Delta\eta_L$, based on deviation from 20 kohms. $\Delta\eta_L$ is derived from the experimental data shown in Figure 4-174. Similarly, a temperature coefficient, $\Delta\eta_T$, based on 25°C is derived from the experimental data of Figure 4-172. The total efficiency of the converter is:

$$\eta = \eta_N + T\ (\Delta\eta_T) + \Delta L\ (\Delta\eta_L)$$

All of these parameters are purposely made functions of input voltage. For any input voltage to the converter, a new efficiency, or transfer constant, had to be established.

f. Assumptions. - In all cases, the gain-bandwidth product of the transistors used were high enough to eliminate the worry of input impedance roll-offs due to Miller effect. The small signal emitter current, i_e, was assumed to be a good approximation of i_c, therefore making the useful relationship hold:

$$A_V = \frac{R_L}{R_E}$$

It follows that h_{FE} is assumed to be high enough at worst case to justify the assumption that the emitter followers do not load the preceding stages.

The maximum allowable output swing of the MC1545G was observed in the lab to be only 2.7 volts instead of the proclaimed 4.0 volts under the same operating conditions. Therefore, a limit of 2.5 volts was set as the maximum in the worst case analysis.

4.7.2.3 Worst Case Calculations. - Worst case calculations are tabulated in Tables 4-50 through 4-52 and 4-54. 0° Max means that the change in components due to tolerances is additive in the sense of yielding the maximum output at the given temperature; 0° min. implies the opposite, i.e., the components change in the opposite sense yielding the minimum output. The outputs in the tables are due to the maximum input signal levels, observing the maximum and minimum tolerances on them; thus, the trivial case where the input is zero, has not been included in tables. This does not imply that the output is zero upon zero input -- it is maximum or minimum offset voltage of the operational amplifier. Further clarification may be found by observing Figures 4-176 through 4-179.

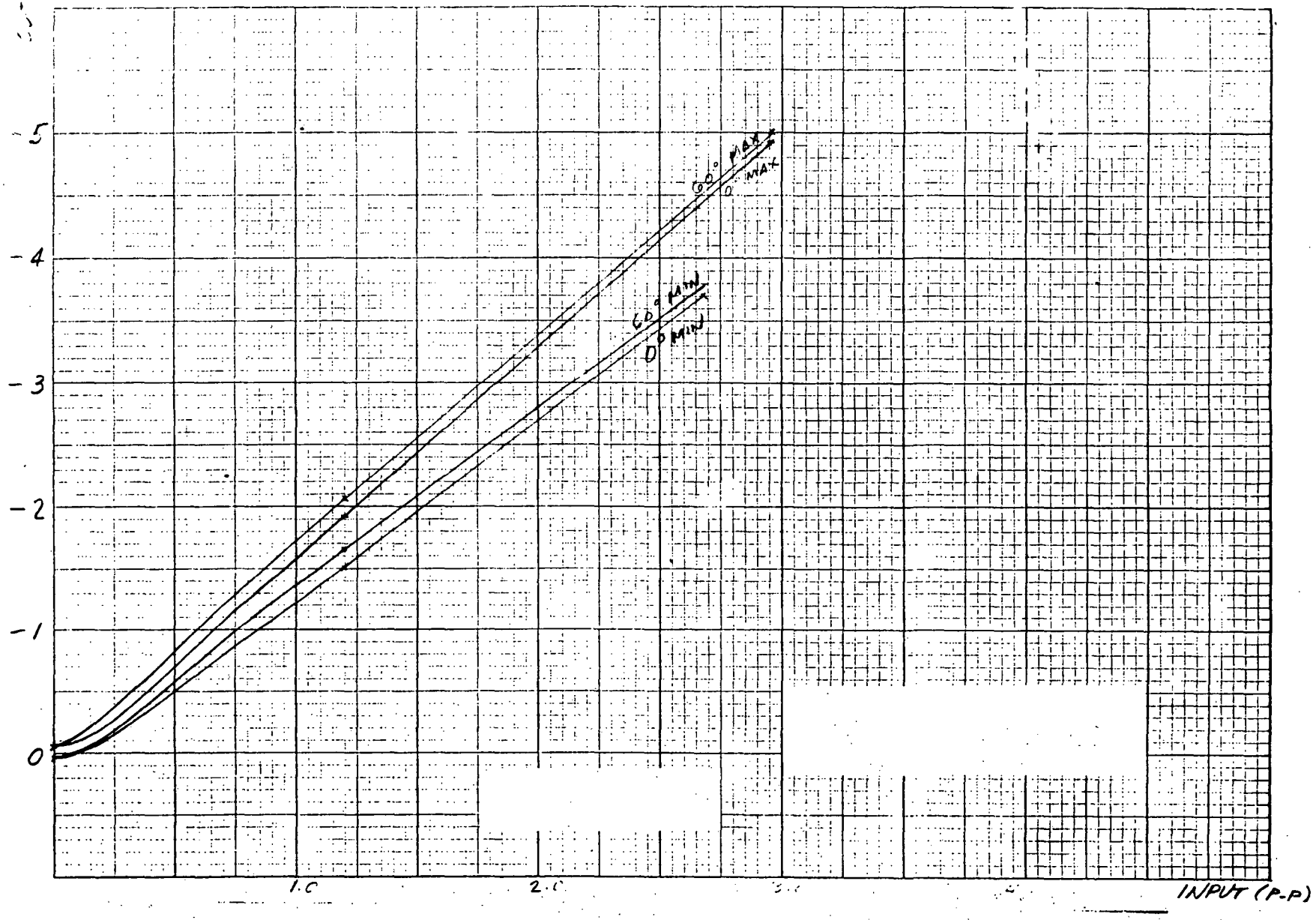


Figure 4-176. Current TM

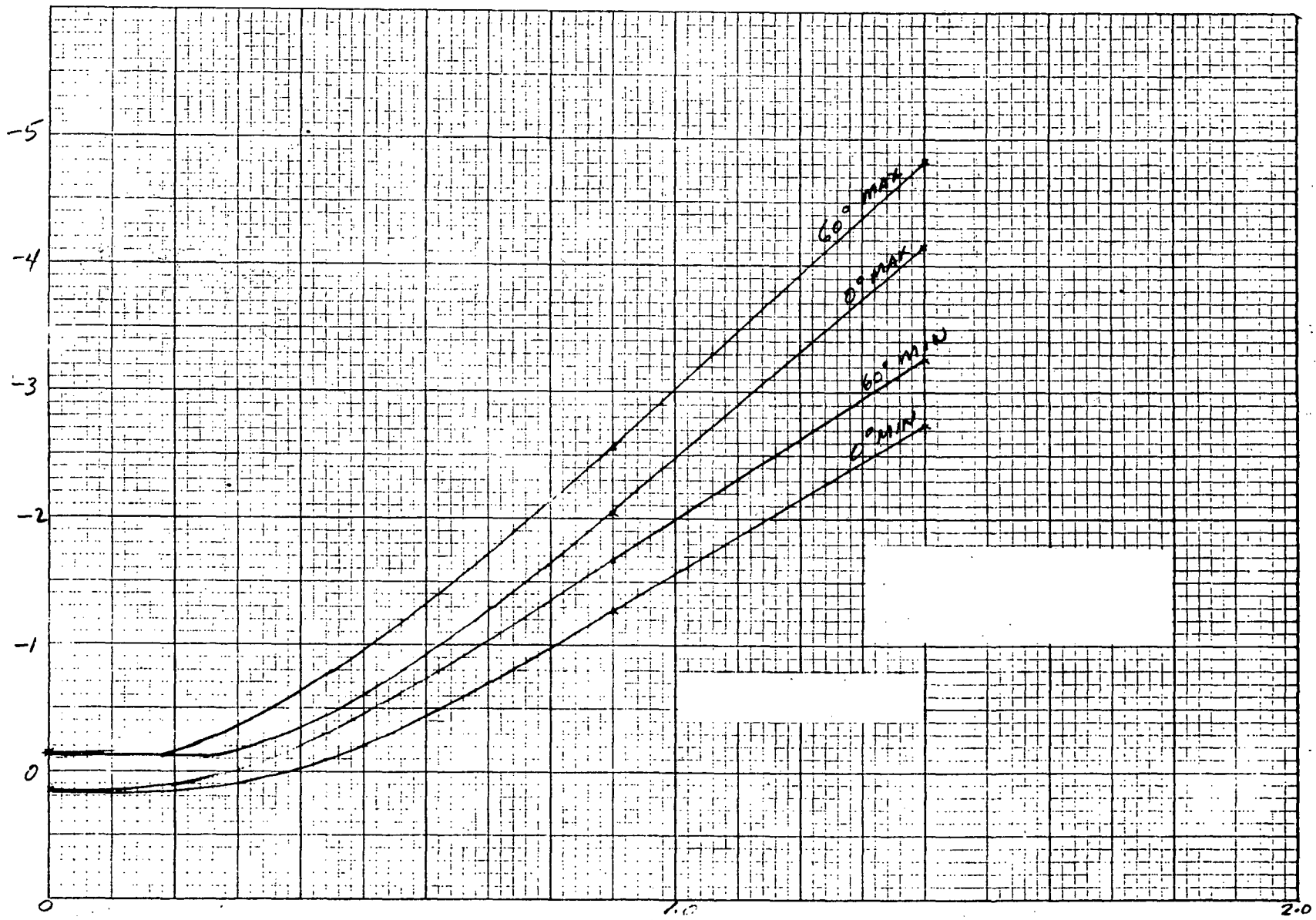


Figure 4-177. Limiter TM

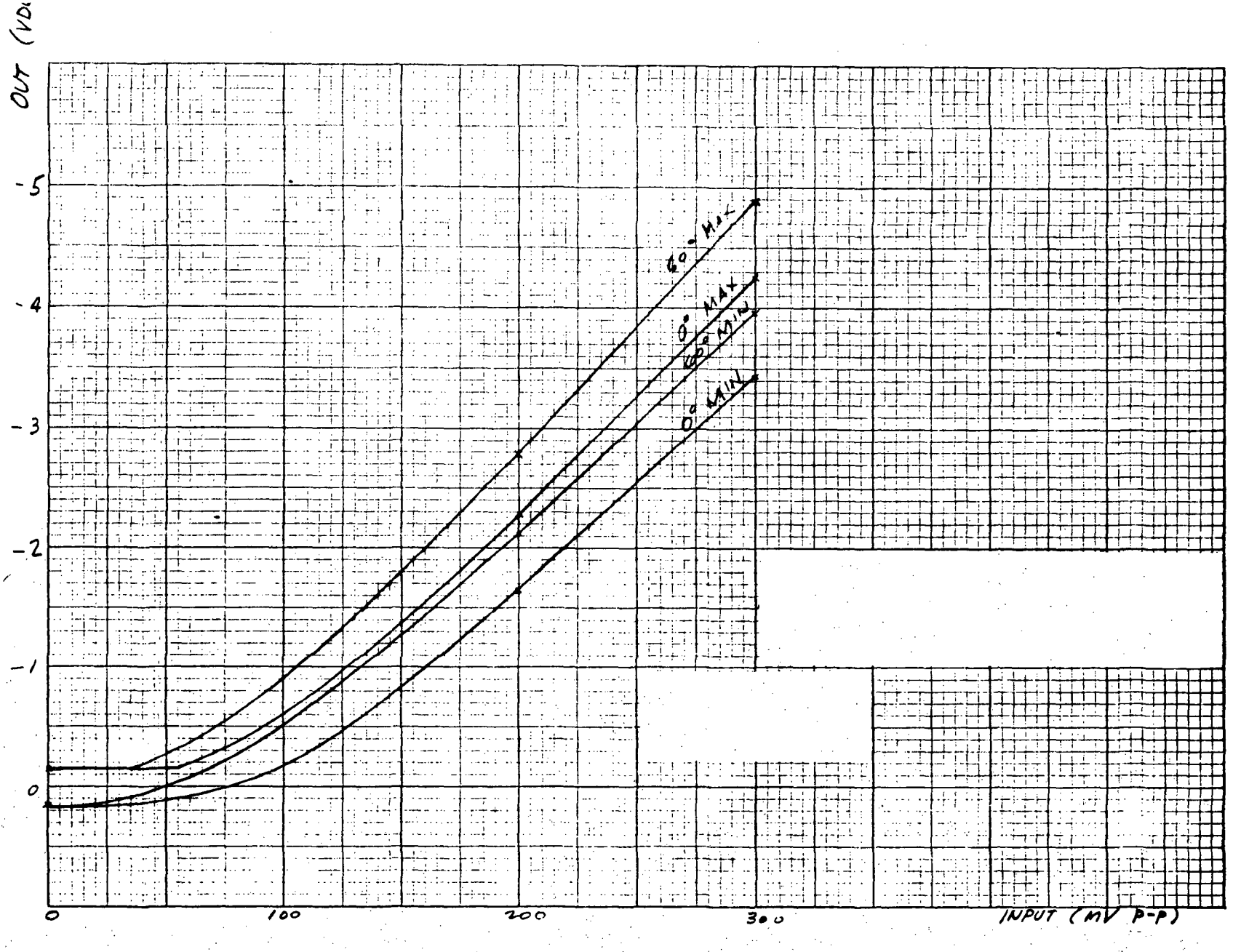


Figure 4-178. Playback Voltage TM

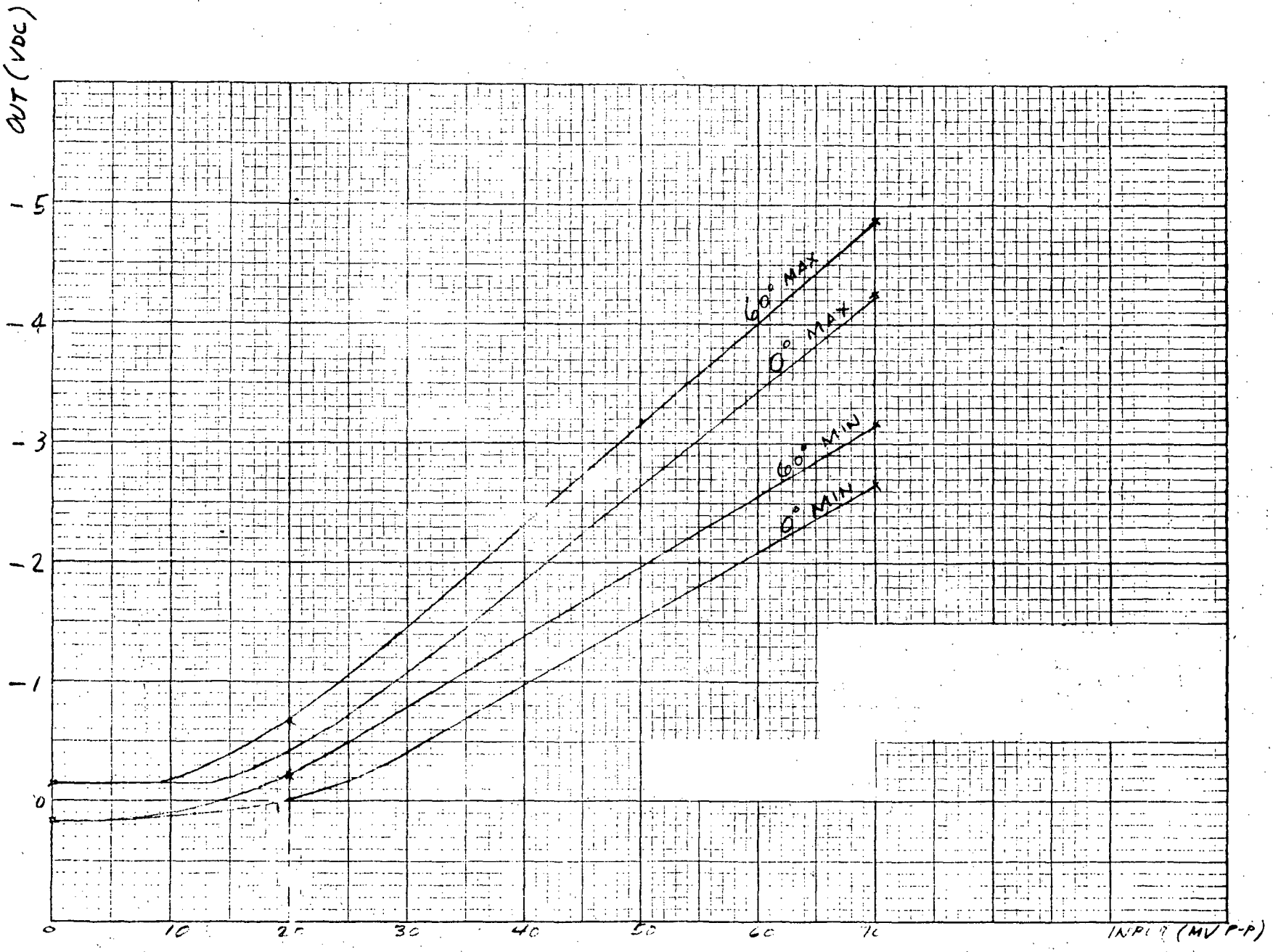


Figure 4-179. Record Current TM

TABLE 4-54. CURRENT TM WORST CASE SUMMARY

Condition	Input	Av (Q1)	Out (Q1)	χ (Conv)	Out (Conv)	Offset U6	Av (U6)	Output
0° Max	2.96	4.1	12.133	70.94	8.607	+50.3	-0.5706	-4.939
0° Min	2.68	3.76	10.875	69.61	7.570	-50.3	-0.5252	-3.949
60° Max	2.96	4.1	12.136	71.64	8.694	+50.3	-0.5719	-5.000
60° Min	2.68	3.76	10.077	71.85	7.240	-50.3	-0.5241	-3.768

a. Current TM (Figure 4-168, Table 4-54). - The signal may be traced as follows:

$$\text{Input} = 2.82 \text{ Vpp} \pm 5\% \text{ given}$$

$$A_V\,(Q1) = \frac{R_9}{R_{10}}$$

$$\text{Out (Q1)} = \text{Input} \cdot A_V\,(Q1)$$

$$\eta(\text{Conv}) = \eta_N + \Delta T\,(\Delta\eta_T) + \Delta L\,(\Delta\eta_L)$$

$$= 70 + \Delta T\,(0.037\%/^\circ C) + \Delta L\,(0.34\%/\text{kohms})$$

from Figures 4-171 through 4-175

$$\text{Out (Conv)} = \text{Out (Q1)} \cdot \eta\,(\text{Conv})$$

$$\text{Offset (U6)} = \text{Input Bias Current} \cdot \text{R14} + \text{Input Offset Current} \cdot \text{R14} + \text{Input Offset Voltage}$$

(for μA741)

$$A_V\,(U6) = \frac{R_{16}}{R_{14}}$$

$$\text{Output} = A_V\,(U6) \cdot [\text{Out (Conv)} + \text{Offset (U6)}]$$

b. Limiter TM (Figure 4-165, Table 4-50). -

$$\text{Input} = \frac{R_{44}\,(1.4)}{R_{44} + 750}$$

$$A_V\,(Q7) = \frac{\text{R47//R49//}\ Z_{in}\,(U1)}{|Z_{E7}|}$$

where

$$|Z_{E7}| = \frac{R48 \cdot X43}{\sqrt{(R48)^2 + (X43)^2}}$$

$|Z_{in}\ (U1)|$ = Magnitude of MC1545G input impedance

$A_V\ (U1)$ = Mfg. Data for ± 7.4V supply

Out (U1) = Input $\cdot A_V\ (Q7) \cdot A_V\ (U1)$

η(Conv) = $\eta_N + \Delta T\ (\Delta\eta_T) + \Delta L\ (\Delta\eta_L$

Out (Conv) = η(Conv) $\cdot$ Out (U1)

$$A_V\ (U9) = \frac{R_{56}}{R_{54}}$$

Output = A_V (U9) [Out (Conv) + Offset (U6)]

c. Playback TM (Figure 4-166, Table 4-51). -

$$\text{Input} = \frac{R_{58}\ (300\ \text{mV})}{R_{58} + 680}$$

$A_V\ (U2)$ = Mfg. Data for ± 7.725V Supply

$A_V\ (U5)$ = Mfg. Data for ± 7.12V Supply

Out (U5) = Input $\cdot A_V\ (U2) \cdot A_V\ (U5)$

η(Conv) = $\eta_N + \Delta T\ (\Delta\eta_T) + \Delta L\ (\Delta\eta_L)$

Out (Conv) = η(Conv.) $\cdot$ Out (U5)

$$A_V\ (U10) = \frac{R_{80}}{R_{78}}$$

Output = [Out (Conv.) + Offset (U6)] $\cdot A_V$ (U10)

d. Records TM (Figure 4-167, Table 4-52). -

Input = 70 mV (expected value of record current)

A_V (U3) = Mfg. data for ±6.85

$$V_{in}\ (Q9) = \frac{\left[|Z_{in}|//R72//R68//R71\right] \cdot \text{INPUT} \cdot A_V\ (U3)}{\left[|Z_{in}|//R72//R68//R71\right] + R64}$$

where

$$|Z_{in}| = \frac{X42 \cdot R74}{\sqrt{X42^2 + R74^2}}$$

$$A_V\ (Q9) = \frac{R73//R75//|Z_{in}\ (U5)|}{|Z_{E9}|}$$

where

$$|Z_{E9}| = \frac{R74 \cdot X42}{\sqrt{R74^2 + X42^2}}$$

A_V (U5) = Mfg. data for ±7.12V supply

Converter IN = A_V (Q9) · A_V (U5) · V_{in} (Q9)

Converter η = $\eta_N + \Delta T\ (\Delta\eta_T) + \Delta L\ (\Delta\eta_L)$

Out (Conv) = Converter IN · Converter η

Output = [Out (Conv) + Offset (U6)] · A_V (U10)

e. Voltage Transfer TM (Figure 4-169). - The prime considerations here are supply variation, VR1 tolerance of reverse breakdown voltage, and power dissipation of the zener.

Typically:

$V_{Out\ 1} = VB \pm \Delta BV$

$$I_Z = \frac{|(V_{Supply} \pm V_{Supply})| - |V_{out\ 1}|}{R4 \pm R4}$$

where

I_Z is the diode reverse current.

$$P_{diss} = I_z \cdot BV$$

The power dissipation was calculated and found to be, at maximum, 51.5 milliwatts. This is well below the critical value of 368 milliwatts. Due to the tolerances supplied:

$|V_{out}\ (0^\circ\ Max.)| = -8.312$ Volts

$|V_{out}\ (0^\circ\ Min.)| = -6.665$

$|V_{out}\ (60^\circ\ Max.)| = -8.34$

$|V_{out}\ (60^\circ\ Min.)| = -6.67$

R4 dissipation at worst case is 100 mW.

f. Electronic Unit Temperature TM (Figure 4-169). - It was found that the capacitor leakage current was insignificant compared to the current drawn by R1 and R2 and was neglected. V_{OUT} 2 is calculated from the relationship:

$$V_{OUT}{}^2 = \frac{(R2//RT)\ (V\ Supply + \Delta V\ Supply)}{(R2//RT) + R1 + R5}$$

where

RT = Thermistor Resistance

All tolerances considered:

$V_{OUT\ 2}\ (0^\circ$ - Max.) = 4.17 Volts

$V_{OUT\ 2}\ (0^\circ$ - Min.) = 3.62

$V_{OUT\ 2}$ (60° - Max.) = 0.965

$V_{OUT\ 2}$ (60° - Min.) = 0.886

4.7.2.4 Conclusions and Recommendations. - The following explains component changes:

(a) R44 and R58 were changed to lower the input level, since the MC1545G maximum output swing was exceeded.

(b) The configuration of the operational amplifier was changed from a non-inverting to an inverting type and the diodes of the converter were reversed to accommodate the change.

(c) R15, R28, R41, R55 and R79 were revalued to acquire minimum offset of the operational amplifiers.

(d) Biasing resistors R7, R8, R9 and R10 were changed to suit interfacing with the transformer source.

(e) R49 and R75 were changed, and both C42 and C43 were added to shape the desired frequency response.

With these changes, the circuit will provide linear amplification and conversion to a dc output without exceeding specifications over almost the entire input level range. It has been mentioned that at low level input conditions the linearity disappears because of the diode forward voltage drops (which can not be avoided without a more elaborate arrangement), and also that a slight positive potential may be observed at worst case. The approximate transfer curves of Figures 4-176 through 4-179 should remove any misunderstanding as to this point.

4.8 Power Budget

The power budget for the EU and TU of the recorder system is given in Table 4-55. During start up the power division between the two units has not been divided; however, the major portion is dissipated in the TU. The primary power profile is shown in Figure 4-180.

TABLE 4-55. POWER BUDGET (ENGINEERING MODEL)

Mode	Power Consumption (Watts)			
	Start-up	Steady State		
	EU and TU	EU	TU	EU & TU
WBVTR ON (MSS or RBV Standby)	(200) (45)	20	23	43
MSS or RBV Record		40	52	92
RBV Playback		33	54	87
MSS Playback		49	54	103
Fast Forward or Rewind	110 (2.05)	16	39	55
WBVTR OFF	—	0.5	—	0.5
After WBVTR OFF and V.P. Negate Commands	—	0.5	—	0.5

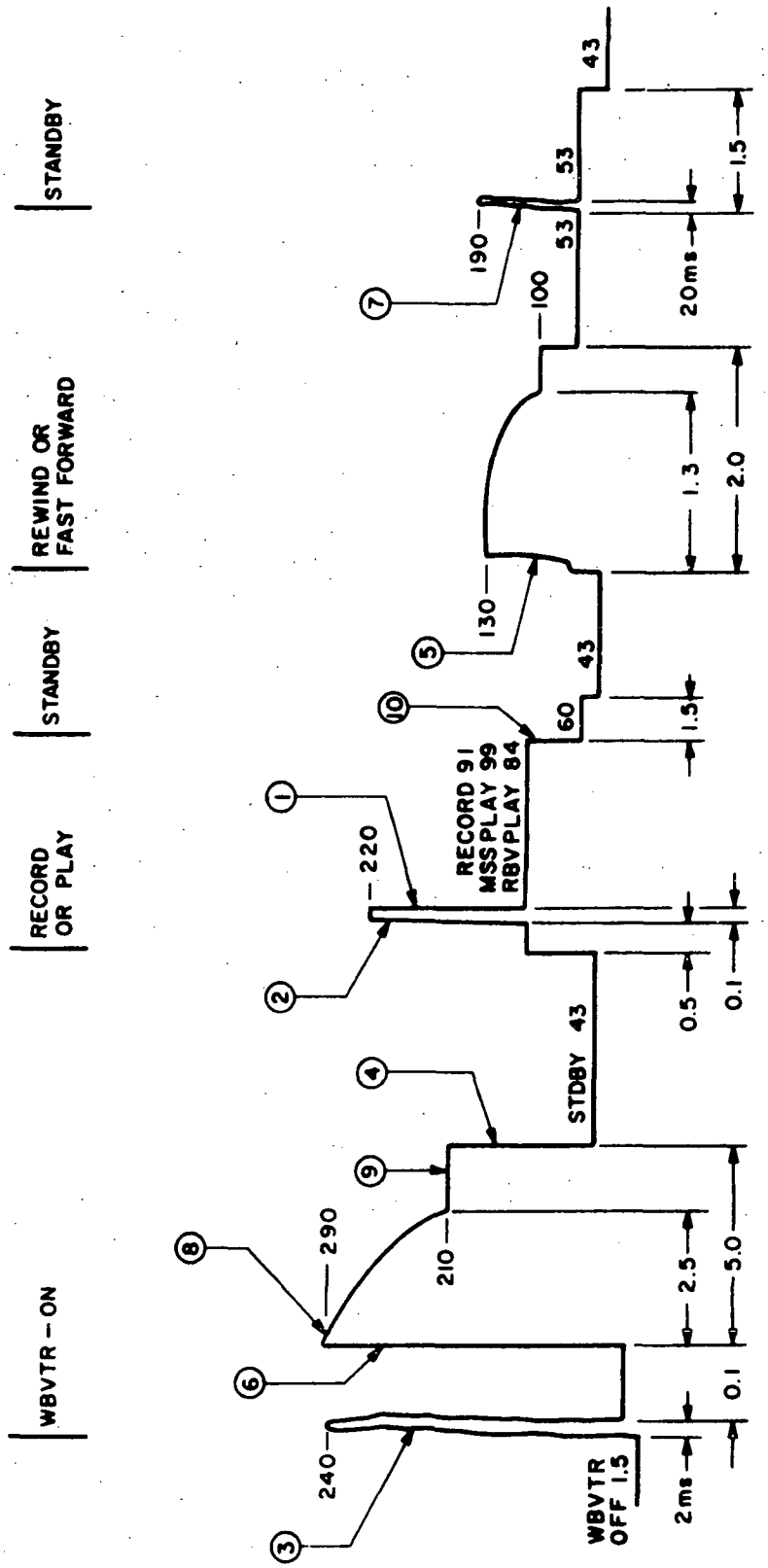


Figure 4-180. Primary Power Profile (Engineering Model)

APPENDIX A

COMPONENT SPECIFICATIONS

TABLE A-1. VIDEO IN COMPONENT SPECIFICATIONS (Sheet 1 of 4)

DESIGN VALUES							RECOMENDED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits			TYPE	Nominal Value	Parameter	Limits		
				0°C	25°C	60°C				0°C	25°C	60°C
V1	+5.6		Max	6	5.9	6			Max			
			Min	5.2	5.3	5.2			Min			
V2	+8.		Max	8.6	8.5	8.6			Max			
			Min	7.4	7.5	7.4			Min			
V3	-8		Max						Max			
			Min						Min			
V4	+22		Max	23.2	25	23.2			Max			
			Min	20.8	21	20.8			Min			
V5	-22		Max						Max			
			Min						Min			
V6	1N3155	+8.4 ±.065mV	Max	8.87	8.8	8.87		±4mV	Max			
			Min	7.93	8.0	7.93			Min			
V7	1N3155	-8.4	Max						Max			
			Min						Min			
V8	1N751A	+5.1 [illegible]	Max		5.35			±6%	Max			
			Min		4.85				Min			
V9	1N753A	-6.2 [illegible]	Max		6.51	[illegible]		±6%	Max			±37mV
			Min		5.89				Min			
V10	1N825	+6.2 ±13mV	Max		6.22			±4mV	Max			
			Min		6.0				Min			
V11	1N941B	+11.7 ±.239	Max		12.28			±4mV	Max			
			Min		11.12				Min			
V12	1N943B	-11.7 [illegible]	Max		12.28			±4mV	Max			
			Min		11.12				Min			
V13	1N751A	-5.1	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
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			Max						Max			
			Min						Min			

TABLE A-1. VIDEO IN COMPONENT SPECIFICATIONS (Sheet 2 of 4)

Video In Network

	DESIGN VALUES						RECOMENDED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C
Q1, Q3	2N2907A		Max						Max			
			Min						Min			
	V_{BE}	.7	Max						Max			
			Min						Min			
	ΘV_B	1.7 mV/°C	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
Q2, Q4	2N2222A		Max						Max			
			Min						Min			
	V_{BE}	.7	Max						Max			
			Min						Min			
	ΘV_B	1.7 mV/°C	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
U3	MC3160L		Max						Max			
			Min						Min			
	V_{OL}	I_o = 1mA .1V	Max		.15	+10mV	aging	+20mV	Max			
			Min		.05				Min			
	V_{OH}	$I_o \approx 0$ 3.2	Max		—			−20mV	Max			
			Min		—	−10mV			Min			
			Max						Max			
			Min						Min			
U8	μA702A		Max						Max			
			Min						Min			
	$e_{os}(T)$	10μV/°C	Max			350μV			Max			
			Min						Min			
	$i_{os}(T)$	5nA/°C	Max			175nA			Max			
			Min						Min			
	e_{os} aging	.65 mV/10,000hrs	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-1. VIDEO IN COMPONENT SPECIFICATIONS (Sheet 3 of 4)

Part No.	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C	RECOMENDED VALUES TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C
VR2	[illegible]		Max						Max			
			Min						Min			
	BV	9.4	Max	8.97	9.3	8.87			Max			
			Min	[illegible]	[illegible]	[illegible]			Min			
	I_Z	10mA	Max		[illegible]				Max			
			Min						Min			
	-		Max						Max			
			Min						Min			
	•		Max						Max			
			Min						Min			
VR3	1N751A		Max						Max			
			Min						Min			
20mA	BV	5.1	Max	[illegible]	[illegible]	[illegible]			Max			
			Min	[illegible]	[illegible]	[illegible]			Min			
	I_Z		Max						Max			
			Min						Min			
7.5mA	TC [illegible]	[illegible]	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
Vref	1N758A		Max						Max			
			Min						Min			
20mA	BV	6.2	Max	[illegible]	[illegible]	[illegible]			Max			
			Min	[illegible]	[illegible]	[illegible]			Min			
	I_Z		Max						Max			
			Min						Min			
7.5mA	TC [illegible]	[illegible]	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
VR5	1N821		Max						Max			
			Min						Min			
	BV	6.2	Max	[illegible]	[illegible]	[illegible]			Max			
			Min	[illegible]	[illegible]	[illegible]			Min			
	I_Z	7.5mA	Max		[illegible]				Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
VR6	1N5111		Max						Max			
			Min						Min			
	BV	11.7	Max	12.52	12.28	12.52			Max			
			Min	10.88	11.12	10.88			Min			
	I_Z	7.5mA	Max						Max			
			Min						Min			
	TC @ 7.5 mA	±.2239V	Max						Max			
			Min						Min			

TABLE A-1. VIDEO IN COMPONENT SPECIFICATIONS (Sheet 4 of 4)

DESIGN VALUES							RECOMENDED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C
1)	RNR	121	Max						Max			
			Min						Min			
R2,R14	RLR	390	Max	[illegible]	425	[illegible]	RWR 2W	280	Max			
			Min	378	375	352			Min			
R3,[illegible] R15,[illegible]	RCR	1K	Max						Max			
			Min						Min			
R5,R36	RNR	4C9	Max						Max			
			Min						Min			
R6,R27	RNR	196	Max						Max			
			Min						Min			
R7,R13	RNR	6.81K	Max						Max			
			Min						Min			
R8,R9 R22,R23,R33	RCR	10	Max						Max			
			Min						Min			
R11,R13 R17,R18	RNR	402	Max	410	409.6	408.3			Max			
			Min	396	394	395			Min			
R12	RNR	3.01K	Max						Max			
			Min						Min			
R15	RNR	E25	Max						Max			
			Min						Min			
R16	RNR	976	Max						Max			
			Min						Min			
R18	RNR	332	Max		334		RNR 2W	422	Max			
			Min		[illegible]				Min			
R19	RNR	1.1K	Max	[illegible]	[illegible]	[illegible]	RNR 1/2W	909	Max			
			Min	[illegible]	1080	1074			Min			
R21,R37	RNR	383	Max						Max			
			Min						Min			
R24	RNR	10K	Max						Max			
			Min						Min			
R26	RCR	1.5K	Max						Max			
			Min						Min			
R28,R39	RNR	681	Max		684				Max			
			Min		680				Min			
R29,R30 R32,	RCR	47	Max						Max			
			Min						Min			
R35	RCR	750	Max						Max			
			Min						Min			
R39	RNR	909	Max	[illegible]	926	928			Max			
			Min	[illegible]	892	890			Min			
R40	RNR	2.21K	Max						Max			
			Min						Min			
R42	RNR	2C1	Max						Max			
			Min						Min			
R[illegible]	RWR	392	Max		399		RLR 1W	560	Max			
			Min		385				Min			
R46,R47 R48,R49	RJ24CX	200	Max				use K in spec		Max			
			Min						Min			
R51	RNR	2.32K										

TABLE A-2. MODULATOR COMPONENT SPECIFICATIONS (Sheet 1 of 4)

	DESIGN VALUES						RECOMENDED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	Limits 60°C	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	Limits 60°C
Q1	2N2907A		Max						Max			
			Min						Min			
	V_{BE}	.7	Max	.77	.71	.65			Max			
			Min	.55	.49	.43			Min			
			Max						Max			
			Min						Min			
	I_{CBO}		Max						Max			
			Min						Min			
	h_{FE}		Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
Q2	2N2222A		Max						Max			
			Min						Min			
	V_{BE}	.7	Max	.77	.71	.65			Max			
			Min	.55	.49	.43			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
Q3, Q4	2N918		Max						Max			
			Min						Min			
	V_{BE}	1.04 +.8 -.56	Max	1.1	1.04	.99			Max			
			Min	.62	.56	.5			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
Q5	2N2857		Max						Max			
			Min						Min			
	V_{BE}	1.04 +.8 -.56	Max	1.16	1.1	1.04			Max			
			Min	.62	.56	.54			Min			
			Max						Max			
			Min						Min			
CR1 CR2	1N5472C		Max						Max			
			Min						Min			
	C_T	47pf	Max	47.4	47.0	49.6			Max			
			Min	45.6	46.1	46.7			Min			
	TC_c	.64% /°C	Max			+1.4%			Max			
			Min	-1%					Min			

TABLE A-2. MODULATOR COMPONENT SPECIFICATIONS (Sheet 2 of 4)

	DESIGN VALUES						RECOMENDED VALUES					
Unit Ref.	TYPE	Nominal Value	Parameter	Limits			TYPE	Nominal Value	Parameter	Limits		
				0°C	25°C	60°C				0°C	25°C	60°C
VR1 VR2	IN827		Max				IN829		Max			
			Min						Min			
	ΔV	6.2V ±2mV	Max	6.512	6.503	6.512		6.2 ± 5mV	Max			
			Min	5.888	5.897	5.888			Min			
	I_Z	7.5mA	Max					aging ±3mV	Max			
			Min						Min			
	b_Z		Max						Max			
			Min						Min			
	I_{Leak}		Max						Max			
			Min						Min			
VR3 VR4	IN941B		Max					aging ±4mV	Max			
			Min						Min			
V_6, V_7	BV	11.7	Max	12.52	12.28	12.52			Max			
			Min	10.88	11.12	10.88			Min			
	I_Z	7.5mA	Max						Max			
			Min						Min			
	b_Z	30Ω @ 7.5mA	Max						Max			
			Min						Min			
	$TC_{@7.5mA}$	±.239V	Max						Max			
			Min						Min			
VR5 VR6	IN944B		Max						Max			
			Min						Min			
V_8, V_9	BV		Max	12.30	12.28	12.30		aging ±3mV	Max			
			Min	11.096	11.12	11.096			Min			
	I_Z	7.5mA	Max						Max			
			Min						Min			
	b_Z	30Ω @ 7.5mA	Max						Max			
			Min						Min			
	$TC_{@7.5mA}$	±.024V	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
VR7 VR8	IN821		Max						Max			
			Min						Min			
V10, V11		6.2	Max		6.5	10.5mA		aging ± 4mV	Max			
			Min		5.6				Min			
			Max						Max			
			Min						Min			
V1	+5.6		Max	6	5.9	6			Max			
			Min	5.2	5.3	5.2			Min			
V2	+8		Max	8.6	8.5	8.6			Max			
			Min	7.4	7.5	7.4			Min			
V3	-8		Max						Max			
			Min						Min			
V4	+22		Max	23.2	23	23.2			Max			
			Min	20.8	21	20.8			Min			
V5	-22		Max						Max			
			Min						Min			

TABLE A-2. MODULATOR COMPONENT SPECIFICATIONS (Sheet 3 of 4)

	DESIGN VALUES						RECOMENDED VALUES					
				Limits						Limits		
Part No.	TYPE	Nominal Value	Parameter	0°C	25°C	60°C	TYPE	Nominal Value	Parameter	0°C	25°C	60°C
R1, R2	RNR-FP	750	Max	765	764	765			Max			
			Min	735	736	735			Min			
R3, R5	"	402	Max	411	410	411	RNR (a 2nd col. [illegible])	750 ¼W	Max			
			Min	393	394	393			Min			
R4, R6	"	110	Max	112.5	112	112.5			Max			
			Min	107.5	108	107.5			Min			
R7, R8 R14, R15	RCR-7P	3.3K	Max	3345	3295	3318	RNR	3.16K	Max	3221	3217	3222
			Min	2609	2805	2715			Min	3099	3103	3098
R9, R16	"	330	Max	395	380	393	RNR	316	Max	322	322	322
			Min	269	290	271			Min	310	310	310
R10, R18 R33	"	470	Max	550	540	550	RLR-6P	470	Max	500	485	501
			Min	390	400	390			Min	440	442	439
R11, R19	"	430	Max	504	494	504	RLR-6P	430	Max	457	455	458
			Min	358	365	358			Min	403	405	403
R12, R20	"	100	Max	117	115	117	RLR	100 ¼W	Max	107	106	107
			Min	83	85	83			Min	93.5	94	93
R13, R17	"	220	Max	255	250	255	[illegible]		Max			
			Min	185	190	185			Min			
R21, R22	RLR-7P	330	Max	362	360	362	RLR	430 ¼W	Max			
			Min	298	[illegible]	298			Min			
R23, R24	RWR-7P	205	Max	210	209	209	RWR	178 ¼W	Max			
			Min	201	201	201			Min			
R25, R23	RCR-7P	43	Max	50.6	49.6	50.6			Max			
			Min	35.9	36.4	35.4			Min			
R26	"	270	Max	316	310	316			Max			
			Min	225	230	225			Min			
R27, R34 R35, R37	"	82	Max	96	94	96	RLR-7P	51	Max		55.6	55.7
			Min	68.5	70	68.5			Min		46.4	46.2
R29, R32	"	75	Max	88	86	88			Max			
			Min	62	64	62			Min			
R30	"	2.2K	Max	2510	2500	2550			Max			
			Min	1950	1950	1850			Min			
R31, R36 R38, R39	"	1K	Max	1185	1150	1180			Max			
			Min	825	850	829			Min			
R40	RJ24 Connector	25K	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
R10, R13	RLR-7P	430	Max		463	471	RLR	430 ¼W	Max			
			Min		392	389			Min			
R12, R14	RLR-7P	100	Max		109	110			Max			
			Min		91	90			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-2. MODULATOR COMPONENT SPECIFICATIONS (Sheet 4 of 4)

DESIGN VALUES								RECOMENDED VALUES					
Part No.	Type	Nom. Value		Parameter	Limits 0°C	25°C	60°C	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	65°C
R R8 R14, R15			Initial	Max				RNR	3.16 K	Max			
				Min						Min			
			aging	Max						Max	3193	3189	3194
				Min						Min	3127	3131	3126
R9, R16			Initial	Max				RNR	316	Max			
				Min						Min			
			aging	Max						Max	319	319	319
				Min						Min	313	313	313
[illegible]			Initial	Max				RLR-6P	470	Max			
				Min						Min			
			aging	Max						Max	491	489	492
				Min						Min	449	451	448
R10, R18 R11, R19			Initial	Max				RLR-6P	430	Max			
				Min						Min			
			aging	Max						Max	449	447	450
				Min						Min	411	413	410
R12, R20			Initial	Max				RLR-[illegible]	100	Max			
				Min						Min			
			aging	Max						Max	104.5	104	105
				Min						Min	95.5	96	95
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			

TABLE A-3. RECORD CURRENT ADJUST COMPONENT SPECIFICATIONS (Sheet 1 of 2)

	DESIGN VALUES						RECOMENDED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	Limits 60°C	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	Limits 60°C
R6	RCR	8.2K	Max	9630	9730	9630			Max			
			Min	6820	6970	6820			Min			
R7	RCR	4.7K	Max	5500	5400	5500			Max			
			Min	3920	4000	3920			Min			
R8		100 (105 / 95)	Max	118.5	115	118			Max			
			Min	82.5	85	82.5			Min			
R9	RNR	825 (833 / 817)	Max	842	841	842.5			Max			
			Min	808	808	807.5			Min			
R10		383 (387.8 / 378.2)	Max	39.4	390	390.6			Max			
			Min	375.6	376	375.4			Min			
R11		178 (180 / 176)	Max	181.6	181.4	181.7			Max			
			Min	174.4	174.6	174.4			Min			
R12	RCR	22	Max	25.9	25.3	25.8			Max			
			Min	19.4	18.7	18.4			Min			
R13		100	Max	118.5	115	118			Max			
			Min	82.5	85	82.5			Min			
R14		560	Max	663	644	661			Max			
			Min	462	476	464			Min			
R15		10	Max	11.8	11.5	11.8			Max			
			Min	8.3	8.5	8.2			Min			
R16	RNR	68.1	Max	69.6	69.5	69.6			Max			
			Min	66.6	66.7	66.6			Min			
R17	RCR	75	Max	88	86	88			Max			
			Min	63	64	62			Min			
R18		700	Max	890	860	890			Max			
			Min	630	690	630			Min			
R19	RNR	100	Max	102.2	102	102.2			Max			
			Min	97.9	98	97.9			Min			
R20	RCR	3.9K	Max	4615	4495	4605			Max			
			Min	3315	3315	3280			Min			
R21		6.8K	Max	7950	7800	7950			Max			
			Min	5680	5800	5660			Min			
R22		120K	Max	140.7	139K	140.7			Max			
			Min	99.3	102K	99.3			Min			
R23		12K	Max	14070	13,800	14070			Max			
			Min	9990	10,200	9990			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
C8-C13	CSR-KP	1 Mf	Max	12.6	13 Mf	13.6			Max			
			Min	6.8	7 Mf	6.7			Min			
			Max						Max			
			Min						Min			

TABLE A-3. RECORD CURRENT ADJUST COMPONENT SPECIFICATIONS (Sheet 2 of 2)

DESIGN VALUES							RECOMENDED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	Limits 60°C	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	Limits 60°C
Q1	2N2218A		Max						Max			
			Min						Min			
	V_{BE}	.84 .7 .56	Max		.92				Max			
			Min		.56				Min			
	V_{CE}	.2 .2V .1	Max		.33				Max			
			Min		.1				Min			
	I_{CBO}		Max		20nA	20uA			Max			
			Min						Min			
	h_{FE}		Max		375	400			Max			
			Min	54	70	90			Min			
Q2	2N2222A		Max						Max			
			Min						Min			
	V_{BE}	.84 .7 .56	Max		.92				Max			
			Min		.56				Min			
	V_{CE}	.2 .1 .05	Max		.22				Max			
			Min		.05				Min			
	I_{CBO}		Max		20nA	200nA			Max			
			Min						Min			
	h_{FE}		Max						Max			
			Min	54	75	90			Min			
K1	412-18	18	Max		24				Max			
			Min		13.5				Min			
	R_L	880 ±10%	Max	890	968	1100			Max			
			Min	720	792	920			Min			
	Operate Time		Max		2ms				Max			
			Min						Min			
	Drop-out Voltage		Max		10V				Max			
			Min						Min			
	Release Time		Max		1.5ms				Max			
			Min						Min			
K2-K4	422-19	18 V	Max		24				Max			
			Min		15.5				Min			
	R_L	1130 ±10%	Max	1140	1243	1400			Max			
			Min	930	1017	1140			Min			
	Operate Time		Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
V_1		+8 V	Max	8.6	8.5	8.6			Max			
			Min	7.4	7.5	7.4			Min			
V_2		-8V	Max						Max			
			Min						Min			
V_3		+22	Max	23.2	23	23.2			Max			
			Min	20.8	21	20.8			Min			
V_4		-22	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-4. FM EQUALIZER COMPONENT SPECIFICATIONS (Sheet 1 of 2)

DESIGN VALUES							RECOMENDED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C
(to Stereo)	RCR	100	Max	117	115	118		10	Max	11.7	11.5	11.8
			Min	83	85	83			Min	8.3	8.5	8.3
Record Amp	RCR	43K	Max	5040	4942	5042			Max			
			Min	3596	3659	3587			Min			
Record Amp	RCR	1K	Max	1170	1150	1180			Max			
			Min	830	850	820			Min			
R23	RCR	22	Max	25.5	25	25.5			Max			
			Min	18.5	19	18.5			Min			
R24	RCR	47	Max	55	54	55			Max			
			Min	39	40	39			Min			
R25	RCR	1K	Max	1170	1150	1180			Max			
			Min	830	850	820			Min			
R26	RCR	390	Max	456	443	456			Max			
			Min	324	332	324			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
C9	CMOS	120pf	Max	126.3	126	126.4			Max			
			Min	113.9	114	113.9			Min			
C11	CMOS	33pf	Max	34.7	34.6	34.7			Max			
			Min	31.4	31.4	31.4			Min			
C15	CMOS	62pf	Max	65.2	65	65.2			Max			
			Min	59	59	59			Min			
C17	CMOS	18 pf	Max	19.1	19	19.1			Max			
			Min	17	17	17			Min			
C13	CKROG	0.1 uf	Max	.126	.12	.126			Max			
			Min	.066	.07	.066			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-4. FM EQUALIZER COMPONENT SPECIFICATIONS (Sheet 2 of 2)

DESIGN VALUES							RECOMENDED VALUE 0671					
part No.	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C
N 1545	V = ±5V		Max						Max			
			Min						Min			
I_{CO}	V_G = 0	Calculated 1.22MA	Max		2.5				Max			
			Min						Min			
	V_G = 5		Max		2uA				Max			
			Min						Min			
	Bandwidth	75 MHz	Max						Max			
			Min		37.5				Min			
	Input Com. Mode	± 2.5 V	Max						Max			
			Min						Min			
	V_{out}	2.5 V_{PP}	Max						Max			
			Min		1.5				Min			
	A_V	18 db	Max		20				Max			
			Min		16				Min			
TTL SN5400	V_{CC}=5.5		Max						Max			
			Min	-55	to	125°C			Min			
	I_{in} (-)		Max		1.6...				Max			
			Min						Min			
	V_{in} = +4V I_{in} (1)		Max		4 uA				Max			
			Min						Min			
	V_{out} (0)	.22 V	Max		.4 V				Max			
			Min						Min			
	V_{out} (1)	3.3 V	Max						Max			
			Min		2.4 V				Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
2N2369A			Max						Max			
			Min						Min			
DC bias	V_{CC} = 5 I_C = 5 mA		Max						Max			
			Min						Min			
	Gain-BW f_t	600MHz	Max						Max			
			Min		450				Min			
	P_T	mW	Max	310	310	230			Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-5. BUFFER LOGIC CIRCUIT COMPONENT SPECIFICATIONS

IPC	Input	Max Input UL	Max Leak Curr. μA	Max Load UL	Turn-ON Delay NS			Turn-off Delay NS			Setup Time NS			Hold Time NS		
					Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
MC3100		1	50	10		6	10		6	10						
MC3101		1	50	10		9	15		9	12						
MC3110		1	50	10		6	10		6	10						
MC3115		1	50	10		8	12		8	12						
MC3120		1.3	50	20		9	15		9	15						
MC3151	J, K	.75	50	10			12			12		8			5	
	S, R	2	140													
	C	2.3	145			14	18		12	18						
MC3160	D	.75	50	10								1-10 0-5	15		5	5
	S	1.15	100													
	R	1.7	140													
	C	1.5	100		10	15	25	10	17	25						
MC3162	J, K	.75	50	10								8	15			
	S	1.75	150													
	C	1.75	150			12	18		12	18						
RF320	C					9	12		6	8						

TABLE A-6. LIMITER DEMODULATOR COMPONENT SPECIFICATIONS (Sheet 1 of 6)

	DESIGN VALUES						RECOMENDED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C
L1, L9	Var W_{80}-VL	.56 μH	Max						Max			
			Min						Min			
	R_L	.05 Ω	Max						Max			
			Min						Min			
L2, L5		.68 μH	Max						Max			
			Min						Min			
	R_L	.06	Max						Max			
			Min						Min			
L3, L6		1.2 μH	Max						Max			
			Min						Min			
	R_L	.09	Max						Max			
			Min						Min			
L7,		8.2 μH	Max						Max			
			Min						Min			
	R_L	.4 Ω	Max						Max			
			Min						Min			
L8, L10		4.7 μH	Max						Max			
			Min						Min			
	R_L	.25	Max						Max			
			Min						Min			
L11,		3.3 μH	Max						Max			
			Min						Min			
	R_L	.165	Max						Max			
			Min						Min			
L12		1.8 μH	Max						Max			
			Min						Min			
	R_L	.11	Max						Max			
			Min						Min			
L4, L16		2.2 μH	Max						Max			
			Min						Min			
	R_L	.12	Max						Max			
			Min						Min			
L15		6.8 μH	Max						Max			
			Min						Min			
	R_L	.33	Max						Max			
			Min						Min			
L9	CT 81500302	39 μH	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
L13	CT 81500402	24 μH	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-6. LIMITER DEMODULATOR COMPONENT SPECIFICATIONS (Sheet 2 of 6)

DESIGN VALUES							RECOMMENDED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits -0°C	Limits [illegible]	Limits [illegible]	TYPE	Nominal Value	Parameter	Limits [illegible]	Limits [illegible]	Limits [illegible]
Q1-Q10	2N3866		Max						Max			
			Min						Min			
	V_{BE}		Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
	h_{FE}	18 d.b @ 100 mHz	Max						Max			
			Min						Min			
	h_{FE}	25 mA pulsed	Max		200				Max			
			Min	30	35	40			Min			
Q1-Q9	2N918		Max						Max			
			Min						Min			
	V_{BE}	.75	Max	1.03	.95	.87			Max			
			Min	.50	.6	.52			Min			
	h_{FE}		Max		200				Max			
			Min		30				Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
	f_T	600 MHz	Max						Max			
			Min						Min			
Q12	2N2219A		Max						Max			
			Min						Min			
I_L=35	V_{BE}	.75	Max		.9		2N709		Max		1.00	
			Min		.6				Min		.57	
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
Q11 Q13	2N5054A		Max						Max			
			Min						Min			
I_L=35	V_{BE}	.75	Max		.9				Max		1.00	
			Min		.6				Min		.54	
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-6. LIMITER DEMODULATOR COMPONENT SPECIFICATIONS (Sheet 3 of 6)

	DESIGN VALUES						RECOMENDED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits			TYPE	Nominal Value	Parameter	Limits		
				0°C	25°C	43°C				0°C	25°C	43°C
R2, R81, R90, R91	RCR	1K	Max	1185	1150	1180			Max			
			Min	825	850	823			Min			
R3, R9,	RCR	75	Max	80	[illegible]	-			Max			
			Min	62	64	62			Min			
R4, R5, R7 R8, R10	RNR	1K initial	Max	1011.3	1010	1011.7	aging	1K ± .5	Max	1010.2	1009	1010.7
			Min	988.7	990	988.3			Min	989.8	991	989.3
R6, R10	RJ24	100	Max						Max			
			Min						Min			
R11, R13 R21, R23, R26, R34, R37, R38	RCR	470	Max	550	540	550			Max			
			Min	390	400	390			Min			
R11, R12 R20, R35 R36, R38	RLR	470	Max	515	512	516			Max			
			Min	426	428	425			Min			
R14, R17 R39	RCR	240	Max	291	276	291			Max			
			Min	200	204	200			Min			
R15, R16 R17, R29, R30 R39, R40, R93	RCR	22	Max	25.5	25	25.5			Max			
			Min	18.5	19	18.5			Min			
R12, R19 R31, R32, 43	RCR	1200	Max	1420	1393	1415			Max			
			Min	990	1020	993			Min			
R20, R22 R45, 54, 64	RCR	100	Max	117	115	117			Max			
			Min	93	85	93			Min			
R46	RCR	750	Max						Max			
			Min						Min			
R 7, R57	RCR	3900	Max	4625	[illegible]	[illegible]			Max			
			Min		3315				Min			
R48, R58	RNR	237	Max				aging	±.2%	Max		23221	
			Min						Min		23249	
R49, R59	RCR	3600	Max		4145				Max			
			Min		3350				Min			
R50, R60	RNR	90.9	Max	92.7	92.6	92.7	aging	±.2%	Max		91.8	
			Min	89.1	89.2	89.1			Min		90	
R51, R61	RCR	680	Max						Max			
			Min						Min			
R52	RWR	344	Max						Max			
			Min						Min			
R53, R63	RCR	22	Max						Max			
			Min						Min			
R55, 65	RCR	270	Max						Max			
			Min						Min			
R56, R66	RCR	27	Max						Max			
			Min						Min			
R62	RWR	374	Max						Max			
			Min						Min			
R67, R68 R69	RNR	51.1	Max						Max			
			Min						Min			
R71	RNR	909	Max						Max			
			Min						Min			
R72, R86	RLR	200	Max	219	218	219.4			Max			
			Min	181.1	182	180.8			Min			

TABLE A-6. LIMITER DEMODULATOR COMPONENT SPECIFICATIONS (Sheet 4 of 6)

	DESIGN VALUES						RECOMMENDED VALUES					
				Limits								
Part No.	TYPE	Nominal Value	Parameter	0°C	[illegible]	[illegible]	TYPE	Nominal Value	Parameter	0°C	[illegible]	[illegible]
1, R76 Rod, R94, R97	RCR	10	Max	11.7	11.5	11.7			Max			
			Min	83	85	83			Min			
R74	RNR	8250	Max	8420	8410	8420		aging ±.5%	Max		8325	
			Min	8090	8090	8080			Min		8175	
R75	sensistor	2700 initial	Nom	2150	2700	3450	aging	2700 ±1%	Max		2727	
									Min		2673	
R77, R78	RNR	196	Max						Max			
			Min						Min			
R80	RNR	100	Max						Max			
			Min						Min			
R82	RNR	221	Max						Max			
			Min						Min			
R83	RNR	2K	NOM	2002.4	2K	20024			Max		2018	
			Min	1997.6		1996.6	aging	±.9%	Min		1982	
R84	RJ24	5K	Nom		5K	5043			Max		5350	
			Min			4957	aging	±7%	Min		4650	
R85	RNR	5110	NOM	5116	5110	5119			Max		5176	
			Min			5101	aging	±.9%	Min		5064	
R87	RNR	1620	Max						Max			
			Min						Min			
R89	RNR	10K	Nom	10012.5	10K	10012.5			Max		10,090	
			Min	9987		9932	aging	±.9%	Min		9910	
R92	RNR	75	Max						Max			
			Min						Min			
R95	RCR	120	Max						Max			
			Min						Min			
R96	RCR	1300	Max						Max			
			Min						Min			
R98	RCR	2K	Max						Max			
			Min						Min			
R84	RJ24	1K	Nom		1K	1009			Max		1070	
			Min			991	aging	±7%	Min		930	
R85	RNR	6810	Nom		6810	6822			Max		6970	
			Min			6798	aging	±.9%	Min		6750	
			Max						Max			
			Min						Min			
V_2		+8	Max	8.6	8.5	8.6			Max			
			Min	7.4	7.5	7.4			Min			
V_3		-8	Max						Max			
			Min						Min			
V_4		+22	Max	23.4	23	23.2			Max			
			Min	20.8	21	20.9			Min			
V_5		-22	Max		23				Max			
			Min		21				Min			
V_6		+21.6	Max		12.68				Max			
			Min		10.52				Min			
V_7		-6.2	Max		6.9				Max			
			Min		5.9				Min			

TABLE A-6. LIMITER DEMODULATION COMPONENT SPECIFICATIONS (Sheet 5 of 6)

DESIGN VALUES							RECOMMENDED VALUES					
Part No.	Type	Nominal Value	Parameter	Limits 0°C	Limits [illegible]	Limits [illegible]	Type	Nominal Value	Parameter	Limits 0°C	Limits [illegible]	Limits [illegible]
R1	IN943B		Max						Max			
			Min						Min			
	BV	11.7	Max		12.20	12.327	No aging		Max			
			Min	12.253	11.12				Min			
	Iz	7.5mA	Max						Max			
			Min						Min			
	bz	.30~	Max						Max			
			Min						Min			
	TC	±.047V	Max						Max			
			Min									
VR2	IN825		Max									
			Min									
	BV	6.2	Max	6.52	6.50	6.52	No aging		Max			
			Min	5.92	5.90	5.88			Min			
	Iz	7.5mA	Max						Max			
			Min						Min			
	bz	15~	Max						Max			
			Min						Min			
	TC	±.219V	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
CR1 - CR3	IN4148		Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
CR4 CR5	IN645		Max						Max			
			Min						Min			
	V_F	.7	Max		1.00		aging		Max		1.05	
			Min		.40				Min		.35	
	$V_F(T)$	-1mV/°C	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
	aging	+50mV	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-6. LIMITER DEMODULATOR COMPONENT SPECIFICATIONS (Sheet 6 of 6)

	DESIGN VALUES						RECOMMENDED VALUES					
Part No.	TYPE	Nominal Value	Power Rating	Limits			TYPE	Nominal Value	Power Rating	Limits		
-U3	CA3028B		Max						Max			
			Min						Min			
	V_{OS}		Max	5MV	5MV	6MV			Max			
			Min						Min			
	I_{OS}		Max		5MA				Max			
			Min						Min			
	Input Bias		Max		40MA				Max			
			Min						Min			
	I_7	.75MA	Max		1				Max			
			Min		.5							
	I_6		Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
	Power Dissip.		Max		42MW				Max			
			Min		29MW				Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
U4, U5	SN527026 (712)		Max						Max			
			Min						Min			
	V_{OOS}	2MV	Max		5				Max			
			Min						Min			
	$V_{OOS}(T)$	10MV/°C	Max		3				Max			
			Min						Min			
	I_{OOS}	0.7MA	Max			3			Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
	Power Dissip	90 MW	Max		120				Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-7. RBV OUTPUT COMPONENT SPECIFICATIONS (Sheet 1 of 5)

DESIGN VALUES							RECOMENDED VALUES					
Part No.	TYPE	Nominal Value	Para-meter	Limits			TYPE	Nominal Value	Para-meter	Limits		
				0°C	25°C	60°C				0°C	25°C	60°C
(5	1N5165		Max						Max			
			Min						Min			
	V_f	.39	Max		.41				Max			
			Min		.37				Min			
		-1.14%/°C	Max			-38mV			Max			
			Min						Min			
VR1	1N4372A	3.15 3.00 2.95	Max		3.15		aging	± 6%	Max		±19mV	
			Min		2.85				Min			
		-2.7mV, -.075%/°C	Max			- 80mV			Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
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			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-7. RBV OUTPUT COMPONENT SPECIFICATIONS (Sheet 2 of 5)

DESIGN VALUES							RECOMENDED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits			TYPE	Nominal Value	Parameter	Limits		
				0°C	25°C	60°C				0°C	25°C	60°C
R42	RCR	10K	Max	11.7	11.5	11.7		8.2K	Max		9.43	
			Min	8.3	8.5	8.3			Min		7.	
R43		33K	Max	39.45	37.95	39.18		22K	Max		25.09	
			Min	26.89	28.05	27.45			Min		19.	
R44		1K	Max	1170	1150	1170			Max			
			Min	830	850	830			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
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			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-7. RBV OUTPUT COMPONENT SPECIFICATIONS (Sheet 3 of 5)

	DESIGN VALUES						AS-MEASURED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	Limits 65°C	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	Limits 65°C
Q7, Q8, Q9	2N2907A		Max						Max			
			Min						Min			
	V_{BE} I=5mA	.65 +.25 −.35	Max	.9	.85				Max			
			Min	.65	.6				Min			
	V_{CE}	.1 +.050 −.05	Max	.16	.165	.175			Max			
			Min	.05	.06	.07			Min			
	h_{FE} I_C=1A		Max						Max			
			Min	60	75				Min			
IN645	-		Max						Max			
			Min						Min			
	V_F	.7	Max		1.00		2 pins		Max		1.05	
			Min		.90				Min		.85	
	V_F @ I	-1 mV/°C	Max						Max			
			Min						Min			
IN751A	TC ±.030 @ 7.5mA	5.35 5.1 ±.85	Max	5.68	5.65	5.68			Max			
			Min	4.52	4.55	4.52			Min			
			Max						Max			
			Min						Min			
Q10	2N2219A		Max						Max			
			Min						Min			
	V_{BE}	.87 -1.4mV/°C	Max		1.25	1.1	2 pins	±10%	Max		1.15	
			Min		.70	.65			Min		.77	
			Max						Max			
			Min						Min			
Q11	2N2905A		Max						Max			
			Min						Min			
	V_{BE}	.87 -1.4mV/°C	Max		1.05	1.1	2 pins	±10%	Max		1.15	
			Min		.70	.65			Min		.77	
			Max						Max			
			Min						Min			
VR2	IN9433	11.7 ±.047	Max		12.29				Max			
			Min		11.13				Min			
			Max						Max			
			Min						Min			
VR3	IN825	6.2 ±.01%	Max		6.5	6.512			Max			
			Min		5.9	6.291			Min			
			Max						Max			
			Min						Min			
VR4	"		Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
V6	+11.7		Max		12.58				Max			
			Min		10.77				Min			
V7	-6.2		Max		6.8				Max			
			Min		5.55				Min			
V8	IN751A	-5.1	Max		6.00				Max			
			Min		4.55				Min			

TABLE A-7. RBV OUTPUT COMPONENT SPECIFICATIONS (Sheet 4 of 5)

DESIGN VALUES								RECOMENDED VALUES					
					Limits						Limits		
Part No.	Type	Nom. Value		Parameter	0°C	25°C	60°C	Type	Nominal Value	Parameter	0°C	25°C	60°C
R22	RNR	1500	Initial	Max		1515				Max			
				Min		1485				Min			
			aging	Max	1529	1527	1529.4			Max			
				Min	1471	1473	1471			Min			
R30	RNR	7500	Initial	Max		7575				Max			
				Min		7425				Min			
			aging	Max	7644	7635	7648			Max			
				Min	7356	7365	7352			Min			
R1	RJ24	10K	Temp ~~Initial~~	Max		10 K	10,018			Max			
				Min			9992			Min			
			aging	Max		10 K	10700			Max			
				Min			9300			Min			
R2	RNR	12.1K	Temp ~~Initial~~	Max		12.1	12,121			Max			
				Min			12097			Min			
			aging	Max		12.1	12,200			Max			
				Min			12007			Min			
R26	RNR	2150	Temp ~~Initial~~	Max		2150				Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			

TABLE A-7. RBV OUTPUT COMPONENT SPECIFICATIONS (Sheet 5 of 5)

DESIGN VALUES								RECOMENDED VALUES					
Part No.	Type	Nom. Value		Parameter	Limits			TYPE	Nominal Value	Parameter	Limits		
					0°C	25°C	60°C				0°C	25°C	60°C
R3	RNR	2150	Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
R8	RNR	6190	~~Initial~~ Temp	Max		6190	6200			Max			
				Min			6180			Min			
			aging	Max		6245				Max			
				Min		6135				Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			
			Initial	Max						Max			
				Min						Min			
			aging	Max						Max			
				Min						Min			

TABLE A-8. REFERENCE GENERATOR COMPONENT SPECIFICATIONS (Sheet 1 of 7)

DESIGN VALUES							RECOMENDED VALUES					
Part #	TYPE	Nominal Value	Para-meter	Limits			TYPE	Nominal Value	Para-meter	Limits		
				0°C	25°C	60°C				0°C	25°C	60°C
R1	RLR	10K	Max		11510	11990			Max			
			Min						Min			
R2		1K	Max						Max			
			Min						Min			
R3			Max					Temp system	Max			
			Min			3			Min			
R4		7K	Max						Max			
			Min	58	62	62			Min			
R5		6.2K	Max						Max			
			Min						Min			
R6			Max						Max			
			Min						Min			
R7			Max						Max			
			Min						Min			
R8	RLR	6	Max						Max			
			Min						Min			
R9, R21, R22		3.3K	Max						Max			
			Min						Min			
R10		1150	Max	1171	1150	1171			Max			
			Min		1094				Min			
R11, R20, 21, R22		100	Max						Max			
			Min	83	85				Min			
R13			Max					Temp system	Max			
			Min						Min			
R15			Max						Max			
			Min						Min			
R16		1K	Max						Max			
			Min						Min			
R23			Max						Max			
			Min						Min			
R27			Max						Max			
			Min						Min			
R28			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
R			Max						Max			
			Min						Min			
			Max						Max			
			Min			40			Min			

TABLE A-8. REFERENCE GENERATOR COMPONENT SPECIFICATIONS (Sheet 2 of 7)

	DESIGN VALUES						RECOMMENDED VALUES					
Part	TYPE	Nominal Value	Parameter	Limits			TYPE	Nominal Value	Parameter	Limits		
				0°C	35°C	65°C				0°C	35°C	65°C
C1	CMOS	18 pf	Max						Max			
			Min						Min			
C2	CTM	.015 mf	Max	.0150	.0135	.0120		Temp Comp	Max			
			Min	.0102	.0122	.0142			Min	.1		
C3	CKR	.01 mf	Max						Max			
			Min						Min			
C4	"	.01 mf	Max						Max			
			Min						Min			
C5	CTM	.0047 mf	Max	.0051	.0052	.0053			Max			
			Min						Min			
C6	CMOS		Max						Max			
			Min						Min			
C7	CTM		Max						Max			
			Min						Min			
C8	CKR	.1 mf	Max						Max			
			Min						Min			
C9	CKR	1,000 pf	Max						Max			
			Min						Min			
C10, C13 C15, C16	CTM	.01 mf	Max	.0150	.0111	.0112		Temp Comp	Max			.01
		.047 mf	Min						Min			
C11		.15 .1 .047	Max	.151	.111	.111			Max			
			Min						Min			
C12		.025 .01 .0047	Max	.041	.0249	.023			Max			
			Min	.021		.021			Min			
C14		.45 .33 .31	Max	.36	.303	.303			Max			
			Min	.297	.3	.3			Min			
C17-C25	CKR	.001 pf	Max						Max			
			Min						Min			
C26	CLR-G	50 pf	Max						Max			
			Min						Min			
C27-C28	CTM-K	.1	Max						Max			
			Min						Min			
L1		Var. 50 mh	Max						Max			
			Min						Min			
	R_{L1}		Max						Max			
			Min						Min			
L2		Var. 500 mh	Max						Max			
			Min						Min			
	R_{L2}	5.3	Max						Max			
			Min						Min			
L3		Var. 3.3 mh	Max						Max			
			Min						Min			
	R_{L3}	42.	Max						Max			
			Min						Min			
L4		10 mh	Max						Max			
			Min						Min			
	R_{L4}		Max			1.5			Max			
			Min						Min			

TABLE A-8. REFERENCE GENERATOR COMPONENT SPECIFICATIONS (Sheet 3 of 7)

	DESIGN VALUES						RECOMMENDED VALUES					
				Limits						Limits		
	TYPE	Nominal Value	Parameter	0°C	25°C	60°C	TYPE	Nominal Value	Parameter	0°C	25°C	60°C
2N2222A			Max						Max			
			Min						Min			
V_{BE}	I_C = 5mA	.6	Max	.84	.78	.70			Max			
			Min	.48	.42	.34			Min			
V_{CE}		.1	Max	.15	.16	.17			Max			
			Min	.03	.04	.05			Min			
I_{CEO}		20nA	Max		20nA	.32μA			Max			
			Min						Min			
			Max						Max			
			Min						Min			
P_D			Max						Max			
			Min						Min			
h_{FE}			Max						Max			
			Min						Min			
Q2 2N2222A			Max						Max			
			Min						Min			
V_{BE}	I_C = 1.5	.6	Max	.87	.78	.7			Max			
			Min	.48	.42	.34			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
h_{FE}			Min	40	56				Min			
			Max			500mW			Max			
P_D			Min						Min			
f_T		100mhz	Max						Max			
			Min						Min			
VR1 IN753A			Max						Max			
		6.2 ±5%	Min						Min			
		2.51	Max	6.57	6.59	6.59			Max			
		5.89	Min	5.82	5.83	5.83			Min			
	TCV	±.05%/°C	Max	-11%		+13%			Max			
			Min						Min			
	I_{Leak}		Max			10μA			Max			
			Min						Min			
	P_L		Max			225mW			Max			
			Min						Min			
VR2 IN963B		12.60	Max	12.6	12.75	12.88			Max			
		12 11.40	Min	11.29	11.30	11.32			Min			
	TCRV	.07%/°C	Max	-.19%		+2.2%			Max			
			Min						Min			
	I_R	10.5mA	Max		32mA				Max			
			Min						Min			
	P_D		Max		500mW	@ 25°C			Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-8. REFERENCE GENERATOR COMPONENT SPECIFICATIONS (Sheet 4 of 7)

	DESIGN VALUES						RECOMMENDED VALUES					
Part #	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	70°C	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	70°C
U1	710		Max						Max			
			Min						Min			
	Offset Voltage		Max	3.0	7.5	10			Max			
			Min						Min			
	Offset Current		Max	7.5	10	15			Max			
			Min						Min			
	$+V_{out}$	3.2	Max		4.0				Max			
			Min		2.8				Min			
	$-V_{out}$	-.5	Max		-0.3				Max			
			Min		-1.5				Min			
			Max						Max			
			Min						Min			
U2, U4	5493		Max						Max			
			Min						Min			
	Same as 5490		Max						Max			
			Min						Min			
	I_{cc}	P Sum 32 mA	Max			45			Max			
			Min						Min			
	I_{in}	V_{in} = 5.5	Max		-3.2				Max			
			Min						Min			
		V_{in} = 5.5	Max		1.2				Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
U3, U5 U11, U15	J-K FF 5473		Max						Max			
			Min						Min			
	Same as 5473		Max						Max			
			Min						Min			
	I_{cc}	9 mA	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-8. REFERENCE GENERATOR COMPONENT SPECIFICATIONS (Sheet 5 of 7)

	DESIGN VALUES						RECOMENDED VALUES					
Part #	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	Limits 60°C	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	Limits 60°C
U6, U7 U17	5-100 (Comp)		Max						Max			
			Min						Min			
	V_{in}		Max		.8	1.0			Max			
			Min		2	2.2			Min			
	V_{out} "1"	3.7	Max						Max			
			Min	2.9					Min			
	V_{out} "0"	0.4	Max			.3			Max			
			Min						Min			
	I_{in} "0"	1 load	Max			1.6mA			Max			
			Min						Min			
	I_{in} "1"	1 load	Max			4.0mA			Max			
			Min						Min			
	I_{out} "0"	16 loads	Max						Max			
	I_{cc}	0 load	Min						Min			
U8-U11 U13, U15, U16	9601		Max						Max			
			Min						Min			
	V_{out} High	3.4	Max						Max			
			Min	2.4	2.4	2.4			Min			
	Low	.2	Max	.25	.4	.5			Max			
			Min						Min			
	V_{in} High		Max	1.8	1.5	1.6			Max			
			Min						Min			
	Low		Max						Max			
			Min	.95	.93	.90			Min			
	Input V_{in} 0	-1mA	Max	-1.6		-1.6			Max			
			Min						Min			
	I_{Leak} V_{in}=4.0		Max			50μA			Max			
			Min						Min			
	I_{PS}	supply load	Max	25mA		25mA			Max			
			Min						Min			
	I_{Load}		Max						Max			
			Min						Min			
U14	5-710 (Comp)		Max						Max			
			Min						Min			
	Same as 5-100		Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-8. REFERENCE GENERATOR COMPONENT SPECIFICATIONS (Sheet 6 of 7)

	DESIGN VALUES						RECOMENDED VALUES					
Ref.	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	Limits 60°C	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	Limits 60°C
T_1	[illegible]		Max						Max			
			Min						Min			
	[illegible]	[illegible]	Max						Max			
			Min						Min			
	[illegible]	[illegible]	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
	$R_{[illegible]}$	[illegible]	Max						Max			
			Min						Min			
	[illegible]	[illegible]	Max						Max			
			Min						Min			
	[illegible]	[illegible]	Max						Max			
			Min						Min			
		[illegible]	Max						Max			
			Min						Min			
	[illegible]		Max						Max			
			Min						Min			
R_{92}	10 K		Max	11050	11500	[illegible]			Max			
			Min	[illegible]	[illegible]	[illegible]			Min			
R_{93}	33K		Max	[illegible]	[illegible]	[illegible]			Max			
			Min	[illegible]	[illegible]	[illegible]			Min			
R_{94}	1K		Max	[illegible]	[illegible]	[illegible]			Max			
			Min	[illegible]	[illegible]	[illegible]			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
V_4	+5.6		Max	[illegible]	[illegible]	[illegible]			Max			
			Min	[illegible]	[illegible]	[illegible]			Min			
V_3	+9		Max	9.6	[illegible]	[illegible]			Max			
			Min	[illegible]	[illegible]	[illegible]			Min			
V_2	−9		Max						Max			
			Min						Min			
V_1	+22		Max	[illegible]	[illegible]	[illegible]			Max			
			Min	[illegible]	[illegible]	[illegible]			Min			
V_5	−		Max	[illegible]	[illegible]	[illegible]			Max			
			Min	[illegible]	[illegible]	[illegible]			Min			
			Max						Max			
			Min						Min			

TABLE A-8. REFERENCE GENERATOR COMPONENT SPECIFICATIONS (Sheet 7 of 7)

	DESIGN VALUES						RECOMENDED VALUES					
Part #	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	Limits 60°C	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	Limits 60°C
L1	Bl 50 5-20-70	5 mH	Max						Max			
			Min						Min			
	R	295 Ω	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
L2		5 mH	Max						Max			
			Min						Min			
	R	6.5 Ω	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
L3		3.5 mH	Max						Max			
			Min						Min			
	R	42 Ω	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
L4	[illegible]	10 mH	Max						Max			
			Min						Min			
		Ω	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-9. TW PROCESSOR COMPONENT SPECIFICATIONS (Sheet 1 of 5)

DESIGN VALUES							RECOMMENDED VALUES					
Part	Type	Nominal Value	Parameter	Limits 0°C	25°C	70°C	Type	Nominal Value	Parameter	Limits 0°C	25°C	70°C
R20	RCR-32	10K	Max	11,840	11,800	11,800			Max			
			Min	9250	8,200	8,080			Min			
R20	RCR	10K	Max	11,840	11,800	11,800			Max			
			Min	9,320		8,230			Min			
R21	RLR	2K	Max	2190	2180	2174			Max			
			Min	1911	1820	1809			Min			
R22	RCR	68	Max	79.9	79.2	79.8			Max			
			Min	57	50	57			Min			
R23	RLR	6.2K	Max	6792	6758	6805			Max			
			Min	5613	5600	5603			Min			
R24	RCR	10K	Max	11,840	11,800	11,800			Max			
			Min	9250	8200	8280			Min			
R25	RLR	430	Max	471	462	470			Max			
			Min	396	391	398			Min			
R26	RCR	68	Max	79.8	79.2	79.8			Max			
			Min	57	50	57			Min			
R27	RLR	11K	Max	12,040	11,980	12,023			Max			
			Min	9,060	10,000	9,080			Min			
R28	RCR	4.7K	Max	5240	5200	5240			Max			
			Min	3950	3900	3			Min			
			Max	37,850	37,500	37,980			Max			
			Min	26,930	26,800	27,040			Min			
R30	RCR	10K 9250	Max	11,840	11,800	11,800			Max			
			Min	9250	8,200	8270			Min			
R31	RCR	1K	Max	1173	1150	1175			Max			
			Min	838	850	841			Min			
R32	RCR	1.2K 100K 35K	Max	113,650	115,000	115,200		82K	Max	99,500	94,300	97,300
			Min	81,600	85,000	82,250			Min	74,500	79,700	82,000
R33	RCR	100	Max	117	115	117			Max			
			Min	83	85	83			Min			
R34	RCR	3.9K	Max	3950	3795	3905			Max			
			Min	2770	2805	2725			Min			
R36	RCR	1.5K	Max	11,840	11,800	11,800			Max			
			Min	9250	8200	8280			Min			
R4	RCR	5.1K 10.5K	Max	5695	5600	6010			Max			
			Min	4210	4200	4230			Min			
R5	RCR	1K 1150	Max	1173	1150	1175			Max			
			Min	838	850	831			Min			
R12	RCR	11K 9250	Max	12,040	11,980	12,070			Max			
			Min	9,060	10,000	9,080			Min			
R13	RCR	1K	Max	1173	1150	1175			Max			
			Min	838	850	841			Min			
		470	Max	556	594	556			Max			
		470	Min	393	401	393			Min			
		71.9	Max	80.1	78.5	80.1			Max			
		66 64.6	Min	57	58.2	57			Min			
			Max						Max			
			Min						Min			

TABLE A-9. TW PROCESSOR COMPONENT SPECIFICATIONS (Sheet 2 of 5)

DESIGN VALUES							RECOMENDED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits			TYPE	Nominal Value	Parameter	Limits		
				0°C	25°C	60°C				0°C	25°C	60°C
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
C5	CSR KP	.062 .047uf .042	Max	.059	.061	.064			Max			
			Min	.03[illegible]	.033	[illegible]			Min			
C6	[illegible] KP	.0105 .01uf .0095	Max	.0109	.011	.0112			Max			
			Min	[illegible]	[illegible]	.0092			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
C10	CSR-[illegible]	.105 0.1uf	Max	.126	.13	.136			Max			
			Min	.066	.07	.073			Min			
C11	CSR-KP	4.7uf 4.2	Max	5.9	6.1	6.4			Max			
			Min	3.2	3.3	3.5			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
V2 +22V	±1 ±.2		Max	23.2	[illegible]	23.2			Max			
			Min	[illegible]	21	[illegible]			Min			
V1 -8V	±.5 ±.1		Max	-8.6	-8.5	-8.6			Max			
			Min	-7.4	-7.5	-7.4			Min			
V4 -22V			Max		23				Max			
			Min		[illegible]				Min			
V2 +5.6			Max	6	[illegible]	6			Max			
			Min	[illegible]	[illegible]	5.3			Min			
[illegible]		21.5	Max	22.7	[illegible]	[illegible]			Max			
			Min	[illegible]	[illegible]	[illegible]			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-9. TW PROCESSOR COMPONENT SPECIFICATIONS (Sheet 3 of 5)

DESIGN VALUES							RECOMENDED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C
2N2222A			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
V_{BE}	2mA	+62 -.6 V	Max	.64	.78	.7			Max			
			Min	.42	.42	.39			Min			
V_{CE}	2mA	-[illegible] .1V	Max	.15	.16	.17			Max			
			Min	.06	.07	.05			Min			
I_{CBO}		20nA	Max		2[illegible]	.32 mA			Max			
			Min						Min			
h_{FE}	I_C=150		Max		375				Max			
			Min	53	75	90			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
2N2907A			Max						Max			
			Min						Min			
V_{BE}		.6	Max	.83	.77	.65			Max			
			Min	.61	.55	.47			Min			
E		.1 .05-.15	Max	.1	.16	.23			Max			
			Min	.03	.05	.12			Min			
I_{CBO}			Max		20nA	.32 uA			Max			
			Min						Min			
h_{FE}	I_C=2mA		Max		5[illegible]				Max			
			Min	57	85	90			Min			
			Max						Max			
			Min						Min			
IN753A	initial	6.2	Max		6.51				Max			
			Min		5.89				Min			
IN753A	aging	6.2	Max	6.17	6.53	6.53			Max			
			Min	5.82	5.83	5.93			Min			
	TC@ I_Z=7.5mA	+.[illegible]% =	Max	-.11		+.15%			Max			
			Min						Min			
	I_{Z} [illegible]		Max			[illegible]			Max			
			Min						Min			
	TO= 25°C ΔV= [illegible]	mV (25°C)	Max						Max			
			Min						Min			
IN538		12.[illegible] 12 [illegible]	Max	12.6	12.7	12.75			Max			
			Min	11.25	11.3	11.35			Min			
	T[illegible]V	.0[illegible]	Max	-.1		+.165			Max			
			Min						Min			
	[illegible]	10.[illegible]mA	Max		3.[illegible]				Max			
			Min						Min			
	[illegible]		Max		3[illegible]	22[illegible]			Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-9. TW PROCESSOR COMPONENT SPECIFICATIONS (Sheet 4 of 5)

DESIGN VALUES							RECOMENDED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C
U1,U2	μA710		Max						Max			
			Min						Min			
	offset voltage		Max	3.2mV	3.1	3.3mV			Max			
			Min						Min			
	offset current		Max	4.9		2.5			Max			
			Min						Min			
	+Vout	3.2	Max		4.5				Max			
			Min						Min			
	-Vout	-.5	Max		0				Max			
			Min		-1.8				Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
U4	5403		Max						Max			
			Min						Min			
	Vin		Max		.5	1.1			Max			
			Min		2.	2.1			Min			
	Vout "1"	3.3	Max						Max			
			Min	2.4					Min			
	Vout "0"	.22	Max			.4			Max			
			Min						Min			
	Iin "0"		Max			1.6mA			Max			
			Min						Min			
	Iin "1"		Max			-40μA			Max			
			Min						Min			
U3,5,6	[illegible]		Max						Max			
			Min						Min			
Vout	High	3.4	Max						Max			
			Min	2.4	2.4	2.4			Min			
	Low	.2	Max	.45	.45	.45			Max			
			Min						Min			
VINPUT	High		Max	1.9	1.9	1.6			Max			
			Min						Min			
	Low		Max						Max			
			Min	.95	.85	.85			Min			
IInput	[illegible]	-1	Max	[illegible]		-1.6			Max			
			Min						Min			
ICC			Max			60mA			Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-9. TW PROCESSOR COMPONENT SPECIFICATIONS (Sheet 5 of 5)

DESIGN VALUES							RECOMENDED VALUES					
Part #	TYPE	Nominal Value	Parameter	Limits 0%	[illegible]	[illegible]	TYPE	Nominal Value	Parameter	Limits 0%	[illegible]	[illegible]
R38	RCR	470 Initial	Max		494				Max			
			Min		446				Min			
		Temp + aging	Max	556	544	556			Max			
			Min	323	401	393			Min			
R39	RCR	68 initial	Max		71.4				Max			
			Min		64.6				Min			
		temp + aging	Max	80.1	78.5	80.1			Max			
			Min	57	58.2	57			Min			
R10	RLR-JP	12,600 12,000 11,400	Max	13,140	13,083	13150			Max			
			Min	10,870	[illegible]	10840			Min			
R18	RLR-JP	15,750 15,000 14,250	Max	16,430	16,310	16,454			Max			
			Min	13550	13650	16230			Min			
R27	RLR-JP	11,550 11,000 10,450	Max	12710	12,650	12740			Max			
			Min	9305	9350	9235			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
RCT	Coil	30±10%	Max	30.2	33	36.7			Max			
			Min	24.7	27	20.5			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-10. DC/DC CONVERTER COMPONENT SPECIFICATIONS (Sheet 1 of 6)

	DESIGN VALUES						RECOMMENDED VALUES					
Part No.	Type	Nominal Value	Tempera-ture	Limits			Type	Nominal Value	Tempera-ture	Limits		
				0°C	25°C	70°C				0°C	25°C	70°C
R1, R11, R13, R15, R12	RCR	10K	Max	11,840	11,500	11,800			Max			
			Min	8350	8500	8350			Min			
R2	RCR	5600	Max	6630	6700	6610			Max			
			Min	4730	4750	4640			Min			
R3, R7	RLR-G	180	Max	190.6	190.4	191.7			Max			
			Min	168.6	169.6	168.6			Min			
R4	RCR	205	Max	231	230	234			Max			
			Min	166	173	166			Min			
R5, R6	RCR	12	Max	14	13.8	14	RLR-G	12	Max	12.78	12.72	12.8
			Min	10	10.2	10			Min	10.7	11.3	10.6
R8	RNR-F	100K	Max	102K	101K	102K			Max			
			Min	98K	99.1K	98K			Min			
R10, R18	PCR	4700	Max	5500	5400	5550		22K	Max	26,300	25,300	26,100
			Min	3920	4000	3920			Min	19,700	19,700	19,300
R12, R14 R16	RCR	1000	Max	1173	1150	1175		10K	Max	11,680	11,550	11,600
			Min	823	850	831			Min	8250	8300	8250
R19	RWR-F	150 3W	Max	152.9	152.7	152.8	RWR-F	182~ 2W	Max	186	185	186
			Min	147.2	147.3	147.2			Min	178	179	178
R20	RNR-F	1000	Max	1020	1015	1020			Max			
			Min	980	991	980			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
C1, C4 C5	CKR K	.1μf	Max	.126	.12	.126			Max			
			Min	.066	.07	.066			Min			
C2	CLG-KP	6.8μf	Max	6.6	7.8	8.4			Max			
			Min	4.6	5.4	5.8			Min			
C3, C6 C20	CLG-KP	5.4f	Max	5.9	5.7	6.1			Max			
			Min	3.7	4.3	4.6			Min			
C7, C8 C11, C13 C14, C16	CK06-K	1μf	Max	1.26	1.2	1.26			Max			
			Min	.67	.7	.67			Min			
C17, C19 C21, C24	CK06-K	1μf	Max						Max			
			Min						Min			
C18, C9 C22, C23	CLG-K	6.8μf	Max	59	59	77			Max			
			Min	41	45	52			Min			
C12, C15 C10	CLG-K	120μf	Max	117	133	148			Max			
			Min	92	96	103			Min			
C25	CKR-K	.00120f	Max	.00126	.00112	.00126			Max			
			Min	.00066	.00067	.00066			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-10. DC/DC CONVERTER COMPONENT SPECIFICATIONS (Sheet 2 of 6)

	DESIGN VALUES						RECOMMENDED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits			TYPE	Nominal Value	Parameter	Limits		
Q1, Q2	2N5038		Max						Max			
			Min						Min			
V_{CE}		100	Max						Max			
h_{FE}	I_C = 2A	75	Min	37	35	47			Min			
		23	Max						Max			
	I_C = 4A	65	Min	30	28	38			Min			
V_{CE}			Max						Max			
h_{FE}	I_C = 3.4	50	Min	25	25	42			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
V_{CE}	I_C = 12A	.175	Max	.91	.82	.59			Max			
		.53	Min	.37	.25	.27			Min			
	I_C = 9A	.35	Max	.56	.57	.59			Max			
		.12	Min	.17	.18	.12			Min			
	I_C = 3A	.45	Max	.49	.5	.52			Max			
		.3	Min	.14	.15	.16			Min			
			Max						Max			
			Min						Min			
V_{BE}	I_B = .1	1.14	Max	1.3	1.22	1.13			Max			
		.95	Min	.72	.70	.7			Min			
	.2	1.38	Max	1.56	1.5	1.47			Max			
		1.15	Min	.98	.92	.9			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
I_{CEO}			Max			10mA			Max			
			Min						Min			
Θ_{J-C}		1.25°C/W	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-10. DC/DC CONVERTER COMPONENT SPECIFICATIONS (Sheet 3 of 6)

DESIGN VALUES							RECOMMENDED VALUES					
Part No	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	50°C	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	50°C
CR1–	UTR		Max						Max			
CR10	G410V		Min						Min			
	I_F		Max			9A			Max			
			Min						Min			
	I_R		Max			15 mA			Max			
			Min						Min			
	I_{surge}		Max		150A				Max			
			Min						Min			
	V_F 50mA	.6	Max	.77	.72	.65			Max			
			Min	.53	.48	.41			Min			
	200	.7	Max	.89	.81	.79			Max			
			Min	.61	.56	[illegible]			Min			
	500	.77	Max	.97	.92	.85			Max			
			Min	.67	.62	.55			Min			
	600	.78	Max	.98	.93	.86			Max			
			Min	[illegible]	.63	.56			Min			
±10%	800	.8	Max	1.01	[illegible]	[illegible]			Max			
Typical			Min	.69	.64	.57			Min			
±10%	2.0A	.9	Max	1.13	1.08	1			Max			
20 mV			Min	.72	.72	.65			Min			
-.2+	3A	.92	Max	1.15	1.10	1.03			Max			
			Min	.79	.71	.67			Min			
(−20 mV	6A	1.05	Max	1.25	1.2	1.130			Max			
+50 mV)			Min	.85	.8	.730			Min			
			Max						Max			
			Min						Min			
	θ_{J-C}	2°/A	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-10. DC/DC CONVERTER COMPONENT SPECIFICATIONS (Sheet 4 of 6)

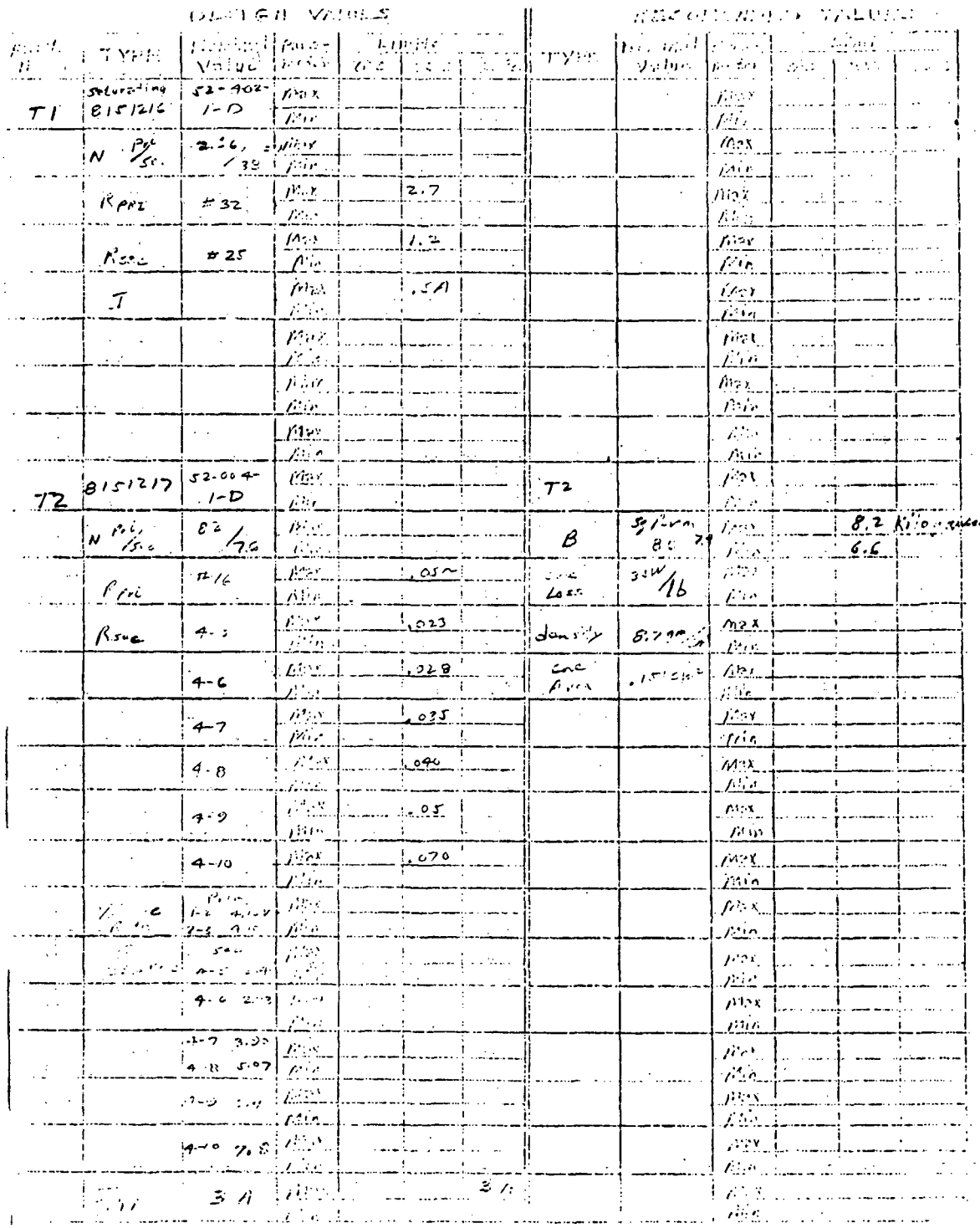


TABLE A-10. DC/DC CONVERTER COMPONENT SPECIFICATIONS (Sheet 5 of 6)

	DESIGN VALUES						RECOMMENDED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	Limits 60°C	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	Limits 60°C
L1	8151215		Max						Max			
			Min						Min			
	R_{L1}		Max	.0091	.0075	.0052			Max			
			Min						Min			
	L	@ 10KC	Max						Max			
			Min		40 u H				Min			
	I_c		Max		2.8A				Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
L2	8151224		Max						Max			
			Min						Min			
	L2 A, E		Max						Max			
			Min		110uH				Min			
	$R_{L2\ A,E}$	.0125 ±2%	Max						Max			
			Min						Min			
	I_A		Max	.5A					Max			
			Min						Min			
	I_C		Max	.25A					Max			
			Min						Min			
			Max						Max			
			Min						Min			
	L2 B,C,D		Max						Max			
			Min		300 u H				Min			
	$R_{L2\ B,C,D}$	.0276 ±2.0%	Max						Max			
			Min						Min			
	I_B		Max	.63A					Max			
			Min						Min			
	I_C		Max	2.5A					Max			
			Min						Min			
	I_D		Max	1.2A					Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-10. DC/DC CONVERTER COMPONENT SPECIFICATIONS (Sheet 6 of 6)

	DESIGN VALUES						RECOMMENDED VALUES					
Part N	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C
L6	8150597 MECHANICAL		Max						Max			
			Min						Min			
	L	3 mH	Max						Max			
			Min		3.1				Min			
	R_L	092Ω ±20%	Max	.101	.11	.124			Max			
			Min	.068	.074	.093			Min			
			Max						Max			
			Min						Min			
C10	CLC7 K7	6.8μF 25V	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
R7	RCR	10	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
	VTR - Encap. CF±		Max						Max			
			Min						Min			
	JL-J2B		Max						Max			
			Min						Min			
	Contact Vol. Drop	10 A	Max			.175V			Max			
			Min			.15V			Min			
	R_{cont}		Max			.0175			Max			
			Min			.015			Min			
	Operate Time		Max		10 ms				Max			
			Min						Min			
	J-J2A		Max						Max			
			Min						Min			
	Operate/ release time		Max		10ms				Max			
			Min						Min			
	Contact Vol. Drop	15A	Max			.175V			Max			
			Min			.15V			Min			
	R_{cont}		Max			.01Ω			Max			
			Min			.01Ω			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-11. VOLTAGE PROTECT COMPONENT SPECIFICATIONS (Sheet 1 of 4)

DESIGN VALUES							RECOMENDED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C
R1	RLR-J	1500	Max	1642	1635	1647	RWR	1470	Max	1493	1497	1493
			Min	1358	1365	1356			Min	1442	1442	1442
R2	RLR-J	27	Max	29.6	29.4	29.6	RNR	27	Max	27.6	27.5	27.6
			Min	[illegible]	24.5	24.5			Min	26.4	26.5	26.4
R3	RNR	680	Max	684	683	682	RNR	681	Max	695	694	695
			Min	606	607	606			Min	667	668	667
R4	RCR	1K	Max	1105	1155	1185	RNR	619	Max	632	631	632
			Min	825	855	825			Min	606	607	606
R5	RNR	3160	Max	3214	3223	3225			Max			
			Min	2906	3177	2978			Min			
R6 R12	RJ24-	500	Max	514	511	514	RJ24	506	Max	511	514.0	514
			Min	487	489	487			Min	493	486	493
R7	RNR	1215	Max	1225	1216	1225			Max			
			Min	1185	1187	1185			Min			
R8	RCR	10K	Max	11050	11050	11050			Max			
			Min	9050	9500	9050			Min			
R9	RNR	4320	Max	4305	4305	4305	RNR	2.15K	Max	2092	2101	2115
			Min	4215	4195	4195			Min	2106	2095	2095
R10	RCR	10K	Max	11050	11050	11050			Max			
			Min	9050	9500	9050			Min			
R11	RNR	3420	Max	3414	3414	3414			Max			
			Min	3336	3336	3336			Min			
R13	RNR	825	Max	841	841	842			Max			
			Min	809	809	809			Min			
R14	RCR	5100	Max	5250	5250	5265			Max			
			Min	4316	4305	4319			Min			
R15	RCR	56K	Max	58300	58300	58300	RCR	10K	Max	11050	11050	11050
			Min	46200	47300	46200			Min	9050	9500	9050
R16	RCR	3000	Max	3045	3045	3045	RNR	2.15K	Max	2184	2191	2195
			Min	2915	2915	2930			Min	2106	2095	2105
R17	RCR	10K	Max	11,300	11500	11,300			Max			
			Min	9050	9500	9050			Min			
R18	RCR	56K	Max	6400	6400	6400	RNR	2.37K	Max	2413	2413	2413
			Min	4600	4700	4600			Min	2322	2303	2321
R19, R20 R21, R22	RCR	3000	Max	3045	3045	3045			Max			
			Min	2915	2915	2930			Min			
			Max						Max			
			Min						Min			
C1	CL67-3P5	7.0 μf	Max	7.0	7.1	33.3	CL67-3P5	170 μf	Max	170	187	202
			Min	5.3	5.5	5.4			Min	131	141	155
C2, C3	CL67-1P6	150 μf	Max	147	172	196	Delete		Max			
			Min	110	130	140			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-11. VOLTAGE PROTECT COMPONENT SPECIFICATIONS (Sheet 2 of 4)

DESIGN VALUES							RECOMENDED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C	TYPE	Nominal Value	Parameter	Limits 0°C	25°C	60°C
Q1	2N3053		Max						Max			
			Min						Min			
I_C=40mA	V_{BE}	.55	Max	.76	.7	.62			Max			
			Min	.56	.5	.42			Min			
	V_{CE}	.2	Max	.25	.32	.42			Max			
			Min	.05	.11	.2			Min			
	I_{CBO}		Max	2mA	2mA	30mA			Max			
			Min						Min			
	h_{FE}	53	Max	62	60	70			Max			
			Min	32	35	44			Min			
I_C 150mA	h_{FE}	55	Max		60				Max			
			Min	34	43	53			Min			
	V_{BE}	.6	Max	.83	.77	.69			Max			
			Min	.61	.55	.47			Min			
			Max						Max			
			Min						Min			
Q2, Q3 Q4, Q5	2N2907A		Max						Max			
			Min						Min			
I_C=2mA	V_{BE}	.6	Max	.82	.77	.69			Max			
			Min	.51	.45	.37			Min			
	V_{CE}	.1	Max	.1	.15	.29			Max			
			Min	.02	.05	.12			Min			
	I_{CBO}		Max	-	20nA	.32μA			Max			
			Min						Min			
	h_{FE}		Max		375				Max			
			Min	57	51	26			Min			
	Q_N		Max						Max			
			Min	.922	.1.5	.905			Min			
	C_{ob}	4.5 pF	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
Q6	2N2907A		Max						Max			
			Min						Min			
I_C = 30mA	V_{BE}	.75	Max	1.05	1.0	.95			Max			
			Min	.72	.65	.58			Min			
	V_{CE}	.2	Max	.35	.34	.42			Max			
			Min	.05	.11	.2			Min			
	h_{FE}		Max		375				Max			
			Min	50	75	75			Min			
I_C = (Q4)	V_{BE}	.75	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

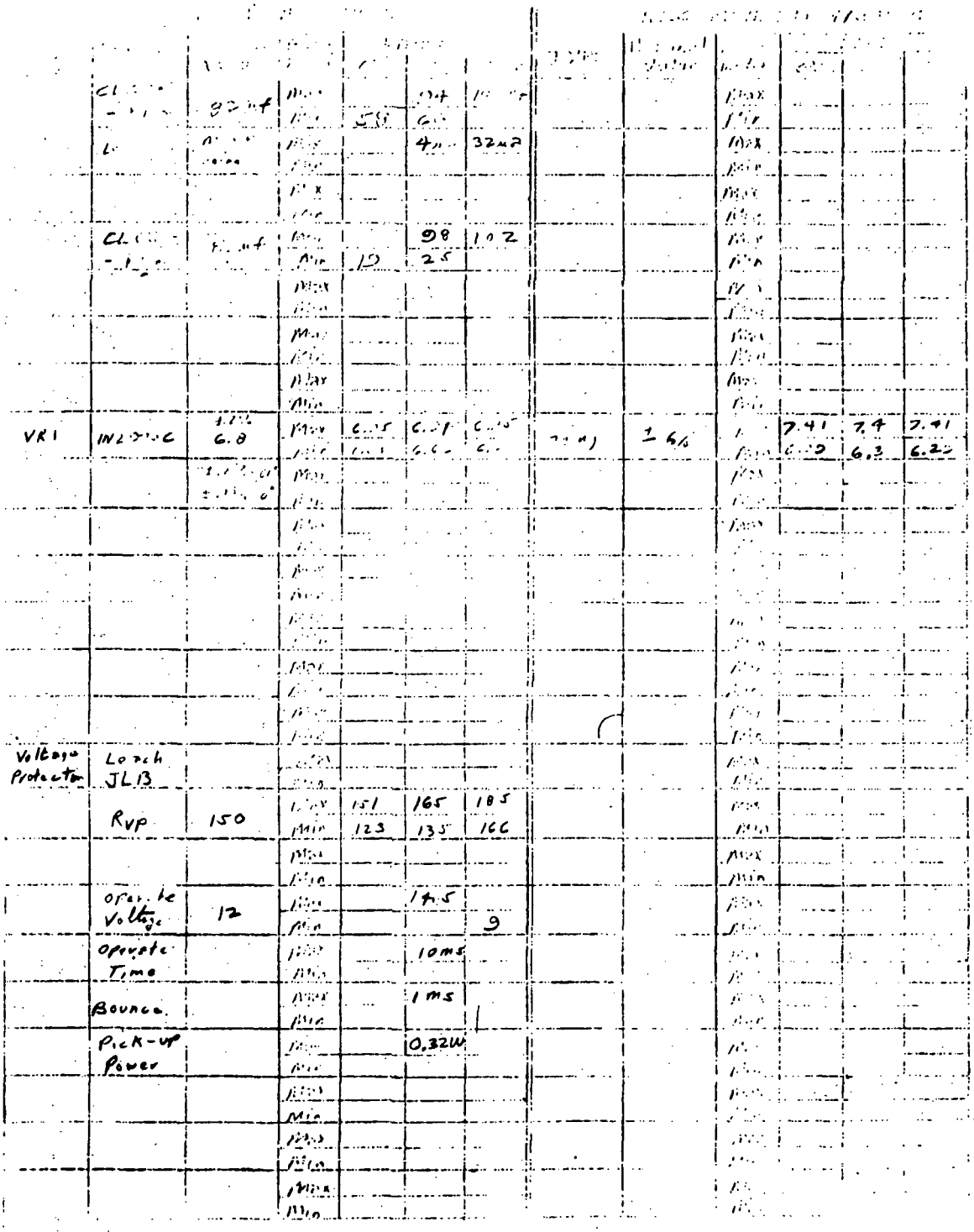
TABLE A-11. VOLTAGE PROTECT COMPONENT SPECIFICATIONS (Sheet 3 of 4)

DESIGN VALUES							RECOMENDED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	Limits 60°C	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	Limits 60°C
VR1	1N9638		Max				use 1N825	12.4	Max	12.98	13.00	13.02
			Min						Min	11.78	11.80	11.82
	BV	12V	Max	13.15	13.4	13.75	VR1 VR2		Max			
			Min	10.9	11.1	11.4			Min			
	I_Z	10.5 mA	Max		32				Max			
			Min						Min			
	b_{Z_1}	11.5Ω	Max						Max			
			Min						Min			
	I_{Leak}	9.1V	Max		10μA	50 mA			Max			
			Min						Min			
VR2	1N825		Max				VR3		Max			
			Min						Min			
	BV	6.2	Max	6.49	6.5	6.51			Max			
			Min	5.91	6.0	5.91			Min			
	I_Z	7.5mA	Max						Max			
			Min						Min			
	Z		Max		15Ω				Max			
			Min						Min			
	I_{Leak}	5V	Max		15μA	50μA			Max			
			Min						Min			
V	1N752A		Max				VR4	1N825	Max			
			Min						Min			
	BV	5.6	Max	6.16	6.2	6.25			Max			
			Min	5.04	5.0	5.04			Min			
	I_Z	20mA	Max						Max			
			Min						Min			
	b_Z	8Ω	Max						Max			
			Min						Min			
	I_{Leak}	2.5V	Max		10μA	50μA			Max			
			Min						Min			
CR1-CR5	1N645		Max						Max			
			Min						Min			
	I_R		Max		.5μA	30μA			Max			
			Min		0	0			Min			
1MA	V_F	.55	Max	.6	.6	.5			Max			
			Min	.56	.5	.45			Min			
100μA		.43	Max	.55	.5	.45			Max			
			Min	.43	.4	.35			Min			
250μA		.5	Max	.6	.55	.5			Max			
			Min	.5	.45	.4			Min			
.5MA		.5	Max	.6	.55	.5			Max			
			Min	.5	.45	.4			Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-11. VOLTAGE PROTECT COMPONENT SPECIFICATIONS (Sheet 4 of 4)

DESIGN VALUES							RECOMENDED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	Limits 60°C	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	Limits 60°C
K1	M5757/42 412-12W		Max						Max			
			Min						Min			
	RL1	390	Max	393	429	472			Max			
			Min	320	351	395			Min			
	L1		Max						Max			
			Min						Min			
	Drop-out Voltage		Max		6.5				Max			
			Min		.41				Min			
	Operate time		Max		2MS				Max			
			Min						Min			
	Release time		Max		1.5MS				Max			
			Min						Min			
	Bounce		Max		1.5MS				Max			
			Min						Min			
	Contact R		Max		.2Ω				Max			
			Min		.1Ω				Min			
	Coil Voltage	12	Max		16				Max			
			Min		9				Min			
K2	Latching 422-13		Max						Max			
			Min						Min			
	RL2	1130	Max	1134	1242	1350			Max			
			Min	920	1017	1150			Min			
	L2		Max						Max			
			Min						Min			
	Operate time		Max		1.5MS				Max			
			Min						Min			
	Release time		Max						Max			
			Min						Min			
	Bounce		Max		2MS				Max			
			Min						Min			
	Contact R		Max		.2Ω				Max			
			Min		.1Ω				Min			
	Coil Voltage	18	Max		24				Max			
			Min		13.5				Min			
Latch 12			Max						Max			
			Min						Min			
	RVP	150	Max	151	165	185			Max			
			Min	124	135	162			Min			
	LVP		Max						Max			
			Min						Min			
	Coil Voltage	12	Max		14.5				Max			
			Min		9				Min			
	Operate time		Max		10MS				Max			
			Min						Min			
	Bounce		Max		1MS				Max			
			Min						Min			
			Max						Max			
			Min						Min			

TABLE A-12. MOTOR AUXILIARY COMPONENT SPECIFICATIONS (Sheet 1 of 2)



		82 nf										
					4μ	32μ						
					98	102						
				10	25							
VR1	IN2970C	6.8								7.41	7.4	7.41
										6.22	6.3	6.22
Voltage Protector	Latch JL13											
	RVP	150	151	165	185							
			123	135	166							
	Operate Voltage	12		14.5								
					9							
	Operate Time			10ms								
	Bounce			1 ms								
	Pick-up Power			0.32W								

TABLE A-12. MOTOR AUXILIARY COMPONENT SPECIFICATIONS (Sheet 2 of 2)

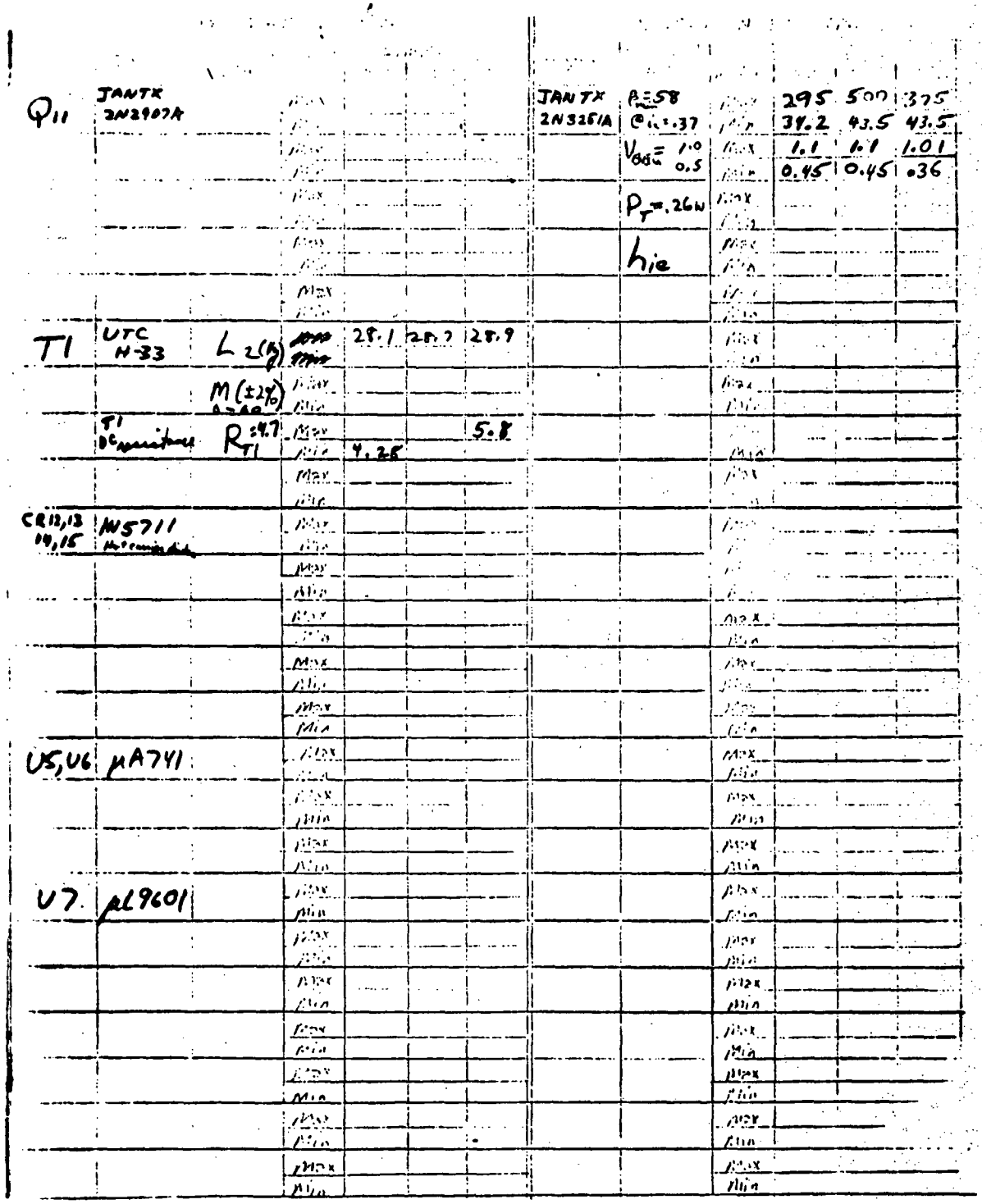
DESIGN VALUES							RECOMMENDED VALUES					
Part No.	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	Limits 100°C	TYPE	Nominal Value	Parameter	Limits 0°C	Limits 25°C	
Q1, Q3	2N		Max						Max			
			Min						Min			
T_r 2-5 μs	$V_{...}$		Max						Max			
			Min						Min			
	V_{i}	.7	Max		1				Max			
			Min		.64				Min			
	$T_{...}$		Max						Max			
			Min						Min			
	h_{FE}		Max		75				Max			
			Min	60	75				Min			
	Θ_{JA}	320°C/W	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
Q2	2N		Max						Max			
			Min						Min			
I_c = 20 mA	V_{CE} sat		Max						Max			
			Min						Min			
	$V_{...}$	.7	Max		.84				Max			
			Min		.56				Min			
	I_{CE}		Max						Max			
			Min						Min			
	h_{FE}		Max						Max			
			Min						Min			
	Θ_{JA}	320°C/W	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
Q4	2N		Max						Max			
			Min						Min			
I_c = 100 mA	V_{CE} sat		Max						Max			
			Min						Min			
	V_{BE} sat	.7	Max		1				Max			
			Min		.64				Min			
	I_{CES}		Max						Max			
			Min						Min			
	h_{FE}		Max						Max			
			Min		40				Min			
	Θ_{JA}	175°C/W	Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
			Max						Max			
			Min						Min			
V_5		-22	Max	23.2	23	23.2			Max			
			Min	20.8	21	20.9			Min			
			Max						Max			
			Min						Min			

TABLE A-13. DAMPER COMPONENT SPECIFICATIONS (Sheet 1 of 2)

* DRIFT ONLY

R36*	RNR55C FP	82.5		83.35	83.24	83.39						
				81.65	81.76	81.61						
R37	"	18.2K		18.34K	18.55K	18.55K						
				17.89K	17.95K	17.94K						
R38*	"	18.2K		18.38K	18.36K	18.35K						
				18.02K	18.04K	18.05K						
R39*	RJ24CK	R≅67.5K 2.50A Var.		72.23K	72.23K	72.21K						
				62.25K	62.27K	62.19K						
R40, R41, R42*	RNR55C FP	150		151.5	151.4	151.6						
				148.5	148.6	148.4						
R43*	"	1.82K		1.839K	1.830K	1.84K	RNR55C 3741 FP	3.74K		3.721K	3.730K	3.78K
				1.801K	1.806K	1.8K				3.702K	3706K	3.7K
R44, R49 R52	RLR07C JP	10K		10.95K	10.9K	10.97K						
				9.05K	9.1K	9.02K						
R45	RNR55C FP	27.4K		27.06K	27.92K	27.97K	RNR55C FP	36.5K		37.24K	37.19K	37.26K
				26.74K	26.55K	26.6K				35.76K	35.81K	35.74K
R46	"	100K		102.9K	101.9K	103.1K						
				97.97K	98.1K	97.9K						
R47	"	3.32K		3.387K	3.383K	3.392K	RNR55E FP	4.53K*		4.574K	4.571K	4.575K
				3.25K	3.257K	3.251K				4.486K	4.492K	4.49K
R48	RNR65C FP	681		694.8	693.9	695.1	RNR65C FP	649		662.1	661.3	662.5
				667.2	668.1	666.4				635.9	636.7	635.5
R50	RLR20C JP	470		514.5	512.3	515.5	RNR55C FP	3.92K		3.972K	3.965K	4K
				425.5	427.7	424.5				3.84K	3.846K	3.859K
R51	"	220		240.9	239.8	241.4	RNR70C FP	487		496.9	496.3	497.1
				199.1	209.2	198.6				477.1	477.7	476.9
R16*	RER65FR	0.1		.1023	.102	.1024						
				.0977	.098	.0976						
R53	(New)						RNR70C 604FP	604		61.62	61.55	61.65
										59.18	59.25	59.15
C15	CK06BX K	.056μ		.0756	.0672	.0754						
				.0252	.0392	.0352						
C16	CH09A3KA J	3.3		3.66 3.52	3.63 3.47	3.64 3.50						
				3.19 3.04	3.22 3.07	3.21 3.06						
C17, C18 C21	CK06BX K	1.0		1.35	1.2	1.35						
				0.45	0.7	0.45						
C19	CSR13F J	39.0		52.6 49.5	46.8 44.9	51.6 48.5	CSR13E 107K	100MF		130 120	135 120	135 120
				31.5 29.7	33.1 31.2	32.5 30.6				66.7 61.7	73 80	73 67.5
C20*	CH09A3KA J	0.1		.107	.105	.107	CQ09A1MC 104J3	0.1MF		.1025	.102	.1025
				.093	.095	.093				.0975	.098	.0975
C26	(new)						CK06BX 105K	1.0		1.35	1.2	1.35
										0.45	0.7	0.45
VR2	JANTX 1N965B	15V @7.5mA		15.6	15.9	16.33	JANTX 1N965B	15V±5% @1mA		15.3	15.3	15.75
				13.8	14.1	14.53				14.39	14.7	14.7
VR3	JANTX 1N752A	5.6V @5mA		5.98	5.94	6.0	JANTX 1N755A	7.5V @1mA		7.84	7.65	8.1
				5.22	5.26	5.2				6.94	7.35	7.2
VR4	(New)						JANTX 1N752A	5.6V @1mA		5.75	5.71	5.79
										5.45	5.49	5.44

TABLE A-13. DAMPER COMPONENT SPECIFICATIONS (Sheet 2 of 2)



APPENDIX B
SIMPLIFIED PLO TRANSFER FUNCTION

A simplified model of the PLO was used where applicable. It is shown in Figure B-1.

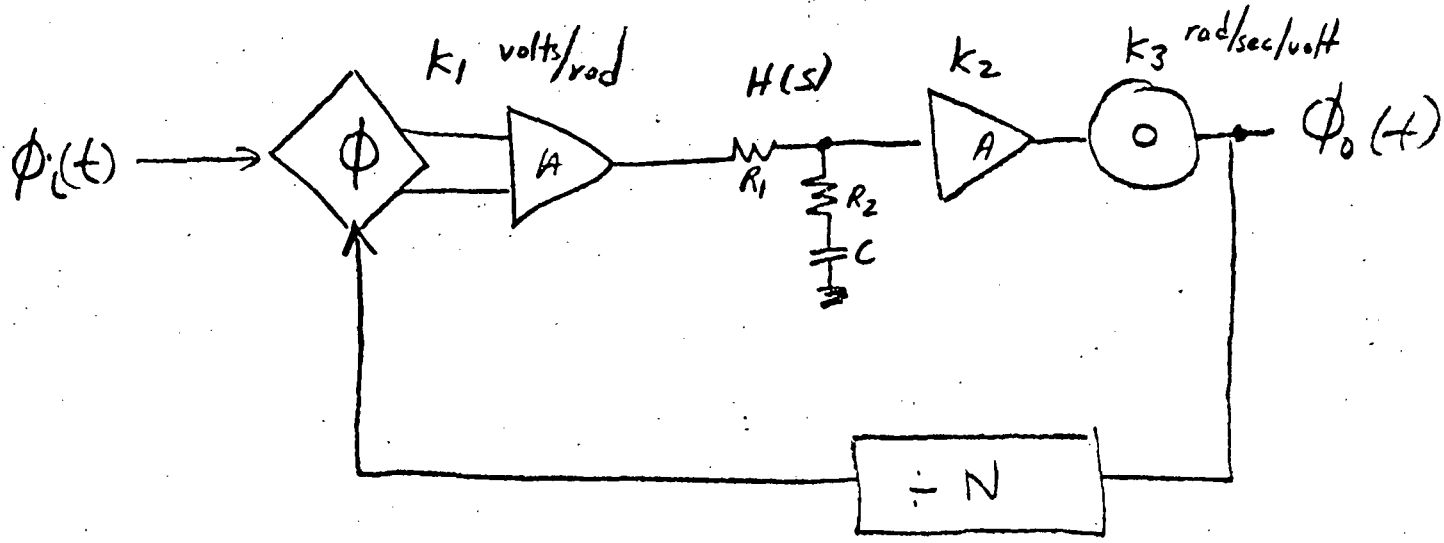


Figure B-1. Simplified Model of PLO

The transfer function resulting from this model is

$$\frac{\varphi_o(S)}{\varphi_i(S)} = \frac{NK_v}{S} \frac{H(S)}{1 + \frac{K_v}{S} H(S)}$$

where

$$H(S) = \frac{T_2 S + 1}{T_1 S + 1}$$

$$T_1 = (R_1 + R_2)\, C$$

$$T_2 = R_2 C$$

$$K = K_1 K_2 K_3$$

$$K_v = \frac{K}{N}$$

If we let

$$\omega n = \left(\frac{K}{T_1 N}\right)^{1/2}, \text{ the natural frequency}$$

$$\xi = \frac{T_2 \omega_n}{2}, \text{ the damping factor}$$

Then, assuming $\frac{K T_2}{N} > 1$, the applicable case, we find

$$\frac{\varphi_o(S)}{\varphi_i(S)} = 2\xi\omega_n N \frac{S + \frac{\omega_n}{2\xi}}{S^2 + 2\xi\omega_n S + \omega_n^2}$$

APPENDIX C

LINEARIZED PLO TRANSFER FUNCTION

A linearized model of the PLO is shown in Figure C-1.

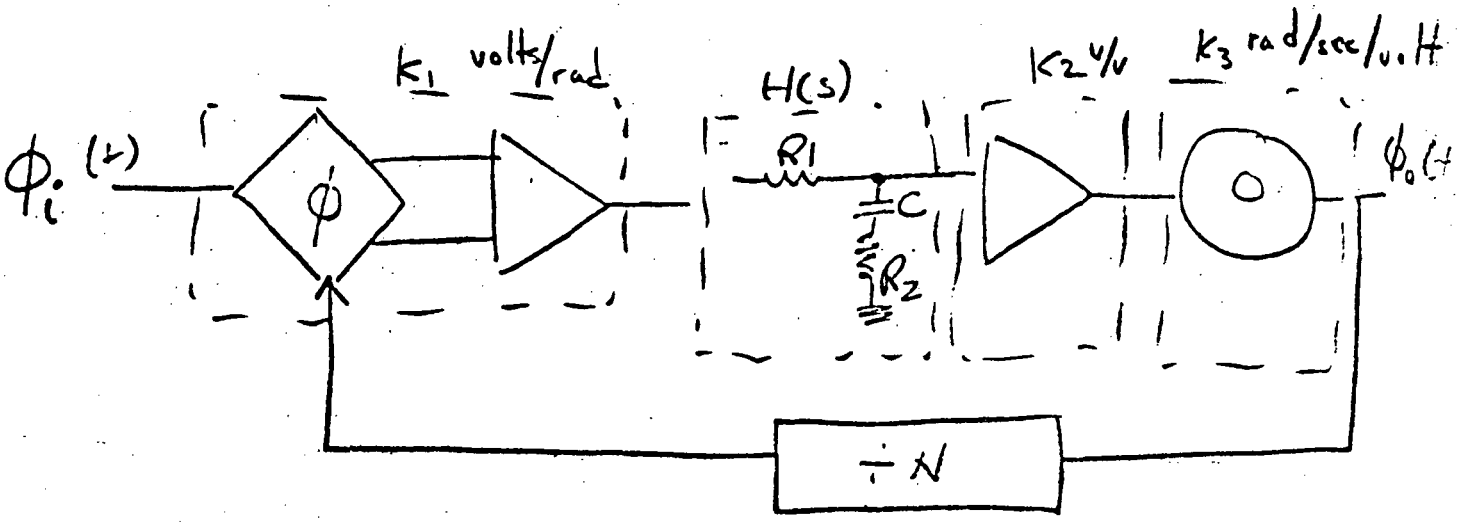


Figure C-1. Linearized Model of PLO

The transfer function resulting from this model is

$$\frac{\phi_o(S)}{\phi_i(S)} = \frac{NK_V}{S} \cdot \frac{\frac{T_2S+1}{T_1S+1}}{1 + \frac{K_V}{S}\frac{T_2S+1}{T_1S+1}}$$

where

$$H(S) = \frac{T_2S+1}{T_1S+1}$$

$$T_1 = (R_1+R_2)C$$

$$T_2 = R_2C$$

$$K = K_1K_2K_3$$

$$K_V = K/N$$

If we let

$$\omega n = \left(\frac{K_V}{T_1 N}\right)^{1/2}, \text{ the natural frequency}$$

$$\xi = \frac{T_2 \omega n}{2}, \text{ the damping factor}$$

Then, assuming $\frac{K_V T_2}{N} > 1$, the applicable case, we find

$$\frac{\phi_o(S)}{\phi_i(S)} = 2\xi\omega nN \quad \frac{S + \frac{\omega n}{2\epsilon}}{S^2 + 2\xi\omega nS + \omega n^2}$$

The response to a step change in phase is found by multiplying the response function by 1/S and performing the LaPlace Transform.

$$\phi_o(t) = \int^{-1} \left\{ \frac{N\Delta\phi}{S} \cdot \frac{2\xi\omega n\left(S + \frac{\omega n}{2\xi}\right)}{S^2 + 2\xi\omega nS + \omega n^2} \right\}$$

$$\phi_o(t) = N\Delta\phi \left\{ 1 - \frac{1}{2}\left(\frac{\xi + \sqrt{\epsilon^2 - 1}}{\sqrt{\epsilon^2 - 1}}\right) e^{-\left(\xi + \sqrt{\epsilon^2 - 1}\right)\omega nt} \right.$$

$$\left. + \frac{1}{2}\left(\frac{\xi - \sqrt{\epsilon^2 - 1}}{\sqrt{\epsilon^2 - 1}}\right) e^{-\left(\xi - \sqrt{\epsilon^2 - 1}\right)\omega nt} \right\}$$

APPENDIX D

DESIGN ASSUMPTIONS, GRAPHICAL ANALYSIS AND DETAILED WORK SHEETS FOR MOTOR DRIVE CIRCUITS WORST CASE ANALYSIS

TABLE D-1, DESIGN ASSUMPTIONS

ITEM	TOLERANCE		PARAMETER	DESIGN			MAX. STRESS		REMARKS
	INITIAL	DESIGN		MIN.	TYP.	MAX.	RATED	DESIGN	
AMBIENT TEMPERATURE	—	—	—	0°C	+25°C	+60°C	—	—	—
POWER SUPPLIES:									
+22 V	—	±7%	—	+20.46	+22	+23.54	—	—	
+8 V	—	±7%	—	+7.44	+8	+8.56	—	—	
+5.6 V	—	±7%	—	+5.21	+5.6	+5.99	—	—	
−22 V	—	±7%	—	−20.46	−22	−23.54	—	—	
−24.5 V	—	±7%	—	−22.79	−24.5	−26.21	—	—	
CONTROL FREQUENCIES:									
HEADWHEEL CKT	—	—	f_{IN}	—	1250 Hz	—	—	—	Control Signal
Iw CKT	—	—	f_{IN}	—	625 Hz	—	—	—	Control Signal
CAPSTAN CKT (1)	—	—	f_{IN}	—	1000 Hz	—	—	—	Control Signal
CAPSTAN CKT (2)	—	—	f_{IN}	—	250 Hz	—	—	—	Control Signal
ACTUAL MOTOR FREQUENCIES:									
HEADWHEEL	—	—	—	—	312.5 Hz	—	—	—	Square wave to motor.
Iw	—	—	—	—	156.25 Hz	—	—	—	Square wave to motor.
CAPSTAN (1)	—	—	—	—	250 Hz	—	—	—	Square wave to motor.
CAPSTAN (2)	—	—	—	—	62.5 Hz	—	—	—	Square wave to motor.

TABLE D-1. DESIGN ASSUMPTIONS (Continued)

ITEM	TOLERANCE		PARAMETER	DESIGN			MAX. STRESS		REMARKS
	INITIAL	DESIGN		MIN.	TYP.	MAX.	RATED	DESIGN	
RESISTORS:									
RNR55C ___	±1%	±2%	—	—	—	—	100 mW	50 mW	50% derating
RNR60C ___	±1%	±2%	—	—	—	—	125 mW	62.5 mW	50% derating
RNR 65C ___	±1%	±2%	—	—	—	—	250 mW	125 mW	50% derating
RLR 07 ___	±5%	±10%	—	—	—	—	250 mW	125 mW	50% derating
CAPACITORS:									
CSR13 ___	±10%		—	—	—	—	V_1	$0.6V_1$	60% rating; 3 a/v ckt. res. req'd
CYR06 ___	±10%		—	—	—	—	V_1	$0.6V_1$	60% rating
3150546	±10%		—	—	—	—	50 V	30 V	60% rating
DIODES:									
1N645	—	—	V_F	*	*	*	—	—	* MFR'S CURVE USED
	—	—	T_j	—	—	—	200°C	110°C	T_j ≤ 110°C max.
	—	—	V_R	—	—	—	225 V	180 V	80% rating
MZ-2361			V_F	1.30	1.35	1.40	—	—	25°C, 10 ma.
			θ_{VF}	*	*	*	—	—	* MFR'S CURVE USED (T.C. OF FWD. VOLTAGE)
			T_j	—	—	—	175°C	110°C	T_j = 110°C max
			θ_{JA}	—	—	100°C/W	—	—	MFR. SPEC.

TABLE D-1. DESIGN ASSUMPTIONS (Continued)

ITEM	TOLERANCE		PARAMETER	DESIGN			MAX. STRESS		REMARKS
	INITIAL	DESIGN		MIN.	TYP.	MAX.	RATED	DESIGN	
TRANSISTORS:	—	—							
2N720A	—	—	V_{CEO}	—	—	—	80 V	64 V	
	—	—	V_{CBO}	—	—	—	120V	96 V	
	—	—	V_{EBO}	—	—	—	7 V	5.6 V	
	—	—	T_j	—	—	—	200°C	110°C	
	—	—	V_{BE} (fwd)				—	—	
	—	—	V_{CE} (sat)				—	—	
	—	—	h_{FE}				—	—	
2N2907A	—	—	V_{CEO}	—	—	—	40 V	32 V	
	—	—	V_{CBO}	—	—	—	60 V	48 V	
	—	—	V_{EBO}	—	—	—	5 V	4.0V	
	—	—	T_j	—	—	—	200°C	110°C	
	—	—	V_{BE} (fwd)				—	—	
	—	—	V_{CE} (sat)				—	—	
	—	—	h_{FE}				—	—	
2N2405	—	—	V_{CEO}						
	—	—	V_{CBO}						
	—	—	V_{EBO}						
	—	—	T_j						
	—	—	V_{BE} (fwd)						
	—	—	V_{CE} (sat)						
	—	—	h_{FE}						

TABLE D-1. DESIGN ASSUMPTIONS (Continued)

ITEM	TOLERANCE		PARAMETER	DESIGN			MAX. STRESS		REMARKS
	INITIAL	DESIGN		MIN.	TYP.	MAX.	RATED	DESIGN	
2N2905	—	—	V_{CSO}	—	—	—	40V	32V	
	—	—	V_{CBO}	—	—	—	60V	48V	
	—	—	V_{EBO}	—	—	—	5V	4.0V	
	—	—	T_J	—	—	—	200°C	110°C	
		—	$V_{BE(fwd)}$				—	—	
	—	—	$V_{CE(sat)}$				—	—	
		—	h_{FE}				—	—	
	—	—	V_{CEO}	—	—	—	60V	48V	
	—	—	V_{CBO}	—	—	—	60V	48V	
		—	V_{EBO}	—	—	—	5V	4.0V	
	—	—	T_J	—	—	—	200°C	110°C	
	—	—	θ_{JA}	—	—	194°C/W	—	—	
	—	—	V_{BE} (fwd)	0.900	1.10	1.30	—	—	I_C = 1A, I_B = 1A } SPEC.
	—	—	V_{BE} (fwd)	0.575	0.675	0.775	—	—	I_C = 60mA, I_B = 6mA } SPEC.
	—	—	V_{BE} (fwd)	0.475	0.575	0.675	—	—	I_C = 5mA, I_B = 0.5mA } SPEC.
	—	—	h_{FE}	15	—	—	—	—	V_{CE} = 0.75V, I_C = 1A } FROM SPEC.
	—	—	h_{FE}	20.5*	—	—	—	—	V_{CE} = 0.75V, I_C = 10A } * FROM MFR'S CURVE
	—	—	h_{FE}	23.5*	—	—	—	—	V_{CE} = 0.75V, I_C = 8A } * FROM MFR'S CURVE
	—	—	θ_{VB}	*	*	*	—	—	* MFR'S CURVE USED
	—	—	$T_{\theta JA}$	—	160 sec	—	—	—	Thermal Time Constant Junction to Ambient (Based on Lab Measurements)

TABLE D-1. DESIGN ASSUMPTIONS (Continued)

ITEM	TOLERANCE		PARAMETER	DESIGN			MAX. STRESS		REMARKS
	INITIAL	DESIGN		MIN.	TYP.	MAX.	RATED	DESIGN	
INTEG. CKT. TI- 5472	—	—	V_{cc}	—	—	—	7 V	5.6V	80% rating
	—	—	T_j	—	—	—	150°C	110°C	
	—	—	I_{OUT}	—	—				
	—	—	FAN-OUT	—	—				
INTEG CKT. TI- 3400	—	—	V_{cc}	—	—	—	7 V	5.6V	80% rating
	—	—	T_j	—	—	—	150°C	110°C	
	—	—	I_{OUT}	—	—				
	—	—	FAN-OUT	—	—				
TRANSFORMER, HEADWHEEL	—	—	N_P	—	800	—	—	—	½ total primary
	—	—	N_S	—	35	—	—	—	each secondary
	—	—	R_P	8.50Ω	9.45Ω	10.87Ω	—	—	Variation over temp.
	—	—	R_S	0.171Ω	0.190Ω	0.208Ω	—	—	Variation over temp.
	—	—	θ_{Cu}	—	0.4%/°C	—	—	—	T.C. of Copper Windings
TRANSFORMER, CAPSTAN & IW	—	—	N_P	—	950	—	—	—	½ total primary
	—	—	N_S	—	44	—	—	—	each secondary
	—	—	R_P	24.1Ω	26.8Ω	30.8Ω	—	—	Variation over temp.
	—	—	R_S	0.437Ω	0.486Ω	0.560Ω	—	—	Variation over temp.
	—	—	θ_{Cu}	—	0.4%/°C	—	—	—	T.C. of Copper Windings
START INTERVALS FOR MOTORS	—	—	HEADWHEEL	—	5 SEC.	—	—	—	FIXED TIMED
	—	—	CAPSTAN	—	¼ SEC.	—	—	—	FORWARD
	—	—	CAPSTAN	—	1 SEC.	—	—	—	FAST REWIND
	—	—	IW	—	4 SEC.	—	—	—	

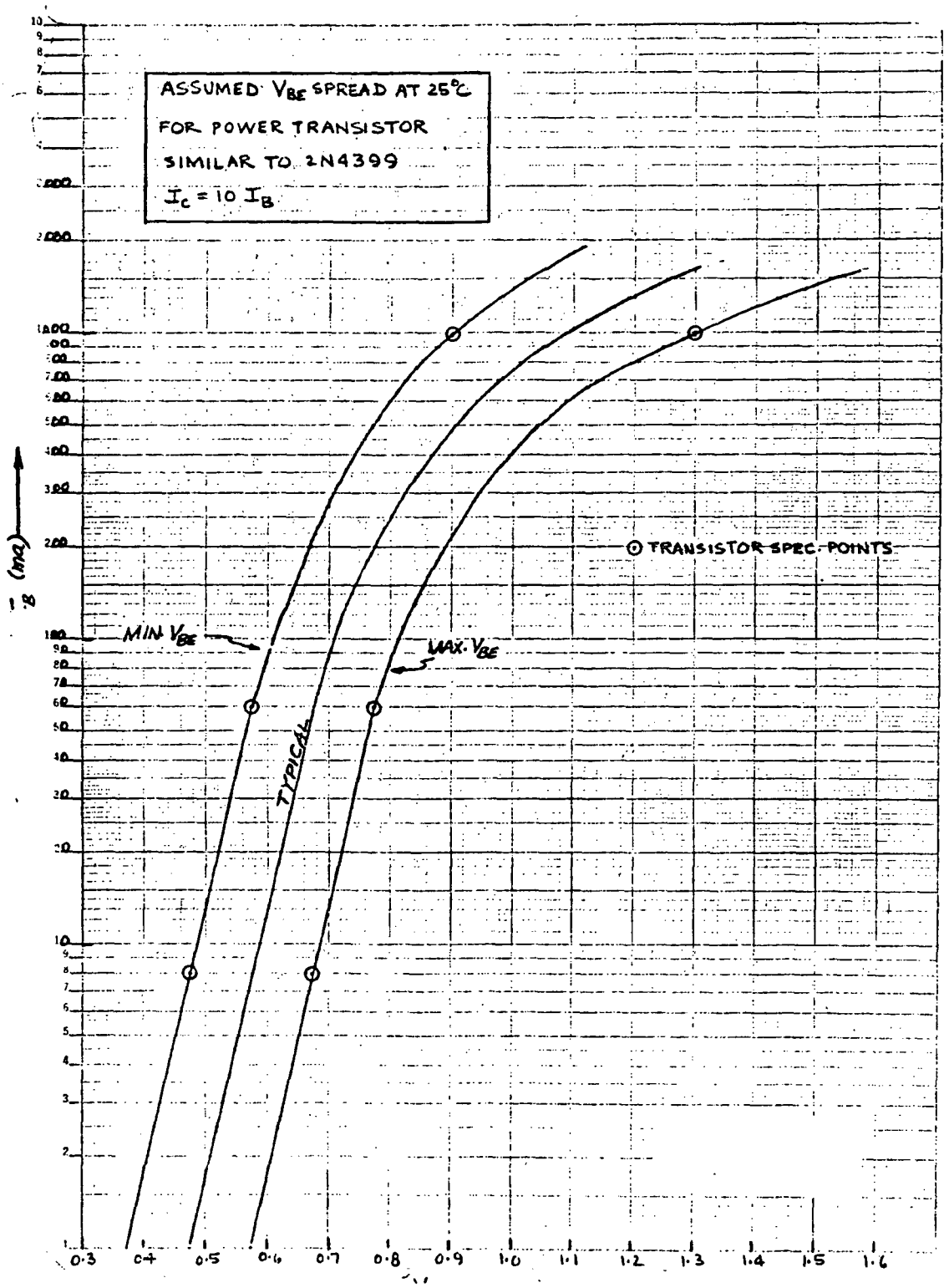


Figure D-1. Power Transistor V_{BE} Spread

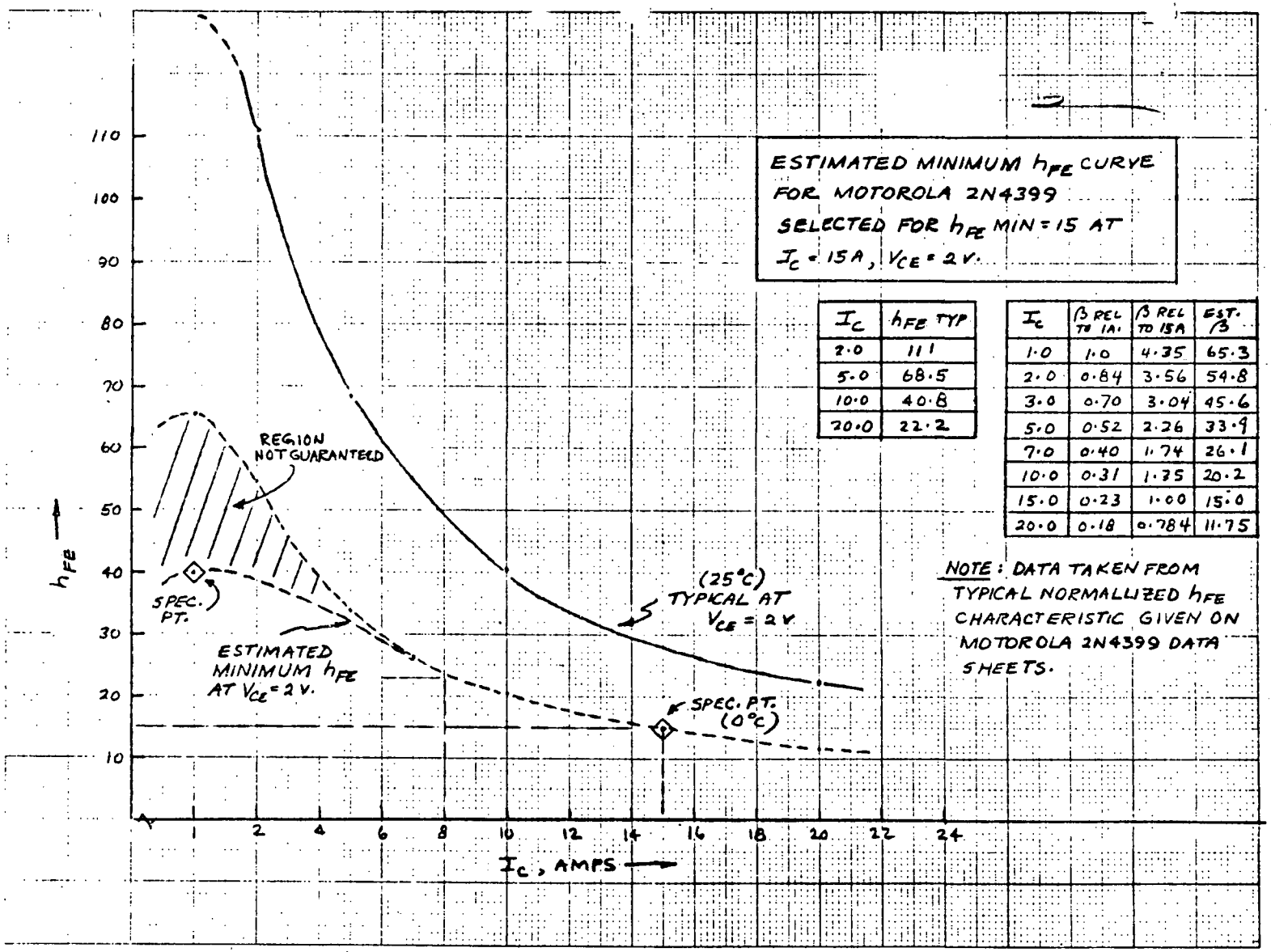


Figure D-2. Estimated Minimum h_{FE} Curve for Motorola 2N4399 Transistor

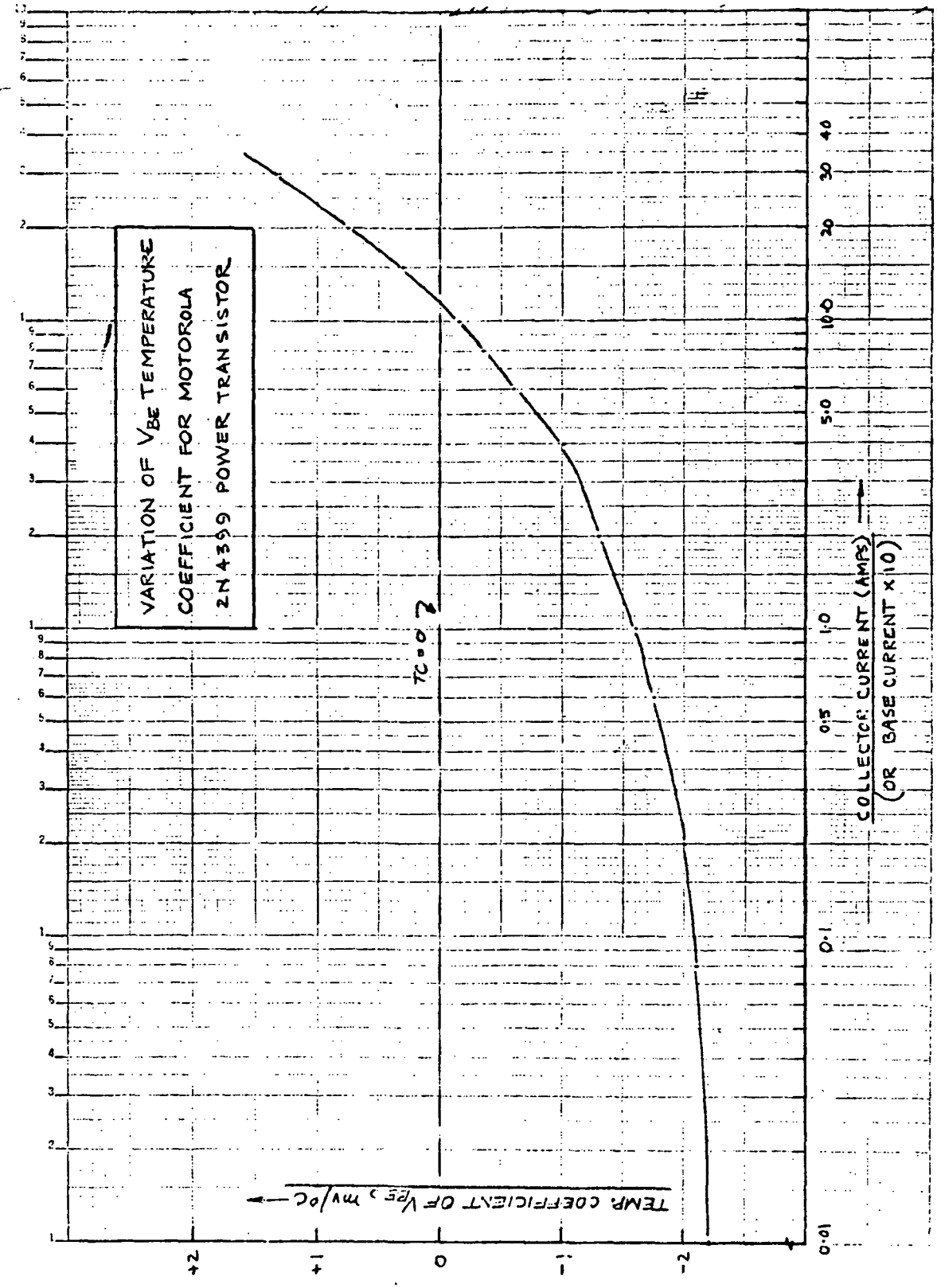


Figure D-3. Variation of V_{BE} Temperature Coefficient for Motorola 2N4399 Transistor

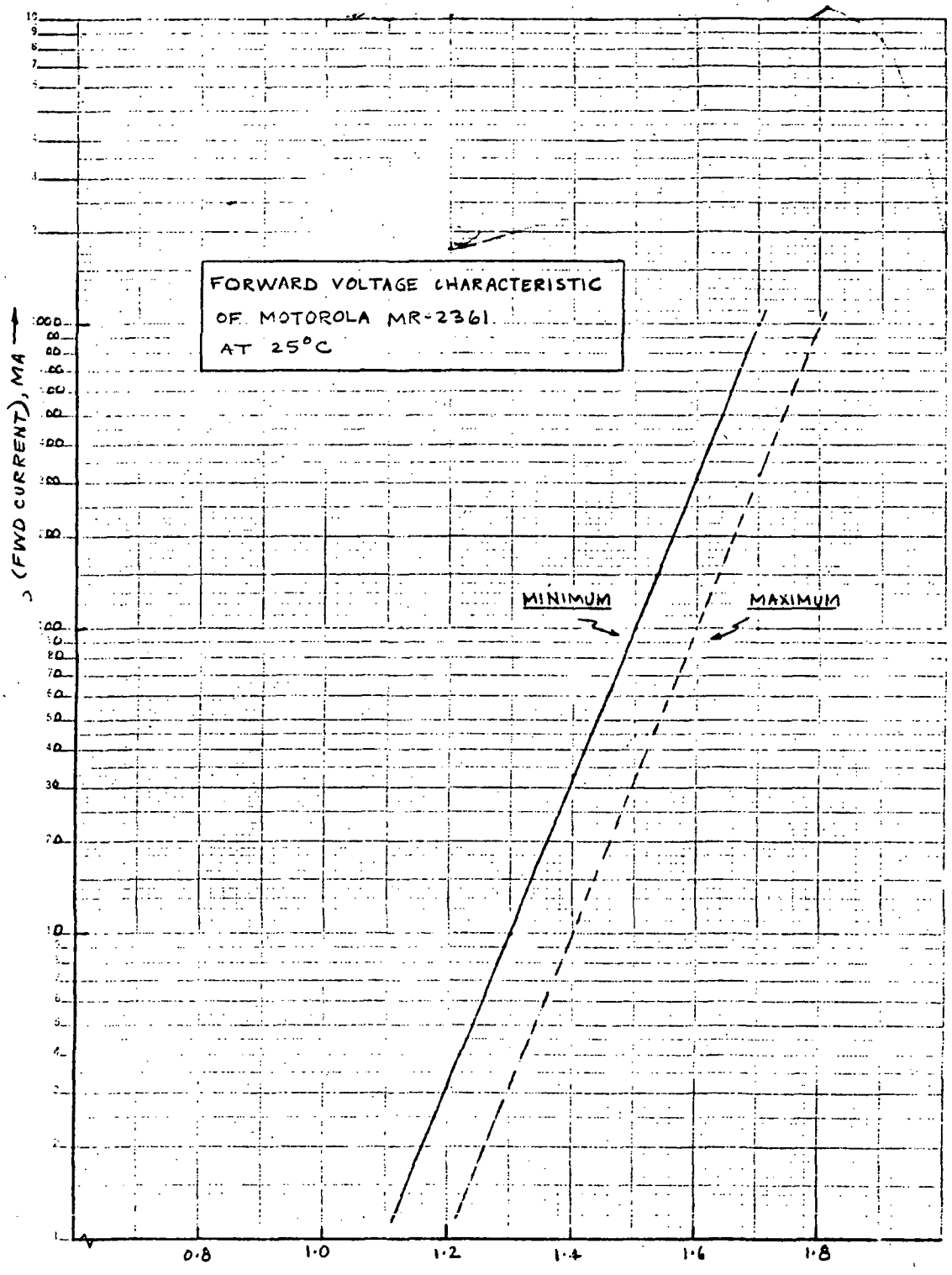


Figure D-4. Forward Voltage Characteristic of Motorola MR-2361 Diode

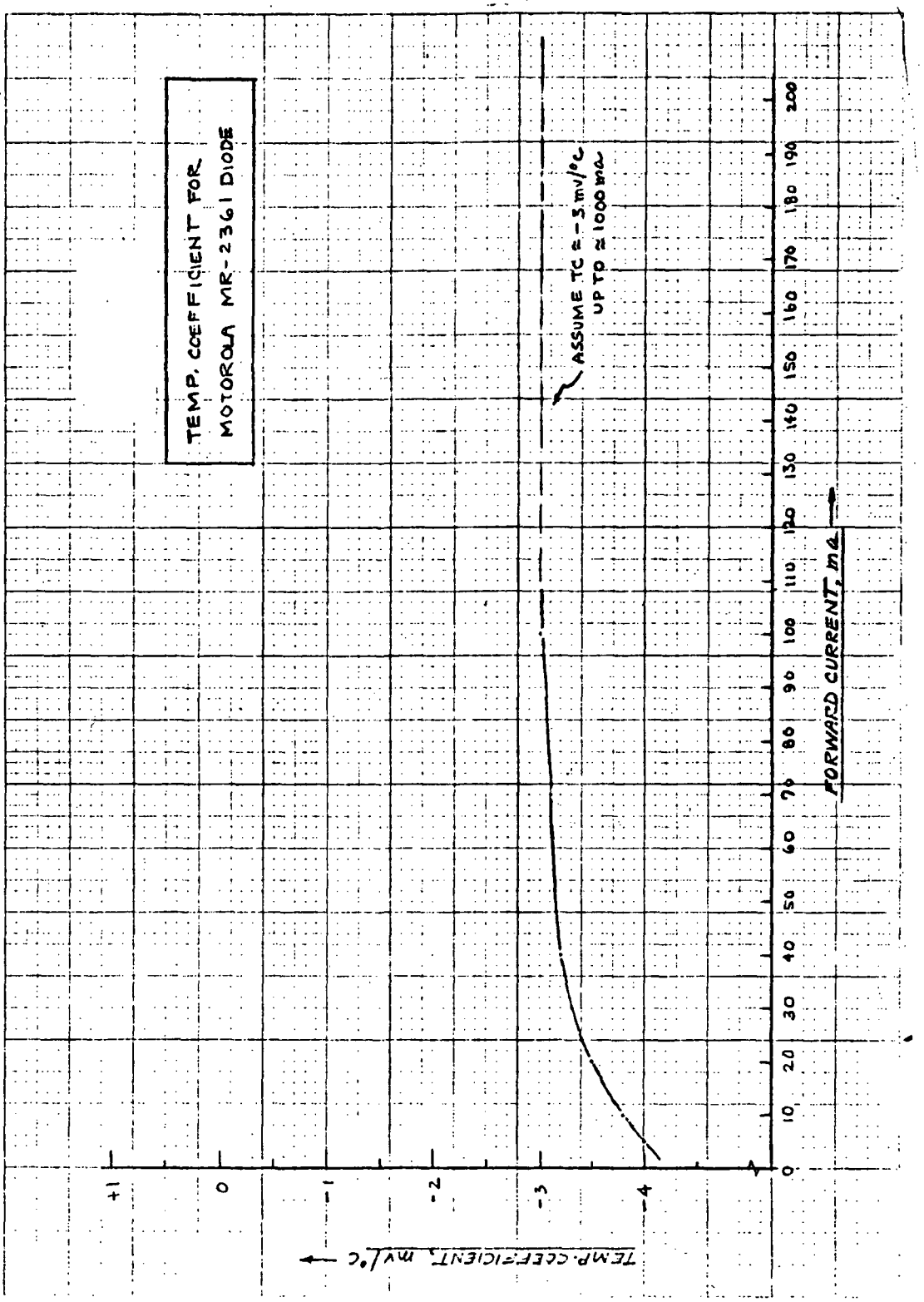


Figure D-5. Temperature Coefficient for Motorola MR-2361 Diode

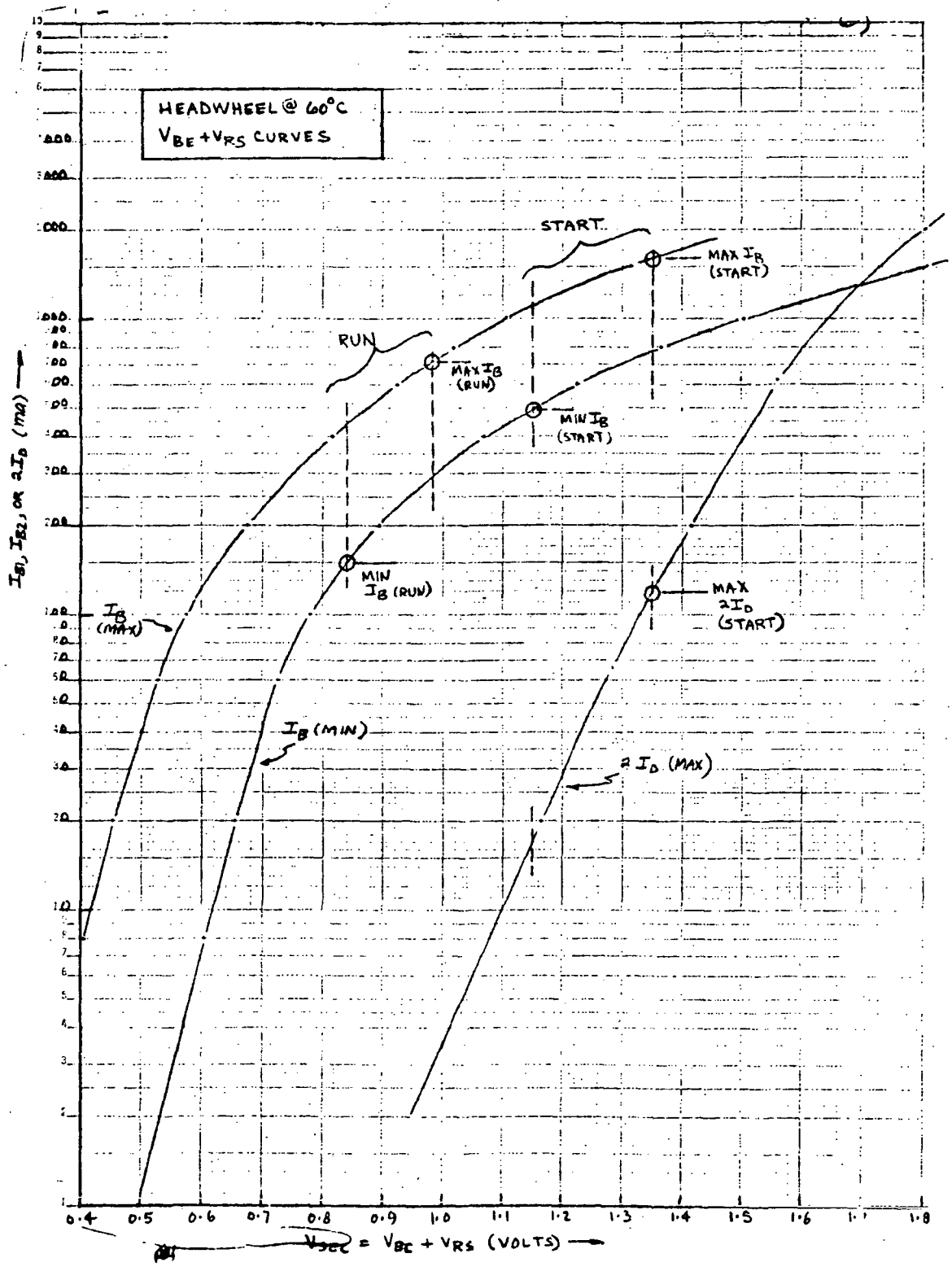


Figure D-6. Headwheel V_{BE} + V_{RS} Curves (60° C)

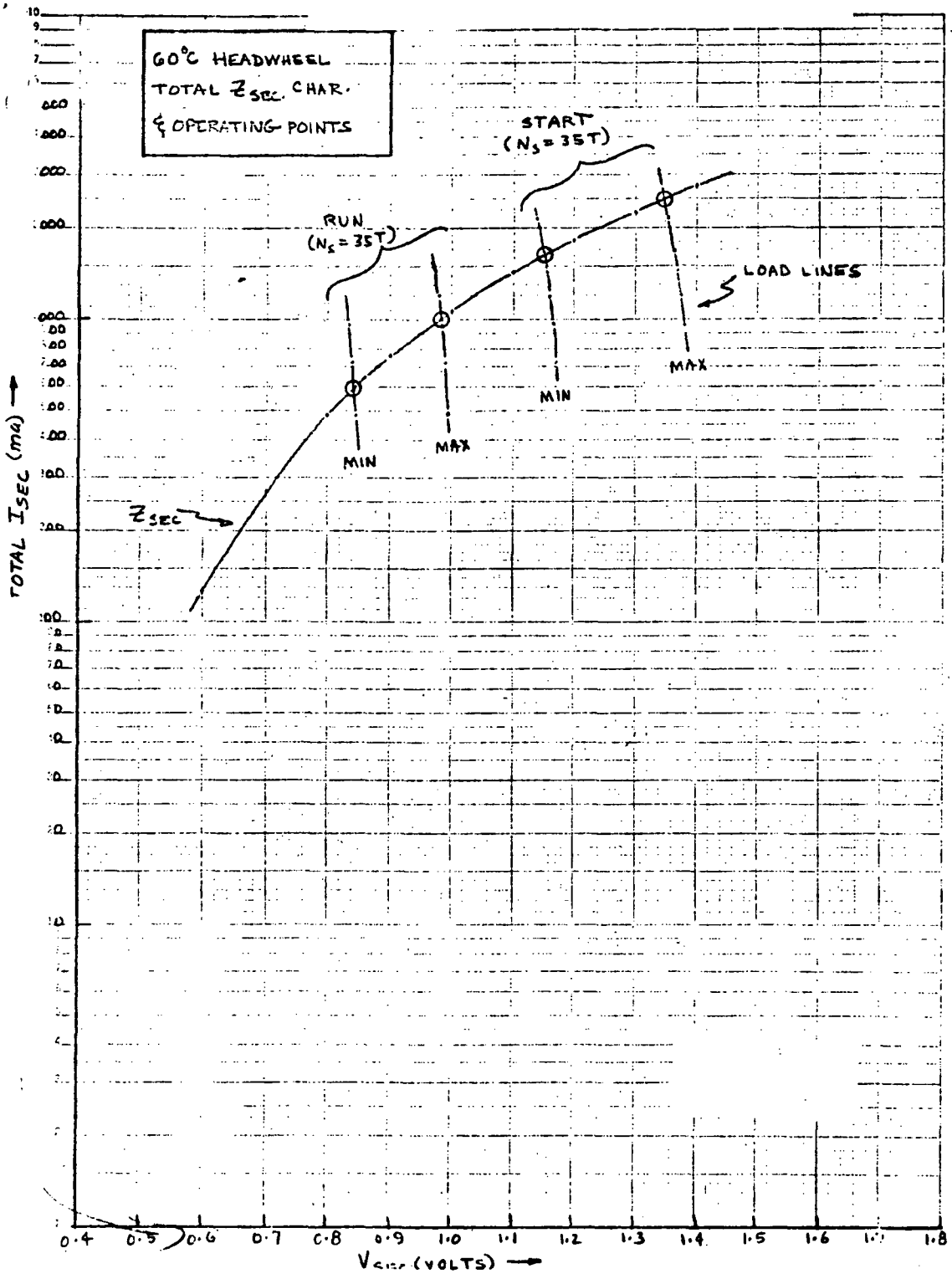


Figure D-7. Headwheel Total Z_{SEC} Characteristics and Operating Points (60° C)

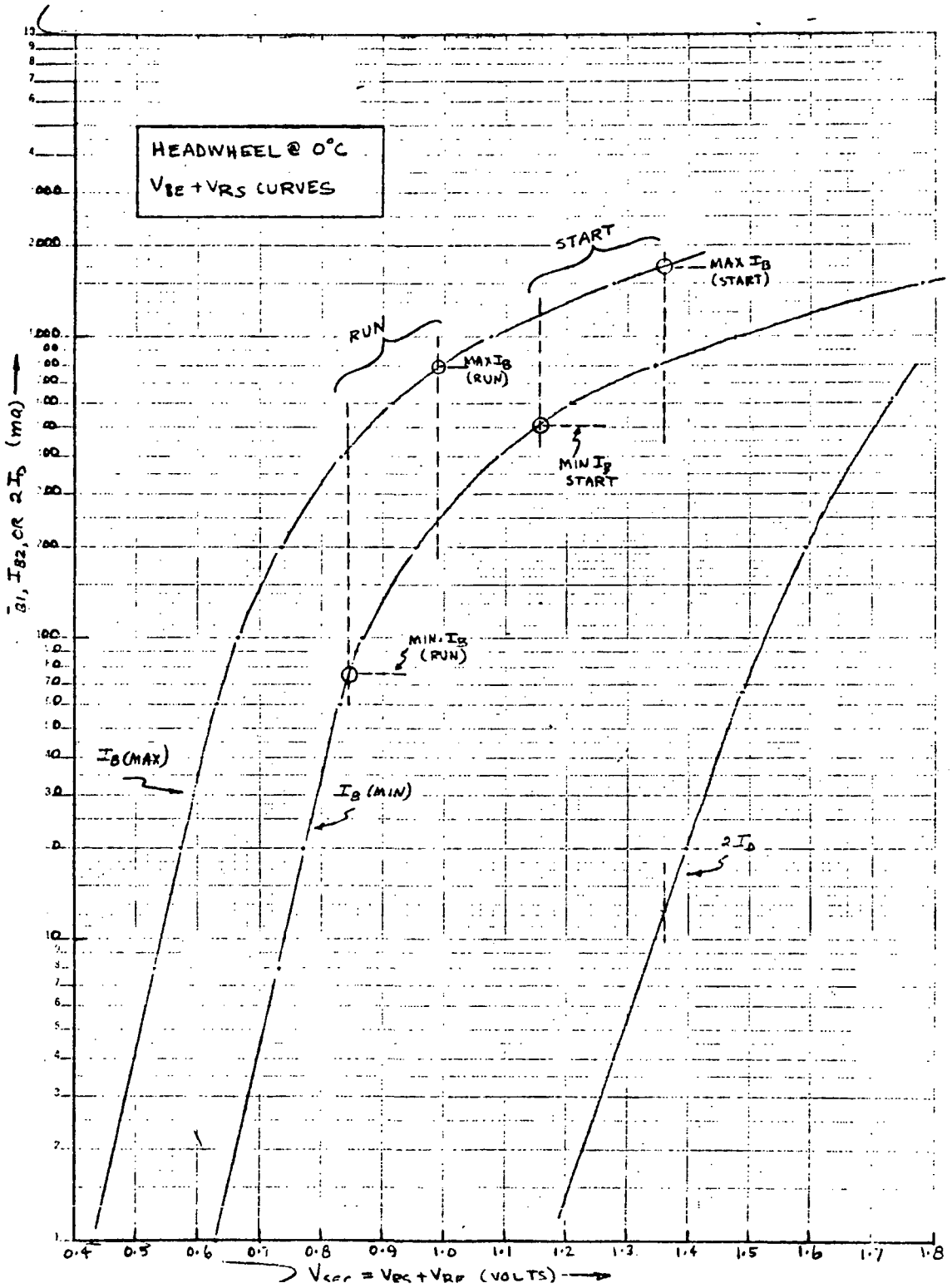


Figure D-8. Headwheel $V_{BE} + V_{RS}$ Curves (0° C)

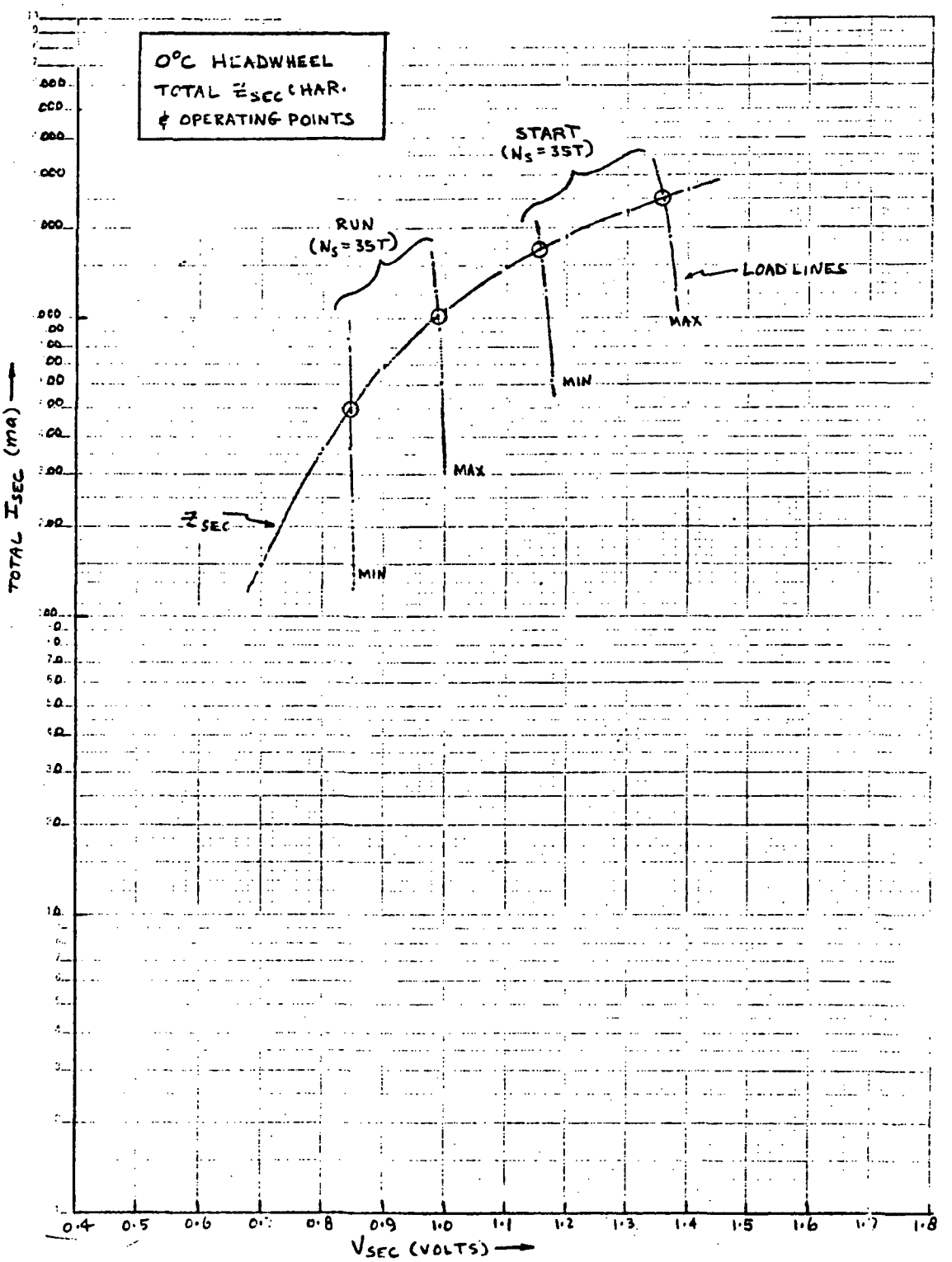


Figure D-9. Headwheel Total Z_{SEC} Characteristics and Operating Points (0° C)

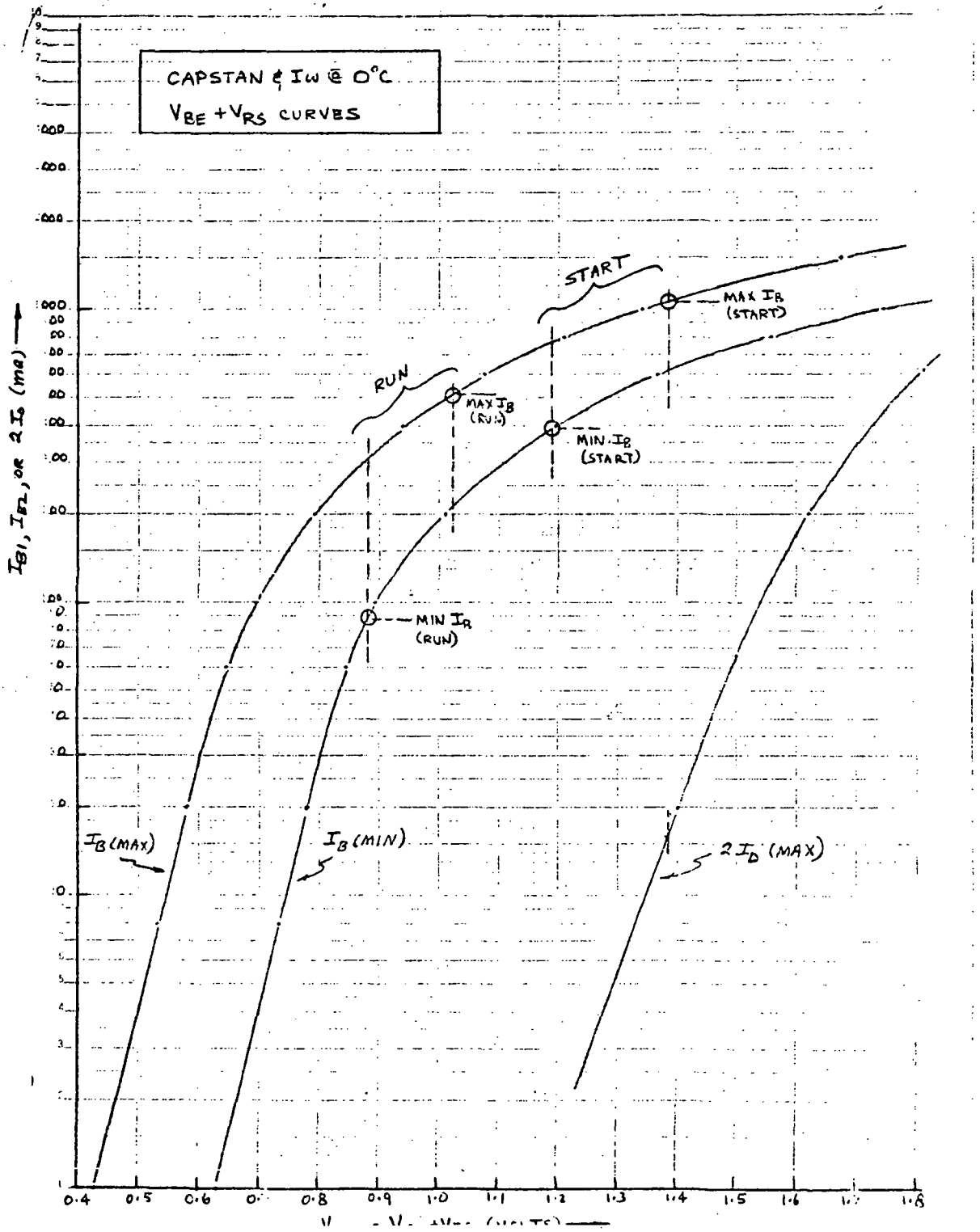


Figure D-10. Capstan and Iω V_{BE} + V_{RS} Curves (0° C)

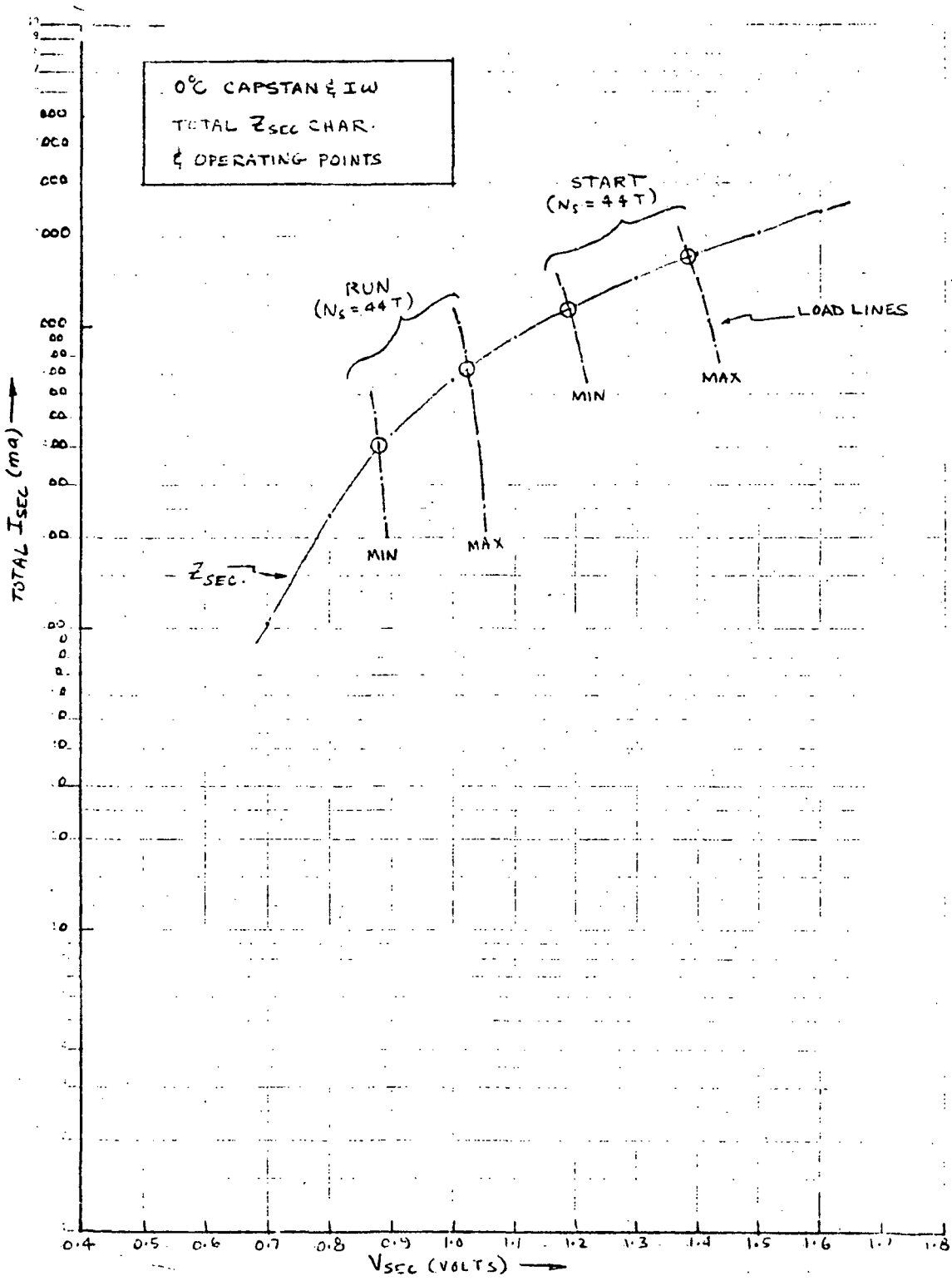


Figure D-11. Capstan and Iω Total Z_{SEC} Characteristics and Operating Points (0° C)

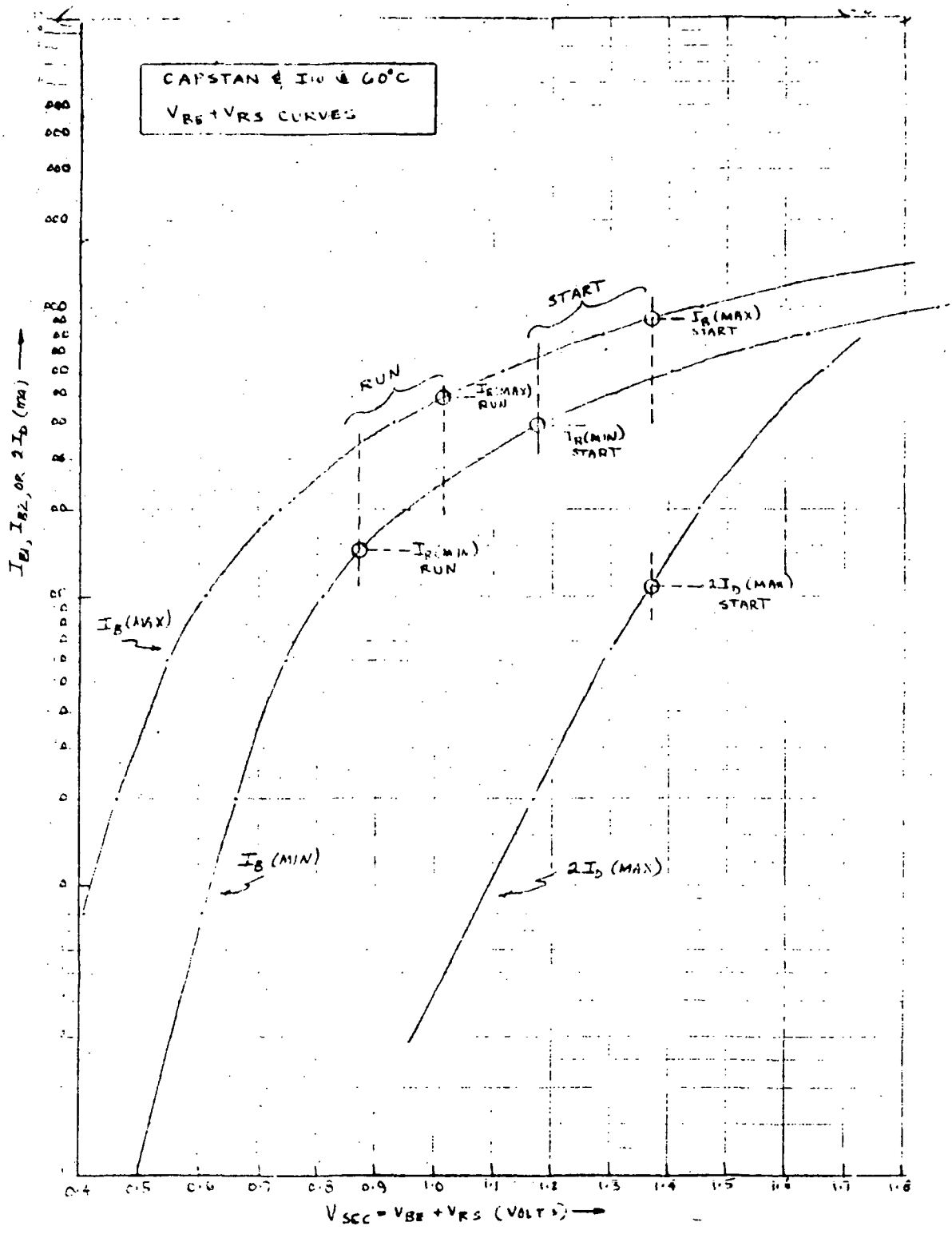


Figure D-12. Capstan and Iw $V_{BE} + V_{RS}$ Curves (60° C)

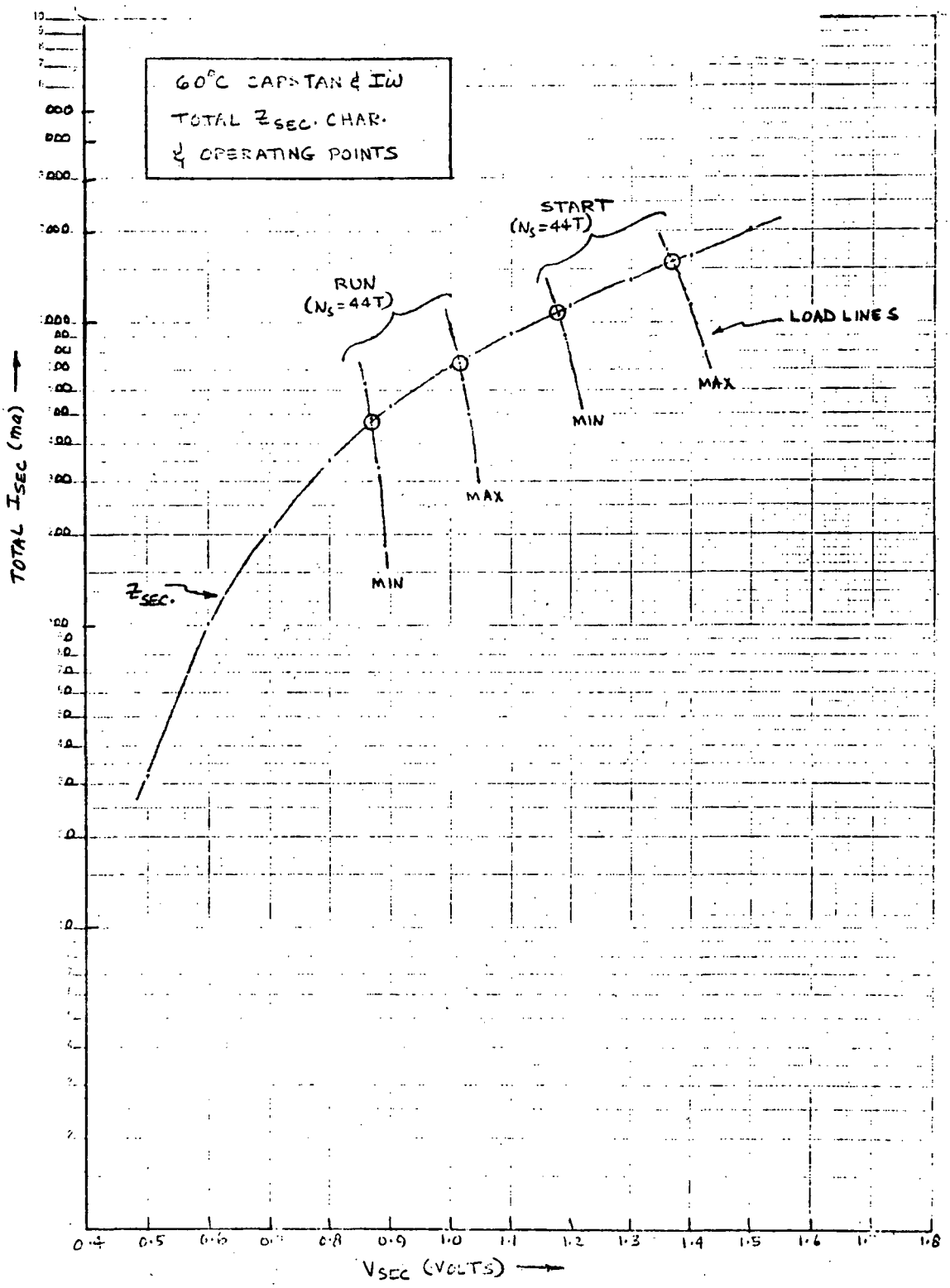


Figure D-13. Capstan and Iω Total Z_{SEC} Characteristics and Operating Points (60° C)

1. Graphical Construction of (V_{BE} + V_{RS}) Curves. -

(Voltages = mV)
(Currents = mA)

I_B	V_{BE} (25°C)		mV/°C T.C.	ΔV to 0°C	ΔV to +60°C	V_{BE} (0°C)		V_{BE} (60°C)	
	MIN	MAX				MIN	MAX	MIN	MAX
1	375	575	-2.2	+55	-77	430	630	298	498
8	475	675	-2.1	+53	-73	528	728	402	602
20	520	720	-2.0	+50	-70	570	770	450	650
60	575	775	-1.75	+44	-61	619	819	514	714
100	610	810	-1.60	+40	-56	650	850	554	754
200	670	890	-1.30	+32	-45	702	922	625	845
400	740	995	-1.00	+25	-35	765	1020	705	960
600	800	1090	-0.60	+15	-21	815	1105	779	1069
800	850	1200	-0.35	+9	-12	859	1209	838	1188
1000	900	1300	-0.15	+4	- 5	904	1304	895	1295
1500	1025	1530	+0.30	-7.5	+10.5	1018	1523	1035	1540

HEADWHEEL

I_B	0°C, R_S = 0.171 ohm			60°C, R_S = 0.208 ohm		
	V_{RS}	V_{BE} + V_{RS}		V_{RS}	V_{BE} + V_{RS}	
		MIN	MAX		MIN	MAX
1	—	430	630	—	298	498
8	1.4	529	729	1.7	404	604
20	3.4	573	773	4.2	454	654
60	10.2	629	829	12.5	527	727
100	17.1	667	867	20.8	575	775
200	34	736	956	41.6	667	887
400	68	833	1088	83.2	788	1043
600	102	917	1207	125	904	1194
800	137	996	1346	166	1004	1354
1000	171	1075	1475	208	1103	1503
1500	257	1275	1780	312	1347	1852

CAPSTAN AND Iω

I_B	0° C, R_S = 0.437 ohm			60° C, R_S = 0.560 ohm		
	V_{RS}	$V_{BE} + V_{RS}$		V_{RS}	$V_{BE} + V_{RS}$	
		MIN	MAX		MIN	MAX
1	0.4	430	630	0.6	299	499
8	3.5	532	732	4.5	407	607
20	8.75	579	779	11.2	461	661
60	26.2	645	845	33.6	548	748
100	43.7	694	894	56	610	810
200	87.5	790	1010	112	737	957
400	175	940	1195	224	929	1184
600	262	1077	1367	336	1115	1405
800	350	1209	1559	448	1286	1636
1000	437	1341	1741	560	1455	1855
1500	655	1673	2178	840	1875	2380

V_D (MR2361 Protective Diodes)

I_D	25° C MIN V_D	mV/° C T.C.	ΔV to 0° C	ΔV to 60° C	V_D (MIN)	
					0°	60°
10	1300	-3.9	+97.5	-137	1397	1163
33	1400	-3.4	+85	-119	1485	1281
100	1500	-3.0	+75	-105	1575	1395
310	1600	-3.0	+75	-105	1675	1495
1000	1700	-3.0	+75	-105	1775	1595

HEADWHEEL

I_D	0° C, R_S = 0.171 ohm		60° C, R_S = 0.208 ohm	
	V_{RS}	$V_D + V_{RS}$ (MIN)	V_{RS}	$V_D + V_{RS}$ (MIN)
10	1.71	1399	2.08	1165
33	5.6	1491	6.8	1288
100	17.1	1592	20.8	1416
310	53	1728	64.5	1560
1000	171	1946	208	1803

CAPSTAN AND Iω

I_D	0°C, R_s = 0.437 ohm		60°C, R_s = 0.560 ohm	
	V_{RS}	$V_D + V_{RS}$ (MIN)	V_{RS}	$V_D + V_{RS}$ (MIN)
10	4.37	1401	5.6	1169
33	14.4	1499	18.5	1300
100	43.7	1619	56	1451
310	135	1810	174	1669
1000	437	2212	560	2155

2. Graphical Construction of Total Secondary Impedance Curves. -

(From Plots of I_{B1}(min), I_{B2}max), and $2I_D$ vs. $V_{sec.}$)

HEADWHEEL

$V_{sec.}$	0°C				60°C			
	I_{B1} (MIN)	I_{B2} (MAX)	$2I_D$	Total $I_{sec.}$	I_{B1} (MIN)	I_{B2} (MAX)	$2I_D$	Total $I_{sec.}$
600	—	—	—	—	7	120	—	127
700	4.5	145	—	150	40	230	—	270
800	34	330	—	364	115	370	—	485
900	135	560	—	695	210	550	—	760
1000	260	820	—	1080	315	750	—	1065
1100	440	1050	—	1490	430	980	10	1420
1200	590	1300	1.4	1891	560	1230	29	1819
1300	740	1550	5.4	2295	760	1480	76	2256
1400	880	1800	21	2701	850	1730	180	2760

CAPSTAN AND I_ω

V_{sec}	0°C				60°C			
	I_{B1}	I_{B2}	$2I_D$	Total I_{sec}	I_{B1}	I_{B2}	$2I_D$	Total I_{sec}
500	—	—	—	—	1	31	—	32
600	—	—	—	—	7	94	—	101
700	4	100	—	104	35	170	—	205
800	29	210	—	239	95	260	—	355
900	105	340	—	445	165	370	—	535
1000	190	480	—	670	236	475	4.4	715
1100	290	640	—	930	320	580	11	911
1200	400	790	—	1190	410	700	27	1137
1300	520	940	5.4	1465	500	820	66	1386
1400	640	1080	20	1740	590	950	135	1675
1500	750	1250	66	2066	690	1050	265	2005
1600	850	1380	170	2400	—	—	—	—

3. Calculated Load Lines. -

HEADWHEEL 0°C

Start (MIN)		Start (MAX)		Run (MIN)		Run (MAX)	
V_{sec}	I_{sec} (mA)	V_{sec}	I_{sec} (mA)	V_{sec}	I_{sec} (mA)	V_{sec}	I_{sec} (mA)
1185	0	1400	0	854	0	1005	0
1175	614	1380	1230	852	123	1000	306
1165	1230	1370	1840	850	245	995	614
1160	1535	1360	2460	848	368	990	920
1155	1840	1350	3070	846	490	985	1230
				840	860	980	1535

HEADWHEEL @ 60°C

Start (MIN)		Start (MAX)		Run (MIN)		Run (MAX)	
V_{sec}	I_{sec} (mA)	V_{sec}	I_{sec} (mA)	V_{sec}	I_{sec} (mA)	V_{sec}	I_{sec} (mA)
1185	0	1400	0	854	0	1005	0
1175	480	1390	480	844	480	995	480
1170	722	1385	722	839	722	990	722
1165	960	1380	960	834	960	985	960
1160	1200	1375	1200	829	1200	980	1200
1155	1440	1370	1440			975	1440
1150	1680	1365	1680				
1140	2160	1355	2160				
1130	2640	1345	2640				

CAPSTAN AND Iω @ 0°C

Start (MIN)		Start (MAX)		Run (MIN)		Run (MAX)	
V_{sec}	I_{sec} (mA)	V_{sec}	I_{sec} (mA)	V_{sec}	I_{sec} (mA)	V_{sec}	I_{sec} (mA)
1250	0	1475	0	902	0	1063	0
1210	774	1430	870	890	232	1050	251
1200	966	1420	1060	880	425	1040	445
1190	1160	1410	1260	885	329	1030	638
1180	1355	1400	1450	875	522	1020	830
		1380	1840			1010	1025

CAPSTAN AND Iω @ 60°C

Start (MIN)		Start (MAX)		Run (MIN)		Run (MAX)	
V_{sec}	I_{sec} (mA)	V_{sec}	I_{sec} (mA)	V_{sec}	I_{sec} (mA)	V_{sec}	I_{sec} (mA)
1250	0	1475	0	902	0	1063	0
1210	606	1420	834	880	334	1040	349
1200	757	1410	985	870	485	1030	500
1190	910	1400	1140	890	182	1020	652
1180	1060	1390	1290	860	636	1010	804
1170	1210	1380	1440			1000	955
		1370	1590				
		1360	1740				

4. Calculations from Graphical Data. -

a. Resulting Power Stress in Protective Diodes. -

1. Headwheel $2\bar{I}_D$ = 12.4 mA from Figure D-8

(a) 0° C $\bar{I}_D$ = 6.2 mA
@ V_D = 1.36 V
} P_D = 8.44 mW peak @ 50% duty cycle = 4.22 mW AVG

$2\bar{I}_D$ = 120 mA from Figure D-6

(b) 60° C $\bar{I}_D$ = 60 mA
@ V_D = 1.35 V
} P_D = 81.0 mW peak @ 50% duty cycle = 40.5 mW AVG.

2. Capstan and Iω

$2\bar{I}_D$ = 16 mA from Figure D-10

(a) 0° C $\bar{I}_D$ = 8.0 mA
@ V_D = 1.385 V
} P_D = 11.1 mW peak @ 50% duty
= 5.55 mW AVG

$2\bar{I}_D$ = 108 mA from Figure D-12

(b) 60° C $\bar{I}_D$ = 54 mA
@ V_D = 1.370 V
} P_D = 74.0 mW peak @ 50% duty
= 37 mW AVG

b. Required Primary Current. -

Per phase current in driver (2N2405) calculated for:

(a) One power transistor is supplied its minimum required base current.

(b) Other power transistor is supplied its maximum base current.

(c) Protective diodes consume their maximum forward currents.

Total current (2 phases) in PNP start circuit (2N2905) = 2 x I per ϕ.

a. Headwheel

0° C Start. - From Figure D-9, I_{sec} = 1700 mA (Min. required)

$$N = \frac{800}{35} = 22.85 \text{ per } \phi, \quad \bar{I}_{pri} = \frac{1700}{22.85} = \boxed{74.4 \text{ mA}}$$

Start Current (2N2905) = 2(74.4) = $\boxed{149 \text{ mA}}$

0° C Run. - From Figure D-8, I_{sec} = 500 mA

I_{pri} = 500/22.85 = $\boxed{21.9 \text{ mA}}$ per ϕ.

60° C Start. - From Figure D-7, I_{sec} = 1640 mA (min required)

$$I_{pri} = \frac{I_{sec}}{N} = \frac{1640}{22.85} = \boxed{71.8 \text{ mA}} \quad (2N2405)$$

$2I_{pri}$ = 2(71.8) = $\boxed{143.6 \text{ mA}}$ Start current 2N2905

60° C Run. - From Figure D-7, I_{sec} = 590 mA (min required)

$$I_{pri} = \frac{590}{22.85} = \boxed{25.8 \text{ mA}} \quad (2N2405)$$

b. Capstan and Iω. - $N = \frac{950}{44} = 21.6$

0° C Start. - From Figure D-11, I_{sec} = 1150 mA (min required)

$$I_{pri} = \frac{1150}{21.6} = \boxed{53.2 \text{ mA}} \quad (2N2405)$$

$2I_{pri}$ = 2(53.2) = $\boxed{106.4 \text{ mA}}$ Start current 2N2905

0° C Run. - From Figure D-11, I_{sec} = 400 mA (min required)

$$I_{pri} = \frac{400}{21.6} = \boxed{18.5 \text{ mA}} \quad \text{(2N2405)}$$

60° C Start. - From Figure D-13, I_{sec} = 1080 mA (min required)

$$I_{pri} = \frac{1080}{21.6} = \boxed{50 \text{ mA}} \quad \text{(2N2405)}$$

$$2I_{pri} = 2(50) = \boxed{100 \text{ mA}} \quad \text{(2N2905)}$$

60° C Run. - From Figure D-13, I_{sec} = 475 mA (min required)

$$I_{pri} = \frac{475}{21.6} = \boxed{22.0 \text{ mA}} \quad \text{(2N2405)}$$

β Required for Driver Transistors (2N2405).

I_B = 2.66 mA (calculated previously)

Circuit		Per ϕ I_{pri} Req'd	Min Base Drive Available	Min β Req'd $= I_c / I_B$
Headwheel				
Start	0° C	74.4	2.66	28.0
	60° C	71.8	2.66	27.0
Run	0° C	21.9	2.66	8.24
	60° C	25.8	2.66	9.7
Capstan and Iω				
Start	0° C	53.2	2.66	20.0
	60° C	50.0	2.66	18.8
Run	0° C	18.5	2.66	6.95
	60° C	22.0	2.66	8.26

APPENDIX E

CAPSTAN SERVO ERROR AMPLIFIER WORST CASE ANALYSIS BODE PLOT COMPUTATIONS

APPENDIX E

CAPSTAN SERVO ERROR AMPLIFIER WORST CASE ANALYSIS BODE PLOT COMPUTATIONS

1. Lead/Lag Network Following Phase Comparator. -

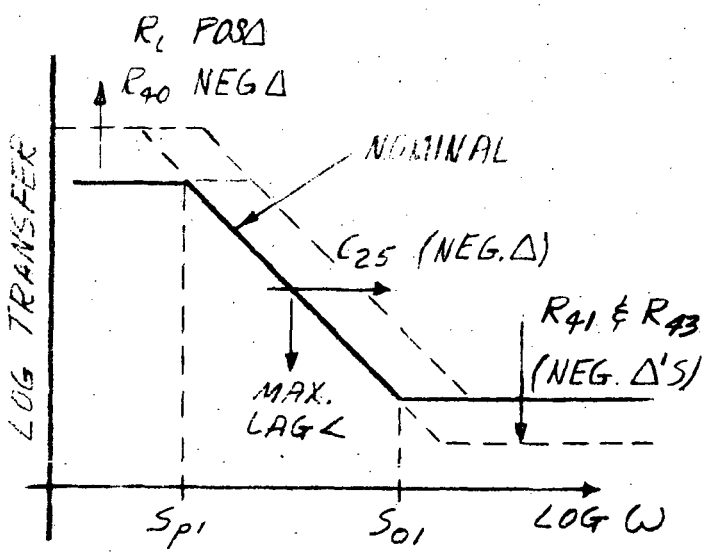
$$A_1(s) = \left[\frac{R_{41} + R_{73}}{R_{40}}\right] \cdot \left[\frac{s + \left(\frac{1}{[R_{41} + R_{73}]1/2\ C_{25}}\right)}{s + \left(\frac{1}{\left(\frac{R_{40}\ R_L}{R_{40} + R_L}\right)1/2\ C_{25}}\right)}\right]$$

$$= A_1 \frac{(s + s_{01})}{(s + s_{p1})}$$

$$A_1(s) = 0.0112 \left[\frac{s + 4.58}{s + 0.0615}\right] \rightarrow \left(\begin{array}{l} 0.83 \\ \text{as } s \rightarrow 0 \end{array}\right)$$

(Nominal)

Worst Case Development with partial Bode Plot:



1 Maximize low frequency gain and minimize high frequency gain, to diminish gain margin.

Implement by:

a) negative Δ's for R_{41} and R_{43} and R_{40}

b) positive Δ for *R_L.

*where R_L is Q10 with maximum $h_{FE} = 900$.

2 Shift curve to right to augment the total system lag angle.

Implement by:

a) negative Δ for C_{25}.

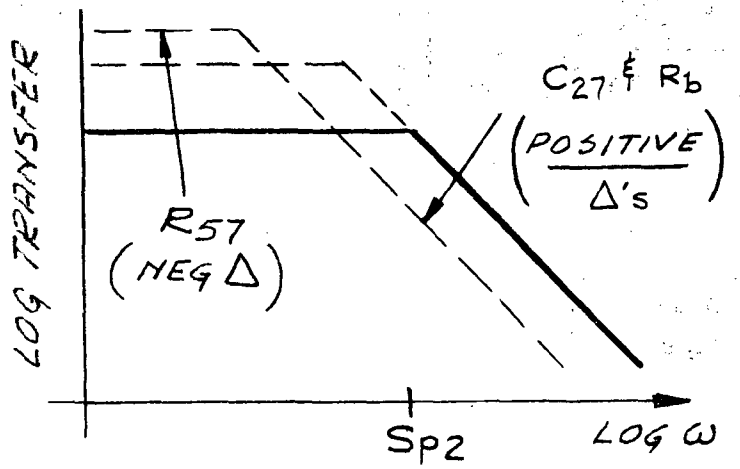
2.

$$A_2(s) = \frac{A_2}{(s + s_{p2})} = -\frac{\left(\frac{1}{R_{57}\,C_{27}}\right)}{\left(s + \frac{1}{R_b\,C_{27}}\right)}$$

$$A_2(s) = -10^4\left[\frac{1}{s + 740}\right] \rightarrow \begin{matrix} 13.5 \\ s \rightarrow 0 \end{matrix}$$

(Nominal)

Worst Case Development with Partial Bode:



1 Shift curve to left to increase lag < and, therefore, system lag < ;

Implement by:

a) C_{27}, positive Δ

b) R_b max; (R_{59} and R_{60} MAX with positive Δ's).

2 Increase transfer by R_{57} with negative Δ.

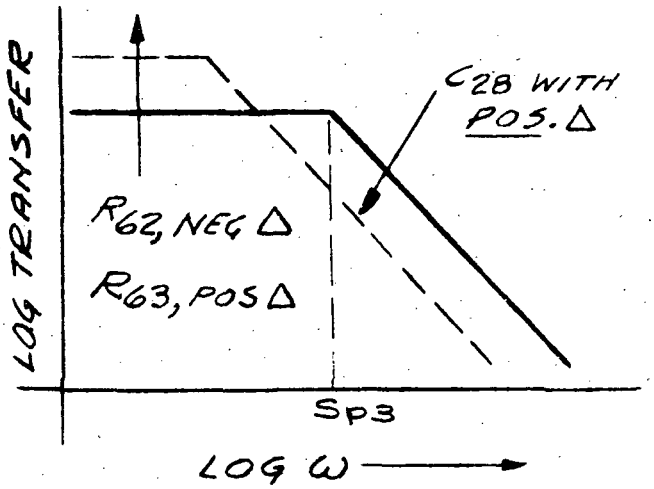
3. Lag Network Following Operational Amplifier. -

$$A_3(s) = \frac{A_3}{(s + s_{p3})} = \frac{\left(\frac{1}{R_{62}\,C_{28}}\right)}{\left(s + \frac{1}{\left(\frac{R_{62}\,R_{63}}{R_{62} + R_{63}}\right)C_{28}}\right)}$$

$$A_3(s) = \left(\frac{10}{s + 20}\right) \rightarrow \begin{matrix} 0.5 \\ \text{as } s \rightarrow 0 \end{matrix}$$

(Nominal)

Worst Case Development with partial Bode plot:



1 Shift curve to left to augment system lag <

Implement by:

C_{28} with positive Δ

2 Enhance transfer:

a) R_{62} with negative Δ

b) R_{63} with positive Δ.

TABLE E-1. WORST CASE COMPONENTS

(with respect to stability criteria)

Symbol No.	Nominal Value (X_i)	ΔX_i	Worst Case X_i
R_{40}	1×10^6 ohms	-1.2×10^5	0.89×10^6 ohms
R_{41} min	10,000 var.	-10,000	0 ohms
R_{73}	6200	-740	5460 ohms
C_{25}/C_{31}	19.5 uF	-5.2 uF	14.3 uF
R_L (h_{fe}Q10)	5.0×10^6	$+2.5 \times 10^6$	7.5×10^6 ohms
R_{57}	10^4	-1.2×10^3	8.8×10^3 ohms
R_{59}	10^4	$+1.2 \times 10^3$	11.2×10^3 ohms
R_{60} max	0.250×10^6 var.	$+35 \times 10^3$	2.85×10^5 ohms
C_{27}	0.01 uF	$+1.1 \times 10^{-12}$	0.0111 uF
R_{62}	10^4	-1.2×10^3	8.8×10^3 ohms
R_{63}	10^4	$+1.2 \times 10^3$	11.2×10^3 ohms
C_{28}	10 uF	$+2.6 \times 10^{-6}$	12.6 uF

4.

$$f(j\omega) = \overbrace{(3.75)(0.496)(5/16)}^{\max\ \varphi \cdot M \cdot (\text{Freq Trans})} \overbrace{\left[0.00612\left(\frac{j\omega+12.8}{j\omega+.088}\right)\cdot\left(\frac{1.02\times10^4}{j\omega+.315}\right)\cdot\left(\frac{9.0}{j\omega+16.2}\right)\right]}^{H_1(j\omega)} \times \overbrace{\left[\frac{300}{j\omega+300}\right]}^{H_4(j\omega)}$$

WORST CASE (stability)

$$\boxed{f(j\omega) = 9.1\ (+19.2\ \text{DB}) \quad \omega \to 0}$$

Drop-out Filters:

$Q_L = 10$

Tuning error $\leq 2\%$

$$f(j\omega) = \overbrace{(3.62)(0.410)(5/16)}^{\text{nominal}} \left[0.0112\left(\frac{j\omega+4.58}{j\omega+.0615}\right)\cdot\left(\frac{10^4}{j\omega+740}\right)\cdot\left(\frac{10}{j\omega+20}\right)\right] \times \left[\frac{300}{j\omega+300}\right]$$

NOMINAL CASE

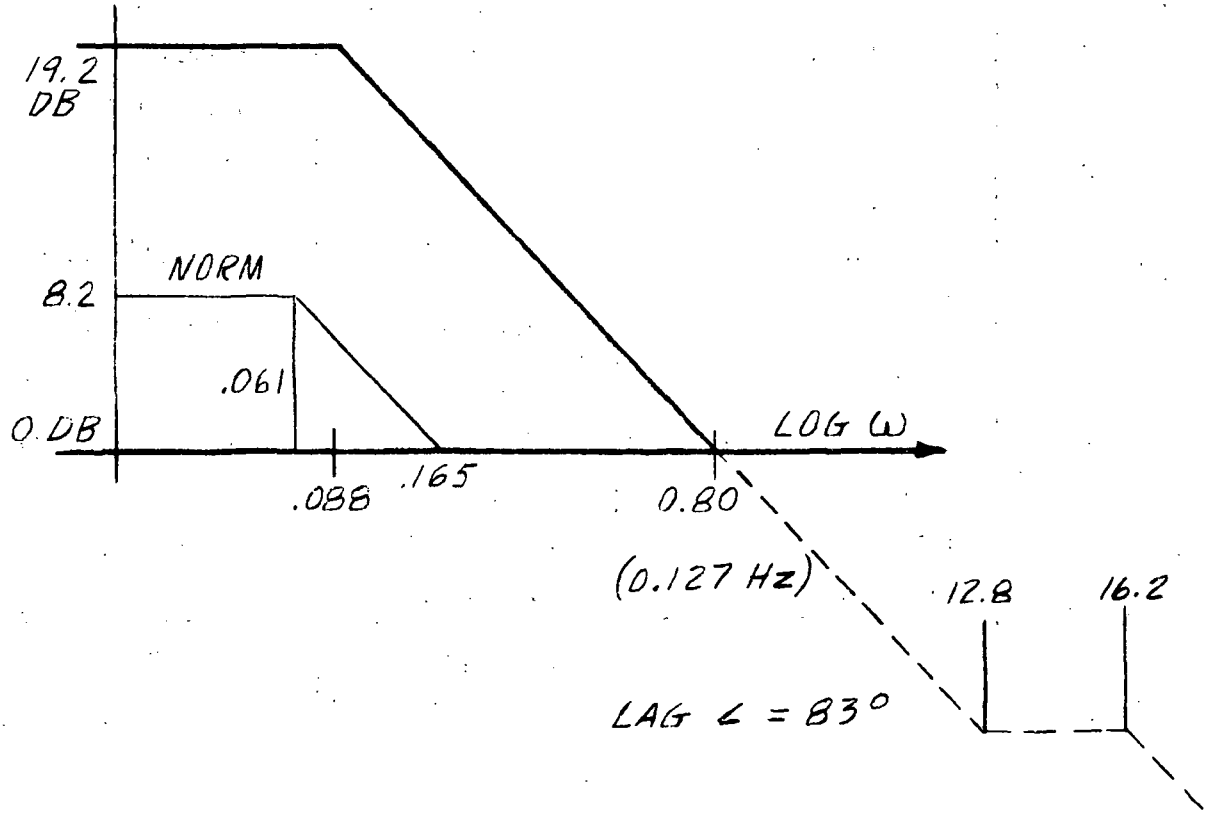
$$\boxed{f(j\omega) = 2.57\ (+8.2\ \text{DB}) \quad \omega \to 0}$$

where: $f(j\omega) = G(j\omega)/H_2(j\omega) \cdot H_3(j\omega)$

and

$$G(j\omega) = \overbrace{H_o}^{\varphi\ \text{comp., VCO \& Freq. Translation}} \times H_1(j\omega)\ (\text{Cumulative LPF}) \times H_2(j\omega)\ (\text{Capstan Motor Drive}) \times H_3(j\omega)\ (\text{Tape Transport Mechanism}) \times H_4(j\omega)\ (\text{Drop-Out Filter})$$

Worst Case Bode



APPENDIX F

MULTIVIBRATOR PULSE WIDTH VARIATION AND h_{ie} CHARACTERISTICS

APPENDIX F

1. Comparison of $(1 + \beta)R_E$ with h_{ie}. -

From Figure F-1: $I_E = \dfrac{V_{VR3} - V_E}{R_E}$

$$I_{E_{min.}} = \frac{7.24 - 4.78}{4.624k} = 0.532 \text{ mA}$$

$$I_E = I_C + I_B = I_C + \frac{I_C}{\beta} = I_C \left(1 + \frac{1}{\beta}\right)$$

$$I_C = \frac{I_E}{(1 + \frac{1}{\beta_{min}})} = \frac{0.532 \text{ mA}}{1 + \frac{1}{51.5}} = 0.522 \text{ mA}$$

$\beta_{min.}$ due to aging and temp = 59

$$\beta_{min} = \frac{170}{195} (59) = 51.5$$

at $I_C \approx 0.522$ mA, $h_{ie} = 12k$ from typical curves. At $I_C = 1$ mA,

$h_{ie_{max}} = 12k$, $h_{ie_{typ}} = 7k$; thus at $I_C = 0.522$ mA,

$$h_{ie_{max}} \approx \frac{12}{7} (12k) = 20.6k$$

$$(1 + \beta)R_E = (52.5)(4.624k) = 243k$$

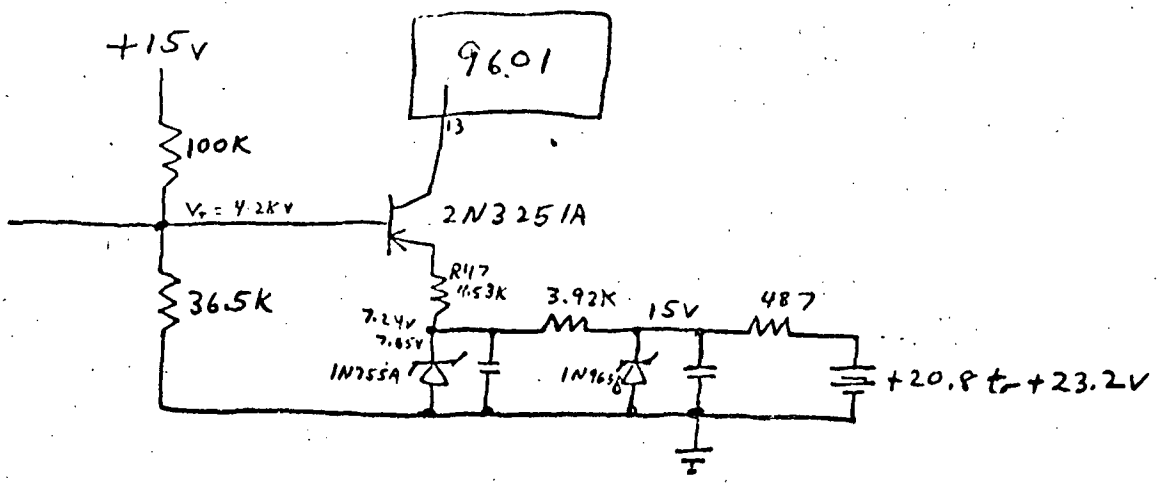


Figure F-1

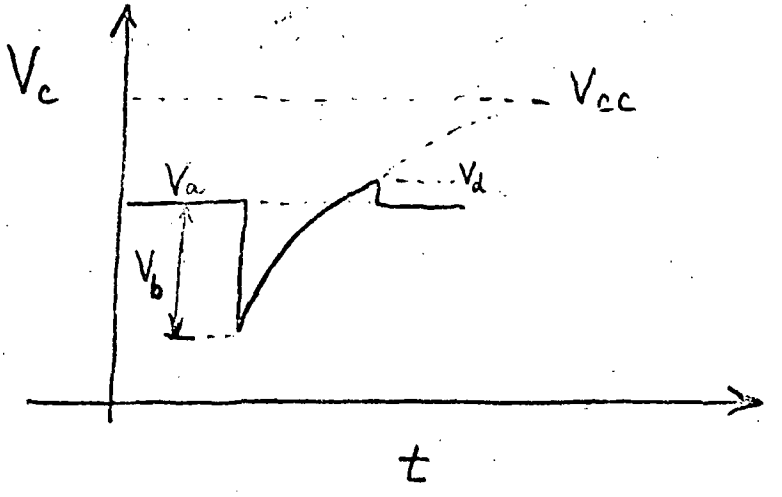


Figure F-2

Therefore,

$$(1 + \beta)R_E >> h_{ie}$$

$$243k >> 20.6k$$

2. Effect of Changes of V_C on T

The general waveform for the voltage on the charging capacitor of a monostable multivibrator is shown in Figure F-2. Equation 1 represents the pulse width, T, of the one-shot corresponding to this waveform.

$$T = \tau \ln \left(\frac{V_{CC} + V_B - V_A}{V_{CC} - V_D} \right) \qquad (1)$$

This waveform is the same as V_C

where

$$V_A = 2V,\ V_B = 1V,\ V_D = V_A + 0.5 = 2.5$$

and

$$V_{CC} = 4.51V.$$

substituting these values into equation 1 yields:

$$T = \tau \ln \frac{5.51 - V_A}{4.01 - V_A} = \tau \ln \frac{3.51}{2.01} = \tau \ln 1.75 = 0.56\tau$$

If V_A (V_C) increases by 8.0%:

$$T = \tau \ln \frac{5.51 - 2.16}{4.01 - 2.16} = \tau \ln \frac{3.35}{1.85} = 0.594\tau$$

$$\% \text{ change in } T = \left(\frac{0.594}{0.56} - 1 \right) 100 = 6\%$$

If $V_A(V_C)$ decreases by 4.6%:

$$T = \tau \ln \frac{5.51 - 1.91}{4.01 - 1.91} = \tau \ln \frac{3.6}{2.1} = 0.54\tau$$

$$\% \text{ change in } T = \left(1 - \frac{0.54}{0.56}\right) 100 = 3.5\%$$

3. Effect of Changes in I_C on T. -

An increase in I_C is analogous to a decrease in R_X, thus for an 11% increase in I_C:

$$T = 0.32\ (5.55 \times 0.89)\ 1 \times 10^5 \left[1 + \frac{0.7}{5.55 \times 0.89}\right] = 181$$

$$\% \text{ decrease in } T = \left(1 - \frac{181}{200}\right) 100 = 9.6\%$$

For a 14.3% decrease in I_C:

$$T = 0.32\ (5.55 \times 1.143)\ 1 \times 10^5 \left[1 + \frac{0.7}{5.55 \times 1.143}\right] = 226$$

$$\% \text{ increase in } T = \left(\frac{226}{200} - 1\right) 100 = 13\%$$

4. Effect of Changes in V_{VR4} on T. -

The following measurements were made on the breadboard model:

V_{VR4}	% Change V_{VR4}	T_{ms}	$\Delta T \mu s$	% Change ΔT
5.2	-7	195	5.6	-9.7
5.6	0	215	6.2	0
6.0	7	230	7.2	+16

The temperature drift of V_{VR4} is -0.7% and 0.98%.

Thus:

$$(\%\,\Delta T)V_{VR4} = \frac{9.7}{7}\ (0.7\%) = -0.97\%$$

$$(\%\,\Delta T)V_{VR4} = \frac{16}{7}\ (0.98) = 2.24\%$$

APPENDIX G

MULTIVIBRATOR DELAYED TURN ON ANALYSIS FOR TTL SN54124 AND CAPSTAN BRAKE DRIVER TRANSISTOR HEAT TRANSFER

APPENDIX G

1. TTL SN 54121 One-Shot Delayed Turn on Analysis. -

The turn on of a TTL S/N 54121 one-shot multivibrator can be delayed so as to fire on power turn-on, by adding the input network shown in Figure G-1. When V_{cc} is applied, the one-shot sees a "low" at pin 5 until the voltage across C charges to the "1" threshold (1.0 to 1.8 volts over 0°C to 60°C range). The turn-on time of the one-shot can only be calculated to lie somewhere within the extremes of two separate charging equations. The minimum charging time equation assumes that the input transistor of the one-shot is always in its active region until the one-shot fires (see Figure G-2). The maximum charging equation assumes that the charging network is isolated from the input transistor of the one-shot, (i.e., that the base-to-emitter diode is always reverse biased or turned off) as capacitor C charges (see Figure G-3). The true charging condition will always lie somewhere between these extremes; however, it is impossible to predict exactly where. A pure solution would require previous knowledge of the input base to emitter diode non-linearity.

The minimum charging time for Vb to rise to a logical "1" threshold and fire the one-shot, can be derived from the expression for Vb(t) which is,

$$Vb(t) = \frac{R_2 (R_1 + R_F) V_{cc}(t) - R_1 R_2 V_F}{R_1 R_F + R_1 R_2 + R_2 R_F} \left[1 - e^{- \frac{(R_1 R_F + R_1 R_2 + R_2 R_F)t}{R_1 R_2 C R_F}} \right] \quad (1)$$

where

$$Vcc(t) = Vcc \left[1 - e^{-500t} \right]$$ (assuming that Vcc rises from 0V to Vcc with an RC time constant of 2 milliseconds).

V_f = Forward base-emitter voltage drop within one-shot (see Figure G-2)

For $\overline{t}$, conditions are

$$\overline{Vcc}, \underline{V_f}, \underline{V_b}, \underline{C}, \underline{R_1}, \overline{R_2}, \underline{R_f}$$

For $\underline{t}$, conditions are

$$\underline{Vcc}, \overline{V_f}, \overline{V_b}, \overline{C}, \overline{R_1}, \underline{R_2}, \overline{R_f}$$

for A12-Z18 one-shot

$$R_1 = \begin{cases} 2210 \\ 2105 \end{cases} \text{ ohms}$$

$$R_2 = \begin{cases} 3226 \\ 3093 \end{cases} \text{ ohms}$$

$$Vcc = \begin{cases} 5.4 \\ 4.6 \end{cases} \text{ volts}$$

$$V_f = \begin{cases} 0.90 \text{ @ } 0°C \\ 0.56 \text{ @ } 60°C \end{cases} \text{ volts}$$

$$R_f = \begin{cases} 2100 \\ 1900 \end{cases}$$

$$C = \begin{cases} 5.66 \text{ uF @ } 0°C \\ 3.88 \text{ uF @ } 60°C \end{cases}$$

$$Vb = \begin{cases} 1.8V \text{ @ } 0°C \\ 1.0V \text{ @ } 60°C \end{cases}$$

Substituting constants into equation (1) and solving explicity for t we get,

$$1.9ms \leq t \leq 3.9ms \tag{2}$$

The maximum charging times for Vb to rise to a "1" threshold can be derived from the expression for Vb (t) derived with the aid of Figure G-3. This expression is,

$$Vb(t) = \frac{R_2 Vcc}{R_1 + R_2} \left[1 - e^{-500t}\right] \left[1 - e^{-t/REC}\right] \tag{3}$$

where

$$R_E = \frac{R_1 R_2}{R_1 + R_2}$$

for t, conditions are

$$\overline{R_2}, \overline{Vcc}, \underline{R_1}, \underline{RE}, \underline{C}$$

for E, conditions are

$$\underline{R_2}, \underline{Vcc}, \overline{R_1}, \overline{RE}, \overline{C}$$

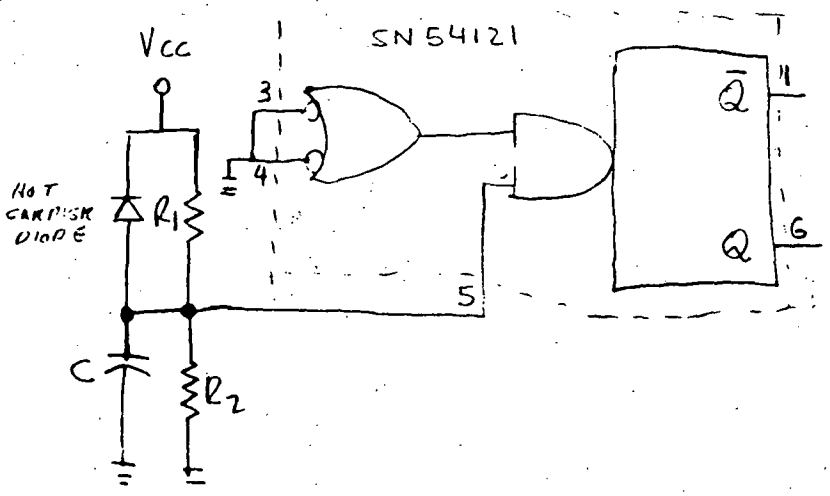


Figure G-1. Input Network

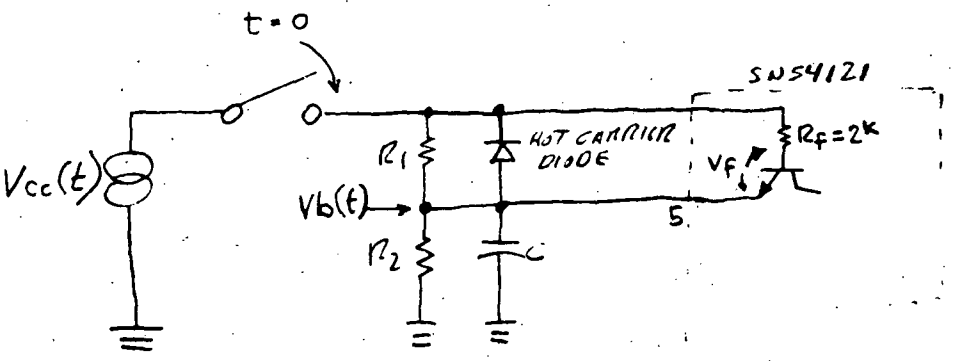


Figure G-2. Minimum Charging Time Network

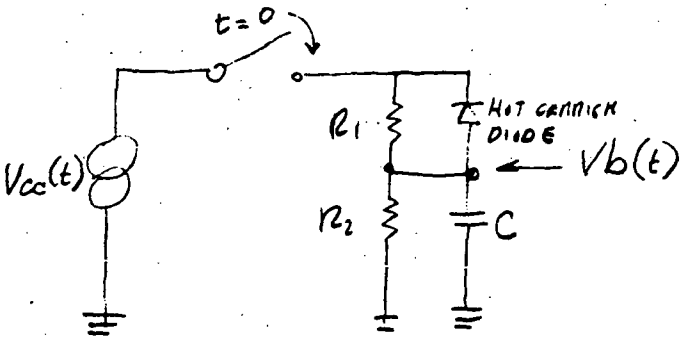


Figure G-3. Maximum Charging Time Network

Substituting constants into equation (3) and solving for t we get,

$$2.75\text{ms} \leqq t \leqq 7.9\text{ms} \tag{4}$$

Utilizing the results of (2) and (4) then, the time required to fire Z18 from power turn on is expressed as Td where, over worst case extremes,

$$1.9\text{ms} \leqq Td \leqq 7.9\text{ms} \tag{5}$$

2. Analysis of TTL SN54121 One-Shot Delay Shortening as a Function of Trigger Time After Power Turn-on. -

If Vcc is applied to the HW and Iω Start/Run timer as a step function (see Figure G-4), external timing capacitors C4 and C5 will charge to Vcc-Vf, where Vf is a saturated forward base-to-emitter voltage drop. When Vcc is applied, the positive terminals of the charging capacitors will charge to +3.5 volts via the dotted line path shown in Figure G-5. At this point Q1 will be turned off, and charging will continue to the final voltage of Vcc-Vf via the dot and dashed path shown.

While the timing capacitors are charging from 0 to +3.5 volts, the series charging resistance may be given as RT where, from Figure G-5,

$$R_T = \frac{R_{o1} \times 530}{530 + R_{01}} + 80 + Rd \tag{1}$$

where

R_{o1} is the emitter output impedance of Q1 (Given by the manufacturer as 70 ohms).[1]

Rd is the dynamic forward resistance of the Q2 base-to-emitter diode.

With regard to equation (1), the tolerance of the 80 ohm resistor will be no worse that of the internal timing resistor, which is given by the manufacturer as +3% at 60°C. If this figure is allowed to double to 6%, so as to take aging into consideration, the maximum value of the 80 ohm resistor will be approximately 85 ohms.

---

[1] This is a reasonable figure based on minimum h_{FE} considerations.

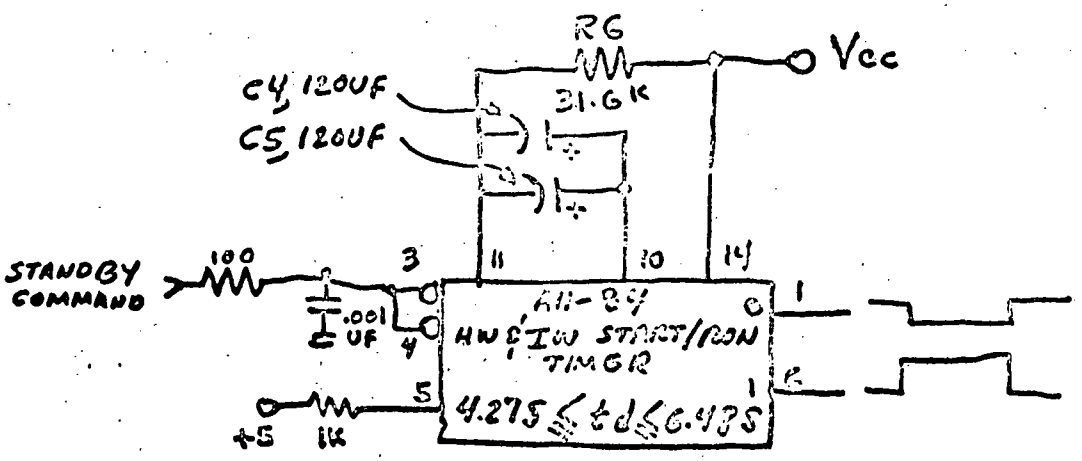


Figure G-4.

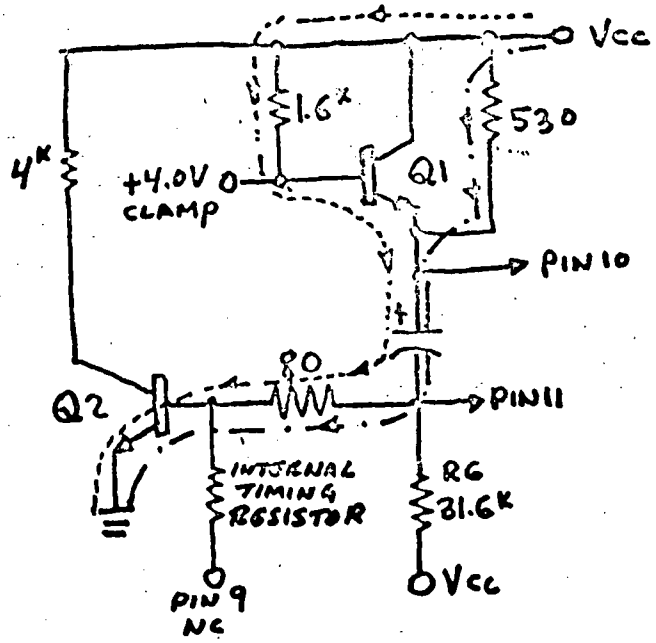


Figure G-5.

It is difficult to predict the dynamic resistance of the base-to-emitter junction of Q2. However, realizing that Q2 is in saturation should enable one to employ the simple diode equation:

$$\overline{Rd} \approx \frac{kT}{q} \cdot \frac{1}{Ie} \qquad (2)$$

$$\approx 0.0286 \cdot \frac{1}{Ie} \text{ @ } 60°C$$

where,

$$\underline{Ie} = \frac{\underline{Vcc} - \overline{VCE(SAT)}}{\overline{R_L}}$$

$$= \frac{4.6 - 0.2^*}{4640}$$

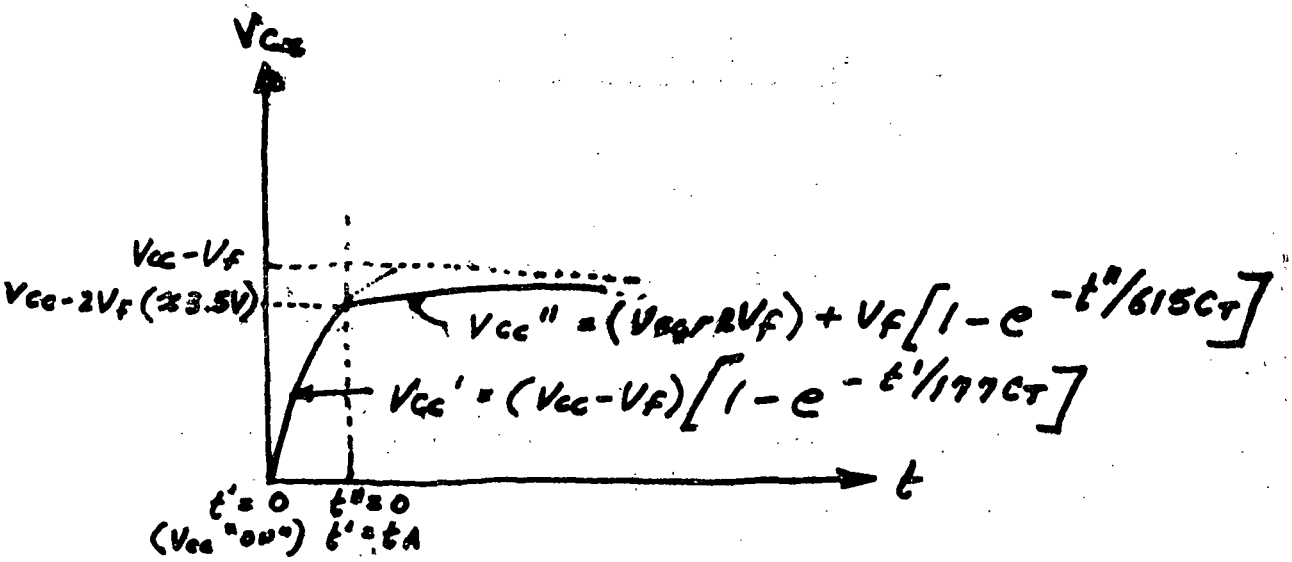
$$= 0.95 \text{ mA}$$

Substituting this value into equation (2) yields Rd = 30 ohms.

If all resistance constants are applied to equation (1), then

$$R_T = 62 + 85 + 30 = 177 \text{ ohms}$$

Thus, for the 0 to +3.5 volt region (with Vcc = 5.0 volts), Ct is charging through a maximum series resistance of approximately 177 ohms. From 3.5 volts to Vcc-Vf, C_T is charging through a maximum series resistance of 500 + 85 + 30, or 615 ohms. The pre-firing charging sequence for C_T is then as shown in Figure G-6 below.

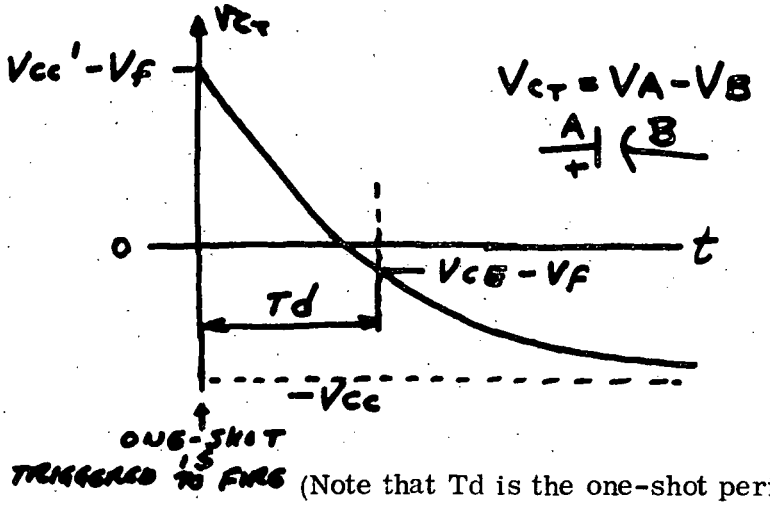


The equations shown assume that Vcc is applied as a step function. Actually it rises linearly in 2 ms. Since 2ms << the charging time of C_T, the step function assumption is valid.

Figure G-6.

*From typical curves

If the Vcc'' charging equation shown in Figure G-6 is ignored, and it is assumed that charging takes place solely via the Vcc' equation, the firing of the one-shot causes the timing capacitance C_T to charge as shown in Figure G-7.



(Note that Td is the one-shot period.)

Figure G-7.

For any capacitor charging between limits of V (initial) to V (final),

$$V_{C_T} = V\,(\text{Final}) - [V\,(\text{Final}) - V\,(\text{Initial})]\, e^{-t/R_T C_T} \tag{3}$$

From Figure G-3

$$V\,(\text{final}) = -Vcc \tag{4}$$

$$V\,(\text{initial}) = Vcc' - V_f \tag{5}$$

substituting (4) and (5) into (3),

$$V_{C_T} = -Vcc - (V_f - Vcc - Vcc')\left[e^{-t/R_T C_T}\right] \tag{6}$$

If firing occurs in the interval $0 \leqq t \leqq t_A$ (see Figure G-6),

$$Vcc' = (Vcc - V_f)\left[1 - e^{-t'/177 C_T}\right] \tag{7}$$

Substituting equation (7) into equation (6),

$$V_{C_T} = -Vcc - \left[V_f - Vcc - (Vcc - V_f) \left[1 - e^{-t'/177C_T} \right] \right] C^{-t/R_T C} \quad (8)$$

Where

t' = time from t = 0 until one-shot fires.

t = Capacitor discharge time starting from time at which the one-shot fires.

With respect to Figure G-7, it will be noted that the one-shot time delay expires when

$$Vc = Vce - Vf$$

Where,

$$\left.\begin{aligned} Vf &= Vbe\ (Sat) \\ Vce &= Vce\ (Sat) \end{aligned}\right\} \text{Of transistors within the integrated circuit.}$$

It is assumed that VCE << Vf, and that td >> t', then substitution into equation (8) yields

$$-V_f = -Vcc - \left[V_f - Vcc - (Vcc - V_f) \left[1 - e^{-t'/177C_T} \right] \right] e^{-td/R_T C_T} \quad (9)$$

where

td = Actual one-shot time delay.

Solving equation (9) for td in terms of t' yields,

$$td = R_T C_T \, Ln \left[2 - e^{-t'/177C_T} \right]^1 \quad (10)$$

If we return to consideration of the HW and Iω Start/Run timer specifically, and assume three cases--i.e., $\overline{C_T R_T}$, $C_T RT$ and CTRT (nominal) it will be possible to obtained three plots of td vs t' using equation (10) above.

---

[1] Note the similarity between this equation and the one given by the manufacturer (which assumes that Ct is fully charged before firing). The equation given by the manufacturer is $td = R_T C_T \ln 2$.

Case I $\overline{(CTR_T)}$ $\overline{CT}$ - 290uF, $\overline{R_T}$ = 32,250 ohms

Solving equation (6) for t' = T_A (i.e., point at which Vcc' = Vcc-2V_f),

$$Vcc - 2V_f = (Vcc - V_f)\left[1 - e^{\frac{-T_A/177C_T}{177ct}}\right]$$

from which,

$$T_A = 177\, C_t\, Ln\left[\frac{Vcc - V_f}{V_f}\right] \qquad (11)$$

= 98.0 milliseconds

Thus T_A = 98 milliseconds establishes the maximum useable limit of the curve to be plotted for Case I. By substituting values for t' from 0 to 98 ms into equation (10), points are obtained for plotting the Case I curve shown in Figure G-8.

Case II C_TR_T C_T = 199 uF, RT = 31,000 ohms

T_A = 177 x 199 x 10-6 x 1.91 (Using equation 11)

= 67.2 ms

Assuming values for t' from 0 to 67.2 ms in equation (10) yields the Case II curve shown in Figure G-8.

Case III C_TR_T (Nominal) CT = 24uF, R_T = 31,600 ohms

T_A = 177 x 240 x 10-6 x 1.91 (using equation 11)

= 81 ms

Assuming values for t' from 0 to 81 ms in equation (10) yields the Case III curve shown in Figure G-8.

In order to substantiate the calculated curves, a typical randomly selected SN54121 chip was tested at room temperature in the laboratory. The results of these tests are shown by the dotted line plot in Figure G-8. Note that this plot closely approximates the nominal value curve (Case III).

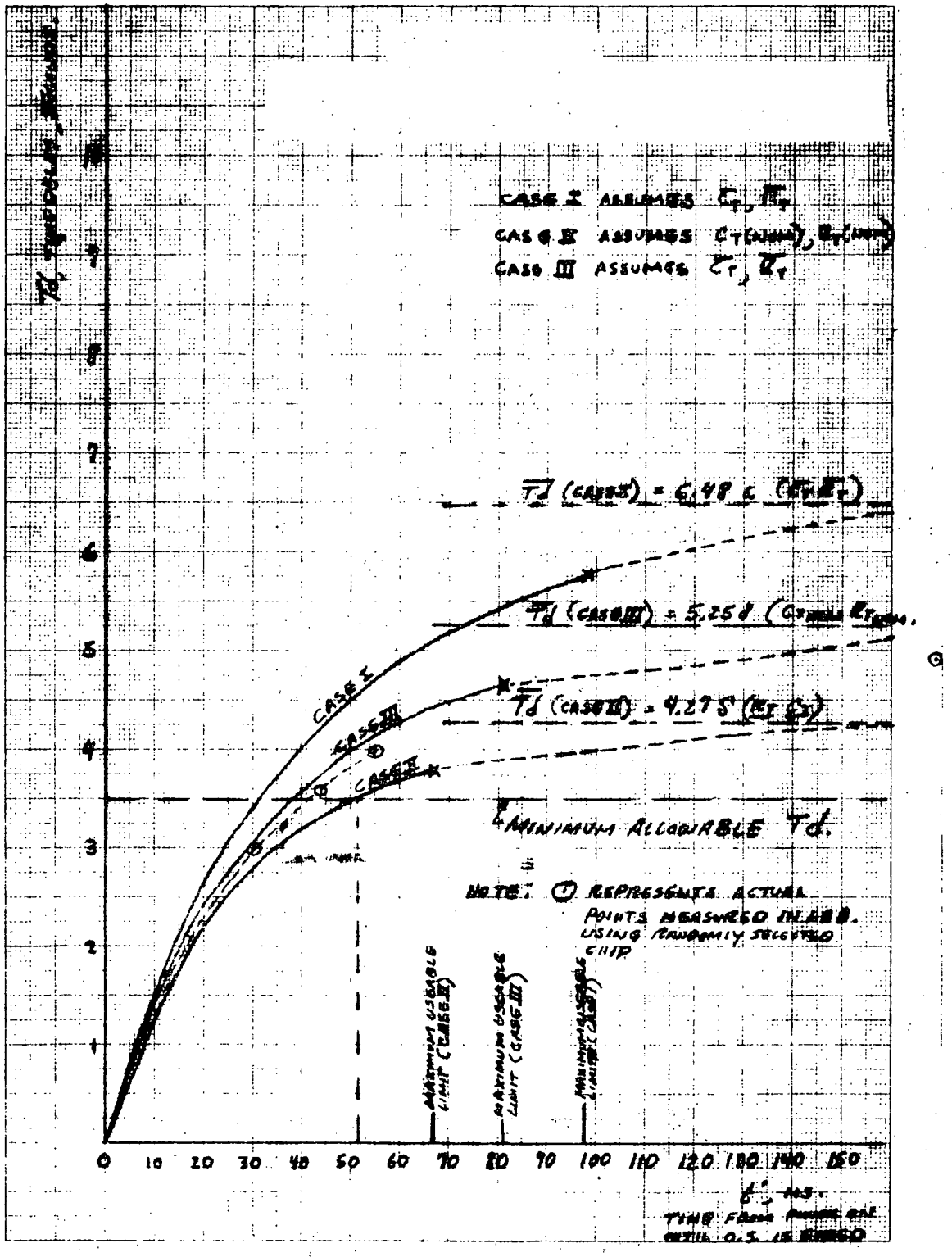


Figure G-8. TTL SN54121 Analysis (T_d vs. Trigger Time After Power On)

With respect to the curves shown in Figure G-8 it is apparent that, in order to guarantee a minimum time delay (T_d) of 3.5 seconds, the HW and Iω one-shot should not be fired until at least 52 milliseconds have elapsed after power turn-on. This 52 millisecond delay requirement establishes the minimum allowable period of power-on sub-sequence 3.

3. Analysis of Heat Transfer via Conduction for Capstan Brake Driver Transistor. -

a. Conductive Heat Transfer via Direct Contact between Transistor Base and Printed Circuit Ground Plane Copper (see Figure 4-158). - Since the collector of Q7 is at ground potential and inwardly connected to the transistor case, it would be possible to promote heat transfer via conduction by mounting the transistor flat on the copper clad printed circuit board -- leaving only clearance for the base and emitter leads (see Figure G-9).

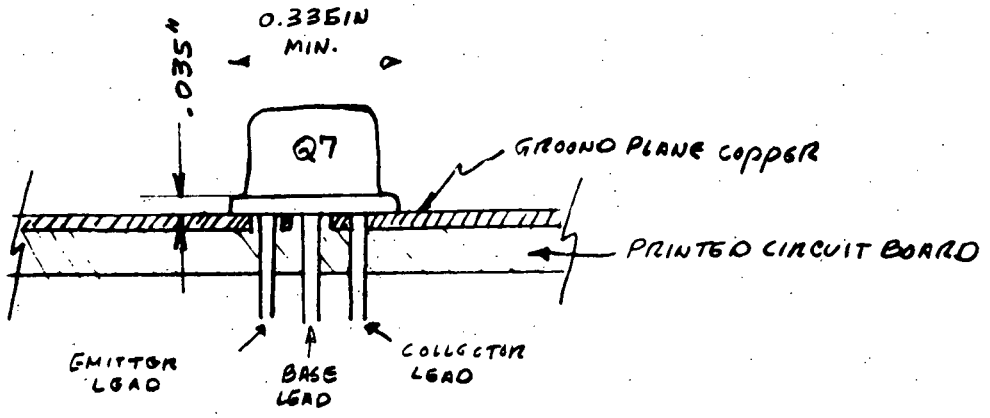


Figure G-9.

The area of contact between the transistor case and the ground plane, $A_{contact}$, is given by:

$$A_{contact} = A_{xsistor\ Base} - A_{clearance\ for\ base\ and\ emitter\ leads}$$

$$A_{xsistor\ Base} = (0.335)^2 = 0.088\ in^2$$

$$A_{clearance\ for\ base\ and\ emitter\ leads} = 2 \times \frac{(0.035)^2}{4} = 0.002\ in^2$$

Thus

$$A_{contact} = 0.088 - 0.002$$

$$= 0.086 \text{ in}^2$$

The length of the conduction path from junction to copper is 0.035 in. as shown in Figure G-9, and the thermal conductivity of the base material (KOVAR) is 0.494 watts/°C - IN. The thermal resistance can thus be calculated from the relation:

$$\theta_{CS} = \frac{\Delta L}{KA} \tag{1}$$

where

ΔL = 0.035 in.

A = Area of Contact = 0.086

K = Thermal Conductivity of Kovar

Thus

$$\theta_{CS} = \frac{0.035}{0.494 \times 0.086} \text{ °C/mW}$$

$$= 0.00082 \text{ °C/mW}$$

Using the relation,

$$T_J = T_S + \bar{P}\,\theta_{JS}$$

$$= T_S + \bar{P}\,(\theta_{JC} + \theta_{CS}) \tag{2}$$

where

T_J = Transistor Junction Temperature

T_S = Sink Temperature of Copper = 68°C (measured)

$\bar{P}$ = Maximum Dissipation of Capstan Brake Driver Transistor Q7, = 286 milliwatts

θ_{JC} = Thermal Resistance (junction to case), given as 0.0175°C/mW

θ_{CS} = Thermal Resistance (case to sink), calculated above as 0.0008°C/mW

Substitution of values yields a maximum junction temperature of 73.2°C. This temperature is well below 110°C, which is the allowable junction temperature.

b. Heat Transfer Via Thermally Conductive Polyurethane Adhesive. - Since the design of the printed circuit board on which the capstan brake driver is mounted has been finalized with Q7 separated from the cleared board via a transistor spacer (see Figure G-10), it would be possible to "sink" the transistor case simply via a thermally conductive adhesive.

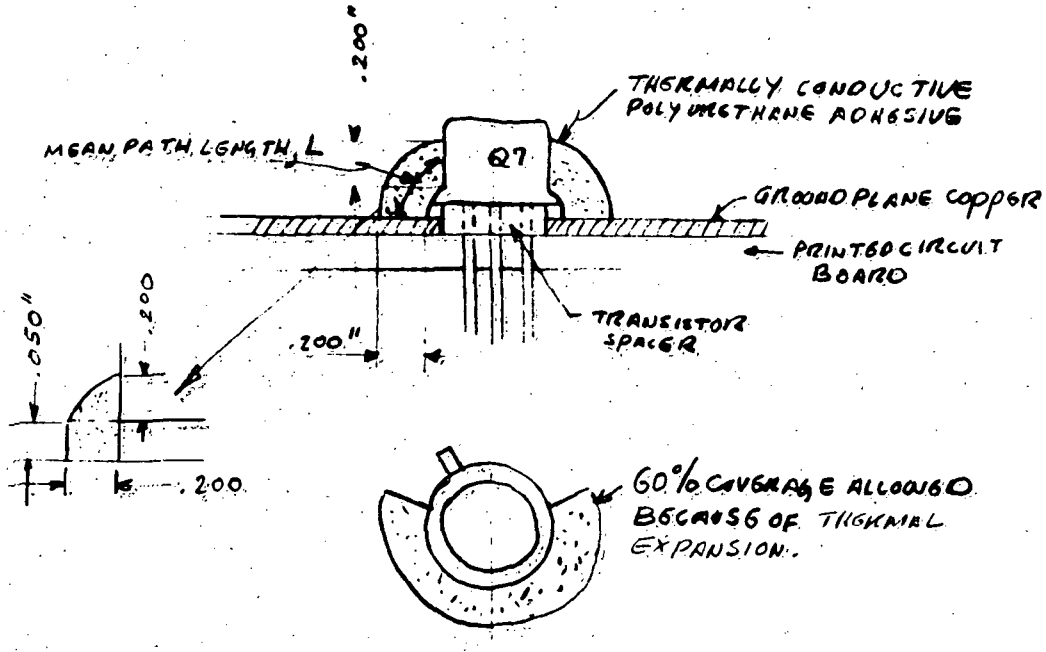


Figure G-10.

The area of contact between the adhesive and the transistor case is A_C, where,

$$A_C = 0.6\pi\,(0.305) \times 0.200$$

$$= 0.115 \text{ in}^2$$

The effective length of the path between the case and the copper ground plane is the mean path length L, where, with reference to the exploded view in Figure G-10,

$$L = 0.05 + \frac{\pi \times 0.200}{4}$$

$$= 0.05 + 0.157$$

$$= 0.207 \text{ in}$$

Thus,

$$\theta_{CS}^{1} = \frac{L}{KA} = \frac{0.207}{0.0128 \times 0.115} = 0.141 \text{ °C/mW}$$

where

L = 0.207 in

A = 0.115 in^2

K = Thermal conductivity of adhesive = 0.0128 watts/°C in.

θ_{CS}' = Thermal resistance of adhesive path

and

$$\theta_{CS}'' = \frac{L'}{K' A'} = \frac{0.125}{0.494 \times 2 \times 10^{-4}} = 1.27 \text{ °C/mW}$$

where

L' = length of transistor collector lead = 0.125 in

A' = cross sectional area of collector lead = 2×10^{-4} in^2

K = Thermal conductivity of lead = 0.494 watts/°C in

θ_{CS}'' = Thermal resistance of collector lead soldered to ground plane

Thus, there are two paths in parallel and the total effective thermal resistance is θ_{CS}, where

$$\theta_{CS} = \frac{\theta_{CS}' \theta_{CS}''}{\theta_{CS}' + \theta_{CS}''}$$

$$= 0.127 \text{ °C/mW}$$

The total thermal resistance of conduction is therefore

$$\theta_{JS} = \theta_{JC} + \theta_{CS}$$

$$= 0.0175 + 0.127$$

$$0.144 \text{ °C/mW}$$

The final junction temperature will then be

$$T_J = T_S + \bar{P} \theta_{JS}$$

$$= 68 + 286 \times 0.144$$

$$= 109.2°C$$

Thus, if the adhesive coverage is made as shown in Figure G-10, the maximum allowable transistor junction temperature will not be reached.

Recommended Component Changes. -

a. Sync Speed Detector Module (A9)

Change:	C4	from CK06BX105K	Capacitor, Cer., 1 uf ± 10%, 50V
		to CK06BX684K	Capacitor, Cer., 68 uF ± 10%, 50V
	C6	from 8150547-41	Capacitor, Tant., 4.7uF ± 10%, 50V
		to 8150547-17	Capacitor, Tant., 12 uF ± 10%, 25V
	C9	from CKR06BX103KP	Capacitor, Cer., 0.01 uf ± 10%, 100V
		to CKRo5BX102KP	Capacitor, Cer., 0.001 uF ± 10%, 100V
	C10	from CSR13C396KP	Capacitor, Tant., 39 uF ± 10%,10V

Change:		to	KG39J10KPS (KGMGT)	Capacitor, Tant., 39 uF ± 5%, 10V
	C13	from	8150547-16	Capacitor, Tant., 82 uF ± 10%, 15V
		to	T230C826J015PS (KGMGT)	Capacitor, Tant., 82 uF ± 5%, 15V
	C14, C15	from	8150547-11	Capacitor, Tant., 18 uF ± 10%, 15V
		to	T230B186J015PS(KGMGT)	Capacitor, Tant., 18uF ± 5%, 15V
	C23	from	CSR13D186KP	Capacitor, Tant., 18 uF ± 10% 15V
		to	KG18J15DPS(KGMGT)	Capacitor, Tant., 19 uF ± 5%, 15V
	R3	from	RCR07GF472JP	Resistor, Comp., 4.7k ± 5%, 1/4W
		to	RCR07GF473JP	Resistor, Comp., 47k ± 5%, 1/4W
	R5	from	RNR55C2002FP	Resistor, Film, 20.0k ± 1%, 1/10W
		to	RNR55C1472FP	Resistor, Film, 14.7k ± 1%, 1/10W
	R7	from	RNR55C2372FP	Resistor, Film, 23.7k ± 1%, 1/10W
		to	RNR55C3482FP	Resistor, Film, 348k ± 1%, 1/10W
	R10	from	RCR07GF102JP	Resistor, Comp., 1k ± 5%, 1/4W
		to	RCR20GF122JP	Resistor, Comp., 1.2k ± 5%, 1/2W
	R11	from	RCR07GF333JP	Resistor, Comp. 33k ± 5%, 1/4W
		to	RNR55C2372FP	Resistor, Film, 23.7k ± 1%, 1/10W

Change:	R12	from	RCR07GF103JP	Resistor, Comp., 10k ± 5%, 1/4W
		to	RNR55C3161FP	Resistor, Film, 3.16k ± 1%, 1/10W
	R13	from	RCR07GF104JP	Resistor, Comp., 100k ± 5%, 1/4W
		to	RNR55C3162FP	Resistor, Film, 31.6k ± 1%, 1/10W
	R16	from	RCR07GF103JP	Resistor, Comp., 10k ± 5%, 1/4W
		to	RNR55C8251FP	Resistor, Film, 8.25k ± 1%, 1/10W
	R17	from	RCR07GF332JP	Resistor, Comp., 3.3k ± 5%, 1/4W
		to	RNR07GF102JP	Resistor, Comp., 1k ± 5%, 1/4W
	R21, R22, R24, R28, R30	from	RCR07GF472JP	Resistor, Comp, 4.7k ± 5%, 1/4W
		to	RNR55C3481FP	Resistor, Film, 3.48k ± 1%, 1/10W
	R40	from	RCR07GF472JP	Resistor, Comp., 4.7k ± 5%, 1/4W
		to	RNR55C4221FP	Resistor, Film, 4.22k ± 1%, 1/10W
	VR1	from	JANTX1N753Z	Diode, Zener 6.2V
		to	JANTX1N756A	Diode, Zener 8.2V

b. Control Module (ALL)

Change:	C4, C5	from	CSR13C127KP	Capacitor, Tant,. 120 uF ± 10%, 10V
		to	KG120J10DPS(KEMGT)	Capacitor, Tant., 120 uF ± 5%, 10V
	C10	from	CSR13B186KP	Capacitor, Tant., 18 uF ± 10%, 15V
		to	KG18J15DPS(KGMGT)	Capacitor, Tant., 18 uF ± 5%, 15V

Change:	R4, R5, R7	from	RCR07GF472JP	Resistor, Comp., 4.7k ± 5%, 1/4W
	R11, R12, R15	to	RNR55C3481FP	Resistor, Film, 3.48k ± 1%, 1/10W
	R10	from	RCR07GF472JP	Resistor, Comp., 4.7k ± 5%, 1/4W
		to	RCR07GF153JP	Resistor, Comp., 15k ± 5%, 1/4W

c. Cycler Module (R12)

Change:	C10	from	815054741	Capacitor, Tant., 4.7 uF ± 5%, 50V
		to	T230B475J0500PS(KGMGT)	Capacitor, Tant., 4.7 uF ± 5%, 50V
	C11	from	CSR13C826KP	Capacitor, Tant., 82 uF ± 10%, 10V
		to	KG82J10DPS(KGMGT)	Capacitor, Tant., 82 uF ± 5%, 10V
	R15	from	RCR07GF103JP	Resistor, Comp., 10k ± 5%, 1/4W
		to	RNR55C1002FP	Resistor, Film, 10k ± 1%, 1/10W
	R28	from	RNR55C3012FP	Resistor, Film, 30.1k ± 1%, 1/10W
		to	RNR55C3162FP	Resistor, Film, 31.6k ± 1%, 1/10W
	R29	from	RCR07GF472JP	Resistor, Comp., 4.7k ± 5%, 1/4W
		to	RNR55C4641FP	Resistor, Film, 4.64k ± 1%, 1/10W
	R30	from	RCR07GF103JP	Resistor, Comp., 10k ± 5%, 1/4W
		to	RCR07GF562JP	Resistor, Comp., 5.6k ± 5%, 1/4W

Change:	R31	from	RCR07GF102JP	Resistor, Comp., 1k ± 5%, 1/4W
		to	RNR55C2151FP	Resistor, Film, 2.15k ± 10%, 1/10W
	R34	from	RCR07GF473JP	Resistor, Comp., 47k ± 5%, 1/4W
		to	RNR55C1002FP	Resistor, Film, 10k ± 1%, 1/10W
	R35	from	RCR07GF472JP	Resistor, Comp., 4.7k ± 5%, 1/4W
		to	RNR55C1961FP	Resistor, Film, 1.96k ± 1%, 1/10W
	R37	from	RCR07GF272JP	Resistor, Comp., 2.7k ± 5%, 1/4W
		to	RNR55C2611FP	Resistor, Film, 2.61k ± 1%, 1/10W
	R38	from	RCR07GF223JP	Resistor, Comp., 22k ± 5%, 1/4W
		to	RNR55C2612FP	Resistor, Film, 26.1k ± 1%, 1/10W
	R39	from	RCR07GF472JP	Resistor, Comp., 4.7k ± 5%, 1/4W
		to	RNR55C1002FP	Resistor, Film, 10k ± 1%, 1/10W
	R40	from	RCR07GF102JP	Resistor, Comp., 1k 6 5%, 1/4W
		to	RNR55C6811FP	Resistor, Film, 6.81k ± 1%, 1/10W
	R42	from	RCR07GF223JP	Resistor, Comp., 22k ± 5%, 1/4W
		to	RNR55C2152FP	Resistor, Film, 21.5k ± 1%, 1/10W
	R43	from	RNR55C2152FP	Resistor, Film, 21.5k ± 1%, 1/10W
		to	RCR07GF752JP	Resistor, Comp., 7.5k ± 5%, 1/4W

Change:	R45	from	RCR07GF103JP	Resistor, Comp., 10k ± 5%, 1/4W
		to	RCR07GF392JP	Resistor, Comp., 3.9k ± 5%, 1/4W
	R47	from	RCR07GF102JP	Resistor, Comp., 1k ± 5%, 1/4W
		to	RNR55C3161FP	Resistor, Film, 3.16k ± 1%, 1/10W
	R49	from	RCR07GF103JP	Resistor, Comp., 10k ± 5%, 1/4W
		to	RNR55C1002FP	Resistor, Film, 10k ± 1%, 1/10W
	R50	from	RCR07GF153JP	Resistor, Comp., 15k ± 5%, 1/4W
		to	RNR55C1472FP	Resistor, Film, 14.7k ± 1%, 1/10W
	R51	from	RCR07GF472JP	Resistor, Comp., 4.7k ± 5%, 1/4W
		to	RNR55C2371FP	Resistor, Film, 2.37k ± 1%, 1/10W

4. Command Module (A13)

Change:	C15	from	8150547-22	Capacitor, Tant., 8.2 uF ± 10%, 35V
		to	T230B825J035PS(KGMGT)	Capacitor, Tant., 8.2 uF ± 5%, 35V
	C17	from	CKR06BX104KP	Capacitor, Cer., 0.1 uF ± 10%, 100V
		to	CKR05BX103KP	Capacitor, Cer., 0.01 uF ± 10%, 100V
	C18, C14	from	8150547-20	Capacitor, Tant., 47 uF ± 10%, 25V
		to	T230C476J025PS	Capacitor, Tant., 47 uF ± 5%, 25V

Change:	C19	from	8150547-7	Capacitor, Tant., 39 uF ± 10%, 10V
		to	T230B396J010PS	Capacitor, Tant., 39 uF ± 5%, 10V
	R1	from	RCR079F103JP	Resistor, Comp., 10k ± 5%, 1/4W
		to	RNR55C6811FP	Resistor, Film, 6.81k ± 1%, 1/10W
	R41	from	RNR55C7501FP	Resistor, Film, 7.5k ± 1%, 1/10W
		to	RNR55C1102FP	Resistor, Film, 11k ± 1%, 1/10W
	R54	from	RCR07GF972JP	Resistor, Comp., 4.7k ± 5%, 1/4W
		to	RNR55C3481FP	Resistor, Film, 3.48k ± 1%, 1/10W
	R56	from	RCR079F330JP	Resistor, Comp., 33 OHMS ± 5%, 1/4W
		to	RCR079F271JP	Resistor, Comp., 270 OHMS ± 5%, 1/4W

APPENDIX H

WORST CASE ANALYSIS CRITERIA SUMMARY

1. Introduction

The ERTS Wideband Video Tape Recorder (VTR) electronic circuits have been analyzed based on the system working environments, operating life and storage requirements. Selection of the critical circuit elements to be analyzed depended primarily upon engineering judgment, taking into account the basic circuit function in relation to overall system performance specifications.

Applicable Mil Specs were used in the determination of worst case component tolerances. In presenting the analysis final report, standard symbols and recommended IEEE abbreviations have been used.

1.1 List of Symbols

The symbols given below are those generally accepted by the electronics and electrical industries. A more detailed listing appears in MIL-S-19500E, Appendix B.

1.1.1 Transistor Symbols. -

BV	Breakdown voltage
NF	Noise figure
Rg	Internal resistance of the generator
T_A	Ambient temperature
T_C	Case temperature
t_d	Delay time
t_f	Fall time
T_J	Junction temperature
t_{off}	Turn-off time
t_{on}	Turn-on time ($tr + t_d$)
T_{op}	Operating temperature
t_p	Pulse time
t_r	Rise time
t_s	Storage time
T_{sig}	Storage temperature
Δ	(Delta) An increment of change in the value of the indicated variable
B, b	Base terminal
BV_{CBO} ...	Breakdown voltage, collector to base, emitter open

BV_{CEO} . . . . Breakdown voltage, collector to emitter, base open

$BV_{CEO(sus)}$ . . Breakdown voltage, collector to emitter, sustained

BV_{CER} . . . . . Breakdown voltage, collector to emitter, with specified resistance between base and emitter

BV_{CES} . . . . . Breakdown voltage, collector to emitter, with base short-circuited to emitter

BV_{CEX} . . . . . Breakdown voltage, collector to emitter, with specified circuit between base and emitter

BV_{EBO} . . . . Breakdown voltage, emitter to base, collector open

C, c . . . . . Collector terminal

C_{ibs} . . . . . Input capacitance (common base), output short circuited

C_{ibo} . . . . . Input capacitance (common base), output open-circuited

C_{ies} . . . . . Input capacitance (common emitter), output short circuited

C_{obo} . . . . . Output capacitance (common base), input open circuited

E, e . . . . . Emitter terminal

I_{hib}, $I_{\infty b}$ . . . . Small-signal short-circuit forward-current transfer-ratio cutoff frequency (common base)

f_{hfe}, $f_{\infty e}$ . . . . Small-signal short-circuit forward-current transfer-ratio cutoff frequency (common emitter)

f_{max} . . . . . Maximum frequency of oscillation

f_t . . . . . Extrapolated unity gain frequency (gain bandwidth product)

g_{ME} . . . . . Static transconductance (common emitter)

g_{mc} . . . . . Small-signal transconductance (common emitter)

G_{PB} . . . . . Large-signal average power gain (common base)

G_{pb} . . . . . Small-signal average power gain (common base)

G_{PE} . . . . . Large-signal average power gain (common emitter)

G_{pe} . . . . . Small-signal average power gain (common emitter)

h_{FB} . . . . . Static value of the forward current transfer ratio (common base)

h_{ib} . . . . . Small-signal short-circuit forward-current transfer ratio (common base)

h_{FE} . . . . . Static value of the forward current transfer ratio (common emitter)

h_{fe} . . . . . Small-signal short-circuit forward current transfer ratio (common emitter)

$|h_{fe}|$ . . . . . Magnitude of common-emitter small-signal short-circuit forward-current transfer ratio

h_{ib} . . . . . Small-signal value of the short-circuit input impedance (common base)

h_{ie}	Small-signal value of the short-circuit input impedance (common emitter)
h_{ob}	Small-signal value of the open-circuit output admittance (common base)
h_{oe}	Small-signal value of the open-circuit output admittance (common emitter)
h_{rb}	Small-signal open-circuit reverse-voltage transfer ratio (common base)
h_{re}	Small-signal open-circuit reverse-voltage transfer ratio (common emitter)
I_B	Base current (d.c.)
i_b	Base current (instantaneous)
I_C	Collector current (d.c.)
i_c	Collector current (instantaneous)
I_{CBO}	Collector cutoff current (d.c.), emitter open
I_{CEO}	Collector cutoff current (d.c.), base open
I_{CER}	Collector cutoff current (d.c.), with specified resistance between base and emitter
I_{CEX}	Collector cutoff current (d.c.) with specified circuit between base and emitter
I_{CES}	Collector cutoff current (d.c.), with base short-circuited to emitter
I_E	Emitter current (d.c.)
I_{EBO}	Emitter cutoff current (d.c.), collector open
P_C	Collector power dissipation
P_T	Total power dissipation
R_B	External base resistance
r_b	Base spreading resistance
R_C	External collector resistance
$r_{CE}(sat)$	Collector to emitter saturation resistance
R_E	External emitter resistance
R_{Ehie}	Real part of the small-signal short-circuit input impedance
Rg	Generator resistance
V_{BE}	Base to emitter voltage (d.c.)
$V_{BE}(sat)$	Base to emitter saturation voltage
V_{CB}	Collector to base voltage (d.c.)

V_{CBF}	D.c. open-circuit voltage (floating potential) between the collector and base, with the emitter biased in the reverse direction with respect to the base
V_{CBO}	Collector to base voltage (static), emitter open
V_{CE}	Collector to emitter voltage (d.c.)
V_{CEO}	Collector to emitter voltage (static), base open
V_{ce}	Collector to emitter voltage (r.m.s.)
v_{ce}	Collector to emitter voltage (instaneous)
$V_{CE}(sat)$	Collector to emitter saturation voltage
V_{CER}	Collector to emitter reverse voltage
V_{EB}	Emitter to base voltage (d.c.)
V_{eb}	Emitter to base voltage (r.m.s.)
v_{eb}	Emitter to base voltage (instantaneous)
V_{EBF}	D.c. open-circuit voltage (floating potential) between the emitter and base, with the collector biased in the reverse direction with respect to the base.
V_{EBO}	Emitter to base voltage (static), collector open
V_{EC}	Emitter to collector voltage (d.c.)
V_{ECF}	D.c. open-circuit voltage (floating potential) between the emitter and collector, with the base biased in the reverse direction with respect to the collector
V_{RT}	Reach through voltage
θ	Thermal resistance
θ_{J-A}	Thermal resistance, junction to ambient
θ_{J-C}	Thermal resistance, junction to case

1.1.2 Diode Symbols -

Breakdown Voltage Regulation (ΔBV). - The breakdown voltage between two specified values of reverse current measured in the breakdown region of the V-I characteristic.

Forward Current (I_F). - Forward current is the current that flows through the semiconductor diode in the forward direction.

Forward Direction. - The forward direction is the direction of easy current flow (conventional) through the semiconductor diode.

Forward Voltage (V_F). - Forward voltage is the voltage drop which results from the flow of forward current through the semiconductor diode.

Large-signal Breakdown Impedance (BZ). - The large-signal breakdown impedance is the ratio of the change in breakdown voltage (ΔBV) to the corresponding change in reverse current (ΔI_R).

Large-signal Forward Impedance (Z_F). - The large-signal forward impedance is the ratio of the change in forward voltage (ΔV_F) to the corresponding change in forward current (ΔI_F).

Limits, Major and Minor. - Several diode specifications use the concept of major and minor limits for certain parameters. While exceeding the minor limit is cause for unit and possible lot rejection, circuit design should be to major limits to reduce degradation effects.

Power Rectification Efficiency (PRE). - The power rectification efficiency is the ratio of the d.c. output power to the a.c. input power in the rectifier circuit specified in the detail specification.

Forward Recovery Time (i_{f_r}). - The forward recovery time of a diode is defined as that time measured between the instant of current reversal from reverse to forward and the instant at which the forward condition specified is reached.

Reverse Recovery Time (t_{rr}). - The reverse recovery time of a diode is defined as that time measured between the instant of current reversal from forward to reverse and the instant at which the specified reverse condition is reached.

Rectification Efficiency (RE). - The rectification efficiency is the ratio, expressed as a percentage, of the d.c. load voltage to the peak a.c. input voltage in a half-wave rectifier circuit.

Reverse Current (I_R). - The reverse current is the current which flows through a semiconductor diode under conditions of applied reverse voltage.

Reverse Direction. - The reverse direction is the direction of greater static resistance to conventional current flow through the semiconductor diode.

Reverse Voltage (V_R). - The reverse voltage is the voltage applied in the reverse direction to a semiconductor diode.

Saturation Current (I_s). - The saturation current is the d.c. reverse current which flows through the semiconductor diode under the reverse voltage conditions specified in the detail specification (normally 80 percent, or less, of BV).

Small Signal Breakdown Impedance (bz). - Small signal breakdown impedance is the ratio of the a.c. voltage to the a.c. current in the breakdown voltage region of the V-I characteristic, under the test conditions specified.

Small Signal Forward Impedance (z_f). - The small signal forward impedance is the ratio of the a.c. voltage to the a.c. current in the forward bias region of the V-I characteristic, under the test conditions specified.

Temperature Coefficient of Breakdown Voltage (TCBV). - The temperature coefficient of breakdown voltage is the percentage change in breakdown voltage per degree centigrade rise in junction temperature of the semiconductor diode above the given junction temperature under the test conditions specified.

1.1.3 Coil Symbols. -

R_L - winding resistance

1.1.4 Supply Symbols. -

V_P = -24.5V primary

V_1 = +5.6V

V_2 = +8V

V_3 = -8V

V_4 = +22V

V_5 = -22V

1.2 Applicable Specifications

a. MILITARY

MIL-S-19500	Semiconductor Devices
MIL-R-11	Resistors, Fixed, Composition
MIL-R-26	Resistors, Fixed, Wirewound
MIL-R-93	Resistors, Fixed, Wirewound (Accurate)

MIL-R-10509	Resistors, Fixed, Film (High Stability)
MIL-R-11804	Resistors, Fixed, Film (Power Type)
MIL-R-18546	Resistors, Fixed, Wirewound Power
MIL-R-22097	Resistors, Variable Non Wirewound
MIL-R-22684	Resistors, Fixed, Film, Insulated
MIL-T-27	Transformers
MIL-R-27208	Resistors, Variable, Wirewound (Lead Screw)
MIL-R-55182	Resistors, Fixed, Film, Established Reliability
MIL-R-30095	Resistors, Fixed, Wirewound, (Accurate) Established Reliability
MIL-R-39007	Resistors, Fixed, Wirewound (Power Type) Established Reliability
MIL-R-39009	Resistors, Fixed, Wirewound, (Power Type Chassis Mt.), Established Reliability
MIL-R-39015	Resistors, Variable, Wirewound, (Lead Screw Act), Established Reliability
MIL-R-39017	Resistors, Fixed Film (Insulated) Established Reliability
MIL-C-17	Cables, Coaxial, RF
MIL-C-20	Capacitors, Fixed, Ceramic Dielectric (TC)
MIL-C-10950	Capacitors, Fixed, Mica Dielectric (Button)
MIL-C-11015	Capacitors, Fixed, Ceramic, Dielectric (Gen Purpose)
MIL-C-14409	Capacitors, Variable (Piston Type)
MIL-C-27287	Capacitors, Fixed, Plastic Dielectric

MIL-C-39001	Capacitors, Fixed, Mica Dielectric Established Reliability
MIL-C-39003	Capacitors, Fixed, Electrolytic, Tantalum, Solid-Electrolyte, Established Reliability
MIL-C-39006	Capacitors, Fixed, Electrolytic, (Non-solid electrolyte), Tantalum, Established Reliability
MIL-C-39014	Capacitors, Fixed, Ceramic Dielectric, (General Purpose), Established Reliability
MIL-C-55514	Capacitors, Fixed, Plastic for Metallized Plastic) Dielectric, Direct Current, In Non-Metallic Cases

b. RCA GCS

Preconditioning Requirements for Electronic Parts

1.3 Notation

a. Symbols including an n refer to specific part numbers. For example, I_{cn} is the collector current for Q_n.

b. An overline indicates a maximum limit ($\bar{I}_c$).

c. An underline indicates a minimum limit ($\underline{I}_c$).

2. General Specifications

2.1 ERTS System

2.1.1 Temperature. - The ERTS Transport Unit (pressurized) and Electronic Unit (vacuum) environmental temperature range is 0°C to +46°C. An additional 15°C internal temperature rise has been allowed due to radiant heat build-up; therefore, the minimum overall design range is 0°C to +61°C.

2.1.2 Aging. - Electrical component degradation due to aging is based on a one year orbital life and two year shelf life. In general, component degradation due to shelf life will be negligible if the system is stored at room temperature, and if temperature cycling is minimized.

Storage temperature is especially critical for Tantalum Foil Electrolytic Capacitors, where the recommended storage temperature with no voltage applied is -55°C to +40°C. A 10,000 hour lifetime (approximately 1.14 years continuous operation) has been used for component derating. When sufficient data is available, however, semiconductor end of life derating should be used. Since the actual VTR operating time will be much less than 10,000 hrs. this aging period is considered to be very conservative.

2.1.3 Primary Power. - The primary supply tolerances are summarized in Table H-1. The following primary power supply specifications are assumed to be measured at the VTR input connector. In other words, it is anticipated that line and relay contact losses are negligible, or will be compensated for at the spacecraft power source.

a. Steady State Operation. - The spacecraft power supply provides -24.5 ±2 percent regulated dc power. Peak current changes (including both increasing and decreasing currents) must conform to the minimum allowable rise time vs current step shown in Figure H-1. This is the minimum current rise time vs current step shown in Figure H-1. This is the minimum current rise time that can occur without a loss of regulation on the regulated power bus.

b. Failure Mode Operation. - Although the VTR is not expected to meet system performance specifications during a failure mode, no component degradation due to overvoltage or excessive power dissipation is permitted.

   1. Transients. - If a regulator malfunctions, the regulated bus voltage drops to the battery tap voltage (-18V) or rises as high as 39V during the time (≈ 35 ms) the redundant regulator is switched in.

   2. Steady State. - During a primary voltage regulator failure, the regulated bus voltage may shift to any level from -20 to -34.5 Vdc. These level changes may be long enough in duration that they must be considered steady state for purposes of component stress analysis.

2.1.4 Voltage Protection Circuit. - The system primary voltage variation is limited to -24.5 ±10% volts by the voltage protection circuit. To avoid unnecessary shutdown due to undervoltage transients, a delay of approximately 50-75 ms (worst case maximum is 321 ms) is permitted before the recorder is disconnected from the primary supply. During an overvoltage condition, however, the voltage protection circuit immediately disconnects the recorder from the power source; the only delay is due to a 12 ms maximum accumulation of relay activation times. In order to protect

TABLE H-1. PRIMARY AND CONVERTER POWER SUPPLY TOLERANCES

Item	Primary	DC Supplies		
Nominal Voltage	-24.5	+5.6	±8.0	±22.0
Operating Mode Characteristics:				
Initial Tolerance	±.5V	±0.3V	±0.5V	±1.0V
Temperature Tolerance (0° to 65°C)		±0.1V	±0.1V	±0.2V
Overall Voltage range	-25.0 to -24.0	5.2 - 6.0	7.4 - 3.6	20.8 - 23.2
Ripple - 20 kHz (pp)		50mV	50mV	50mV
Noise - 100 Hz to 1 MHz (pp)	250mV			
Feedback Voltage (pp)	50mV			
Allowable Current loading step 0-2A	0.01ms			
2-14A	1.4ms/A			
Failure Mode Characteristics[1]:				
Transient Voltage - 35 ms	18 - 39V	4	6	16
- 12 ms		7.4	13	36
Continuous at 35°C	20 - 34.5	4.7 - 6.5	6.7 - 9.3	19.1 - 25

[1] Failure Mode assumes Voltage Protection Circuit is Activated

the integrated circuits from this 12 rms overvoltage transient, a separate instantaneous acting circuit has been incorporated into the +5.6 Volt converter output. As a result, the +5.6V supply is limited to a maximum of 7.4V during all overvoltage conditions.

2.1.5 DC/DC Converter. - The DC/DC Converter output tolerances are summarized in Table H-1. The dc voltage allowable initial tolerances are approximately ±5% with 50 mVpp ripple. Except for the +5.6V supply, which is clamped at +7.4V, each supply may experience a transient up to 12 ms in duration at a peak of +56%, -25% of nominal voltage. Because of the voltage protection circuit in the continuous failure mode, the maximum continuous deviation for all supplies is ±10% of nominal voltage.

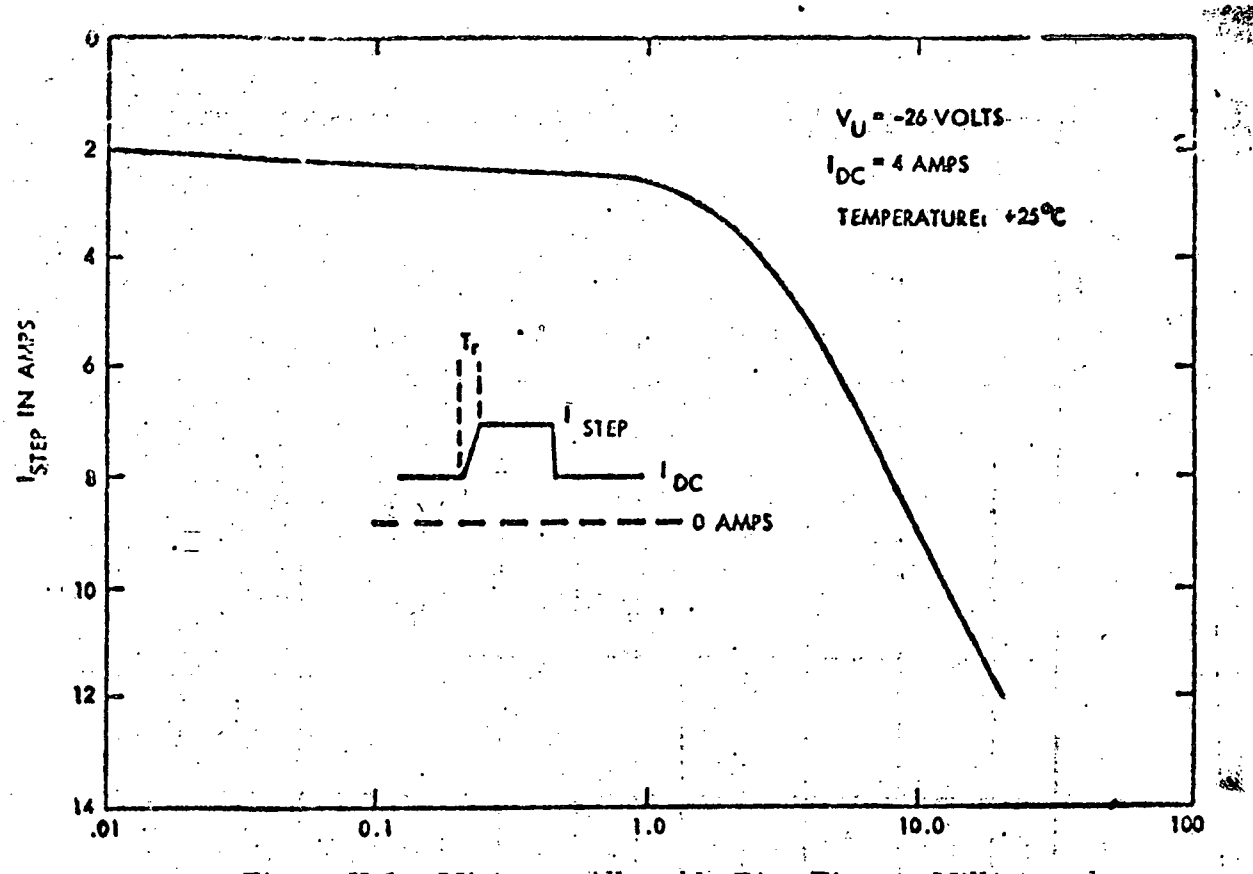


Figure H-1. Minimum Allowable Rise Time in Milliseconds

2.2 Component Derating Guidelines

Worst case component derating and degradation factors due to temperature and aging are based on RCA Defense and Spacecraft Standards, which satisfy the requirements of applicable Military Equipment Specifications. When non-approved parts are used, design limits are based on the manufacturer's specified initial limits with modifications to improve reliability as determined by engineering judgment of component specialists. The following guidelines take into account the additional power dissipation derating required in a zero atmosphere environment.

2.2.1 Resistors. - The power dissipated by a resistor, averaged over a 30 second period, shall not exceed 50 percent of its power ratings at the intended ambient temperature nor shall it be subjected to a voltage exceeding 80 percent of its maximum rated voltage for non-stacked resistors.

When two or more resistors are stacked vertically, the derating factors as shown will be multiplied by 0.8. When two or more resistors are stacked horizontally, the derating factors as shown will be multiplied by 0.6.

Fixed composition resistors with nickel weldable leads shall be derated further by a factor of 0.5.

Carbon Film	Maximum level of 50 percent of rated power.
Carbon Composition	Maximum level of 50 percent of rated power.
Metal Film	Maximum level of 50 percent of rated power.
Power Wirewound	Maximum level of 50 percent of rated power.
Precision Wirewound 1%	Maximum level of 50 percent of rated power.
Precision Wirewound 0.1%	Maximum level of 25 percent of rated power.
Precision Wirewound 0.5%	Maximum level of 35 percent of rated power.
Precision Wirewound 0.25%	Maximum level of 25 percent of rated power.
Precision Wirewound 0.05%	Maximum level of 25 percent of rated power.
Precision Wirewound 0.05%	Maximum level of 15 percent of rated power.

A summary of resistor derating factors, including transient operation, for the ERTS system environmental requirements is given in Table H-2.

2.2.2 Capacitors

Mica	Dipped - 50% of rated voltage (max.). Molded - 35% of rated voltage (max.).
Ceramic	Maximum level of 50 percent of rated voltage.
Mylar, Polystyrene Polycarbonate	Maximum level of 45 percent of rated voltage.

TABLE H-2. RESISTOR DERATING FACTORS

	Tolerance		Temperature Characteristics			Power Derating	Transient Overload			Failure Rate
	Initial	Initial Plus 10,000 hr Degrad.	R Range	0°C	60°C		Power Rating	Overload X Rated P	R Change	Per 10^6 hrs.
RCR07- -JP	±5%	±15%	RZ 1K	±2%	±2.2%	50%		6.2	±2.5%	1
			1.1K ≤ R ≤ 10K	±3.1%	±2.6%					
			11K ≤ R ≤ 0.1M	±4.1%	±3.3%					
			0.1M ≤ R ≤ 1M	±4.7%	±4.4%					
RWR- -FP	±1%	±1.8%			±0.05%	40%				1
RNR-XXC-FP -XXE-FP	±1%	±1.9%		±0.125%	±0.175%	50%	55, 57 60	5	±0.25%	1
	±1%	±1.9%		±0.063%	±0.88%		63 65	4	±0.25%	
							70	2.25	±0.25%	
RLR-XXC-JP	±5%	±9%		±0.5%	±0.7%					
RLR-XXC-GP	±2%	±6%		±0.5%	±0.7%					
RJ24CX	±10%	Rhco ±17% Pot. ±4% Vol.	Pot.	±0.625%	±0.87%					
RT 22C	±5%	Rhco ±17% Pot. ±4% Vol.	Pot.	±0.125%	±0.175%					
RER65FR	±1%	±3%		±0.25%	±0.35%					

Glass, Ceramic Paper	Maximum level of 50 percent of rated voltage.
*Solid Tant. (Polar)	Maximum level of 60 percent of rated voltage.
*Solid Tant. (Non-Polar)	Maximum level of 60 percent of rated voltage.
Herm. Sealed Tant. (WET), Foil or Slug	Maximum level of 70 percent of rated voltage.
Trimmer	Maximum level of 50 percent of rated voltage

The design shall also provide derating under ac, pulse or transient voltages. All solid tantalums should have at least 3 ohms/volt series impedance. The derating factors apply only for operating temperatures not exceeding 85°C (65°C for polystyrene capacitors). Additional derating must be applied for higher operating temperatures. These can be provided upon request.

A summary of capacitor derating factors and storage conditions for the ERTS system temperature and aging requirements are given in Table H-3.

2.2.3 Transformers and Inductors, - The maximum voltage stress to which a winding is to be exposed shall be less than 50 percent of its normal dielectric capability based on insulation thickness and spacing.

The operating temperature shall not exceed 80 percent of the operating temperature for the class of operation per MIL-T-27A.

Maximum current for the following wire sizes is 50 percent of the rated value:

#24 - 213.5 madc

#28 - 105.8 madc

#31 - 52.8 madc

#34 - 26.5 madc

#36 - 16.7 madc

*Circuits on internal supply will have current limited by dc/dc supply.

TABLE H-3. CAPACITOR DERATING FACTORS

Type	Tolerance		DC Leakage Current			Voltage Derating	Temperature Characteristic		Failure Rate	Storage
	Initial	Initial Plus 10,000 hr Degrad.	Cap. in μF	25° C	60° C		0° C	60°	Per 10° hrs	
CSR- -KP Electrolytic Tantalum-soln	±10%	±30%	8.2	5μA	31 μA	40% Rating	-3.3%	+4.8%	1	-55° C to +125° C
			18	9 μA	47					
			22	11 μA	58					
CL67-JPG Taltalum Wet Slug Elect.	±5%	+10% -15%	70	1 μA	4		-8.7%	+8.2%	0.13	-55° C to +125° C
			170	2μ A	10		-9%	+8.2%		
CH09A3RAJ	±5%	+5%, - 10%					-2.7%	+2.5% -1.5%		
CQ09A1MCJ3	±5%	±5.5%					±2% 0-70° C			
CL67-KPG	±10%	+15% -20%	150	2 μ A	18		-15%	+7.6%	0.13	
CKR06BX-KP (Ceramic)	±10%	+20% -30%					±4.7%	±5.25%		Values 70.01 μF dec. 2-6%
CK06BX-KP MP	±10% ±20%	+20%, -30% +40%, -50%					+4.7% -7.8%	+5.25% -8.75%		
CN05LD-J03 (Mica)	±5%	±5.5%					-0.05% +0.25%	-0.07% +0.35%		-55° C to +125° C
CTM VAJ (Mylar)	±5%	±10%					-1%	+1.5%		-55° C to -125° C
CL 21 23 31-32										1 year at +65° C max.
Tantalum Fail Elect. CYFRXXC--6	±2%	±3%					-.413%	+.578%		4 years at -55° C to +40° C Max.

#39 - 8.2 madc

#40 - 6.6 madc

#41 - 5.2 madc

2.2.4 Transistors. - The normalized junction temperature (T_N) shall be limited to 0.40 when the average power is calculated over a 30 second time period.

NOTE

Average power is calculated over a 30 second time period. No voltage transient shall exceed 80 percent of the device's rated terminal breakdown voltages. Power transistor deratings are also based on the use of heat sinks which limit the transistor case temperature rise above ambient to 6°C/watt. In no case, however, shall the junction temperature be allowed to exceed 110°C for any transistor.

General Purpose	Derate to 40 percent of rated power (max.)
High Speed Switching	Derate to 40 percent of rated power (max.)
Medium Power	Derate to 30 percent of rated power (max.)
High Power	Derate to 30 percent of rated power (max.)

Field Effect Transistors

All Types	BV_{DSO}, BV_{DGO}, BV_{SGO} - derate to 75 percent of rated value.

NOTE

MOS-FET's are vulnerable to damage by static electricity discharge and, therefore, precautions must be taken to ground hands and tools to grounded work bench and to maintain shorting strap on leads in accordance with RCA procedures.

a. Parameter Derating Factors - When transistor specifications are not well defined with respect to temperature or operating point characteristics, the parameter derating factors shown in Table H-4 have been used. These derating guidelines are relatively conservative and are considered to be applicable to the ERTS system operating and storage requirements.

b. Power Dissipation - Transistor thermal impedance may be represented by thermal resistors in parallel with thermal capacitors as shown in Figure H-2.

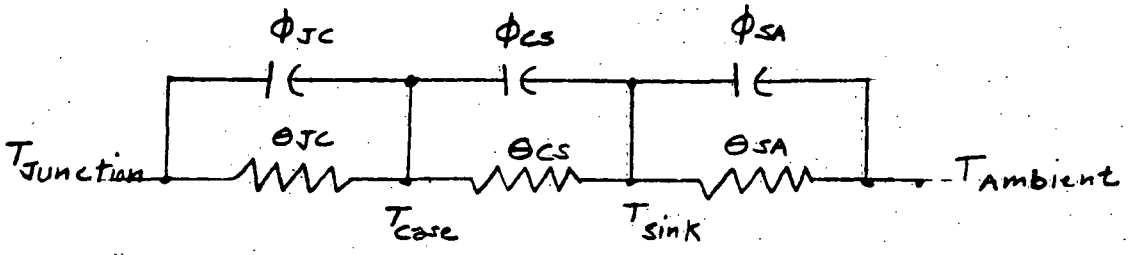


Figure H-2. Transistor Thermal Impedance Equivalent Circuit

Where the thermal time constant, τ, may be considered to be

$$\tau_x = \theta_x \phi_x$$

In pulse applications, for most duty cycles, the external time constants are large (several seconds), thus ϕ_{cs} and $\phi_{sa} \approx \infty$ and are usually ignored. The internal time constant, ϕ_{jc}, however, is small and cannot be ignored. If the duty cycle involves pulses of power dissipation occurring over a period of time comparable to (or longer than) τ_{jc}, then junction temperature rise is governed by the peak instantaneous power dissipation. Or, in other words, if

$$\text{Frequency of Operation} \leq \frac{1}{2\pi \tau_{jc}}$$

Then, use instantaneous power dissipation and assume $\phi_{jc} = 0$. On the other hand, if the duty cycle involves pulses of power dissipation occurring over a period of time much shorter than τ_{jc}, then the junction temperature rise is based on average power dissipation. Or, if the frequency of operation is high,

$$f >> \frac{1}{2\pi \tau_{jc}}$$

TABLE H-4. TRANSISTOR PARAMETER DERATING FACTORS

Parameter	Derating Factor
Saturation Voltages	10% increase of maximum limit for aging
V_{BE} (Sat)	Derate typical ±20% for max. and min.
	Decrease 2.5 mV/° C rise in junction temperature
V_{CE} (Sat)	Derate typical ±50% for max. and min. Increase 0.2 - 0.5 mV/° C rise in junction temperature
Breakdown Voltages $BV_{CE°}$, $BV_{EB°}$, $BV_{CB°}$	10% decrease of minimum breakdown voltage for aging
Leakage Current	100% increase at maximum limit for aging
$I_{CB°}$, $I_{CE°}$, $I_{EB°}$	Double every 14° C rise in junction temperature for GE Double every 10° C rise in junction temperature for Si
Gain (h_{FE})	50% decrease of +25° C value for -55° C 16% decrease of +25° C value for 0° C
T0-5 or smaller	Derate limits ±25% for aging
1 watt or greater	Derate limits ±30% for aging
Gain Bandwidth (ft)	25% decrease of minimum limit for aging
h Parameters (hrb, hib, hob, hre, hie, hoe	Derate limits ± 20% for aging
Input and Output Capacitance (cibo, cobo)	No change in limits due to aging
Switching Response	No change in limits due to aging
Noise Figure (NF)	No change in limits due to aging
fhfb, f_{hfe}	No change in limits due to aging

Then, use average power dissipation and assume $\phi_{jc} \longrightarrow \infty$. In general, average power is used when the pulse period is less than 1/10 of the transistor time constant, τ_{jc}. When the external heat transfer conditions are known, for a fixed dissipation, P, the transistor junction temperature is given by:

$$\theta_{JA} = \theta_{JC} + \theta_{cs} + \theta_{SA} = \frac{T_J - T_A}{P}$$

or

$$T_J = T_A + \theta_{JA} P$$

where,

T = temperature - 0° C

θ = thermal resistance - 0C/watt

It should be noted that in the zero gravity ERTS environment the affect of air convection on θ_{sa} (thermal resistance from sink to ambient) will be negligible.

c. Heat Transfer. - Since the ERTS Electronic Unit will be operating in a vacuum, there is no heat convection, thus heat transfer will be entirely due to radiation and conduction. When no heat sink is used, the radiating surface is simply the component case area.

On the other hand, the Transport Unit is pressurized and some convection is possible. However, except for the air circulation induced due to the zero gravity environment, by the rotation components in the transport unit, convection will be slight.

1. Radiation. - When the area of the heat sink is much smaller than the area of the surrounding surface, the radiant heat transfer in BTU/hr is given by:

$$Q = A_1 e_1 \quad (T_1^4 - T_2^4)$$

where,

A_1 = heat sink area (ft^2)

e_1 = emissivity (1 for a black body)

σ = Stefan-Boltzman constant (0.173×10^{-8} BTU/hr $-ft^2 -R^4$)

T_1 = Temperature of heat sink (° RanKine)

T_2 = Temperature of surrounding surface (° RanKine)

Applicable radiation equation conversion factors are:

° RanKine = ° F + 460°

Watt = 3.42 BTU/hr

If the above equation is applied to low power transistors, mounted on a standard plastic pad, the maximum allowable power dissipation for a radiation sink temperature of 61° C is as follows:

Radiating Surface	TO-5	TO-18
e_1 = 0.95 (painted surface)	123	43 mW
e_1 = 0.6 (unpainted surface)	78	27 mW

2. Conduction - When heat dissipation by conduction is utilized in the ERTS system, conduction is directly to the outer chassis, which is considered to be an infinite heat sink. Thus the maximum heat sink temperature will be 46° C, the VTR maximum environmental temperature.

2.2.5 Diodes

a. Zener voltage reference and stabistor diodes. - The maximum average power dissipation allowable is 50 percent of the 25° C power rating calculated over a second time period. Use the manufacturer's maximum allowable dissipation with liner devating for higher temperatures.

b. Signal, switch, rectifier, computer and zener regulator diodes. - Maximum average power dissipation allowable is 20 percent of 25° C rated power calculated over a 30 second time period.

c. Rectifier Diodes. - Maximum forward current allowable is 50 percent of 25° C rated forward current. Peak inverse voltages and surge currents shall be limited to 80 percent of the device rating.

d. General purpose diodes. - The normalized junction temperature (T_N) shall be limited to 0.4 when the average power is calculated over a 30 second time period.

NOTE

In no case shall the junction temperature be allowed to exceed 110° C for any diode. In addition, no voltage transients shall exceed 80 percent of the rated peak inverse voltage of the device; nor shall surge current exceed 80 percent of the device rating.

T_N is defined as: $\frac{\text{Operating Junction Temp } -25^\circ \text{ C}}{\text{Max. Rated Junction Temp } -25^\circ \text{ C (manufacturer's max.)}}$

Additional diode derating factors are given in Table H-5.

TABLE H-5. DIODE PARAMETER DERATING FACTORS

Forward Voltage (V_F)	5% increase of maximum limit for aging derate typical ± 20% for max. and min. Decrease 2 mV/° C rise in junction temperature.
Zener Breakdown Voltage (B_V)	Derate limits ± 1.0% for aging
Leakage Current (I_R)	100% increase of maximum limit for aging Double every 14° C rise in junction temperature for GE Double every 10° C rise in junction temperature for SL.
Breakdown Voltage (V_R)	10% decrease of minimum breakdown voltage for aging

2.2.6 Integrated Circuits. - Maximum Derating (percent of rated):

Digital - AC Fan-Outs - 60% - Power supply voltage to be as specified.

- DC Fan-Outs - 60% - Series connected logic gates are specified for a given supply voltage, max. operating temp., and frequency of clock operation.

- Combination of AC and DC Fan-Outs:

a. Load limit of AC levels - 60%

b. Load limit of DC levels - 40%

- Series connection of - 80%

- logic gates (max.)

Linear - Turn-on or Turn-off voltage transients (max. voltage ratings) - 95% - Supply voltages shall be as specified.

2.3 Input/Output Impedance and Signal Specifications

Individual circuit input and output impedance and signal characteristics are specified in the ERTS specification, Electrical Section.

APPENDIX I

SUMMARY OF RBV AND MSS INPUT/OUTPUT DRIFT STATISTICAL ANALYSIS

1. Introduction

The RBV and MSS signal dc offsets and gain variations as a function of temperature and aging have been summarized from the statistical analysis of the FM input/output networks in order to project the maximum input to output dc offset and gain drift. The RBV channel consists of the RBV Input, Modulator, Mixer, FM Amplifier, Limiter/Demodulator, and RBV Output circuits. During MSS operation, the signal path is identical to the RBV path except for the MSS Input and Output networks.

2. Summary

Detailed amplifier and component drift factors as a result of temperature and aging are given in the worst case analysis of each network. In addition, drift coefficients for a number of components (variable inductors, varicaps) which were not available for the worst case analysis have been obtained or given an estimated value for the statistical summary.

The percent dc offset and gain drift for the individual MSS and RBV networks is given in Table I-1. As noted in the table, the drifts are given as a percent of nominal peak to peak output signal. The total RBV dc offset drift is +12.6 percent due to temperature and +30 percent due to aging. The record to playback gain variation is ±0.82 percent and ±7.1 percent due to temperature and aging respectively. Similarly, the total MSS dc offset drift is ±29 percent due to temperature and ±65.8% due to aging, and the record to playback gain variation is ±0.93 percent due to temperature and ±4.6% due to aging.

3. Statistical Analysis

The results of Table I-1 were obtained using statistical combinations. This technique is based on the following assumptions:

a. The component part tolerances are not large relative to the component part's nominal value.

b. The component part values are independent variables.

c. The component drift is normally distributed about its nominal value.

These assumptions are usually satisfied for most electronic circuits, but even when they are not fully realized, the results obtained are more realistic than direct addition (worst case) of component part value limits.

When normally distributed component drifts are added statistically, the performance variable will also follow a normal distribution. Thus, the probability of the performance variable falling within the three sigma limits is 99.7%

TABLE I-1. MSS/RBV STATISTICAL DRIFT SUMMARY

Network	RBV Drift Referenced to Video Ouput				MSS Drift Referenced to Decoder Input			
	dc Offset (%)		Gain (%)		dc Offset (%)		Gain (%)	
	Temp.	Aging	Temp.	Aging	Temp.	Aging	Temp.	Aging
RBV Input	-1	±2.1	±0.35	±5.8				
MSS Input					+4.6 -3.3	+1 -2	±0.87	±4
Modulator	±12.5	±29			±28.2	±65		
Limiter/Demod	±.8	±1.1	±0.27	±1.35	±5.4	±13.8	±0.34	±2.2
RBV Out	+1 -2.1	+9.4 -5.5	±0.7	±3.9				
Statistical Total	±12.6	±30	±0.82	±7.1	±29	±65.8	±0.93	±4.6

Notes: 1. Percent drift is based on: RBV = 1.5Vpp, MSS = 500mVpp.
2. Where temperature compensation is included in the network design, temperature drift was assumed to be negligible.

The general expression for obtaining the standard deviation of the performance variable is given by

$$(\sigma y)^2 = \frac{(dy)^2}{dx_1} (\sigma x_1)^2 + \frac{(dy)^2}{dx_2} (\sigma x_2)^2 + \ldots \frac{(dy)^2}{dx_n} (\sigma x_n)^2 \quad (1)$$

where the performance variable, y, must be represented by an analytical function that relates it to the various component parts of a network, or

$$y = f(X_1, X_2 - - -, X_n) \quad (2)$$

The partial derivatives yield the individual component sensitivity factors and σx_n is the component three sigma deviation limit.

The application of equation 1 may be simplified when combining tolerances of simple sums, differences or products. When the performance variable consists of sums and differences, the deviation distribution is the RMS of the individual component deviations expressed in the component units (ohms, uF, etc.). When the performance variable is a function of a product, the tolerance distribution is the root-mean-square of the individual component tolerance expressed as percentages.

In general, the component sensitivities used in the statistical analysis were obtained from the network worst case analysis. However, computer programs were utilized for the modulator and the demodulator delay line statistical summary. In order to optimize the modulator component sensitivities, enough stray capacitance was added to the oscillator tuned circuits to permit tuning the analytical equivalent circuits at their nominal frequencies with nominal component values. The demodulator delay line component sensitivities were obtained by successive variation of each component in an ECAP transient analysis and then determining the change in output pulse width. To obtain the total input to output drift, the statistical results for each network were added statistically.

4. Conclusion and Recommendations

As shown in Table I-1, the modulator is the source of practically all the potential drift, both due to temperature and aging. The modulator drift is a result of the extremely high component sensitivities which are characteristic of the oscillator tank circuit. As shown in the modulator statistical summary, Table I-2, for example, a 0.5 percent change in inductance results in a 12.5 percent MSS signal deviation. However, since a balanced type modulator is used, the difference frequency will be relatively constant when the corresponding components of the two oscillator tank circuits track each other. Thus temperature drift may be minimized by matching components, and as a precaution against modulator temperature drift, each board should be temperature cycled and any marginal components replaced.

TABLE I-2. MODULATOR DRIFT CHARACTERISTICS

Component	Sensitivity	Tolerance (%)			Oscillator Deviation (kHz)	
		Temp.		Aging	Temp.	Aging
		0°	61°		25° - 61°C	
C2 - 100 pF	-108 kHz/pF		0 to +.25	±0.5	0 to -27	±54
C13 - 100 pF	-101 kHz/pF		0 to +.25	±0.5	0 to -25.2	±50.4
L3 - 46nH	-1.06 MHz/nH		±0.5	±1.5	-245	±735
L6 - 60nH	-863 kHz/nH		±0.5	±1.5	-250	±745
CR1 - 42pF	-611 kHz/pF		+1.22 to +2.44	±2.0	-310 to -620	±515
CR2 - 42pF	-570 kHz/pF		+1.22 to +2.44	±2.0	-290 to -580	±480
Modulator Drift						
Worst Case					±952	±2.65MHz
Statistical					±564	±1.31MHz

Notes: 1. Oscillator frequencies for component sensitivity factors: F1 = 100.13 MHz, F2 = 107.31 MHz.

2. Output signal sensitivity is: RBV = 0.33mV/kHz, MSS = 0.25mV/kHz

Further modulator temperature stabilization may be accomplished by regulating the bias current of the RBV and MSS Input circuit emitter followers. Therefore, for temperature stability purposes, it may be desirable to match individual RBV and MSS input boards to a specific modulator.

Since the polarity of component aging coefficients is not predictable, compensation for modulator aging drift is not possible. As a result, the saturation level of each demodulator should be checked to insure that enough dynamic range is available to accommodate the maximum carrier frequency plus deviation which may occur due to aging drift (MSS nominal + 1MHz + 1.31 MHz).

Since the aging coefficients of the varicap and variable inductions used in the analysis are not well defined, some revision of the data presented in Table I-2 is possible. The varicap aging coefficient used in the computations is based on the aging coefficient of a similar diode which has been documented in the "RCA Standards", and the variable inductor aging coefficient was projected from the aging coefficient of a fixed inductor of similar construction.