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PROTOTYPE DATA TERMINAL - MULTIPLEXER/DEMULTIPLEXER

FINAL REPORT
(Operations Manual)

For work performed under Contract NAS8-27538

MARTIN MARIETTA CORPORATION
DENVER DIVISION

PROTOTYPE DATA TERMINAL - MULTIPLEXER/DEMULTIPLEXER

FINAL REPORT

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INTRODUCTION AND SUMMARY

This document describes the design and operation of a quad redundant data terminal and a multiplexer/demultiplexer (MDU) designed and constructed by the Denver Division of Martin Marietta. The work was performed under NASA/MSFC Contract NAS8-27538.

The most unique feature of the work performed is the design of the quad redundant data terminal. This is one of the few designs that we know of where the unit is fail/op, fail/op, fail/safe. Laboratory tests indeed confirm that the unit will operate satisfactorily with the failure of three out of four channels.

Although the design utilizes state-of-the-art technology. The waveform error checks, the voting techniques, and the parity bit checks are believed to be used in unique configurations. Correct word selection routines are also novel, if not unique.

The MDU design, while not redundant, utilizes, the latest state-of-the-art advantages of light couplers and integrated circuit amplifiers. Much of the technology employed was an evolution of prior NASA contracts related to the Addressable Time Division Data System. A good example of the earlier technology development was contract NAS8-25066 which resulted in the development of a low level analog multiplexer, a high level analog multiplexer, and a digital multiplexer.

The following chapters discuss system concepts; describe the data terminal and MDU; present theory of operation; and provide instructions for installation, operation, and testing of the units. A list of all drawings is included for reference and all schematic, block and timing diagrams are incorporated as a part of the report.

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I. GENERAL SYSTEM DESCRIPTION

1. System Concept

Under NASA Contract NAS8-27538 a prototype quad redundant data terminal and associated multiplexer/demultiplexer units (MDU's) have been designed and built. The quad redundancy allows the system to meet a fail operational, fail operational, fail safe criteria. As shown in Figure 1 , the data terminal interfaces with a redundant main supervisory bus and a redundant main data bus. Up to 64 data terminals can be operated from these buses. Three redundant local buses, for supervisory words, data in, and data out, are provided to interface with the MDU's. Data from the MDU's is stored in memory in the data terminal until requested. Provision is made for transfer of data between data terminals. The system can operate at either a 1 MHz or 500 kHz bit rate. Words are 20 bits in length with each data word containing two eight bit bytes. Each MDU has 32 analog and 32 bi-level (digital) inputs and the same number of outputs. The system design has been conceived to provide flexibility to adapt to changing data handling requirements, minimum software complexity, and minimum bus transfer rate for a given vehicle data flow requirement.

The following paragraphs provide a general description of both the data terminal and MDU.

TYPICAL DATA BUS SYSTEM

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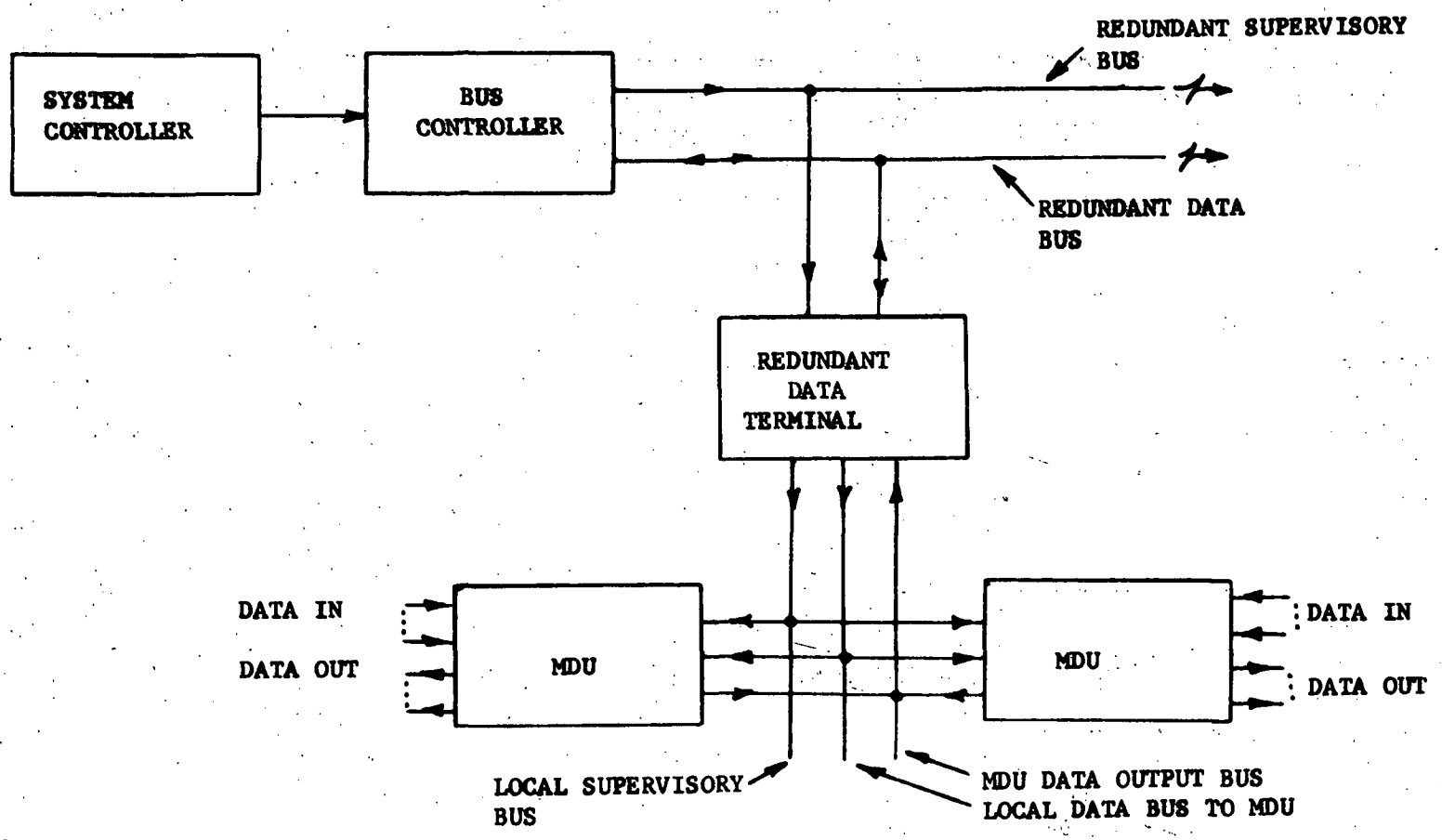


FIGURE 1.

2. Redundant Data Terminal

The Data Terminal is an element of a data bus subsystem and serves as an entry and exit point to the data cable for messages whose destination or point of origin is one or more user subsystems located in a given localized area of a vehicle. The Data Terminal is quad redundant with a fault tolerance criteria of fail operational/fail operational/failsafe.

The Data Terminal Functions are: a) detect the signalling waveforms on the supervisory and data cables, b) perform waveform checks, parity checks, and comparison checks on the detected inputs, c) decode supervisory commands, d) produce the proper format and waveform for subsystem, f) buffer data inputs from the user subsystem in a scratch pad (random access) memory to accommodate the timing requirements of data bus transfer operations, g) produce on the data cable the proper outputs at the times dictated by the supervisory commands.

The Data Terminal receives supervisory information from a set of 4 supervisory cables all of which carry the same supervisory commands. However, the time relationship is altered; so that the commands are delayed by 0, 5, 10, or 15 bits. The Data Terminal realigns the commands and then compares them all in each of four separate channels. Each channel has its own power supply and functions independently from the other three channels. All timing and synchronization signals are derived from the supervisory input which is a bi-phase level (Manchester) waveform.

Each channel checks its own supervisory input to ascertain that the incoming signal has the correct waveform at the correct frequency. If an error is detected a waveform error signal is issued. Next, each command is checked for correct parity. A clock and sync signal are also generated in each channel. Each channel uses the clock generated by its own supervisory input unless a waveform error is detected in which case it selects a clock from one of the other channels. This clock is put into a Johnson counter to generate the timing signals required by the channel.

The supervisory command, error signals, and sync signal are aligned for all four channels through the use of delay registers. Then each channel assembles its own version of the supervisory command on a bit by bit basis.

To do this, each channel compares its own bits against those received by the other channels. If a waveform error is detected in a channel, the bit from that channel is not used in the comparison. The bit which is in the majority is entered into a storage register. In the case of a tie vote, the channel uses its own bit.

The parity bit is received at the end of the supervisory word when the storage register is fully loaded. At this time, each channel selects the word in its own register unless a waveform or parity error has been detected in that channel; in which case it selects the word from one of the other channels where no errors have been detected. The word finally selected by each channel is referred to as the authentic supervisory word. If errors are detected on all four channels, that particular supervisory word is rejected and not acted upon.

The Data Terminal also receives and transmits information on a set of 4 main data bus cables each of which is associated with one channel of the Data Terminal. (The time relationship between these cables is altered the same as for the supervisory cables.) The incoming data words are checked and compared and an authentic data word is selected exactly as with the supervisory word. The authentic data word is then either stored in the memory or transmitted to the user subsystem.

Outgoing words on the main data cables are handled somewhat differently from the incoming data words. These words are taken from the buffer memory and are available in parallel with a known parity. Thus, a parity check can be performed immediately; and channels with words whose parity is incorrect can select the word from another channel. These words are now compared on a bit by bit basis as the word is being shifted out of the Data Terminal. Here again, each channel selects the bit which is in the majority. However, in the case of a tie vote a signal is generated which causes the word to be transmitted with even parity (odd parity is correct). In this way, the receiving system will be warned that the data is bad and will reject it.

In this design, it is assumed that the local user systems with which the Data Terminal will interface are redundant. Therefore, each channel of the Data Terminal has its own local output data bus, local input data bus, and local supervisory bus. The information transmitted to the user system is not compared. This should be done at the user system to detect any errors, such as noise, which may occur during transmission.

For most types of failures, this design should continue to function properly despite three failures. Only if a failure occurred at the same point in three of the four channels would three failures result in erroneous operation; and this is an extremely low probability type of occurance.

3. Multiplexer/Demultiplexer

The multiplexer/demultiplexer (MDU) interfaces with the data terminal and the various subsystems. The MDU can receive information from and transfer information to the subsystems. Twenty bit polar RZ supervisory and data words are transmitted from the data terminal to the MDU. Bit twenty is actually a missing bit to provide word synchronization. The MDU can be operated in two Modes (A & B) both of which are time synchronous with the data terminal because the clock is derived from the supervisory word. In Mode A the MDU is completely controlled by the data terminal. A supervisory word enables the multiplexer to accept subsystem data or the demultiplexer is enabled to provide data to the subsystem. In Mode B the demultiplexer is enabled by the supervisory word but the multiplexer is wired to an internal address generator which continuously sequences through all of the multiplexer addresses. The internally generated addresses are sent to the data terminal on the data line, with each address followed by the related data. Consequently the data in the data terminal is continuously updated.

The MDU has 32 analog and 32 binary data channels in both the multiplexer/demultiplexer portions. Analog data levels are 0 to +5 volts and binary data levels are TTL compatible.

All multiplexer analog addresses either from a supervisory word or from the internal address generator enable two analog channels to 8 bit digital form during the first half of the word time following receipt of the address. The data from the second channel is similarly processed during the second half of the word. Both 8-bit words, are loaded into a data output register for transmission back to the data terminal during the next word time after processing. Thus 16 bits of data are transmitted. As long as a Mode A MDU is addressed, there will be a continuous stream of data returned to the data terminal. However, Mode B MDUs will always return information continuously, but as indicated previously every other word will be the address of the succeeding data. Bit seventeen is an odd parity bit which defines the parity of the sixteen bits. Bits eighteen and nineteen are zeros.

Two multiplexer binary addresses each enable sixteen binary channels. Control logic enables ampling of these channels two at a time in four sequential time periods during the word time following the address. As in the case of the analog data. The data is transmitted to the data terminal during the next word time. Parity bit 17 and zero bits 18 and 19 are again added to the data stream.

Similarly the analog and the binary demultiplexer addresses enable the acceptance of data. Each analog data address enables two channels and a binary address enables sixteen channels. There is only one mode of operation for the demultiplexer and all addressing is done by a supervisory word from the data terminal. When a supervisory word conveying a demultiplexer address is transmited the related data will be transmitted during the third word time after completion of the address. Therefore, the demultiplexer contains a buffer storage register in the address receiver so that address decoding occurs during the data receipt time.

All demultiplexer data is received in digital form. The data word format is basically the same as a supervisory word, that is, 20 bits long with the twentieth bit missing for sync. Because of other system requirements bits 1, 18, and 19 are not used. Bits 2 through 17 are data.

If the data is related to an analog address the sixteen bits represent two 8 bit digital equivalents of the two desired analog outputs. These digital words are loaded into 8-bit storage registers which interface with two D/A converters. The resulting 0 to 5 volt analog voltages are supplied to the user through linear buffer amplifiers.

If the data is related to binary outputs, bits 2 through 17 are parallel loaded into output storage registers where each output line of the register acts as a TTL compatible binary source for each of the 16 users.

II. THEORY OF OPERATION OF DATA TERMINAL

1. General Explanation

The Data Terminal contains four redundant channels. The logic circuitry for each channel is contained on three Cambion boards making a total of twelve boards per Data Terminal. Two of the three boards have 126 sixteen pin sockets for dual in line packages. The third board is a universal board on which larger size sockets can be mounted. This board is used to mount the 24 pin memory packages and some large size component boards as well as a variety of 14 and 16 pin packages. The schematics for these boards are designated 380-111, 112, and 113 with 380-112 being the universal board. A block diagram of one channel of the Data Terminal is shown on schematic 380-110. Dotted lines indicate how the various blocks have been allocated to each board. The partitioning was based on minimizing interconnections between boards. In general, each block in the diagram represents one sheets of the schematic.

2. Board No. 380-111 Supervisory Word Logic

a. Sheet 2 - Adjustable Delay

This sheet contains the adjustable delay circuit which is used to compensate for the different distances from each Data Terminal to the Bus Controller. Single shots G18 and G17 are set for identical pulse lengths and are used to delay the leading and trailing edges of the supervisory word signal (SW) coming into the board from the line receiver. For demonstration purposes a 0.3 μsec. delay has been chosen. A leading (positive going) edge triggers G18. When G18 times out, flip-flop, E15, is set. E15 remains set until a trailing (negative going) edge triggers G17. When G17 times out, it triggers F16, which produces a 0.2 microsecond pulse to reset E15. Thus, the output of E15 reproduces the input signal delayed by the time for which G17 and G18 are set.

b. Sheet 3 - Waveform Detector 1.

This sheet contains circuitry which generates a sync pulse, clock pulses and data bits from the supervisory word line pulses. Checks are made to ensure that the incoming signal has a transition in the middle of each bit time and that parity is correct. The times for the single shots used on this sheet have been chosen for a 1MHz input bit rate and would need to be changed for 500KHz operation.

Figure 1 shows the timing for most of the significant signals generated in the waveform detector. At the top, a typical signal to the positive supervisory word input is shown. This signal is differentiated by an input gating arrangement to produce the X pulses shown in the figure. These pulses are between 50 and 100 nanoseconds duration. As shown in the figure an X pulse occurs at least every 2 microseconds except for the period at the end of a word (bits 17-20) when there is a 3.5 microsecond gap. Consequently, F15 is constantly being retriggered and does not time out until the last half of bit 19, at which time flip-flop, E15, is set. The Q output from E15 enables F12. On the next X pulse, which occurs in the middle of bit 20, F12 triggers and puts out a sync pulse, which clear E15 and triggers G15 and G16. The output from G15 is the clock pulse. When G16 triggers, its output is used to inhibit further inputs to G15 and G16 until G16 times out. In this way, X and Y signals which occur at the beginning of a bit time are filtered out and only transitions in the middle of a bit time will generate clock pulses. Only bits 17 and 19 do not have transitions

in the middle of a bit time. To generate clock pulses for these bits, D15 is used to provide a 0.27 microsecond delay after G16 times out. When D15 times out, D16 triggers and provides a pulse, which will cause a clock pulse to be generated, provided that the T1-T16 signal is not present and that an X or Y pulse has not appeared.

Flip-flop, E9, counts the number of zeros in a supervisory word during the period T1-T16. An even count at the end of this period indicates a parity error and places a high signal on the SP line.

G14 is retriggered every time a clock pulse occurs. If it should ever time out, it would indicate that something was wrong with the waveform on the supervisory word line or that a failure had occurred in the input circuitry. G13 is also triggered by the clock pulses. When it times out, G12 is triggered. If the clock pulse is still present when the pulse from G12 appears, it is an indication that the clock pulses are appearing too frequently or are of too long a duration. If either of these error indications occurs, flip-flop, E9, is set and a "hard" error indication signal, SH, is generated.

c. Sheet 4 - Clock Selector and Delay Register

The clock selector circuit is shown at the top of Sheet 4. The 93L18, C3, is a priority encoder whose output is an address corresponding to the highest order input. The inputs are the hard error indication from the four redundant channels. The signal SHW is the hard error indication for this particular channel and is low in the absence of a hard error. Since, this signal is connected to the highest order input of C3(7), address seven would normally appear at the output pins. (Because the address selects only one of four clocks, only the two least significant bits of the address are actually used.) A hard error in this particular channel would cause SHW to go high and C3 would then put out the address of the next highest order input that remained low. C2 is a four input multiplexer that selects one of four inputs in accordance with address bits S_o and S_1.

The delay register is used to realign the entering data. Thus, different delays must be used for each of the four channels. The data, sync, and hard error indications are delayed in shift registers. The parity indication, which is only used on a word basis, requires only one flip-flop, which provides a one word time delay. The 74L99 circuits are four stage shift registers. The data and sync information are delayed by 15 bits for channel A, 10 bits for channel B, and 5 bits for channel C. Because the hard error indication is generated in the bit time succeeding the one in which the error occurred, it is delayed by one bit less per channel. The signals for channel D are not delayed at all.

d. Sheet 5 - Sync Selector

The two flip-flops designated D14 are used to check for the sync pulse coming at the correct time. The top flip-flop is cleared at T19 and generates an error signal until the advanced sync pulse is detected. The bottom flip-flop is cleared during the first half of the T1 bit time. If an advanced sync pulse occurs any time from T1 through T19, the bottom flip-flop is set, generating an error signal. An error signal causes the next sync, in order of priority, to be selected by the 93L18 priority encoder and 93L09 four input multiplexer.

e. Sheet 6 - Supervisory Word Channel Selector

The 93L21 circuits, which are one of four decoders, on this sheet are actually part of the bit selection circuitry shown on Sheet 7. The state of the hard error signals from the four channels are decoded to energize one of 16 output lines. Only seven of these lines are actually used for bit selection. The states are given in Table 1. The manner in which these signals are used and the bit selection process are discussed under the description for Sheet 7.

Once the parity bit has been received, additional information is available to select a complete word. This is done using the priority encoder D9. Each channel will use the word in its own supervisory register (Sheet 7) provided that a hard error or a parity error for that particular channel does not exist. A check is made to see if all channels have errors. If this is the case a signal is fed to the all faults logic (Sheet 5 on Board 380-113) causing the supervisory word just received to be rejected.

f. Sheet 7 - Supervisory Word Bit Selector

Each channel forms a new supervisory word by selecting bits on the basis of the error indications that are available. If three of the four channels have hard errors, as indicated by H7, H11, H13, or H14, the bit from the remaining channel is selected. If such a situation does not exist, the entering bits from all four channels are compared using the five 93L21 blocks shown (Each 93L21 is a one of four decoder. Together, they make up a one of 16 decoder.) The various comparison states are given in Table 2. Where one channel disagrees with the other three, that channel is presumed to be in error (i.e., states C7 and C8). When a two vs two comparison exists and the bus agreeing with bus W has a hard error, but the other two busses do not have hard errors, then bus W is presumed to be in error. These error

TABLE 1

HARD ERROR DECODING

STATE IDENTIFICATION	HARD ERROR		DETECTOR STATE		OUTPUT POINT
	HW	HX	HY	HZ	
Ho	0	0	0	0	Not Used
H1	0	0	0	1	G11-11
H2	0	0	1	0	G11-10
H3	0	0	1	1	Not Used
H4	0	1	0	0	G10-4
H5	0	1	0	1	Not Used
H6	0	1	1	0	Not Used
H7	0	1	1	1	G10-7
H8	1	0	0	0	Not Used
H9	1	0	0	1	Not Used
H10	1	0	1	0	Not Used
H11	1	0	1	1	G10-9
H12	1	1	0	0	Not Used
H13	1	1	0	1	G9-5
H14	1	1	1	0	G9-6
H15	1	1	1	1	Not Used

TABLE 2

DATA COMPARISON TABLE

STATE IDENTIFICATION	BIT DESIGNATIONS W	X	Y	Z	OUTPUT POINT	REMARKS
Co	0	0	0	0	Not Used	No Errors
C1	0	0	0	1	Not Used	Bus Z in Error
C2	0	0	1	0	Not Used	Bus Y in Error
C3	0	0	1	1	C11-7	Two Buses In Error
C4	0	1	0	0	Not Used	Bus X in Error
C5	0	1	0	1	C12-5	Two Buses in Error
C6	0	1	1	0	C12-6	Two Buses in Error
C7	0	1	1	1	C12-7	Bus W in Error
C8	1	0	0	0	C11-12	Bus W in Error
C9	1	0	0	1	C11-11	Two Buses in Error
C10	1	0	1	0	C11-10	Two Buses in Error
C11	1	0	1	1	Not Used	Bus X in Error
C12	1	1	0	0	C12-12	Two Buses in Error
C13	1	1	0	1	Not Used	Bus Y in Error
C14	1	1	1	0	Not Used	Bus Z in Error
C15	1	1	1	1	Not Used	No Errors

combinations, along with the bus W hard error singla, are combined in gate B9 to form a bus W error indications, SEW.

Based on the error signals discussed above, the priority encoder, A11, generates an address which the one of four multiplexer, B11, uses to select a bit. This bit is shifted into a 16 stage register A9 and A10 at the middle of a bit time. This allows one-half of a bit time for propagation delay through the bit selection logic. The output of flip-flop, B10, which is set from T1 through T16, is used to gate the shift clock pulses to the register. Since no shift pulses occur from T17 through T20 the output of the register remains constant during this time period.

g. Sheet 8 - Supervisory Word Multiplexer

Using the address bits generated on Sheet 6, the multiplexers on this sheet select the output from one of the four supervisory word registers, Sheet 7. This word is then available, in parallel, for use in the channel control logic.

h. Sheet 9 - Address Comparator

The requirement exists that a data terminal must receive certain selected words transmitted by other data terminals. This means that the data terminal addresses and data word addresses must be stored for comparison purposes. This is done using programmable read only diode matrices. Six bits comprise a data terminal address, and up to seven bits may be used for a data address within the data terminal. These thirteen bits are entered into a 26 x 10 diode array. Since both the true and false states of the address bits must be used to detect a comparison, 26 inputs are used. Ten possible comparisons may be programmed. The RM-184 is an 8 x 5 array and the RM-177 is a 5 x 5 array. When a comparison is detected, one of the ten output lines from the diode array is energized. These output signals are then inverted through the RD-1534 circuits.

i. Sheet 10 - Address Generator

When an address comparison is indicated by one of the input lines, W1-W10, going low, a stored address is read from the 10 x 7 programmable diode array implemented with the RM-113 circuits. At the same time a comparison signal is generated. Interface inverters are used to provide a TTL drive capability for the seven output address lines.

j. Sheet 11 - M/DU Supervisory Word Generator

The data terminal transmits commands to the M/DU over the local supervisory bus instructing the M/DU to transmit or receive data or to receive a command. The address bits for the local supervisory word may come either directly from the main supervisory word or from the programmable diode array on Sheet 10. Selection is accomplished using quad 2 input multiplexer circuits, G4 and G5, which provide parallel inputs to the local supervisory word register, F1, G3, and F2. A zero is always loaded into the output stage of the register, F1-4. Shift pulses are provided to the register only during the T9-T19 time period. This insures that bits 1-9 of the local supervisory word, which are not used, are always zero. Flip-flop, B10, provides a signal which disables the output clock during the T20 period.

k. Sheet 12 - Programming Boards

The component socket adapters, B2 and B3, contain only wires. They are used to provide a Data Terminal address (000001 in this instance), a means of changing the mode of operation (A or B), and two local supervisory word bits (LSW10 and LSW11) which are used to provide bits required by the M/DU, but which are not included in the main supervisory work. The DT SELECT signal is generated at T19 bit time if the main supervisory word contains the correct address. Grounding the Mode Control line will cause the Data Terminal to operate in Mode A, while connecting it to +5V will provide Mode B operation.

3. Board No. 380-112 Input Data Word and Memory Logic

a. Sheet 2 - Waveform Detector 2

This detector reconstructs the data and checks the parity and the form of the incoming waveform. An input on line DR1 corresponds to a positive pulse on the Main Data Bus; an input on line DR2 corresponds to a negative pulse. Flip-flops (28, 64/1) and (28, 64/2) check the width of the incoming pulses and put out a hard error signal (DH) if the input does not last at least 0.8μsec. One additional hard error check is performed by flip-flops (30, 48/1) and (30, 48/2). These flip-flops produce a hard error signal if the inputs DR1 and DR2 do not alternate, corresponding to the laternating polarity of the Bi-Polar NRZ waveform.

The Input pulses are smoothed out to a consistent 0.8μsec by one shots (22, 72) and (20, 72). These signals are then ORed together to produce the Main Bus Data, MBD. Finally, the parity of the MBD is determined by flip-flop (20, 64/1) and a data parity error signal (DP) is produced if the parity is even.

b. Sheet 3 - Data Clock Selector

The pulses on the main data bus input may be delayed up to 750 nanoseconds with respect to the supervisory word clock. This delay overlaps the clock pulse transition time making it possible for clock transition and data transitions to occur so close together that the operation of flip-flops and registers cannot be guaranteed. To circumvent this problem, the circuitry on this sheet selects the clock phase (CL or $\overline{\text{CL}}$) whose leading edge occurs after the start of the data pulse but before its conclusion.

To accomplish this, the leading edge of the first bit of a data word (which is always a one) is used to set flip-flop (20, 64). The next leading edge of a clock phase will cause either flip-flop (20, 55/1) or (20, 56/2) to be set. This selects that particular clock phase and resets flip-flop (20/64). The clock phase remains selected for the duration of the data word. The selection flip-flops are reset at the 20th bit time of the corresponding supervisory word.

c. Sheet 4 - Data Delay Register

The selected clock is used to clock data into a flip-flop (30, 40/1) from which it is clocked into the delay register using $\overline{\text{CLW}}$. The data hard error signal (DH2) is also delayed in a register. The parity error indication is stored in a flip-flop.

d. Sheet 5 - Data Channel Selector

The data channel selector is identical to the supervisory channel selector described for Board No. 380-111.

e. Sheet 6 - Data Bit Selector

The data bit selector is identical to the supervisory bit selector described for Board No. 380-111.

f. Sheet 7 & 8 - Data Selector

The data selector is identical to the supervisory word selector described for Board No. 380-111. Sheet 8 contains the circuitry for selecting the seventeenth bit (excluding the initial one) of the word.

g. Sheet 9 - Local Output Register

The local output register is an eighteen stage register which is loaded with a data word from the main data bus. The first bit of the word is always a one, so the output stage is preset to a one when the register is loaded. Register shift pulses are inhibited during T19 and T20 when the register is being loaded. The XFER to M/DU signal cuts off during the last half of T19 so no LOB clock pulse is generated during T20.

h. Sheet 10 - Memory Input Data Selector

Data from the local input bus (LDI) is shifted into a 17 stage register. Either the outputs from this register or the data from the main data bus can be selected by the 93L22 multiplexers. Normally, the local data is selected unless the Receive From Main Data Bus and T20 signals are present.

i. Sheet 11 - 64 x 17 RAM

Each MK4002P contains storage for 64 four bit words. Five of these circuits are used to provide a total word length of 20 bits, of which only 17 bits are used. Reading or writing occurs when the Read Enable or Write Enable line is pulsed.

4. Board No. 380-113 Control and Output Data Logic

a. Sheet 2 - Bit Timer

The bit timer supplies all timing signals used by a channel of the data terminal. It consists of a ten stage shift register with inverted feedback which is cleared by the aligned sync pulse from the supervisory bus. During the ten clock pulses after the sync, ones are shifted into the register until it is completely loaded with ones. The, during the next ten ones, zeros are shifted in until the register is completely cleared. The sync occurs during the 20th bit when the register would normally be cleared anyway. With this arrangement all timing signals can be generated using two input gates with inverters where required.

b. Sheet 3 - Control Logic 1

The control logic generates the command signals used to control the logic in a channel of the data terminal. It also provides delay shift registers for storing the information until it is required. Information is set into the first stages of the delay registers at T19 time. It is then shifted by each T18 pulse.

A preset signal is generated at B11-4 whenever a type B or C supervisory word is received addressed to that particular data terminal (i.e., whenever the data terminal is to transmit or receive data). If a comparison signal is generated (See board 380-111 sheet 10) and if the transmit (S7) and destination (S8) bits are true, a preset signal is generated at C11-4. A preset signal is generated at C14-4 whenever the transmit (S7) bit is true. A preset signal is generated at D12-4 whenever the destination (S8) bit is true. The information in the registers is decoded to obtain channel control signals. Figure 2 shows the timing for these signals.

c. Sheet 4 - Control Logic 2

This sheet contains the logic which controls the storage and selection of status data, the reading of the memory, and the loading and shifting of output data.

To read out status data, a supervisory command word (Type A supervisory word) is sent to the data terminal. The command bits are S10 through S15. Command No. 1 (000001) is used to request a status readout. When this command is received, a preset signal is generated at C7-4. Then, two word times later, a status data select signal is generated which causes the data terminal to feed status data instead of memory data into the output register.

The read address select signal is used to select the proper address when reading the memory. The Bit 1 signal ensures that the first bit of each output data word is a 1. The local clock signal gates either status data or memory data into the output data register. This register is then shifted by the data register shift signal. The data shift enable signal enables the output delay register which provides the proper skew between output data words. The read enable signal is the signal that actually causes the memory to read.

d. Sheet 5 - All Faults Logic

When all four channels in the Data Terminal indicate faults, it is imperative that action be taken to prevent improper data being used in the user system. If errors are detected in all four output data words, even parity is transmitted to indicate an erroneous word. If all four input data words are in error, the word is rejected and no data is transmitted to the M/DU. If all four supervisory words are in error, the supervisory word is not used (decoding is inhibited).

The information that all words had simultaneous errors is also stored in flip-flops until a command is received to read out a status word. The all error indications are then read out as status bits 13, 14, and 15.

e. Sheet 6 - Status Register

When a status word is commanded, the error signals for operations immediately preceeding transmission of the status word are stored to make up the bits for the status word. Four bits are used for output data word error indications; four bits are used for input data word error indications; four bits are used for supervisory word error

indications; and three bits are used for the all error indications. The sixteenth bit (SI17) is not used and a parity indication is generated by the 74L86 exclusive or gates for the seventeenth bit (SI18).

f. Sheet 7 - Data Register and Parity Checker

The quad 2-input multiplexers, 93L22s, normally select the memory output data unless the status data select signal is present. The selected data is entered into a seventeen stage register (G8, G7, G6, G5 and G2) when the load clock pulse occurs. It is then shifted out by the data register shift signal during the T7-T4 time interval. The bit 1 signal is entered at T6 time to make the first bit of the word a one. Parity is checked by the exclusive or gates. If parity is correct flip-flop, D3, is set and PW, the parity error indication, will be low.

g. Sheet 8 - Authentic Data Selector

When wrong parity is indicated for an output data word, the next highest order word without a parity error is selected by the priority encoder, 93L18. The priorities differ from channel to channel as specified in Table 3. This is done to ensure that in the cases of two channels with parity errors, the same data will not be used as a substitute for both.

	Channel No.			
Designation	A	B	C	D
W	A	B	C	D
X	C	D	A	B
Y	B	C	D	A
Z	D	A	B	C

TABLE 3

CHANNEL BIT SELECTION PRIORITIES

The selected word, W', is now compared bit by bit with the selected words from the other three channels, where W' compares with at least two of the other three bits, it is transmitted. If W' does not compare with any of the other three bits, then X' is transmitted in its place. If W' compares with only one other bit, then a conclusive selection is not possible and even parity is transmitted to indicate the word may contain a possible error.

h. Sheet 9 - Output Delay Register

Because of differences in design, the output delay registers for all four channels are shown on this sheet. These registers provide the skew required between output words. The 74L91 is an eight stage shift register, while the 74L99 is a four stage shift register. Channel D is delayed by 15 bits; channel C is delayed by 10 bits; channel B is delayed by 5 bits; and channel A is not delayed.

i. Sheet 10 - Main Data Bus Waveform Generator

The logic on this sheet converts the data and clock signals to the signal required by the line drivers for the main Data Bus. On the Main Data Bus, ones are indicated by alternating polarity and zeros by a zero level. The waveform generator causes the first one in a word to appear on the DCB line, and the next one to appear on the DAB line, etc. For a zero both DCB and DAB are high.

j. Sheet 11 - Local Data Input Logic

This sheet contains the logic which gates the first 17 bits of a data word into the memory input register. It also contains logic for sync detection, address recognition, and write control during Mode B operation.

Flip-flop, A5/1, is set by the supervisory word sync pulse. This allows data clock pulses to be gated into the four bit counter, A4. At the end of the sixteenth clock pulse A5/1 is cleared; and at the end of the seventeenth clock pulse, the input to A4 is inhibited. Thus, exactly 17 clock pulses are allowed through on the LDC line.

In Mode B operation, the M/DU sends first an address word and then a data word on the local data input line. The 20th pulse of each word is deleted for sync purposes. Single shot, B4, is continuously retriggered until the missing sync pulse allows it to time out. Single shot, B7, is then initiated, clearing flip-flop, A2/1, on its leading edge. This causes the succeeding data word to be gated into a nine state register consisting of A1 and A5/2. On the next sync pulse, if the last two bits, OA and OB, in the register are ones, flip-flop A2/1 is set. This provides an output from B2-6 which enables the next 17 clock pulses on the LDC

line. These pulses clock the next 17 bits into the memory input register. On the next T18 pulse, a LA XFER signal is generated which transfers the local address bits into the memory address register. A WRITE B signal is also generated at this time to write the data into the memory.

k. Sheet 12 - Memory Address Register

The memory address register actually consists of four separate registers each of which hold the address for one word time. A7 and A6 are loaded with an address from the incoming supervisory word at the middle of T19. This address is then parallel transferred down through the other registers at the middle of each succeeding T19 bit time. C2 and C1 are four bit data selectors/storage registers which select either the address from the supervisory word or the local address for writing data.

E2 and E1 are quad 2 input multiplexers which select either a read address or a write address as desired.

5. Line Drivers and Receivers

The line drivers and receivers for the Data Terminal are shown on schematic 380-114. There are a total of six circuits of three different types: the Local Data Bus Receiver, the Main Data Bus Receiver, and the Main Supervisory Bus Receiver are the same; the Local Data Bus Transmitter and the Local Supervisory Bus Transmitter are the same; the Main Data Bus Transmitter is different from the other two transmitters because of isolation requirements. Each redundant channel has an identical set of six circuits. All 24 circuits are packaged on three PC boards which are identical. These boards are designated -009, -019 and -029. Two sets of component designations and pin numbers appear on each sheet of the schematic. These sets are assigned as follows:

CIRCUIT NAME	SHEET NO.	CHANNEL	FIRST NO. (LEFT OR TOP)	SECOND NO. (RIGHT OF BOTTOM)
Main Data Bus Xmitter	2	A	-009	
Main Data Bus Xmitter	2	B		-009
Main Data Bus Xmitter	2	C	-019	
Main Data Bus Xmitter	2	D		-019
Supervisory Bus Receiver	3	A	-009	
Supervisory Bus Receiver	3	B	-019	
Supervisory Bus Receiver	3	C	-029	
Supervisory Bus Receiver	3	D		-009
Main Data Bus Receiver	4	A	-009	
Main Data Bus Receiver	4	B	-019	
Main Data Bus Receiver	4	C	-029	
Main Data Bus Receiver	4	D		-019

CIRCUIT NAME	SHEET NO.	CHANNEL	FIRST NO. (LEFT OR TOP)	SECOND NO. (RIGHT OR BOTTOM)
Local Sup. Bus Xmitter	5	A	-009	
Local Sup. Bus Xmitter	5	B	-019	
Local Sup. Bus Xmitter	5	C	-029	
Local Sup. Bus Xmitter	5	D		-009
Local Output Bus Xmitter	6	A	-009	
Local Output Bus Xmitter	6	B	-019	
Local Output Bus Xmitter	6	C	-029	
Local Output Bus Xmitter	6	D		-019
Local Data Bus Receiver	7	A	-009	
Local Data Bus Receiver	7	B	-019	
Local Data Bus Receiver	7	C	-029	
Local Data Bus Receiver	7	D		-029

The design of the receiver and transmitters is similar to the equivalent circuits in the M/DU.

III. THEORY OF OPERATION OF MULTIPLEXER/DEMULTIPLEXER

1. Block Diagram

a. General

Figure 380-19 is a block diagram of the Multiplexer/Demultiplexer (MDU). The unit consists of a multiplexer which is very similar to the units developed for the Addressable Time Division Data System under contract NAS8-25066. The demultiplexer is a new circuit design. Although the functions of the multiplexer and demultiplexer are generally independent, the address receiving and some control logic are common.

b. Multiplexer

The basic operation of the multiplexer is to receive a supervisory word from the data terminal, decode an address from the supervisory word and in response to a correct address, sample data. Sampled analog data is converted to digital form and is returned to the data terminal serially. Sampled binary data is also returned to the data terminal in digital form. The multiplexer is capable of interrogating 32 analog channels and 32 binary channels. Two analog channels are sampled for each related address and 16 binary channels are sampled per assigned address. Both supervisory and data words are twenty bits long. Analog data words consist of two 8-bit data samples, a parity bit, two zero's and a missing pulse for sync. Binary data words contain 16 binary bits, a parity bit, two zero's and missing pulse for sync.

The multiplexer is designed to run in two modes if wiring changes are made. When a multiplexer is connected in the most common mode, designated A, data is only sampled and updated upon command from the data terminal. Reiterating, analog data is sampled and converted to digital form upon decoding of a valid address. The data processing occurs during the word time after the correct address. The data is transmitted to the data terminal two word time after the address. In the other mode, designated B, the multiplexer is used as a dedicated unit and data to the data terminal is updated continuously. In the mode B operation the multiplexer is wired to operate from an internal format generator. This generator continuously cycles through all of the valid addresses. The internally generated addresses are sent back to the data terminal serially on the data line. Each address is followed by its related data. In mode B all addresses are still encoded in a 20 bit word, but only bits 12 through 20 are necessary for identifying the addresses. Bits 12 through 17 are specific addresses; bits 18 and 19 are ones and bit twenty is missing for sync. The data format is the same as that described for mode A.

c. Demultiplexer

The operation of the demultiplexer is to receive data upon command from the data terminal and transmit it to the user. All received data is in serial digital form. Analog originated data is reconverted to analog form for the user and binary data is separated into the necessary discrete outputs. Thirty-two analog channels and 32 discrete channels are demultiplexed. Similar to the multiplexer, the demultiplexer decodes correct addresses and receives corresponding data. Timing is such that data is not received until the start of the third word after the address. Data to the user is updated at the end of the third word after the related address. Like the multiplexer each address corresponds to two analog words or to 16 binary bits of data.

d. Common Circuits

As can be seen from the block diagram there are some circuits common to both the multiplexer and demultiplexer sections of the MDU. Only one address receiver is necessary for receiving all addresses from the data terminal for multiplexing and demultiplexing and the basic control logic of the multiplexer is usable for the demultiplexer control. Detailed descriptions of these common circuits and all the rest of the circuits are presented in the discussion to follow:

2. Address Processing

a. Waveform

The address receiver receives twenty bit supervisory words from the data terminal. The waveform is a bipolar RZ with positive going information representing a digital one and negative going information is a digital zero. Zero level is quiescent. Drawing 380-52 shows this waveform. The voltage levels of the waveform are +4 $\pm$ 10%, -4 $\pm$ 10%, and 0.

A supervisory word contains 19 information bits and a missing twentieth pulse for sync. The nineteenth bit is the least significant bit. Bits 9 through 18 and sync are the bits used to address the MDU.

b. Receiver Circuits

Drawing 380-23, sheet 1, contains the schematic diagram of the address receiver. The input amplifier, HA2515 and associated components, comprise a unity gain high input impedance buffer amplifier for loading of the address line. The amplifier is operated from plus and minus 12 volts which are provided by an isolated winding in the power transformer so that the MDU system ground is isolated from the data terminal ground. Since a dc-isolated coupling is required between the two systems, two MCD-2 light couplers interface the output of the amplifier with LM-306 comparators in the MDU system. Diode CR5 couples positive going pulses (ones) into one light coupler and diode CR6 couples negative going pulse (zeros) into the other coupler. One LM306 converts the output of the "ones" coupler to TTL compatible one information pulses and the other LM306 converts the "zeros" coupler to zero information pulses. OR combining of one and zero pulses provides a system clock (A11, A3 of 380-23, sheet 2.) Although the light couplers are fast their inherent circuit capacities degrade rise and fall times of output pulses unless considerable input drive power is used. Transformers T1 and T2 are peaking transformers used to maintain good switching times without excessive power.

c. Sync Generators

The schematic diagram of the sync generators is shown on drawing 380-23, sheet 2. Three type 74L122 low power retriggerable one shots (A5, A6, A7) are used for sync generation. The clock derived from the supervisory word is used to trigger A5. The time constant of A5 is set slightly longer than one clock period; therefore, A5 will never time out as long as there are clock pulses. When no clock pulse occurs during the twentieth bit time A5 will time out and changes states, which will trigger A6 to generate a 300 nanosecond sync pulse. Since there is some need for a delayed sync pulse the output of A6 is used to trigger A7 which generates another 300 nanosecond pulse immediately following the first sync pulse.

d. Multiplexer Address Decoding In Mode A

The output of the address "1" comparator is fed into a ten bit serial shift register (F1 thru F10). The first 9 bits of a supervisory word are shifted out the end of the register. Bits 10 through 19 are the multiplexer address and these bits fill the register prior to twentieth bit. A sync pulse which is derived at the twentieth bit time transfers the 10 address bits in parallel into a holding register (F11 thru F20). The Q and $\bar{Q}$ outputs are decoded by a two level decoder which was developed on contract NAS8-25066, "Remote Multiplexer". The first level decoder consists of AND gates which decode all the outputs of the ten bit storage register into three groups. By combining various outputs of the three groups into three input AND gates any of the 1024 possible addresses can be decoded. The second level decoder consists 18 three input AND gates and a printed circuit grid matrix to connect the gates to the various first level group outputs as desired. Drawings 380-20 and 380-21 are diagrams of the decoders.

e. Multiplexer Addressing in Mode B

Drawing 380-23, sheet 3 shows the address shift register connections for Mode B operation. Flip-flops F1 thru F6 are connected to form a counter. Flip-Flops F7 thru F10 are hardwired to form the most significant bits of the address which must be the same for all addresses in a specific multiplexer. Flip-Flops F1 thru F10 have their correct direct set or clear circuits hard wired to Address Encode Logic (EA), which cyclically loads the smallest numerical address into the flip-flops.

The address encode pulse occurs at the delayed sync pulse time. Another pulse designated "Address Load and Update" (ALU) transfers the contents of the counter - register into the address holding register and into the output data register. ALU also increments the address in the counter register by one count after transferral of the initial address to the holding register. ALU occurs at every other sync pulse so that an address can be sent back to the data terminal one word time followed by data the next word time. The ALU pulse is generated by logic shown on drawing 380-23, sheet 1. Basically this logic counts clock pulses and gates the count with the sync pulse. Since each word time represents an odd number of clock pulses a toggle-connected flip-flop will alternate states at sync bit times and thus the ALU is generated.

All eighteen addresses are loaded in the address register by ALU. At the same time a count-to-eighteen counter A8 thru A18, drawing 380-23, sheet 1 counts ALU pulses to generate Address Encode EA which starts the cycle over. In mode B the incoming supervisory word is not loaded into the address registers, but the clock and sync data are still obtained from the supervisory word.

f. Demultiplexer Address Processing

Demultiplexer addresses are received by the same address receiver as the multiplexer. Decoding, however, is performed by a separate circuit because demultiplexing must be performed in both modes A and B which prohibits a common use of the decoder. Drawing 380-25 is the schematic diagram of the demultiplexer decoder. Operation is the same as the multiplexer with some exceptions. The first difference is that two holding registers are added to provide two additional word delays before an address is decoded. A second difference is that only the last eight bits of a supervisory word need be decoded to perform all demultiplexing functions. This number of bits will allow two bits for distinguishing demultiplexing from multiplexing and the remaining six bits can identify 64 addresses for demultiplexing. Only eighteen addresses are required per demultiplexer so one data terminal can interface with three separate MDU's. Another change is the addition of a clock signal to the channel address decoders. This clock signal is derived from the incoming data so that no clock will exist unless data is actually transmitted. This design takes care of the situation where an address is sent down saying "demultiplex", but in the processing of data to follow, a discovery is made that no valid data can be identified. Consequently, the transmission of no data is considered preferable to updating with questionable data.

The programmable decoder matrix in the demultiplexer is the same as the multiplexer except for size.

3. Multiplexer Data Processing

a. General

Drawings 380-52 and 380-53 are timing diagrams showing the relationship between supervisory words, and associated data. As was previously stated, the multiplexer in mode A decodes a supervisory word; processes data during the next word time; and sends data to the data terminal the second word time after the address. The multiplexer in mode B generates an address; sends the address back to the data terminal; and data related to the address is sent to the data terminal immediately after the address. In mode B, bits 18 and 19 are always one's for an address and zeros for data so that the data terminal can distinguish the two. Again repeating, the demultiplexer timing is independent of the mode of the multiplexer. Data for demultiplexing is received as the third word after the related address. It is important to note that bits 12 and 13 of a supervisory word determine whether the word contains a multiplexer or a demultiplexer address. Control logic for data processing will be described next.

b. Control Logic

A nine stage Johnson counter is the foundation of the MDU control logic. This counter is shown on drawing 380-22. Flip-flops FF1 through FF9 form the counter. Flip-flop FF10 inhibits the counter at bits 18 and 19. Various states of the counter can be decoded spike free to control most of the data processing of the MDU. The counter operates continuously from clock pulses. When power is first applied to the system the states of the Flip-flop will be random, but all of the output logic is gated with the address decoder so no operation occurs unless a valid address has been received. It is possible for a valid address to appear incorrectly at turn on, but the first sync pulse will set all flip-flops of the control counter and address registers to correct states and the unit will operate correctly thereafter. Valid addresses are recognized by OR gates (A16, A17, A12) shown on drawings 380-23, sheet 1. The outputs of the OR gates are inverted by AND gates (A12) and routed to the control logic as signals LA1, LA2, LB. In mode A one of these signals is always present with a correct address, but in mode B indications of correct address must be inhibited one word time before data processing can occur so that the address can first be sent back to the data terminal. Data Load (L) enables the gates outputing LA1, LA2, and LB in ode B. L is generated at alternate word times by using the odd bit count of a word from the same toggle flip-flop that generates ALU. Drawing 380-53 shows the timing diagrams of the control functions. The timing diagram is generally self-explanatory in the respect that logic equations are shown for functions generated by multiple states of the Johnson counter. The use of the control signals is further defined in following descriptions of the various data processing circuits.

c. Analog Data Processing

Drawing 380-28 is a diagram of the multiplexer data sampling switch pc-board. The switches are all double pole MOS-FET for balanced input to a differential amplifier. Two pc boards are used in this MDU with only sixteen of the possible twenty channels being used on each board. The switches are divided into two equal groups per board as can be seen from the diagram. Each switch has a separate control and each group of switches has two group controls. One group control (first level), which enables all switches, is hardwired to +5 volts for continuous enable. The other group control (2nd level), enables a double pole switch, which is in series with all channel switches in that group. The individual channels are enabled by a decode address. Two channels, one in each group, are enabled by a decoded address applied to the channel controls, e.g., C1 and C11, etc. The second level controls are enabled by "ODD" and "EVEN" control pulses COA and CEA as shown on the timing diagram. COA enables one 2nd level control and CEA enables the other 2nd level control. This arrangement provides the sequential sampling of two channels per address. In actual circuit configuration COA1, COA2, CEA1 and CEA2 are generated so that each multiplexer board has separate second level controls. This is done by gating the COA and CEA pulses with the valid analog address group signals G1 and G2 (drawing 380-23, sheet 1). This design minimizes input circuit capacity and also limits the number of channels to eight that could be conceivably impared by any type of single channel failure.

The closing of a multiplexer switch connects data of the associated channel to the input of a unity gain buffer amplifier (A1 thru A4). The amplifier circuit is shown on the signal conditioner schematic diagram, drawing 380-29. The amplifier is a proven circuit used previously on NASA contract NAS8-25066, "Remote Multiplexer." At the time a valid analog address is recognized the first associated data channel is sampled for 4 bit times. During the sample time a sample-hold switch Q1 is closed and a sample-hold capacitor C14 is charged to the data voltage. Capacitor C14 is coupled to an A/D converter thru a high input impedance buffer amplifier (A6 and A7). As shown on the timing diagram, an A/D convert start pulse is generated the last 1/2-bit time of the sample. At the time of the sample pulse trailing edge capacitor C14 is charged and isolated from the input and A/D conversion starts.

The sampled analog voltage is converted to an eight bit binary equivalent by a successive approximation converter manufactured by Varadyne (Model ADC-M8B2A1). This converter, shown diagramatically by drawing 380-27, has its own internal asynchronous clock. The conversion time is 3.8 microseconds maximu. Five bit times of the MDU are allowed for the conversion and after conversion is completed a load pulse transfers, in parallel, all of the eight bits of the A/D converter into the output register. At the same time the load pulse occurred the second analog switch associated with the selected address closes and the data processing cycle is repeated for the second word. During processing of the second word, data in the output register is shifted toward the output so that the register is clear to accept the second word. The second word is loaded into the output register on the eighteenth bit time. The data output register and other data output circuits are discussed in more detail in later paragraphs.

Analog data processing is essentially the same for modes A and B except in mode A data output occurs in response to a supervisory word and can occur as often as every word time. In mode B, however, data output always occurs every other word period.

d. Binary Data Processing

Binary data processing uses multiplexer switches identical with those described for the analog data. Two of the multiplexer circuit boards are also used for binary multiplexing. Again, only 16 of the 20 possible channels on each board are used. One binary address, addresses a multiplexer board by enabling the second level controls. Each group of eight channels is connected to its own buffer input amplifier. One buffer amplifier circuit consists of IC amplifiers A8, A9, and A10. The other amplifier circuit consists of A11, A12, and A13. This arrangement allows the sampling of two binary channels at a time. At the time a binary address is valid, binary load pulses shown on the timing diagrams are generated from decoding of the Johnson counter. Eight sequencial pulses are generated and each pulse enables two channel gates on the multiplexer boards. Binary load pulses transfer two binary bits at a time into the output data register until sixteen bits of binary data have been loaded. Variations in operation between modes A and B are the same as was described in the analog multiplexing section.

e. Data Output Circuits

Drawing 380-27 previously mentioned to show the diagram of the A/D converter also shows the data output register. This output register consists of 20 flip-flops FF1 through FF20. All data except the parity bit is loaded into flip-flops FF1 through FF10. Flip-flops FF11 through FF20 are primarily used for buffer storage so that the nineteen bit data words can be assembled for ultimate transmission back to the data terminal. To some extent the loading of data has already been described, but some of this description will be repeated and expanded upon.

When analog data has been interrogated and converted to digital form the parallel output bits of the A/D converter 2^1 through 2^8 are loaded into the output register. Analog, odd or even, load commands enable gates coupling the data to the direct sets of flip-flops FF3 through FF10. The least significant bit is set in FF3. A careful examination of the timing diagram will show that "odd" analog word is shifted into FF1 through FF18 before the "even" analog word is loaded at the eighteenth clock time. In mode A operation FF1 and FF2 contain zeros. The nineteenth clock pulse shifts the 16 data bits into FF4 through FF19 and a zero is shifted into

FF3. Since data is to be transmitted out beginning with the first bit of the next word, the data register is properly loaded. The first bit of the next word will shift 16 bits of data and one zero into FF4 through FF20 and another zero will be loaded in FF3.

Data actually is being transmitted beginning at the first bit time of the word after data processing, because Output Data Control (ODC) enables the line driver so that the contents of FF20 actually appear on the data line. The generating circuit for ODC is shown on drawing 380-22, sheet 1. Normally, the output of FF12 is low which inhibits the line driver. When a valid address occurs, a one is set into FF11. At the next sync bit time (end of referenced valid address) the one is transferred from FF11 to FF12 and the line driver is enabled. At the same time a zero is clocked into FF11 if no new valid address is recognized. If a new address becomes valid F11 retains a one, therefore, at the next sync time the ODC will go low if no new data is forthcoming or will remain high for any immediately following data.

The line driver is shown on sheet 2 of drawing 380-22. It is interfaced with the data register by the logic gates shown

4. Demultiplexer Data Processing

a. General

If a supervisory word containing a demultiplexer address is received by the MDU, the address will have been shifted to the output of the demultiplexer decoder by three word times after the initiation of the address. Related data will be arriving from the data terminal at the same time the valid address is decoded. The address will be either associated with data representing the binary equivalent of two analog words or with a binary word consisting of 16-bits of discrete data. If the data is intended as an analog output, data processing will end with D/A conversion. If the data is discrete, processing will end with parallel separation of the 16 bits. Timing diagrams are shown on drawing 380-53 and -54. Details of the circuits are described as follows:

b. Data Receiver

The incoming data has the same waveform and sync bit configuration as the supervisory word. The data receiver (schematic diagram shown on drawing 380-24, sheet 1) is identical with the address receiver already described.

c. Analog Demultiplexing

There are 32 analog data output channels as previously indicated. Each channel output circuit consists of an output amplifier driven by an 8-bit D/A converter. An 8-bit storage register drives each D/A converter. Two of these 8-bit registers are connected serially so that the 16 bits of incoming data representing the two words can be received serially. When a correct address is decoded the decoder output, in effect, enables the clock circuit to the appropriate pair of registers so that the 16 bits can be loaded. The complement of the data is loaded into the reigsters because the D/A converter requires inverted logic to provide the desired 0 to +5 volt input. Since incoming data is actually nineteen bits long, logic control from the MDU control counter is used to control the data loading. The timing diagrams show that seventeen bits are actually shifted into the register. The first bit is not real data and is shifted out the end. Bits 18 and 19 which are parity and undefined bits are not clocked into the register. While the registers are being loaded the analog data output may be changing with the bit variations, but the total response time of the amplifier and user circuits will be slow enough so that transient changes will be ignored. Analog output data will correspond to the digital input word within a few microseconds after the registers have been loaded. Schematic diagrams of analog demultiplexing circuits are shown by drawings 380-24, sheet 3 and 380-26, sheets 1 through 5.

d. Discrete Data Demultiplexing

The demultiplexer contains a serial input 16-bit shift register. Decoding of either of the two discrete data addresses enables the shift reigster clock so that data is clocked into the register. Seventeen bits of data are clocked into the register as is the case for the analog data. Again the first bit, which is not real data, is clocked out of the register and bits 18 and 19 are not entered into the register. After the register is loaded a pulse, generated from the MDU control logic acts as a clock for parallel entry of the sixteen bits into one of two sets of 16 storage/output flip-flops. The decoded addresses enables a gate to route the load pulse to the correct set of flip-flops. Binary demultiplexer circuitry is shown by drawing 380-24, sheet 2.

IV. INSTALLATION, OPERATION AND TESTING

1. Specifications

The data terminal and demultiplexer are designed constructed and tested to operate in accordance with NASA/MSFC Specification Number GC-110547. These specifications provide for operation at laboratory environments only. The units as constructed will operate at a system clock rate of 1MHz but operation at any lower frequency is possible. For any other frequency operation the one shot circuits that provide sync and clock pulses at the missing twentieth bit intervals must be modified to time out at the center of the desired time interval. These changes are basically the changes of RC time constants. No other circuit modifications are required. Regardless of the frequency of operation, the knowledge of some design specifications other than presented by GC-110547 is desirable for optimum performance. These are as follows:

Data Terminal

Input power: 16 watts/channel @ 28VDC
Supervisory bus, Data bus, and local bus
Signal Amplitudes: Positive going +4 ±10% VDC
Negative going - 4 ±10% VDC
Zero level signals - 0.7 to +0.7 VDC

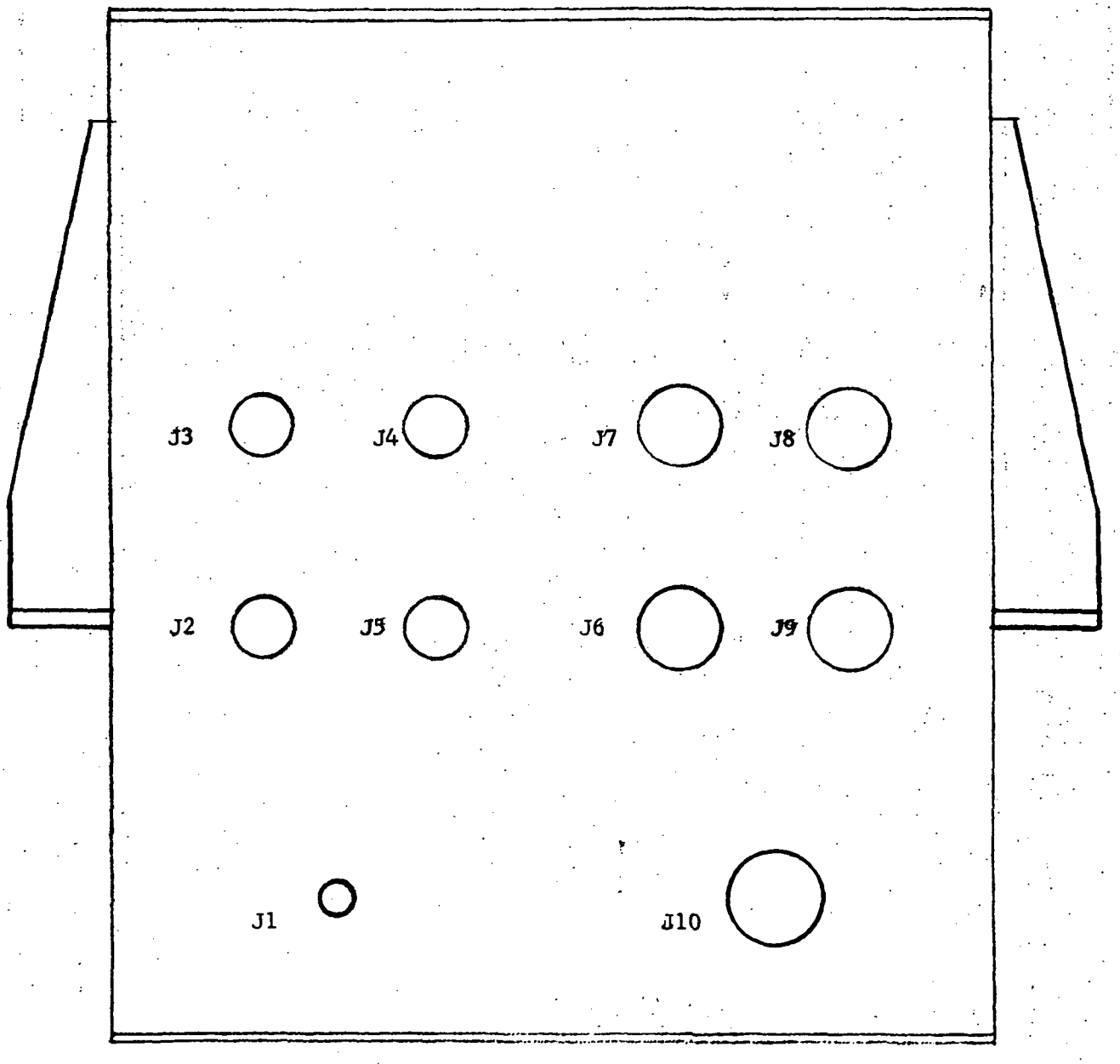
MDU

Input power: 23 watts @ 28 VDC
Local bus signal amplitudes: Positive going +4 ±10% VDC
Negative going -4 ±10% VDC
Zero level -0.7 to +0.7 VDC

2. Data Terminal

a. Installation and Operation

While the installation of the data terminal in a system is relatively simple, certain precautions must be observed. Wiring to the connectors should conform with the connector arrangement drawing, Figure 2 , and with the Pin Assignment list, Table 4. Cables should be 75 ohm shielded twisted pair similar to Trompeter, TWC-78-2. If the data terminal is interfaced via the main buses to only one other piece of gear, such as the bus controller no line termination is required. However, if several



DATA TERMINAL CONNECTOR ARRANGEMENT

FIGURE 2.

TABLE 4

DATA TERMINAL CONNECTOR PIN ASSIGNMENTS

J1-A, B	+28 VDC
C, D	+28 V RET
J2-A	Main Data Bus A1
L	Main Data Bus A1 RET.
M	Main Data Bus A1 Shield
C	Main Data Bus A2
B	Main Data Bus A2 RET
N	Main Data Bus A2 Shield
E	Main Sup. Bus A1
D	Main Sup. Bus A1 RET
P	Main Sup. Bus A1 Shield
H	Main Sup. Bus A2
G	Main Sup. Bus A2 RET
R	Main Sup. Bus A2 Shield

J3, J4, J5 are wired the same as J2 but for channels B, C, D respectively.

J6-B	Local Sup. Bus A
C	Local Sup. Bus A RET
A	Local Sup. Bus A Shield
H	Local Output Bus A
G	Local Output Bus A RET
J	Local Output Bus A Shield
E	Local Input Bus A
L	Local Input Bus A RET
K	Local Input Bus A Shield

J7, J8, J9 are wired the same as J6 but for channels B, C, D, respectively.

J10-A	Clock A
B	Sync A
C	GND A
D	Clock B
E	Sync B
F	GND B
G	Clock C
H	Sync C
J	GND C
K	Clock D
L	Sync D
M	GND D

stations are daisy chained along the line, a matching load resistor will be required on the line at points most distant from the transmitter. In the case of the supervisory bus a 75 ohm resistor would be located at the most remote point from the bus controller. In the case of the data bus, however, the line must always have some termination at the controller and the most remote station. Depending on cable lengths, the matching impedances are not necessarily restricted to as low a value as the cable characteristic impedance. However, if the cables are longer than 200 feet characteristic termination is likely necessary.

Since terminations on the lines do load line drivers, the drive capability must be adequate to drive the terminations at required voltage levels. It has already been specified that the prototype data terminal requires plus and minus 4 volts. Obviously this may result in undesirably high powers. The power consumption can be reduced by increasing receiver amplifier gains for operation at lower signal levels. This is fairly easily done by changing the feedback resistors. Increasing receiver gains, however, is not done without penalty. Signal to noise ratios are reduced but this penalty may be acceptable if the amplifier gains aren't made greater than 3.

No terminations will be required on local buses to the MDU since these lines are all 50 feet or less.

All bus controllers and/or other interfacing equipment must have line driver circuits with the appropriate 5-bit information skewing between the quad redundant buses, and this skew must be accurate to 1/2 bit. Since local buses are not redundant to the MDU, no such criterion exists for local buses.

b. Testing

No specific test routines are recommended here for installed systems, except the general procedure of the Functional Test Plan and Procedure MCR-72-66 can be followed. This plan can be used directly if a basic system of a central controller one data terminal, and one or more MDU's is involved. If the system is more complex various procedures must be established. General test routines can be established to monitor and correlate command functions, input/output data, and status. Automatic test routines and data analyses can be performed by interfacing the system with a computer.

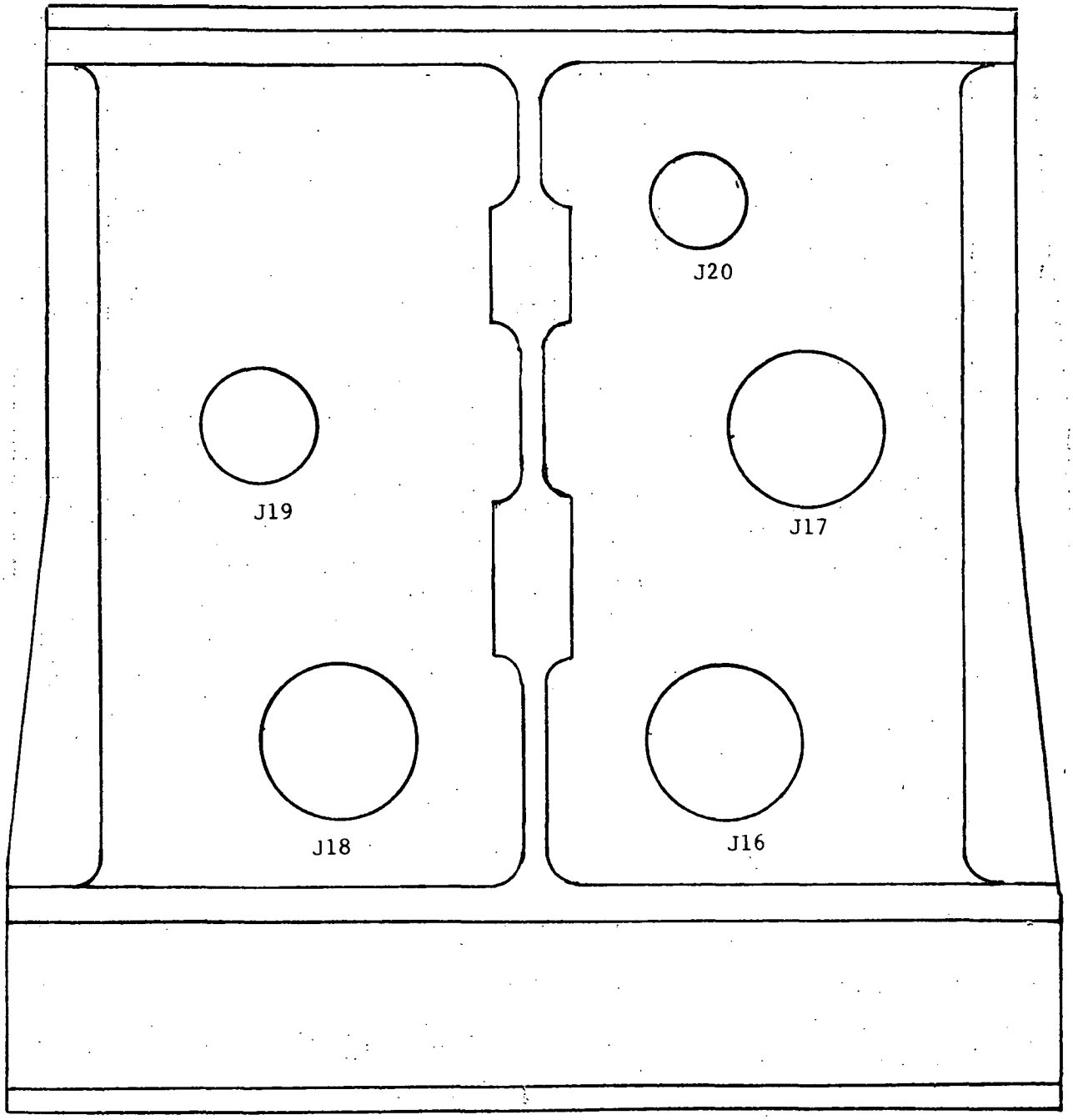
3. Multiplexer/Demultiplexer

a. Installation and Operation

Only minimal precautions are necessary in the installation of the MDU. All wiring connections must conform with the Connector Arrangement Drawing Figure 3, and the Connector Pin Assignment List, Table 5. Again shielded twisted pair are the recommended cables. As previously stated, local buses require no terminating loads. The terminations to the subsystem data input/output circuits are also not critical except they must conform to the requirements of the specifications. The prototype MDU is wired to operate with the address words listed in Table 6.

b. Testing

Again no specific test routines are recommended for installed systems except for the general procedures of the Functional Test Plan and Procedure MCR-72-66. Without an automated routine most testing is more readily performed with Mode A connection because of difficulties in bookkeeping in Mode B. General accuracy and data reproducibility is easily tested in either mode but fault and impedance tests are difficult with Mode B connections. Although the prototype MDU is constructed in Mode B configuration most acceptance testing was done in Mode A. Therefore, a computerized check program looks especially appealling with Mode B operation.



MDU CONNECTOR ARRANGEMENT

FIGURE 3.

TABLE 5

MDU CHASSIS PIN CONNECTOR ASSIGNMENTS

ANALOG INPUT CONNECTOR J16

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	Channel 1H	31	Channel 11H
2	Channel 1L	32	Channel 11L
3		33	
4	Channel 2H	34	Channel 12H
5	Channel 2L	35	Channel 12L
6		36	Chassis
7	Channel 3H	37	Channel 13H
8	Channel 3L	38	Channel 13L
9	Chassis	39	
10	Channel 4H	40	Channel 14H
11	Channel 4L	41	Channel 14L
12		42	
13	Channel 5H	43	Channel 15H
14	Channel 5L	44	Channel 15L
15		45	Chassis
16	Channel 6H	46	Channel 16H
17	Channel 6L	47	Channel 16L
18	Chassis	48	
19	Channel 7H	49	Channel 17H
20	Channel 7L	50	Channel 17L
21		51	
22	Channel 8H	52	Channel 18H
23	Channel 8L	53	Channel 18L
24		54	Chassis
25	Channel 9H	55	Channel 19H
26	Channel 9L	56	Channel 19L
27	Chassis	57	
28	Channel 10H	58	Channel 20H
29	Channel 10L	59	Channel 20L
30		60	

MDU CHASSIS PIN CONNECTOR ASSIGNMENTS

ANALOG INPUT CONNECTOR J16 (CONT.)

PIN NO.	SIGNAL	PIN NO.	SIGNAL
61	Channel 21H	87	Channel 31L
62	Channel 21L	88	Channel 30H
63	Chassis	89	Channel 30L
64	Channel 22H	90	Chassis
65	Channel 22L	91	Channel 31H
66			
67	Channel 23H		
68	Channel 23L		
69			
70	Channel 24H		
71	Channel 24L		
72	Chassis		
73	Channel 25H		
74	Channel 25L		
75			
76	Channel 26H		
77	Channel 26L		
78	Chassis		
79	Channel 27H		
80	Channel 27L		
81	Channel 32L		
82	Channel 28H		
83	Channel 28L		
84	Channel 32H		
85	Channel 29H		
86	Channel 29L		

MDU CHASSIS PIN CONNECTOR ASSIGNMENTS

BINARY INPUT CONNECTOR J17

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	Channel 1H	28	Channel 10H
2	Channel 1L	29	Channel 10L
3		30	
4	Channel 2H	31	Channel 11H
5	Channel 2L	32	Channel 11L
6		33	
7	Channel 3H	34	Channel 12H
8	Channel 3L	35	Channel 12L
9	Chassis	36	Chassis
10	Channel 4H	37	Channel 13H
11	Channel 4L	38	Channel 13L
12		39	
13	Channel 5H	40	Channel 14H
14	Channel 5L	41	Channel 14L
15		42	
16	Channel 6H	43	Channel 15H
17	Channel 6L	44	Channel 15L
18	Chassis	45	Chassis
19	Channel 7H	46	Channel 16H
20	Channel 7L	47	Channel 16L
21		48	
22	Channel 8H	49	Channel 17H
23	Channel 8L	50	Channel 17L
24		51	
25	Channel 9H	52	Channel 18H
26	Channel 9L	53	Channel 18L
27	Chassis	54	Chassis

MDU CHASSIS PIN CONNECTOR ASSIGNMENTS

BINARY INPUT CONNECTOR J17 (CONT.)

PIN NO.	SIGNAL	PIN NO.	SIGNAL
55	Channel 19H	84	Channel 32H
56	Channel 19L	85	Channel 29H
57		86	Channel 29L
58	Channel 20H	87	Channel 31L
59	Channel 20L	88	Channel 30H
60		89	Channel 30L
61	Channel 21H	90	Chassis
62	Channel 21L	91	Channel 31H
63	Chassis		
64	Channel 22H		
65	Channel 22L		
66			
67	Channel 23H		
68	Channel 23L		
69			
70	Channel 24H		
71	Channel 24L		
72	Chassis		
73	Channel 25H		
74	Channel 25L		
75			
76	Channel 26H		
77	Channel 26L		
78	Chassis		
79	Channel 27H		
80	Channel 27L		
81	Channel 32L		
82	Channel 28H		
83	Channel 28L		

MDU CHASSIS PIN CONNECTOR ASSIGNMENTS

RSM 04-27-30 PX J18

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	Bit 2 Binary Data 17 Out	30	Bit 12 Binary Data Out
2	Bit 3 Binary Data 17 Out	31	Bit 13 Binary Data Out
3	Bit 4 Binary Data 17 Out	32	Bit 14 Binary Data Out
4	Bit 5 Binary Data 17 Out	33	Bit 15 Binary Data Out
5	Bit 6 Binary Data 17 Out	34	Bit 16 Binary Data Out
6	Bit 7 Binary Data 17 Out	35	Bit 17 Binary Data Out
7	Bit 8 Binary Data 17 Out	36	GND
8	Bit 9 Binary Data 17 Out	37	GND
9	Bit 10 Binary Data 17 Out	38	GND
10	Bit 11 Binary Data 17 Out	39	Analog Chan. 1 Data Out
11	Bit 12 Binary Data 17 Out	40	Analog Chan. 2 Data Out
12	Bit 13 Binary Data 17 Out	41	Analog Chan. 3 Data Out
13	Bit 14 Binary Data 17 Out	42	Analog Chan. 4 Data Out
14	Bit 15 Binary Data 17 Out	43	Analog Chan. 5 Data Out
15	Bit 16 Binary Data 17 Out	44	Analog Chan. 6 Data Out
16	Bit 17 Binary Data 17 Out	45	Analog Chan. 7 Data Out
17	GND	46	Analog Chan. 8 Data Out
18	GND	47	Analog Chan. 9 Data Out
19	GND	48	Analog Chan. 10 Data Out
20	Bit 2 Binary Data Out	49	GND
21	Bit 3 Binary Data Out	50	GND
22	Bit 4 Binary Data Out	51	GND
23	Bit 5 Binary Data Out	52	Analog Chan. 11 Data Out
24	Bit 6 Binary Data Out	53	Analog Chan. 12 Data Out
25	Bit 7 Binary Data Out	54	Analog Chan. 13 Data Out
26	Bit 8 Binary Data Out	55	Analog Chan. 14 Data Out
27	Bit 9 Binary Data Out	56	Analog Chan. 15 Data Out
28	Bit 10 Binary Data Out	57	Analog Chan. 16 Data Out
29	Bit 11 Binary Data Out	58	Analog Chan. 17 Data Out

MDU CHASSIS PIN CONNECTOR ASSIGNMENTS

RSM 04-27-30 PX J18 (CONT.)

PIN NO.	SIGNAL	PIN NO.	SIGNAL
59	Analog Chan. 18 Data Out	90	
60	Analog Chan. 19 Data Out	91	Sync Inhibit
61	Analog Chan. 20 Data Out		
62	GND		
63	GND		
64	GND		
65	Analog Chan. 21 Data Out		
66	Analog Chan. 22 Data Out		
67	Analog Chan. 23 Data Out		
68	Analog Chan. 24 Data Out		
69	Analog Chan. 25 Data Out		
70	Analog Chan. 26 Data Out		
71	Analog Chan. 27 Data Out		
72	Analog Chan. 28 Data Out		
73	Analog Chan. 29 Data Out		
74	Analog Chan. 30 Data Out		
75	Analog Chan. 31 Data Out		
76	Analog Chan. 32 Data Out		
77	Chassis		
78	Chassis		
79	Chassis		
80	Chassis		
81	Chassis		
82	Chassis		
83			
84			
85			
86			
87			
88			
89			

MDU CHASSIS PIN CONNECTOR ASSIGNMENTS

LOCAL BUSES J19

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	Address		
2	Address Return (Iso. GND)		
3	RZ Data In		
4	Data Return (Iso. GND)		
5	NRZ Data Out		
6	NRZ Data Return (Iso. GND)		
7	Chassis		
8	Chassis		
9	Chassis		
10			
11			
12			
13			
14			
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25			

MDU CHASSIS PIN CONNECTOR ASSIGNMENTS

POWER INPUT J-20

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	+28 VDC		
2	+28V Common		
3	Chassis		
4			
5			
6			
7			
8			
9			
10			
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23			
24			
25			

TABLE 6

ALL MULTIPLEXER ADDRESSES

Channel	Bit No. 1 thru 9	10	11	12	13	14	15	16	17	18	19
Analog 2,1	X → X	0	0	1	0	0	0	0	0	0	1
18,17							0	0	0	1	0
4,3							0	0	0	1	1
20,19							0	0	1	0	0
6,5							0	0	1	0	1
22,21							0	0	1	1	0
8,7							0	0	1	1	1
24,33							0	1	0	0	0
10,9							0	1	0	0	1
36,25							0	1	0	1	0
12,11							0	1	0	1	1
28,27							0	1	1	0	0
14,13							0	1	1	0	1
30,29							0	1	1	1	0
16,15							0	1	1	1	1
32,31							1	0	0	0	0
Bin. Wrd. 17							1	0	0	0	1
Bin. Wrd. 18							1	0	0	1	0

DEMULTIPLEXER ADDRESSES

Channel	Bit No. 1 thru 11	12 13	14	15	16	17	18	19
	Serial No. ALL	ALL	123	123	123	123	123	123
Analog 1,2	X → X	0 1	011	001	000	000	000	100
3,4					000	000	000	111
5,6					000	000	111	000
7,8					000	000	111	111
9,10					000	111	000	000
11,12					000	111	000	111
13,14					000	111	111	000
15,16					000	111	111	111
17,18					111	000	000	000
19,20					111	000	000	111
21,22					111	000	111	000
23,24					111	000	111	111
25,26					111	111	000	000
27,28					111	111	000	111
29,30					111	111	111	100
31,32				1	011	011	011	011
Bin. Wrd. 17			00	11	000	001	010	100
Bin. Wrd. 18			00	11	000	001	110	011

Rev. A, 12/11/72

LOCAL DATA WORD FROM DATA TERMINAL

BIT POSITION	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Analog	X	MSB							LSB	MSB							LSB	X	X
	ODD CHANNEL									EVEN CHANNEL									
Binary	X	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	X	X

V. DRAWINGS

1. Drawing List

NUMBER	SHEETS	TITLE
380-1	1	Assy. - Remote Multiplexer/Demultiplexer Unit
380-2	1	Multiplexer/Demultiplexer - Housing
380-3	1	Multiplexer/Demultiplexer - Retainer Support
380-4	1	Multiplexer/Demultiplexer - Cover, Top
380-5	1	Multiplexer/Demultiplexer - Collar
380-10	1	Multiplexer/Demultiplexer - Isometric View
380-13	1	Multiplexer/Demultiplexer - Seal, Top
380-14	1	Multiplexer/Demultiplexer - Cover, Bottom
380-15	1	Multiplexer/Demultiplexer - O-ring Seal
380-19	1	Multiplexer/Demultiplexer - Block Diagram
380-20	1	Electrical Schematic - Multiplexer/ Demultiplexer - Multiplexer Decoder, Programmable Level
380-21	1	Electrical Schematic - Multiplexer/Demultiplexer - Multiplexer Decoder, First Level
380-22	2	Electrical Schematic - Multiplexer/ Demultiplexer - Control Logic and Multiplexer Data Output Line Driver
380-23	3	Electrical Schematic - Multiplexer/ Demultiplexer - Address Input Logic, Multiplex Address Register
380-24	3	Electrical Schematic - Multiplexer/ Demultiplexer - Data Receiver, Binary Demultiplexer, 2 Analog Demultiplexers
380-25	2	Electrical Schematic - Multiplexer/Demultiplexer - Demultiplexer Decoder
380-26	5	Electrical Schematic - Multiplexer/ Demultiplexer - 10 Channel Analog Demultiplexer Board

NUMBER	SHEETS	TITLE
380-27	1	Electrical Schematic - Multiplexer/ Demultiplexer - A/D Converter and Output Data Register
380-28	1	Electrical Schematic - Multiplexer/ Demultiplexer - Multiplexer
380-29	1	Electrical Schematic - Multiplexer/ Demultiplexer - Analog/Binary Signal Conditioner
380-30	2	Printed Circuit Board - MDU - Multiplexer Decoder, Programmable Level
380-31	2	Printed Circuit Board - MDU - Multiplexer Decoder, First Level
380-32	2	Printed Circuit Board - MDU - Detail - Multiplexer/Demultiplexer - Control Logic, Mux, Data Output, Line Driver
380-33	2	Printed Circuit Board - MDU - Address Input Logic, Mux. Address Register
380-34	2	Printed Circuit Board - MDU - Data Receiver, Binary Demultiplexer, 2 Channel Analog Demultiplexer
380-35	2	Printed Circuit Board - MDU - Demultiplexer Decoder
380-36	2	Printed Circuit Board - MDU - 10 Channel Analog Demultiplexer
380-37	2	Printed Circuit Board - MDU - A to D Converter and Output Data Register
380-38	2	Printed Circuit Board - MDU - Multiplexer
380-39	2	Printed Circuit Board - MDU - Analog/Binary Signal Conditioner
380-40	1	Assy. - Multiplexer/Demultiplexer - Multiplexer Decoder, Programmable Level

NUMBER	SHEETS	TITLE
380-42	1	Assy. - Multiplexer/Demultiplexer - Control Logic, Multiplex Data Outputs, Line Driver
380-43	1	Assy. - Multiplexer/Demultiplexer - Address Input Logic, Multiplex Address Register
380-44	1	Assy. - Multiplexer/Demultiplexer - Data Receiver, Binary Demultiplexer, 2 Channels Analog Demultiplexer
380-45	1	Assy. - Multiplexer/Demultiplexer - Demultiplexer Decoder
380-46	1	Assy. - Multiplexer/Demultiplexer - 10 Channels Analog Demultiplexer
380-47	1	Assy. - Multiplexer Demultiplexer - A to D Converter and Output Data Register
380-48	1	Assy. - Multiplexer/Demultiplexer - Multiplexer
380-49	1	Assy. - Multiplexer/Demultiplexer - Analog/Binary Signal Conditioner
380-52	1	Multiplexer/Demultiplexer - MDU Timing Diagrams
380-53	3	Multiplexer/Demultiplexer - Control Logic Timing Diagrams
380-54	1	Multiplexer/Demultiplexer - Demultiplexer Timing Diagrams
380-110	2	Data Terminal-Block Diagram
380-111	12	Electrical Schematic - Data Terminal - Supervisory Word Logic
380-112	11	Electrical Schematic - Data Terminal - Input Data Word and Memory Logic
380-113	12	Electrical Schematic - Data Terminal - Control and Output Data Logic

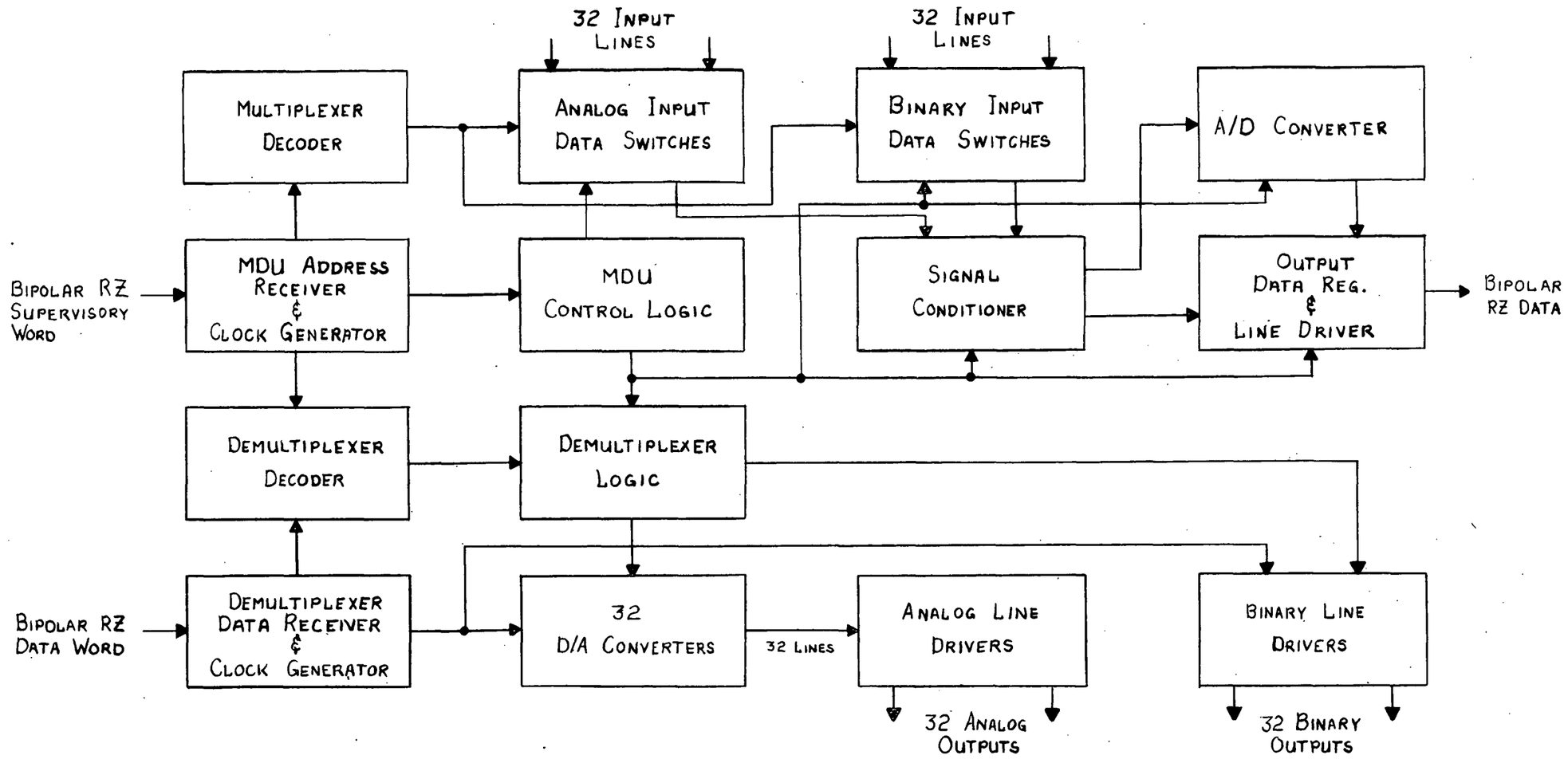
NUMBER	SHEETS	TITLE
380-114	7	Electrical Schematic - Data Terminal - Line Drivers and Receivers
380-140	1	Assy. - Data Terminal - Line Driver, Line Receiver
4100-29	1	Assy. - Power Supply
4100-59	1	Electrical Schematic - Power Supply
4100-63	1	Power Supply - Power Supply Housing Insulator and Washer
4100-66	1	Power Supply - Transformer
4100-67	1	Power Supply - Transformer
4100-68	1	Power Supply - Transformer
4100-69	1	Power Supply - Inductor Filter
4100-70	1	Power Supply - Inductor
4100-71	1	Assy. - Power Supply - Input Filter
4100-72	1	Assy. - Power Supply - Pre-Regulator
4100-73	1	Power Supply - Assy., Converter-Rectifier; Insulator
4100-74	1	Assy. - Power Supply - Output Filter
4100-81	2	Power Supply - Printed Wiring Board
4100-82	2	Power Supply - Printed Wiring Board
4100-83	2	Power Supply - Printed Wiring Board
4100-84	2	Power Supply - Printed Wiring Board
25738-100	1	Assy. - Data Terminal
25738-200	1	Assy. - Data Terminal - Case
25738-201	1	Data Terminal - Side Plate

NUMBER	SHEETS	TITLE
380-41	1	Assy. - Multiplexer/Demultiplexer - Multiplexer Decoder, First Level
25738-202	1	Data Terminal - End Plate
25738-203	1	Data Terminal - Cover, Top, and Bottom
25738-204	1	Data Terminal - Power Supply - Plate
25738-205	1	Data Terminal - P.C. Connector - Plate
25738-206	1	Data Terminal - Support Rail
380-31	1	Printed Circuit Board - Data Terminal - Redundant Line Drivers and Receivers

2. Included Drawings

The following drawings are included in this report:

380-19	
380-22	2 Sheets
380-23	3 Sheets
380-24	3 Sheets
380-25	2 Sheets
380-26	5 Sheets
380-29	
380-52	
380-53	3 Sheets
380-54	
380-110	2 Sheets
380-111	12 Sheets
380-112	11 Sheets
380-113	12 Sheets
380-114	7 Sheets
4100-59	
380-20	
380-21	
380-28	
380-29	

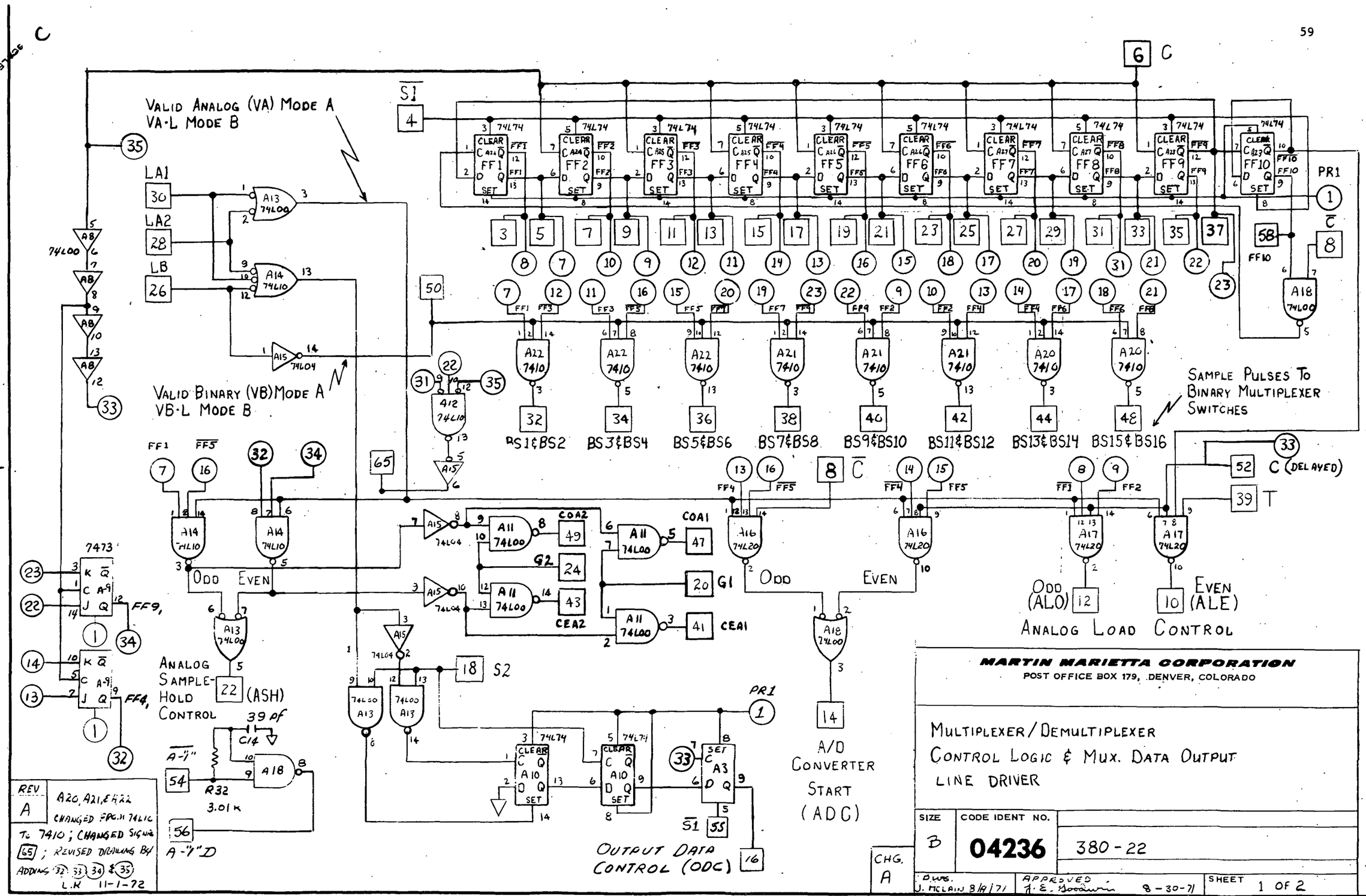


MARTIN MARIETTA CORPORATION
POST OFFICE BOX 179, DENVER, COLORADO

MULTIPLEXER/DEMULTIPLEXER
BLOCK DIAGRAM

SIZE	CODE IDENT NO.	
B	04236	380-19

DWG. J. MCLAIN 8/19/71 | APPROVED J. E. Goodwin 8-30-71 | SHEET 1 OF 1



REV	
A	A20, A21, & A22 CHANGED FROM 74LIC TO 7410; CHANGED SIGNAL 65; REVISED DRAWING BY ADDING 32 33 34 & 35 L.K 11-1-72

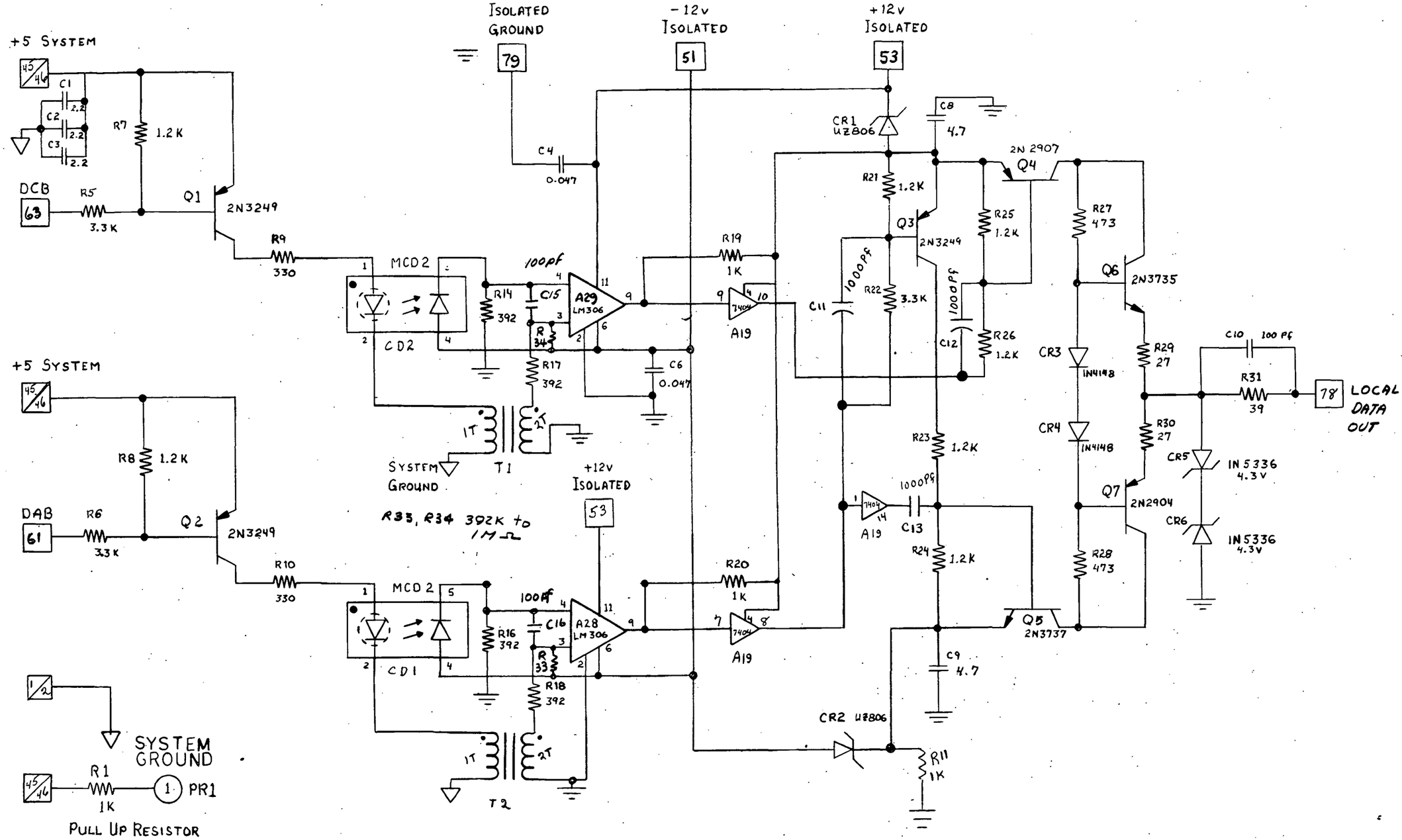
MARTIN MARIETTA CORPORATION
POST OFFICE BOX 179, DENVER, COLORADO

MULTIPLEXER/DEMULTIPLEXER
CONTROL LOGIC & MUX. DATA OUTPUT
LINE DRIVER

SIZE	CODE IDENT NO.	
B	04236	380-22

CHG.	DWG.	APPROVED	SHEET
A	J. McLAIN 8/9/71	J. E. Goodwin 8-30-71	1 OF 2

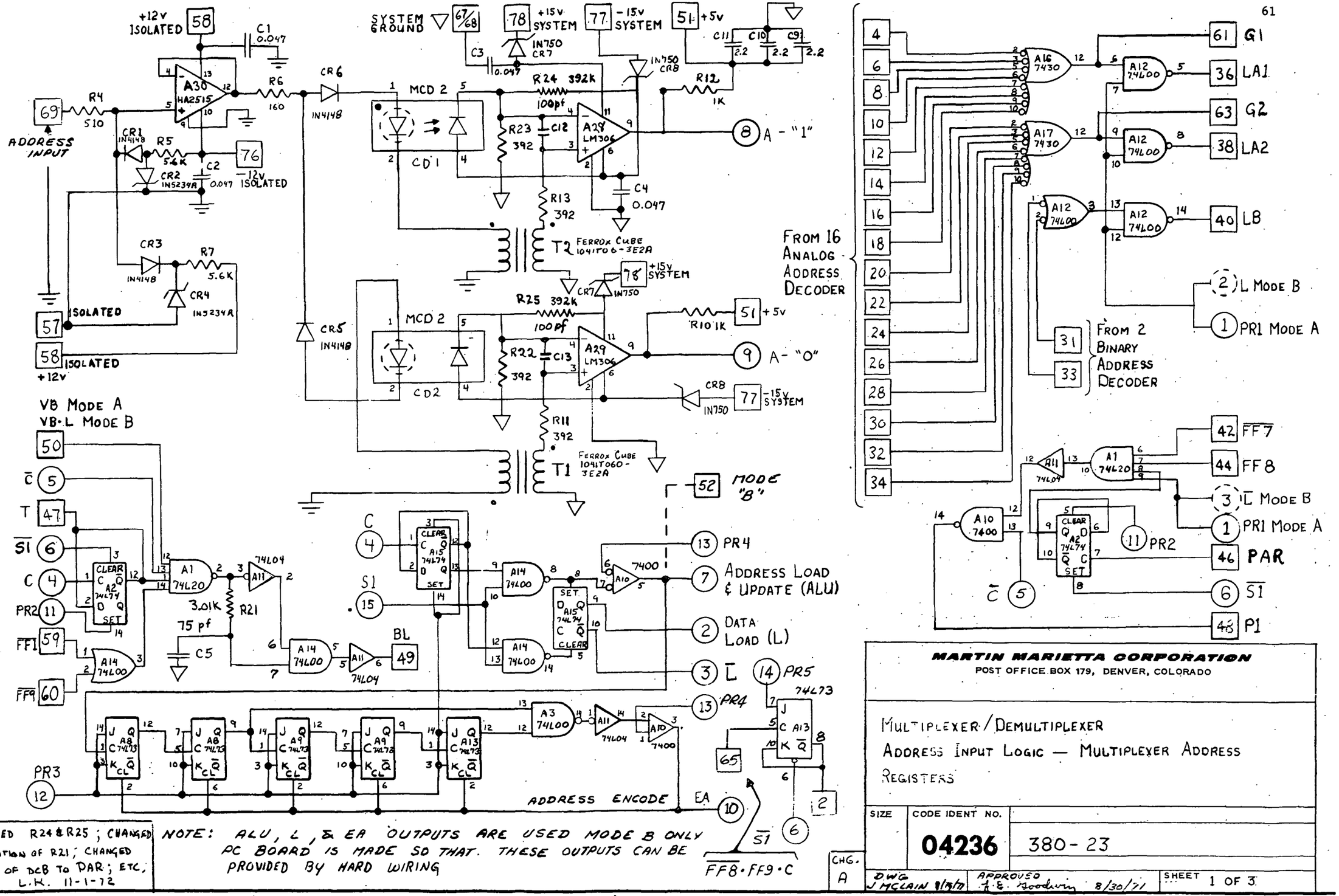
PRINTED IN USA OZALID 888-838



CHG. A: INTERCHANGED DAB & DCB
ADDED R33 + R34
L.K 11-1-72

SIZE	CODE IDENT NO.	
B	04236	380-22
CHG A		SHEET 2 OF 2

PRINTED IN USA OZALID 888-838
E-404D(2-62)



NOTE: ALU, L, & EA OUTPUTS ARE USED MODE B ONLY PC BOARD IS MADE SO THAT THESE OUTPUTS CAN BE PROVIDED BY HARD WIRING

REV	
A	ADDED R24 & R25; CHANGED LOCATION OF R21; CHANGED NAME OF DCB TO DAR; ETC. L.K. 11-1-72

CHG. A

MARTIN MARIETTA CORPORATION
POST OFFICE BOX 179, DENVER, COLORADO

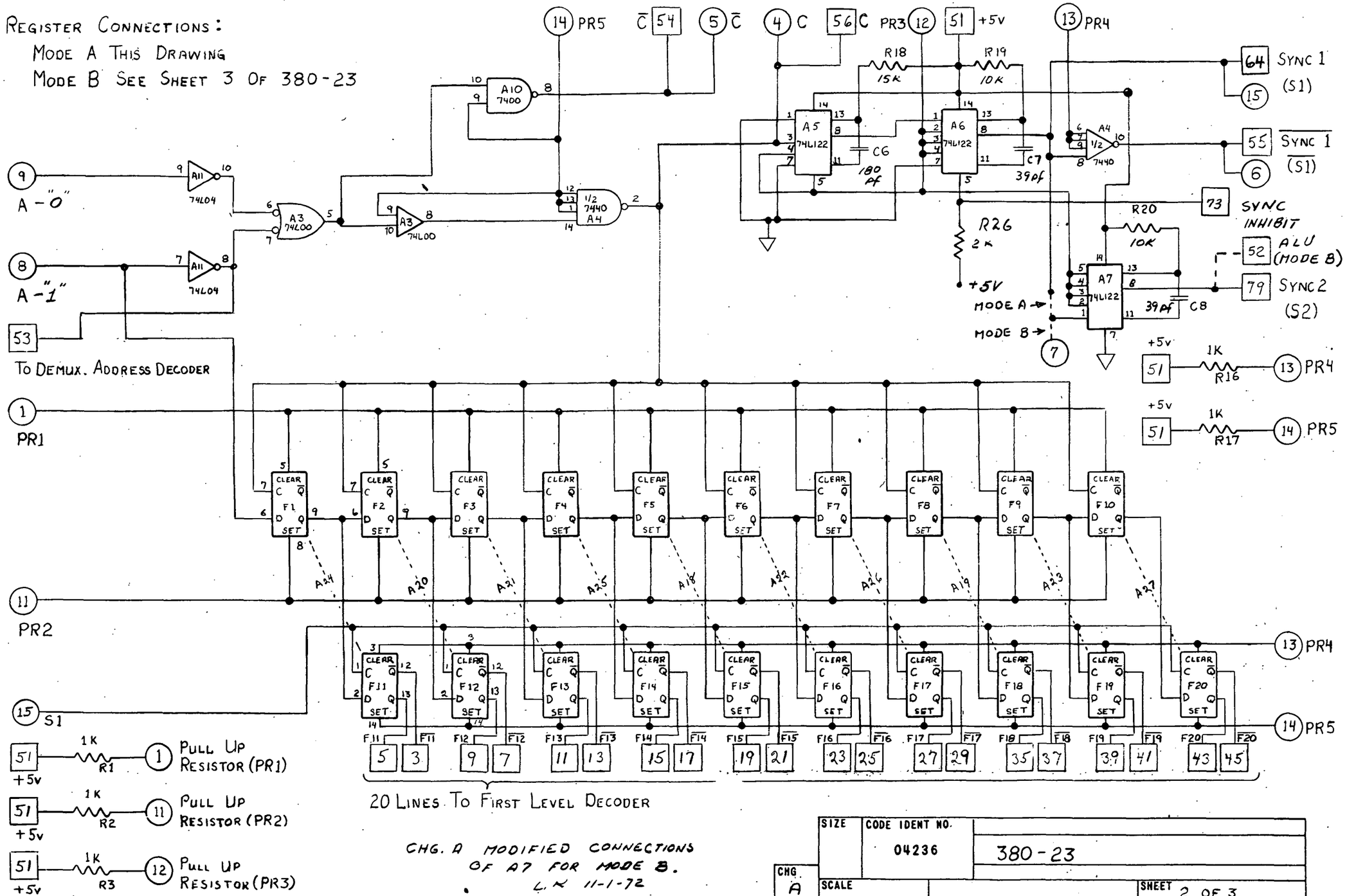
MULTIPLEXER / DEMULTIPLEXER
ADDRESS INPUT LOGIC — MULTIPLEXER ADDRESS REGISTERS

SIZE	CODE IDENT NO.	
	04236	380-23

DWG J MCLAIN 8/19/71 | APPROVED A. E. Goodwin 8/30/71 | SHEET 1 OF 3

PRINTED IN USA OZALID 888-838

REGISTER CONNECTIONS:
MODE A THIS DRAWING
MODE B SEE SHEET 3 OF 380-23



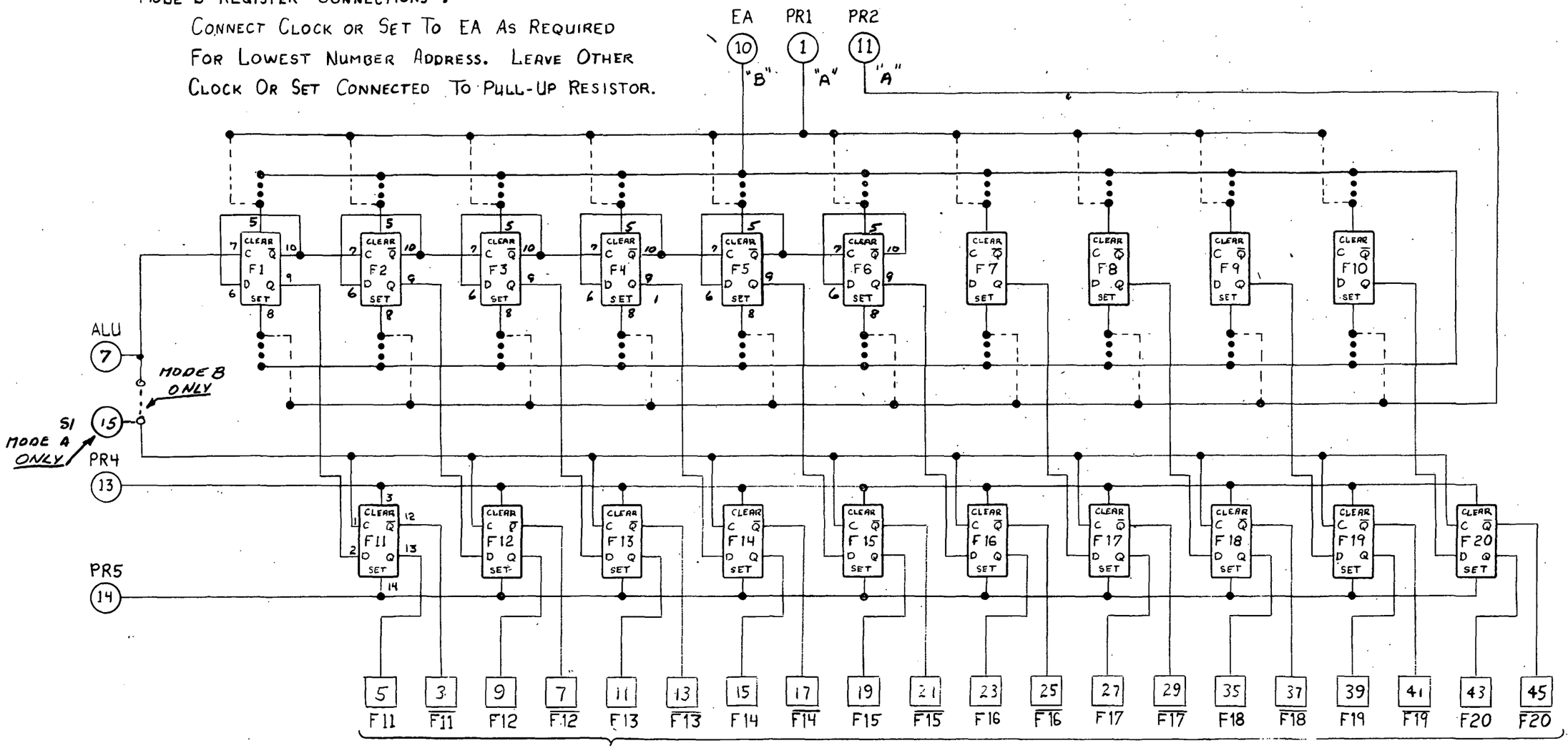
CHG. A MODIFIED CONNECTIONS OF A7 FOR MODE B.
L.K 11-1-72

SIZE	CODE IDENT NO.	
	04236	380-23
CHG A	SCALE	SHEET 2 OF 3

PRINTED IN USA OZALID 888-838
E-404D(2-62)

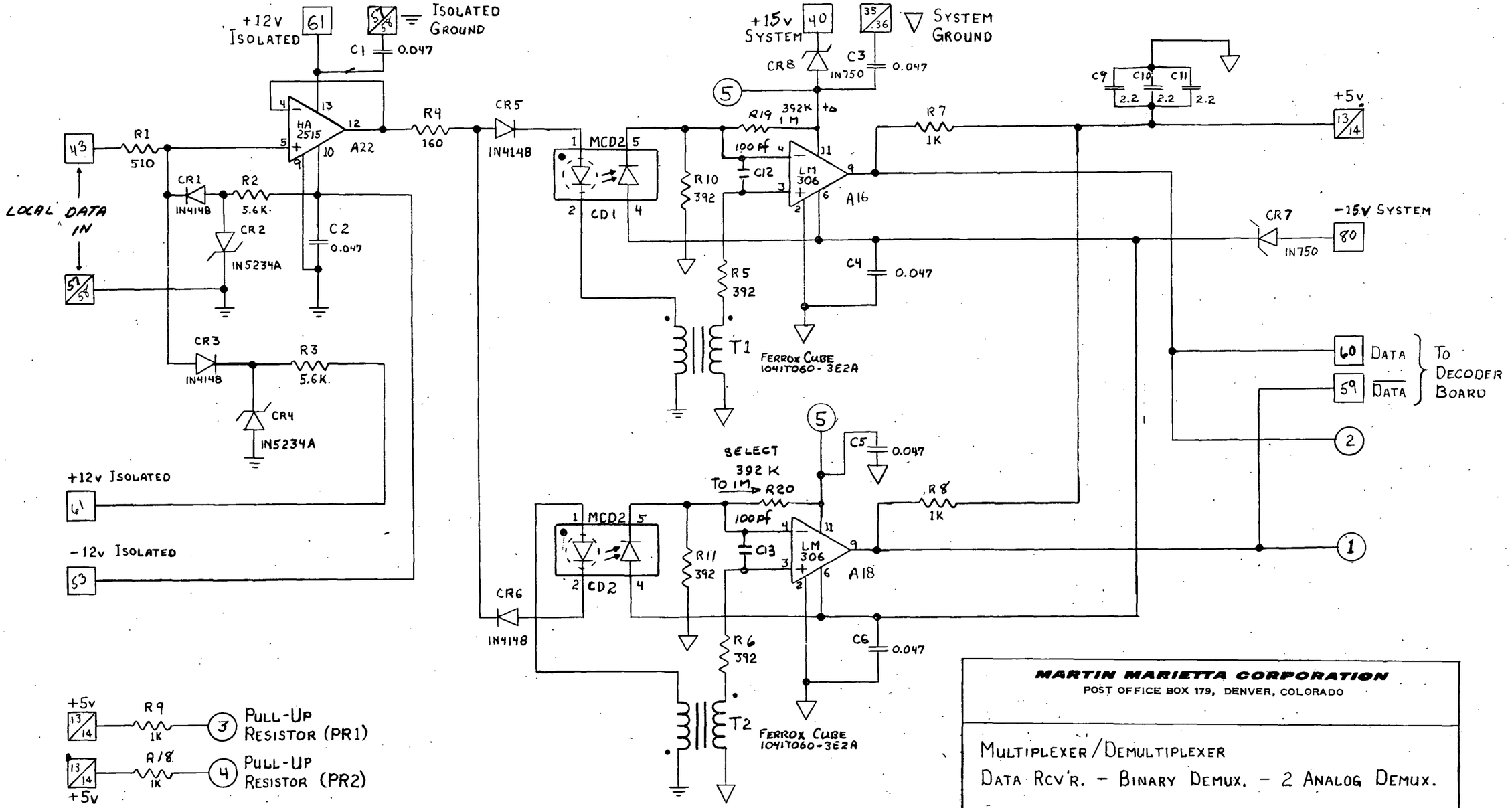
MODE B REGISTER CONNECTIONS :

CONNECT CLOCK OR SET TO EA AS REQUIRED FOR LOWEST NUMBER ADDRESS. LEAVE OTHER CLOCK OR SET CONNECTED TO PULL-UP RESISTOR.



20 LINES TO FIRST LEVEL DECODER

SIZE	CODE IDENT NO.	
	04236	380-23
CHG	SCALE	SHEET 3 OF 3



CHG. A ADD R19 & R20 SELECTED TO BALANCE OFFSET. L.K 11-1-72

MARTIN MARIETTA CORPORATION
POST OFFICE BOX 179, DENVER, COLORADO

MULTIPLEXER/DEMULTIPLEXER
DATA RCV'R. - BINARY DEMUX. - 2 ANALOG DEMUX.

SIZE	CODE IDENT NO.	
	04236	380-24

CHG	DWG	APPROVED	SHEET
A	J.MCLAIN 8/19/71	T.E. Goodwin 8/30/71	1 OF 3

BINARY DATA OUT WORD 17

20 21 22 23 24 25 26 27 28 29 30 31 32 34 33 37

A2 74L164 — A8 74L95 — A14 74L95 — A20 74L95 — A26 74L95

A1 74L164 — A7 74L95 — A13 74L95 — A19 74L95 — A25 74L95

A21 7400 — A27 7410

42 D17
41 $\overline{FF8}$
46 FF9
38 D18

3 PR1
4 PR2

13/14 +5v
C10

$\overline{D17}$ 44 — A21 7400 — 45 $\overline{D18}$

"1" DATA IN (2)

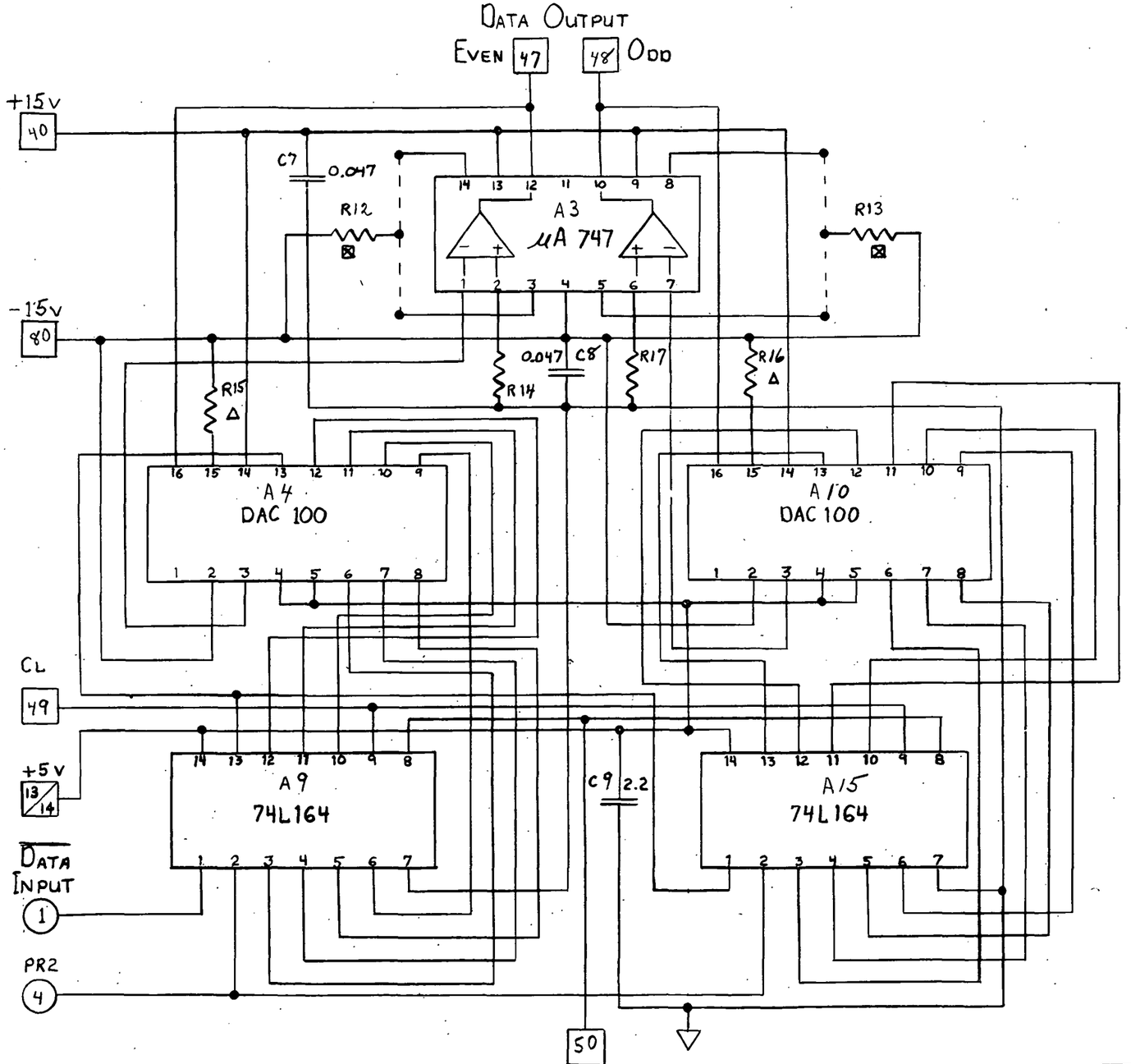
1 2 3 4 6 7 8 9 10 11 12 18 19 15 16 17

BINARY DATA OUT
WORD 18

CHG. A REWIRED FF9 TO 46 INSTEAD OF 39
L.K 11-1-72

CHG	SIZE	CODE IDENT NO.	
A		04236	380 - 24
	SCALE		SHEET 2 OF 3

E-404D(2-62)



ALL RESISTANCE VALUES IN OHMS.
ALL CAPACITOR VALUES IN μfd.

⊠ SELECT RESISTOR & CONNECTORS FOR ZERO VOLTAGE OUT WITH BINARY ZERO IN.

Δ SELECT RESISTOR FOR 5 VOLTS OUT OF AMPLIFIER WITH BINARY 5 VOLTS IN.

SIZE	CODE IDENT NO.	
	04236	380-24
CHG	SCALE	SHEET 3 OF 3

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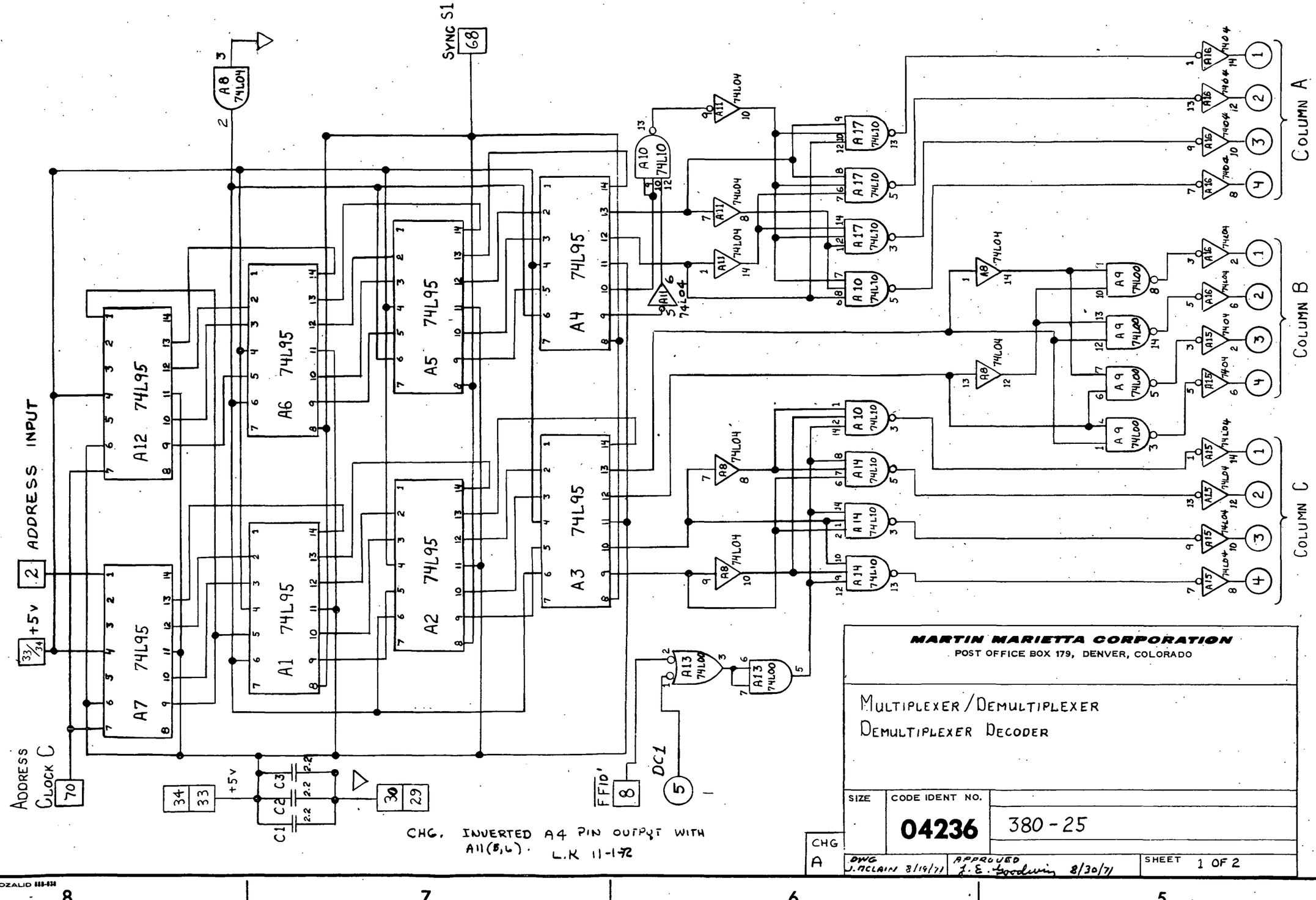
E-404D(2-62)



MARTIN MARIETTA CORPORATION
POST OFFICE BOX 179, DENVER, COLORADO

MULTIPLEXER / DEMULTIPLEXER
DEMULTIPLEXER DECODER

SIZE	CODE IDENT NO.	
	04236	380-25

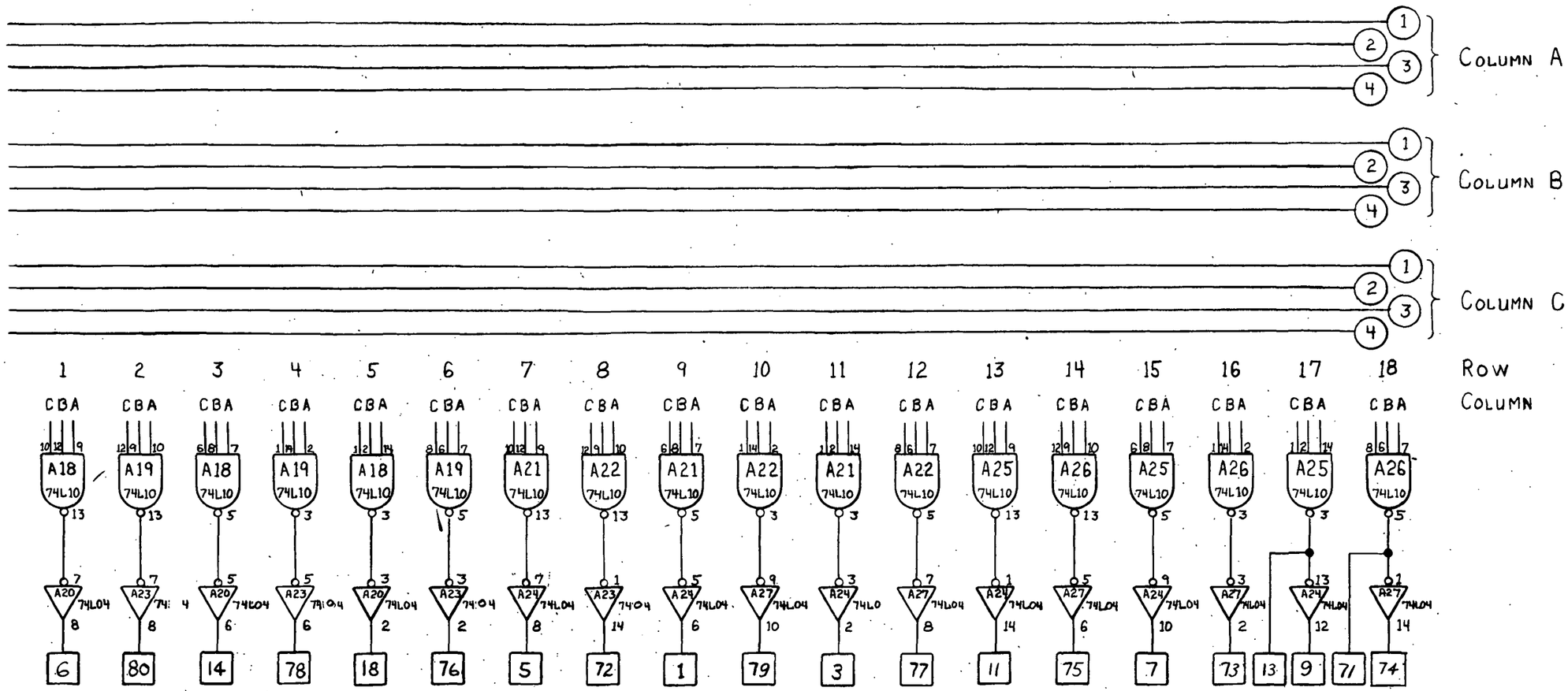
CHG A

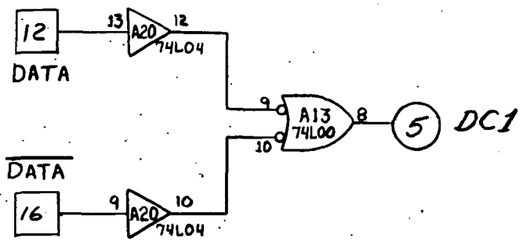
DWG J. MCLAIN 8/19/71 | APPROVED L. E. Goodwin 8/30/71 | SHEET 1 OF 2

PRINTED IN USA OZALID 888-838

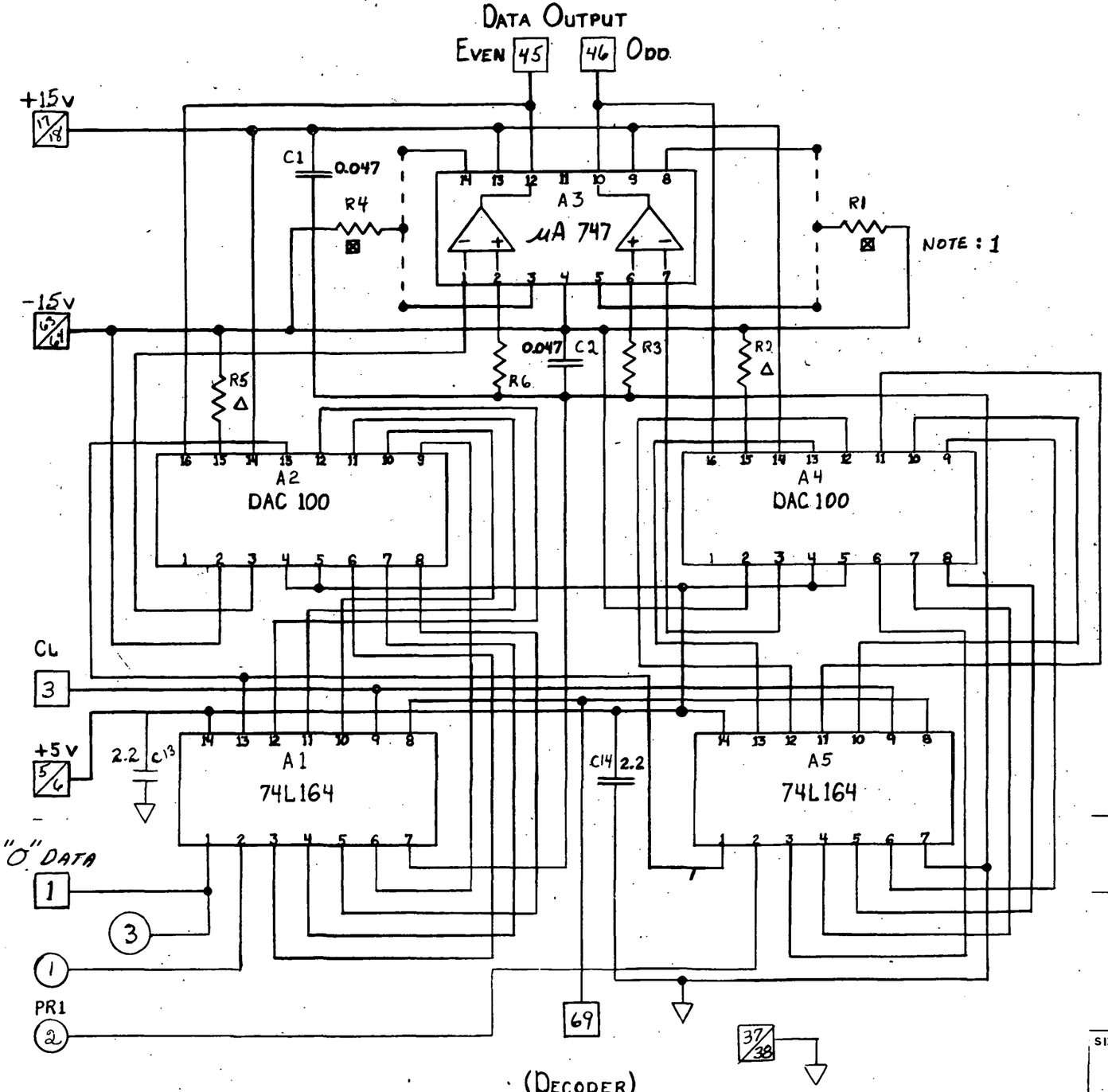
B A

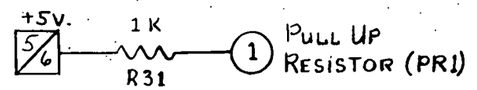
8 7 6 5





SIZE	CODE IDENT NO.	
	04236	380-25
CHG	SCALE	SHEET 2 OF 2





ALL RESISTANCE VALUES IN OHMS.
ALL CAPACITOR VALUES IN μfd.

⊠ SELECT RESISTOR & CONNECTORS FOR ZERO VOLTAGE OUT WITH BINARY ZERO IN.

Δ SELECT RESISTOR FOR 5 VOLTS OUT OF AMPLIFIER WITH BINARY 5 VOLTS IN. (0 to 200 Ω)

NOTE 1 : NO RESISTOR REQUIRED FOR ZERO ± 10 MV

MARTIN MARIETTA CORPORATION
POST OFFICE BOX 179, DENVER, COLORADO

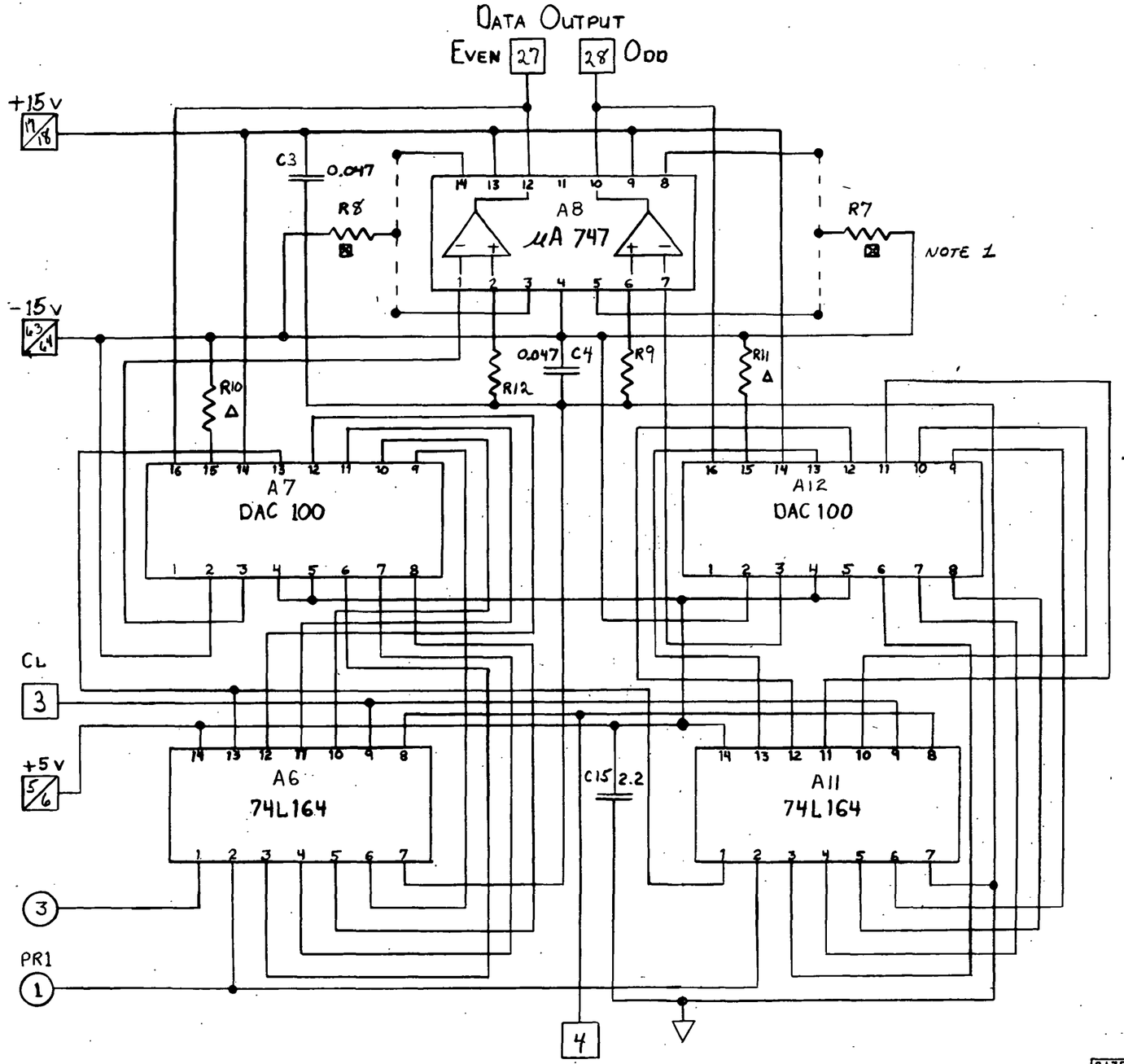
MULTIPLEXER / DEMULTIPLEXER
10 CHANNEL ANALOG DEMULTIPLEXER BOARD

SIZE	CODE IDENT NO.	
	04236	380-26

DWG. J MCLAIN 8/9/71 | APPROVED J. E. Goodwin 8/30/71 | SHEET 1 OF 5

B A

8 7 6 5



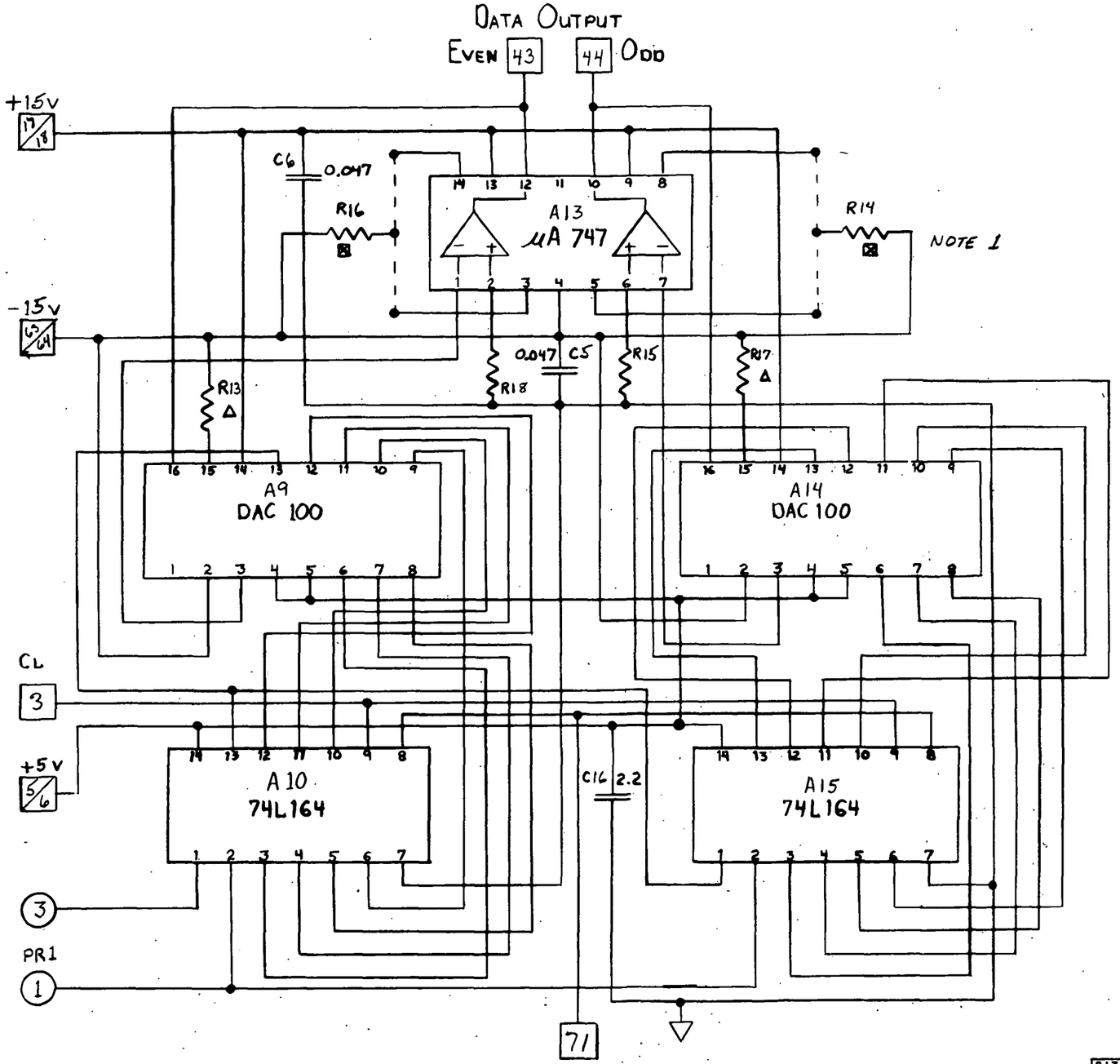
(DECODER)

ALL RESISTANCE VALUES IN OHMS.
ALL CAPACITOR VALUES IN μfd.

⊠ SELECT RESISTOR & CONNECTORS FOR ZERO VOLTAGE OUT WITH BINARY ZERO IN.

△ SELECT RESISTOR FOR 5 VOLTS OUT OF AMPLIFIER WITH BINARY 5 VOLTS IN. (0 to 200 Ω)

SIZE	CODE IDENT NO.	
	04236	380 - 26
CHG	SCALE	SHEET 2 OF 5



ALL RESISTANCE VALUES IN OHMS.
ALL CAPACITOR VALUES IN μfd.

⊠ SELECT RESISTOR & CONNECTORS FOR ZERO VOLTAGE OUT WITH BINARY ZERO IN.

Δ SELECT RESISTOR FOR 5 VOLTS OUT OF AMPLIFIER WITH BINARY 5 VOLTS IN. (0 TO 200 Ω)

SIZE	CODE IDENT NO.	
	04236	380-26
CHG	SCALE	SHEET 3 OF 5

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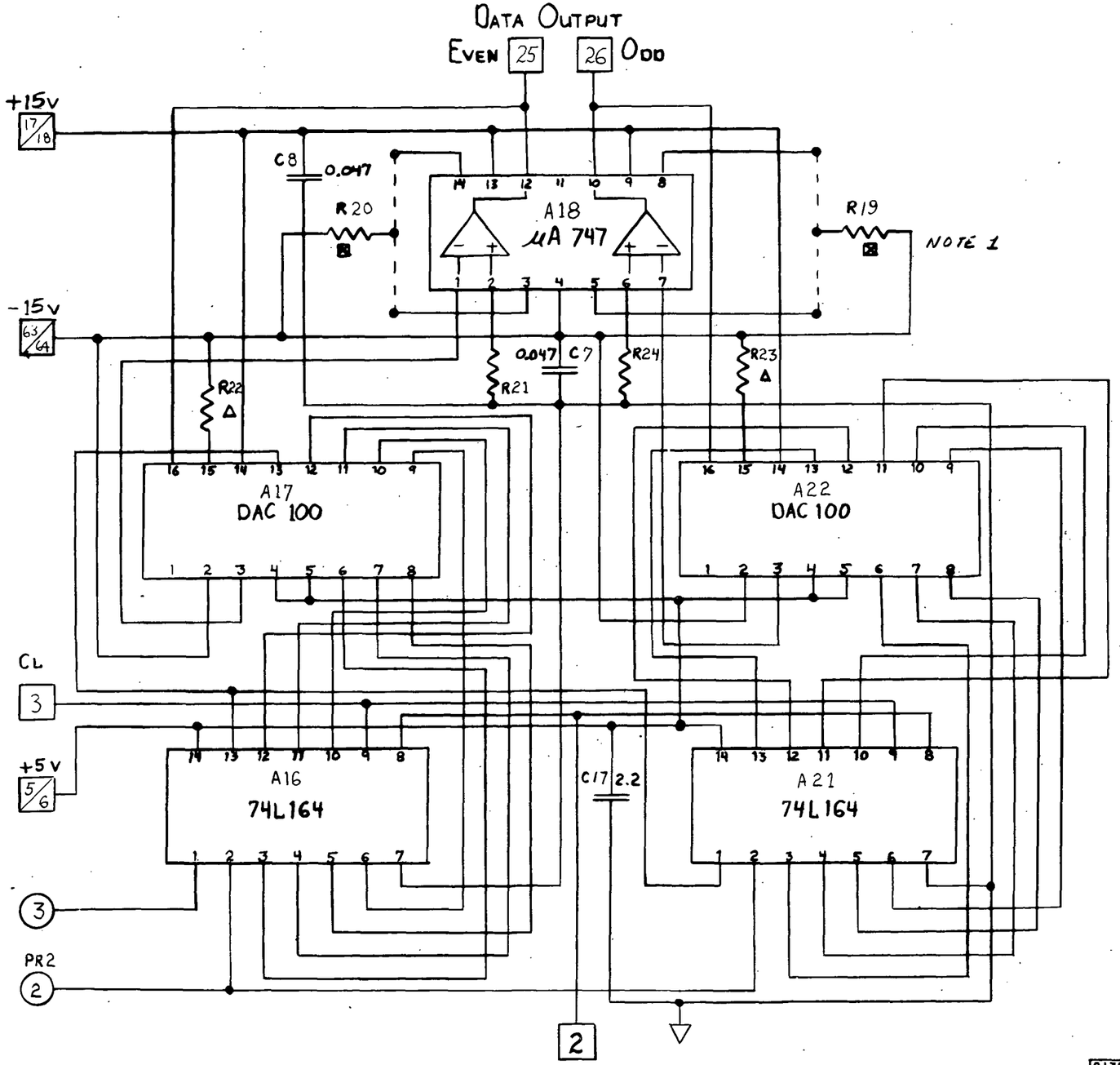
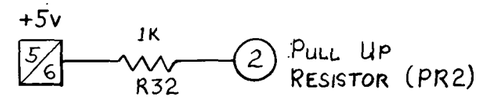
E-404D(2-62)





ALL RESISTANCE VALUES IN OHMS.
ALL CAPACITOR VALUES IN μfd.

⊠ SELECT RESISTOR & CONNECTORS FOR ZERO VOLTAGE OUT WITH BINARY ZERO IN.

Δ SELECT RESISTOR FOR 5 VOLTS OUT OF AMPLIFIER WITH BINARY 5 VOLTS IN. (0 to 200Ω)

SIZE	CODE IDENT NO.	
	04236	380-26
CHG	SCALE	SHEET 4 OF 5

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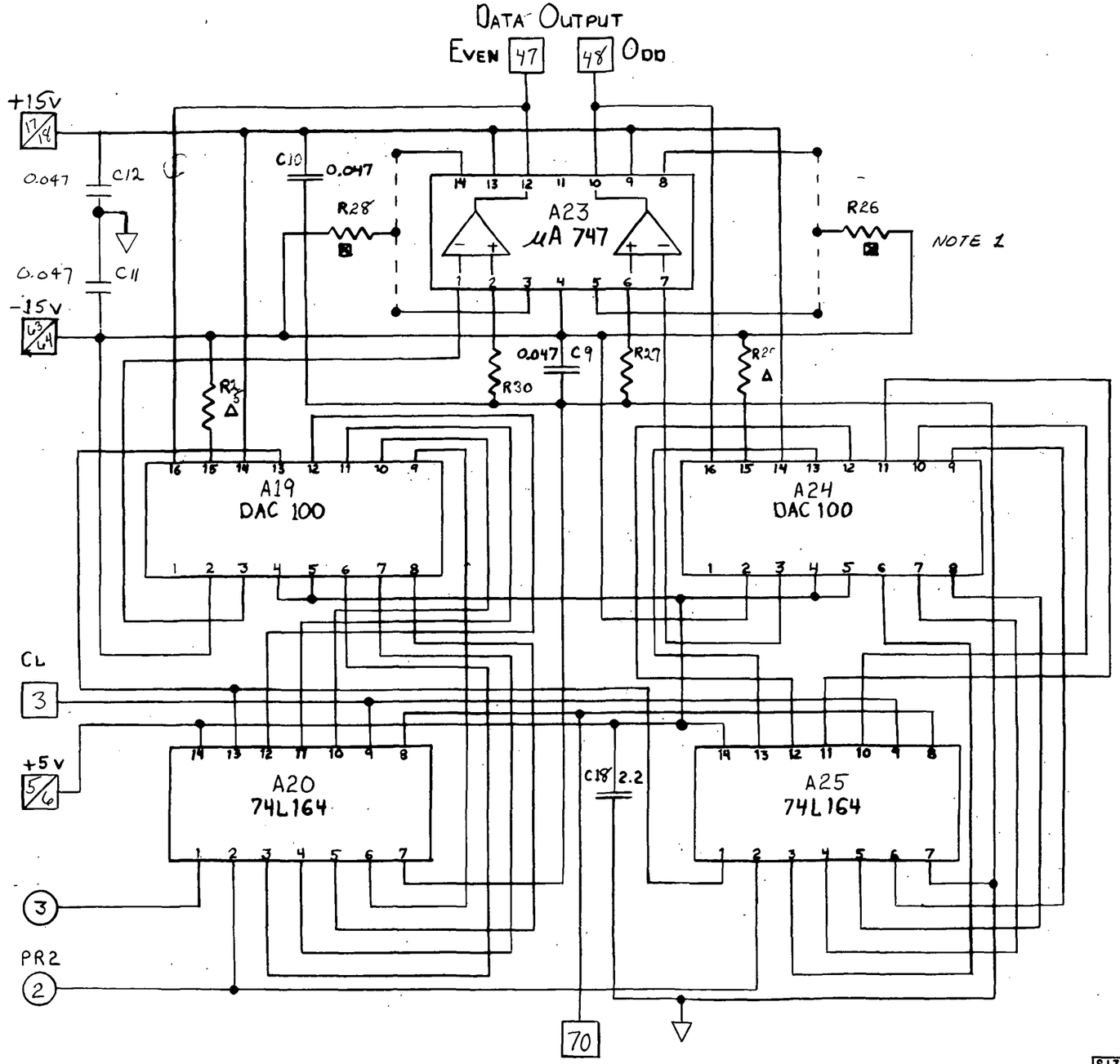
E-404D(2-62)



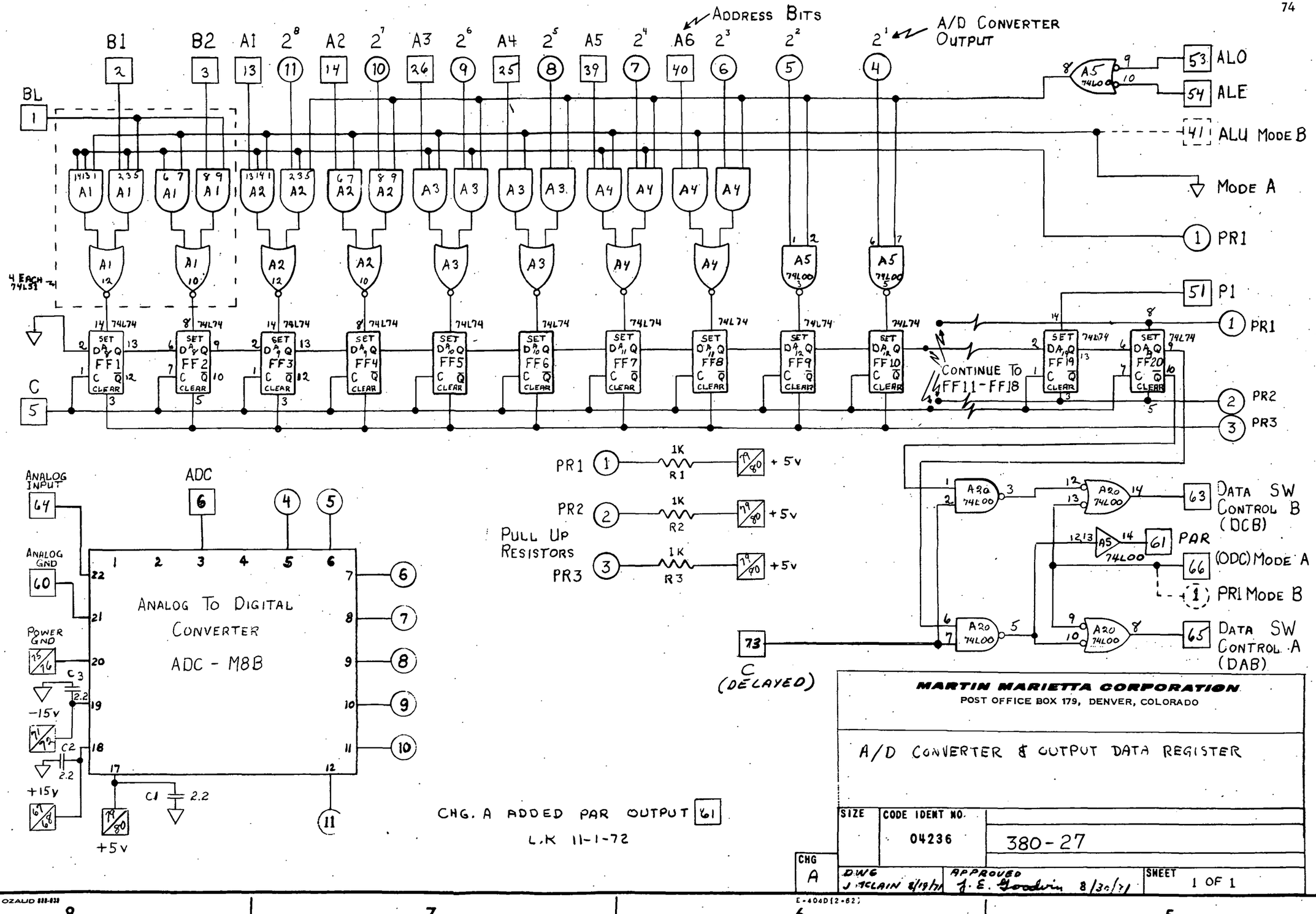
(DECODER)

ALL RESISTANCE VALUES IN OHMS.
ALL CAPACITOR VALUES IN μfd.

⊠ SELECT RESISTOR & CONNECTORS FOR ZERO VOLTAGE OUT WITH BINARY ZERO IN.

△ SELECT RESISTOR FOR 5 VOLTS OUT OF AMPLIFIER WITH BINARY 5 VOLTS IN. (0 to 200Ω)

SIZE	CODE IDENT NO.	
	04236	380-26
CHG	SCALE	SHEET 5 OF 5



CHG. A ADDED PAR OUTPUT 61

L.K 11-1-72

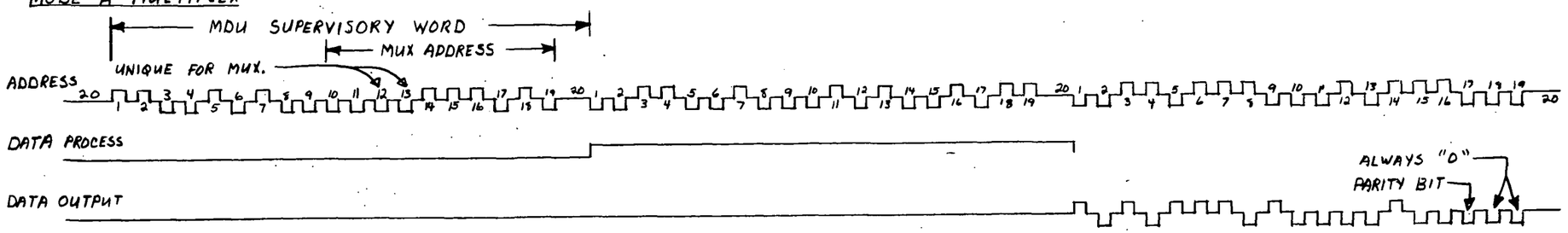
MARTIN MARIETTA CORPORATION
POST OFFICE BOX 179, DENVER, COLORADO

A/D CONVERTER & OUTPUT DATA REGISTER

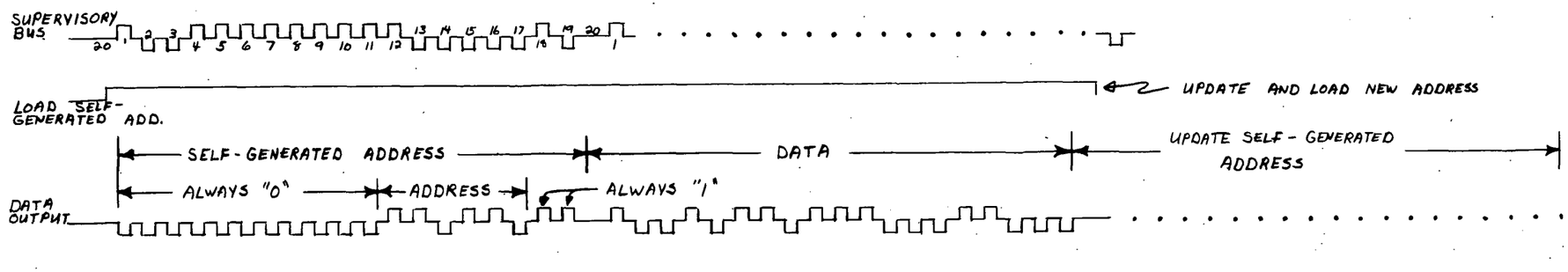
SIZE	CODE IDENT NO.	
	04236	380-27

CHG	DWG	APPROVED	SHEET
A	J. McClain 8/19/71	J. E. Goodwin 8/30/71	1 OF 1

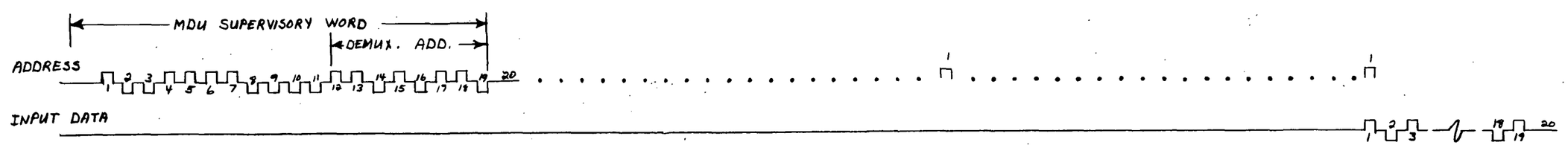
MODE A MULTIPLEX



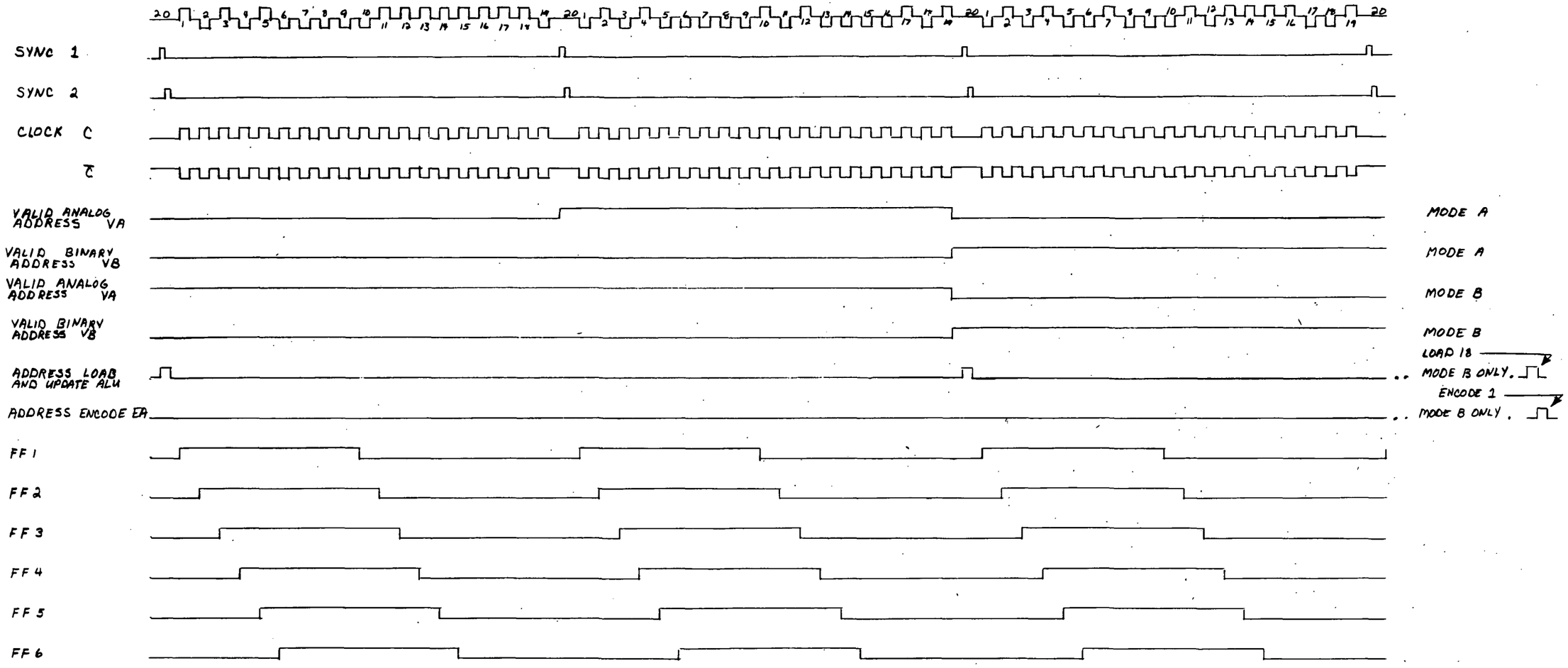
MODE B MULTIPLEX



DEMULTIPLEX ALL MODES



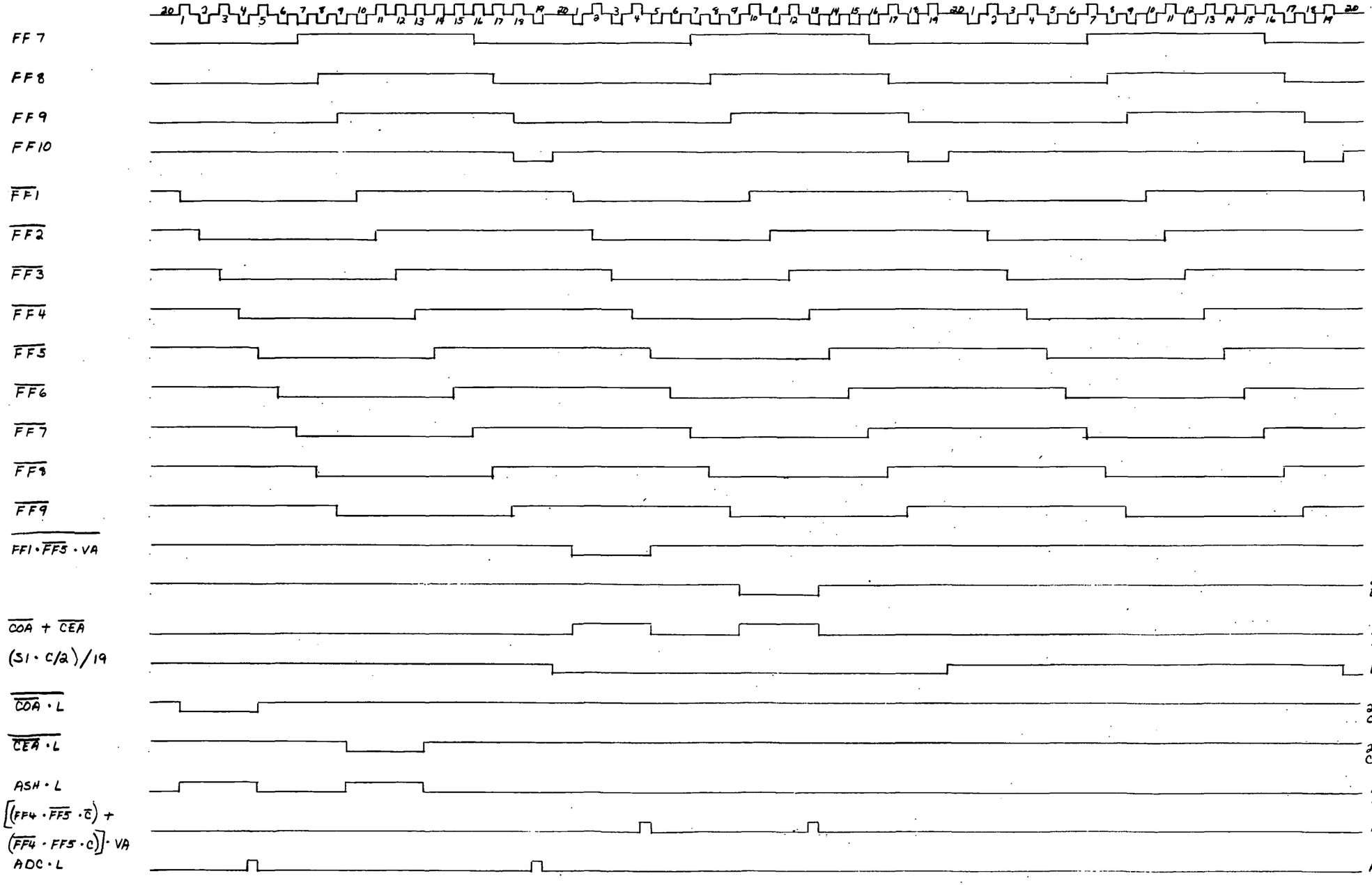
MARTIN MARIETTA CORPORATION POST OFFICE BOX 179, DENVER, COLORADO	
MULTIPLEXER / DEMULTIPLEXER MDU TIMING DIAGRAMS	
SIZE	CODE IDENT NO. 04236
	380-52
~~CONF~~ DWG E. S.	APPROVED: J. E. Goodwin 11-1-71
	SHEET 1 of 1



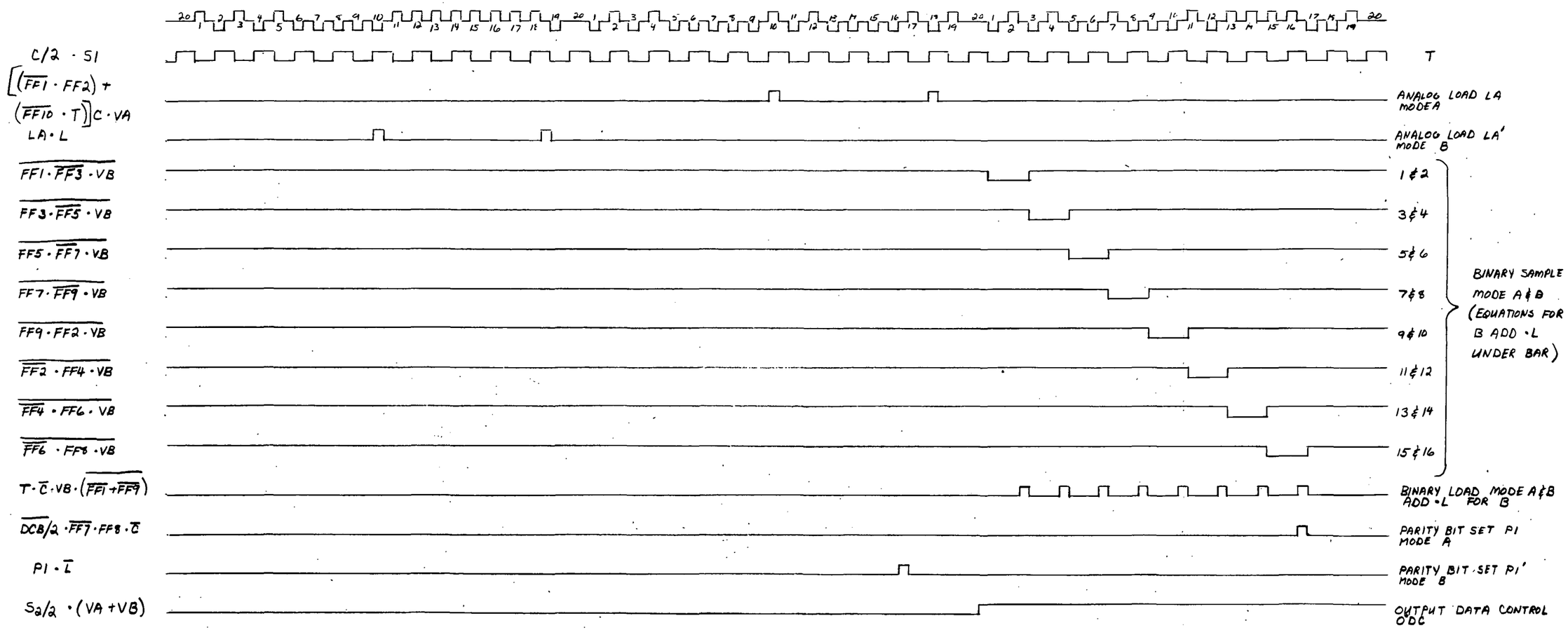
MARTIN MARIETTA CORPORATION
POST OFFICE BOX 179, DENVER, COLORADO

MULTIPLEXER / DEMULTIPLEXER CONTROL LOGIC TIMING DIAGRAMS

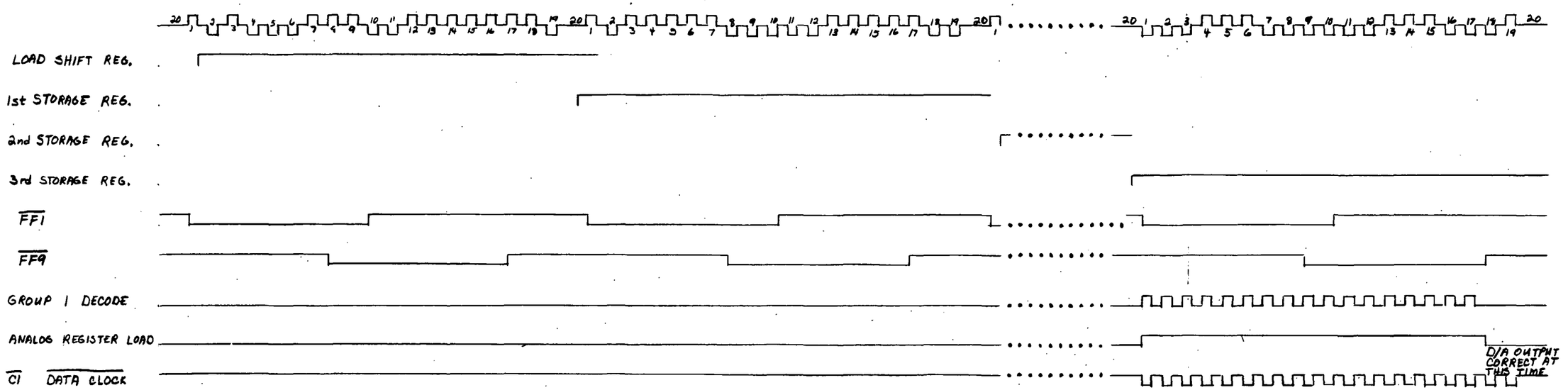
SIZE	CODE IDENT NO.	
	04236	380-53
SCALE		SHEET 1 of 3



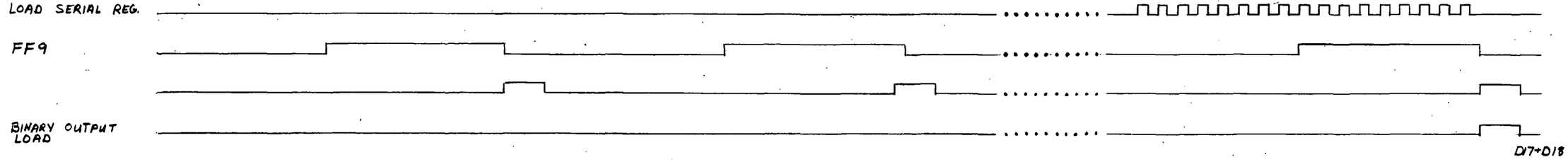
CHG	SIZE	CODE IDENT NO. 04236	380-53
	SCALE		SHEET 2 of 3



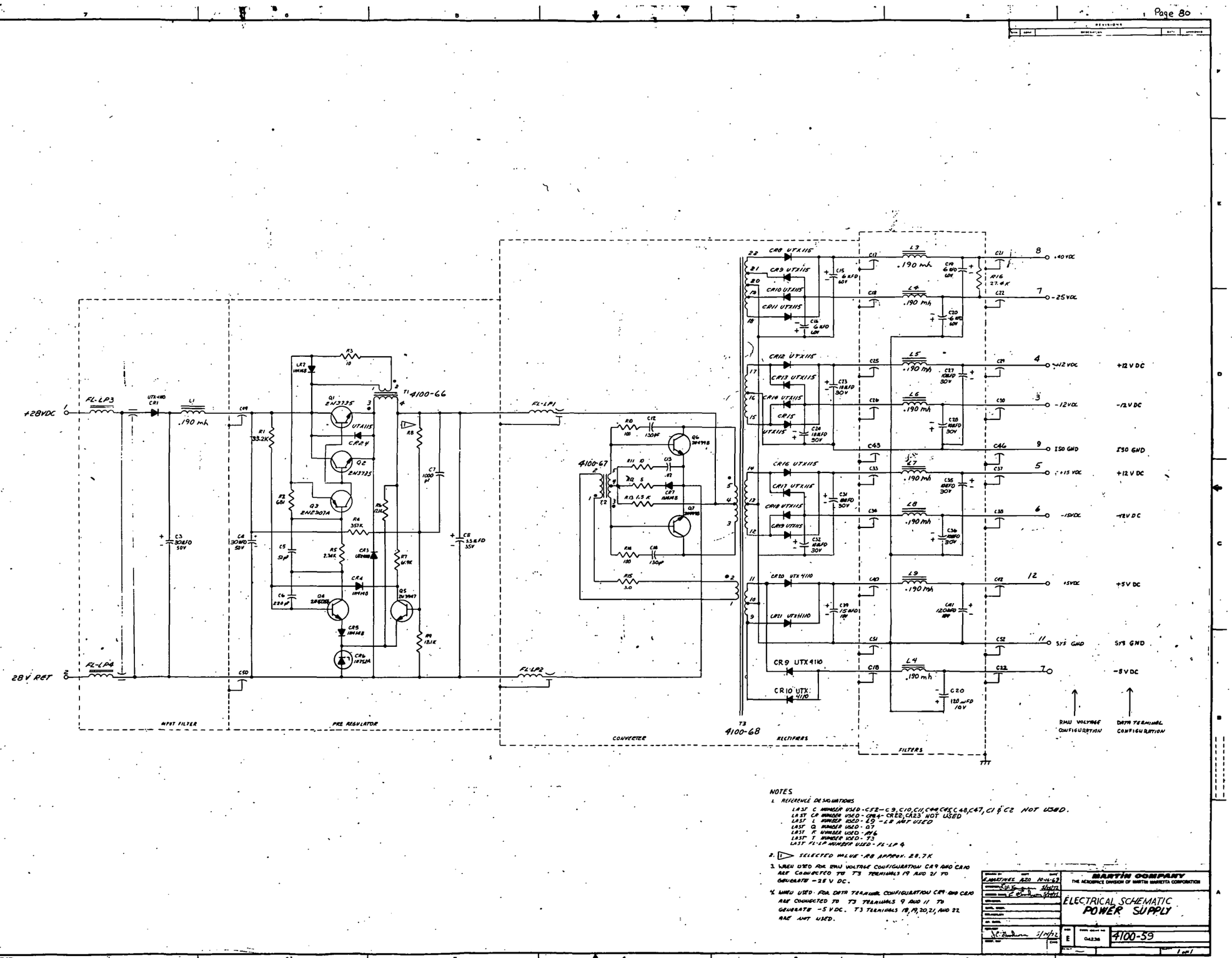
CHG	SIZE	CODE IDENT NO. 04236	380 - 53
	SCALE		SHEET 3 of 3



FOR DIGITAL - D ADDRESS LOADING IS AS FOLLOWS :



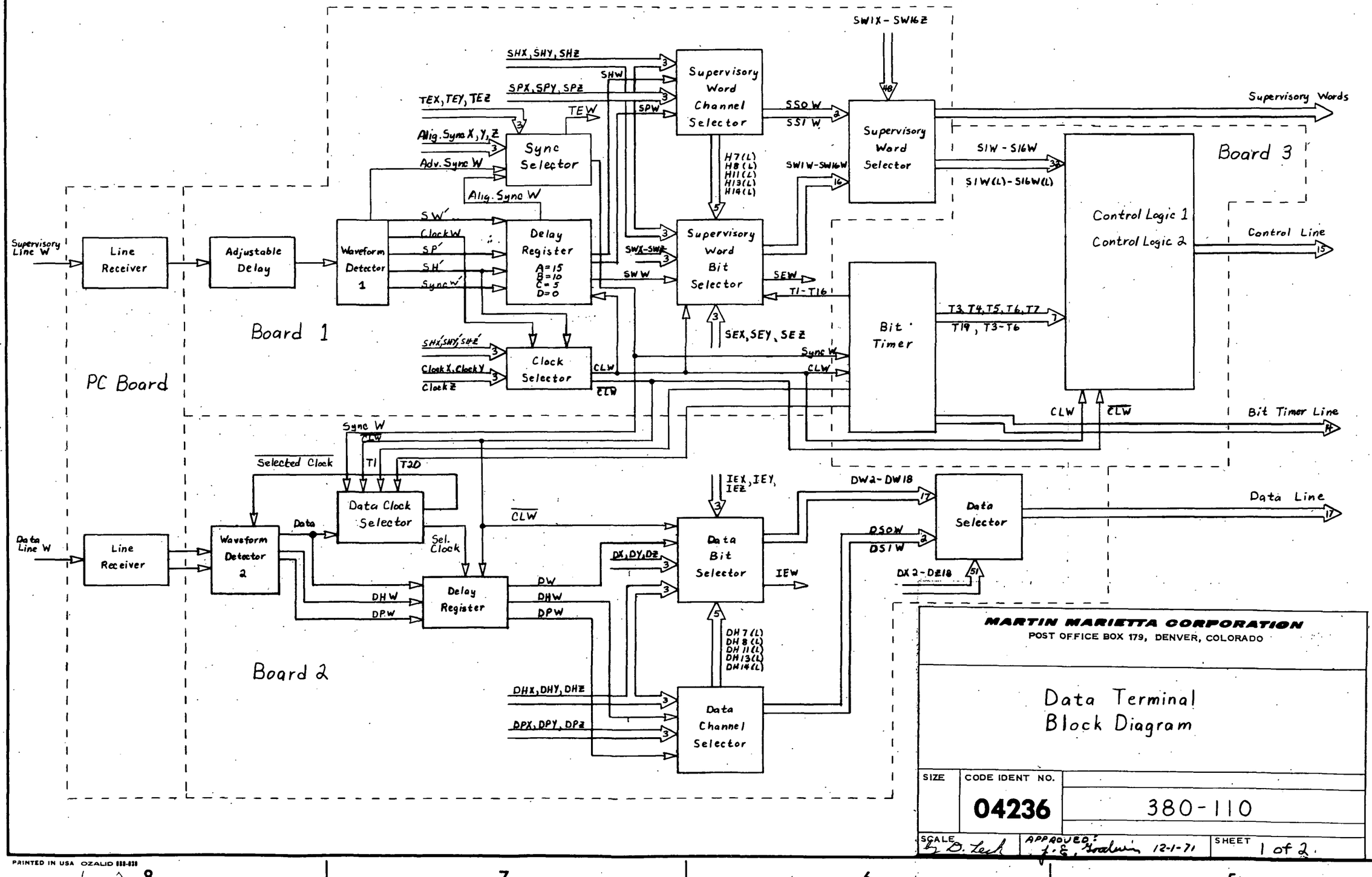
MARTIN MARIETTA CORPORATION POST OFFICE BOX 179, DENVER, COLORADO		
MULTIPLEXER / DEMULTIPLEXER DEMULTIPLEXER TIMING DIAGRAMS		
SIZE	CODE IDENT NO. 04236	380-54
~~SCALE~~ DWG E.S.	APPROVED. J.E. Woodrum 11-1-71	SHEET 1 of 1



NOTES

1. REFERENCE DESIGNATIONS
   - LAST C NUMBER USED - C52 - C9, C10, C11, C46, C45, C48, C47, C1 & C2 NOT USED.
   - LAST CR NUMBER USED - CR24 - CR22, CR23 NOT USED
   - LAST L NUMBER USED - L9 - L2 NOT USED
   - LAST Q NUMBER USED - Q7
   - LAST R NUMBER USED - R16
   - LAST T NUMBER USED - T3
   - LAST FL-LP NUMBER USED - FL-LP 4
2. ▷ SELECTED VALUE - R8 APPROX. 28.7K
3. WHEN USED FOR RMU VOLTAGE CONFIGURATION CR9 AND CR10 ARE CONNECTED TO T3 TERMINALS 19 AND 21 TO GENERATE -28 V DC.
4. WHEN USED FOR DATA TERMINAL CONFIGURATION CR9 AND CR10 ARE CONNECTED TO T3 TERMINALS 9 AND 11 TO GENERATE -5 V DC. T3 TERMINALS 18, 19, 20, 21, AND 22 ARE NOT USED.

DRAWING NO.	4100-59	MARTIN COMPANY	
SIZE	E	THE AEROSPACE DIVISION OF MARTIN MARIETTA CORPORATION	
CAGE CODE	04236	ELECTRICAL SCHEMATIC POWER SUPPLY	
SHEET	1 of 1		

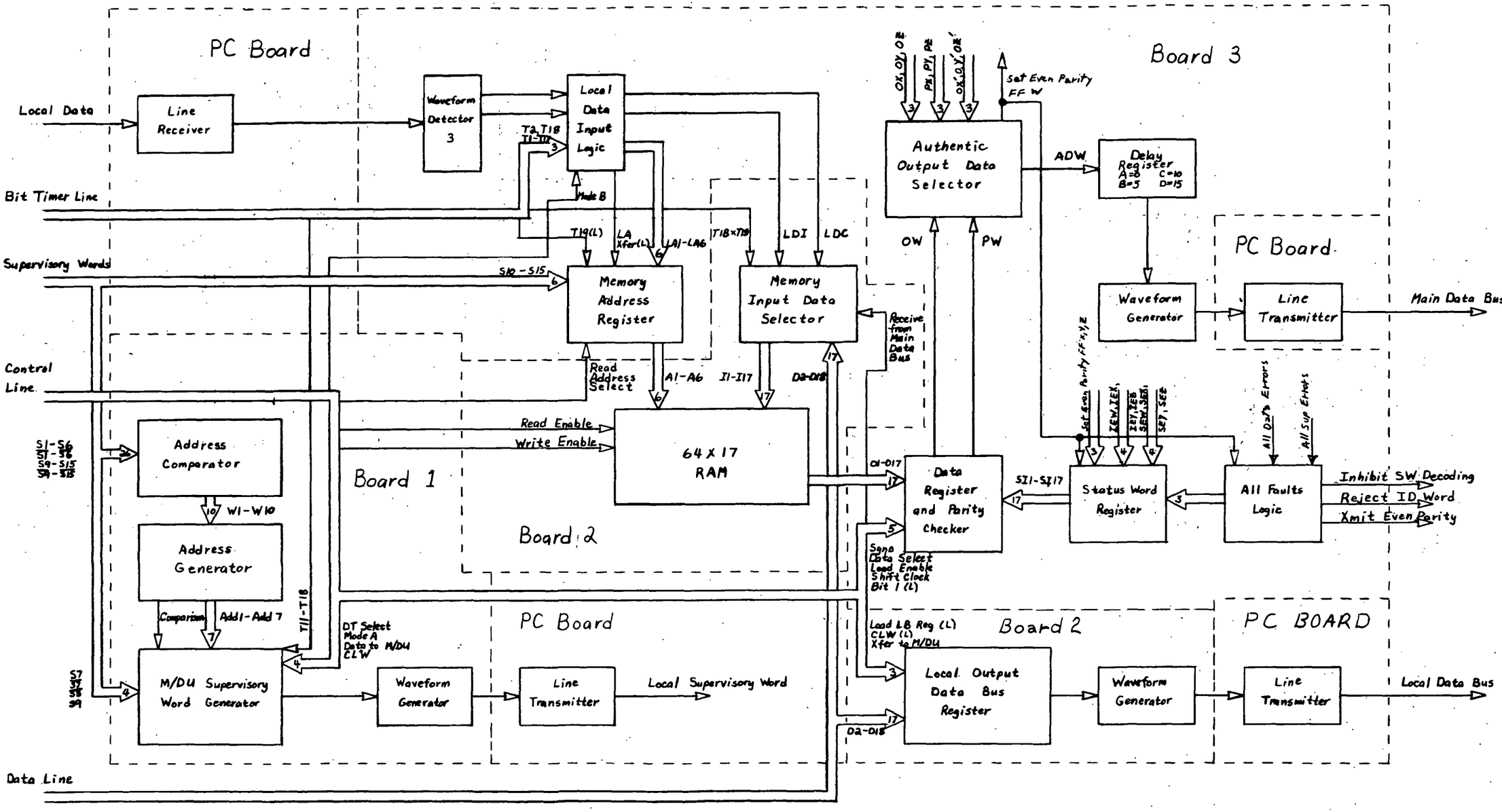


MARTIN MARIETTA CORPORATION
POST OFFICE BOX 179, DENVER, COLORADO

Data Terminal Block Diagram

SIZE	CODE IDENT NO.	
	04236	380-110

SCALE: None | APPROVED: J. E. Gralwin 12-1-71 | SHEET 1 of 2



SIZE	CODE IDENT NO.	380-110
CHG	04236	
	SCALE	SHEET 2 of 2

E-404D(2-62)

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8 7 6 5

NOTES:

1. The following symbols are used on this schematic:
   - □ Connection to board connector (board has two 70 pin connectors - J and H)
   - ◯ Signal continued to other sheets of schematic as indicated
   - Y Test point connection
2. The letters A, B, C, and D denote the four redundant channels
3. The letters W, X, Y and Z are general designations for which A, B, C, and D may be substituted when considering a specific channel.
4. The alpha numeric designation in each logic symbol indicates the package location on the board.
5. Pin numbers on this schematic are package pin numbers. The board contains only 16 pin sockets; consequently, for packages with less than 16 pins, some pin numbers will change on the board back plane wiring list.

TEST POINT ASSIGNMENTS

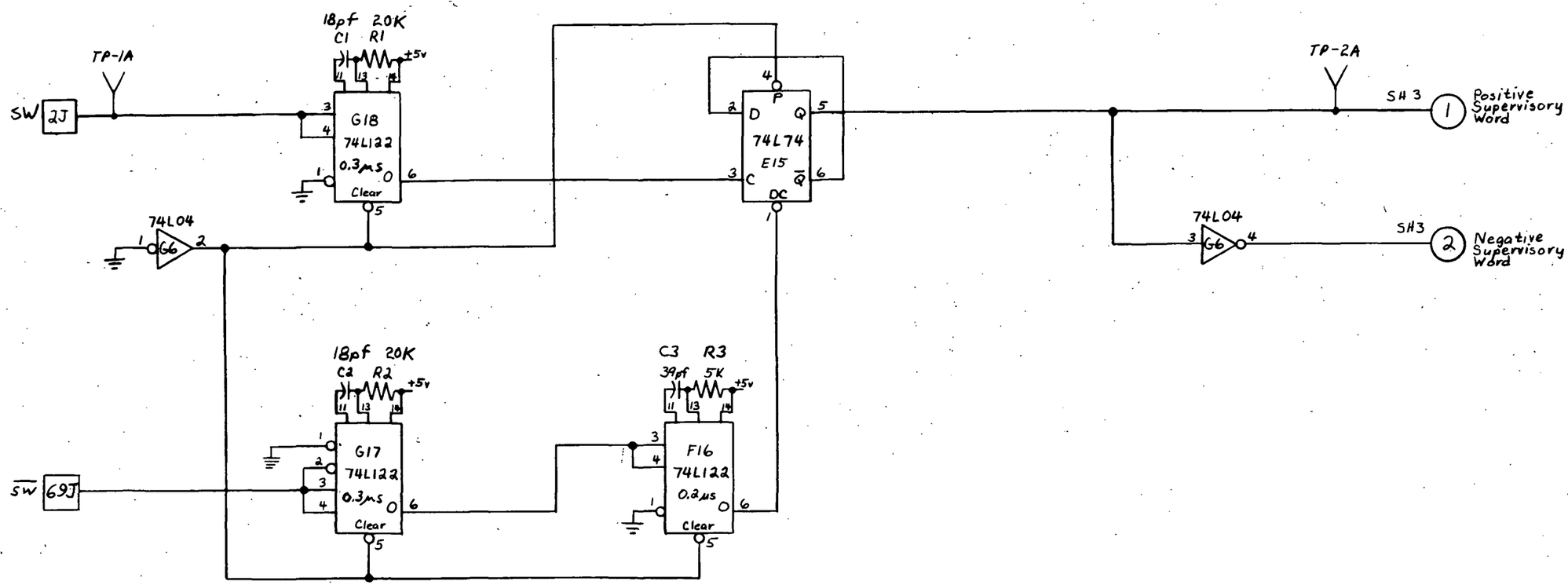
T.P No	SIGNAL NAME	Sheet No.
1A	SW	2
2A	Positive Supervisory Word	2
3A	SPW'	3
4A	SYNC W'(L)	3
5A	SHW'	3
6A	CLOCK W	3
7A	F	3
8A	CLW	4
9A	M/DU Supervisory Word(L)	
10A	SWW	4
1B	Aligned Sync	4
2B	SHW	4
3B	SPW(L)	4
4B	TEA	5
5B	SW SYNC(L)	5
6B	SUP. Word Reg. Input	7
7B	SEW	7
8B	All Sup. Errors	7
9B	Translate (L)	11
10B	DT Select (L)	12

DRAWN BY	DEPT	DATE
Ed Schlotfeldt	1622	19 Nov 71
CHECKER		
STRESS ENGR		
WT ENGR		
MATL ENGR		
RELIABILITY		
GR ENGR D. Leach 11-19-71		
PROJECT J. E. Goodwin 12-1-71		
CUST RPRSNTV		

MARTIN MARIETTA CORPORATION
POST OFFICE BOX 179, DENVER, COLORADO

SUPERVISORY WORD LOGIC

SIZE	CODE IDENT NO.	
	04236	380-111
SCALE		SHEET 1 of 12



Adjustable Delay

SIZE	CODE IDENT NO.	
	04236	380 - 111
CHG A	SCALE	SHEET 2 of 12

CHG. D. ADDED PARITY CLOCK OUTPUT FROM E10. J.E.Y. 9/12/72

T6 - T1 (A)
T11 - T6 (B)
T16 - T11 (C)
T1 - T16 (D)

3J

1 SH2 Positive Supervisory Word

2 SH2 Negative Supervisory Word

68 J

110 SH4 T2+T4 (A) T7+T9 (B) T12+T14 (C) T17+T19 (D)

102 SH5 SW SYNC

74L00 D18 · 74L04 D17 · 74L00 D18 · 74L00 D18 · 74L04 D17 · 74L00 C18 · 74L00 C18 · 74L04 D17 · 74L00 C18

X

74L04 D17 · C4 180pf · R4 30K · +5V

F15 74L122 2.75μs Clear

74L04 G6

74L10 E14 · ȳ

74L00 E11 · 74L04 E10

F12 74L122 0.5μs Clear · C6 39pf · 20K R6 · +5V

74L10 E14 · 74L04 E17

74L74 E9 · TP-3A · TP-4A · TP-5A

C15 39pf · R22 10K · +5V

C1 74L122 0.27μs CLEAR

SH4 7 SYNC W'

SH4 3 Supervisory Data W'

SH4 4 SPW'

5J SYNC W(L)

SH4 5

SH4 6 SHW'

7J

74L74 E9

74L10 E14

74L00 E11 · 6J ADV SYNC

74L04 D12

C10 180pf · R10 20K · +5V · G14 74L122 1.4μs Clear

C11 180pf · R11 5K · +5V · G13 74L122 0.6μs

C12 39pf · 5K R12 · +5V · G12 74L122 0.2μs

SH4 9 CLOCK W

15J Clock W

SH4 8 SW CL

4J H(L)

74L04 E10

74L04 D17 · C13 39pf · R13 17.8K · +5V · G15 74L122 0.43μs Clear

C7 39pf · R7 28.K · +5V · G16 74L122 0.61μs Clear

74L04 E17

74L00 C10

+5V · R9 3K · 18pf C9 · D16 74L122 0.14μs Clear

+5V · R8 6.8K · 18pf C8 · D15 74L122 0.30μs Clear

C14 18.pf · R21 7.5K · +5V · D3 74L122 0.2μs CLEAR

TP-7A

Waveform Detector 1

SIZE	CODE IDENT NO.	
	04236	380-111
CHG D	SCALE	SHEET 3 of 12

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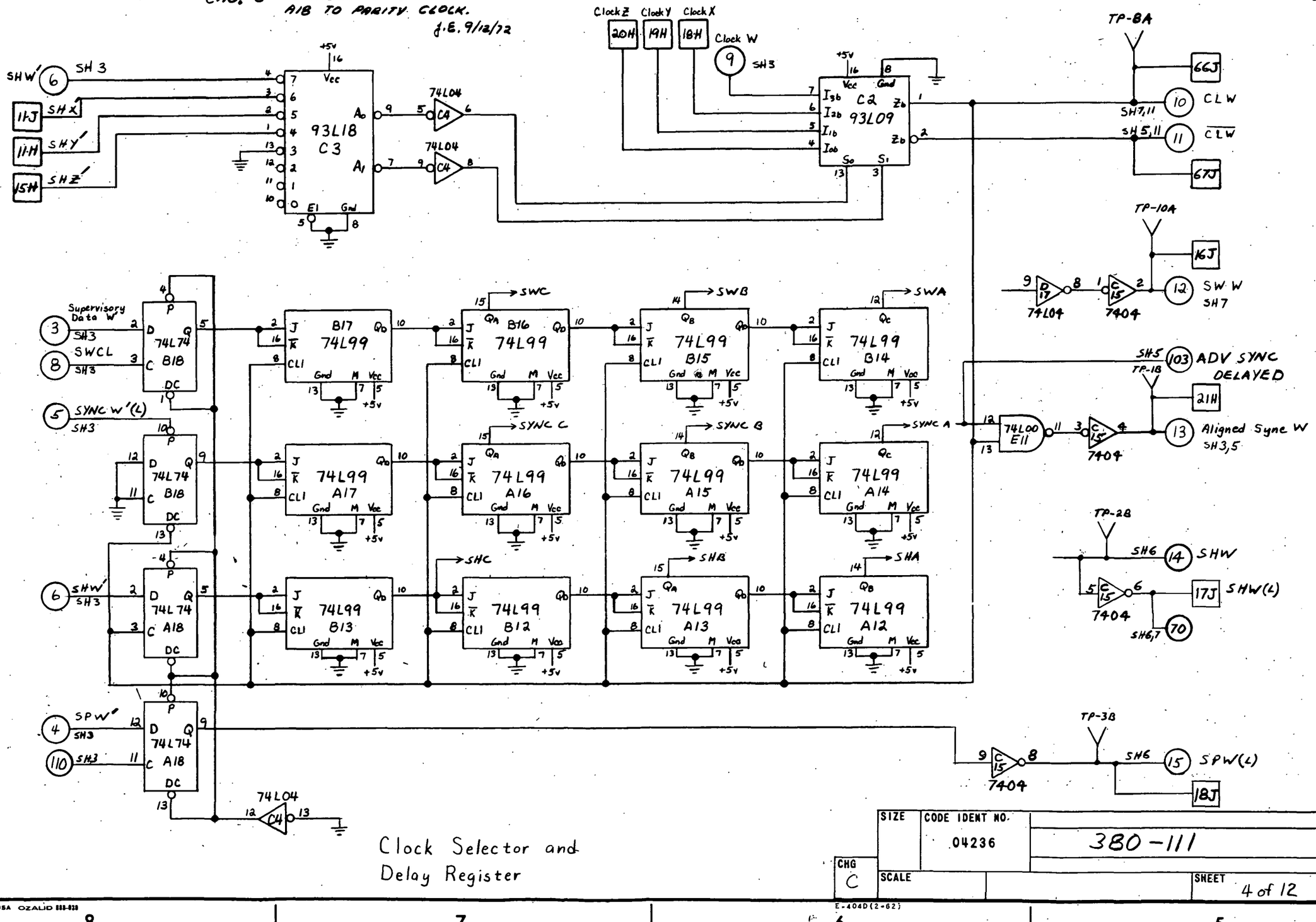
E-404D (2-62)

CHG. C CHANGED CLOCK ON A1B TO PARITY CLOCK.
J.E. 9/12/72



Clock Selector and Delay Register

CHG	SIZE	CODE IDENT NO.	
C		04236	380-111
	SCALE		SHEET 4 of 12

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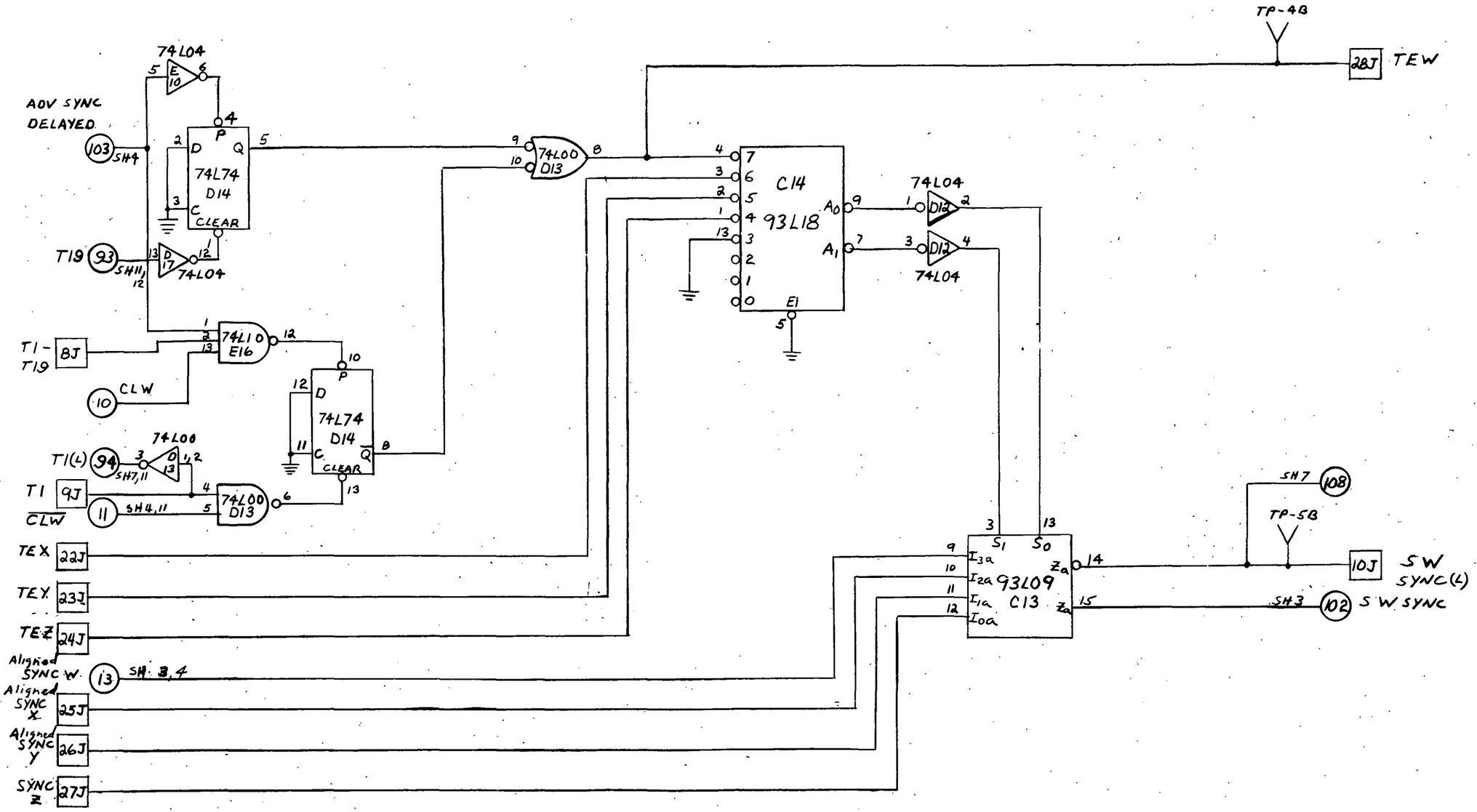
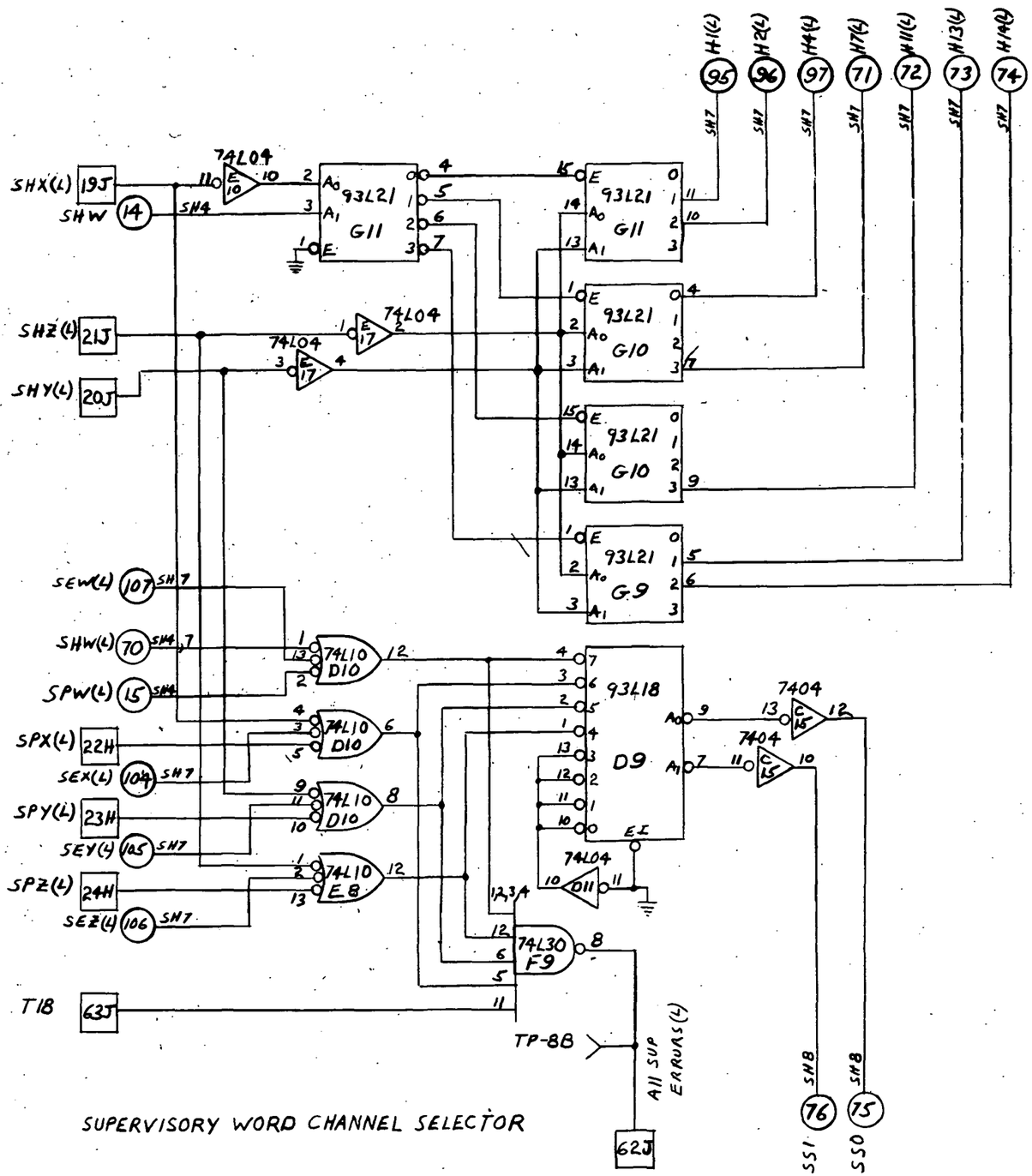
E-404D(2-62)

8 7 6 5



Sync Selector

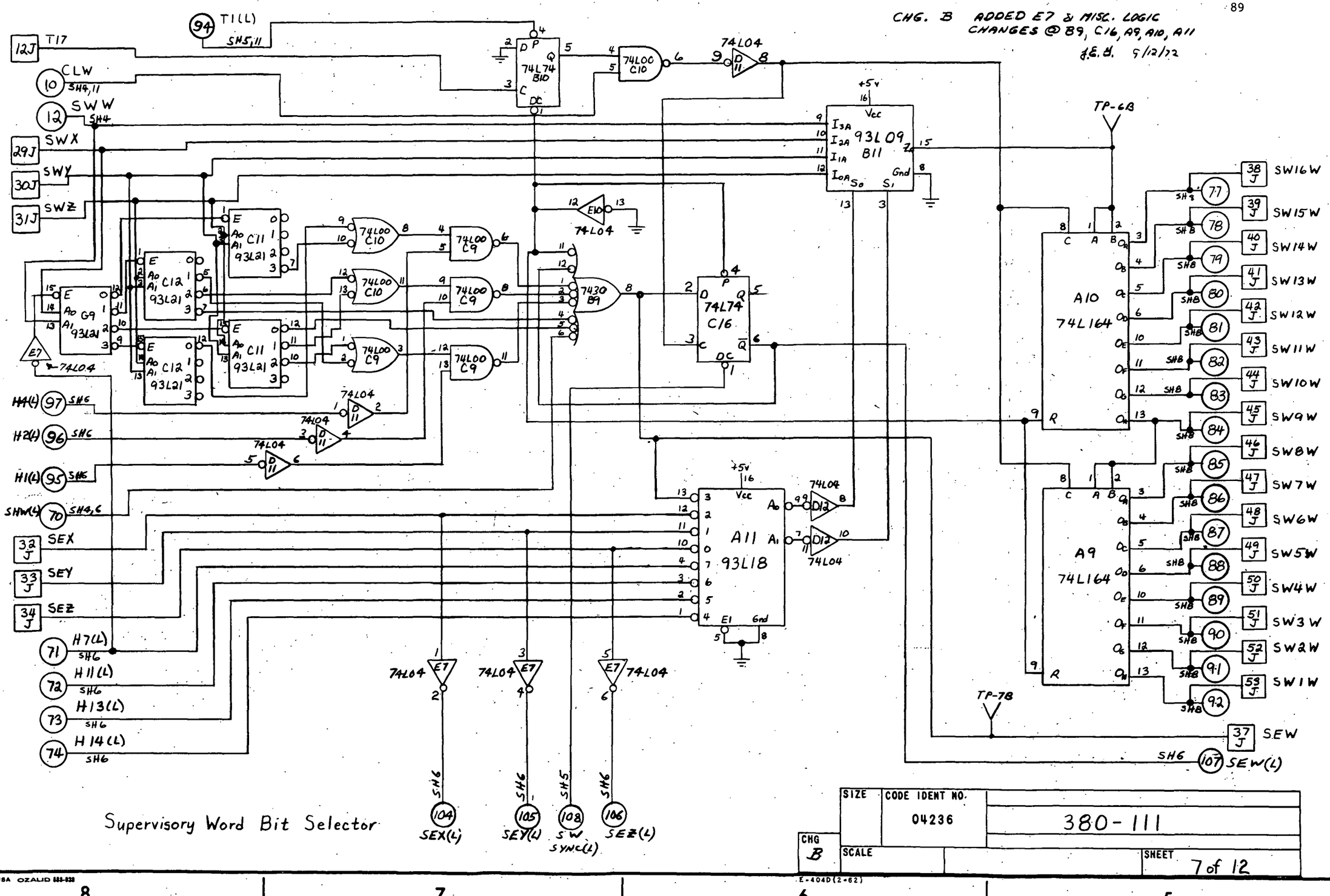
CHG	SIZE	CODE IDENT NO.	
B		04236	380-111
	SCALE		SHEET 5 of 12



SUPERVISORY WORD CHANNEL SELECTOR

SIZE	CODE IDENT NO.	
	04236	380-111
CHG B	SCALE	SHEET 6 of 12

CHG. B ADDED E7 & MISC. LOGIC
CHANGES @ B9, C16, A9, A10, A11
J.E.B. 5/12/72



Supervisory Word Bit Selector

SIZE	CODE IDENT NO.	
	04236	380-111
CHG B	SCALE	SHEET 7 of 12

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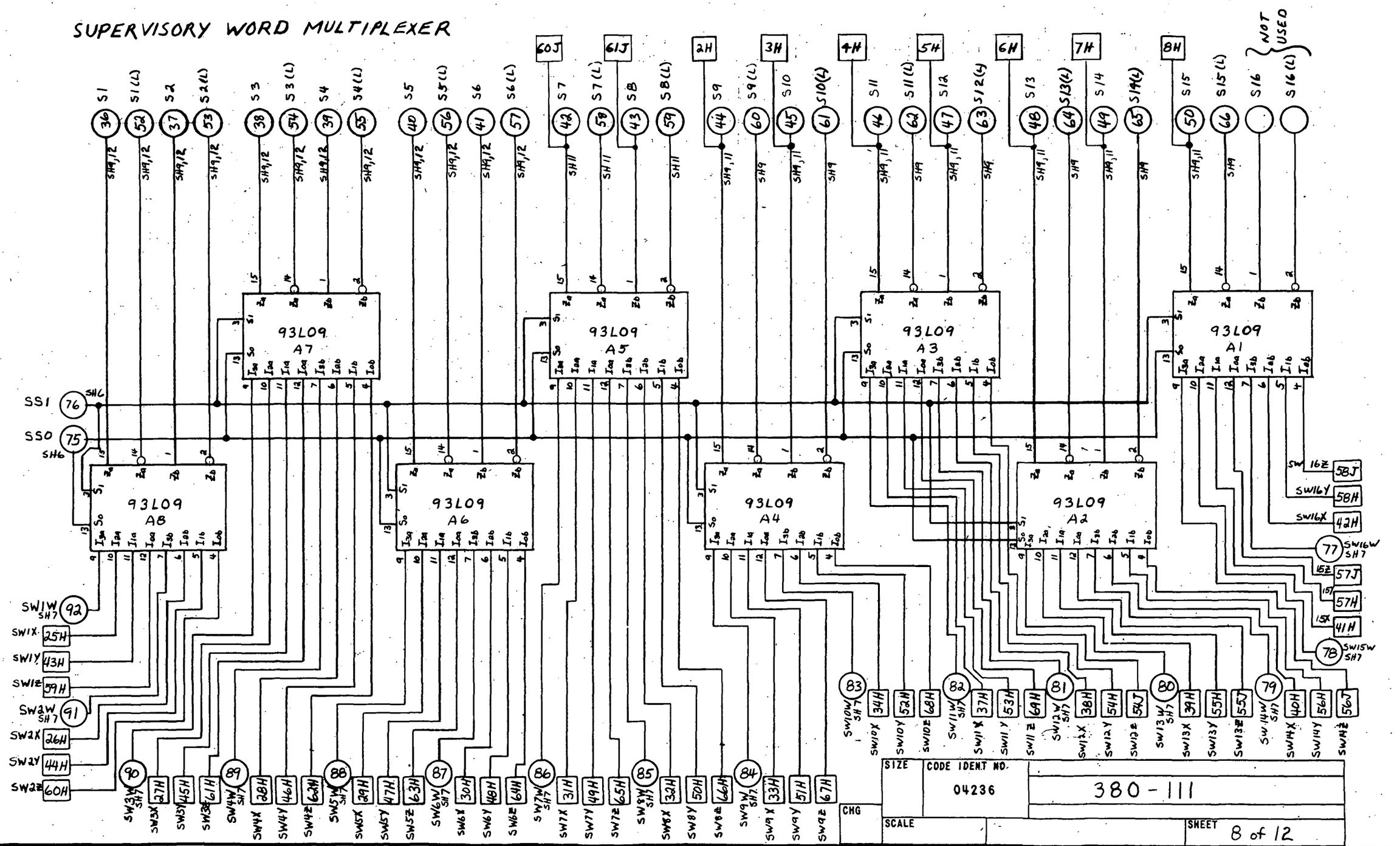
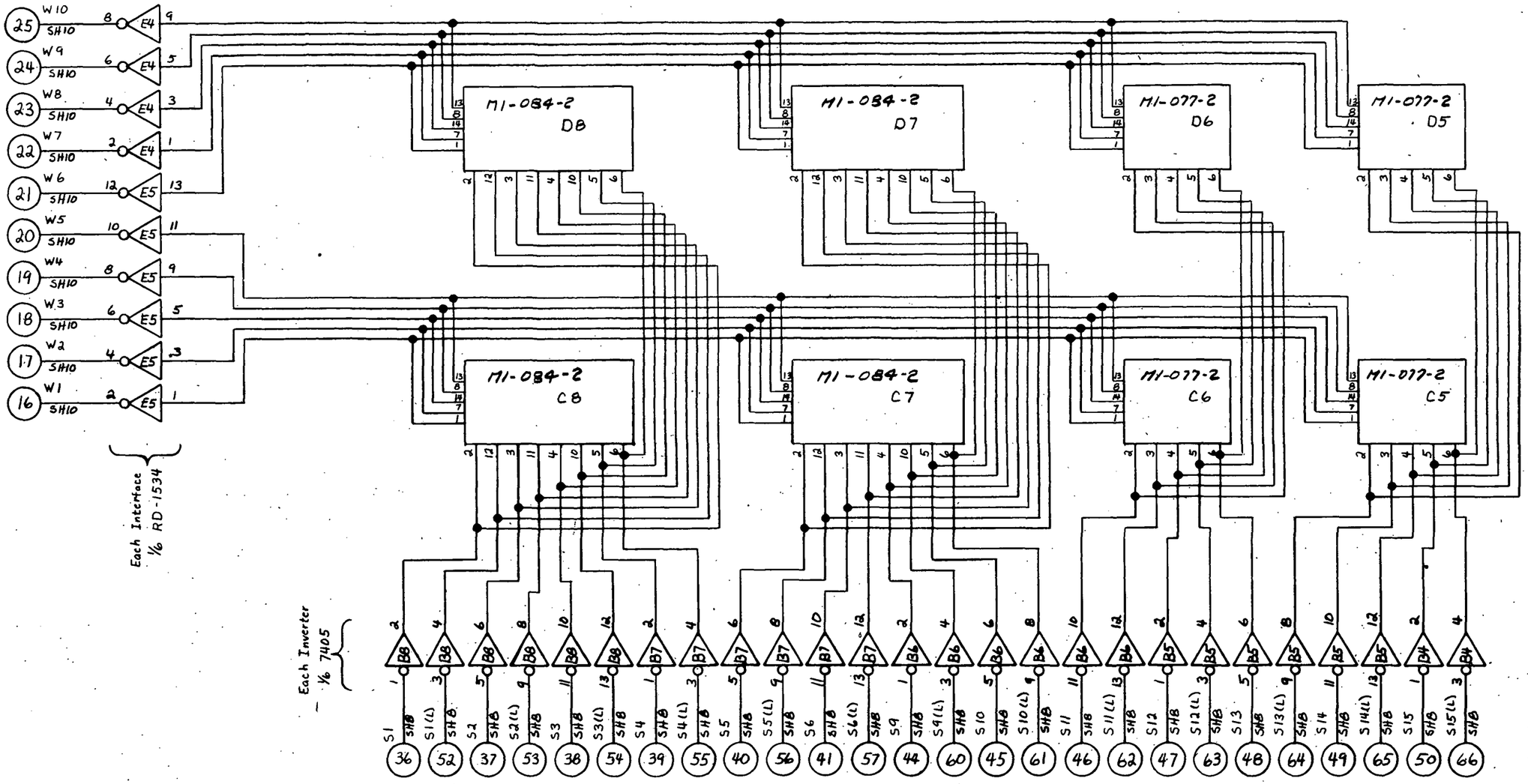
E-404D(2-62)

8 7 6 5

SUPERVISORY WORD MULTIPLEXER



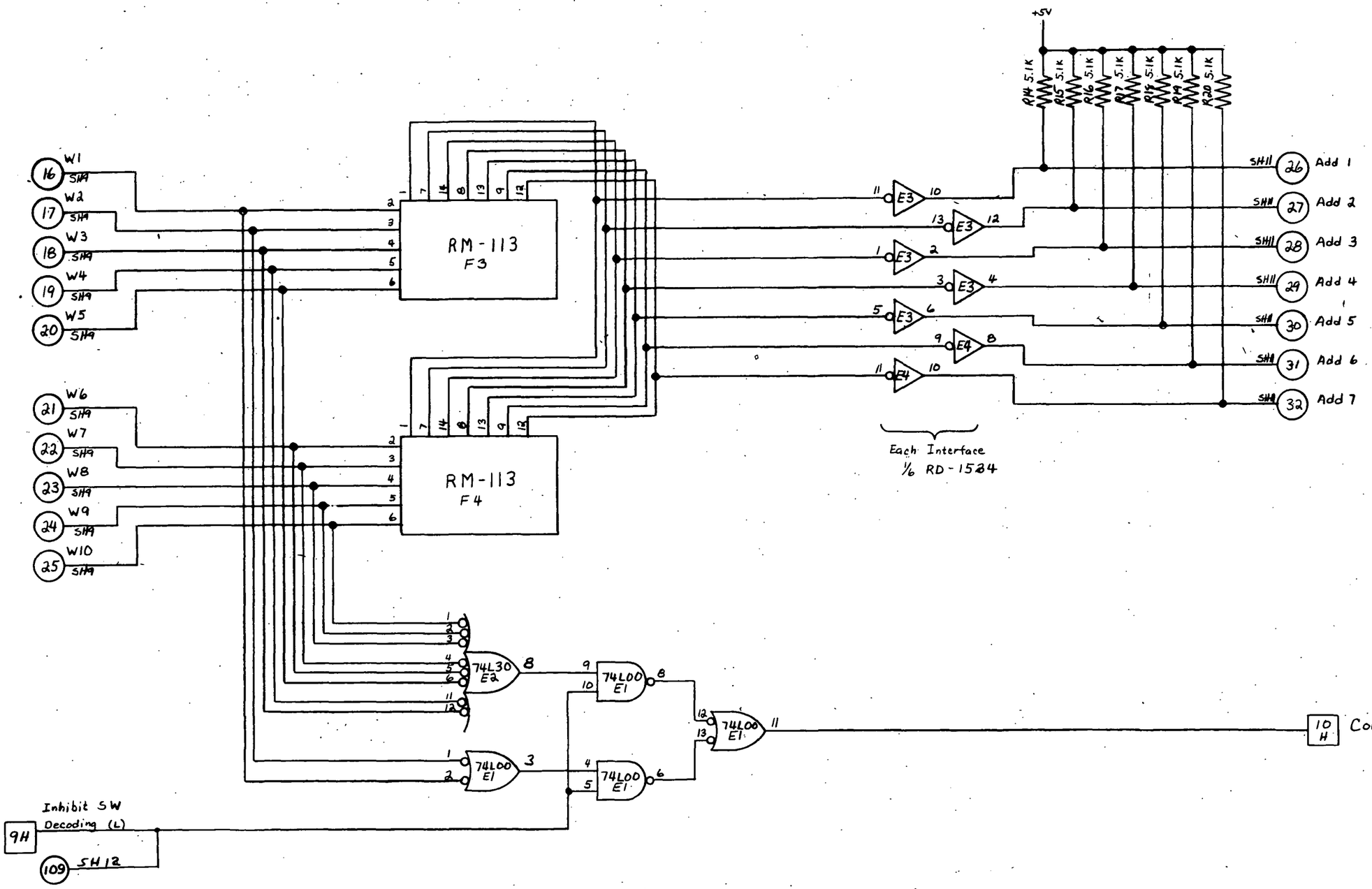
SIZE	CODE IDENT NO.	380-111
CHG	SCALE	SHEET 8 of 12



Address Comparator

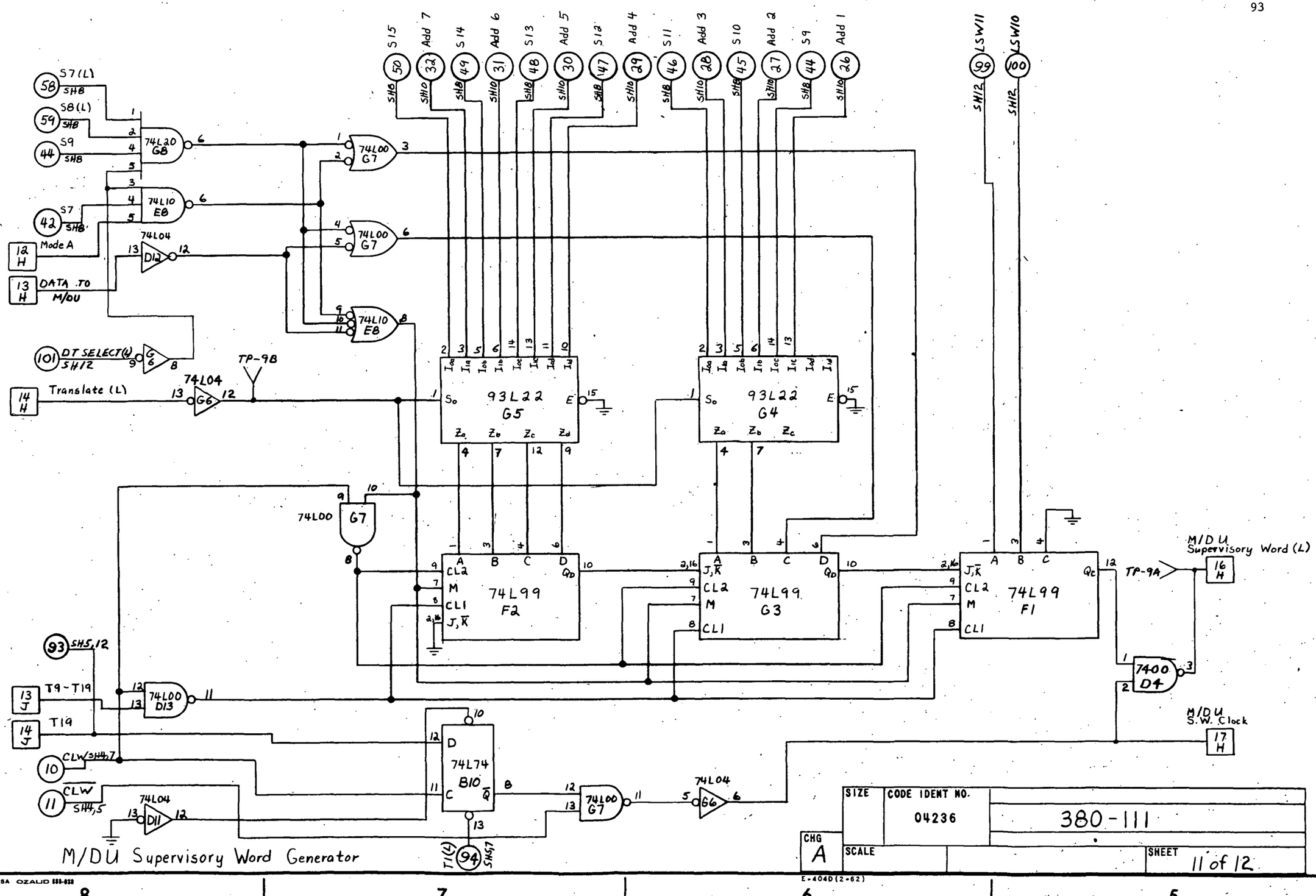
CHG. A UPDATED MATRIX PART NO.S J.E.B. 9/12/72

SIZE	CODE IDENT NO.	
	04236	380-111
CHG A	SCALE	SHEET 9 of 12



Address Generator

CHG	SIZE	CODE IDENT NO. 04236	380-111
	SCALE		SHEET 10 of 12



CHG A	SIZE	CODE IDENT NO. 04236	380-111
	SCALE		SHEET 11 of 12

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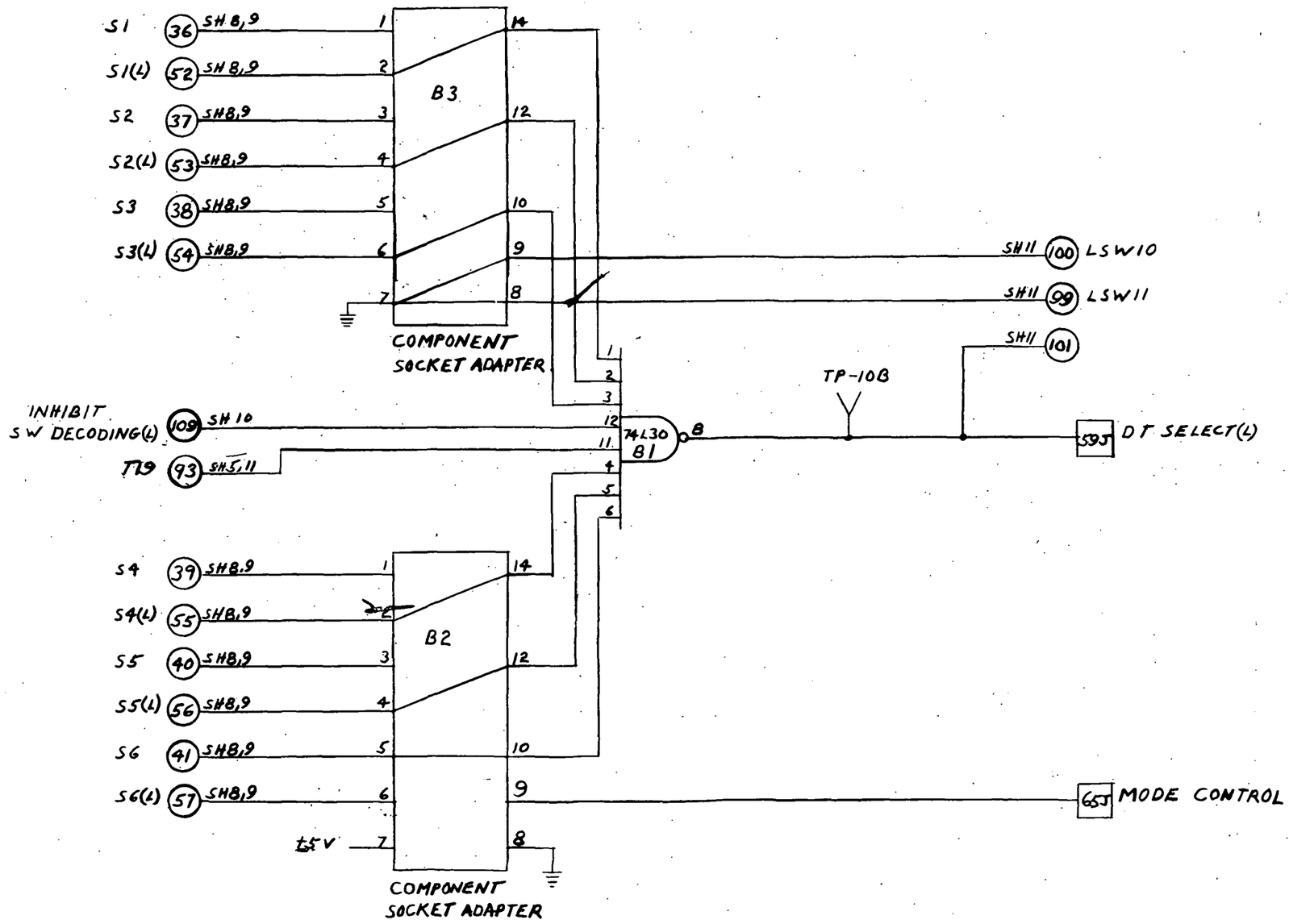
E-404D (2-62)



PROGRAMING BOARDS

SIZE	CODE IDENT NO.	
	04236	380-111
CHG	SCALE	SHEET 12 of 12

E-404D(2-62)

NOTES:

1. The following symbols are used on this schematic
   - □ Connection to board connector (board has two 70 pin connectors - J and H)
   - ○ Signal continued to other sheets of schematic as indicated
   - Y Test point connection
2. The letters A, B, C, and D denote the four redundant channels.
3. The letters W, X, Y, and Z are general designations for which A, B, C, and D may be substituted when considering a specific channel.
4. The numbers in parentheses in each logic symbol designate the location of pin 1 of the package on the board according to an x,y grid arrangement.
5. This board is a universal board which can accept different size sockets; 14, 16, and 24 pin packages with equivalent sockets are used on this board.

TEST POINT ASSIGNMENTS

T.P. No.	SIGNAL NAME	Sheet No.
1 A	MBD	2
2 A	DH	2
3 A	DP	2
4 A	Selected Clock	3
5 A	DW	4
6 A	DHW	4
7 A	DPW(L)	4
8 A	Data Word Reg. Input	6
9 A	IEW	6
10 A	All Data Errors	6
1 B	DSO	5
2 B	DS1	5
3 B	Local Output Register Clock	9
4 B	LOB DATA	9
5 B	LDIP	10
6 B	Read Enable	11
7 B	DR1	2
8 B	DR2	2
9 B		
10 B		

DRAWN BY Ed Schlafman	DEPT 1622	DATE 19 Nov 71
CHECKER		
STRESS ENGR		
WT ENGR		
MATL. ENGR		
RELIABILITY		
GR ENGR D. Leach		11/19/71
PROJECT J. E. Goodwin		12/1/71
CUST RPRSNTV		

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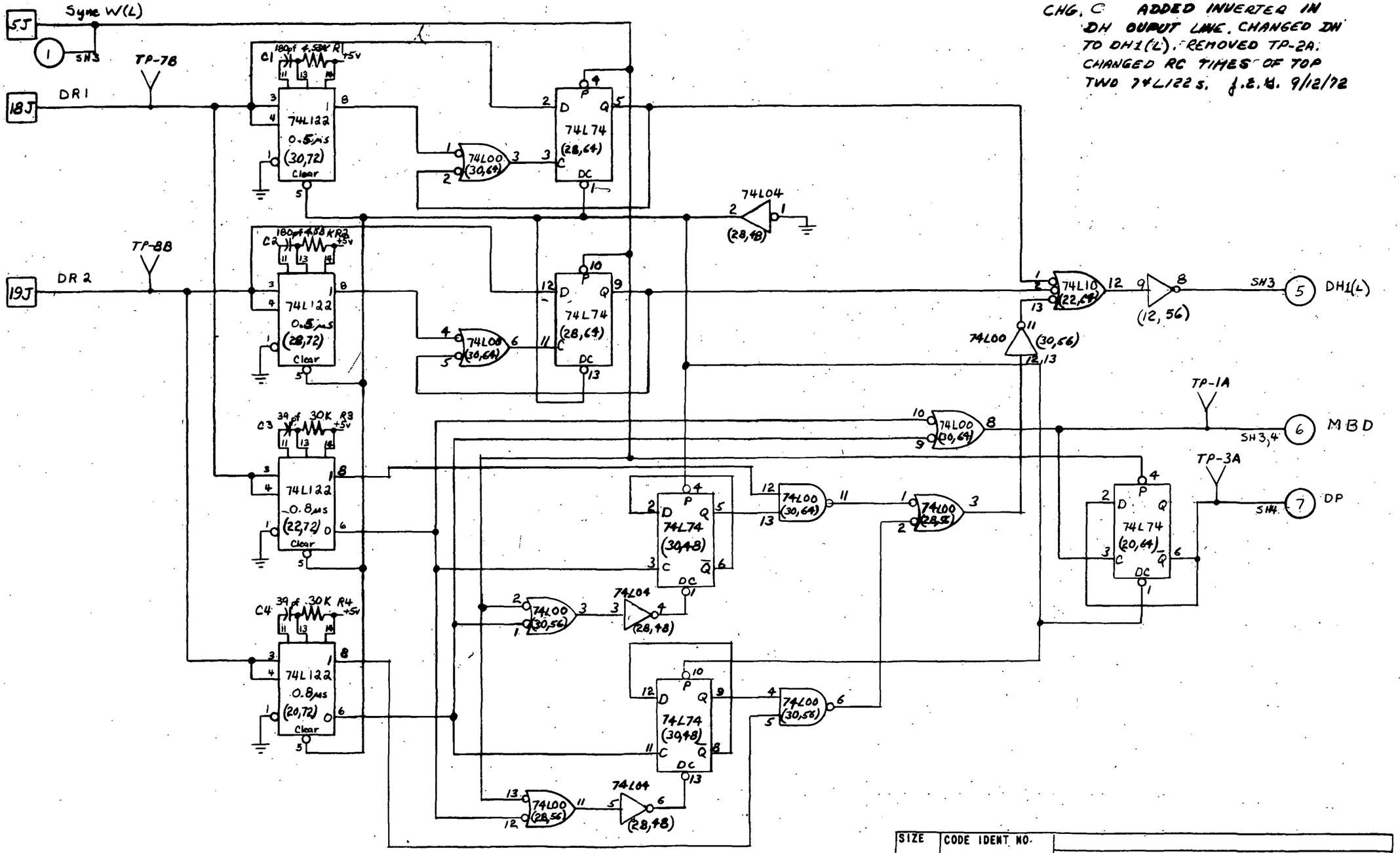
INPUT DATA WORD AND MEMORY LOGIC

SIZE	CODE IDENT NO.	
	04236	380-112
SCALE		SHEET 1 of 11

CHG. C ADDED INVERTER IN DH OUPUT LINE. CHANGED DH TO DH1(L). REMOVED TP-2A. CHANGED RC TIMES OF TOP TWO 74L122s. J.E.M. 9/12/72



Waveform Detector 2

CHG	SIZE	CODE IDENT NO.	
C		04236	380-112
	SCALE		SHEET 2 of 11

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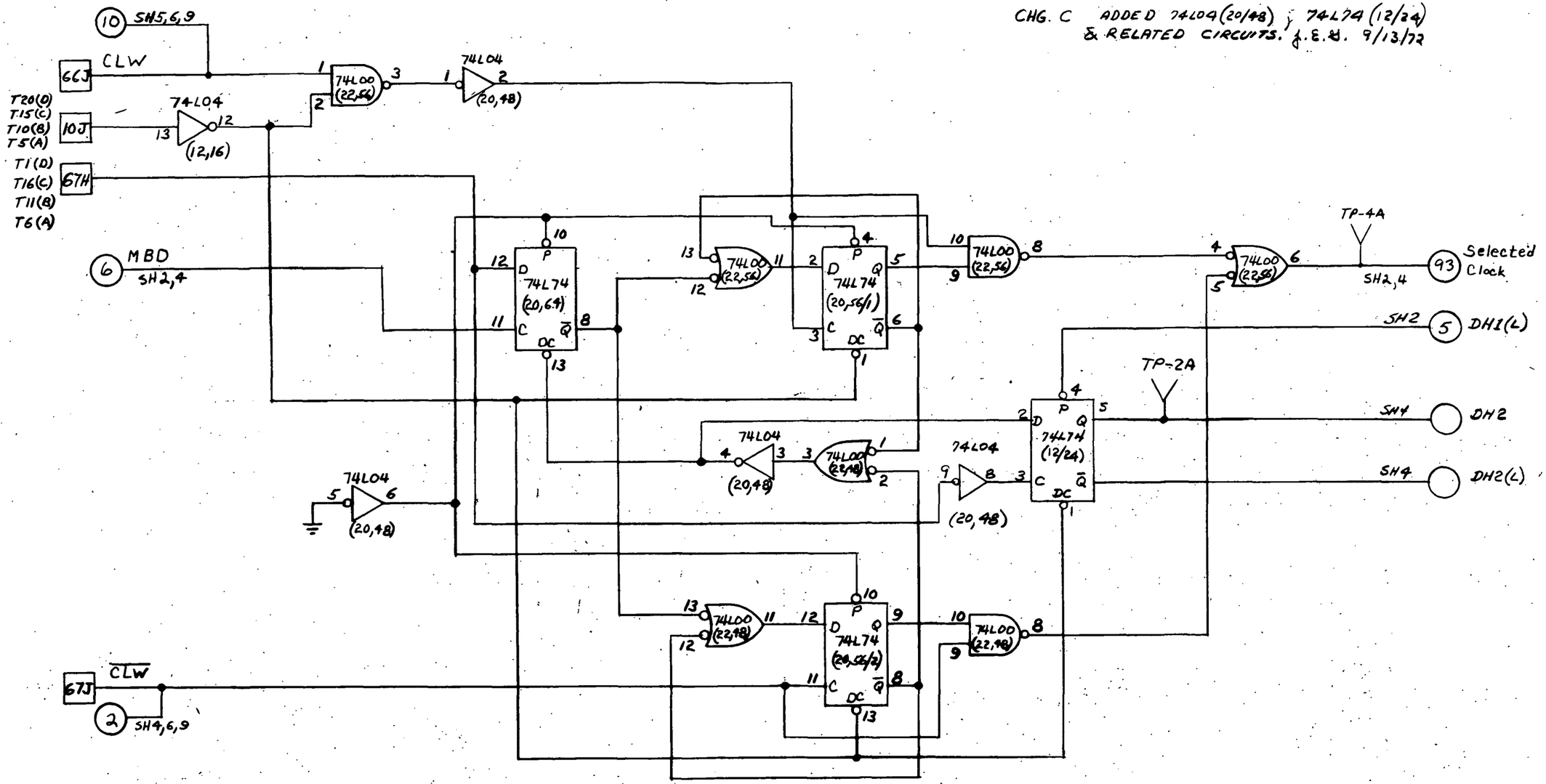
E-404D(2-62)

8 | 7 | 6 | 5

CHG. C ADDED 74L04 (20/48) & 74L74 (12/24) & RELATED CIRCUITS. J.E.H. 9/13/72



Data Clock Selector

SIZE	CODE IDENT NO.	380-112
CHG C	SCALE	SHEET 3 of 11

E-404D (2-62)

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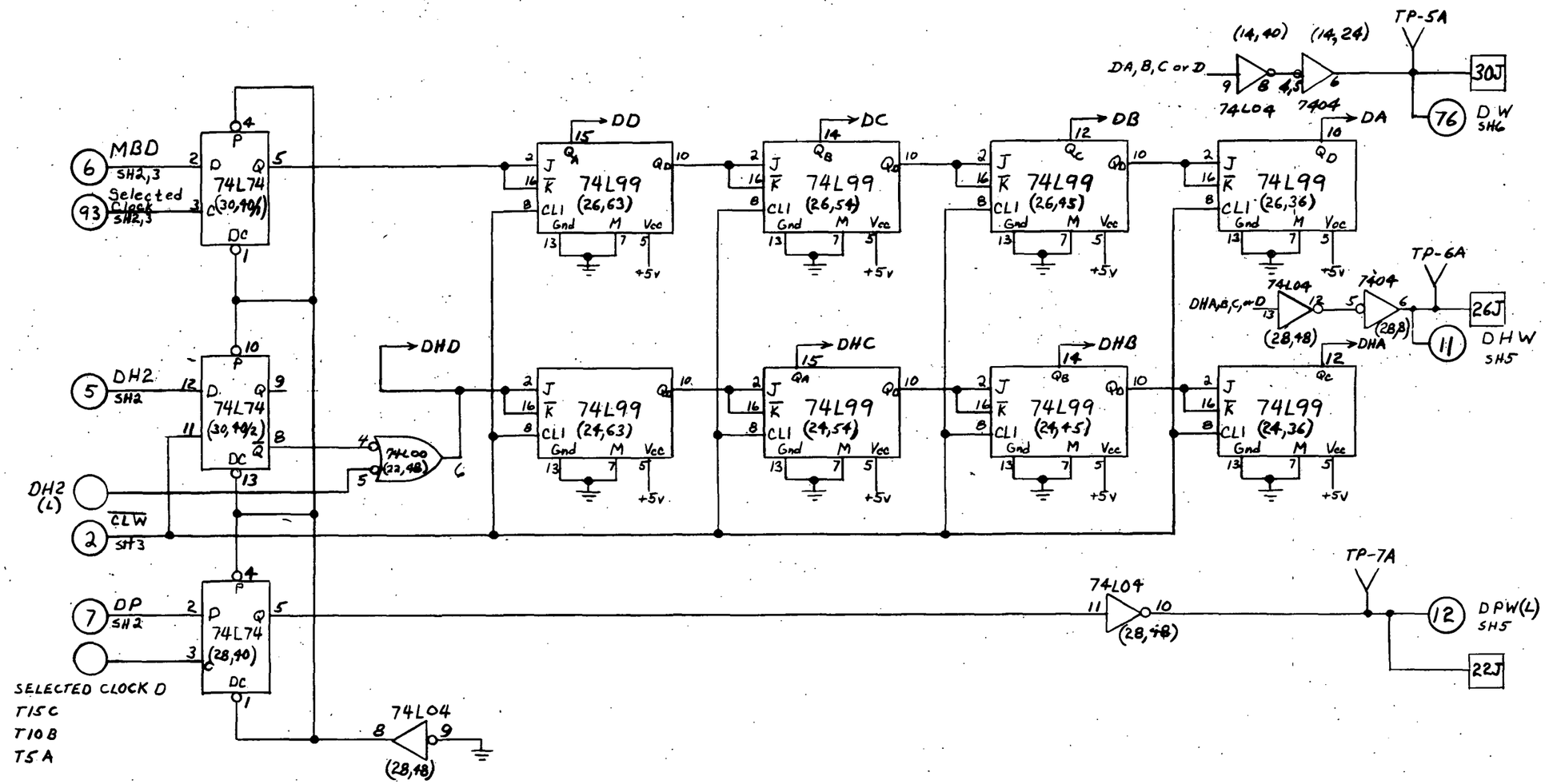
8 7 6 5



Data Delay Register

CHG. B ADDED BUFFER GATE TO DW OUTPUT. ADDED NOR GATE TO 74L74 (30,40/2) $\overline{Q}$ OUTPUT.
J.E.H. 9/13/72

CHG	SIZE	CODE IDENT NO.	
B		04236	380-112
	SCALE		SHEET 4 of 11

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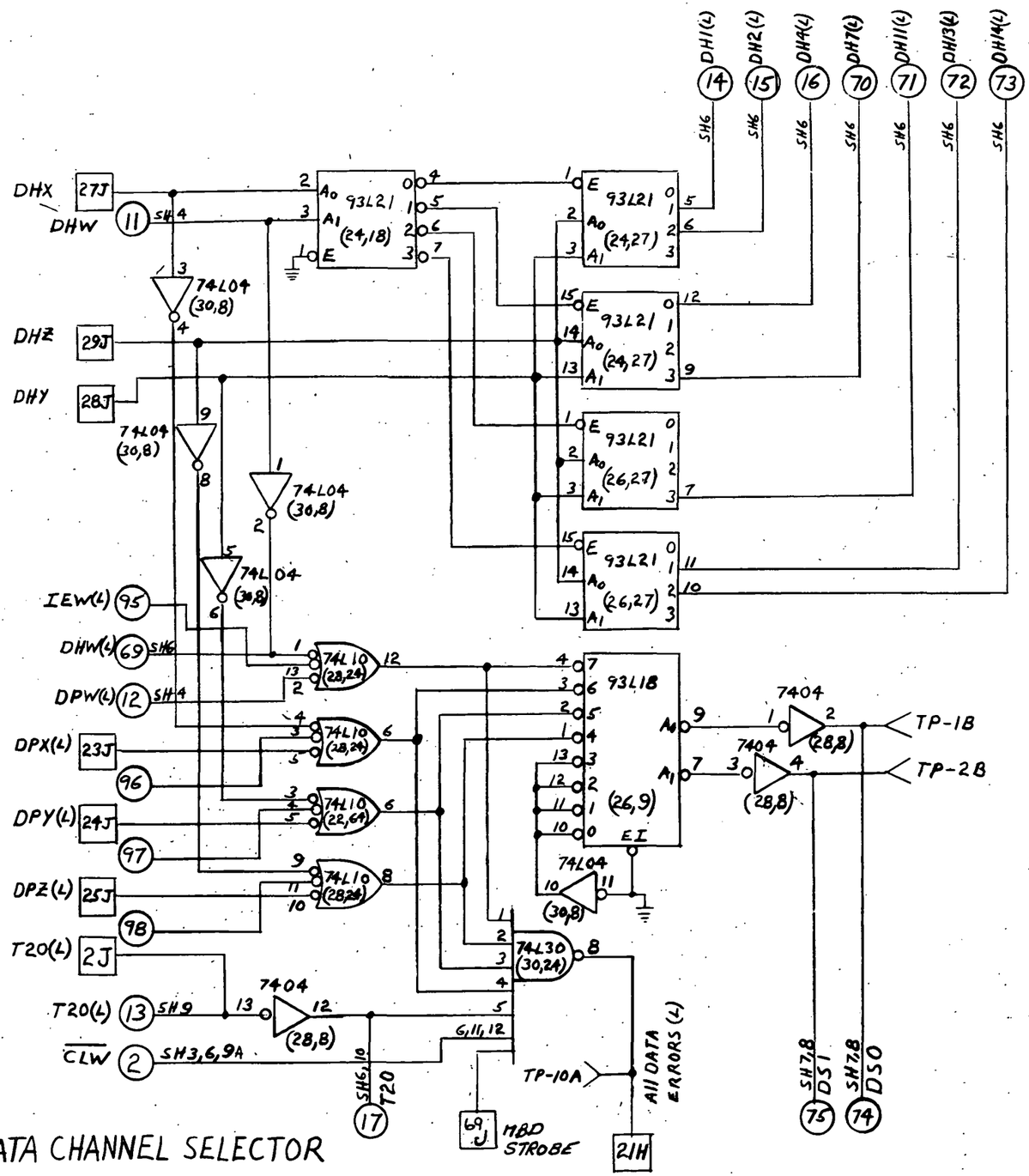
E-404D(2-62)

8 7 6 5



DATA CHANNEL SELECTOR

CHG. B ADDED MBD STROBE INPUT TO 74L30. J.E.M. 9/13/72

CHG B	SIZE	CODE IDENT NO. 04236	380-112
	SCALE		SHEET 5 of 11

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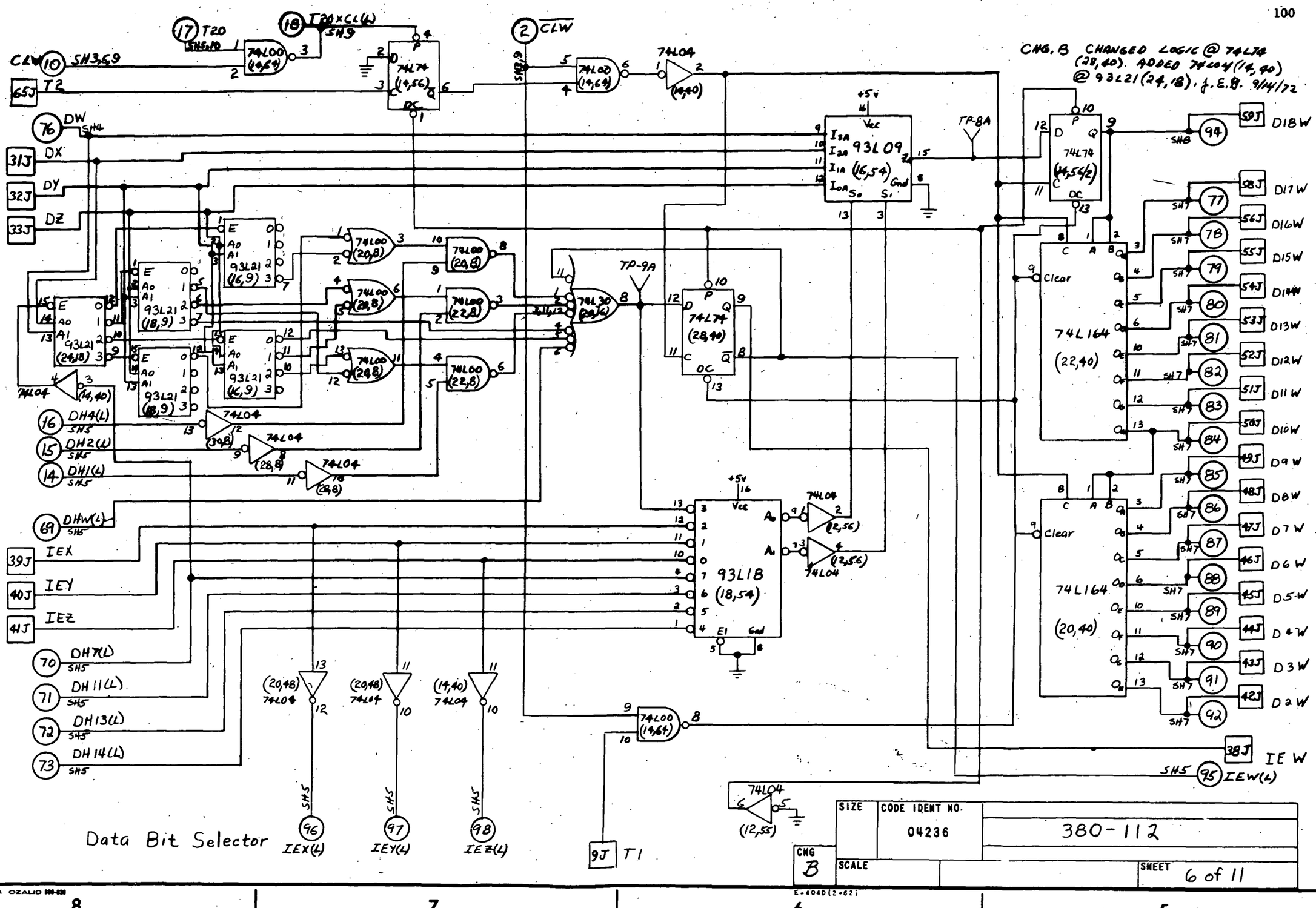
CHG. B CHANGED LOGIC @ 74L74 (28,40). ADDED 74L04(14,40) @ 93L21(24,18). J.E.B. 9/14/72



SIZE	CODE IDENT NO.	380-112
CHG B	SCALE	SHEET 6 of 11

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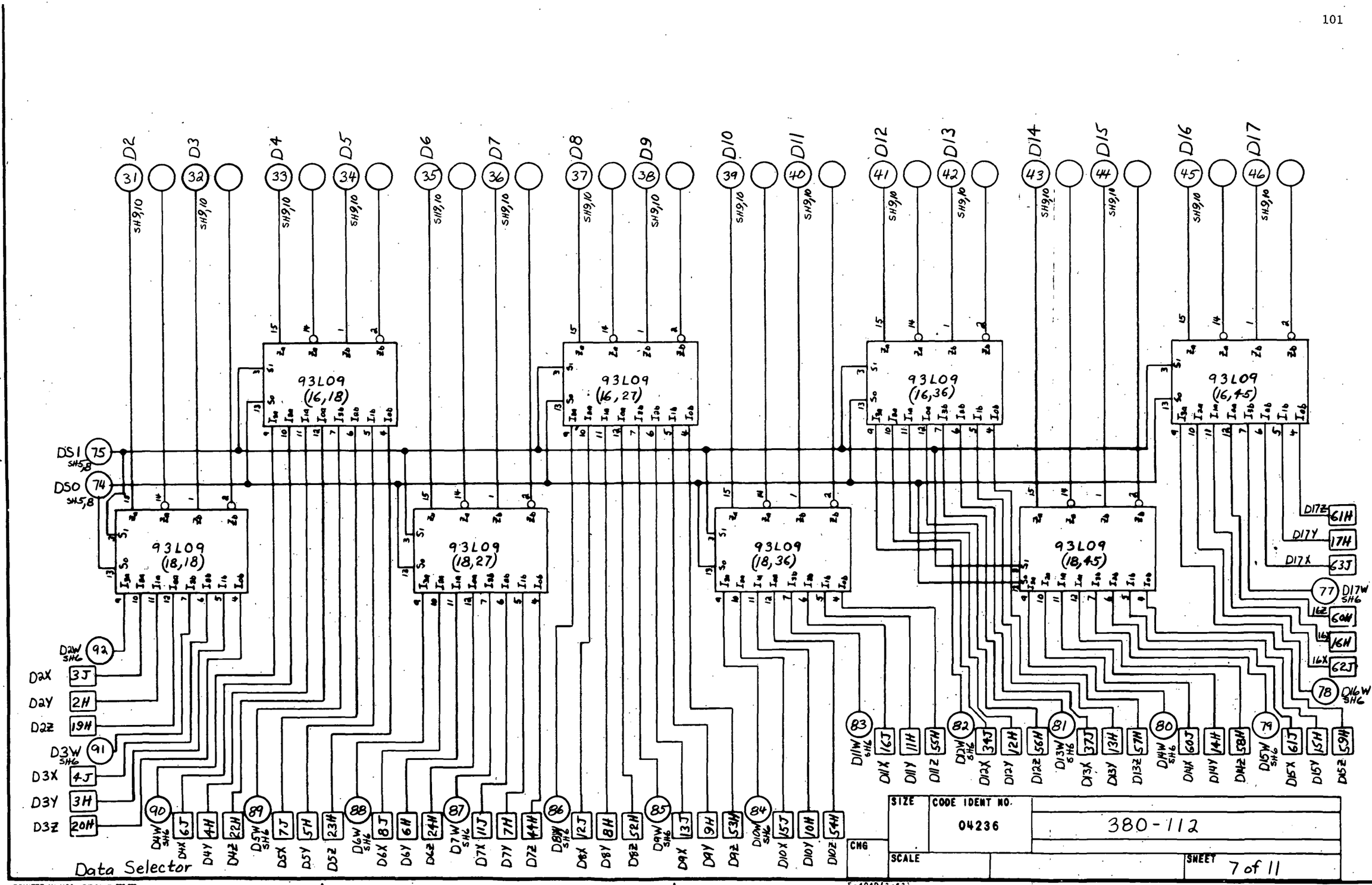
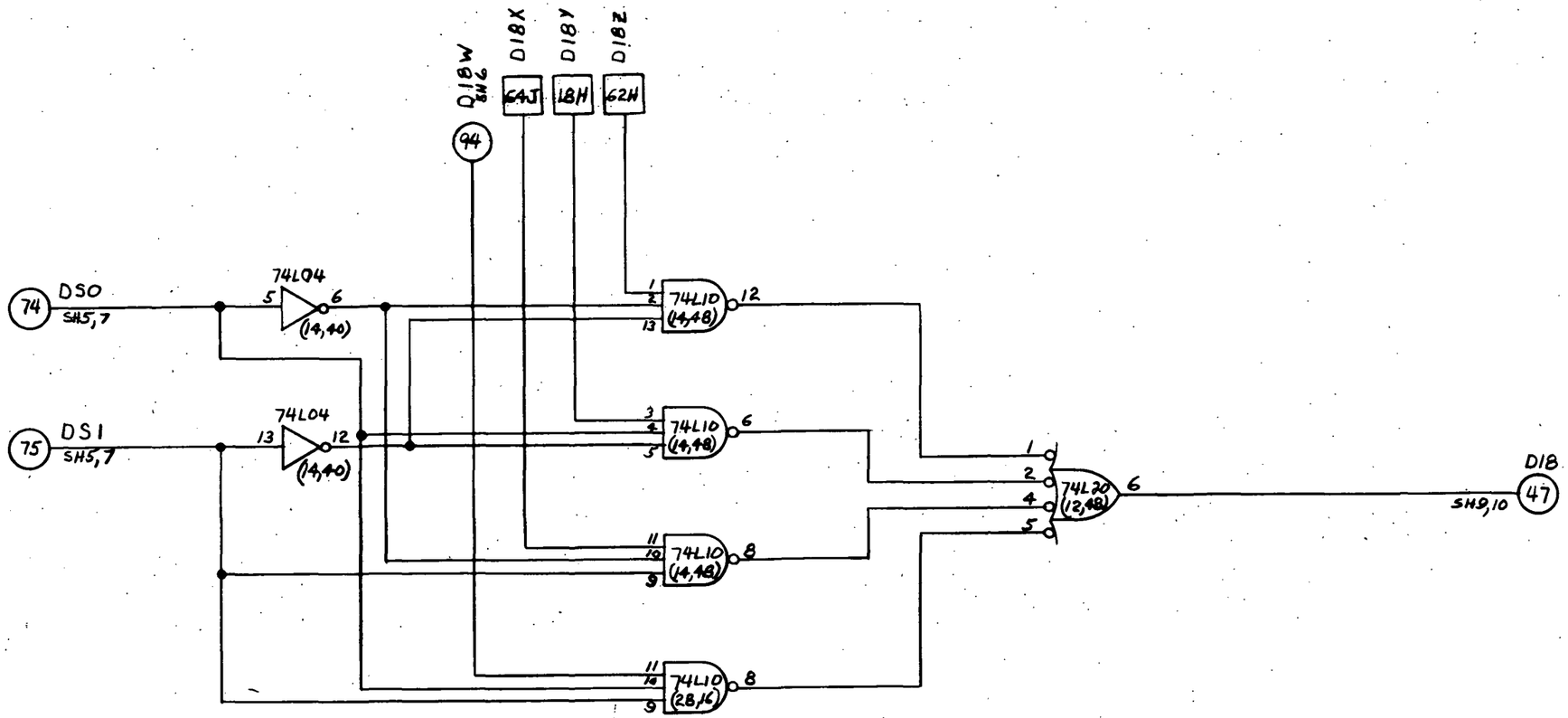
E-404D (2-62)

A

B

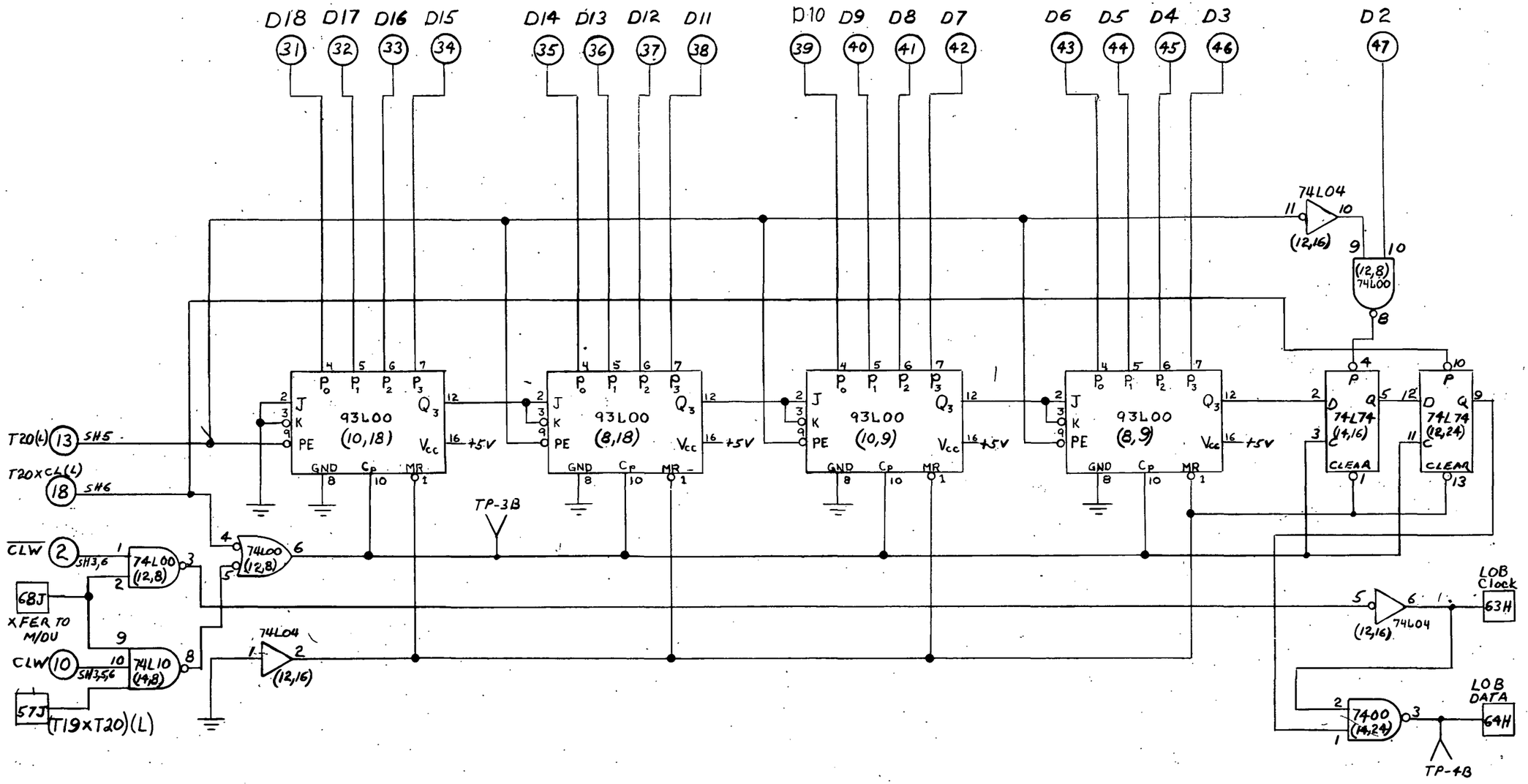
8 7 6 5


D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
93L09 (16,18)
93L09 (16,27)
93L09 (16,36)
93L09 (16,45)
93L09 (18,18)
93L09 (18,27)
93L09 (18,36)
93L09 (18,45)
DS1 SH5,8
DS0 SH5,8
D2W SH6
D3W SH6
D4W SH6
D5W SH6
D6W SH6
D7W SH6
D8W SH6
D9W SH6
D10W SH6
D11W SH6
D12W SH6
D13W SH6
D14W SH6
D15W SH6
D16W SH6
D17W SH6
D2X 3J
D2Y 2H
D2Z 19H
D3X 4J
D3Y 3H
D3Z 20H
D4X 6J
D4Y 4H
D4Z 22H
D5X 7J
D5Y 5H
D5Z 23H
D6X 8J
D6Y 6H
D6Z 24H
D7X 11J
D7Y 7H
D7Z 44H
D8X 12J
D8Y 8H
D8Z 52H
D9X 13J
D9Y 9H
D9Z 53H
D10X 15J
D10Y 10H
D10Z 54H
D11X 16J
D11Y 11H
D11Z 55H
D12X 34J
D12Y 12H
D12Z 56H
D13X 37J
D13Y 13H
D13Z 57H
D14X 60J
D14Y 14H
D14Z 58H
D15X 61J
D15Y 15H
D15Z 59H
D17Z 61H
D17Y 17H
D17X 63J
16Z 60W
16Y 16H
16X 62J
Data Selector
SIZE
CODE IDENT NO. 04236
380-112
CHG
SCALE
SHEET 7 of 11
PRINTED IN USA OZALID
E-404D(2-62)
A
B
8
7
6
5



Data Selector (con't)

SIZE	CODE IDENT NO.	
	04236	380-112
CHG	SCALE	SHEET 8 of 11



LOCAL OUTPUT REGISTER

SIZE	CODE IDENT NO.	
	04236	380-112
CHG	SCALE	SHEET 9 of 11

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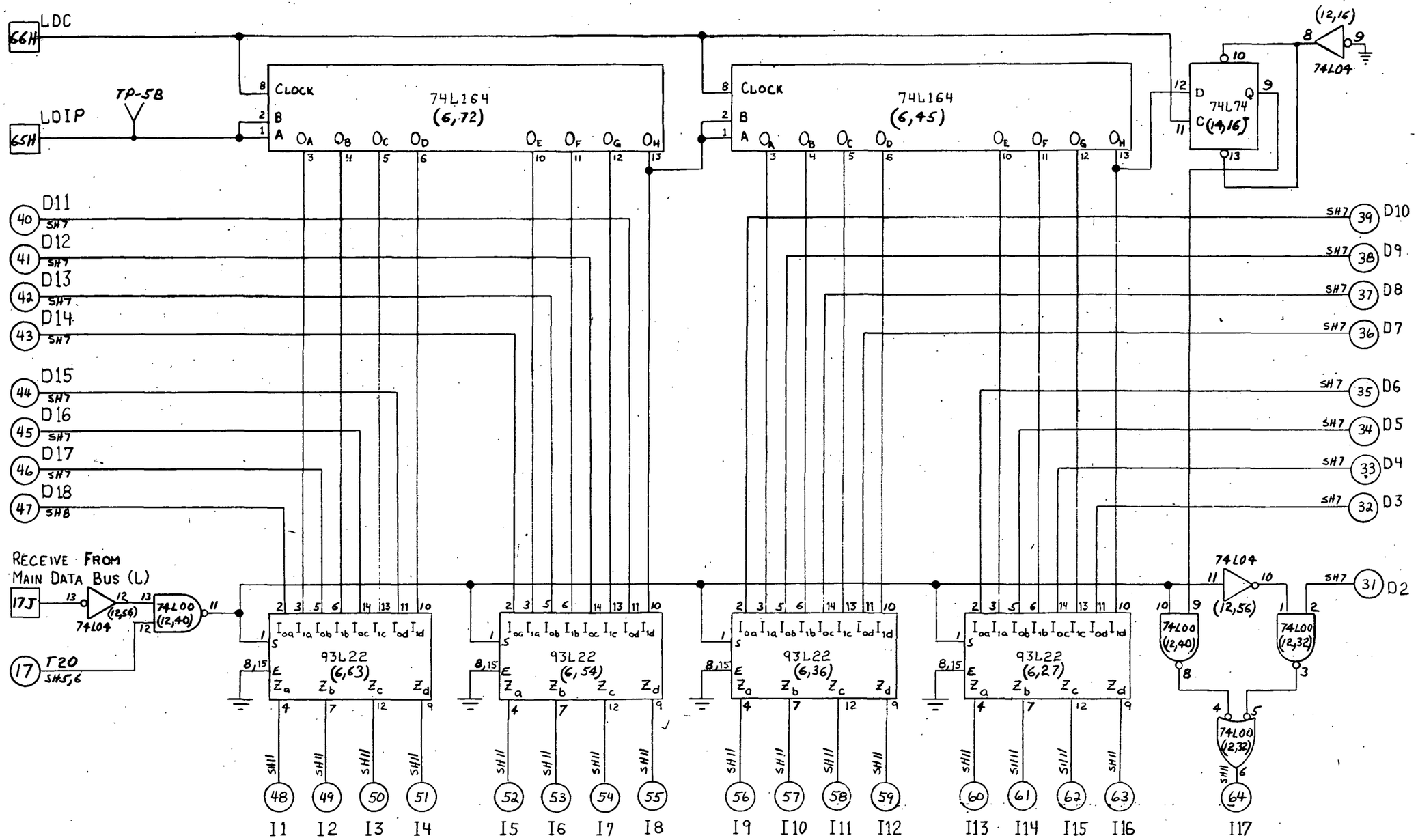
E-404D(2-62)

8 | 7 | 6 | 5



Memory Input Data Selector

SIZE	CODE IDENT NO.	
	04236	380-112
CHG A	SCALE	SHEET 10 of 11

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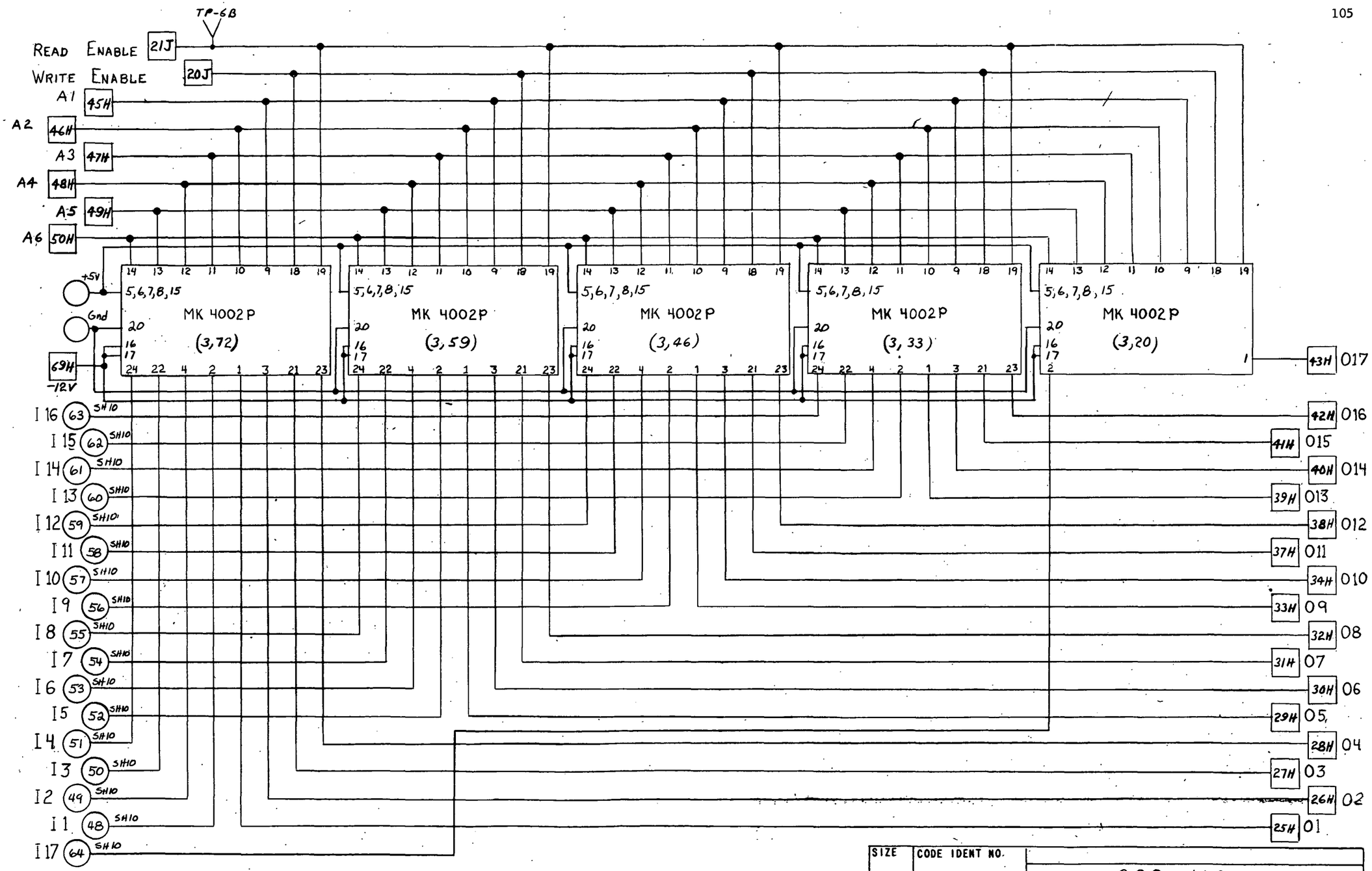
E-404D(2-62)



64 X 17 RAM

SIZE	CODE IDENT NO.	380-112
CHG	04236	
	SCALE	SHEET 11 of 11

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E-404D(2-62)

NOTES:

1. The following symbols are used on this schematic:
   - □ Connection to board connector (board has two 70 pin connectors - J and H)
   - ○ Signal continued to other sheets of schematic as indicated
   - Y Test point connection
2. The letters A, B, C, and D denote the four redundant channels.
3. The letters W, X, Y, and Z are general designations for which A, B, C, and D may be substituted when considering a specific channel.
4. The alpha numeric designation in each logic symbol indicates the package location on the board.
5. Pin numbers on this schematic are package pin numbers. The board contains only 16 pin sockets; consequently, for packages with less than 16 pins, some pin numbers will change on the board back plane wiring list.

TEST POINT ASSIGNMENTS

T.P. No.	SIGNAL NAME	Sheet No.
1A	L.A. Xfer (L)	11
2A	Data To M/DU	3
3A	Receive From MDB (L)	3
4A	Write Enable	3
5A	Xfer To M/DU	3
6A	Status Data Select	4
7A	Read Address Select	4
8A	Load Clock (L)	4
9A	Data Shift Enable	4
10A	Data Reg Shift (L)	4
1B	LDC	11
2B	Xmit Even Parity	5
3B	Reject I. D. Word (L)	5
4B	Inhibit SW Decoding (L)	5
5B	OW	8
6B	OW'	8
7B	Set Even Parity F.F. W	8
8B	ADW	8
9B	DCB	10
10B	DAB	10

DRAWN BY Ed Schlytter	DEPT 1622	DATE 19 Nov 71
CHECKER		
STRESS ENGR		
WT ENGR		
MATL ENGR		
RELIABILITY		
GR ENGR D. Leck		11/19/71
PROJECT F. E. Hoolwin		12-1-71
CUST RPRSNTV		

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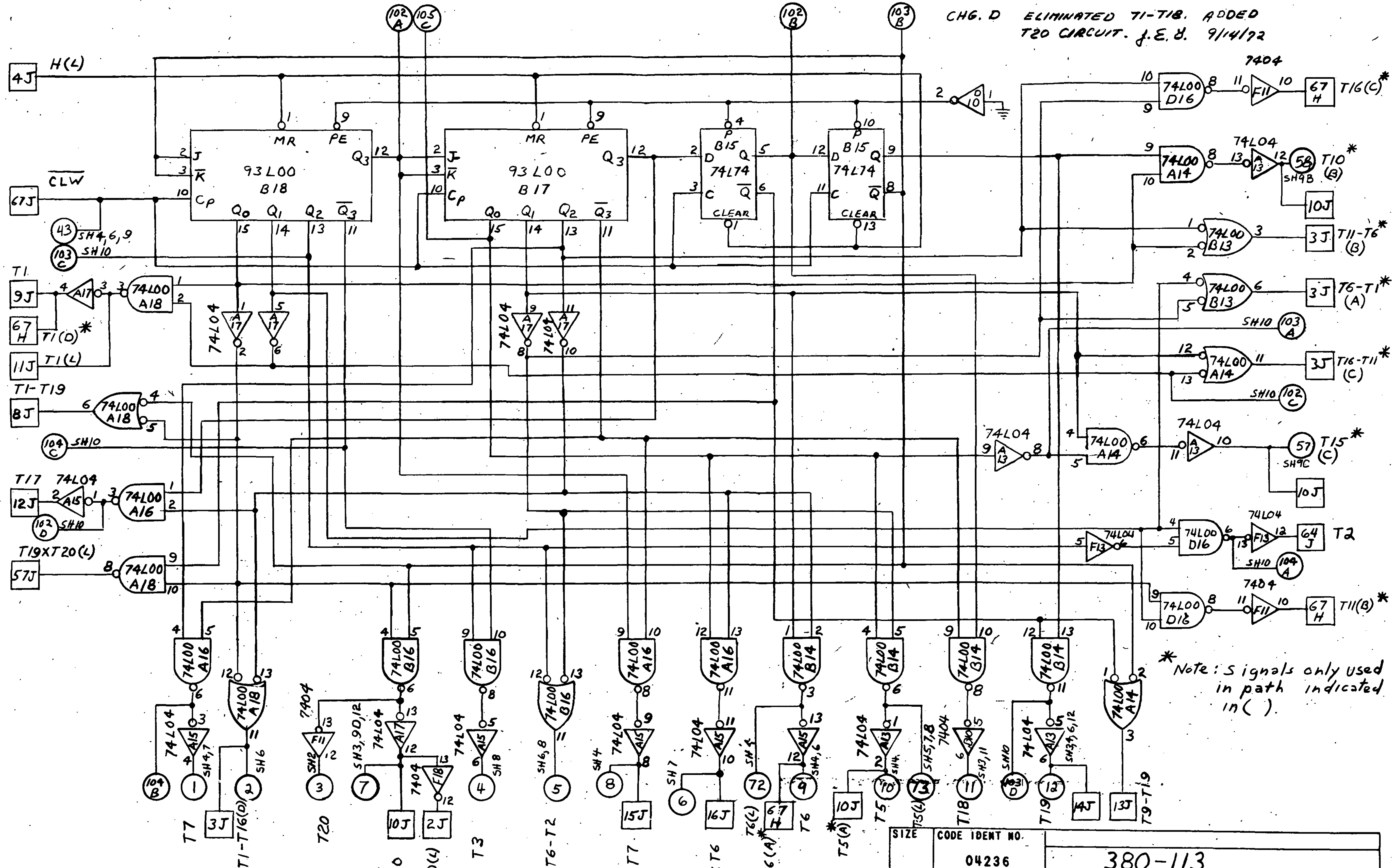
POST OFFICE BOX 179, DENVER, COLORADO

CONTROL AND OUTPUT DATA LOGIC

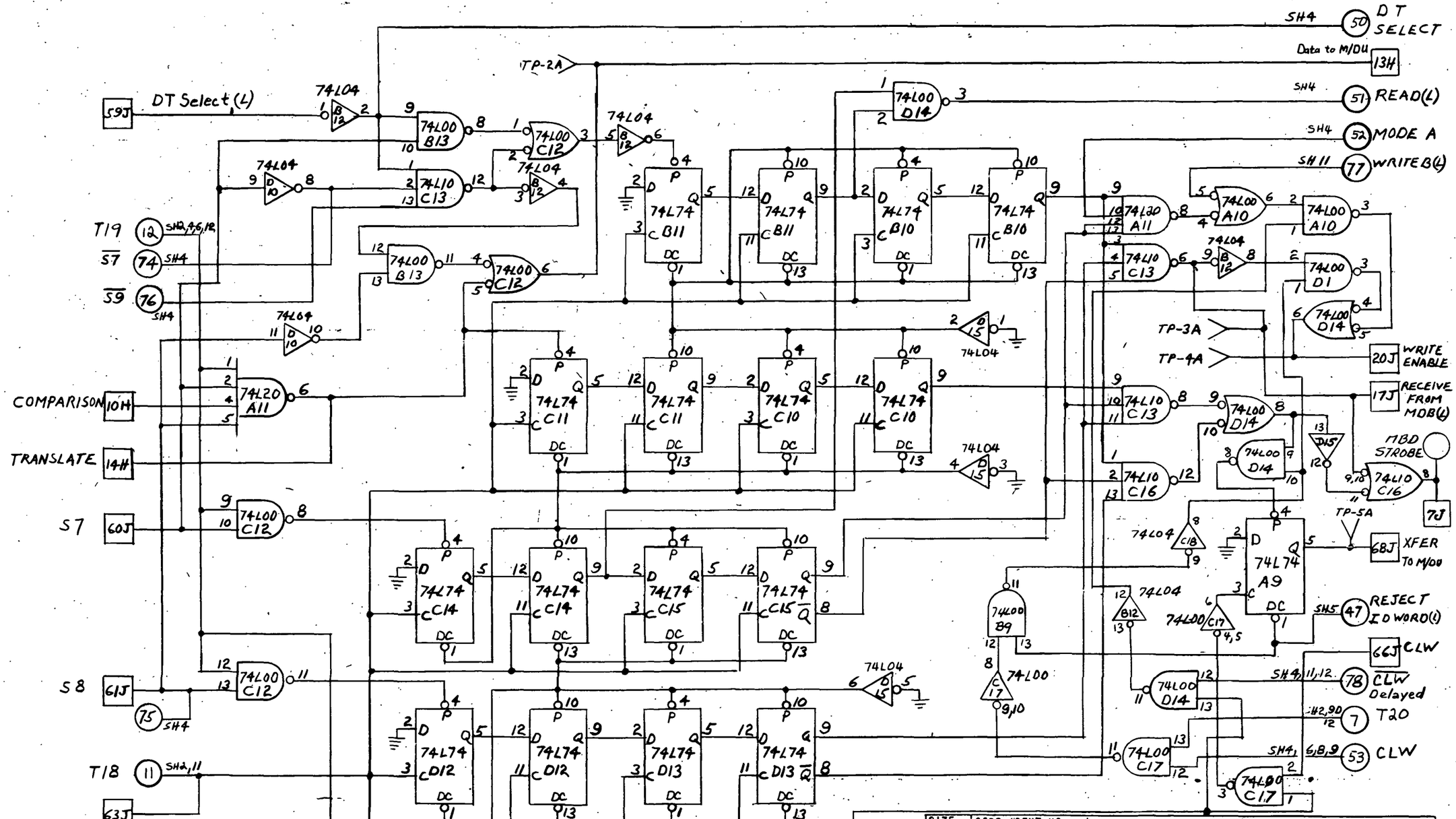
SIZE	CODE IDENT NO.	
	04236	380-113
SCALE		SHEET 1 of 12



BIT TIMER

SIZE	CODE IDENT NO.	
	04236	380-113
CHG D	SCALE	SHEET 2 of 12

CHG. D ADDED B9, C16, C18, D15
& RELATED CKTS J.E.B. 9/18/72



CONTROL LOGIC 1

CHG	SIZE	CODE IDENT NO.	
D		04236	380-113
	SCALE		SHEET 3 of 12

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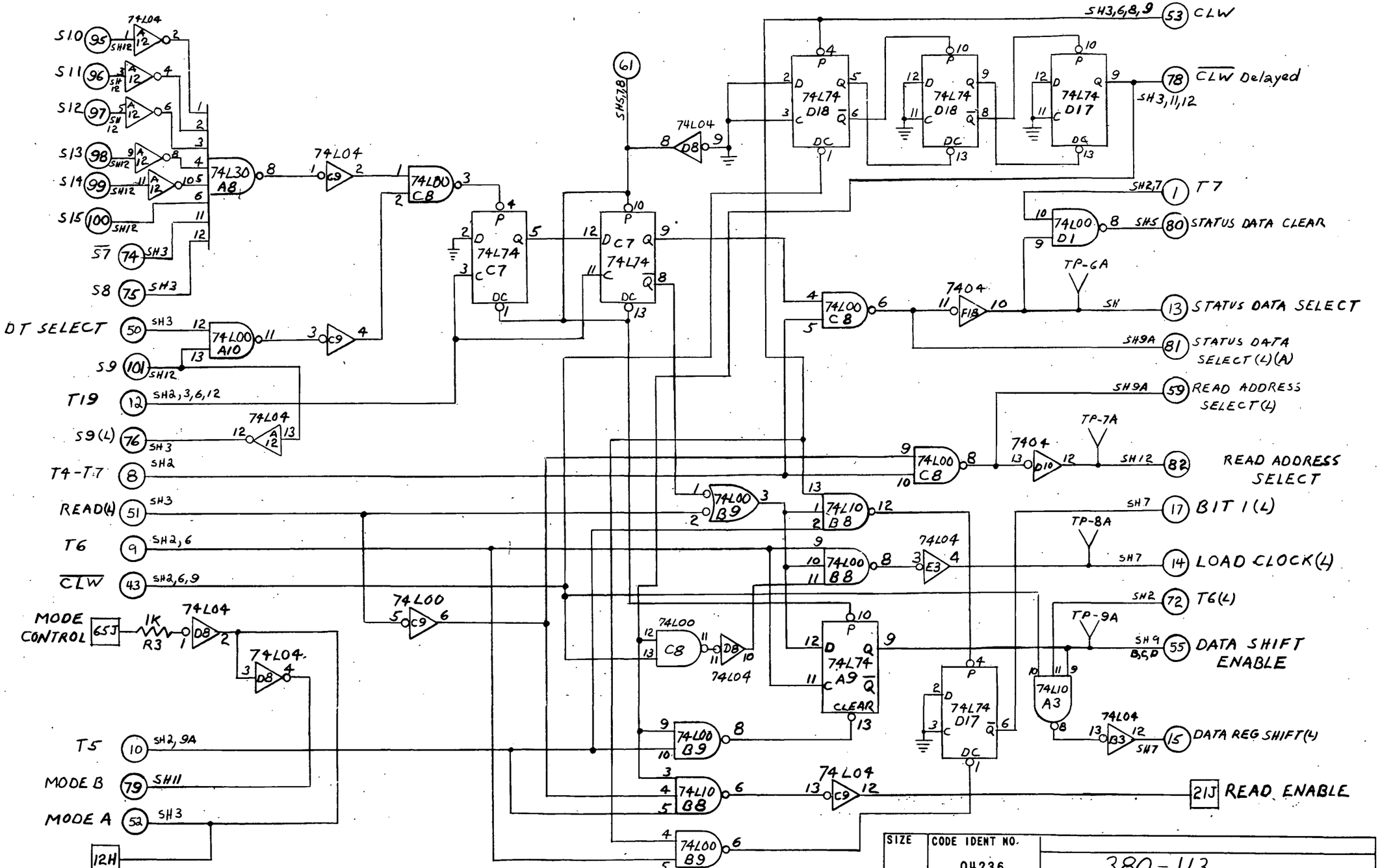
E-404D (2-62)

B

A

8 7 6 5



CONTROL LOGIC 2

CHG. C ADDED C8, D8, E3 & RELATED CIRCUITS. J.E.H. 9/18/72

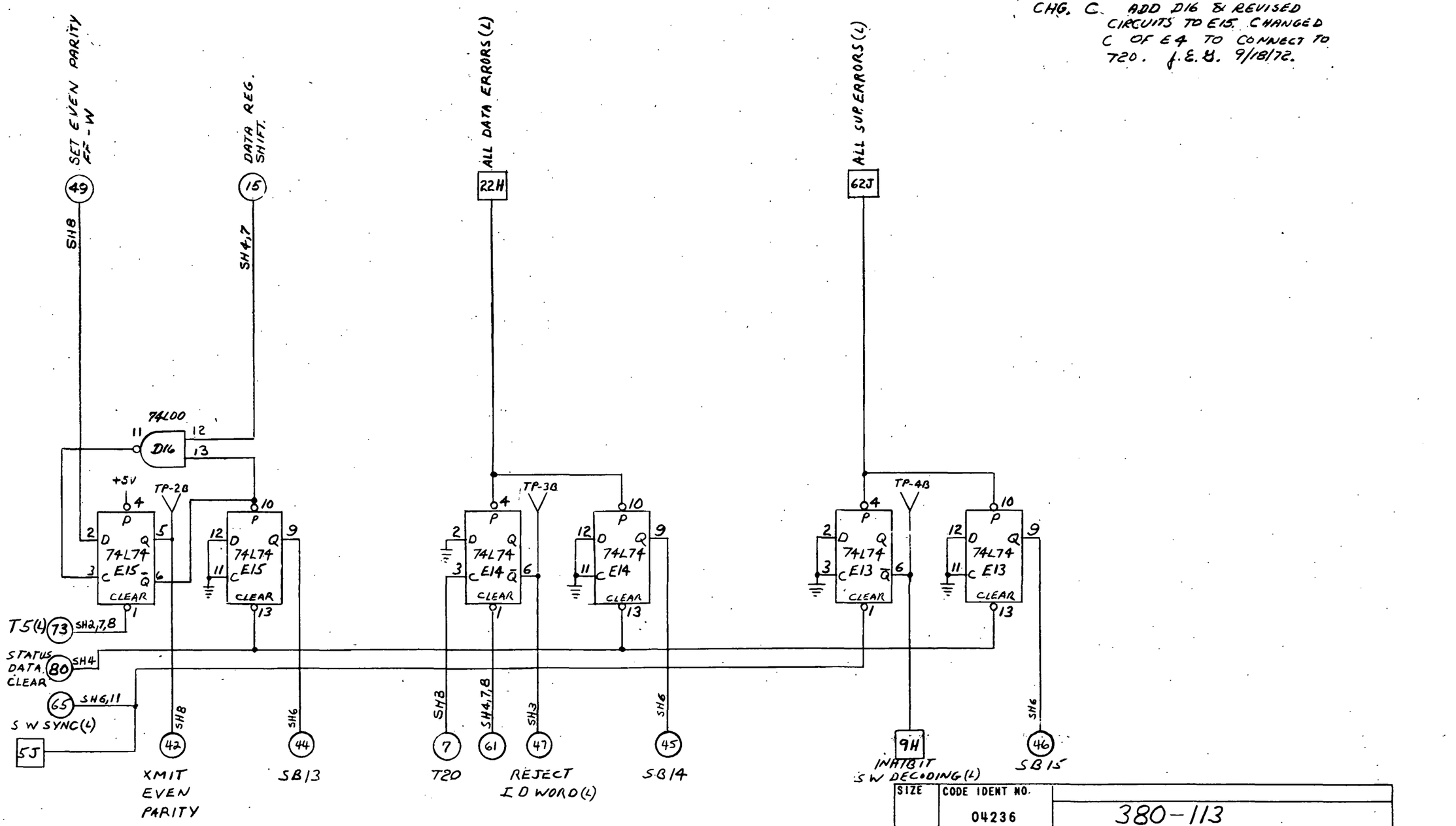
SIZE	CODE IDENT NO.	380-113
	04236	
CHG C	SCALE	SHEET 4 of 12

E-404D(2-62)

CHG. C. ADD D16 & REVISED CIRCUITS TO E15. CHANGED C OF E4 TO CONNECT TO 720. J.E.B. 9/18/72.

B

A



ALL FAULTS LOGIC

SIZE	CODE IDENT NO.	380-113
	04236	
CHG C	SCALE	SHEET 5 of 12

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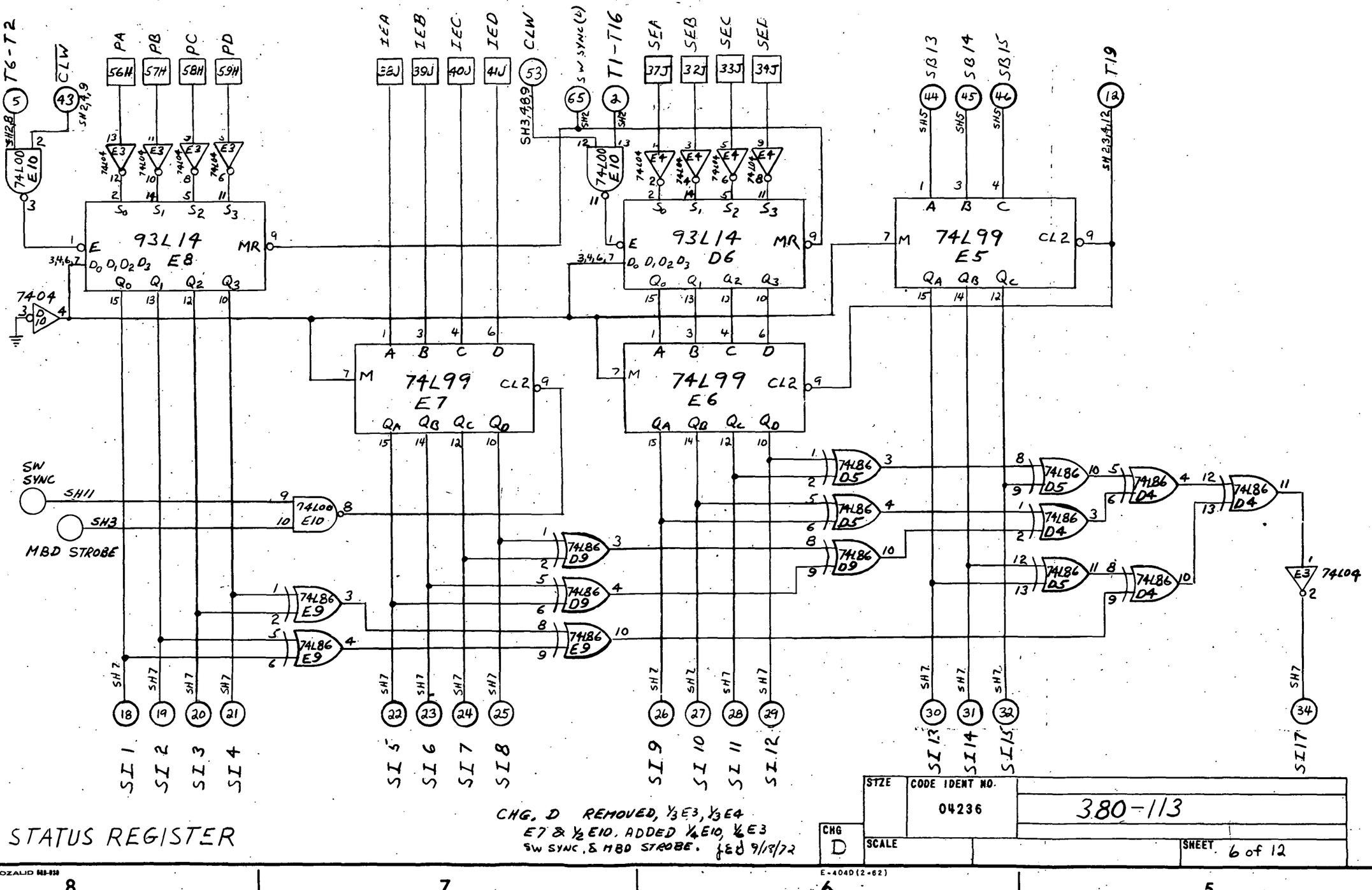
E-404D (2-62)

8 7 6 5



CHG. D REMOVED, ½ E3, ½ E4
E7 & ½ E10, ADDED ¼ E10, ½ E3
SW SYNC. & MBD STROBE. fed 9/8/72

STATUS REGISTER

CHG	SIZE	CODE IDENT NO.	
D		04236	380-113
	SCALE		SHEET 6 of 12

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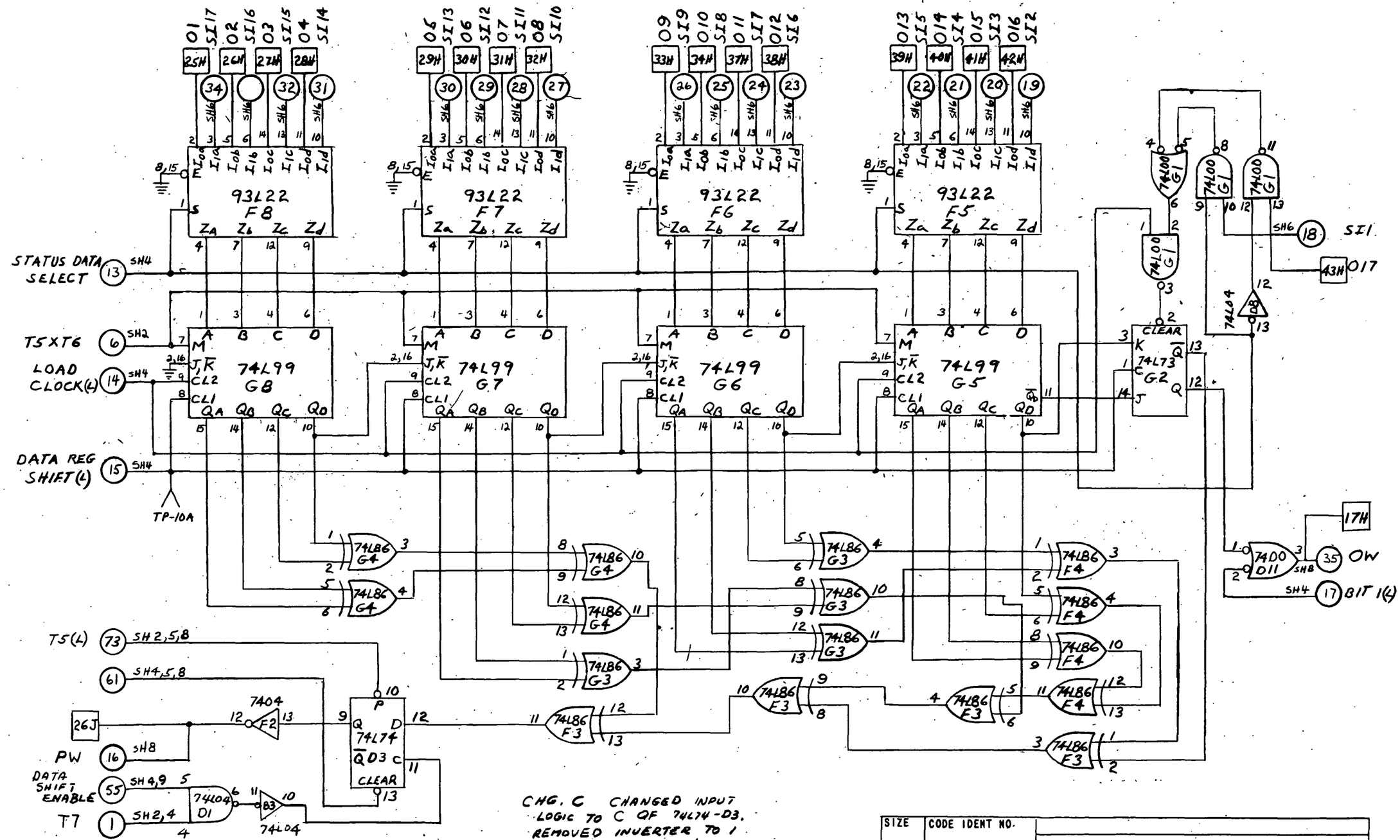
E-404D(2-62)



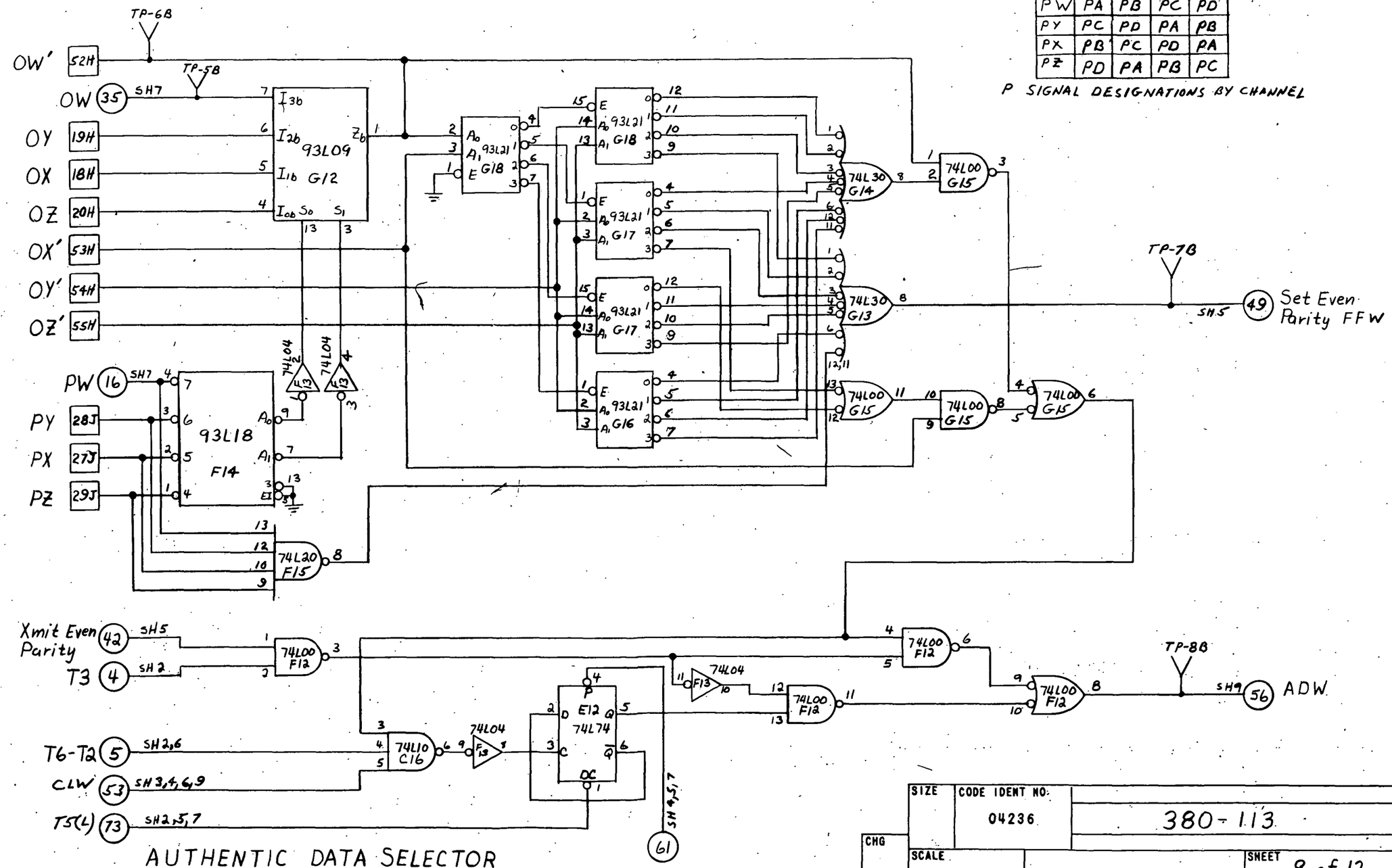
CHG. C CHANGED INPUT LOGIC TO C OF 74L74-D3. REMOVED INVERTER TO 1 INPUT 61. J.E.S 9/18/72

DATA REGISTER & PARITY CHECKER

CHG	SIZE	CODE IDENT NO.	380-113
C		04236	
	SCALE		SHEET 7 of 12

SIG. NAME	CHANNEL A	B	C	D
PW	PA	PB	PC	PD
PY	PC	PD	PA	PB
PX	PB	PC	PD	PA
PZ	PD	PA	PB	PC

P SIGNAL DESIGNATIONS BY CHANNEL



AUTHENTIC DATA SELECTOR

SIZE	CODE IDENT NO.	380-113
	04236	
CHG	SCALE	SHEET 8 of 12

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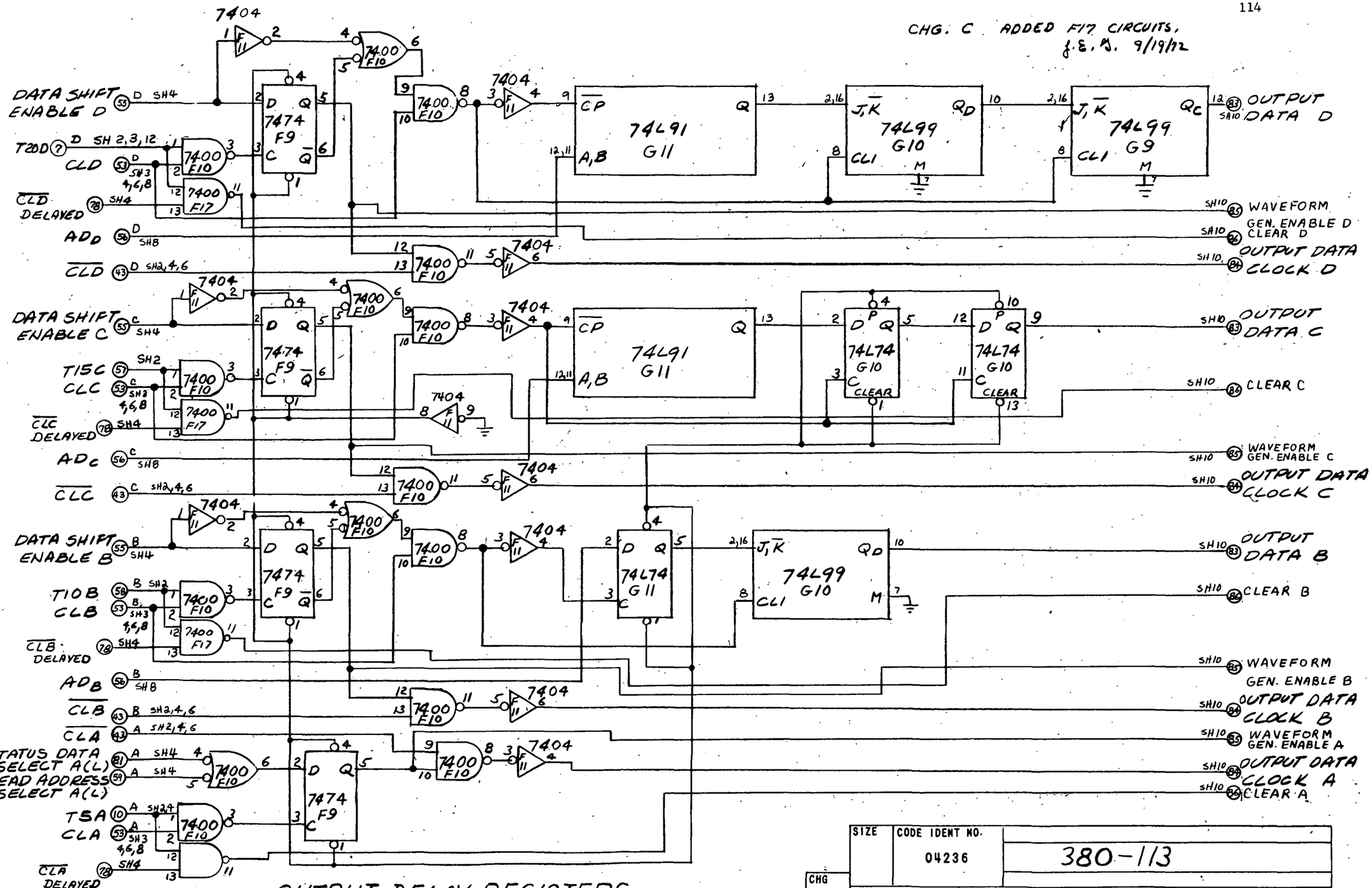
E-404D(2-62)

CHG. C ADDED F17 CIRCUITS,
J.E.M. 9/19/72



OUTPUT DELAY REGISTERS

SIZE	CODE IDENT NO.	
	04236	380-113
CHG C	SCALE	SHEET 9 of 12

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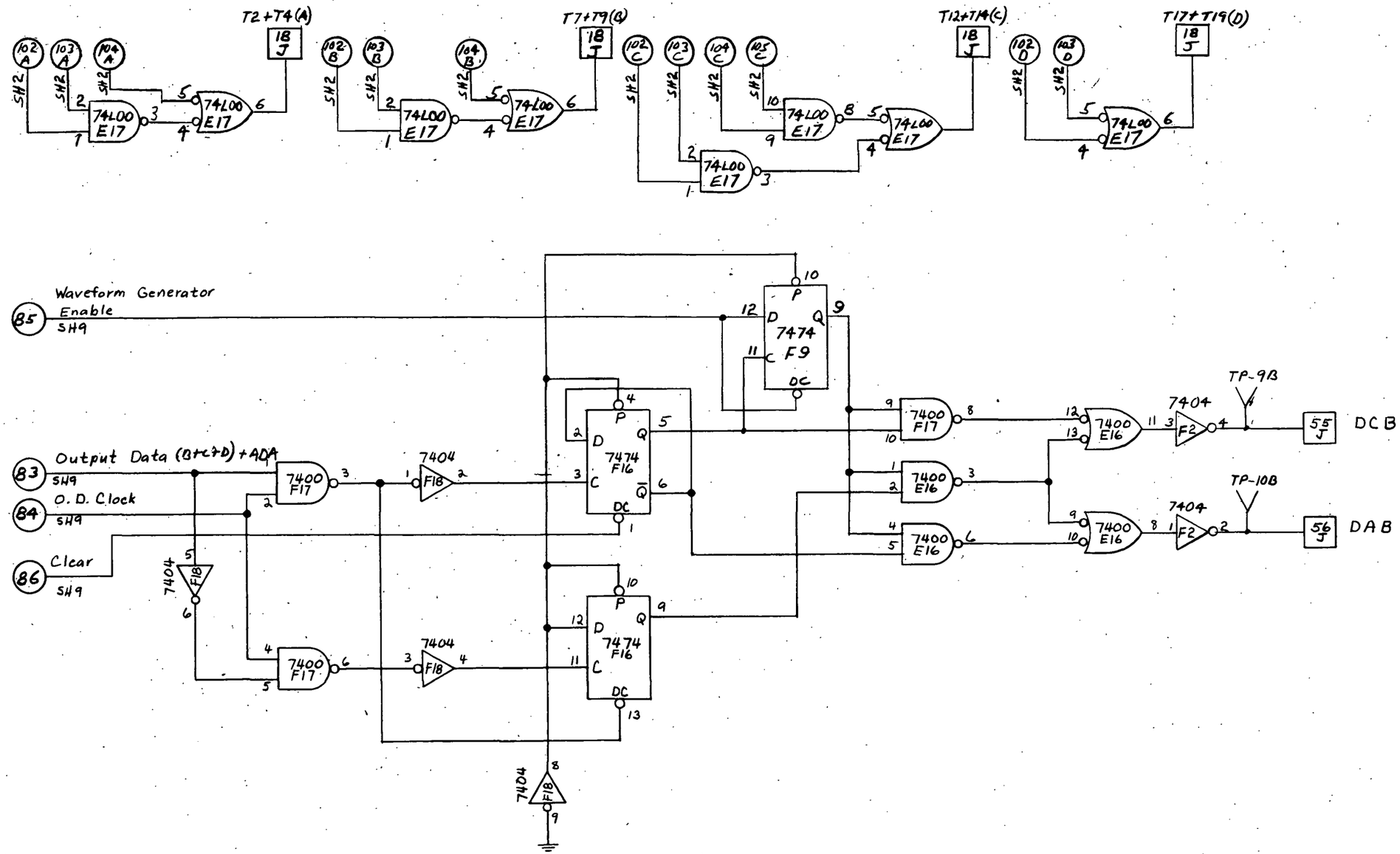
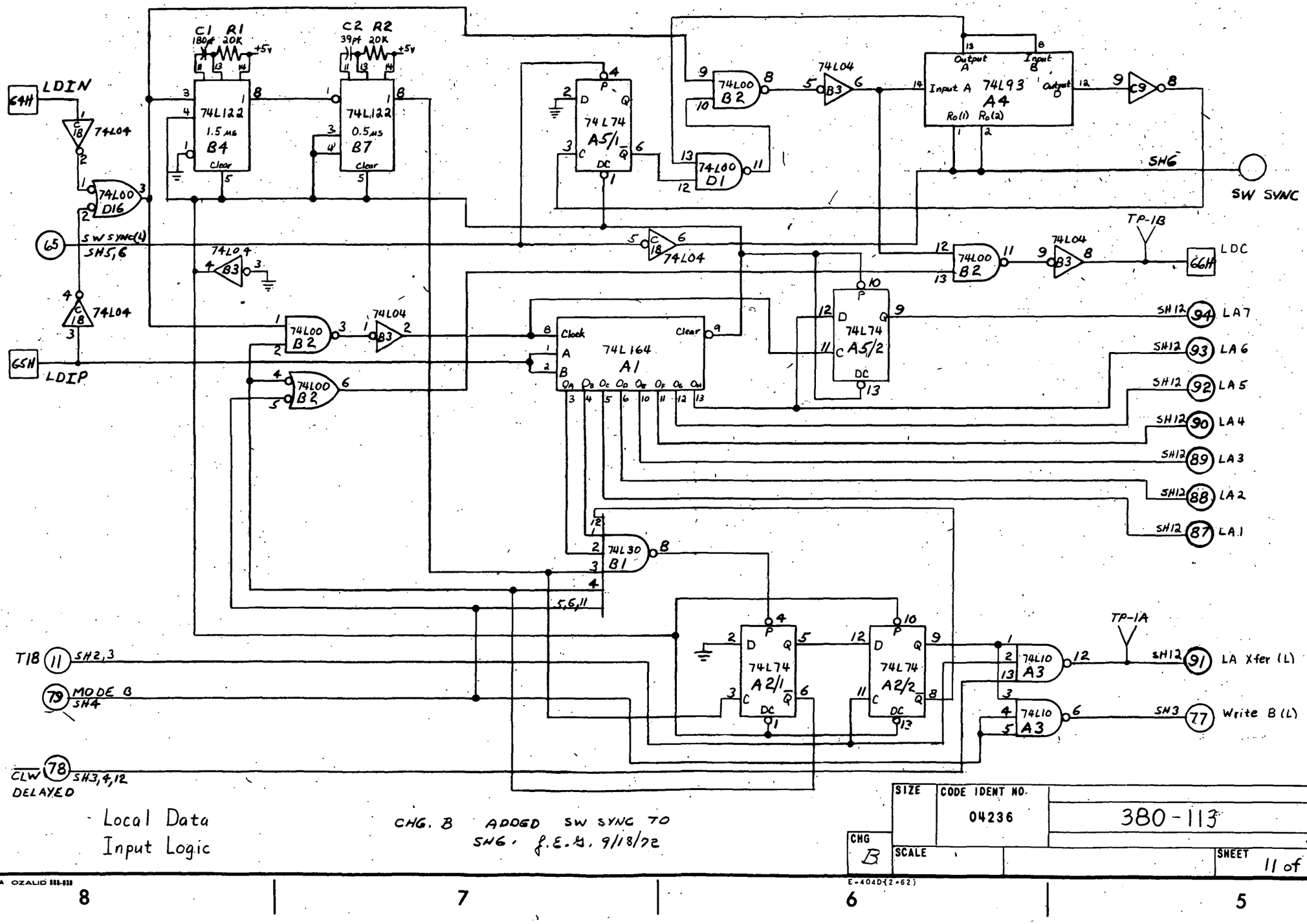
E-404D(2-62)



MAIN DATA BUS
WAVEFORM GENERATOR

CHG	SIZE	CODE IDENT NO.	
A		04236	380-113
	SCALE		SHEET 10 of 12



Local Data Input Logic

CHG. B ADDED SW SYNC TO SH6. J.E.S. 9/18/72

SIZE	CODE IDENT NO.	380-113
CHG B	SCALE	SHEET 11 of 12

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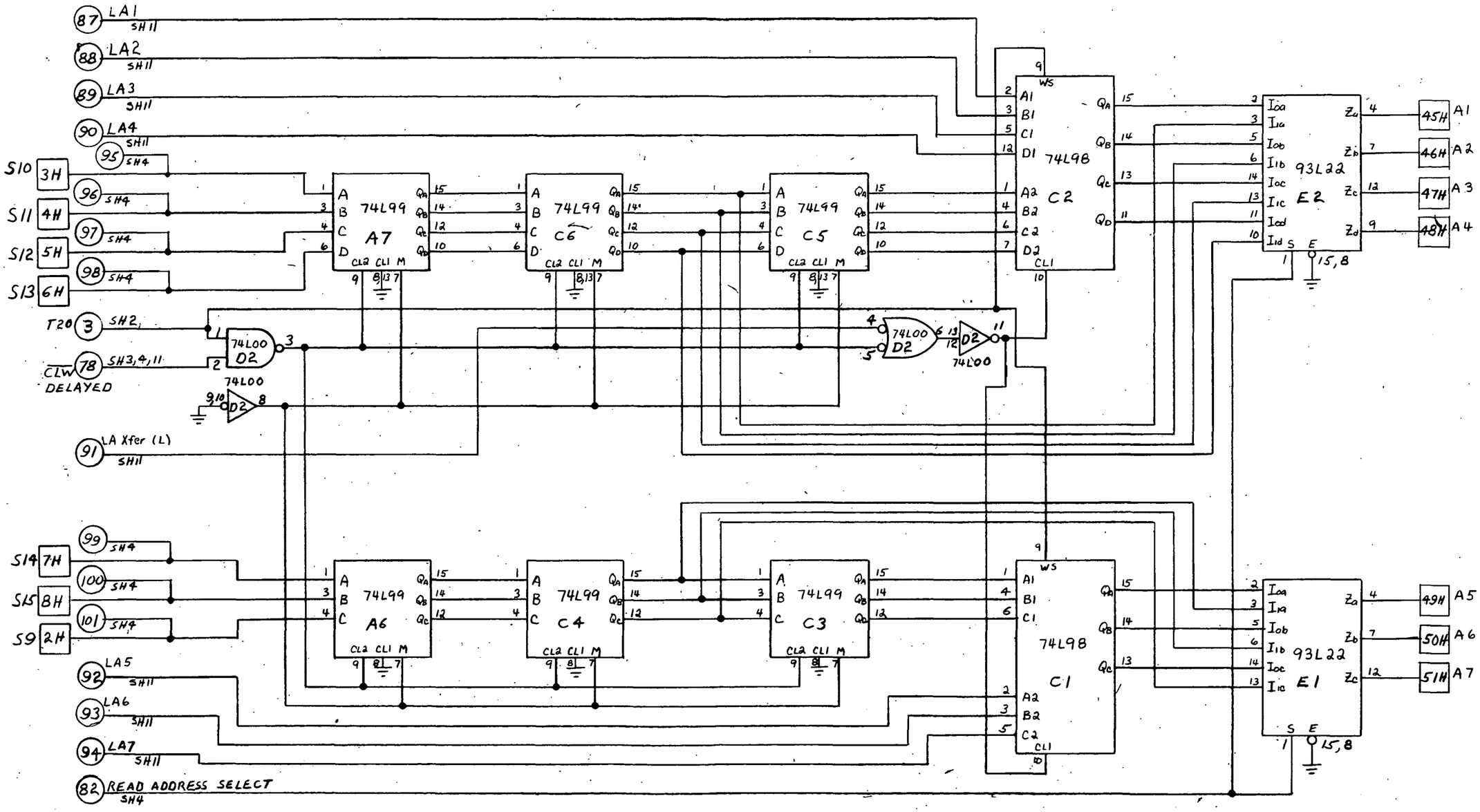
E-404D(2-62)



Memory Address Register

CHG. C CHANGED T20 BALLON NO. FROM 12 TO 3. DELETED REF. TO SH3 & 9D ON T20 LINE. J.E.P. 9/18/72

SIZE	CODE IDENT NO.	380-113
CHG C	SCALE	SHEET 12 of 12

NOTES:

1. This schematic shows the various transmitters and receivers used in one channel of the Data Terminal. The circuits for all four channels are contained on three printed circuit boards. The circuits and the boards on which they appear are tabulated below. Two numbers are assigned for each terminal shown on the schematics. This is because more than one circuit of the same type is located on a board. The top numbers refer to one circuit and the bottom numbers to another. To aid in locating a particular circuit, the number(s) of the terminal(s) on which the output signal appears is also included in the tabulation. For more information refer to assembly drawing 380-140.

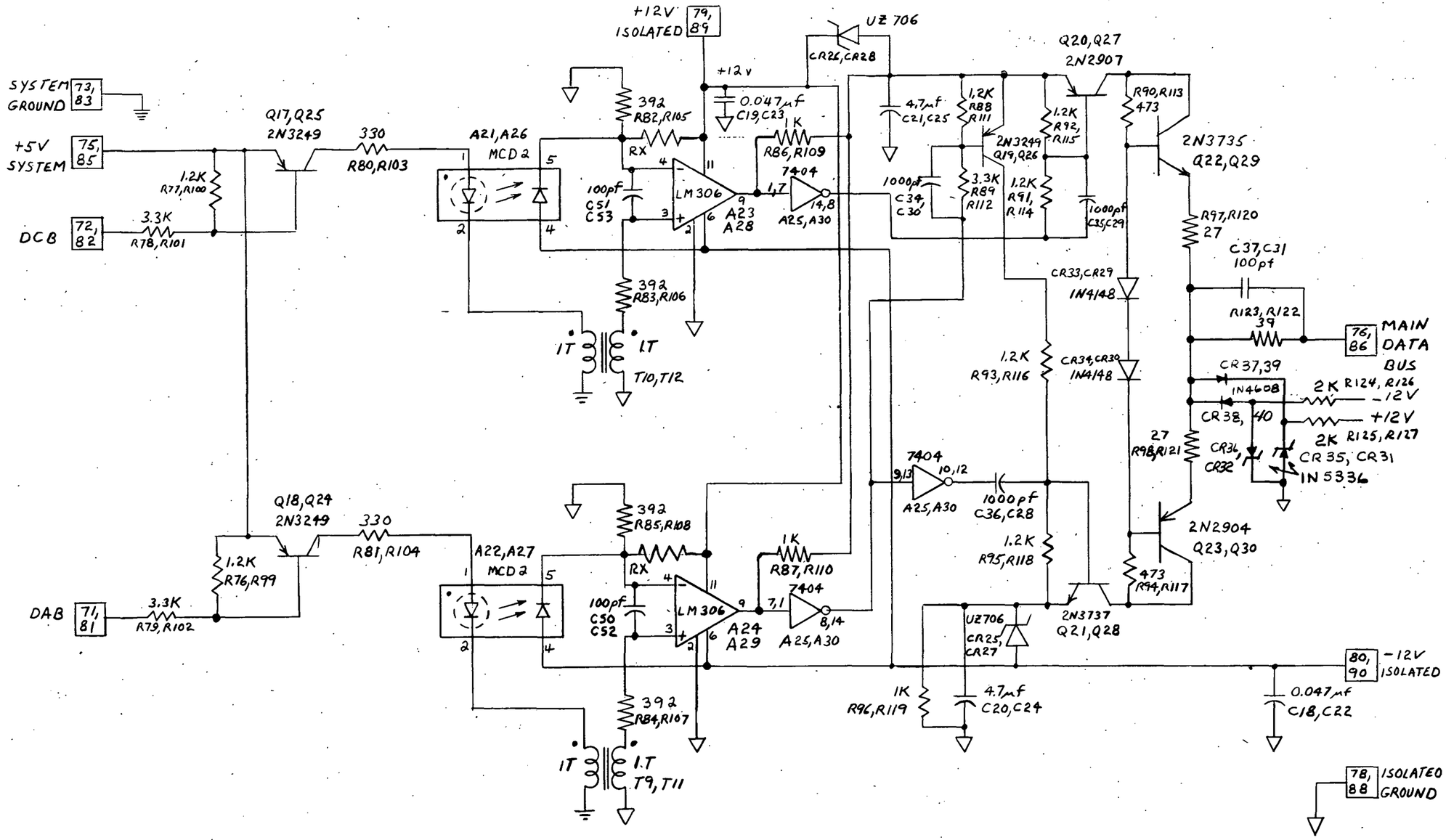
	CHANNEL DESIGNATION							
	A		B		C		D	
CIRCUIT NAME	Bd No.	Term. No.	Bd No.	Term. No.	Bd No.	Term. No.	Bd No.	Term. No.
Main Data Bus Driver	-009	86	-009	76	-019	86	-019	76
Main Sup. Bus Receiver	-009	8	-019	8	-029	8	-009	38
Main Data Bus Receiver	-009	18,15	-019	18,15	-029	18,15	-019	38,35
Local Sup. Bus Driver	-009	45	-019	45	-029	45	-009	65
Local Data Bus Driver	-009	55	-019	55	-029	55	-019	65
Local Data Bus Receiver	-009	28,25	-019	28,25	-029	28,25	-029	38,35

DRAWN BY O. LECK	DEPT 1622	DATE 4-27-72
CHECKER		
STRESS ENGR		
WT ENGR		
MATL ENGR		
RELIABILITY		
GR ENGR		
PROJECT J. E. Goodwin		5/1/72
CUST RPRSNTV		

MARTIN MARIETTA CORPORATION
POST OFFICE BOX 179, DENVER, COLORADO

DATA TERMINAL
LINE DRIVERS & RECEIVERS

SIZE	CODE IDENT NO.	
	04236	380-114
SCALE		SHEET 1 of 7

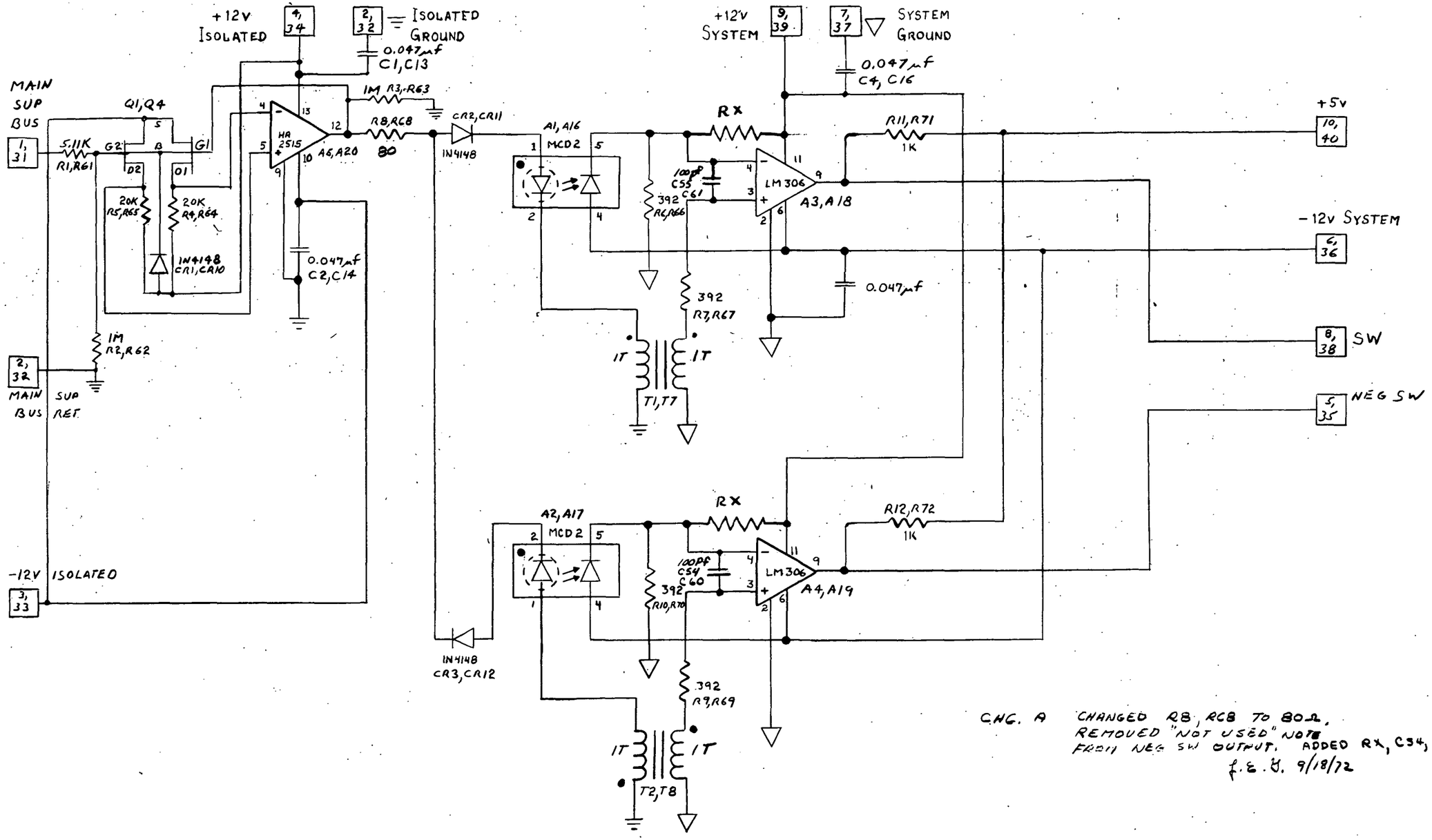


CHG. A: REVISED ZENER OUTPUT CLAMP CKT. ADDED RX, C51, 53, 50, 52 J.E.S. 11-17-72

Main Data Bus Transmitter

CHG	SIZE	CODE IDENT NO.	
A		04236	380-114
	SCALE		SHEET 2 of 7

E-404D(2-62)



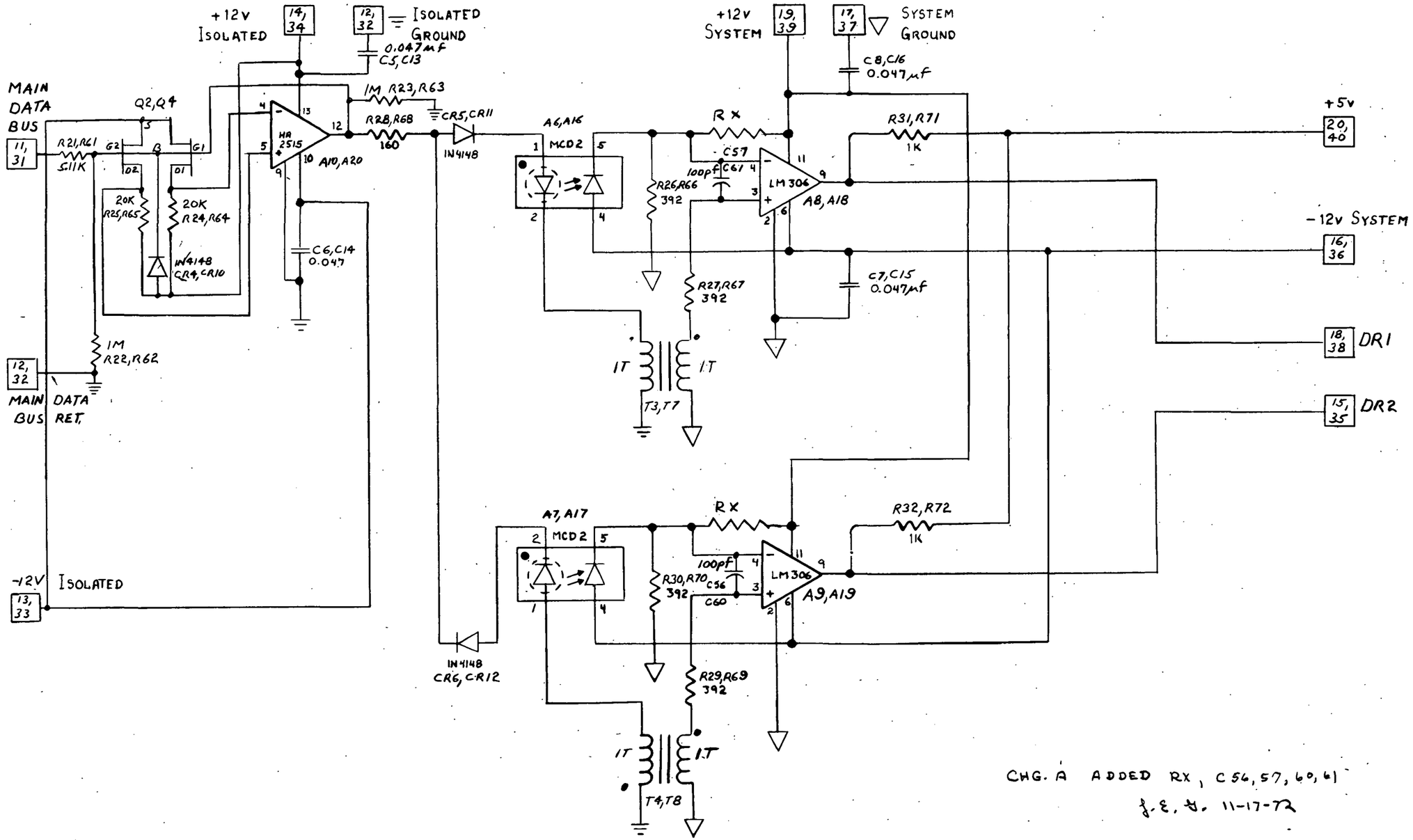
CHG. A CHANGED RB, RC8 TO 80Ω, REMOVED "NOT USED" NOTE FROM NEG SW OUTPUT. ADDED RX, C54, 55, 60, 61
f.e.u. 9/18/72

Supervisory Bus Receiver

SIZE	CODE IDENT NO.	
	04236	380-114
CHG A	SCALE	SHEET 3 of 7

PRINTED IN USA OZALID 888-838

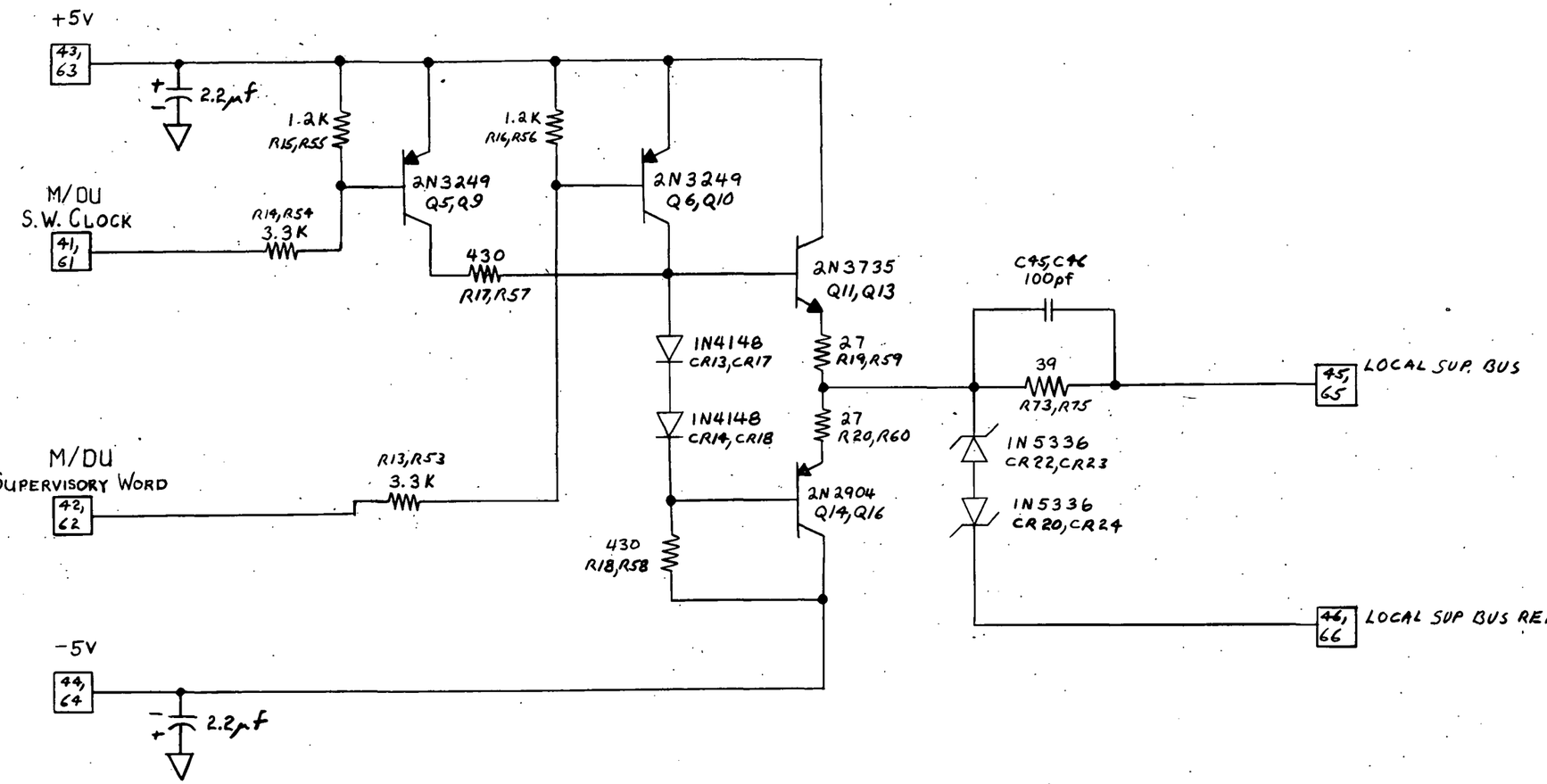
E-404D (2-62)



CHG. A ADDED RX, C54, 57, 60, 61
J.E.H. 11-17-72

Main Data Bus Line Receiver

CHG	SIZE	CODE IDENT NO.	
A		04236	380-114
	SCALE		SHEET 4 of 7



LOCAL SUPERVISORY BUS TRANSMITTER

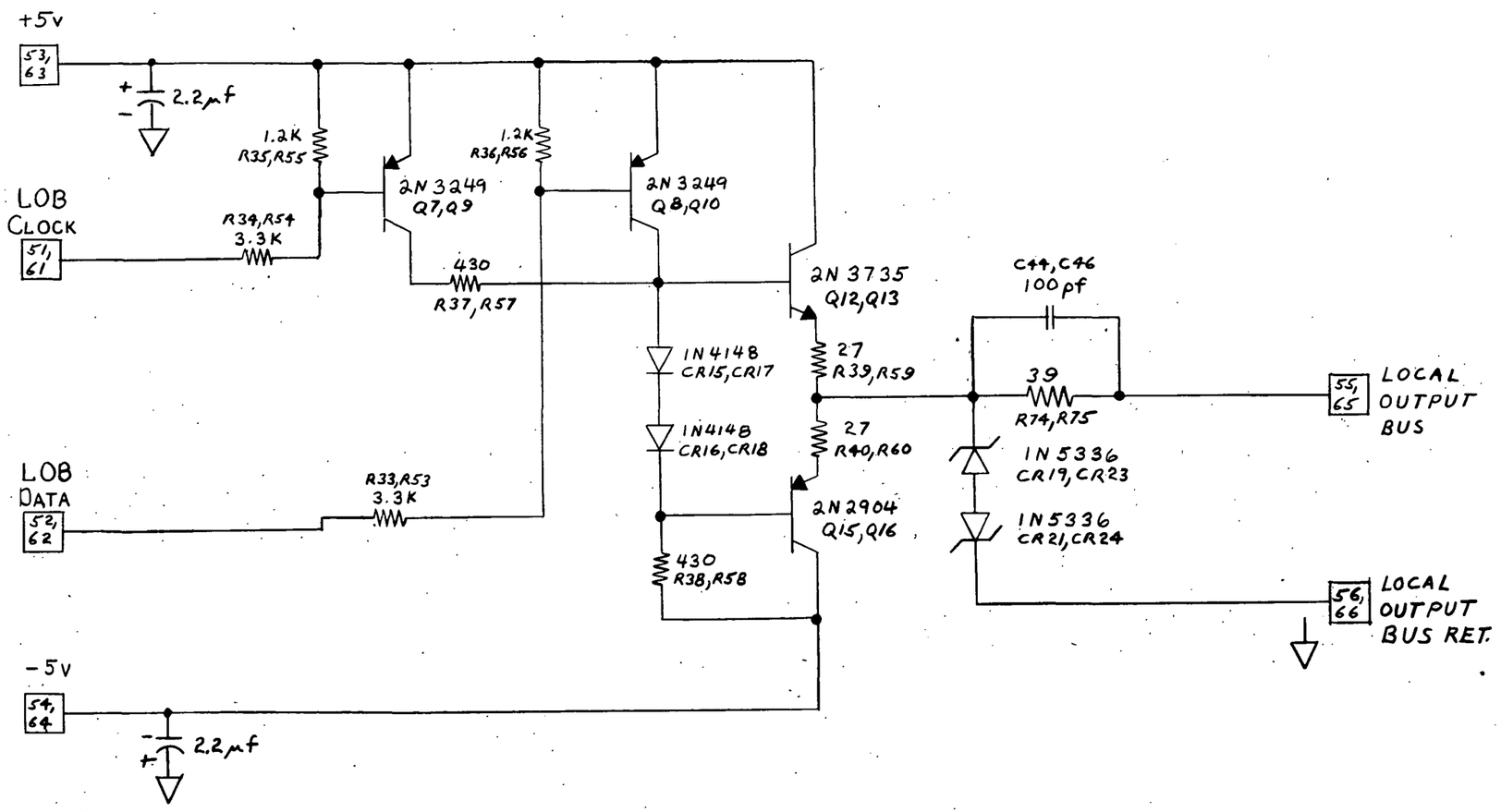
SIZE	CODE IDENT NO.	
	04236	380-114
CHG	SCALE	SHEET 5 of 7

PRINTED IN USA OZALID 888-838

E-404D(2-62)

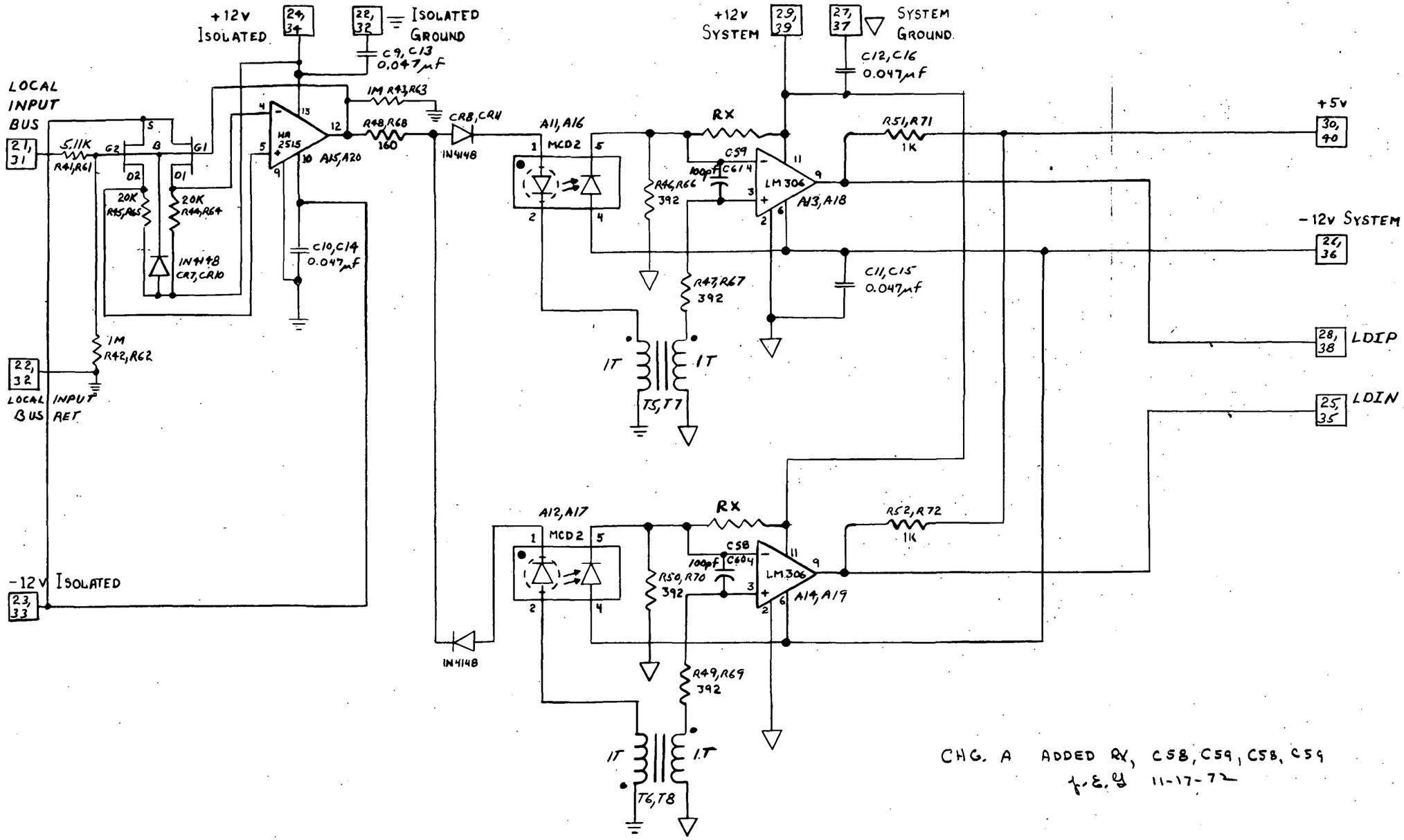
8 7 6 5

B A



LOCAL OUTPUT BUS TRANSMITTER

SIZE	CODE IDENT NO.	
	04236	380-114
CHG	SCALE	SHEET 6 of 7

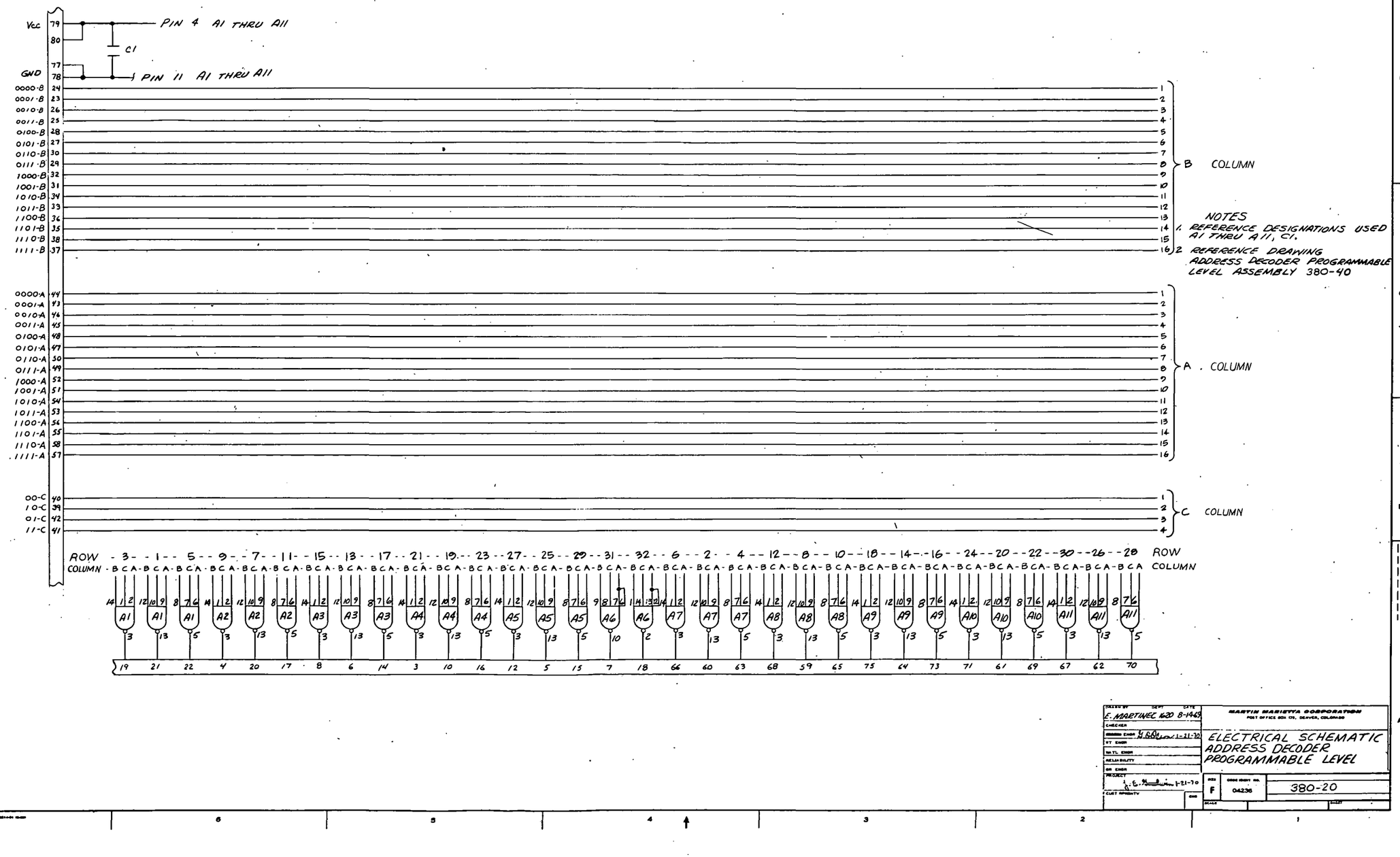


CHG. A ADDED RX, C58, C59, C58, C59
J.E.G 11-17-72

Local Data Bus Line Receiver

CHG	SIZE	CODE IDENT NO.	
A		04236	380-114
	SCALE		SHEET 7 of 7

REVISIONS				
ZONE	SYMBOL	DESCRIPTION	DATE	APPROVED

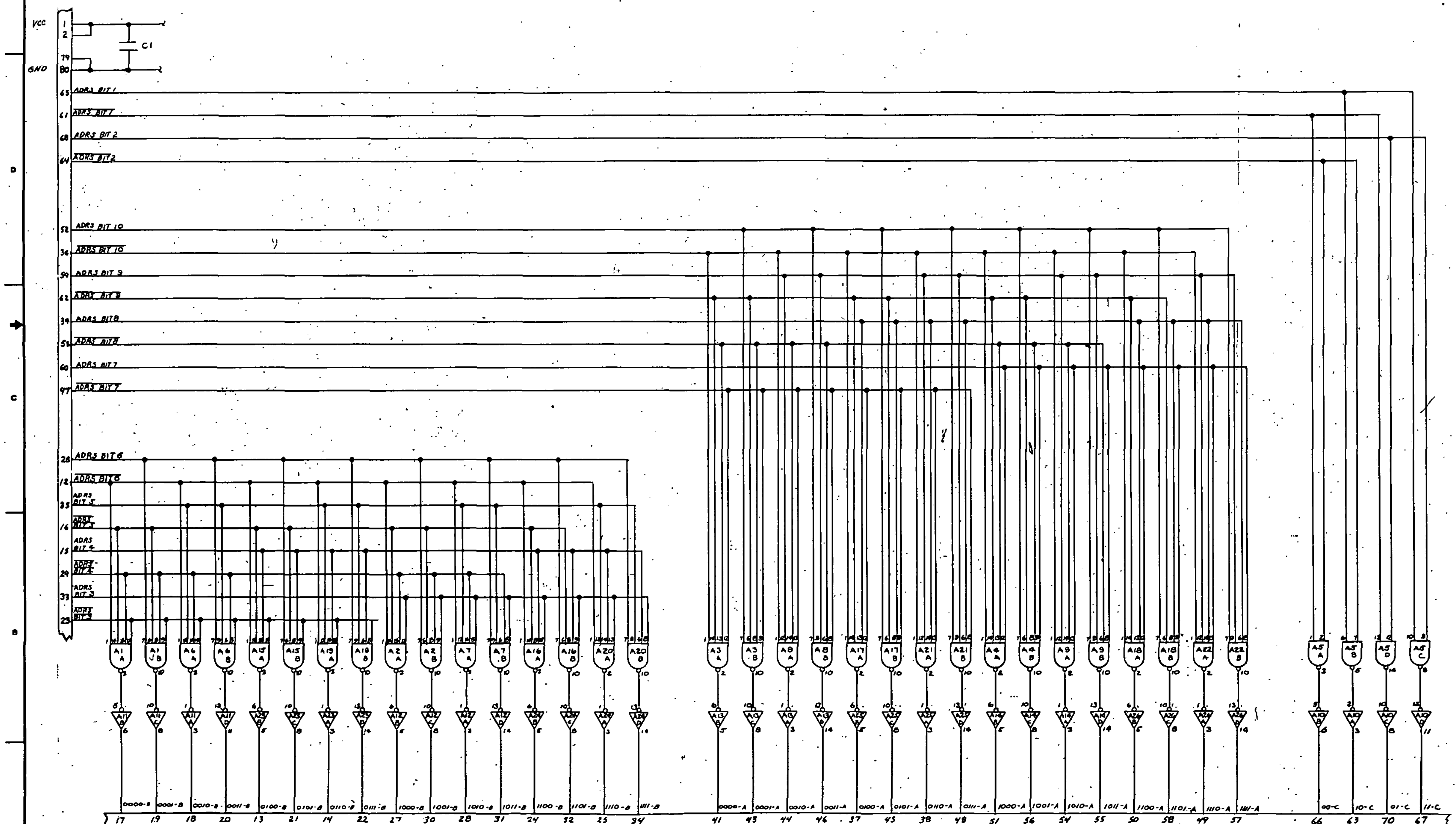


NOTES
1. REFERENCE DESIGNATIONS USED A1 THRU A11, C1.
2. REFERENCE DRAWING ADDRESS DECODER PROGRAMMABLE LEVEL ASSEMBLY 380-40

DRAWN BY E. MARTINEZ	DEPT 1620	DATE 8-1969	MARTIN MARIETTA CORPORATION, POST OFFICE BOX 179, DENVER, COLORADO
CHECKED			
ENGINEERING ENGR		1-21-70	ELECTRICAL SCHEMATIC ADDRESS DECODER PROGRAMMABLE LEVEL
QUALITY ENGR			
MFG'G. ENGR			
RELIABILITY			
QA ENGR			
PROJECT E. E. [illegible]		1-21-70	SIZE F, CODE IDENT NO. 04236, 380-20
CUST APPROVAL		DATE	SCALE

NOTES

1. REFERENCE DESIGNATIONS USED
   C1
   A1 - A26
2. REFERENCE DRAWING ASSEMBLY
   380-41
3. A1 - A26 PIN 11 TO GROUND
   A1 - A26 PIN 4 TO Vcc
   A10 - PINS 14, 1, 9, 12 TO Vcc
   A12, A13, A14, A23, A24, A25, A26 } PINS 2, 7, 9, 12 TO Vcc
   A 10, A11, PIN 7 TO GND
   A 11 PIN 2, 4, 9, 12, 14, TO VCC



ELECTRICAL SCHEMATIC
ADDRESS DECODER
FIRST LEVEL

E. MARTINEZ

1-21-70

E 04236 380-21

P5

ANALOG DATA H 8

ANALOG DATA L 10

BINARY DATA L1 22

BINARY DATA H1 30

BINARY DATA L2 26

BINARY DATA H2 28

P5

ANALOG DATA

4 ANALOG DATA

68 ANALOG GND

32 SAMPLE

64 CB1

62 CB2

24 +15 v

79 GND

80 GND

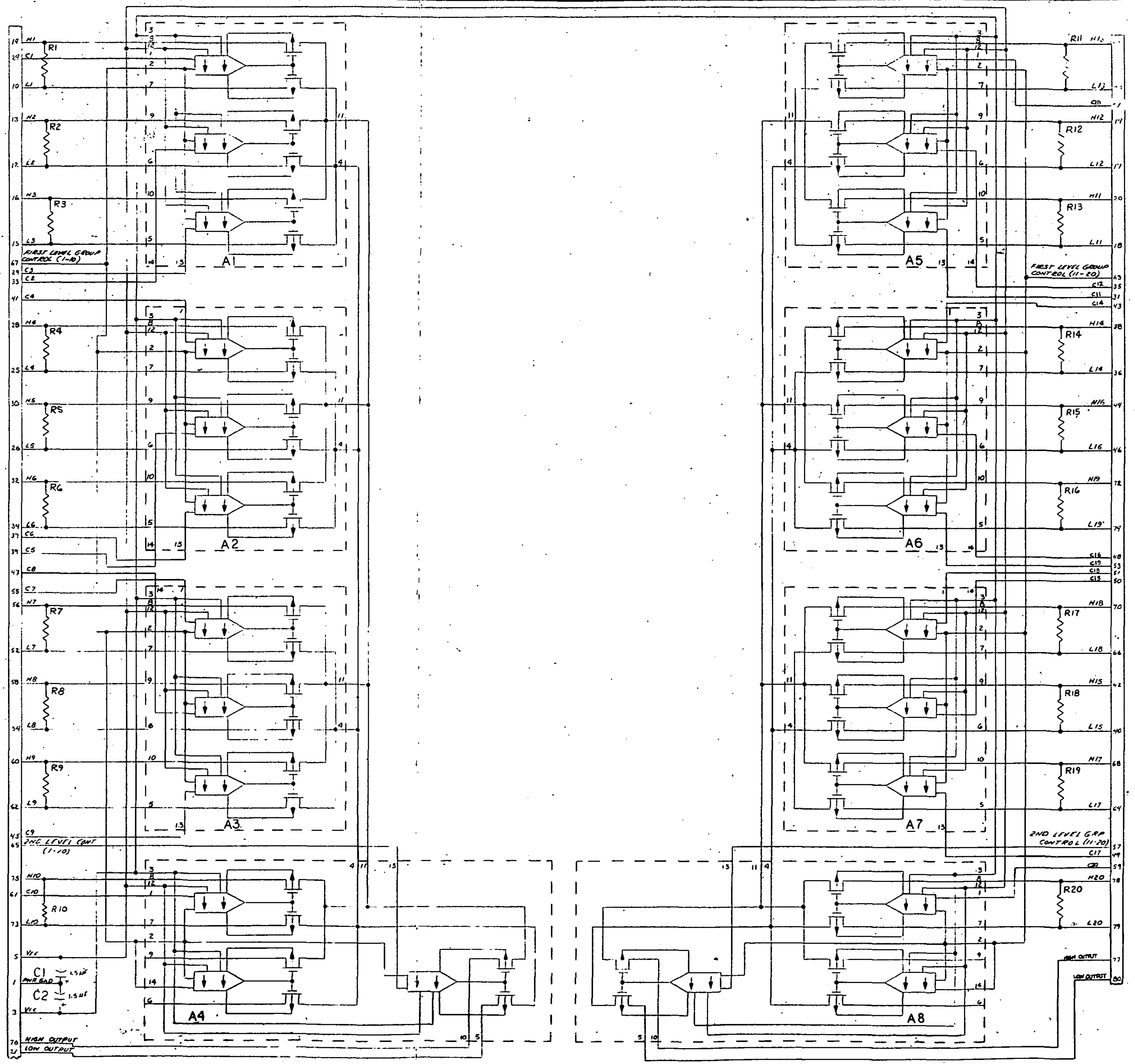
14 Vcc (+5 v)

46 -15 v

NOTE: UNLESS OTHERWISE SPECIFIED:
1) ALL RESISTOR VALUES ARE IN OHMS;
2) ALL CAPACITOR VALUES ARE μf;
3) ALL RESISTORS ARE MFSC EXCEPT 0.1%.

ELECTRICAL SCHEMATIC-
ANALOG/DIGITAL SIGNAL CONDITIONER

380-29



NOTES

1. REFERENCE DRAWINGS
   MULTIPLEXER ASSEMBLY 4100-22
   PRINTED WIRING BOARD 4100-32
   PRINTED WIRING MASTER 4100-52
2. REFERENCE DESIGNATIONS USED
   A1 THRU A8, C1 & C2, R1 THRU R20
3. A1 THRU A8 PART No. 50G210C
4. R THRU R20 ARE 10K, 0.1%.

ELECTRICAL SCHEMATIC
MULTIPLEXER

2-17-72

5-24-72

04236 | 380-28