OPTICAL MODULATOR SYSTEM

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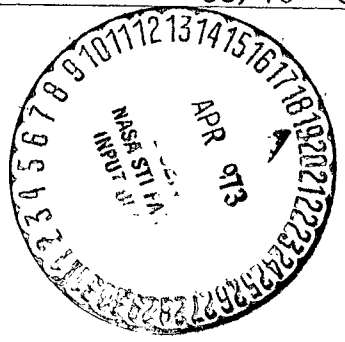
Final Report



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16. Abstract

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The signal processing electronics include encoding electronics which are capable of digitizing analog signals between the limit of ± 0.75 volts at a maximum rate of 80 megasamples per second with 5 bit resolution. The digital samples are serialized and made available as a 400 Mbps serial NRZ data source for the modulators. A pseudorandom (PN) generator is also included in the signal processing electronics. This data source generates PN sequences with lengths between 31 bits and 32,767 bits in a serial NRZ format at rates up to 400 Mbps.

The worst case dynamic extinction ratio of the 0.53 μm modulator was 15:1 with 72% transmission. The 1.06 μm modulator worst case extinction ratio was 13:1 with 50% transmission.

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OPTICAL MODULATOR SYSTEM

1. INTRODUCTION

The optical modulator system hardware which was fabricated, tested, and delivered under this program included a 0.53 μm modulator (Figure 1-1), a 1.06 μm modulator with power supply (Figure 1-2), and signal processing electronics with power supply (Figure 1-3). The electrooptic modulators function as high speed optical gates on the output of a 400 MHz mode locked Nd:YAG laser radiating at either 1.06 μm or 0.53 μm. The modulator units were designed to operate with digital signal sources with MECL logic levels. Each modulator unit contains the necessary amplifiers, thermal control, compensation circuits, and optics to provide stable, high quality optical gating. The signal processing electronics include encoding electronics which are capable of digitizing analog signals between the limits of $\pm$ 0.75 volts at a maximum rate of 80 megasamples per second with 5 bit resolution. The digital samples are serialized and made available as a 400 Mbps serial NRZ data source for the modulators. A pseudorandom (PN) generator is also included in the signal processing electronics. This data source generates PN sequences with lengths between 31 bits and 32,767 bits in a serial NRZ format at rates up to 400 Mbps.

This report contains a functional description, operating instructions, and performance test results for the above mentioned hardware.

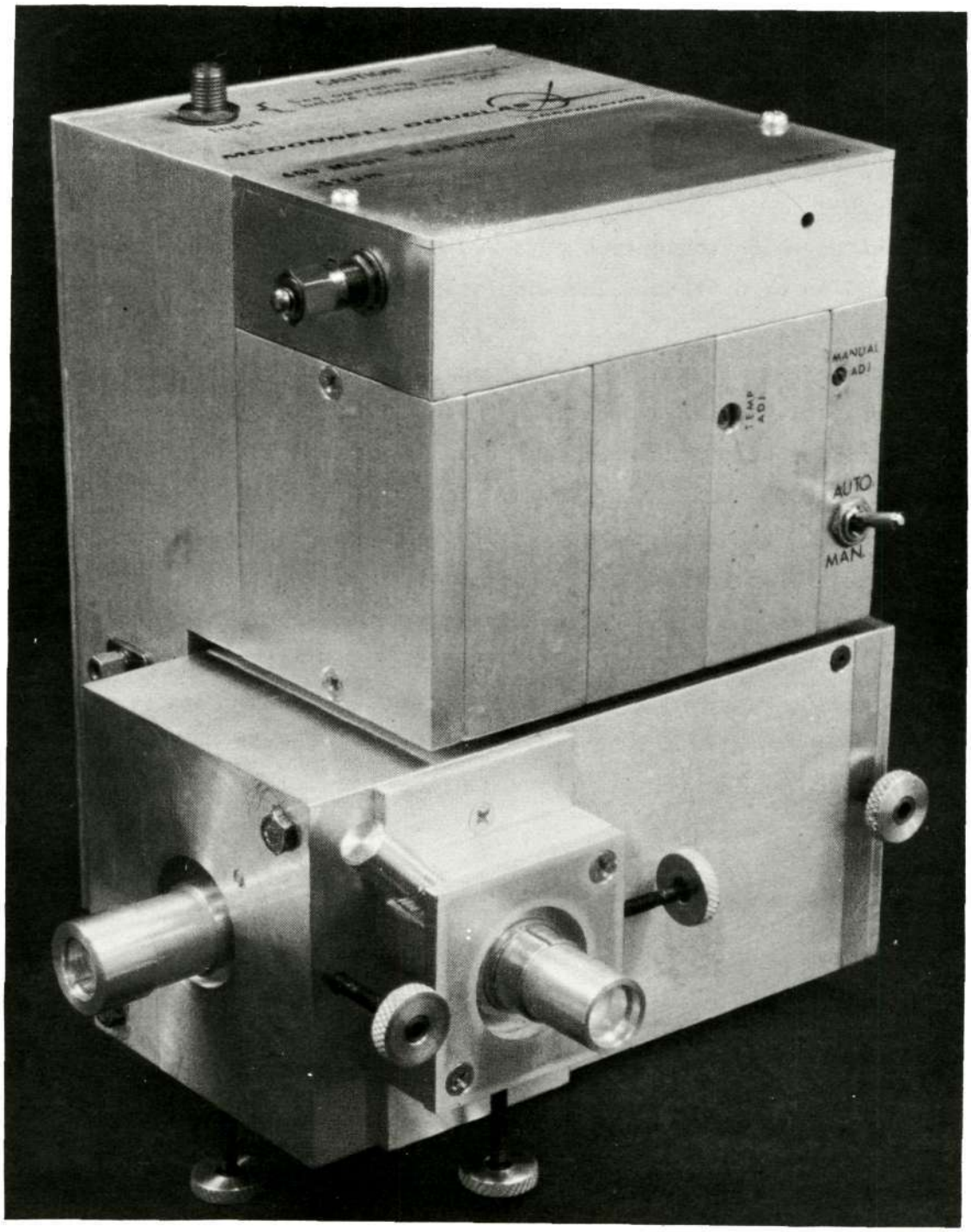


FIGURE 1–1 400 Mbps 0.53μM MODULATOR

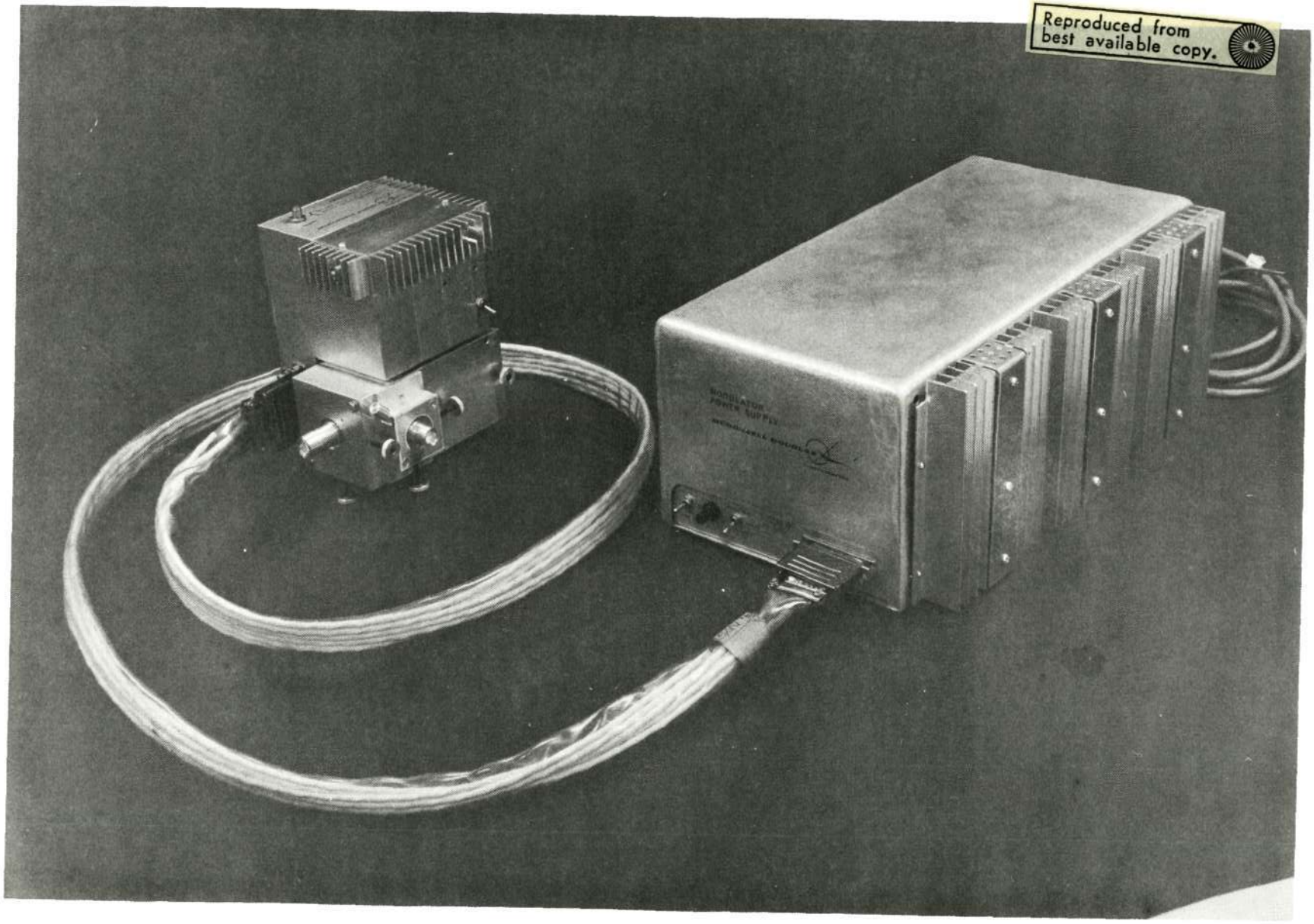


FIGURE 1–2 400 Mbps 1.06μM MODULATOR AND POWER SUPPLY

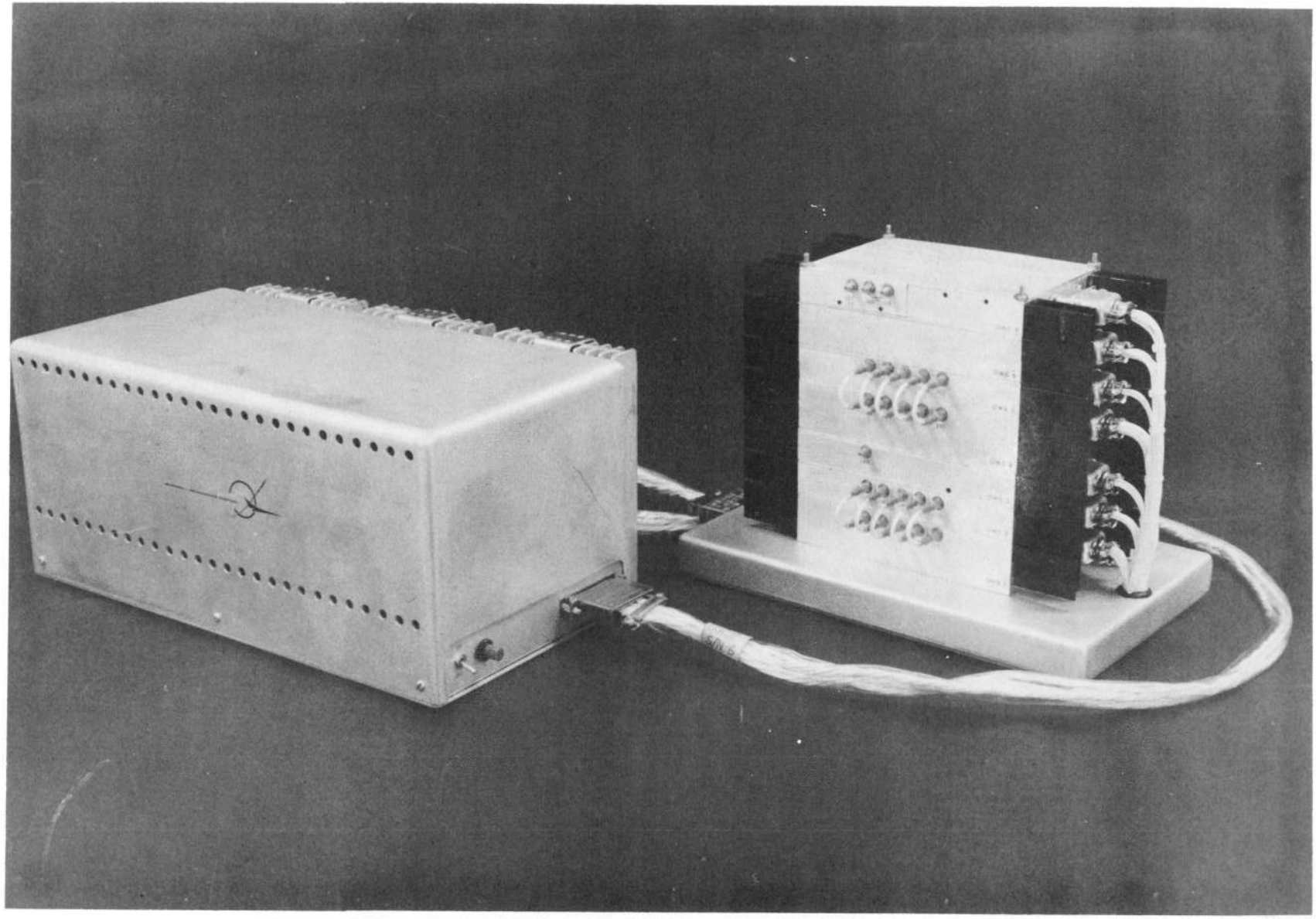


FIGURE 1–3 400 Mbps SIGNAL PROCESSING ELECTRONICS AND POWER SUPPLY

2. PERFORMANCE SUMMARY

The modulators delivered in this program are intended for incorporation in a mode-locked Nd:YAG laser communication system. The important interface parameters for the modulators in such an application are given in Table 1. Likewise, the interface specifications for the signal processing electronics which serve as a data source for the modulators are given in Table 2.

Table 3 summarizes the measurement results for critical modulator parameters. These results are typical of measurements made during various modulator tests at different times. The results vary depending on the care taken in optically aligning the modulators when they are set up for a test. More detailed test results are given in Section 5 of this report.

TABLE 1

400 Mbps LASER MODULATOR INTERFACE SPECIFICATIONS

Characteristic		Specification	
		0.53 μm Modulator	1.06 μm Modulator
Input Beam	Wavelength	0.53 μm	1.06 μm
	Average Power[1] (with compensator)	0.5 mW-10 mW	0.5 mW-10 mW
	Pulse Repetition Frequency	400 Mpps max.	400 Mpps max.
	Pulse Width (10% points)	500 ps max.	500 ps max.
	Beam Characteristics	Gaussian TEM_{oo}	Gaussian TEM_{oo}
	Beam Diameter	2mm nom.	2mm nom.
	Beam Divergence (1/e points)	0.3 mrad nom.	0.6 mrad nom.
	Polarization	Horizontal	Horizontal
Driver Input	Waveform	Bilevel, NRZ	Bilevel, NRZ
	Logical one level	-0.8V $\pm$ 0.1V	-0.8V $\pm$ 0.1V
	Logical zero level	-1.7V $\pm$ 0.1V	-1.7V $\pm$ 0.1V
	Input Impedance (nominal)	50 ohm	50 ohm
	Reflection coefficient (with 1ns risetime)	$\leq$ 0.2	$\leq$ 0.2
	Rise, Fall times (10-90%)	$\leq$ 1.3 ns	$\leq$1.3 ns
	Data Jitter, Symmetry with respect to data clock	$\leq \pm$ 100 ps	$\leq \pm$ 100 ps
Output Beam	Beam Characteristics	Gaussian TEM_{oo}	Gaussian TEM_{oo}
	Beam Diameter	2mm nom.	2mm nom.
	Divergence	0.3 mrad nom.	0.6 mrad nom.
	Polarization	Horizontal	Horizontal

NOTE:

1. Will operate with power levels exceeding this range when used with the manual compensator.

TABLE 2

SIGNAL PROCESSING ELECTRONICS INTERFACE SPECIFICATIONS

	Characteristic	Specification
PN Generator Clock Input	Waveform	Sinusoidal
	Frequency[1]	400 MHz ±5 MHz
	Amplitude	1V pp
	Load Impedance	50 ohms nominal
Data Output	Waveform	Bilevel, Serial NRZ
	Frequency	Same as Clock Input Frequency
	Logical one level	-0.8V ±0.1V
	Logical zero level	-1.7V ±0.1V
	Rise, Fall time (10-90%)	≤ 1.3 ns
	Jitter Symmetry with respect to Clock	≤ ±100 ps
	Load Impedance	50 ohm nominal
Encoding Electronics Clock Input	Waveform	Sinusoidal
	Frequency	10-400 MHz
	Amplitude	3V pp
	Load Impedance	50 ohms nominal
Analog Input	Amplitude	≤ ±0.75V pp
	Bandwidth[2]	dc - 32 MHz
	Load Impedance	50 ohms nominal
Data Output	Waveform	Bilevel
	Frequency	Same as Clock input
	Logical one level	-0.8V ±0.1V
	Logical zero level	-1.7V ±0.1V
	Rise, Fall time (10-90%)	≤ 1.3 ns
	Jitter, Symmetry with respect to Clock	≤ 100 ps
	Load Impedance	50 ohms nominal

NOTES:

1. Cables are also furnished to allow operation at 200 MHz and 300 MHz with a 63 bit sequence. The generator can be made to operate at any frequency below 400 MHz if the proper cable lengths are used.

2. The analog signal bandwidth should be at least 2.5 times less than the sampling rate.

TABLE 3

400 Mbps LASER MODULATOR PERFORMANCE SUMMARY

Characteristic	0.53 μm Modulator	1.06 μm Modulator
Transmission	72%	50%
Depth of Modulation	>98%	>97%
Extinction Ratio		
Static	>50:1	>30:1
Dynamic	>15:1	>13:1
Power Dissipation	22 watts	30 watts

Definitions:

1) $\text{Transmission} = \frac{P_{\text{in ave.}} - P_{\text{out ave.}}}{P_{\text{in ave.}}} \times 100$

2) $\text{Depth of Modulation} = \frac{\text{Maxium 1 level-Minimum 0 level}}{\text{Maximum 1 level}} \times 100 = (1 - \frac{1}{\text{Static Ext. Ratio}}) \times 100$

3) $\text{Static Extinction Ratio} = \frac{P_{\text{out ave. (all 1's)}}}{P_{\text{out ave. (all 0's)}}}$

4) $\text{Dynamic Extinction Ratio} = \frac{\text{Minimum 1 level in optical pulse train}}{\text{Maximum 0 level in optical pulse train}}$

Dynamic extinction ratio is measured using a 63 bit pseudorandom code as a data source

NOTES:

1. Optical alignment of the modulators are critical when attempting to measure the above performance parameters.
2. Measurement of dynamic extinction ratio is limited by the ability to discern 0 levels down in the detector and oscilloscope noise levels.

3. HARDWARE DESCRIPTION

3.1 0.53 μm MODULATOR.

A photograph of the 0.53 μm modulator is shown on Figure 3-1 and a functional diagram of the unit is given of Figure 3-2. The 0.53 μm modulator consists of a 0.53 μm modulator subassembly, modulator driver, temperature controller, automatic electronic compensator, manual compensator, and chassis. The chassis contains the wideband 50 ohm loads, power connector, and all the power and signal cables to the various modules. The dimensions of the 0.53 μm modulator are 10.35 cm x 12.5 cm x 14.0 cm. It weighs 1.7 kilograms and dissipates 22 watts average.

The horizontally polarized, mode locked laser beam enters the modulator through the transparent half of a window as shown in Figure 3-3. It then passes through two cascaded crystals whose longitudinal axes are parallel to the light beam. The beam is then reflected from a mirror at the exit from the second crystal, such that it passes in the return direction again through both crystals. If the crystals are energized during the period that a pulse passes through, the pulse polarization is rotated by 90°. If the crystals are not energized, the polarization of a given pulse remains unchanged. After leaving the crystals, the beam is reflected by a second mirror to a polarized beam splitter. Here, the beam is split into two: 1) a modulated, horizontally polarized output beam, and 2) a modulated, vertically polarized beam which is detected by the compensator diode and used as the correction signal for the automatic compensator.

3.1.1 Modulator Subassembly

The modulator subassembly consists of the optics head, oven subassembly, and lens holders.

Figure 3-4 shows an exploded view of the oven subassembly. The oven is used for mechanical support and as an isothermal enclosure which thermally stabilizes the modulator interior with respect to the laboratory environment. The matching network cables, heater leads, and thermistor leads enter the oven through the base of the housing which acts as a ground plane for the high frequency signals. The unshielded leads are bypassed with feedthrough capacitors to this ground plane which prevents pickup of the several watts of circulating RF power from entering the control loop of the temperature controller. The oven core is held in place by the teflon end bells.

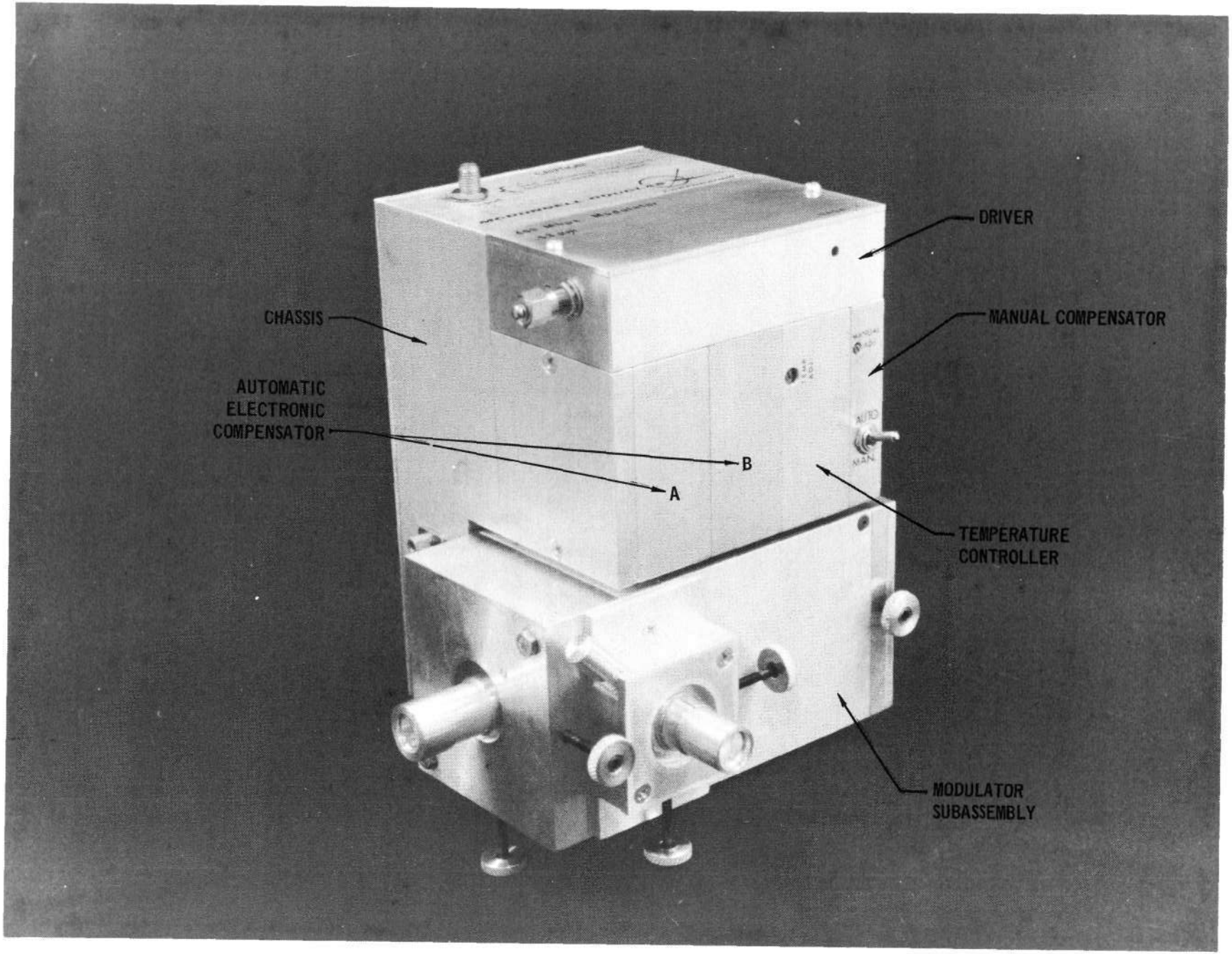


FIGURE 3–1 400 Mbps 0.53 μM MODULATOR

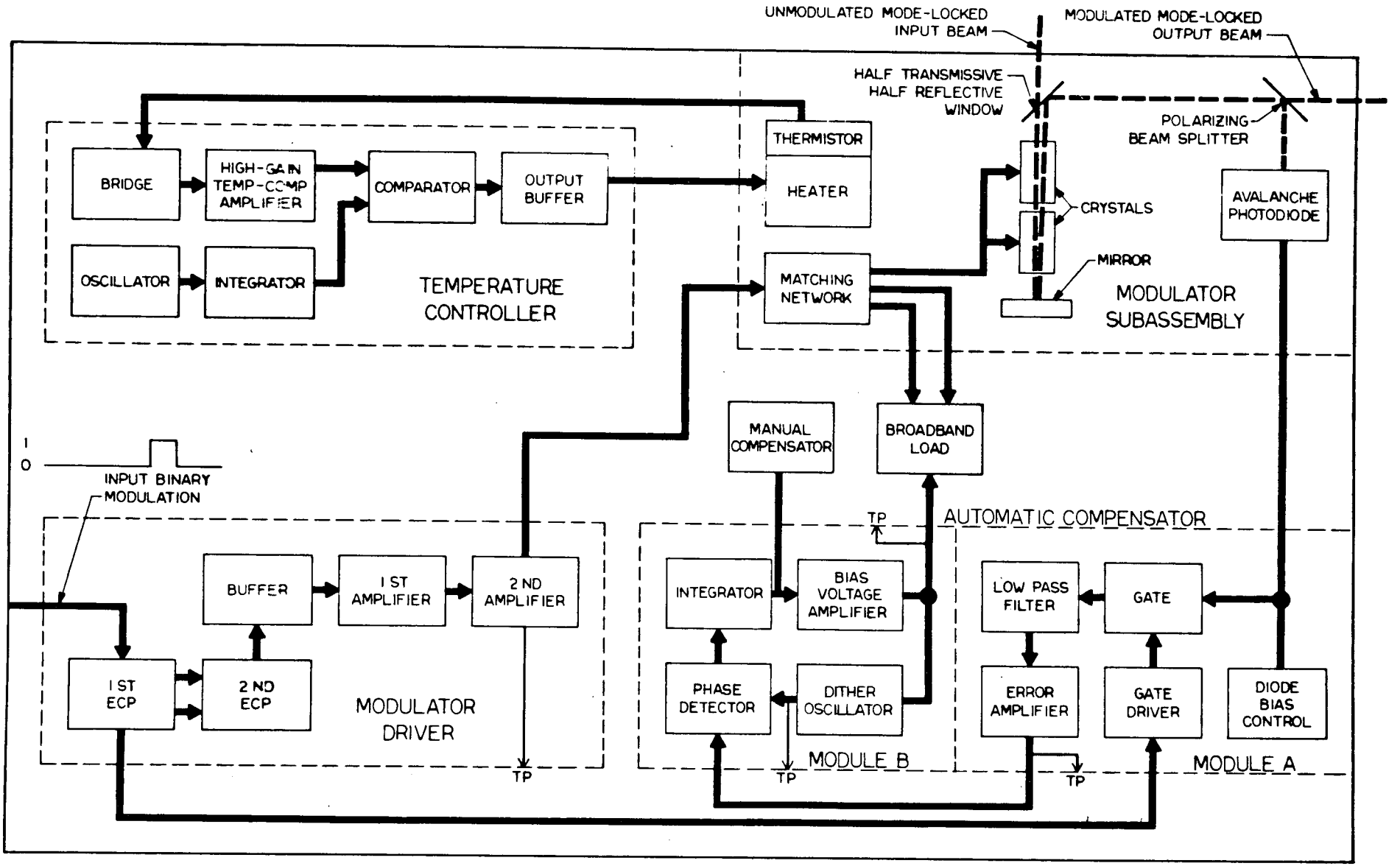


FIGURE 3–2 LASER MODULATOR FUNCTIONAL BLOCK DIAGRAM

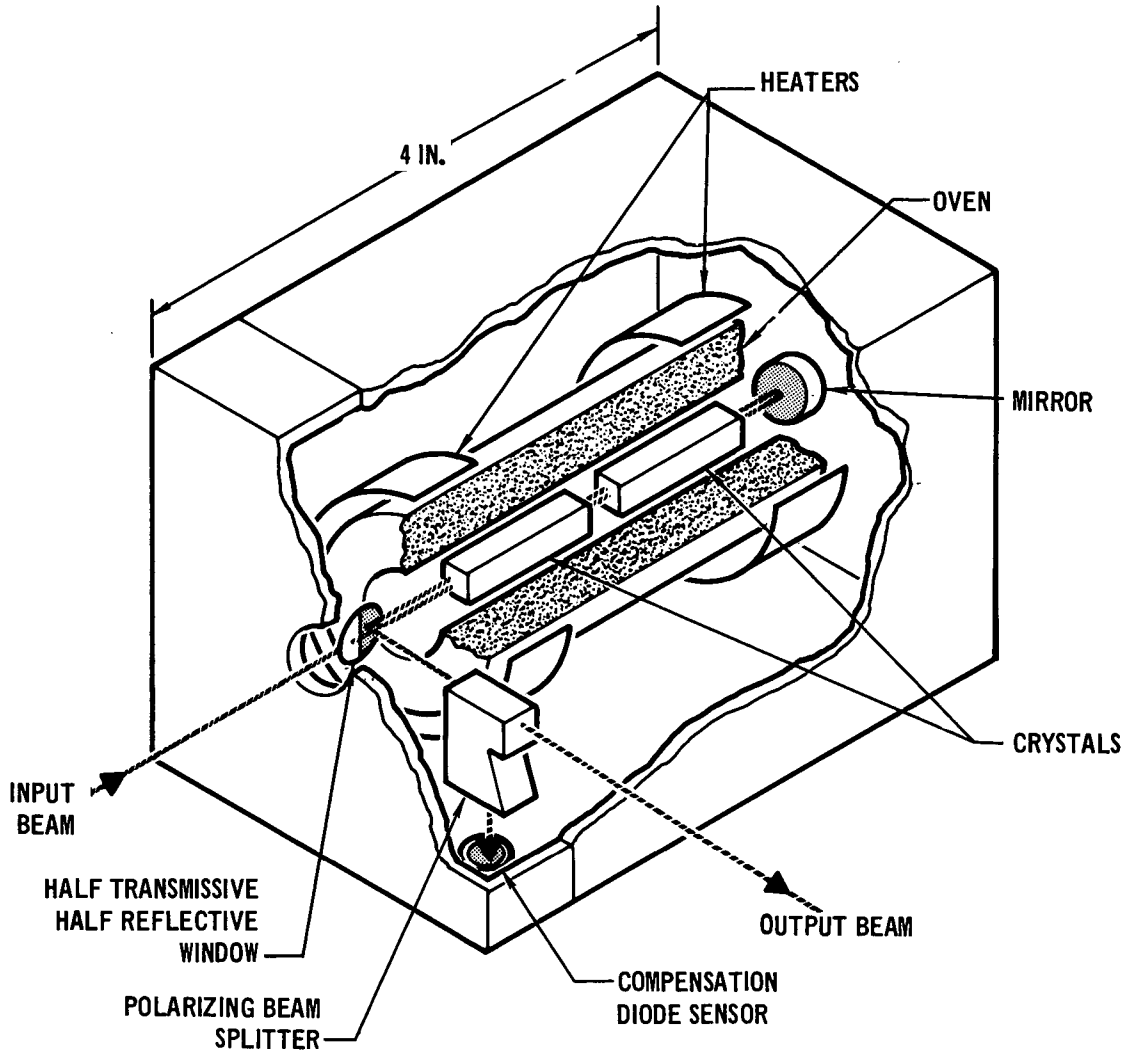


FIGURE 3-3 MODULATOR SUBASSEMBLY CUTAWAY

These end bells are shaped for maximum support of the oven core and also provide a minimal heat leak from the oven core to the oven housing. The end bells are made of teflon to minimize the reactive interaction with the matching network components.

The oven core is made of boron nitride. Boron nitride was chosen for its low dielectric loss tangent and high thermal conductivity. Only beryllium oxide would be better in this respect, but it is extremely difficult to machine and handle beryllium oxide because of its very toxic nature. The oven core holds the mounted crystals and heaters. It acts as the high temperature isothermal enclosure. The ends of the oven core are shaped to hold the heaters. The nichrome wire heaters are wound in grooves in

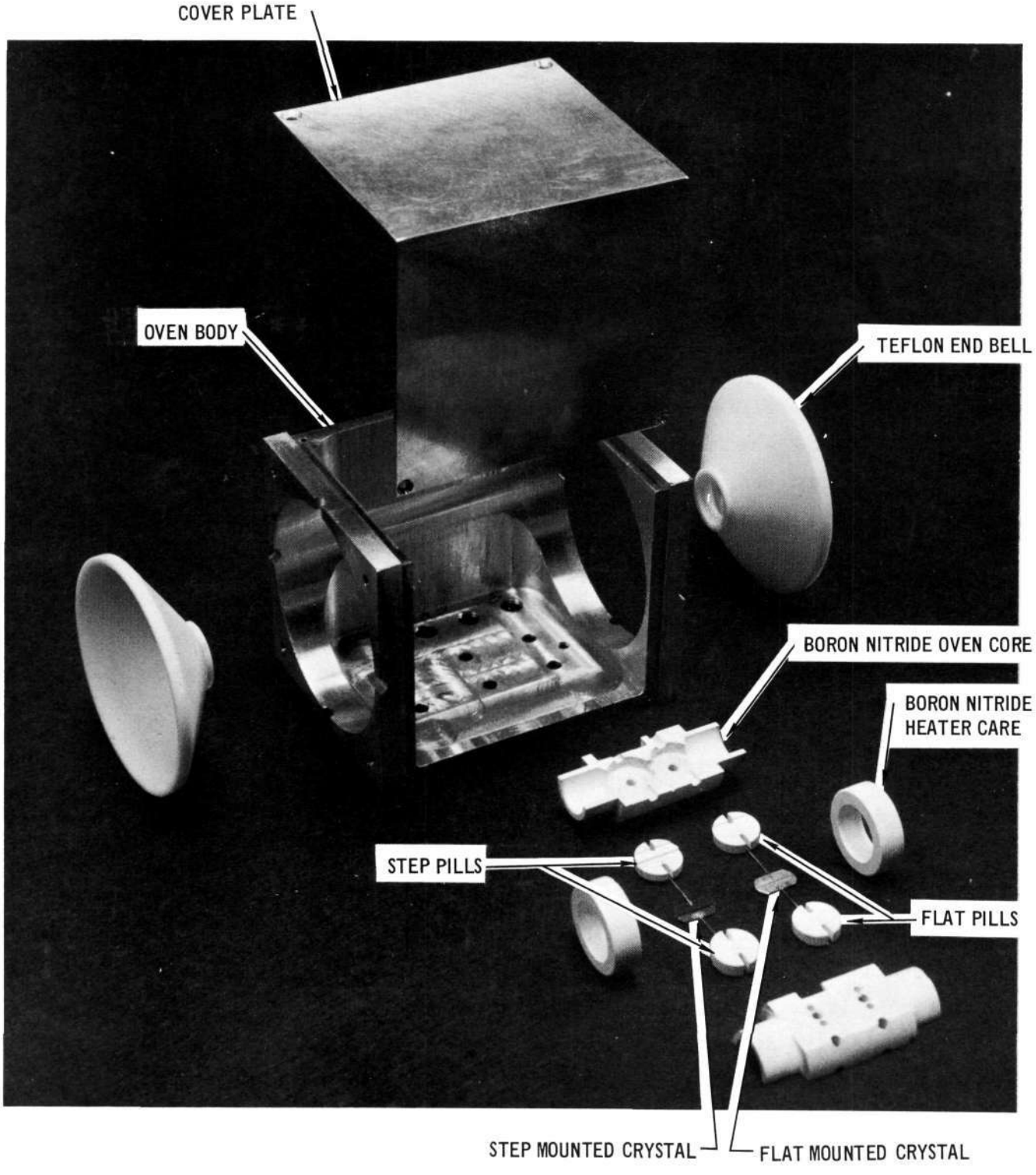


FIGURE 3–4 MODULATOR OVEN SUBASSEMBLY

boron nitride cylinders which fit snugly around the oven core. The length of the groove in the cylinders was chosen so that about 22 ohms of nichrome wire are used. This impedance was chosen to match the temperature controller output stage. The heaters were located away from the oven center so that there is as little electrical interaction as possible between the heaters and matching network.

The crystals are soldered to copper electrodes. One crystal is a flat configuration where the electrode comes in from the side. It mounts between two flat boron nitride pills. The other crystal is placed between two similar electrodes, one above and one below the crystal. The boron nitride pills used for mounting this crystal have a step of height equal to the crystal and electrode thickness. The pills are bonded to the electrodes with an RTV cement. The pills are then optically aligned in the oven core and bonded in place in the same manner.

An exploded view of the optics head is shown in Figure 3-5. The body of the optics head is shaped to hold the component parts. Its back side is shaped to fit into the oven body to hold the teflon end bell in place. The beam splitter mirror holder fits into the optics head body from the back side; it slides between the body and a metal backup plate. Adjustment is accomplished by turning the two screws which push rods against the shoulders in the mirror holder. Back pressure is applied by the spring loaded plunger pressing against the cylindrical part of the mirror holder. The two screws which hold the plates together can be tightened for locking the mirror holder in place. The mirror is held in the mirror holder between two press fit 45° rings. The polarizing beam splitter prism sits in a recess in the optics head body. Its center aligns with the center of the beam splitter mirror. It is held in place by spring pressure from the metal retainer. The compensator diode is held in place beneath the polarizing beamsplitter by a plastic holder. The plastic holder is adjustable to position the diode in the compensator output beam by sliding it into place and clamping the holder by tightening the two screws which hold the diode holder. The output cable from the diode exits through the large hole in the left of the optics head body.

An exploded view of the front lens holder is shown on the right hand side of Figure 3-5. The adjustment motion is produced by a sliding

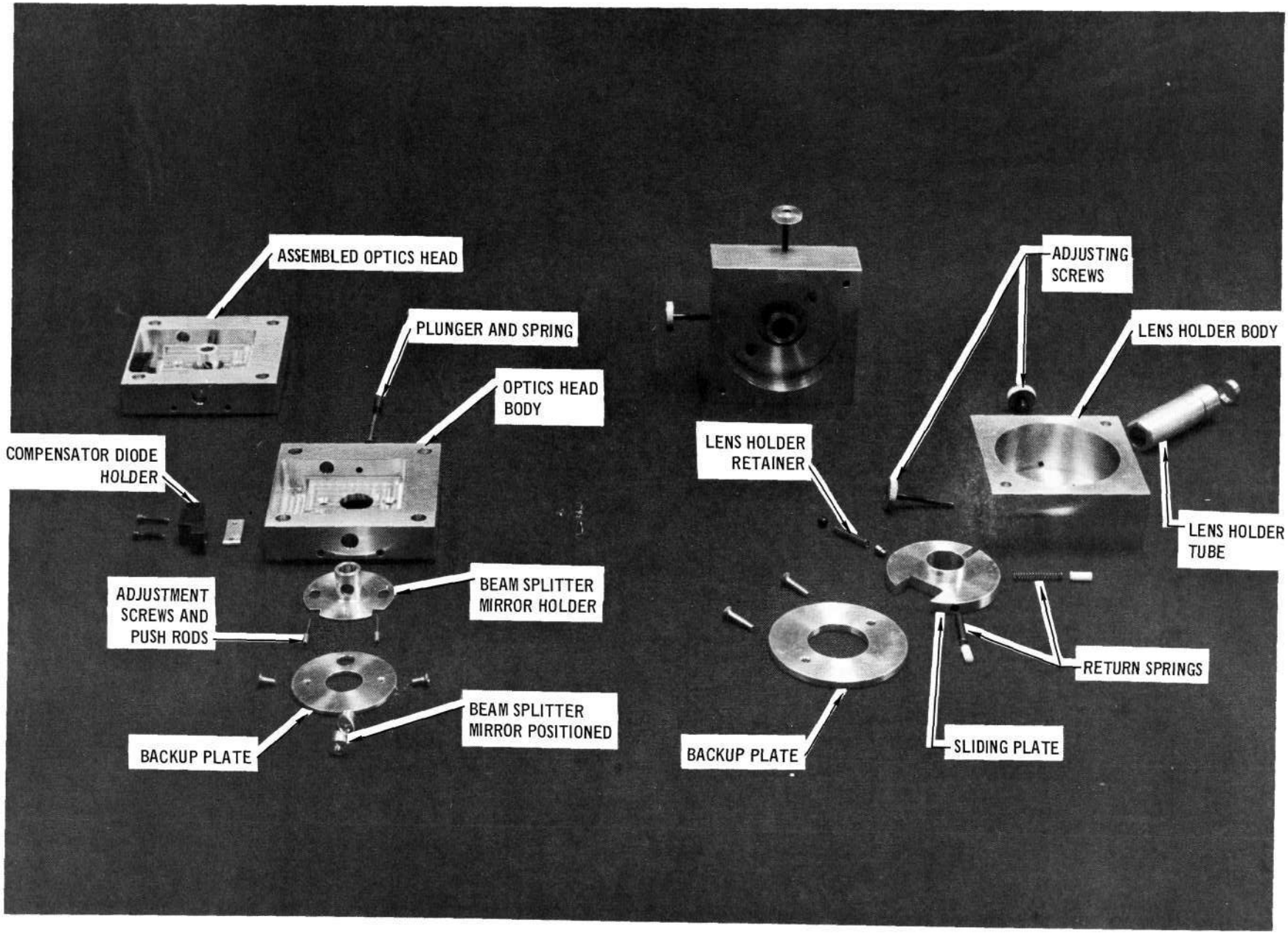


FIGURE 3–5 MODULATOR OPTICS HEAD AND LENS HOLDER

plate, as in the optics head. The difference here is that only X and Y degrees of freedom are required while restricting rotation. The horizontal adjustment is accomplished by a screw on one side of the sliding plate with a spring on the other side opposing it. The vertical adjustment works in a similar manner. The lens is held in a cylinder which is a close slip fit into the sliding plate with a spring loaded retainer. The lens can be pushed in and out for focusing adjustments.

An exploded view of the rear mirror holder is shown in Figure 3-6. The rear mirror holder is quite similar in design and function to the front lens holder. Its stability of position is more critical, however, because of the short focal length of the rear mirror. This requires spring loading of the sliding plate in all three directions. The helical spring holds the sliding plate against the rear mirror holder body. The rear mirror holder body has the same kind of shoulder as the optics head for holding the teflon end bell in place in the oven body. The mirror is mounted in the stainless steel post which extends into the oven interior for proper location of the rear mirror.

3.1.1.1 Crystal Material Selection

Each of the modulators delivered under this program use two high quality lithium tantalate crystals. Prior to this program, we had conducted a trade analysis of the available electrooptic crystals which might be useful for 400 Mbps modulation. At that time, based on the best data available, we concluded that strontium barium niobate, SBN ($Sr_{05}Ba_{0.5}Nb_2O_6$) was the best crystal choice for this application. This decision was based upon its availability in good quality specimens, low half wave voltage, acceptable crystal capacitance, and immunity to optical damage at 0.53 μm. We knew that the dielectric loss tangent was a few percent and the piezoelectric coupling was quite high. At the time, however, we considered SBN to be the best available material for use in this program.

During the course of this program we also conducted an extensive modulator materials evaluation study (under Air Force contract F33615-71-C-1909) of the current and readily achievable optical quality of several candidate modulator materials. The material that emerged from that study, and the study conducted under this program, as the choice for high data rate space data relay applications was lithium tantalate. This decision was partly

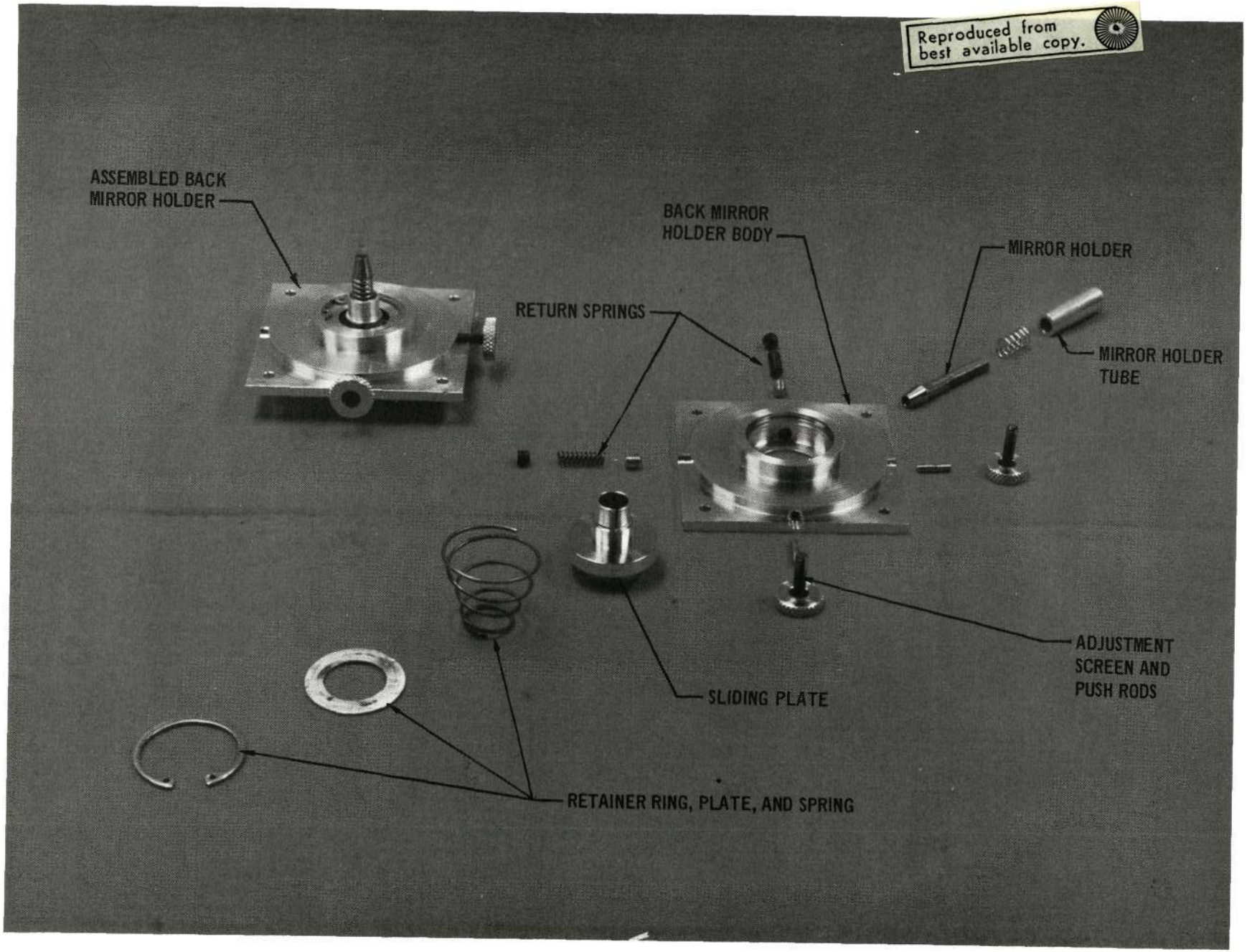


FIGURE 3–6 MODULATOR REAR MIRROR HOLDER

based upon the fact that we were never able to completely suppress the piezoelectric body resonance in the SBN modulators. Intersymbol interference always occurred when modulation codes containing low frequency components were used. The decision was also influenced by the increased availability of lithium tantalate during the course of this program. In fact, we were able to obtain usable samples of lithium tantalate from four separate sources, although only one source produces exceptionally good material.

The decision to use lithium tantalate was made early enough in the program that we were able to accomplish most of the program goals. The use of lithium tantalate required increasing the oven temperature from a nominal 50°C to 150°C for prevention of optical damage, with a corresponding increase in heater power. The increased switching voltage required more driver power than we had originally budgeted.

3.1.1.2 Crystal Configuration

The lithium tantalate crystals are oriented so that the polarized laser light travels through the crystals in a direction parallel to the "C" faces. The light enters the crystals polarized at 45° with respect to the crystal axes. In this configuration, the input beam is divided equally into the two polarizations within the crystal, i.e., ordinary (O-wave) and extraordinary (E-wave). The two crystals are oriented so that their axes are crossed as shown in Figure 3-7. The light which travels as O-wave light in the first crystal will travel as E-wave light in the second crystal. Similarly, light which travels as E-wave light in the first crystal will travel as O-wave light in the second crystal. One can see that, when the two crystals are identical in length as they are when cut from a single piece of material, the total optical length traversed by each polarization is identical, provided that each crystal is at the same temperature. This provides above two orders of magnitude of cancellation of thermal effects in a single crystal. Therefore, the control range required by the automatic electronic compensator and the accuracy of control required by the temperature controllers are greatly reduced.

The phase retardation induced by placing a voltage across the "C" faces is a field distance product. The crystals are therefore made as long and thin as practical so that the field distance product required to achieve half-wave switching is minimized. A factor of two is gained by operating

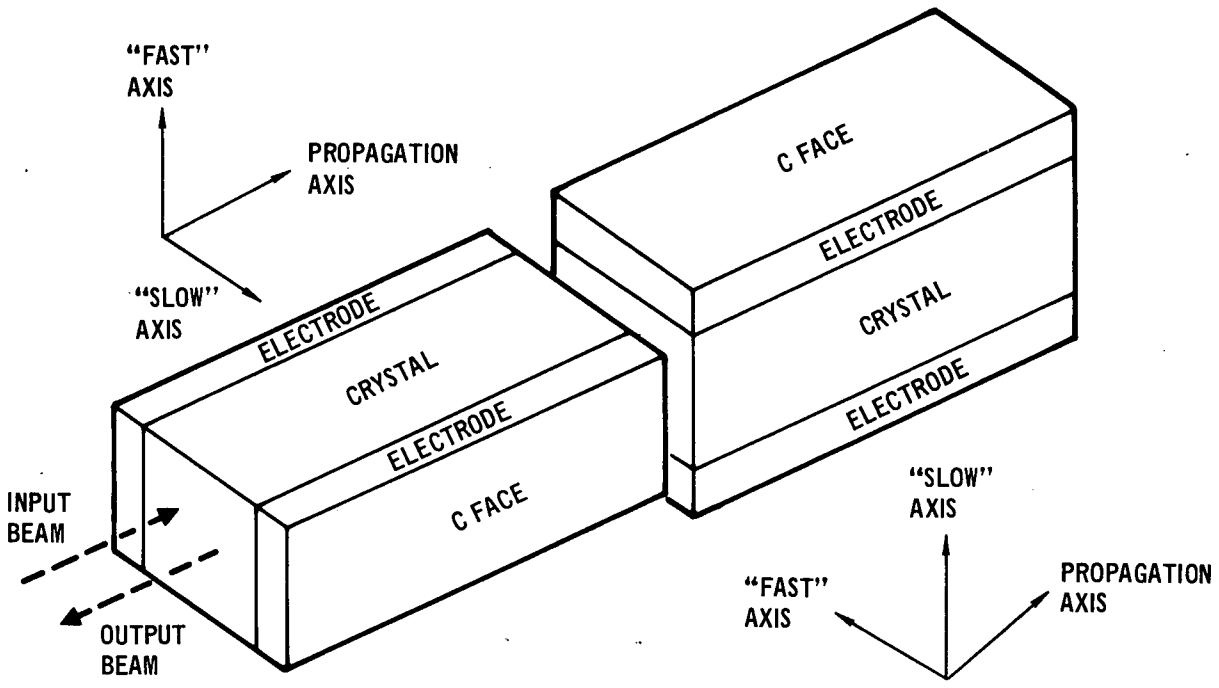


FIGURE 3-7 CROSSED AXES CRYSTAL MOUNTING ARRANGEMENT

the modulator in the double pass configuration so that the light passes through the crystals twice. The optimum size of the crystals for minimizing driver power in the 0.53 μm unit is 0.3mm aperture with each crystal being 10mm long. The aperture was increased to 0.4mm to increase the extinction ratio because we were not able to eliminate the surface strain in the crystals. The crystal capacitance and rise time was not affected by this change but the switching voltage was increased to about 22 volts.

3.1.2 Modulator Driver.

The Modulator Driver (Figure 3-2) amplifies the signal from the digital data source to drive the modulator crystals. The driver input and output signal characteristics are defined in Table 4.

The input section is made up of two emitter-coupled-pairs (ECP) which operate in the switching mode to isolate the driver output from noise and amplitude variation on the input signal. The first stage has an output which is used to gate the automatic electronic compensator. The second stage provides some power gain. The output of the second stage is buffered, and drives a two stage wideband output amplifier which drives the 50 ohm matched modulator load.

TABLE 4

MODULATOR DRIVE INPUT CHARACTERISTICS

Load Impedance	50 ohm nominal
Reflection Coefficient	<0.2
Logical Zero Input Level	-1.7 ±0.1 Vdc
Logical One Input Level	-0.8 ±0.1 Vdc
Rise & Fall Time	<1.0 ns

MODULATOR DRIVER OUTPUT CHARACTERISTICS

	0.53 μm	1.06 μm
Logical Zero Output Level	+30.0 ±2.2 Vdc	+40.0 ±3.0 Vdc
Logical One Output Level	+8.0 ±2.2 Vdc	+10.0 ±3.0 Vdc
Rise & Fall Times	<0.7 ns	<1.0 ns
Load Impedance	50 ohms nominal	50 ohms nominal

The 0.53 μm driver is completely dc coupled. Under normal operating conditions (50% duty cycle) it furnishes 4.8 watts to the matched load while dissipating 6.2 watts internally.

3.1.3 Temperature Controller.

The Temperature Controller (Figure 3-2) provides slow-response, long-term temperature control of the modulator crystals. Crystal temperature is controlled at 150° ± 1°C by heaters that are supplied with electrical power from the Temperature Controller.

A temperature sensing thermistor is inserted into one leg of a bridge, and resistors are used in the other legs. The thermistor has a temperature coefficient of approximately 1% per degree Centigrade, and has a nominal impedance of 200 ohms at 150° Centigrade. The resistors are selected so that the bridge output is nulled at the desired operating temperature. Any

error in the bridge null is amplified by the high-gain temperature controlled amplifier and is used as a bias voltage for the comparator. A triangular waveform (the integrated square-wave-oscillator output) that has an average value of zero is used as the second signal to the comparator. The comparator switches on and off as the triangular waveform changes above and below the bias voltage developed from the bridge. Thus, the bridge controls the on-off ratio or duty cycle of the voltage applied to the heater. The output buffer switches the required amount of power to the heater.

3.1.4 Automatic Electronic Compensator.

The function of the Automatic Electronic Compensator (Figure 3-2) is to compensate for thermal effects not compensated by the crossed axis crystals and to compensate for any dc bias level applied by the driver amplifier. Compensation is provided by adjustment of the dc bias that is applied to the crystals. A dither control system is used to automatically adjust the dc bias to maintain the electrooptic modulator at maximum extinction ratio.

The light rejected by the polarizing beam splitter is the complement of the light transmitted. The amplitude of the rejected zeros is maximum at the time when the transmitted zeros are minimum. This rejected light is monitored while a low amplitude dither signal is applied to the modulator bias. The The amplitude and phase of the recovered dither signal is used as an error signal to provide bias amplitude and polarity information for optimum operation.

An avalanche photodiode is used to monitor the rejected light. Diode bias voltage adjustment and current limiting are provided in Module "A". The detected light pulses pass through a gate which is synchronized with the modulator driver binary signal. The gate drive signal is delayed so that it coincides with the time of arrival of the detected signal at the gate. The gate is turned on for the rejected pulses and off for the transmitted pulses. The filter recovers the dither signal from the rejected pulses. The error amplifier increases the signal to the required level and automatically adjusts for a wide range of input signals via its AGC circuits. The amplified error signal is then compared with the phase of the dither oscillator. The phase detector output is a full-wave rectified waveform proportional to the amplitude of the error signal. The polarity is positive when the two signals are in-phase and negative when out-of-phase. The

rectified wave form is then integrated, amplified, summed with the dither signal, and applied to the crystals through the breadboard load.

3.1.5 Manual Compensator.

The Manual Compensator permits operation of the modulator exclusive of the Automatic Compensator electronics. The Manual Compensator provides a bias that is adjustable by setting a potentiometer. It switches off the plus and minus 15 Vdc supply voltages to the error amplifier and the dither oscillator/detector, and connects these voltage to an adjustable resistor which permits manual control of the dc signal to the bias amplifier.

3.1.6 Power Supply.

Figure 3-8 is a block diagram of the power supply. Eleven voltages are provided for the operation of the Modulator Driver, Automatic Electronic Compensator, and Temperature Controller. Each supply is voltage regulated and current limited, except the batteries. The function of the batteries is to supply stable, ripple-free power to the silicon photodiode at a very low current level. Table 5 lists the voltages provided.

3.2 1.06 μm MODULATOR

The 1.06 μm modulator is shown in the photograph on Figure 3-9. This modulator is 12.5 cm x 11.55 cm x 14.9 cm, weighs 1.67 kilograms, and dissipates 30 watts average. It is very similar to the 0.53 μm modulator described in Section 3.1 except for the added fins which facilitate dissipation of the additional heat from this unit. This modulator does not contain an automatic electronic compensator, but provisions have been made to incorporate one by removing the two blank modules, inserting the compensator modules, and making the wiring changes noted in Section 4.3.

3.2.1 1.06 μm Modulator Subassembly

The 1.06 μm modulator subassembly is identical to the 0.53 μm modulator subassembly described in Section 3.1.1 except that the crystals are 0.3mm cross section and are coated for 1.06 μm wavelength.

3.2.2 Modulator Driver

The 1.06 μm driver is identical functionally to the 0.53 μm driver described in Section 3.1.2. It differs only in that different transistors

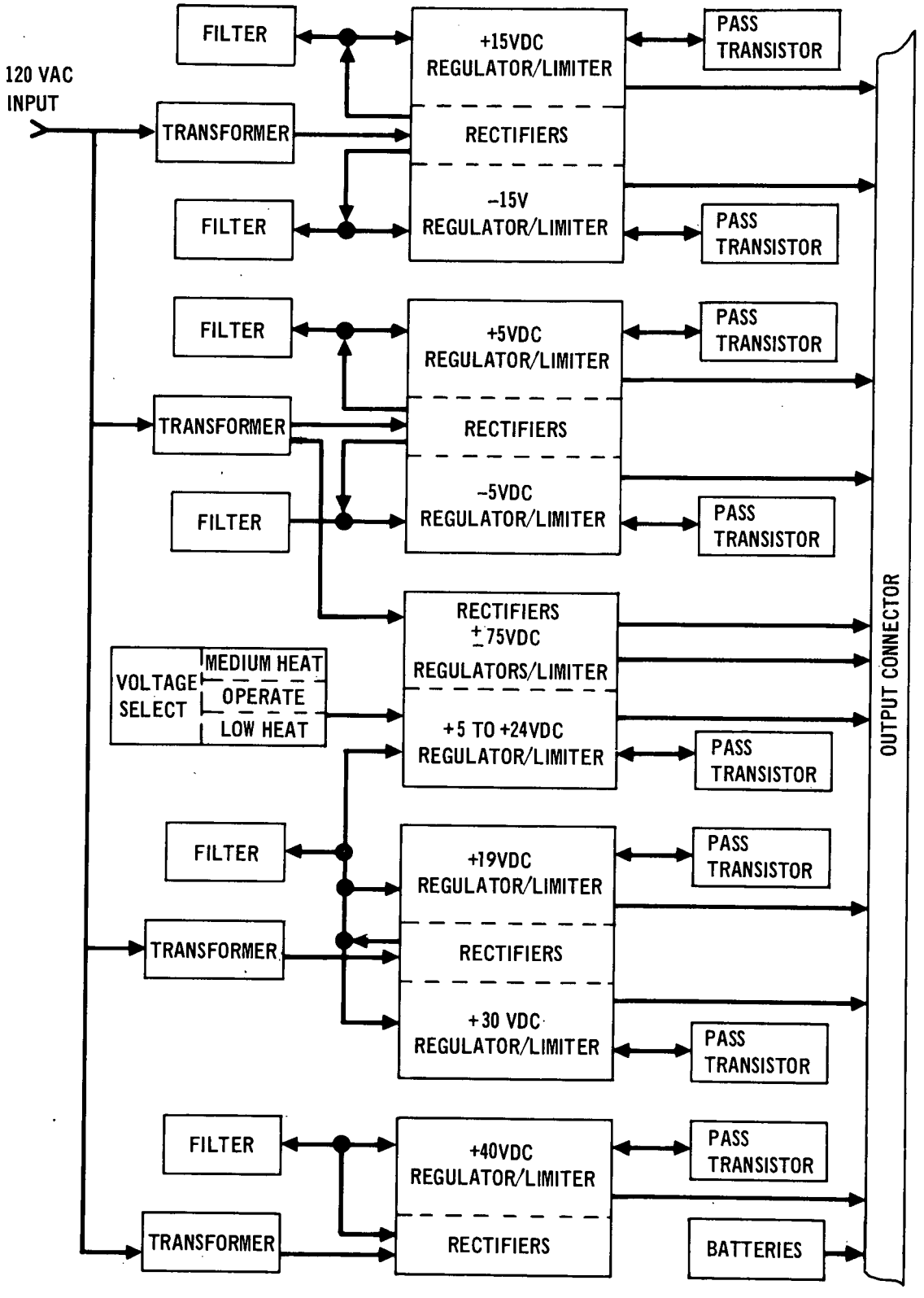


FIGURE 3–8 POWER SUPPLY

TABLE 5

MODULATOR POWER SUPPLY VOLTAGES

+5.0	Vdc - Regulated, for Automatic Compensator
-5.2	Vdc - Regulated, for Modulator Driver, Automatic Compensator
+15	Vdc - Regulated, for Automatic Electronic Compensator and Temperature Controller
-15	Vdc - Regulated, for Automatic Electronic Compensator and Temperature Controller
+6/19	Vdc - Regulated, for Modulator Driver (6V for 1.06 μm, 19V for 0.53 μm driver)
+18/30	Vdc - Regulated, for Modulator Driver (21V for 1.06 μm, 30V for 0.53 μm driver)
+40	Vdc - Regulated, for Modulator Driver (1.06 μm Driver only)
+24	Vdc - Regulated, for Heater
+75	Vdc - Zener regulated, Filtered, for Automatic Compensator
-75	Vdc - Zener regulated, Filtered, for Automatic Compensator
+200	Vdc - Battery for Silicon Photodiode

are used in the power stages and different bias voltages are used. It operates with the same input signal characteristics (Table 1) as the 0.53 μm drive. It delivers a 30 V pp signal (9 watts at 50% duty cycle) to the matched load while dissipating 9.5 watts internally.

3.2.3 Temperature Controller

The Temperature Controller used in the 1.06 μm modulator is identical to the 0.53 μm modulator temperature controller described in Section 3.1.3.

3.2.4 Automatic Electronic Compensator

The 1.06 μm modulator does not contain an Automatic Electronic Compensator. The 0.53 μm compensator described in Section 3.1.4 was designed to operate in the 1.06 μm modulator when the proper bias voltages are supplied. Space has been allotted to insert the automatic compensator modules and the avalanche photodiode has been included in the optics head. Thus with the incorporation of minor chassis wiring changes the compensator can be incorporated in the 1.06 μm modulator.

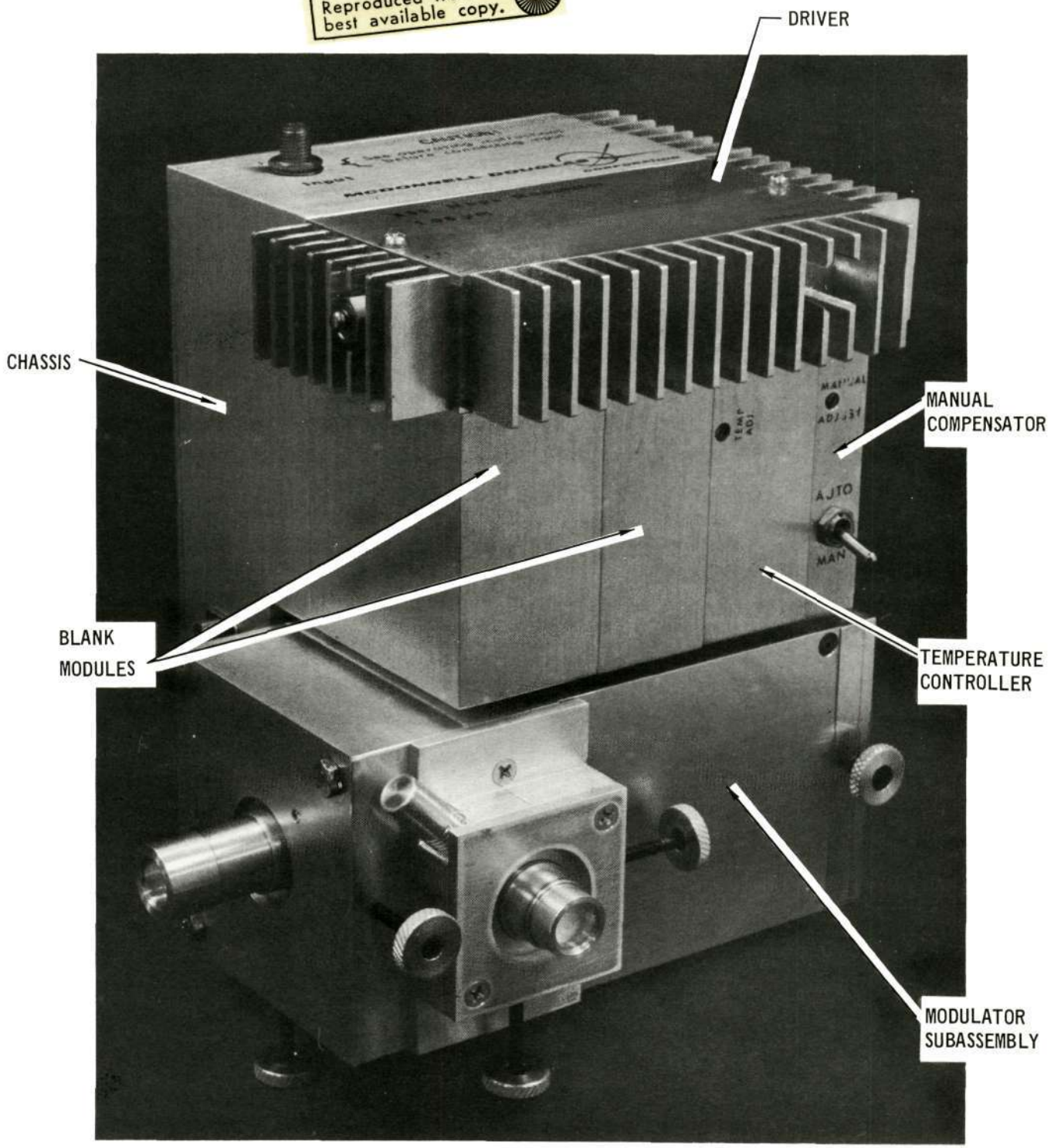


FIGURE 3–9 400 Mbps 1.06μ M MODULATOR

3.2.5 Manual Compensator.

When the Automatic Electronic Compensator is not installed, the Manual Compensator connects directly to the broadband load and provides an adjustment range of plus and minus 75 volts. When the Automatic Electronic Compensator is installed, the Manual Compensator function is identical to that described in Section 3.1.5.

3.2.6 Power Supply.

The power supply is the same unit described in Section 3.1.6. The 40 volt supply is used for the 1.06 μm system only. The 6/18 and 18/30 volt supplies which are set for the 0.53 μm modulator require readjustment for use with the 1.06 μm modulator. When the Automatic Electronic Compensator is not used the +5.0V, ±75V, and the 200 Vdc supplies are not used.

3.3 SIGNAL PROCESSING ELECTRONICS

The block diagram of the Signal Processing Electronics is shown on Figure 3-10. The electronics supply digital data to the modulator in the form of pseudorandom codes or digitally encoded analog data. The Signal Processing Electronics consists of 8 modules in a 10.1 cm x 15.7 cm x 17.8 cm stack which dissipate approximately 50 watts. Figure 3-11 is a photograph of the electronics.

The pseudorandom code word generator outputs serial NRZ data (MECL levels) at bit rates up to 400 Mbps to the modulator driver. It operates from an external 1V pp clock source which is locked to the laser pulse frequency and can be connected to obtain several different code sequence lengths.

The encoding electronics digitizes analog signals within a ± 0.75V pp range into a serial NRZ digital train (MECL levels) which can be used as a data source for the modulator driver. The encoding is accomplished with two identical 200 Mbps processing chains whose outputs are interleaved to obtain the 400 Mbps serial data. Each chain contains a buffered sample/hold capable of 40 MHz sampling rates, a 5 bit simultaneous type analog/digital converter which quantizes the analog sample to 32 discrete levels, and a shift register to convert the 5 bit parallel samples into a serial bit stream. The timing and control module accepts a 1V pp clock signal (400 MHz maximum) which is locked to the laser pulse frequency and phase. The reference voltage generator supplies adjustable filtered bias voltages for the A/D converter comparator references.

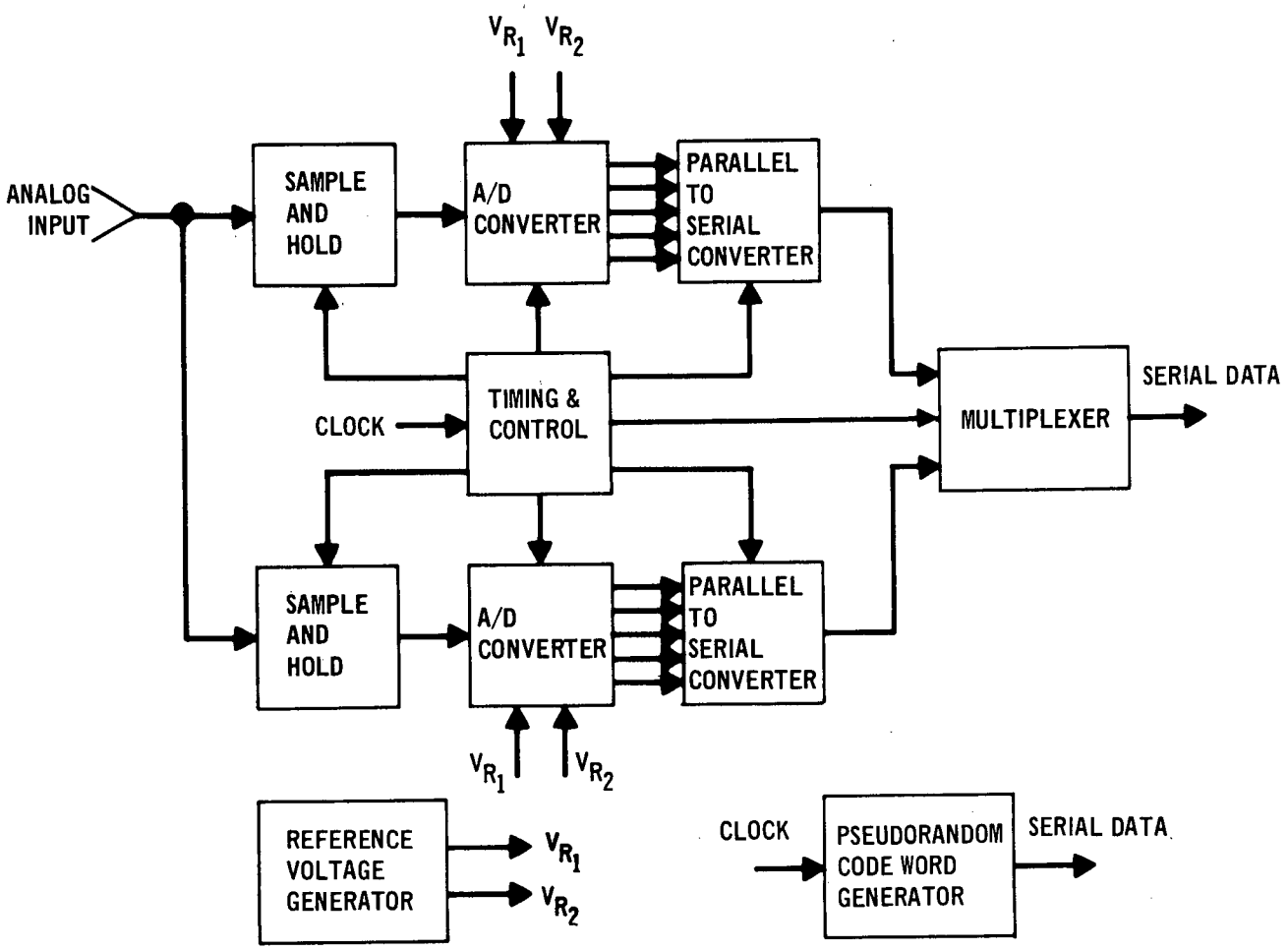


FIGURE 3-10 BLOCK DIAGRAM OF SIGNAL PROCESSING ELECTRONICS

3.3.1 Pseudorandom Generator

The pseudorandom (PN) generator was designed using passive delay lines in lieu of active elements in the shift register as shown in the functional diagram of Figure 3-12 . Any specific maximal length sequence can be obtained by modulo 2 feedback from the N_i and N_t stages of the generator. The desired feedback condition is obtained by selection of delay line cable lengths. Delay 1 sets up the proper delay for stage 2 through N_i and delay 2 gives the proper delay for stage N_{i+1} through N_t.

This approach has the following advantages relative to the conventional implementation of a PN generator with all active elements: 1) the maximum generator operating frequency is limited only by the maximum flip/flop toggle frequency, 2) Various code sequences can be obtained by proper selection of delay line cable length, 3) Power dissipation is minimized. The only disadvantage of this approach is that the clock frequency can only be varied

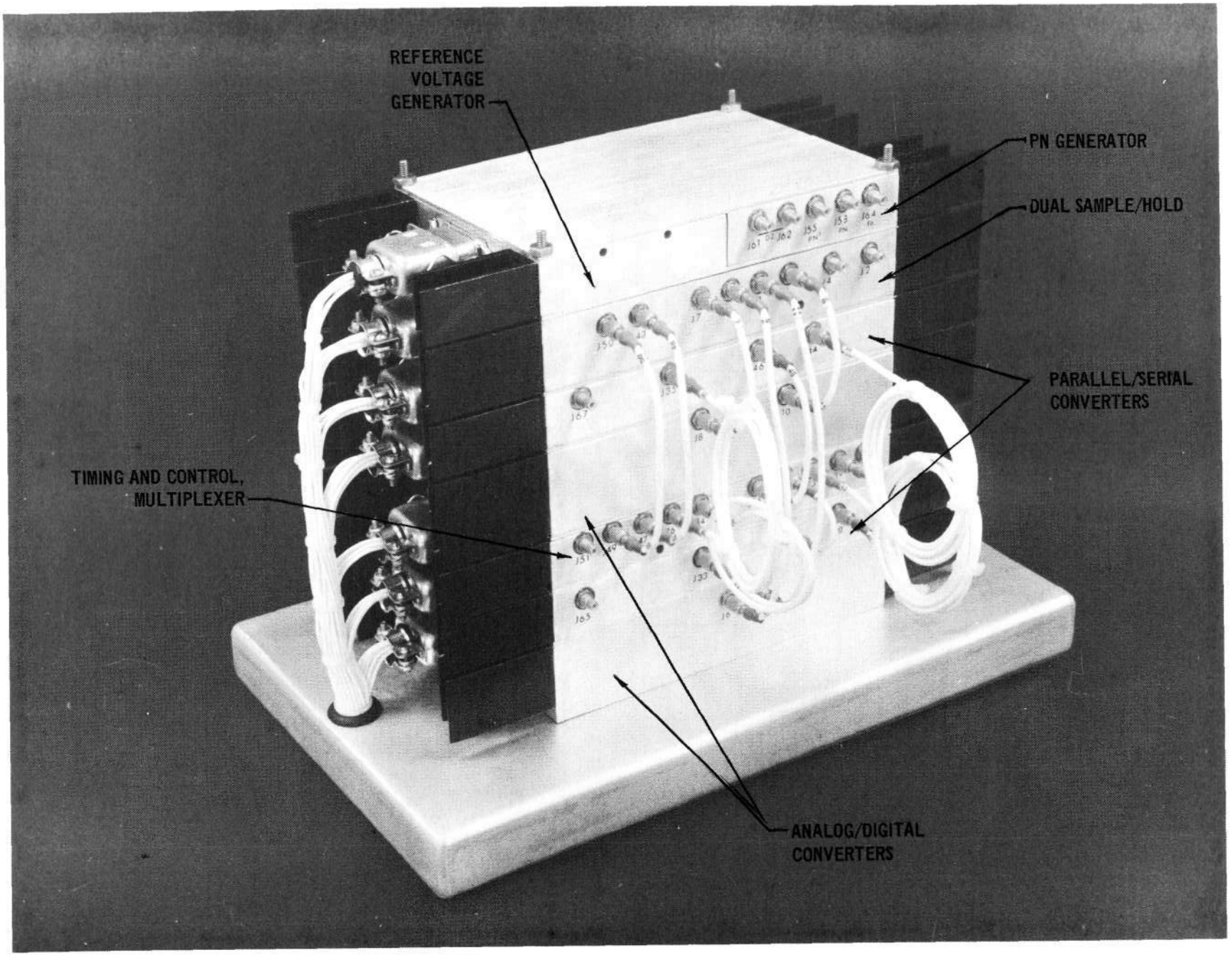


FIGURE 3–11 SIGNAL PROCESSING ELECTRONICS

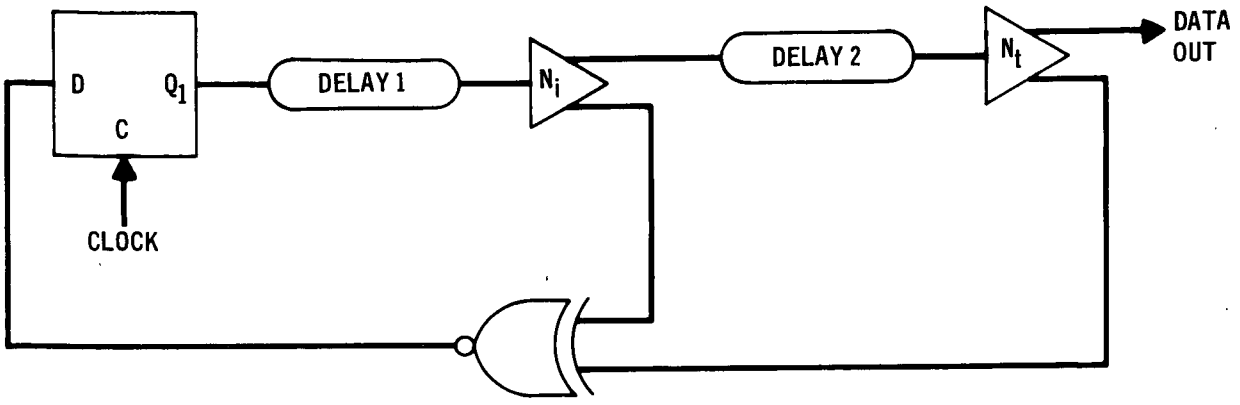


FIGURE 3-12 FUNCTIONAL DIAGRAM – PN GENERATOR

approximately 5% about the nominal for any given set of delay lines. This is not a restriction for normal operating conditions.

The delay lines to implement maximal length PN sequences of 31, 63, 127, 511, 1023, 2047, and 32,767 bits at 400 MHz and 63 bits at 200 MHz and 300 MHz are furnished with the unit.

3.3.2 Dual Sample Hold

The functional diagram of the dual sample/hold is shown on Figure 3-13. This unit samples analog data within the limits of $\pm$ 0.75V pp and holds each sample at a constant level for a sufficient time to allow the comparators in the A/D converter to reach a binary decision. The two sample/holds are strobed out of phase with each other at rates up to 40 MHz. This results in an effective maximum analog input sampling rate of 80 MHz. The bandwidth of the analog input signal should be restricted to approximately 2.5 times less than the sampling rate. The two sample/holds were matched and designed to minimize the contribution of aperture error, feedthrough, offsets, droop, and nonlinearity to the overall encoding system accuracy.

The diode bridges are driven from buffer amplifiers with low output impedance. Low impedance drive to the bridges is necessary to obtain maximum slewing capability for the circuit. The slewing is limited by a RC time constant composed of the output impednace of the buffer, the "on" resistance of the bridge, and the capacitance of the holding capacitor. The bridge is composed of four hot carrier diodes that are matched and mounted in hybrid form in a single package. This arrangement reduced parasitics and minimized

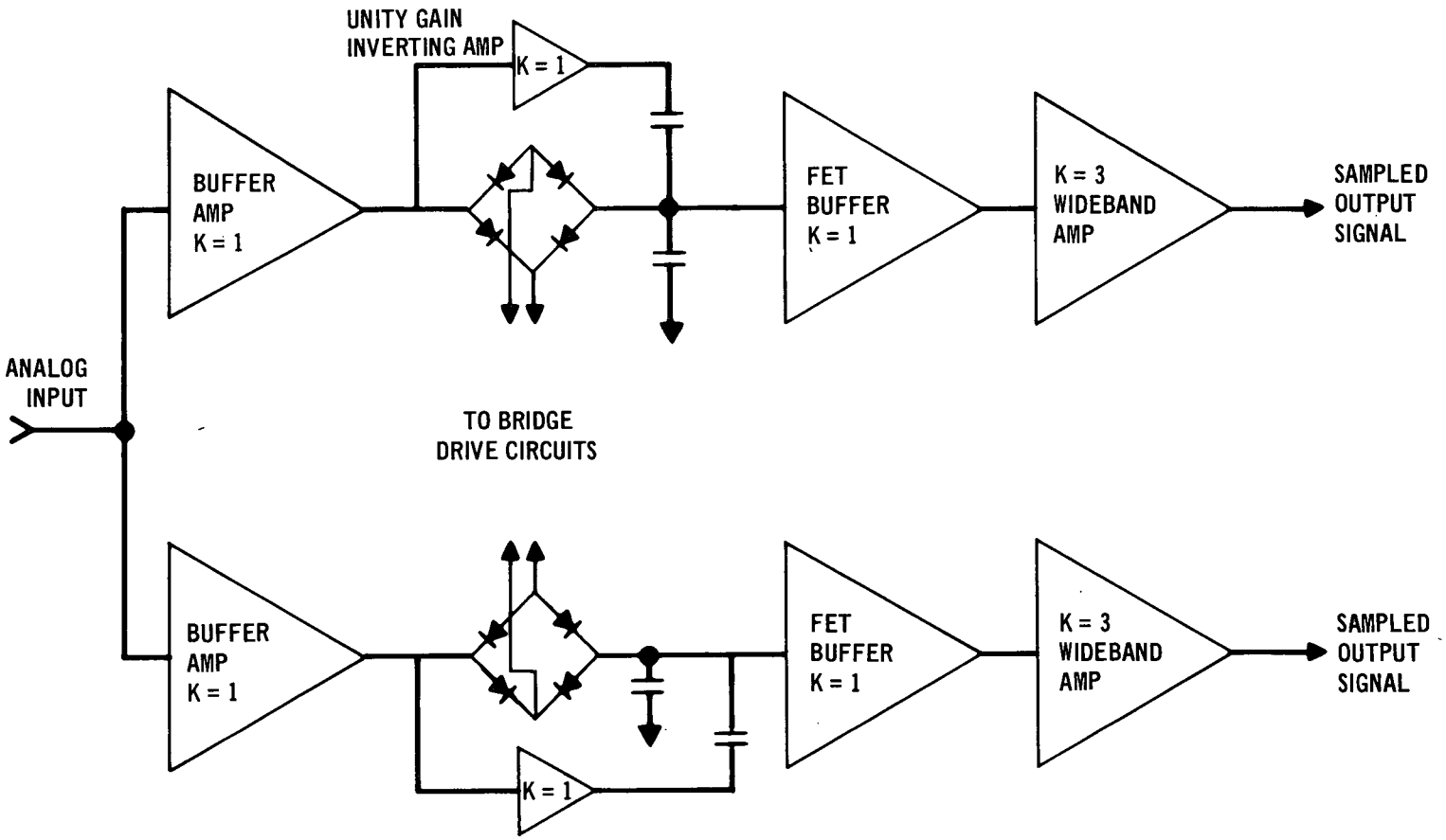


FIGURE 3–13 DUAL SAMPLE/HOLD

feedthrough. The size of the holding capacitor was determined by a tradeoff between slewing capability and holding droop. The unity gain inverting amplifier was used to cancel capacitive feedthrough of the analog input while the bridge is in its off condition. FET input unity gain buffers were used at the output of the bridges to maintain high impedance conditions at the holding capacitor. Wideband amplifiers having gains of 3 follow the FET input buffers. Amplification of the signal at this point minimizes the error contribution of the A/D converter comparator offset and hysteresis.

3.3.3 Analog/Digital Converter

Figure 3-14 is a functional diagram of the A/D converter which was implemented using the parallel conversion technique. Thirty-one differential comparators were used in parallel. A divider chain composed of equal value resistors was used to set references at each comparator input. The analog sample is simultaneously compared to the 31 equally spaced reference levels. At this stage, the analog input is linearly related to the output states of the 31 comparators. A linear to binary converter was used to get the digital information into 5 bit binary format. Each differential comparator has a strobe input which is used to latch the data. This insures stable outputs during parallel to serial conversion.

The A/D converters were implemented using Mecl III type comparators and logic elements.

3.3.4 Parallel/Serial Converter

Figure 3-15 is a functional diagram of the parallel to serial converter. The 5 bit parallel words from the A/D converter are presented to the converter at inputs B1 through B5. These inputs are seen by the binary logic elements during the parallel strobe clock pulse at which time the binary logic element is either set or reset depending on whether a binary "1" or "0" is present at the respective B input. After this parallel strobing action the data is shifted to the right of the shift register at a rate that is equal to the frequency of the serial clock. Figure 3-16 shows the parallel strobe clock and the serial clock in the proper phase alignment. The serial clock has a pulse missing every five clock periods, this is to allow time for a new 5 bit parallel word to be strobed into the shift register. The input from B1 is present at the serial data output immediately after the parallel

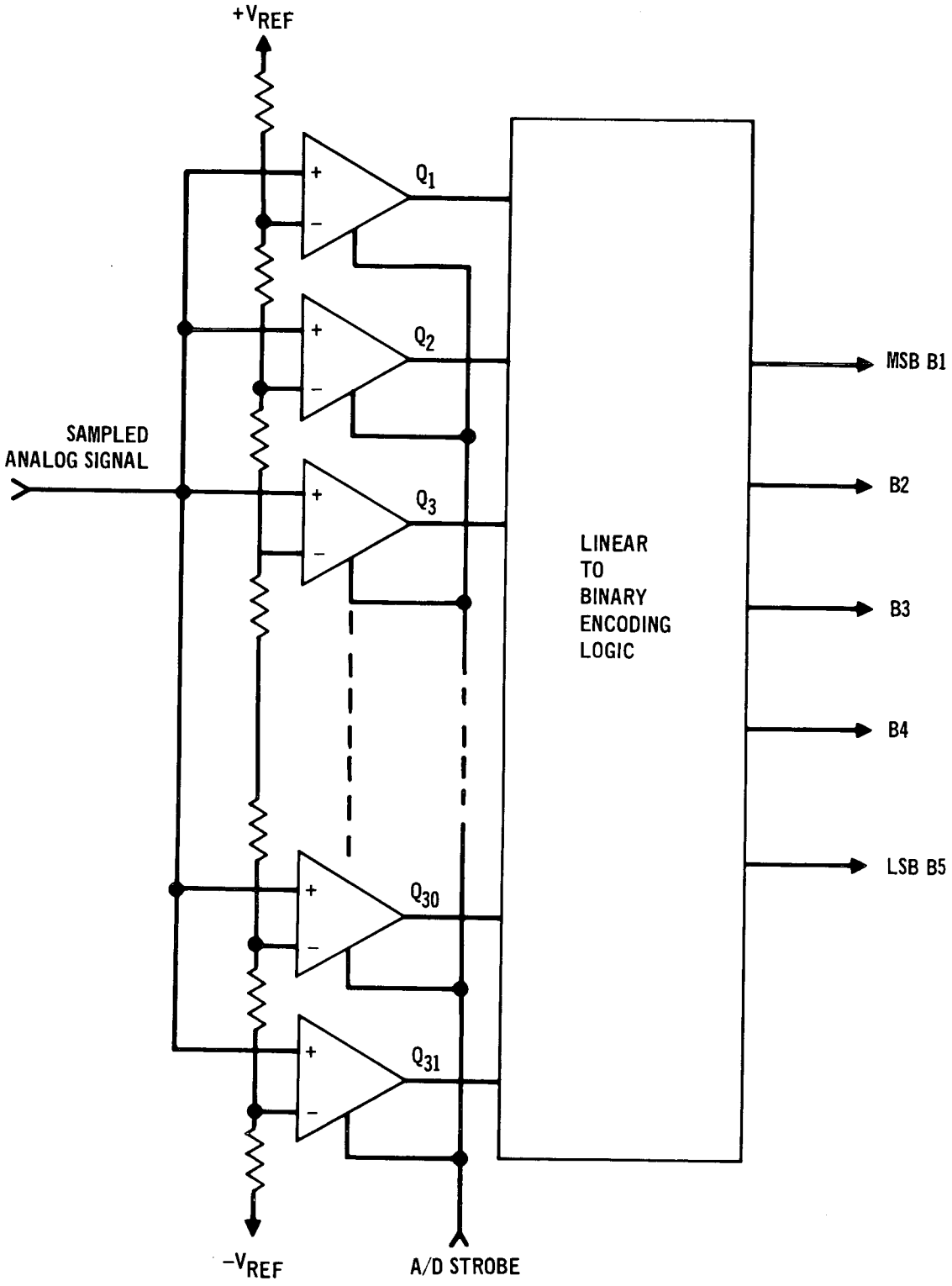


FIGURE 3–14 A/D CONVERTER FUNCTIONAL DIAGRAM

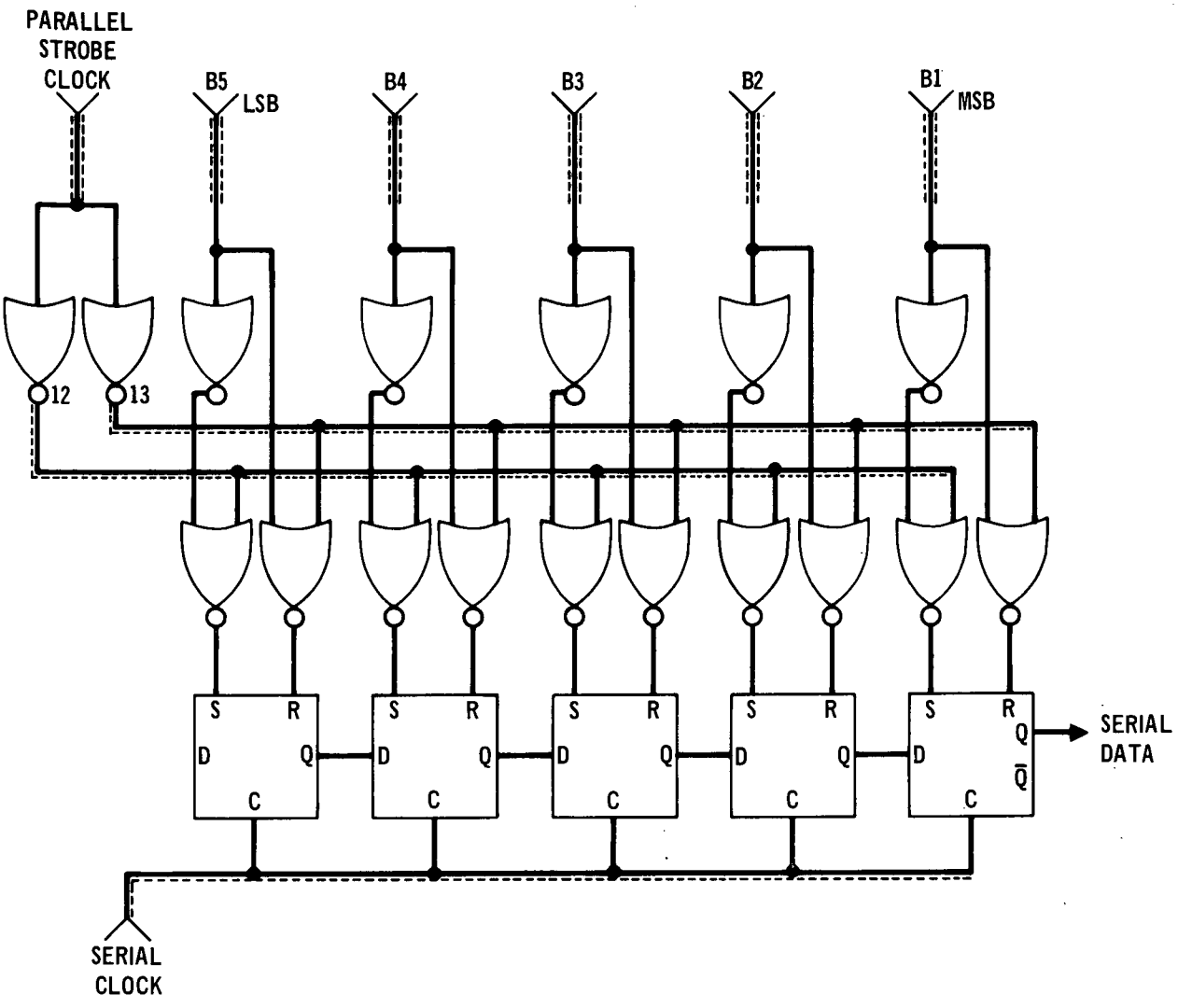


FIGURE 3-15 PARALLEL/SERIAL CONVERTER FUNCTIONAL DIAGRAM

strobe. Thus the serial bit stream is not interrupted by the absence of the serial clock pulse.

The parallel/serial converter was implemented using Mecl III type integrated circuits and discrete clock and output drivers.

3.3.5 Timing and Control/Multiplexer

The timing and control board contains circuits for clock countdown, clock conditioning, and clock driving necessary for proper operation of the entire signal processing electronics package. In addition it contains a digital

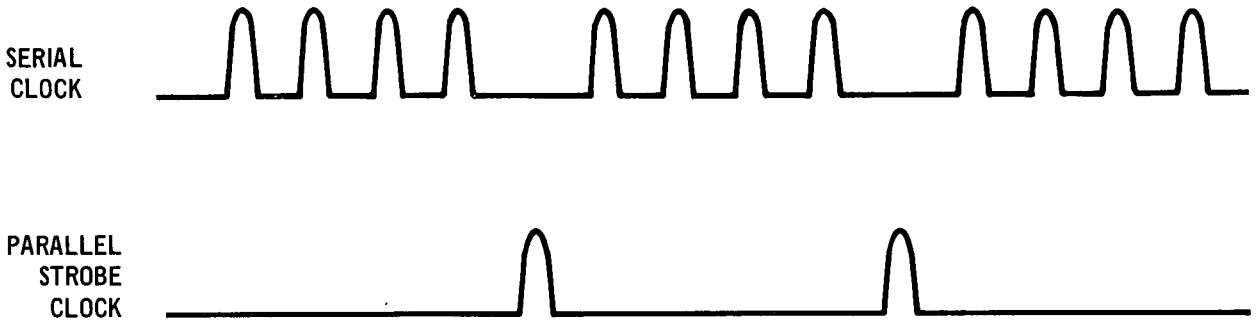


FIGURE 3-16 PARALLEL/SERIAL CLOCK WAVEFORMS

multiplexer which accepts two 200 Mbps serial data trains and combines them into a 400 Mbps serial NRZ data train with MECL logic swings. Figure 3-17 is a functional diagram of the timing and control/multiplexer module. Figure 3-18 shows the clock waveforms produced at each of the outputs on Figure 3-17 . The system clock, f_o, is brought into the timing and control board and first divided by two and then by five. The $f_o/10$ output is then divided into two separate channels and phasing between the two channels is positioned to 180°. Each channel is then fed through a shaping circuit which outputs 3.3 ns pulses at a frequency of $f_o/10$. The logical compliment is also made available in each case. The $f_o/2$ output is put into a conditioning circuit where it is separated into two channels which are 180° out of phase with each other. Each of these channels are then conditioned with $f_o/10$ signals such that every fifth pulse is eliminated. The missing pulse for each channel occurs 180° out of phase as shown in Figure 3-18 . The timing and control electronics were designed such that the phase relationship between outputs remain 180° for any value of f_o.

The multiplexer is composed of two "and" gates, one "or" gate, and a reclocking circuit. Each serial data stream to be multiplexed is "anded" with either the $f_o/2$ clock or its compliment. By performing the logical "or" function on the output of these "and" gates we obtain a multiplexed bit pattern. This bit pattern is then reclocked with f_o.

3.3.6 Reference Voltage Generator

Figure 3-19 is a functional diagram of the A/D reference voltage generators. These generators supply the reference voltages required by the A/D

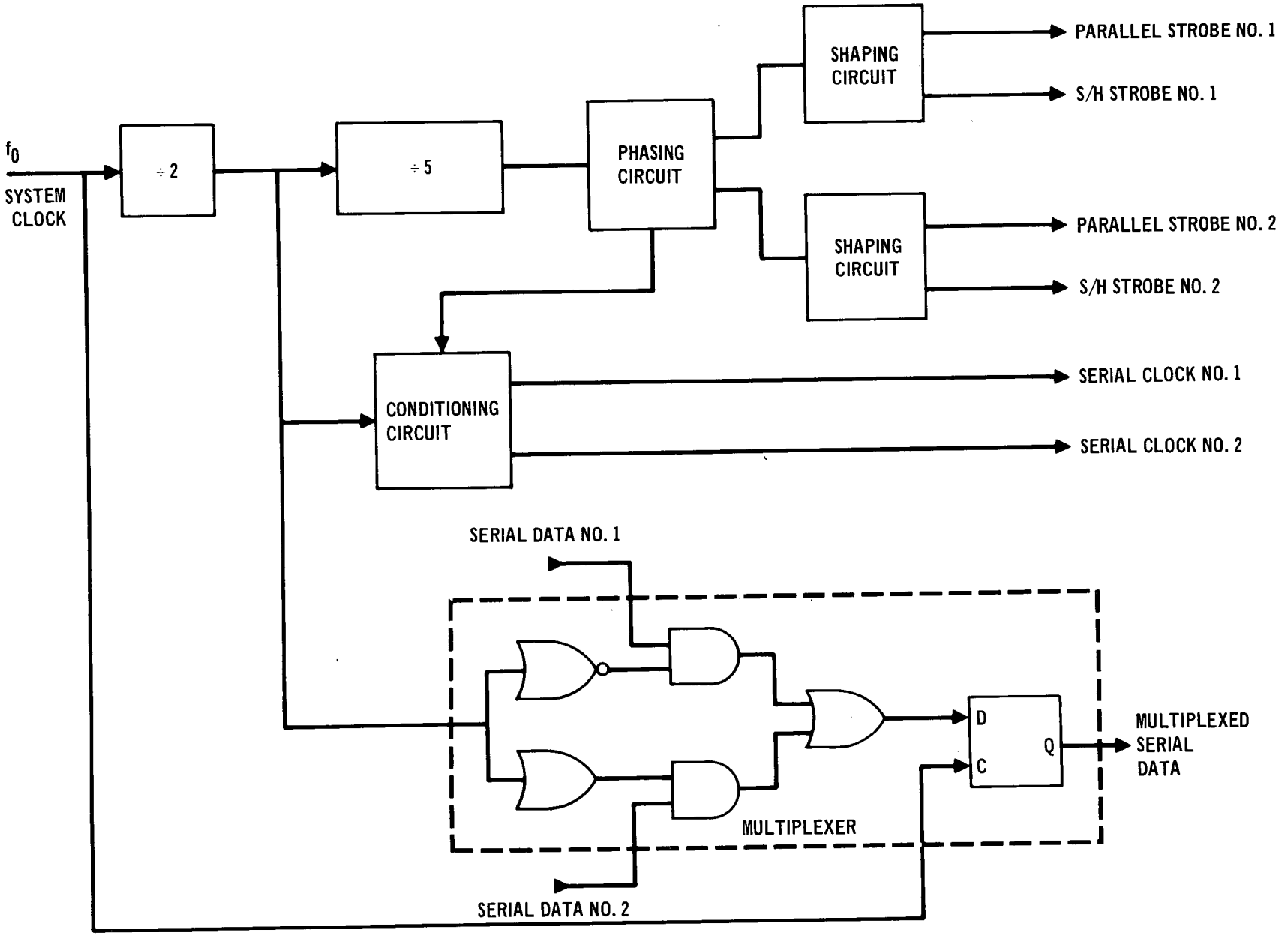


FIGURE 3–17 TIMING AND CONTROL/MULTIPLEXER FUNCTIONAL DIAGRAM

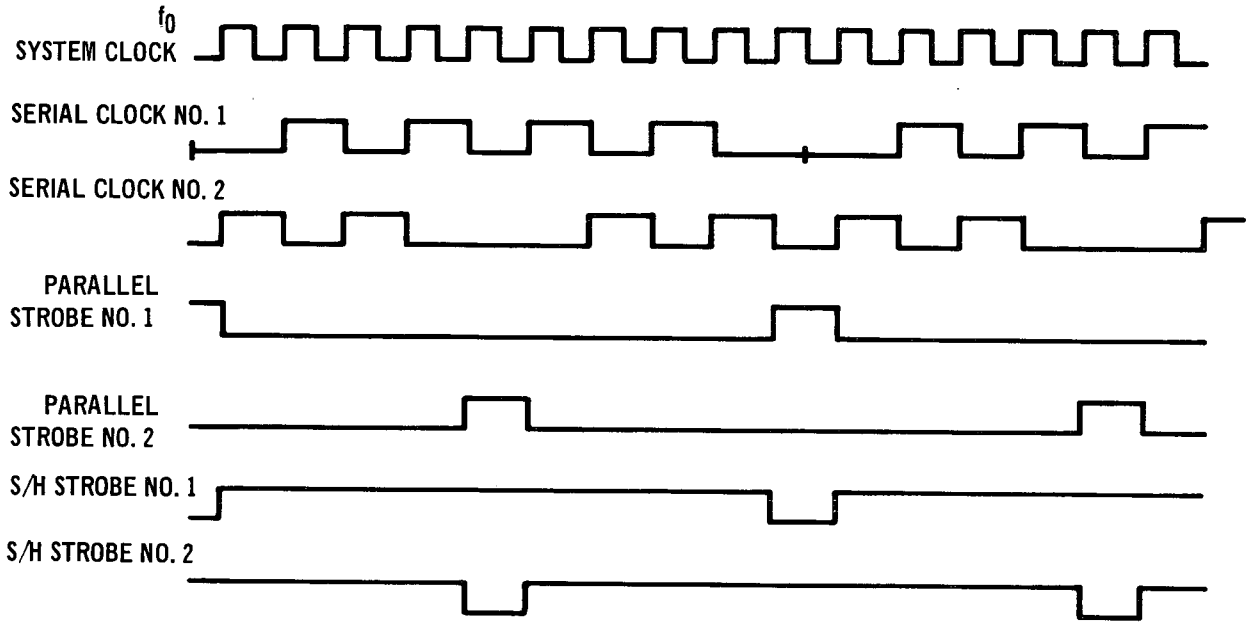


FIGURE 3-18 TIMING AND CONTROL CLOCK WAVEFORMS

converters to set the limits on the conversion intervals. Each reference generator consists of a voltage follower and resistor divider network. The regulated +V and -V voltages are supplied by the signal processing power supply. The resistor network values were selected such that the maximum reference voltage obtainable from any one unit is $\pm$ 2.5 volts. This is the maximum voltage allowed at any A/D comparator input. Each reference generator is independent and can supply any voltage in the range of $\pm$ 2.5 volts.

3.3.7 Signal Processing Electronics Power Supply

Figure 3-20 is a block diagram of the signal processing electronics power supply. Five voltages are provided for the operation of the signal processing electronics. Each supply is voltage regulated and current limited. Table 6 lists the voltages provided.

Table 6 - Signal Processing Electronics Power Supply Voltages

-2.0 Vdc - Regulated,
+5.2 Vdc - "
-5.2 Vdc - "
+12.0 Vdc - "
-12.0 Vdc - "

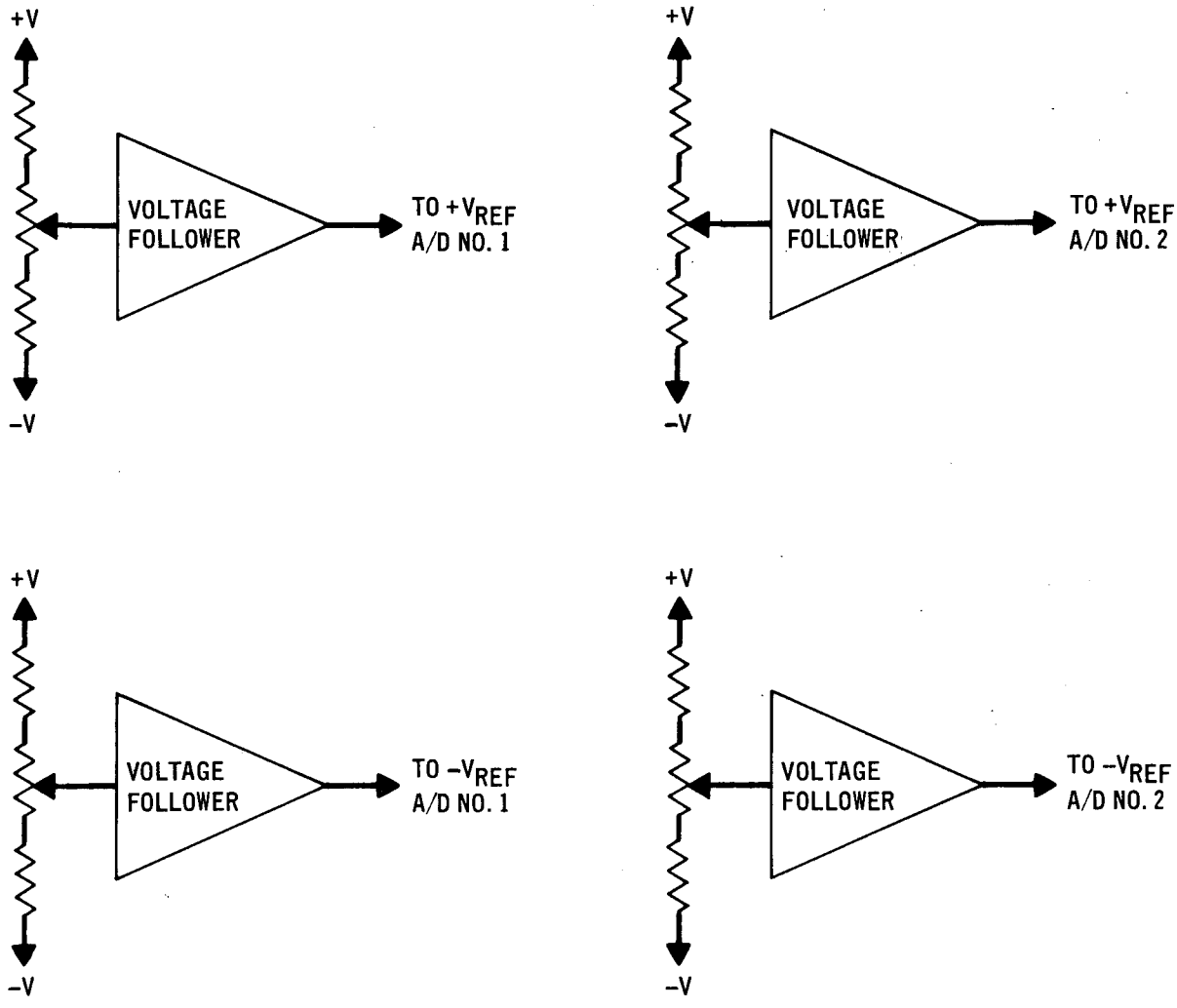


FIGURE 3–19 A/D REFERENCE VOLTAGE GENERATORS FUNCTIONAL DIAGRAM

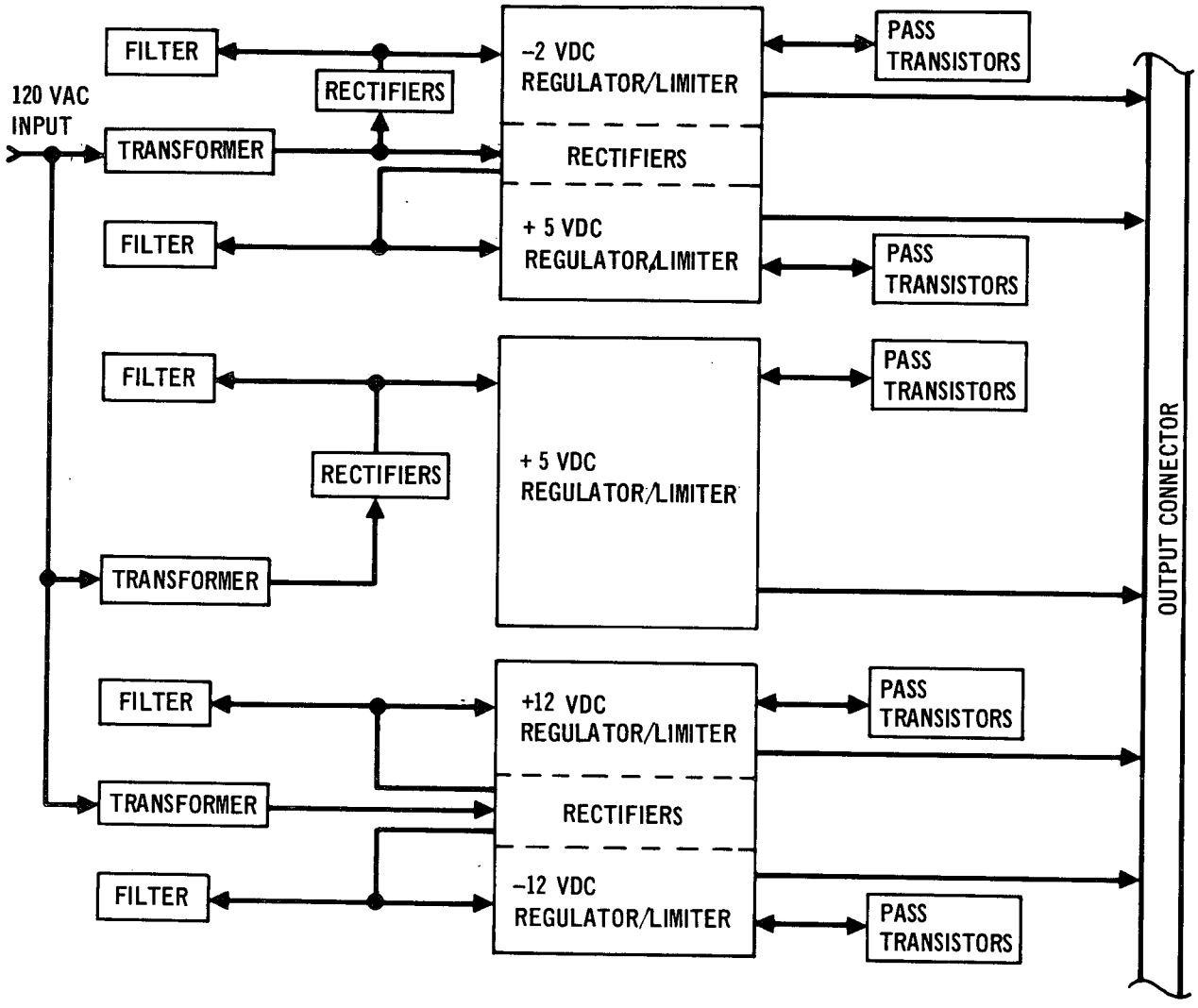


FIGURE 3–20 POWER SUPPLY

4. OPERATING INSTRUCTIONS

4.1 MODULATOR OPTICAL ALIGNMENT

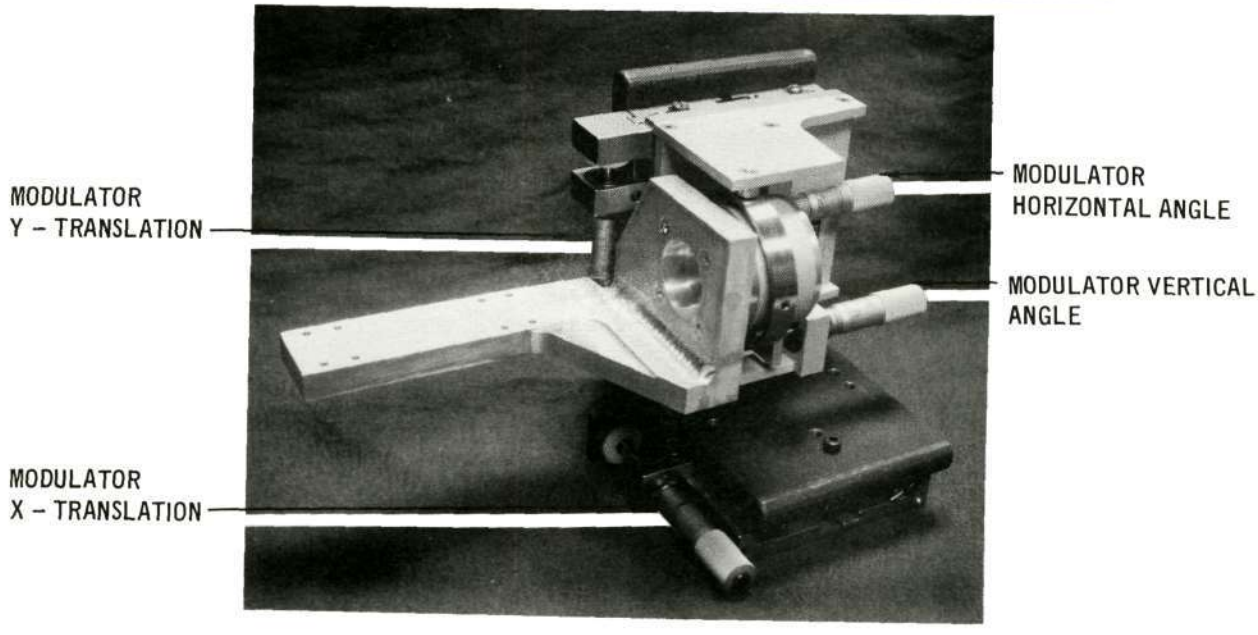
The alignment of the modular is a straightforward procedure which must be done properly to realize the maximum transmission and extinction ratio capabilities of the modulator. If one step of the alignment is not done properly it is likely that the whole alignment procedure will have to be repeated. It is not usually possible to correct an alignment deficiency by guess work due to the large number of interacting adjustments. The steps of the alignment procedure follow in order. Figure 4-1 shows the adjustment locations on the modulator mount, optics head, and rear mirror holder. This figure should be referred to when reading the alignment instructions.

(1) Examine the laser output. The laser mode configuration must be TEM_{oo}. This can be verified by visually examining the laser beam on a screen. For this examination the beam should be expanded to a few inches in diameter. Any visible intensity changes, or beam diameter changes, will seriously degrade modulator performance. A detector should be used to look at the pulse shape and width of the mode locked signal. Any phase state switching or other changes will hamper the proper timing adjustment of the modulator driver and compensator gate. As a final check for the 0.53 μm unit only, be sure that no 1.06 μm laser output is entering the modulator.

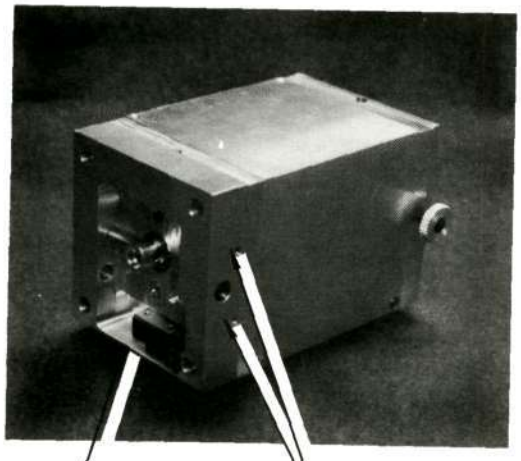
Another problem which can be encountered with modulator alignment is any 1.06 μm output being reflected directly back into the laser will upset the mode locking stability. If the laser goes unstable during modulator alignment or use, blocking the beam to the modulator will tell whether this is a problem or not.

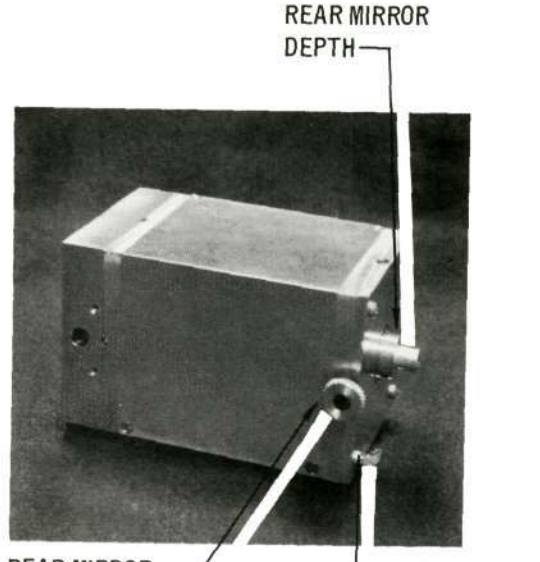
(2) Adjust the laser polarization. The laser output must be horizontally polarized for proper operation of the modulator. A half-wave plate can be used to rotate the polarization if necessary.

Insert a polarizer in the laser beam and adjust it so that minimum transmission occurs. Remove the polarizer and set it aside for later use in the alignment procedure. Extinction ratio achieved with this polarizer should be very good as it is limited only by the degree of polarization of the laser light.



A) MODULATOR HOLDER





C) REAR MIRROR HOLDER LOCATION

FIGURE 4–1 MODULATOR ALIGNMENT ADJUSTMENT LOCATIONS

(3) Place the modulator in the beam. Remove the front lens and pull out the back mirror. If the optics head has been removed, or a complete realignment is desired, the initial position of the beamsplitting mirror should allow passage of the entire beam. This adjustment uses the two recessed screws on the right side of the optics head shown in Figure 4-1(B). The side lens holder must be removed to reach these screws. Align the modulator so that the back reflections from the crystal faces are quite close to the incoming beam. The four adjustments shown in Figure 4-1(A) are used for this alignment procedure. Light transmitted through the modulator should be seen. Be sure that the modulator is at operating temperature (∿150°C). Place a lens in the transmitted beam so that the back crystal edges are sharply focused on a screen. A 30 to 60mm focal length lens is suggested for this purpose. If all four crystal edges are not equally sharp the crystals are slightly tilted in the beam. Tilt and walk the modulator until maximum light is transmitted through the crystals. Again use the adjustments shown in Figure 4-1(A) for this procedure.

Place the polarizer which was previously calibrated and set aside, in the output beam. Adjustment of the manual compensator will move the fringe pattern in the crystal image. The black area of the fringe pattern should be as dark as possible. If the modulator is off more than a few degrees in rotation about the incoming optical beam from its proper position the extinction ratio of the various parts of the pattern will be degraded. If it is off by 45°, the light will be pure O-wave and pure E-wave and no fringes will appear in the pattern. Turn the modulator in the mount for the best definition of the crystal fringe pattern.

(4) Adjust for best single pass operation. Place the front lens in the front holder if the front holder is attached to the modulator head. Otherwise, use an XYZ lens holder in front of the optics head for positioning the lens. A single lens will suffice for confocally focusing the laser beam into the modulator, if its focal length is chosen properly. The best convergence angle of the light entering the modulator is about 17 mrad for the 0.53 μm unit and 22 mrad for the 1.06 μm unit. Do not use more convergence than this. It is permissible to decrease the divergence by as much as 10% without affecting modulator performance. An increase in divergence will broaden the incoming and outgoing beams at the polarizing

beamsplitter and consequently require larger separation of the two beams. The beam convergence should be checked for each new setup because any change in laser beam width, or divergence, produces a proportional change in the convergence angle for a particular lens.

Adjust the front lens so that light passes through the crystals and onto the screen (used before for the alignment in the unfocused laser beam). The back lens is still in place for this adjustment. Adjust for a focused spot in this screen. The optical bias should be set for maximum transmission at the crystal center. Now remove the lens which focuses the spot on the screen but leave the front lens in place. Adjust the lens position for maximum extinction ratio by observing the expanded spot on the screen. In some cases a minor adjustment in the modulator position may be necessary at this time.

After these adjustments are completed the back mirror should be inserted and adjusted so that the beam falls back on itself and is of the same characteristics as the incoming beam. CAUTION: INSERT REAR MIRROR SLOWLY AND CAREFULLY AS IT CAN CONTRACT REAR SURFACE OF CRYSTAL AND CAUSE DAMAGE. A SCRIBE MARK DENOTES NOMINAL DEPTH. The two screws at the side and bottom of the rear of the modulator shown in Figure 4-1(C) are used for the alignment of the beam. Beam divergence is controlled by sliding the mirror holder back and forth in its sleeve. Mark the depth of the mirror holder and pull it out if the beamsplitter mirror is to be adjusted at this time.

(5) Adjustment of the beam splitting mirror. The beam splitting mirror may be adjusted with the modulator aligned for best single pass operation as in the preceding section. In this case the two adjustment screws on the right side of the optics head are backed off so that the aperturing of the beam by the coated portion of the mirror is noticeable. The angle of output cannot be adjusted yet as no output beam is available.

An alternate and probably preferable method of making this same adjustment is to remove the front lens and replace the back lens. Do not move the modulator with respect to the incoming collimated laser beam. The focused back face is now observed as the beam splitter mirror is walked into place with the two adjustment screws. The aperture of the face by the coated portion of the mirror creates a shaded area with

a slightly uncertain boundary between. The mirror is adjusted so that the shaded area covers somewhat less than half the crystal aperture. If this method of adjustment is used the front lens should be replaced and the pattern of the preceding paragraph observed.

(6) Adjust for best double pass operation. This alignment procedure can begin only when it is known that the front lens is at its proper distance from the crystals and in place for best single pass operation, the beam-splitting mirror is in the proper position, and the back mirror has been adjusted for proper depth and approximate lateral position.

Use horizontal angular and translational adjustment of the modulator to tilt the modulator to the left about 1° so that a return beam comes back from the back mirror. Do not use the side lens here, as the beam should be viewed expanded as in the single pass alignment. The position of the beamsplitter mirror has been adjusted previously. The angle may now be adjusted by turning one screw in and the other out an equal amount until the exit beam comes out through the polarizing beamsplitter prism. This adjustment is not too critical as the output lens can translate enough to accomodate two or three millimeters of translation. The compensator diode is affected by this adjustment, however, and if the automatic electronic compensator is to be used the signal must fall on the diode. The diode may be translated a few beam diameters by loosening the two screws in the bottom of the optics head and moving the diode by hand. The location of these screws is shown in Figure 4-1(B). This adjustment can only be made if the front lens holder is removed and the lens held in an external mount. No adjustment of the beam splitter mirror or diode position should be necessary unless the optics head has been disassembled or removed from the modulator for some reason.

After the beamsplitter mirror is in final position the modulator is ready for final alignment adjustments. The degree of static transmission and extinction ratio attainable in this adjustment determines the dynamic operational limits, so care spent here will more than repay itself.

The position of the back reflections from the crystal faces should be observed. Even though each reflection is only a percent or less, the sum total of the eight surfaces is a significant factor in comparison to the amplitude of the zero level. Because of this the modulator should

be walked around an axis such that the transmission is not degraded but the back reflections are about a spot diameter removed from the signal beam. An aperture placed anywhere in the exit beam will then eliminate these spurious reflections. Be careful in making transmission measurement that none of this spurious signal gets into the detector. The safety factor of the 0.53 μm unit does not have a sufficiently large aperture to fully accomodate this adjustment. There is, however, some tilt of the crystal faces which decreases the tilt required for good alignment.

Each of the adjustments of the modulator position, back mirror position, and front lens distance from the crystals should be varied by very small amounts to optimize the extinction ratio. Once the modulator has been aligned, only the modulator position adjustments need be changed to compensate for minor changes in laser beam position such as occur when the laser is stabilized by mirror adjustments for best mode locking.

The signal should be observed using a high speed detector. Modulation should be present at this time. A repetition of the minor adjustments described in the preceding paragraph can be repeated to optimize the quality of the modulated pulse train. A variable delay line is necessary for aligning the modulator drive signal with the laser pulse train.

The alignment of a double pass modulator is rather tedious when tried for the first time. It is straightforward, however, and only two or three times through the alignment procedure are required for sufficient proficiency to achieve satisfactory alignment. Several hours may be required for alignment of the modulator when every adjustment is grossly out of place. The delivered modulators have been prealigned and about two hours should be sufficient to complete the alignment from start to finish including the performance tests such as transmission, static extinction ratio, and dynamic extinction ratio.

4.2 0.53 μm MODULATOR OPERATING INSTRUCTIONS.

After the modulator is set up and optically aligned, the steps listed below should be followed to put the modulator in a fully operational condition:

(1) DISCONNECT DATA SOURCE FROM MODULATOR DRIVER INPUT BEFORE APPLYING POWER TO MODULATOR.

(2) Adjust the power supply voltages as shown in Table 7 before connecting the power supply cable to the modulator.

TABLE 7

POWER SUPPLY ADJUSTMENTS - 0.53 μm MODULATOR

REGULATOR	POWER CONNECTOR		VOLTAGE
	PIN (HI) TO	PIN (LOW)	
+5.0	1	2	+5.0 Vdc
-5.2	3	2	-5.2 Vdc
+15	5	6	+15.0 Vdc
-15	7	6	-15.0 Vdc
+6/19	9	10	+19.0 Vdc
+18/30	11	10	+30.0 Vdc
5/24 (Operate)	12	10	+20.0 Vdc
5/24 (Medium Heat)	12	10	+14.0 Vdc
5/24 (Low Heat)	12	10	+9.0 Vdc

NOTE: Adjusting pots are located and marked on the power supply printed circuit cards and are accessible when the power supply cover is removed.

(3) Turn power supply off and allow at least two minutes for the unloaded voltages to bleed off before connecting to modulator.

(4) Connect power cable to modulator and position heater switch to "MEDIUM HEAT" and turn power switch to the "ON WITHOUT BATTERY" position.

(5) Allow 30 minutes for the modulator subassembly to warm up and then position the heater switch to "OPERATE" and allow another 10 minutes for the temperature to stabilize.

(6) Monitor the modulator driver TP (using a 50 ohm input impedance scope) to determine that the driver is in the logic "0" state (approximately +150 mV dc).

(7) Connect the output of the data source to be used to a 50 ohm input scope. Verify that the data is present with the correct logic swings and does not exceed 70% duty cycle steady state in the logic "1" state.

(8) Connect the data source to the modulator driver (do not turn data source power off while making this connection) input and note that the code is present (inverted) at the driver output test point.

(9) To operate the Manual Compensator position the compensator switch to "MAN" and adjust the manual adjust screw to desired point.

(10) To operate the automatic electronic compensator turn the power supply power switch to "ON WITH BATTERY" and turn the compensator switch to "AUTO."

(11) To shut-down remove modulation-signal cable from modulator input. Turn power supply to "ON WITHOUT BATTERY" and heater switch to "LOW HEAT" for 45 minutes. Then turn power supply to "OFF."

NOTES:

(1) Connection of either of the signal processing data sources to the modulator when these sources are without power results in the modulator driver output stage being biased on 100% duty cycle. The excessive power dissipation in this state can damage, or shorten the useful life of the output transistor. For the same reason data codes with greater than 70% logic "1" duty cycle should not be used.

(2) The low heat and medium heat modes have been incorporated as a precaution to prevent unnecessary thermal shocks to the modulator crystals.

(3) The wiring diagram for the 0.53 μm modulator chassis is given in Figure 4-2.

4.3 1.06 μm MODULATOR OPERATING INSTRUCTIONS.

The steps required to operate the 1.06 μm modulator with the manual compensator are identical to steps 1-9 in Section 4.2 with the exception that the power supply voltages should be adjusted per Table 8. The notes following the turn on procedure for the 0.53 μm modulator also apply to the 1.06 μm modulator. The wiring diagram for the 1.06 μm modulator chassis when connected for manual compensator operation only is given in Figure 4-3.

In order to operate the 1.06 μm modulator with the Automatic Electronic Compensator (AEC), the AEC modules "A" and "B" must be installed in the space pro-

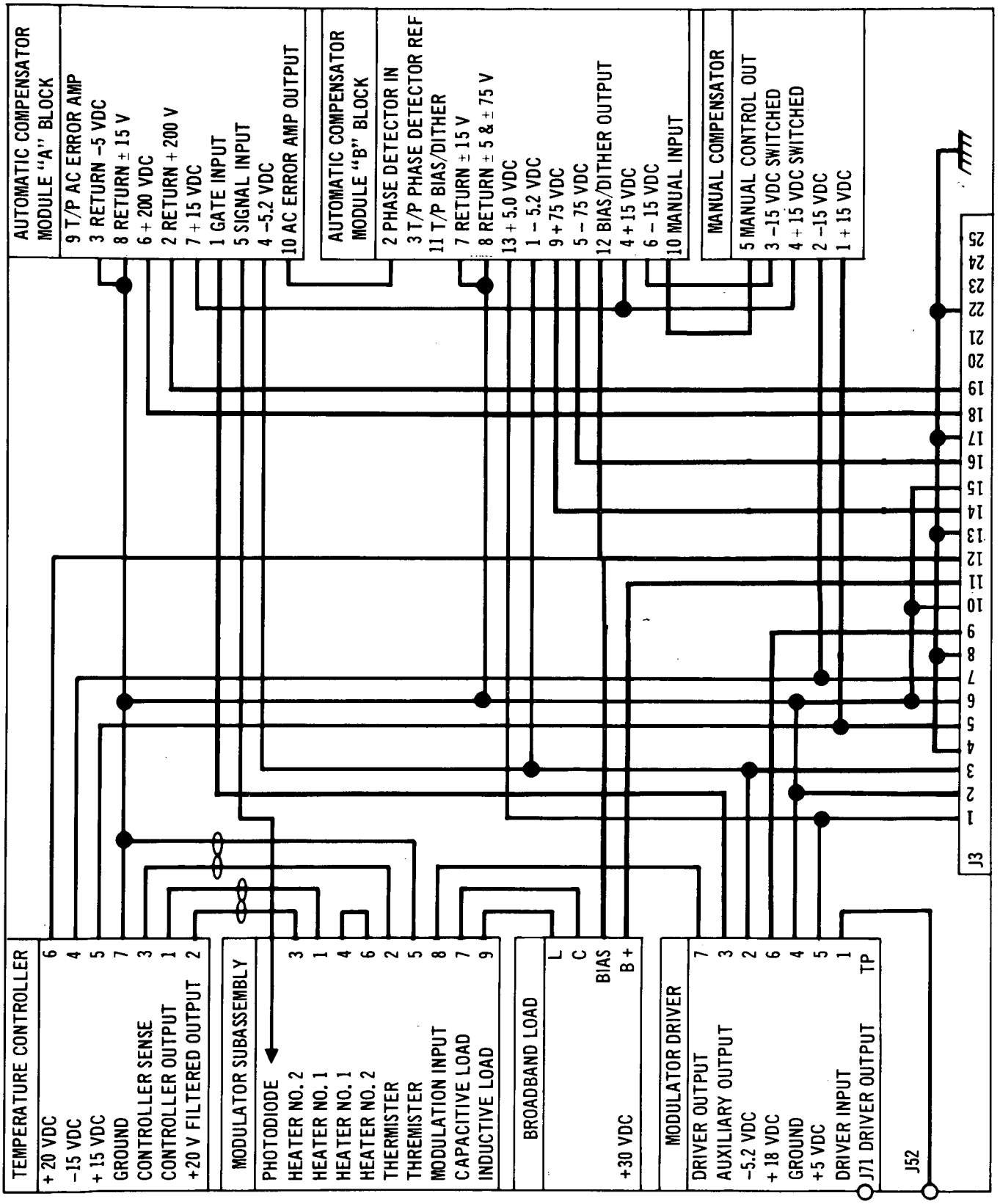


FIGURE 4–2 0.53μM MODULATOR WIRING DIAGRAM WITH AUTOMATIC ELECTRONIC COMPENSATION

TABLE 8 POWER SUPPLY ADJUSTMENTS - 1.06 μm MODULATOR

REGULATOR	POWER CONNECTOR		VOLTAGE
	PIN (HI) TO	PIN (LOW)	
+5.0	1	2	+5.0 Vdc
-5.2	3	2	-5.2 Vdc
+15.0	5	6	+15.0 Vdc
-15.0	7	6	-15.0 Vdc
+6/19	9	10	+6.0 Vdc
+18/30	11	10	+21.0 Vdc
+40	23	24	+40.0 Vdc
5/24 (Operate)	12	10	+20.0 Vdc
5/24 (Medium Heat)	12	10	+14.0 Vdc
5/24 (Low Heat)	12	10	+9.0 Vdc

vided for them on the modulator package. The wiring change listed in Table 9 must be made to change the modulator wiring from the configuration shown in Figure 4-3 to that shown in Figure 4-4 . The wires, or coax, used should be equivalent to their counterparts in the 0.53 μm modulator. The length of the semirigid cable from the modulator driver (J3) to AEC module A (J1) is critical to insure that the gate drive signal is present when the detected pulses (rejected "0's") are present at the gate input. This cable length can be optimized as follows:

(1) Select length to be identical to corresponding cable in 0.53 μm modulator (95.3 cm).

(2) Before connecting cable, remove top from AEC module "A" and connect a 50Ω scope monitor to the gate output test point (OSSM connector on circuit board). The gate is biased on when the drive is not connected, therefore, the detected pulse train will appear at the gate output.

(3) Line up a pulse on a scope graticule as a timing reference and connect the drive cable. A small differentiated portion of the drive signal

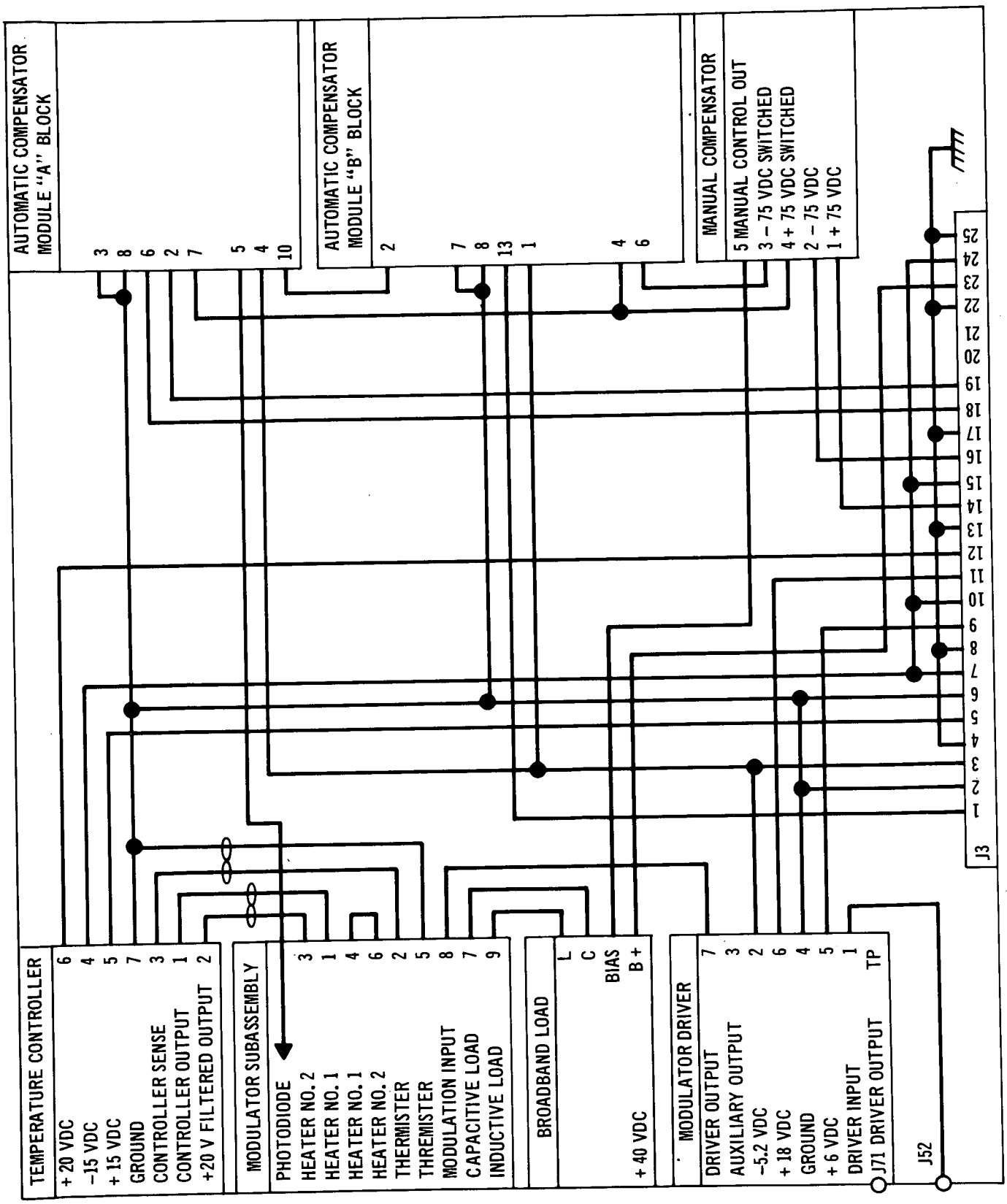


FIGURE 4–3 1.06μM MODULATOR WIRING DIAGRAM WITHOUT AUTOMATIC ELECTRONIC COMPENSATION

TABLE 9

1.06 μm MODULATOR REWIRING

FOR

AUTOMATIC ELECTRONIC COMPENSATOR

Remove wires from the:

Power Connector - J3-Pin 14	to	Manual Compensator - J1
Power Connector - J3-Pin 16	to	Manual Compensator - J2
Broadband Load - Bias	to	Manual Compensator - J5

Add wires from the:

Power Connector - J3-Pin 14	to	AEC Module "B"	- J9
Power Connector - J3-Pin 16	to	AEC Module "B"	- J5
Temperature Controller - J5	to	Manual Compensator	- J1
Temperature Controller - J4	to	Manual Compensator	- J2
AEC Module "B" - J10	to	Manual Compensator	- J5
Broadband Load - Bias	to	AEC Module "B"	- J12
Modulator Driver - J3	to	AEC Module "A"	- J1

will appear at the test point. The spikes representing the transitions on the drive code should be centered on the detected pulses. If not adjust the drive cable length accordingly and repeat.

4.4 SIGNAL PROCESSING ELECTRONICS OPERATING INSTRUCTIONS.

A photograph of the signal processing electronics and its associated power supply is given on Figure 1-3. All of the dc voltage necessary to operate the signal processing electronics are supplied by this power supply. The turn on procedure for applying power to the system is to connect the power supply cable to the electronics package, plug the power supply into a 110 volt ac outlet and turn the power switch "ON."

As mentioned in Section 3.3, the signal processing electronics consist of two independent digital data sources, the PN generator and the analog to digital encoding electronics. The operating instructions for each of these data sources are discussed in the following sections.

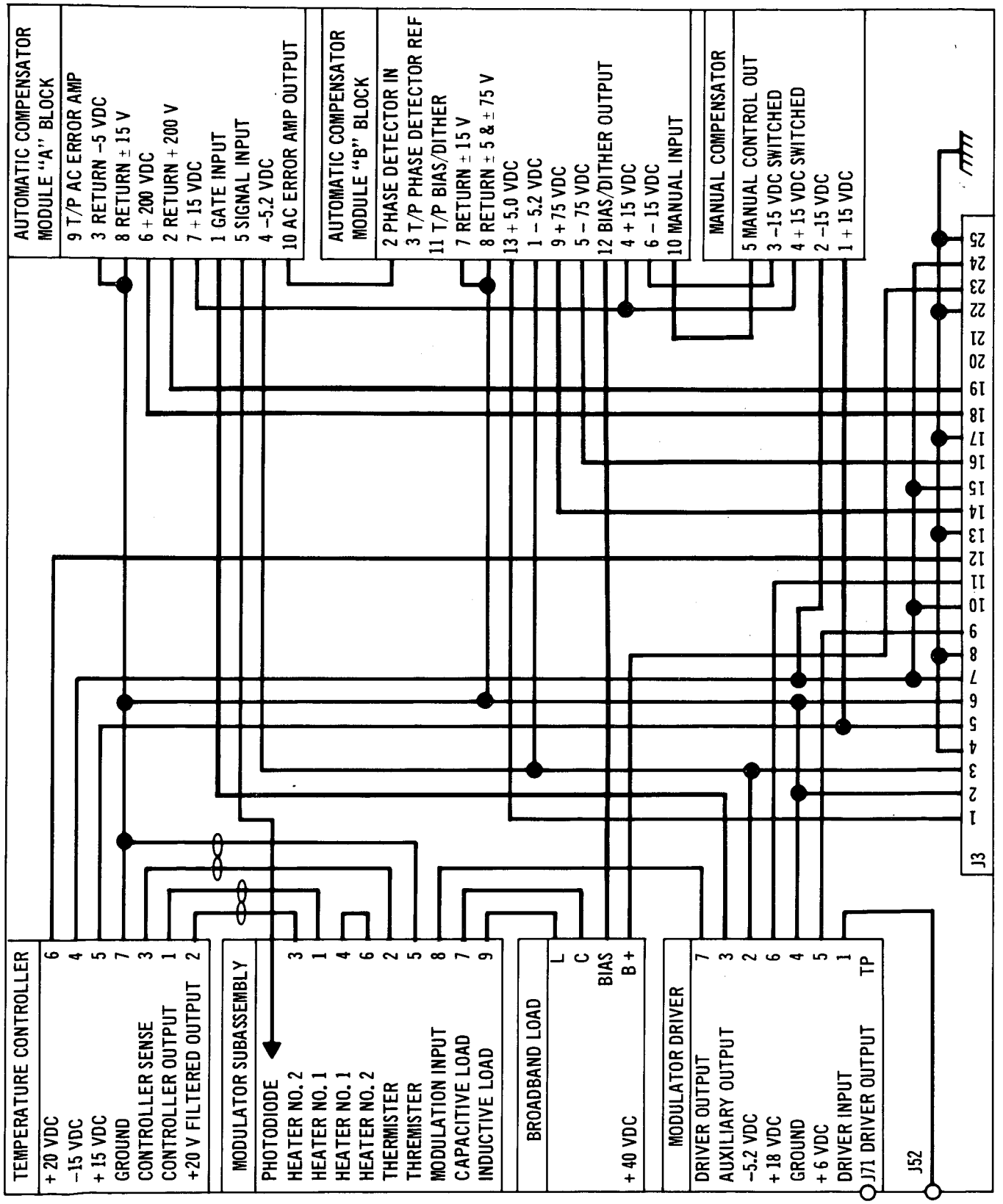


FIGURE 4–4 1.06μM MODULATOR WIRING DIAGRAM WITH AUTOMATIC ELECTRONIC COMPENSATION

4.4.1 PN Generator

Figure 4-5 is a functional diagram of the PN generator. The PN generator is designed to operate at 400 Mbps for 5, 6, 7, 9, 10, 11 and 15 stage codes. It will also operate as a 6 stage generator at 200 Mbps and 300 Mbps. Table 10 gives the proper cable lengths to be connected to the delay terminals for various modes of operation. When the mode of operation is decided upon, one need only refer to Table 10, obtain the correct cable lengths (each cable furnished with the generator has a tag indicating its length) and install them in the proper delay positions which are marked on the generator. Power need not be removed when changing cables. The generator is now ready for operation. The system clock (customer furnished) should be a 1V pp sinewave with a frequency equal to that of the bit rate to which the generator is set. The system clock should be capable of driving 50 ohms to ground. This clock signal should be verified on a scope with a 50 ohm load prior to connecting it to the generator. If the clock signal differs from the nominal by ± 0.2 volts improper operation may result. If it exceeds 2V pp circuit damage could occur. The P_N and P_N' outputs both give the same PN sequence but the P_N' output is delayed by some number of bits depending on the operating mode. These outputs have typical MECL levels and are capable of driving 50 ohm loads connected directly to ground. Either one of these outputs can be used to drive the modulator driver directly, while the other is used as a scope monitor point. The scope sync output is a filtered version of the PN sequence. The lowest frequency present in a PN sequence must be used for proper scope sync. By passing the PN sequence through a low-pass filter the low frequencies are accentuated and the scope sync circuitry has a much easier task in finding the lowest frequency. The scope sync output is also capable of driving 50 ohms to ground. The sync output has a 1 volt dc offset and thus may require a dc block for some scope sync inputs.

CAUTION - DO NOT REMOVE POWER FROM THE PN GENERATOR WHILE IT IS CONNECTED TO THE MODULATOR DRIVER, AS THIS BIASES THE DRIVER ON STEADY STATE. THE EXCESSIVE POWER DISSIPATION IN THIS STEADY STATE ON CONDITION CAN DAMAGE OR DEGRADE THE DRIVER OUTPUT STAGE.

4.4.2 Analog/Digital Encoding Electronics

Figure 4-6 is a block diagram of the analog-to-digital encoding electronics. There are only four connectors used to interface this subsystem to

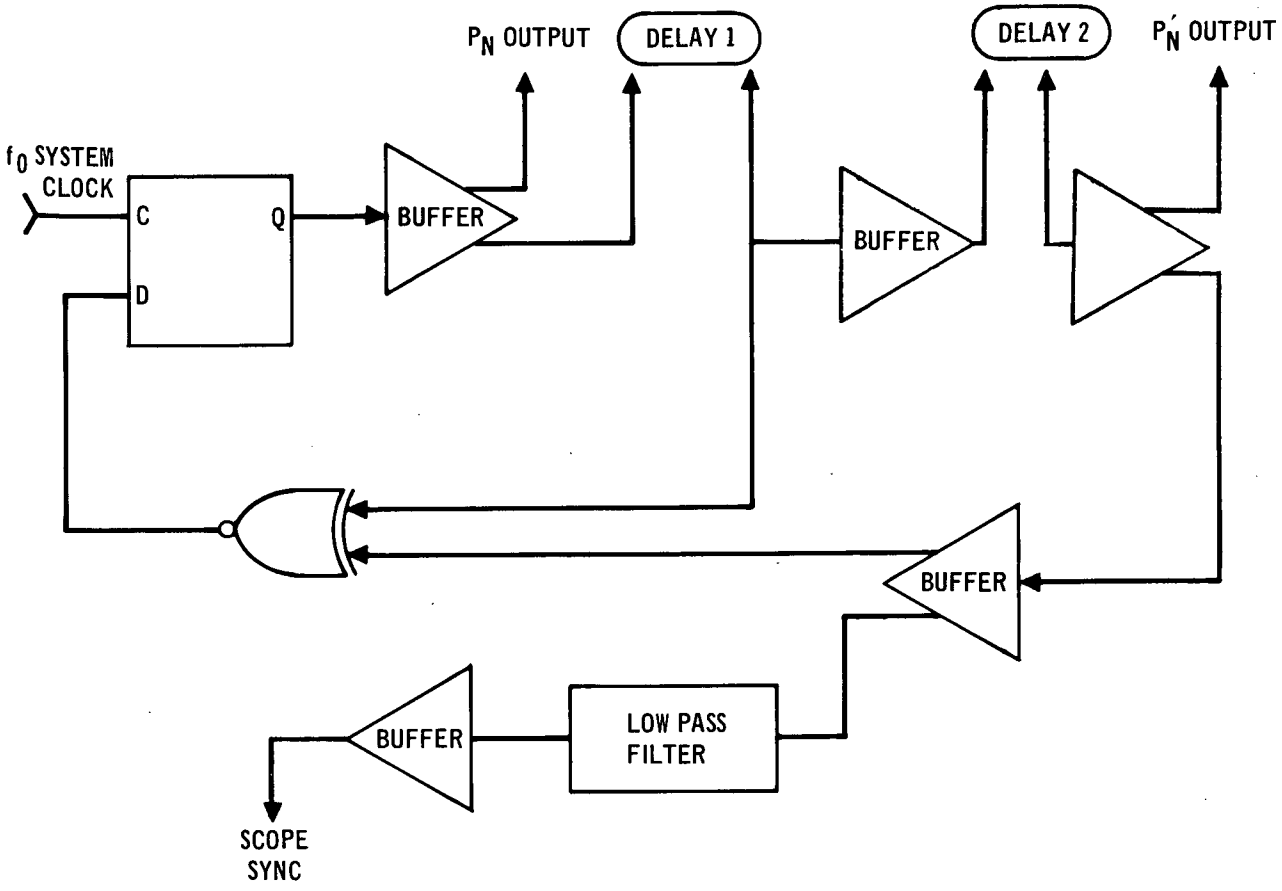


FIGURE 4–5 FUNCTIONAL DIAGRAM OF PN GENERATOR

TABLE 10
PN GENERATOR CABLE DELAY LENGTHS

DATA RATE	NUMBER OF STAGES	CODE LENGTH	DELAY 1 (IN.)	DELAY 2 (IN.)
400 MBPS	5	31	4	21
400 MBPS	6	63	42	4
400 MBPS	7	127	60	2
400 MBPS	9	511	44	55
400 MBPS	10	1,023	79	42
400 MBPS	11	2,047	121	21
400 MBPS	15	32,767	219	4
300 MBPS	6	63	71	8
200 MBPS	6	63	128	21

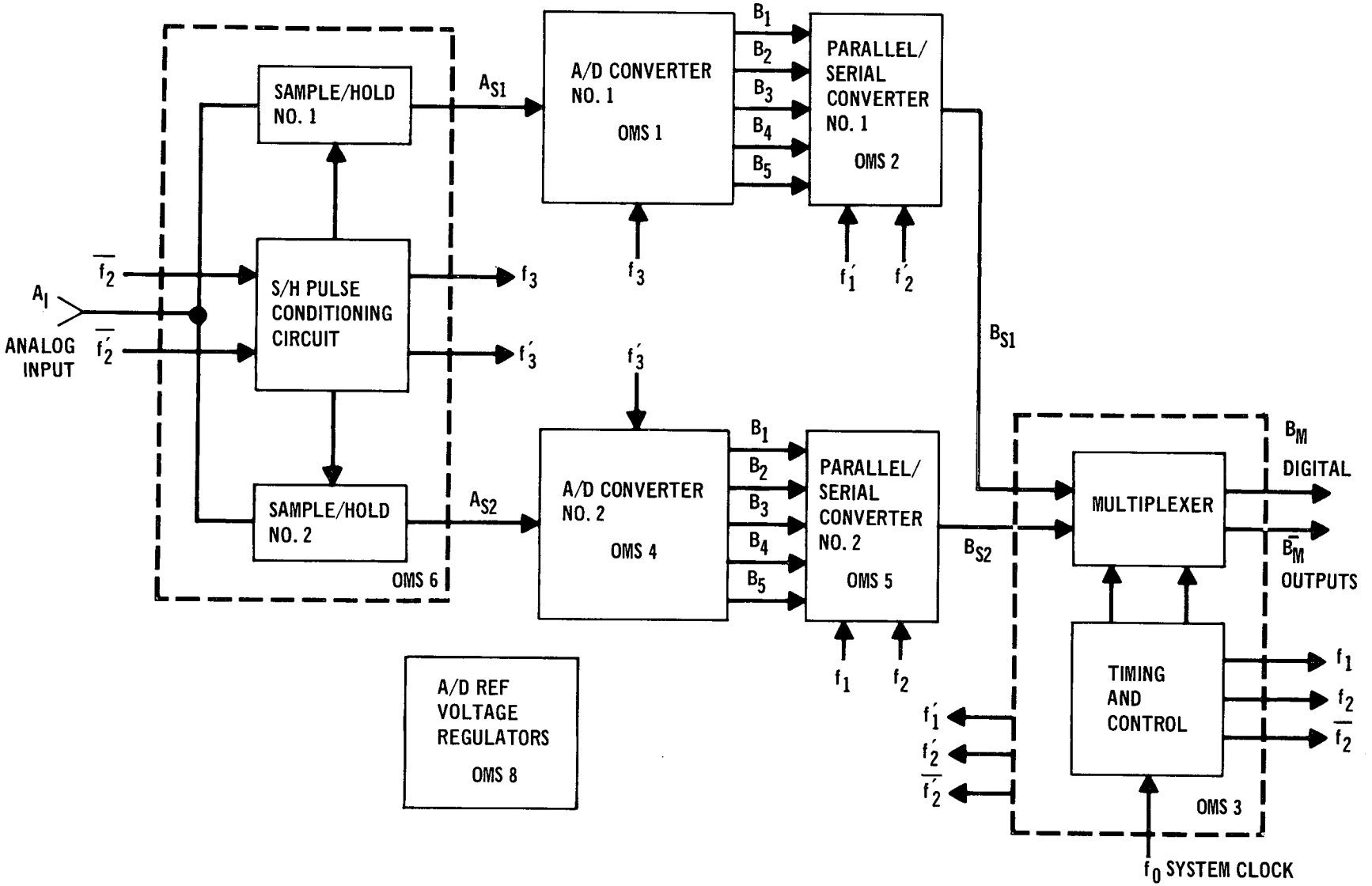


FIGURE 4–6 BLOCK DIAGRAM OF ANALOG-TO-DIGITAL ENCODING ELECTRONICS

the rest of the overall system. These connectors are f_o, A_i, B_m, and $\overline{B_m}$. The system clock is brought into the unit at f_o. This clock should be a 3V pp sinewave capable of driving 50 ohms to ground. The analog data to be digitized is brought into the unit at A_i. The maximum amplitude limitations on this input are $\pm$0.75V. The bandwidth limitations on this input are dc to $f_o/12.5$. B_m and $\overline{B_m}$ are the serial digital outputs and are logical compliments of each other. These outputs have typical MECL levels and are capable of driving 50 ohms to ground. Either can be connected to the modulator driver while the other is used as a monitor point. Before attempting operation of the encoder all of the intersystem connections shown in Figure 4-6 should be made with the proper cables that are supplied with the system. Most of these cable lengths are critical and care should be taken for their proper installation. CAUTION - THE ENCODING ELECTRONICS SHOULD NEVER BE CONNECTED TO THE MODULATOR DRIVER IF IT IS PROCESSING A STEADY STATE ANALOG SIGNAL WHICH RESULTS IN A LOGIC ONE DUTY CYCLE GREATER THAN 70%. THIS IS NOT CONSIDERED A NORMAL SYSTEM OPERATION CONDITION. IT CAUSES EXCESSIVE POWER DISSIPATION IN THE MODULATOR DRIVER WHICH CAN DAMAGE OR SHORTEN THE LIFE OF THE POWER STAGE. SIMILARLY POWER SHOULD NEVER BE REMOVED FROM THE ENCODING ELECTRONICS WHILE CONNECTED TO THE MODULATOR DRIVER. THE RESISTANCE TO GROUND OF THE SIGNAL SOURCE WILL BIAS THE DRIVER INTO AN ALL 1'S CONDITION.

NOTE: (PAGE 56 IS BLANK)

5. PERFORMANCE TESTS

All of the hardware delivered on this program has been subjected to a variety of tests at the module level, unit assembly level and integrated subsystem level. The results of typical tests are documented in this section.

5.1 0.53 μm MODULATOR TESTS

5.1.1 Modulator Unit Tests

The assembled modulator unit was tested to verify proper functional operation with optical input power levels of 0.5 - 10 mW. The unit was tested with the signal processing electronics data sources. Pseudorandom code sequences from 63 bits to 32,767 bits were used to verify that no abnormal code sensitivity existed. The encoding electronics were used to generate codes with a 30-70% duty cycle to verify proper modulator operation under this condition. Automatic electronic compensation over several fringes was demonstrated using an external Babinet compensator.

The 0.53 μm modulator was optically evaluated for transmission and for extinction ratio. Since it was very difficult to decrease the instability of the laser to less than a few percent, a differential technique was used for the transmission measurement. Figure 5-1 shows a schematic of the setup used for this measurement. A reference beam was split off the signal and fed into a power meter which had the same linearity characteristics as the power meter used after the modulator. The two signals were adjusted (without the modulator) to give the same amplitude trace on a dual channel oscilloscope. The differential of the signals was then displayed on an expanded scale. When both signals increased or decreased simultaneously due to the laser power fluctuations the trace remained stationary. The modulator was then inserted in the beam and the attentuator adjusted to regain equal amplitudes again. The amount of added attenuation was equal to the modulator transmission loss. Better than one percent accuracy was achievable with this technique with a laser that fluctuated $\pm$ 10% or more. This measurement technique showed that the 0.53 μm modulator had better than 90% transmission for a single pass of the light through the modulator. The double pass transmission was 72% with all the optics in place and the modulator adjusted for optimum alignment.

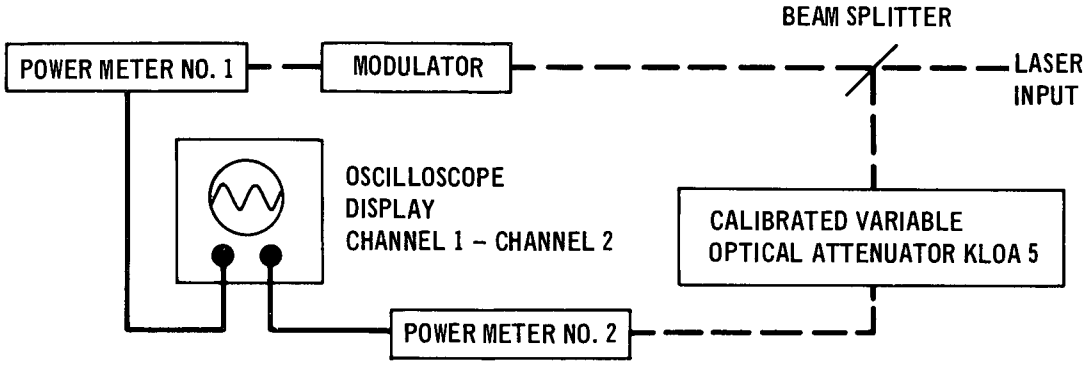
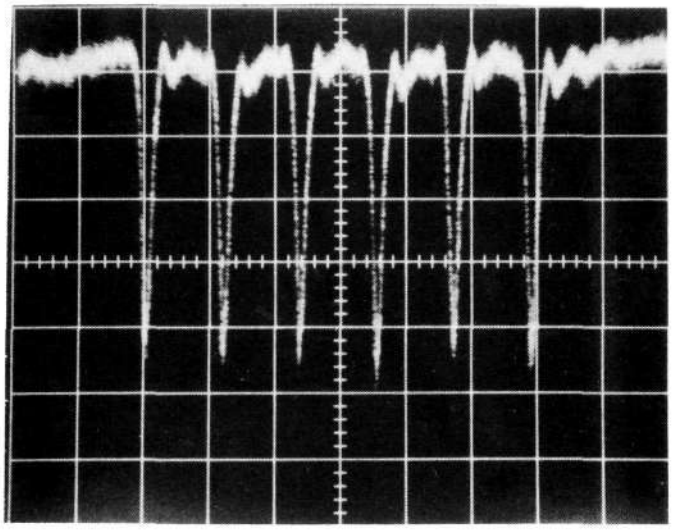


FIGURE 5-1 SETUP FOR MODULATOR TRANSMISSION MEASUREMENTS

The static extinction ratio was measured using a single power meter rather than a differential technique because the calibration accuracy of the two power meters was not adequate over the widely different power levels, the single pass static extinction ratio was better than 100:1 and the double pass static extinction ratio was better than 50:1.

The dynamic extinction ratio measurements are made with the modulator operating with a pseudorandom code input. A high speed detector with sufficient bandwidth to follow the laser pulses is required for accurate measurements of the dynamic operating characteristics of the modulator. The oscilloscope traces of Figures 5-2 and 5-3 were taken using a TIXL55 detector diode. Figure 5-2 shows the optical response to selected areas of a pulse train made up of sixty-three bit words. Figure 5-3 shows the worst case bits in the code (smallest "1" and largest "0"). The ratio of these two is the worst case dynamic extinction ratio. There is sufficient noise present in the trace that there is a considerable uncertainty as to the exact height of the two bits. Detector diode nonlinearity and laser amplitude fluctuations also contribute to the uncertainty in this measurement. The best estimate of the worst case dynamic extinction ratio from these photographs is about 15:1. Informal tests run at other times have demonstrated a better dynamic extinction ratio than this.

Modulator operation with longer pseudorandom sequences is demonstrated by the waveforms in Figure 5-4 . This figure shows the driver output test point and the corresponding modulator optical output for positions of a 1023 bit pseudorandom code. The pictures denote operation with repetitive ones, repetitive zeros, and alternate ones and zeros. The longer PN codes did not cause any apparent increase in intersymbol interference.



VERTICAL:
5 MV/DIV

HORIZONTAL:
2 NS/DIV

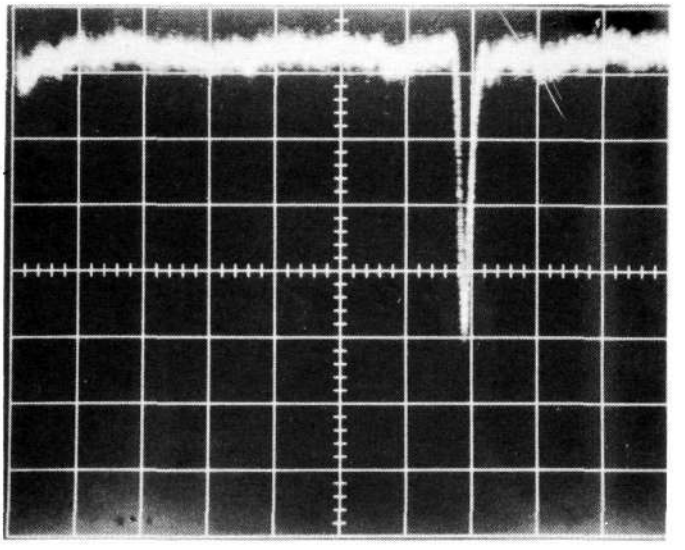
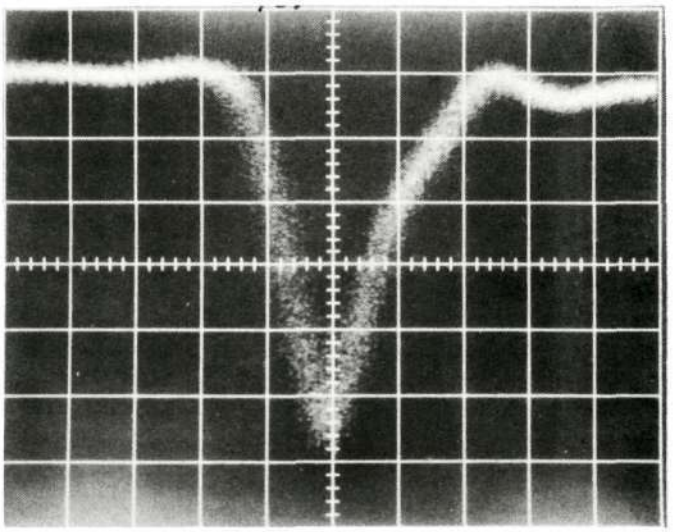
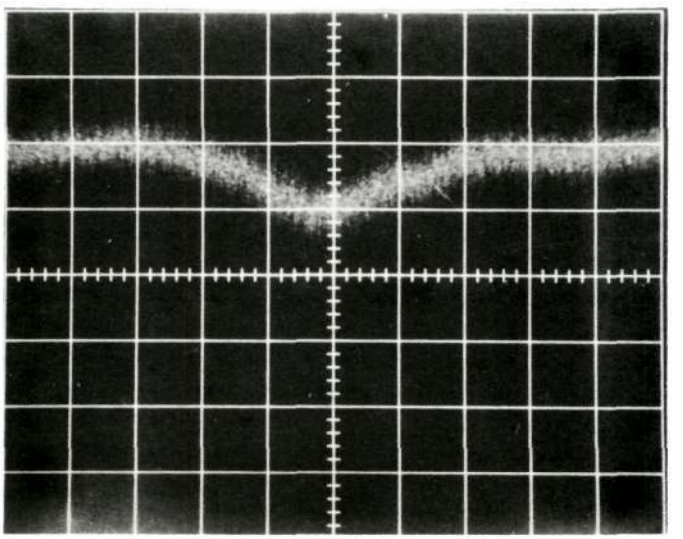


FIGURE 5–2 OPTICAL RESPONSE OF 0.53 μ M MODULATOR WITH 63 BIT CODE



VERTICAL:
5 MV/DIV
HORIZONTAL:
200 PS/DIV

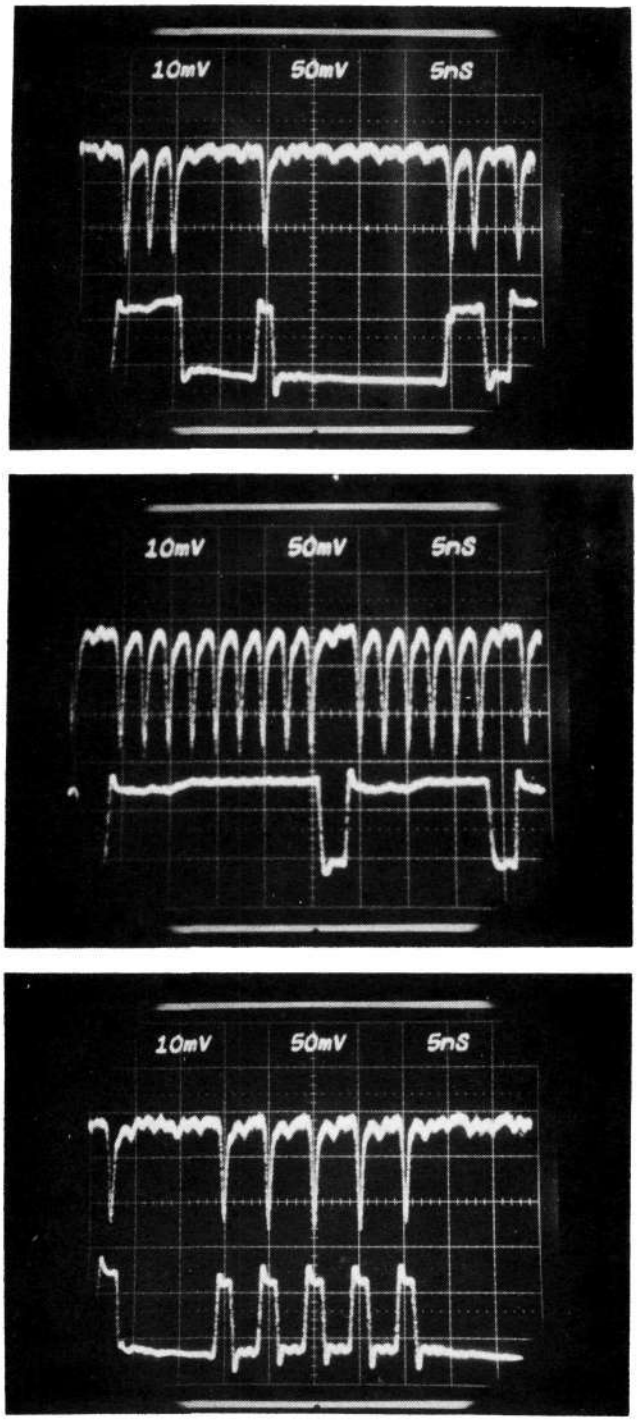
A) SMALLEST "1"



VERTICAL:
2 MV/DIV
HORIZONTAL:
200 PS/DIV

B) LARGEST "0"

FIGURE 5–3 WORST CASE BITS. 0.53μM MODULATION WITH 63 BIT CODE

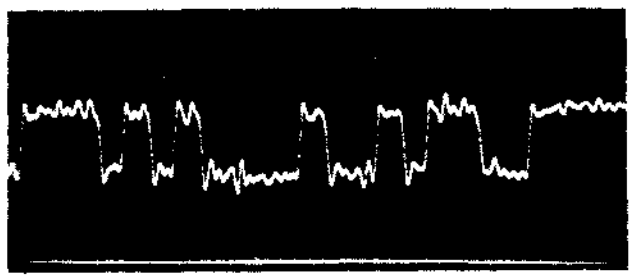


UPPER WAVEFORMS
OPTICAL OUTPUT 5 MV/CM
LOWER WAVEFORMS
DRIVER TP 50 MV/CM x 200 = 10 V/CM

FIGURE 5–4 0.53μM MODULATOR OPTICAL OUTPUT AND DRIVER TEST POINT SELECTED FROM A 1023 BIT PN SEQUENCE

5.1.2 Driver Tests

Bench tests were conducted on the modulator driver using a dummy 50 ohm load to insure that it supplied the correct switching voltage, level flatness, rise and fall times, and timing symmetry, Figure 5-5 shows the waveforms of a 500 Mbps, 31 bit PN generator which was used as a data source for the driver tests. Figure 5-6 shows the corresponding driver output using a x100, 5K ohm scope probe. The PN generator clock waveform is superimposed to show timing symmetry. Using the peak of the clock waveform as a timing



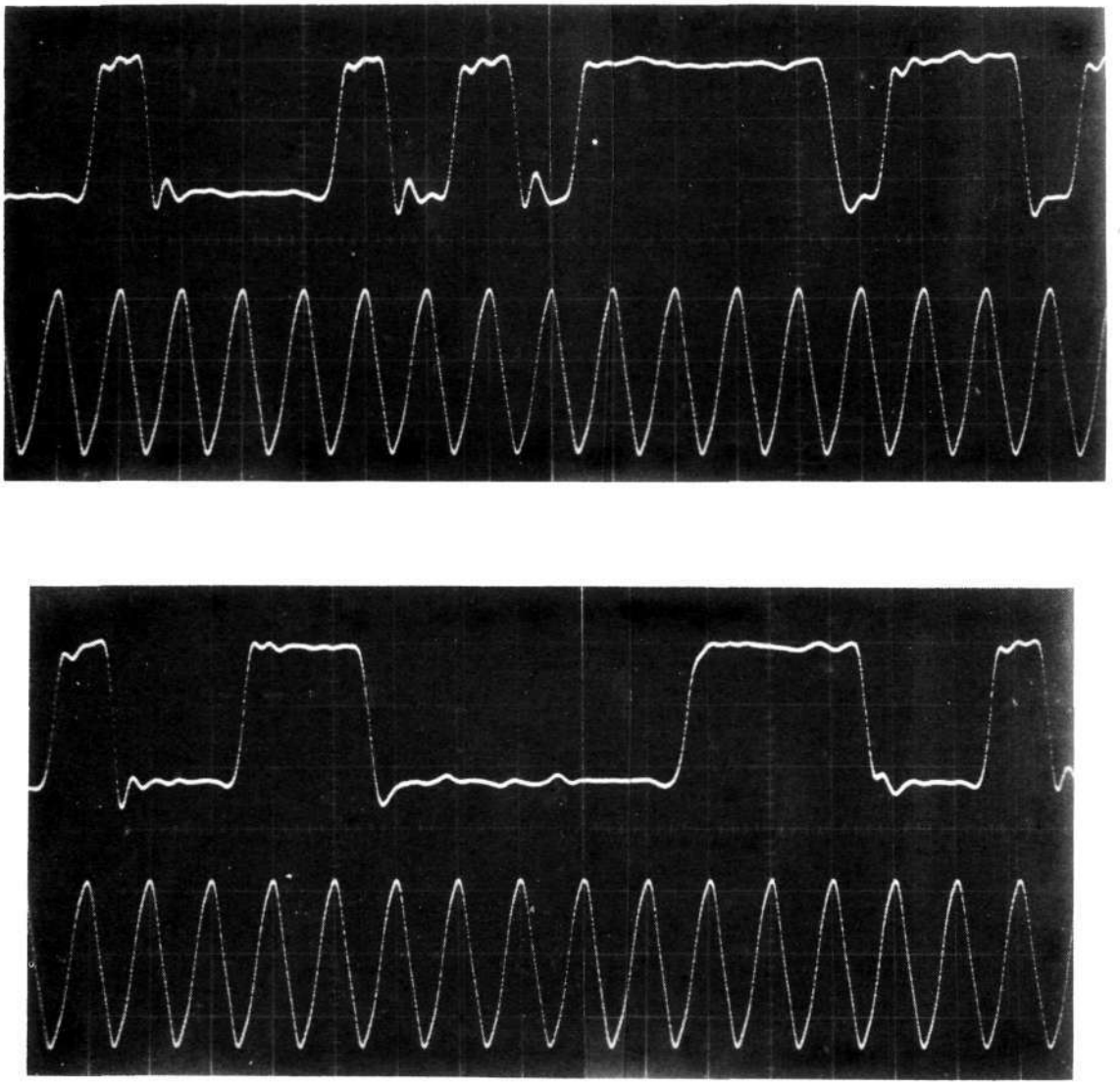
VERTICAL: 0.5 V/CM
HORIZONTAL: 5 NS/CM

FIGURE 5-5 TYPICAL MODULATOR DRIVER INPUT USED DURING TIMING BENCH TEST

mark it can be seen that all bits have reached their quiescent condition within the allotted time and that all transistions are less than 1ns. The nominal voltage swing is 22V pp which corresponds to the 0.4mm crystal switching voltage. The amplitude fluctuations on the top and bottom of the waveform are less than $\pm$ 6% ignoring the initial overshoots which are beyond the response of the matching network.

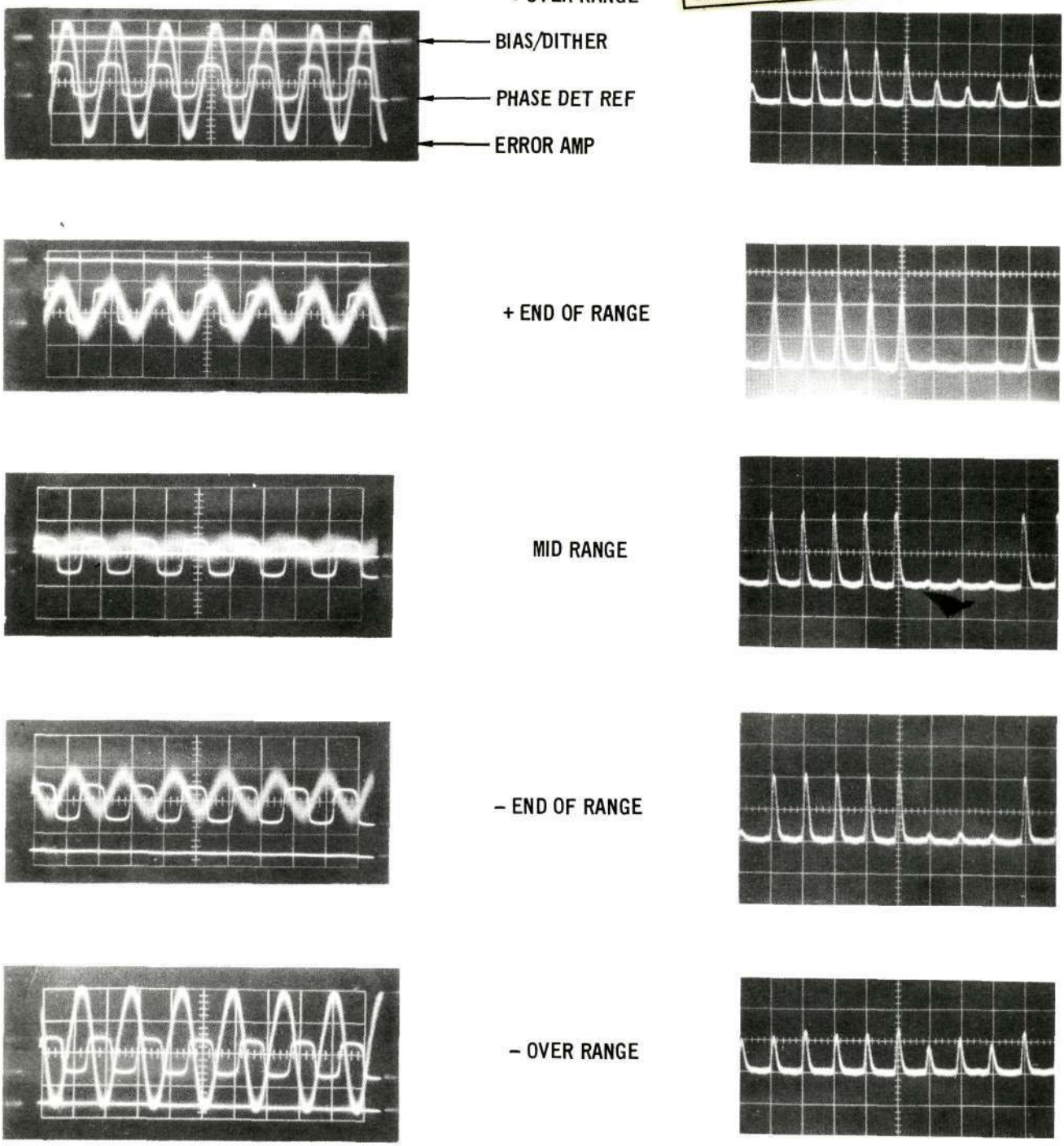
5.1.3 Automatic Electronic Compensator (AEC) Tests

The series of pictures in Figure 5-7 demonstrate AEC operation. The pictures on the left show the crystal bias signal from the AEC, the error signal, and the phase detector reference dither signal for several conditions. The photos on the right denote the optical output for each condition. The AEC can provide $\pm$75V bias correction (compared to 22V switching voltage) before the extinction ratio starts to degrade as shown on Figure 5-7.



VERTICAL:
DRIVER OUTPUT: 10 V/CM
CLOCK: 0.2 V/CM
HORIZONTAL: 2 NS/CM

FIGURE 5–6 0.53μM MODULATOR DRIVER OUTPUT VS PN CODE GENERATOR CLOCK
500 Mbps, 31 BIT PN SEQUENCE



BIAS/DITHER TP	50 V/CM
PHASE DET REF	1 V/CM
ERROR AMP	0.2 V/CM
TIME	5μS/CM

OPTICAL WAVE FORM 20 MV/CM
TIME 2 NS/CM

FIGURE 5–7 AUTOMATIC ELECTRONIC COMPENSATOR WAVEFORMS

Beyond this range the error signal increases and the optical zero's start increasing in amplitude. The bias error at the plus/minus ends of range points was 2V versus 1V at midrange for an optical input of 0.6mW, 50% duty cycle code, and 1% dither on the optical signal.

5.1.4 Temperature Controller Tests

Tests were also conducted on the temperature controller at the module level to demonstrate proper operation. The controller, which uses pulse width modulation to control the average heater current, was checked for correct frequency, waveform, sensitivity, and adjustment range. The test results are listed in Table 11.

TABLE 11

TEMPERATURE CONTROLLER TEST RESULTS

Frequency	5.8 kHz
Rise Time	< 1.0 μs
Fall Time	< 0.5 μs
On Level	0.9V
Sensitivity	9.1% duty cycle change/ohm input change 1.2 watts/ohm input change with 20V heater supply 5.7 watts/°C for 3%/°C thermistor which has a value of 160 ohms at 150°C.
Adjustment Range	126-222 ohms for 135°C-160°C.

5.1.5 Modulator Power Supply Tests

The regulated supplies were each checked for adjustment range, current limit, short circuit current, ac ripple, and the change in voltage from no load to 90% full load. The adjustment range tests were made with no load. The ac ripple was taken with 90% of the current limit load. All tests were taken using the lab bench ac power (120 to 125 Vac 60 Hz). Table 12 contains the recorded data.

TABLE 12

MODULATOR POWER SUPPLY TEST DATA

Regulator	Adjustment Range		Current	Short Circuit	90% load	90% load
Volts	Low Volts	High Volts	Limit mA	Current mA	AC Ripple mV	V Volts
+5.0	3.2	7.8	220	225	<1	0.04
-5.2	<-0.1	-8.5	580	600	1	0.07
+15.0	0.8	19.8	220	225	<1	0.06
-15.2	<-0.1	-19.8	220	225	<1	0.02
+6/19	5.0	24.0	395	405	<1	0.07
+18/30	15.0	33.0	490	500	1	0.05
+40	26.0	44.0	650	50	10	0.15
+75	-	78.9	3.8	24.0	120	1.66
-75	-	-79.9	3.75	24.6	120	1.52
5/24 OP	5.0	37.0	810	125	10	0.11
5/24 MED	5.0	15.0				
5/24 LOW	5.0	15.0				

The 40 volt regulator current limit can be adjusted between 1 and 1.2 amps. Short circuit current changes as the limit is adjusted.

5.2 1.06 μm MODULATOR TESTS.

5.2.1 Modulator Unit Tests

This modulator unit was also subjected to a variety of functional tests to demonstrate its performance. All tests were performed using the manual compensator since the automatic compensator was installed in the 0.53 μm modulator. Dynamic tests included operation with pseudorandom code sequences from 31 to 32,767 bits long. The modulator performance was not degraded for the longer sequence lengths.

The optical tests for 1.06 μm modulator were performed in the same manner as those of the 0.53 μm unit. The static transmission and extinction ratio were not quite as high as for the 0.53 μm unit because the crystals are 0.3mm aperture. It was not possible to increase the crystal aperture to improve the transmission because a proportional increase in switching voltage would be required. The single pass transmission was about 80% and the single pass

static extinction ratio was about 90:1. The double pass transmission exceeded 50% and the double pass static extinction ratio was about 30:1. Figure 5-8 shows the optical response for several interesting sections of a 1023 bit code. The dynamic extinction ratio of all codes used was about 13:1 for the worst bits. Our detectors are not quite as fast at 1.06 μm as at 0.53 μm so the optical response was not quite as clean as for the 0.53 μm modulator. Figure 5-8 also shows the output of the driver test point aligned with the optical signal.

5.2.2 Driver Tests

This driver was also tested to verify the output level, rise and fall times, and timing symmetry. Figure 5-9 shows the driver output waveform (monitored with a X100 probe) into a 50 ohm load. Using the clock peaks as a timing reference it can be seen that all bits have completed their transitions within the required time. The rise/fall times are less than 1 ns and the nominal voltage swing is 32V pp. The top of the waveform has ±6% variations while the bottom has ±9% variations ignoring the initial overshoot. Figure 5-10 shows two photos which denote the driver output as viewed at the output test point and with a X100 probe. The waveforms are shown for the purpose of comparison only. It should be noted that neither represents the actual output waveform with perfect fidelity because of parasitics.

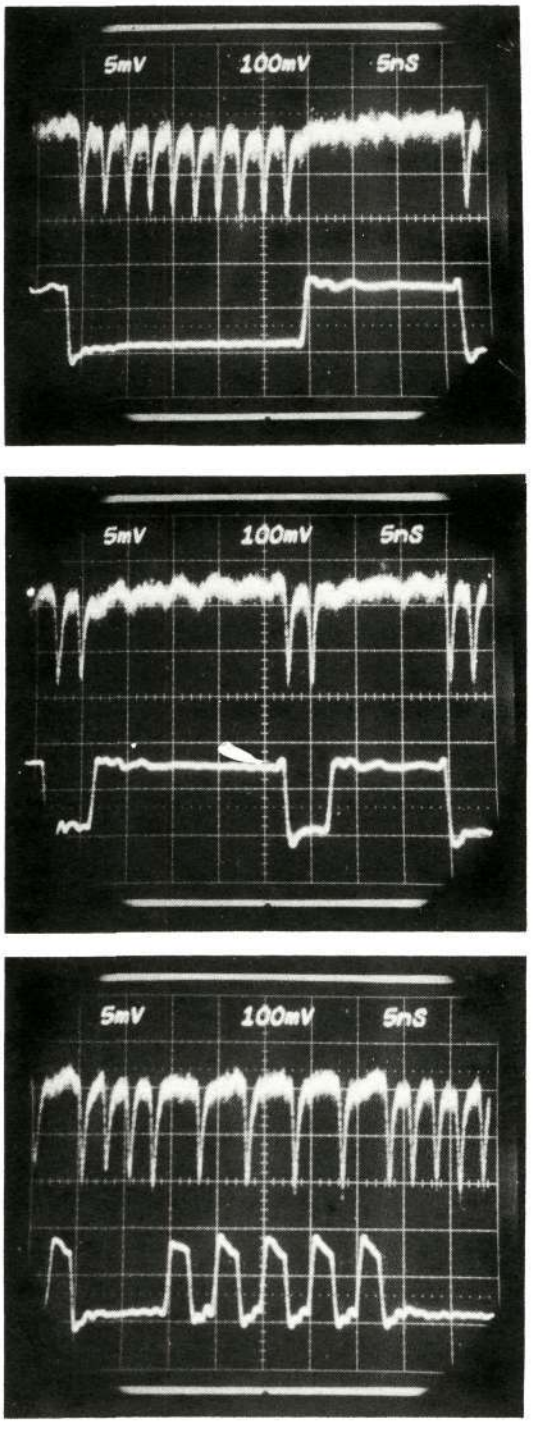
5.2.3 Other 1.06 μm Modulator Tests

The temperature control tests for this unit were the same as described in Section 5.1.4. The test results for the AEC and modulator power supply also apply for 1.06 μm operation since the same equipment is used for 0.53 μm or 1.06 μm operation.

5.3 SIGNAL PROCESSING ELECTRONICS TESTS.

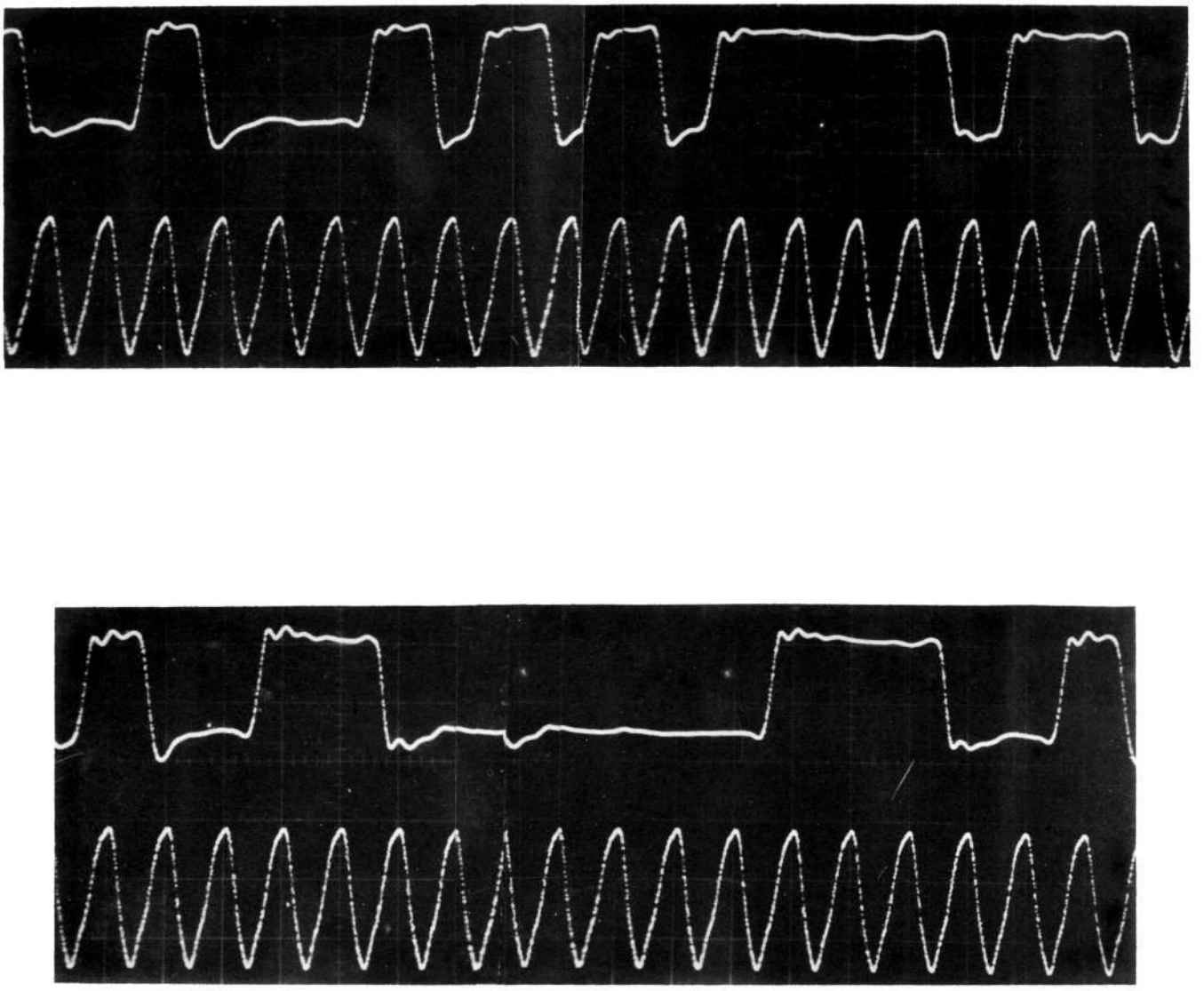
5.3.1 PN Generator

The PN generator was tested for proper operation in every configuration shown in Table 10 of Section 4.4.1. In each case the clock amplitude, power supply voltage, and clock frequency were varied to the point where the output PN code waveform degraded in amplitude or timing symmetry. For all sequence lengths the clock amplitude could be varied from 800 mV pp - 1200 mV pp, the



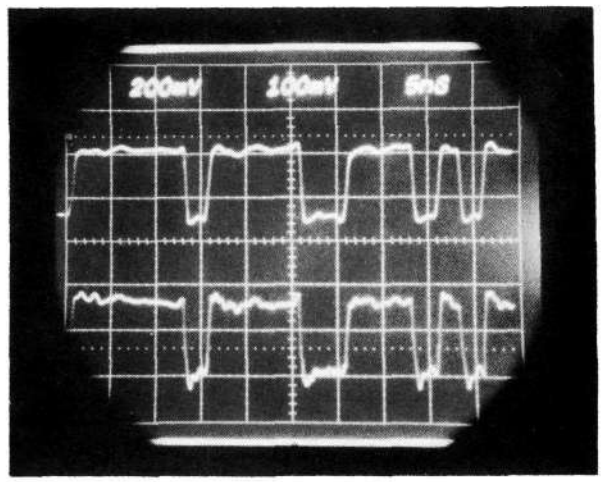
UPPER WAVEFORMS: OPTICAL OUTPUT, 5 MV/CM
LOWER WAVEFORMS: DRIVER TEST POINT, 20 V/CM

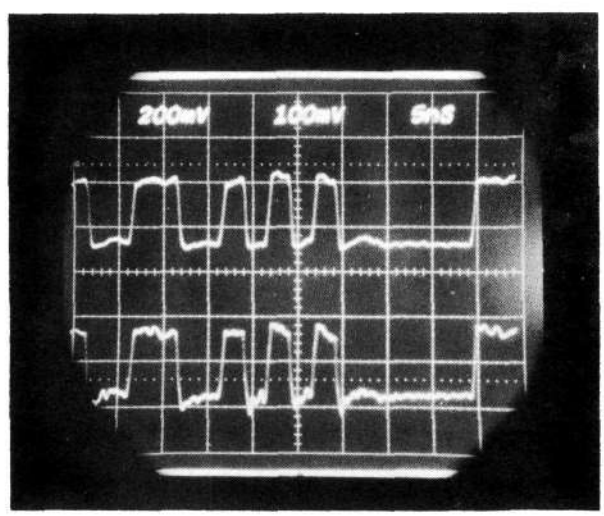
FIGURE 5–8 1.06μM MODULATOR OPTICAL OUTPUT AND DRIVER TEST POINT. SELECTED FROM A 1023 BIT PN SEQUENCE



DRIVER OUTPUT	20 V/CM
CLOCK	0.2 V/CM
TIME	2 NS/CM

FIGURE 5–9 1.06 μM MODULATOR DRIVER OUTPUT VS PN CODE GENERATOR CLOCK
500 Mbps, 31 Bit PN Sequence





TOP WAVEFORMS
DRIVER PROBED OUTPUT
200 MV/CM x 100 = 20 V/CM
BOTTOM WAVEFORMS
100 MV/CM x 200 = 20 V/CM
5 NS/CM

FIGURE 5–10 COMPARISON OF 1.06μM DRIVER TEST POINT VS PROBED OUTPUT

power supply voltage could be varied from -4.9V to -5.4V and the clock frequency could be adjusted ±5 MHz from the center frequency before degradation occurred.

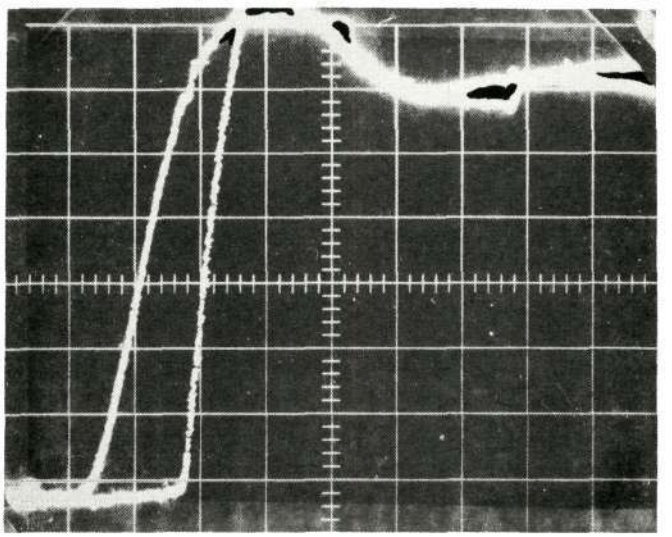
5.3.2 Dual Sample/Hold

As shown on the functional diagram of Figure 3-13, this module contains two identical sample/hold circuits which are strobed out of phase with respect to each other. The tests and results mentioned below apply to both sample/hold circuits in the dual module.

Each sample/hold circuit is capable of slewing the range of the input analog signal during the S/H strobe period. The S/H strobe period is approximately 10 ns. The unity gain input buffers actually have gains of 0.95. Thus, for analog signals with a range of ±0.75 volts the sampling bridge need handle only ±0.7125 volts. Figure 5-11 shows two photographs that illustrate the slewing capability of the sampling bridge for positive and negative going input changes. The held voltage sample after slewing, 1.425 volts, is identical to the input voltage at the time of bridge turn off within the 3% accuracy of the oscilloscope presentation. The sampling bridge post amplifier is capable of slewing 4.14 volts in the sampling strobe interval. Figure 5-12 is a photograph showing the sampling bridge output superimposed on the post amplifier output. The vertical scale of the oscilloscope was in an uncalibrated position for the postamplifier input in order to obtain this relative comparison.

The other significant performance parameters which were measured for each sample/hold over the entire operating range were aperture error, holding droop, overall gain, and linearity. The results of the tests were:

Aperture error	< 100 ps
Holding Droop	< 1%
Overall GAin	2.69
Linearity error	< ± 1.3%



VERTICAL:
200 MV/DIV

HORIZONTAL:
10 NSEC/DIV

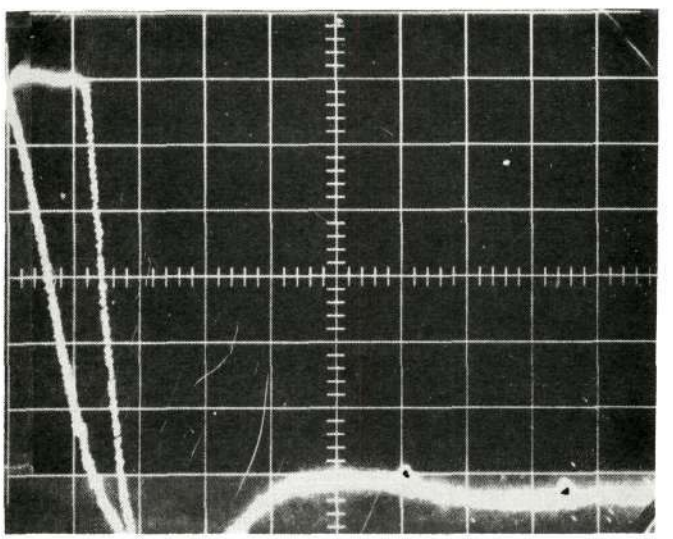
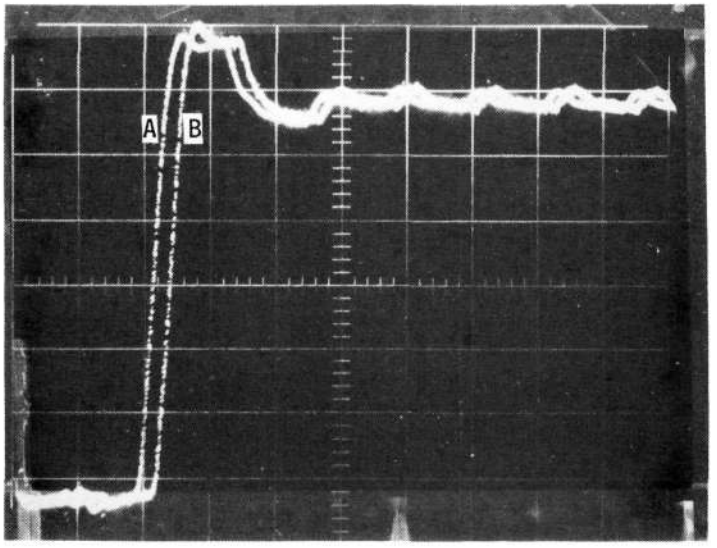


FIGURE 5–11 MAXIMUM SLEWING TESTS ON SAMPLE/HOLD CIRCUIT



VERT:
a) UNCALIBRATED
b) 200 MV/DIV
HOR: 200 NS/DIV

FIGURE 5-12 RELATIVE COMPARISON OF BRIDGE OUTPUT AND POSTAMPLIFIER OUTPUT

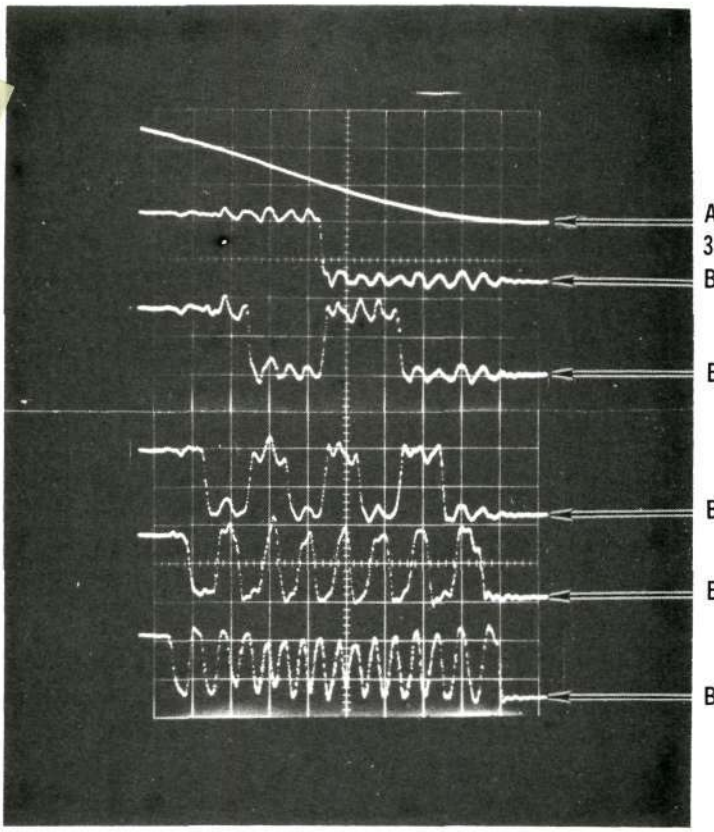
5.3.3 Analog/Digital Converters

Figure 5-13 shows the results of the ripple through test performed on the A/D converter. This test illustrated the maximum conversion speed of the A/D converter. For this test, a sinewave was used as an input signal to the converter. The frequency of the sinewave input was increased to the point where the LSB was just making full transitions. The time between transitions is a good indication of the maximum conversion speed. From Figure 5-13, the maximum conversion speed is seen to be approximately 7 nanoseconds.

The results of the dc linearity test on both A/D converters are shown in Table 13 and 14.

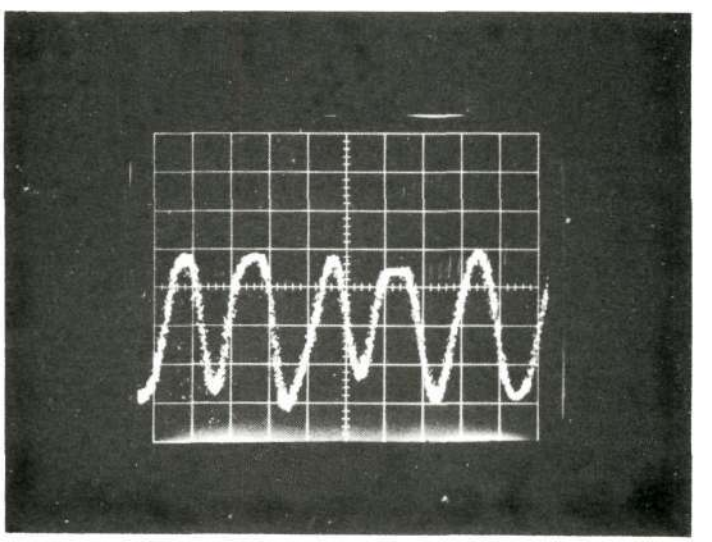
Both A/D converters were connected to the dual sample hold module and the combined units were tested for linearity and relative tracking ability. Table 15 gives the results of this test in tabular form and Figure 5-14 shows the results in graphical form.

A test to show dynamic performance of the sample/hold and A/D converter was performed by placing a ramp waveform into the sample/hold and observing the A/D output bits. The slewing rate of the ramp was adjusted such that, for each sample converted, the amplitude of the ramp increased by one quantizing level. The results of this test are shown in Figure 5-15 .



VERTICAL:
0.2 V/DIV

HORIZONTAL:
5 NSEC/DIV



"WORST CASE"
SWITCHING
OF LSB

FIGURE 5–13 RIPPLE TEST ON A/D CONVERTER

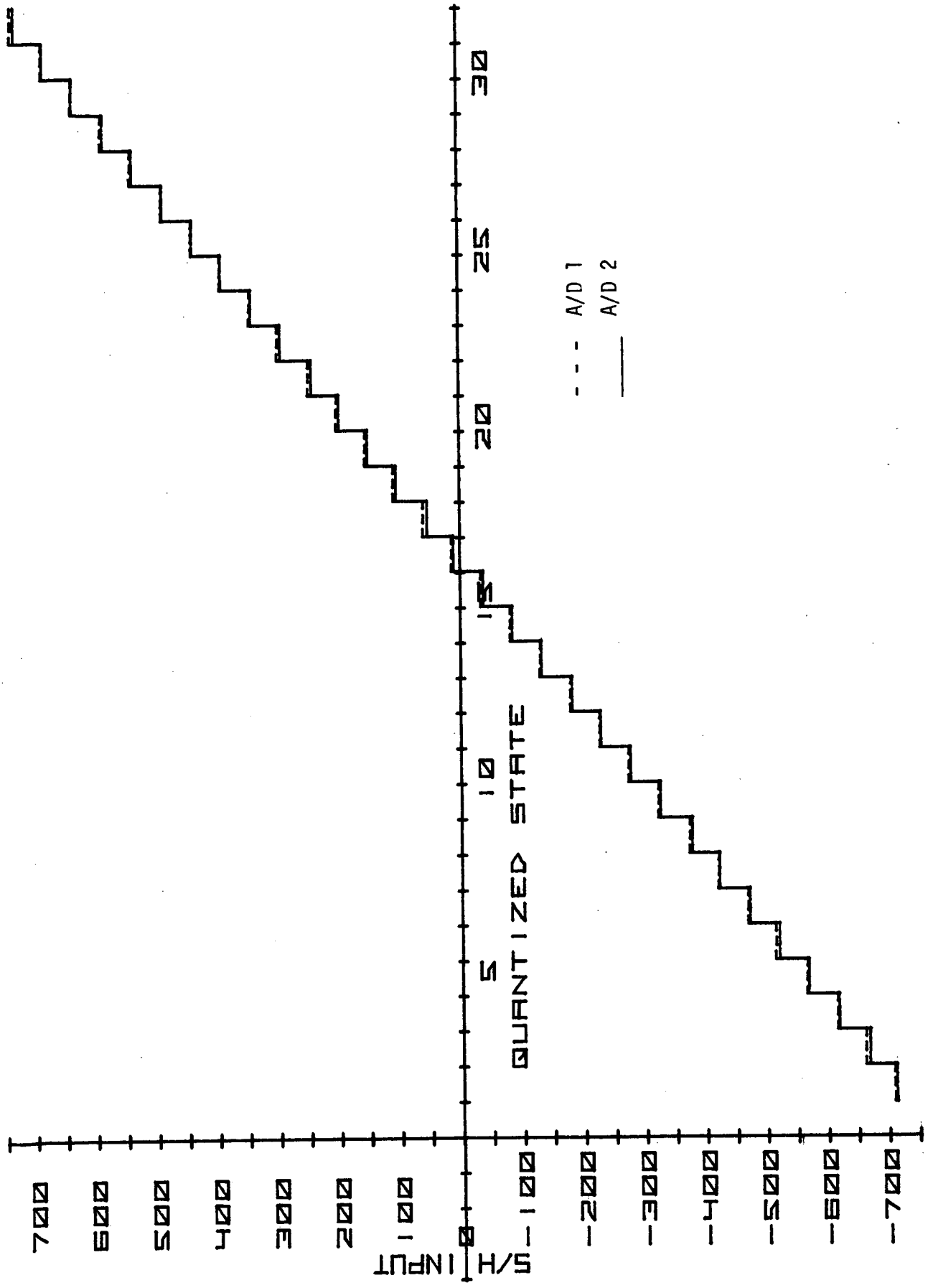


FIGURE 5–14 A/D CONVERTER RELATIVE TRACKING AND LINEARITY RESULTS

TABLE 13

DC LINEARITY TEST RESULTS A/D #1

BINARY OUTPUT	SWITCHING POINT	BIT SIZE (mV)	SWITCHING POINT	BIT SIZE (mV)	HYSTERESIS (mV)
00000			-2.499	160	31
00001	-2.468		-2.339	160	38
00010	-2.301	167	-2.179	177	35
00011	-2.144	157	-2.002	155	35
00100	-1.967	177	-1.847	160	37
00101	-1.810	157	-1.687	172	39
00110	-1.648	162	-1.515	159	39
00111	-1.476	172	-1.356	183	38
01000	-1.318	158	-1.173	162	39
01001	-1.134	184	-1.011	167	38
01010	-.973	161	-.844	163	38
01011	-.806	167	-.681	162	31
01100	-.645	161	-.519	164	37
01101	-.482	163	-.355	155	35
01110	-.320	162	-.200	165	37
01111	-.163	157	-.035	149	38
10000	+.003	166	.114	172	36
10001	+.150	147	.286	160	35
10010	+.321	171	.446	163	36
10011	+.482	161	.609	167	38
10100	+.647	165	.776	160	36
10101	+.812	165	.936	171	35
10110	+.971	159	1.107	164	33
10111	+1.140	169	1.271	177	33
11000	+1.304	164	1.448	154	33
11001	+1.481	177	1.602	163	30
11010	+1.632	151	1.765	173	33
11011	+1.798	166	1.938	161	32
11100	+1.970	172	2.099	165	34
11101	+2.133	163	2.264	180	33
11110	+2.297	164	2.444		34
11111	+2.478	181			

TABLE 14

DC LINEARITY TEST RESULTS A/D #2

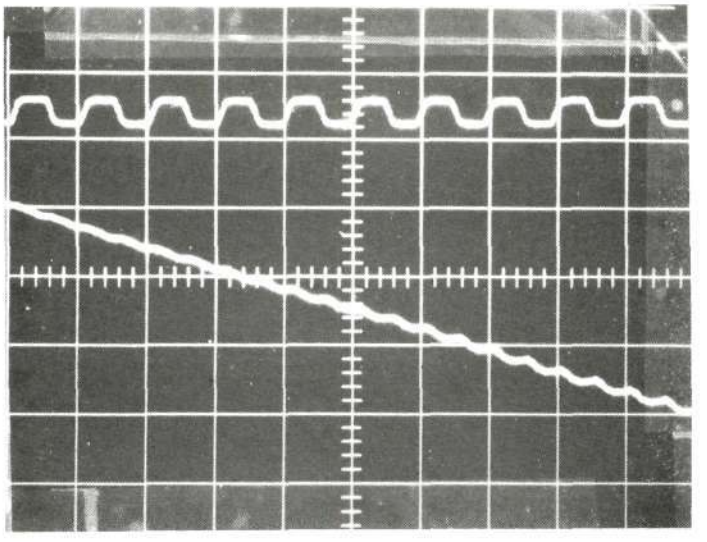
BINARY OUTPUT	SWITCHING POINT	BIT SIZE (mV)	SWITCHING POINT	BIT SIZE (mV)	HYSTERESIS (mV)
00000			-2.358	158	24
00001	-2.334		-2.200	156	30
00010	-2.170	164	-2.044	159	35
00011	-2.009	161	-1.885	155	26
00100	-1.859	150	-1.730	152	32
00101	-1.698	161	-1.578	166	31
00110	-1.547	151	-1.412	155	17
00111	-1.395	152	-1.257	160	18
01000	-1.239	156	-1.097	165	33
01001	-1.064	175	-.932	144	33
01010	-.899	165	-.788	165	39
01011	-.749	150	-.623	154	40
01100	-.583	166	-.469	157	32
01101	-.437	146	-.312	159	28
01110	-.284	153	-.153	154	25
01111	-.128	156	+.001	132	29
10000	+.030	158	+.133	156	34
10001	+.167	137	+.289	149	30
10010	+.319	152	+.438	150	27
10011	+.465	146	+.588	141	29
10100	+.617	152	+.729	166	24
10101	+.753	136	+.895	150	27
10110	+.922	169	+1.045	154	33
10111	+1.078	156	+1.199	202	37
11000	+1.236	158	+1.401	159	25
11001	+1.426	190	+1.560	156	27
11010	+1.587	161	+1.716	157	25
11011	+1.741	154	+1.873	155	28
11100	+1.901	160	+2.028	159	33
11101	+2.061	160	+2.187	157	37
11110	+2.224	163	+2.344		33
11111	+2.377	153			

TABLE 15

S/H - A/D TRACKING AND LINEARITY TESTS RESULTS

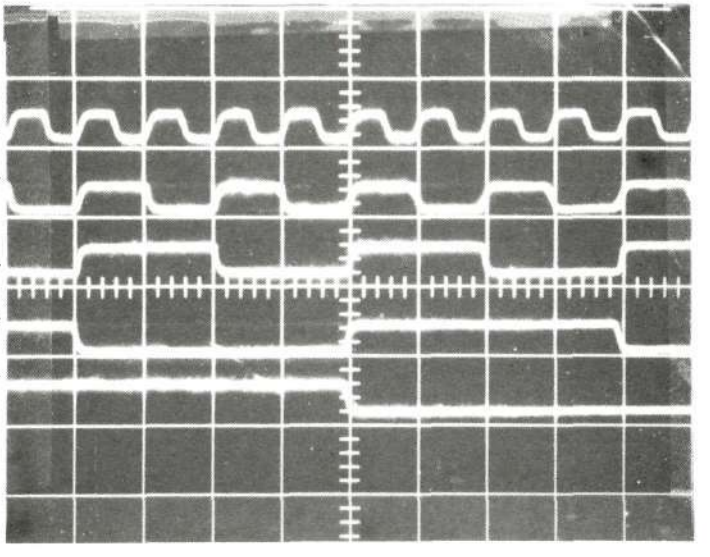
BINARY OUTPUT	SWITCHING POINT A/D #1 (mV)	BIT SIZE A/D #1 (mV)	SWITCHING POINT A/D #2 (mV)	BIT SIZE A/D #2 (mV)
00000	-711		-708	
00001	-668	43	-661	47
00011	-617	51	-615	46
00100	-567	50	-565	50
00101	-520	47	-514	51
00110	-472	48	-469	45
00111	-422	50	-420	49
01000	-377	45	-373	47
01001	-325	52	-322	51
01010	-276	49	-273	49
01011	-228	48	-226	47
01100	-182	46	-179	47
01101	-132	50	-130	49
01110	-85	47	-82	48
01111	-39	46	-34	48
10000	10	49	13	47
10001	53	43	60	47
10010	103	50	108	48
10011	150	47	154	46
10100	197	47	201	47
10101	242	45	247	46
10110	292	50	297	50
10111	340	48	343	46
11000	389	49	390	47
11001	436	47	437	47
11010	484	48	485	48
11011	533	49	536	51
11100	581	48	584	48
11101	632	51	633	49
11110	680	48	682	49
11111	728	48	733	51

a) LSB AND S/H RAMP OUTPUT



VERTICAL:
TOP TRACE 1 V/DIV
BOTTOM TRACE 2 V/DIV
HORIZONTAL:
50 NSEC/DIV

b) A/D OUTPUT BITS



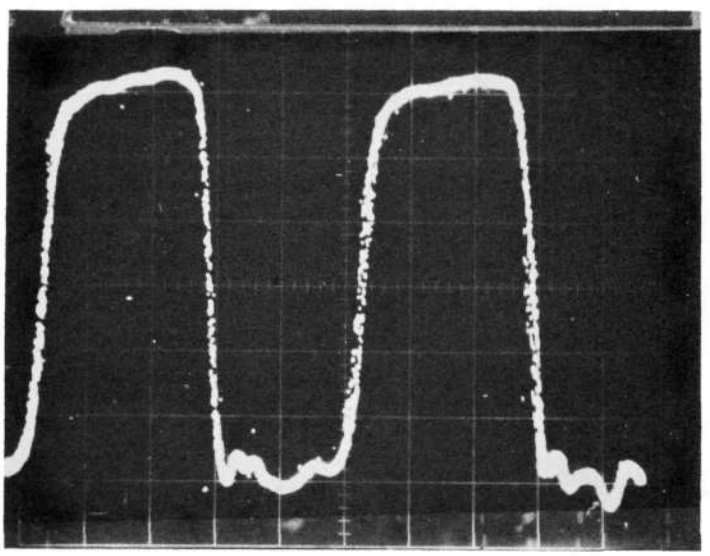
VERTICAL:
1 V/DIV
HORIZONTAL:
50 NSEC/DIV

FIGURE 5–15 A/D OUTPUT BITS WITH RAMP INPUT

5.3.4 Parallel/Serial Converters

Operation of the parallel/serial converters was tested by applying 5 bit parallel words from a PN generator operating at 40 Mbps to the parallel inputs of the converter and noting the output bit pattern. Figure 5-16 is a portion of the P/S output used to show "one-zero" symmetry.

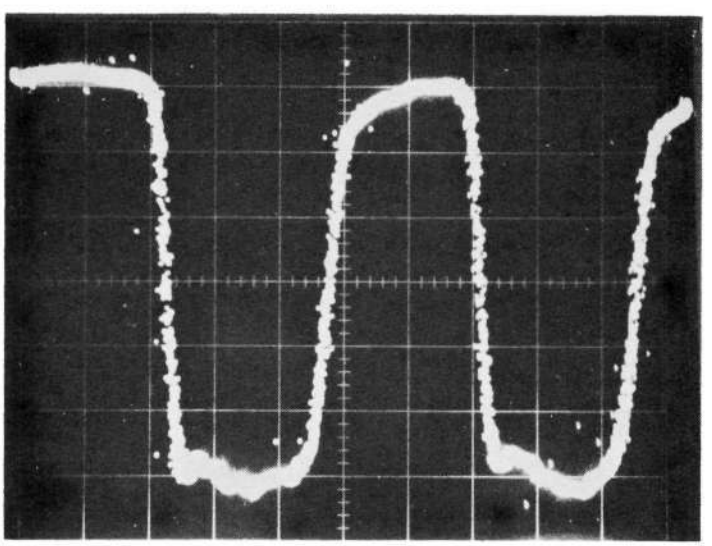
a) PARALLEL/SERIAL CONVERTER NO. 1 OUTPUT



VERTICAL:
100 MV/DIV

HORIZONTAL:
2 NS/DIV

b) PARALLEL/SERIAL CONVERTER NO. 2 OUTPUT



VERTICAL:
100 mV/DIV

HORIZONTAL
2 NS/DIV

FIGURE 5-16 PARALLEL/SERIAL CONVERTER OUTPUTS ILLUSTRATING GOOD "ONE ZERO" SYMMETRY

5.3.5 Timing and Control/Multiplexer

The timing and control circuit was operated over the frequency range of 100 MHz to 400 MHz. No abnormal operation was noted during these tests.

The multiplexer was first tested by using the outputs of a PN generator operating at 200 Mbps as the multiplexer inputs. Proper operation of the multiplexer was confirmed by correlating the output code patterns with the input PN codes. Figure 5-17 illustrates the good "one-zero" symmetry observed at the multiplexer output.

The multiplexer was also tested using the two parallel/serial converters as sources for its input.

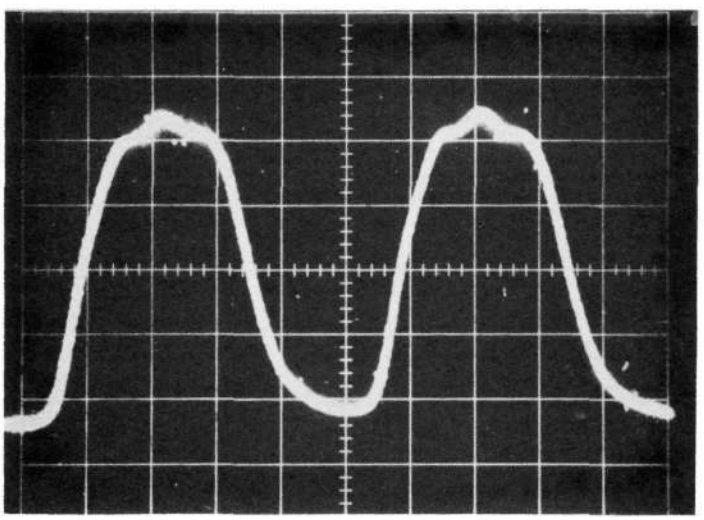


FIGURE 5-17 MULTIPLEXER OUTPUT ILLUSTRATING GOOD "ONE ZERO" SYMMETRY

5.3.6 Signal Processing Electronics Integration

The entire signal processing electronics was packaged and inter-connected for integrated operation. Thermal tests were performed on the entire package with the system operating in a static mode. Figure 5-18 shows the case and inner module temperatures at various locations on the package. The results of the temperature test agreed closely with design predictions.

The entire system was checked for operation by applying dc levels to the analog input that corresponded with the 32 quantization levels. By correlating the dc input with the digital output, proper operation of the electronics for all digital word combinations was confirmed.

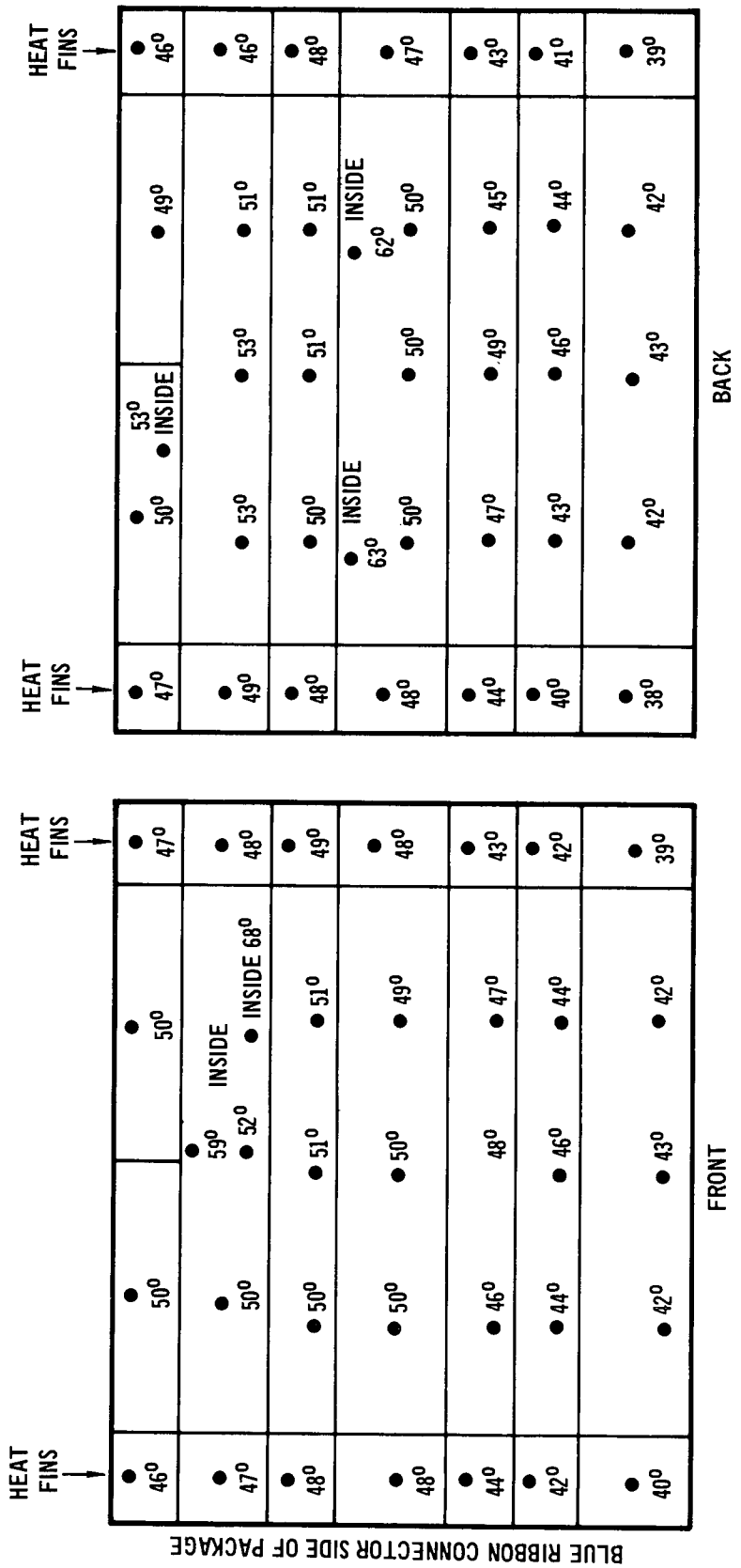


FIGURE 5–18 OMS SIGNAL PROCESSING PACKAGE TEMPERATURE TEST RESULTS

5.3.7 Signal Processing Power Supply Tests

Each regulator in this power supply was checked for adjustment range, current limit, short circuit current, ripple and regulation from no load to 90% full load. The test results are given in Table 16.

TABLE 16

SIGNAL PROCESSING POWER SUPPLY TESTS

Regulator	Adjustment Range		Current Limit	Short Circuit Current	90% Load AC Ripple	90% Load ΔV
	Low	High				
Volts	Volts	Volts	Amps	Amps	mV	Volts
-2.0	< -0.1	-8.0	2.3	1.7	1	.10
+5.2	3.5	8.6	1.47	0.75	5	.05
-5.2	< -0.1	13.1	8.8	3.6	5	.10
+12.0	3.1	20.9	0.82	0.83	1	.10
-12.0	< -0.1	-21.4	0.82	0.83	1	.10

5.4 ERROR RATE TESTS.

Several error tests were conducted on the 400 Mbps, 0.53 μm modulator and receiver as a function of the optical signal level and test code sequence length. Typical results are given on Figure 5-19. No special significance should be attached to the fact that the longer sequence lengths produced lower error rates since the tests were conducted on different days and all the system parameters and operating points may not have been the same. Also it should be noted that data points below 10^{-7} bit error rate were extremely difficult to obtain because the test laser amplitude instabilities prohibited counting errors for long periods of time, such as 10 seconds.

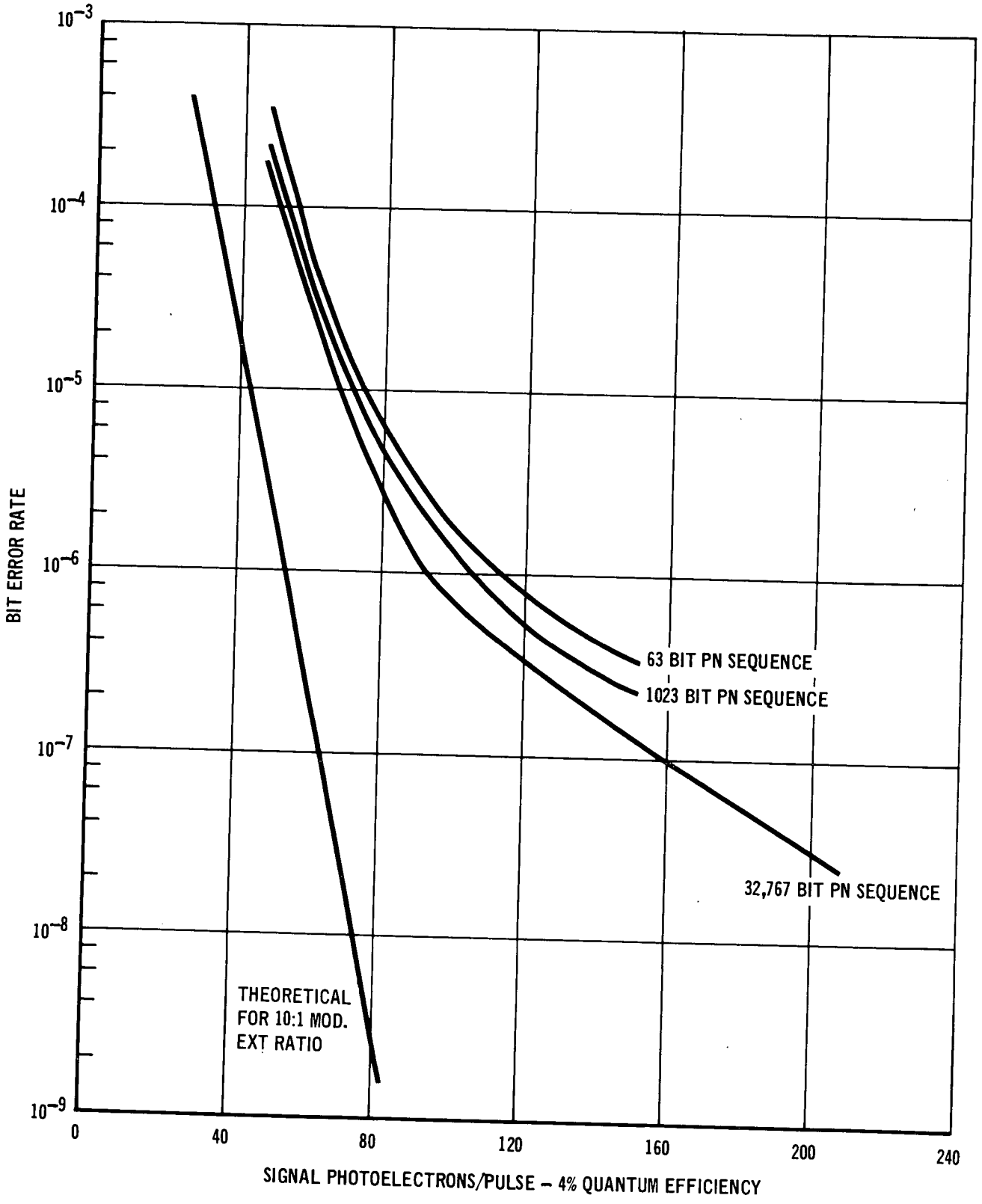


FIGURE 5–19 400 Mbps 0.53 μ M MODULATOR/RECEIVER ERROR RATE DATA

6. CONCLUSIONS AND RECOMMENDATIONS

The hardware constructed and tested during this program included a 0.53 μm modulator, 1.06 μm modulator, signal processing electronics, and power supplies for the modulators and electronics. The program demonstrated that it is quite feasible to design and fabricate a space qualifiable 0.53 μm or 1.06 μm modulator and associated electronics. The total power required by a space qualified modulator unit would be approximately 30 watts for 1.06 μm operation and 20 watts for 0.53 μm operation.

While the transmission and extinction ratio of the units delivered on this program were quite good, they were limited by the double pass configuration and required precise optical alignment. Work underway in our laboratories, which is a part of our continuing IRAD effort in modulator development, indicates that it is feasible to construct a single pass modulator which would operate with approximately the same power required for the present double pass units. Since the static extinction ratio of a single pass unit would be in the neighborhood of 100:1 a worst case dynamic extinction ratio of 30:1 could be readily achieved. Moreover, optical transmission would be increased to 90% and 80% respectively for a 0.53 μm unit and a 1.06 μm unit. The single pass modulator would be constructed with etched crystals which would greatly reduce the surface work strain. Hybrid circuit techniques would be used for the modulator driver and matching network to obtain improved performance and reproducibility.

The signal processing electronics for this program was constructed primarily using existing monolithic logic elements. This dictated an approach using two 200 Mbps encoding chains whose outputs were interleaved by a 400 Mbps digital multiplexer. It should be noted that the use of hybrid circuit logic elements would enable implementation of a single 400 Mbps encoding chain with a very significant decrease in power, size, and weight relative to the electronics delivered on this program.

We recommend an improved 400 Mbps modulator design program which would utilize latest available construction techniques and be based on single pass operation with inherently better transmission and extinction ratio. The modulator resulting from this program would be more representative of the final design of a space qualified unit.