C-MOS Array Design Techniques
Contract NAS 12-2233

SUMC-DV HARDWARE MANUAL

November 1972

Prepared for
George C. Marshall Space Flight Center
National Aeronautics and Space Administration
Marshall Space Flight Center, Alabama 35812

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Advanced Technology Laboratories
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by

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FOREWORD

This report describes the assembly, the physical and electrical characteristics, and the basic electrical tests of the Space Ultrareliable Modular Computer - Demonstration Vehicle (SUMC-DV). Included are descriptions of (1) the packaging concepts, physical assembly, design and fabrication using design automation techniques of 10 different types of custom CMOS LSI arrays, (2) the fabrication and testing of the various components including the LSI arrays, (3) the hierarchy of the memory complement and the clock generation and distribution system, (4) system testing techniques, and (5) the procedure employed in the electrical checkout of the system.

Section I includes a description of the CMOS technology with emphasis on some of the more important system advantages of the CMOS technology. Section II includes a brief description of the CMOS standard cell design automation technology and its application to generating LSI arrays. This section includes a description of the characteristics and statistics of the 10 LSI array types.

Section III includes a detailed description of the chip evaluation and testing procedures. Included are examples of the application of computer programming and simulation techniques, logic simulation, circuit simulation and automatic generation of test sequence bit patterns. Section III includes an extensive set of static and dynamic tests for all of the 10 array types. Included in these tabulated data are the results of the functional, static and leakage measurements, the life test data, and the propagation delay measurements.

Section IV covers the testing done at a subsystem level. This includes subsystem propagation delay measurements, life testing, capacitive measurements and temperature distribution. Section V covers the SUMC-DV test set and the front panel. This section describes the test set and its use in debugging and maintaining the SUMC-DV

computer. A brief user's operational guide is presented. All the controls and switches on the front panel are also covered in this section which includes a brief user's procedure for operating the SUMC-DV system from the front panel.

Sections VI, VII and VIII contain descriptions of the IAROM and MROM, Scratch Pad and Main Memory systems. In each case the organization, timing, interface and operation of the several memories are included.

Section IX contains a detailed description of the clock generation and distribution system employed in the SUMC-DV. Section X covers the power supply and distribution approach used. Section XI describes and illustrates the packaging and interconnection techniques used in fabrication of the SUMC-DV.

SECTION I

CIRCUIT TECHNOLOGY

Exclusive of main memory, read-only memory, the clock generator, and interface amplifiers/level shifters, the SUMC-DV was implemented with 10 types of custom LSI complementary MOS chips using the standard cell technique. Within the framework of the standard cell topology, all of the inherent advantages and efficiency of custom design were incorporated into the circuit design of the required logic functions. Since it was necessary to design a circuit only once, greater effort was exercised in development of the optimum circuit. Different geometry N and P devices were used to optimize the rise/fall time and performance of each circuit. Each circuit design was then simulated using the FETSIM transient analysis program described in Section IIIA2 and the design was modified when necessary. The standard cells designed for the SUMC-DV are described in the Cell User's Handbook.

Although the outstanding features and advantages of CMOS have been well documented in the literature, some of the special features of this circuit technology from a systems viewpoint are listed below.

(1) Symmetrical high noise immunity - 40 to 45% of power supply voltage.

(2) Two firm signal levels equal to supply voltage and ground.

(3) Single power supply.

(4) Extremely low power dissipation resulting in reduced power supply requirements, simplified power distribution and simplification of packaging because of virtual elimination of cooling requirements.

(5) High ratio of rise/fall time to propagation delay results in low crosstalk and reduced complexity of interconnections.

(6) High integration levels provide dramatic reduction in volume and weight of equipment and in total parts requirement. The high packaging density achieved results in higher performance, simplification of system debugging and lower documentation costs.

(7) Reliable operation over wide process, circuit parameter and voltage variations including wide temperature variations.

(8) Excellent interface capability with other technologies.

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SECTION II

LSI CMOS STANDARD CELL ARRAYS

A. CHIP DESIGN AND FABRICATION

Following partitioning of the SUMC-DV logic, a series of new standard cell circuits was designed and added to the standard cell library so that the required chips could be designed and fabricated. Chip design starts with validation of the chip logic using the LOGSIM program. This program and its application to simulating the adder (ALU) arrays are detailed in Section IIIA1. The chip logic is further analyzed for performance using the FETSIM transient analysis program. A description of this simulator and its use in analyzing the ALU data path is given in Section IIIA2. This analysis aided in the selection of standard cell circuits used in the data path to optimize performance.

Once the logic was validated, four input files required for the Place-Route-Fold (PRF) program were provided: (1) the logic net list, (2) the cell pin data file, (3) the gate to cell pattern assignment, and (4) the initial placement. The PRF program first optimizes the cell placement in a linear array to minimize crossovers and total interconnect length. The program then interconnects the cell into the required logic configuration using metal or deffused "P" tunnels and then folds the linear array into a two-dimensional array of cell rows so as to make the folded array as nearly square as possible. Manual intervention using the PRF MANMOD subroutine was then used to optimize pad location and improve array performance by removing highly resistive and capacitive tunnels from chip output pad interconnections.

The Artwork (ARTWRK) and adjunct programs were used to prepare control tapes for driving the CALCOMP and Gerber plotters to provide chip checkplots and final 80X artwork, respectively. The ALU checkplot which was used to validate the adder connectivity is shown in Fig. 2-1. The checkplot uses cell outlines rather than detailed plots for checking simplicity and reduced plotting time; detailed

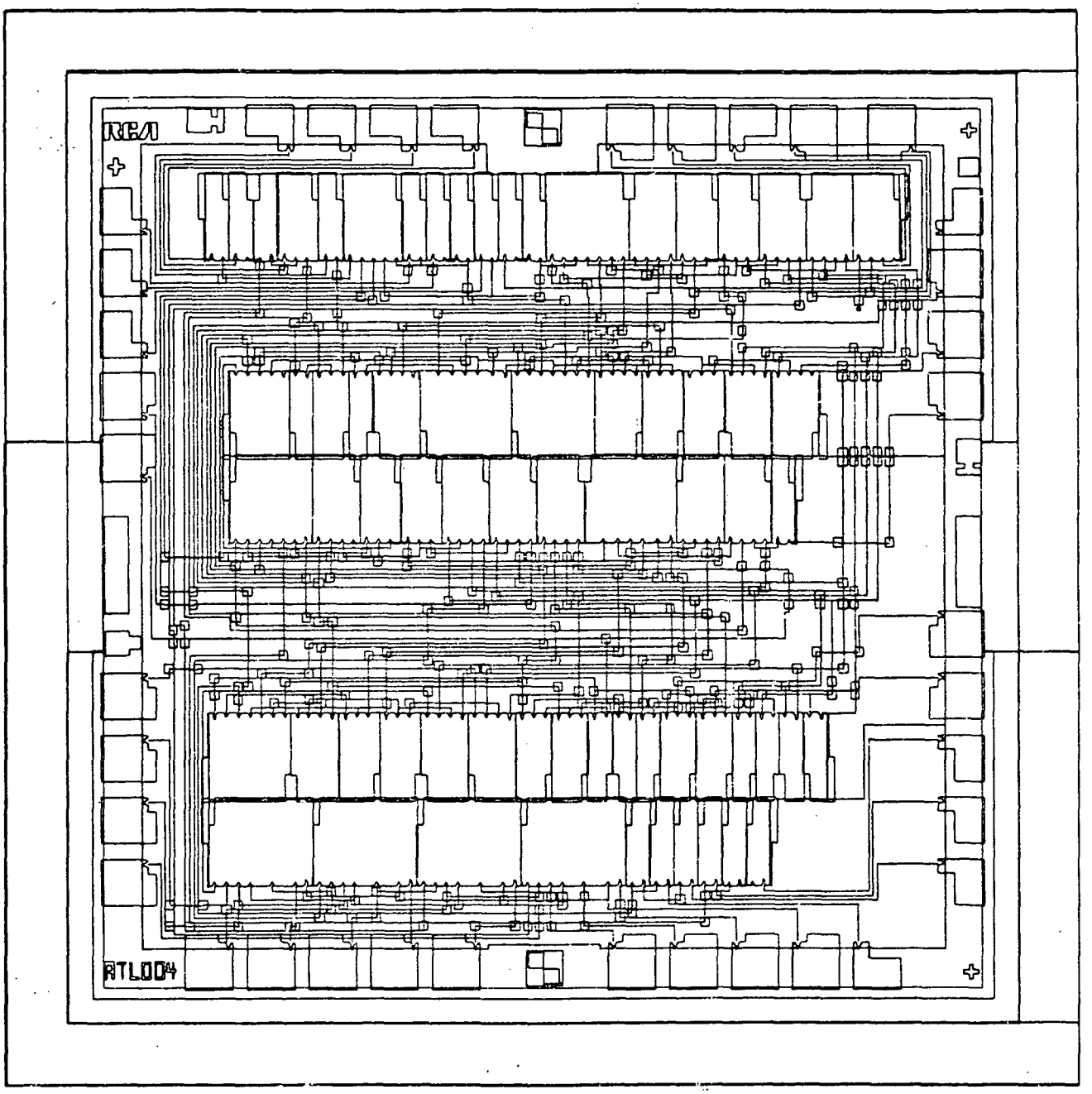


Fig. 2-1. Outline checkplot of ALU array.

checkplots of each standard cell were previously verified at 100X by storing all the polygons of each of the seven masks levels of each cell in the standard cell library. The ARTWRK program combined the output of the PRF program with the contents of the cell library to generate the Gerber artwork tape comprising all the required plotter commands and movements to generate the seven 80X artwork plates. Following final inspection and touchup, these plates were then photoreduced to make a 10X reticle for the step-and-repeat camera. A set of seven processing photomasks were then produced by the step-and-repeat camera on 2-1/2-inch glass plates.

B. SUMC-DV LSI ARRAY TYPES

A summary of the ten chip types follows.

ATL-000 - Multiple Purpose Register (MPR)

The MPR is a six-bit register unit which can be used as a data or master/slave register. The inputs to the register are clocked and the outputs are either direct or clocked outputs. An additional capability of the MPR is shifting data right one, left one, or directly to the slave when the chip is used in a master/slave register arrangement.

ATL-001A - Product Result Register (PRR)

The PRR chip contains a four-bit master/slave register with two multiplexed inputs. One of the inputs is a direct path to the register, while the other input has the capability of passing data directly or shifting logically, arithmetically or with forced end effects. The input with shifting capability can shift data right one or four bits, or left one, two or four bits.

ATL-002A - Multiply Quotient Register (MQR)

The MQR chip contains a four-bit master/slave register with two multiplexed inputs and a four-bit data register with one direct input. One of the master/slave register inputs is a direct path to the register while the other input is shifted right four bits, or left one or two bits. The outputs of the chip are the four master/slave outputs and four data outputs.

ATL-004A - Arithmetic Logic Unit (ALU)

The ALU is a four-bit adder unit with a direct input and two multiplexed inputs. One of the operands is the direct input and the other operand is one of the multiplexed inputs. One of the multiplexed inputs is a direct path to the adder while the other is either direct or shifted arithmetically right one bit. The combinatorial adder logic on the chip has the capability of adding, subtracting, reverse subtracting, logical AND, logical OR, and logical exclusive OR.

ATL-005 - Scratch Pad Address and Interrupt (SPA-INT)

The ATL-005 is used in the SUMC-DV system as a scratch pad addressing generator. The custom array has the capability of forming a five-bit address under interrupt level control. The chip has five D-type flip-flops with a common clock. Three of the flip-flops have three-input data multiplexers with control and the other two flip-flops contain external inputs and an interrupt level input. The remaining part of the chip contains a three-bit interrupt request register, priority allocation logic and a three-bit interrupt level register.

ATL-006A - Condition Code Generator and Interrupt Status Register (CC-ISR)

The ATL-006A is used in the SUMC-DV system as a condition code generator and an Interrupt Status Register (ISR). A portion of the chip contains control to form condition codes for Spectra 70 and IBM 360 type instructions. A four-bit ISR is on the chip with a multiplexed data input and control generated input for each flip-flop of the register, and the outputs are multiplexed with external signals.

ATL-007A - Adder Control Logic (ADCON)

The ATL-007A is used in the SUMC-DV system as a control chip for the arithmetic units and their input multiplexers. The chip generates control bit patterns for all the arithmetic and logic functions used in SUMC by using read-only memory inputs and data inputs used in multiplication, division and square root algorithms. The chip also generates quotient bits for square root and division.

ATL-008A - A-MUX and B-MUX Control

The ATL-008A contains four two-input multiplexers with control and combinatorial logic used to generate multiplexer control signals used in the arithmetic chip (ATL-004A). The four outputs of the multiplexer are complemented with respect to the input.

ATL-009A - Sequence Control and Iteration Counter (SEQ-IC)

The ATL-009A is used in the SUMC-DV system as sequence control chip. It contains a four-bit sequence counter with the capability of accepting one of two external inputs, incrementing the previous count, or leaving the count unchanged. This chip also contains a two-bit iteration counter which can be set by two external inputs, decrementing a previous count by 1, or leaving a count unchanged.

ATL-010A - Control for Sequence and Iteration Counter (SEQ-IC Cont)

The ATL-010A is used in the SUMC-DV system as a control chip for the Sequence Control and Iteration Counter (ATL-009A). It contains specialized control logic which decodes read-only memory bit patterns and produces the selection signals for ATL-009A.

SECTION III

CHIP TESTING AND EVALUATION

All chip testing consisted of at least two basic procedures. Initially, computer simulation and computer breadboarding techniques were used to predict and analyze circuit performance, verify the logic implementation and functional correctness of the logic, and automatically generate test sequence patterns for complete static, dynamic and functional testing of the fabricated parts. This was followed, for all chip types, by static, dynamic and functional testing. For some chip types, whose performance is critical to the overall throughput of the SUMC-DV systems, such as the ALU chip types (ATL-004A), additional propagation delay measurements were made in the SUMC-DV computer. These measured results were used to compare the expected propagation delay of these chips in the system against the actual system propagation delay. One of the objectives in so doing was to enhance the accuracy of predicting system performance of selected chip types based on computer simulation and dynamic measurements made on the corresponding chip type in the laboratory.

The following paragraphs describe all these various aspects of chip testing as they were implemented on the SUMC-DV chip types and computer.

A. COMPUTER SIMULATION, ANALYSIS AND TEST SEQUENCE GENERATION

1. Logic Simulation - Application of LOGSIM Computer Program to the ALU Array

The LOGSIM program shown in the flowchart of Fig. 3-1 can be used by the designer to check the logic design. The simulation output is formatted to permit both functional and timing relationships to be verified. This section illustrates the application of the LOGSIM logic simulation program to the ALU chip type whose partitioned logic is shown in Fig. 3-2.

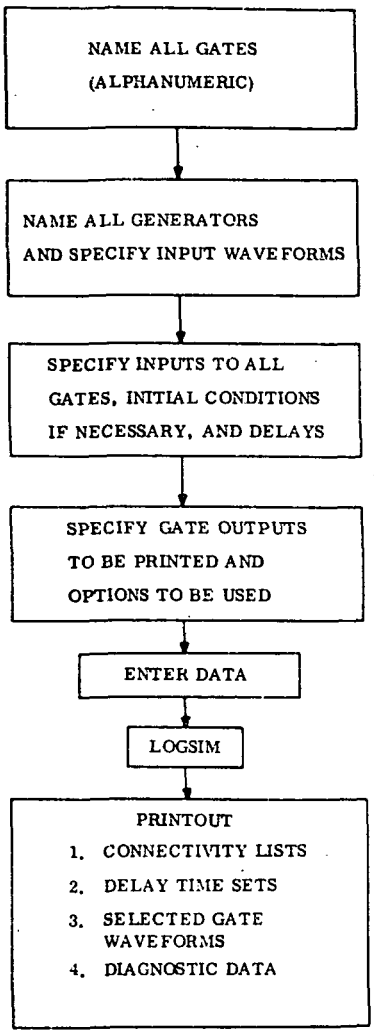


Fig. 3-1. User flow chart for LOGSIM.

Considerable flexibility is provided the user in controlling the simulation procedure. This control includes simple clerical accuracy checks, functional errors in the logic, and detailed checking for logic race conditions that might result from timing and propagation delay variations. Variants of the simulation program permit the user to observe the effect of logic element timing variations due to capacitive loading and system packaging effects.

Figure 3-3, the simulation control statement, provides to the user a summary of the input controls to be specified and a preview of the output that will follow. The control statements vary as a function of the input control specifications.

LOGSIM provides the option of printing out a cross reference connectivity list which is needed during the debugging stage. It is also extremely useful as

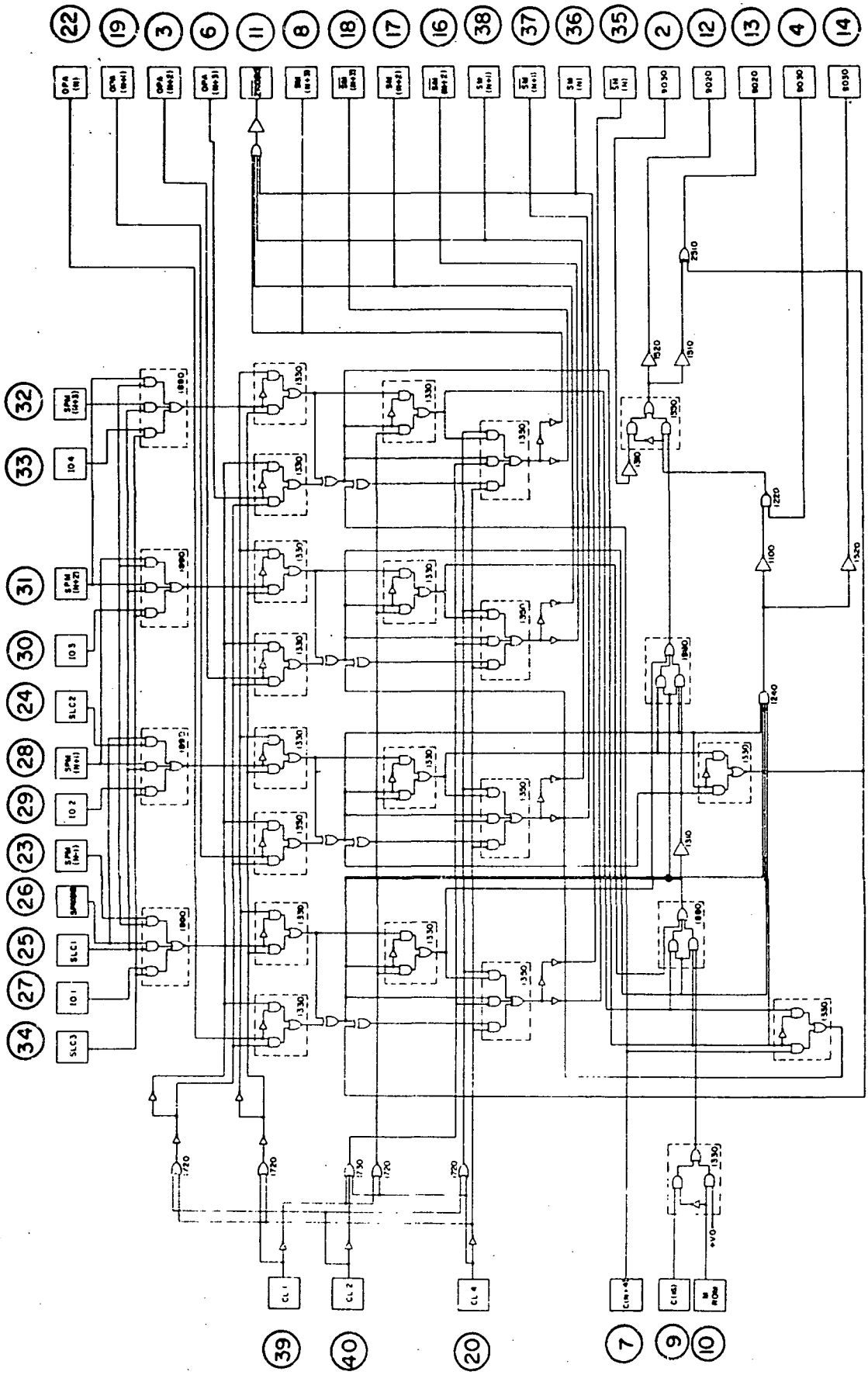


Fig. 3-2. Arithmetic and logic unit (ALU) partitioned logic.

```
ARITHMETIC LOGIC UNIT FOR SUMC-DV CMOS COMPUTER

PRINT MATRIX WILL BE READ
SPIKE NOTICES WILL BE PRINTED
CONNECTIVITY LIST WILL BE PRINTED
MAXIMUM INTERNAL CLOCK VALUE = 570000
TOTAL NUMBER OF LOGIC GATES = 128
TOTAL NUMBER OF GENERATORS = 22
SECURITY CLASSIFICATION = UNCLASSIFIED
```

Fig. 3-3. LOGSIM control statement.

reference after a valid LOGSIM simulation has been completed. Figures 3-4 and 3-5 show examples of the cross reference connectivity lists; one the input loads of a given gate and the other the output loads of a given gate. Each gate is assigned a unique number. These numbers are used to identify the gates that are referenced by the program throughout the printout. In Fig. 3-4 and 3-5 the first two columns are used to assign the identification number with the appropriate gate name. The next column defines the function performed by the particular gate. Most of the gate types are common single level logic functions: AND, OR, EXOR, etc. LOGSIM also provides an option of entering a new gate function different from the common types. All that is needed to enter a new gate type is the truth table; HALB and ANAB in this column are examples of new gate functions that were used in this simulation. HALB (High A, Low B) has the Boolean expression F = AC + CB where input C is the controlling input (see cell 1330). ANAB is the function F = AB. The next column in Fig. 3-4 specifies the initial conditions of the output. This is optional for input and is usually used when defining the initial conditions for sequential logic. The last two columns of 3-4 and 3-5 specify the number of inputs or output loads connected to the gate and the names of gates that are connected. The figures do not show the complete listing of all the input and output names for every gate.

This logic simulation program gives the engineer the option of defining the propagation time through the logic gates by a fixed delay, by a table of delay versus load (output gate capacitance or numerical weight), or by a random delay specified between two given limits. Figure 3-6 is an example of the delay versus capacitive

ARITHMETIC LOGIC UNIT FOR SUMC-DV CMOS COMPUTER

NO.	GATE NAME	TYPE	INIT.	# INPUTS	INPUT NAMES		
1	SCAI	NOR	*	1	SCA0		
2	SCAO	NOR	*	2	CL20	CL4BAR	
3	SCB1	NOR	*	1	SCB		
4	SCBO	NOR	*	2	CL1	CL4BAR	
5	SCDBAR	DR	*	3	CL1BAR	CL2BAR	CL4
6	ORC	NOR	*	2	CL1BAR	CL4	
7	SCEBAR	OR	*	2	CL2	CL4	
8	CL1BAR	NAND	*	1	CL1		
9	CL2BAR	NAND	*	1	CL2		
10	CL4BAR	NAND	*	1	CL4		
11	OFLOBAR	EXOR	*	2	CN	CN1	
12	AOPN	HALB	*	3	SCA0	SCA1	OPAN
13	AOPNA	HALB	*	3	SCB0	SCB1	OPBN
14	FNON	EXOR	*	2	AOPN	AUPNA	
15	FNAN	HALB	*	3	ORC	AUPNA	FNON
16	N	EXOR	*	2	CN1	FNON	
17	SNA	ANAB	*	2	CL4BAR	N	
18	SNB	ANAB	*	2	SCDBAR	FNON	
19	SNC	ANAB	*	2	SCEBAR	FNAN	
20	SN	OR	*	3	SNA	SNB	SNC
21	SMNBAR	NAND	*	1	SN		
22	SMN	NAND	*	1	SMNBAR		
23	AOPN1	HALB	*	3	SCA0	SCA1	OPAN1
24	AOPN1A	HALB	*	3	SCB0	SCB1	OPBN1
25	FNDN1	EXDR	*	2	ADPN1	AUPN1A	
26	FNAN1	HALB	*	3	ORC	AOPN1A	FNDN1
27	N1	EXDR	*	2	CN2	FNDN1	
28	SN1A	ANAB	*	2	CL4BAR	N1	
29	SN1B	ANAB	*	2	SCDBAR	FNON1	
30	SN1C	ANAD	*	2	SCEBAR	FNAN1	
31	SN1	OR	*	3	SN1A	SN1B	SN1C
32	SMN1BAR	NAND	*	1	SN1		
33	SMN1	NAND	*	1	SMN1BAR		
34	AOPN2	HALB	*	3	SCA0	SCA1	OPAN2
35	AOPN2A	HALB	*	3	SCB0	SCB1	OPBN2
36	FNON2	EXOR	*	2	AOPN2	AUPN2A	
37	FNAN2	HALB	*	3	ORC	AUPN2A	FNON2
38	N2	EXDR	*	2	CN3	FNON2	
39	SN2A	ANAB	*	2	CL4BAR	N2	
40	SN2B	ANAB	*	2	SCDBAR	FNON2	
41	SN2C	ANAB	*	2	SCEBAR	FNAN2	
42	SN2	OR	*	3	SN2A	SN2B	SN2C
43	SMN2BAR	NAND	*	1	SN2		
44	SMN2	NAND	*	1	SMN2BAR		
45	AOPN3	HALB	*	3	SCA0	SCA1	OPAN3
46	AOPN3A	HALB	*	3	SCB0	SCB1	OPBN3
47	FNON3	EXOR	*	2	AOPN3	AUPN3A	
48	FNAN3	HALB	*	3	ORC	AUPN3A	FNON3
49	N3	EXOR	*	2	CN4	FNON3	
50	SN3A	ANAB	*	2	CL4BAR	N3	
51	SN3B	ANAB	*	2	SCDBAR	FNON3	
52	SN3C	ANAB	*	2	SCEBAR	FNAN3	
53	SN3	OR	*	3	SN3A	SN3B	SN3C
54	SMN3BAR	NAND	*	1	SN3		

Fig. 3-4. Gate input connectivity list.

NO.	GATE NAME	TYPE	# LOADS	CONNECTIVITY LIST INTERCONNECTIONS		
1	SCA1	NOR	8	AOPN	AOPN1	AOPN2
				AOPN7		
2	SCA0	NOR	9	SCA1	AOPN	AOPN1
				AOPN6	AOPN7	
3	SCB1	NOR	8	AOPNA	AOPN1A	AOPN2A
				AOPN7A		
4	SCB0	NOR	9	SCB1	AOPNA	AOPN1A
				AOPN6A	AOPN7A	
5	SCOBAR	OR	8	SNB	SN1B	SN2B
				SN7B		
6	ORC	NOR	8	FNAN	FNAN1	FNAN2
				FNAN7		
7	SCEBAR	OR	8	SNC	SN1C	SN2C
				SN7C		
8	CL1BAR	NAND	2	SCDBAR	ORC	
9	CL2BAR	NAND	1	SCDBAR		
10	CL4BAR	NAND	10	SCA0	SCB0	SNA
				SN5A	SN6A	SN7A
11	OFLOBAR	EXOR	0			
12	AOPN	HALB	1	FNON		
13	AOPNA	HALB	2	FNON	FNAN	
14	FNON	EXOR	6	FNAN	N	SNB
15	FNAN	HALB	2	SNC	COUTOBAR	
16	N	EXOR	1	SNA		
17	SNA	ANAB	1	SN		
18	SND	ANAB	1	SN		
19	SNC	ANAB	1	SN		
20	SN	OR	1	SMNBAR		
21	SMNBAR	NAND	1	SMN		
22	SMN	NAND	1	ZROABAR		
23	AOPN1	HALB	2	FNON1	CN1	
24	AOPN1A	HALB	2	FNON1	FNAN1	
25	FNON1	EXOR	6	FNAN1	N1	SN1B
26	FNAN1	HALB	2	SN1C	SM1TH1A	
27	N1	EX7R	1	SN1A		
28	SN1A	ANAB	1	SN1		
29	SN1B	ANAB	1	SN1		
30	SN1C	ANAB	1	SN1		
31	SN1	OR	1	SMN1BAR		
32	SMN1BAR	NAND	1	SMN1		
33	SMN1	NAND	1	ZROABAR		
34	AOPN2	HALB	1	FNON2		
35	AOPN2A	HALB	2	FNON2	FNAN2	
36	FNON2	EXOR	6	FNAN2	N2	SN2B
37	FNAN2	HALB	2	SN2C	COUT2BAR	
38	N2	EXOR	1	SN2A		
39	SN2A	ANAB	1	SN2		
40	SN2B	ANAB	1	SN2		
41	SN2C	ANAB	1	SN2		
42	SN2	OR	1	SMN2BAR		
43	SMN2BAR	NAND	1	SMN2		
44	SMN2	NAND	1	ZROABAR		

Fig. 3-5. Gate output connectivity list.

ARITHMETIC LOGIC UNIT FOR SUMC-DV CMOS COMPUTER

NO.	GATE NAME	TYPE	CAPACITANCE	TIMESET #	FALL DELAY	RISE DELAY
1	SCA1	NOR	6D	101	31	43
2	SCA0	NOR	2D	102	11	16
3	SCB1	NOR	6D	101	31	43
4	SCB0	NOR	2D	102	11	16
5	SCDBAR	UR	8E	103	42	60
6	DRC	NOR	6D	101	31	43
7	SCEBAR	OR	7D	104	36	53
8	CL1BAR	NAND	4G	105	6	9
9	CL2BAR	NAND	4G	105	6	9
10	CL4BAR	NAND	4G	105	6	9
11	OFLOBAR	EXOR	10I	106	56	45
12	AOPN	HALB	3H	107	15	9
13	AOPNA	HALB	4H	108	17	10
14	FNON	EXOR	8I	109	53	42
15	FNAN	HALB	4H	108	17	10
16	N	EXOR	3I	110	45	32
17	SNA	ANAB	3I	0	0	0
18	SNB	ANAB	3I	0	0	0
19	SNC	ANAB	3I	0	0	0
20	SN	UR	6B	111	16	22
21	SMNBAR	NAND	6C	112	10	12
22	SMN	NAND	24C	113	23	29
23	AOPN1	HALB	5H	114	19	12
24	AOPN1A	HALB	4H	108	17	10
25	FNON1	EXOR	8I	109	53	42
26	FNAN1	HALB	4H	108	17	10
27	N1	EXOR	3I	110	45	32
28	SN1A	ANAB	3I	0	0	0
29	SN1B	ANAB	3I	0	0	0
30	SN1C	ANAB	3I	0	0	0
31	SN1	UR	6B	111	16	22
32	SMN1BAR	NAND	6C	112	10	12
33	SMN1	NAND	24C	113	23	29
34	AOPN2	HALB	3H	107	15	9
35	AOPN2A	HALB	4H	108	17	10
36	FNON2	EXOR	8I	109	53	42
37	FNAN2	HALB	4H	108	17	10
38	N2	EXOR	3I	110	45	32
39	SN2A	ANAB	3I	0	0	0
40	SN2B	ANAB	3I	0	0	0
41	SN2C	ANAB	3I	0	0	0
42	SN2	UR	6B	111	16	22
43	SMN2BAR	NAND	6C	112	10	12
44	SMN2	NAND	24C	113	23	29
45	AOPN3	HALB	5H	114	19	12
46	AOPN3A	HALB	4H	108	17	10
47	FNON3	EXOR	8I	109	53	42
48	FNAN3	HALB	4H	108	17	10
49	N3	EXOR	3I	110	45	32
50	SN3A	ANAB	3I	0	0	0
51	SN3B	ANAB	3I	0	0	0
52	SN3C	ANAB	3I	0	0	0
53	SN3	UR	6B	111	16	22
54	SMN3BAR	NAND	6C	112	10	12

Fig. 3-6. Delay of gates based on capacitance versus delay table.

load option. Given a capacitance versus delay table plus the input capacitance for each gate, the LOGSIM program will choose the proper delay for the given gate. Up to 500 different tables (capacitance load versus delay) can be entered into the program. When the capacitance is specified in the input data, the particular table is also specified by the letter adjacent to it. Figure 3-6 shows the identification number, gate name, type, the capacitance (in pF) and the letter indicating the table the program is to refer to. The remaining columns indicate the calculated rise and fall delays (defined as a time set) and the time set number. Up to 400 delay time sets can be generated by LOGSIM based on loading data calculated by the program or capacitance data supplied by the user.

Figure 3-7 is a typical waveform output with the spike option specified. During simulation, LOGSIM exercises the logic net in accordance with the levels specified in the input data. LOGSIM propagates these changes throughout the logic net, using the time delays assigned to each gate by the user. When all changes have been completed at a particular time, the gate output levels specified by the user are printed. The program internal clock is then advanced to the next time at which a gate output is to change. The change is made and propagated throughout the logic net. In this manner data compression is performed on the output levels. A possible spike condition exists when a gate output is driven in two directions at the same time as a result of the differences in rise and fall delays assigned to a particular gate, or as a result of an input changing too rapidly for the output to follow. This condition is noted in LOGSIM whenever a gate level is to change. However, no spike notices are printed unless the spike option has been selected. LOGSIM terminates the simulation if excessive spike conditions are detected.

The printout has the compressed time scale (in nanoseconds) on the bottom and the gate identification numbers on the y-axis (the order of the gates are specified by the users).

TIME	22	21	33	32	44	43	55	54	66 SLOTS	65	77	76 0-999
1125	0	1	0	0	0	1	0	1	1	0	1	0
1135	0	1	0	1	0	1	0	1	1	0	1	0
1142	0	1	0	1	0	1	0	1	1	0	1	0
1146	0	1	0	1	0	1	0	1	1	0	1	0
1147	0	1	0	1	0	1	0	1	1	0	1	0
1151	0	1	0	1	0	1	0	1	1	0	1	0
1160	0	1	0	1	0	1	0	1	1	0	1	0
1170	0	1	0	1	0	1	0	1	1	0	1	0
1177	0	1	0	1	0	1	0	1	1	0	1	0
1192	0	1	0	1	0	1	0	1	1	0	1	0
1224	0	1	0	1	0	1	0	1	1	0	1	0
2001	0	1	0	1	0	1	0	1	1	0	1	0
2018	0	1	0	1	0	1	0	1	1	0	1	0
POSSIBLE SPIKE AT T = 2020 GATE 91 SCHEDULED TO REACH OUTPUT												
2020	0	1	0	1	0	1	0	1	1	0	1	0
2035	0	1	0	1	0	1	0	1	1	0	1	0
2037	0	1	0	1	0	1	0	1	1	0	1	0
2069	0	1	0	1	0	1	0	1	1	0	1	0
2073	0	1	0	1	0	1	0	1	1	0	1	0
3001	0	1	0	1	0	1	0	1	1	0	1	0
3013	0	1	0	1	0	1	0	1	1	0	1	0
3023	0	1	0	1	0	1	0	1	1	0	1	0
3055	0	1	0	1	0	1	0	1	1	0	1	0
3065	0	1	0	1	0	1	0	1	1	0	1	0
3068	0	1	0	1	0	1	0	1	1	0	1	0
3077	0	1	0	1	0	1	0	1	1	0	1	0
3087	0	1	0	1	0	1	0	1	1	0	1	0
3091	0	1	0	1	0	1	0	1	1	0	1	0
3100	0	1	0	1	0	1	0	1	1	0	1	0
3104	0	1	0	1	0	1	0	1	1	0	1	0
3114	0	1	0	1	0	1	0	1	1	0	1	0
3116	0	1	0	1	0	1	0	1	1	0	1	0
3129	0	1	0	1	0	1	0	1	1	0	1	0
3174	0	1	0	1	0	1	0	1	1	0	1	0
4001	0	1	0	1	0	1	0	1	1	0	1	0
4010	0	1	0	1	0	1	0	1	1	0	1	0
4011	0	1	0	1	0	1	0	1	1	0	1	0
POSSIBLE SPIKE AT T = 4020 GATE 91 SCHEDULED TO REACH OUTPUT												
4020	0	1	0	1	0	1	0	1	1	0	1	0
4062	0	1	0	1	0	1	0	1	1	0	1	0
4063	0	1	0	1	0	1	0	1	1	0	1	0
4079	0	1	0	1	0	1	0	1	1	0	1	0
4086	0	1	0	1	0	1	0	1	1	0	1	0
4091	0	1	0	1	0	1	0	1	1	0	1	0
4095	0	1	0	1	0	1	0	1	1	0	1	0
4104	0	1	0	1	0	1	0	1	1	0	1	0
4114	0	1	0	1	0	1	0	1	1	0	1	0
4121	0	1	0	1	0	1	0	1	1	0	1	0
4136	0	1	0	1	0	1	0	1	1	0	1	0
4168	0	1	0	1	0	1	0	1	1	0	1	0
5001	0	1	0	1	0	1	0	1	1	0	1	0
5013	0	1	0	1	0	1	0	1	1	0	1	0

Fig. 3-7. Logical output waveforms of gates.

2. Application of the Circuit Analysis Program (FETSIM) to the ALU Array

FETSIM is a computer program written in Fortran IV which does dc and transient analysis of MOS circuits. Circuits employing almost any combination of R-C elements, NMOS transistors and/or PMOS transistors may be analyzed. FETSIM requires an input containing the complete circuit connectivity, device parameters, process parameters, and control parameters. The user can specify initial node conditions and the input pulse format. For example, pulse rise time, fall time, width and time between succeeding pulses are all independently controllable. A user's flowchart for the FETSIM program is given in Fig. 3-8. The adjacent letters correspond to the data shown in Fig. 3-11 and 3-12 which is a printout for the input data for the circuit of Fig. 3-9 and Fig. 3-10.

The program contains a sophisticated mathematical model that can accurately simulate either NMOS or PMOS transistors. Sensitivity to process change is maintained by permitting process and device parameters to be entered separately for each transistor.

The present version has the following dimensions, although it can easily be redimensioned. (For example, with a memory system having 64,000 full words, the nodes can be extended to approximately 75 and the transistor count to approximately 100.)

19 nodes
5 repeatable input pulses
100 branches
50 resistors
50 capacitors
20 NMOS transistors
20 PMOS transistors

The output data contains all circuit node voltages and transistor currents as a function of time. The user determines the time intervals at which the outputs are printed.

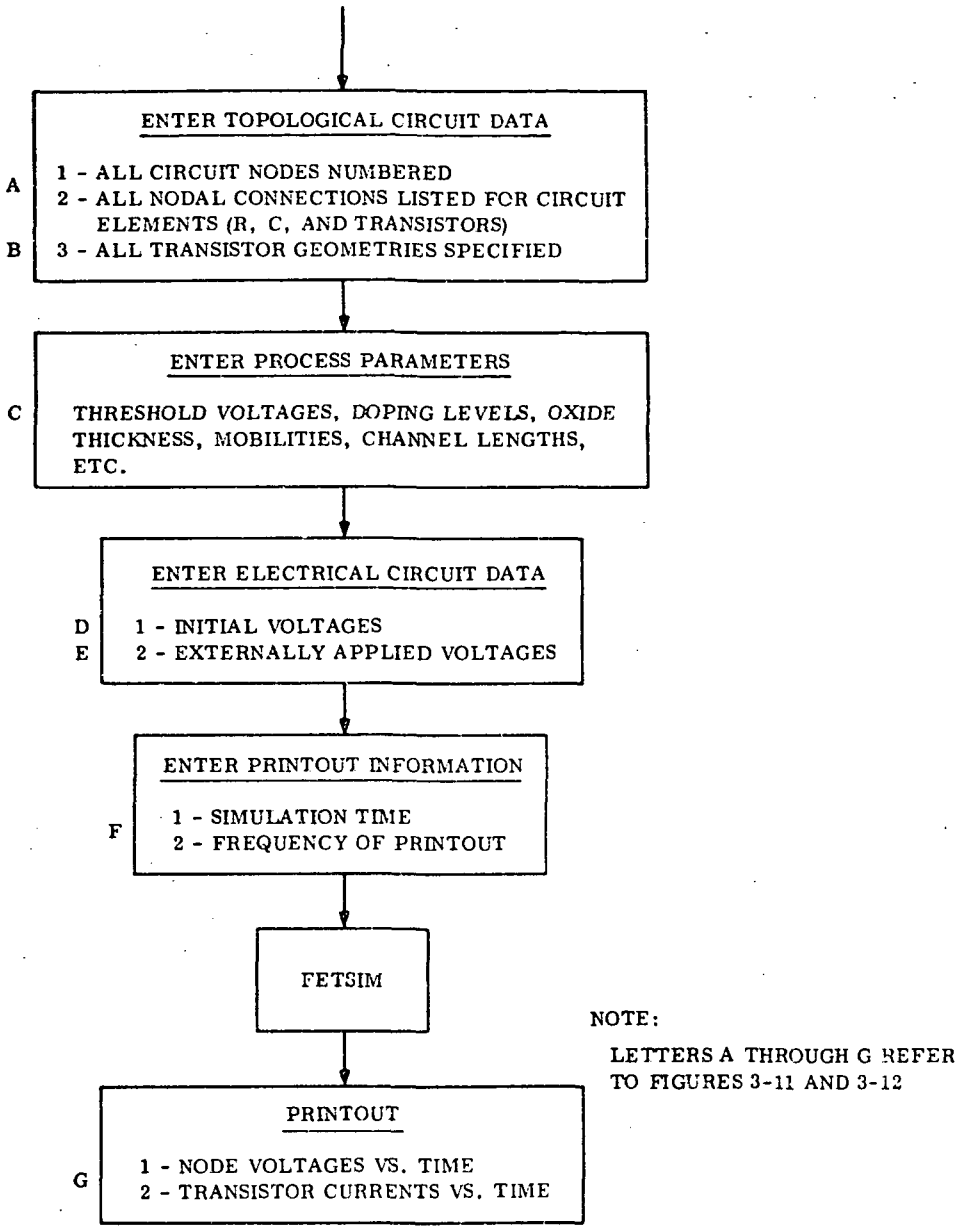


Fig. 3-8. FETSIM flowchart.

In this section the analysis of one bit of an ALU array data path is used as an example of the FETSIM circuit simulation of a complex CMOS circuit. The logic equivalent for the simulated circuit is shown in Fig. 3-9 and Fig. 3-10. In Fig. 3-9 the sequential data path passes through a 3 x 1 input multiplexer (cell 1890), through an operand true/complement select gate (1330) and an exclusive-OR of the two input operands. In Fig. 3-10 the output of the first data path is exclusive-ORed (cell 2310) with the carry input to form the sum which passes through the select gate (cell 1350) and buffers to the sum output line.

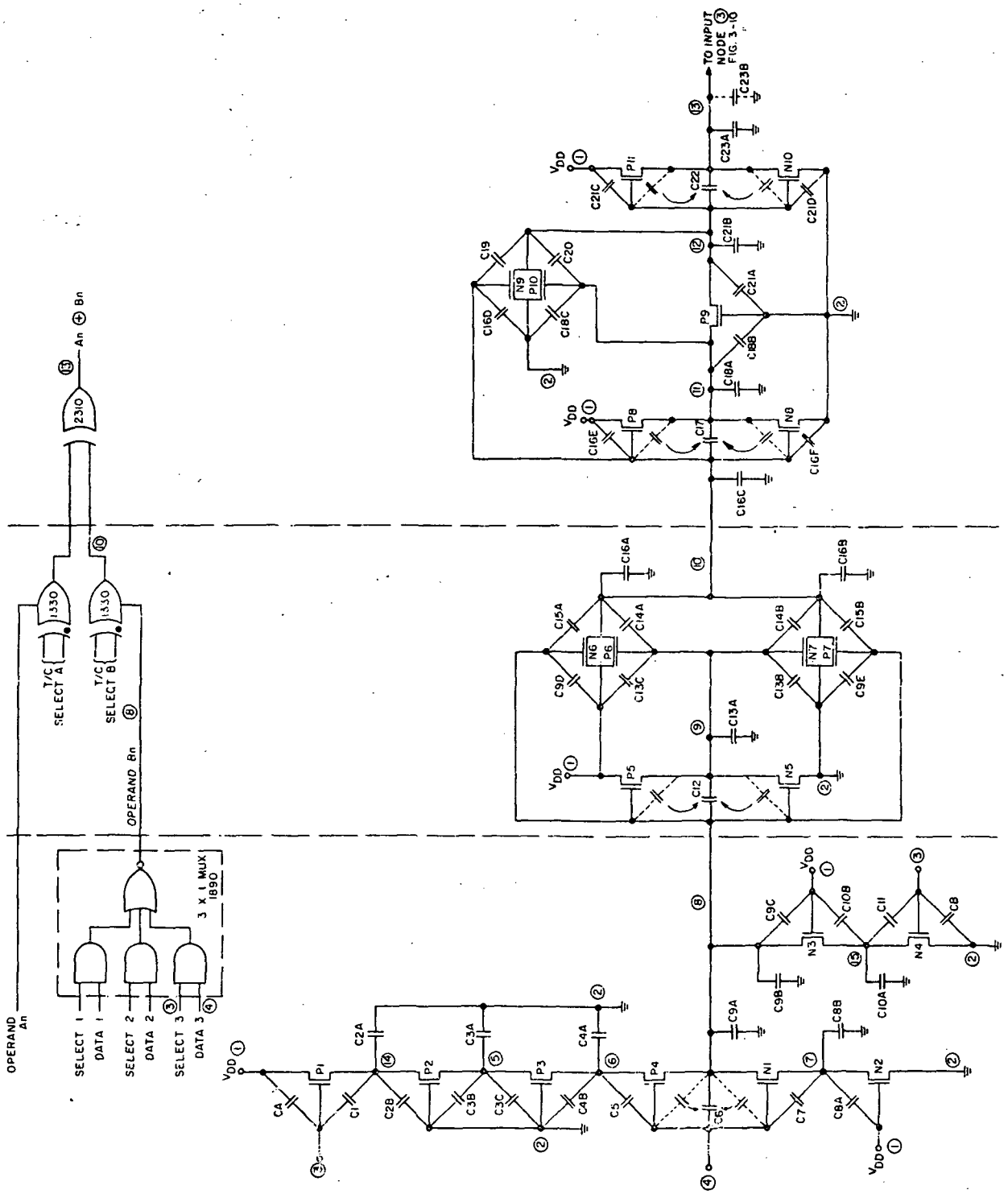


Fig. 3-9. Data path 1, logic and circuit diagram.

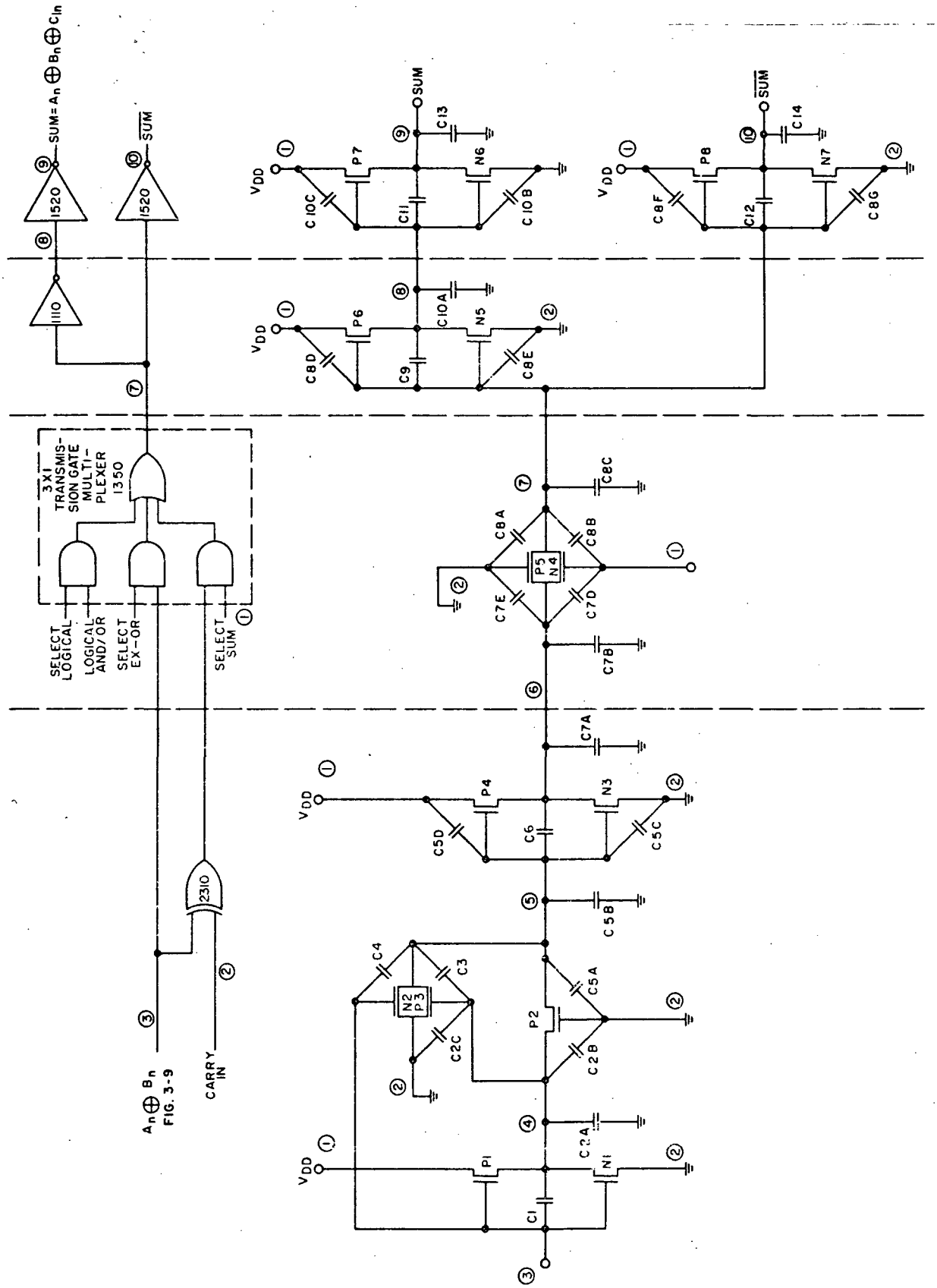


Fig. 3-10. Data path 2, logic and circuit diagram.

```
FORTRAN IV PROGRAM FETSM4 (LINK-EDITED AS FETSM4) STARTED --- 03/15/71

        NI  NO  NP  NN  NR  NC NPJL
         4  11  11  10   0  23   2

          ELEMENT       NUMBER        GATE  SOURCE  DRAIN     VT      W      L
        P TRANSISTOR       1            3     14      1    -2.50   6.60   0.19
        P TRANSISTOR       2            2      5     14    -2.50   4.60   0.19
        P TRANSISTOR       3            2      6      5    -2.50   4.60   0.19
        P TRANSISTOR       4            4      8      6    -2.50   4.60   0.19
        P TRANSISTOR       5            8      9      1    -2.50   3.00   0.19
        P TRANSISTOR       6            9     10      1    -2.50   4.50   0.19
        P TRANSISTOR       7            8     10      2    -2.50   5.50   0.19
        P TRANSISTOR       8           10     11      1    -2.50   1.80   0.19
        P TRANSISTOR       9            2     12     11    -2.50   1.80   0.19
        P TRANSISTOR      10           11     12      2    -2.50   1.80   0.19
        P TRANSISTOR      11           12     13      1    -2.50   4.10   0.19
        N TRANSISTOR       1            4      8      7     1.60   2.00   0.19
        N TRANSISTOR       2            1      7      2     1.60   2.00   0.19
        N TRANSISTOR       3            1      8     15     1.60   2.00   0.19
A, B    N TRANSISTOR       4            3     15      2     1.60   2.00   0.19
        N TRANSISTOR       5            8      9      2     1.60   2.00   0.19
        N TRANSISTOR       6            8     10      1     1.60   3.00   0.19
        N TRANSISTOR       7            9     10      2     1.60   3.60   0.19
        N TRANSISTOR       8           10     11      2     1.60   1.20   0.19
        N TRANSISTOR       9           10     12      2     1.60   1.20   0.19
        N TRANSISTOR      10           12     13      2     1.60   2.70   0.19

          ELEMENT       NUMBER             NODE A  NODE B      VALUE IN KOHMS OR PF
         CAPACITOR         1                  3      14      0.200E 00
         CAPACITOR         2                 14       7      0.120E 01
         CAPACITOR         3                  1       5      0.140E 01
         CAPACITOR         4                  1       5      0.120E 01
         CAPACITOR         5                  4       5      0.200E 00
         CAPACITOR         6                  4       8      0.300E 00
         CAPACITOR         7                  4       7      0.130E 00
         CAPACITOR         8                  7       1      0.400E 00
         CAPACITOR         9                  8       1      0.360E 01
         CAPACITOR        10                 15       1      0.400E 00
         CAPACITOR        11                 15       3      0.100E 00
         CAPACITOR        12                  8       9      0.200E 00
         CAPACITOR        13                  9       2      0.140E 01
         CAPACITOR        14                  9      10      0.500E 00
         CAPACITOR        15                  8      10      0.400E 00
         CAPACITOR        16                 10       2      0.380E 01
         CAPACITOR        17                 10      11      0.100E 00
         CAPACITOR        18                 11       2      0.110E 01
         CAPACITOR        19                 10      12      0.100E 00
         CAPACITOR        20                 11      12      0.100E 00
         CAPACITOR        21                 12       2      0.160E 01
         CAPACITOR        22                 12      13      0.300E 00
         CAPACITOR        23                 13       7      0.750E 01

        EOX    ESI        TOX     LEFFN       CONDRS    LEFFP      ACCEPT    SLOPEN    SLOPEP
C -->   4.00  12.00   0.100E-04   400.0     0.310E 16   177.0   0.130E 17    0.0000    0.0000

       PULSE   HEIGHT     BASE     DELAY     WIDTH      TAUR      TAUF      NODE
         1     10.00      0.00  0.150E-06 0.150E-06 0.150E-07 0.150E-07      3
         2    -10.00     10.00  0.000E 00 0.450E-06 0.150E-07 0.150E-07      4

         PRINT      STOP    INTERVA
        0.50E-08  0.90E-06  0.20E-09

D, E   INTERVAL     TIME     V1    V2    V3    V4    V5    V6    V7    V8    V9   V10   V11   V12   V13   V14   V15   V16   V17   V18   V19

       0.20E-09
             0.000E 00
                        10.00  0.00  0.00 10.00 10.00 10.00  0.00  0.00 10.00  0.00 10.00 10.00  0.00 10.00  0.00
       STEPS=  1  IMOS=    0.000       0.000       0.000       0.000       0.000       0.000       0.000       0.000       0.000       0.000
                           0.000       0.000       0.000       0.000       0.000       0.000       0.000       0.000       0.000       0.000
                           0.000

       0.80E-09
             0.580E-08
                        10.00  0.00  0.00  5.79  9.89  9.82 -0.08 -0.16  9.99 -0.00 10.00 10.00 -0.00  9.95 -0.15
       STEPS= 13  IMOS=    0.057       0.065       0.080       0.009       0.004       0.000       0.000       0.000       0.000       0.000
                           0.000      -0.060      -0.103      -0.007       0.000       0.000       0.000      -0.008       0.000       0.000
                           0.000

       0.80E-09
             0.114E-07
                        10.00  0.00  0.00  4.68  9.76  9.56 -0.05 -0.09 10.00  0.00 10.00 10.00  0.00  9.89 -0.10
       STEPS= 22  IMOS=    0.122      -0.149       0.210       0.258      -0.004       0.000       0.000      -0.000      -0.000       0.000
                           0.000      -0.021      -0.038       0.017       0.000       0.000       0.000       0.008       0.000       0.000
                           0.000

       0.80E-09
             0.170E-07
                        10.00  0.00  0.00  3.22  9.45  9.04  0.02  0.24 10.02  0.01 10.00 10.00  0.00  9.75  0.20
       STEPS= 26  IMOS=    0.275       0.314       0.396       0.488      -0.014       0.000       0.000      -0.000      -0.000       0.000
                           0.000       0.044       0.020       0.047       0.000       0.000       0.000       0.025       0.000       0.000
                           0.000

       0.80E-09
             0.226E-07
                        10.00  0.00  0.00  2.22  9.14  8.54  0.00  0.77 10.03  0.02 10.00 10.00  0.00  9.61  0.72
F, G   STEPS= 33  IMOS=    0.431       0.464       0.535       0.621      -0.019       0.000       0.000      -0.000      -0.000       0.000
                           0.000       0.014       0.001       0.054       0.000       0.000       0.000       0.041       0.000       0.000
                           0.000

       0.16E-08
             0.282E-07
                        10.00  0.00  0.00  1.53  9.89  8.13 -0.01  1.47 10.04  0.02 10.00 10.00  0.00  9.49  1.39
       STEPS= 39  IMOS=    0.549       0.574       0.627       0.695      -0.023       0.000       0.000      -0.000      -0.000       0.000
                           0.000       0.000      -0.010       0.004       0.000       0.000       0.000       0.051       0.000       0.000
                           0.000

       0.16E-08
             0.346E-07
                        10.00  0.00  0.00  1.00  8.69  7.79 -0.01  2.36 10.04  0.03 10.00 10.00  0.00  9.40  2.26
       STEPS= 43  IMOS=    0.541       0.657       0.693       0.742      -0.019       0.000       0.000      -0.000      -0.000       0.000
                           0.000       0.000      -0.007       0.068       0.000       0.021      -0.026       0.068       0.000       0.000
                           0.000

       0.16E-08
             0.410E-07
                        10.00  0.00  0.00  0.65  8.56  7.55 -0.00  3.31  9.95  0.07 10.00 10.00  0.00  9.34  3.15
       STEPS= 49  IMOS=    0.701       0.711       0.734       0.768       0.022       0.000       0.000      -0.001      -0.000       0.000
                           0.000       0.000      -0.004       0.070       0.000       0.111      -0.143       0.148       0.000       0.000
                           0.000

       0.32E-08
             0.474E-07
                        10.00  0.00  0.00  0.42  8.47  7.40 -0.00  4.29  9.65  0.14 10.00 10.00  0.00  9.30  4.03
       STEPS= 51  IMOS=    0.738       0.745       0.760       0.763       0.101       0.000       0.000      -0.002      -0.001       0.000
                           0.000       0.000      -0.003       0.065       0.000       0.287      -0.349       0.302       0.000       0.000
                           0.000
```

SUM PATH 1

Fig. 3-11. Input data and partial output for circuit of Fig. 3-9.

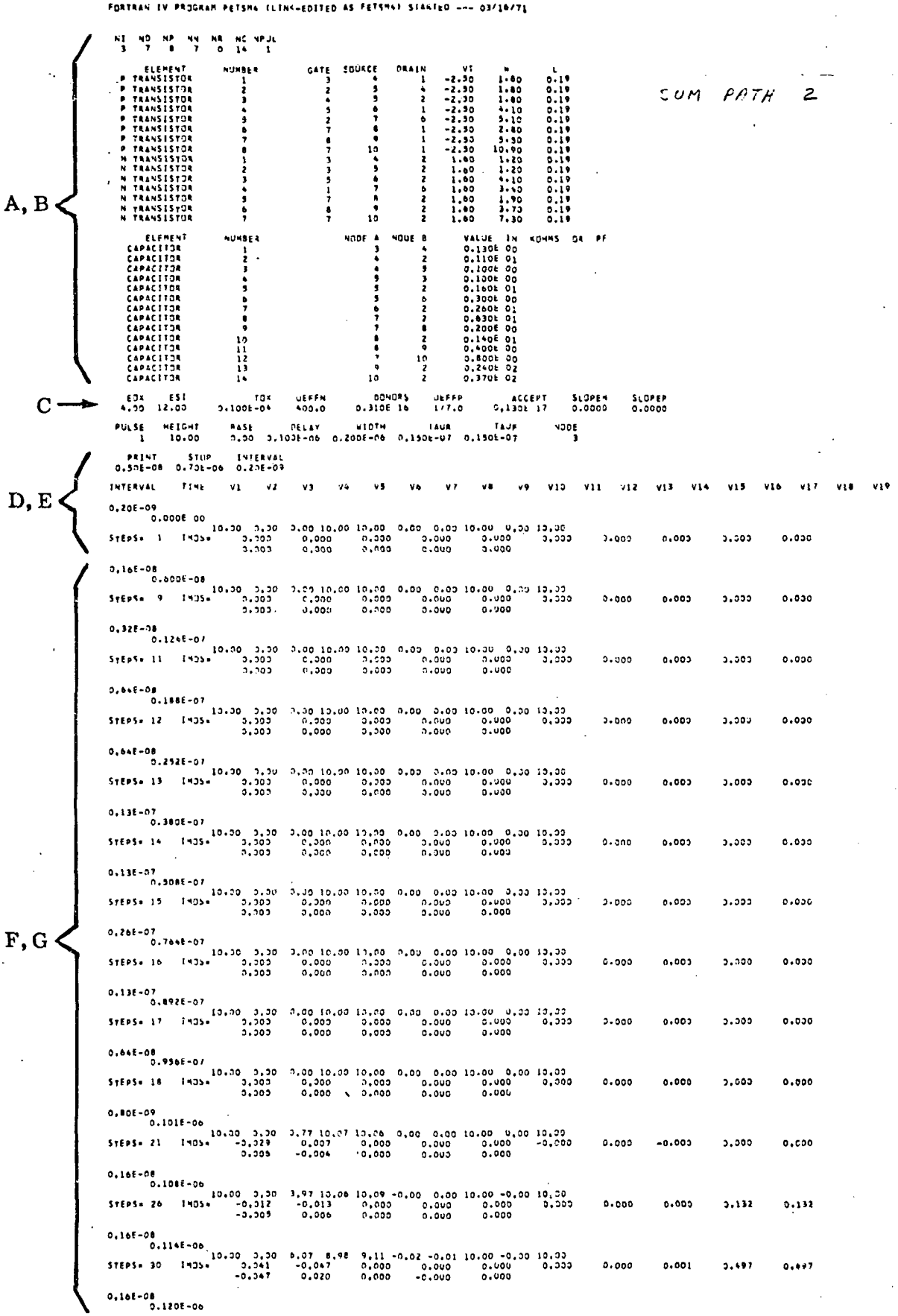


Fig. 3-12. Input data and partial output for circuit of Fig. 3-10.

The simulation results, using almost worst case processing parameters for both N and P type devices, indicate a one-bit add time of 194 nanoseconds; 105 ns required for path 1 and 89 ns for path 2.

The first two pages of printout of the simulation of data paths 1 and 2 are listed in Fig. 3-11 and 3-12, respectively. The correlation of the printout to the flowpath, Fig. 3-8, is given by the letters A through F on the flowpath and the printouts.

3. Automatic Test Sequence Generation - Application of the AGAT Computer Program to the ALU Array

AGAT (Automatic Generation of Array Tests) is a computer program designed to generate a complete set of tests for a combinatorial logic net. The complete set of tests will examine the logic net for every possible fault. Faults are defined as gate inputs and outputs that are stuck at a logical "1" or a logical "0" condition. AGAT automatically derives these tests from a user's input data which describes the logic connectivity of the array. Each individual test specifies a complete set of net levels (0 or 1) to be applied to the array, and the corresponding normal net output levels. In addition to generating the inputs necessary to completely exercise the LSI array, AGAT also provides sufficient diagnostic data to isolate internal faults, generally two within several gates. The procedure for using the AGAT program is shown in the flowchart of Fig. 3-13.

Although AGAT was primarily designed for combinational logic, it has been used successfully with sequential circuitry. In this case the engineer generates the test words necessary to prime the logic for the desired internal states. The logical connectivity data is then entered as if the array is combinatorial. Further simplicity of testing is achieved by designing all sequential arrays so that all internal feedback loops can be broken. This permits the forced setting of all internal states simplifying the test sequence requirements of the AGAT program.

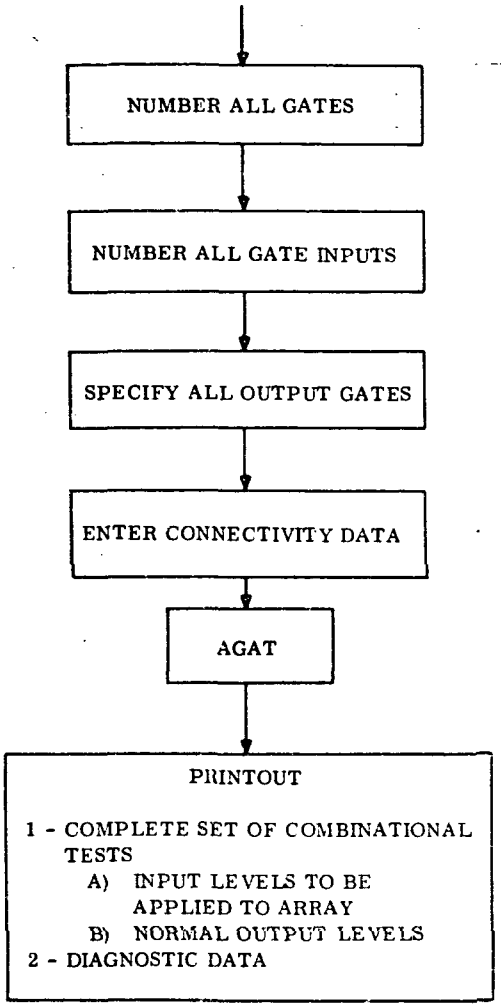


Fig. 3-13. User flowchart for AGAT.

To generate the test sequence, the AGAT program selects an untested fault and places appropriate levels at the inputs and outputs of the gate containing the selected fault. This process is continued until levels have been assigned to all gates in the sensitized path, thus permitting observation of the selected fault at a net output.

Output data is presented to the user in the form of a printout. Each AGAT run presents the user with connectivity lists, load lists, fault tables, and a list of untested faults (if any).

The AGAT program has been used as an aid in generating the test sequences for arrays containing sequential logic. It has been used to produce the entire test sequence for many combinational arrays such as the Arithmetic Logic Unit (ATL-004A).

Figure 3-14 shows the input logic used to set up the connectivity data for ALU array. As shown, the array has 23 inputs, 13 outputs, 156 internal nodes, and 192 logical gates. All the inputs to the array have been numbered arbitrarily from 500 to 522 and all array outputs have been labeled with an X.

The AGAT output for the ALU array contained 27 combinatorial tests and conflict messages. The conflict messages were traced to redundant logic configurations within the array. (Redundant logic configurations are inherently untestable by any method.) The 27 combinatorial tests, therefore, form a complete test set.

Figure 3-15 shows the AGAT output for one of these 27 tests. In this test, for example, the inputs numbered 500, 501 and 502 are set at 0, 0, and 1 (respectively). The outputs, numbered 133, 135, 136 will be 0, 0 and 1 (respectively) if the array is to pass this test. The large block of data in the middle of this page of printout is the logical levels for all internal nodes of the array.

When the array under test has passed all 27 tests, the array is functionally perfect.

B. STATIC AND DYNAMIC PERFORMANCE OF THE CMOS LSI CHIPS

Static and dynamic tests have been conducted on nine of the CMOS LSI chip types used in the SUMC-DV. The following paragraphs describe the tests that were performed and typical results for each of the tests.

The tests conducted on the LSI chips fall into the categories of functional testing, leakage tests, life tests and propagation delay. All tests were conducted with a 10-V supply voltage and 10-V input pulses (where applicable). In addition, propagation delay measurements on the ATL-001A Product Result Register (PRR) and the ATL-002A Multiply Quotient Register (MQR) were made with a 5-V input pulse. All of the chips tested were housed in 40-pin dual-in-line ceramic packages with 0.600-inch row centers and 0.100-inch pin spacing.

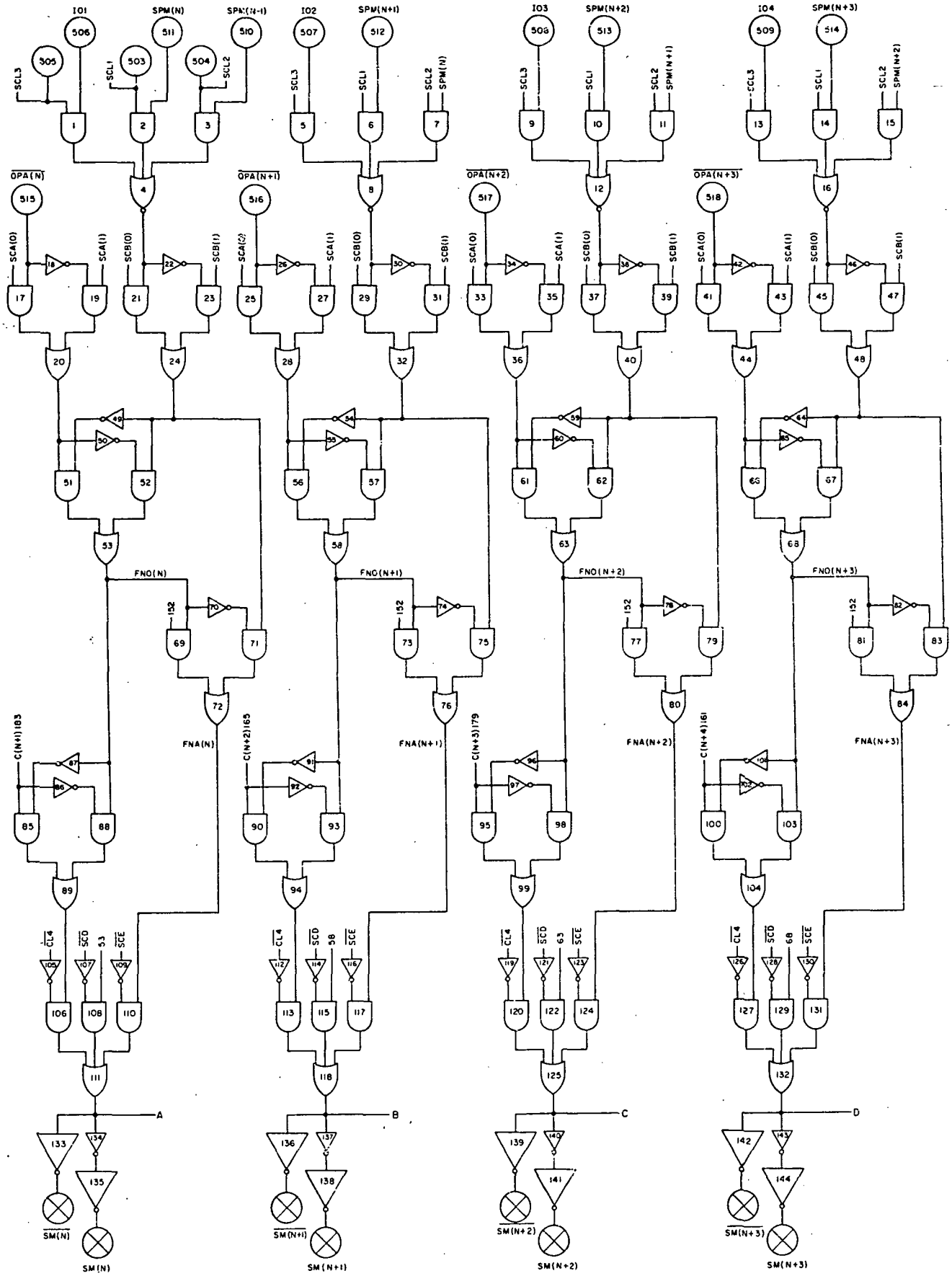


Fig. 3-14. AGAT connectivity drawing, ALU (ATL-004A), (sheet 1 of 2).

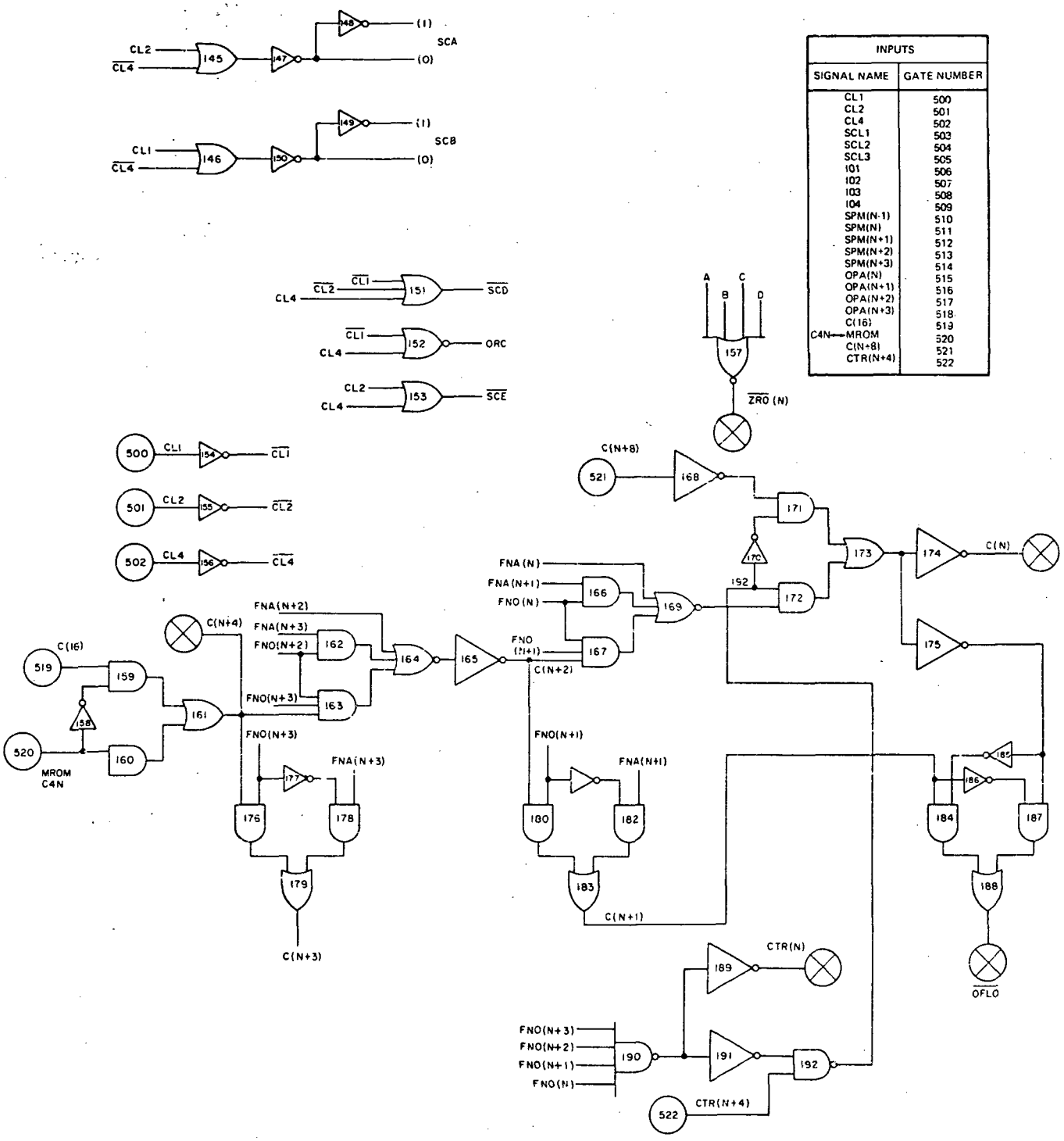


Fig. 3-14. AGAT connectivity drawing, ALU (ATL-004A), (sheet 2 of 2).

```
DATA-TEST NO. = 5

FAULT MODE INDICATOR TOTALS . . . . . SEE LEGEND
(-1) 0; (0) 206; (1) 313; (2) 40; (3) 152

INITIAL FM GATE = 3 MI LIST INPUT = 0

23 INPUTS (NET INPUT-LEVEL)
500 0 501 0 502 1 503 1 504 1 505 0 506 1 507 1 508 1 509 0 510 1 511 0 512 1 513 0 514 0
515 0 516 1 517 1 518 0 519 0 520 1 521 1 522 0

13 OUTPUTS (GATE NO. - NET OUTPUT LEVEL
133 0 135 1 136 1 138 0 139 1 141 0 142 1 144 0 157 1 161 1 176 0 158 1 189 0

(GATE NO. - OUTPUT LEVEL)
  1 0   2 0   3 1   4 0   5 0   6 1   7 0   8 0   9 0  10 0  11 0  12 0  13 0  14 0  15 0
 16 1  17 0  18 1  19 0  20 0  21 0  22 1  23 0  24 0  25 1  26 0  27 0  28 1  29 0  30 1
 31 0  32 0  33 1  34 0  35 0  36 1  37 0  38 1  39 0  40 0  41 0  42 1  43 0  44 0  45 1
 46 0  47 0  48 1  49 1  50 1  51 0  52 0  53 0  54 1  55 0  56 1  57 0  58 1  59 1  60 0
 61 1  62 0  63 1  64 0  65 1  66 0  67 1  68 1  69 0  70 1  71 0  72 0  73 0  74 0  75 0
 76 0  77 0  78 0  79 0  80 0  81 0  82 0  83 0  84 0  85 1  86 0  87 1  88 0  89 1  90 0
 91 0  92 0  93 0  94 0  95 0  96 0  97 0  98 0  99 0 100 0 101 0 102 0 103 0 104 0 105 1
106 1 107 0 108 0 109 0 110 0 111 1 112 1 113 0 114 0 115 0 116 0 117 0 118 0 119 1 120 0
121 0 122 0 123 0 124 0 125 0 126 1 127 0 128 0 129 0 130 0 131 0 132 0 133 0 134 0 135 1
136 1 137 1 138 0 139 1 140 1 141 0 142 1 143 1 144 0 145 0 146 0 147 1 148 0 149 0 150 1
151 1 152 0 153 1 154 1 155 1 156 0 157 0 158 0 159 0 160 1 161 1 162 0 163 1 164 0 165 1
166 0 167 0 168 0 169 1 170 0 171 0 172 1 173 1 174 0 175 0 176 1 177 0 178 0 179 1 180 1
181 0 182 0 183 1 184 1 185 1 186 0 187 0 188 1 189 0 190 1 191 0 192 1

SIMULATION TIME = 2583 MILLISECONDS                    192 LOGICAL GATES
```

Fig. 3-15. AGAT output for one ALU test sequence.

1. Functional Testing

All of the LSI chips of each chip type have had the functionality of their internal logic tested. The AGAT computer program was used to generate a test sequence for each SUMC-DV chip type. The application of the AGAT program to generating the test sequence for the ALU chip is detailed in Section IIIA3. The test sequence not only verifies that the finished array performs the required logic function, but also checks every gate in the system for the stuck at "1" or stuck at "0" case. The test bit sequences generated by AGAT were programmed into a programmable tester, which not only tested the chips for proper operation, but also identified those outputs where the error occurred and the corresponding bit sequences which resulted in an error condition.

2. Leakage

Static leakage current was measured in the ground lines of each of the nine LSI chip types. Leakage current was measured first with all chip inputs tied to the supply voltage (+10 V) and then with all chip inputs tied to ground. Figure 3-16 shows the test setup used in the static leakage test. The median static leakage for each of the chip types is shown in Fig. 3-17 along with number of units tested of each chip type.

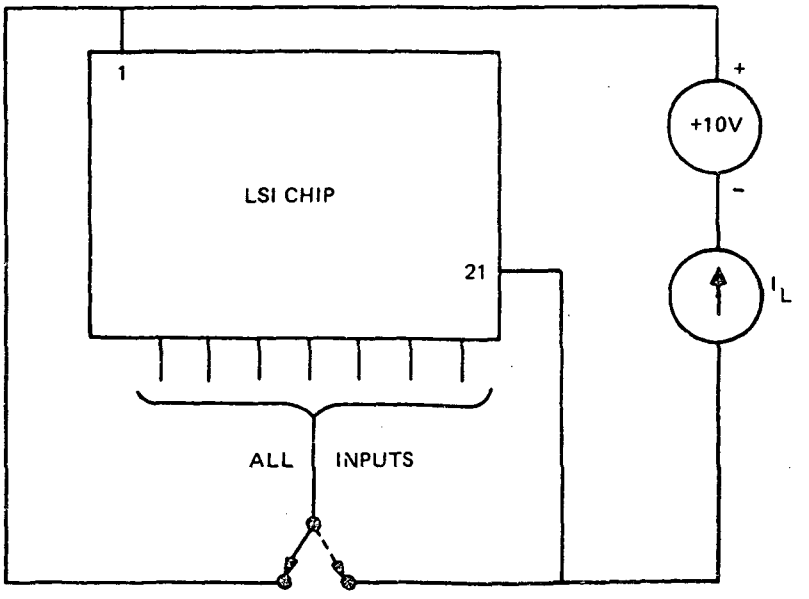


Fig. 3-16. Static leakage test setup.

CHIP TYPE	MEDIAN STATIC LEAKAGE (μA)	NO. OF CHIPS TESTED
ATL-001A	<1	99
ATL-002A	<1	51
ATL-004A	325	22
ATL-005	10	16
ATL-006A	8	21
ATL-007A	462	22
ATL-008A	750	21
ATL-009A	22	8
ATL-010A	9	15

Fig. 3-17. Median static leakage.

Dynamic leakage was measured in the ground line of four ATL-001A and four ATL-002A chips. The logic diagrams of the ATL-001A and ATL-002A are presented in Fig. 3-18 and 3-19. As can be seen from Fig. 3-18, the ATL-001A has four primary data paths each containing a master/slave flip-flop (cell 1820). Dynamic leakage was measured on the ATL-001A while all four flip-flops were being simultaneously clocked with clock frequencies up to 1 MHz. This was done in an attempt to maximize the dynamic power loss. The ATL-002A also has four primary data paths containing master/slave flip-flops. In addition, the ATL-002A contains four "D" type flip-flops (cell 1830). Dynamic leakage was measured in the ATL-002A while all eight of its flip-flops were being simultaneously clocked at clock frequencies of up to 1 MHz.

The results of the dynamic leakage tests on the four ATL-001A and four ATL-002A chips are presented in Fig. 3-20 as a graph of average power dissipation versus frequency for the two chip types. The results in Fig. 3-20 are for the case where no capacitive loading is associated with any of the outputs other than the intrinsic output capacitance of the chip and the packaging socket capacitance. Since, on a CMOS chip, the dynamic power can be expressed as CV^2f, the addition of external output capacitance will increase the dynamic power consumption.

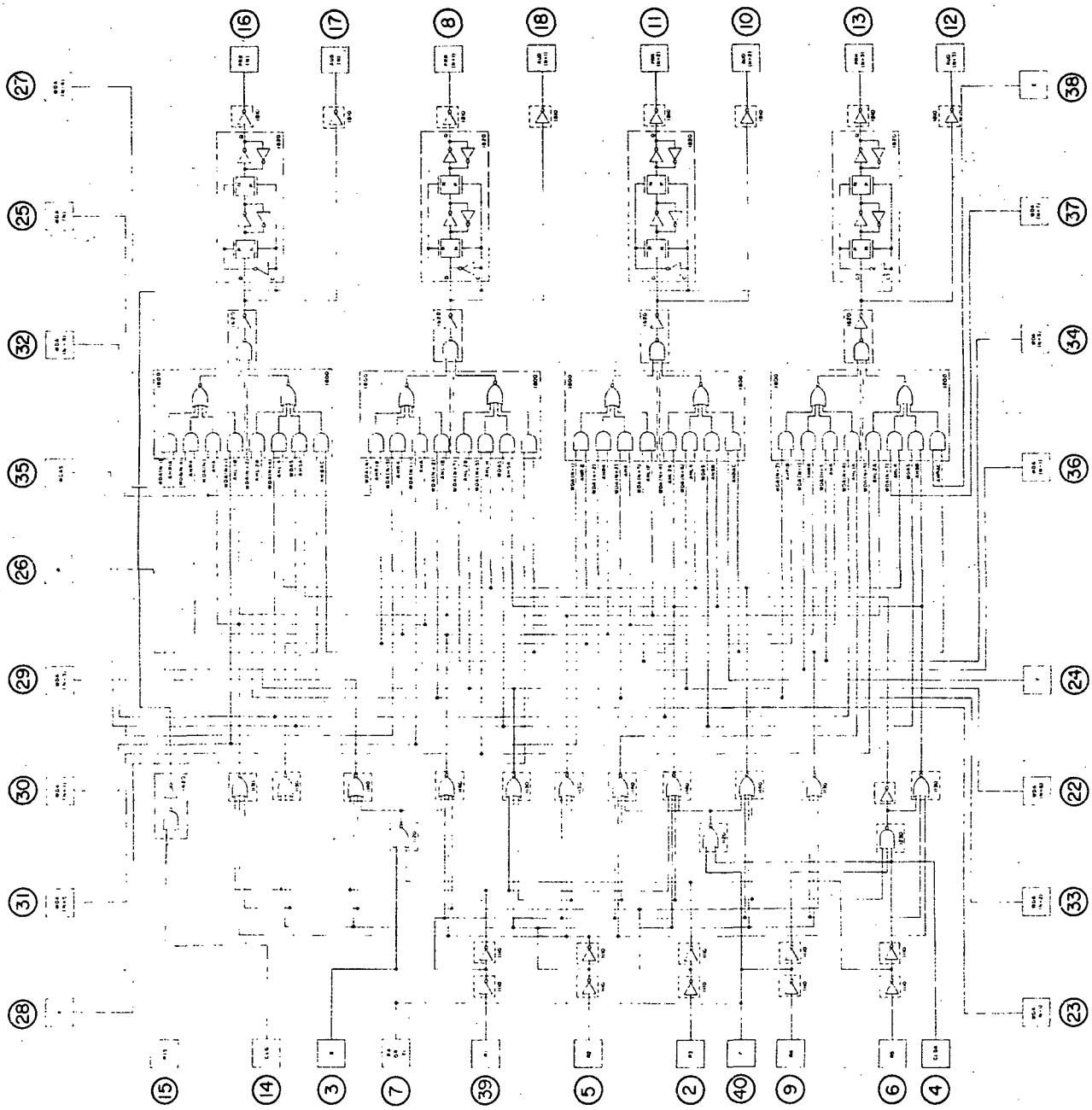


Fig. 3-18. ATL-001A logic diagram.

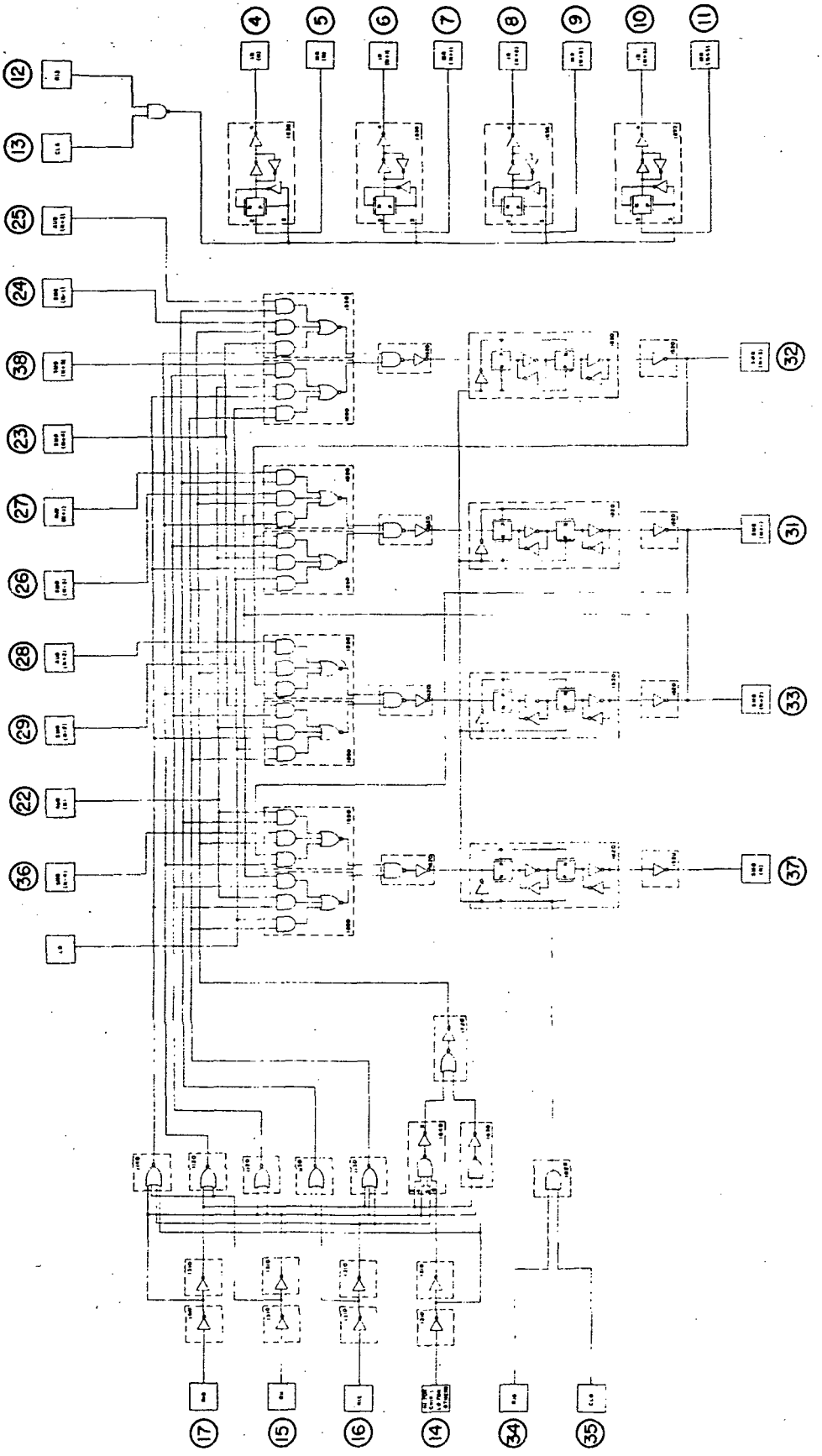


Fig. 3-19. ATL-002A logic diagram.

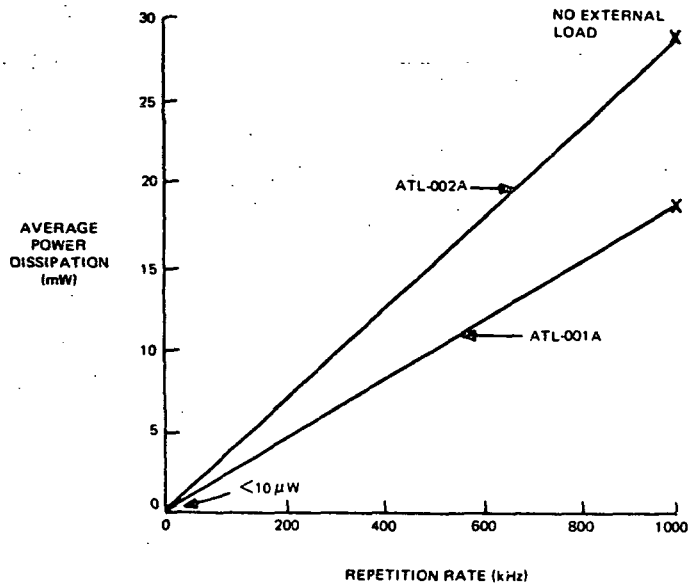


Fig. 3-20. Power dissipation vs frequency.

3. Life Tests

A static leakage life test at elevated temperatures has been conducted on two ATL-001A chips to check the effect that continual temperature and voltage stress has on the leakage characteristics. Static leakage has been measured as per Fig. 3-16 with all inputs tied to ground. In addition to measuring leakage on the PRR chips, provisions had been made to check the dynamic performance of these same chips while under temperature stress. Figure 3-21 contains condensed data on the static leakage test taken during the first 200 days of testing. Future test plans for these two chips include provisions for an accelerated temperature cycling routine over a more extreme temperature range.

Two additional CMOS LSI standard cell chips, the ATL-NASA test chip and the ATL-000, have been under continuous dynamic stress at 25°C for 200 days. No degradation in dynamic performance has occurred.

4. Propagation Delay

Propagation delay measurements have been conducted on each of the nine LSI chip types. This section presents some of the typical delay paths examined for each chip type along with the mean average delay measurements, output line node

DAYS SINCE TEST BEGAN	TEMPERATURE (°C)	LEAKAGE TEST CHIP 1 (μA)	LEAKAGE TEST CHIP 2 (μA)
0	25	25	0.014
1	60	33	0.055
5	60	41	0.160
35	60	42	0.200
63	60	42	0.200
64	85	43.5	0.210
109	85	43.5	0.190
110	100	46	0.230
166	100	46	0.300
167	25*	39.5	0.260
200	25*	38.5	0.260

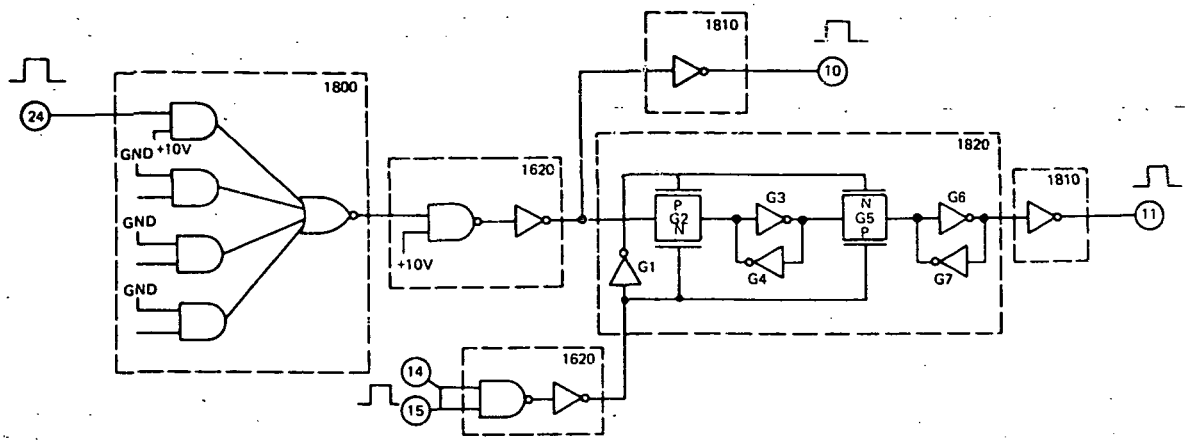
*Equipment shut down during laboratory move.

Fig. 3-21. Condensed life test, static leakage at elevated temperatures.

capacitance and stage delays. All chip types were tested using a 10-volt supply voltage. In addition, the ATL-001A and ATL-002A were also tested with a 5-volt supply voltage. The input driving waveforms for all tests had 10%-90% rise and fall times of 40 ns. Propagation delay was measured between the 50% points of the input and output waveforms.

a. ATL-001A

The ATL-001A chip type (shown in Fig. 3-18) contains four primary data paths each containing a D-type master-slave register (cell 1820). Four delay measurements were made on one of these paths. The test path is shown in Fig. 3-23. The 1820 master-slave flip-flop cell is used on the 001A, 002A and 009A chips. The flip-flops, shown in detail in Fig. 3-22, is a single input register in which not only can the data, D, be jam-transferred into the master register (the combination of G3 and G4), but the input can also be multiplexed from a common bus because of G2, which is used to isolate the D input line from the master register. The jam-transfer capability with a single input arises out of the special high impedance (low capacitance) characteristics of the CMOS technology combined with the



OPERATING VOLTAGE (volts)	T (ns) IN OUT	T (ns) IN OUT	OUTPUT NODE CAPACITANCE (pF)	NUMBER OF STAGES	AVERAGE STAGE DELAY T_1 (ns)	AVERAGE STAGE DELAY T_2 (ns)	NUMBER OF CHIPS TESTED
	⌐-24 ⌐-11	⌊-24 ⌊-11	RIPPLE THROUGH TEST				
10	*140	*115	10.9	8	17.5	14.4	9
10	*162	*129	28.9		20.3	16.1	9
5	*500	*350	10.9		62.5	43.8	8
5	*560	*380	28.9		70	47.5	8
	⌊-14 ⌐-11	⌊-14 ⌊-11	CLOCK-OUT TEST				
10	68	50	10.5	6	11.3	8.3	25
10	90	66	28.5		15	11	25
5	245	107	10.5		40.8	17.8	8
5	306	132	28.5		51	22	8
	⌐-24 ⌐-10	⌊-24 ⌊-10	DIRECT FEED THROUGH TEST				
10	67	82	11.1	4	16.8	20.5	25

*Includes setup time on both master and slave inputs.

Fig. 3-22. Propagation delay tests on the ATL-001A.

special design of the G2 and G4 gates. The G4 gate is designed with very low conductance devices that keep the output impedance of G4 high enough so that it can be driven directly from the data, D, through G2; but low enough so that it can hold stored data in the master register, which consists of G3 and G4. Gate G5 is a bidirectional switch that is used to isolate the slave register, G6, and G7, when new data is being stored in the master.

Three delay measurements were made on the 1820 cell in the data path of Fig. 3-22. The three tests are designated: (1) the "ripple through" test, (2) the "clock-out" test, and (3) the "minimum clock pulse width" test. The "ripple through" time is the minimum time necessary to place a bit of information at a chip input (pin 24 for the ATL-001A), clock the information first into the master and then into the slave of the 1820 cell, and to receive this information at the chip output (pin 11

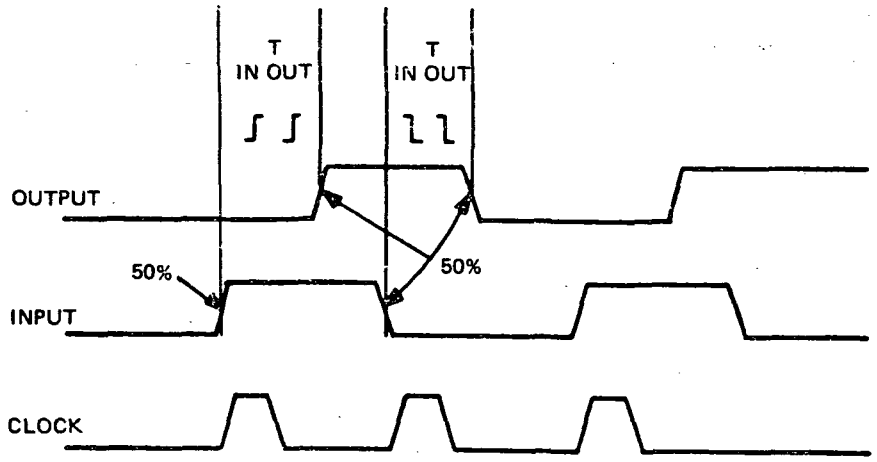


Fig. 3-23. "Ripple through" timing waveforms.

for the ATL-001A). The timing waveforms for the "ripple through" test are shown in Fig. 3-23. The test data for the "ripple through" test on the ATL-001A is presented in Fig. 3-22.

The "clock-out" time is the time delay between the application of the clock edge which passes the cell 1820 master information to the slave and the appearance of the slave information at the chip output. Pictorially, the "clock-out" timing waveforms are shown in Fig. 3-24. The "clock-out" test data taken on the ATL-001A chip types is presented in Fig. 3-22.

The third test conducted on the cell 1820 flip-flop was the determination of the minimum width clock pulse necessary to pass information from the data D input into the master of the cell 1820 flip-flop. For 10- volt ATL-001A chip operation, the minimum clock pulse width averaged 22 ns. Reducing the supply voltage to 5 volts increased the average minimum allowable clock pulse width to 80 ns.

Test data for one combinatorial logic path in the ATL-001A is presented in Fig. 3-22. The test is designated as the "direct feed through" test. In this test the propagation delay was measured from chip input pin 24 to chip output pin 10. Four internal levels of logic were involved with this path.

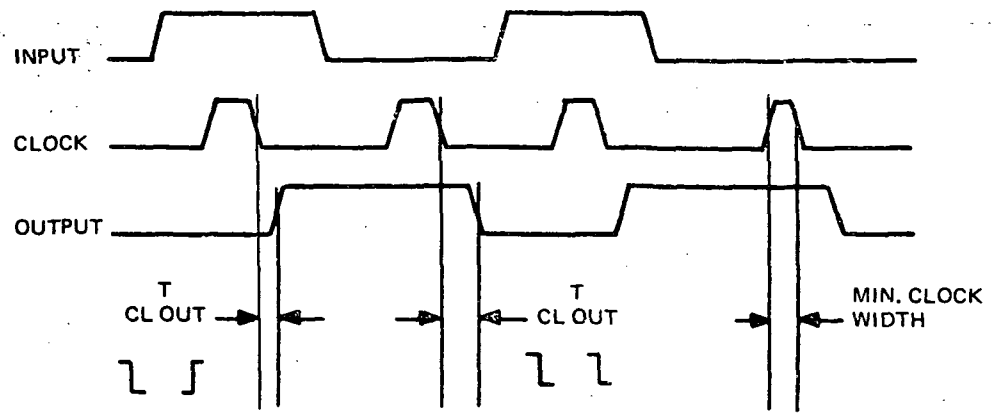


Fig. 3-24. "Clock-out" and "minimum clock pulse width" timing waveforms.

b. ATL-002A and ATL-009A

The "ripple through" test and the "clock-out" test were run on data paths containing the cell 1820 master-slave flip-flop on both the ATL-002A and ATL-009A chip types. The data paths and test results for these two chip types are shown in Fig. 3-25 and 3-27. Figure 3-26 represents the logical layout of the ATL-009A chip.

c. ATL-004A, ATL-005, ATL-006A, ATL-007A, ATL-008A and ATL-010A

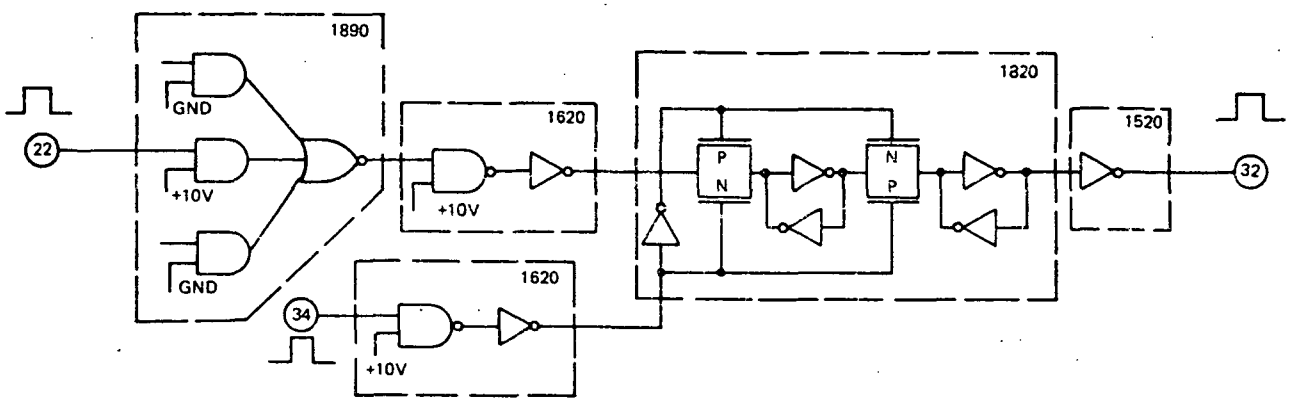
The remaining six chip types all contain logic paths that are combinatorial or that can be viewed as combinatorial for purposes of propagation delay measurements. Figures 3-28 through 3-48 present the logic diagrams, propagation delay test paths, and test results of the remaining six chip types. All of the test results represent mean average values of recorded data using a 10-volt supply voltage.

5. Summary of Chip Propagation Delay Measurements

The results of the stage delay measurements calculated for each of the test paths are summarized in Fig. 3-49 on a "chip type" level. The average stage delay for each chip type was arrived at by averaging the stage delays of the individual test paths measured for each chip type. The data in Fig. 3-49 is based on test results

taken with a +10 V chip supply voltage and a chip output node capacitance in the 10- to 15-pF range.

Also included in Fig. 3-49 is the average stage delay that can be attributed to all nine of the CMOS LSI chip types taken collectively. Based on the results of 6664 stages, the average stage delay was found to be 16.7 ns.



RIPPLE THROUGH PATH							
SUPPLY VOLTAGE (VOLTS)	OUTPUT NODE CAPACITANCE (pF)	T(ns) 22 32 ⎍ ⎍	T(ns) 22 32 ⎎ ⎎	NUMBER OF STAGES	AVERAGE STAGE DELAY (ns) ⎍ ⎍	AVERAGE STAGE DELAY (ns) ⎎ ⎎	NUMBER OF CHIPS TESTED
10	14.3	125	110	8	15.6	13.8	22
5	14.3	244	212	8	30.5	26.5	3
CLOCK-OUT PATH							
SUPPLY VOLTAGE (VOLTS)	OUTPUT NODE CAPACITANCE (pF)	T(ns) 34 32 ⎎ ⎍	T(ns) 34 32 ⎎ ⎎	NUMBER OF STAGES	AVERAGE STAGE DELAY (ns) ⎎ ⎍	AVERAGE STAGE DELAY (ns) ⎎ ⎎	NUMBER OF CHIPS TESTED
10	14.3	55	47	6	9.2	7.8	22
5	14.3	113	101	6	18.3	16.8	3

Fig. 3-25. Propagation delay tests on the ATL-002A.

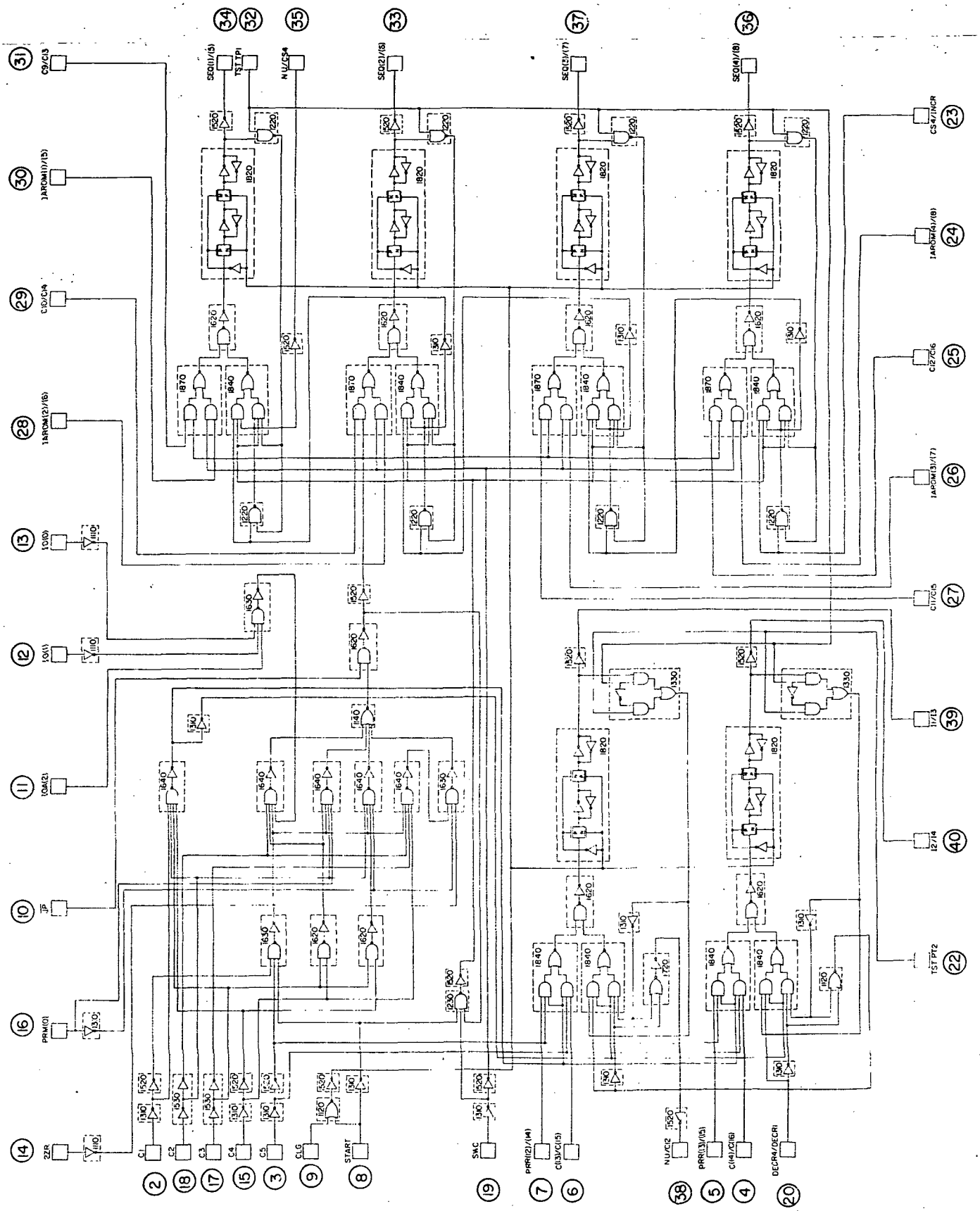
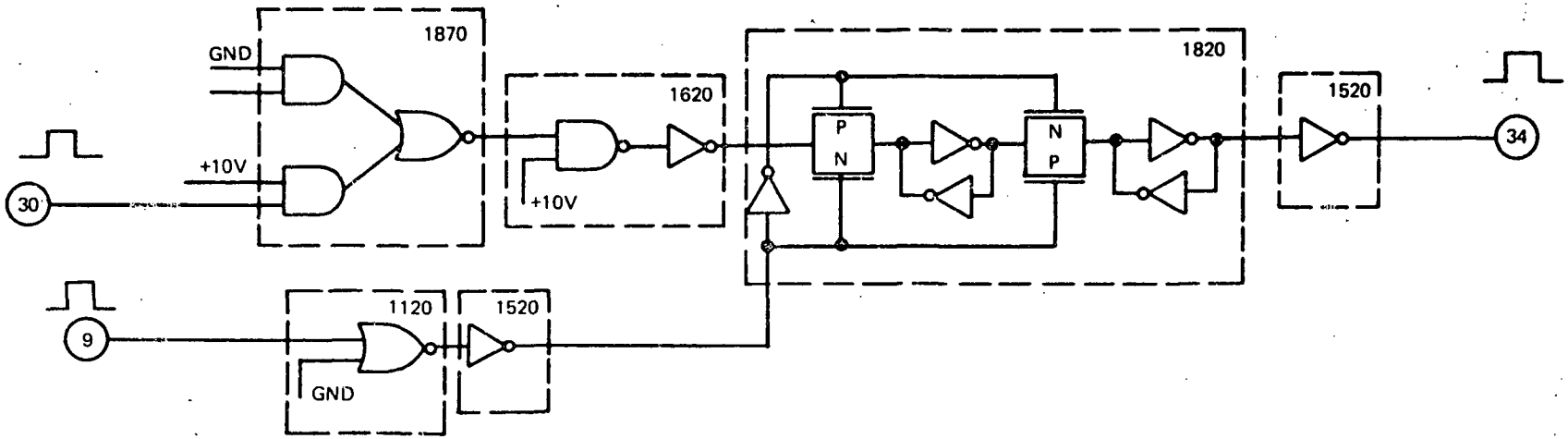


Fig. 3-26. ATL-009A logic diagram.



OUTPUT NODE CAPACITANCE	RIPPLE THROUGH PATH					NUMBER OF CHIPS TESTED
	T 30 34 ⌐¬⌐¬	T 30 34 ¬⌐¬⌐	NUMBER OF STAGES	AVERAGE STAGE DELAY ⌐¬⌐¬	AVERAGE STAGE DELAY ¬⌐¬⌐	
10.5 pF	*174 ns	*133 ns	8	*21.8 ns	*16.6 ns	9
	CLOCK-OUT PATH					
	T 9 34 ¬⌐⌐¬	T 9 34 ¬⌐¬⌐	NUMBER OF STAGES	AVERAGE STAGE DELAY ¬⌐⌐¬	AVERAGE STAGE DELAY ¬⌐¬⌐	
	158 ns	119 ns	6	26.3 ns	19.5 ns	

*Includes setup time on master and slave inputs.

Fig. 3-27. Propagation delay tests on the ATL-009A.

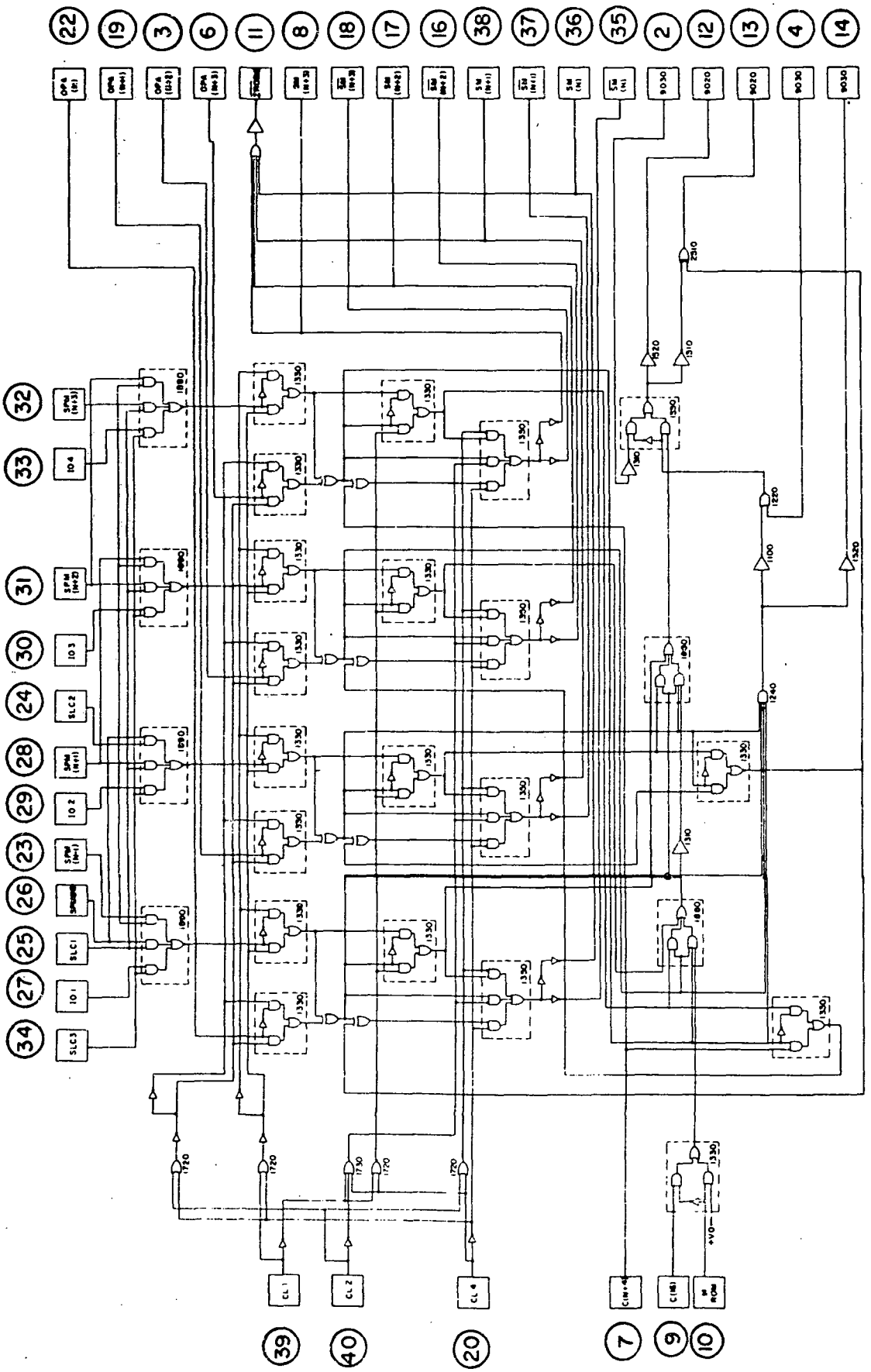
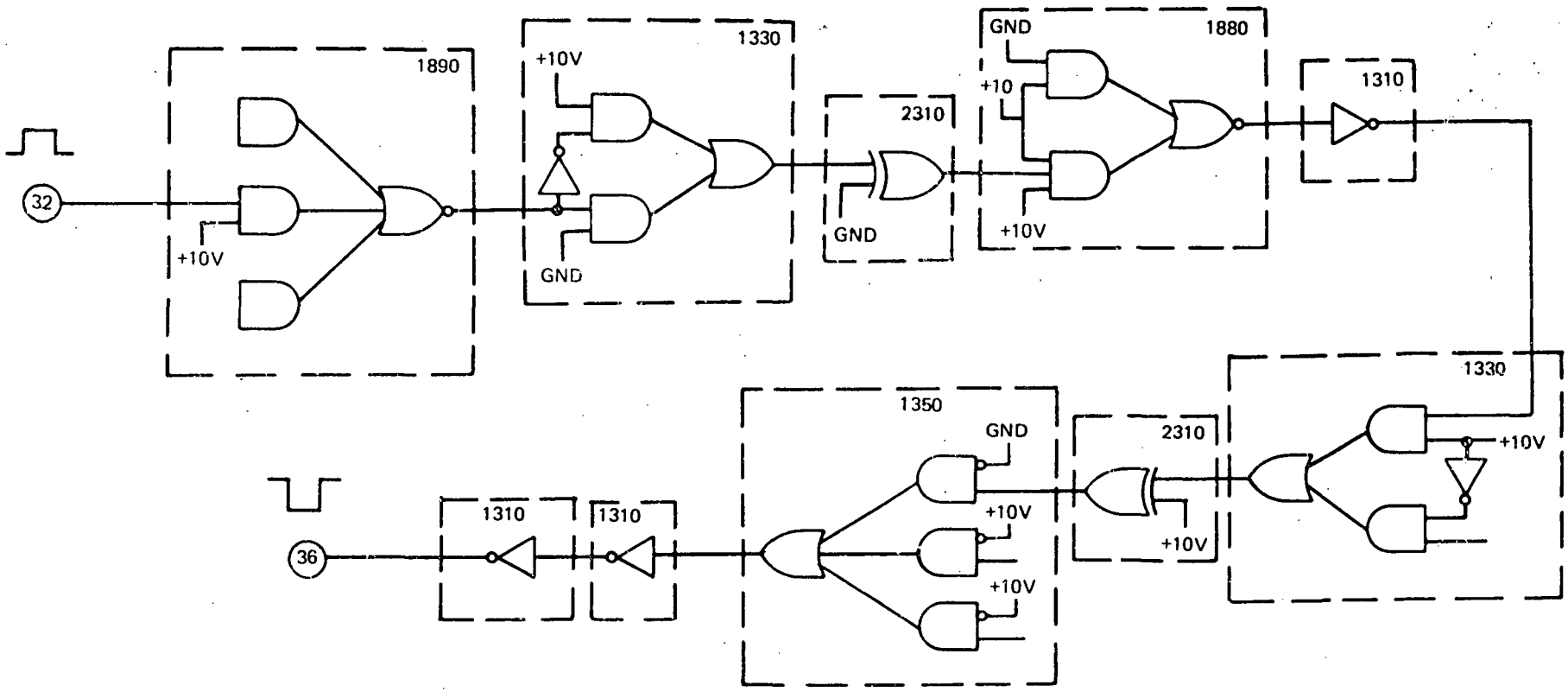
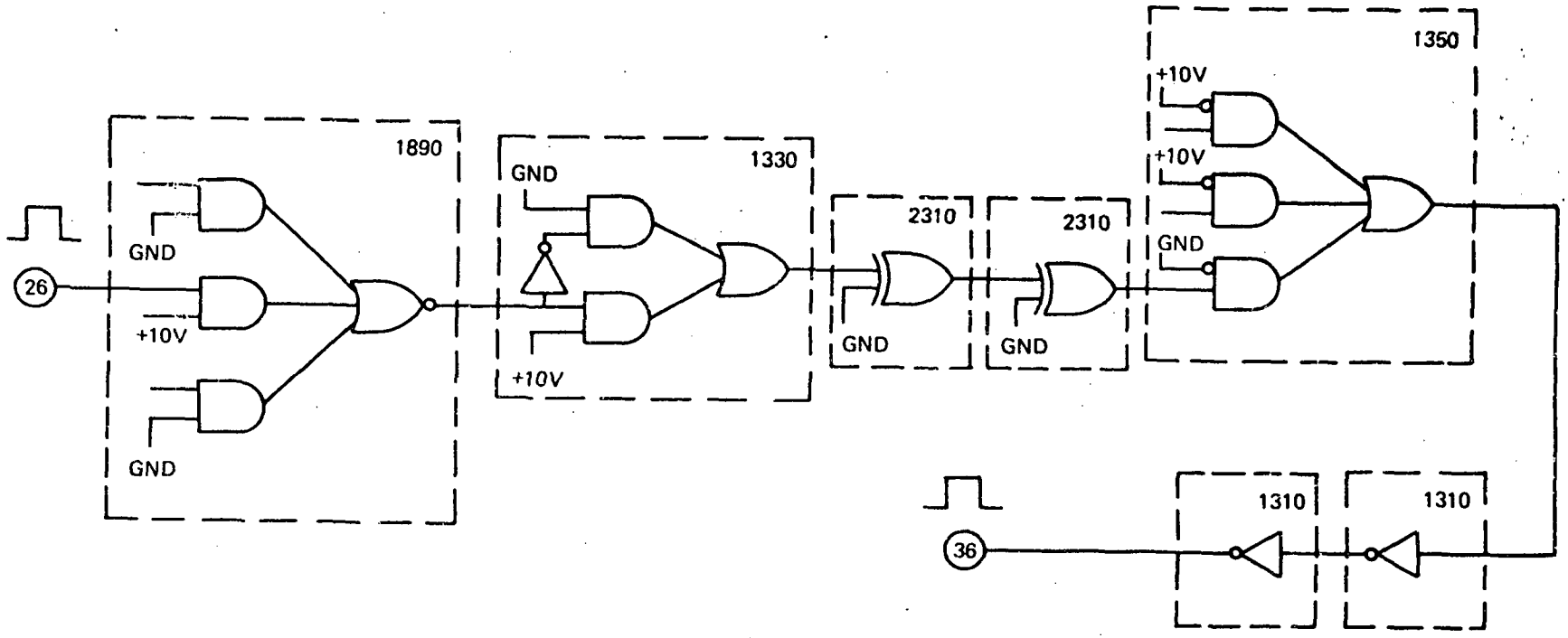


Fig. 3-28. ATL-004A logic diagram.



OUTPUT NODE CAPACITANCE	T 32 36 ⌐¬	T 32 36 ¬⌐	NUMBER OF STAGES	AVERAGE STAGE DELAY ⌐¬	AVERAGE STAGE DELAY ¬⌐	NUMBER OF CHIPS TESTED
11.2 pF	351 ns	374 ns	15	23.4 ns	25 ns	24

Fig. 3-29. Propagation delay through a four-bit add/carry path.



OUTPUT NODE CAPACITANCE	T 26 36 ⌐¬	T 26 36 ¬⌐	NUMBER OF STAGES	AVERAGE STAGE DELAY ⌐¬	AVERAGE STAGE DELAY ¬⌐	NUMBER OF CHIPS TESTED
11.5 pF	266 ns	254 ns	12	22.2 ns	21.2 ns	25

Fig. 3-30. Propagation delay through add path on the ATL-004.

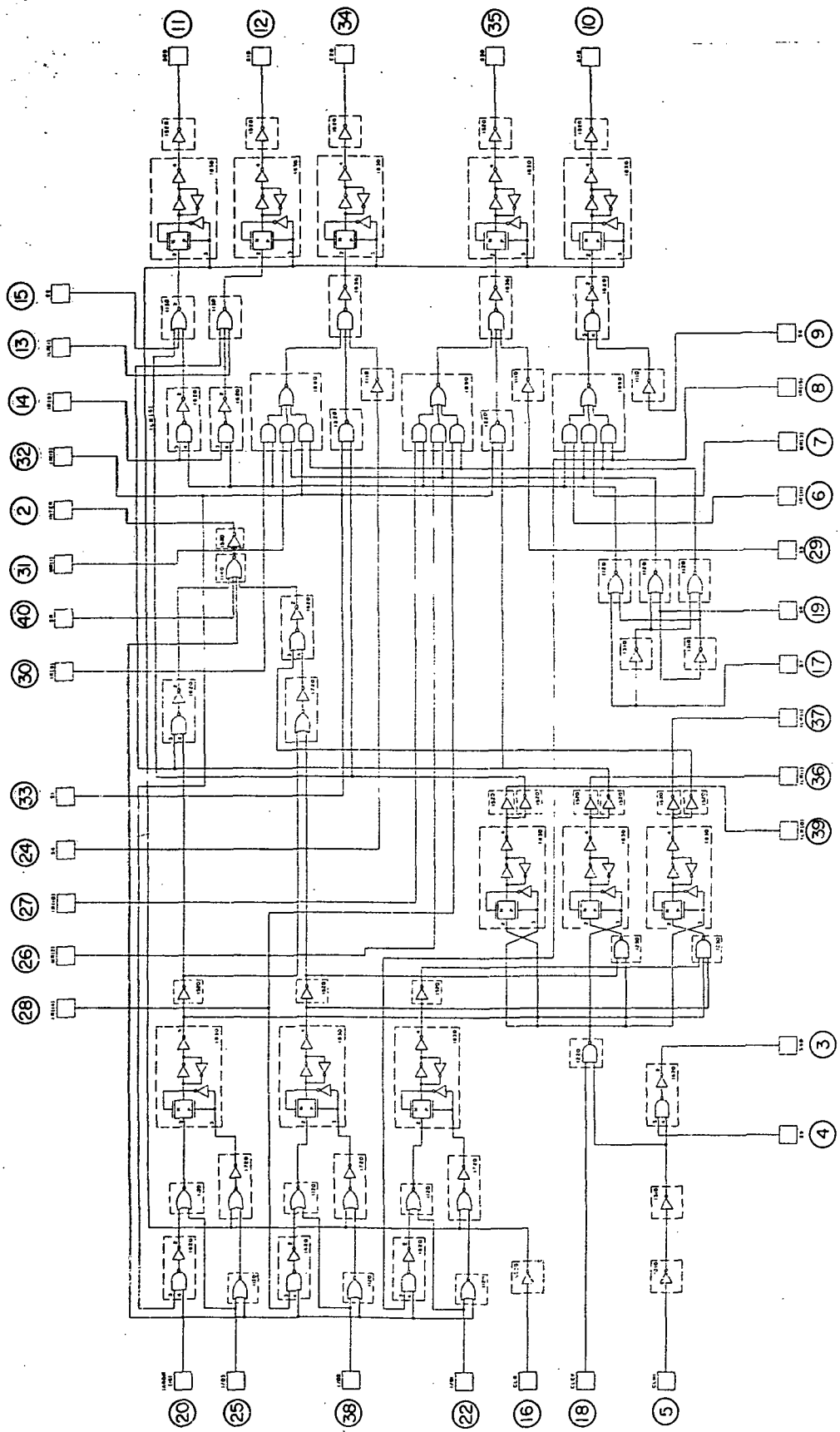
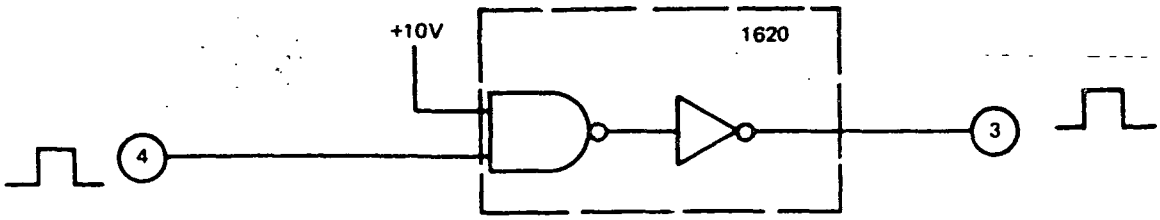
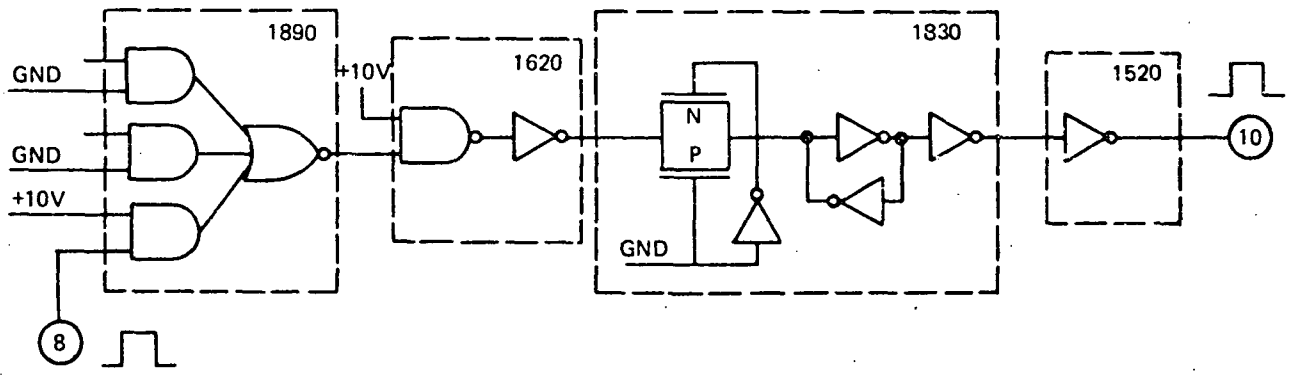


Fig. 3-31. ATL-005 logic diagram.



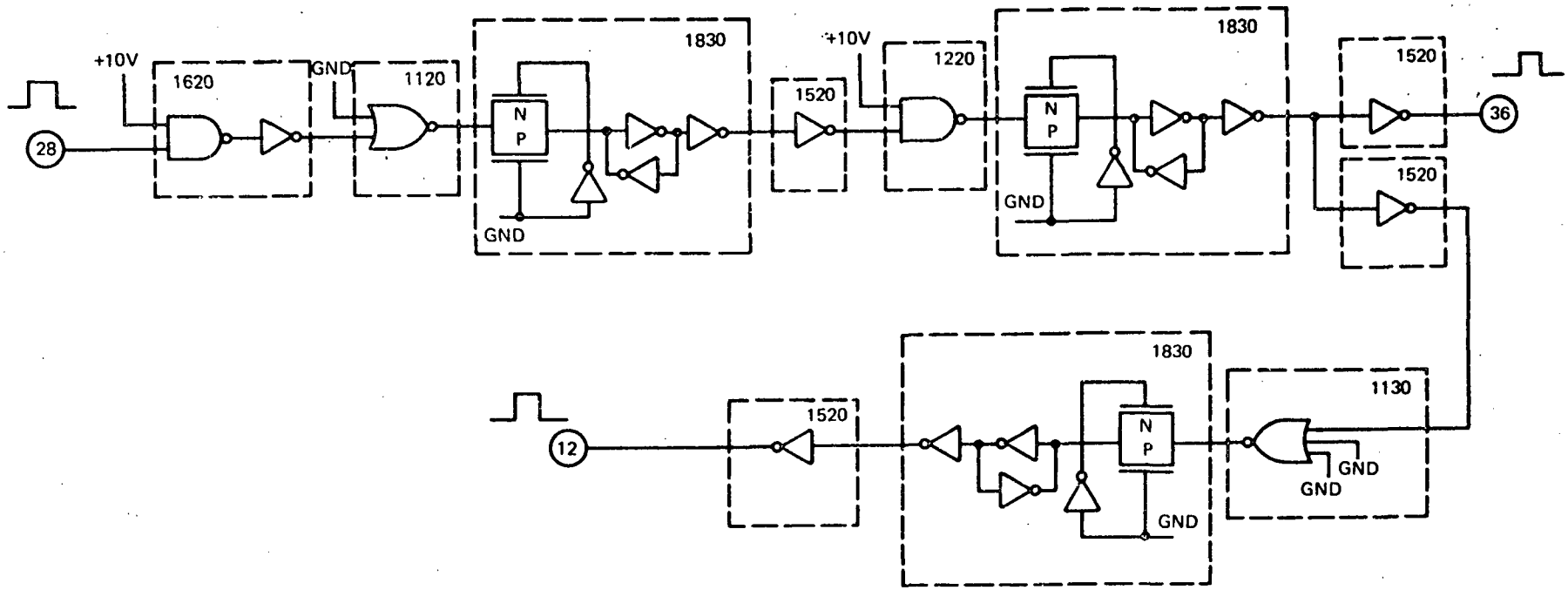
AVG. OUTPUT NODE CAPACITANCE	T 4 3 ⎍ ⎍	T 4 3 ⎏ ⎏	NUMBER OF STAGES	AVERAGE STAGE DELAY ⎍ ⎍	AVERAGE STAGE DELAY ⎏ ⎏	NUMBER OF CHIPS TESTED
13.3 pF	31.7 ns	45.7 ns	2	15.9 ns	22.9 ns	21
28.3 pF	50.5 ns	63.5 ns	2	25.3 ns	31.8 ns	2

Fig. 3-32. Propagation delay path 4 to 3 on ATL-005.



AVG. OUTPUT NODE CAPACITANCE	T 8 10 ⎍ ⎍	T 8 10 ⎏ ⎏	NUMBER OF STAGES	AVERAGE STAGE DELAY ⎍ ⎍	AVERAGE STAGE DELAY ⎏ ⎏	NUMBER OF CHIPS TESTED
10.8 pF	95.7 ns	90.4 ns	7	13.7 ns	12.9 ns	21
25.8 pF	105.0 ns	99.5 ns	7	15.0 ns	14.2 ns	2

Fig. 3-33. Propagation delay path 8 to 10 on ATL-005.



AVG. OUTPUT NODE CAPACITANCE (pF)	T(ns) 28 36 ⌐¬ ⌐¬	T(ns) 28 36 ⌐¬ ⌐¬	T(ns) 28 12 ⌐¬ ⌐¬	T(ns) 28 12 ⌐¬ ⌐¬	NUMBER OF STAGES	AVERAGE STAGE DELAY (ns) ⌐¬ ⌐¬	AVERAGE STAGE DELAY (ns) ⌐¬ ⌐¬	NUMBER OF CHIPS TESTED
11.8	147	181.2			12	12.3	15.1	21
26.8	170	200.5			12	14.2	16.7	2
11.2			211.9	257.7	17	12.5	15.2	21
26.2			228.5	274.5	17	13.4	16.1	2

Fig. 3-34. Propagation delay paths 28 to 36 and 28 to 12 on ATL-005.

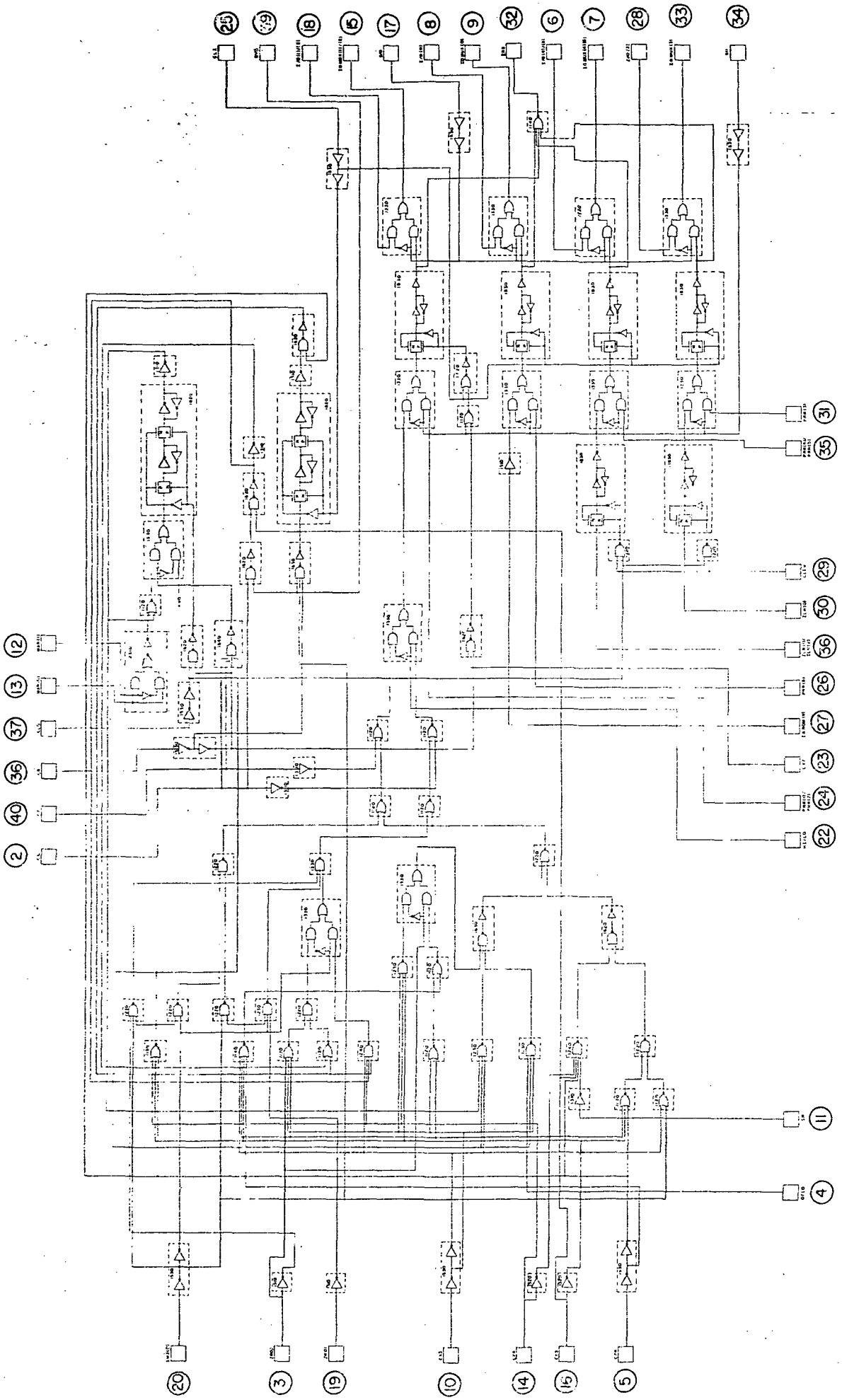
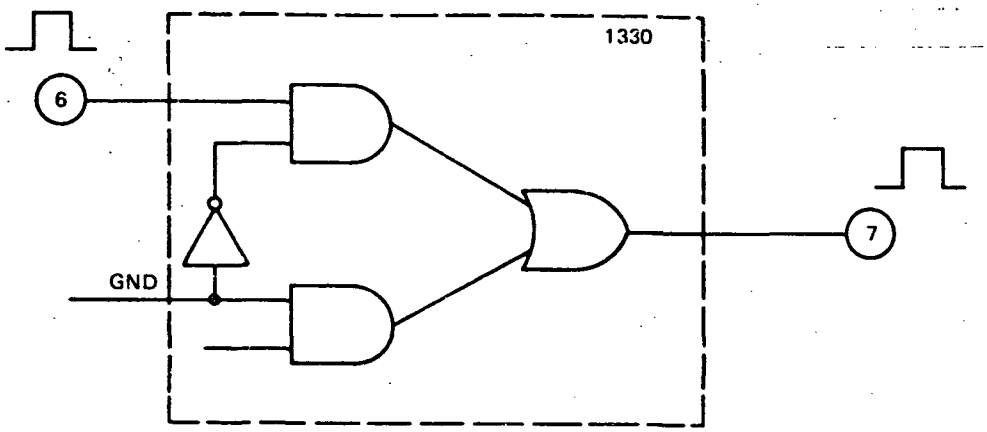
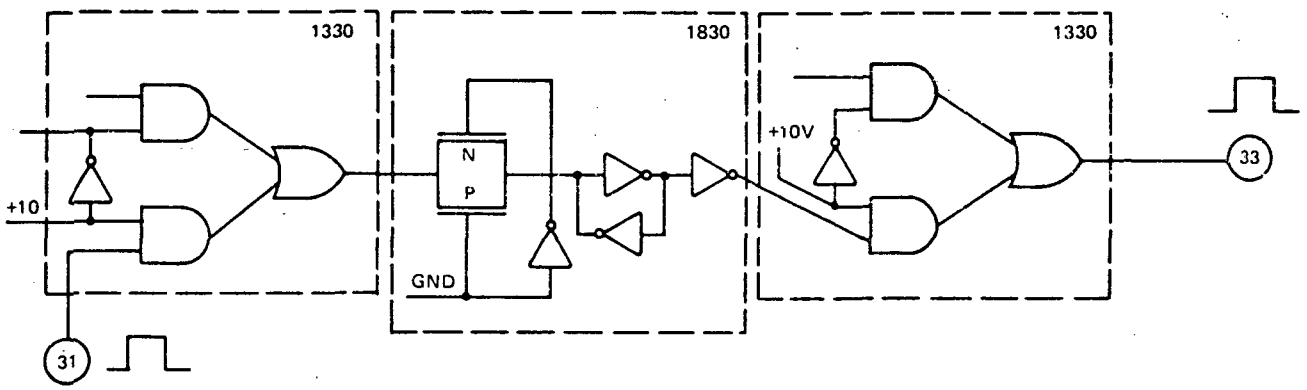


Fig. 3-35. ATL-006A logic diagram.



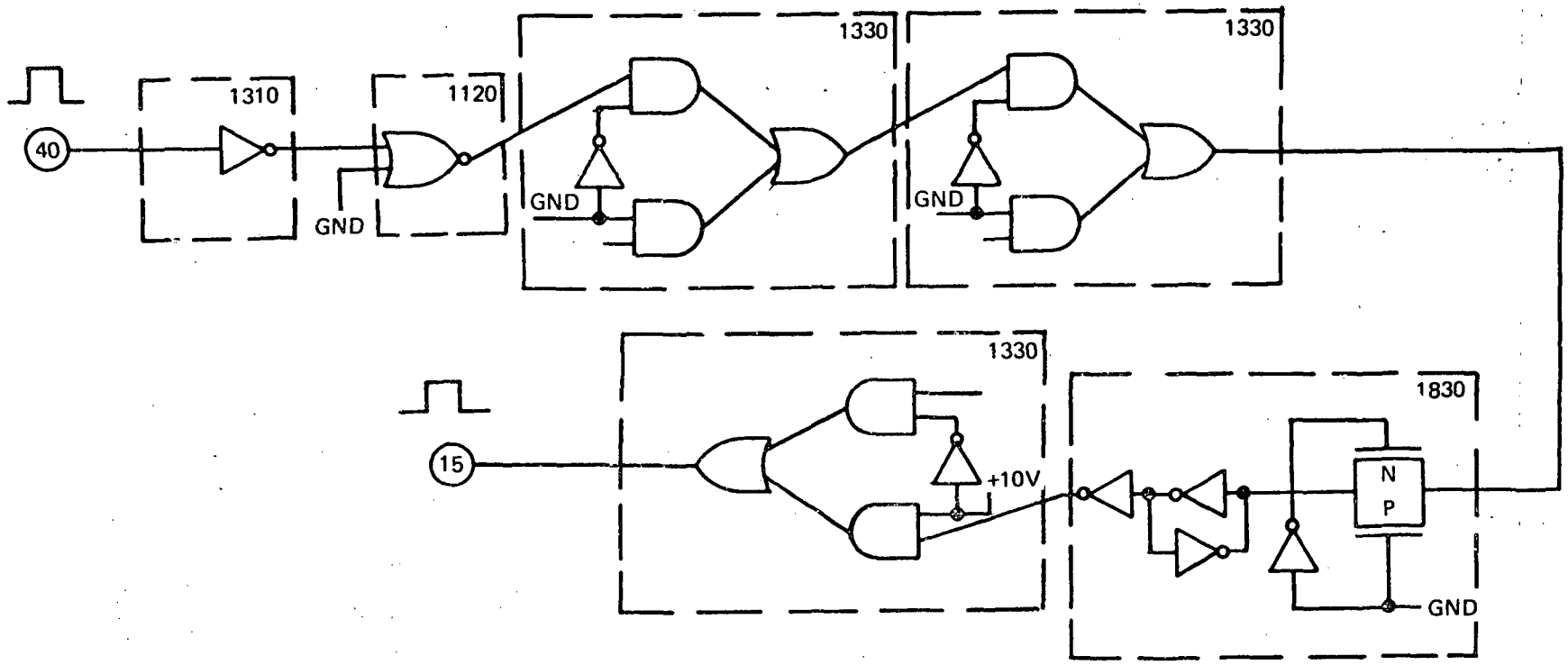
OUTPUT NODE CAPACITANCE	T 6 ⎍ 7 ⎍	T 6 ⎏ 7 ⎏	NUMBER OF STAGES	AVERAGE STAGE DELAY ⎍ ⎍	AVERAGE STAGE DELAY ⎏ ⎏	NUMBER OF CHIPS TESTED
11.4 pF	29.7 ns	28.6 ns	1	29.7 ns	28.6 ns	19

Fig. 3-36. Propagation delay path 6 to 7 on ATL-006A.



OUTPUT NODE CAPACITANCE	T 31 ⎍ 33 ⎍	T 31 ⎏ 33 ⎏	NUMBER OF STAGES	AVERAGE STAGE DELAY ⎍ ⎍	AVERAGE STAGE DELAY ⎏ ⎏	NUMBER OF CHIPS TESTED
11.3 pF	124.5 ns	100.3 ns	5	24.9 ns	20.1 ns	19

Fig. 3-37. Propagation delay path 31 to 33 on ATL-006A.



OUTPUT NODE CAPACITANCE	T 40 15 ⌐¬	T 40 15 ¬⌐	NUMBER OF STAGES	AVERAGE STAGE DELAY ⌐¬	AVERAGE STAGE DELAY ¬⌐	NUMBER OF CHIPS TESTED
13.2 pF	229.7 ns	132.3 ns	8	28.7 ns	16.5 ns	19

Fig. 3-38. Propagation delay path 40 to 15 on ATL-006A.

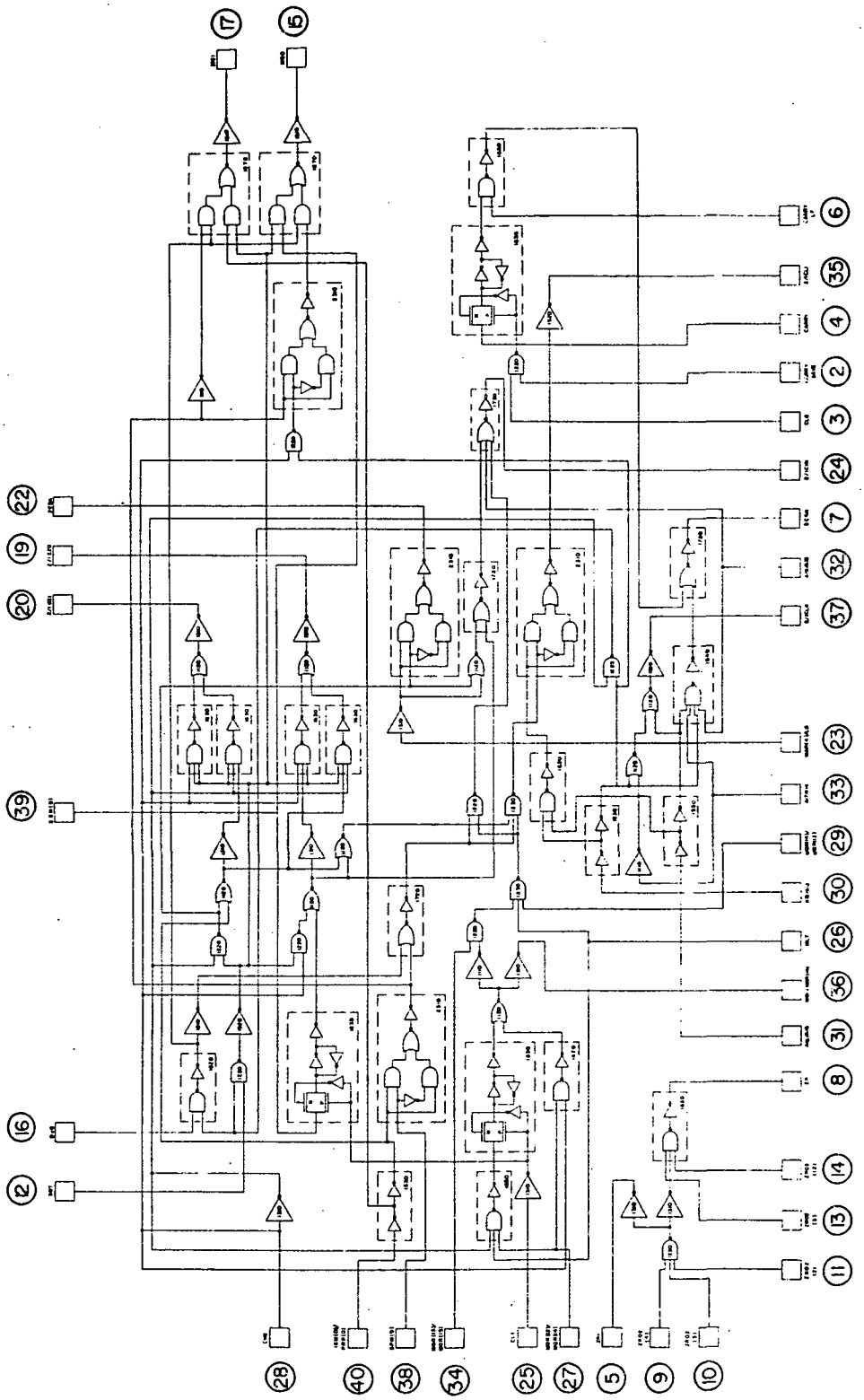
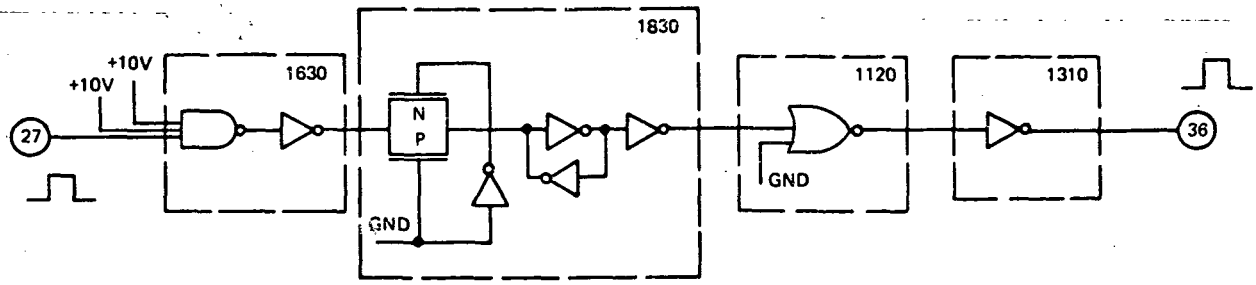
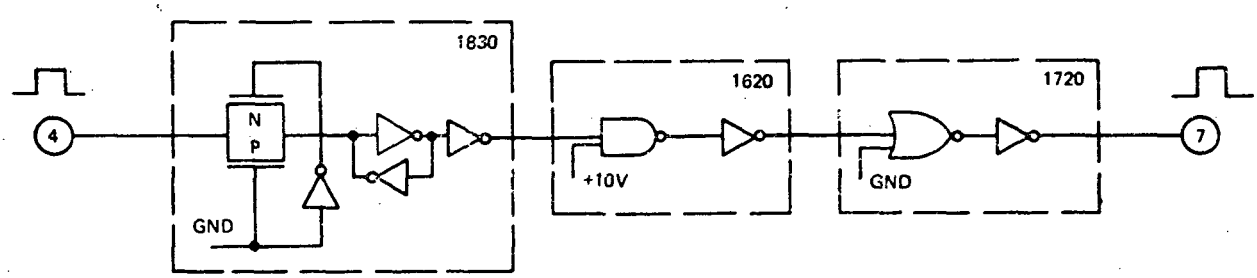


Fig. 3-39. ATL-007A logic diagram.



OUTPUT NODE CAPACITANCE	T 27 36 ⌐¬ ⌐¬	T 27 36 ⌐¬ ⌐¬	NUMBER OF STAGES	AVERAGE STAGE DELAY ⌐¬ ⌐¬	AVERAGE STAGE DELAY ⌐¬ ⌐¬	NUMBER OF CHIPS TESTED
10 pF	101.4 ns	111.1 ns	7	14.5 ns	15.9 ns	20

Fig. 3-40. Propagation delay path 27 to 36 on ATL-007A.



OUTPUT NODE CAPACITANCE	T 4 7 ⌐¬ ⌐¬	T 4 7 ⌐¬ ⌐¬	NUMBER OF STAGES	AVERAGE STAGE DELAY ⌐¬ ⌐¬	AVERAGE STAGE DELAY ⌐¬ ⌐¬	NUMBER OF CHIPS TESTED
8.8 pF	93.4 ns	94.2 ns	7	13.3 ns	13.5 ns	20

Fig. 3-41. Propagation delay path 4 to 7 on the ATL-007A.

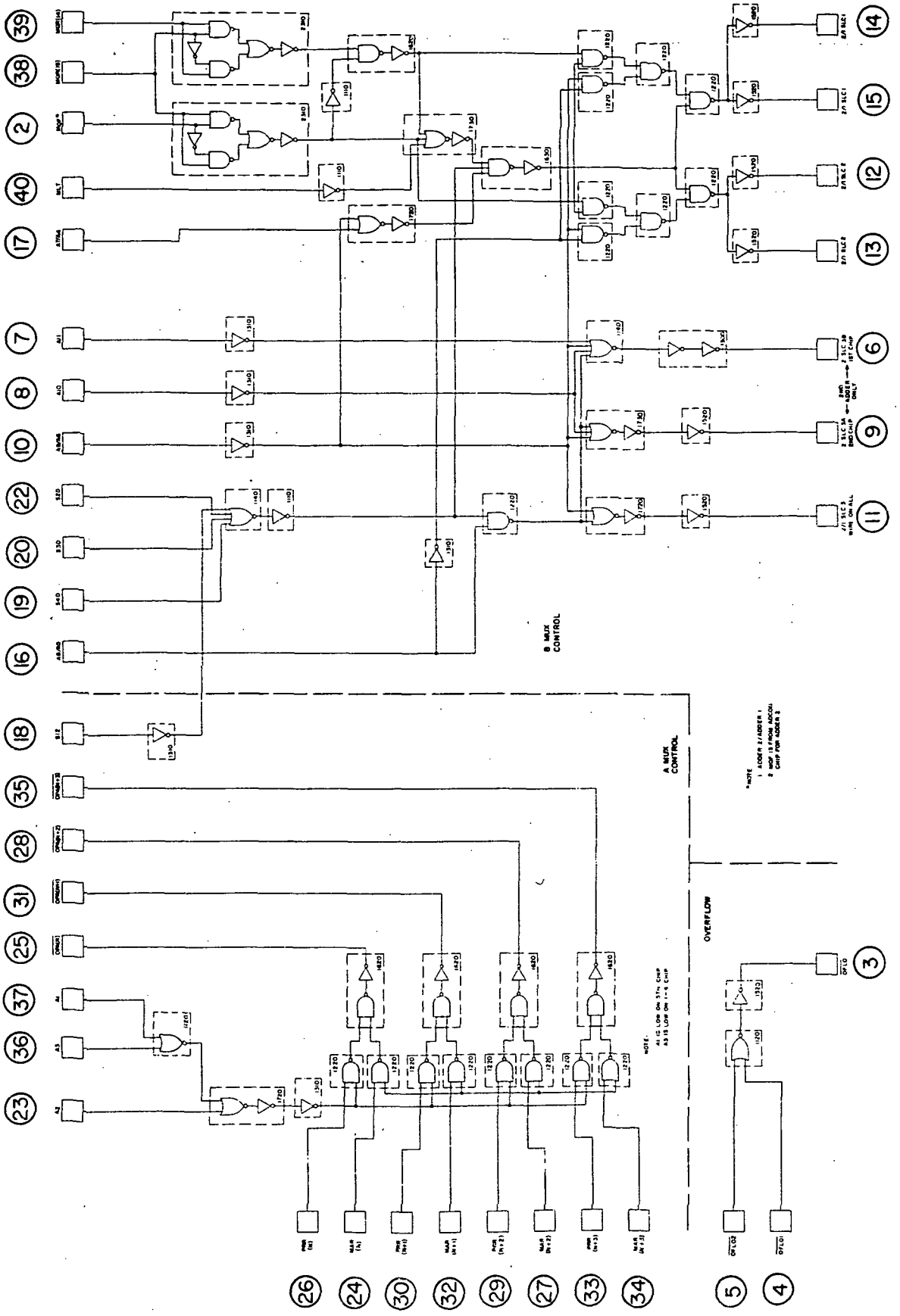
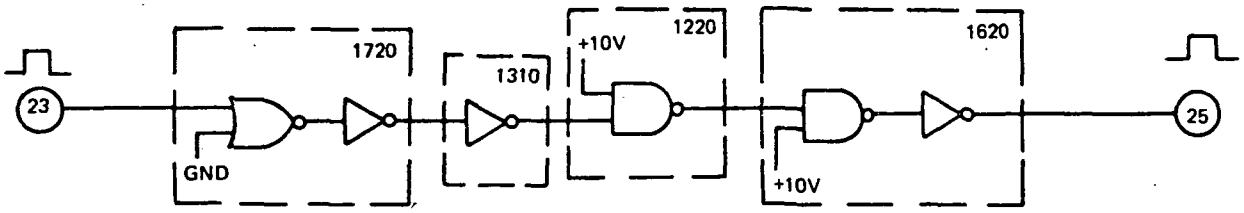
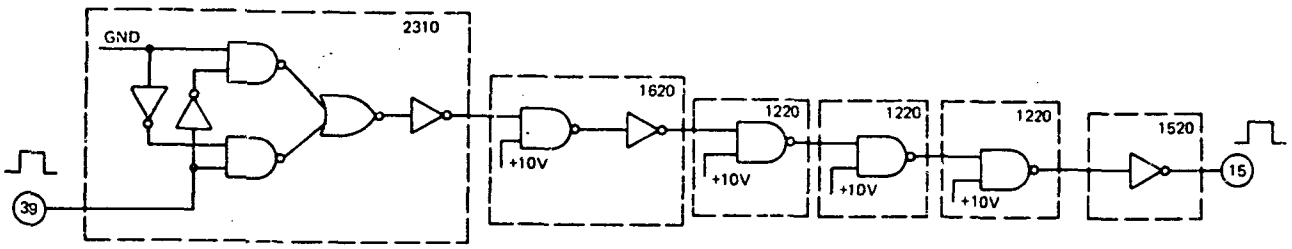


Fig. 3-42. ATL-008A logic diagram.



OUTPUT NODE CAPACITANCE	T 23 25 ⎍ ⎍	T 23 25 ⎏ ⎏	NUMBER OF STAGES	AVERAGE STAGE DELAY ⎍ ⎍	AVERAGE STAGE DELAY ⎏ ⎏	NUMBER OF CHIPS TESTED
11.3pF	97 ns	101.5 ns	6	16.2 ns	16.9 ns	20

Fig. 3-43. Propagation delay path 23 to 35 on the ATL-008A.



OUTPUT NODE CAPACITANCE	T 39 15 ⎍ ⎍	T 39 15 ⎍ ⎍	NUMBER OF STAGES	AVERAGE STAGE DELAY ⎍ ⎍	AVERAGE STAGE DELAY ⎏ ⎏	NUMBER OF CHIPS TESTED
10.7 pF	132 ns	139 ns	9	14.7 ns	15.4 ns	20

Fig. 3-44. Propagation delay path 39 to 15 on the ATL-008A.

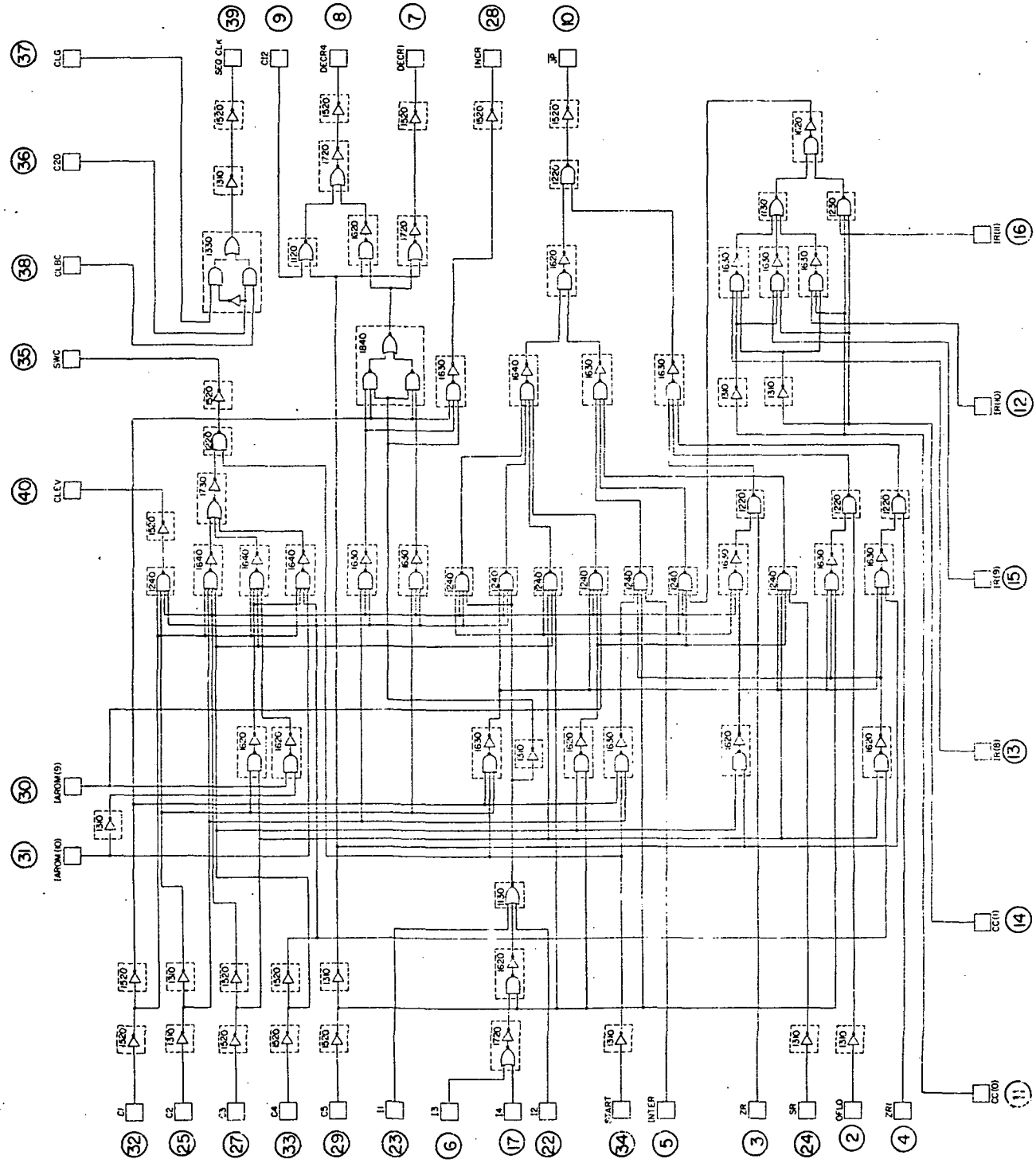
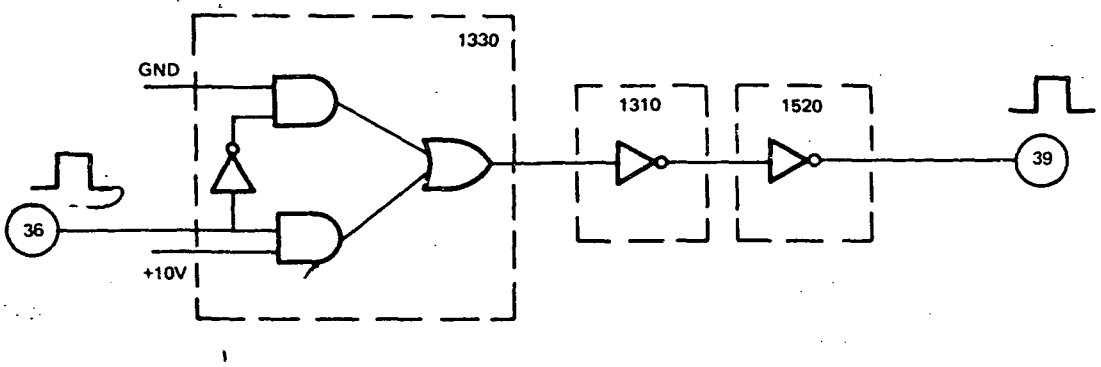
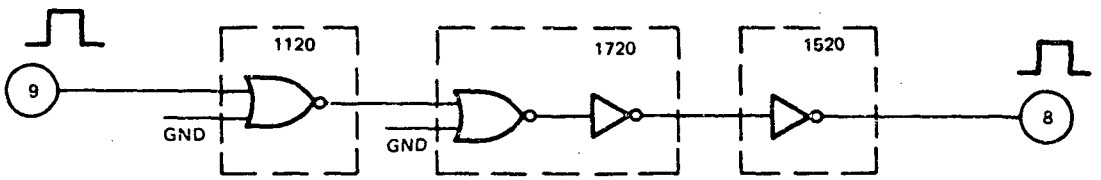


Fig. 3-45. ATI-010A logic diagram.



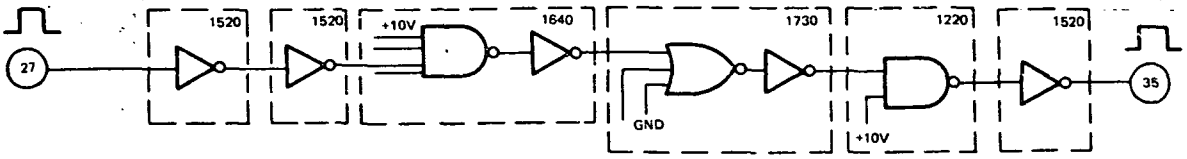
OUTPUT NODE CAPACITANCE	T 36 ↑ 39 ↑	T 36 ↓ 39 ↓	NUMBER OF STAGES	AVERAGE STAGE DELAY ↑ ↑	AVERAGE STAGE DELAY ↓ ↓	NUMBER OF CHIPS TESTED
12.5pF	47ns	50.8ns	4	11.8ns	12.7ns	17

Fig. 3-46. Propagation delay path 36 to 39 on the ATL-010A.



OUTPUT NODE CAPACITANCE	T 9 ↑ 8 ↑	T 9 ↓ 8 ↓	NUMBER OF STAGES	AVERAGE STAGE DELAY ↑ ↑	AVERAGE STAGE DELAY ↓ ↓	NUMBER OF CHIPS TESTED
10.8pF	42.5ns	42.7ns	4	10.6ns	10.7ns	17

Fig. 3-47. Propagation delay path 9 to 8 on the ATL-010A.



OUTPUT NODE CAPACITANCE	T 27 ⎍ 35 ⎍	T 27 ⎏ 35 ⎏	NUMBER OF STAGES	AVERAGE STAGE DELAY ⎍ ⎍	AVERAGE STAGE DELAY ⎏ ⎏	NUMBER OF CHIPS TESTED
10.8pF	107ns	123.2ns	8	13.4ns	15.4ns	17

Fig. 3-48. Propagation delay path 27 to 35 on the ATL-010A.

CHIP TYPE	MEAN AVG. STAGE DELAY (ns)	NUMBER OF STAGES AVERAGED
001A	13.9	644
002A	12.0	616
004A	23.1	1320
005	14.0	1596
006A	23.0	532
007A	14.3	560
008A	15.6	600
009A	20.8	252
010A	12.9	544
AVG. OF ALL CHIP TYPES	16.7	6664

Fig. 3-49. Average +10 V stage delay for all chip types.

SECTION IV

SUMC-DV SUBSYSTEM TESTING

In Section III each of the LSI chip types was considered to be a stand-alone unit. This section deals with the performance of the SUMC-DV system as a group of interconnected CMOS and bipolar packages. The parameters that were investigated on a system level include temperature distribution, life testing, capacitive loading and critical path delay measurements.

A. TEMPERATURE DISTRIBUTION

The SUMC-DV system is contained on 11 plug-in boards and one permanently attached board on the top panel (Fig. 4-1). Of the 40 watts of power consumed by the SUMC-DV, 26 watts are used by the four bipolar main memory boards. These four boards are located side-by-side (boards 1 through 4) and are the only significant heat source in the system. Using a copper-constantan thermocouple, the case temperature on the four main memory boards was measured at approximately 80°C. Boards 5 through 11 contain all of the low power CMOS LSI chips used as well as some scattered bipolar circuits. The CMOS LSI chips on board 5 (MRU) have the highest operating case temperature of any of the CMOS chips due to their proximity to the four main memory boards. Case temperatures on the MRU board are in the neighborhood of 50°C. The operating case temperatures of the chips on boards 6 through 11 are in the range of 30°C to 45°C. Case temperature variations on the CMOS chips are due primarily to their proximity to bipolar circuits and to the flow patterns of the convection currents.

B. LIFE TESTING

Over 4000 hours of life testing have been accumulated on the SUMC-DV using a reference life test program. The purpose of the life test program was to ensure prolonged functional operation as well as to determine if there were any waveform

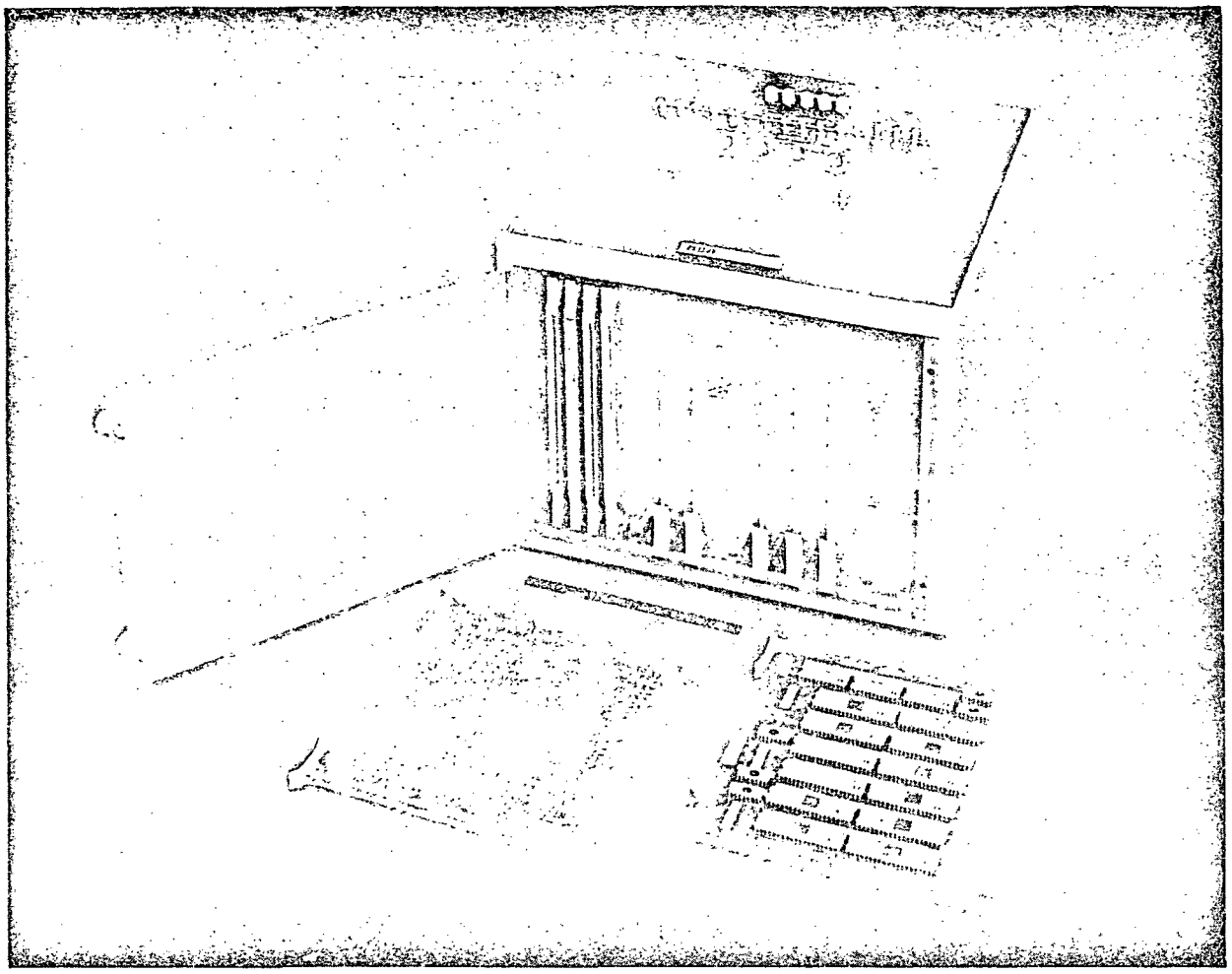


Fig. 4-1. SUMC-DV interior and plug-in cards.

deterioration associated with extended chip performance. Over the life of the test, no functional breakdowns occurred and there was no waveform degradation on the monitored signal lines.

The life test program consisted of an RX addition, an RR subtraction and an RR branch-on-condition which looped back to the RX addition. One loop of the program consisted of 15 elementary operations (EO): 12 short elementary operations and 3 long elementary operations. A 2.9-μs short EO and a 3.48-μs long EO were used for the life test.

Figure 4-2 presents typical waveforms monitored during the life test. The waveforms shown are clock signal CLBC, bit 0 (MSB) out of the first adder unit and the

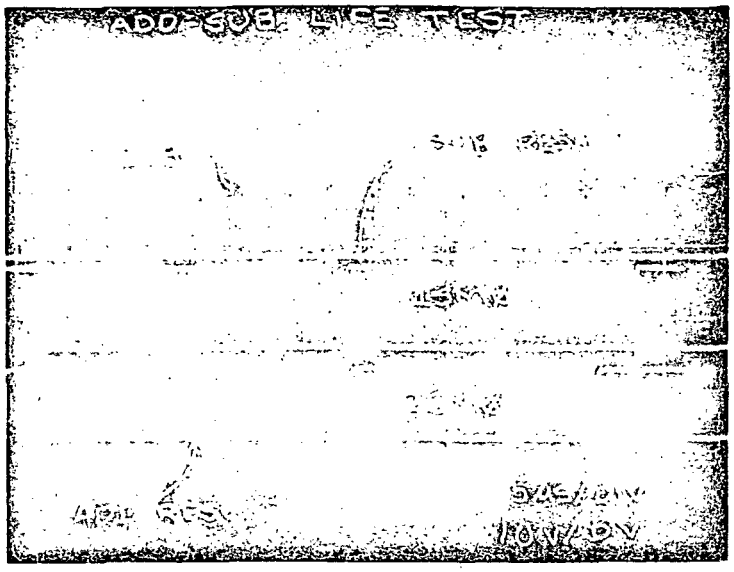


Fig. 4-2. Typical waveforms during life test.

0 bit out of the second adder. The addition performed adds $FFFF_{16}$ to 0001_{16} and the subtraction instruction subtracts 0001_{16} from 0000_{16}. The addition and subtraction results are shown in Fig. 4-2.

C. CAPACITIVE LOADING

Capacitive measurements were made on selected signal paths in order to define the sources and magnitudes of the line capacitance as well as to determine if the standard cell output rise and fall times were consistent with the predicted values.

The results of the capacitive measurements indicated that the sources of capacitance exhibited ranges of values as shown in Table 4-1 which lists the sources and ranges of capacitance as determined from the measurements.

As an example, the capacitance associated with signal 1SM0 on the 1 ALU board is theoretically calculated. 1SM0 enters the 1 ALU board via a P connector and travels through 2 inches of wire to an ATL-004A chip (pin 36). Pin 36 on the ATL-004A is an

output pin driven by an inverting buffer (cell 1520). Cell 1520 also drives one on-chip cell. The best and worst case capacitances are shown in Table 4-2.

TABLE 4-1. SOURCES AND MAGNITUDES OF CAPACITANCE

Source	Capacitance Range (pF)
1 inch of wire	0.4 - 1.5
Backplane pin	0.8 - 1.5
P connector pin	0.8 - 2.3
Socket pin	0.6 - 1.0
Chip input/output	6.0 - 7.5*

*Capacitance is for a fan in (fan out) of 1. Add 2 pF for each additional on-chip fan in (fan out).

TABLE 4-2. 1SM0 SIGNAL CAPACITANCE

Source	Minimum (est) Capacitance (pF)	Maximum (est) Capacitance (pF)
P pin	0.8	2.3
2 inch wire	0.8	3.0
Socket pin	0.6	1.0
Chip output	6.0	7.5
1 additional on-chip fan in	2.0	2.0
TOTAL	10.2	15.8

The capacitance of this path was measured as 12.0 pF.

The Standard Cell CMOS LSI Array User's Handbook predicts rise and fall times as a function of load capacitance for all of the CMOS standard cell types. The predicted ranges in the handbook assume an input rise or fall time of 40 ns to the standard cell. As input rise and fall times to a standard cell increase or decrease, the output rise and fall times as well as the propagation delay will also increase or decrease. The predicted rise or fall time of standard cell 1520 was verified on five signal lines in the SUMC-DV. Cell 1520 is an inverting buffer typically used as an output stage for driving large off-chip capacitances. Since cell 1520 appears at the end of a multi-stage on-chip logic chain in all five cases, the input rise or fall time to the cell can be expected to be sufficiently close to 40 ns. The results of this test appear in Table 4-3.

Capacitance measurements were made on several other signal lines to insure that the rise and fall times of the observed waveforms at these points were consistent with the capacitive loading conditions. Some of the typical line capacitances encountered are presented in Table 4-4.

D. DELAY MEASUREMENTS

Propagation delay and system measurements were made on the critical signal lines associated with an addition-subtraction reference program. The purpose of the measurements was to diagnose any series timing problems and also to provide reference data for future use.

Measurements were made on all of the first and second adder units' sum outputs, the adder carry paths, the condition code inputs, the multiply quotient register and the scratch pad register. Figure 4-3 is typical of the type of system timing conditions that were investigated. Figure 4-3(a) shows the timing relationship between clock pulse BC and the 0 bit output of the first adder. The function being performed in picture is an RR format subtraction with a logical 1 being the correct result for this bit. The measured delay from Fig. 4-3(a) is taken from the leading edge of CLBC to the leading edge of 1SM0. This time defines the time necessary to access the scratch pad memory and to perform the subtraction. From Fig. 4-3(a) this

TABLE 4-3. RISE/FALL TIMES OF CELL 1520 INVERTING BUFFER

Signal Name	Measured Capacitance (pF)	Predict Range of the Rise/Fall Time (ns)	Measured Rise/Fall (ns)
2SM11	69	50-98	90
2SM12	76	53-105	80
2SM0	140	84-196	160
MQR0	62	47-91	80
S3D	60	36-84	50

TABLE 4-4. SUMC-DV LINE CAPACITANCE

Signal Name	Line Capacitance (pF)	Signal Name	Line Capacitance (pF)
S4D	55	2SM7	63
1SM0	37	2SM15	78
$\overline{\text{1SM3}}$	31	MQR3	45
$\overline{\text{1SM11}}$	31	MQR7	43
2SM3	74	MQR15	72

time is 360 ns. In this test program the data state of the 0 bit of the scratch pad memory was correct before CLBC accessed the correct scratch pad memory location, thus producing a fast subtract. If the data state of the scratch pad memory was required to change when the correct scratch pad location was accessed, the subtraction result would be delayed. This condition can be observed by referring to the 1SM0 signal of Fig. 4-2. Prior to output of the first adder assuming its correct state, a voltage spike appeared. This spike occurred while the scratch pad memory was in the process of changing its data state on the 0 bit.

Figure 4-3(b) shows the time delay between clock pulse BC and the 0 output bit of the second adder. An RX addition is being performed and the correct data result for 2SM0 is a logical 0. The time interval between the leading edge of CLBC and the falling edge of 2SM0 defines the time necessary to access the scratch pad memory and to perform the addition.

Figure 4-3(c) shows the interval between the completion of the addition of (b) and the clocking of that correct answer into the 0 bit of the multiply quotient register. The measured time interval in (c) is the time between the falling edge of 2SM0 and the leading edge of clock pulse CLG. From (c), this time is 520 ns. The length of a long elementary operation for this testing sequence was 3.48 μs.

(a)

(b)

(c)

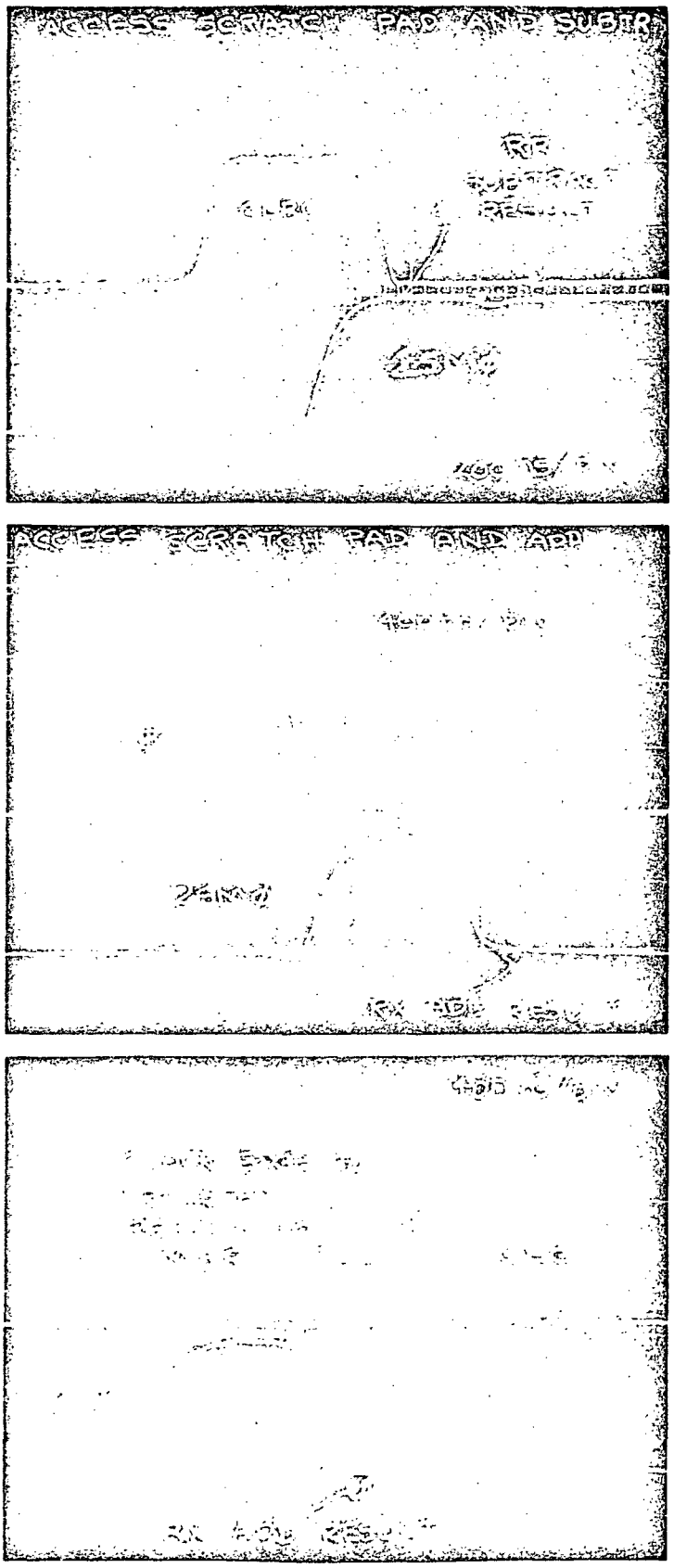


Fig. 4-3. Typical system timing relationships.

SECTION V

SUMC-DV TEST SET AND FRONT PANEL CONTROLS

This section contains a description of and how to use the SUMC-DV test set for debugging, monitoring and maintaining the SUMC-DV. The test set is a special piece of test equipment that provides a pluggable connection to the SUMC-DV permitting all but one register to be directly monitored. In addition, the test set provides the capability to load both main memory and scratch pad off-line. This section also includes a description of the front panel of the SUMC-DV and how to use the controls on the front panel for normal operation as well as in debugging and maintenance procedures.

A. TEST SET

1. Test Set Controls

The layout of the front panel of the test set is given in Fig. 5-1. The panel layout contains the various switches, controls and indicators that have been designed to facilitate the debugging of the SUMC-DV computer. The test set schematic diagram is shown in Fig. 5-2. Referring to Fig. 5-1, the first row of seven lamps at the top of the drawing, DS1 through DS6, labeled ISR, display the Interrupt Status Register, I00 through I06 at all times regardless of the position of the MONITOR SELECTOR switch.

The next row of 16 lamps, DS8 through DS23, labeled DATA, constitute a general 16-bit display field which displays which of the ten 16-bit buses that the 19-position MONITOR SELECTOR switch, SW35, is selecting. The IR position of this switch causes the Instruction Register bus, IR0-IR15, to be displayed 0 through 15 from left to right. The MAR & SPA position displays the main memory address, MAR5 through MAR15 in the left-hand 11 positions, and the scratch pad address, S0D through S4D in the right-hand 5 positions. The PRR position displays the product remainder register, PRR0 through PRR15. The SP position displays the

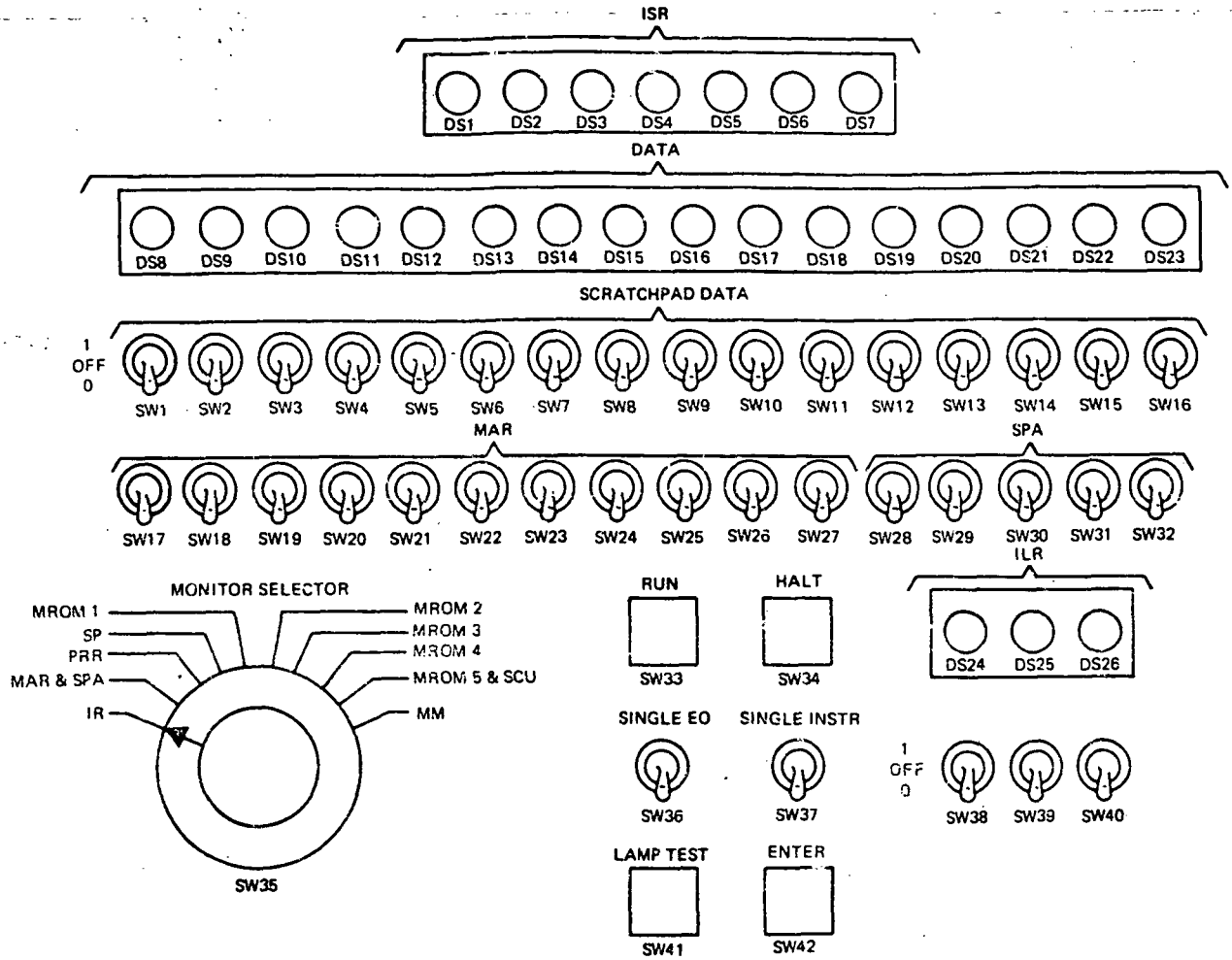


Fig. 5-1. SUMC-DV Test Set.

scratchpad memory output SPM0 through SPM15. The next four positions, MROM1, MROM2, MROM3 and MROM4, display 64 bits of the 72-bit MROM field in the locations shown in the MROM field drawing in Fig. 5-3. The MROM5 & SCU position displays the remaining 8 bits of the MROM field in the left-hand half of the display field in the locations shown in the MROM field drawing, and also displays the 8 sequencer bits which address the MROM, SEQ1 through SEQ8 in the right-hand half of the display field. The MM position displays the output of the main memory, MR0 through MR15.

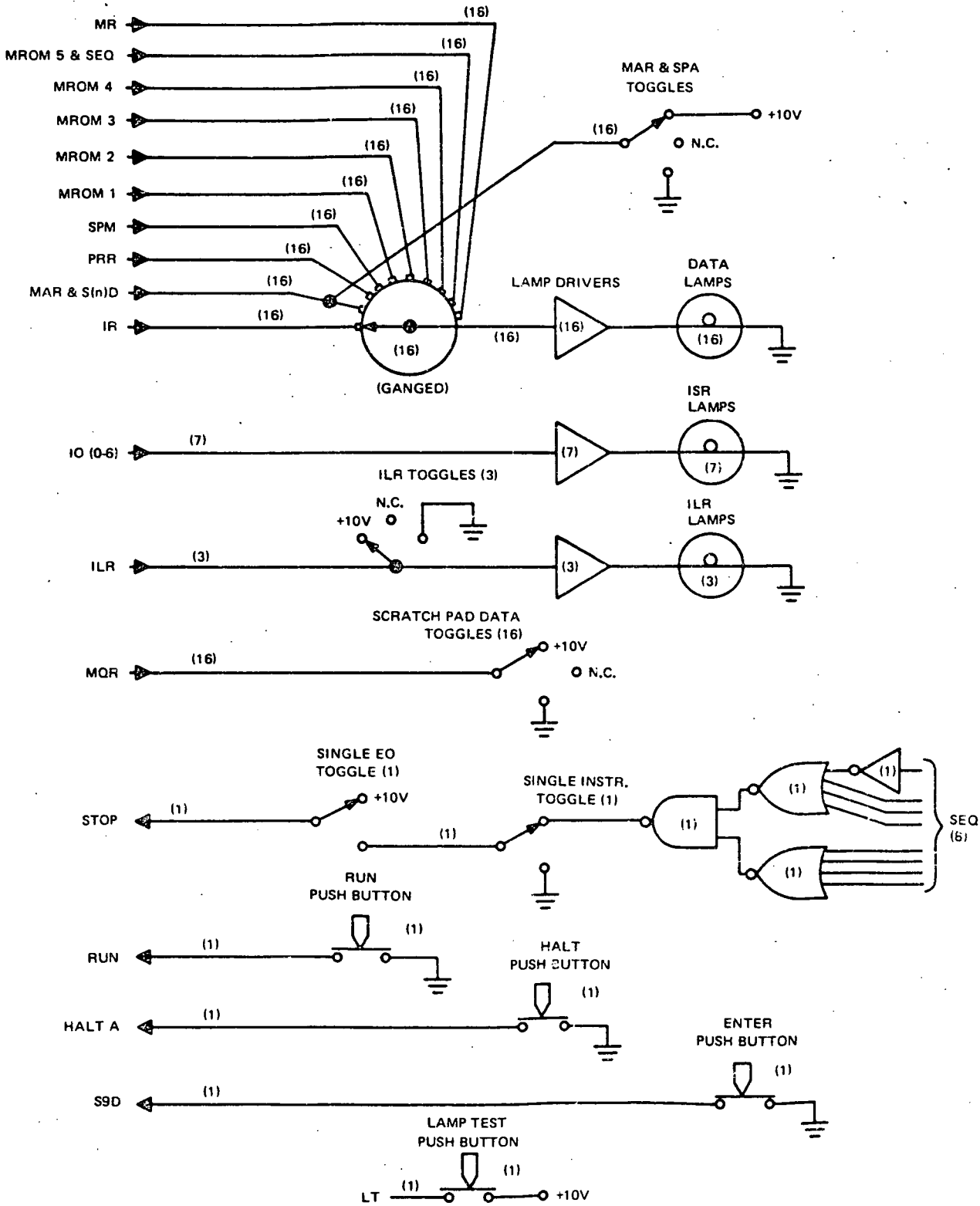


Fig. 5-2. Test set schematic diagram.

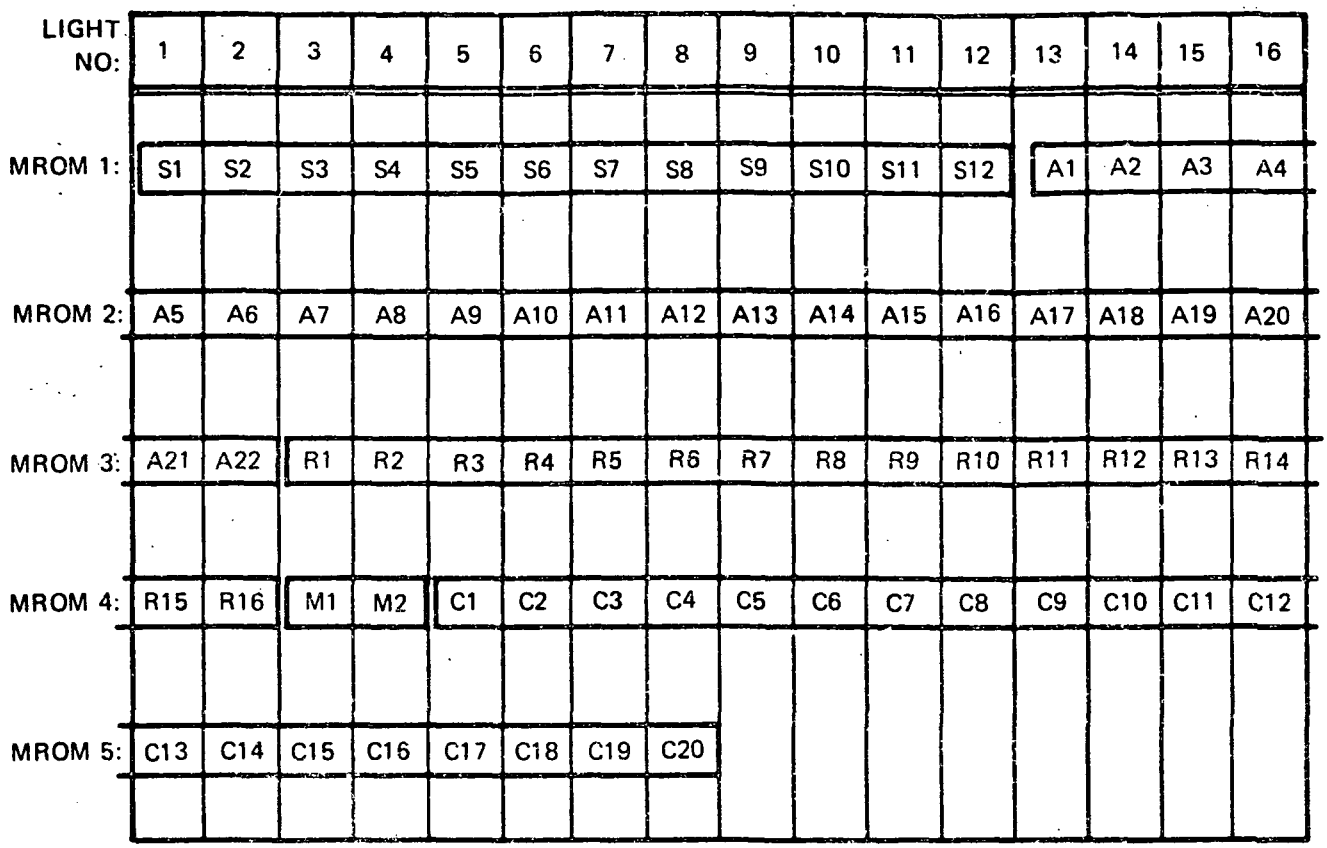


Fig. 5-3. MROM fields on test set.

The next row of devices on the Test Set panel are 16 three-position toggle switches, SW1 through SW16, labeled SCRATCH PAD DATA. These switches have their center arm (as shown in the Test Set schematic) connected to the multiply quotient register bus, MQR0 through MQR15. When they are in the center neutral position, they make no connection to this bus, but when any of these switches is in the up position, it connects the corresponding bit of the MQR bus to +10 volts, forcing a logical "one" and when any of these switches is in the down position, it connects to ground forcing a logical "zero". These switches are provided to load information manually into the scratch pad during debugging, since the MQR bus is the scratch pad data input.

The next row of three position toggle switches SW17 through SW32 is divided into two groups for labeling. The left-hand 11 labeled MAR are connected to the main memory address bits MAR5 through MAR15, and can be used for manual addressing of the main memory. The right-hand five switches labeled SPA are connected to the

scratch pad address bits S0D through S4D, and can be used for manual addressing of the scratch pad. These 16 toggles, like the row above it previously described, force manual override levels when thrown up or down, and disconnect when returned to the center neutral position.

In the lower right-hand corner of the Test Set panel there is a row of three display lamps, DS24 through DS26, under which is a row of three position toggles, SW38 through SW40. This group, labeled ILR, displays and permits manual override of the three interrupt level register bits, ILR0 through ILR2. These bits are monitored at all times and do not go through the MONITOR SELECTOR switch. Manual override does not occur when the three toggles switches are returned to the neutral center position.

SW33 is a pushbutton labeled RUN and SW34 is a pushbutton labeled HALT; these buttons set and reset a flip-flop on the IR board which starts and stops the clock generator.

The SINGLE EO and the SINGLE INSTR two-position toggles, SW36 and SW37, respectively, are wired to stop the clock generator automatically for debugging the SUMC-DV. As shown in Fig. 5-2, the end of an instruction is recognized by sensing when the sequencer returns to the MROM address for the EO which loads the next instruction into the instruction register from main memory. This code has a zero in all bits but the least significant bit which has a one. This combination of the sequencer bits is decoded by two CMOS packages in the Test Set. If the SINGLE EO toggle switch is down and the SINGLE INSTR toggle switch is up, the output of this decoder is sent back to the IR board to stop the clock at the end of each instruction. If the SINGLE EO toggle switch is up, the other toggle switch is ignored and a wired high is set back on the STOP line to stop the DV at the end of each EO.

The LAMP TEST pushbutton, SW41, connects the anode of a diode in every lamp driver circuit to +10 V when pressed, lighting every lamp on the Test Set panel to check for burned out lamps or nonfunctional lamp driver circuits.

The "ENTER" button, SW42, manually overrides the scratch pad write control to ground. This is for entering the scratch pad data which has been set up manually from the Test Set.

2. Use of the Test Set in Debugging

When the Test Set is used for debugging, it is generally advisable to have all 14 of the ribbon connectors plugged into the boards of the SUMC-DV. Figure 5-4 shows how each of the fourteen 16-pin connectors at the end of the 14 ribbon cables interface with the seven SUMC-DV boards and map into the 224-pin terminal board whose internal wiring is shown in Fig. 5-5. When operating with the Test Set, the CLOCK toggle on the SUMC-DV panel should be in the SLOW position. After any manual loading operations from the Test Set, it is important to remember to return all manual loading toggles to their central neutral positions before attempting to run.

The SINGLE EO and SINGLE INSTR modes will be found particularly useful, but it should be remembered that the states displayed in these modes are always the states at the end of the last clock pulse of the EO, and that intermediate states within the EO cannot be displayed on the Test Set panel. It is only when the SINGLE EO or the SINGLE INSTR mode is in use that the RUN pushbutton on the Test Set front panel is used to advance from EO to EO or from instruction to instruction, since this pushbutton does not clear the sequencer. The only exception to this is when a program has been halted manually at some random EO for inspection and it is desired to continue the program from the point at which it happened to stop. Whenever a program is restarted at the beginning, the first main memory address must be loaded manually, and then the START pushbutton on the SUMC-DV panel must be pressed. On the other hand, the two HALT pushbuttons are equivalent in every way.

The use of the MONITOR SELECTOR switch to display 10 sets of 16 bits each is self explanatory. In order to get a meaningful display on the Test Set, of course, the SUMC-DV clock must always be stopped while observing the display. Various colored lamp covers have been used to divide the lamps into groups of four for hexadecimal reading of the displays. Corresponding switches and lamps have been aligned vertically for greater clarity.

A1A5J16 (MRU)	PRR 15	PRR 14	PRR 13	PRR 12	PRR 11	PRR 10	PRR 9	PRR 8	E8 ← E1 E9 → E16	P1
	o	o	o	o	o	o	o	o		
	16	15	14	13	12	11	10	9		
	1	2	3	4	5	6	7	8		
	o	o	o	o	o	o	o	o		
	PRR 0	PRR 1	PRR 2	PRR 3	PRR 4	PRR 5	PRR 6	PRR 7		
A1A5J19 (MRU)	MAR 15	MAR 14	MAR 13	MAR 12	MAR 11	MAR 10	MAR 9	MAR 8	E28 ← E21 E29 → E36	P2
	o	o	o	o	o	o	o	o		
	16	15	14	13	12	11	10	9		
	1	2	3	4	5	6	7	8		
	o	o	o	o	o	o	o	o		
	N.C	N.C	+10V	GND	MAR 4	MAR 5	MAR 6	MAR 7		
*A1A5J22 (MRU)	R16	R15	R14	N.C.	R12	R11	R10	R9	E48 ← E41 E49 → E56	P3
	o	o	o	o	o	o	o	o		
	16	15	14	13	12	11	10	9		
	1	2	3	4	5	6	7	8		
	o	o	o	o	o	o	o	o		
	R1	R2	R3	R4	R5	R6	R7	R8		
A1A6J1 (ALU-2)	N.C.	N.C.	N.C.	N.C.	A22	A21	A20	A19	E76 ← E69 E61 → E68	P4
	o	o	o	o	o	o	o	o		
	16	15	14	13	12	11	10	9		
	1	2	3	4	5	6	7	8		
	o	o	o	o	o	o	o	o		
	A7	A8	A9	A10	A11	A15	A16	A17		
A1A7J1 (ALU-1)	N.C.	N.C.	S12A	A22A	A21A	A20A	A18A	A14A	E96 ← E89 E81 → E88	P5
	o	o	o	o	o	o	o	o		
	16	15	14	13	12	11	10	9		
	1	2	3	4	5	6	7	8		
	o	o	o	o	o	o	o	o		
	A1A	A2A	A3A	A4A	A5A	A6A	A12A	A13A		
*A1A8J1 (SPM)	MQR 15	MQR 14	MQR 13	MQR 12	MQR 11	MQR 10	MQR 9	MQR 8	E108 ← E101 E109 → E116	P6
	o	o	o	o	o	o	o	o		
	16	15	14	13	12	11	10	9		
	1	2	3	4	5	6	7	8		
	o	o	o	o	o	o	o	o		
	MQR 0	MQR 1	MQR 2	MQR 3	MQR 4	MQR 5	MQR 6	MQR 7		
*A1A8J2 (SPM)	SPM 15	SPM 14	SPM 13	SPM 12	SPM 11	SPM 10	SPM 9	SPM 8	E128 ← E121 E129 → E136	P7
	o	o	o	o	o	o	o	o		
	16	15	14	13	12	11	10	9		
	1	2	3	4	5	6	7	8		
	o	o	o	o	o	o	o	o		
	SPM 0	SPM 1	SPM 2	SPM 3	SPM 4	SPM 5	SPM 6	SPM 7		

*These connectors are rotated 180° with respect to the others.

Fig. 5-4. Test set connectors (sheet 1 of 2).

	S8	S9	S0D	S1D	S2D	S3D	S4D	S9D		
	o	o	o	o	o	o	o	o	E156←E149	
A1A9J1	16	15	14	13	12	11	10	9		P8
(IR)	1	2	3	4	5	6	7	8	E141→E148	
	o	o	o	o	o	o	o	o		
	R13	S1	S2	S3	S4	S5	S6	S7		
	IR15	IR14	IR13	IR12	IR11	IR10	IR9	IR8		
	o	o	o	o	o	o	o	o	E176←E169	
A1A9J2	16	15	14	13	12	11	10	9		P9
(IR)	1	2	3	4	5	6	7	8	E161→E168	
	o	o	o	o	o	o	o	o		
	IR0	IR1	IR2	IR3	IR4	IR5	IR6	IR7		
	N.C.	J3	J3	N.C.	N.C.	N.C.	N.C.	N.C.		
	o	o	o	o	o	o	o	o	E196←E189	
A1A9J3	16	15	14	13	12	11	10	9		P10
(IR)	1	2	3	4	5	6	7	8	E181→E188	
	o	o	o	o	o	o	o	o		
	GND	STOP	RUN	HALT	ILR 0	ILR 1	ILR 2	N.C.		
	C19	C18	C17	C16	C15	C14	C13	C12		
	o	o	o	o	o	o	o	o	E216←E209	
A1A10J1	16	15	14	13	12	11	10	9		P11
(MROM)	1	2	3	4	5	6	7	8	E201→E208	
	o	o	o	o	o	o	o	o		
	C1	C2	C3	C4	C5	C9	C10	C11		
	N.C.	N.C.	N.C.	N.C.	N.C.	M2A	M1A	SEQ		
	o	o	o	o	o	o	o	o	E236←E229	
A1A10J2	16	15	14	13	12	11	10	9		P12
(MROM)	1	2	3	4	5	6	7	8	E221→E228	
	o	o	o	o	o	o	o	o		
	C20	SEQ 1	SEQ 2	SEQ 3	SEQ 4	SEQ 5	SEQ 6	SEQ 7		
	N.C.	N.C.	N.C.	N.C.	S11	S10	C8	C7		
	o	o	o	o	o	o	o	o	E256←E249	
A1A11J1	16	15	14	13	12	11	10	9		P13
(I/O)	1	2	3	4	5	6	7	8	E241→E248	
	o	o	o	o	o	o	o	o		
	IO0	IO1	IO2	IO3	IO4	IO5	IO6	C6		
	MR15	MR14	MR13	MR12	MR11	MR10	MR9	MR8		
	o	o	o	o	o	o	o	o	E276←E269	
A1A6J2	16	15	14	13	12	11	10	9		P14
(ALU-2)	1	2	3	4	5	6	7	8	E261→E268	
	o	o	o	o	o	o	o	o		
	MR0	MR1	MR2	MR3	MR4	MR5	MR6	MR7		

*These connectors are rotated 180° with respect to the others.

Fig. 5-4. Test set connectors (sheet 2 of 2).

ITEM	DESCRIPTION
C1	
CR2 THRU CR9 CR11 THRU CR28	1N914 DIODE
Q2 THRU Q8 Q11 THRU Q28	2N2219A TRANSISTOR
R3, 5, 7, 9, 11, 13, 15, 17, 21, 23 25, 27, 29, 31, 33, 35, 37, 39, 41 43, 45, 47, 49, 51, 53, 55	1000Ω ½W 10% RESISTOR

ITEM	DESCRIPTION
R4, 6, 8, 10, 12, 14, 16, 18, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 44, 46, 48, 50, 52, 54, 56	4700Ω ½W, 10% RESISTOR
Z1 & Z2	

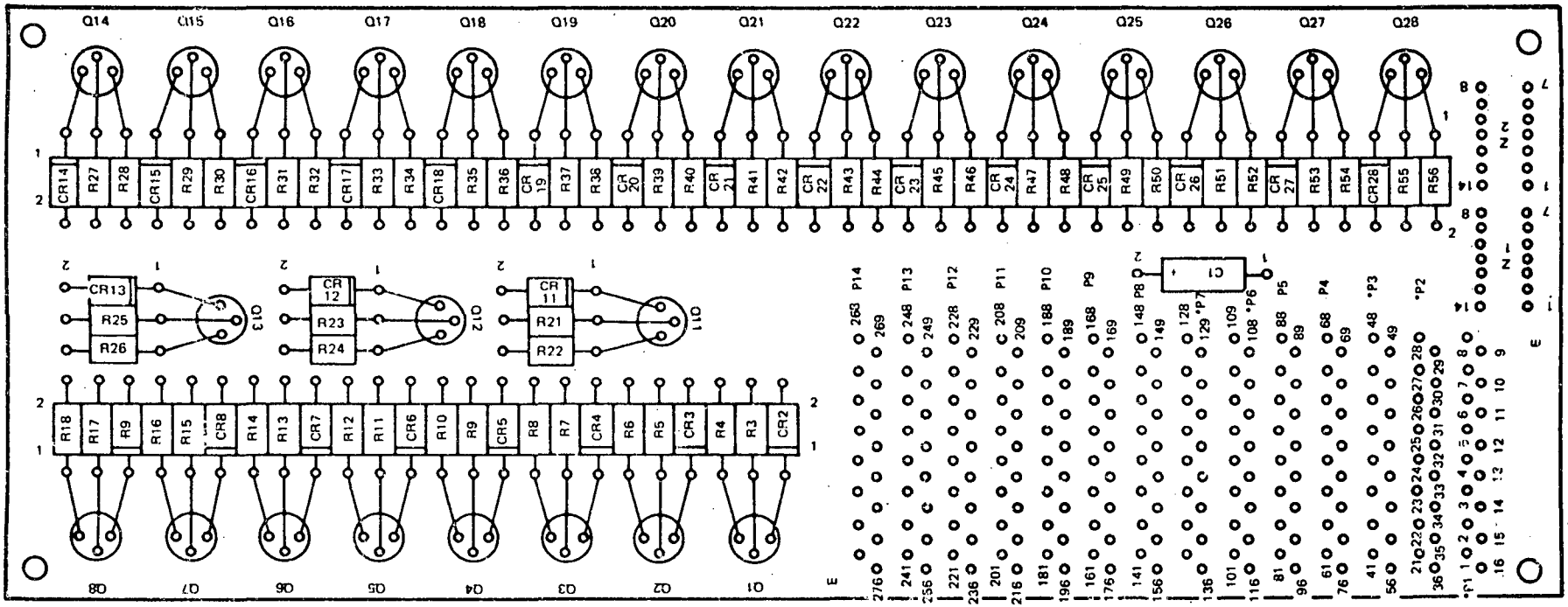


Fig. 5-5. Test set terminal board, internal wiring.

The procedure for loading the main memory from an address set manually on the Test Set is as follows:

(1) Press the HALT pushbutton (either SUMC-DV or Test Set).

(2) Turn the DATA switch to SET mode (SUMC-DV).

(3) Turn the MEMORY ADDRESS switch to RUN mode (SUMC-DV).

(4) Set up the desired main memory address on the 11-bit field labeled MAR (Test Set).

(5) Set up the desired data word on the MAIN MEMORY DATA toggle switches (SUMC-DV).

(6) Press the ADDRESS ENTRY pushbutton (SUMC-DV).

(7) Press the DATA ENTRY pushbutton (SUMC-DV).

(8) Repeat steps (4) through (7) until all the desired entries are made in main memory.

(9) Turn the DATA switch to the RUN position (SUMC-DV).

(10) Return all toggle switches on the Test Set to the center position (straight up).

The SUMC-DV is now ready to run, and can either be continued from the present state of the machine by pushing the RUN pushbutton on the Test Set, or started at the beginning of the program by loading the starting address into main memory, removing all override conditions, and pressing the START pushbutton on the SUMC-DV.

The procedure for loading the scratch pad memory manually from the Test Set is as follows:

(1) Press the HALT pushbutton (Test Set or SUMC-DV).

(2) Set up the desired address on the five SPA toggle switches (Test Set).

(3) Set up the desired data on the 16 SCRATCH PAD DATA toggle switches (Test Set).

(4) Press the ENTER pushbutton (Test Set).

(5) If more scratch pad words are to be entered, repeat steps (2) through (4) as needed.

(6) Return all three-position toggle switches on the Test Set to their center positions.

The SUMC-DV can now be continued from where it is in the program, or restarted from the beginning as described below.

In using the Test Set for debugging, it is important to understand the way in which the manual override functions. All of the data lines which are brought into the Test Set for display, and/or manual override are CMOS levels driven from CMOS transistors which swing from ground to +10 volts. It is a characteristic of CMOS drivers that their output can be shorted to either ground or to the positive supply without damage to the driving transistors. Moreover, since each CMOS register in the SUMC-DV is isolated from the output pins by buffers, the internal states of these registers are not affected by manual override from the Test Set. When the override toggle switches are returned to the center positions, the original data in the driving registers reappears on these data buses, although the memory accessed by the data lines or address lines may have meanwhile entered the manually presented data or address.

B. SUMC-DV FRONT PANEL

1. Front Panel Controls

The front panel layout is shown in Fig. 5-6. This figure also shows the reference designation which identify the controls and indicators in the schematic diagram and in the wiring lists for the SUMC-DV.

Figure 5-7 shows the schematic which relates each item on the front panel to the signal lines which are switched or displayed by that item. This same schematic also shows all of the units which are located on the nonpluggable board A14, mounted just behind the front panel; these units are intimately related to the front panel.

Referring to Fig. 5-7, the five lights which are located at the top of the panel labeled MAIN MEMORY ADDRESS show at all times the state of the manual address counter which is located physically on the nonpluggable board A14. This counter is advanced manually by the INCREMENT ADDRESS pushbutton, SW20, and

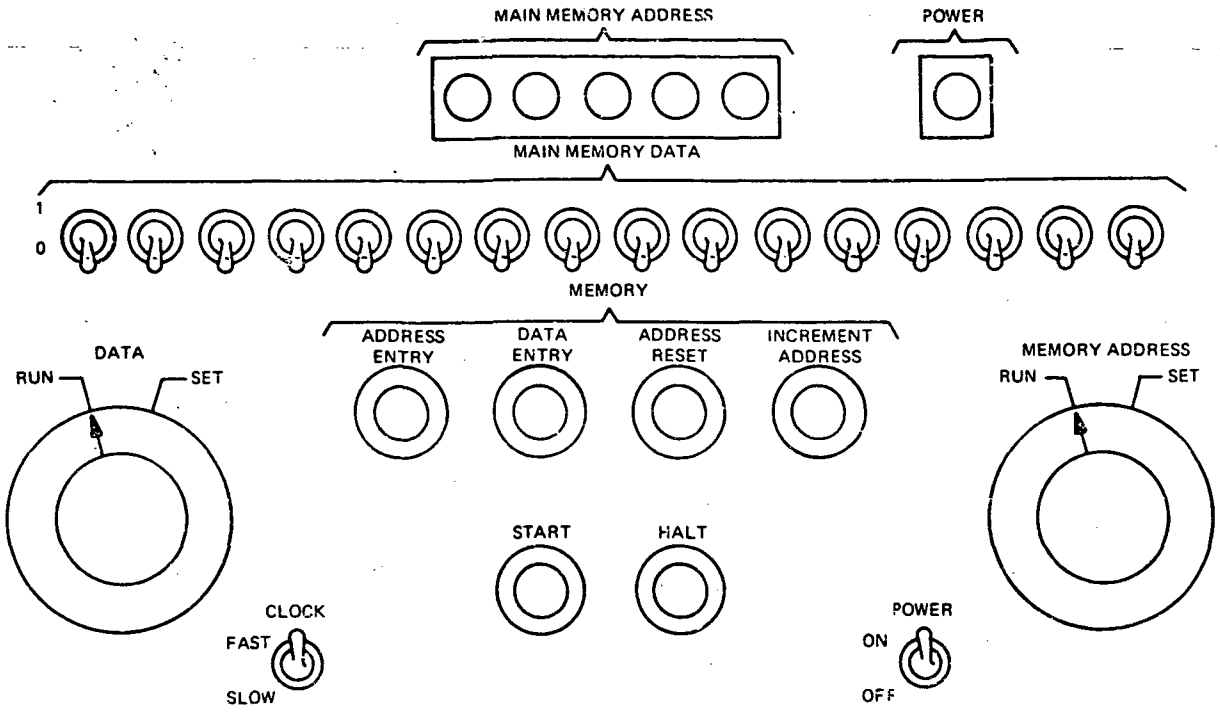


Fig. 5-6. SUMC-DV front panel.

reset manually by the ADDRESS RESET pushbutton, SW19. The manual address counter is used only for loading the main memory manually, and is connected to the main memory address lines only when the MEMORY ADDRESS rotary switch, SW26, is in the SET position. With SW26 in the SET position, and the CPU in a halted state, the contents of the manual address counter do not enter the main memory address register until the ADDRESS ENTRY pushbutton, SW17, is pressed.

It should be noted that there are only five bits in the manual address counter. When the MEMORY ADDRESS rotary switch is in the SET position, these five bits become the least significant bits (MAR11 through MAR15) and the remaining six bits (MAR5 through MAR10) are forced to the "zero" state. This makes it possible to access manually only the first 32 locations of the main memory. All of the 2048 locations can be accessed manually, however, from the Test Set when it is connected to the SUMC-DV.

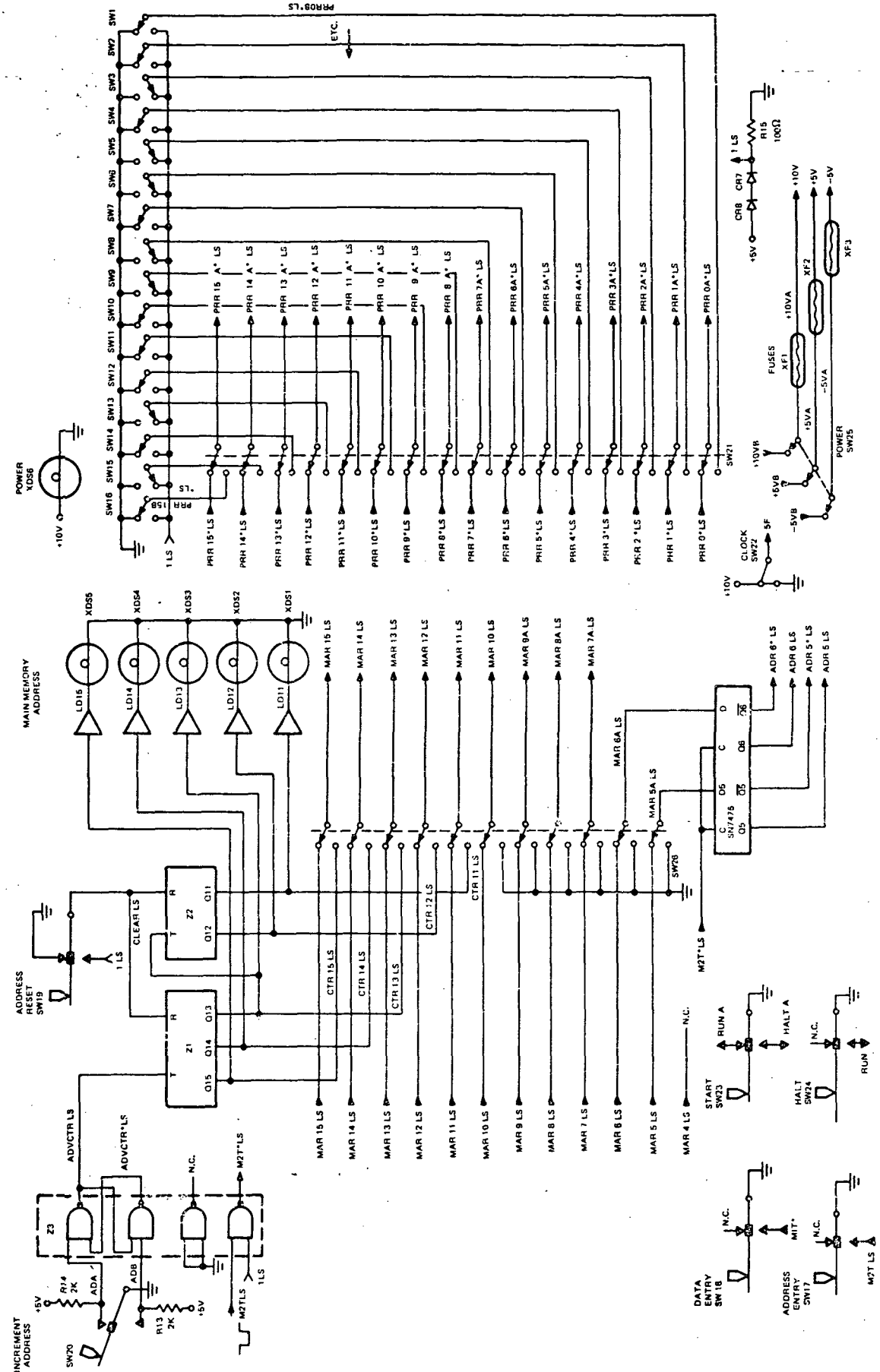


Fig. 5-7. SUMC-DV front panel and panel mounted board, schematic diagram.

The row of 16 toggle switches (SW1 through SW16) labeled MAIN MEMORY DATA are for the purpose of manual data entry into the main memory. When the DATA rotary switch, SW21, is in the SET position, the contents of these toggle switches appear at the data input to the main memory (inverted since data in main memory is inverted). This data, however, does not enter the addressed location until the DATA ENTRY pushbutton, SW18, is pressed.

Other items found on the front panel are the POWER toggle switch, SW25, the CLOCK toggle switch, SW22, the START and HALT pushbuttons, SW23 and SW24, respectively, and the POWER light which is a 10-volt bulb wired across the 10-volt supply beyond the power switch and the fuse.

The POWER toggle switch is simply a single-throw, three-pole switch with a section for each supply: the +10 volt, the +5 volt and the -5 volt supply. The START pushbutton clears the sequencer, and then sets a flip-flop which gates the oscillator into the clock pulse generator. The HALT pushbutton resets this flip-flop and inhibits the clock pulse generator at the end of the EO during which it was pressed. The SUMC-DV will not stop in the middle of an EO. The CLOCK toggle switch has two positions: FAST and SLOW. These two positions select one of the two internal oscillator frequencies. The ranges of these two internal clocks are given in Section IX.

2. Use of the Front Panel for Debugging and for Normal Operation

During debugging the entire Test Set is generally connected tothe SUMC-DV. The extra capacitance which this adds to the internal lines of the SUMC-DV makes it imperative that the CLOCK switch be left in the SLOW position. Under these conditions a program of any desired length permitted by the main memory capacity can be loaded into the SUMC-DV manually. To do this, the MEMORY ADDRESS switch on the front panel is left in the run position, and the address is set up from the 11 Test Set panel toggle switches labeled MAR. Then the ADDRESS ENTRY pushbutton on the SUMC-DV front panel is pressed entering the address. Data is entered into this address from the front panel by means of the 16 MAIN MEMORY DATA toggles. The

DATA switch must be in the SET position while different data is entered into one word after another in main memory, but before attempting to run it is important to remember that both the DATA and the MEMORY ADDRESS rotary switches must be returned to the RUN positions. Also if the Test Set is connected, all of the three-position toggle switches on the Test Set must be carefully checked to see that they are in the neutral center positions before attempting to run.

During debugging, frequent use is made of the two switches on the Test Set, labeled SINGLE EO and SINGLE INSTR. When one or the other of these toggle switches is thrown up, the program will not run continuously, but will halt automatically at the end of each EO or each instruction as the case may be to permit examination, and/or alteration of various internal register contents. It must be remembered that the program can be continued after such a halt only from the Test Set RUN pushbutton, and not from the SUMC-DV front panel START pushbutton. This is because the Test Set RUN pushbutton does not reset the sequencer, while the SUMC-DV START pushbutton does, causing the program to start over from the beginning again.

During normal operation, the Test Set is not connected to the SUMC-DV, and the CLOCK switch should be in the FAST position. Under these conditions, manual loading can only be accomplished for a program of no longer than 32 words. This limitation can, however, be overcome by the use of an I/O device such as a teletype machine with the SUMC-DV.

Programs up to 32 words in length may be entered manually by the following procedure:

(1) Turn on the POWER switch.

(2) Press the HALT pushbutton.

(3) Turn the DATA and the MEMORY ADDRESS switches to the SET mode.

(4) Press the ADDRESS RESET pushbutton.

(5) Set up a data word with all "zeros" except a "one" in the least significant bit on the DATA switches. (This is always the starting instruction for every program which does the initial housekeeping in the SUMC-DV.)

(6) Press the ADDRESS ENTRY pushbutton.

(7) Press the DATA ENTRY pushbutton.

(8) Press the INCREMENT ADDRESS pushbutton.

(9) Set up the next main memory word for the desired program.

(10) Repeat steps (6) through (9) until all of the program words and data are loaded. (Not more than 31 words.)

(11) Press the ADDRESS RESET pushbutton. (Returning to word "0", the starting location.)

(12) Press the ADDRESS ENTRY pushbutton.

(13) Turn the DATA and MEMORY ADDRESS switches to the RUN mode,

(14) Press the START pushbutton.

The SUMC-DV will now proceed to execute the program.

SECTION VI

IAROM AND MROM SUBSYSTEMS

A. GENERAL DESCRIPTION

Figure 6-1 shows the environment and the signal interfaces of the IAROM and the MROM which store the microinstructions and fetch them in the proper sequence with the proper timing.

The IAROM (Instruction Address Read Only Memory) consists of 256 words by 16 bits. It receives its 8-bit address from the eight lower order bits of the Instruction Register. The first eight bits of the output go directly to preset the sequencer each time a new instruction has been fetched and is ready to be executed. The remaining eight bits control certain functions which are invariant with respect to a given instruction.

The MROM (Microprogram Read Only Memory) consists of 256 words by 72 bits. The 8-bit address of this memory comes from the sequencer and changes each time a different type of EO is required. The 72 MROM bits go to buffer registers to be held while the EO which they control is being executed so that the MROM can be fetching the contents of the next address during this time.

B. HARDWARE IMPLEMENTATION

Both the IAROM and the MROM are implemented using the 1601 electrically programmable PMOS 2048-bit ROM chips. The chips are organized 256 words by 8 bits each. The IAROM requires two of these chips with the eight address lines paralleled. The MROM requires nine of these chips with the eight address lines paralleled. All interfaces to CMOS circuits are made straightforward and direct by shifting V_{DD} on the 1601 to -5 volts and shifting V_{CC} to +10 volts. Under these conditions, the chip is capable of accepting zero to +10-volt logic swings at the address inputs, and delivering zero to +10-volt logic swings at the data outputs fully compatible with CMOS logic.

Power dissipation averages 0.5 watt per chip, which gives a total power consumption of 1 watt for the IAROM, and 4.5 watts for the MROM. Because of the direct interfacing with CMOS levels, there is no further power loss or delay in level conversion buffers.

The 1601 is electrically programmable. This can be accomplished either by returning new chips to the manufacturer with a tape containing the desired information content in a format specified on the data sheet, or by building a manual programmer from an inexpensive kit supplied by the manufacturer. Electrical programming is accomplished at elevated voltage levels.

C. MROM REGISTERS

The ATL-000 24-pin MOS LSI chip is used as a buffer register for the 72-bit MROM field. Each of these chips has six CMOS static registers with a common input clock. The option for a direct (unclocked) output is used in this application. Although each of the six registers is a dual register only one of the two sections is actually used.

D. PACKAGING

The two IAROM chips are packaged on the IR board (A9). The nine MROM chips are packaged on the MROM board (A10). The MROM register chips are distributed among all the boards where the MROM field is actually utilized.

E. TIMING

Refer to Fig. 6-1, block diagram, and to Fig. 6-2 the system timing diagram.

A new instruction is clocked into the Instruction Register during CLA. It trickles through the instruction register and the IAROM, and appears at the output of the IAROM by 1 μs after CLA. From here it is clocked into the sequencer during

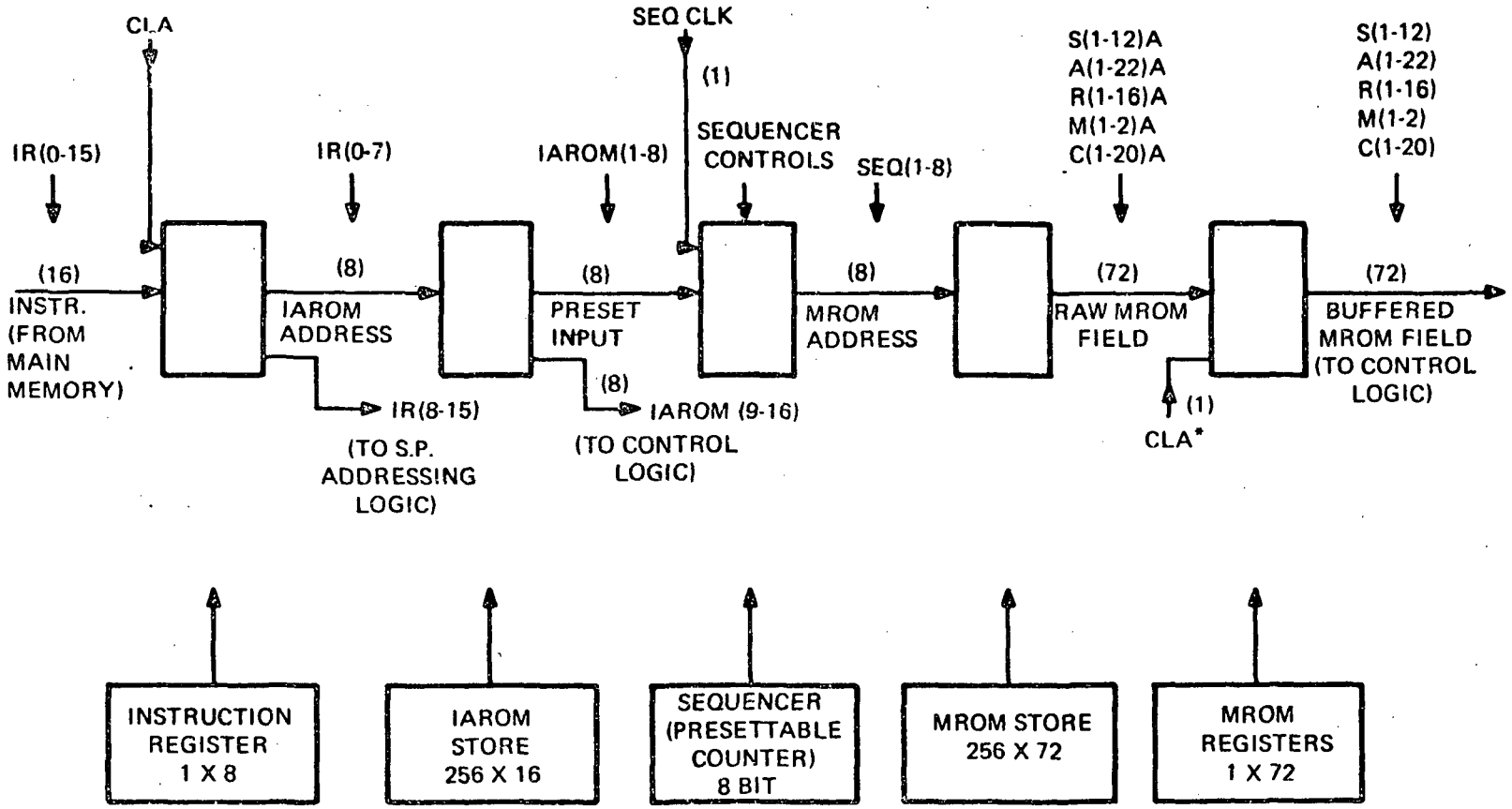


Fig. 6-1. IAROM and MROM block diagram.

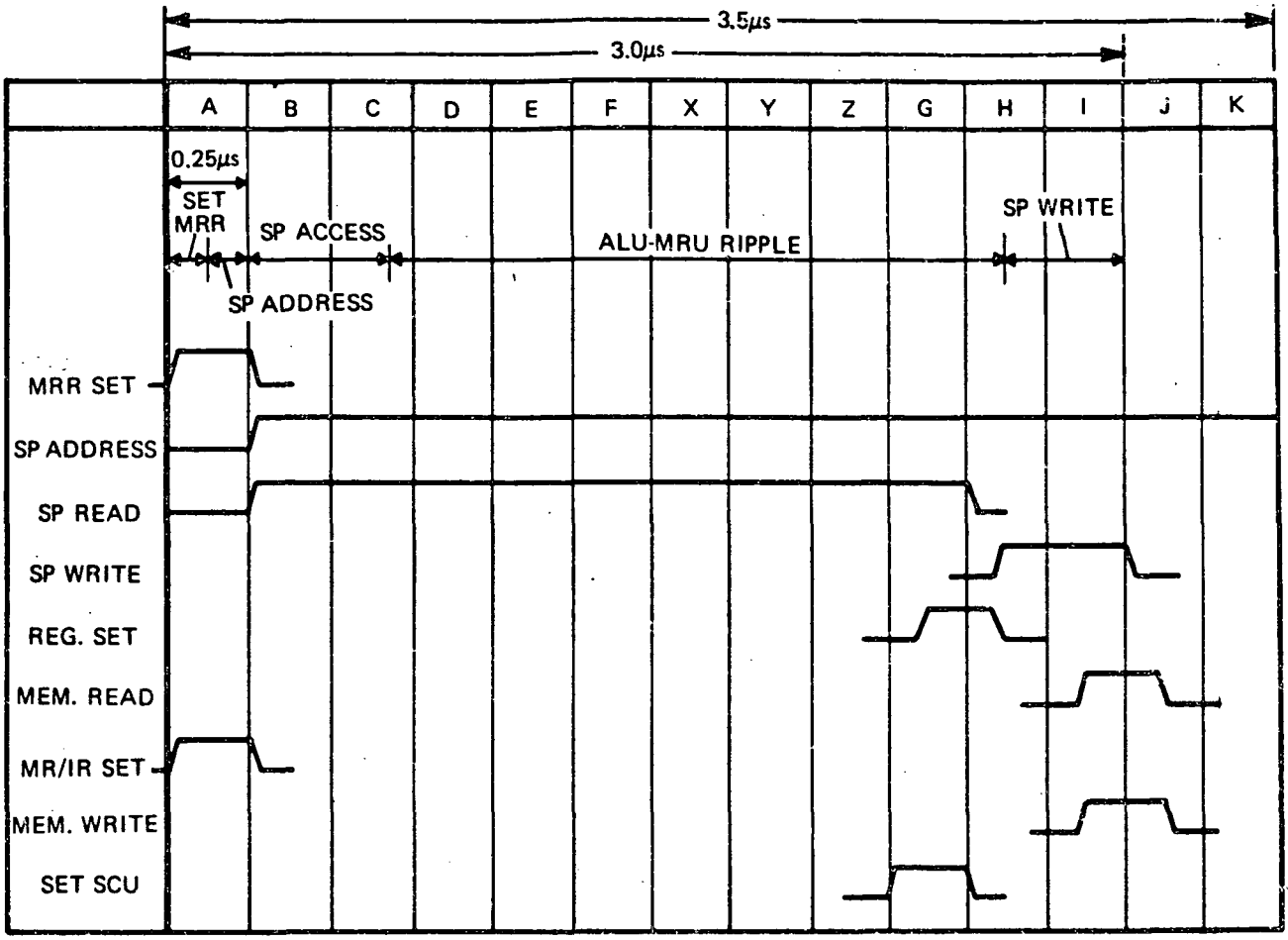


Fig. 6-2. System timing.

the same EO by the clock signal called SEQ CLK. This is a logically derived clock which is derived from CLG during a long EO. At this time the new address for the MROM trickles through the sequencer and into the MROM. After another microsecond, the new MROM field for this new address is available at the output of the MROM, and it is clocked into the MROM register by the CLA pulse at the beginning of the following EO.

The sequencer contents (and hence the MROM address) might change during any EO during the time slot controlled by SEQ CLK, but the controls are buffered by the MROM register until the start of the following EO.

SECTION VII

SCRATCH PAD MEMORY SUBSYSTEMS

A. ORGANIZATION AND PACKAGING

The scratch pad memory is a random access CMOS memory with current sensing. A block diagram of the memory, showing graphically how it is organized, is shown in Fig. 7-1. It has 32 words of 16 bits each. This memory is located on the A8 plug-in board of the SUMC-DV which contains 53 dual-in-line packages as shown in Fig. 7-2. Four of these packages have 16 pins, the rest 14 pins. In addition there are 51 resistors, a diode, and decoupling capacitors. As shown in Fig. 7-3, the data input from the scratch pad memory is on the MQR bus: MQR0 through MQR15. The data output from the scratch pad memory are located on the SPM bus: SPM0 through SPM15. The address registers for the scratch pad memory are located on the ATL-005 chip on the IR board (A9). The outputs from the address register S0D through S4D go from A9 to A8 on the backplane. The address decoding is on A8. There is one control line: S9D. This line goes low during a write to SPM and high during a read from SPM.

B. BASIC MEMORY UNIT

The RAM chip used in the scratch pad memory is a 16-word by 1-bit CMOS chip with X-Y select and current sensing. It is contained in a 14-pin dual-in-line package, and is a member of RCA's CMOS product line. For further information see the data sheet for the CD4005D.

Thirty-two of these units on the A8 board make up the total storage of 32 words by 16 bits.

C. ADDRESS DECODER

The address decoder for the scratch pad memory is implemented by CMOS 16-pin dual-in-line packages. There are four CD chips in the scratch pad memory

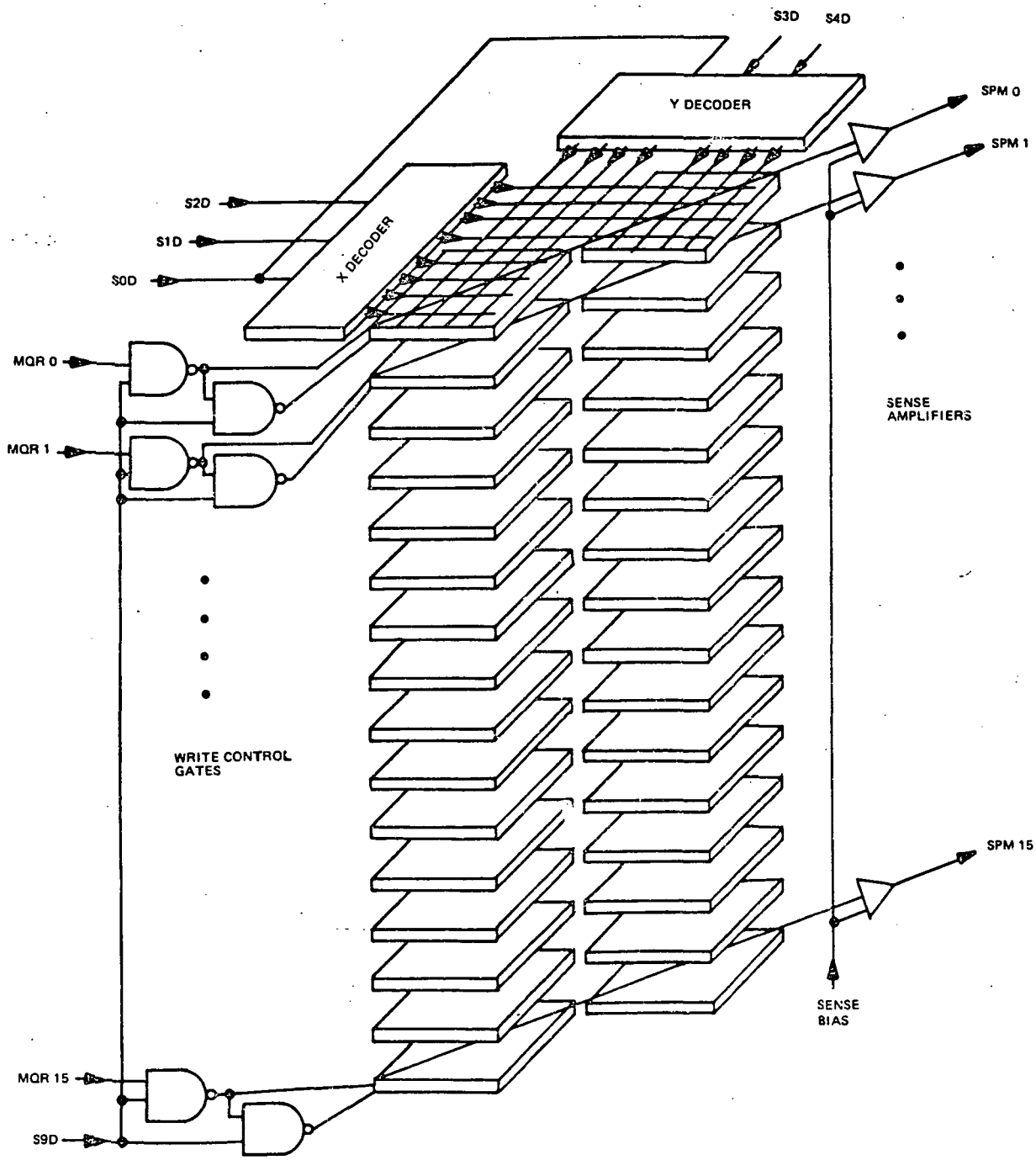
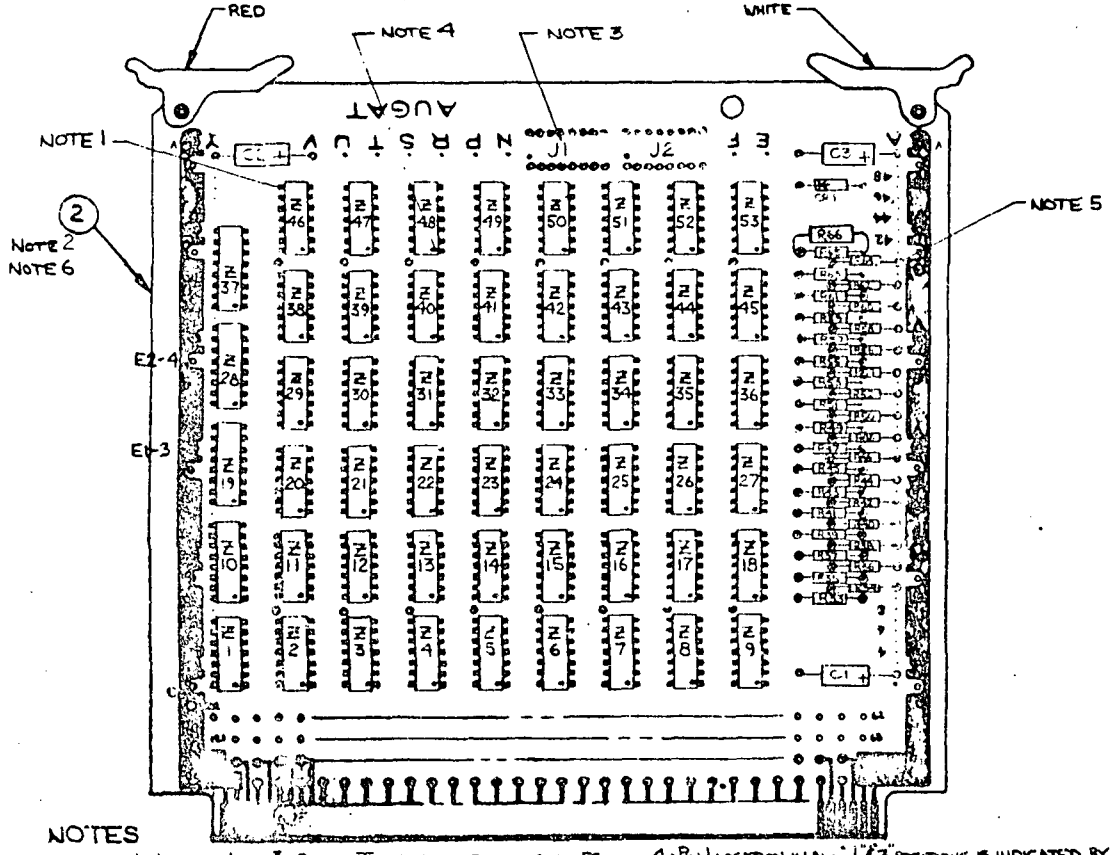


Fig. 7-1. SUMC-DV scratch pad block diagram.



NOTES

1- INSTALL ITEM 3 SOCKET TERMINAL IN EXISTING HOLES FOR ALL ITEM "Z" PIN LOCATIONS.
2- WIRE OPPOSITE SIDES OF BOARD IN ACCORDANCE WITH ITEM 9 USING ITEMS 5,6,7 & 8 APPROPRIATELY
3- J1 & J2 ARE FORMED BY DRILLING .055 +.001 -.002 DIA HOLES (IF NON-EXISTANT) IN THE LOCATIONS SHOWN AND INSTALLING ITEM 3 SOCKET TERMINALS IN THESE LOCATIONS.
4- PIN 1 LOCATION IN ALL "J" & "Z" POSITIONS IS INDICATED BY A DOT(•).
5- INSTALL ITEM 4 TERMINALS IN THE LOCATIONS SHOWN FOR MOUNTING C1,C2,C3, CR1, AND R33 THRU R66 INCLUSIVE.
6- SEE TABLE 1 ON SHEET 2 FOR LOCATION OF ITEMS MOUNTED ON THE WIRING SIDE OF THE BOARD.

ITEM	QTY	PART NUMBER	DESCRIPTION
R19	–		
R18	–		
R17	–		
R16	–		
R15	–		
R14	–		
R13	–		
R12	–		
R11	–		
R10	2	RC07GF220K	RESISTOR, CARBON COMP
R9	2	RC20GF471K	
R8	1	RC07GF182K	
R7	1	RC07GF182K	
R6	1	RC07GF182K	
R5	1	RC07GF182K	
R4	1	RC07GF182K	
R3	1	RC07GF182K	
R2	1	RC07GF182K	
R1	1	RC07GF182K	RESISTOR, CARBON COMP
J2			NOTE 3
J1			
CR1	1	IN483B	DIODE
C6	1	5C023104X500B3	SPRAGUE-MONOLYTHIC CERAMIC CAPACITOR .1, 50V.
C5	1	5C023104X500B3	SPRAGUE-MONOLYTHIC CERAMIC CAPACITOR .1, 50V.
C4	1	5C023104X500B3	SPRAGUE-MONOLYTHIC CERAMIC CAPACITOR .1, 50V.
C3	1	CS13BD226K	CAPACITOR
C2	1	CS13BD226K	CAPACITOR
C1	1	CS13BD226K	CAPACITOR
9	X	WLSK12127IRGA	WIRE CONNECTION LIST
8	AR	2240350-820	SOLDER, ROSIN CORE, 63/37
7	AR	8418740-6	SLEEVING
6	AR	299/2	ALPHA - WIRE, SOLID, TINNED CU #28 AWG
5	AR	B5097745-3	WIRE, SOLID, TINNED COPPER, INSULATED
4	74	155-3849-01-08	CAMBION - WIREWRAP TERMINAL
3	798	LSG-1F66-1	AUGAT INC. - SOCKET/TERMINAL
2	1	AX145-71-161	AUGAT INC. - I.C. PACKAGING PANEL
1	1		ASSEMBLY, WIRED BOARD

BOARD ASSEMBLY SPM
(SCRATCH PAD MEMORY)

RCA, ATL
CAMDEN, N.J.

SHEET 1 OF 2

B | SKI2127IRGA

Fig. 7-2. Scratch pad memory plug-in board A8 (sheet 1 of 2)

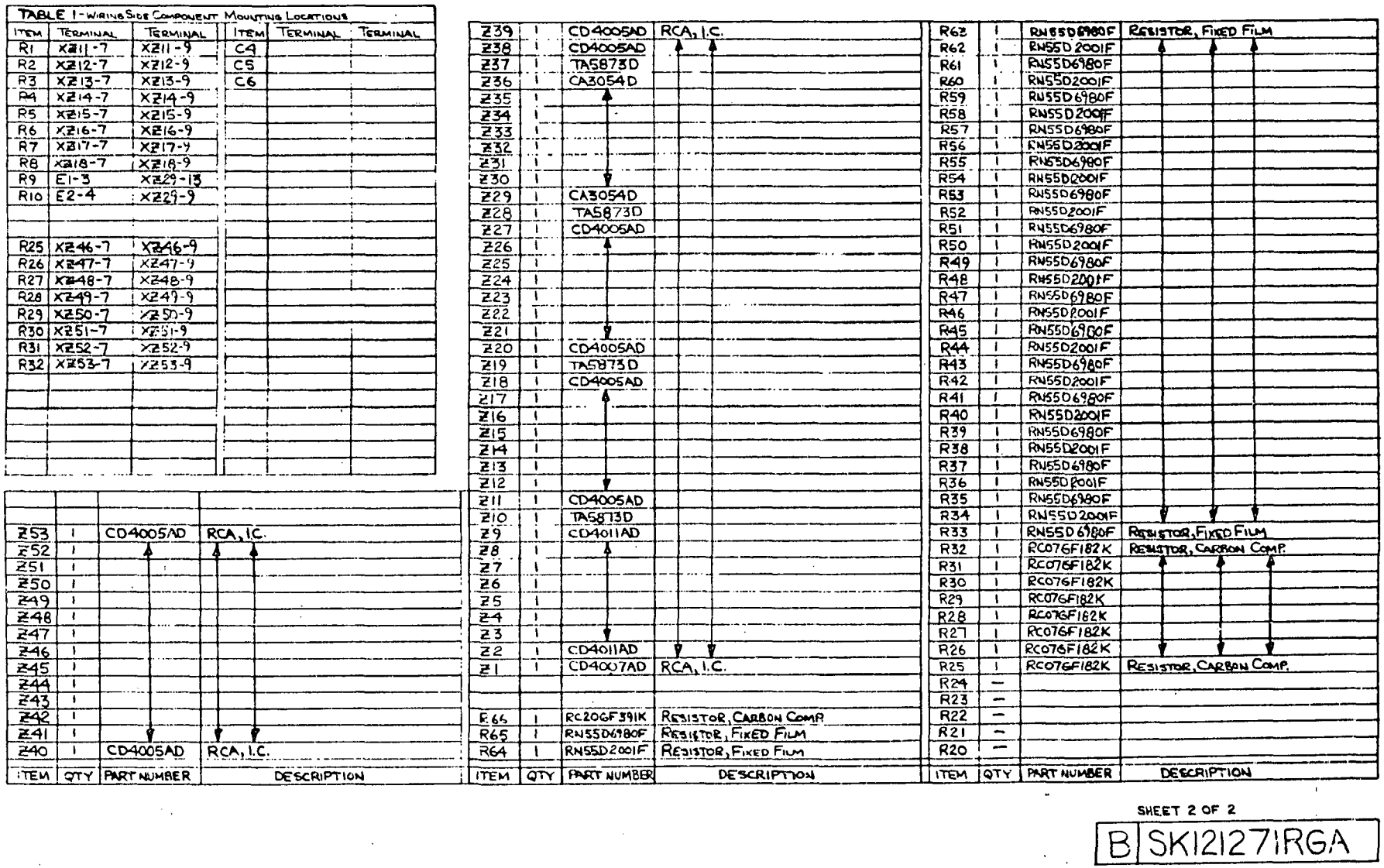


TABLE 1 - WIRING SIDE COMPONENT MOUNTING LOCATIONS

ITEM	TERMINAL	TERMINAL	ITEM	TERMINAL	TERMINAL
R1	XZ11-7	XZ11-9	C4		
R2	XZ12-7	XZ12-9	C5		
R3	XZ13-7	XZ13-9	C6		
R4	XZ14-7	XZ14-9			
R5	XZ15-7	XZ15-9			
R6	XZ16-7	XZ16-9			
R7	XZ17-7	XZ17-9			
R8	XZ18-7	XZ18-9			
R9	E1-3	XZ29-13			
R10	E2-4	XZ29-9			
R25	XZ46-7	XZ46-9			
R26	XZ47-7	XZ47-9			
R27	XZ48-7	XZ48-9			
R28	XZ49-7	XZ49-9			
R29	XZ50-7	XZ50-9			
R30	XZ51-7	XZ51-9			
R31	XZ52-7	XZ52-9			
R32	XZ53-7	XZ53-9			

ITEM	QTY	PART NUMBER	DESCRIPTION
Z53	1	CD4005AD	RCA, I.C.
Z52	1		
Z51	1		
Z50	1		
Z49	1		
Z48	1		
Z47	1		
Z46	1		
Z45	1		
Z44	1		
Z43	1		
Z42	1		
Z41	1		
Z40	1	CD4005AD	RCA, I.C.
Z39	1	CD4005AD	RCA, I.C.
Z38	1	CD4005AD	
Z37	1	TA5873D	
Z36	1	CA3054D	
Z35	1		
Z34	1		
Z33	1		
Z32	1		
Z31	1		
Z30	1		
Z29	1	CA3054D	
Z28	1	TA5873D	
Z27	1	CD4005AD	
Z26	1		
Z25	1		
Z24	1		
Z23	1		
Z22	1		
Z21	1		
Z20	1	CD4005AD	
Z19	1	TA5873D	
Z18	1	CD4005AD	
Z17	1		
Z16	1		
Z15	1		
Z14	1		
Z13	1		
Z12	1		
Z11	1	CD4005AD	
Z10	1	TA5873D	
Z9	1	CD4011AD	
Z8	1		
Z7	1		
Z6	1		
Z5	1		
Z4	1		
Z3	1		
Z2	1	CD4011AD	
Z1	1	CD4007AD	RCA, I.C.
R66	1	RC20GF391K	RESISTOR, CARBON COMP
R65	1	RN55D6980F	RESISTOR, FIXED FILM
R64	1	RN55D2001F	RESISTOR, FIXED FILM
R63	1	RN55D6980F	RESISTOR, FIXED FILM
R62	1	RN55D2001F	
R61	1	RN55D6980F	
R60	1	RN55D2001F	
R59	1	RN55D6980F	
R58	1	RN55D2001F	
R57	1	RN55D6980F	
R56	1	RN55D2001F	
R55	1	RN55D6980F	
R54	1	RN55D2001F	
R53	1	RN55D6980F	
R52	1	RN55D2001F	
R51	1	RN55D6980F	
R50	1	RN55D2001F	
R49	1	RN55D6980F	
R48	1	RN55D2001F	
R47	1	RN55D6980F	
R46	1	RN55D2001F	
R45	1	RN55D6980F	
R44	1	RN55D2001F	
R43	1	RN55D6980F	
R42	1	RN55D2001F	
R41	1	RN55D6980F	
R40	1	RN55D2001F	
R39	1	RN55D6980F	
R38	1	RN55D2001F	
R37	1	RN55D6980F	
R36	1	RN55D2001F	
R35	1	RN55D6980F	
R34	1	RN55D2001F	
R33	1	RN55D6980F	RESISTOR, FIXED FILM
R32	1	RC076F182K	RESISTOR, CARBON COMP.
R31	1	RC076F182K	
R30	1	RC076F182K	
R29	1	RC076F182K	
R28	1	RC076F182K	
R27	1	RC076F182K	
R26	1	RC076F182K	
R25	1	RC076F182K	RESISTOR, CARBON COMP.
R24	—		
R23	—		
R22	—		
R21	—		
R20	—		

Fig. 7-2. Scratch pad memory plug-in board A8 (sheet 2 of 2).

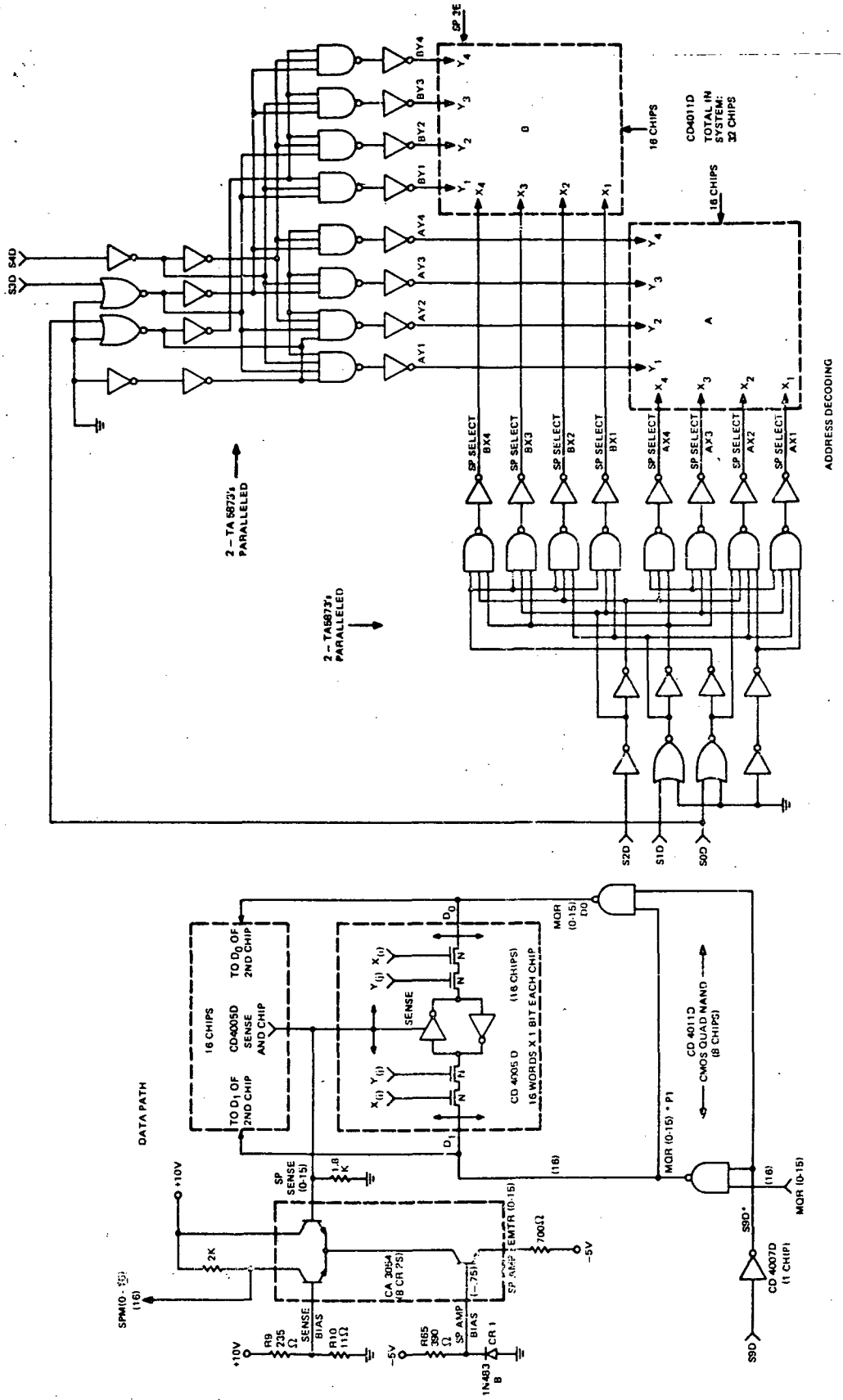


Fig. 7-3. Scratch pad RAM (32 words x 16 bits), schematic diagram.

board. Two of them, with all inputs and outputs wired in parallel, drive the X selection lines of the 32 storage chips. The other two drive the Y selection lines of the 32 storage chips as shown in Fig. 7-3. Note that each paralleled output drives only 16 storage chips, which is a fan out of eight-to-one per output of the decoder. This optimum balancing of the load is made possible by the diagonal positions of the two alternate blocks of memory seen in the schematic, and this in turn is achieved by repeating address bit SOD in the corresponding input to both the X and Y decoders. The purpose of paralleling decoder chips is to speed up the access time by reducing the capacitive loading on the decoder output.

D. SENSE AMPLIFIER

The sense amplifier in the scratch pad memory is a bipolar differential integrated circuit amplifier with three discrete resistors per amplifier plus one biasing divider network for the entire group of 16 amplifiers. The integrated circuit chip is in a 14-pin dual-in-line package with two differential amplifiers per package.

The circuit arrangement for the scratch pad memory sense amplifier is shown in Fig. 7-3. It is a common emitter current steering circuit with the input base driven from a current sensing resistor. The minimum current developed through the current sensing resistor by the selected storage element during the sensing of a logical "one" is 0.5 mA, which develops a sense voltage of 0.9 volt at the input to the current steering amplifier. The sense bias voltage on the opposite base of the amplifier is fixed by the divider at 0.45 volt which is midway between a "zero" and a worst case "one". This is the amount of differential voltage needed to insure the full 10-volt swing at the output collector. There is no inversion at the collector output since the noninverting output transistor of the complementary circuit is used.

A diode reference voltage fixes the voltage across the emitter resistor. This sets the load current at 0.5 mA, which will pull the output to zero volts across the 2K output resistor when all the current is switched. See Fig. 7-3.

During a read operation both D1 and D0 are held high since the CMOS NAND gates driving these modes are both inhibited by the read-write control, S9D.

During a write operation, the output of the sense amplifiers are forced to zero.

E. INTERFACE WITH TEST SET OVERRIDES

The A8 scratch pad memory board has two J connectors which can be used for connecting to the Test Set for diagnostic purposes. One of these two connectors, J1, carries the 16-bit MQR bus which serves as an input bus for writing into scratch pad memory. This bus cannot be displayed on the Test Set panel, but when J1 of A8 is connected to P6 on a ribbon connector from the Test Set, it is then possible to override the MQR bus from the 16 SCRATCH PAD DATA toggle switches on the Test Set panel. These switches do not destroy the contents of the MQR register, but can be made to override the bus and permit manual loading of the scratch pad from the test set. When returned to the central neutral position, the manual toggle switches disconnect and return control of the bus to the previous contents of the MQR register. The purpose of these override toggle switches is to allow manual writing into the scratch pad memory for diagnostic purposes. Once the MQR bus is set manually, writing into the scratch pad will still not occur with the ENTER push-button on Test Set panel depressed. This pushbutton overrides the S9D write control signal (normally high) causing it to go momentarily low so that manual write to the scratch pad memory can occur.

This can only be accomplished when J1 of A9 (the IR board) is connected to P8 on a ribbon connector from the Test Set, since the write control signal, S9D, is carried to the Test Set by this connector. Also carried by J1 of A8 are the five scratch pad address bits S0D, S1D, S2D, S3D and S4D. When writing manually from the Test Set, it is usually desirable to manually set up the scratch pad address. This can be done when J1 of A9 is connected to P8 of the Test Set by using the five switches labeled SPA on the Test Set panel to override the scratch pad address bus in exactly

the same manner as described for overriding the MQR bus data. Again, the neutral center position returns control to the scratch pad address register. In this case, no pushbutton is needed to enter the address into the memory.

The scratch pad address can be overridden by the SPA switches on the Test Set panel regardless of the position of the MONITOR SELECTOR switch on the Test Set panel. However, if it is desired to monitor the scratch pad address, this can be done by turning the MONITOR SELECTOR switch to the MAR & SPA position. Then if J1 of A9 is connected to P8 of the Test Set, the right five DATA lights will show the contents of the scratch pad address register as they feed into the memory board, A8.

Connector J2 of A8 carries the 16-bit SPM bus which is the data output bus from the scratch pad memory. When J2 of A8 is connected to P7 on the ribbon connector from the Test Set, it becomes possible to display the 16-bit SPM bus on the 16 SCRATCH PAD DATA indicator lamps by turning the MONITOR SELECTOR switch to the SP position.

When the test set is connected to the SUMC-DV, all override toggle switches must be in the neutral position when attempting to run a program with the SUMC-DV.

F. TIMING

The scratch pad memory is in the critical delay portion of the data path for the SUMC-DV. See Fig. 7-4, the block diagram for the SUMC-DV. The worst case EO time occurs on an EO which begins with a scratch pad access, continues through an arithmetic operation involving worst case carry in both arithmetic units, receives the result in the MQR register, and ends by writing this result back into the scratch pad memory at the same scratch pad address where the read was done initially. The measured read access time for the scratch pad memory in an actual program being run in the DV from the 50% n point of the S0D through S4D address bus to the 50% point of the SPM bus is 400 ns reflecting the system loading. With no external loading on the output bus, the measured access time during bench testing was 300 ns.

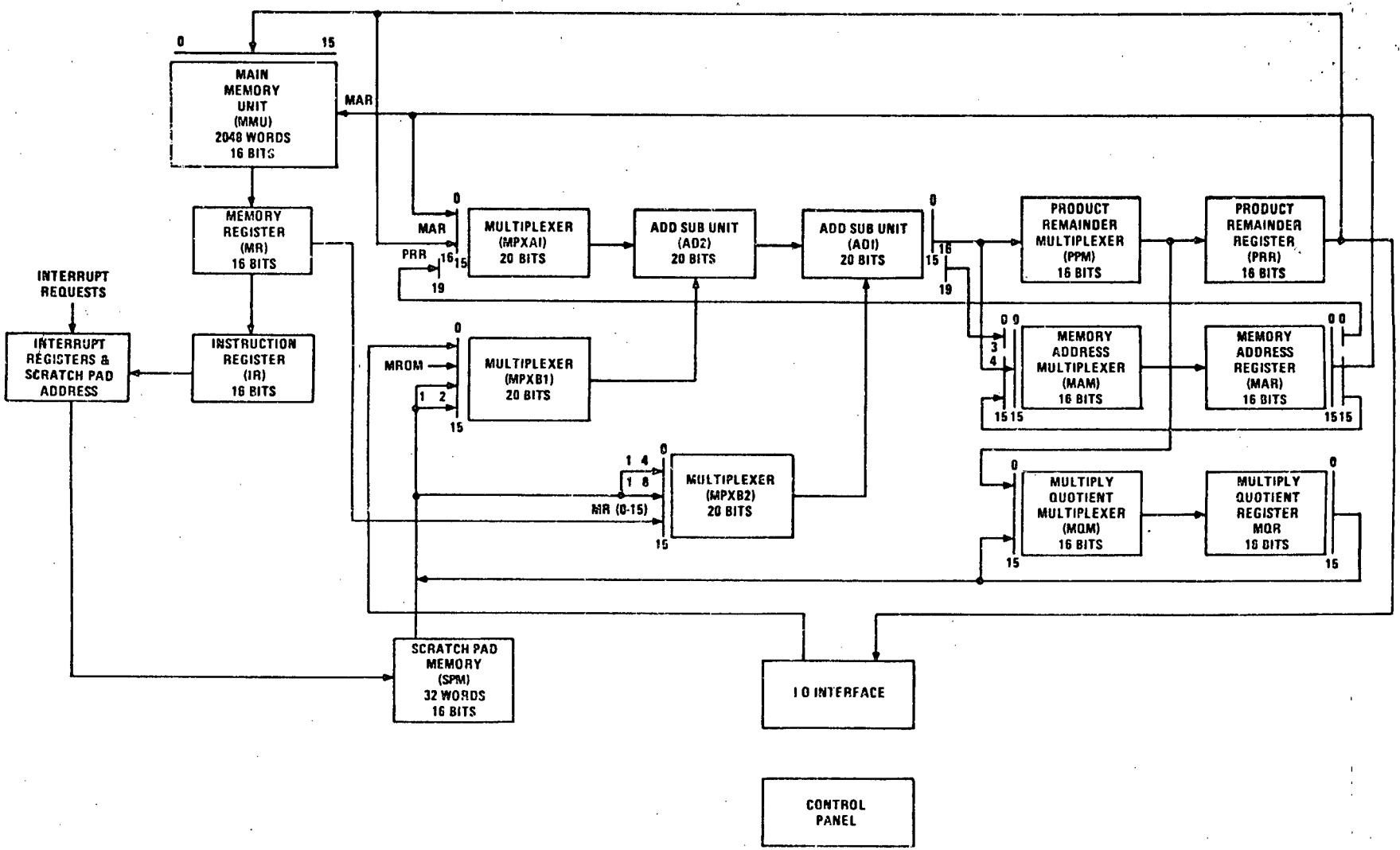


Fig. 7-4. SUMC-DV block diagram.

The loading on the SPMO output of the scratch pad in the SUMC-DV, for example, was measured as 120 pF. This results in a 120-ns delay from the start of the output transition to the 50% point. Another 200 ns of the access time is in the decoder circuit. This delay is primarily due to the large fan out required to drive the appropriate memory chips located on the scratch pad board. The data sheet for the CD4005D shows a delay of 25 ns from X, Y selection to the sense current output, which is nominally 0.5 mA. In order to fully switch the output current of the differential amplifier, a voltage swing of 1 volt is required. The total load capacitance at the output node is 40 pF. To charge this output node through 1 volt with 0.5 mA of current requires 80 ns which adds directly to the access time and the critical path delay.

Within the framework of the same basic design, the access time reflects a speed/power ratio in that reduced access times are achievable with increased power dissipation.

G. POWER DISSIPATION

The power dissipation of the scratch pad memory is divided among the two amplifier biasing networks which dissipate 400 mW for the sense bias and 60 mW for the current control, and the leakage of the CMOS chips which is only a few microwatts at most. The sense amplifiers each have a constant current drain of 5 mA regardless of whether they are sensing a "one" or a "zero". This current flows between the -5-V and the +10-V power supplies, resulting in a power dissipation of 75 mW per sense amplifier. The 16 amplifiers on the A8 board together dissipate 1.2 watts. Thus the total power dissipation on the scratch pad board is:

$$1.2\ W + 0.4\ W + 0.06\ W = 1.66\ \text{watts}$$

If the current in the sense amplifier were doubled, the 120 ns delay from the start of the output transition to the 50% point could be cut in half. The cost in power for reducing the access time by 60 ns would be a doubling of the 1.2 watts in the amplifier to 2.4 watts, or an increase of 1.2 watts in the dissipation on the A8 board.

SECTION VIII

MAIN MEMORY SUBSYSTEM

A. ORGANIZATION

The main memory in the SUMC-DV is a random access memory organized in a 2,048-word by 16-bit format. This provides an addressable capability up to 65,536 words.

Figure 8-1 shows the main memory block diagram. The main memory contains an internal address register. The M2TLS (normally high) control pulse must be set low to clock the 11-bit address (MAR5 through MAR15) into the address register. Since there is no data register in the main memory, the contents of the new address appear directly on the 16 data output lines MR0 through MR15. One other control pulse, M1T LS (normally low), goes high to write new information into the main memory. This new information is entered into the word at the address location held in the internal address register at the time of data entry. Data entry during write is accomplished from the bus PRR0 through PRR15.

B. TECHNOLOGY

The main memory in the SUMC-DV is made up of four purchased printed circuit boards. Each board contains a number of hybrid packages made up of two LSI chips each. The technology used in the LSI chips is all bipolar. The interfaces on all of these boards are T^2L logic interfaces. Each of the four boards has 1,024 words. Two boards have 8 data bits and the other two have 9 data bits. The extra data bit is not used in the SUMC-DV, and the output pins on these boards are such that all four boards are completely interchangeable. Expansion of the four boards is accomplished by phantom "or" connections between corresponding data output connections. The P_s input on each board is wired to the E_1' and E_1 reconfiguration inputs for the address extension. This node must go high to select a pair of boards.[1]

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1. Refer to SEMI, Inc. data sheet RAM 388B for additional details.

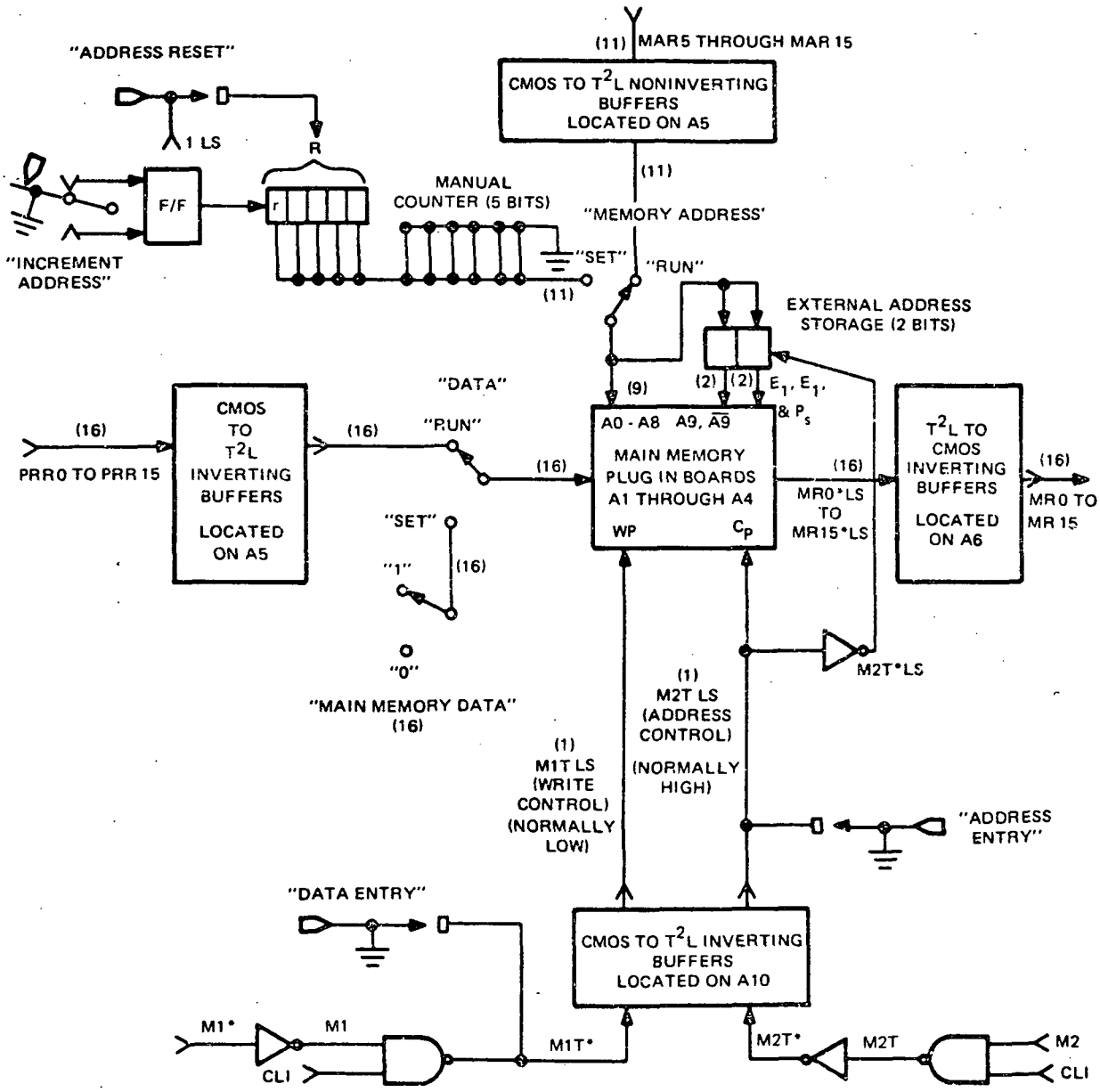

Fig. 8-1. Main memory block diagram.

C. ADDRESS DECODING

The address registers and decoding are on all boards for address bits MAR7 through MAR15. Address bits MAR5 and MAR6 both require external registers, but no external decoding. For MAR5 the true and inverted outputs from the external register both go to all four boards. For MAR5 the true outputs from the external register select boards A1 and A3, while the inverted outputs select boards A2 and A4. These external T^2L registers are located on the board which is mounted on standoffs behind the control panel of the SUMC-DV.

D. MANUAL LOADING FROM THE CONTROL PANEL

When power to the SUMC-DV is switched on, the main memory may assume arbitrary random states. Before a program can be loaded into the main memory via the I/O interface, it is necessary to load a few locations manually near the start of main memory to facilitate a bootstrap instruction which exists in the MROM. To accomplish this the control panel of the SUMC-DV (Fig. 5-6) has 16 MAIN MEMORY DATA toggle switches for entering data manually into the main memory. In addition there is a DATA rotary switch with 16 poles. When this switch is in the SET position, it switches the memory data inputs from the PRR in the SUMC-DV to these 16 manual switches. There is also a DATA ENTRY pushbutton which manually overrides the M1T* signal which is normally high. This pushbutton forces the signal momentarily to ground. The M1T LS signal on the memory interface is derived from this through an inverting level shifter. When it goes high momentarily, data enters the memory.

During the manual load operation it is also necessary to set up the address manually. In order to accomplish this, there is a five-bit counter located on the board behind the main panel which can be advanced by means of the INCREMENT ADDRESS pushbutton on the SUMC-DV front panel, and reset by means of the ADDRESS RESET pushbutton on the same panel. There are also five lights at the top of this panel which indicate the state of the address counter at all times.

In order to present this address to the main memory rather than the address which is present in the MAR, the MEMORY ADDRESS rotary switch must be turned to the SET position. Although the manual address is then presented at the main memory interface, it does not enter the internal address register until the ADDRESS ENTRY pushbutton on the SUMC-DV panel is depressed. This pushbutton is a direct override of the M2T LS T^2L level signal (normally high) which momentarily shorts it to ground. During manual address entry, the counter bits are entered as the five least significant address bits while the remaining six most significant bits are wired to ground. Thus only the 32 words with minimum address are available for direct manual entry, which is more than adequate for bootstrapping operations.

E. INTERFACE WITH CPU

Since the main memory requires a T^2L interface (0 to 3.5 V with a current sink for low levels) and the CPU requires a CMOS interface (0 to +10 V with no standby power), conversion buffers are used. The T^2L to CMOS buffer used in the SUMC-DV is an inverting buffer. It is similar to the standard T^2L inverter with an open collector except that the output collector is designed to withstand higher voltages. This makes it possible to tie the external pull up resistors to +10 V to effect the level change from T^2L to CMOS levels. The CMOS to T^2L buffer used in the SUMC-DV is on a CMOS chip and comes in both inverting and noninverting forms.

The memory register (MR) lines from the main memory use the T^2L to CMOS buffer. Since this is an inverting buffer, all data in the main memory is stored in the inverted form. These T^2L to CMOS buffer inverters are located on the ALU-2 board.

The PRR outputs are connected to the data input lines of the main memory through CMOS to T^2L inverting buffers which are located on the MRU board.

The MAR outputs are connected to the main memory address inputs through CMOS to T^2L noninverting buffers which are also located on the MRU board.

The M1T and the M2T control signals are controlled by the MROM, gated with the CLI clock, and converted to T^2L levels by passing through CMOS to T^2L buffers located on the MROM board.

F. TIMING

As shown in Fig. 6-2, the SUMC-DV timing diagram reading from main memory requires one EO time period to place the desired address in the MAR. Near the end of this EO during clock pulse CLI, M2T clocks the address into the main memory internal register. By the beginning of the following EO, the data will be on the MR data lines ready to use.

Writing into main memory requires two ECs. During the first EO, the address is transferred into the MAR and clocked on CLI just as in a read. During the second EO the data to be written is transferred into the PRR and clocked into the main memory near the end of this EO by means of the M1T LS line which is gated with the CLI clock. This data enters the word address which was set up on the previous EO and is firm on the MR lines in time to be used on the following EO if desired.

G. POWER DISSIPATION

The main memory boards proper dissipate 25 watts. The interface circuits which adapt the main memory to the processor dissipate an additional 0.8 watt.

SECTION IX

SUMC-DV CLOCK GENERATOR

The clock generator provides the basic timing pulses for the SUMC-DV. It also implements the RUN, HALT, SINGLE EO and SINGLE INSTR modes of operation. Two variable master oscillators provide flexibility in selection of the basic timing slot interval and hence the length of the basic elementary operation.

A. IMPLEMENTATION

Circuit construction is implemented entirely with Complementary-Symmetry/ Metal-Oxide Semiconductor (COS/MOS or CMOS) small scale and medium scale integrated packages. Eighteen packages are required for full clock generator implementation. All of the clock generator circuitry is operated off the +10-volt supply line and is completely contained on the Interrupt Register (IR) plug-in board.

The clock generator can be divided into five functional blocks as shown in Fig. 9-1. These blocks are designated as the control circuitry, sync circuitry, two-phase shift register, oscillator and the gating circuitry. Activation of the clock generator is initiated when the console START or test set RUN pushbutton is depressed. The control circuitry accepts the initiate signal and, in turn, conditions the sync circuitry to begin clock pulse generation. The free running oscillator continually pulses both the sync circuitry and the two-phase shift register. When the clock generator is in the HALT mode of operation, the sync circuitry inhibits a regenerative feedback loop in the two-phase shift register from generating the proper logic for clock pulse formation. When the sync circuitry is conditioned to RUN, the feedback circuitry in the two-phase shift register is activated and the oscillator pulses to the two-phase shift register are phase oriented. The two-phase shift register is now able to generate the waveforms shown in Fig. 9-2. By selectively gating these waveforms, the gating circuitry generates the clock pulses used to drive the SUMC-DV. The SUMC-DV clock pulses are shown in Fig. 9-3.

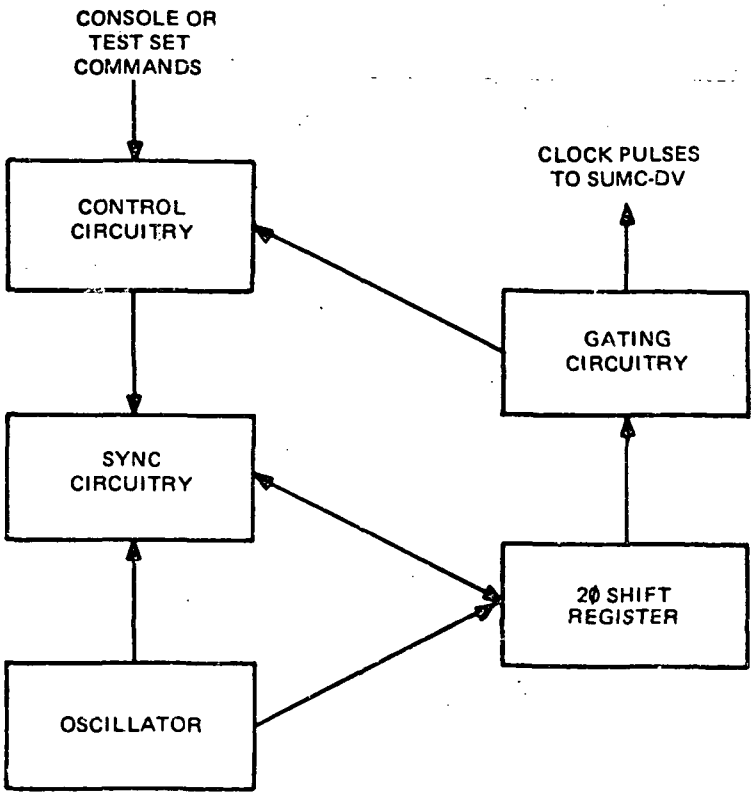

Fig. 9-1. SUMC-DV clock generator block diagram.

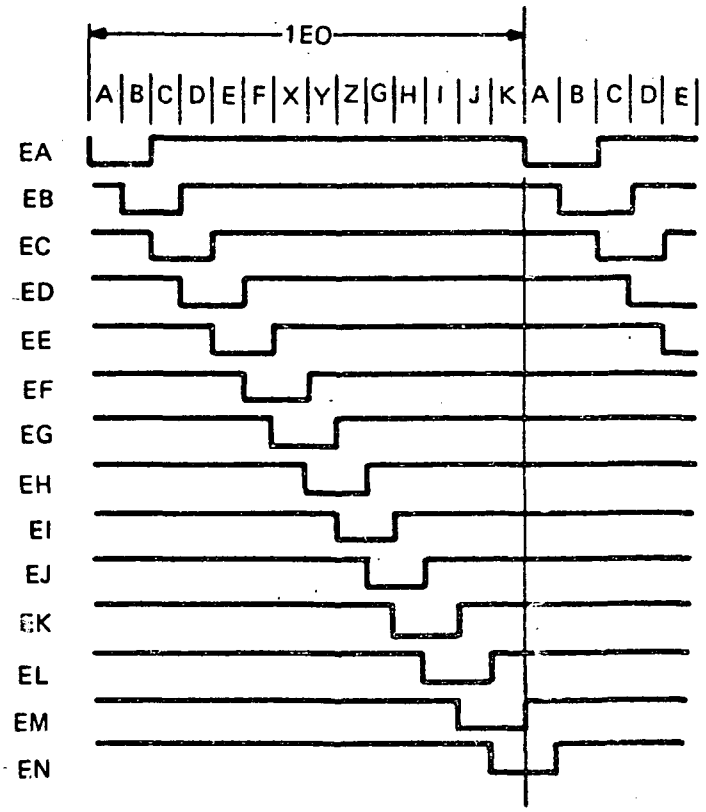

Fig. 9-2. 2-phase shift register output waveforms.

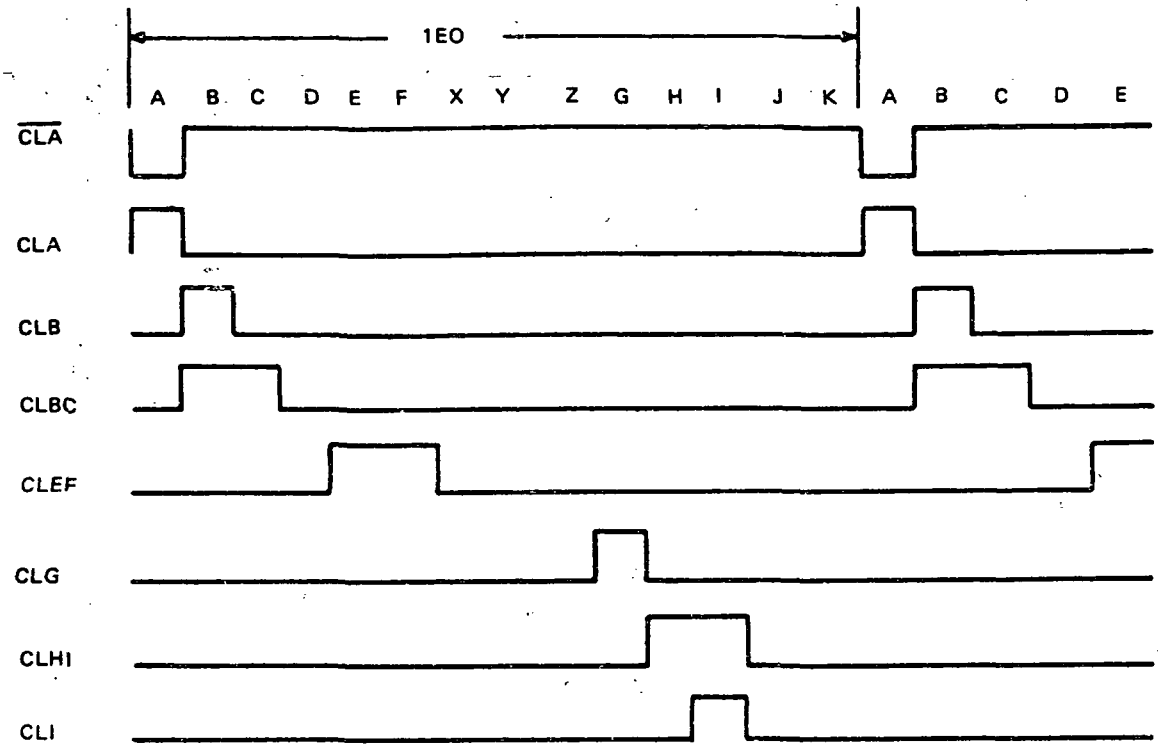

Fig. 9-3. SUMC-DV clock pulses.

The logic diagram of the clock generator is presented in Fig. 9-4. It is partitioned into blocks to correspond with the block diagram of Fig. 9-1.

B. OSCILLATOR

Two oscillator circuits are included in the clock generator. Each of the circuits is a two-inverter astable multivibrator utilizing an R-C combination as the timing components. Potentiometers in the resistance leg allow a range of frequency adjustment and diode shunting provides duty cycle control. Each oscillator uses a two-input nor gate as one of its inverters to provide an oscillator inhibit capability. Oscillator selection is controlled from the CLOCK switch on the SUMC-DV panel. With the CLOCK switch in the SLOW position, signal SF is a logical 0. This inhibits the fast oscillator and allows the slow oscillator to free run. Switching the CLOCK switch to the FAST position changes signal SF from a logical 0 to a logical 1. This inhibits the slow oscillator and allows the fast oscillator to free run.

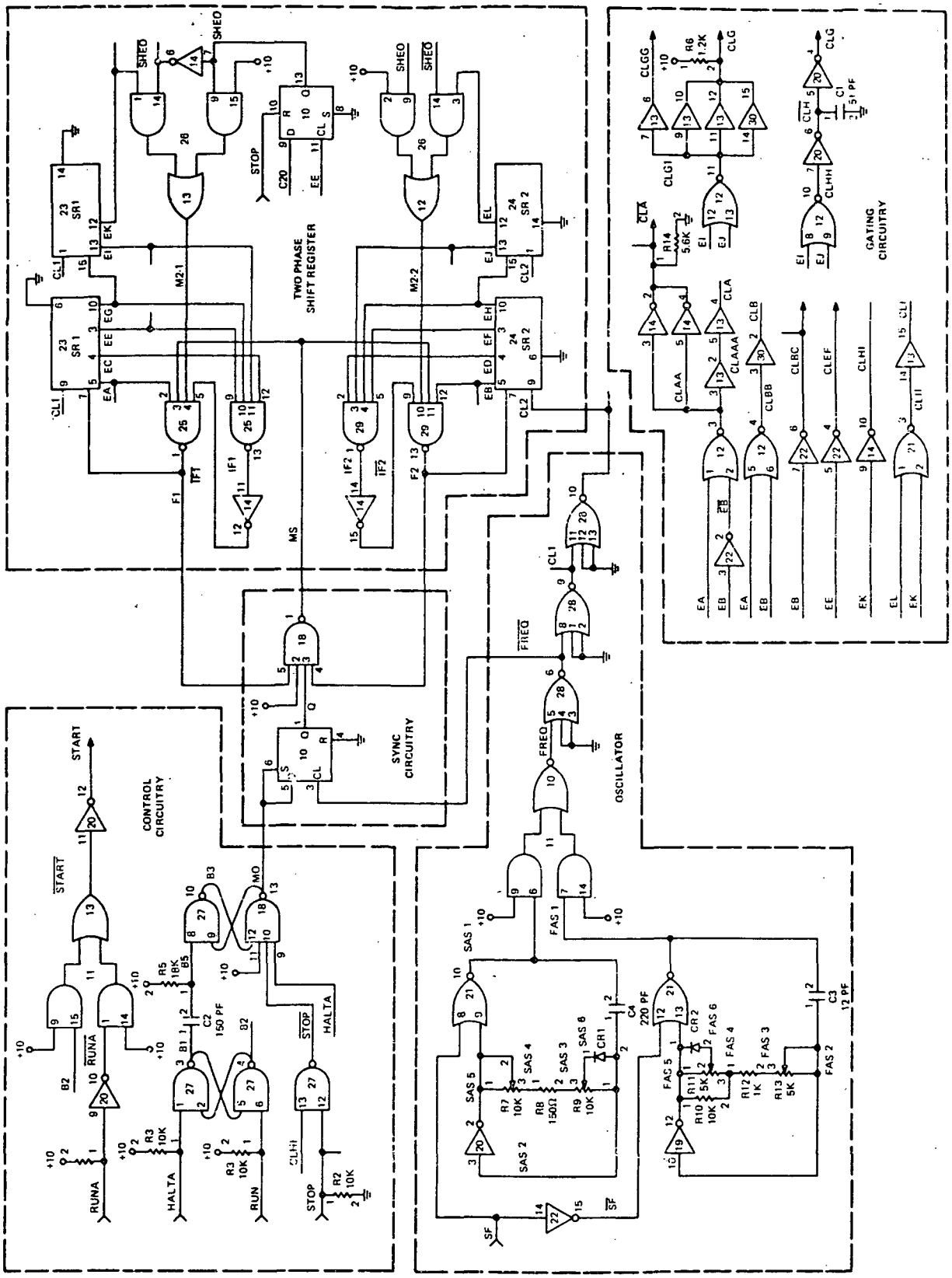

Fig. 9-4. Clock generator logic diagram.

The slow oscillator has a continuously variable range of frequency adjustment from 210 kHz to 300 kHz. This frequency range guarantees a range of 23.3 μs to 33.3 μs in the length of an elementary operation. Adjustment of the slow oscillator frequency is made by adjusting potentiometer R7. Potentiometer R9 is adjusted to control the duty cycle of the slow oscillator.

The fast oscillator is continuously variable from 1.88 MHz to 2.44 MHz, guaranteeing a 2.9 μs to 3.7 μs elementary operation. The frequency of the fast oscillator is varied by adjusting R13, while adjusting R11 varies the duty cycle.

C. CONTROL CIRCUITRY

The control circuitry controls the mode of operation of the clock generator. External commands to run, halt, perform a single elementary operation, or to perform a single instruction all enter the clock generator through the control circuitry.

The control circuitry incorporates two logic circuits. One circuit consists of two differentially coupled nand gate latches. With the clock generator in the HALT mode, signals HALTA, RUN, B1, STOP, and MO are resting at a logical 1. The sync circuitry inhibits the two-phase shift register feedback due to signal MO being at a logical 1. By depressing the SUMC-DV console START pushbutton or test set RUN pushbutton, signal RUN is shorted to ground. This changes the state of the first latch forcing signal B1 from a logical 1 to a logical 0. Signal B5 is capacitively coupled to B1 and thus sees a negative-going spike of sufficient magnitude to change the state of the second latch. When the second latch changes state, signal MO is driven from a logical 1 to a logical 0. With signal MO at a logical 0, the sync circuitry can enable the feedback loop of the 2-phase shift register so that clock pulse generation can begin.

Included in the control circuitry is a circuit which clears the sequencer when the SUMC-DV console START pushbutton is depressed. The pulse to clear the sequencer (on signal line START) is formed during the time that the START pushbutton is between its internal contacts. With the START pushbutton in its released position, signal line RUNA is held at a logical 0. As the START pushbutton is depressed, signal RUNA is

pulled to a logical 1 by R1, thus generating a logical 1 level at signal line START to clear the sequencer. When the START pushbutton reaches the end of its travel, a logical 0 is introduced to signal line RUN which changes the state of the first control circuit latch. Signal B2 now assumes a logical 1 state which is used to drive signal line START back to a logical 0.

Clock pulse generation may be terminated in one of three ways: by activating the single instruction or single elementary operation mode from the SUMC-DV Test Set or by depressing the HALT pushbutton on either the SUMC-DV panel or Test Set. Each of the three halting mechanisms works in a similar manner. When the single elementary operation mode is entered, signal STOP in the control circuitry is switched from a logical 0 to a logical 1. Signal STOP is gated with clock signal CLHI so that the first time that signal CLHI is generated, signal MO switches from a logical 0 to a logical 1. This causes the sync circuitry to inhibit the two-phase shift register feedback and clock pulse generation is terminated. Activation of the single instruction mode also causes the state of signal STOP to switch from a logical 0 to a logical 1, however, the state of signal STOP does not change until the last elementary operation in the instruction. Gating circuitry internal to the SUMC-DV Test Set guarantees the proper generation of the STOP signal. Once signal STOP switches to a logical 1, clock generation is terminated as in the single elementary operation mode. Halting the SUMC-DV via the single instruction or single elementary operation modes relies on changing the state of the second control circuitry latch without changing the state of the first latch. In order to ready the control circuitry so that the RUN mode may be reentered it is necessary to also change the state of the first latch. This is manually accomplished by depressing either the SUMC-DV panel or Test Set HALT pushbutton after clock pulse generation has ceased. The SUMC-DV may be halted after an arbitrary elementary operation by depressing either the SUMC-DV panel or Test Set HALT pushbutton. This simultaneously changes the state of both control circuitry latches by forcing signal HALTA from a logical 1 to a logical 0. As before, signal MO is thus driven from a logical 0 to a logical 1 resulting in an interruption of the two-phase shift register feedback and therefore clock pulse generation.

D. TWO-PHASE SHIFT REGISTER

The two-phase shift register consists of two banks of static shift registers that are alternately triggered by the oscillator circuitry. Both edges of each oscillator pulse are utilized in the triggering scheme so that each of the shift register banks is triggered at a rate equal to the oscillator frequency. Trigger pulses enter the shift register banks on signal lines CL1 and CL2.

Each shift register contains its own regenerative feedback. The feedback loops in each of the two shift register banks are identical in design. The effective construction of each loop consists of a nanding of the first six output lines of each shift register with an inhibit signal (MS). The output of the effective seven-input nand is returned to the data input of the shift register.

When the clock generator is in the halt mode, inhibit signal MS is resting at a logical 0. This guarantees that the outputs of each of the nand feedback loops (data inputs to the shift registers) are held at a logical 1. Since both banks of shift registers are continually triggered, all shift register data outputs fill with logical 1's. The gating circuitry can generate no clock pulses when the two-phase shift register assumes this output state.

When the run mode is entered, inhibit signal MS assumes a logical 1 state thus driving each of the shift register data inputs to a logical 0. The next trigger pulse to each shift register bank places a data 0 in the first shift register location. Each successive trigger pulse shifts the data 0 one location. With a data in any of the first six locations of either shift register bank, the feedback associated with that bank places a logical 1 at the data input (signal F1 or F2). When the data 0 has been shifted out of the first six shift register locations, the feedback regenerates the sequence by placing a logical 0 at the shift register data input. The resultant shift register output waveforms are shown in Fig. 9-2.

Also included in the two-phase shift register is the circuitry which implements a long or short elementary operation. A long elementary operation is called for whenever there is a data dependent branch condition. When this is the case, signal line

C20 is driven to a logical 0 shortly after the leading edge of clock pulse CLB. C20 is the data input to a "D" type flip-flop. The data 0 is transferred to the output of the flip-flop (SHEO) by shift register output EE. A data 0 at signal line SHEO allows shift register outputs EK and EL to assume active roles in the shift register feedback loops.

Signal line C20 is driven to a logical 1 when a short elementary operation is to be performed. When this data 1 is transferred to signal line SHEO, shift register outputs EK and EL are overridden in the shift register feedback loops. Overriding these two signals results in a 14% reduction in the length of the elementary operation.

E. SYNC CIRCUITRY

The sync circuitry serves as an interface between the control circuit and the two-phase shift register. When the clock generator is in its run mode, input signal MO to the sync circuitry is at a logical 0 and output signal MS is at a logical 1. With signal MS at a logical 1, the two-phase shift register's feedback loops are enabled and the clock generator is free running. When the halt mode is entered via the control circuitry, signal MO switches from a logical 0 to a logical 1. This sets a "D" type flip-flop in the sync circuitry and forces signal Q to a logical 1. As soon as the feedback signals (F1 and F2) from the shift register feedback loops also simultaneously assume logical 1 levels, signal MS is driven from a logical 1 to a logical 0. This inhibits the shift register feedback and terminates the clock pulse generation at the end of that elementary operation.

Entering the run mode from the halt mode causes signal MO to switch from a logical 1 to a logical 0. The sync circuitry phase orients the trigger pulses to the two-phase shift register before enabling the shift register feedback loops. This is done by clocking the logical 0 level of signal MO to signal line Q on the leading edge of signal FREQ. When signal Q assumes a logical 0 level, signal MS switches to a logical 1, and enables the shift register feedback loops. Using signal FREQ as a reference point to enable the shift register feedback loops orients the shift register trigger pulses so that signal line CL1 sees the first rising (trigger) edge after the two-phase shift register has been enabled.

F. GATING CIRCUITRY

The clock gating circuitry generates the clock pulses used to drive the SUMC-DV. The clock pulses are generated by selectively gating the outputs from the two-phase shift register. Clock pulses are buffered, wave shaped or delayed where necessary before being distributed to the SUMC-DV.

G. CLOCK PULSE DISTRIBUTION

The SUMC-DV clock pulses are used to directly drive circuitry on six of the eleven plug-in boards. Fig. 9-5 shows the fan-out distribution for each of the clock pulses. The five boards not directly accessed by the clock pulses are the four main memory boards (MM1, MM2, MM3 and MM4) and the scratch pad memory (SPM) board.

The following listing is a functional breakdown of the clock signals on the basis of the computer operation that each clock signal initiates.

(1) CLA pulse, conditioned with a read-only memory (ROM) bit, clocks the main memory data lines into the instruction register (IR).

(2) $\overline{\text{CLA}}$ pulse clocks ROM data into the microprogrammed read-only memory (MROM) data registers.

(3) CLB pulse clocks the scratch pad (SP) address lines into the scratch pad address registers.

(4) CLBC pulse is used to strobe the input/output (I/O) lines to an external teletype connection.

(5) CLEF pulse clocks data into the sequencer to initiate a short elementary operation.

(6) CLG pulse clocks in the sign change and left shift instructions to the input/output (I/O) board. On the multiplexer register unit (MRU) board, CLG clocks data into the memory address register (MAR), product remainder register (PRR) and the multiply quotient register (MQR). On the arithmetic logic unit board (ALU1 and ALU2), CLG performs the unused function of generating a carry latch for double precision operation.

(7) CLGG pulse clocks data into the sequencer to initiate a long elementary operation.

(8) CLHI pulse is used to update the state of the interrupt register and to generate the scratch pad memory write signal. CLHI is also used to initiate the halt operation when the clock generator is in its single elementary operation mode.

(9) CLI pulse clocks in the sign bit for the multiply and square root algorithms on the arithmetic logic unit (ALU1 and ALU2) boards. On the microprogrammed read-only memory (MROM) board, CLI, conditioned with a read-only memory (ROM) bit, generates the read/write signal into the main memory. On the input/output (I/O) board, CLI is used to clock data into the interrupt status register (ISR).

	CLA	$\overline{\text{CLA}}$	CLB	CLBC	CLEF	CLG	CLGG	CLHI	CLI
MM1	-	-	-	-	-	-	-	-	-
MM2	-	-	-	-	-	-	-	-	-
MM3	-	-	-	-	-	-	-	-	-
MM4	-	-	-	-	-	-	-	-	-
MRU	-	3	-	-	-	12	-	-	-
ALU2	-	2	-	-	-	1	-	-	1
ALU1	-	3	-	-	-	1	-	-	1
SPM	-	-	-	-	-	-	-	-	-
IR	4	2	1	1	-	-	-	2	-
MROM	-	6	-	-	1	-	1	-	2
I/O	-	1	-	-	-	2	-	-	2
TOTAL FAN-OUT	4	17	1	1	1	16	1	2	6

Fig. 9-5. Clocks Fair-Out Distribution.

SECTION X

POWER SUPPLY AND DISTRIBUTION

A. GENERAL DESCRIPTION

The SUMC-DV and Test Set utilize a three-output power supply. The three nominal operating voltages required by SUMC-DV are +10 volts, +5 volts and -5 volts. The power supply provides +10 volts at 1.8 amperes, +5 volts at 15 amperes and -5 volts at 3 amperes. Manufacturer's specifications guarantee 0.1% line and load regulation, 0.1% noise and ripple control, and an operating temperature of from 0 to 55°C. The power supply operates at 120 Vac ±10% and can be made to operate at 240 Vac.

To provide the desired nominal operating voltages at the SUMC-DV plug-in boards, the outputs of the power supply were set at +5.8 volts, +10.2 volts and -5.05 volts, resulting in +5 volts, +10 volts and -5 volts, respectively, at the SUMC-DV boards.

During nominal operation, the SUMC-DV consumes 39 watts of power. Of this, the +10 volt circuits use 8 watts (0.8 ampere at 10 volts). Included in the +10-volt circuits are the 54 LSI chips. During nominal operation these 54 chips use about 1 watt. The other 7 watts are distributed among the microprogrammed read-only memory, the scratch pad memory, the sense amplifiers, the clock generator and various level shifting circuits. The +5-volt circuits consume 27.5 watts (5.5 amperes at 5 volts). The bipolar main memory dissipates 24 of the 27.5 watts. The -5-volt supply dissipates the remaining 3.5 watts used by the SUMC-DV (0.7 ampere at -5 volts). The main memory and microprogrammed read-only memory consume the majority of this power.

The power supply contains both overcurrent and overvoltage protection. The overcurrent protection is in the form of foldback current limiting. The internal adjustment is set so that the +10-volt supply current begins folding back at 2.7 amperes, the +5 volt supply current at 15 amperes and the -5 volt supply current at 2.5 amperes.

The internal overvoltage protection is in the form of an SCR crowbar across each output. The +10-volt supply SCR turns on at 11.1 volts, the +5-volt supply SCR is set to turn on at 6.35 volts, and the -5-volt supply is limited to -5.6 volts by its SCR crowbar.

B. OVERVOLTAGE AND OVERCURRENT PROTECTION

The overcurrent protection internal to the SUMC-DV takes the form of three fuses, one for each of the three supply voltages. The +10-volt and the -5-volt supplies each have 2-A fuses, and the +5-volt supply has an 8-A fuse. These fuses are located on the nonpluggable board behind the front panel of the SUMC-DV. The overvoltage protection internal to the SUMC-DV takes the form of three 50-watt zeners which are located just beside the backplane wiring for the four main memory boards.

These three zener diodes each have a nominal voltage which is 20% higher than the nominal operating voltage for the supply being protected. During normal operation, these three zeners remain out of conduction and do not add to the SUMC-DV power dissipation. However, if an overvoltage of 20% occurs, on any supply, the corresponding zener will conduct and prevent any further overvoltage. With the power rating that these zeners have, they are designed to blow the fuse for the supply they are protecting before damage to the zener can occur.

Another protective diode has been placed between the +10-volt and the +5-volt supplies to prevent the +10-volt supply from dropping below the +5-volt supply, since this could result in damage to the CD4009 and CD4010 CMOS to T^2L level shifters in the SUMC-DV. This makes the SUMC-DV insensitive to power supply sequencing.

All three supplies come in through the external connector, through the multipole power switch and the three fuses, and then to three terminal posts on the backplane chassis, from which they are distributed to the various boards. Each board is decoupled by one or more electrolytic capacitors and by one or more ceramic capacitors for each supply.

SECTION XI

PACKAGING

A. MECHANICAL DESIGN OF THE SUMC-DV AND TEST SET

1. Design Approach

The basic approach to the mechanical configuration of the SUMC-DV and Test Set was one of providing a flexible system that could accommodate a variety of package types, provide custom printed cards, and permit a short design and fabrication cycle. Consistent with this approach, all active devices were considered to be pluggable elements requiring highly reliable sockets with a wirable termination. In addition the wiring arrangement had to satisfy not only the flexibility requirements, but was constrained to avoid excessive interconnectivity capacitance.

In order to assure adequate facility for test and checkout, a large number of test points were incorporated into the system. The test point connections were established to facilitate attachment and removal, ease of maintenance and assembly. Because of the low dissipation of the system, natural air convection is used consistent with operation in the normal ambient temperatures of the laboratory environment.

Virtually all of the CPU active components are in dual-in-line packages with 40, 24, 16 or 14 leads. Evaluation of various memory approaches resulted in the use of a purchased T^2L arrangement on four plug-in printed wiring boards. Each of the memory boards has planar dimensions of 7.0 in by 5.5 in and terminates in a 60-pin board edge connector. The final component parts configuration complement for the CPU and its memories is given by function in Table 11-1. For this CPU alone, the total part count is 178. Table 11-2 summarizes the components used in the Test Set.

TABLE 11-1. SUMC-DV COMPONENT COMPLEMENT

Function		DIPs (No. of Leads)				Resistors	Capacitors	Transistors	Diodes	Fuses
		40	24	16	14					
CPU	MRU	12	3	5			4			
	ALU2	7	2		7*		6			
	ALU1	11	3				4			
	IR	5	4	10	11*	16	14		2	
	MROM	3	13	2	1		8			
	I/O	2	1		15*		6			
Scratchpad Memory				4	50	54	6		1	
Lamp Driver Board					4	13		5	2	3
Chassis									3	
TOTAL		40	26	21	88	83	48	5	8	3

*Includes Terminating Resistor Networks

Function	Rotary Switches 16 PDT	Toggle Switches		Momentary Switches	Lamps
		SPDT	4PDT		
Control Panel	2	17	1	6	6

TABLE 11-2. TEST SET COMPONENT COMPLEMENT

Function	DIP, 14-LEAD	Resistors	Capacitors	Transistors	Diodes
Lamp Driver Board	2	52	1	12	26

Function	Rotary Switches 16P10T	Toggle Switches		Momentary Switches	Lamps
		SPDT	On-Off-On		
Test Panel	1	2	35	4	26

In order to facilitate the checkout and the debugging of the computer, a large number of test points were utilized. In establishing these test points, various constraints were evaluated. These constraints include the minimization of external capacitance and convenient accessibility.

2. Design Implementation

The SUMC-DV computer is packaged in an overall configuration as shown in Fig. 11-1 with basic dimensions of 12.0 inches wide, 10.5 inches high and 9.0 inches deep. The assembly comprises an outer fabricated welded and riveted aluminum alloy housing assembly; a fabricated control panel; a fabricated, formed and welded backplane connector mounting plate; two fabricated card guide support brackets; 26 card guides; 4 plug-in main memory board assemblies; 7 plug-in CPU board assemblies; 1 wired-in lamp driver board assembly; 2 external connectors; 4 nylon mounting feet; and an assemblage of connectors, lamps, sockets, switches, wiring and mechanical fasteners.

The outer housing is fabricated from 0.090-inch-thick aluminum alloy to provide the basic frame for support of the entire computer. Hinged doors are riveted at openings in the front and back surfaces of the housing with the opening ends secured or opened by two quarter-turn knurled-head stud fasteners engaging "S" springs on each door stop. The top surface of the housing has a 1-1/2-inch slope down from the back to the front and is open in picture frame fashion. Two connector openings are provided in the left wall on the lower half close to the back edge. Seven

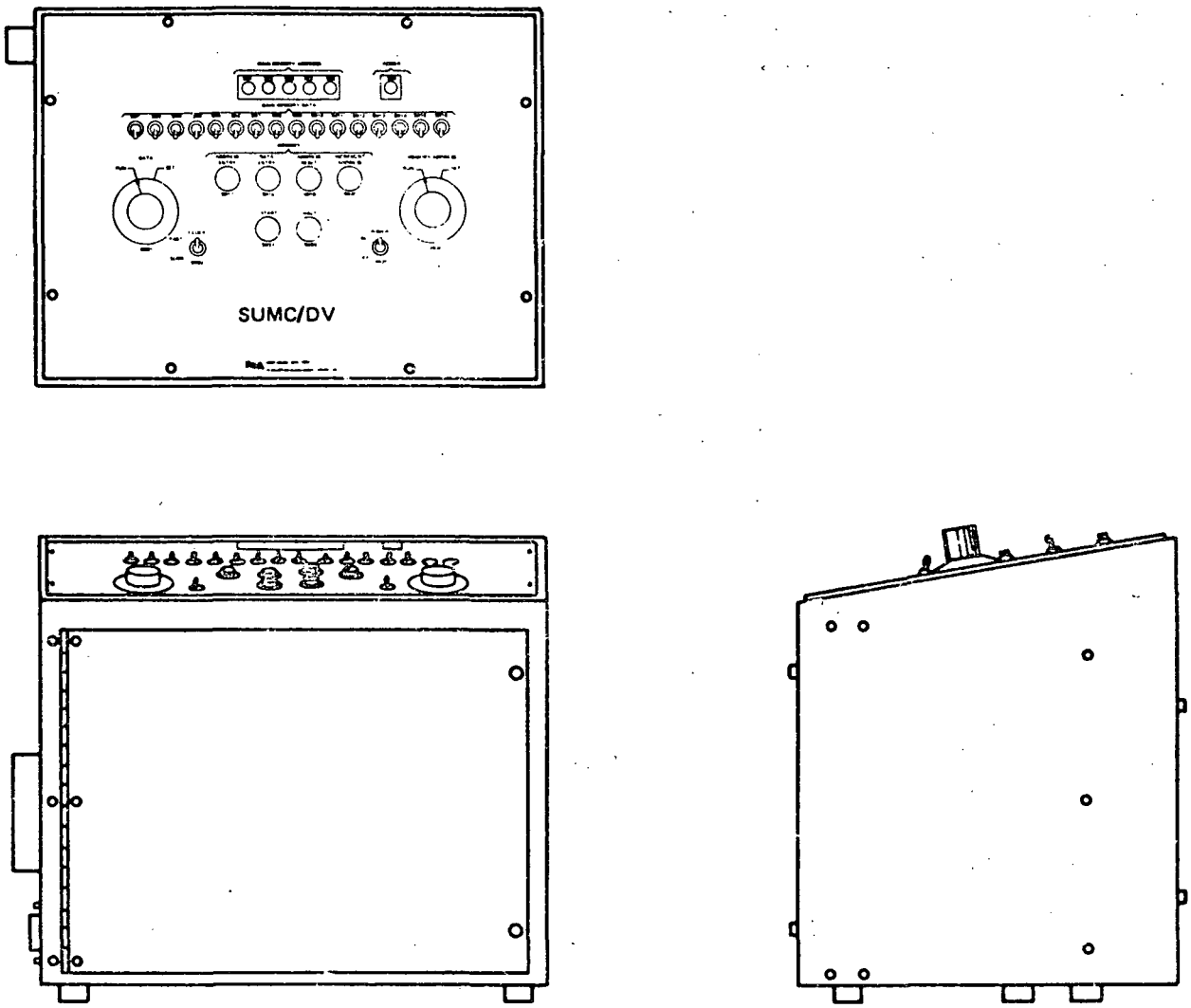

Fig. 11-1. SUMC-DV chassis assembly.

countersunk screw holes are provided in both the left and right side walls for mounting the backplane connector plate and the two board guide mounting brackets. The top "picture frame" surface has eight captivated clinch nuts for mounting and fastening the control panel.

The housing is finished all over with a chemical treatment which leaves a light yellow chromate film on the surface. The outside surfaces of the housing are painted with a shadow blue vinyl coating.

The control panel is a flat 0.090-inch-thick aluminum alloy plate with switch, lamp socket and countersunk screw mounting holes located in appropriate locations. Figure 11-2 shows the component parts arrangement on the control panel. The rear of the control panel has six clinch studs extending from it to provide mountings for the lamp driver board standoffs. The lamp driver board assembly shown in Fig. 11-3 is screw-mounted to the six 1-inch-long internally threaded standoffs which extend from the clinch studs on the back of the control panel. The toggle and rotary switches are retained in the panel with front applied nuts on the threaded shaft bushings. The pushbutton switches are retained in a similar fashion with the mounting nuts applied from the rear. The main memory address lamps are in a multiple socket which is retained in its slot by two press-on "Tinnerman" nuts. The single socket for the power lamp is also retained by a "Tinnerman" nut.

The control panel is finished all over with a chromate film and painted with midnight blue enamel on the top and edge surfaces. Control panel marking is screened on using white epoxy paint. It mounts on the top of the housing with eight flat-head screws.

The backplane connector panel is fabricated from 0.090 inch-thick aluminum alloy material. The back surface is stepped and cut out to provide the mounting locations for up to 13 plug-in board connectors. The step in the back surface compensates for the length-variation between the memory and CPU boards. The upper and lower

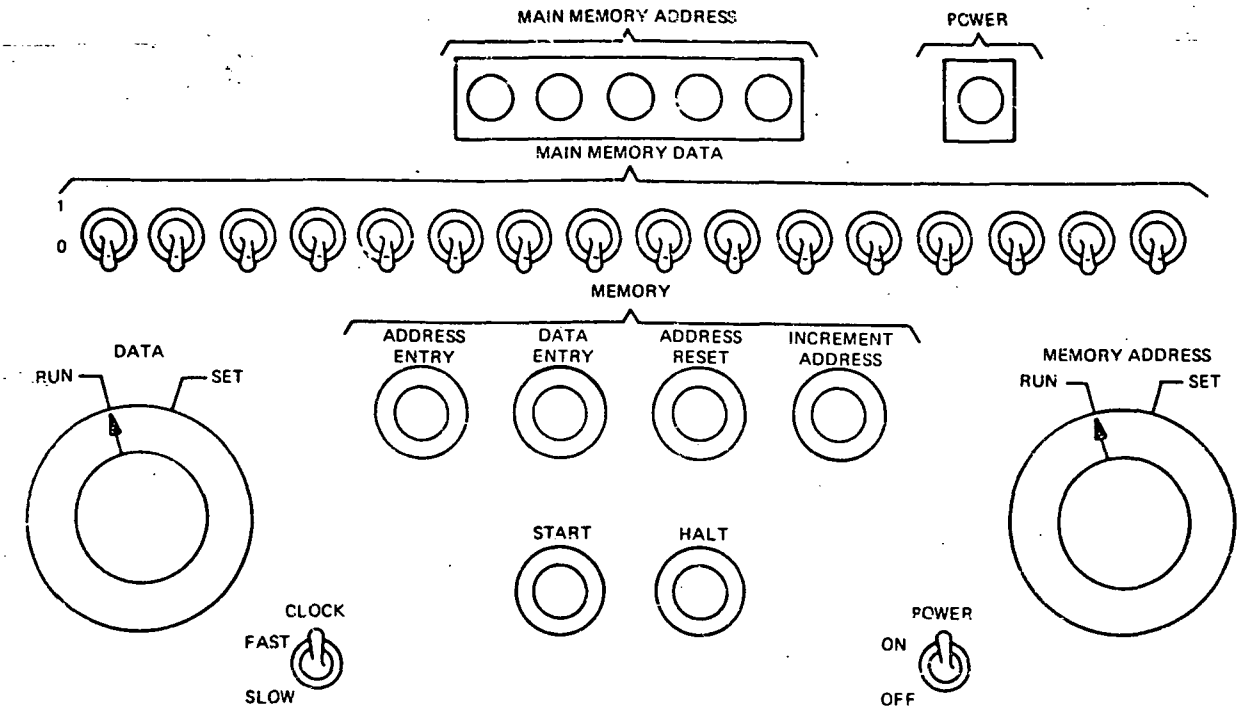

Fig. 11-2. SUMC-DV control panel.

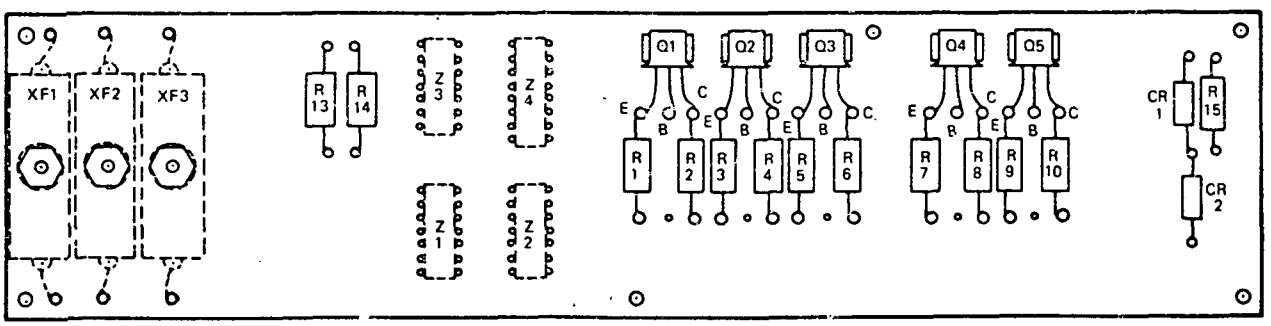

Fig. 11-3. SUMC-DV lamp driver board assembly.

folds of the plate provide stiffening and support attachment surfaces for the back end of the board guides. Clinch nuts are provided on these surfaces to mate with the board guide mounting screws. The side ends of the connector plate are folded forward 0.75 inch and provided with three clinch nuts on each side to mount the connector plate in the housing. Additional holes are included near the top and bottom of the back surface for standoff terminals holding voltage bus wires. Holes are also provided in the lower left corner of the back plate, below the memory card connector cutouts, for mounting the voltage crowbar zener diodes. Two holes with clinch nuts are also on the bottom fold of the back plate to which the mounting feet attach.

The plane for the back wiring is formed by the wire wrap pins extending from the back of the plug-in board connectors when they are mounted in the plate.

The two card guide support brackets are formed from 0.090-inch-thick aluminum alloy and finished with a chromate film coating. The front and back edges are formed into 0.38-inch-long bends for cross stiffening. The sides are formed in a similar bend with two holes and clinch nuts to fasten the brackets to the housing. One bracket mounts in the top front of the housing and the other in the lower front of the housing. Properly located holes with clinch nuts are in the flat surfaces of the brackets, to which screws for the front end of the board guides attach. The lower bracket is also provided with two holes and clinch nuts near each end for attachment of the mounting feet.

The board guides are vendor purchased plastic parts which are modified by the addition of countersunk front and back mounting holes. Two different sizes are used. One size has a slot width and length to accommodate the 0.063-inch-thick memory boards. The other accommodates the 0.125-inch-thick longer CPU boards. The guides are mounted with flat-head machine screws in the top and bottom of the housing between their front mounting brackets and the back plane connector plate. Four shims are used between the guides for the main memory cards and their mounting surfaces to adjust the height of the opening to the main memory card width.

The four main memory boards plug into the first four positions on the left while the seven CPU boards plug into the next seven locations in the following order: MRU, ALU2, ALU1, SPM, IR, MROM, and I/O. Two vacant slots exist, one of which is reserved for a planned memory expansion of 2,048 words of a CMOS beam lead memory.

The CPU plug-in board configuration is a specially designed variation of a vendor available board. It consists of a 0.125-inch-thick fiberglass epoxy material with planar dimensions of 7.353 inches by 7.000 inches. One end of the board has 122 (61 on each side) gold plated board edge connector tabs. The connector tabs have printed wiring paths extending back to wire-wrap-type terminals pressed and soldered in the board on a 0.200 inch by 0.200 inch grid. The end two tabs on each side and both surfaces are attached to voltage and ground printed wiring strips running along the edges of the board. Six wire wrap terminals are provided at equally spaced positions along each strip for wiring access. The board has 22 rows of 50 holes running along its length spaced 0.300 inch apart. Holes in each row are spaced 0.100 inch apart and are sized to accept wire-wrap-type socket terminals. The end of the board opposite to the connector has two ejector keys to aid in board removal from its connector.

Each individual board in the CPU was adapted to its use by appropriate population of the socket/terminals to match the component arrangements.

Board wiring was implemented using random point-to-point runs with wrap and solder terminations on the socket terminals in order to minimize length of parallel runs, total wire length and total interconnection capacitance.

Back plane wiring was implemented in a similar manner between terminals on the plug-in card connectors. The +10-volt supply and ground were distributed to the CPU connectors with bus wires running across the top and bottom of the back-plane connector plate.

The entire functional SUMC-DV computer can be subassembled outside of the outer housing after which it can be placed and fastened to the housing. This greatly simplifies initial wiring and assembly access.

B. TEST SET

The Test Set is packaged in a vendor purchased and RCA modified chassis as shown in Fig. 11-4. It has basic dimensions of 8.0 inches by 12.0 inches by 4.0 inches. Five basic parts and subassemblies are used to build up the Test Set; they are the chassis, a test set panel, a lamp driver/terminal board assembly, a subchassis, and four mounting feet.

Figure 11-5 is a sketch of the component arrangement on the Test Set panel. The lamp driver/terminal board assembly is shown in Fig. 11-6. The 14 sets of test leads are in the form of 16 conductor flat ribbon wires.

C. EVALUATION OF THE DESIGN IMPLEMENTATION

The SUMC-DV structure has proven to be adequately rigid to withstand all of the operational and handling forces. Cooling of the components used in the assembly by naturally convected air in a laboratory environment is sufficient to keep the maximum temperatures within specified operating limits. The design approach was flexible enough to easily absorb the evolution of the electrical design. Interwiring capacitance is sufficiently low to permit the system to meet its operational requirements. The assembly techniques used provided the expected degree of ease for both assembly and maintenance. Future expansion capabilities are available from two unused plug-in card positions in the CPU end of the SUMC-DV.

The Test Set connection, switching and indicating systems have proven valid in their use to completely check out, fault locate and debug the SUMC-DV.

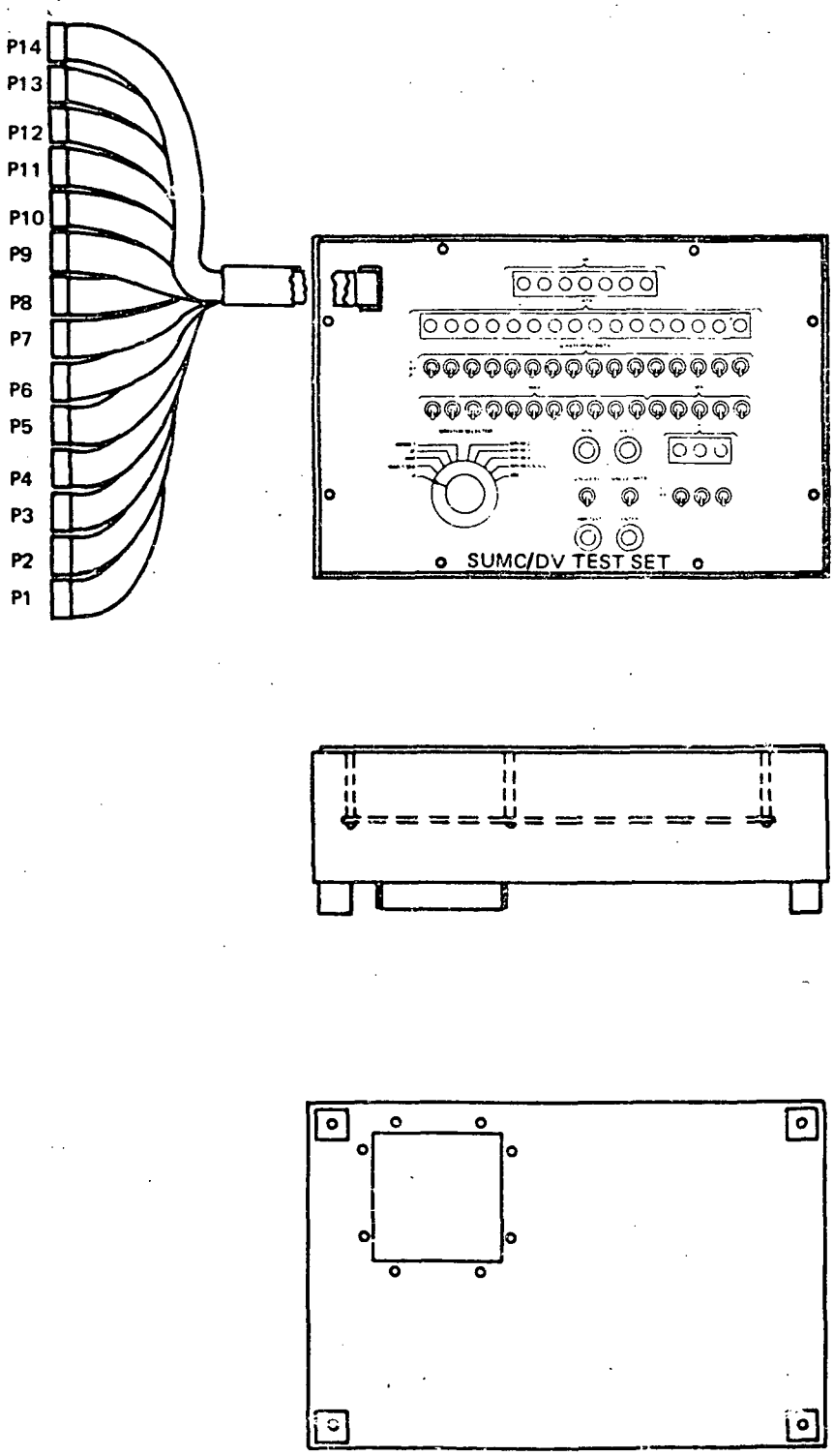

Fig. 11-4. Test set assembly.

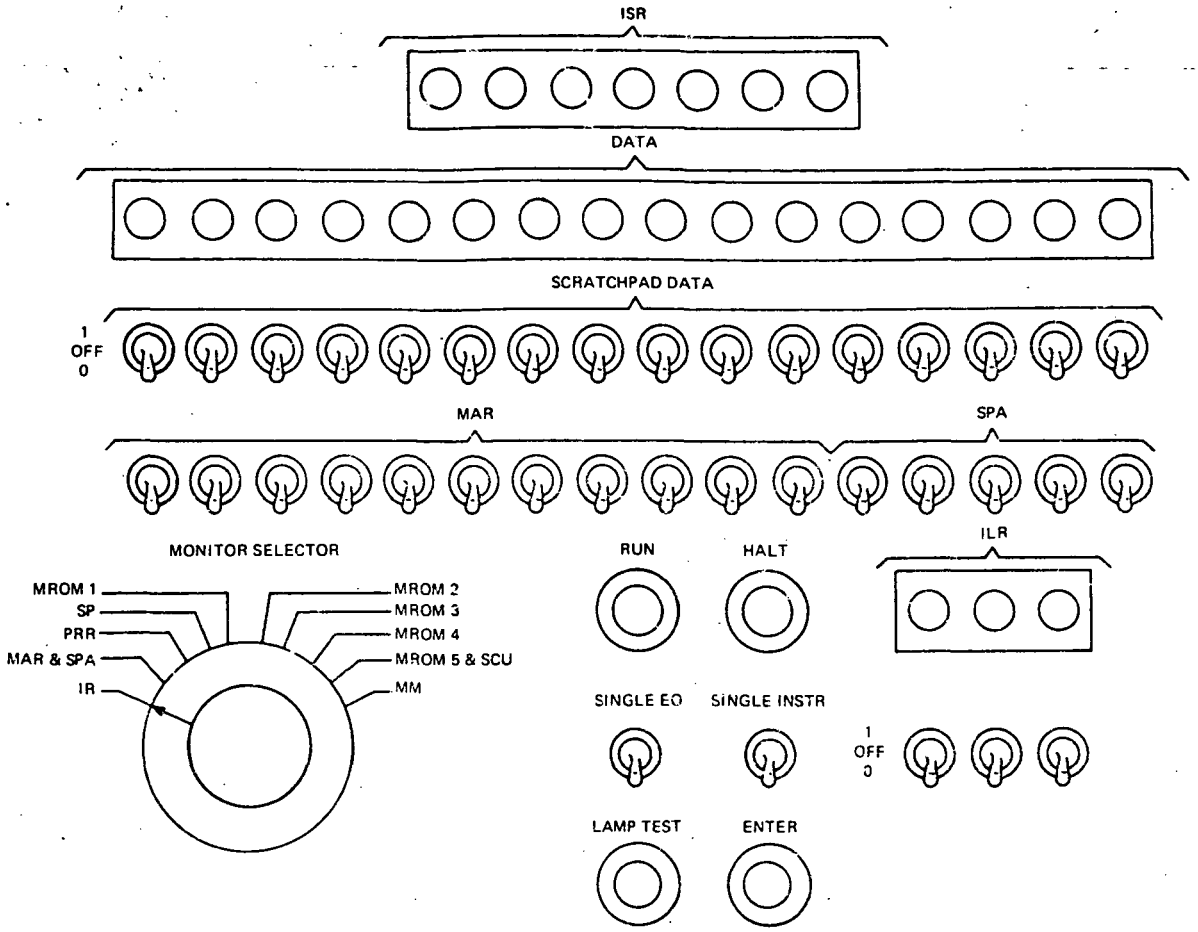

Fig. 11-5. Test set panel.

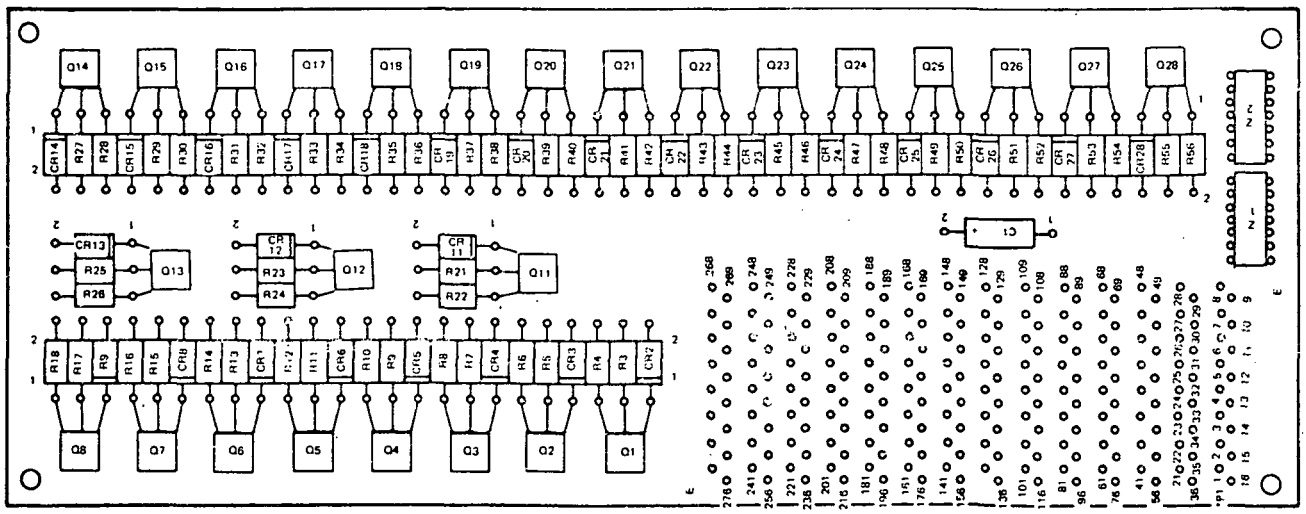

Fig. 11-6. Test set lamp driver/terminal board assembly.