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RELIABILITY LABORATORY, INC.

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FINAL REPORT

NASA CONTRACT #NAS 8-25897

EXTENDED LIFE TESTING EVALUATION OF COMPLEMENTARY MOS INTEGRATED CIRCUITS

MARCH 1971 thru MAY 1972

Prepared for:

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DCA FINAL REPORT #203

JULY 7, 1972

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1.0 PURPOSE OF EVALUATION

The purpose of this extended life testing evaluation of complementary MOS integrated circuits is twofold:

1. To ascertain the long life capability of complementary MOS devices.
2. To assess the objectivity and reliability of various accelerated life test methods as an indication or prediction tool.

The above goals are to be realized by utilizing those methods of life testing as described in MIL-STD-883, Method 1005 (Steady State Life), supplemented by Method 1008 (High Temperature Storage).

In addition, the determination of a suitable life test sequence for these devices is of importance.

2.0 DESCRIPTION OF TEST SPECIMENS

2.1 PART TYPES

CD4002 Dual 4-input Gate, CMOS Integrated Circuit

CD4003 Dual D-type flip-flop, CMOS Integrated Circuit

2.2 CONSTRUCTION

Structure: Single monolithic chip with "N" and "P" channel diffusions on the same chip.

Intended Use: Digital equipment in which the clock or operating rate is less than ten megahertz and low power dissipation of the devices is required.

2.3 CASE STYLE

Hermetically sealed 14 lead "flat pack" with ceramic and metal package.

2.4 MANUFACTURER

Radio Corporation of America, Somerville, New Jersey

3.0 HISTORY OF TEST SPECIMENS

Most of the integrated circuits (160) used in this evaluation program were devices from the NASA/Ames Research Center (ARC) qualification program conducted under contract #NAS 2-5760. These units and the balance of the test sample were furnished by Marshall Space Flight Center to DCA RELIABILITY LABORATORY, INC. The evaluation consisted of 184 units, of which 160 units were processed per the Flow Chart (Figure 1) shown on Page 7. This flow chart shows the testing done on ARC contract #NAS 2-5760.

Additional units were provided by Marshall Space Flight Center to DCA Reliability Laboratory, Inc. to make a total of 184 units. DCA Reliability Laboratory, Inc. is not aware of any history for these additional units, although there were some indication that these units had undergone some degree of prior testing because they had been serialized.

The breakdown of the results of the tested units is shown in the Historical Chart (Table 1) on Page 6.

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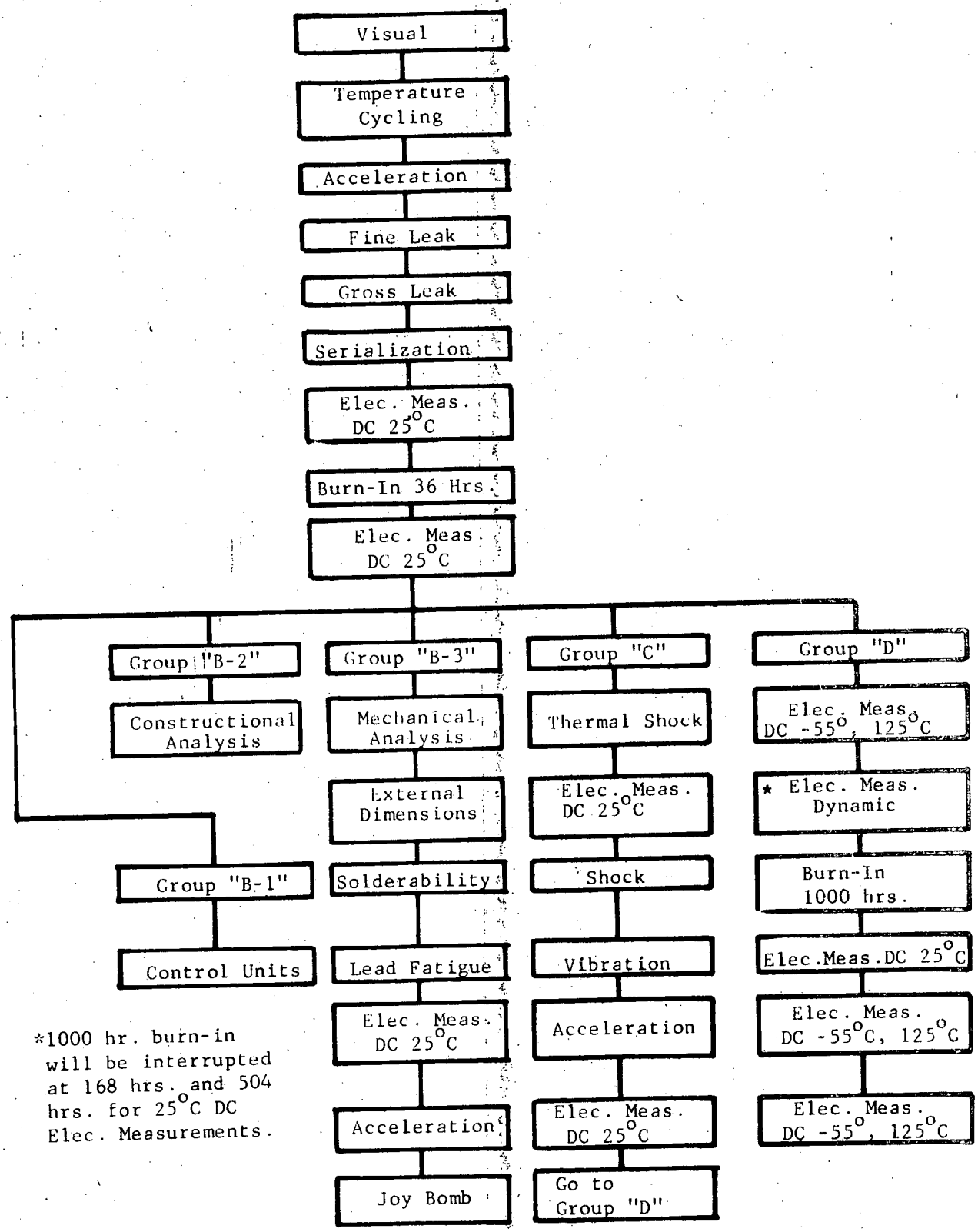
TABLE I

HISTORICAL CHART

Quantity		Historical Results
CD4002	CD4003	
13	1	Exceeded manufacturer's specified parameter limits after the 36 hour burn-in and received no further testing on the ARC contract.
8	15	Exceeded DCA/ARC parameter drift criteria during the 36 hour burn-in and received no further testing on the ARC contract.
12	29	Exceeded DCA/ARC parameter drift criteria during the 1000 hour burn-in on the ARC contract.
32	42	Parameters remained stable within the manufacturer's specifications throughout the ARC Qualification.
0	1	This unit remained stable within the manufacturer's specification during the 36 hour burn-in and was not subjected to further testing on the ARC contract.
8	0	Exceeded manufacturer's specified parameter limits during the 1000 hour burn-in on the ARC contract.
23	0	These units did not receive testing on the ARC contract. These units were received with serial numbers attached which indicates that some processing was performed prior to receipt at DCA. The prior history is unknown.



ARC TEST MATRIX

FIGURE 1

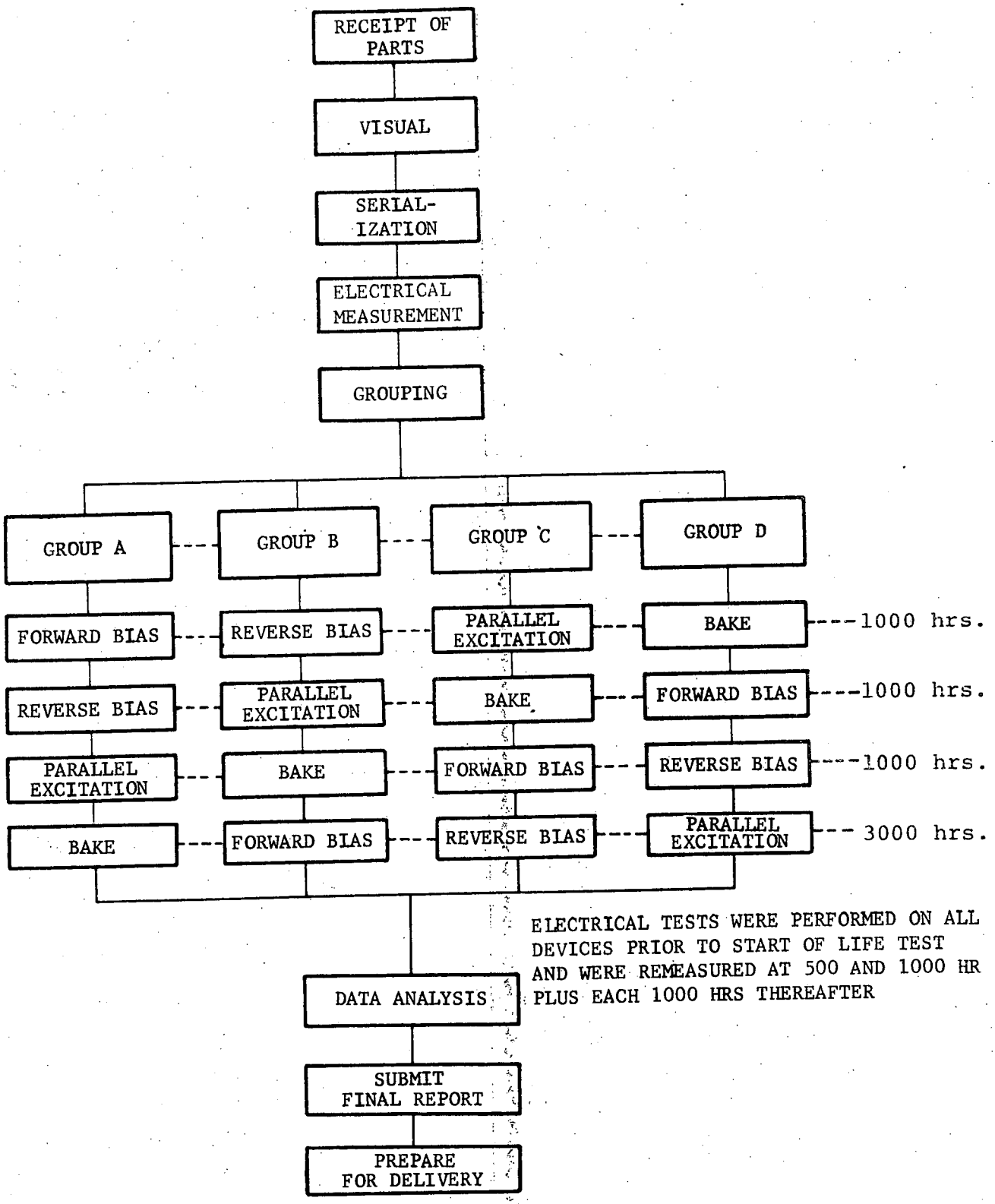
4.0 INDIVIDUAL TEST DESCRIPTIONS, SEQUENCE AND RESULTS

For the ARC contract various life test sequences were developed and designed to expose the dominant failure modes prevalent in CMOS integrated circuits. Based on this previous study, a life test matrix was developed for the MSFC contract which would provide information pertaining to the various confidence levels weighed against the applicable life test sequences involved. This matrix is shown on Page 9, Figure 2.

These stresses were designed to detect junction bulk and junction surface defects, which could then be analyzed for the most effective reliability screening techniques to be used for the devices.

4.1 ELECTRICAL MEASUREMENTS

The electrical test consisted of the DC parameters measured on the Fairchild 4000 at 25°C. The forcing function, parametric limits and drift criteria are delineated in Appendix C. The measurements were taken at 0 hours, 500 hours, 1000 hours and each 1000 hours thereafter for a total of 6000 hours. A-1 parametric readings were evaluated relative to the manufacturer's limits and DCA drift criteria. The drift was calculated back to the initial measurement point.



MSFC TEST MATRIX

FIGURE 2

4.2 LIFE TEST DESCRIPTIONS

The life test matrix as outlined on Page 9, Figure 2 was developed by MSFC and DCA. The life test was performed on an accelerated basis and distributed into four individual tests. Each test was designed to activate failure mechanisms which might be encountered under normal life operation. These failure mechanisms were detected by electrical degradation which may be caused by chemically active surfaces, ionic contamination, hot spots, channeling or other thermal chemical processes. Each stress is described below.

4.2.1 PARALLEL EXCITATION TEST @ 125°C (PE)

This test consists of switching the complementary pair of transistors in the device on and off simultaneously. This was done by forcing the output alternately high and low by means of a pulse at one of the inputs. When this applied voltage and/or current pulse goes high the input P-channel MOS transistor is turned off while the complementary N-channel is turned on; and the reverse is also true. This life test conforms to MIL-STD-883, Method 1015, Condition D.

4.2.2 REVERSE BIAS @ 125°C (RB)

This test configuration ties the inputs of the device to V_{DD}. In this manner the P-channel transistors are turned off while the N-channel transistors are on. Therefore, the P-channel transistors are exposed to a high temperature reverse bias, while the N-channel transistors are not being stressed. This condition conforms to MIL-STD-883, Method 1015, Condition A.

4.2.3 FORWARD BIAS @ 125°C (FB)

This configuration ties the gates of the input transistors to ground, thereby turning the P-channel transistors on and the N-channel transistors off. This creates a high temperature reverse bias on the N-channel transistors, while the P-channel transistors are not stressed. This life test configuration conforms to MIL-STD-883, Method 1015, Condition B.

4.2.4 HIGH TEMPERATURE STORAGE @ 150°C (BAKE)

This consisted of placing the units in an ambient temperature of 150°C for the specified duration. This test is sometimes referred to as "stabilization bake". This condition conforms to MIL-STD-883, Method 1008, Condition C.

4.3 RESULTS

For the determination of effectiveness on the various types of life test all measurements thru the 500 hours time point which includes the ARC evaluation were used as a reference point.

The results are based on three variables; (1) those units which exceeded manufacturer's limits during the initial 500 hours of test; (2) those units which exceeded the DCA drift criteria during the initial 500 hours of test; (3) those units which exceeded the manufacturer's limits after the initial 500 hours of test.

4.3.1 The following represents the percent failures during the initial 500 hours of life test utilizing the manufacturer's limits as the reject criteria.
i.e., The FB for the CD4002 states 17.4%. This means 17.4% of the units exceeded manufacturer's limits during the initial 500 hours of test.

	FB	RB	PE	BAKE
CD4002	17.4%	33.3%	6.6%	0%
CD4003	0%	2.7%	0%	0%

4.3.2 The following percent failures is the same as paragraph 4.3.1 with the addition of the DCA drift limit included as the reject criteria.
i.e., The FB for the CD4002 states 34.7%. This means 34.7% of the units exceeded the manufacturer's limits and the DCA drift criteria during the initial 500 hours of burn-in.

	FB	RB	PE	BAKE
CD4002	34.7%	61.5%	20.0%	15.7%
CD4003	14.2%	86.4%	30.0%	25.0%

4.3.3 The following percentages indicate the predictability effectiveness of infant mortality utilizing the DCA drift criteria. The units which indicated instability during the initial 500 hours were categorized as potential failures. At the conclusion of the test these parts were analyzed for limit failure.
i.e., The FB for CD4002 states 100%. This means all parts which were categorized as potential failures during the initial 500 hours of test eventually exceeded the manufacturer's limits.

	FB	RB	PE	BAKE
CD4002	100%	63.6%	50.0%	33.3%
CD4003	0%	6.4%	0%	60.0%

4.3.4 The following percentages indicate the undetected post 500 hour failures. These failures escaped detection in that they were stable during the initial 500 hours of test, i.e., The FB for the CD4002 states 6.6%. This means 6.6% of the units which indicated stability during the initial 500 hours of test eventually failed.

	FB	RB	PE	BAKE
CD4002	6.6%	0%	16.6%	10.5%
CD4003	5.5%	0%	0%	20.0%

4.3.5 There were 35% of the CD4002 and 28% of the CD4003 which passed all tests. There were 10 units which failed catastrophically during the test program of which two parts failed due to handling, five parts failed at random and three parts failed as predicted using drift criteria during the first 500 hours.

4.3.6 The recorded data for rejects is given in Appendix F and G. This data gives the critical failed parameter.

4.3.7 The data for the acceptable devices is given in Appendix D and E. This data is in graphical form giving the maximum, mean and minimum value for each parameter in percentile form.

5.0 CONCLUSION

The conclusions of the NASA/Ames Research Center (ARC) Qualification under contract NAS 2-5760 were that the Complementary Metal Oxide Silicon (CMOS) Micro-circuits as manufactured by RCA were not acceptable for high reliability application without indepth process controls and post seal reliability screening.

The ARC conclusions were based on a qualification study which consisted of a 1000 hour life test. It was felt that a life test of 1000 hours was not sufficient to evaluate the long term life capability of these devices. To substantiate the above premise, contract NAS 8-25897 by NASA/Marshall Space Flight Center (MSFC) to perform a matrix of life tests extending to 6000 hours. The results of this long term test indicated that various life test techniques in conjunction with tight parameter drift control was necessary to predict and remove from the lot population, the devices which were most likely to fail in system equipment.

A series of burn-in configurations is necessary to stress the devices to display for recognition the various failure mechanisms.

These stresses include:

A. High Temperature Storage: This screen should be performed as part of the environmental sequence and should not be used as a tool for parameter drift control.

5.0 CONCLUSION (continued)

B. "N"-Channel High Temperature Reverse Bias:
During this burn-in the maximum number of "N"-Channel transistors are stressed in a high temperature reverse bias mode of operation.

C. "P"-Channel High Temperature Reverse Bias:
During this burn-in the maximum number of "P"-Channel transistors are stressed in a high temperature reverse bias mode of operation.

D. Power Burn-In (PE): This screen stresses the input and output transistors by applying an A-C signal to the inputs.

The order in the series of applied stress is of significance since PE and temperature storage could mask the failure mechanisms revealed in the other stresses.

5.1 RECOMMENDATIONS

The following recommendations are based on the conclusions of the MSFC and ARC contracts.

5.1.1 QUALITY CONTROL

In process quality control should monitor the critical processing steps. Scanning Electron Microscope (SEM) analysis and tight precap visual inspection should be imposed to insure the manufacturing integrity of the devices.

5.1.2 RELIABILITY SCREENING

A. Environmental stresses should be performed per MIL-STD-883, Method 5004. This will insure the mechanical integrity of the package. Any unit which fails these environments should be removed from the lot.

B. Burn-in should be performed in a serial manner. The sequence should be:

1. Read and Record Critical Electrical Parameters
2. Stress Maximum Amount of "N" Channel Transistors
3. Read and Record Critical Electrical Parameters
4. Stress Maximum Amount of "P" Channel Transistors
5. Read and Record Critical Electrical Parameters
6. Power Burn-In (PE)
7. Read and Record Critical Electrical Parameters

5.1.2 RELIABILITY SCREENING (continued)

C. Parameter Drift Screen: Prior to and after each burn-in described in "B" above, the leakage and output currents should be serially recorded by unit serial number. The allowable drift for the critical electrical parameters of "output" current and "input" current should be ± 10% of the device limit.

5.1.3 RADIOGRAPHIC INSPECTION

After the reliability screening, radiographic inspection should be performed. The radiographic inspection will give a permanent record of the parts prior to use.

5.1.4 LOT ACCEPTANCE

A representative sample should periodically undergo lot acceptance testing to assure consistant manufacturing.

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APPENDIX A

DEVICE BEHAVIOUR FOR THE CD4002

Reference
Figure 2, Page 9

TABLE I	-	Group A	- Cross Reference Index to ARC Contract and Device Behaviour
TABLE II	-	Group B	- Cross Reference Index to ARC Contract and Device Behaviour
TABLE III	-	Group C	- Cross Reference Index to ARC Contract and Device Behaviour
TABLE IV	-	Group D	- Cross Reference Index to ARC Contract and Device Behaviour

KEY TO TABLES I, II, III and IV

A = Acceptable Units: These units conformed to the parametric and drift limits.

L = Limit Rejects: These units were functional units but did not meet the manufacturer-s limits.

D = Drift Rejects: These units were rejected due to DCA drift criteria but were otherwise within manufacturer's specifications.

X = Catastrophic unit and removed from test.

NEW S/N	ARC S/N	HISTORY				MSFC BI							
		RB	AMES QUAL				FB		RB	PE	BAKE		
		36	168	500	1000	0	500	1000	2000	3000	4000	5000	6000
N13303		UNITS WITH NO KNOWN HISTORY				A	A	A	A	A	A	A	A
N13304						A	A	A	A	A	A	A	A
N13305						A	A	D	D	D	D	D	D
N13306										D	D	D	D
N13307								D		D			
N13308						A	A	A	A	A	A	A	A
N13309	602	A	A	A	A	A	A	A	A	A	A	A	A
N13310	603	A	A	A	A	A	A	A	A	A	D	D	D
N13311	608	A	A	A	A	A	A	A	A	A	D	A	A
N13312	609	A	A	A	A	A	A	A	A	D	D	D	D
N13313	610	A	A	A	A	A	A	A	A	A	A	A	A
N13314	614	A	A	A	A	A	A	A	A	A	A	A	A
N13315	617	A	A	A	A	A	A	A	A	A	A	A	X
N13316	618	A	A	A	A	A	A	A	A	A	D	D	D
N13317	601	A					A	D			A	A	A
N13318	606	A	D	D	D	D	D	D	D	D	D	D	D
N13319	607	A	D	D	D			D	D	D	D	D	D
N13320	611	A	A	A	D	D	A	A	A		A	A	A
N13321	615	A	D	D	D	A	A	A	A	D	A	A	A
N13322	604	A	-	-	-	A	A		A		A	A	A
N13323	613		-	-	-	D	D	D	D		A	D	A
N13324	624	A	-	-	-	A	D	D			D	A	A
N13325	625		-	-	-						A	D	D
N13326	639	D	-	-	-	D	D	D	D		A	A	A
N13327	640	D	-	-	-	D	D	D			D	D	D
ACCEPTABLE		15	9	9	8	15	16	13	14	10	14	14	14
LIMIT REJECTS		2	1	1	1	5	4	3	6	8	1	1	1
DRIFT REJECTS		2	3	3	4	5	5	9	5	7	10	10	9
TOTAL		19	13	13	13	25	25	25	25	25	25	25	24

CD4002 Group A Device Behaviour
Table I - Appendix A

NEW S/N	ARC S/N	HISTORY				MSFC BI							
		RB	AMES QUAL				RB		PE	BAKE	FB		
		36	168	500	1000	0	500	1000	2000	3000	4000	5000	6000
N13328		UNITS WITH NO KNOWN HISTORY				A	A	D	D	D	D	D	D
N13329						A	A	A	A	A	A	A	A
N13330						A	A	A	A	A	A	A	A
N13331						A	A	A	A	A	A	A	A
N13332						A	A	A	A	A	A	A	A
N13333						A	A	A	A	A	A	A	A
N13334	619	A	A	A	A	D	A	A	A	A	D	A	A
N13335	628	A	A	A	A	A	A	A	A	A	A	A	A
N13336	642	A	A	A	A	A	A	A	A	A	A	A	A
N13337	643	A	A	A	A	A	A	A	A	A	A	A	A
N13338	645	A	A	A	A	A	A	A	D	A	D	A	A
N13339	648	A	A	A	A	A	A	A	A	A	A	A	A
N13340	651	A	A	A	A	A	A	A	A	D	D	D	D
N13341	654	A	A	A	A	A	A	A	A	A	A	A	A
N13342	620	L	L	L	L	L	D	L	L	A	L	A	L
N13343	622	A	A	D	D	A	A	A	D	A	A	A	A
N13344	631	A	A	A	A	D	D	A	A	A	A	A	A
N13345	633	A	D	D	A	L	A	A	A	A	A	A	A
N13346	646	A	A	D	L	D	A	D	L	D	L	A	D
N13347	681	D	–	–	–	D	A	A	A	A	A	A	A
N13348	635	L	–	–	–	L	X						
N13349	641	L	–	–	–	D	L	L	L	L	L	D	L
N13350	644	L	–	–	–	L	L	L	L	A	L	L	L
N13351	649	L	–	–	–	D	D	L	L	A	D	A	A
N13352	652	D	–	–	–	A	A	A	A	A	D	A	A
ACCEPTABLE		12	11	9	10	15	19	18	16	20	14	20	18
LIMIT REJECTS		5	1	1	2	4	2	4	5	1	4	1	3
DRIFT REJECTS		2	1	3	1	6	3	2	3	3	6	3	3
TOTAL		19	13	13	13	25	24	24	24	24	24	24	24

CD4002 Group B Device Behaviour
Table II - Appendix A

NEW S/N	ARC S/N	HISTORY				MSFC BI							
		RB	AMES QUAL				PE		BAKE	FB	RB		
		36	169	500	1000	0	500	1000	2000	3000	4000	5000	6000
N13353		UNITS WITH NO KNOWN HISTORY				A	A	A	A	A	A	A	A
N13354						A	A	A	A	A	A	A	A
N13355						A	A	A	A	A	A	A	A
N13356						A	A	A	A	A	A	A	A
N13357						A	A	A	A	A	A	A	A
N13358						A	A	L	L	L	L	L	L
N13359	661	A	A	A	A	A	A	A	A	A	D	D	D
N13360	664	A	A	A	A	A	A	A	A	A	D	D	D
N13361	667	A	A	A	A	A	A	A	A	A	D	D	D
N13362	670	A	A	A	A	A	D	D	D	L	D	D	D
N13363	671	A	A	A	A	X							
N13364	672	A	A	A	A								
N13365	674	A	A	A	A	A	A	A	A	A	A	A	A
N13366	675	A	A	A	A	A	L	A	A	A	A	A	A
N13367	677	A	A	A	A	A	A	A	A	A	A	A	A
N13368	647	D	D	D	D	D	D	D	D	D	L	L	L
N13369	650	A	L	D	A	A	A	A	A	D	A	A	A
N13370	656	A	A	A	D	A	A	A	A	D	D	D	D
N13371	657	A	A	D	L	D	D	D	A	L	D	A	A
N13372	659	A	A	A	D	A	A	A	A	D	A	A	A
N13373	653	D	-	-	-	D	D	D	D	D	L	L	L
N13374	655	A	-	-	-	A	A	A	A	D	X		
N13375	658	L	-	-	-	A	A	A	D	A	A	A	A
N13376	660	D	-	-	-	D	D	A	A	L	L	L	L
N13377	663	L	-	-	-	L	L	D	D	D	X		
ACCEPTABLE		14	12	11	10	18	16	17	17	12	11	12	12
LIMIT REJECTS		2	1		1	1	2	1	1	4	4	4	4
DRIFT REJECTS		3	1	3	3	4	5	5	5	7	6	5	5
TOTAL		19	14	14	14	23	23	23	23	23	21	21	21

CD4002 Group C Device Behaviour
Table III - Appendix A

NEW S/N	ARC S/N	HISTORY				MSFC-BI							
		RB	AMES QUAL				BAKE		FB	RB	PE		
		36	168	500	1000	0	500	1000	2000	3000	4000	5000	6000
N13378		UNITS WITH NO KNOWN HISTORY				A	D	D	D	D	D	D	D
N13379						A	D	D	D	A	D	A	D
N13380						A	A	L	A	A	A	A	A
N13381						A	A	A	A	A	A	A	A
N13382													
N13383						A	D	D	D	D	D	D	D
N13384						A	A	A	A	A	A	A	A
N13385	679	A	A	A	A	A	A	A	A	A	A	A	A
N13386	680	A	A	A	A	A	A	A	A	A	A	A	A
N13387	682	A	A	A	A	A	A	A	A	A	A	A	A
N13388	683	A	A	A	A	A	A	A	A	A	A	A	A
N13389	684	D	A	A	A	A	A	A	A	D	D	D	D
N13390	688	A	A	A	A	A	A	A	A	A	A	A	A
N13391	689	A	A	A	A	A	A	A	A	A	A	A	A
N13392	690	A	A	A	A	A	A	A	A	A	A	A	A
N13393	662	A	L	L	L	D	A	A	A	D	D	D	D
N13394	666	A	D	L	L	D	A	A	A	A	A	A	A
N13395	668	A	D	D	D	D	D	D	D	D	D	D	D
N13396	685	D	D	D	D	X							
N13397	637	A	A	A	A	A	A	A	A	A	A	A	A
N13398	665	L	-	-	-	L	D	A	A	D	A	A	A
N13399	669	L	-	-	-	A	A	A	A	D	D	A	A
N13400	673	A	-	-	-	A	A	A	A	A	A	A	A
N13401	676	L	-	-	-	L	D	A	A	A	A	A	A
N13402	678	D	-	-	-	D	A	A	A	A	A	A	A
ACCEPTABLE		12	9	9	9	17	17	18	19	16	16	18	17
LIMIT REJECTS		3	1	2	2	2		1					
DRIFT REJECTS		3	3	2	2	4	6	4	4	7	7	5	6
TOTAL		18	13	13	13	23	23	23	23	23	23	23	23

CD4002 Group D Device Behaviour
Table IV - Appendix A

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APPENDIX B

DEVICE BEHAVIOUR FOR THE CD4003

TABLE I	-	Group A	- Cross Reference Index to ARC Contract and Device Behaviour
TABLE II	-	Group B	- Cross Reference Index to ARC Contract and Device Behaviour
TABLE III	-	Group C	- Cross Reference Index to ARC Contract and Device Behaviour
TABLE IV	-	Group D	- Cross Reference Index to ARC Contract and Device Behaviour

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A = Acceptable Units: These units conformed to the parametric and drift limits.

L = Limit Rejects: These units were functional units but did not meet the manufacturer's limits.

D = Drift Rejects: These units were rejected due to DCA drift criteria but were otherwise within manufacturer's specifications.

X = Catastrophic unit and removed from test.

NEW S/N	ARC S/N	HISTORY				MSFC BI							
		RB	AMES QUAL				FB		RB	PE	BAKE		
		36	168	500	1000	0	500	1000	2000	3000	4000	5000	6000
N13405	9	A	A	A	A	A	A	A	A	A	A	A	A
N13406	10	A	A	A	A	A	A	A	A	A	A	A	A
N13407	11	A	A	A	A	A	A	A	A	A	A	A	A
N13408	13	A	A	A	A	A	A	A	A	A	A	A	A
N13409	15	A	A	A	A	A	A	A	A	A	A	A	A
N13410	18	A	A	A	A	A	A	A	A	A	A	A	A
N13411	19	A	A	A	A	A	A	A	A	A	A	A	A
N13412	21	A	A	A	A	A	A	A	A	A	A	A	A
N13413	23	A	A	A	A	A	A	A	A	A	A	A	A
N13414	24	A	A	A	A	A	A	A	A	A	A	A	A
N13415	8	A	D	D	A	A	A	A	A	A	A	A	A
N13416	12	D	A	A	A	A	A	A	A	A	A	A	A
N13417	17	A	D	A	A	A	A	A	A	A	A	A	A
N13418	22	A	A	D	D	A	A	A	A	A	A	A	A
N13419	30	A	D	D	D	D	D	D	D	D	D	D	D
N13420	31	A	A	D	D	D	A	A	A	A	A	A	A
N13421	32	A	A	A	A	A	A	A	A	A	A	A	A
N13422	3	L	-	-	-	A	A	A	L	L	L	L	A
N13423	4	D	D	D	D	A	A	A	A	A	A	A	A
N13424	20	D	-	-	-	D	D	A	D	D	A	A	A
N13425	25	A	-	-	-	A	A	A	D	D	A	A	A
N13426	26	D	-	-	-	D	A	A	D	D	D	D	D
ACCEPTABLE		17	14	13	14	18	20	21	17	17	19	19	20
LIMIT REJECTS		1							1	1	1	1	
DRIFT REJECTS		4	4	5	4	4	2	1	4	4	2	2	2
TOTAL		22	18	18	18	22	22	22	22	22	22	22	22

CD4003 Group A Device Behaviour
Table 1 - Appendix B

NEW S/N	ARC S/N	HISTORY				MSFC BI							
		RB	AMES QUAL				RB		PE	BAKE	FB		
		36	168	500	1000	0	500	1000	2000	3000	4000	5000	6000
N13427	28	A	A	A	A	A	A	D	D	D	D	D	D
N13428	29	A	A	A	A	A	A	A	A	A	A	A	A
N13429	35	A	A	A	A	A	A	A	A	A	L	L	L
N13430	36	A	A	A	A	A	A	A	A	A	D	D	D
N13431	37	A	A	A	A	A	A	A	A	A	D	A	D
N13432	38	A	A	A	A	A	A	A	A	A	D	D	D
N13433	39	A	A	A	A	A	A	A	A	A	D	D	D
N13434	40	A	A	A	A	A	A	A	A	A	A	A	A
N13435	41	A	A	A	A	A	A	A	A	A	A	A	A
N13436	42	A	A	A	A	A	A	A	A	A	A	A	A
N13437	34	A	A	A	D	A	D	D	A	A	X		
N13438	47	A	D	D	D	A	A	A	A	A	D	A	D
N13439	48	A	D	A	A	A	A	A	A	A	A	A	A
N13440	49	A	D	A	A	A	A	A	A	A	A	A	A
N13441	52	A	D	A	A	A	A	A	A	A	A	A	A
N13442	53	A	D	D	D	A	D	D	D	D	D	D	D
N13443	54	A	D	D	D	A	A	A	A	A	D	A	D
N13444	27	D	–	–	–	A	D	D	D	D	D	D	D
N13445	33	D	–	–	–	D	D	D	D	D	D	D	D
N13446	45	A	–	–	–	A	A	A	A	A	D	D	D
N13447	50	D	–	–	–	D	D	D	D	D	D	D	D
N13448	51	A	–	–	–	A	A	A	A	A	D	D	D
ACCEPTABLE		19	11	14	13	20	17	16	17	17	7	10	7
LIMIT REJECTS											1	1	1
DRIFT REJECTS		3	6	3	4	2	5	6	5	5	13	10	13
TOTAL		22	17	17	17	22	22	22	22	22	21	21	21

CD4003 Group B Device Behaviour
Table II - Appendix B

NEW S/N	ARC S/N	HISTORY				MSFC BI							
		RB	AMES QUAL				PE		BAKE	FB	RB		
		36	168	500	1000	0	500	1000	2000	3000	4000	5000	6000
N13449	43	A	A	A	A	A	A	A	A	A	A	A	A
N13450	44	A	A	A	A	A	A	A	A	A	A	A	A
N13451	46	A	A	A	A	A	A	A	A	A	A	A	A
N13452	56	A	A	A	A	A	A	A	A	A	A	A	A
N13453	58	A	A	A	A	A	A	A	A	A	A	A	A
N13454	67	A	A	A	A	A	A	A	A	A	A	A	A
N13455	72	A	A	A	A	A	A	A	A	D	A	A	A
N13456	74	A	A	A	A	A	L	L	A	A	A	A	A
N13457	75	A	A	A	A	L	L	L	X				
N13458	76	A	A	A	A	A	A	A	A	A	A	X	
N13459	55	A	D	A	A	A	A	A	A	A	A	A	A
N13460	59	A	D	D	D	A	A	A	A	D	A	A	A
N13461	62	A	D	D	D	A	A	A	A	D	A	A	A
N13462	63	A	D	A	A	A	A	A	A	A	A	A	A
N13463	64	A	D	D	D	D	A	A	D	D	A	A	A
N13464	65	A	D	D	D	A	A	A	A	D	A	A	A
N13465	68	A	D	A	A	A	A	A	A	A	A	A	A
N13466	69	A	D	D	D	A	A	A	A	D	A	A	A
N13467	57	D	-	-	-	A	A	A	X				
N13468	60	D	-	-	-	D	A	A	A	D	A	A	A
N13469	61	D	-	-	-	L	D	D	D	D	D	D	D
N13470	78	D	-	-	-	D	D	D	A	D	D	D	D
ACCEPTABLE		18	10	13	13	17	18	18	18	11	18	17	17
LIMIT REJECTS						2	2	2					
DRIFT REJECTS		4	8	5	5	3	2	2	2	9	2	2	2
TOTAL		22	18	18	18	22	22	22	20	20	20	19	19

CD4003 Group C Device Behaviour
Table III - Appendix B

NEW S/N	ARC S/N	HISTORY				MSFC BI							
		RB	AMES QUAL				BAKE		FB	RB	PE		
		36	168	500	1000	0	500	1000	2000	3000	4000	5000	6000
N13471	77	A	A	A	A	A	A	A	A	A	A	A	A
N13472	79	A	A	A	A	A	A	A	A	A	A	A	A
N13473	80	A	A	A	A	A	A	A	D	A	A	A	A
N13474	81	A	A	A	A	A	A	A	A	A	A	A	A
N13475	82	A	A	A	A	A	A	A	D	A	A	A	A
N13476	86	A	A	A	A	A	A	A	D	D	D	D	D
N13477	87	A	A	A	A	A	A	A	D	A	A	A	A
N13478	93	D	A	A	A	A	A	A	D	D	D	D	D
N13479	94	A	A	A	A	A	A	A	A	A	A	A	A
N13480	95	A	A	A	A	A	A	A	A	A	D	A	A
N13481	96	A	A	A	A	A	A	A	D	D	D	D	D
N13482	70	A	D	A	D	A	A	A	A	A	A	A	A
N13483	71	A	D	D	D	D	D	D	D	D	D	D	D
N13484	73	A	D	A	D	A	A	A	D	D	A	A	A
N13485	89	A	D	A	A	A	L	L	L	L	L	L	L
N13486	90	D	D	D	D	D	D	L	D	D	D	D	D
N13487	91	D	A	D	A	A	A	A	A	A	A	A	A
N13488	100	B	D	D	D	L	L	L	D	D	D	D	D
N13489	83	D	-	-	-	D	A	A	D	A	A	A	A
N13490	84	D	-	-	-	A	A	A	A	A	A	A	A
N13491	85	D	-	-	-	D	A	A	D	D	D	A	D
N13492	99	D	-	-	-	A	A	A	D	A	A	A	A
ACCEPTABLE		14	12	14	13	17	18	18	8	13	13	15	14
LIMIT REJECTS						1	2	3	1	1	1	1	1
DRIFT REJECTS		8	6	4	5	4	2	1	13	8	8	6	7
TOTAL		22	18	18	18	22	22	22	22	22	22	22	22

CD4003 Group D Device Behaviour
Table IV - Appendix B

APPENDIX C

APPENDIX C-1	CD4002 Limits and Drift
APPENDIX C-2	CD4003 Limits and Drift
APPENDIX C-3	CD4002 Pin Matrix
APPENDIX C-4	CD4003 Pin Matrix

APPENDIX C-1

TABLE 1 - CD4002

(Dual Four Input Gate)

DATA FIELD	PARAMETER	SYMBOL	TEST COND.[1]	MFG. LIMITS MIN.	MFG. LIMITS MAX.	UNITS	ALLOWABLE DRIFT
1-8	"0" Output Voltage	V_{OUT} "0"	V_{IN} = 10V		0.01	Volts	.005V
9-10	"1" Output Voltage	V_{OUT} "1"	V_{IN} = 0V	9.99		Volts	.005V
11-18	"1" Level Threshold Drain Current	Ith "1" (I17)	V_{IN} to anyone Input = 9.0V		10.0	uA	0.1 uA
19-20	"0" Level Threshold Drain Current	Ith "0" (I07)	All Inputs = 1.0V		10.0	uA	0.1 uA
21-28	Noise Margin	V_{NM}	V_{IN} = V_{OUT}	3.3	6.7	Volts	5%
29	Quiescent Device Dissipation	PT	All Inputs = 0V		100	nA	10 nA
30-37	Quiescent Device Dissipation	PT	V_{IN} to anyone Input = 10V		100	nA	10 nA
38-39	Drain to Source Current	IDS14	V_{GS} = 10V V_{DS} = 3.8V	1.3		mA	5%
40-41	Drain to Source Current	IDS14	V_{GS} = 10V V_{DS} = 3.0V	.25		mA	5%
42-49	Drain to Source Current	IDS 7	V_{GS} = 10V V_{DS} = 3.0V	2.0		mA	5%
50-57	Drain to Source Current	IDS 7	V_{GS} = 10V V_{DS} = 0.5V	.70		mA	5%

[1]Static electrical characteristic, at T_A - 25°C, V_{DD} 10V, V_{SS} 0V. All unused inputs at ground.

APPENDIX C-2

TABLE 2 - CD4003

(Dual D-Type Flip Flop)

DATA FIELD	PARAMETER	SYMBOL	TEST COND.	MFG. LIMITS MIN.	MAX.	UNITS	ALLOWABLE DRIFT
1-2	"O" Output Voltage	VO 1	Reset=+10V		.01	Volts	5 mV
3-4	"1" Output Voltage	VI 2	Reset=+10V	9.99		Volts	5 mV
5-6	Quiescent Device Dissipation per Pkg.	PT	VIN= 0 VIN=10V		2.0	uA	5 nA
7-8	Output Drive Capability	IDS "P"	V_{GS}=10V V_{DS}=-3.8V	-1.3		mA	5%
9-10	Output Drive Capability	IDS "P"	V_{GS}=10V V_{DS}=-0.5V	-0.15		mA	5%
11-12	Output Drive Capability	IDS "N"	V_{GS}=10V V_{DS}= 3V	2.0		mA	5%
13-14	Output Drive Capability	IDS "N"	V_{GS}=10V V_{DS}=0.5V	0.7		mA	5%
15-16	Threshold Voltage Reset line going"HIGH"	Vth	V_{DD}= 6V	1.4	4.5	Volts	10%
17-18	Threshold Voltage Reser line going"HIGH"	Vth	V_{DD}=14V	5.6	9.7	Volts	5%

APPENDIX C-2

TABLE 2 - CD4003

(DUAL D-TYPE FLIP FLOP)

(CONT)

DATA FIELD	PARAMETER	SYMBOL	TEST COND.	MFG. LIMITS MIN.	MAX.	UNITS	ALLOWABLE DRIFT
19-20	Threshold Voltage Data Line going"LOW"	Vth	V_{DD}=6V	1.4	4.5	Volts	10%
21-22	Threshold Voltage Data Line going"LOW"	Vth	V_{DD}=14V	5.6	9.7	Volts	5%
23-24	Threshold Voltage Data Line going"HIGH"	Vth	V_{DD}=6V	1.4	4.5	Volts	10%
25-26	Threshold Voltage Data Line going"HIGH"	Vth	V_{DD}=14V	5.6	9.7	Volts	5%
27-28	Threshold Voltage Clock line going"LOW"	Vth	V_{DD}=6V	1.4	4.5	Volts	10%
29-30	Threshold Voltage Clock line going"LOW"	Vth	D_{DD}=14V	5.6	9.7	Volts	5%
31-32	Threshold Voltage Clock line going"LOW"	Vth	V_{DD}=6V	1.4	4.5	Volts	10%
33-34	Threshold Voltage Clock line going"LOW"	Vth	D_{DD}=14V	5.6	9.7	Volts	5%
35-36	Threshold Voltage Clock line going"HIGH"	Vth	V_{DD}=6V(master)	1.4	4.5	Volts	10%
37-38	Threshold Voltage Clock line going"LOW"	Vth	D_{DD}=14V(master)	5.6	9.7	Volts	5%

APPENDIX C-2

TABLE 2 - CD4003

(Dual D-Type Flip Flop)

(CONT)

DATA FIELD	PARAMETER	SYMBOL	TEST COND.	MFG. LIMITS MIN.	MAX.	UNITS	ALLOWABLE DRIFT
39-40	Threshold Voltage Clock line going"HIGH"	Vth	V_{DD}=6V(Slave)	1.4	4.5	Volts	10%
41-42	Threshold Voltage Clock line going"LOW"	Vth	V_{DD}=14V(Slave)	5.6	9.7	Volts	5%

TEST NO	TEST	SENSE	TEST CONDITIONS													TEST LIMITS		
			PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	PIN 11	PIN 12	PIN 13	PIN 14	MIN	MAX	
1	Vo	1		10 V	GND	GND	GND		GND		GND	GND	GND	GND		10 V		10 mV	
2	Vo	1		GND	10 V	GND	GND		GND		GND	GND	GND	GND		10 V		10 mV	
3	Vo	1		GND	GND	10 V	GND		GND		GND	GND	GND	GND		10 V		10 mV	
4	Vo	1		GND	GND	GND	10 V		GND		GND	GND	GND	GND		10 V		10 mV	
5	Vo	13		GND	GND	GND	GND		GND		10V	GND	GND	GND		10 V		10 mV	
6	Vo	13		GND	GND	GND	GND		GND		GND	10V	GND	GND		10 V		10 mV	
7	Vo	13		GND	GND	GND	GND		GND		GND	GND	10V	GND		10 V		10 mV	
8	Vo	13		GND	GND	GND	GND		GND		GND	GND	GND	10V		10 V		10 mV	
9	V_1	1		GND	GND	GND	GND		GND		GND	GND	GND	GND		10 V		10 mV	(1)
10	V_1	13		GND	GND	GND	GND		GND		GND	GND	GND	GND		10 V		10 mV	(1)
11	I_1	7		9 V	GND	GND	GND		GND		GND	GND	GND	GND		10 V		10 uA	
12	I_1	7		GND	9 V	GND	GND		GND		GND	GND	GND	GND		10 V		10 uA	
13	I_1	7		GND	GND	9 V	GND		GND		GND	GND	GND	GND		10 V		10 uA	
14	I_1	7		GND	GND	GND	9 V		GND		GND	GND	GND	GND		10 V		10 uA	
15	I_1	7		GND	GND	GND	GND		GND		9 V	GND	GND	GND		10 V		10 uA	
16	I_1	7		GND	GND	GND	GND		GND		GND	9 V	GND	GND		10 V		10 uA	
17	I_1	7		GND	GND	GND	GND		GND		GND	GND	9 V	GND		10 V		10 uA	
18	I_1	7		GND	GND	GND	GND		GND		GND	GND	GND	9 V		10 V		10 uA	
19	I_0	7		1 V	1 V	1 V	1 V		GND		GND	GND	GND	GND		10 V		10 uA	
20	I_0	7		GND	GND	GND	GND		GND		1 V	1 V	1 V	1 V		10 V		10 uA	
21																			
22																			
23																			
24																			

(1) Measure with ref. to pin #14.

(2) 100 KΩ resistor ext. 4-3 to ext. 5-3.

TEST NO	TEST	SENSE	TEST CONDITIONS														TEST LIMITS		
			PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	PIN 11	PIN 12	PIN 13	PIN 14	MIN	MAX	
1	V_{NM}	1	R1	R1	GND	GND	GND		GND		GND	GND	GND	GND		10 V	3.3V	6.7V	(2)
2	V_{NM}	1	R1	GND	R1	GND	GND		GND		GND	GND	GND	GND		10 V	3.3V	6.7V	(2)
3	V_{NM}	1	R1	GND	GND	R1	GND		GND		GND	GND	GND	GND		10 V	3.3V	6.7V	(2)
4	V_{NM}	1	R1	GND	GND	GND	R1		GND		GND	GND	GND	GND		10 V	3.3V	6.7V	(2)
5	V_{NM}	13		GND	GND	GND	GND		GND		R1	GND	GND	GND	R1	10 V	3.3V	6.7V	(2)
6	V_{NM}	13		GND	GND	GND	GND		GND		GND	R1	GND	GND	R1	10 V	3.3V	6.7V	(2)
7	V_{NM}	13		GND	GND	GND	GND		GND		GND	GND	R1	GND	R1	10 V	3.3V	6.7V	(2)
8	V_{NM}	13		GND	GND	GND	GND		GND		GND	GND	GND	R1	R1	10 V	3.3V	6.7V	(2)
9	PT	*		GND	GND	GND	GND		GND		GND	GND	GND	GND		10 V		100 nA	
10	PT	*		10 V	GND	GND	GND		GND		GND	GND	GND	GND		10 V		100nA	
11	PT	*		GND	10 V	GND	GND		GND		GND	GND	GND	GND		10 V		100nA	
12	PT	*		GND	GND	10 V	GND		GND		GND	GND	GND	GND		10 V		100nA	
13	PT	*		GND	GND	GND	10 V		GND		GND	GND	GND	GND		10 V		100nA	
14	PT	*		GND	GND	GND	GND		GND		10 V	GND	GND	GND		10 V		100nA	
15	PT	*		GND	GND	GND	GND		GND		GND	10 V	GND	GND		10 V		100nA	
16	PT	*		GND	GND	GND	GND		GND		GND	GND	10 V	GND		10 V		100nA	
17	PT	*		GND	GND	GND	GND		GND		GND	GND	GND	10 V		10 V		100nA	
18																			
19																			
20																			
21																			
22																			
23																			
24																			

(1) Measure with ref. to pin #14

(2) R1 is a 100 K Ω resistor ext. 4-3 to ext. 5-3.

* See page 2A of 3

TEST NO.	TEST	SENSE.
9	PT	2,3,4, 5, 7, 9, 10, 11, 12,
10	PT	3, 4, 5, 7, 9, 10, 11, 12
11	PT	2, 4, 5, 7, 9, 10, 11, 12
12	PT	2, 3, 5, 7, 9, 10, 11, 12
13	PT	2, 3, 4, 7, 9, 10, 11, 12
14	PT	2, 3, 4, 5, 7, 10, 11, 12
15	PT	2, 3, 4, 5, 7, 9, 11, 12
16	PT	2, 3, 4, 5, 7, 9, 10, 12
17	PT	2, 3, 4, 5, 7, 9, 10 , 11

TEST NO	TEST	SENSE	TEST CONDITIONS														TEST LIMITS	
			PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	PIN 11	PIN 12	PIN 13	PIN 14	MIN	MAX
1	I_{DS}	14	-3.8V	-10V	-10V	-10V	-10V		-10V		-10V	-10 V	-10V	-10V		GND	-1.3mA	
2	I_{DS}	14		-10V	-10V	-10V	-10V		-10V		-10V	-10 V	-10V	-10V	-3.8V	GND	-1.3mA	
3	I_{DS}	14	-0.5V	-10V	-10V	-10V	-10V		-10V		-10V	-10V	-10V	-10V		GND	-0.25mA	
4	I_{DS}	14		-10V	-10V	-10V	-10V		-10V		-10V	-10V	-10V	-10V	-0.5V	GND	-0.25mA	
5	I_{DS}	7	3.0V	10V	GND	GND	GND		GND		GND	GND	GND	GND		10 V	2 mA	
6	I_{DS}	7	3.0V	GND	10 V	GND	GND		GND		GND	GND	GND	GND		10 V	2 mA	
7	I_{DS}	7	3.0V	GND	GND	10 V	GND		GND		GND	GND	GND	GND		10 V	2 mA	
8	I_{DS}	7	3.0V	GND	GND	GND	10 V		GND		GND	GND	GND	GND		10 V	2 mA	
9	I_{DS}	7		GND	GND	GND	GND		GND		10 V	GDN	GND	GND	3.0V	10 V	2 mA	
10	I_{DS}	7		GND	GND	GND	GND		GND		GND	10 V	GND	GND	3.0V	10 V	2 mA	
11	I_{DS}	7		GND	GND	GND	GND		GND		GND	GND	10 V	GND	3.0V	10 V	2 mA	
12	I_{DS}	7		GND	GND	GND	GND		GND		GND	GND	GND	10V	3.0V	10 V	2 mA	
13	I_{DS}	7	0.5V	10 V	GND	GND	GND		GND		GND	GND	GND	GND		10 V	0.7mA	
14	I_{DS}	7	0.5V	GND	10 V	GND	GND		GND		GND	GND	GND	GND		10 V	0.7mA	
15	I_{DS}	7	0.5V	GND	GND	10 V	GND		GND		GND	GND	GND	GND		10 V	0.7mA	
16	I_{DS}	7	0.5V	GND	GND	GND	10 V		GND		GND	GND	GND	GND		10 V	0.7mA	
17	I_{DS}	7		GND	GND	GND	GND		GND		10 V	GND	GND	GND	0.5V	10 V	0.7mA	
18	I_{DS}	7		GND	GND	GND	GND		GND		GND	10 V	GND	GND	0.5V	10 V	0.7mA	
19	I_{DS}	7		GND	GND	GND	GND		GND		GND	GND	10 V	GND	0.5V	10 V	0.7mA	
20	I_{DS}	7		GND	GND	GND	GND		GND		GND	GND	GND	10 V	0.5V	10 V	0.7mA	
21																		
22																		
23																		
24																		

(1) Measure with ref. to pin #14.

(2) 100 KΩ resistor ext. 4-3 to ext. 5-3.

TEST NO	TEST	SENSE	TEST CONDITIONS														TEST LIMITS	
			PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	PIN 11	PIN 12	PIN 13	PIN 14	MIN	MAX
1	V_0	1			GND	10 V	GND		GND		GND	GND	GND			10V		10 mV
2	V_0	13			GND	GND	GND		GND		GND	10 V	GND			10V		10 mV (1)
3	V_1	2			GND	10 V	GND		GND		GND	GND	GND			10V		10 mV
4	V_1	12			GND	GND	GND		GND		GND	10 V	GND			10V		10 mV (1)
5	PT	*			GND	GND	GND		GND		GND	GND	GND			10V		2uA
6	PT	7			10 V	10 V	10 V		GND		10 V	10 V	10 V			10V		2 uA
7	I_{DSP}	1	-3.8V	-10V	-10V	-10V	-10V		-10V		-10 V	-10 V	-10 V			GND	-1.3mA	
8	I_{DSP}	13		-10V	-10 V	-10V	-10V		-10V		-10 V	-10 V	-10 V	-10 V	-3.8V	GND	-1.3mA	
9	I_{DSP}	1	-0.5V	-10V	-10 V	-10V	-10V		-10V		-10 V	-10 V	-10 V			GND	-0.15mA	
10	I_{DSP}	13		-10V	-10 V	-10V	-10V		-10V		-10 V	-10 V	-10 V	-10V	-0.5V	GND	-0.15mA	
11	I_{DSN}	1	3.0V	10V	GND	GND	GND		GND		GND	GND	GND			10 V	2.0mA	
12	I_{DSN}	13		GND	GND	GND	GND		GND		GND	GND	GND	10 V	3.0V	10 V	2.0mA	
13	I_{DSN}	1	0.5V	GND	GND	GND	GND		GND		GND	GND	GND			10 V	0.7mA	
14	I_{DSN}	13		GND	GND	GND	GND		GND		GND	GND	GND	10 V	0.5V	10 V	0.7mA	
15																		
16																		
17																		
18																		
19																		
20																		
21																		
22																		
23																		
24																		

(1) Measure with ref. to pin # 14. * Pin #5- Sense, #3,4,5,7, 9, 10, 11

TEST NO	TEST	SENSE	TEST CONDITIONS														TEST LIMITS	
			PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	PIN 11	PIN 12	PIN 13	PIN 14	MIN	MAX
1	V_{TH}	4		DET	MOM	+Rmp	6 V		GND		GND	GND	GND			6 V	1.4V	4.5V
2	V_{TH}	10			GND	GND	GND		GND		6 V	+Rmp	MOM	DET		6 V	1.4V	4.5V
3	V_{TH}	4		DET	MOM	+Rmp	14 V		GND		GND	GND	GND			14V	5.6V	9.7V
4	V_{TH}	10			GND	GND	GND		GND		14V	+Rmp	MOM	DET		14V	5.6V	9.7V
5	V_{TH}	5		DET	CLOCK	GND	-Rmp		GND		GND	GND	GND			6V	1.4V	4.5V
6	V_{TH}	9			GND	GND	GND		GND		-Rmp	GND	CLOCK	DET		6V	1.4V	4.5V
7	V_{TH}	5		DET	CLOCK	GND	-Rmp		GND		GND	GND	GND			14V	5.6V	9.7V
8	V_{TH}	9			GND	GND	GND		GND		-Rmp	GND	CLOCK	DET		14V	5.6V	9.7V
9	V_{TH}	5	DET		CLOCK	GND	+Rmp		GND		GND	GND	GND			6V	1.4V	4.5V
10	V_{TH}	9			GND	GND	GND		GND		+Rmp	GND	CLOCK		DET	6V	1.4V	4.5V
11	V_{TH}	5	DET		CLOCK	GND	+Rmp		GND		GND	GND	GND			14V	5.6V	9.7V
12	V_{TH}	9			GND	GND	GND		GND		+Rmp	GND	CLOCK		DET	14V	5.6V	9.7V
13	V_{TH}	3		DET	-Rmp	GND	MOM		GND		GND	GND	GND			6V	1.4V	4.5V
14	V_{TH}	11			GND	GND	GND		GND		MOM	GND	-Rmp	DET		6V	1.4V	4.5V
15	V_{TH}	3		DET	-Rmp	GND	MOM		GND		GND	GND	GND			14V	5.6 V	9.7V
16	V_{TH}	11			GND	GND	GND		GND		MOM	GND	-Rmp	DET		14V	5.6V	9.7V
17	V_{TH}	3	DET		-Rmp	GND	MOM		GND		GND	GND	GND			6V	1.4V	4.5V
18	V_{TH}	11			GND	GND	GND		GND		MOM	GND	-Rmp		DET	6V	1.4V	4.5V
19	V_{TH}	3	DET		-Rmp	GND	MOM		GND		GND	GND	GND			14V	5.6V	9.7V
20	V_{TH}	11			GND	GND	GND		GND		MOM	GND	-Rmp		DET	14V	5.6V	9.7V
21																		
22																		
23																		
24																		

			TEST CONDITIONS														TEST LIMITS	
TEST NO	TEST	SENSE	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	PIN 11	PIN 12	PIN 13	PIN 14	MIN	MAX
1	V_{TH}	3		DET	+Rmp	GND	MOM		GND		GND	GND	GND			6 V	1.4V	4.5V
2	V_{TH}	11			GND	GND	GND		GND		MOM	GND	+Rmp	DET		6 V	1.4V	4.5V
3	V_{TH}	3		DET	+Rmp	GND	MOM		GND		GND	GND	GND			14V	5.6V	9.7V
4	V_{TH}	11			GND	GND	GND		GND		MOM	GND	+Rmp	DET		14 V	5.6V	9.7V
5	V_{TH}	3	DET		+Rmp	GND	MOM		GND		GND	GND	GND			6 V	1.4V	4.5V
6	V_{TH}	11			GND	GND	GND		GND		MOM	GND	+Rmp		DET	6 V	1.4V	4.5V
7	V_{TH}	3	DET		+Rmp	GND	MOM		GND		GND	GND	GND			14 V	5.6V	9.7V
8	V_{TH}	11			GND	GND	GND		GND		MOM	GND	+Rmp		DET	14 V	5.6V	9.7V
9																		
10																		
11																		
12																		
13																		
14																		
15																		
16																		
17																		
18																		
19																		
20																		
21																		
22																		
23																		
24																		

DGA

APPENDIX D

CD4002 DATA GRAPHS

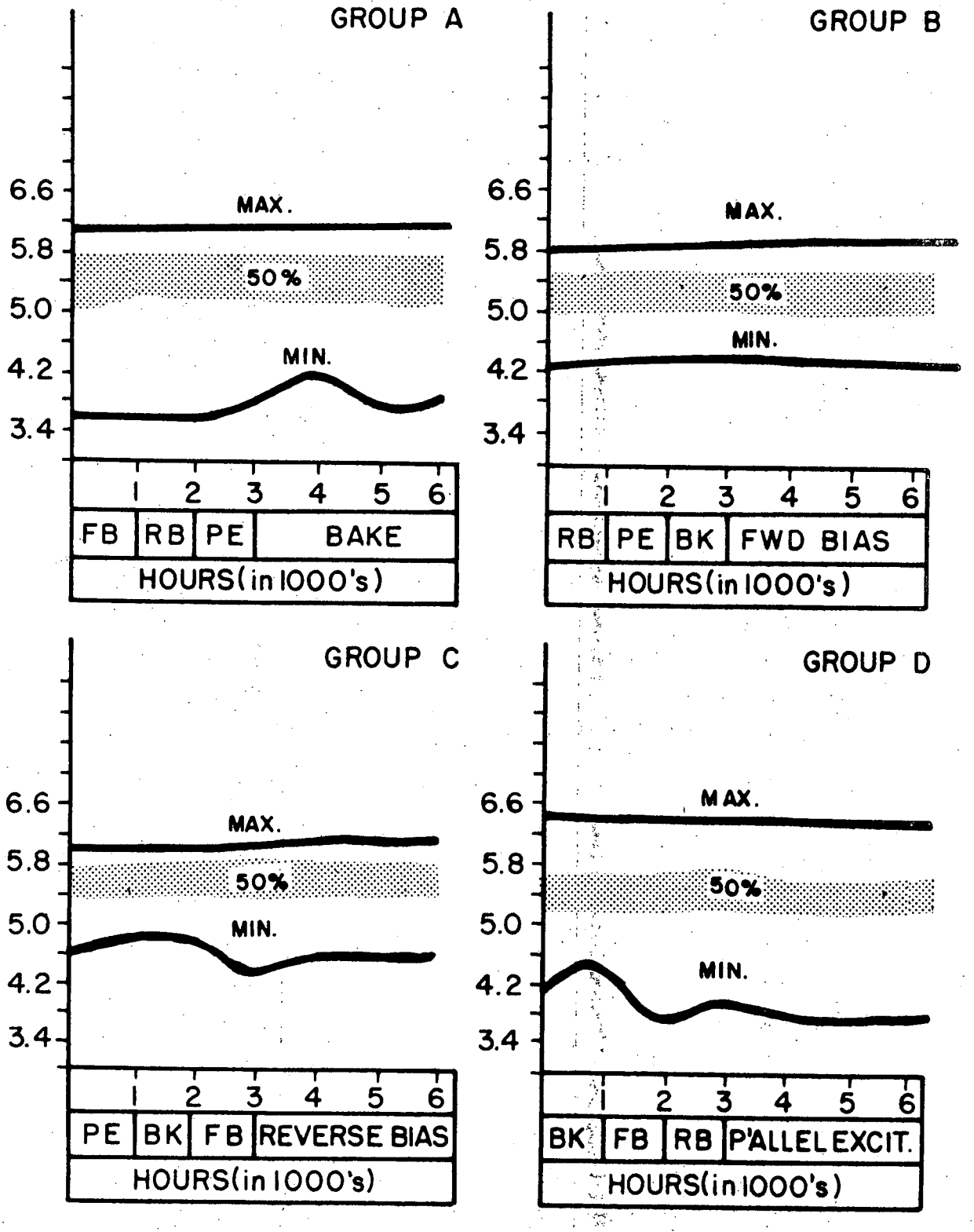
The acceptable data is presented in graphical form. The axis for the graph has time in hours vs the parameter unit of measure.

The graphs of this appendix are a representative sample of each parameter and displays the minimum, mean and maximum value in centile form.

CD 4002

UNITSmA

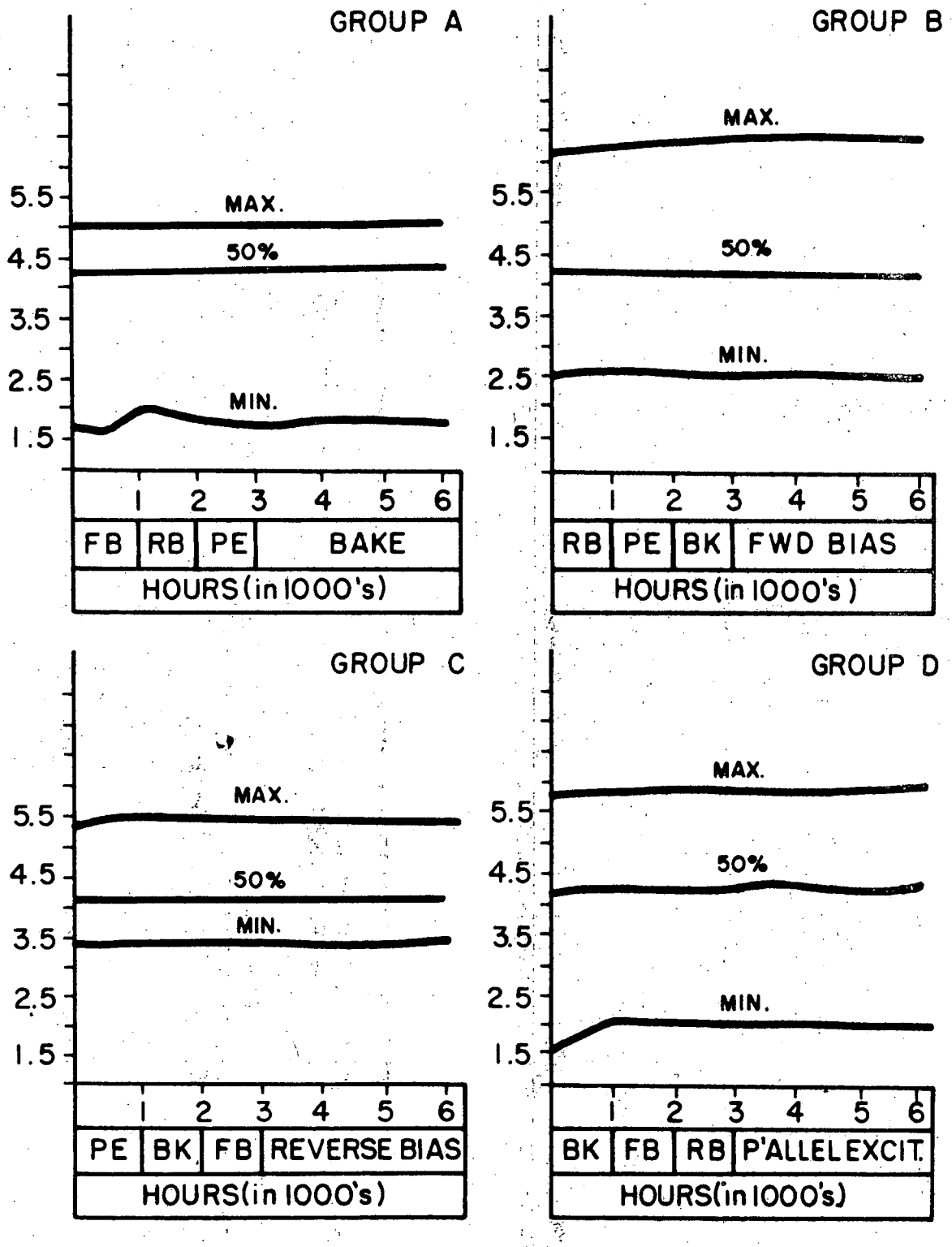
PARAMETER:--- VNM Noise Margin
SYMBOL:------- VNM
CONDITIONS:--- VlN = Vout
LIMITS:------- 3.3 to 6.7 Volts
NUMBER:------ 1



CD 4002

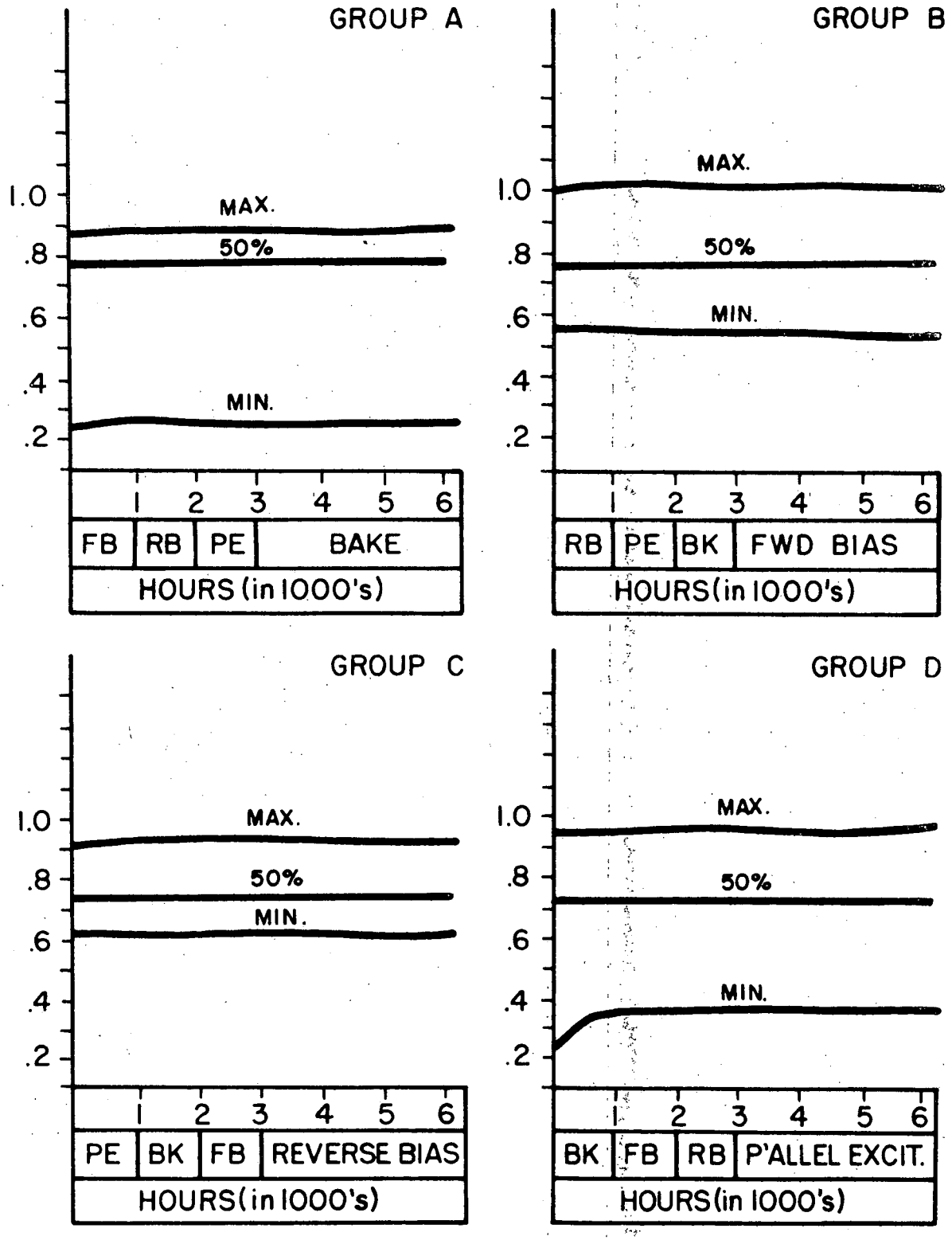
UNITS mA

PARAMETER:--- Drain to Source Current
SYMBOL:------ IDS14
CONDITIONS:--- Vgs = 10V, Vds = 3.8V
LIMITS:------- 1.3 mA
NUMBER:------ 2



CD 4002 UNITS mA

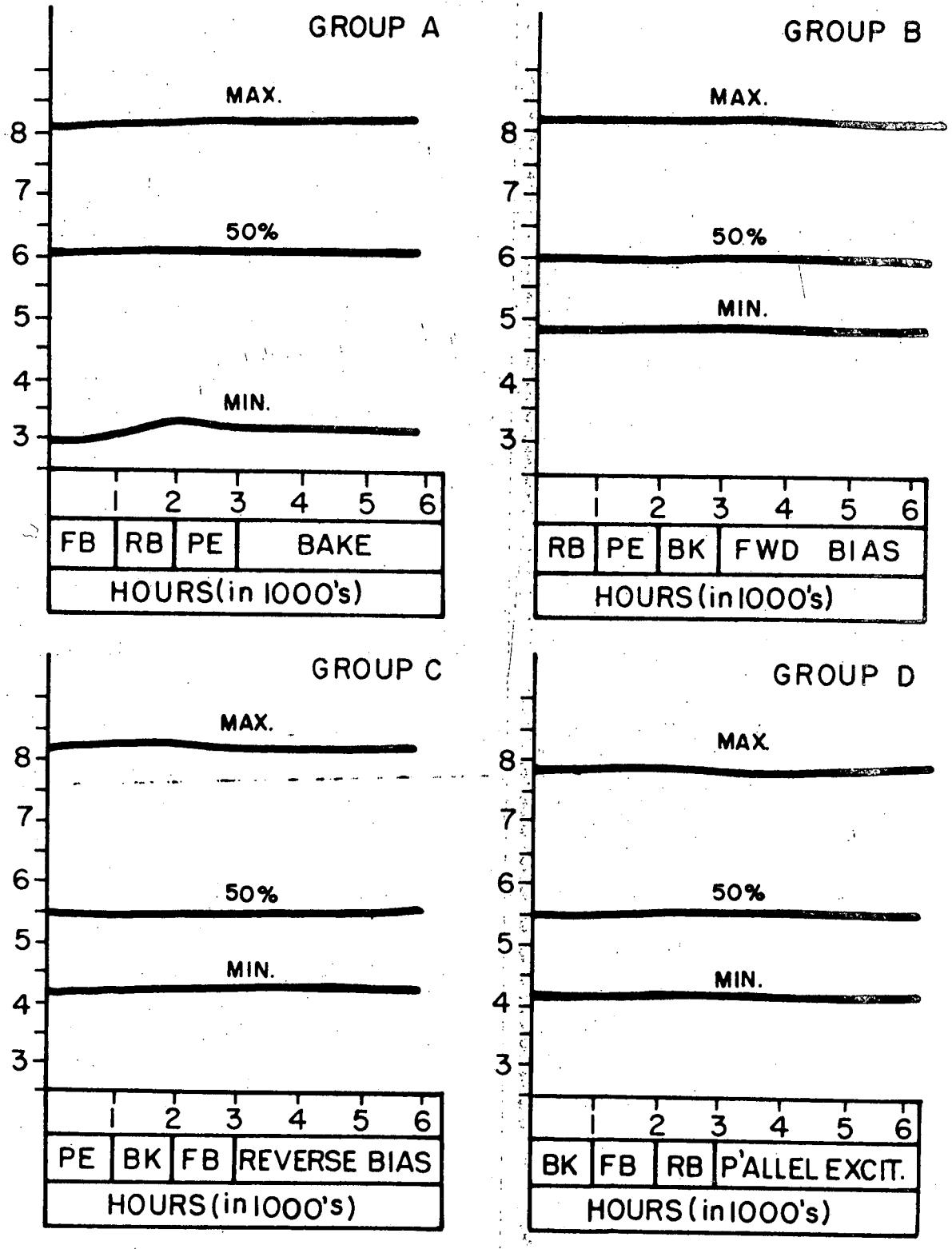
PARAMETER: --- Drain to Source Current
SYMBOL: ------ IDS14
CONDITIONS: --- Vgs = 10V, Vds = 3.0V
LIMITS: ------ .25mA
NUMBER: ------ 3



CD 4002

UNITS mA

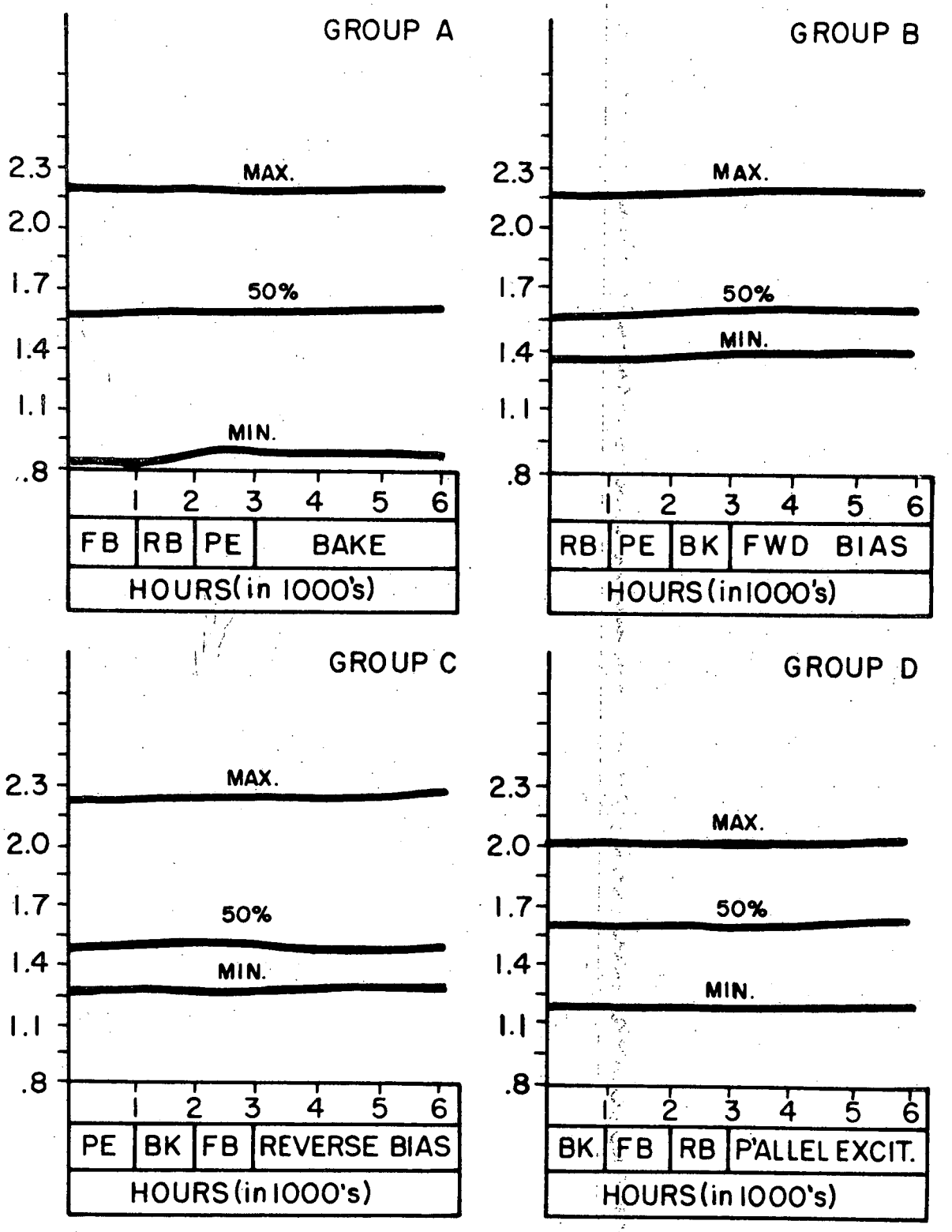
PARAMETER:--- Drain to Source Current
SYMBOL:------- IDS7
CONDITIONS:--- Vgs = 10V, Vds = 3.0V
LIMITS:------- 2.0mA
NUMBER:------- 4



CD4002

UNITS mA

PARAMETER:--- Drain to Source Current
SYMBOL:------ IDS7
CONDITIONS:--- Vgs = 10V, Vds 0.5V
LIMITS:------- 0.7mA
NUMBER:------ 5

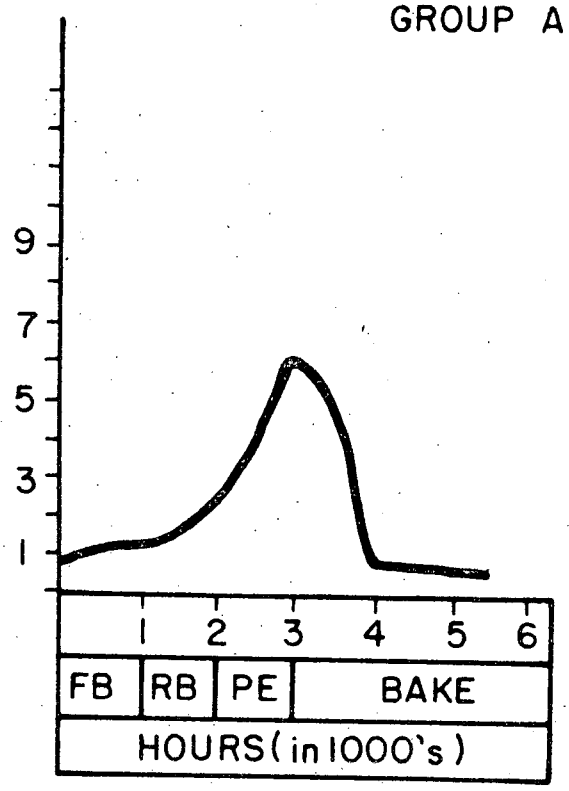


CD 4002

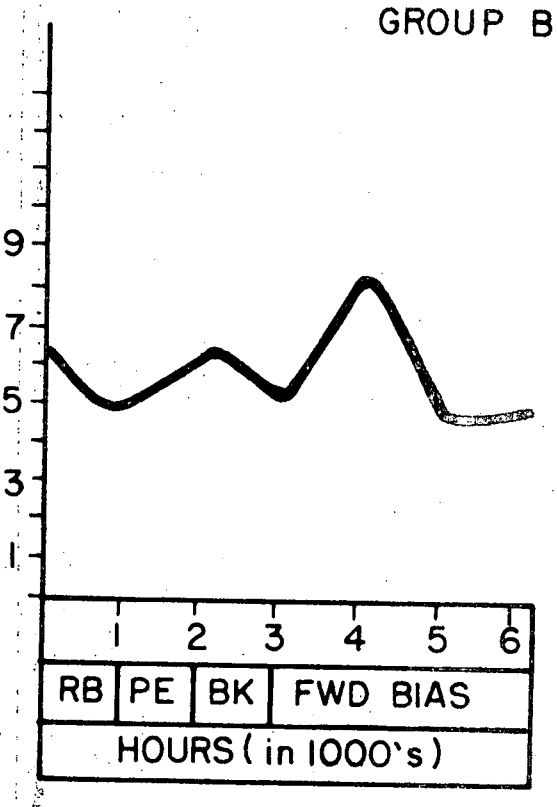
UNITS uA

PARAMETER:--- Threshold Drain Current
SYMBOL:------ Ith (1)
CONDITIONS:-- VDD=10V,VIN to any one input = 9V
LIMITS:------ 10mA
NUMBER:----- 6

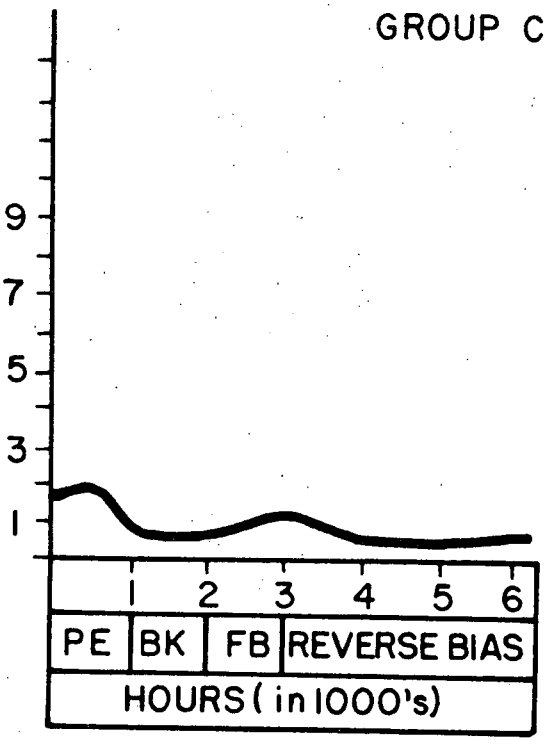
GROUP A



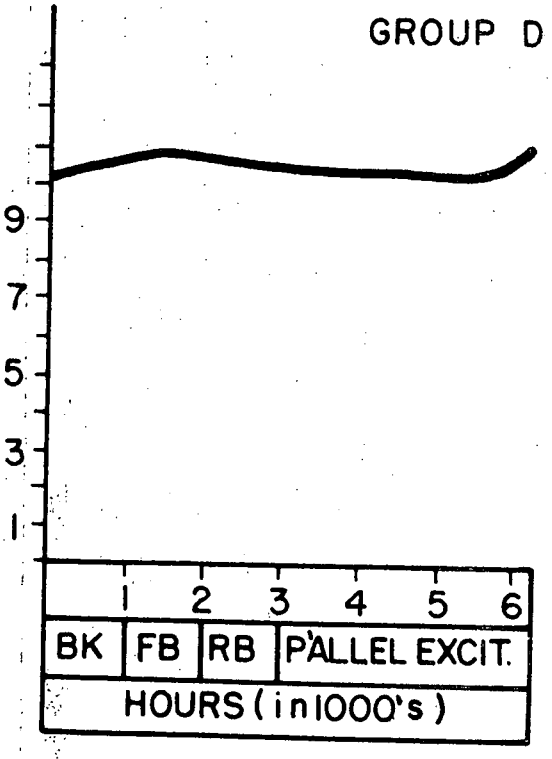
GROUP B



GROUP C



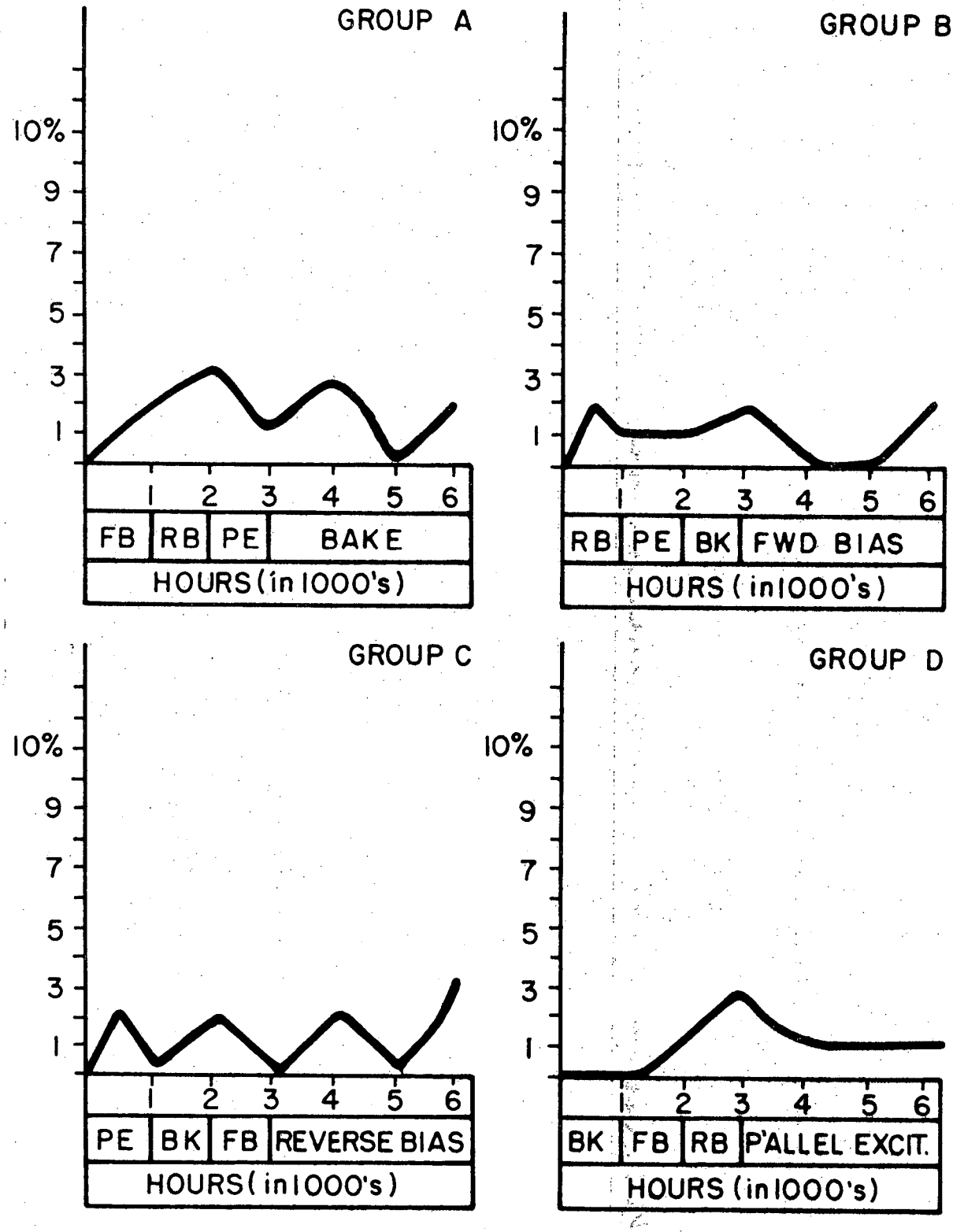
GROUP D



CD 4002

UNITS %

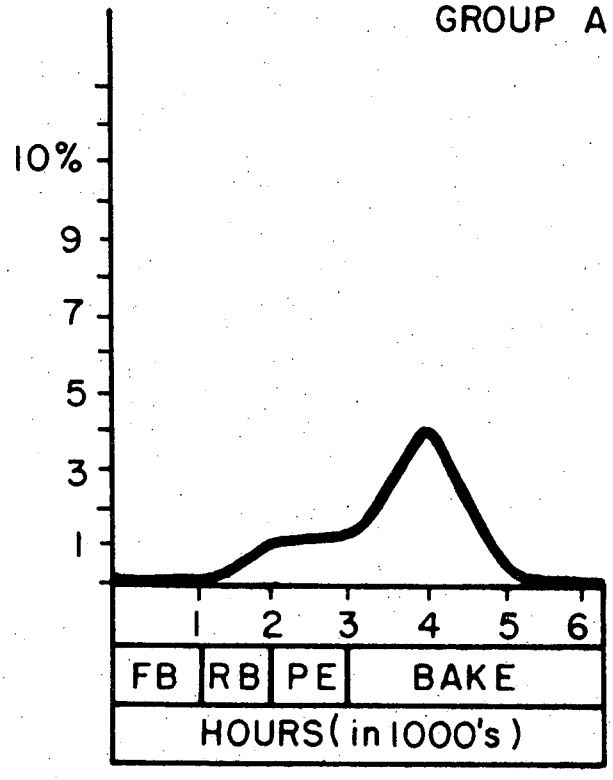
PARAMETER:-- Drain to Source Current
SYMBOL:----- IDS7
CONDITIONS:-- Vgs = 10V, Vds = 3.0V
LIMITS:----- 2.0mA
NUMBER:----- 9

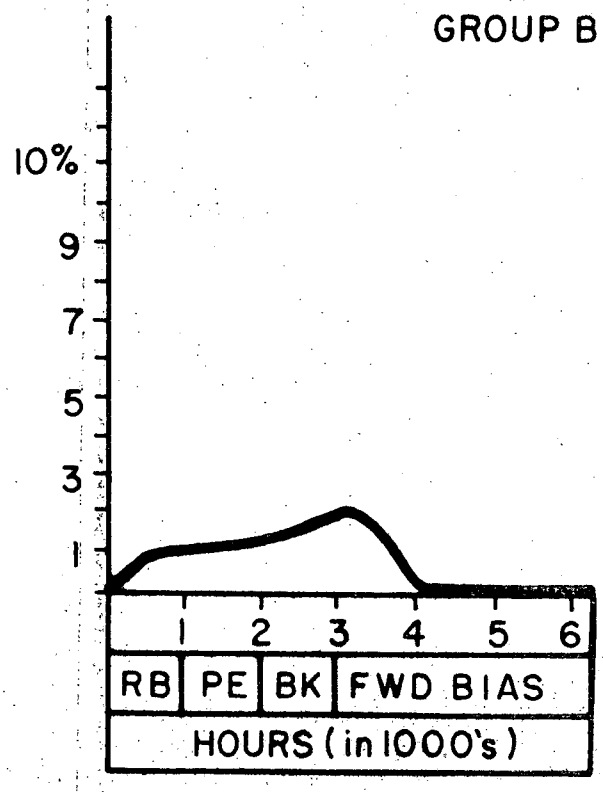


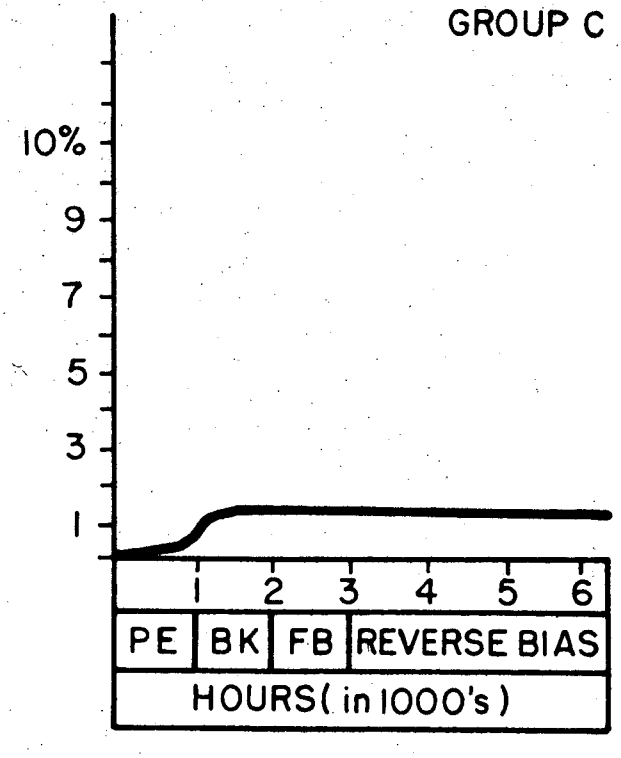
CD 4002

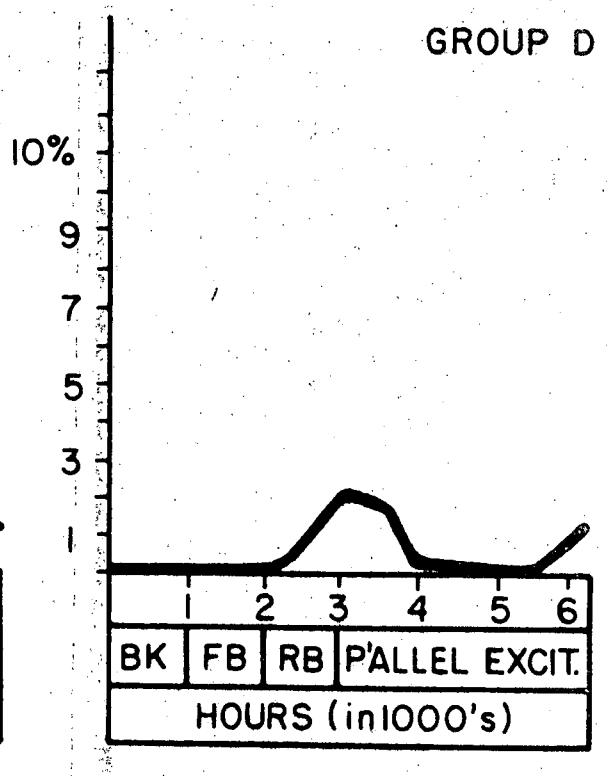
UNITS %

PARAMETER:-- Drain to Source Current
SYMBOL:----- IDS7
CONDITIONS:-- Vgs = 10V, Vds 0.5V
LIMITS:----- 0.7mA
NUMBER:----- 10



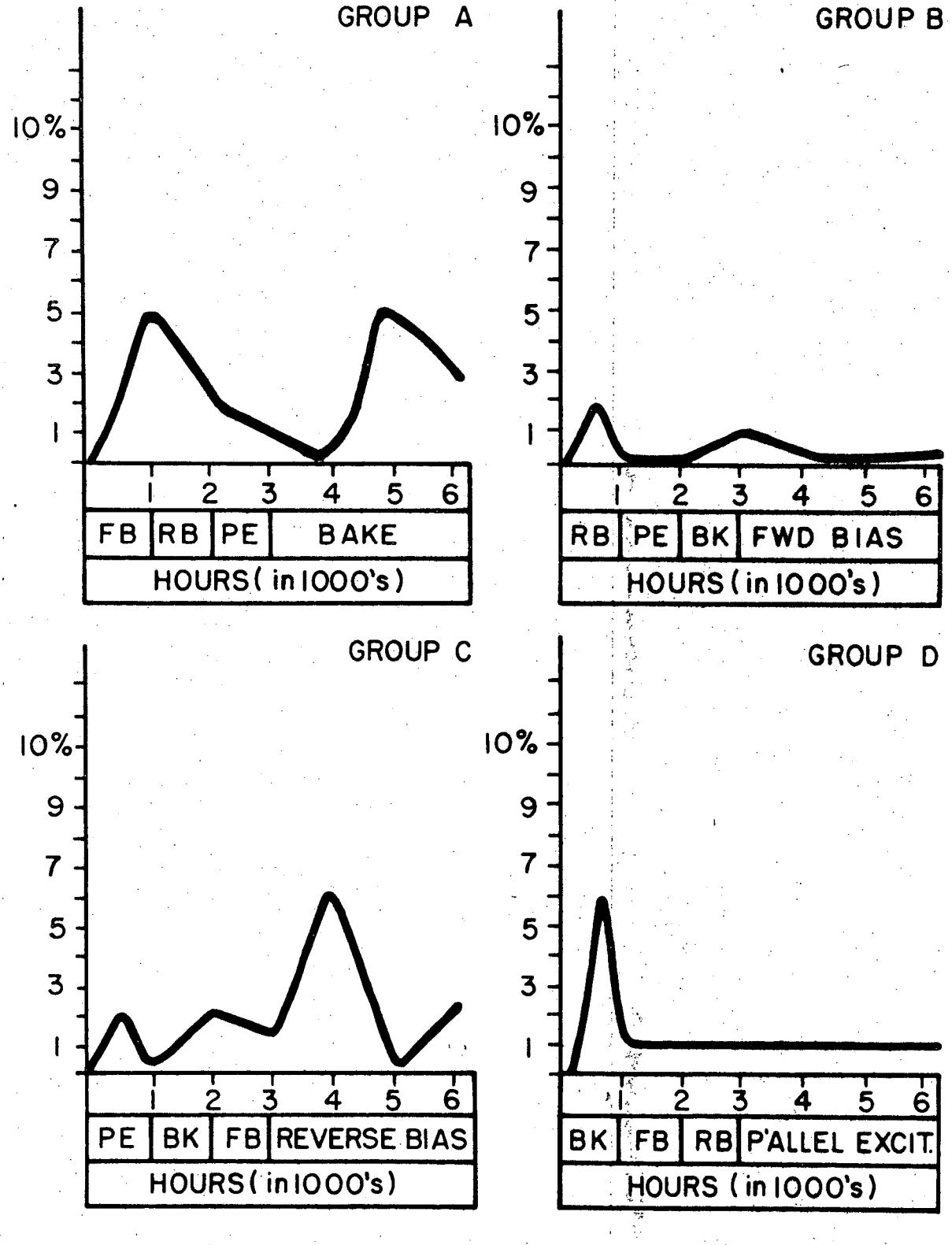






CD 4002 UNITS %

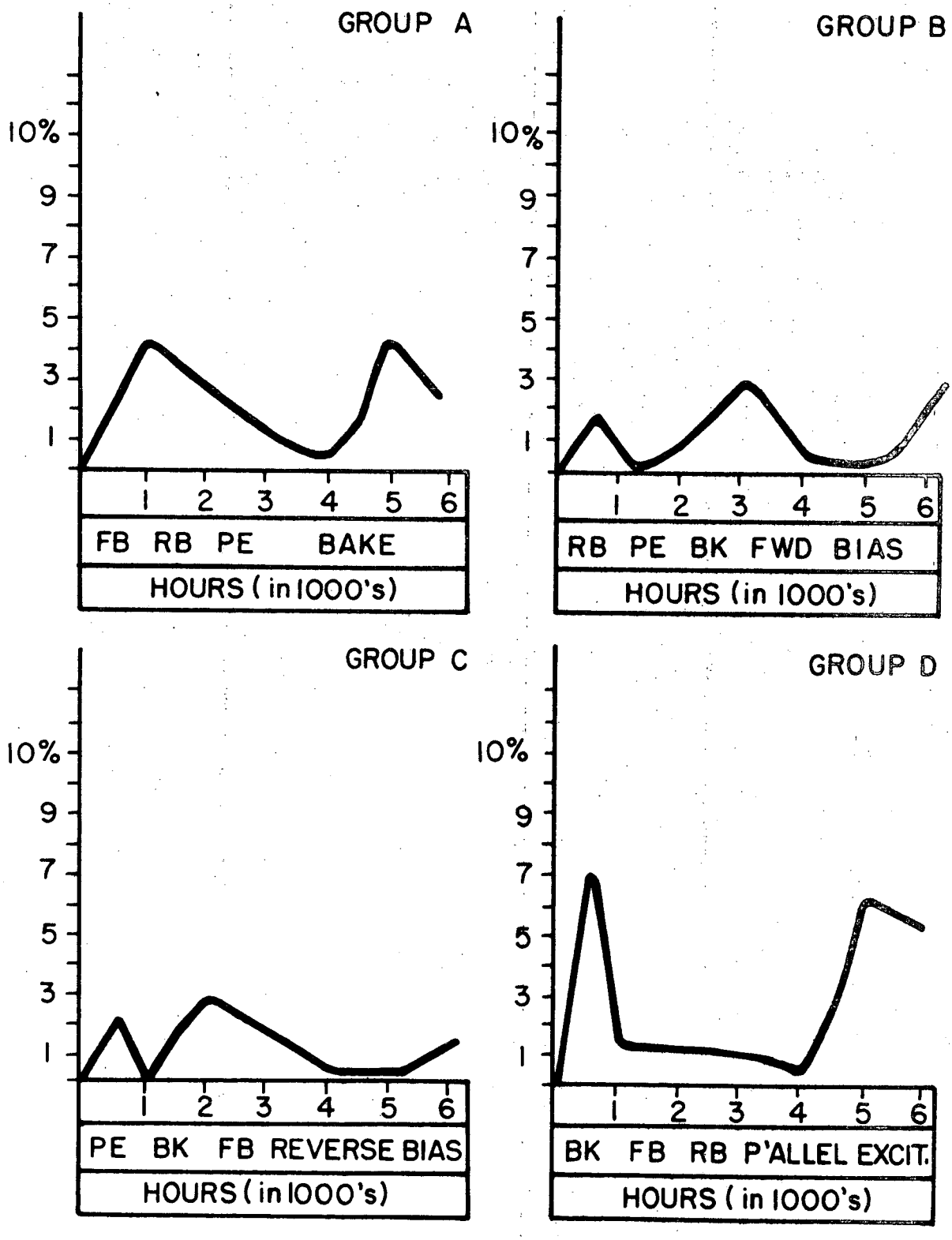
PARAMETER: Drain to Source Current
SYMBOL: IDS14
CONDITIONS: Vgs = 10V, Vds = 3.0V
LIMITS: .25mA
NUMBER: 11



CD 4002

UNITS %

PARAMETER:-- Drain to Source Current
SYMBOL:----- IDS14
CONDITIONS:-- Vgs = 10V, Vds = 3.8V.
LIMITS:------ 1.3mA
NUMBER:----- 12

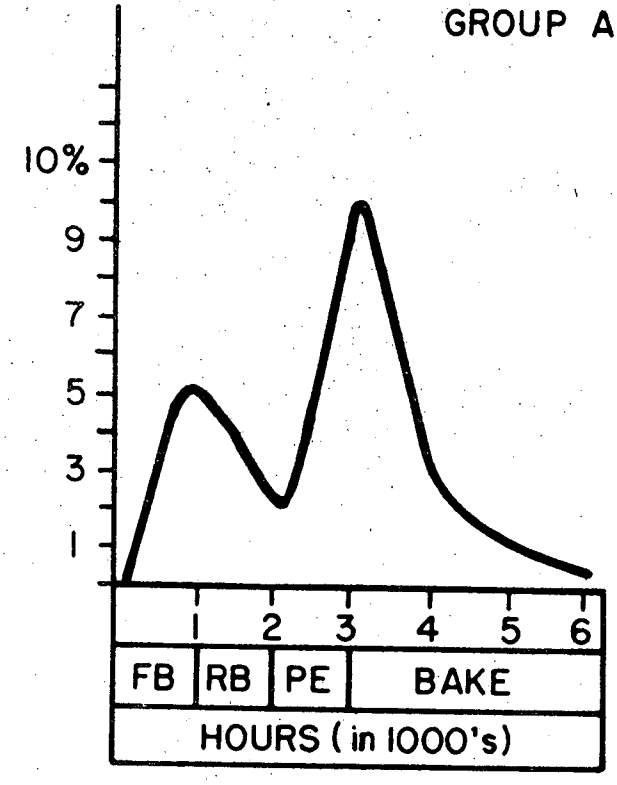


CD 4002

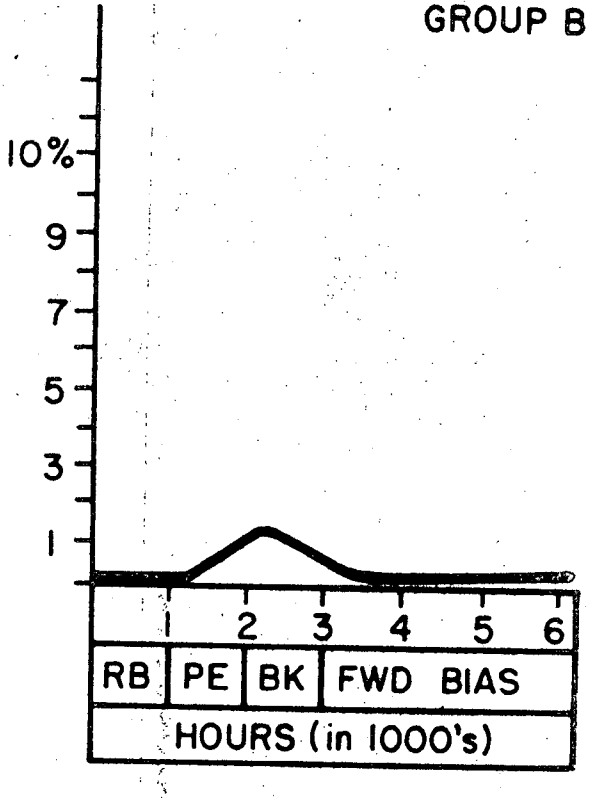
UNITS %

PARAMETER:--- VNM Noise Margin
SYMBOL:------ VNM
CONDITIONS:-- VlN = Vout
LIMITS:------ 3.3 to 6.7 Volts
NUMBER:----- 13

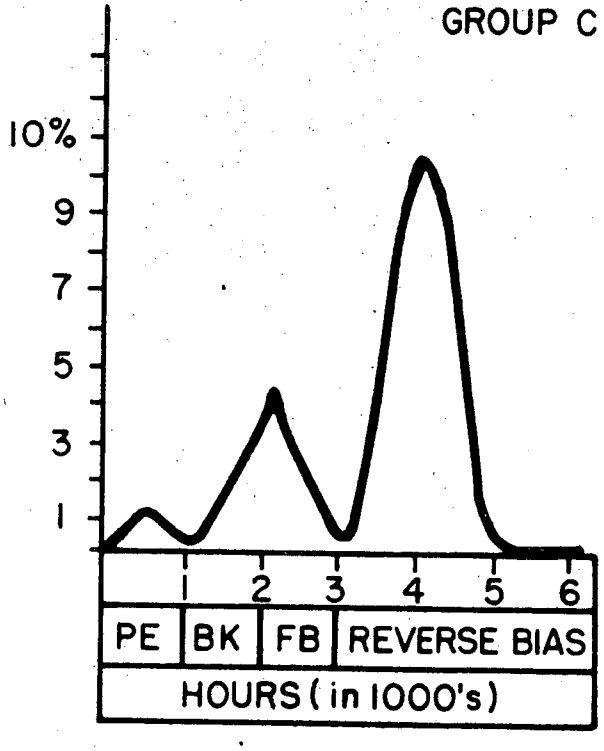
GROUP A



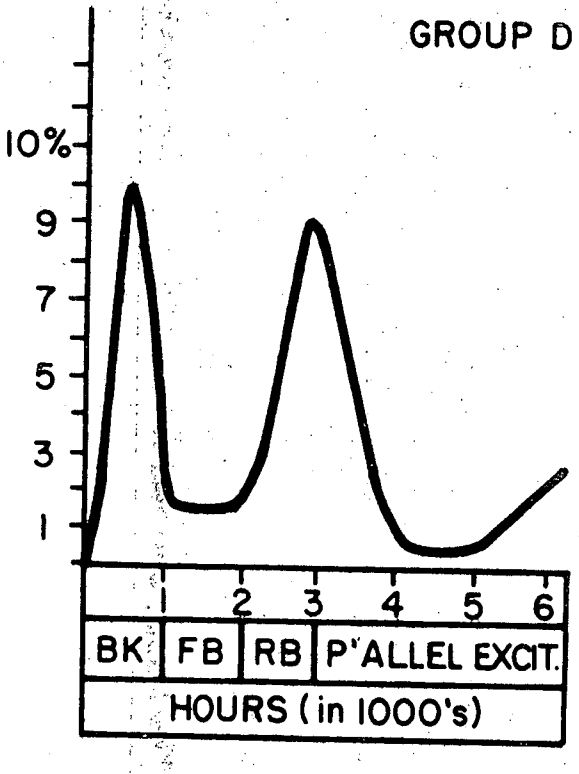
GROUP B

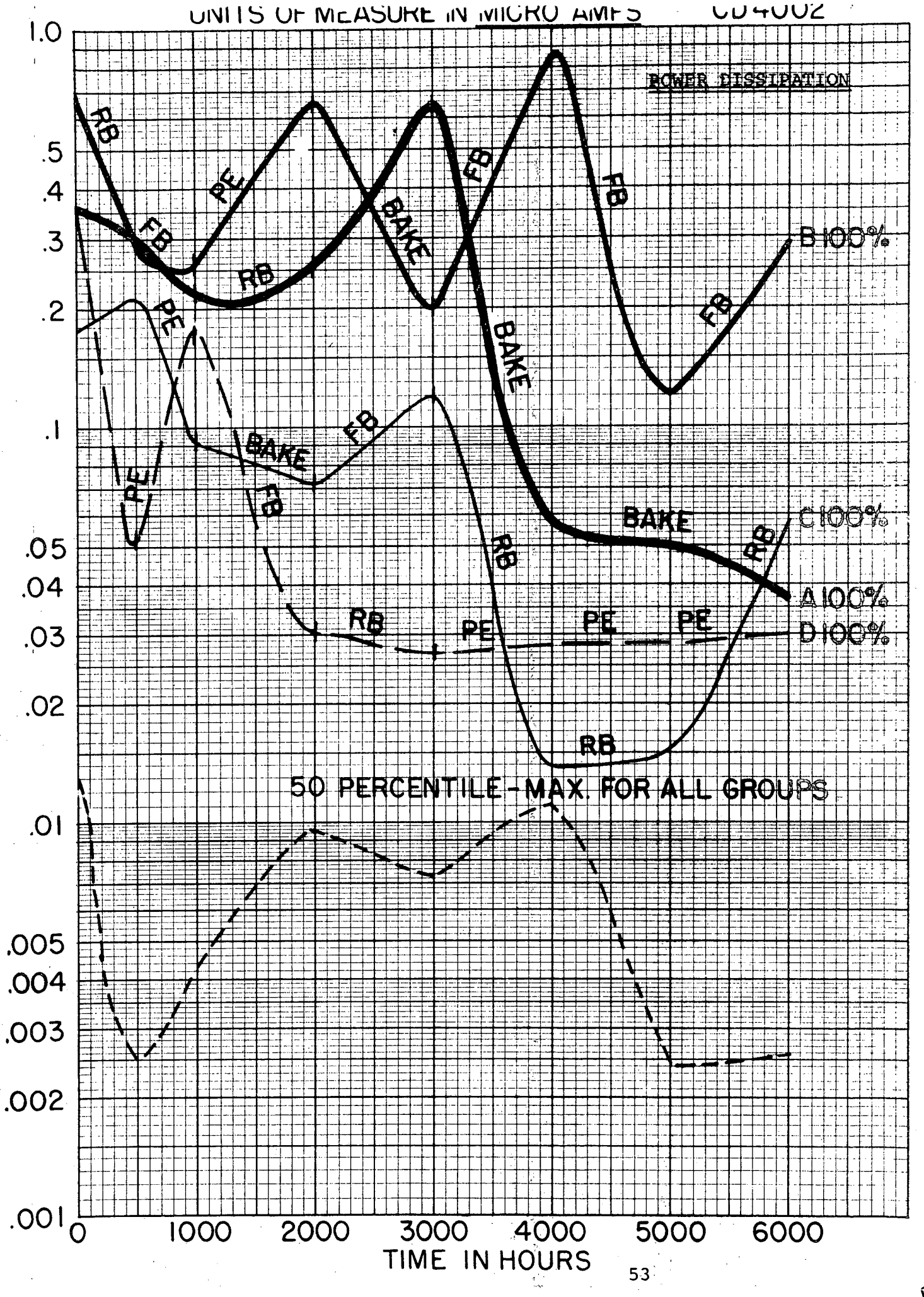


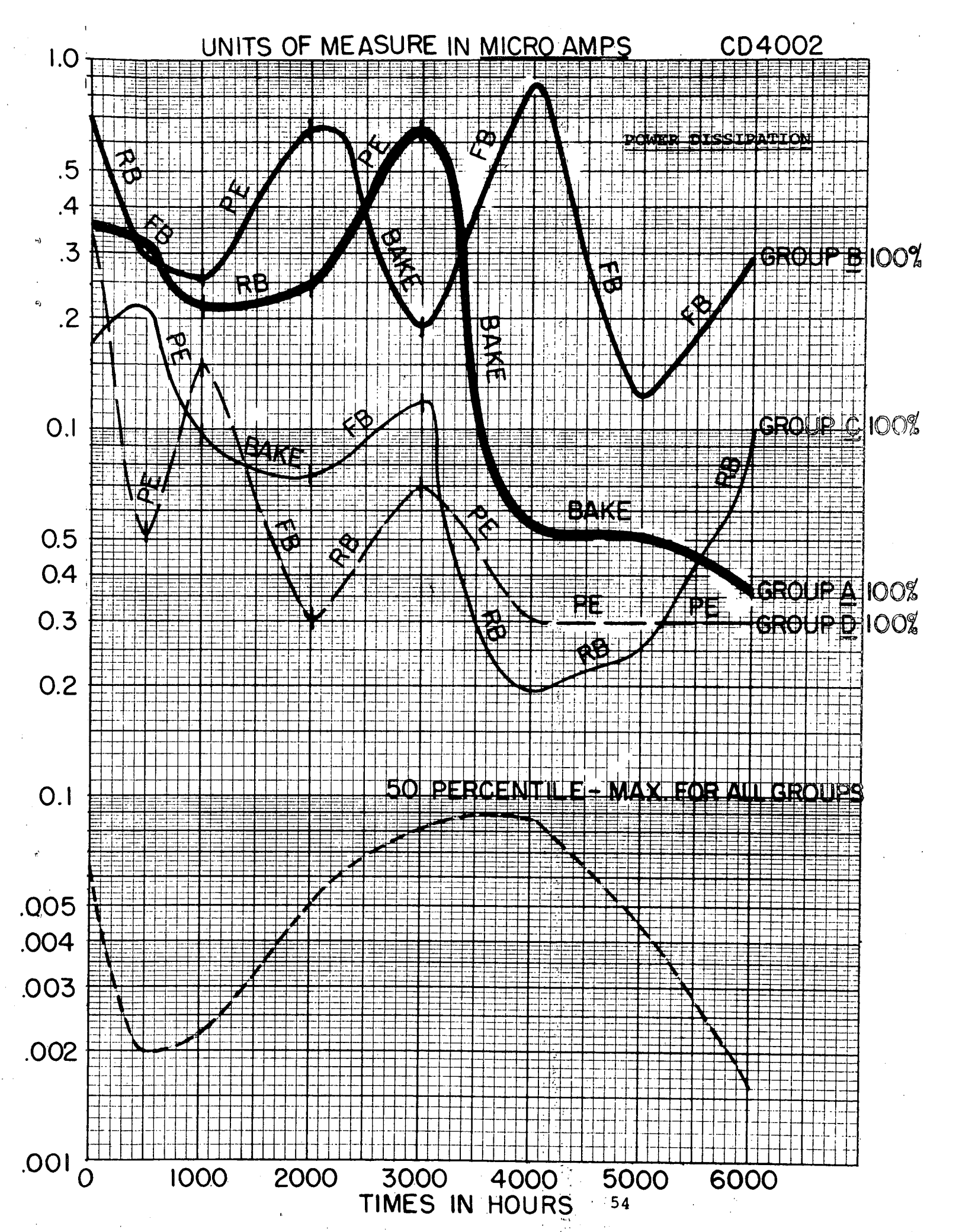
GROUP C



GROUP D




UNITS OF MEASURE IN MICRO AMPS
CD4002
POWER DISSIPATION
1.0
.5
.4
.3
.2
.1
.05
.04
.03
.02
.01
.005
.004
.003
.002
.001
RB
FB
PE
BAKE
B 100%
C 100%
A 100%
D 100%
50 PERCENTILE - MAX. FOR ALL GROUPS
0
1000
2000
3000
4000
5000
6000
TIME IN HOURS


UNITS OF MEASURE IN MICRO AMPS
CD4002
POWER DISSIPATION
1.0
.5
.4
.3
.2
0.1
0.5
0.4
0.3
0.2
0.1
.005
.004
.003
.002
.001
0
1000
2000
3000
4000
5000
6000
TIMES IN HOURS
RB
FB
PE
BAKE
GROUP B 100%
GROUP C 100%
GROUP A 100%
GROUP D 100%
50 PERCENTILE - MAX. FOR ALL GROUPS

DCA

APPENDIX E

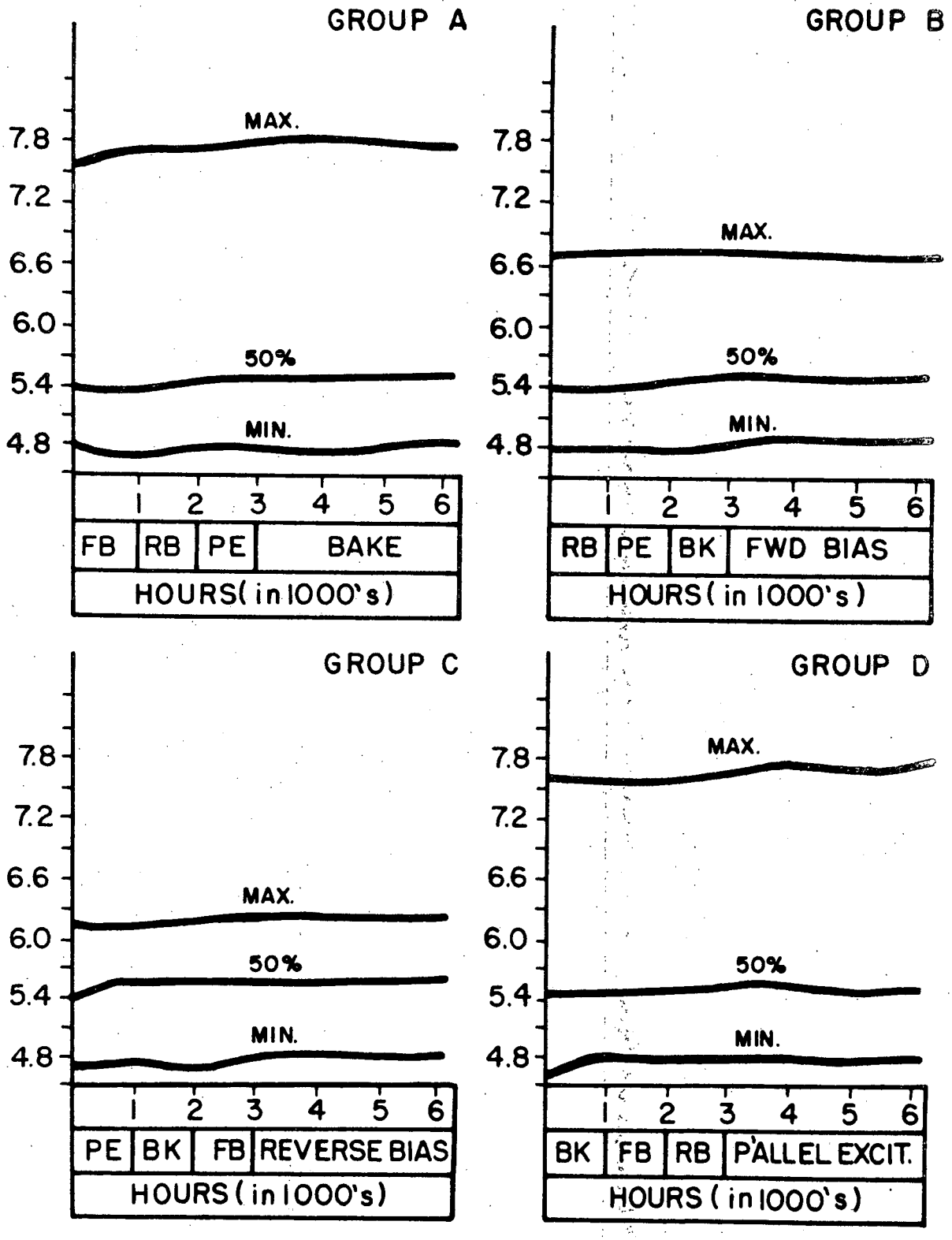
CD4003 DATA GRAPHS

The acceptable data is presented in graphical form. The axis for the graph has time in hours vs the parameter unit of measure.

The graphs of this appendix are a representative sample of each parameter and displays the minimum, mean and maximum value in centile form.

CD 4003 UNITS mA

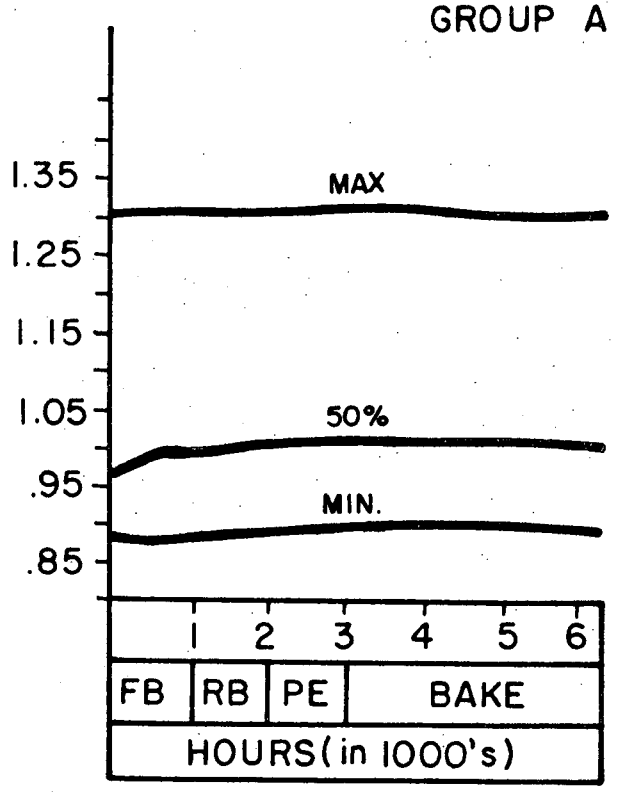
PARAMETER:--- Output Drive Capability
SYMBOL:------ IDS "P"
CONDITIONS:-- VDD = +10V, VGS = 10V, VDS = -3.8V
LIMITS:------ -1.3 mA minimum
NUMBER:------ 2



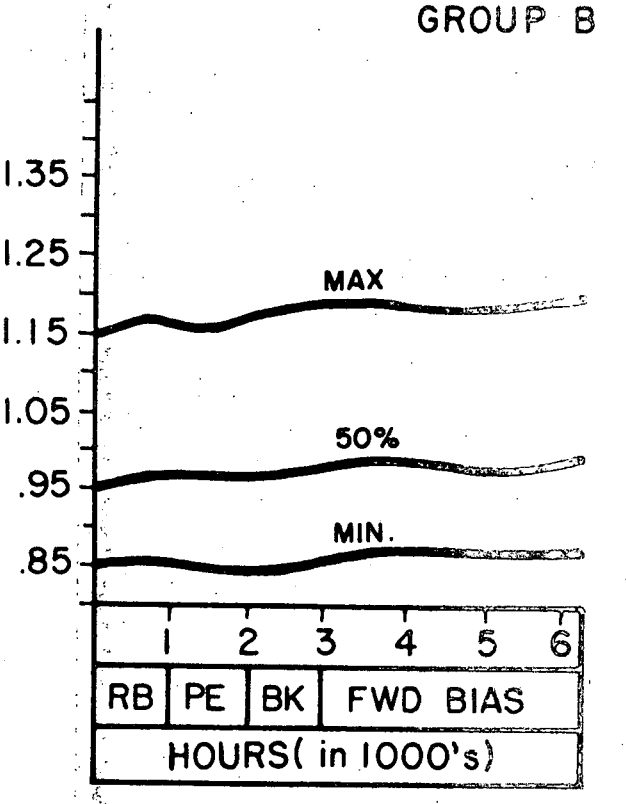
CD 4003 UNITS mA

PARAMETER:--- Output Drive Capability
SYMBOL:------ IDS "P"
CONDITIONS:-- VDD = 10V, VGS = 10V, VDS = -0.5V
LIMITS:------ -0.15 mA
NUMBER:----- 3

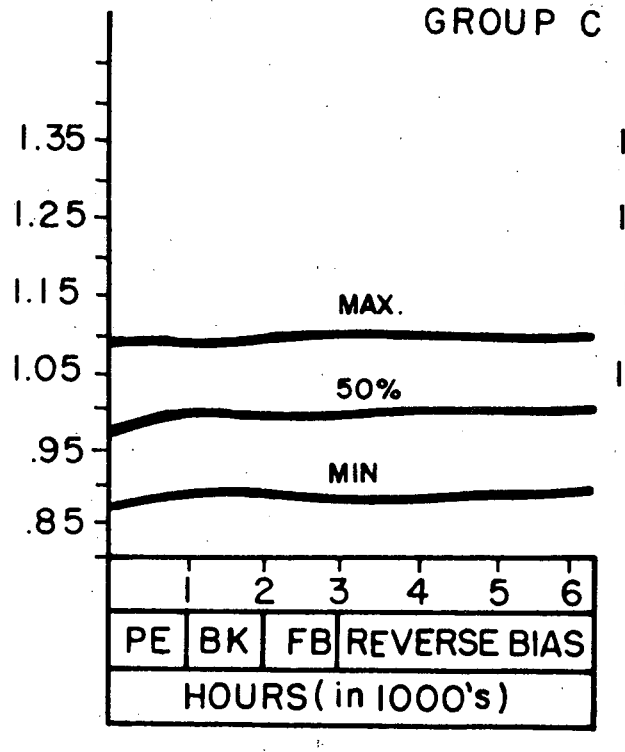
GROUP A



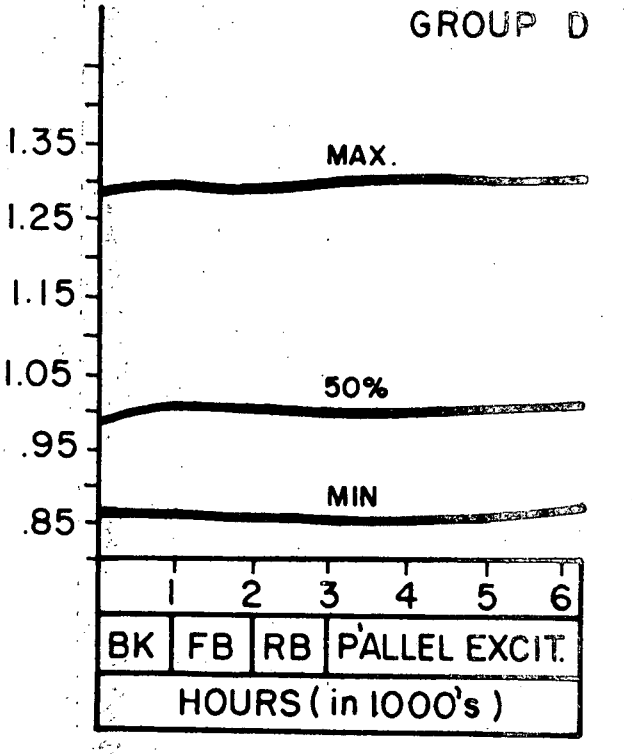
GROUP B



GROUP C

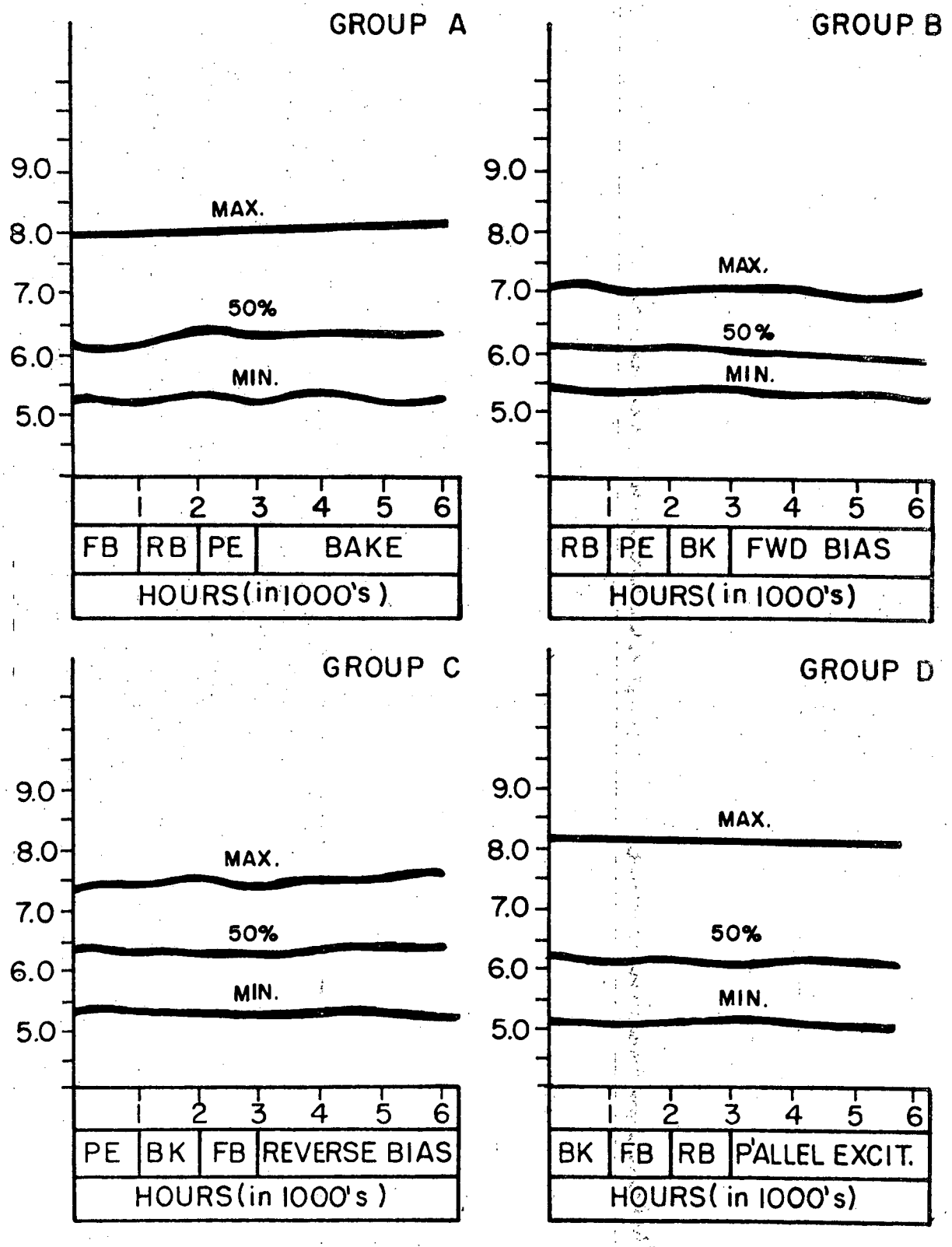


GROUP D



CD 4003 UNITS mA

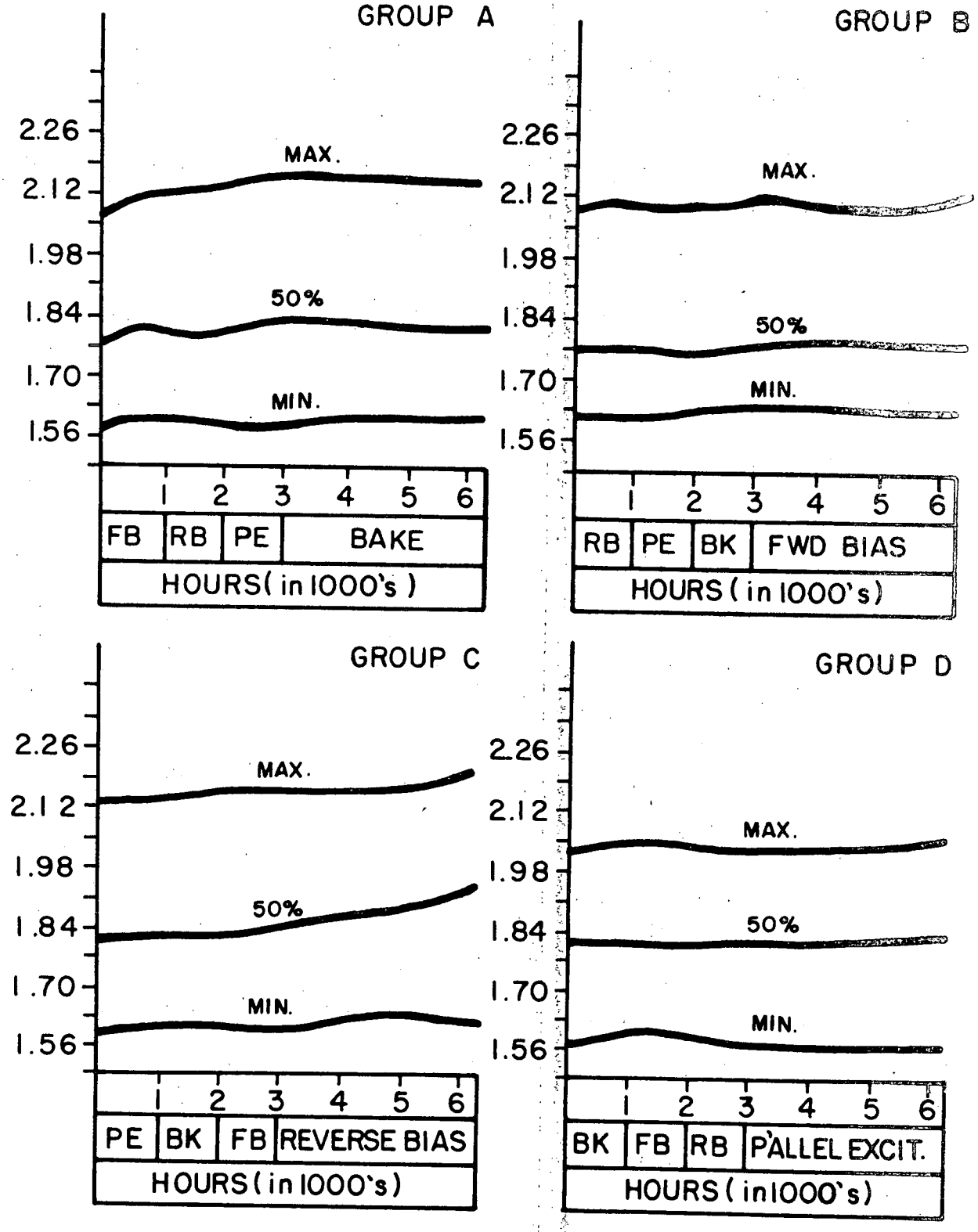
PARAMETER:--- Output Drive Capability
SYMBOL:------ IDS "N"
CONDITIONS:--- VDD = 10V, VGS = 10V, VDS = 3.0V
LIMITS:------ 2.0 mA minimum
NUMBER:------ 4



CD 4003

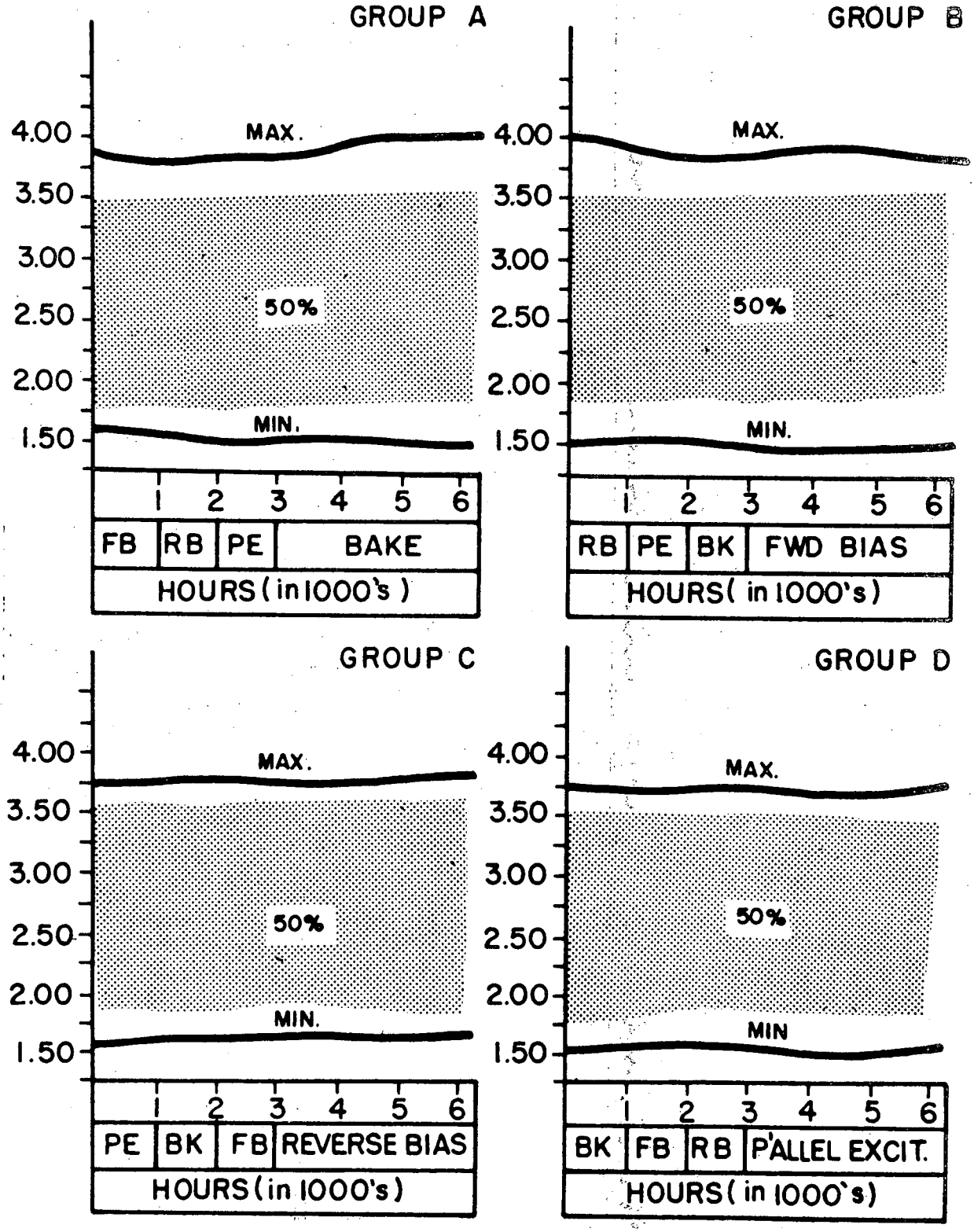
UNITS mA

PARAMETER:--- Output Drive Capability
SYMBOL:------ IDS "N"
CONDITIONS:--- VDD = 10V, VSG = 10V, VDS = 0.5V
LIMITS:------- 0.7 mA minimum
NUMBER:------ 5



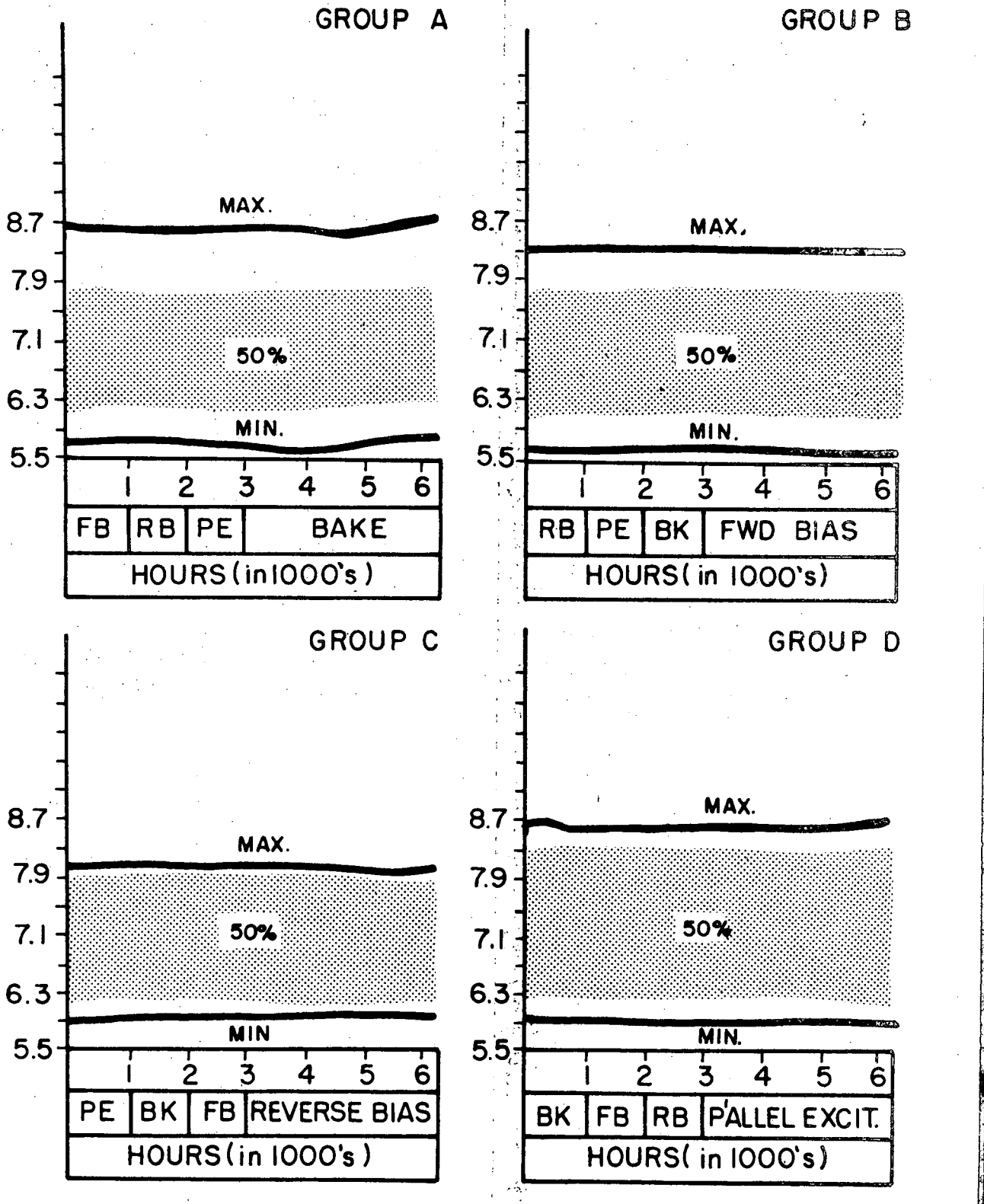
CD 4003 UNITS VOLTS

PARAMETER:--- Threshold Voltage
SYMBOL:------ Vth
CONDITIONS:--- VDD = 6.0V
LIMITS:------- 1.4 thru 4.5V
NUMBER:------- 6



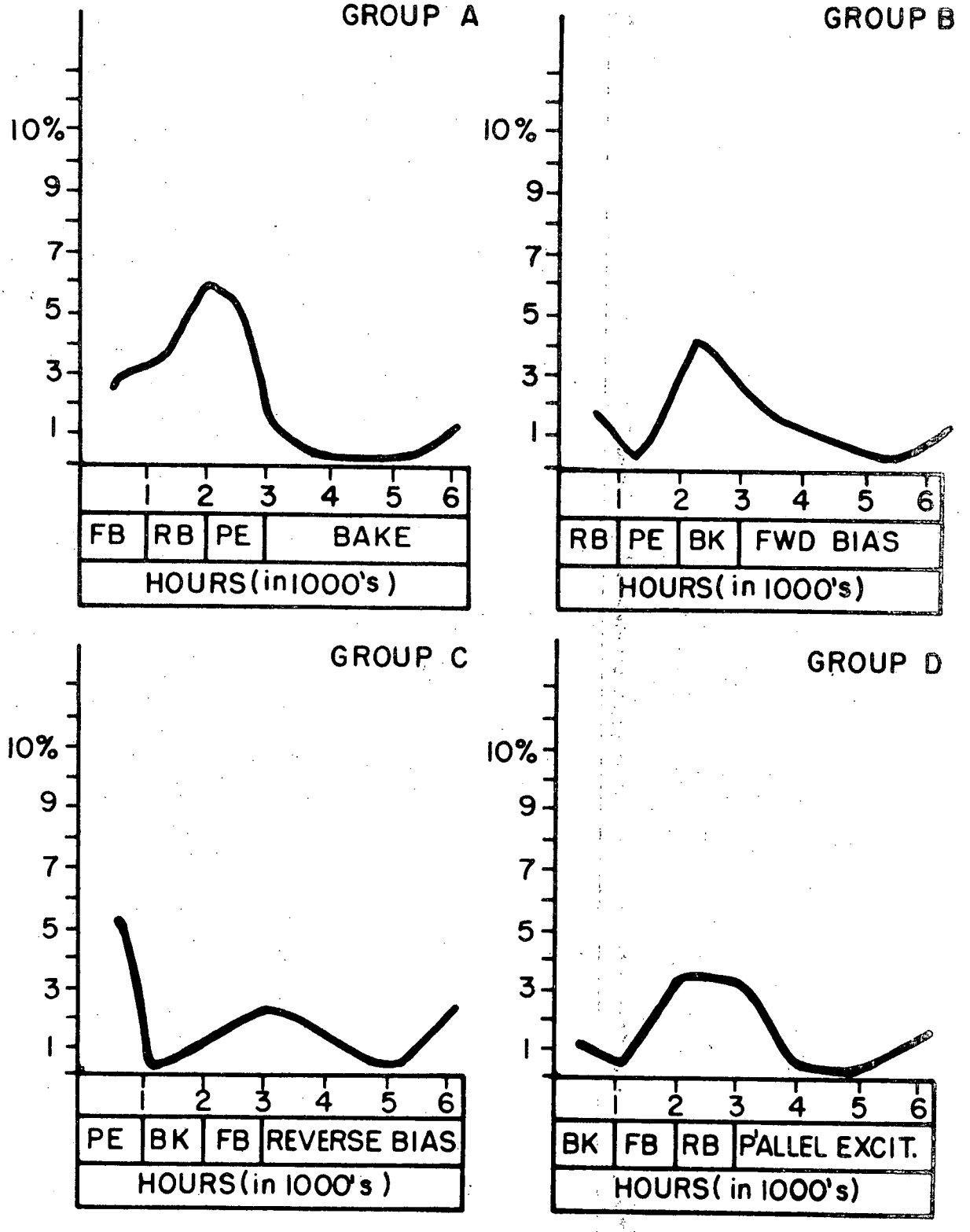
CD 4003 UNITS VOLTS

PARAMETER:--- Threshold Voltage
SYMBOL:------ Vth
CONDITIONS:--- VDD = 14V
LIMITS:------ 5.6 thru 9.7
NUMBER:------ 7



CD 4003 UNITS %

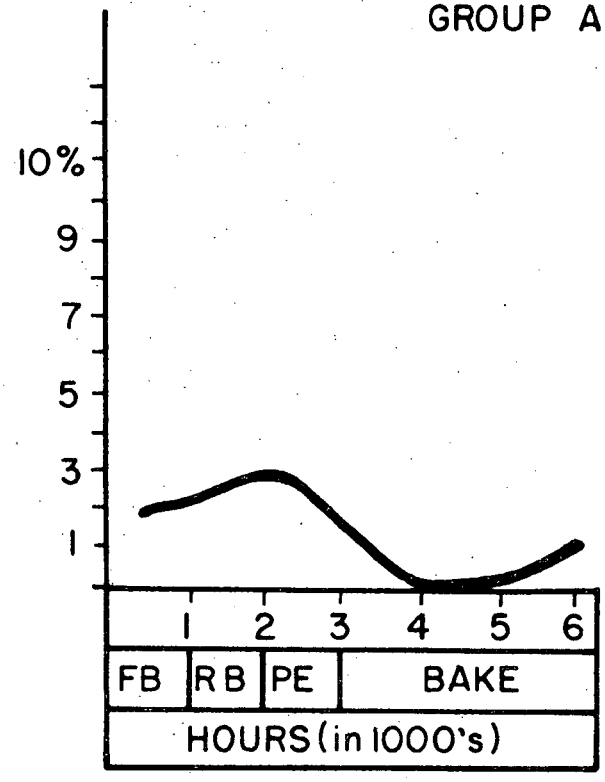
PARAMETER:--- Output Drive Capability
SYMBOL:------ IDS "P"
CONDITIONS:--- VDD = +10V, VGS = 10V, VDS = -3.8V
LIMITS:------ -1.3 mA minimum
NUMBER:------ 8



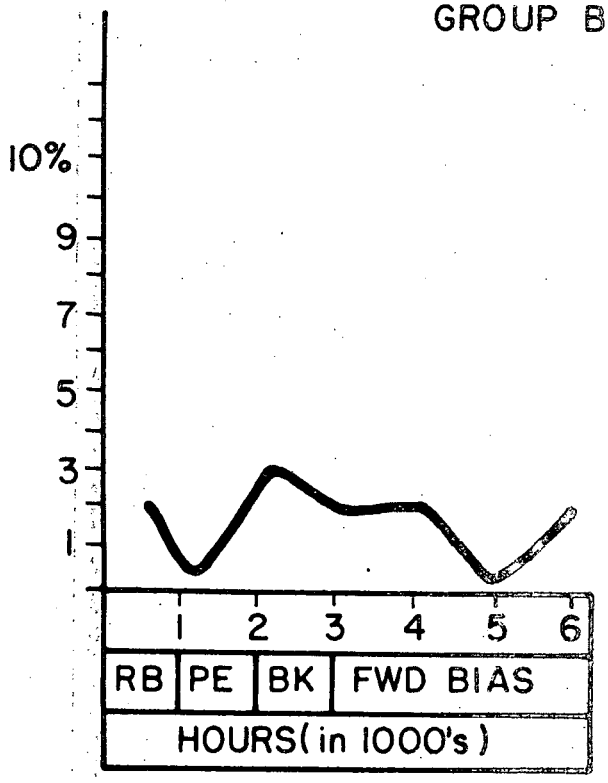
CD 4003 UNITS %

PARAMETER:--- Output Drive Capability
SYMBOL:------ IDS "P"
CONDITIONS:--- VDD = 10V, VGS = 10V, VDS = -0.5V
LIMITS:------- -0.15 mA
NUMBER:------ 9

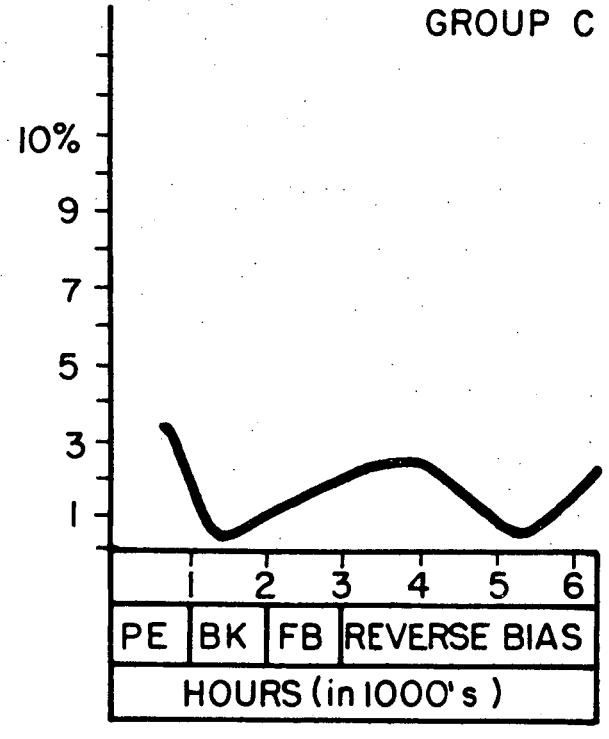
GROUP A



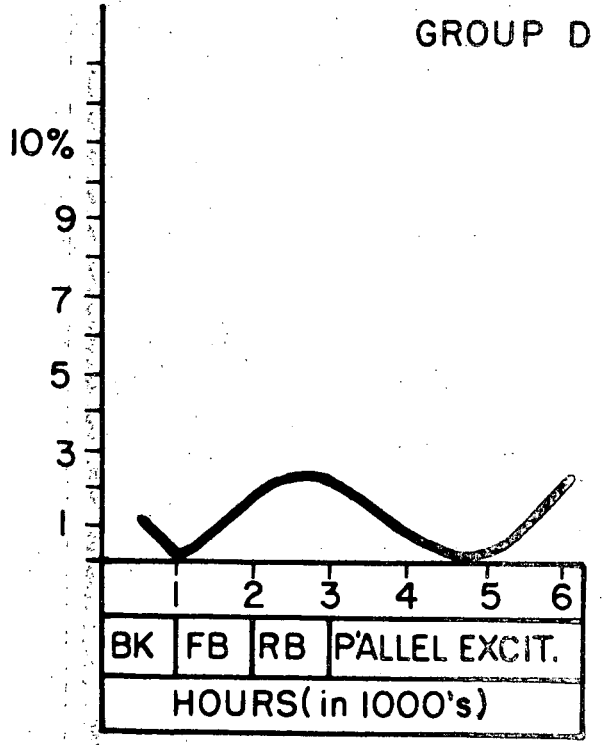
GROUP B



GROUP C

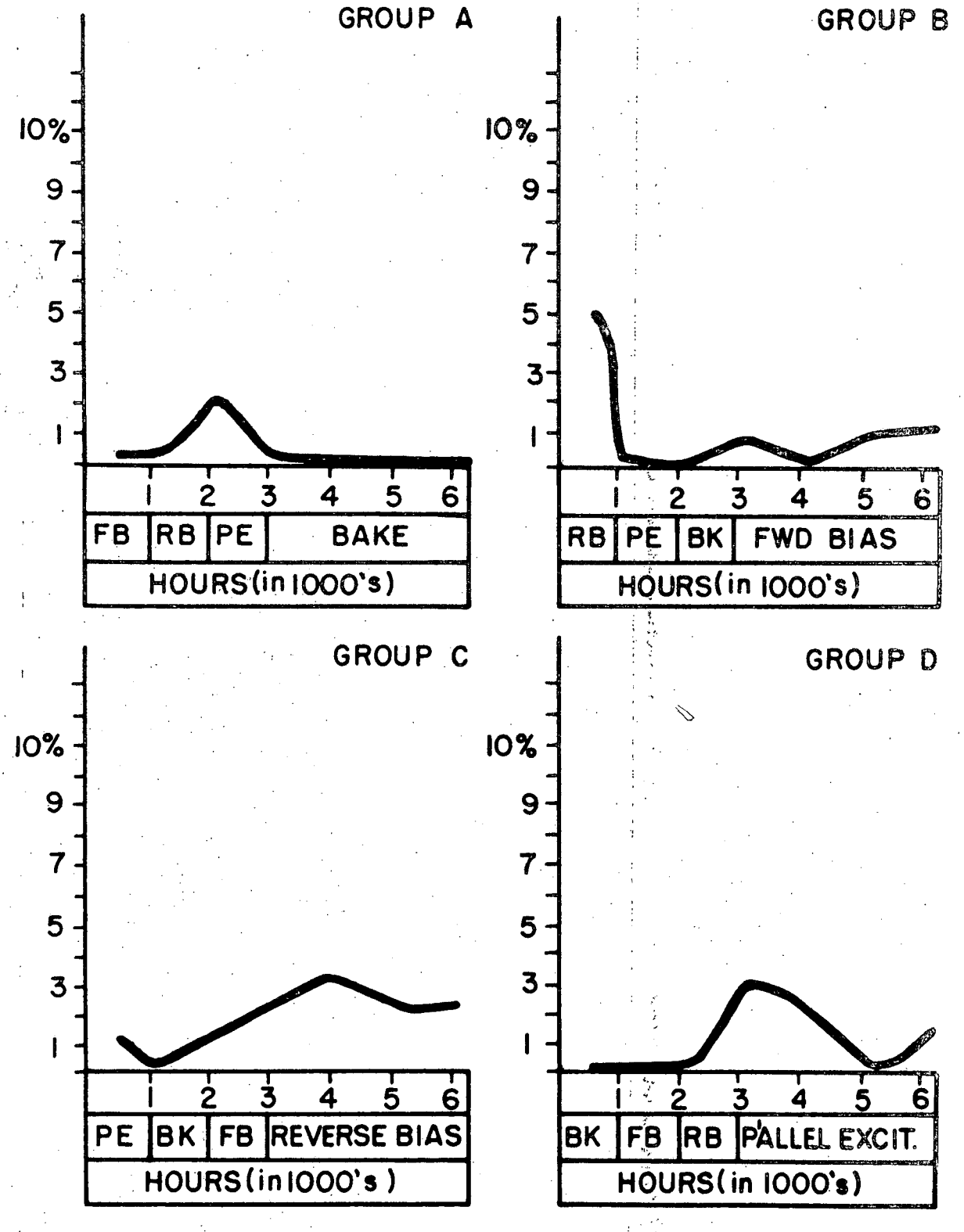


GROUP D



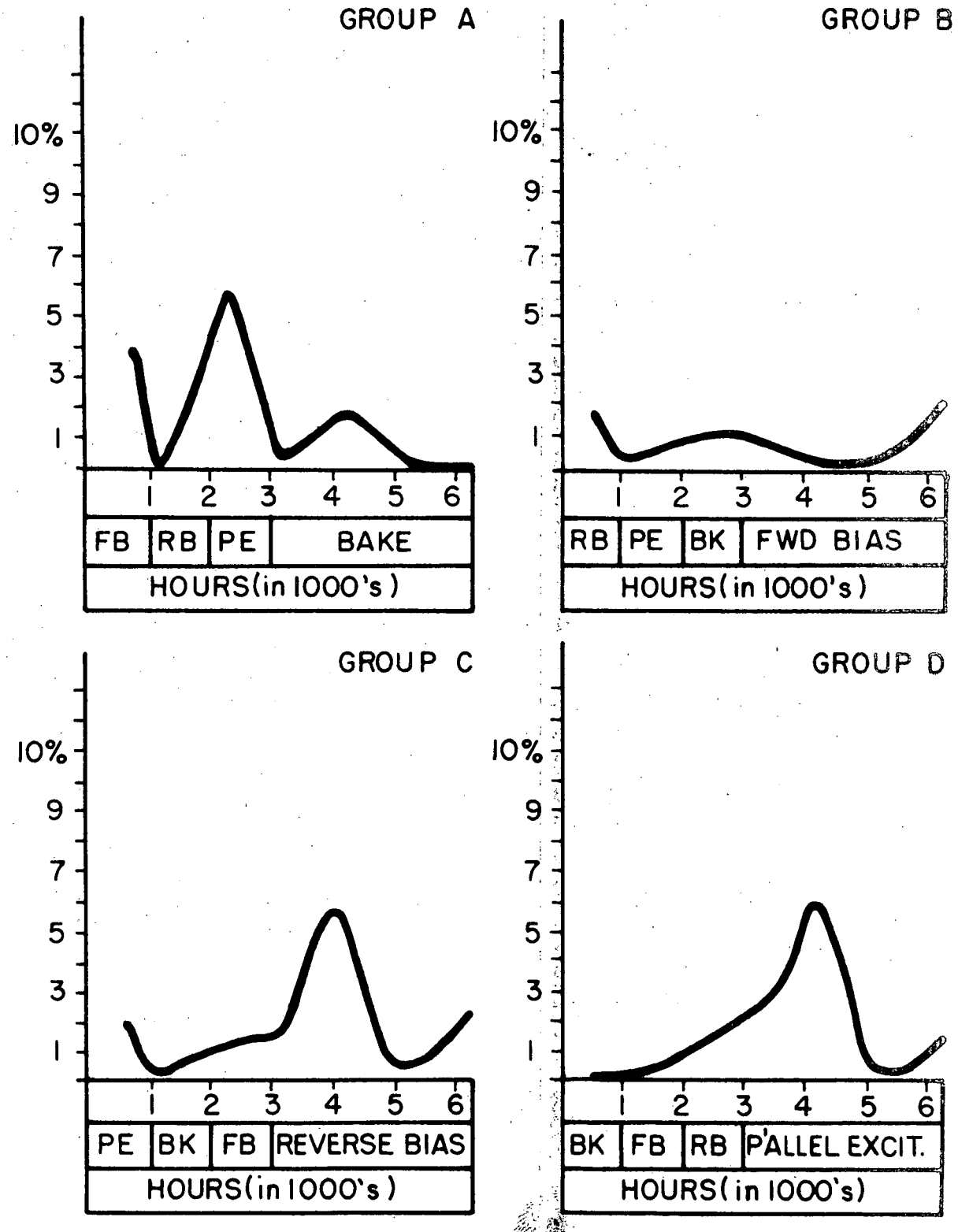
CD 4003 UNITS %

PARAMETER:--- Output Drive Capability
SYMBOL:------ IDS "N"
CONDITIONS:--- VDD = 10V, VGS = 10V, VDS = 3.0V
LIMITS:------- 2.0 mA minimum
NUMBER:------ 10



CD 4003 UNITS %

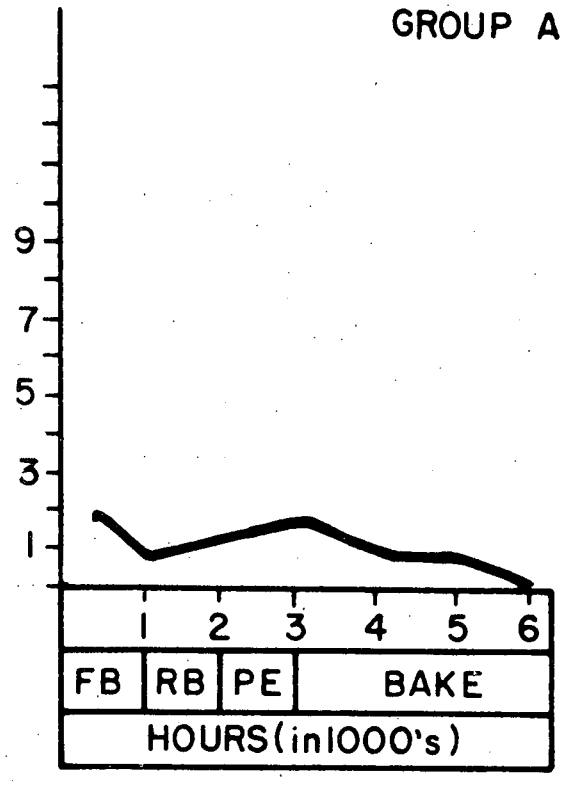
PARAMETER:--- Output Drive Capability
SYMBOL:------ IDS "N"
CONDITIONS:--- VDD = 10V, VSG = 10V, VDS = 0.5V
LIMITS:------- 0.7 mA minimum
NUMBER:------ 11

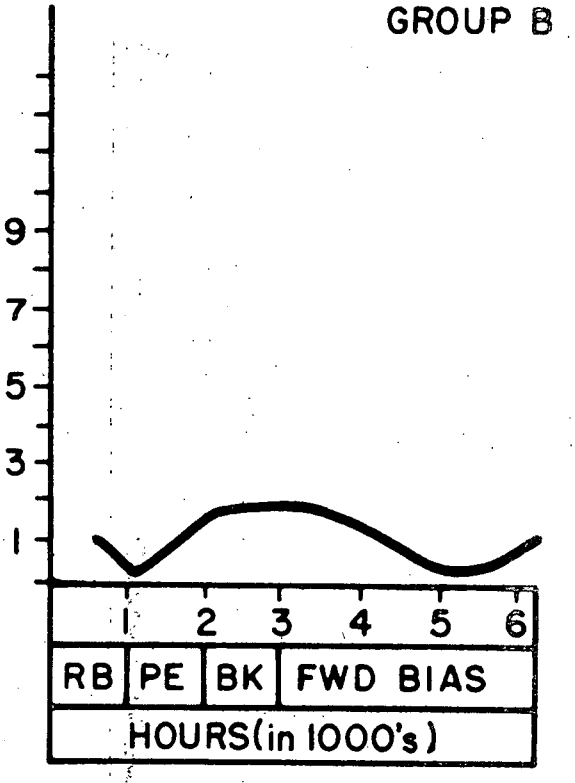


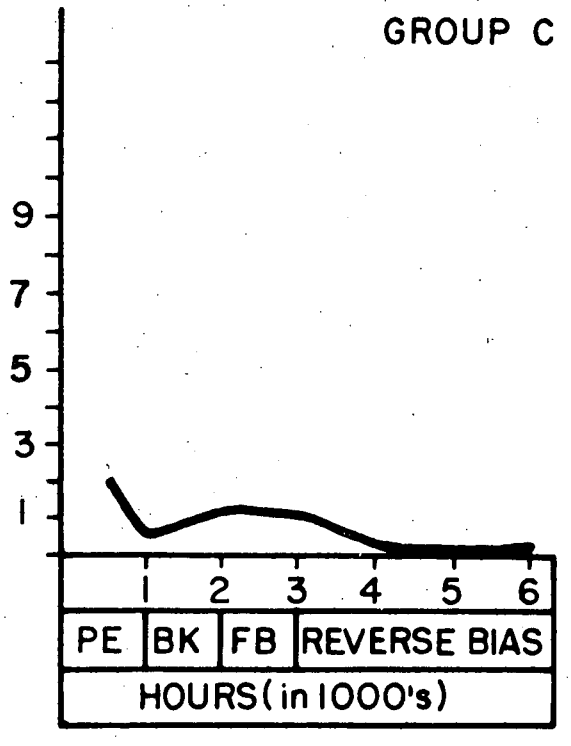
CD 4003

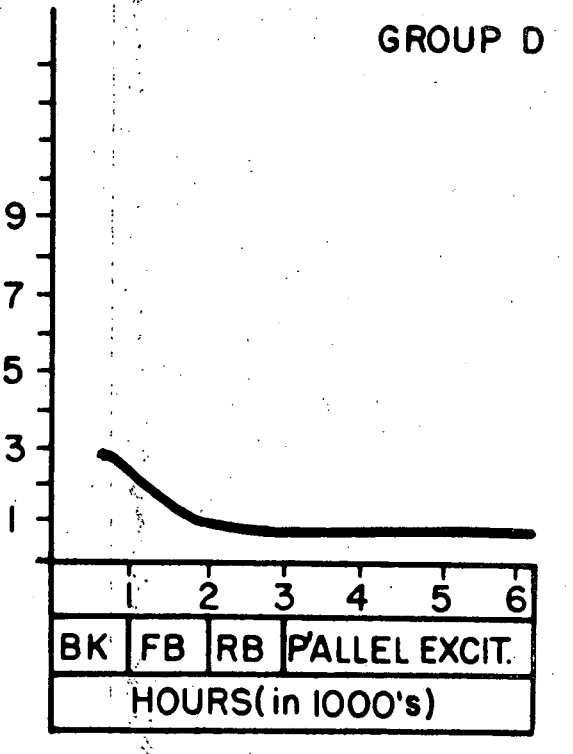
UNITS %

PARAMETER:--- Threshold Voltage
SYMBOL:------ Vth
CONDITIONS:--- VDD = 14V
LIMITS:------- 5.6 thru 9.7
NUMBER:------ 13







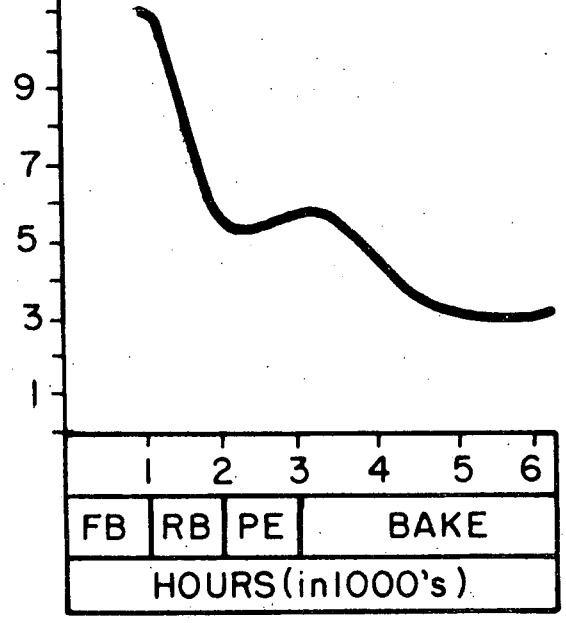


CD 4003

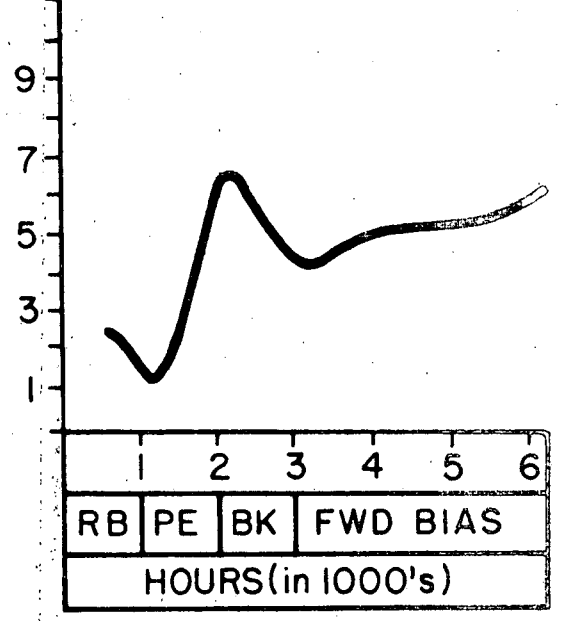
UNITS %

PARAMETER:--- Threshold Voltage
SYMBOL:------ Vth
CONDITIONS:--- VDD = 6.0V
LIMITS:------- 1.4 thru 4.5V
NUMBER:------ 12

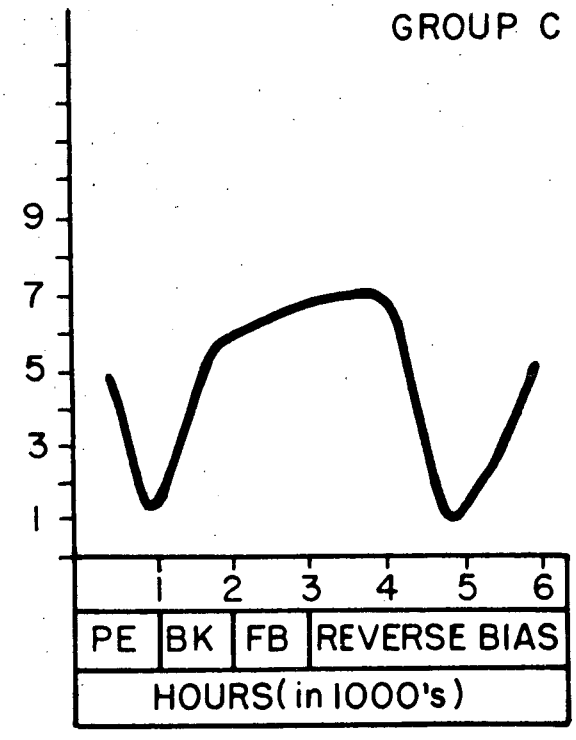
GROUP A



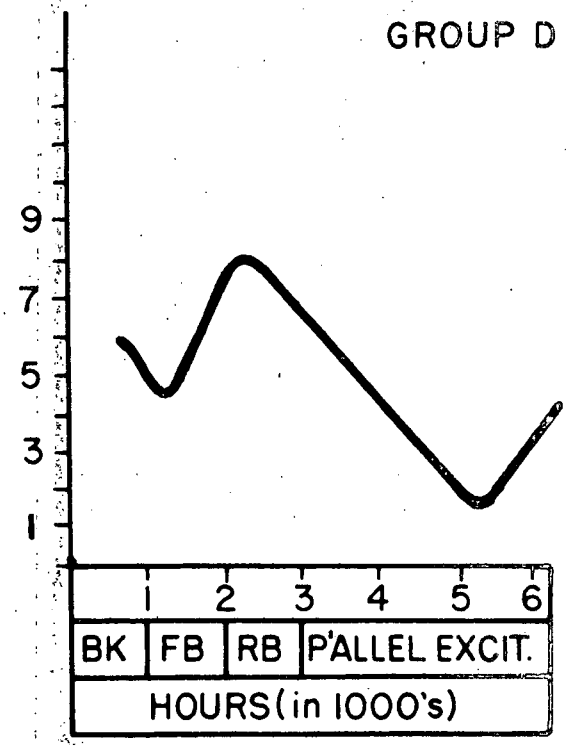
GROUP B



GROUP C

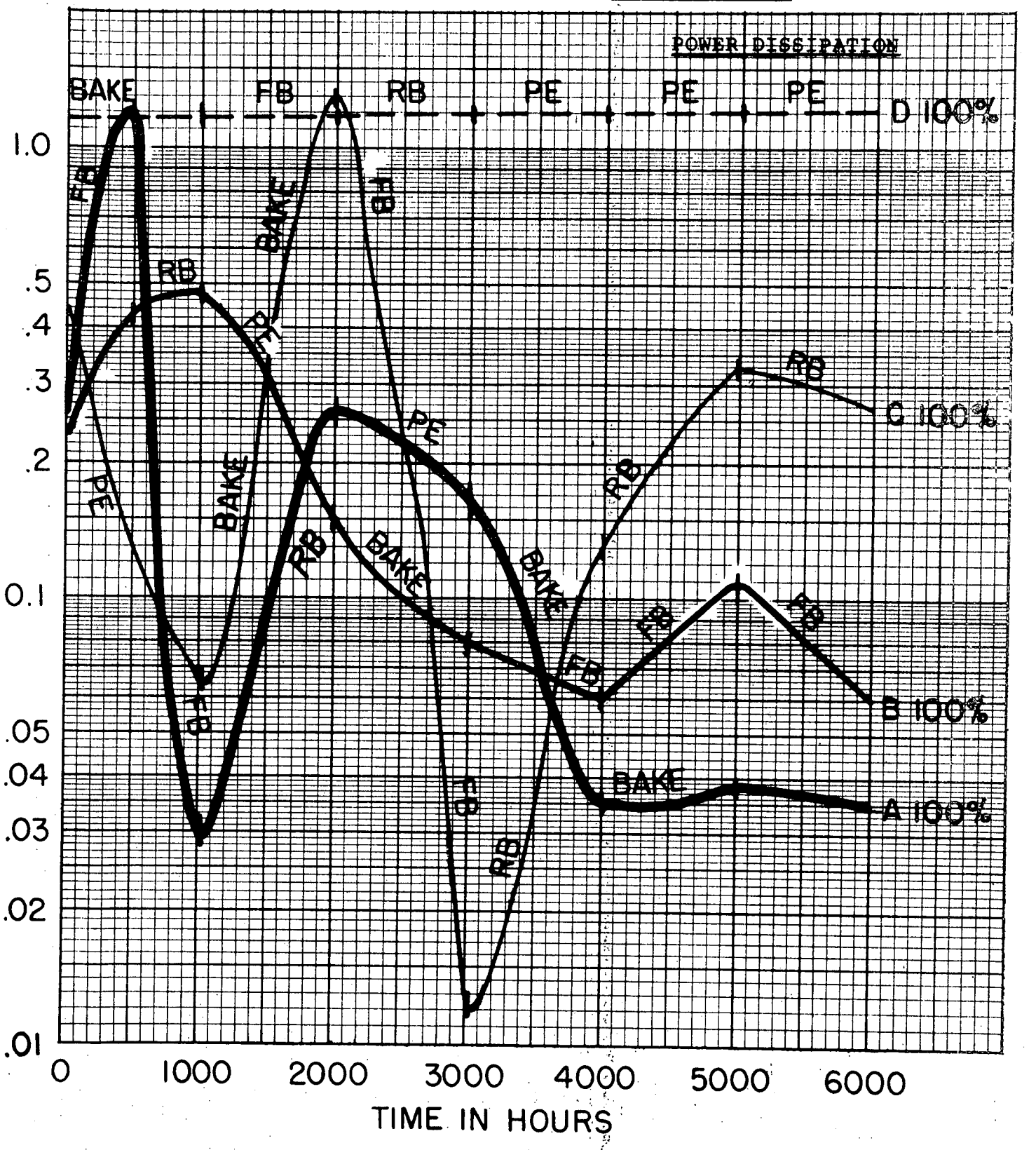


GROUP D



CD4003

UNITS OF MEASURE IN MICRO AMPS



DCA

APPENDIX F

CD4002

Tabulated Data on the Limit and Drift Failures

CONTRACT															
	SERIAL NUMBER		3306	3307	3317	3320	3322	3323	3324	3325	3326	3327			
	ARC LIFE TEST		N/A	N/A	PE	FB	N/A	N/A	N/A	N/A	N/A	N/A			
	PARAMETER		IPT	IPT	IPT	IPT	IPT	IPT	IPT	IPT	IPT	IPT			
	UNIT OF MEAS.		uA	uA	uA	uA	uA	uA	uA	uA	uA	uA			
	TYPE OF LIFE TEST	TIME POINT IN HOURS	LIMIT 0.10 MAX.	LIMIT 0.10 MAX.	LIMIT 0.10 MAX.	LIMIT 0.10 MAX.	LIMIT 0.10 MAX.	LIMIT 0.10 MAX.	LIMIT 0.10 MAX.	LIMIT 0.10 MAX.	LIMIT 0.10 MAX.	LIMIT 0.10 MAX.			
ARC	-	0	NO HISTORY		.000	.000	.001	.010	.001	.000	.001	.000			
	FB	36			.001	.000	.966	.122	.001	.162	.028	.047			
	See Life Test Above	168			.275	.000	PULLED								
		500			.155	.064									
		1000			>1.0	.093									
MSFC	-	0	.355	.107	.595	.070	.011	.085	.001	.105	.023	.037			
	FB	500	.310	.102	.002	.000	.002	.073	.062	.147	.032	.060			
	FB	1000	.212	.051	.041	.000	.033	.050	.081	.119	.058	.061			
	RB	2000	.185	.063	>1.6	.009	.070	.021	.248	.110	.122	>1.6			
	PE	3000	.020	.035	.615	.105	.503	.651	.604	.476	.278	.427			
	BAKE	4000	.055	.025	.000	.000	.000	.002	.051	.000	.002	.011			
	BAKE	5000	.008	.024	.000	.000	.000	.001	.051	.000	.002	.018			
	BAKE	6000	.007	.015	.000	.000	.000	.001	.037	.000	.001	.030			
COMMENTS:			Channel VDD to Pin 11	Channel VDD to Pin 12	Channel VDD to GND	Channel VDD to GND	Channel VDD to Pin 5	Channel VDD to GND	Channel VDD to GND	Channel VDD to GND	Channel VDD to GND	Channel VDD to GND			

NOTE: S/N 3315 - Failed catastrophically at measurement point 8 due to missing pin.

CD4002 LIMIT FAILURES - GROUP "A"

CONTRACT														
	SERIAL NUMBER		3342	3345	3346	3349	3350	3351						
	ARC LIFE TEST		FB	FB	RB	N/A	N/A	N/A						
	PARAMETER		IPT	IPT	IPT	IPT	IPT	IPT						
	UNIT OF MEAS.		uA	uA	uA	uA	uA	uA						
	TYPE OF LIFE TEST	TIME POINT IN HOURS	LIMIT 0.10 MAX.	LIMIT 0.10 MAX.	LIMIT 0.10 MAX.	LIMIT 0.10 MAX.	LIMIT 0.10 MAX.	LIMIT 0.10 MAX.						
ARC	-	0	.003	.004	.000	.007	.003	.011						
	RB	36	.278	.004	.000	.117	.424	.149						
	See Life Test Above	168	>1.0	.025	.011	PULLED								
		500	>1.0	.032	.093									
		1000	>1.0	.008	.198									
MSFC	-	0	1.332	.119	.045	.085	.674	.062						
	BAKE	500	.049	.036	.008	.225	.285	.068						
	BAKE	1000	.217	.047	.051	.246	.188	.124						
	FB	2000	1.523	.021	.192	.666	.670	.147						
	RB	3000	.002	.036	.028	.194	.001	.002						
	PE	4000	1.251	.009	.222	.777	.883	.087						
	PE	5000	.005	.022	.002	.036	.116	.008						
	PE	6000	.128	.037	.053	.204	.288	.010						
COMMENTS:			Channel VDD to GND	Channel VDD to GND	Channel VDD to GND	Channel VDD to GND	Channel VDD to GND	Channel VDD to GND						

NOTE: S/N 3348 - Failed catastrophically at measurement point 2 due to Gate 1 being open; at measurement point 1 this unit was out of manufacturer's specification.

CD4002 LIMIT FAILURES - GROUP "B"

CONTRACT														
	SERIAL NUMBER		3366	3368	3368	3368	3371	3377	3368	3368	3368	3373	3373	3368	3362
	ARC LIFE TEST		BAKE	RB	RB	RB	RB	N/A	RB	RB	RB	N/A	N/A	RB	BAKE
	PARAMETER		IPT	IPT	IPT_1	IPT_2	IPT	IPT	ITH 1	ITH 0	ITH 0	ITH 0	ITH 0	V1	IDS
	UNIT OF MEAS.		uA	uA	uA	uA	uA	uA	uA	uA	uA	uA	uA	V	mA
	TYPE OF LIFE TEST	TIME POINT IN HOURS	LIMIT 0.10 MAX.	LIMIT 0.10 MAX.	LIMIT 0.10 MAX.	LIMIT 0.10 MAX.	LIMIT 0.10 MAX.	LIMIT 0.10 MAX.	LIMIT 10 MAX.	LIMIT 10 MAX.	LIMIT 10 MAX.	LIMIT 10 MAX.	LIMIT 10 MAX.	LIMIT .01 MAX.	LIMIT 1.3 MIN.
ARC	-	0	.001	.019	.017	.023	.001	.059	0.01	0.02	0.01	5.35	4.17	.000	3.65
	RB	36	.001	.003	.001	.002	.000	.242	0.01	0.20	0.01	9.67	7.77	.000	3.70
	See Life Test Above	168	.000	.003	.001	.002	.002		0.01	0.08	0.02			.000	3.65
		500	.001	.002	.001	.002	.038	PULLED	0.01	0.06	0.01	PULLED		.000	3.73
		1000	.000	.003	.002	.002	.148		0.01	0.05	0.02			.000	3.74
MSFC	-	0	.000	.002	.001	.001	.051	.172	0.01	0.01	0.04	8.12	6.41	.000	3.69
	PE	500	.150	.003	.001	.002	.042	.215	0.01	0.01	0.03	9.34	7.47	.000	2.03
	PE	1000	.001	.004	.001	.003	.075	.094	0.03	0.00	0.38	4.01	3.14	.000	1.54
	BAKE	2000	.001	.003	.001	.002	.000	.074	0.03	0.00	0.02	3.75	2.94	.000	3.02
	FB	3000	.000	.002	.001	.001	.119	.091	0.02	0.00	0.02	3.64	2.86	.000	1.27
	RB	4000	.000	>1.6	>1.6	>1.6	.014	.015	14.50	37.15	48.89	63.92	56.59	.011	1.90
	RB	5000	.000	>1.6	>1.6	>1.6	.000	.008	19.25	50.23	61.71	114.24	103.4	.014	2.02
	RB	6000	.000	.272	.226	.459	.002	.007	23.10	60.92	74.61	153.99	141.5	.017	2.12
COMMENTS:			Channel VDD to GND	Total	Gate 1	Gate 2	Channel VDD to GND	Channel VDD to GND	Input Leakage Problems at Marginal Levels			Input Leakage Problem at Marginal Levels		Marginal Output "N" Channel Gate 2	Marginal Output "N" Channel Gate 1
				Various Channels											

NOTES: S/N 3363 - This unit survived the ARC Life Test but was received in catastrophic condition for the MSFC Life Test.

S/N 3374 - Failed catastrophically at measurement point 6.

S/N 3376 - Failed catastrophically at measurement point 6.

S/N 3358 - Failed catastrophically at measurement point 2.

CD4002 LIMIT FAILURES - GROUP "C"

CONTRACT	SERIAL NUMBER		3380	3398	3401											
	ARC LIFE TEST		N/A	N/A	N/A											
	PARAMETER		IPT	IPT	IPT											
	UNIT OF MEAS.		uA	uA	uA											
	TYPE OF LIFE TEST	TIME POINT IN HOURS	LIMIT 0.10 MAX.	LIMIT 0.10 MAX.	LIMIT 0.10 MAX.											
ARC	-	0	NO HISTORY	.025	.003											
	RB	36		.559	.120											
	See Life Test Above	168		PULLED												
		500														
		1000														
MSFC	-	0	.002	.348	.106											
	BAKE	500	.006	.042	.049											
	BAKE	1000	.150	.018	.002											
	FB	2000	.000	.017	.000											
	RB	3000	.001	.045	.009											
	PE	4000	.000	.020	.000											
	PE	5000	.000	.017	.000											
	PE	6000	.000	.016	.000											
COMMENTS:			Channel VDD to Pin 3	Channel VDD to GND	Channel VDD to GND											

NOTE: S/N 3396 - This unit survived the ARC Life Test with some drift but was received in catastrophic condition for MSFC Life Test.

CD4002 LIMIT FAILURE - GROUP "D"

CONTRACT														
SERIAL NUMBER			3310	3310	3312	3312	3316	3316	3311	3321	3318	3318	3318	3305	3305
ARC LIFE TEST			PE	PE	PE	PE	FB	FB	PE	FB	PE	PE	PE	N/A	N/A
PARAMETER			Ith0	Ith0	Ith0	Ith0	Ith0	Ith0	Ipt	Ipt	Vnm	Ids	Ids	Idsn	Idsn
UNIT OF MEAS.			uA	uA	uA	uA	uA	uA	uA	uA	V	mA	mA	mA	mA
	TYPE OF LIFE TEST	TIME POINT IN HOURS	DRIFT + 0.1 MAX.	DRIFT + 0.1 MAX.	DRIFT + 0.1 MAX.	DRIFT + 0.1 MAX.	DRIFT + 0.1 MAX.	DRIFT + 0.1 MAX.	DRIFT +.01 MAX.	DRIFT +.01 MAX.	DRIFT + 5% MAX.	DRIFT + 5% MAX.	DRIFT + 5% MAX.	DRIFT + 5% MAX.	DRIFT + 5% MAX.
ARC	-	0	0.02	0.02	0.03	0.02	0.03	0.03	.000	.002	4.64	4.03	4.54	NO HISTORY	
	RB	36	0.02	0.02	0.05	0.03	0.10	0.10	.003	.003	4.64	4.05	4.51		
	See Life Test Above	168	0.02	0.02	0.05	0.03	0.02	0.02	.000	.061	4.64	3.80	4.39		
		500	0.02	0.02	0.05	0.03	0.02	0.01	.000	.064	4.55	2.29	3.90		
		1000	0.03	0.02	0.08	0.04	0.02	0.02	.001	.014	4.06	1.76	3.41		
MSFC	-	0	0.02	0.00	0.06	0.03	0.00	0.00	.000	.002	3.90	1.61	3.52	4.79	5.87
	FB	500	0.00	0.00	0.03	0.02	0.00	0.00	.000	.001	3.92	1.95	3.89	4.58	5.77
	FB	1000	0.01	0.01	0.04	0.02	0.01	0.01	.000	.002	3.96	2.18	3.96	4.48	5.65
	RB	2000	0.01	0.01	0.09	0.03	0.01	0.01	.001	.002	4.03	2.14	3.97	5.25	6.43
	PE	3000	0.02	0.02	0.14	0.05	0.03	0.04	.001	.035	4.51	3.70	4.21	5.11	6.19
	BAKE	4000	0.27	0.35	0.14	0.21	1.05	1.29	.020	.001	4.13	2.33	4.11	4.60	6.35
	BAKE	5000	0.37	0.47	0.25	0.71	1.65	2.00	.000	.001	4.18	2.43	4.15	4.60	6.34
	BAKE	6000	0.33	0.42	0.38	1.49	1.59	2.04	.000	.002	4.21	2.52	4.18	4.57	6.32
COMMENTS:			Unstable Inputs With Marginal Low Levels			Unstable Inputs With Marginal Low Levels			Channel from VDD to GND	Channel from VDD to Pin 5	Channel from Gate 1 to GND	Output "P" Channel Unstable on Both Gates		Output "N" Channel Unstable on Both Gates	

CD4002 DRIFT REJECTS - GROUP "A"

CONTRACT														
	SERIAL NUMBER		3328	3328	3340	3344	3334	3338	3343	3344	3347	3352			
	ARC LIFE TEST		N/A	N/A	RB	FB	FB	FB	FB	FB	N/A	N/A			
	PARAMETER		Ith0	Ith0	Ith0	Ith0	Ipt	Ipt	Ipt	Ipt	Ipt	Ipt			
	UNIT OF MEAS.		uA	uA	uA	uA	uA	uA	uA	uA	uA	uA			
	TYPE OF LIFE TEST	TIME POINT IN HOURS	DRIFT + 0.1 MAX.	DRIFT + 0.1 MAX.	DRIFT + 0.1 MAX.	DRIFT + 0.1 MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.			
ARC	-	0	NO HISTORY		0.01	0.01	.003	.000	.000	.013	.000	.000			
	RB	36			0.01	0.01	.003	.000	.000	.004	.060	.029			
	See Life Test Above	168			0.01	0.01	.013	.001	.000	.003	PULLED				
		500			0.01	0.01	.005	.001	.017	.003					
		1000			0.02	0.02	.004	.001	.042	.016					
MSFC	-	0	2.46	2.58	0.00	3.46	.057	.001	.001	.042	.044	.000			
	RB	500	2.40	2.53	0.00	0.13	.009	.000	.000	.027	.001	.000			
	RB	1000	2.57	2.76	0.01	0.05	.007	.000	.001	.022	.003	.000			
	PE	2000	2.67	2.98	0.01	0.06	.004	.017	.017	.005	.009	.002			
	BAKE	3000	2.27	3.75	0.19	0.02	.006	.000	.000	.019	.000	.000			
	FB	4000	2.36	4.74	0.21	0.04	.020	.042	.010	.006	.008	.030			
	FB	5000	2.37	4.21	0.15	0.03	.006	.000	.000	.004	.000	.000			
	FB	6000	2.28	4.28	0.18	0.04	.012	.000	.002	.003	.000	.000			
COMMENTS:			Unstable Inputs With Marginal Low Levels		Gate 1 Unstable with Low marginal levels	Gate 2 Unstable with Low marginal levels	Channel from VDD to GND	Channel from VDD to GND	Channel from VDD to GND	Channel Gate 1 to GND	Channel from VDD to GND	Channel from VDD to GND			

CD4002 DRIFT REJECTS - GROUP "B"

CONTRACT														
	SERIAL NUMBER		3359	3359	3360	3361	3369	3372	3375	3370	3370	3370			
	ARC LIFE TEST		RB	RB	RB	RB	RB	RB	N/A	RB	RB	RB			
	PARAMETER		Ith0	Ith0	Ith0	Ith0	Ipt	Ipt	Ipt	Ids	Ids	Vnm			
	UNIT OF MEAS.		uA	uA	uA	uA	uA	uA	uA	mA	mA	V			
	TYPE OF LIFE TEST	TIME POINT IN HOURS	DRIFT + .1 MAX.	DRIFT + .1 MAX.	DRIFT + .1 MAX.	DRIFT + .1 MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.	DRIFT + 5% MAX.	DRIFT + 5% MAX.	DRIFT + 5% MAX.			
ARC	-	0	0.01	0.01	0.03	0.01	.000	.002	.001	4.37	4.56	4.72			
	RB	36	0.01	0.02	0.02	0.02	.006	.002	.148	4.38	4.58	4.71			
	See	168	0.01	0.02	0.03	0.02	.101	.002		4.26	4.48	4.69			
	Life	500	0.01	0.01	0.03	0.02	.028	.006	PULLED	4.25	4.50	4.68			
	Test	1000	0.01	0.02	0.03	0.02	.004	.032		4.14	4.44	4.62			
	Above														
MSFC	-	0	0.00	0.00	0.02	0.00	.001	.002	.001	4.16	4.42	4.63			
	PE	500	0.00	0.00	0.02	0.00	.000	.002	.001	4.26	4.50	4.68			
	PE	1000	0.01	0.01	0.02	0.01	.000	.002	.001	4.15	4.44	4.66			
	BAKE	2000	0.01	0.01	0.02	0.01	.000	.002	.018	4.28	4.50	4.70			
	FB	3000	0.01	0.01	0.01	0.01	.023	.020	.000	4.62	4.13	4.21			
	RB	4000	0.57	0.17	0.12	2.11	.000	.002	.002	4.13	4.42	4.33			
	RB	5000	0.43	0.19	0.14	3.85	.000	.002	.001	4.12	4.41	4.55			
	RB	6000	0.60	0.34	0.27	4.99	.000	.002	.001	4.16	4.47	4.55			
COMMENTS:			Unstable Inputs with Marginal Low Levels		Channel from Gate 2 to GND	Channel from Gate 1 to GND	Channel from VDD to GND	Channel from VDD to GND	Channel from VDD to Pin 12	Channel from VDD to GND	Channel from VDD to GND	Channel from Gate 1 to GND			

CD4002 DRIFT REJECTS - GROUP "C"

CONTRACT														
	SERIAL NUMBER		3379	3379	3383	3383	3389	3389	3393	3389	3393	3394	3399	3402	
	ARC LIFE TEST		N/A	N/A	N/A	N/A	BAKE	BAKE	RB	BAKE	RB	RB	N/A	N/A	
	PARAMETER		Ith0	Ith0	Ith0	Ith0	Ith0	Ith0	Ith0	Ipt	Ipt	Ipt	Ipt	Ipt	
	UNIT OF MEAS.		uA	uA	uA	uA	uA	uA	uA	uA	uA	uA	uA	uA	
	TYPE OF LIFE TEST	TIME POINT IN HOURS	DRIFT + .1 MAX.	DRIFT + .1 MAX.	DRIFT + .1 MAX.	DRIFT + .1 MAX.	DRIFT + .1 MAX.	DRIFT + .1 MAX.	DRIFT + .1 MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.	
ARC	-	0	NO HISTORY				0.04	0.04	0.01	.030	.003	.000	.000	.001	
	RB	36					0.06	0.19	0.01	.029	.003	.000	.695	.033	
	See Life Test Above	168					0.04	0.04	0.21	.032	.199	.091	PULLED		
		500					0.04	0.04	0.21	.029	.200	.268			
		1000					0.04	0.04	0.14	.029	.133	.232			
MSFC	-	0	1.06	1.07	2.28	2.61	0.03	0.03	0.05	.031	.056	.014	.000	.031	
	BAKE	500	.82	.83	1.89	2.15	0.03	0.03	0.00	.030	.003	.000	.000	.010	
	BAKE	1000	.83	.83	1.87	2.11	0.03	0.03	0.01	.033	.004	.000	.000	.000	
	FB	2000	.80	.80	1.85	2.07	0.03	0.03	0.00	.032	.004	.000	.001	.000	
	RB	3000	1.07	1.08	2.47	2.91	0.33	0.81	2.56	.050	.004	.001	.070	.000	
	PE	4000	.94	.96	2.11	2.89	0.14	0.33	0.10	.032	.003	.000	.024	.000	
	PE	5000	.99	1.04	2.26	3.20	0.12	0.28	0.14	.032	.003	.000	.000	.000	
	PE	6000	.91	.96	2.13	3.15	0.10	0.23	0.13	.029	.003	.000	.000	.000	
COMMENTS:			Unstable Inputs With Marginal Low Levels		Unstable Inputs With Marginal Low Levels		Unstable Inputs With Marginal Low Levels		Gate 2 Unstable With Marginal Low Levels	Channel from VDD to GND	Channel from VDD to GND	Channel from VDD to Pin 5	Channel from VDD to GND	Channel from VDD to GND	

CD4002 DRIFT REJECTS - GROUP "D"

DCA

APPENDIX G

CD4003

Tabulated Data on the
Limit and Drift Failures

CONTRACT																
	SERIAL NUMBER		3422													
	ARC LIFE TEST		N/A													
	PARAMETER		VtH-3													
	UNIT OF MEAS.		VOLT													
	TYPE OF LIFE TEST	TIME POINT IN HOURS	LIMIT 5.6 thru 9.7													
ARC	-	0	5.62													
	FB	36	5.58													
	See Life Test Above	168 500 1000	PULLED													
MSFC	-	0	5.61													
	FB	500	5.61													
	FB	1000	5.61													
	RB	2000	5.56													
	PE	3000	5.54													
	BAKE	4000	5.55													
	BAKE	5000	5.59													
	BAKE	6000	5.61													
COMMENTS:			Marginal													

CD4003 LIMIT REJECT - GROUP "A"

CONTRACT															
	SERIAL NUMBER		3429	3429											
	ARC LIFE TEST		FB	FB											
	PARAMETER		V-1	Pt											
	UNIT OF MEAS.		V	W											
	TYPE OF LIFE TEST	TIME POINT IN HOURS	LIMIT .01 MAX.	LIMIT 2.0 MAX.											
ARC	-	0	.000	.002											
	RB	36	.000	.001											
	See Life Test Above	168	.000	.002											
		500	.000	.002											
		1000	.000	.002											
MSFC	-	0	.000	.000											
	RB	500	.000	.000											
	RB	1000	.000	.001											
	PE	2000	.000	.004											
	BAKE	3000	.000	.001											
	FB	4000	.019	>1.6											
	FB	5000	.031	>1.6											
	FB	6000	.023	63.13											
COMMENTS:			Channeling Accelerated By FB												

NOTE: S/N 13437 - Failed catastrophically at measurement point 6.

CONTRACT																
	SERIAL NUMBER			3456	3469											
	ARC LIFE TEST			BAKE	BAKE											
	PARAMETER			Pt	Pt											
	UNIT OF MEAS.			W	W											
	TYPE OF LIFE TEST	TIME POINT IN HOURS		LIMIT 2.0 MAX.	LIMIT 2.0 MAX.											
ARC	-	0		.001	1.471											
	RB	36		.001	.877											
	See Life Test Above	168		.001	//////											
		500		.001	PULLED											
		1000		.001	//////											
MSFC	-	0		.002	6.321											
	PE	500		>1.6	.013											
	PE	1000		>1.6	.014											
	BAKE	2000		.001	1.288											
	FB	3000		.000	.012											
	RB	4000		.001	.128											
	RB	5000		.001	.356											
	RB	6000		.001	.263											
COMMENTS:				Unstable FF2	Unstable FF1											

NOTE: S/N 13457 - Failed catastrophically at measurement point 4.

S/N 13458 - Failed catastrophically at measurement point 7.

S/N 13467 - Failed catastrophically at measurement point 4

CD4003 LIMIT REJECTS - GROUP "C"

CONTRACT																
	SERIAL NUMBER		3485	3486	3488											
	ARC LIFE TEST		BAKE	BAKE	BAKE											
	PARAMETER		V-1	Pt	Pt											
	UNIT OF MEAS.		V	W	W											
	TYPE OF LIFE TEST	TIME POINT IN HOURS	LIMIT .01 MAX.	LIMIT 2.0 MAX.	LIMIT 2.0 MAX.											
ARC	-	0	.000	.290	.727											
	RB	36	.000	.219	.651											
	See Life Test Above	168	.000	.353	1.698											
		500	.000	.568	1.694											
		1000	.000	.582	1.538											
MSFC	-	0	.000	.797	2.394											
	BAKE	500	.064	.609	2.326											
	BAKE	1000	.059	13.96	13.69											
	FB	2000	.071	.000	.001											
	RB	3000	.069	.001	.001											
	PE	4000	.068	.002	.001											
	PE	5000	.067	.002	.001											
	PE	6000	.069	.001	.001											
COMMENTS:			FF 1													

CD4003 LIMIT REJECTS - GROUP "D"

CONTRACT														
	SERIAL NUMBER		3419	3420	3424	3424	3425	3426	3425	3425	3426	3426		
	ARC LIFE TEST		FB	FB	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A		
	PARAMETER		Ipt	Ipt	Ipt	Ipt	Ipt	Ipt	Idsn1	Idsn13	Idsn1	Idsn13		
	UNIT OF MEAS.		uA	uA	uA	uA	uA	uA	mA	mA	mA	mA		
	TYPE OF LIFE TEST	TIME POINT IN HOURS	DRIFT +.01 MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.	DRIFT + 5% MAX.	DRIFT + 5% MAX.	DRIFT + 5% MAX.	DRIFT + 5% MAX.		
ARC	-	0	.023	.000	.004	.002	.013	.016	5.46	5.59	5.58	5.60		
	RB	36	.024	.001	.129	.003	.017	.023	5.85	5.90	5.96	5.96		
	See Life Test Above	168	.002	.048	PULLED									
		500	.023	.322										
		1000	.025	.653										
MSFC	-	0	.024	.251	.198	.002	.013	.018	5.76	5.83	5.87	5.88		
	FB	500	.193	.001	1.207	.068	.013	.018	5.64	5.72	5.73	5.74		
	RB	1000	.729	.001	.032	.034	.015	.018	5.55	5.64	5.65	5.66		
	RB	2000	.270	.001	.083	.025	.083	.263	6.18	6.23	6.37	6.36		
	PE	3000	.603	.001	.093	.012	.067	.174	6.06	6.06	6.19	6.19		
	BAKE	4000	.029	.001	.007	.003	.015	.019	5.90	5.95	6.04	6.06		
	BAKE	5000	.029	.001	.003	.002	.014	.019	5.83	5.88	5.96	5.98		
	BAKE	6000	.026	.001	.002	.001	.013	.015	5.80	5.85	5.93	5.96		
COMMENTS:			Channel Acc.* by PE&FB Cured by Bake	Unstable	Channel is Cured by Bake	Channel is Cured by Bake	Channel is Cured by Bake	RB Caused Channel Bake Cured	Both Output N-Channel Degraded		Both Output N-Channel Degraded			

*NOTE: Accelerated

CD4003 DRIFT REJECTS - GROUP "A"

CONTRACT														
	SERIAL NUMBER		3426	3419	3425	3425	3426	3426						
	ARC LIFE TEST		N/A	FB	N/A	N/A	N/A	N/A						
	PARAMETER		Vth5	Vth3	Vth3	Vth11	Vth3	Vth3						
	UNIT OF MEAS.		V	V	V	V	V	V						
	TYPE OF LIFE TEST	TIME POINT IN HOURS	DRIFT + 10% MAX.	DRIFT + 10% MAX.	DRIFT + 10% MAX.	DRIFT + 10% MAX.	DRIFT + 10% MAX.	DRIFT + 10% MAX.						
ARC	-	0	1.88	3.14	3.49	3.11	3.38	2.13						
	RB	36	1.82	3.05	3.02	2.97	3.28	2.04						
	See Life Test Above	168	PULLED	2.96	PULLED									
		500		2.89										
		1000		2.27										
MSFC	-	0	1.82	2.84	3.44	3.04	3.33	2.05						
	FB	500	2.02	2.88	3.45	3.06	3.28	2.09						
	FB	1000	2.08	2.88	3.35	2.99	3.24	2.10						
	RB	2000	2.03	2.83	2.08	2.19	2.11	1.85						
	PE	3000	2.01	2.39	2.09	2.21	2.18	1.84						
	BAKE	4000	1.96	2.91	2.25	2.85	3.22	1.92						
	BAKE	5000	1.93	2.92	3.23	2.90	3.25	1.98						
	BAKE	6000	1.91	2.93	3.29	2.94	3.27	2.03						
COMMENTS:			Data Line Going Low VDD= 6V FF#1	Clock Line Going High VDD= 6V FF#1 Master	Clock Line Going High VDD= 6V FF#1 Mastr.	Clock Line Going High VDD= 6V FF#2 Mstr.	Clock Line Going High VDD= 6V FF#1 Mstr.	Clock Line Going Low VDD= 6V FF#1 Slave						

CD4003 DRIFT REJECTS - GROUP "A"

CONTRACT														
	SERIAL NUMBER		3445	3447	3448	3442	3444	3445	3446	3446	3447	3448	3444	3444	
	ARC LIFE TEST		N/A	N/A	N/A	RB	N/A	NA	N/A	N/A	N/A	N/A	N/A	N/A	
	PARAMETER		Vth9	Vth3	Vth5	Pt	Pt	Pt	Pt	Pt	Pt	Pt	Idsn1	Idsn13	
	UNIT OF MEAS.		V	V	V	uA	uA	uA	uA	uA	uA	uA	mA	mA	
	TYPE OF LIFE TEST	TIME POINT IN HOURS	DRIFT + 10% MAX.	DRIFT + 10% MAX.	DRIFT + 10% MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.	DRIFT + 5% MAX.	DRIFT + 5% MAX.	
ARC	-	0	1.68	2.15	1.58	.204	.018	.001	.001	.001	.002	.007	5.44	5.47	
	RB	36	1.69	2.10	1.58	.205	.018	.145	.001	.001	.064	.014	5.76	5.79	
	See Life Test Above	168	PULLED			.001	PULLED								
		500				.001									
		1000				.001									
MSFC	-	0	1.69	2.05	1.60	.227	.018	.112	.002	.000	.069	.010	5.68	5.71	
	RB	500	1.69	2.02	1.59	.001	.018	.443	.001	.000	.108	.003	5.97	6.00	
	RB	1000	1.68	2.02	1.57	.000	.019	.478	.000	.001	.098	.002	6.01	6.04	
	PE	2000	1.70	2.04	1.61	.000	.023	.149	.010	.012	.094	.040	5.92	5.93	
	BAKE	3000	1.68	1.82	1.58	.000	.017	.076	.000	.001	.007	.012	5.83	5.85	
	FB	4000	1.90	1.79	1.78	.001	.375	.063	.001	1.292	.002	.223	5.76	5.78	
	FB	5000	1.77	1.79	1.65	.001	1.124	.067	.115	.655	.002	.344	5.76	5.78	
	FB	6000	1.78	1.84	1.76	.001	1.367	.056	.057	1.205	.002	.292	5.76	5.78	
COMMENTS:			Data Line Going Low VDD= 6V FF#2	Clock Line Going High VDD= 6V FF#1 Slave	Data Line Going Low VDD= 6V FF#1	Unstable	Channel Acc.* by FB	Channel Acc.* by FB	Channel Acc.* by FB	Channel Acc.* by FB	Channel Acc.* by FB&RB Cured by Bake	Channel Acc.* by FB	Output N-Channel Degraded FF#1	FF#2	

*NOTE: Accelerated

CD4003 DRIFT REJECT - GROUP "B"

CONTRACT														
	SERIAL NUMBER		3427	3427	3427	3430	3431	3432	3432	3433	3438	3443	3444	3444	3444
	ARC LIFE TEST		FB	FB	FB	FB	FB	FB	FB	FB	RB	RB	N/A	N/A	N/A
	PARAMETER		Vth11	Vth11	Vth5	Vth5	Vth9	Vth9	Vth9	Vth5	Vth5	Vth5	Vth5	Vth5	Vth3
	UNIT OF MEAS.		V	V	V	V	V	V	V	V	V	V	V	V	V
	TYPE OF LIFE TEST	TIME POINT IN HOURS	DRIFT + 10% MAX.	DRIFT + 5% MAX.	DRIFT + 10% MAX.	DRIFT + 10% MAX.	DRIFT + 10% MAX.	DRIFT + 10% MAX.	DRIFT + 10% MAX.	DRIFT + 10% MAX.	DRIFT + 10% MAX.	DRIFT + 10% MAX.	DRIFT + 10% MAX.	DRIFT + 10% MAX.	DRIFT + 10% MAX.
ARC	-	0	2.50	6.36	1.73	1.76	1.67	1.93	3.69	1.81	1.87	1.71	1.77	3.72	3.25
	RB	36	2.48	6.33	1.73	1.77	1.67	1.92	3.69	1.82	1.88	1.72	1.78	3.72	3.15
	See Life Test Above	168	2.46	6.31	1.73	1.77	1.67	1.92	3.68	1.81	2.11	1.90	PULLED		
		500	2.44	6.30	1.73	1.77	1.67	1.93	3.68	1.81	2.12	1.91			
		1000	2.43	6.29	1.73	1.76	1.67	1.93	3.69	1.81	2.13	1.92			
MSFC	-	0	2.41	6.35	1.74	1.78	1.68	1.93	3.70	1.83	1.95	1.79	1.79	3.73	3.19
	RB	500	2.40	6.34	1.73	1.77	1.67	1.93	3.71	1.83	1.94	1.79	1.79	3.75	3.02
	RB	1000	2.11	6.12	1.75	1.77	1.67	1.92	3.69	1.81	1.92	1.77	1.78	3.73	2.91
	PE	2000	2.18	6.17	1.77	1.79	1.69	1.95	3.68	1.86	1.92	1.77	1.85	3.57	2.27
	BAKE	3000	2.24	6.20	1.73	1.77	1.67	1.93	3.69	1.83	1.90	1.74	1.81	3.63	3.04
	FB	4000	1.83	5.84	1.95	2.03	1.86	2.16	2.35	2.11	2.13	1.94	2.21	3.50	2.43
	FB	5000	1.81	5.86	1.84	2.02	1.76	2.15	2.36	2.11	1.99	1.84	2.26	2.49	2.42
	FB	6000	1.84	5.88	1.94	2.02	1.86	2.15	2.35	2.12	2.11	1.92	2.27	2.48	2.42
COMMENTS:			Clock Line Going High VDD= 6V FF#2 Slave	Clock Line Going Low VDD= 6V FF#2 Slave	Data Line Going Low VDD= 6V FF#1	Data Line Going Low VDD= 6V FF#1	Data Line Going Low VDD= 6V FF#2	Data Line Going Low VDD= 6V FF#2	Data Line Going High VDD= 6V FF#2	Data Line Going Low VDD= 6V FF#1	Data Line Going Low VDD= 6V FF#1	Data Line Going Low VDD= 6V FF#1	Data Line Going Low VDD= 6V FF#1	Data Line Going High VDD= 6V FF#1	Clock Line Going High VDD= 6V FF#1 Master

CD4003 DRIFT REJECTS - GROUP "B"

CONTRACT															
	SERIAL NUMBER		3468	3470	3470	3460	3461	3463	3464	3466	3468	3470	3455		
	ARC LIFE TEST		N/A	N/A	N/A	RB	RB	RB	RB	RB	N/A	N/A	BAKE		
	PARAMETER		Pt	Pt	Pt	Vth5	Vth9	Vth9	Vth5	Vth5	Vth5	Vth9	Vth5		
	UNIT OF MEAS.		uA	uA	uA	V	V	V	V	V	V	V	V		
	TYPE OF LIFE TEST	TIME POINT IN HOURS	DRIFT + .01 MAX.	DRIFT + .01 MAX.	DRIFT + .01 MAX.	DRIFT +10 % MAX.	DRIFT + 10% MAX.	DRIFT + 10% MAX.	DRIFT + 10% MAX.	DRIFT + 10% MAX.	DRIFT + 10% MAX.	DRIFT + 10% MAX.	DRIFT + 10% MAX.		
ARC	-	0	.001	.008	.043	1.76	1.66	1.81	1.81	1.82	1.53	1.75	1.76		
	RB	36	.059	.401	.068	1.78	1.66	1.81	1.81	1.82	1.53	1.75	1.69		
	See Life Test Above	168	PULLED			2.04	1.84	2.05	2.04	2.06	PULLED		1.68		
		500				2.05	1.85	2.07	2.05	2.08			1.68		
		1000				2.05	1.86	2.09	2.05	2.08			1.68		
MSFC	-	0	.110	.442	.051	1.85	1.77	2.05	1.88	1.88	1.54	1.76	1.69		
	PE	500	.033	.130	.365	1.86	1.73	1.92	1.89	1.89	1.56	1.78	1.69		
	PE	1000	.015	.065	.018	1.84	1.72	1.91	1.87	1.88	1.56	1.77	1.69		
	BAKE	2000	.000	.002	.015	1.80	1.70	1.87	1.83	1.84	1.53	1.75	1.67		
	FB	3000	.000	.002	.229	2.06	1.87	2.06	2.05	2.05	1.74	1.94	1.86		
	RB	4000	.014	.085	.096	1.85	1.75	1.91	1.87	1.87	1.57	1.78	1.73		
	RB	5000	.028	.144	.062	1.84	1.74	1.91	1.87	1.87	1.56	1.78	1.72		
	RB	6000	.021	.119	.048	1.83	1.72	1.87	1.86	1.85	1.55	1.76	1.71		
COMMENTS:			Channel Acc.* by FB&RB Cured by Bake	Channel Acc.* by FB&RB Cured by Bake	Channel Acc.* by FB	Data Line Going Low VDD= 6V FF#1	Data Line Going Low VDD= 6V FF#2	Data Line Going Low VDD= 6V FF#2	Data Line Going Low VDD= 6V FF#1	Data Line Going Low VDD= 6V FF#1	Data Line Going Low VDD= 6V FF#1	Data Line Going Low VDD= 6V FF#2	Data Line Going Low VDD= 6V FF#1		

*NOTE: Accelerated

CD4003 DRIFT REJECTS - GROUP "C"

CONTRACT															
	SERIAL NUMBER		3478	3480	3483	3484	3489	3489	3491	3478	3478	3475	3476	3477	3478
	ARC LIFE TEST		BAKE	BAKE	RB	BAKE	N/A	N/A	N/A	BAKE	BAKE	BAKE	BAKE	BAKE	BAKE
	PARAMETER		Pt	Pt	Pt	Pt	Pt	Pt	Pt	Idsn 1	Idsn13	Vth9	Vth9	Vth5	Vth5
	UNIT OF MEAS.		uA	uA	uA	uA	uA	uA	uA	mA	mA	V	V	V	V
	TYPE OF LIFE TEST	TIME POINT IN HOURS	DRIFT ±.01% MAX	DRIFT ±.01% MAX	DRIFT ±.01% MAX	DRIFT ±.01% MAX	DRIFT ±.01% MAX	DRIFT ±.01% MAX	DRIFT ±.01% MAX	DRIFT +5% MAX	DRIFT +5% MAX	DRIFT +10% MAX	DRIFT +10% MAX	DRIFT +10% MAX	DRIFT +10% MAX
ARC	-	0	.013	.001	.935	.001	.002	.013	.001	5.56	5.50	1.77	1.71	1.80	1.82
	RB	36	.015	.001	.932	.002	.059	.024	.053	5.90	5.84	1.77	1.68	1.80	1.83
	See Life Test Above	168	.013	.001	.421	.060	Pulled			5.75	5.69	1.77	1.68	1.79	1.82
		500	.018	.002	.002	.015				5.61	5.55	1.77	1.67	1.79	1.83
		1000	.018	.001	.449	~~.252~~ .252				5.59	5.53	1.77	1.67	1.79	1.82
MSFC	-	0	.013	.000	.403	.001	.072	.018	.062	5.60	5.54	1.78	1.68	1.80	1.83
	BAKE	500	.015	.000	.406	.002	.002	.000	.000	5.57	5.50	1.78	1.68	1.80	1.83
	BAKE	1000	.016	.000	.408	.003	.000	.001	.001	5.50	5.42	1.77	1.66	1.79	1.81
	FB	2000	.015	.001	.414	.067	.000	.059	.000	5.45	5.38	1.96	1.91	2.00	2.19
	RB	3000	.015	.001	.001	.075	.001	.042	.001	5.48	5.42	1.84	1.74	1.86	2.08
	PE	4000	.033	.204	1.078	.000	.002	.038	.000	6.06	6.07	1.86	1.77	1.88	2.09
	PE	5000	.028	.000	1.079	.002	.000	.032	.000	6.06	6.05	1.86	1.76	1.87	2.08
	PE	6000	.126	.000	1.078	.002	.000	.035	.000	6.18	6.15	1.83	1.73	1.85	2.06
COMMENTS:			Unstable	Unstable	Channel Cured by RB	Channel Acc.* by FB&RB Bake & PE Cured	Channel Cured by Bake	Channel Acc.* by FB Cured by Bake	Channel Acc.* by RB Cured by Bake	Both Output N-Channel Degraded		Data Line Going Low VDD= 6V FF#2	Data Line Going Low VDD= 6V FF#2	Data Line Going Low VDD= 6V FF#1	Data Line Going Low VDD= 6V FF#1

*NOTE: Accelerated

CD4003 DRIFT REJECTS - GROUP "D"

CONTRACT	SERIAL NUMBER		3481	3489	3491	3492	3473	3476	3476	3478	3478	3478	3481	3491	
	ARC LIFE TEST		BAKE	N/A	N/A	N/A	BAKE	BAKE	BAKE	BAKE	BAKE	BAKE	BAKE	N/A	
	PARAMETER		Vth5	Vth 5	Vth 5	Vth5	Vth 3	Vth11	Vth 3	Vth 3	Vth 3	Vth 3	Vth 3	Vth 11	
	UNIT OF MEAS.		V	V	V	V	V	V	V	V	V	V	V	V	
	TYPE OF LIFE TEST	TIME POINT IN HOURS	DRIFT ± 10% MAX	DRIFT ± 10% MAX	DRIFT ±10% MAX	DRIFT ±10% MAX	DRIFT ±10% MAX	DRIFT ±10% MAX	DRIFT ±10% MAX	DRIFT ±10% MAX	DRIFT ±10% MAX	DRIFT ±10% MAX	DRIFT ±10% MAX	DRIFT ±10% MAX	
ARC	-	0	1.82	1.57	1.57	1.58	2.27	1.74	2.32	1.95	3.40	2.08	1.93	1.72	
	RB	36	1.83	1.58	1.57	1.58	2.24	1.81	2.32	1.98	3.31	1.98	1.98	1.76	
	See	168	1.83				2.26	1.73	2.34	1.93	3.38	2.06	1.92		
	Life	500	1.83	Pulled			2.27	1.74	2.36	1.95	3.38	2.09	1.94	Pulled	
	Test	1000	1.83				2.27	1.73	2.38	1.93	3.38	2.10	1.92		
	Above														
MSFC	-	0	1.84	1.59	1.58	1.59	2.23	1.80	2.33	1.95	3.38	2.07	1.96	1.79	
	Bake	500	1.84	1.57	1.56	1.56	2.23	1.81	2.34	1.96	3.37	2.09	1.99	1.80	
	Bake	1000	1.82	1.54	1.54	1.54	2.22	1.79	2.35	1.94	3.37	2.13	1.96	1.77	
	FB	2000	2.12	1.73	1.75	1.73	1.92	1.97	2.08	2.28	3.26	2.14	2.18	1.95	
	RB	3000	1.90	1.60	1.60	1.58	2.04	1.87	2.07	2.20	3.30	2.12	2.19	1.97	
	PE	4000	1.93	1.62	1.62	1.61	2.04	1.96	2.14	2.21	2.24	1.90	2.17	1.95	
	PE	5000	1.92	1.62	1.62	1.61	2.05	1.88	2.14	2.26	2.28	1.93	2.17	1.85	
	PE	6000	1.90	1.60	1.61	1.60	2.08	1.96	2.19	2.17	2.14	1.84	2.17	1.92	
	COMMENTS:		Clock Line Going Low VDD= 6V FF#1	Clock Line Going Low VDD= 6V FF#1	Clock Line Going Low VDD= 6V FF#1	Clock Line Going Low VDD= 6V FF#1	Clock Line Going High VDD= 6V FF#1 Slave	Clock Line Going Low VDD= 6V FF#2	Clock Line Going Low VDD= 6V FF#1	Clock Line Going Low VDD= 6V FF#1	Clock Line Going High VDD= 6V FF#1 Master	Clock Line Going High VDD= 6V FF#1 Slave	Clock Line Going Low VDD= 6V FF#1	Clock Line Going Low VDD= 6V FF#2	

CD4003 DRIFT REJECTS - GROUP "D"

CONTRACT														
	SERIAL NUMBER		3378	3378	3378	3378	3378	3378	3395	3395	3395	3395			
	ARC LIFE TEST		N/A	N/A	N/A	N/A	N/A	N/A	RB	RB	RB	RB			
	PARAMETER		Vnm	Ids	Ids	Ids	Ids	Ids	Vnm	Vnm	Ids	Ids			
	UNIT OF MEAS.		V	uA	uA	uA	uA	uA	V	V	uA	uA			
	TYPE OF LIFE TEST	TIME POINT IN HOURS	DRIFT ±5% MAX	DRIFT ±5% MAX	DRIFT ±5% MAX	DRIFT ±5% MAX	DRIFT ±5% MAX	DRIFT ±5% MAX	DRIFT ±5% MAX	DRIFT ±5% MAX	DRIFT ±5% MAX	DRIFT ±5% MAX			
ARC	-	0	NO HISTORY						4.82	5.10	4.06	4.23			
	RB	36							4.81	5.09	4.09	4.24			
	See Life Test Above	168							4.50	5.02	3.71	3.99			
		500							4.37	4.96	3.52	3.90			
		1000							4.21	4.86	3.24	3.70			
MSFC	-	0	4.42	2.15	1.37	7.17	7.10	6.21	4.28	5.17	3.19	3.72			
	BAKE	500	4.60	2.89	1.85	7.19	7.13	6.23	4.71	5.29	3.85	4.11			
	BAKE	1000	4.60	2.89	1.85	7.20	7.14	6.20	4.77	5.09	3.92	4.12			
	FB	2000	4.59	2.88	1.84	7.18	7.13	6.23	3.91	4.21	2.25	2.79			
	RB	3000	4.59	2.88	1.84	7.23	17.18	6.27	4.12	4.62	3.27	3.66			
	PE	4000	4.59	2.88	1.84	7.19	17.12	6.24	3.84	4.10	2.40	2.87			
	PE	5000	5.48	3.87	1.83	17.09	17.10	16.18	3.83	4.13	2.57	3.04			
	PE	6000	5.47	3.46	1.82	17.05	17.06	16.12	3.85	4.06	2.70	2.94			
						Pin 5	Pin 9	Pin 10							
	COMMENTS:		Input and Output Transistors Indicated Instability in the "On" State						Input and Output Transistors Indicated Instability in the "on" State						

CD4003 DRIFT REJECTS - GROUP "D"

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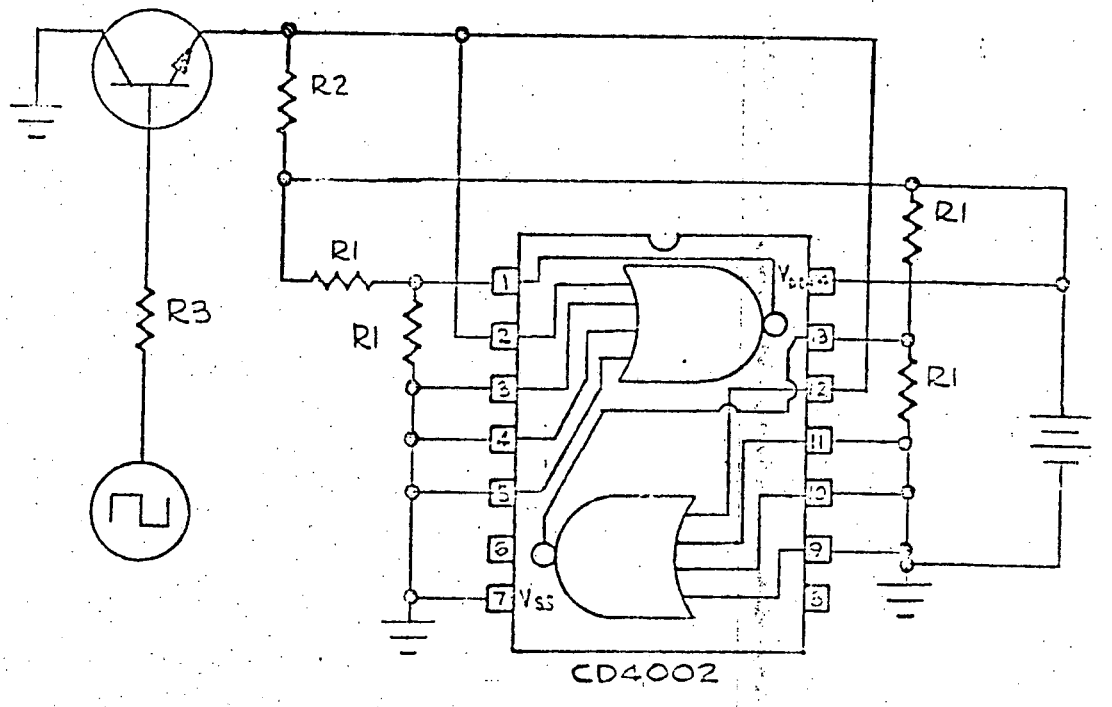
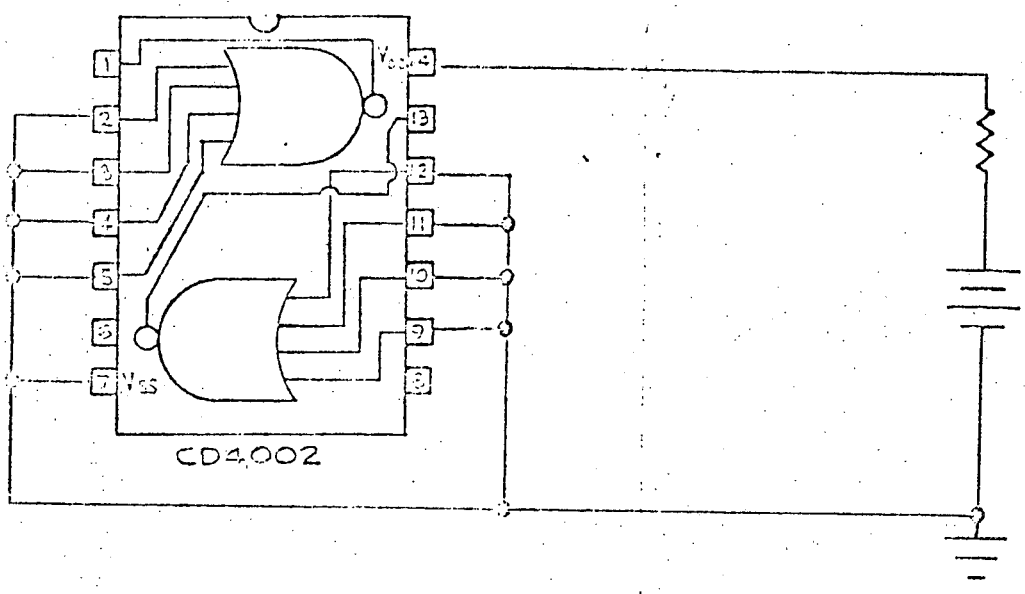
APPENDIX H

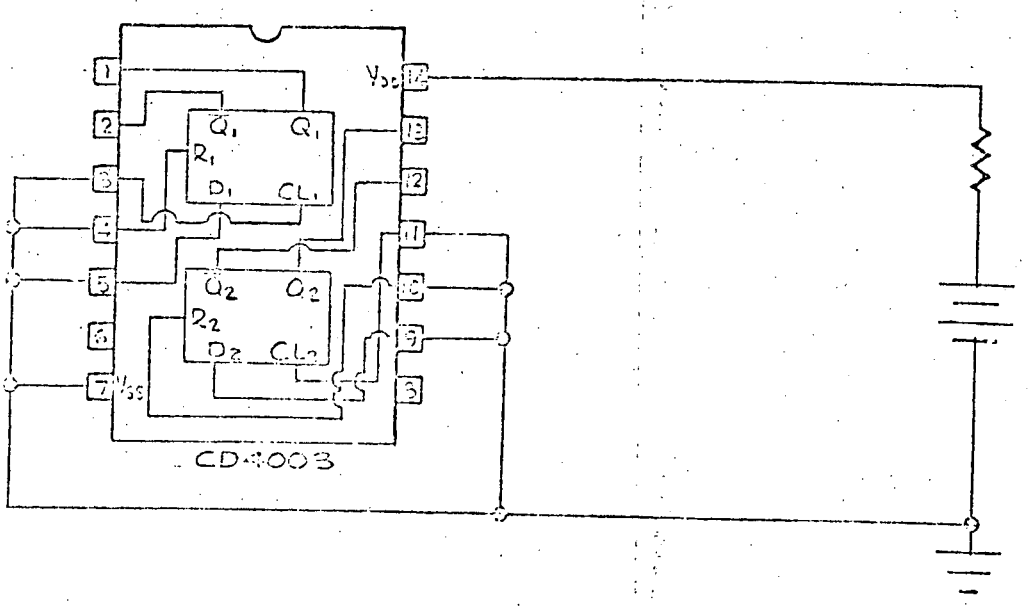
Life Test Circuits



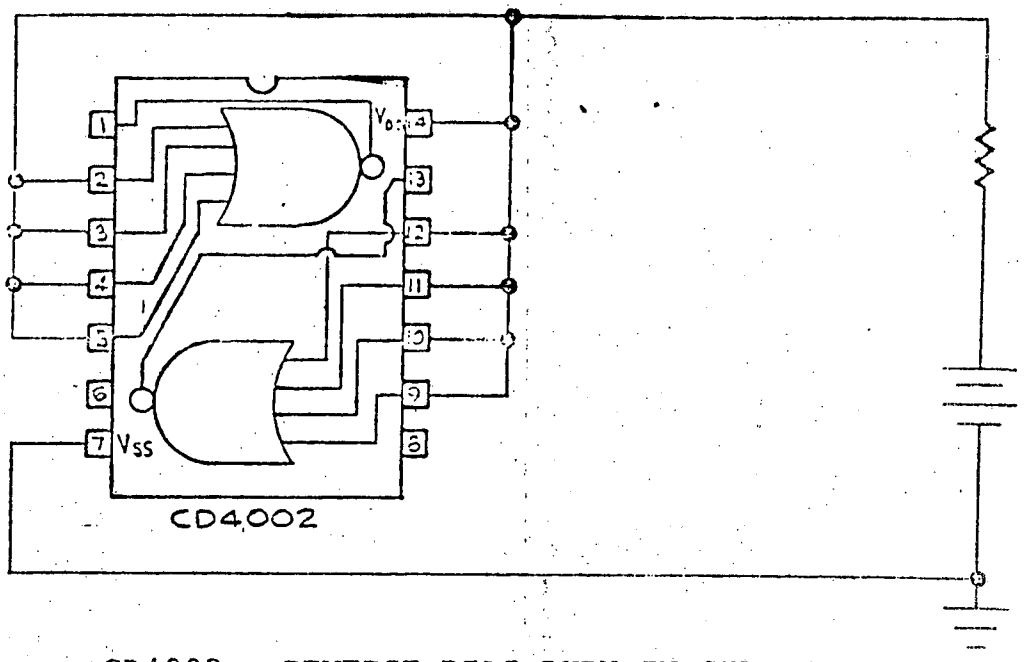
CD4002 PARALLEL EXCITATION BURN-IN CIRCUIT



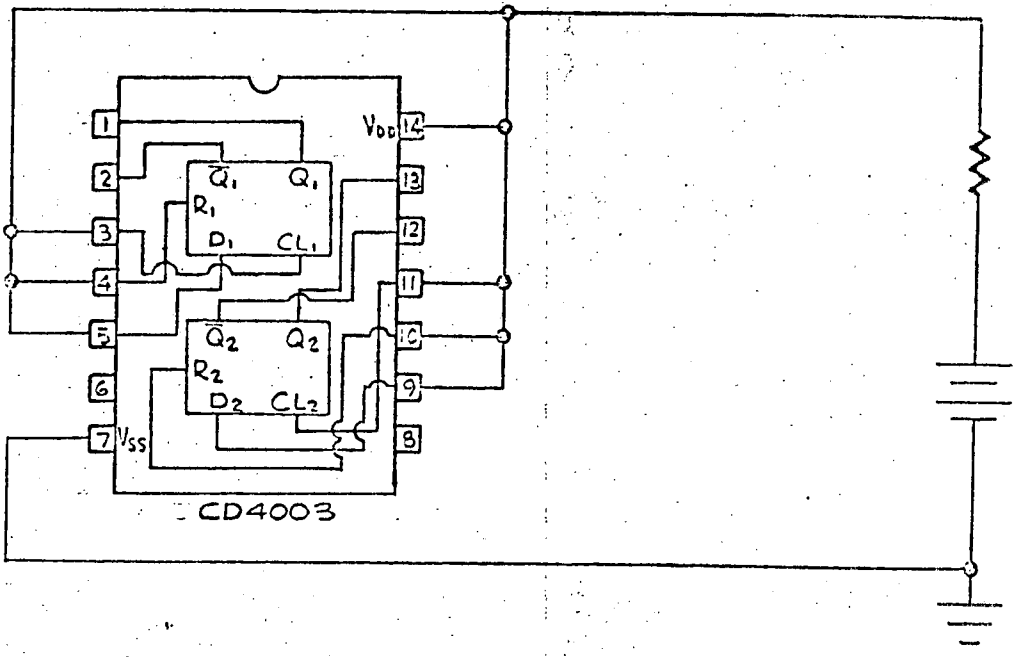
CD4-02 FORWARD BIAS BURN-IN CIRCUIT



CD4003 FORWARD BIAS BURN-IN CIRCUIT



CD4002 REVERSE BIAS BURN-IN CIRCUIT



CD4003 REVERSE BIAS BURN-IN CIRCUIT

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APPENDIX I

NASA/ARC Contract Number NAS 2-5760 Abstract

C 2

DCA

ABSTRACT

PART TYPE:	CD4002 and CD4003
MANUFACTURER:	RCA
NASA AMES SPECIFICATION:	A-15923
DCA TEST PROCEDURE:	No. 136

This abstract describes the nature, purpose, and results of the NASA Ames Qualification Test, performed for NASA Ames during the period of time between January 1970 and June 1970, by DCA RELIABILITY LABORATORY.

THE NATURE

Two hundred RCA integrated circuits were subjected to a pre-qualification inspection which consisted of temperature cycling, acceleration, fine leak, gross leak, electrical measurements, burn-in, and electrical measurement. Upon completion the units were divided into the following test groups:

B-1	Control Group
B-2	Constructional Analysis Group
B-3	Mechanical Analysis Group
C	Environmental Group
D	Life Test Group

The Environmental Group was subjected to four (4) environmental stresses which were in accordance with NASA and military semiconductor

THE NATURE (CONT)

qualification standards. Both the Environmental Group and the Life Test Group were then subjected to a 1000 hour Life Test which consisted of an electrical stress at an ambient temperature of 125°C.

THE PURPOSE

To evaluate the physical and electrical integrity of the COS MOS integrated circuits manufactured by RCA for use on the PIONEER Program.

RESULTS

Pre-Qualification

1. All the units failed Fine Leak.
2. All the units failed Gross Leak.
3. One CD4003 failed and all other units passed the Initial Electrical Test.
4. Second Electrical Test
   a. The CD4002 had twenty seven units which exceeded the manufacturer's limits and an additional twenty units, which indicated instability through parametric drift, within the manufacturer's limits (drift limits are specified in Appendix II).
   b. The CD4003 had two units which exceeded the manufacturer's limits and an additional twenty five units indicated instability through parametric drift within the manufacturers limits.

CONSTRUCTIONAL ANALYSIS

1. All the units passed the external visual inspection.
2. All the units failed the internal visual inspection.

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CONSTRUCTIONAL ANALYSIS (CONT)

3. Diffusion depths, metalization thickness, and die thickness were measured and recorded using angle lapping and straining techniques.

MECHANICAL ANALYSIS

1. All the units passed the Mechanical Stresses

2. After successful completion of the Lead Fatigue Test, one unit had a lead broken off during the process of removing the device from its carrier for electrical measurement.

ENVIRONMENTAL GROUP

1.. One of the CD4002 devices exceeded the manufacturer's limits at the post Thermal Shock measurement. The other units passed the testing.

2. The CD4003 devices passed the testing.

LIFE TEST GROUP

1. The CD4002 devices had a total of nine limit rejects and twelve units which showed excessive drift during the 1000 hour Life Test.

2. The CD4003 devices had no limit rejects but twenty nine units showed excessive drift during the 1000 hour Life Test.

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CONCLUSIONS

1. The intention of NASA Contract NAS2-5760 was to determine if the RCA COS MOS family of integrated circuits were qualified for use in high reliability space applications. The conclusion based on the parts tested and the test results obtained therein is that the devices are not acceptable.

2. An indepth analysis of the test results and part inspections reveals the following significant details:

   a. It is apparent from the Constructional Analysis that the parts were not subjected to a precap visual inspection to the acceptance criteria defined in MIL-STD-883, Method 2010, Condition A or B.

   b. The failure mechanism for hermeticity was identified to be a glass epoxy insulator attached to the case. This epoxy has a helium entrapment potential.

   c. The pattern of the Life Test characteristics is such that the vast majority of devices, which eventually failed or approached failure, could be identified early (within 200 hours) by utilizing a parameter drift screening technique.

Should these facts be considered and the following recommendations be incorporated, it is concluded by DCA RELIABILITY LABORATORY that the RCA COSMOS series integrated circuits may have the capability of passing the qualification reuqirements.

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RECOMMENDATIONS

1. Parts should be procured to a Pre-Cap Visual Inspection to the acceptance criteria of MIL-STD-883, Method 2010, Condition A or B.

2. Parts should be procured without a glass epoxy insulator in order to guarantee hermeticity . This insulator can be applied after completion of screening.

3. Parts should be procured to a screening inspection according to MIL-STD-883, Method 5004, Class A with the addition of a lot jeopardy clause and parameter drift screen.