N73-23293

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MCR-73-91

FREQUENCY DIVISION MULTIPLEXER
CODE 04236, SERIAL NO. 001

FINAL REPORT
PHASE II
CONTRACT NAS8-25987, MOD. 5

PREPARED FOR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GEORGE C. MARSHALL SPACE FLIGHT CENTER
HUNTSVILLE, ALABAMA 35812

Martin Marietta Aerospace
Denver Division
P. O. Box 179
Denver, Colorado 80201

FINAL REPORT

PHASE II
CONTRACT NAS8-25987, MOD. 5

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FOREWORD

This report is submitted in response to NASA/MSFC Contract NAS8-25987, Modification 5.

TABLE OF CONTENTS

TABLE OF CONTENTS
(CONT)

I. INTRODUCTION

In 1970 the Denver Division of Martin Marietta Aerospace developed and delivered a frequency division multiplexer (FDM) to NASA/MSFC under contract NAS8-24682. This multiplexer as delivered will multiplex 24 channels plus a service channel spaced at 4 kHz from d.c. to 104 kHz with 64 kHz and 68 kHz set aside for pilot and reference tones respectively. Operation of each channel is selectable between double or single sideband with audio bandwidths of 1 or 2 kHz respectively.

Phase I of this contract, NAS8-25987, Modification 5, was a study to determine the optimum channel modifications or redesign to accommodate one 8 kHz DSB and one 16 kHz SSB channel. The areas covered by this study were as follows: (a) wideband operational amplifiers, (b) power supply modifications (c) trade-off to determine requirements for precision components (d) printed circuit board layout, (e) the applicability of original equipment specification No. 110438 and (f) optimum wideband channel design. The results of this Phase I study are contained in Martin Marietta Corporation Report No. MCR-72-235.

Phase II of contract NAS8-25987, Modification 5, is the hardware implementation of the conclusions obtained in Phase I.

The following report describes the design and the test results of the accommodation of two wideband channels, 8 kHz DSB located at 44 kHz and 16 kHz SSB located at 104 kHz. The Acceptance Test Procedure for the FDM unit, modified to wideband operation, is contained in Martin Marietta Corporation Report No. MCR-72-285.

II. WIDEBAND MODIFICATIONS

A. General

Figure 1 shows the block diagram of the frequency division multiplexer (FDM). The unit will accept 24 data channels with channel modulation being selectable between single sideband (SSB) or double sideband (DSB) suppressed carrier. Detailed theory, operation and alignment of the unit is described in Reference 1. The only circuits requiring changes for wideband operation are the channel units. The actual wideband modifications performed under this contract are as follows.

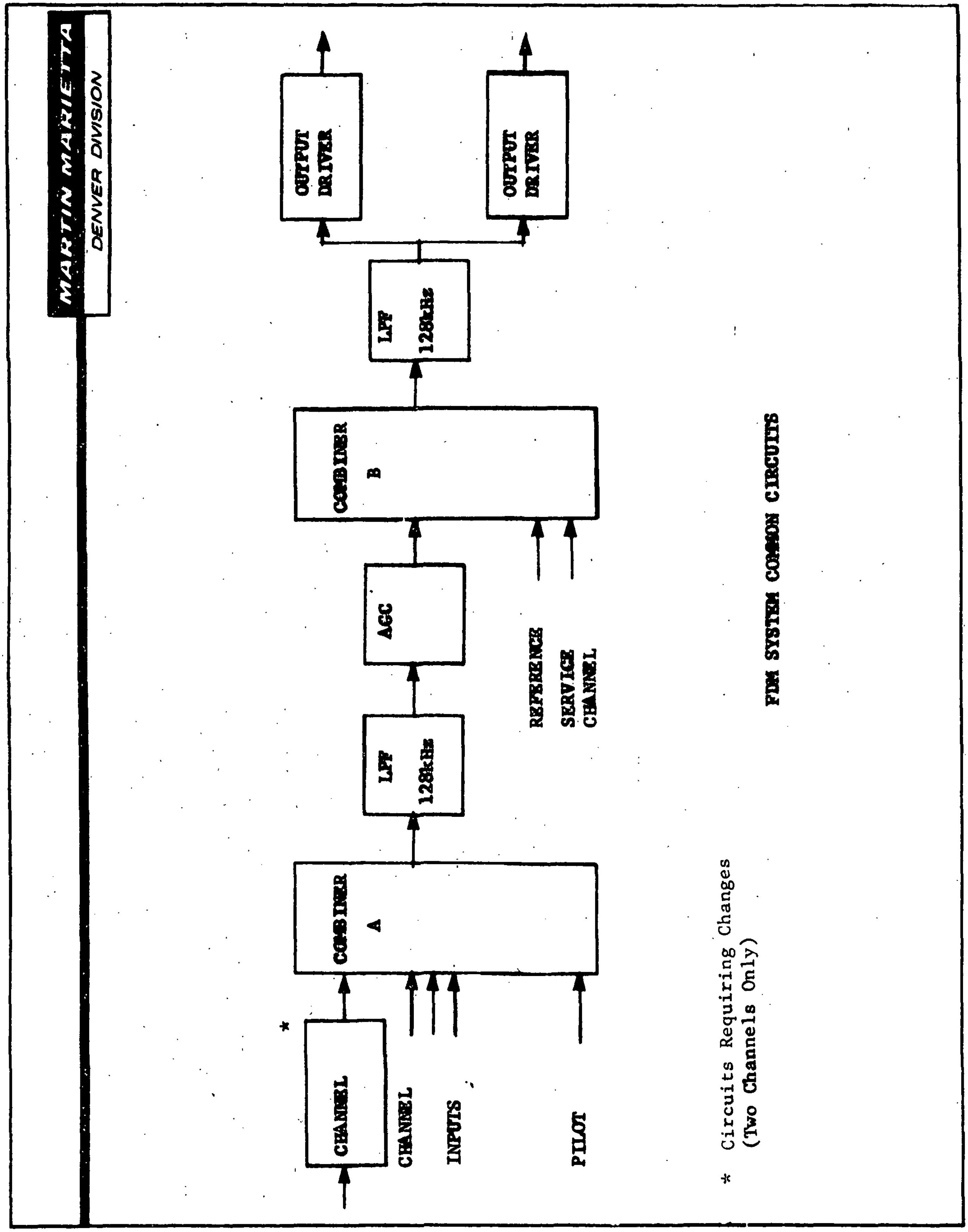
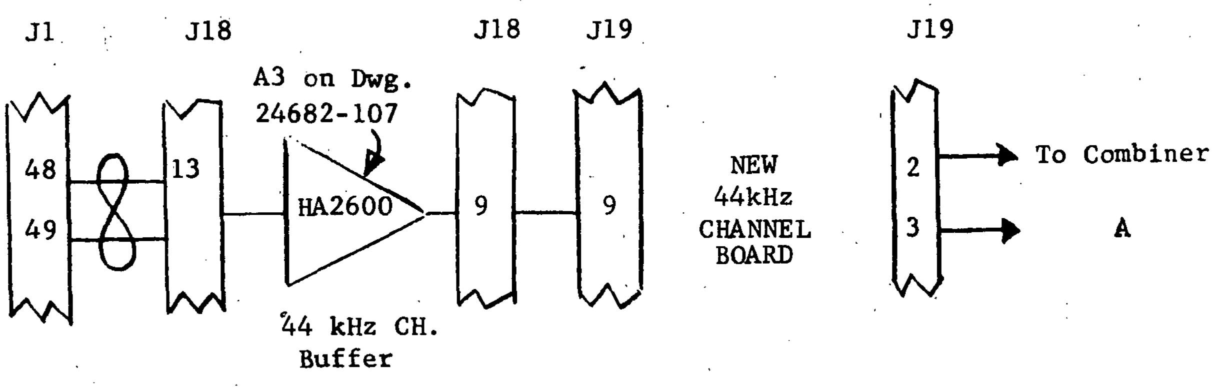

MARTIN MARIETTA
DENVER DIVISION
CHANNEL
CHANNEL
INPUTS
PILOT
COMBINER
A
LPF
128kHz
AGC
REFERENCE
SERVICE
CHANNEL
COMBINER
B
LPF
128kHz
OUTPUT
DRIVER
OUTPUT
DRIVER
FDM SYSTEM COMMON CIRCUITS
*
* Circuits Requiring Changes
(Two Channels Only)

FIGURE 1

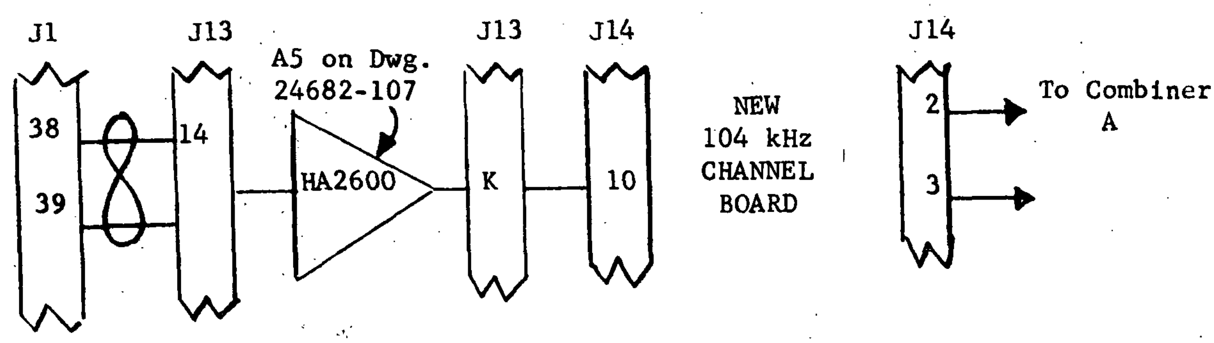
(a) To demonstrate 8 kHz bandwidth capability in the DSB mode modifications were required as shown in Figure 2. The changes include new wideband operational amplifiers, and redesign of the channel filter to provide 0.1 dB flatness over the entire channel bandwidth (16 kHz centered at 128 kHz).

(b) To demonstrate 80 Hz to 16 kHz bandwidth capability in the SSB mode modifications were required as shown in Figure 3. The changes include the above DSB channel modifications. Additionally the 10 pole frequencies in the polyphase network were moved up in frequency by a factor of 8 with respect to the old 10 Hz to 2 kHz design.

The hardware built under this contract include one new board with a single 8 kHz DSB channel, and one new board with a single 16 kHz SSB channel. Modifications to the existing input filter/buffer boards were performed through the substitutions of wideband amplifiers (HA2600) for the 44 and 104 kHz channel locations only. All wideband performance testing were conducted with the new DSB board in the 44 kHz location and the new SSB board in the 104 kHz location as shown below. (It should be noted that the new boards are universal and can be used in any channel location provided (a) appropriate other channels must be deleted to make room for the extended bandwidth, (b) the accompanying channel buffer amplifier must be a wideband amplifier.

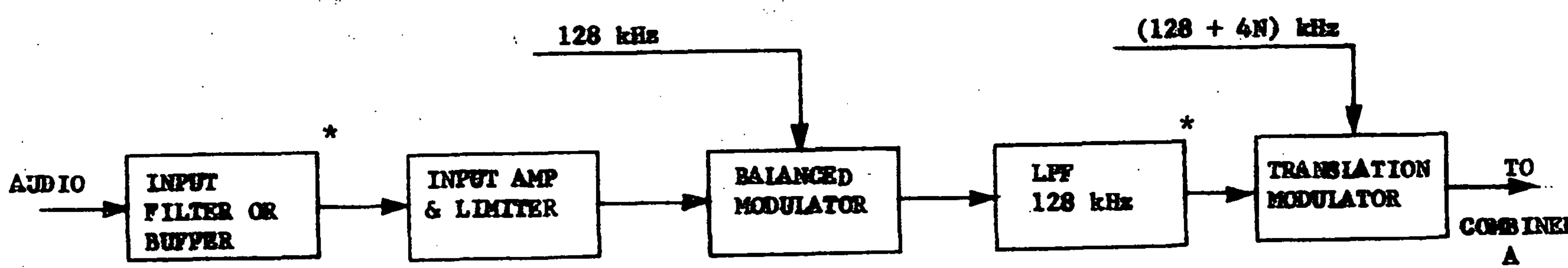


44 kHz DSB CHANNEL SIGNAL PATH



104 kHz SSB CHANNEL SIGNAL PATH

MARTIN MARIETTA
DENVER DIVISION



* CIRCUITS REQUIRING CHANGES

FDM DOUBLE SIDEBAND CHANNEL

FIGURE 2

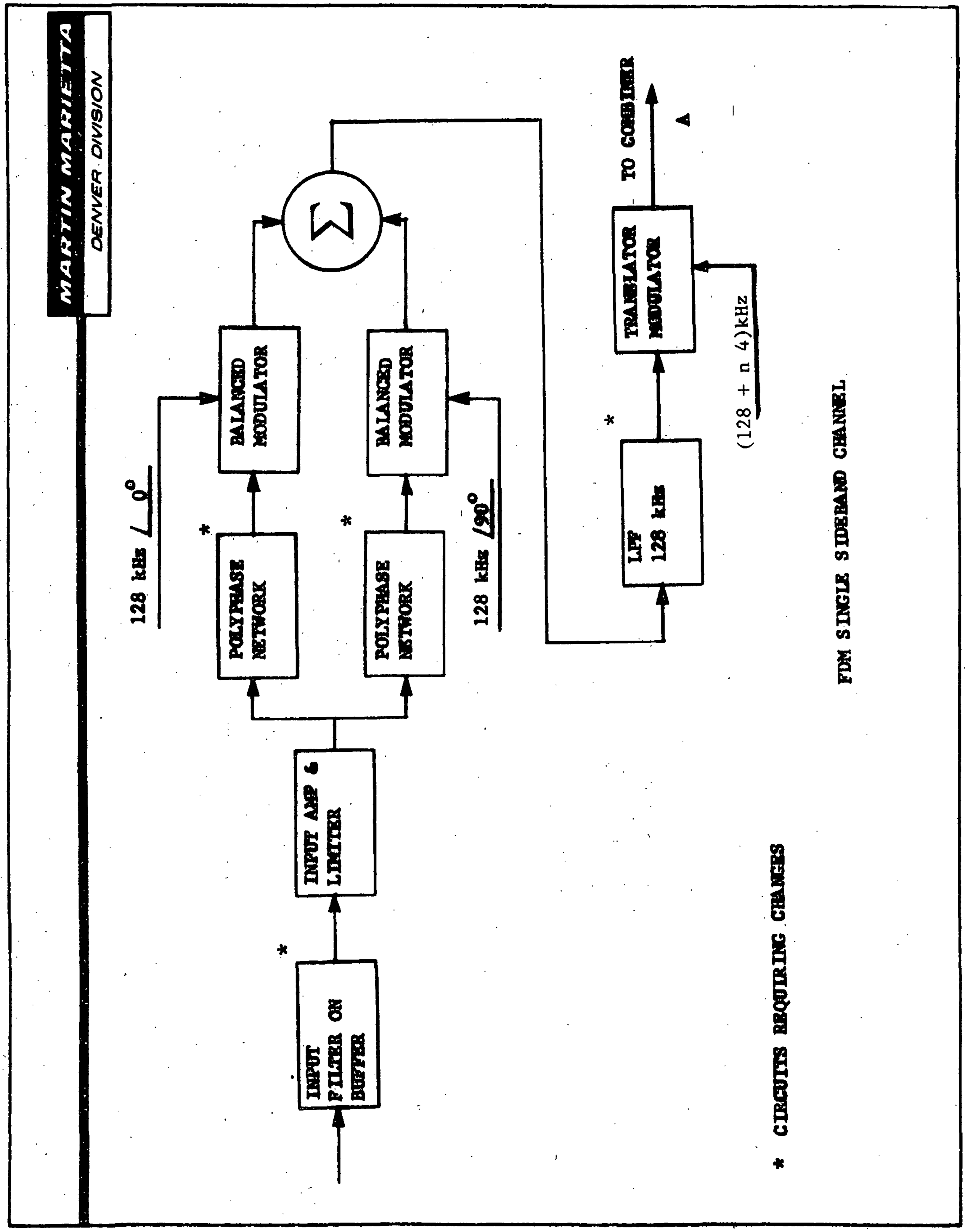

MARTIN MARIETTA
DENVER DIVISION
INPUT FILTER OR BUFFER
INPUT AMP & LIMITER
POLYPHASE NETWORK
POLYPHASE NETWORK
BALANCED MODULATOR
BALANCED MODULATOR
128 kHz ∠0°
128 kHz ∠90°
Σ
LPF 128 kHz
TRANSLATOR MODULATOR
(128 + n 4)kHz
TO COMBINER
FDM SINGLE SIDEBAND CHANNEL
* CIRCUITS REQUIRING CHANGES

FIGURE 3

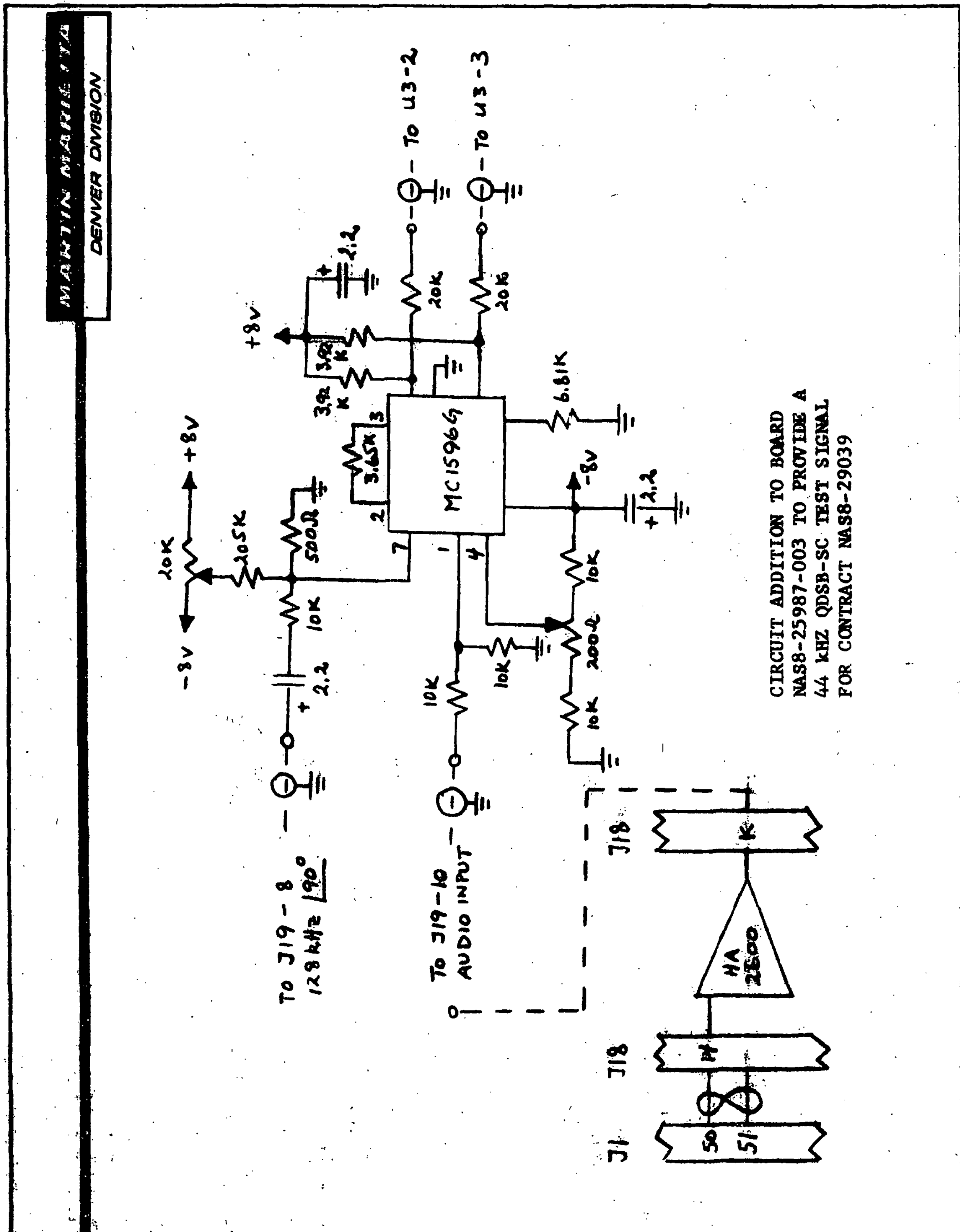
B. DSB Operation

Drawing NAS8-25987-001 gives the details of the new wideband DSB board. The 44 kHz channel audio input is jumpered from connector pin 9 to the input buffer U1. The buffer may operate with the input signal dc level either at ground or at +2.5 vdc. The dc level operation is selected with a jumper from R4. The output of U1 is biased at -4 vdc. CR1. and the negative saturation behavior of U1 itself provide limiting during over voltage data fault conditions. Modulator U2 transforms the input audio signal to a DSB-SC signal centered at 128 kHz. U2 is a balanced modulator operating with a square wave 128 kHz carrier, and at the output of U2 sidebands about the odd harmonics of the carrier are produced, as well as the wanted sidebands about the carrier itself. These unwanted odd harmonics of the carrier are filtered by the output low pass filter L1-L3. The filter is a 7 pole Chebychev filter, 0.01 dB ripple, with the -3 dB point at 183 kHz. The main requirement for this in-line channel filter is a 0.1 dB flatness over the channel bandwidth, which is ±8 kHz centered at 128 kHz in the wideband DSB mode. The filtered signal is down translated from 128 kHz to the channel frequency by the second modulator U4 by a 172 kHz carrier. The odd harmonic spectrum caused by the second balanced modulator is filtered by two low pass filters located on the AGC board (24682-108).

During contract NAS8-29039 the FDM modulator unit is used to provide input signals to the Adcom Model G-146 FDM demodulator and the 44 kHz DSB channel board is modified to provide a quadrature DSB signal with the circuit shown in Figure 4. The Figure 4 circuit is physically located on the NAS8-25987-003 printed circuit board, and the QDSB channel audio is routed through the 48 kHz channel buffer/audio input (to J19-10).

C. SSB Operation

Drawing NAS8-25987-002 gives the details of the new wideband SSB board. The 104 kHz channel audio is jumpered from connector pin 9 to the input buffer U1, which can operate in either the 0 vdc or 2.5 vdc input modes CR1 and CR2 provide over voltage data limiting. The audio is phase shifted through two different paths in a 10-pole Chebychev poly-phase network, U2, 4, 6, 8, 10 and U3, 5, 7, 9, 11 respectively. This phase shift is such that for data frequencies from 80-16000 Hz the phase difference between the audio at U10-6 and U11-6 is 90 ±0.16 degrees. The two audio signals are quadrature translated by U12 and U13 to produce two DSB signals at the modulator output with phase relationships such that



CIRCUIT ADDITION TO BOARD
NAS8-25987-003 TO PROVIDE A
44 KHZ QDSB-SC TEST SIGNAL
FOR CONTRACT NAS8-29039

FIGURE 4

(a) the low side sidebands are cancelled if the two signals are added, and (b) the high side sidebands are cancelled if the two signals are subtracted. U14 performs an addition, and at U14-6 we have SSB with the wanted sideband being the upper side band. Filter L1-L3, as in Section IIB, filters the odd carrier harmonic caused by U12 and U13. The filter wideband requirement in the SSB mode is 0.1 dB flatness over $\pm$16 kHz, centered at 128 kHz. U15 provides down translation from 128 kHz to 104 kHz with translation frequency being 232 kHz. It should be noted that the wanted upper sideband from 128 kHz at U14-6 is transformed to the lower sideband from 104 kHz at the output of modulator U15. As was the case for the 44 kHz channel the odd harmonics caused by U15 are filtered by the two low pass filters located on the AGC board (24682-108).

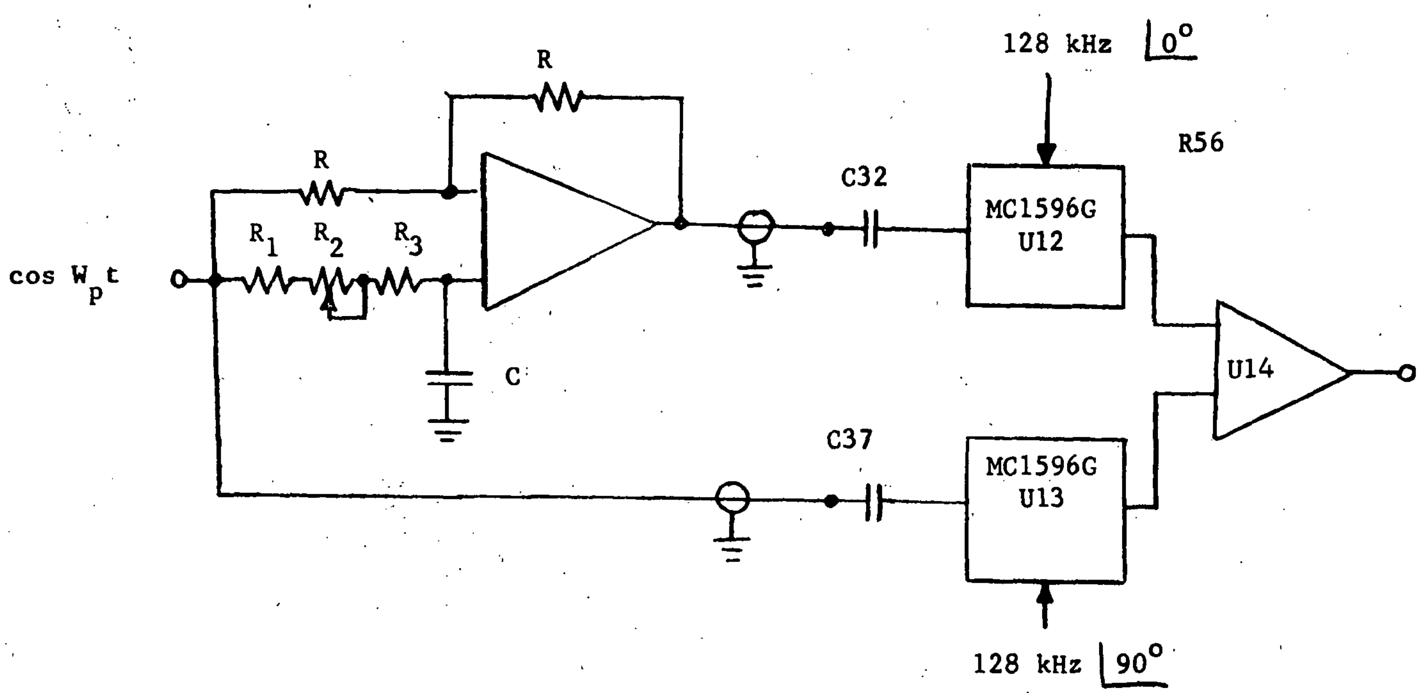
III. ALIGNMENT OF THE WIDEBAND CHANNELS

A. DSB Alignment

Potentiometers R7 and R8 are provided to give the proper dc-bias at the U1 output. The main adjustment is R7. This potentiometer should be adjusted so as to bring the U2-1 input dc level to within about 10 mV of the dc level of U2-4 with R14 in the mid position. Note that R7 changes the channel gain while R8 does not. R14 adjust the carrier suppression in the channel. The carrier null can be checked with a wave analyzer tuned to 128 kHz being connected to U2-6/9, or tuned to the channel frequency and being connected to U4-6/9 or to the FDM output. R9 controls the audio feedthrough in U2. This feedthrough will show up as sidebands around (128 + n4) kHz on the output of U4. For the lower channels this unwanted sideband, may not be suppressed enough by the filters on the AGC board and should be nulled out. The gain in the channel is adjusted with either R16 or R32. The approximately output levels at U2-6/9 and U4-6/9 should be 1.6 vpp with full scale (5 vpp) audio input to the channel. R27 adjusts the feedthrough of the downtranslation carrier (128 + n4) kHz in U4, and R40 adjust the "audio" feedthrough (at 128 kHz $\pm$ channel audio frequency) in U4. Filter coils L1-L3 are adjustable. Adjustment of these coils is not required to make the flatness of the low pass filter flat to within 0.1 dB over the range 128 kHz $\pm$ 8 kHz. However, since two in-line low pass filters are present in the AGC circuit (old filter design with maximum bandwidth requirement of 2 kHz around each channel frequency), these adjustments were required to make the total data path (including the AGC circuit) flat to within 0.1 dB for the wideband channel.

B. SSB Alignment

The channel carrier suppression is adjusted with R54 and R67. With a narrowband wave analyzer tuned to the carrier frequency being connected to the FDM output or to U15-6/9. It is necessary to go back and forth between R54 and R67 until the lowest null is reached. Tune the wave analyzer to the upper sideband of the 104 kHz channel and adjust R56 for null. This adjustment balances the gain between the two quadrature signal paths for maximum suppression of the unwanted sideband. The channel gain adjustment is R83. Adjust this potentiometer for approximately 1.6 vpp with full scale (5 vpp) audio input. R103 and R101 adjust feedthrough at an output frequency of 128 + n4 kHz $\pm$ the audio frequency. R105 and R88 adjust feedthrough in U15 at 128 kHz $\pm$ the audio frequency and (128 $\pm$ n4) kHz respectively. The coil adjustments, L1-L3, is used to provide 0.1 dB channel flatness over the $\pm$16 kHz channel bandwidth. The polyphase network, U2-U11, is aligned as shown below.



Each one-pole phase shifter is aligned independently using the calculated pole frequency, for which the phase shift is exactly 90°, as the input signal. The remainder of the board is used in a SSB check on the adjustment. With the precise pole frequency applied to the phase shifter, the audio inputs to U12 and U13 are exactly at 90° when R2 is correctly adjusted.

The upper sideband at the output of U14 should, therefore, show a null under this condition. Great care must be exercised to provide equal lengths and good shielding of the input connections to U12 and U13. The pole frequency for the wideband polyphase network is shown below.

PHASE SHIFTER	POLE FREQUENCY (HZ)
U2	27.31
U4	205.25
U6	808.27
U8	3113.40
U10	13546.70
U3	94.49
U5	411.12
U7	1583.62
U9	6236.16
U11	46869.30

IV. TEST RESULTS

The frequency division multiplexer code 04236, Serial No. 001, with wideband modifications as described above on the 44 and 104 kHz channels was tested in accordance with Acceptance Test Procedure MCR-72-285. The acceptance test were performed by Martin Marietta Aerospace, Denver Division to show compliance with requirements of contract NAS8-25987, Modification 5. The tests proved the performance of the wideband modified FDM unit to exceed all requirements as stated in MCR-72-285. The acceptance test results are summarized in the following section, and are referenced with paragraph numbers corresponding to those found in Acceptance Test Procedure MCR-72-285. A list of the test equipment used during the acceptance testing is shown in Section V, and the actual laboratory test data sheets are contained in Figures 5 through 20.

2.0 Harmonic Suppression

Channels 44 kHz and 104 kHz were tested in the DSB and SSB mode respectively. All harmonics and unwanted frequencies were suppressed 50 dB or more as verified by attached plots, Figures 5 and 6.

3.0 Data References Level

When the FDM unit was tested with the 44 and 104 kHz channels modified for 2.5 vdc operation, there was essentially no change from Test 2.0. The output plot for the DSB channel is shown in Figure 7. All unwanted frequency components were suppressed by 50 dB or more. The DC level in the audio portion of the SSB channel was found to be approximately zero, and audio clipping will not occur for full scale audio input.

4.0 Sideband Suppression

The 104 kHz SSB channel was tested for sideband suppression at data frequencies of 80, 160, 320, 640, 1280, 5120, 10240 and 16000 Hz. The upper sideband was suppressed 50 dB or more as verified by Figure 8.

5.0 Linearity

The 44 and 104 kHz channels were tested for amplitude linearity. Both channels were within the ± 0.25 dB linearity requirement. The actual data is presented in Figures 9 and 10.

6.0 Individual Passband Characteristics

6.1 The frequency response of the 104 kHz SSB channel was measured and found to be flat within 0.1 dB for data frequencies between 80 and 16000 Hz as shown in Figure 11.

6.2 The frequency response of the 44 kHz DSB channel was measured and found to be flat within 0.1 dB for data frequencies between dc and 8 kHz as shown in Figure 12.

7.0 Data Source Fault

Overvoltage protection testing was performed on the 44 and 104 kHz channels. The channel limiters were verified to become active at input levels beyond approximately ±7.5 vdc. Figure 13. shows the channel signal spectrums for partially limited 100 Hz input signals verifying the harmonics caused by the limiter action. Figure 13 also shows the 50 dB suppression of the upper sidebands in the 104 kHz SSB channel.

8.0 Power Supply Regulation

No detectable degradation was recorded in the 44 and 104 kHz channels as a result of setting the primary power source to 23.8 and 32.2 vdc. Harmonic suppression testing was performed at both voltage settings and the channel output plots are shown in Figures 14 through 17.

9.0 Information Drift

The amplitude tracking between the 44 and 104 kHz channels with respect to the pilot and the reference signal amplitudes was within 0.1 dB after 4 hours. This result is better than the 0.5 dB test requirement. The appropriate signal amplitudes at the start and finish of this test are shown in Figure 18.

10.0 Channel Input Impedance

The input impedances for the 44 and 104 kHz channels were found to be equal at 99.2K ohm as verified by the data in Figure 19.

11.0 Back Current

The input back currents for the 104 and 44 kHz channel were measured and found to be well below the 1 microampere test requirement, as verified by the actual measurements shown in Figure 20.

12.0 Ground Isolation

The ground isolation current was found to be 20 nA. With an electrometer internal impedance of 2M ohms this corresponds to an isolation resistance of 2500M ohms, which is 50 times higher than required.

V. TEST EQUIPMENT

DESCRIPTION	MFGR.	MODEL.	I.D.	CAL. DUE
Sensitive DC Meter	Booton Electronics	95A	EQ590615	11/29/72
Wave Analyzer	Hewlett-Packard	3590A	EQ528777	12/17/72
Sweeping Local Oscillator	Hewlett-Packard	3594A	EQ527880	12/17/72
X-Y Recorder	Hewlett-Packard	7005B	EQ528778	01/07/73
Digital Voltmeter	DANA	5500	EQ526003	11/15/72
Frequency Synthesizer	FLUKE	303A	EQ521786	01/17/73
Oscillator	Hewlett-Packard	204D	EQ531588	12/12/72
LF Oscillator	Hewlett-Packard	202C	EQ500562	02/28/73
RMS Voltmeter	Ballantine	323-07	EQ529146	10/23/72

VI. REFERENCES

Reference 1. Martin Marietta Aerospace Report No. MCR-70-304. Frequency Division Multiplexer Final Report, Contract NAS8-24682.

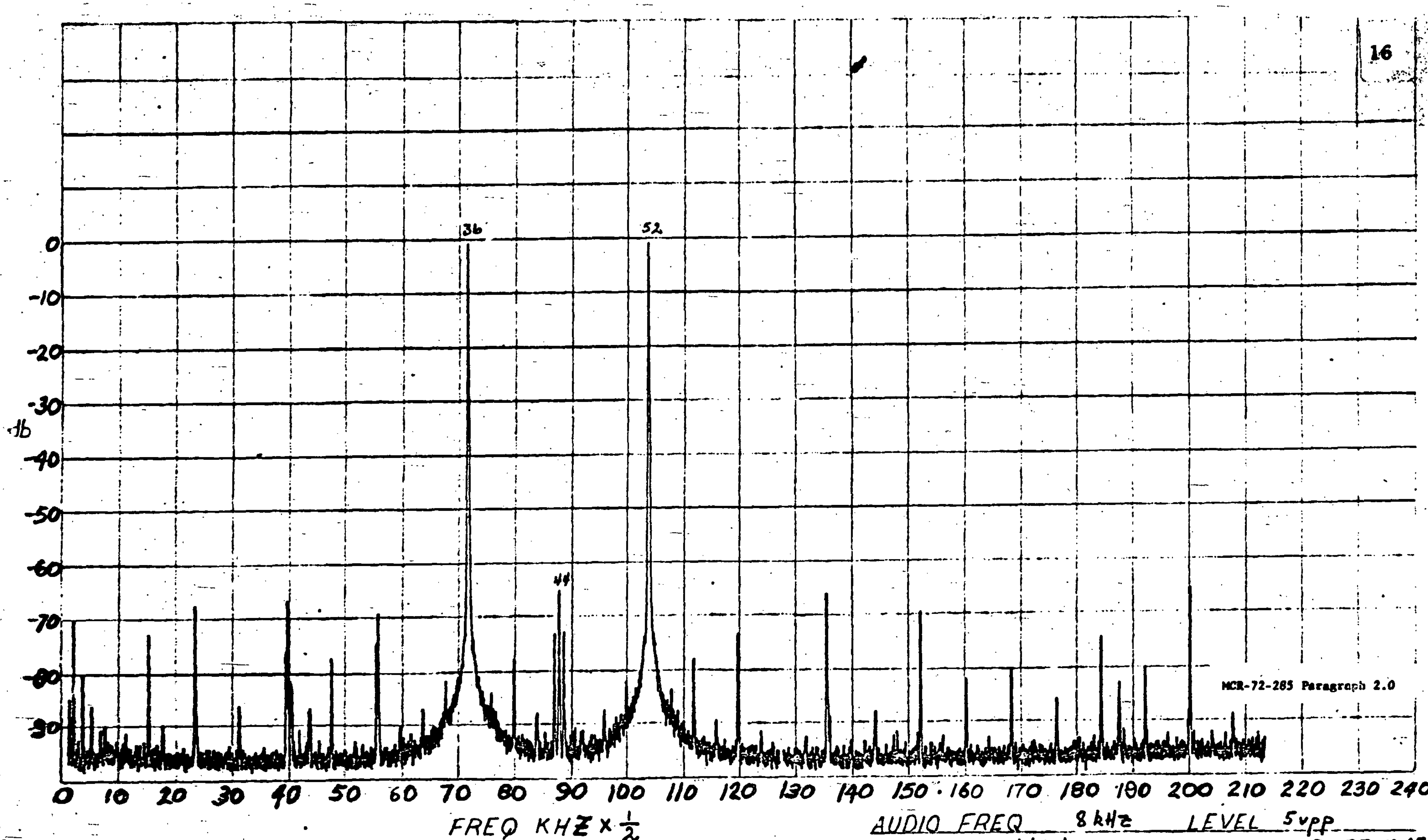
VII. CONCLUSIONS AND RECOMMENDATIONS

An increase of bandwidth from 1 and 2 kHz to 8 and 16 kHz for DSB and SSB respectively has been accomplished for the FDM unit with no major design changes. Minor changes have been performed as follows: (a) wideband operational amplifiers have been substituted as required and (b) the Polyphase Network pole-frequencies have been changed to reflect the 16 kHz upper bound on the bandwidth in the SSB mode, while retaining the 200:1 ratio between the frequency extremeties.

The wideband performance was found to be equivalent to the narrowband performance with 50 dB suppression of unwanted sidebands/harmonics in the channel units. Power consumption increase for the wideband channels is of the order 100 mW for DSB and approximately 450 mW for SSB compared to the narrowband operation.

A number of area presents themselves for future work. During alignment of the present FDM, feedthrough and pick up problems exist. This is mainly a packaging problem, and could be improved in any of the following ways: (a) multilayer boards and rearrangement of the channel VCO locations with respect to the other channel components, (b) shielding between boards in a metal partitioned configuration, and/or overhead shields on the boards themselves, (c) rerouting of system interconnect wiring with improved grounding/shielding, (d) locations of critical adjustments so that these can be made with the board in place rather than on an extender card (to prevent coupling/feedthrough changes when the board is put in place).

For airborne applications, where a wide temperature variation may be expected, the in-line low pass filtering in the double translation method may cause objectionable channel-to-pilot phase tracking. The use of true multipliers with single conversion (sine-wave carriers) could eliminate this potential problem. Also the temperature effect on the polyphase networks needs some investigation.



AUDIO FREQ 8 kHz LEVEL 5vpp
OUTPUT 44 kHz CHANNEL DATE 10-27-72

FIGURE 5

MCR-62-285 Paragraph 2.0

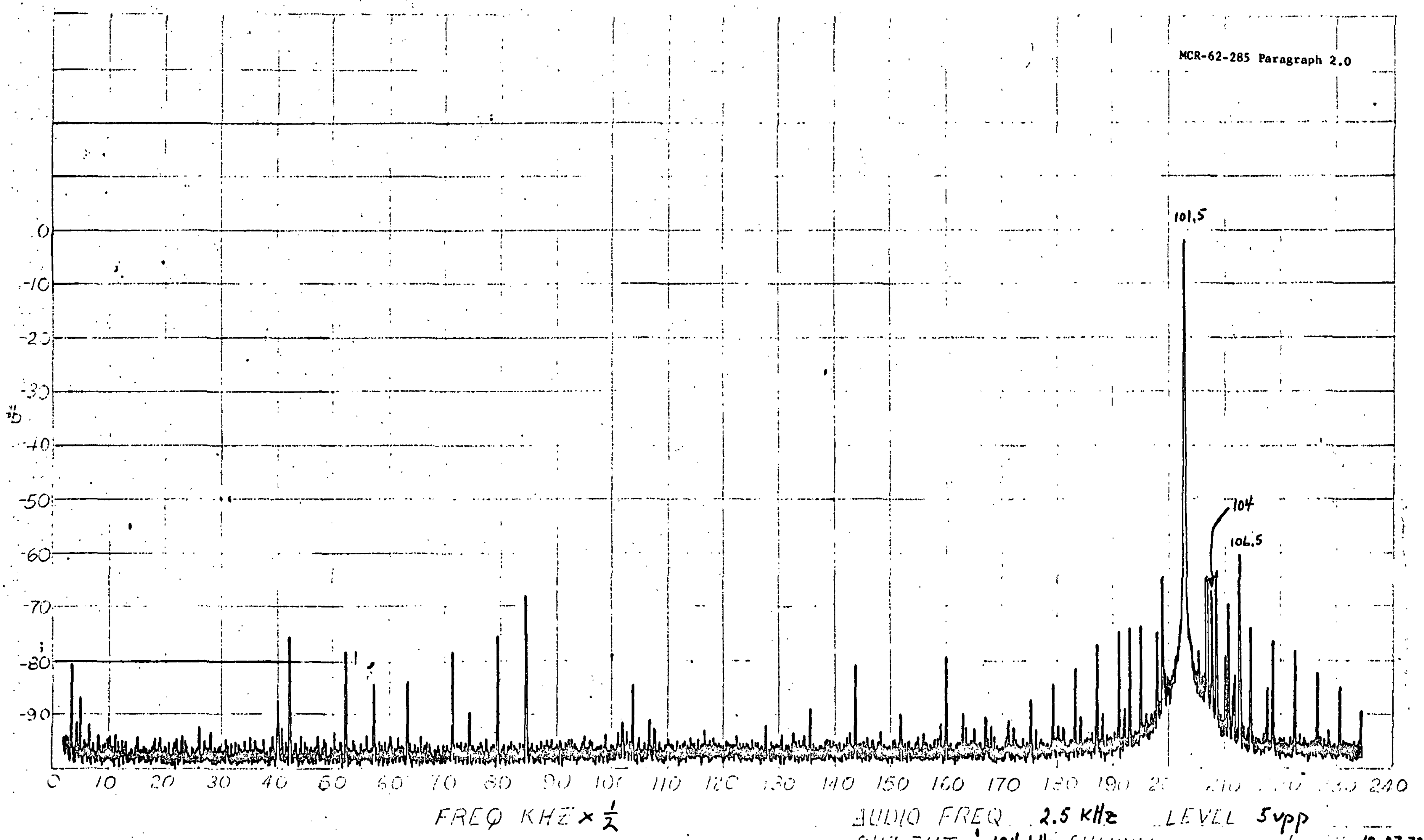


FIGURE 6

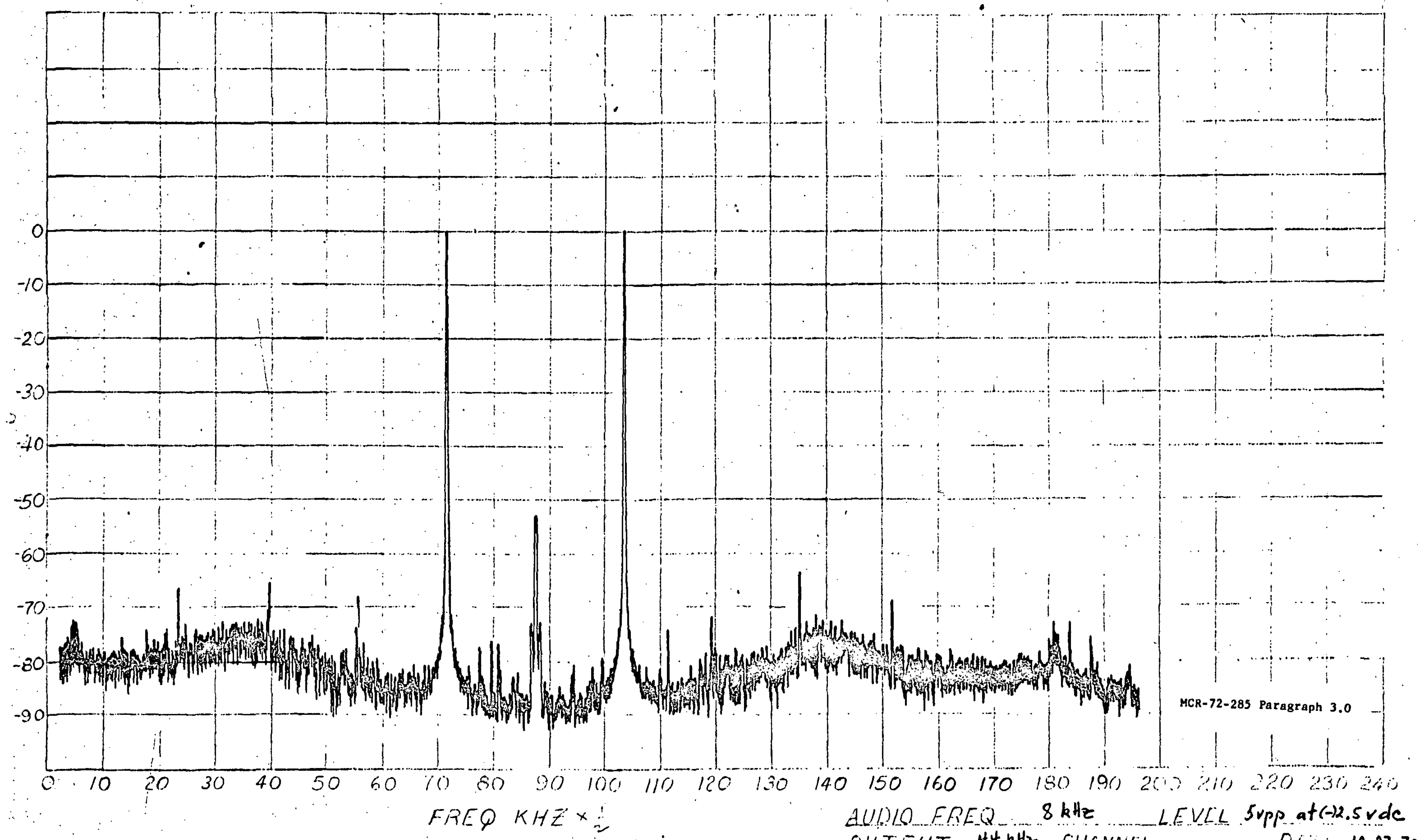

MCR-72-285 Paragraph 3.0
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
0 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150 160 170 180 190 200 210 220 230 240
FREQ KHZ × ½
AUDIO FREQ 8 kHz
LEVEL 5vpp at(-)2.5vdc
OUTPUT 44 kHz CHANNEL
DATE 10-27-72

FIGURE 7

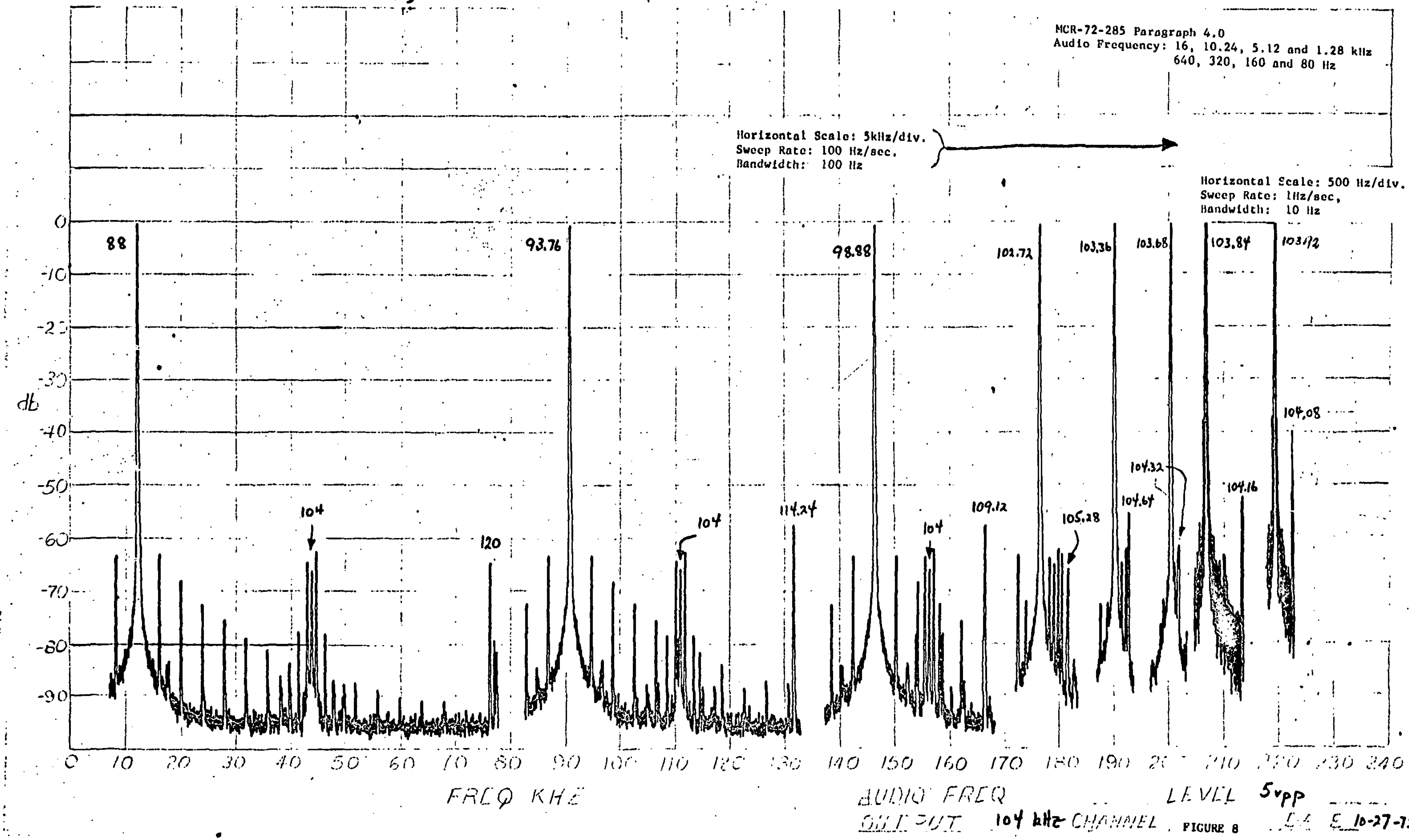

MCR-72-285 Paragraph 4.0
Audio Frequency: 16, 10.24, 5.12 and 1.28 kHz
640, 320, 160 and 80 Hz
Horizontal Scale: 5kHz/div.
Sweep Rate: 100 Hz/sec.
Bandwidth: 100 Hz
Horizontal Scale: 500 Hz/div.
Sweep Rate: 1Hz/sec,
Bandwidth: 10 Hz
88
93.76
98.88
102.72
103.36
103.68
103.84
103.92
104.08
104.32
104.64
104.16
105.28
109.12
114.24
104
104
104
120
db
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
0 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150 160 170 180 190 200 210 220 230 240
FREQ KHZ
AUDIO FREQ
LEVEL 5vpp
OUTPUT 104 kHz CHANNEL
E 10-27-72

FIGURE 8

MCR-72-285 Paragraph 5.0
CHANNEL LINEARITY

44 kHz CHANNEL

V_{in} (RMS)	V_{in} (dB)	V_o (dB)	Deviation (dB)
.3535	0	0	0
.707	+6.02	+6	-0.02
1.061	+9.54	+9.6	+0.06
1.414	+12.04	+11.8	-0.24
1.768	+13.98	+13.75	-0.23

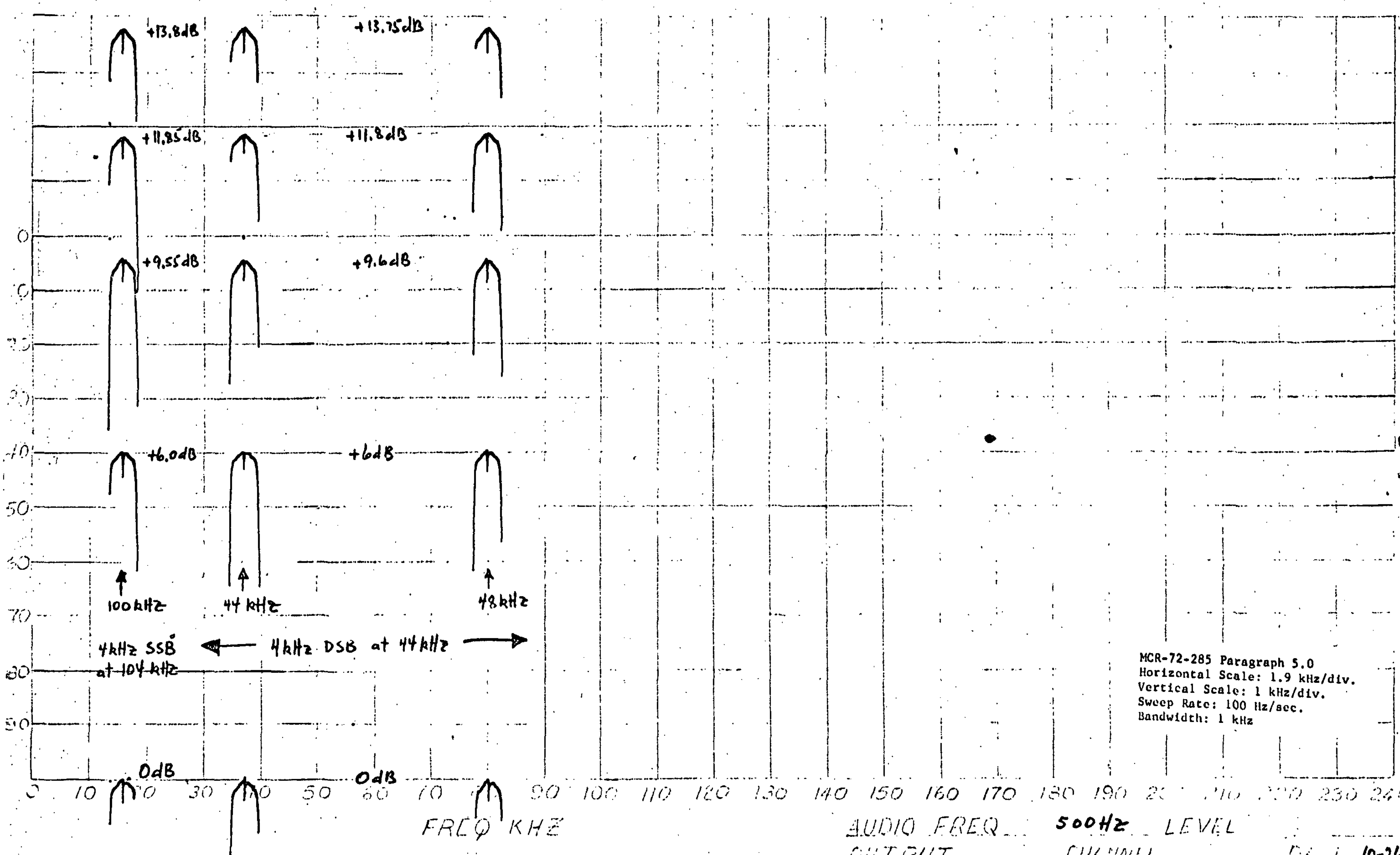
44 kHz channel linearity for best straight line is within $\pm$0.12 dB.

104 kHz CHANNEL

V_{in} (RMS)	V_{in} (dB)	V_o (dB)	Deviation (dB)
.3535	0	0	0
.707	+6.02	+6.0	-0.02
1.061	+9.54	+9.55	+0.01
1.414	+12.04	+11.85	-0.19
1.768	+13.98	+13.8	-0.18

104 kHz channel linearity for best straight line is within $\pm$0.1 dB.

FIGURE 9



AUDIO FREQ 500Hz LEVEL

OUTPUT CHANNEL

FIGURE 10

10-26-72

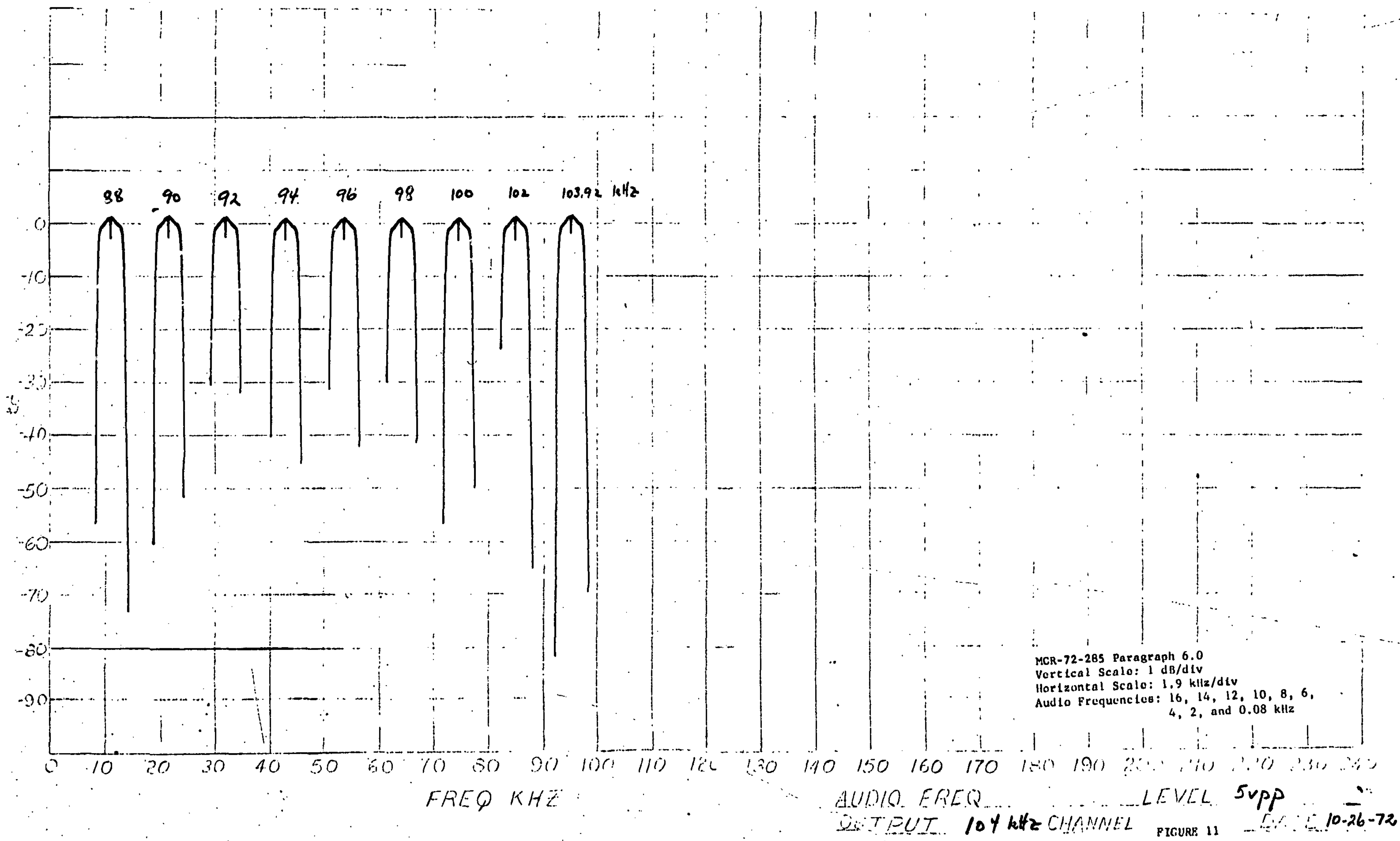
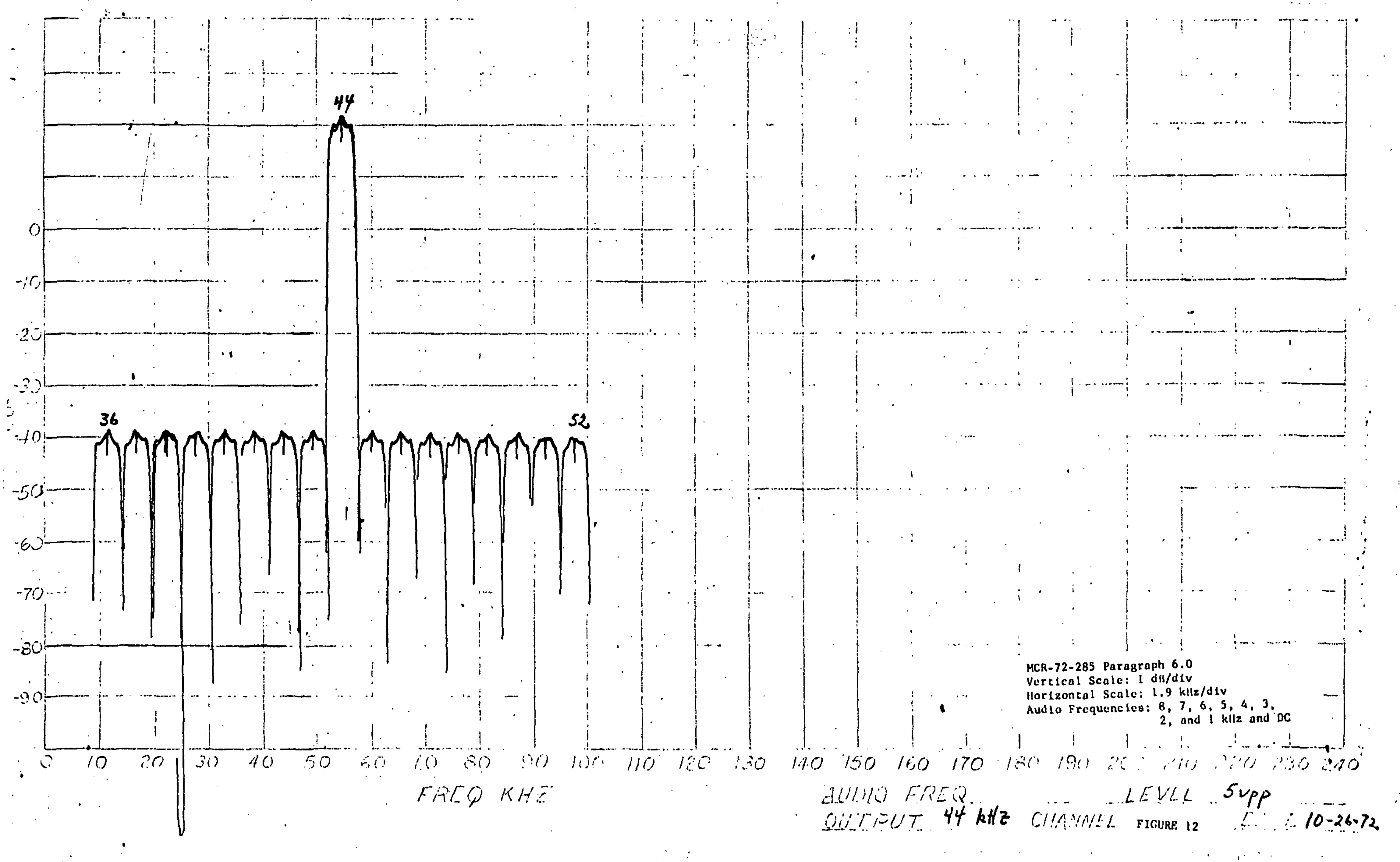
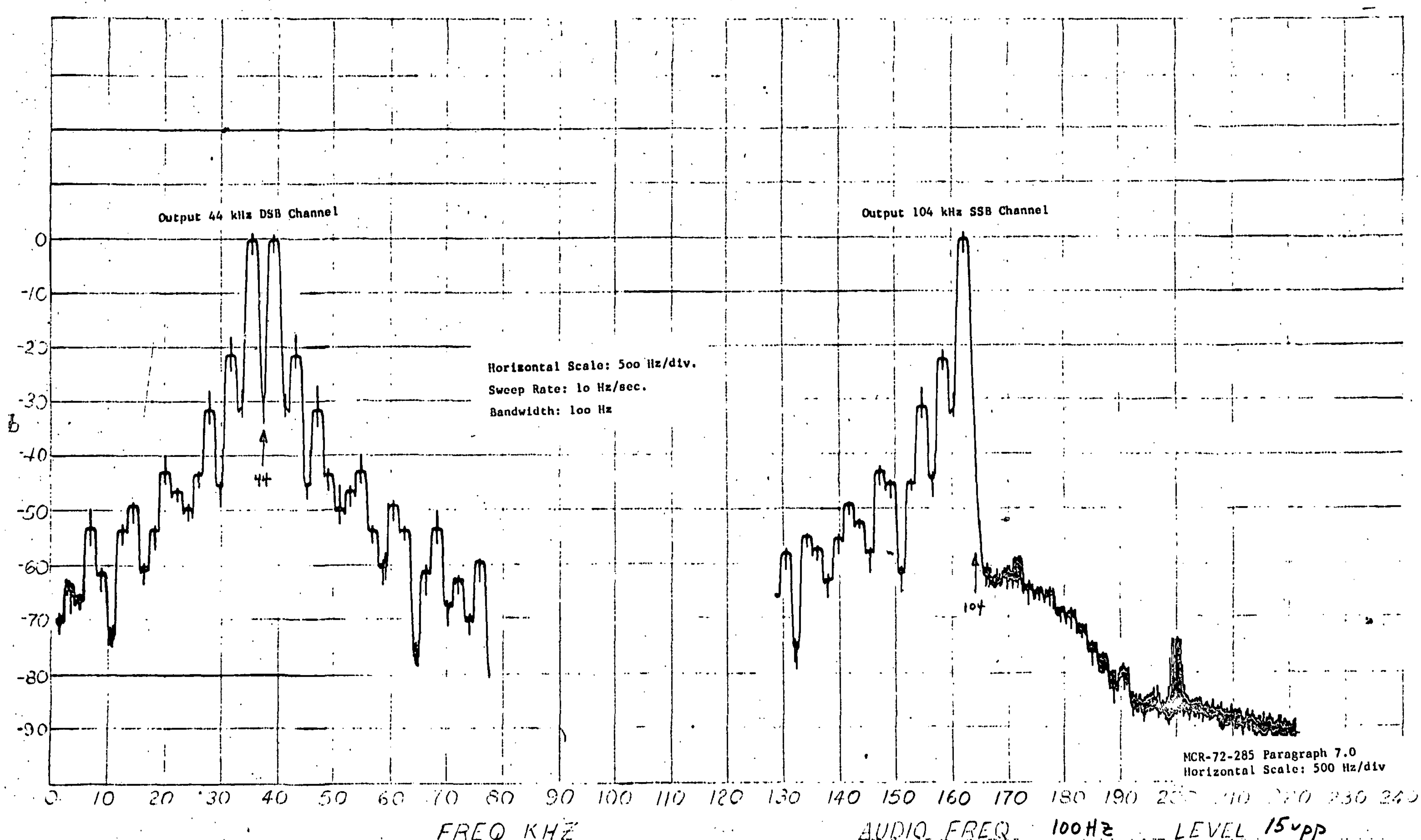

88
90
92
94
96
98
100
102
103.92 kHz
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
0 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150 160 170 180 190
FREQ KHZ
MCR-72-285 Paragraph 6.0
Vertical Scale: 1 dB/div
Horizontal Scale: 1.9 kHz/div
Audio Frequencies: 16, 14, 12, 10, 8, 6, 4, 2, and 0.08 kHz
AUDIO FREQ
LEVEL 5vpp
OUTPUT 104 kHz CHANNEL
DATE 10-26-72

FIGURE 11



MCR-72-285 Paragraph 6.0
Vertical Scale: 1 dB/div
Horizontal Scale: 1.9 kHz/div
Audio Frequencies: 8, 7, 6, 5, 4, 3, 2, and 1 kHz and DC

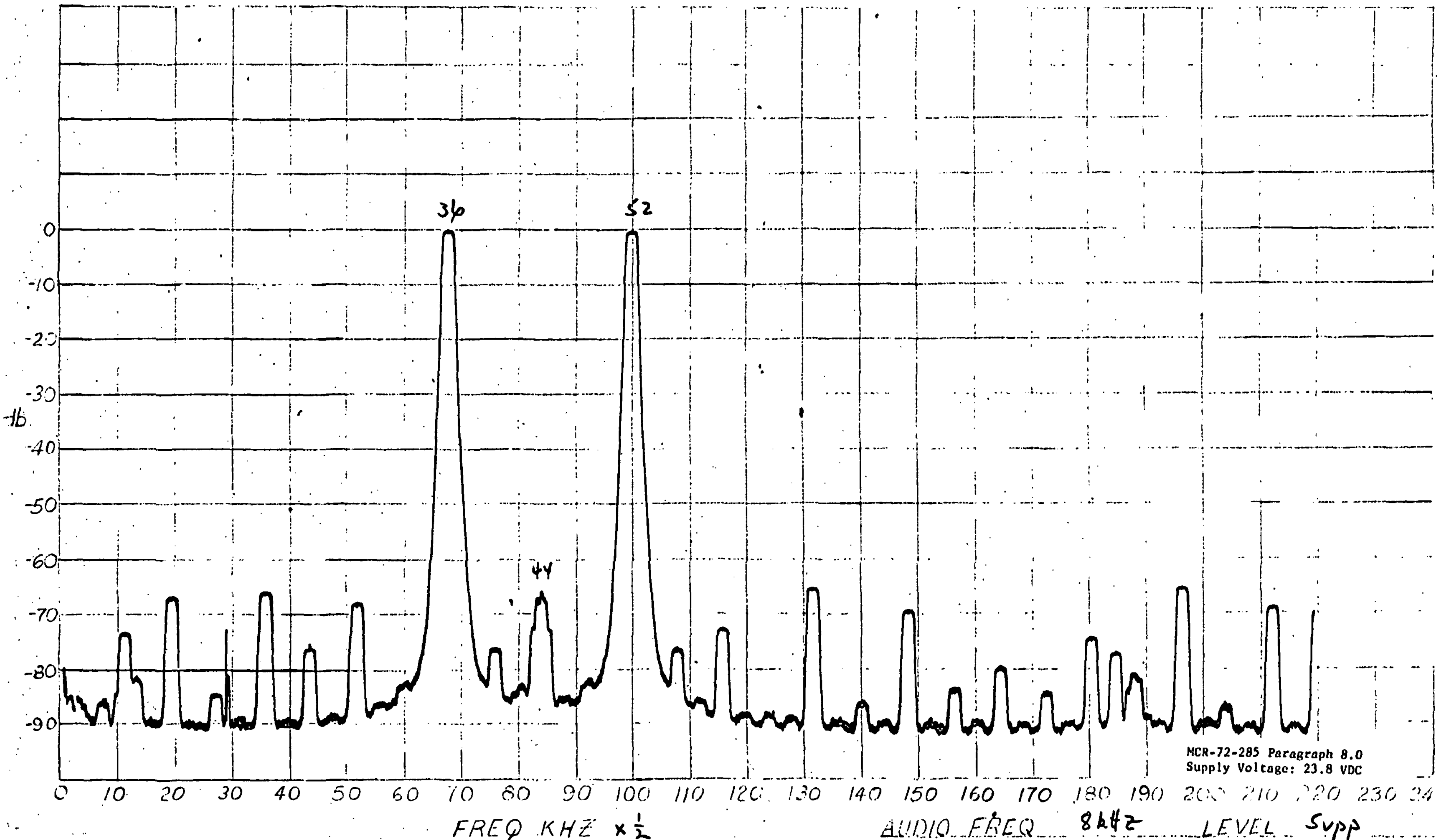
FIGURE 12



MCR-72-285 Paragraph 7.0
Horizontal Scale: 500 Hz/div

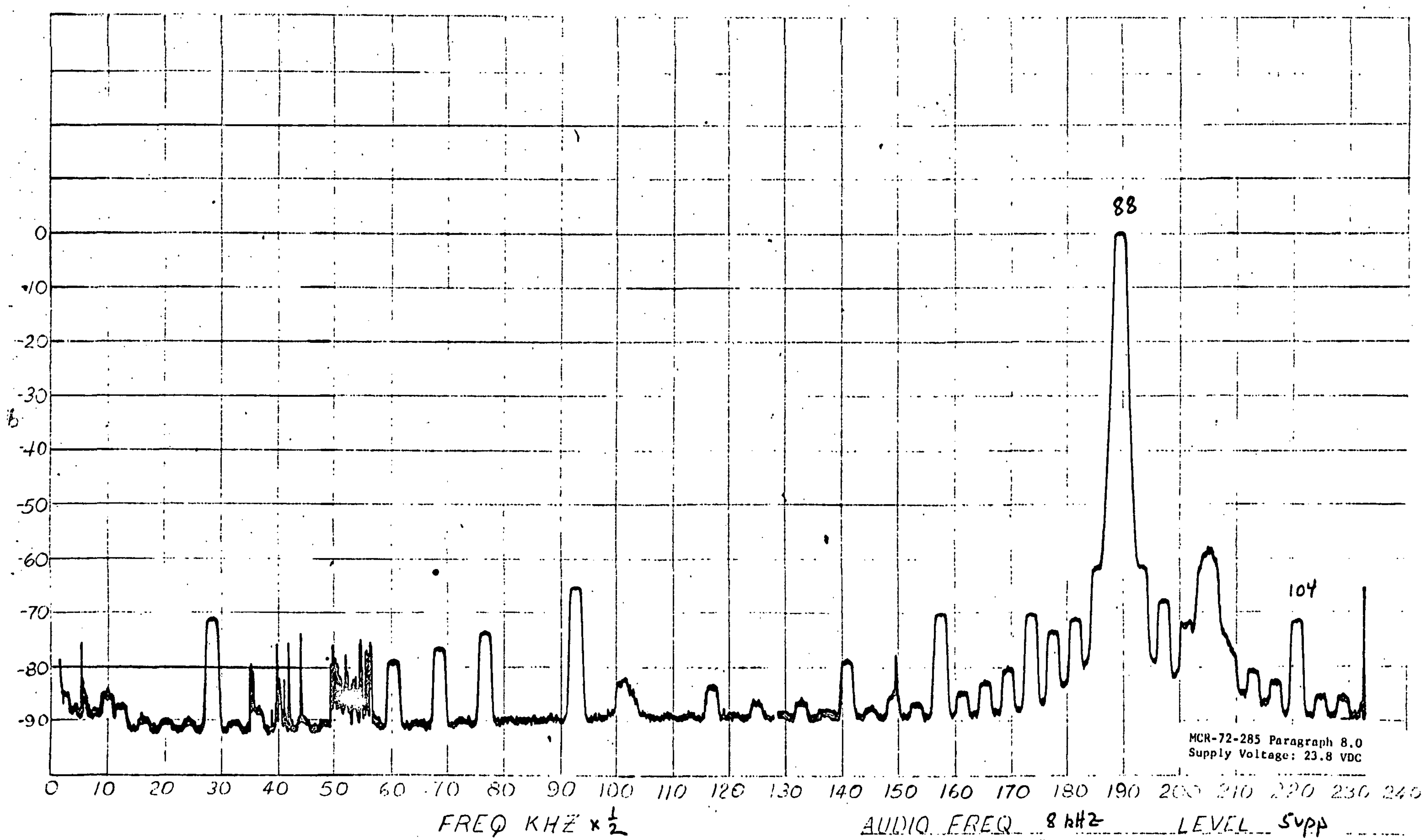
AUDIO FREQ 100Hz LEVEL 15vpp

OUTPUT 44/104 KHz CHANNEL FIGURE 13 10-30-72

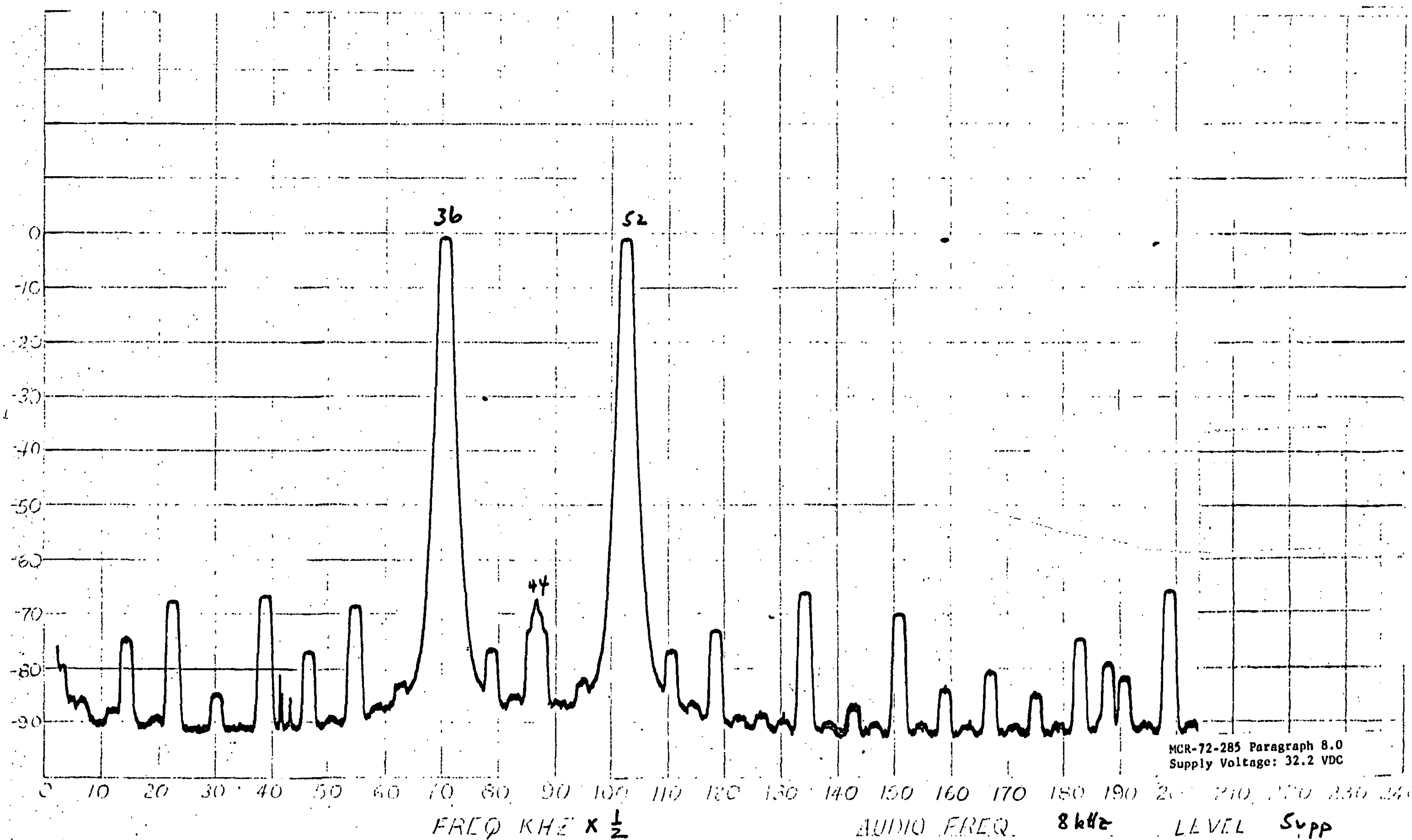


AUDIO FREQ 8 kHz LEVEL Supp

OUTPUT 44 kHz CHANNEL FIGURE 14 DATE 10-30-72



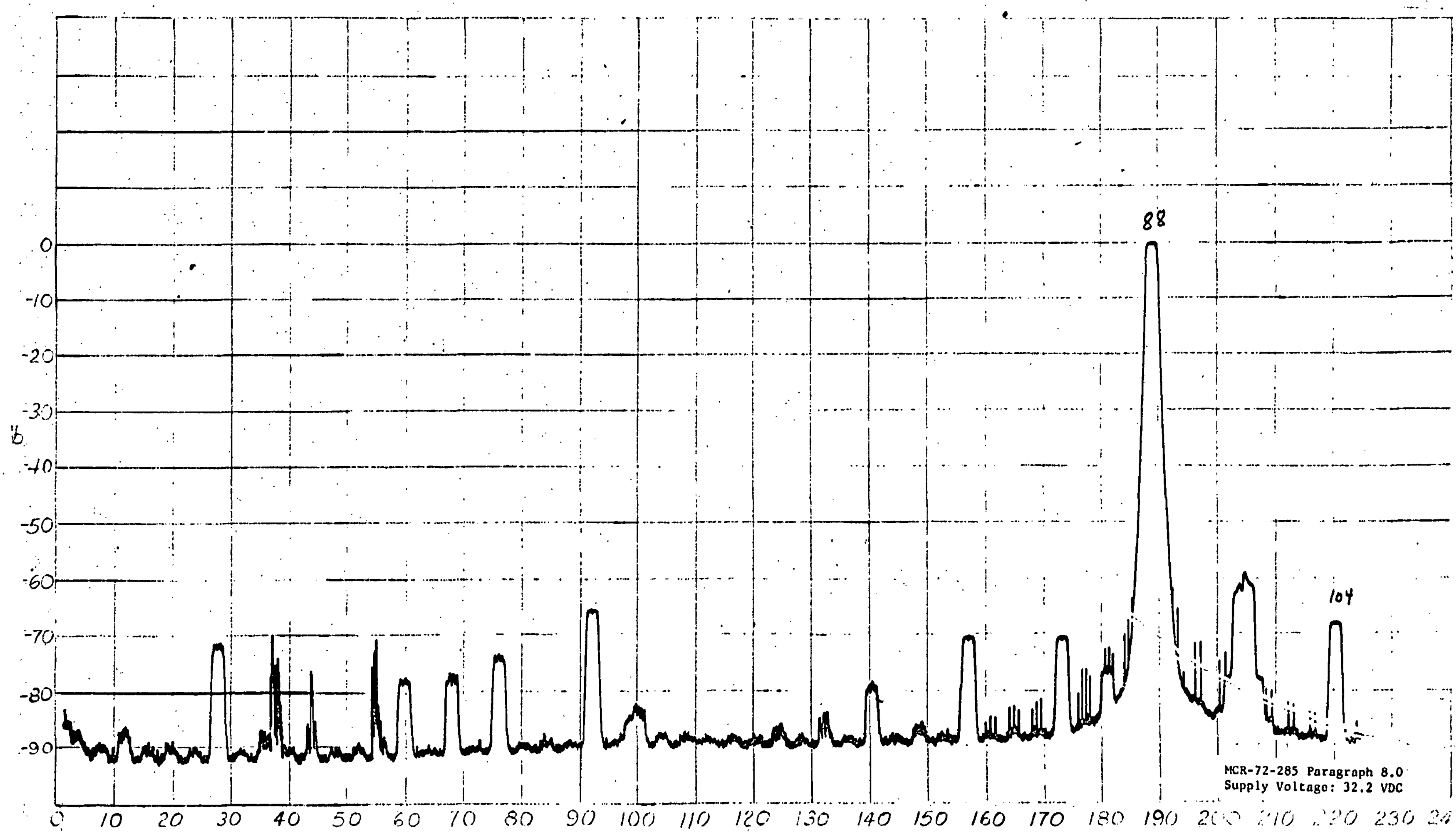
AUDIO FREQ 8 kHz LEVEL 5vpp
OUTPUT 104 kHz CHANNEL FIGURE 15 DATE 10-30-72



MCR-72-285 Paragraph 8.0
Supply Voltage: 32.2 VDC

AUDIO FREQ 8 kHz LEVEL Supp
OUTPUT 44 kHz CHANNEL DATE 10-30-72

FIGURE 16



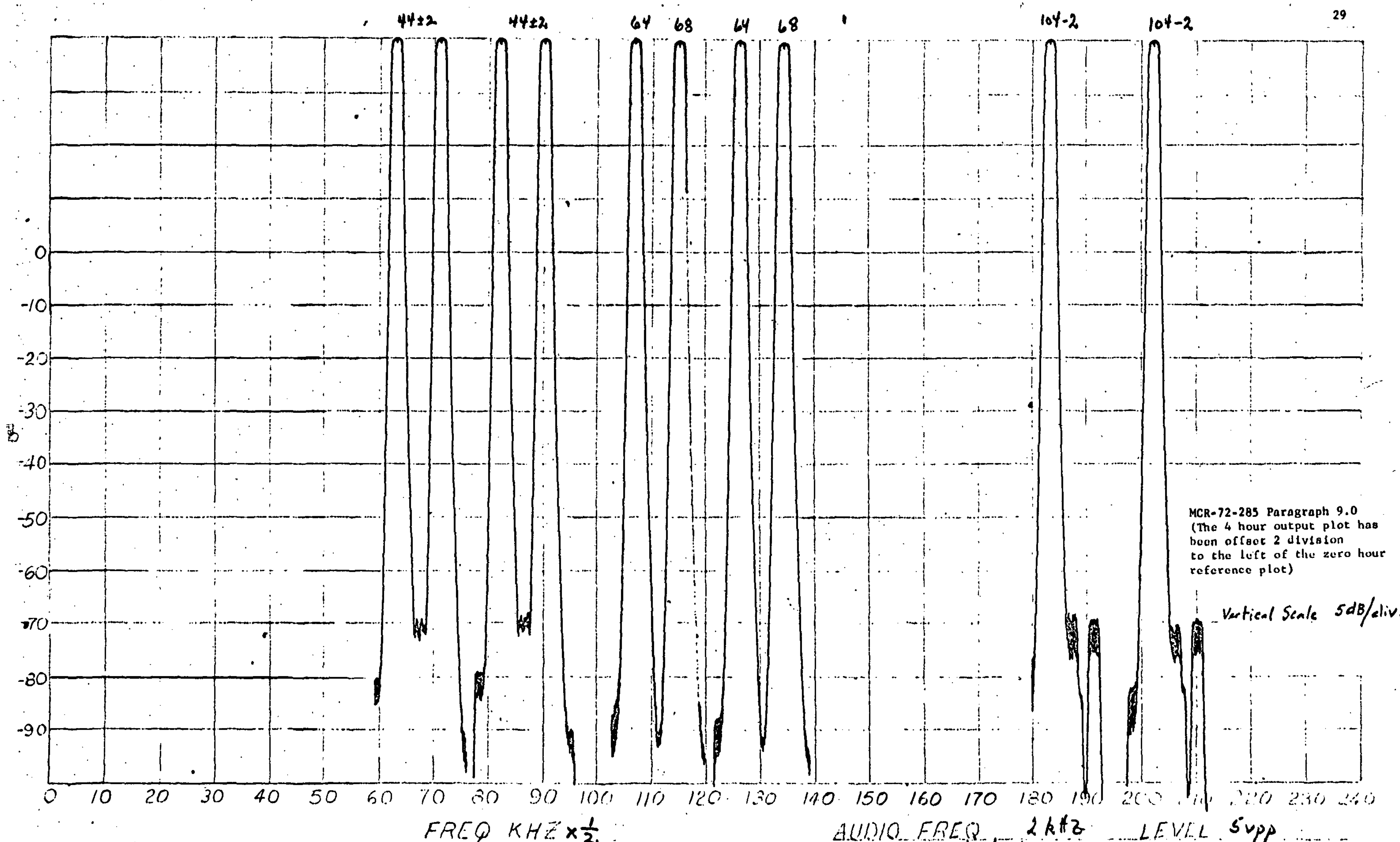
FREQ KHZ × ½

AUDIO FREQ 8 kHz LEVEL 5vpp

OUTPUT 104 kHz CHANNEL

FIGURE 17

DATE 10-30-72



AUDIO FREQ 2 kHz LEVEL 5vpp
OUTPUT 44/64/68/104 CHANNEL

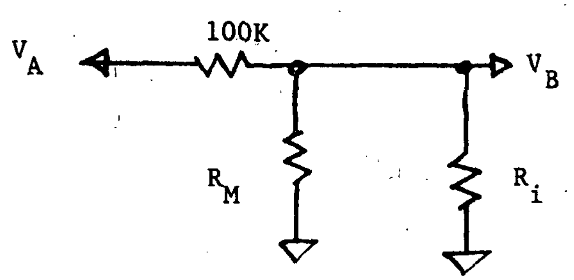
FIGURE 18

DATE 10-31-72

MCR-72-285 Paragraph 10.0

CHANNEL INPUT IMPEDANCE

	44 kHz CHANNEL	104 kHz CHANNEL
V_A (RMS)	1.768	1.768
V_B (RMS)	0.858	0.858



R_M = Meter Impedance = 2M ohms

R_i = Channel Input Impedance

The calculated input impedances of the two channels are approximately 99.2 k ohms.

FIGURE 19

MCR-72-285 Paragraph 11.0

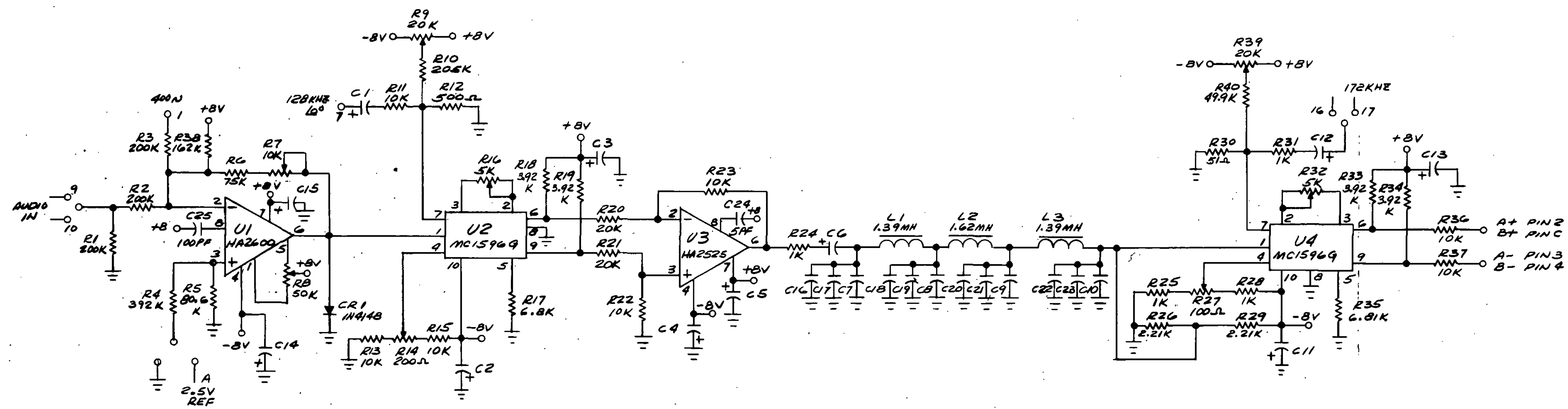
BACK CURRENT

	44 kHz CHANNEL	104 kHz CHANNEL
I_B (pA)	6.3	23

The impedance of the electrometer for the above readings were 10M ohms, and taking this into account the true back current for short circuited channel inputs will be approximately 115 pA for the 104 kHz channel and 315 pA for the 44 kHz channel.

FIGURE 20.

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED



NOTE;

1. ALL CAPS. ARE 2.2 MFD. 20V. KEMET "J" SERIES UNLESS OTHERWISE NOTED
2. C16, C17, C7 ARE 793 PFD
   C18, C19, C8 ARE 1740 PFD
   C20, C21, C9 ARE 1740 PFD
   C22, C23, C10 ARE 793 PFD
3. LAST U NO. 4
   R NO. 40
   C NO. 26
   CR NO. 1
   L NO. 3
4.

	CONN. PIN NO.		CONN. PIN NO.
400N	1	2.5V REF.	A
+A OUTPUT	2	+B OUTPUT	C
-A OUTPUT	3	INPUT A CHAN.	L
-B OUTPUT	4	INPUT B CHAN.	K
128KHZ∠0° A CHAN.	7		
128KHZ∠90° B CHAN.	8		
INPUT A CHAN.	9		
INPUT B CHAN.	10		
128+N4KHZ A CHAN.	16		
128+N4KHZ B CHAN.	17		
GND	18		
-8V	20		
+8V	21		

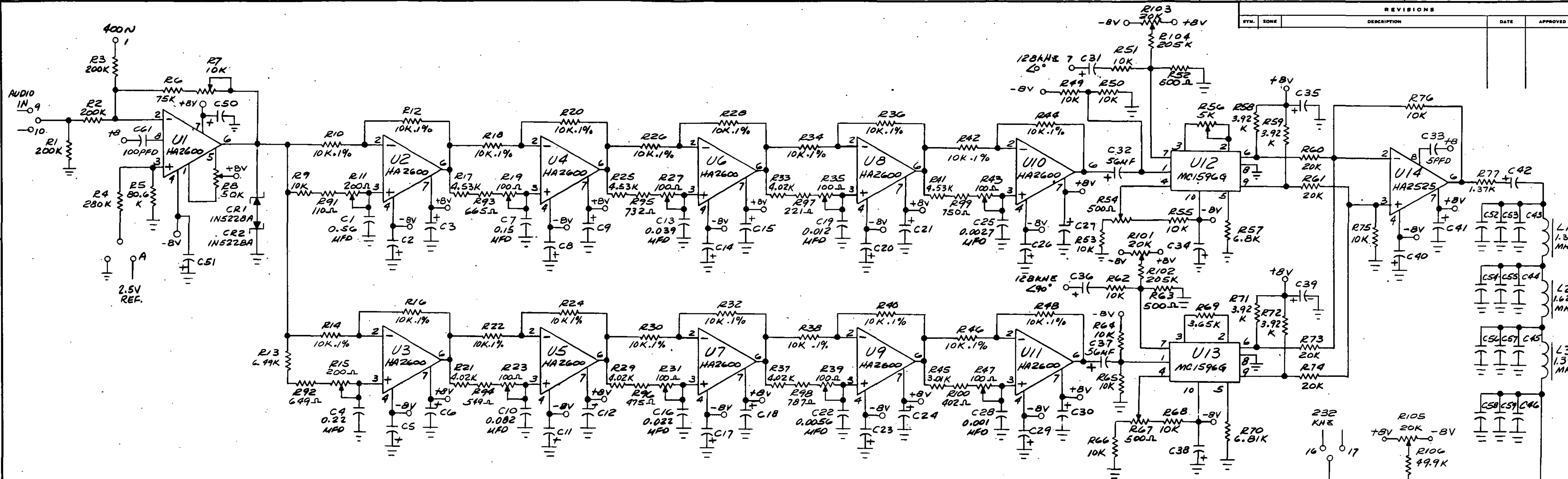
5. PRINTED CIRCUIT LAYOUT NAS8-25987-003

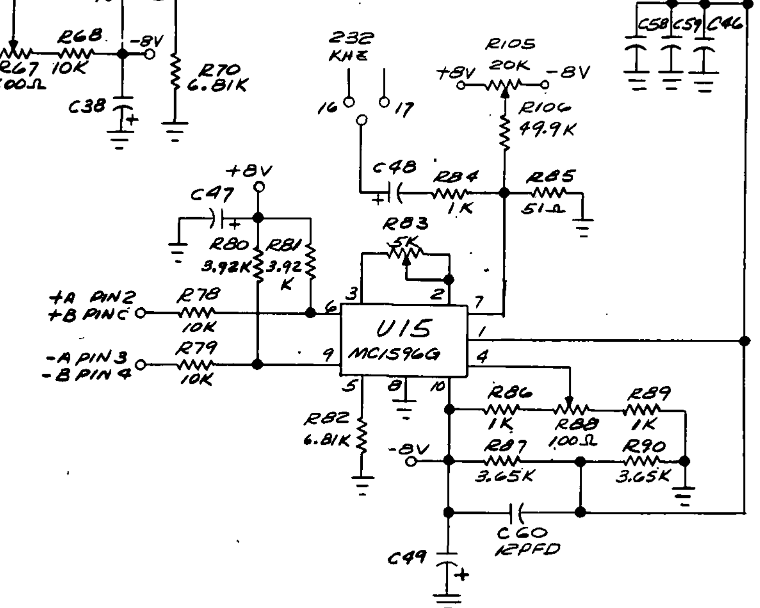
MARTIN MARIETTA CORPORATION
POST OFFICE BOX 179, DENVER, COLORADO

8kHz DSB CHANNEL

SIZE	CODE IDENT NO.	
D	04236	NAS8-25987-001
SCALE		RES 7/72 SHEET 1 OF 1

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED





NOTE:

1. ALL CAPS. ARE 2.2 MFD. 20V KEMET "J" SERIES UNLESS OTHERWISE NOTED.
2. C52, C53 & C43, C58, C59 & C46 ARE 793 PFD
   C54, C55, C44, C56, C57 & C45 ARE 1740 PFD.
3. LAST U NO. 15
   R NO. 106
   C NO. 61
   CR NO. 2
   L NO. 3
4.

	CONN PIN NO.		CONN. PIN NO.
400N	1	2.5V REF.	A
+A OUTPUT	2	+B OUTPUT	C
-A OUTPUT	3	INPUT A CHAN.	L
-B OUTPUT	4	INPUT B CHAN.	K
128 KHz ∠0° A CHAN.	7		
128KHz ∠90° B CHAN.	8		
INPUT A CHAN.	9		
INPUT B CHAN.	10		
128+N4KHz A CHAN.	16		
128+N4KHz B CHAN.	17		
GND	18		
-8V	20		
+8V	21		

5. PRINTED CIRCUIT LAYOUT NAS8-25987-004

MARTIN MARIETTA CORPORATION
POST OFFICE BOX 179, DENVER, COLORADO

16kHz SSB CHANNEL

SIZE	CODE IDENT NO.	
D	04236	NAS8-25987-002
SCALE	RES 7/72	SHEET 1 OF 1

APPENDIX A

MODIFICATIONS TO FREQUENCY DIVISION MULTIPLEXER, CODE 04236, SERIAL No. 001

APPENDIX A has been included in this report for two reasons; (a) to explain the reason for modifying the NAS8-25987-001 printed circuit broad to provide quadrature double sideband on the 44 kHz channel as shown in Figure 4 of this report, and (b) to explain a potential problem area relating to the carrier voltage controlled oscillators in the FDM unit.

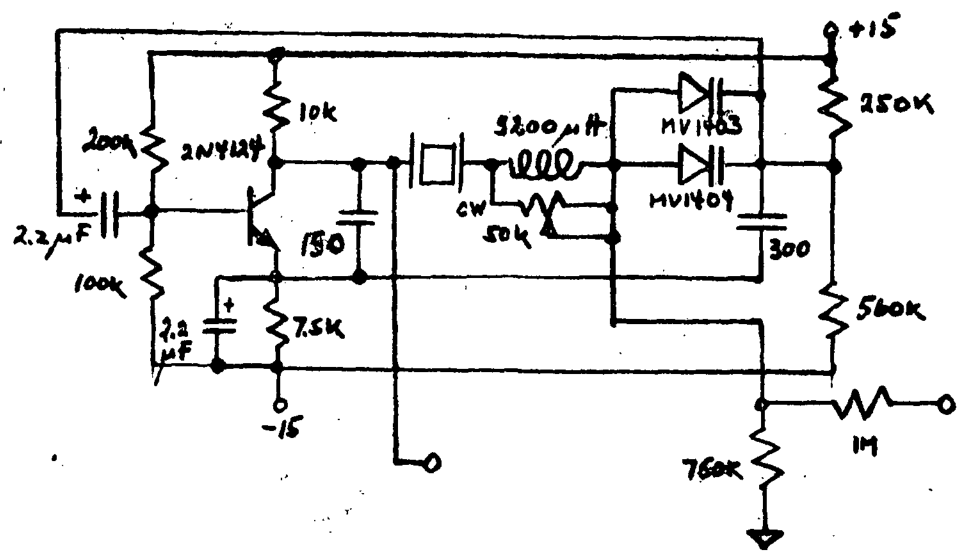
I. FDM UNIT MODIFIED FOR QDSB OPERATION ON 44 kHz CHANNEL

The 44 kHz channel board has been modified through the addition of the circuit shown in Figure 4 of this report. This modification was performed to provide a QDSB signal on the 44 kHz channel for initial tests of the Adcom Model G-146 demultiplexer under Contract NAS8-29039, for which the FDM unit was used to provide the input baseband signal. It should be noted, however, that this modification should only be used for single audio frequency operation, that is, an input signal should only be applied to either the co-phase or the quadrature input at any one time when used in combination with the Adcom demultiplexer. This will provide the proper input signals to the demultiplexer to determine quadrature suppression for any given single frequency within the required bandwidth.

The above circuitry cannot be used to determine quadrature suppression at two different frequencies at the same time. The reason for this is that the 44 kHz QDSB signal passes through three filters in the FDM unit (channel filter plus two in-line filters on the AGC board). Since the phase slope in these filters are nonlinear the average phase of the co-phase and quadrature signals will no longer be 90° apart. There is no phase adjustment in the demultiplexer to rectify this situation, and proper detection can no longer be accomplished. To accomplish the dual quadrature detection on contract NAS8-29039 only the pilot, the reference and the 104 kHz wideband SSB signal were supplied by the FDM unit. The 44 kHz QDSB signal was supplied through modification of previous NAS8-25987 contract hardware (Linear Modulator Breadboard).

II. FDM UNIT VOLTAGE CONTROLLED OSCILLATORS AND PHASE LOCKED LOOPS

The pilot phase locked loop is located next to the FDM unit power supply, and with the printed circuit board in place in the unit the temperature build up may tend to pull the VCO crystal frequency, and loop cycle slippage may occur. An added problem in this particular loop is that the 768 kHz crystal used was a spare part which tends to run slightly above the required frequency. Extreme frequency pulling is, therefore, required to bring the frequency within the loop lock-in range. The pilot VCO has therefore been rebuilt as shown below. (The original loop is shown on Schematic Diagram 24682-109, MCR-70-304; Final Report Contract NAS8-24682)



The result of the above redesign is an increase in loop gain and capture range by a factor of 2. Also the pulling range of the crystal, or the initial adjustment range of the VCO, has been doubled.

The gain of the VCO using the MV1403/1404 varactor combination is:

$$K = 4.5 \text{ Hz/volt at } 768 \text{ kHz}$$

Referred to the 2 kHz comb locking frequency we have:

$$K = 4.5 \cdot \frac{360}{384} \cdot 2\pi \text{degree/sec/volt} = 29 \text{ dB}$$

The phase detector gain is:

$$K_{pd} = \frac{2.5 \cdot 2 \cdot 10^3}{90 \cdot 128 \cdot 10^3} \text{ volt/degree} = -68 \text{ dB}$$

Taking the loop amplifier DC gain as 100 dB the total loop gain is 61 dB.

Referring to Section VIII of Report No. MCR-72-81, Linear Modulator Final Report, Contract NAS8-25984 Modification 4, which contains an extensive treatment of phase locked loop theory, we now can find the required conditions for loop lock-in.

$$2\pi \cdot \Delta f = AK\,Kpd \sin\theta$$

where Δf = open loop difference between the VCO frequency and the input pilot

AK Kpd = loop gain

θ = Phase error in the locked condition

From the above we have that AKKpd = 61 dB referred to the 2 kHz comb frequency. Assuming that the pilot loop is in the locked condition with phase error no greater than 1°, the corresponding VCO maximum offset frequency will be:

Δf = 61 - 16 dB = 45 dB = 0.5 Hz with respect to the 2 kHz comb frequency. From this it can be seen that the gain of the pilot loop is adequate to provide better than 1° phase error at VCO frequency offsets up to 192 Hz referred to the 768 kHz VCO frequency.

The capture range of the loop (the loop unity gain crossover) is at approximately 0.3 Hz. Referred to the 768 kHz VCO frequency this amounts to a required initial VCO frequency adjustment to within 110 Hz of the wanted frequency.

The redesign/rebuild of the pilot VCO pulling range permits the initial capture of the system comb. The increased loop lock-in range will keep the loop in proper lock for crystal frequency drift versus temperature of up to 0.002% in the negative direction and 0.02% in the positive direction.