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Volume II

Final Report

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Long-Life Assurance Studies of EEE Parts and Packaging

Long-Life Assurance Study for Manned Spacecraft Long-Life Hardware

MARTIN MARIETTA

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LONG-LIFE
ASSURANCE STUDIES
OF EEE PARTS
AND PACKAGING

LONG-LIFE ASSURANCE STUDY
FOR MANNED SPACECRAFT
LONG-LIFE HARDWARE

Approved

R. W. Burrows

R. W. Burrows,
Program Manager

MARTIN MARIETTA CORPORATION
P. O. Box 179
Denver, Colorado 80201

FOREWORD

This document is Volume II of a five-volume final report prepared by Martin Marietta Corporation, Denver Division for the National Aeronautics and Space Administration, Manned Spacecraft Center (NASA-MSC) under Contract NAS9-12359, *Long-Life Assurance Study for Manned Spacecraft Long-Life Hardware*. This study was performed with J. B. Fox, Manned Spacecraft Center, as Technical Monitor and R. W. Burrows, Martin Marietta, as Program Manager. Acknowledgment is made to the individual contributors identified in each volume and to R. A. Homan and J. C. DuBuisson, Task Leaders for the electrical/electronic and mechanical areas, respectively.

The five volumes submitted in compliance with Data Requirements List T-732, Line Item 4, are as follows:

Volume I - Summary of Long-Life Assurance Guidelines;

Volume II - Long-Life Assurance Studies of EEE Parts and Packaging;

Volume III - Long-Life Assurance Studies of Components;

Volume IV - Special Long-Life Assurance Studies;

Volume V - Long-Life Assurance Test and Study Recommendations.

CONTENTS

I. INTRODUCTION

I. INTRODUCTION

A. STUDY OBJECTIVES

The objectives of this Long-Life Assurance Study were to develop and document the engineering approach necessary to assure that hardware selected for manned spacecraft is based on the experience gained from the manned and unmanned space programs conducted to date, and will meet the following long-life goal: A five-year operational lifetime goal without maintenance is considered the minimum long-life goal with a 10-year desired operational lifetime.

B. SCOPE

A detailed engineering study was conducted of the design; application; failure mechanisms; manufacturing processes and controls; screen and burn-in techniques; functional, qualification and life testing; and other factors affecting the hardware items under study. The hardware items investigated are listed in Table 1. In addition, special studies of a more general nature, not oriented towards specific parts or hardware items, were also accomplished. The special studies performed are listed in Table 2.

C. APPROACH

The approach included a comprehensive review of the available technical data and an industry survey to establish a baseline for current hardware capability from which improvements for increased life and reliability goals can be assessed. Emphasis was placed on the review of failure history of the hardware as used in NASA and DOD manned and unmanned space and missile programs to ascertain the lifetime and corrective measures necessary to insure long-life operation. For EEE parts a user survey was performed to determine unique or state of the art procurement practices for high reliability parts including test or design specification practices.

Many of the issues discussed are controversial and, while the recommended guidelines are believed to represent the concensus opinion, it should be recognized that some guidelines may require tailoring to specific program constraints and objectives.

Table 1 List of Hardware Items Studies

EEE Parts and Packaging (Volume II)

1) Monolithic Integrated Circuits;

2) Hybrid Integrated Circuits;

3) Transistors;

4) Diodes;

5) Tantalum Capacitors;

6) Relays;

7) Switches and Circuit Breakers; and

8) Electronic Packaging.

Components (Volume III)

9) Electric Motors and Bearings;

10) Accelerometers;

11) Gyroscopes and Bearings;

12) Compressors and Pumps;

13) Magnetic Tape Recorders;

14) Plumbing Components and Tubing;

15) Check Valves;

16) Pressure Regulators and Solenoid Valves;

17) Thermal Control Valves;

18) Pressure Vessels and Positive Expulsion Devices;

19) Ni-Cd Batteries; and

20) Transducers.

Table 2 List of Special Studies (Volume IV)

1) Temperature Cycling as Employed in the Production Acceptance Testing of Electronic Assemblies (*Black Boxes)*

2) Accelerated Testing Techniques

3) Electronic Part Screening Techniques

4) Industry Survey of Electronic Part Derating Practice

5) Vibration Life Extension of Printed Circuit Board Assemblies

6) Tolerance Funneling and Test Requirements

D. ORGANIZATION

This final report is divided into five volumes for convenience; viz:

1) Summary of Long-Life Assurance Guidelines;
2) Long-Life Assurance Studies of EEE Parts and Packaging;
3) Long-Life Assurance Studies of Components;
4) Special Long-Life Assurance Studies, and;
5) Long-Life Assurance Test and Study Recommendations.

In this volume, Volume II, the specific studies identified in Table 1 are presented in eight separate chapters. The guidelines derived in each study are summarized at the beginning of each chapter. The remainder of each chapter is a review of the data accummulated during the study concerning Life Limiting Problems and Solutions, Test Methodology and Requirements, and Process Control Requirements. A recommended parts list is included for each study which is addressed to a specific part type.

The guidelines and data were derived from surveys of industry, government agencies, and the literature. The guidelines presented are believed to represent the consensus of opinions as of this publication date. Pertinent minority opinions are presented in the texts of the individual studies.

II. MONOLITHIC INTEGRATED CIRCUITS

by E. J. Sinclair

II. MONOLITHIC INTEGRATED CIRCUITS

A. INTRODUCTION

Integrated circuits comprise the most significant failure risk among the electronic parts. An analysis performed by the Planning Research Corporation involving 304 spacecraft from 41 programs[1]* yielded the following failure rates for in-orbit spacecraft:

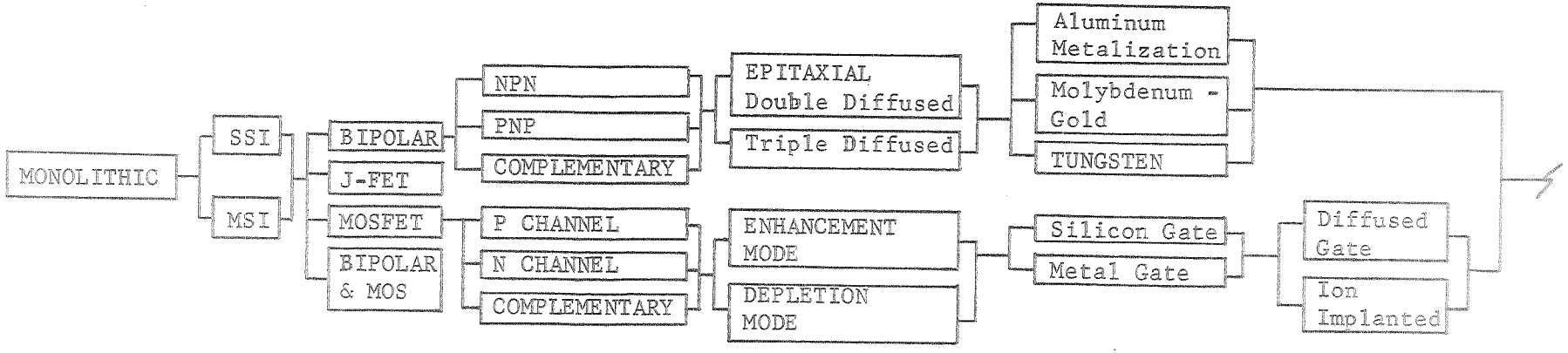
Part Type	Failure Rate/10^9 hr (Upper 90% Confidence)
Integrated Circuits	26.0
Transistors	3.1
Diodes	2.8
Capacitors	1.5
Resistors	2.0

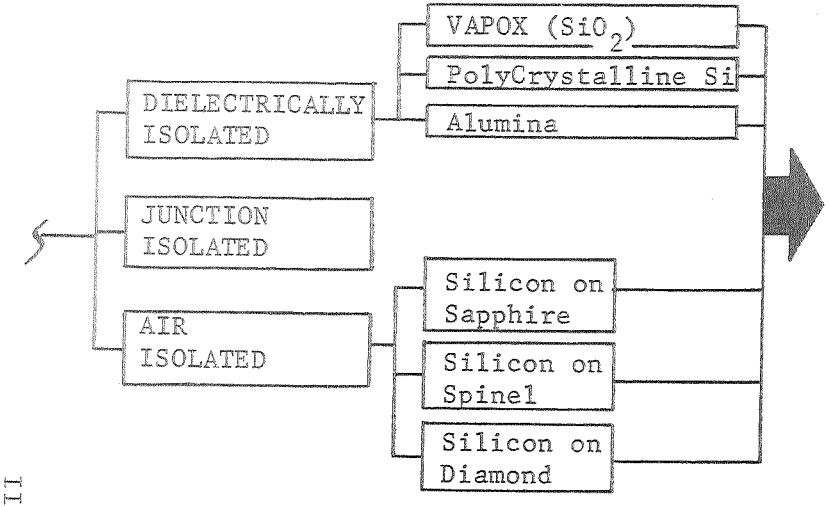
An industry survey conducted by Martin Marietta Aerospace[2] developed a corroborating value of 30 failures/10^9 hr. Although these failure rates (26 or 30 failures per billion hours) seem small, the chance that a 5000-logic element computer, without redundancy will survive for 1 yr without a failure is only 27% and essentially 0% for a 10-yr period. The relatively high failure rate of integrated circuits, coupled with the large number of these devices used in complex digital equipment justifies considerable effort toward more reliable devices as well as extensive redundancy.

*Superscripts identify references listed in section H of this chapter.

This chapter includes the failure mechanisms, test methodology, and process control requirements as related to monolithic integrated circuits only. Those topics as related to hybrid integrated circuits are contained in Chapter III. The information herein is further limited to small-scale integrated (SSI) circuits and medium-scale integrated (MSI) circuits, generally defined as up to 10 equivalent gating functions, and from 10 to 100 equivalent gating functions, respectively. Large-scale integrated (LSI) circuits with complexity of greater than 100 equivalent gating functions have also been avoided here because they are a specific topic being investigated by the National Aeronautics and Space Administration George C. Marshall Space Flight Center (NASA-MSFC).

In discussions related to failure mechanisms, process control, and test methodology of integrated circuits, the descriptive terminology *Monolithic* and *SSI* or *MSI* are totally insufficient. Figure 1 illustrates a few of the many variations in processing that have tremendous influence on the discussions. Furthermore, this report is concerned with the full temperature range, hermetically sealed type of part and is specifically not intended to include *plastic* parts or commercial quality limited range devices.





Other variations include:

Zener or Schottky barrier diode protection.

Glassivation of total silicon surface under metalization, over metalization, or on metal surfaces only.

Crystal orientation of MOS in 100 or 111 plane.

Deposition of silicon nitride for control of MOS gate characteristics.

Vertical or lateral bipolar transistors.

Beam-lead, Flip-chip or Eutectic die attach.

Monometalic or gold-aluminum interconnects.

Thermocompression or ultrasonic lead bonds.

Figure 1 Process Variations

B. GUIDELINES FOR LONG LIFE ASSURANCE

The life expectancy of properly constructed and applied integrated circuits is greatly in excess of 10 years. Failures are caused first by defects introduced during manufacture and second by errors in test, handling, and application. Wearout is only a minor problem that is alleviated by derating. The guidelines that follow will enable use of integrated circuits with minimum probability of defects and a practically indefinite service life.

1. Design Guidelines

1) Use phosphosilicate glass over the thermal oxide with a maximum thickness of 0.24 micron to getter surface sodium contamination.

2) Use silicon nitride or other glassification over the chip to protect the SiO_2/Si interface from external sources of channel-including contamination, immobilize residual contamination, and protect the chip surface from handling damage and particulate shorts. Since glass will not adhere satisfactorily to gold, the moly-gold system will require an additional layer of molybdenum atop the gold.

3) Use eutectic alloy bonding of chip to header which will withstand 300°C storage temperature without degration because epoxy or other polymer bonds do not provide the bond strength, the thermal conductivity, or the temperature capability of eutectic bonds. (Does not apply to beam lead or flip chip devices.)

4) Use monometallic system for chip metalization, interconnect wires, and bonding pads of external leads to eliminate formation of intermetallic compounds that result in poor bonds. There are no established advantages in the use of either aluminum or gold with respect to the effects of radiation of space or nuclear power sources such as RTGs.

5) When using aluminum metalization, the thickness must be at least 10,000 Å to avoid oxide step defects, window microcracks, and dangerously thin metalizations.

6) Maximum design-use aluminum current density must be 5×10^4 amp/cm^2 to minimize electromigration effects.

7) Use high-temperature glass in package lead seals because low-temperature glass has high lead oxide content that can be reduced and short external leads.

8) Use hermetically sealed packages only with a maximum leak rate of 1×10^{-8} Atm cc/sec to eliminate contamination of the integrated circuit from external use ambients. Plastic, epoxy, and silicone encapsulation methods are not presently developed to the point where moisture traveling up the lead has been satisfactorily controlled.

9) Prohibit use of cadmium-plated packages and control use of organic material because nonsubliming materials are preferred in space applications. Acceptable package materials are Kovar, gold-plated Kovar, or nickel.

10) The TO-type can and the flat pack are preferred packages for long life usage.

2. Process Control Guidelines

1) Use metalization deposition processes and annealing procedures that result in large uniform grain structures with a minimum grain size of 8 microns to minimize electromigration effects. Wafer should be heated to 300°C or greater during deposition.

2) Use a planetary deposition system for metalization to eliminate shadowing at oxide steps.

3) The following processes must be reviewed and assurance obtained that they are adequate, stabilized, and under proper control by the manufacturers to minimize contamination and metalization imperfections, and to provide high yield, stability, and precise characteristics.

(a) Thorough wafer cleaning at each process step.

(b) Precise mask layout, dimensional control, alignment, and exposure.

(c) Uniform resistivity of basic wafer.

(d) Purity of photoresist, proper application, spin, and bake.

(e) Thorough resist development and post-development inspection.

(f) Controlled depth, rate, angle, and undercut of oxide etch processes and thorough post-etch inspection.

(g) Thorough resist removal.

(h) Precise diffusion or deposition and drive-in, re-oxidation purity.

(i) Precise oxide growth, removal, and epitaxial growth.

3. Test Guidelines

1) Use a 100% non-destructive bond pull test on all devices to detect marginal bonds. Also perform 100% screen, burn-in and precap tests.

2) Submit a wafer sample from each metallization run to a detailed scanning electron microscope inspection to assure uniform and continuous metallization over window cuts and oxide steps, to avoid undercutting and waterfall effects from oxide etch, to detect oversintering, and to verify mask alignment. Inspection at the wafer level is the most economical point in the process sequence for performance. Screening tests are not 100% effective in detecting these faults and further costly processing is avoided.

3) Submit a wafer sample from each metallization run to a profilometer test to verify metallization thickness and avoid electromigration problems.

4) Perform the qualification tests of Group C in MIL-M-38510 in sequence on the same group of parts as opposed to performing the tests in parallel. This will impose the additive effects of environments that are more realistic to real life use. Also, the screening effectiveness can be evaluated.

4. Application Guidelines

1) Circuit voltage transients should be limited and static charge precautions should be followed in handling because built-in protective circuits are not generally provided and circuit damage must be avoided.

2) Case temperature should be limited to $85^{\circ}C$ to minimize temperature dependent failure mechanisms.

3) Current-limiting should be provided when interfacing with the similar circuits so that power dissipation limits will not be exceeded.

4) Reduce fanout to 80% of the rated maximum to increase reliability by derating.

5) Derate linear circuits as follows so that end of life drift characteristics will be considered in product design.

   (a) Initial offset voltage, ±½ mv

   (b) Initial bias current, X2

   (c) Offset current, X2

   (d) Open-loop gain, ±20%

   (e) Slew rate, ±20%

   (f) Common mode rejection, ±20%

   (g) Power supply rejection, ±20%.

5. Special Considerations

1) Use established processes and material/process combinations whose failure mechanisms are well known. New or unique processes, such as amorphous semiconductors are characterized by a lack of understanding of the basic principles by which they operate. Failure mechanisms, life capability, and reliability are unknown.

2) Use parts with established reliability history as first choice, considering the possibility that parts with the longest history may be superseded by improved techniques of design or processing. Parts without sufficient data must be thoroughly evaluated before approval.

3) Use parts that are available from several sources in active production. During a long-term program, the probability of a single supplier discontinuing production is increased.

4) Identify a production lot of all parts resulting from a single metalization deposition run because the metalizadeposition process is responsible for some failures.

C. SUMMARY

1. Failure Mechanisms

It is apparent that most faults in integrated circuits are due to operator oversight or error, and that only a minor portion are inherent in the materials and processes. Fortunately, most operator caused faults are detectable by a good screen. Approximately 50 failure mechanisms are detailed in this report, although most of the faults are detected through a quality screening and are never delivered by a supplier. The failure mechanisms that a high reliability program must be concerned with are basically those that are time-dependent or that are intermittent in operation. The major faults in this category are:

1) Surface ionic contamination - Resulting in gradually increasing leakage currents, to a level where transistors will not turn off.

2) Surface particulate contamination - Due, in a majority of cases, to solder balls introduced into the package during final sealing, and resulting in intermittent short circuit operation.

3) Microcracks at oxide steps - Generally caused by thin metallization on the vertical walls of the cuts through the oxide layers. This condition is further aided by undercutting in the oxide layer resulting in metallization "waterfall" effect, and by oversintering the metal to silicon contact, which allows the aluminum to diffuse into the bare silicon.

4) Electromigration in aluminum metallization - This is a physical phenomena in which the metal is physically transported toward the more positive points of the conductor. The rate of migration is highly dependent on temperature and current density in the conductor. Scratches in the metal that reduce the cross-section, thus increasing the current density, are the major site of migration failures.

5) Wire bond separation - Wire bond separation is due to several causes:

   (a) Intermetallic formation of aluminum metallization and gold wire, resulting in voids and disappearing metallization;

(b) Underbonding resulting in insufficient adherence of the wire to the interconnecting pad;

(c) Overbonding resulting in extreme reduction in wire cross section at the heel of the bond, and separation under mechanical stress;

(d) Contamination in the bond area causing incomplete adherence;

(e) Corrosive substances on the wire or in the bonding areas that further corrode the bonds or wire.

2. Design

Selection criteria become extremely important in long-life assurance; parts must be thoroughly investigated before approval to ensure that they do not contain basic design weaknesses. A typical example of this situation is the "709" operational amplifier, which failed in a "latch up" condition during Mariner 8 launch. In addition, the construction techniques must be known to properly define failure mechanisms, the history must be reviewed to ensure satisfactory operation under use environment, production must be checked to ensure the part is in active production and will *remain* so, for the length of the program. Another factor of design, just as important as proper selection of parts, is the proper application in system design. The application guidelines define the electrical/mechanical and thermal derating that must be applied as safety factors, along with transient protection and interface requirements.

3. Test Methodology

Present methods of qualification and screening tests have been reviewed and found unsatisfactory for long-life assurance. This section contains the present tests and sequence and the tests and sequence as revised and recommended for high reliability. The basic change in qualification consists of serial tests for additive effects as opposed to parallel testing to MIL-M-38510. Screening tests were revised to incorporate wafer tests and inspections to detect specific failure mechanisms such as insufficient metalization, and surface contamination.

4. Process Control Requirements

The basic processes involved in manufacturing integrated circuits are identified, and the impact of poor control is detailed. All processes in production of the parts are considered critical. Selected processes are defined as necessary in the long-life configuration of circuits.

5. Parts List

A basic selection of specific integrated circuits having a high-reliability history are identified by commercial part numbers and selected parameter limits. These parts should be used as the basic start for a complete long-life parts list.

D. LIFE-LIMITING PROBLEMS AND SOLUTIONS

1. Failure Mechanism Analysis

To provide the proper screening, controls and qualification testing required of integrated circuits for long-life assurance, the failure modes of the circuits must be identified, then an understanding of the physical or chemical cause of the failures must be understood, and finally, test and screening conditions must be defined that will accelerate the degradation of each mechanism, wherever possible. The screening tests must be devised so a minimum number of tests will aid in detection of a maximum number of inferior parts.

A number of failure mechanisms can be avoided merely by prohibiting specific materials, such as polymer encapsulation to eliminate moisture susceptibility, certain corrosive effects and thermal expansion mismatches; combinations of gold and aluminum interconnects; i.e., gold metallization and aluminum wire bonds, or aluminum metallization and gold wire bonds to avoid gold-aluminum intermetallic compounds commonly referred to as various color "plagues"; glass frit used as die bond material to avoid die to header separation under mechanical stress that fractures the glass frit; and external lead to lead leakage by eliminating lead oxide (PbO) sealing glasses.

An additional number of failure mechanisms can be minimized by requiring a thorough and detailed visual inspection, such as scratches on metallization, misalignment of masks in diffusion and etching, diffusion or etching flaws due to contamination or dust particles, misplaced wire bonds, over or under bonding, deformation of wire, cracks in dice due to excess stress, excess slack in lead wires, and particulate contamination.

A third group of failure mechanisms can be readily detected by electrical testing. These flaws include diffusion or metallization flaws causing opens, shorts, reduced voltage breakdown, and excess current leakages.

A fourth grouping of failure mechanisms, much more subtle, requires far more complex testing to detect. These failure mechanisms include incomplete adherence at bonding interfaces; improper cleaning, which allows corrosive substances to remain on the die;

conductors which allow excess current densities, causing migration of the metalization; surface contaminations, which can cause excess surface leakages; and improper etching of oxide in contact windows, which can cause high resistance contacts.

With consideration to the various types of failure mechanisms in monolithic integrated circuits, this section is divided into the following classes or causes of failure:

1) Surface - Failures related to contamination on the surface of the die.

2) Metallurgical - Failures in the metalization system including surface conductors, bonds, and interconnecting wires.

3) Oxide - Failures due to defects in the silicon dioxide or other passivation materials.

4) Mechanical - Failures due to the integrated circuit package.

5) Masking and diffusion - Failures caused by improper masking and diffusions.

6) Bulk - Failures due to faults in the basic starting material--the silicon wafer.

In the discussions that follow, refer to Fig. 2 for an illustrative view of the time-dependent failure modes. This is a composite of the metalization and bonding systems used and would not occur in practice on one single die. These failure mechanisms are listed in Table 1.

a. Surface Contamination[3] - Surface contamination includes any material inadvertantly left on the surface of the semiconductor die or any material introduced in processing that can degrade the surface. These contaminates include corrosive etchants, photo resist, wire lubricant, package sealing materials, lead particles, and loose chips from the die.

1) Corrosive Contaminants - Residue remaining on the die surface, entrapped in undercut areas, in etch pits and in porous areas of metalization can recombine with moisture in the enclosed atmosphere or from moisture retained by improper drying processing. The activated etchants, further aided by high-temperature exposure and time, can result in further etching on the circuit and cause serious degradation.

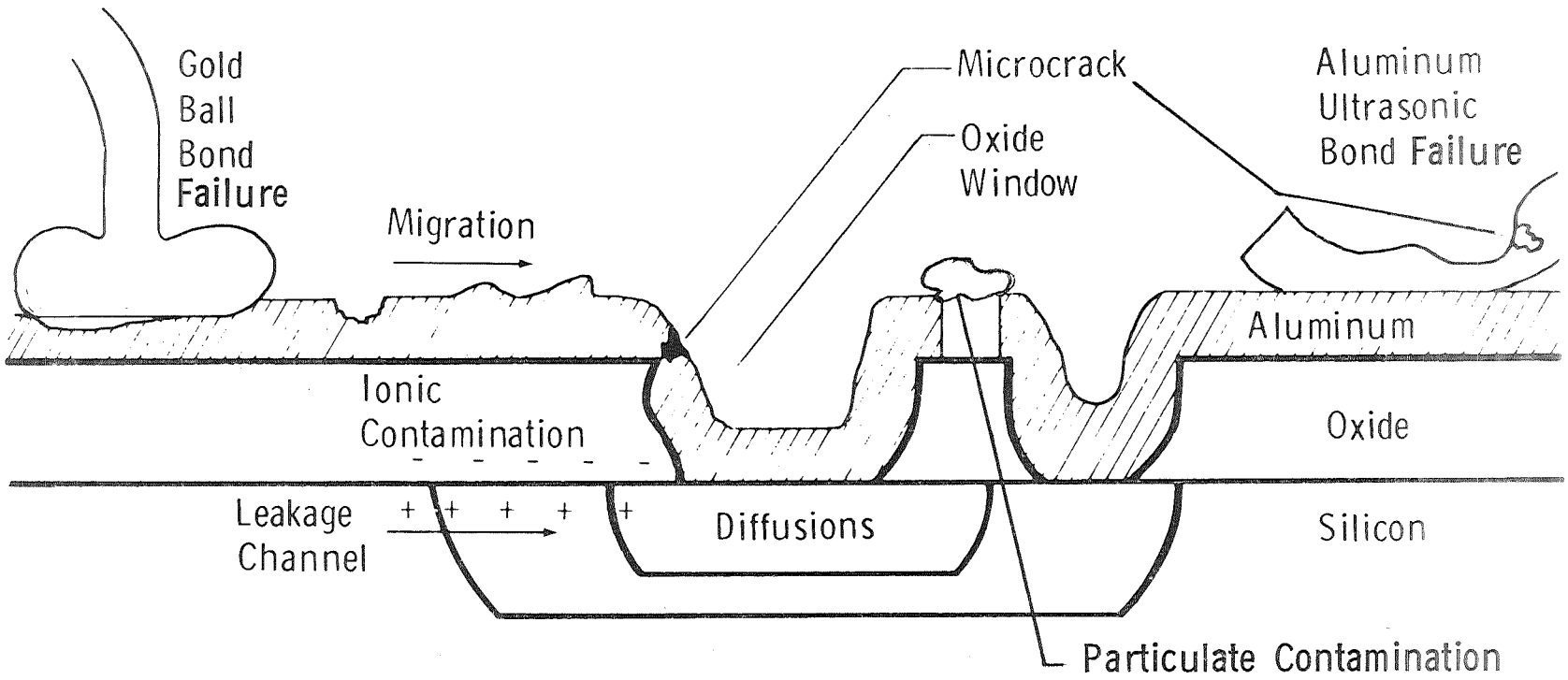


Figure 2 Time-Dependent Failure Modes

General Class Integrated Circuit

Construction Monolithic, MOS and Bipolar

Table 1 Failure Mechanism Analysis (1 of 8) (Surface Contamination)

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Opens due to corrosion.	Entrapped corrosive residue and moisture react on surface causing further etching.	High temperature storage and electrical test.	Microprobe analysis of surface contamination, SEM Inspection.
Parameters out-of-limits due to diffusion faults.	Photoresist and stains on surface caused faulty diffusions.	Visual inspection, electrical test.	Improved resist-removal process control.
Open circuit due to corrosion on wire and bond.	Lubricant on wire drawing die containing chlorine is transferred to wire, causes corrosion later in use.	High temperature storage and electrical test.	Chemical analysis on incoming materials.
Shorts or intermittant operation due to internal conductive particles.	Solder particles from lid or die preform introduced into package in sealing, cause short circuit on metalization.	(a) Monitored vibration or mechanical shock and electrical test. (b) Radiographic	(a) Glassivation on surface over metal. (b) Improved process control in sealing and die attach.
Short circuit due to pieces of internal lead material.	In process of terminating internal leads, or reworking internal wires, particles of wire inadvertently left in package.	Precap visual, radiographic, and electrical test.	Improved precap visual control and surface glassivation.
Open metal due to scratches from die particles and migration.	Loosely attached die chips separated under mechanical stress, scratches metal surface, reducing cross section.	Precap visual for die cracks. Vibration, burn-in and electrical test.	Improved precap inspection

General Class Integrated Circuit

Construction Monolithic, MOS and Bipolar

Table 1 Failure Mechanism Analysis (2 of 8) (Metallurgical)

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Open die metalization	Scratch across metalization opens circuit or allows overload burn-out.	Precap Visual; burn-in and electrical test.	Glassivate surface.
	Metal migration due to insufficient cross-section.	Lot sample on SEM and profilometer.	(a) Limit design current density. Glassivate to retard migration. (b) Require molygold, or control Al. thickness and grain size.
	Overalloying of thin metal causes open around contact windows.	Precap visual, SEM inspection at wafer and die stages.	(a) Control minimum metal thickness. Define alloying time/temperature. (b) Require molygold.
	Microcracks at oxide steps due to steep etch angle and thin metal.	SEM inspection at wafer stage. Thermal stress and electrical test.	Control oxide etch rate and metal thickness. Require planetary deposition chamber.
	Corrosive etch-through of metal from photoetch residue.	Visual inspection; burn-in and electrical test.	Control wash processes at supplier. Perform microprobe analysis of surface areas.
	Open due to electrolytic action from internal moisture and contamination.	Visual inspection. SEM inspection, burn-in and electrical test.	Control moisture content of internal atmosphere.
	Lifted bonding pad, torn metallization from poor adhesion and mechanical stress.	High "g" acceleration or shock and X-Ray or electrical test.	Control cleaning process.
	Improper mask alignment, open at insufficient window coverage.	Precap visual. Burn-in and electrical test.	Inspect wafer for alignment prior to committing parts to hi-rel.
	Flaking Aluminum	Visual Inspection, SEM, electrical test.	Require other type of metal.
	Overetched	Visual, SEM, electrical	Improved process control.

General Class Integrated Circuit

Construction Monolithic, MOS and Bipolar

Table 1 Failure Mechanism Analysis (3 of 8) (Metallurgical)

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Shorted die metalization.	Underetched.	Visual inspection, SEM, electrical test.	Improved process control
	Smeared metal	Visual Inspection, SEM electrical test.	Glassivate surface.
Increased Resistance of metalization.	Increasing thickness of aluminum due to temperature and atmosphere.	Electrical test.	Glassivation over aluminum

General Class Integrated Circuit

Construction Monolithic, MOS and Bipolar

Table 1 Failure Mechanism Analysis (4 of 8) (Metallurgical)

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Open Interconnect Wires	Formation of gold-aluminum compounds (plague) at wire bond interfaces.	Precap visual, mechanical stress and electrical test.	(a) Control process (b) Require monometallic interconnect systems.
	Overbonding or underbonding allows separation at bond.	Precap visual, mechanical stress and electrical test.	Require 100% non-destructive bond pull.
	Corrosive open in lead wire or at bond due to chlorine ions in wire drawing lube.	Precap visual, burn-in and electrical test.	Chemical analysis required on incoming materials at manufacturers.
	Lead wire melted open due to nicks and high current.	Visual precap, burn-in and electrical test.	Process control required in handling wire to prevent scratches and nicks.
Shorted interconnect wires	Excess lead length and deformation allows short to each other, header, or die.	Precap visual. Mechanical stress and electrical test.	Specify maximum slack allowable.
	Wires shorted at crossover due to wire deformation.	Precap visual. Mechanical and electrical test.	Prohibit crossover of wires.

General Class Integrated Circuit

Construction Monolithic, MOS and Bipolar

Table 1 Failure Mechanism Analysis (5 of 8) (Oxide Defects)

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Excess reverse current due to inversion layer.	Leakage channel across reverse biased PN junction from ionic build-up.	High temperature reverse and electrical test.	Improved process control on surface cleanliness. Apply Phosphosilicate glass over oxide to immobilize ions.
Parameters shorted or out-of-limit due to diffusions through faults in oxide.	Oxide cracks/crazing due to thermal mismatch and mechanical stress on thin layer of oxide.	Electrical test.	Additional thickness required on oxide layer.
Short due to metal contact through pinhole to silicon.	Faulty oxide growth due to poor photoresist, damage mask, undercut in etch or contamination allows "pinholes" to surface beneath.	Burn-in and electrical test.	(a) Improved process control. (b) Require glassivation prior to metalization.
Severe corrosion on metal surface causing open.	Etchants trapped in etch pits during processing is activated at elevated temperatures causing etching of metal.	High temperature bake and electrical test.	SEM inspection.

General Class Integrated Circuit

Construction Monolithic, MOS and Bipolar

Table 1 Failure Mechanism Analysis (6 of 8) (Mechanical Defects)

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Loss of hermeticity due to fractured glass in seal area.	Thermal or mechanical stress cause glass to fracture.	(a) Visual inspection (b) Seal leak test	Substitute ceramic and metal packages
Short circuit due to internal wires contacting a conductive lid.	Mechanical stress forces wires against metal lid of package.	Radiographic and electrical test.	Control internal clearance and slack of leads.
Package fractured in seal test or handling.	Flexible lid/base not capable of withstanding high pressures in seal leak testing or being held in tweezers.	Visual inspection.	Require calculated seal leak test. Control handling procedures.
Current leakage between leads.	Low resistance path on external surface due to reduction of PbO glass to Pb.	Electrical test.	(a) Require ceramic/metal packages (b) Prevent exposure to reducing environment.
External lead separation at brazed junction.	Brazed lead to pad fractured in handling or improper brazing separated in later handling.	Visual inspection.	Subject all such packages to a non-destructive lead pull.
External leads shorted within glass seal area.	External lead frame not properly spaced when placed in glass seal.	Radiographic and electrical test.	100% radiographic in production prior to using parts.
Seal fracture due to insufficient sealing area.	Cap offset reduces designed seal area allowing fracture in test.	Visual inspection	Provide holding jog for cap alignment through sealing operation.
Poor solderability due to contamination under gold plating.	Gold plating bridges contamination on lead until soldering is attempted.	Solder coating leads.	(a) Require peanut oil reflow on all leads. (b) Nickel flash under gold plating.
Lead separation at glass/ceramic interface.	External plating on leads ends at package interface, allowing corrosion to occur at that pt.	Lead fatigue test.	Require lead coating prior to installing lead frame in package.

General Class Integrated Circuit

Construction Monolithic, MOS and Bipolar

Table 1 Failure Mechanism Analysis (7 of 8) (Masking-Etching-Diffusion)

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
High resistance contact resulting in parameter drift.	Incomplete removal of oxide at contact window causes increasing resistance with time.	High temperature bake and electrical test.	Improved process control.
Misaligned metal masking resulting in open.	Incomplete periphery of windows covered, allows migration.	Burn-in and electrical test precap visual.	Visual inspection of wafer stage. SEM inspection.
Mis-registered or improper diffusion (shorts, opens, out-of-spec.)	Change in electrical characteristics due to improper dimensions and separation.	Precap visual, burn-in and electrical test.	Improved process control.
Open due to overetching or undercutting of oxide or metal.	Undercutting of oxide provides "Waterfall" effect on metal. Undercutting of metal provides traps for etchant and reduces cross-sectional area.	High temperature bake and electrical test.	Improved process control.

General Class Integrated Circuit

Construction Monolithic, MOS and Bipolar

Table 1 Failure Mechanism Analysis (8 of 8) (Bulk Defects)

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Bulk-Concentration Gradients	Lattice strain due to steep concentration gradients finally released as dislocations.	Mechanical stress and electrical test.	
Bulk Impurities	Diffusion into dislocations during epitaxial growth.	Electrical test for breakdown voltage.	
Bulk Resistivity Gradients	Large local stresses causing change in resistance.	Electrical test.	

2) Photo Resist - The incomplete removal of photo resist following each masking and etching process will react as undesirable masks, preventing diffusions in those areas. In addition, if the photo resist is allowed to remain for too long a period, there is a possibility that a stain will be produced that could affect the diffusion process.

3) Wire Lubricants[4] - Materials used in lubricating the wire drawing die can contain chlorine.[5] In the process of forming the wire, traces of the lubricant will adhere to the wire. When this wire is later used as interconnections in integrated circuits, the highly corrosive substance is then able to cause catastrophic corrosion of the wire or to aluminum metalization by migrating to that area.

4) Package Sealing Material - In the process of sealing flatpacks with solder preforms, a very common occurrence[6,7] is the splattering or wicking of this sealing material into the internal cavity of the package. When the lid is seated and scrubbed on the case while the preform is in a liquid state, particles of the molten eutectic can be forced onto the surface of the die and surrounding areas. If the conductive particles do not immediately form a short, they may, at a later time, reorient to cause intermittents or shorts.

5) Lead Particles - In the process of terminating lead wires by breaking the wire and removing excess length, it is not uncommon for the severed particles to fall within the package cavity. Unless these extraneous wire particles are detected during precap visual inspection, particles, large enough to cause shorts between conductors, will remain in the package.

6) Die Chips - Loosely attached chips around the edge of the die can be separated under environmental exposure. Although not highly conductive, these particles can, under vibration or shock, cause damage to leads and portions of the chip surface.

b. Metallurgical Defects - Metallurgical defects are those defects occurring in the metalized interconnection pattern on the surface of the die, the interconnecting wires from die pads to external leads, the bonds at each end of the wire, and the metal eutectic used in bonding the die to the base of the package.

1) Metalization - Metalization defects account for a major portion of the failures in bipolar integrated circuits. Generally, the metalization failures are open circuit. The following faults are included in this category: electromigration, Kirkendall effect (silicon dissolving into aluminum), hillocks and whisker growth, scratches and resultant melting of metal, non-adhesion of metal to oxide, surface reconstruction.

Electromigration - Electromigration is the physical transport of the conductor material by ion migration towards the more positive end of the conductor. The rate of movement of the ions is exponential and is proportional to both the cross-sectional area of the conductor, and to the square of the current (current density squared). The equation used to define the rate is

$$\frac{1}{MTF} = AJ^2 \exp - \frac{\phi}{kT},$$

where

MTF = median time to failure, hr,

A = a constant that contains a factor involving the cross-sectional area of the film,

J = current density, amp/cm^2,

ϕ = an activation energy, Ev,

k = Boltzman's constant,

T = film temperature, °K.

Circuit failures occur where the cross section of the metalization is the smallest (greatest current density), usually at scratches or at oxide steps. The failure mode is always an open circuit. Note that the activation energy of the material is proportional to the structural grain size.[8]

Kirkendall Effect[9] - The Kirkendall effect defines the shift in interface between two bonded dissimilar metals or alloys, usually towards the material with the lower melting point. The shift is due to a greater number of atoms from one material flowing to the other than there are flowing in the reverse direction. The unbalanced flow rate causes the reduced side to become porous or to contain actual voids. When this effect occurs between the

silicon and aluminum, the silicon diffuses faster to the aluminum than is returned, and can leave voids under the metalization.[8] This can cause separation of metal from die and eventual open circuit under mechanical stress.

Opens at Oxide Steps - A significant failure mechanism in integrated circuits is nearly invisible cracks in the metalization at oxide steps. Although ionic migration may contribute to this failure mechanism, it is more commonly believed to be a thermal mismatch problem in which the thinnest metal, occurring at the step, breaks.

A similar failure often occurs around contact windows, except in this instance, oversintering of the aluminum to silicon is the major contributor, with excess aluminum diffusing into the bare silicon.

Overetch/Underetch - Conductor-to-conductor shorts/opens in the metalization can occur due to insufficient etching or overetching, but these mechanisms are very minor because most parts will be detected in visual inspection and electrical test.

Hillocks and Whisker Growth[8] - Hillocks, voids, whiskers and other nondescript extruded appearing formations are growth resulting from migration. Because the rate of migration is proportional to the temperature and current density, locations in the metalization that are at a lower temperature or, due to increased cross section, have a reduced current density will have a lower rate of migration. This accumulation of ions from a region with a more rapid rate tend to settle-out into the noted formations. In a similar manner, voids are formed between a reduced rate and a fast rate region, where ions move out faster than they are replaced. The voids can cause opens, while the growth can cause current leakage or shorts to nearby conductors.[10]

Scratches - Failures due to scratches in the metalization can range from opens with the scratch completely severing the conduction path, reduced cross section (subject to migration or melting open), to short circuit where the metal is smeared to adjacent conductors. Scratches impose a major reliability risk in using commercial grade parts because no precap visual inspection/rejection criteria are required. A thorough visual inspection before capping will detect these faults.

Nonadhesion to Oxide - Lifted pads or other areas where the metalization does not adhere properly to the silicon dioxide surface is basically due to contamination on the surface before metalization. The reliability risk of such a fault is that the thin film metalization is then subject to mechanical testing that was designed for the stronger interconnecting wire and bonds. This is an insignificant failure mechanism and should be detected in visual inspection, mechanical testing, and final electrical tests.

Surface Reconstruction[11] - Through temperature and time, the surface texture of aluminum can change from a smooth surface to a random "combed" look and even include hillocks and whiskers. This change in texture not only fractures glassivated surfaces but may also indicate an increasing sheet resistance. Silicon dioxide (SiO_2) overcoating appears to prevent the problem although the reasons are not clearly understood. Thermal cycling seems to aggravate the condition, whereas the addition of 2% Cu appears to retard it. The general causes of this phenomenon appear to be diffusional creep of the material.

Flaking Aluminum[12,13] - Aluminum conduction films have been found to break up into smaller areas that tend to flake off from the film. This effect generally occurs within 10 mils of a silicon contact area. Silicon migration into the film tends to precipitate at grain boundaries of the aluminum. This produces more distinct and wider boundaries that appear to have less cohesion to the silicon dioxide and result in the separation.

Increased Conductor Resistance[14] - A high temperature bake increases the thickness of the surface oxide on aluminum conductors. This increasing resistance could possibly cause out of tolerance of parameters due to a higher voltage drop in the conductor, or cause a thermal rise in the metal that would speed up electromigration.

Other failure mechanisms, all very minor, include hydrate of the aluminum film, lateral migration under the oxide and improper routing of the conductors.

2) Interconnecting Wires - Failure mechanisms of the interconnecting wires include reduction in the wire size by "necking down" due to excess tension of the bonding machine or high g forces applied to the part. This reduction in cross section in the wire is then subject to failure by overheating or mechanical separation. Lead wires of insufficient length or improper dress can fail under thermal cycling. Excess lead length can allow lead to lead or lead to case shorts under mechanical stress.

3) Wire Bonds - Overbonding (excess pressure/temperature) often results in cracked die, particularly when there are voids under the die. Additional problems include formation of oversized gold-ball bonds allowing the bonds to overlap the bonding pad and possibly short to edge of die or excessive necking or cracking of aluminum ultrasonically bonded wires providing a point that will break under thermal stressing.

Underbonding (insufficient pressure/temperature) results in weak bonds that will separate under mechanical and thermal stresses.

The formation of numerous intermetallic compounds (plagues: purple, black, tan, white, yellow, etc) can occur when gold wire is bonded to aluminum metalization. This phenomenon is the subject of many detailed studies with conflicting conclusions. The compounds appear to provide weak or brittle bonds or increased contact resistance. The Kirkendall effect further weakens the bond due to the formation of voids in the aluminum. Bonding to contaminated surfaces can provide weak bonds, similar to underbonding, except that visual inspection will not easily detect the fault.

Thermocompression bonding of aluminum wires has an unsatisfactory history of cracks at the heel of the bond, which later failed under power cycling. This type of bonding should not be permitted in long-life parts.

4) Die Bonding Failures - Typical die attach materials are (1) epoxy, (2) glass frit, and (3) metal eutectic. Typical faults include poor adhesion due to improper temperature or scrubbing action; incomplete coverage of bonding material over the total interface area; dice canted from the plane of the header; and particles of attachment material splashed on die surface or other areas on the header and pedestals of bonding material that can break free.

Specific faults associated with the individual bonding material are:

1) Epoxy - This material may outgass organic material that can contaminate sensitive surfaces such as MOS. The long-term physical properties of this material are unknown, therefore, the holding strength, brittleness, thermal conductive properties, and rate of contamination cannot be defined for long-life parts and the material should not be used.

2) Glass frit die bonding (low-temperature glass) - Glass should not be used in packages that can be flexed such as flatpacks or dual-in line packages with a Kovar base. When pressure is applied, the base will flex causing fracture of the glass and possible die separation.

3) Metal eutectic - A unique failure mechanism is associated with eutectic die bonding. To properly attach to the eutectic, the dice must first be coated on the reverse side with a gold film, at the wafer stage. Unless the gold backing is properly applied, a separation will occur between the backing and the silicon.

c. Oxide Defects - Oxide defects are those faults occurring in the silicon dioxide or other surface passivation layer. These defects account for a major portion of the failures in MOS circuits due to the high impedances, but a much lesser portion in bipolar circuits. The defects in this classification account for inversion, channeling, pin-hole shorts, and leakages and diffusion errors. In general, the defects lead to increased current leakages or shorts from the metalization to diffusion areas or substrate, or to excess leakages across diffused junctions.

1) Inversion[15] - When PN junctions are biased in the reverse direction, inversion layers grow in strength over the surface adjacent to the junction due to motion of ions on the surface of the oxide. The field exerted through the oxide tends to produce inversion layers on both the n-region and p-region that lead to increases in reverse current. For thermally grown oxides, the positive charges within or on the oxide induce a negative charge on the silicon, making it n-type.

2) Oxide Cracks or Crazing[10,15] - Due to the mismatch in thermal expansion rate of silicon and silicon dioxide, mechanical stresses can be set up at the interface, when the wafers are cooled from >1000°C to room temperature. Thin oxides are particularly susceptible to cracking. Diffusion through oxide is then possible.

3) Pinholes[16] - Pinholes in the oxide may vary in depth, and, at worst case, expose the silicon surface to the metalized interconnections on the oxide. In instances where the pinhole or metalization does not extend completely to the surface of the silicon, a time-dependent migration or low-voltage breakdown mechanism may be introduced. These pinholes can be caused by faulty oxide growth, a damaged mask, poor photoresist or an undercut by the etching process.

4) Etch Pits[15,17] - The presence of triangular[15] or truncated triangular[17] pits have been noted in the surface of dry oxide grown on the 111 crystal orientation of silicon. The specific cause of the pits has not been defined. The dimension of the pits vary from 500 to 1000 Å on a side and about 200 Å deep. The etchant entering these pits does not exchange rapidly with the bulk solution nor with the neutralizing and rinse liquids; thus, the pores or pits become traps retaining sodium contamination and corrosive agents.

d. Mechanical Defects - Mechanical defects are those basic faults of package construction or the processing errors in the assembly of the constituent parts.

The defects include the following:

1) Package - The TO-type can and the flat pack are the only packages that can be recommended for high reliability, long-life use. The dual-in-line (DIP) package was developed specifically for computer and other high volume applications. The package is designed for automated insertion into printed wiring boards or sockets and wave or flow soldering (through the board attachment). Due to the heavy lead material, excess stress can be exerted on the glass seal area in the through-the-glass type construction. Also, due to the longer rectangular dimensions, excessive torque can be exerted on this seal during insertion of the parts and any flexing of the circuit boards. Extensive damage has occurred to the sealing glass, requiring retrofit of space systems. (NASA MSC PPIN No. NB-L-335-72, MMC Skylab Alert No. F3-72-12, MSFC Alert No. MSFC-A-72-12.) The externally brazed on lead type of construction has, in the past, experienced fracture of the braze and separation of external leads.

   Other disadvantages of the DIP include:

   (a) The weight of a DIP is approximately six times as great as an equivalent 14-lead flatpack.

   (b) Due to the stand-off of the leads, the center of gravity of a printed wiring board is shifted significantly when a quantity is attached to one board.

(c) The leads are aligned outward at an angle from the vertical (positive loaded) for automatic insertion and self-retention, therefore, when inserted by hand, each lead must be sprung in toward the center line and forced into the hole (feedthrough), thus, each lead is subjected to individual stress and possible contamination or damage.

(d) With the package in the fully inserted stand-off position, all thermal conduction must be through the leads. Since the body is not in contact with the surface, it cannot contribute to the thermal conduction.

Therefore, dual-in-line packages cannot be recommended for use in long-life high reliability applications.

2) Glass fracture - Unique to the glass to metal and glass to ceramic sealed package is the possibility of fracture of the sealing glass between leads under thermal or mechanical stress causing loss of hermeticity.

3) Solder balls - The packages with metal lids are normally sealed using solder preforms. A major failure mechanism of this package is the introduction of solder balls from the preform into the interior of the package resulting in short circuit or intermittent operation.

4) Short circuit to cap - An additional failure mechanism of the Kovar or other metal lidded package is the possibility of shorting leads to the conductive lid when subjected to mechanical stress. This is a very minor failure mode and is detectable in electrical test.

5) Crushing - The thin metal lid and/or metal base packages are very likely to be damaged if subjected to the normal high pressures encountered in seal leak testing. There is also a high probability of damage if these packages are handled by the case with tweezers, because very great pressure can be excited on the flexible lid or base.

6) Glass reduction - The glass used in final seal of a package *must* be of a low temperature melting point to avoid subjecting the die and bonds to high temperature. One of the basic constituent materials required to provide a low melting point in the glass is lead oxide (PbO). This material is very susceptible to reduction to metallic lead (Pb) by exposure to reducing agents. The resulting lead (Pb) on external surfaces will provide a low resistance short between leads.

7) Separation of brazed leads - Packages consisting of thick film conductors through the walls with external leads brazed to external pads has a major failure mechanism consisting of fracture and separation of the lead brazing. Any external pressure on the leads is transferred directly to the brazed junction. Once a fracture is started, very little force will break the lead free of the package.

8) Lead frame shorts - A failure mechanism that has occurred on a very minor number of parts is the shorting of the external lead frame inside the glass or ceramic walls. This mechanism is detectable by electrical test and radiographic inspection.

9) Cap offset - Although packages are designed with sufficient sealing area, the assembly of the lid on the package can be offset in a manner that will considerably reduce the designed contact area. This reduction in seal area results in a part much more susceptible to seal failure under thermal or mechanical stress.

10) Lead plating - The typical Kovar leads on packages are normally gold plated. If the basic Kovar lead material is contaminated or contains excessive iron oxide on the surface, the gold plating may bridge the fault. When such a part is then soldered to a circuit board an unsatisfactory joint occurs, making the external connection very susceptible to mechanical failure.

11) Corrosion at glass/ceramic interface - The general processing method in manufacturing integrated circuits is to plate the lead *after* sealing it into the case material. This process leaves a very small junction of glass to lead or when the glass miniscus is broken, a much larger area of the basic lead material is exposed to all environments and subject to corrosion and failure.

e. Masking, Etching and Diffusion -

1) Improper Ohmic Contact - The formation of a high resistance contact between the metalization and the silicon diffused areas at windows in the silicon dioxide is usually the result of incomplete removal of the oxide in the contact areas before depositing the aluminum on the wafer. This condition may temporarily heal under application of voltage, but can be reestablished by high-temperature stabilization bake or storage. Thus, this failure mode is considered time dependent.

2) Misregistration of Metalization - Reduced metalization coverage at windows is due to the misalignment of metalization masks before etching. The optimum condition in alignment is to completely cover the window contact areas and provide conduction paths in 360° from the silicon surface to the metal atop the silicon dioxide. A very slight misalignment of the metalization masks can result in only two sides of a window and oxide step having conduction paths. This provides a much greater chance of open circuit due to migration or oversintering (annealing).

3) Misregistered or Improper Diffusions - Diffusions that are due to misalignment of masks reduce the base and emitter or base and collector junction spacings. Other faults include discontinuous isolation diffusions and odd shapes on edges of diffusions possibly due to dust particles on masks. These faults can change transistor and resistor characteristics to a degree that circuit operation is affected.

4) Undercutting of Oxide or Metalization - Overetching can cause undercutting of oxides allowing a waterfall effect in metalization that is highly subject to heating and migration effects and thermal microcracks. Undercutting of metalization produces reduction in cross section. Both the undercutting of metal and oxides provides traps for etchants and other contaminates that can result in time degrading or corrosive effects.

f. Bulk Defects - Bulk defects are those occurring in the basic silicon starting material. These defects account for only a minor portion of the failures in integrated circuits. The defects in this classification are dislocations, impurity diffusions and precipitations, etch pits[18], and resistivity gradients resulting from mechanical and thermal shock[19]. These defects can lead to diffusion spikes, which, in turn, cause hot spots, voltage breakdown, and other deviations from the desired electrical characteristics. Such defects are usually induced in the crystal-preparation process.

The steep concentration gradients found in epitaxial diffusion result in crystal lattice strain. This strain is subsequently released by the formation of dislocation structures that contain edge components perpendicular to the concentration gradient. The chip is structurally weaker at the dislocation fault plane; thus bulk failure can be triggered by mechanical stress.

Deviations in epitaxial growth, resulting in impurity diffusion, are another source of bulk failures. Impurity diffusion is more likely along edge dislocations, particularly along the arrays of edge dislocations that form small-angle grain boundaries. The precipitation of impurities at the resulting crystal-lattice-orientation fault planes is believed to lower the reverse breakdown voltage in epitaxial devices.

Resistivity gradients caused by a heat differential between the center and the outer surface of the chip can result in secondary breakdown. Large local stresses can cause changes in resistivity and, hence, in electrical characteristics. These local stresses can be caused by mechanical shock or vibration, which would generally result in microphonics. The stress levels usually would have to be so high as to be destructive in other areas (seals, bonds, etc). Sufficiently large stress concentrations can crack the die.

It has been determined that the major number of dislocations occure at depths of 2000 to 6000 Å below the oxide interface.[20] This subsurface dislocation count was greatly reduced by annealing the wafers for 17 hr at 900°C.

2. Design

a. Integrated Circuit Selection Criteria - The criteria for selection of integrated circuits for a long-life program must be thoroughly and clearly defined, and enforced, to avoid rejection of the parts in a later phase of the program. If a part is initially approved, even tentatively, it is then too late, economically, to reject it; immediately upon *tentative approval*, the requestor who finds the part characteristics advantageous will *design-in* the part in a system. The penalty in cost of redesign and rescheduling may then become prohibitive.

Therefore, in the selection of integrated circuits for long-life assurance, particular attention must be paid to manufacturing processes and materials that contribute to long-term stability or instability. Those processes with known wearout mechanisms or time-dependent failure mechanisms that affect the life of the program *must* be identified and carefully avoided, or minimized. In addition, parts should be selected that minimize the potential failure mechanisms detailed in the previous sections of this chapter. The following details are summarized in Table 2, which appears after Subsection 2.a.11).

1) Chip Fabrication - Both silicon nitride and phosphosilicate glass (PSG) overcoatings have been found to greatly enhance the reliability and improve the surface stability of both MOS and bipolar devices.[21,22,23] These glassivation materials act as gettering agents for sodium ions, thus making the contamination far less mobile. When deposited over the total surface, including the metalization, the material not only provides an excellent protection against metalization scratches but also retards metal migration in the aluminum conductors.[21,22]

Because this one process can minimize four time-dependent failure mechanisms (flaking, inversion, scratches, and migration), it becomes a very important selection criterion for long-life parts.

2) Chip-to-Header Bond - Experience has proven glass frit die bond as totally unsatisfactorily in Kovar-glass packages.[6] Due to the brittleness of the frit, the material separates when the parts are subjected to mechanical shock and when the packages are flexed. The intent of the referenced NASA-ALERT is to prohibit the use of glass frit die bonding in any package that can be flexed.

The long-term effects of epoxy and other polymer die-attach materials is unknown and, therefore, should be avoided, especially because the final characteristics depend on the proportions of adhesive and hardener and the time and temperature of curing. Furthermore, because many of the polymer die-attach materials are filled with silver to increase thermal conduction, and the migration characteristics of silver are well established, this type of material should not be used. Therefore, eutectic alloy die attach should be the only material approved for dice attachment.

Beam lead attachment has great reliability potential but requires further development. The "bump" or flip-chip process has proven unsatisfactory in past usage by one major commercial manufacturer, and is not generally acceptable at this time.

3) Internal Interconnection Wires - Monometallic internal interconnect systems are a necessity for long-life assurance. Therefore, gold wires are mandatory with gold metalized dice and aluminum interconnecting wires with aluminum metalized dice. From an overall reliability standpoint, the all-gold system must be the recommended process for long-life assurance: the gold ball bonding process has many years of production history; the gold metalization system, although presently only used on one major production line, is nearly unaffected, in comparison to aluminum, by

the effects of electromigration, microcracks, and other reliability problems encountered on the aluminum systems. In addition, the gold system appears to provide greater advantages in the development of beam-lead processing.

The aluminum system also has specific advantages:

Availability - The all-aluminum system is presently available on nearly all parts from all suppliers;

Economical - Since the aluminum system is in general production, it is far less costly than imposing the all-gold system requirements on suppliers.

However, the ultrasonic bonding process is very complex and stringent controls must be imposed if this bonding procedure is to be used for devices intended for aerospace applications where very high reliability is required.[24] The operator, the machine, and the materials involved all interact to affect the strength and reliability of ultrasonic wire bonds.

4) Metalization - Electromigration has been found to be proportional to the current density in an aluminum conductor.[8,25] The density will be much greater at the thinnest point along a conductor because the current remains constant while the metalization becomes less. Therefore, parts having metalization scratches, reduction by etching, or thin metal at oxide steps will be far more susceptible to failure at those sites. Methods of minimizing the problem of thin metal are (1) require metal thickness that is approximately the same as the maximum oxide depth, to provide sufficient cross section at the steepest oxide steps, (2) control the design of the part so that current density will be less than 5×10^4 amp/cm^2 or as further defined by a specific program, (3) control grain size of the metalization to >8 microns, and (4) glassivate the surface over the metal.

5) Established Processes - Regardless of the potential reliability gain possible by approval of newer processes, the risk cannot be assumed on long-life assurance programs. Until a process is thoroughly evaluated and the failure mechanisms identified, an efficient screening program cannot be defined. Therefore, unproven processes must be given important consideration in the selection criteria.

Processes that fall into the unproven or insufficiently evaluated category include beam-lead devices, bump or flip-chip processing, and amorphous semiconductors. Also field programmable and reprogrammable memories are apparent improvements that require additional evaluation before acceptance, just as are some of the newer die metalization materials, interconnection wires, and bonding capabilities.

6) Package Sealing Glasses - Low-temperature sealing glass is another example of a material with a known failure mechanism that can be avoided in many instances. These solder glasses contain a high lead oxide (PbO) content that can be reduced to metallic lead by exposure to reducing agents.[26] Wherever possible, selection criteria should specify high-temperature glass or ceramic in the external lead sealing area.

Other undesirable materials include polymers[27] (epoxy, silicone, plastics, etc) in seal areas due to poor hermetic capability and moisture resistance in addition to corrosive capability and poor thermal expansion characteristics. For long-term reliability, seal leak rate also plays an important part in selection of parts. A seal leak rate of 1×10^{-6} ATM cc/s will allow the internal atmosphere of a part to be replaced with external atmosphere 100 times while an equivalent package with a leak rate of 1×10^{-8} undergoes one internal atmosphere replacement. The moisture and contamination possibilities are obvious.

7) Usage History - A prime consideration in the selection of parts must be usage history. The more extensively a part is used, the more knowledge is gained of applicable failure mechanisms and the more efficient development of screening techniques. Past usage also aids in the identification of time-dependent failure mechanisms that may not be detected in screening.

The possibility of obsolescence in part selection criteria becomes very important in long-term programs. Replacement parts must be available in the event of testing errors, or the resultant redesign could have tremendous schedule and packaging impact. This is one example when usage history must be declared of secondary importance.

8) Multiple Procurement Sources - Multiple sources for parts must also be considered in the selection criteria for parts. The rapid growth in the field of integrated circuit manufacturers, the merging of many of the firms, and the present trend of even

major manufacturers to withdraw from the scene indicates the necessity for selecting parts manufactured by more than one supplier. Multiple sourced parts are usually more competitively priced, and the competition tends to spur improvements in the product. In addition, a program stands a much better chance of not losing all sources by the failure of one company. Furthermore, multiple sourced parts are usually available with a wider selection of packages and manufacturing process than single source items.

9) External Materials - Selection criteria must include prohibiting the use of subliming or outgassing materials. In long-term use, the systems may be exposed to space environments a multiple of times, thus the contamination effects on surrounding surfaces become additive, providing a time-dependent failure mechanism to those surfaces. In addition, many materials are known to deteriorate with age and environment, so they must be carefully selected.

10) Active Production - The production history of parts is very important in selecting parts for long-term use. Numerous times, suppliers have advertised parts and supplied samples before placing the parts in full production. When the expected market did not materialize, the supplier found it was not economically feasible to place the part in production and ceased further effort. Again design and schedules can be jeopardized.

11) Additional Process Controls - It has been noted that when the substrate is heated to at least 300°C during the deposition of the metallization, the grain size increases to a more desirable level. It was also noted that a much better metalization thickness at the oxide step is achieved if the PSG is kept less than 0.24 micron thick.

Table 2 summarizes the above details.

Table 2 Integrated Circuit Selection Criteria

DESIGN FACTORS	REMARKS
Chip Fabrication	Silicon nitride or other glassivation layer over silicon oxide to protect the SiO_2-Si interface from a source of channel-inducing contamination; to immobilize residual contamination; and, to protect surface from manufacturing damage.
Chip-to-header bond	Eutectic alloy bonding required on other than Flip-chip or beam-lead chips. Alloy must withstand 300°C storage temperature without degradation. Epoxy or other polymer bonding prohibited.
Internal Interconnection Wire	Monometallic bonding system, for chip metallization, interconnecting wire and bonding pad of external leads, to prevent formation of intermetallic compounds. Long life of gold-aluminum systems are questionable.
Metalization	Minimum metalization thickness of 10,000 Å to eliminate oxide step defects, maximum designed current density 5×10^4 Amps per square centimeter. Grain structure of aluminum must be large and uniform to minimize electromigration.
Established Processes	Only those processes whose failure mechanisms are well known should be permitted. New or unique processing such as Amorphous Semiconductors should be prohibited until firmly established.
Package Sealing Glass	Avoid low temperature glass in lead-sealing area. This glass usually has high LEAD OXIDE (PbO) content which can be reduced to metallic lead (Pb), shorting external leads.
Packaging	Use hermetically sealed devices only. Use of polymer (plastic, epoxy, silicone, etc.) encapsulation should not be permitted due to device degradation. Seal leak rate must not exceed 1×10^{-8} Atm cc/sec. Package must not be unique to single supplier.

Table 2 (concl)

DESIGN FACTORS	REMARKS
Usage History	Parts with usage history must be selected as first choice, but obsolescence must be considered. Parts without sufficient data must be evaluated prior to approval. Review alerts for failure history.
Multiple Procurement Sources	Parts must have multiple sources for long-term programs, in the event that major supplier discontinues production.
External Materials	Prohibit use of cadmium plated packages. All metal packages should be Kovar, gold-plated Kovar, Nickel or other non-subliming material. Control use of organic materials.
Design Maturity	Parts must be in active production, to avoid "designing-in" parts that are cancelled prior to production or in early production, by suppliers.

b. Results of Survey - Aerospace users of electronic parts were surveyed in regard to their procurement and specification practices in obtaining high reliability integrated circuits. Table 3 lists the results of this survey.

Table 3 Survey of Electronic Part Users

Monolithic ICs		
User	Unique Test or Specification Requirement	Rationale/Justification
MSFC (Mr. Leon Hamiter)	Wafer lot traceability	To retrieve all of a bad lot and provide identicality.
	Lot size limit	To minimize traceability problems.
	SEM wafer sample	Detect poor metalization.
	Metal thickness test	Detect inadequate thickness.
	Sample extended thermal shock	Thermal expansion compatability of materials.
	Sample wire bond pull	To detect improper bonds and bonders.
	Sample chip removal	To detect improper chip attachment.
	Sample SEM inspection	To evaluate effects of screening.
GSFC (Mr. Don Anna) (CMOS: MIL-M-38510	Wafer lot traceability	To retrieve all of a bad lot
	SEM wafer lot sample	To detect poor metalization.
	Burn-in: HTRB "N" and "P" channel plus forward bias	To maximize the effects of electrical stress by subjecting each channel to worst case bias, then overall functional burn-in.
JPL (Mr. Erv Klippenstein)	Seal wafer inspection	To detect poor metalization.
	Materials inspection	To detect poor materials.
Hughes (Mr. Cliff Ryerson)	Some long burn-in	Spacecraft use only (not many failures beyond 200/300 hours)
	Extended temperature cycle at card level approx. 100 cycles	Detects bad parts and processes in assembly.
Sandia (Mr. D. G. Skogmo)	100% lead bond pull	To detect operator error or out-of-calibration equipment.

c. Alternative Approaches - Although this title is not really applicable to SSI and MSI integrated circuits, a few alternative approaches are noted in Table 4. This table identifies some of the tradeoff studies that are required for considering approaches as alternates to integrated circuits in circuit design.

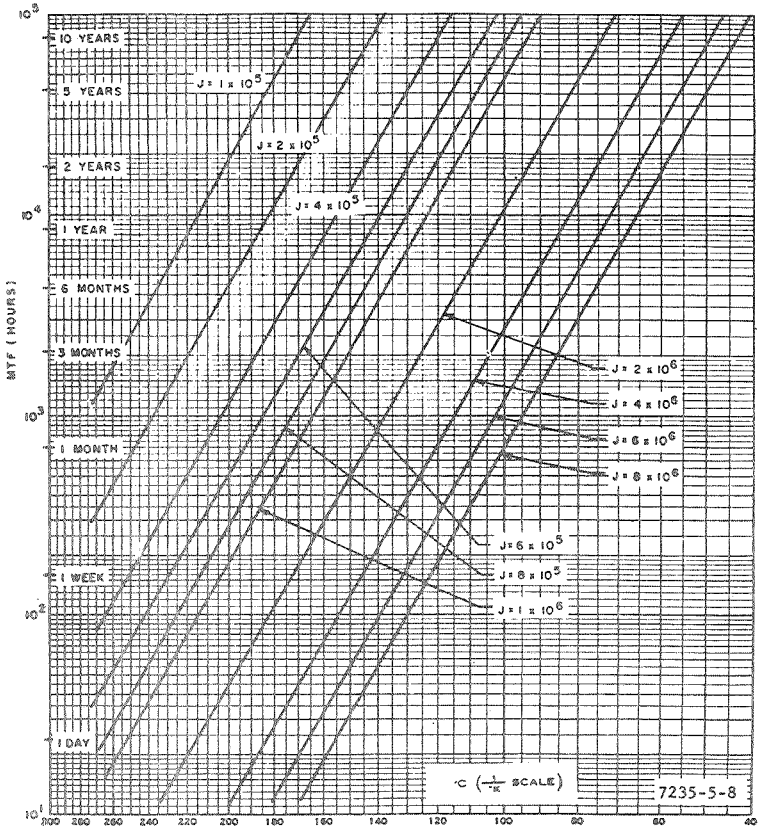
Table 4 Alternative Approach Tradeoffs

Alternative Approach	Tradeoff
Design	
LSI	Requires custom design in many functions; occupies less volume; less weight; greater potential reliability due to many fewer interconnections, bonding wires, die bonds, packages and seals; higher cost due to custom masks; more complex electrical screening tests and fixtures required; much longer schedules and turn around time on custom LSI.
Hybrid	Less reliable than monolithic; greater accuracy; more custom capabilities; more costly than standard SSI/MSI; greater volume and weight than monolithic.
Discrete Parts	Maximized external interconnects; least uniform in reliability; greatest volume and weight; greatest accuracy, most capability in customizing circuitry.
Manufacturing Controls	
Processes and Materials	Impact of specifying desired process and materials in procurement contracts.
Screening	
Burn-in	Cost and reliability tradeoffs between conventional techniques, parameter drift screening, accelerated methods, etc.
Environmental	Cost and reliability tradeoffs between normally established environmental tests and levels, and program unique tests and levels.
Application	
Lead Preforming	Cost and reliability tradeoffs between procurement of parts with preformed leads, user doing the preforming, and damage in attachment of nonpreformed leads.
Bipolar and Various MOS Configurations	Reliability tradeoffs between bi-polar circuits and the numerous variations available in MOS.

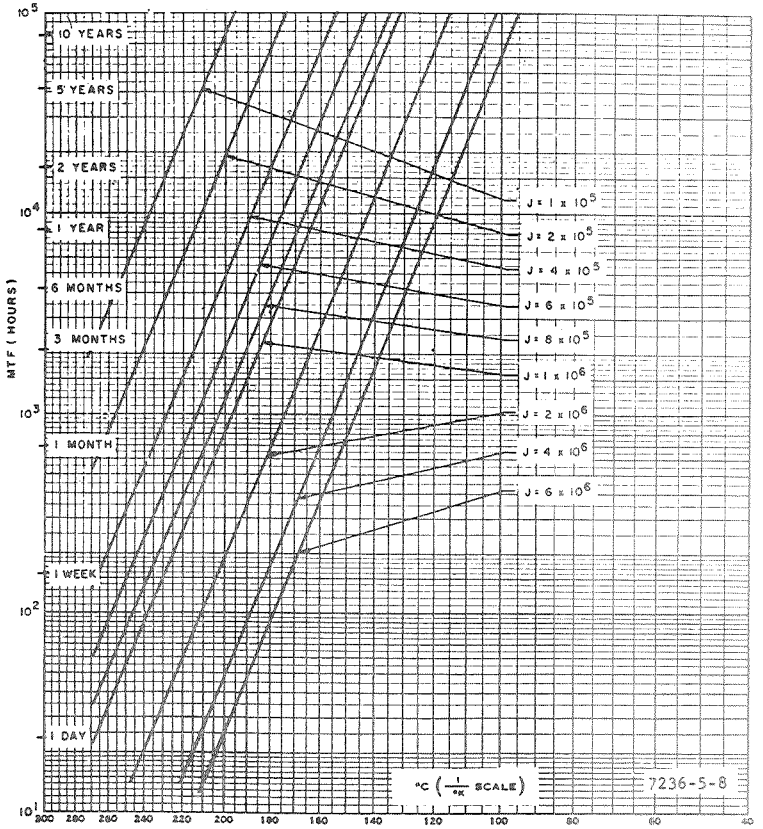
d. Hardware Life - Integrated circuit failures are primarily caused by defects during manufacturing and secondarily by errors during test and improper handling. Wearout is only a minor failure problem that becomes nearly insignificant when used in applications with proper deratings. The time-dependent failure mechanisms summarized in Table 5 are *not* supplier-dependent but are unique to specific processes, several of which can be avoided.

Table 5 Part/Component Time Dependent Mechanisms

Part/Component: Integrated Circuit		
Process or Mechanism	Life Estimate	Martin Marietta Consensus
Electromigration	Dependent on time, temperature, grain size and current density. See Fig. 3.	Control: Current density and grain size in manufacturing the part, temperature in application to define life of $\geq$ 10 yr.
Gold-Aluminum, Eutectic at Wire Bond Sites	Variable, dependent on temperature; quantity of metals; atmosphere.	Avoid mechanism by specifying monometallic interconnect system at all points.
Surface Degradation due to Contamination	Variable, dependent on amount and type of contamination.	Can be minimized by control of processes and requiring glassivation.
Diffusion of Metalization under Oxide	Undetermined, temperature dependent.	Limit temperature exposure to comparatively low ($\leq$100°C) levels or specify Mo-Au.
Increasing Contact Resistance	Undetermined, temperature dependent.	Limit temperature exposure to comparatively low levels or specify Mo-Au.



Large crystallite aluminum film lifetime of conductors with 10^{-5} cm² cross-sectional area.



Classed large crystallite aluminum film lifetime for conductors with a cross section of 10^{-5} cm².

Fig. 3 Aluminum Metalization Lifetimes (from Ref 8)

e. Application Guidelines - The selection, qualification, and screening of parts and inclusion on a controlled parts list merely assures that the parts do not contain basic design faults and that those parts containing operator errors have been removed from the lot of parts delivered by the supplier. The improper application of the parts can negate all the effort expended in manufacturing and testing.

There are a number of design practices and requirements that are considered essential for the reliable application of parts that will, in fact, enhance the basic reliability of the parts. These practices and requirements, detailed below, are necessary to ensure long life assurance. The impact of system design criteria on reliability is listed in Table 6.

1) General,

   a) Integrated circuits generally do not have built-in static charge protection. Thus, they require precautionary handling procedures and careful attention to safety limit circuit voltage transients.

   b) The case temperature should be limited to 85°C to minimize temperature-dependent failure mechanisms.

   c) When interfacing with other similar circuits, current limiting should be provided to ensure that power dissipation capabilities are not exceeded.

2) Digital systems,

   a) All logic systems shall be broken into functional blocks so a logical verification can be made by using analytical techniques (truth tables, Karnaugh maps, state tables, timing diagrams, etc).

   b) All systems requiring time correlation for logic operation (i.e., flip-flop gating, sequential data handling, etc) should be implemented as a synchronous (clocked) system. The clock may be time or data correlatable but must be unambiguous. The inhibit time duty cycle of the clock should contain all of the clock triggered switching transients that may cause ambiguous states during decommutating/decoding. To minimize noise susceptibility in the master mode of a conventional J-K flip-flop, the enable duty cycle of the clock should be minimized.

Table 6 System Design Usage Factors

System Design Criteria	Impact on Reliability and Design
1. Voltage, current and temperature ranges must be derated	Increases expected life, minimizes inoperable failures caused by drift.
2. Leakage currents double each 8 to 12°C temperature rise	System temperature range must be controlled to prevent unacceptable leakages and accelerated life.
3. Parts are electrostatic sensitive	Manufacturing and design must incorporate protective measures.
4. Most parts are available in hermetically sealed flat packs only	Planar packaging by soldering must be employed, connecting pads must be on 0.050 centers. Provides center of gravity very near that of the PC card.
5. Supply voltages must have typically 10% tolerance	Regulation of power system to less than 10% required by design.
6. Low power parts are limited to low MHz operations range; typical maximum of higher power parts limited at 50 to 100 MHz range	For low power designation system design *must* design with low speeds. Very high speed systems *must* be designed discrete.
7. Circuits packaged in very small volume; low power dissipation; less weight	Design can allow for greater capability or redundancy in less volume and weight than discretes. Heat sinking not critical.
8. Parts readily available only in Standard Building Blocks	System must be designed compatible with available circuits rather than optimized function.
9. All elements and bonds are of more uniform reliability in a circuit	Maverick parts more easily detected. Screening tests accomplished at level equivalent to PC board of discretes.

c) Logic systems with memory elements used in counters or shift registers should be analyzed to determine the effects on the total system when an unused state is entered. Provisions should be made to ensure that such a logic function cannot lock up in an unused state or generate an erroneous function when an unused state is entered. The selection of the counter type should be scrutinized to minimize the total logic required to provide proper decoding and minimum unwanted states.

d) Any signal received into a synchronous system should have a single point of synchronization. This prevents logic ambiguities that exist when an incoming signal is synchronized at more than one point by clock signals which are skewed.

e) Monostable multivibrators (one shots) should not be used for delay or time correlation of logic. These functions should be implemented by using clocked counters or delay lines. All "one shots" that are used for other purposes should have 6 dB margin for any predicted noise on signal inputs, power inputs, or output feedback.

f) When signals are transmitted over controlled impedance lines (i.e., coax, twinax, twisted pair, etc), line characteristics such as RC distortion, attenuation, and propagation delays should be determined and their effects used in the worst-case analysis of the system.

g) Logic circuitry should be insensitive to spurious signals, particularly to those generated outside the black box or equipment rack. To facilitate this requirement, system interface circuits that do not receive information from controlled impedance transmission lines should provide means for rejecting transients less than 1.0 ms in duration, and having a magnitude equal to the maximum power supply voltage of the two interfacing systems. Random transients should be assumed to have a 1% duty cycle.

h) Selection of a specific type of integrated circuit logic family to be used in a system should be based on the following criteria:

(1) Power consumption;

(2) Weight and volume requirements;

(3) Noise immunity;

(4) Speed.

All interfaces of discrete to IC circuitry, and ICs of a different family should have a margin of 10% or 0.5 v, whichever is greater, in the high state and 6 db in the low state. The following exceptions are allowable: 5% or 0.3 v whichever is greater, in the high state and 3 db in the low state should be required when such circuits are tied into a common ground in a module or on a PC board or all interfaced with a controlled and matched impedance transmission line. The latter cases must also have no external noise source affecting the sensing mode.

All black box/black box, or rack/rack logic interfaces should have a margin of 10% or 0.5 v, whichever is greater, in the high state and 6 db in the low state, when referenced to ground.

i) All circuits must operate with the specified minimum propagation delay -20% and a maximum of the specified limit +20%. Factors that should be used in determining timing margins are the specified logic element delay including capacitive loading effects, through delay of counter gating, the effect of clock skew, and the effect of line delay.

j) No transient input must be allowed to reach a "master slave" flip-flop that can cause the "master" portion of the flip-flop to be set and remain in an erroneous state such that it may be subsequently transferred to the "slave". All data lines must be stable within the enable portion of clock under worst-case conditions.

k) Circuits that have a memory requirement during loss of power at power transfer or during the maximum transient specified should maintain the memory capability for the duration of the transient or power dropout, plus 25% margin. Analysis must show that no catastrophic outputs will be generated during power up or power down conditions.

ℓ) Logic that drives flip-flops must be arranged so that a logically indeterminant condition cannot occur.

m) Self-induced switching transients must be determined and suppressed by adding capacitance to each printed wiring board or module. The total amount of capacitance required is to be calculated to keep B+ and ground line voltage changes at a safe level, cutting into the specified noise margin by no more than 6 db (50%).

Capacitors that are effective at the relatively high frequency present in the switching current spikes should be used. For integrated circuit boards, ceramic capacitors should be used for this purpose to optimize both high capacitance per size and good RF characteristics. Capacitor leads should be held to a minimum length and the required capacitance should be distributed over the PC board or module.

The number of capacitors required must be based on the printed wiring board lead inductance existing between the capacitor and the switching elements. This inductance must be determined and minimized to realize the benefit provided by the added capacitors. Multilayer printed wiring boards, with B+ and ground planes as internal layers and closely spaced, should be considered for minimum inductance, particularly when any logic element with an active pullup is used.

n) The logic power supply should be designed such that the worst-case output voltage delta from nominal is <60% of what is allowed by the logic family used.

3) Input Considerations,

a) Unused inputs in logic and/or switching circuits require special consideration as follows:

(1) DTL integrated circuits - Leave unused inputs open.

(2) T^2L integrated circuits - Tie up all unused inputs, including preset and clear, to a voltage equal to V_{OH}, but less than V_{IN}. Possible ways of handling unused inputs are:

(a) Connect to a voltage supply of 2.4 to 3.5 v.

(b) Connect (except preset or clear) to a driven input.

(c) Connect to the logical 1 output of an unused gate.

(d) Connect to V_{CC} through a 1 K resistor. One to 25 unused inputs may be connected to each 1 K resistor.

b) The worst-case setup and release times for flip-flop inputs must be determined.

c) Overshoot and ringing may be present at the end of transmission lines that carry fast rise time data information. This overshoot and ringing should be controlled to prevent logic ambiguities and to ensure that both positive and negative input voltage limitations are not exceeded at the receiving circuits. This should be controlled by one or more of the following methods:

(1) Terminate at least one and preferably both sending and receiving ends of the transmission line in its characteristic impedance.

(2) Limit the rise time of the data at the sending or receiving end of the transmission line in systems with slow data rate requirements.

(3) Use a diode clamp to suppress negative transients.

4) Output considerations,

a) Fanout must not exceed 80% of the rated maximum for the circuit and must be reduced from that level where greater noise immunity or corrections for higher than specified circuit differential temperatures are needed.

b) Arrange logic so that interface signals between black boxes use the high- or low-level state that offers the greatest noise immunity as the safe or unarmed condition of a function.

c) "Wired-Or" connections impose loading on the output in addition to the normal fanout load. This loading should be included in the loading analysis. "Wired-Or" conditions are not permitted with circuits having a push-pull output stage.

5) Linear systems,

a) Provide power supply decoupling with 0.1 μf ceramic capacitors from the B+ and B- terminals to ground. The effective lead length from the capacitor to the B+ and B- terminals and ground should be kept to a minimum.

b) The recommended frequency compensation network must be provided. In addition, circuit capacitance loading effects on the phase and gain margin must be determined.

c) Unless more stringent derating is required by the specific usage, the following deratings should be used to allow for end of life drift.

Initial offset voltage	±1/2 mv
Initial bias current	x 2
Offset current	x 2
Open-loop gain	±20%
Slew rate	±20%
Common mode rejection	±20%
Power supply rejection	±20%

d) It is necessary to limit the high-frequency gain of feedback amplifiers, to prevent oscillations from occurring in the packaged circuitry, due to parasitic feedback loops.

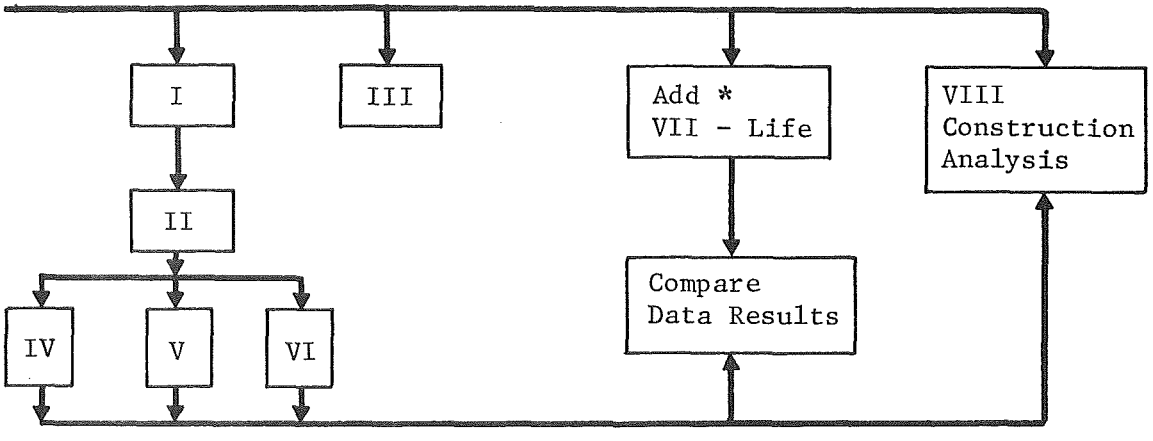
e) The output voltage swing should be limited to 75% of the manufacturer's specified range.

E. TEST METHODOLOGY AND REQUIREMENTS

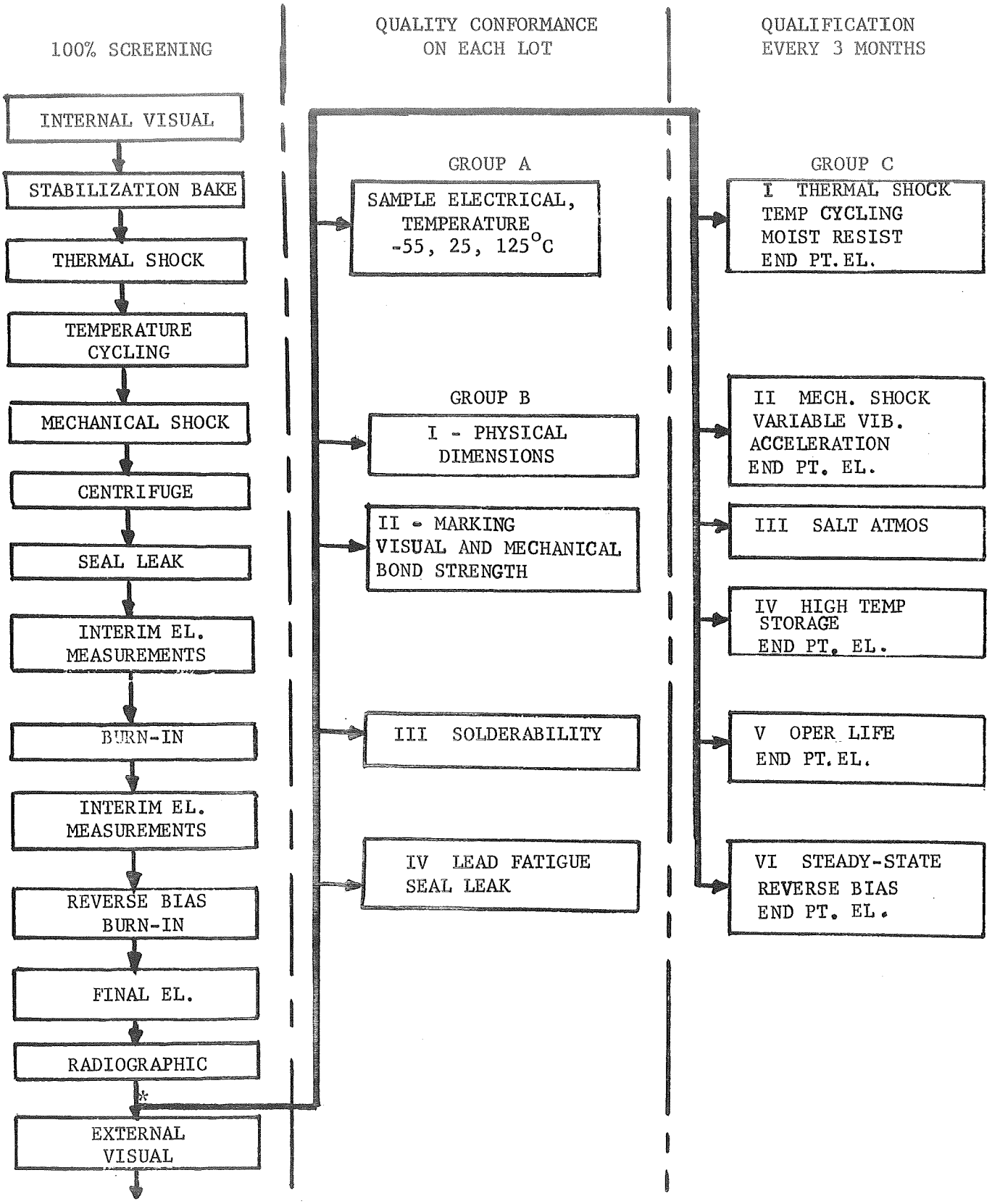
1. Qualification Testing

There are numerous ways in which the traditional qualification testing per Established Reliability MIL-SPECS can be improved. Figure 4 presents the tests and sequence required per MIL-M-38510, the "improved TX" integrated circuit specification. The test flow shown is equivalent to most Established Reliability MIL-SPECS.

The first and most obvious improvement consists of changing Group C subgroups from parallel testing to a form of serial/parallel testing to determine the additive degradation of the tests shown. A more desirable sequence would be as follows.



In the suggested sequence, the stresses imposed on parts by thermal testing are then further aggravated by mechanical testing, in an attempt to degrade inferior parts to an obviously detectable level. The sample is then subjected to long-term life and storage testing to aid in the detection of subtle changes not readily noted on a single electrical test. In parallel with the noted sequence, a sample that has been subjected to screening only (Group VII) should be placed on life test. This sample achieves a two-fold purpose: (1) End results are indicative of normal part changes that can be used to compare with the environmentally tested parts and (2) the sample provides an evaluation of the screening techniques and the quality of part that will result therefrom. Finally, a small sample of parts that have been subjected to the full environmental testing and to screening only should be opened to (1) study the actual configuration and as a reference for comparison of production parts to



* Select quality conformance samples each lot.
Select qualification samples initial lot and each 3 months.

Fig. 4 Traditional Qualification (MIL-M-38510)

detect supplier changes and (2) to detect internal physical changes that may have occurred during the environmental testing that is not present on the screened only part sample.

2. Accelerated Testing

A review of the failure mechanisms indicates that there are several groups when defined by the basic mechanism and tests and environments that will hasten the mechanism to failure or to a detectable condition. The groups are as shown in Table 7. When the environmental factors of the table are increased beyond normal use conditions, but kept below stress levels that introduce *new* failure mechanisms, the corresponding mechanisms of Table 7 degrade at a much more rapid rate. The maximum temperature that the parts can be subjected to, without introducing additional failure mechanisms, depends on the specific processes used in the manufacture of the part. Typical temperatures range from 200 to 350°C.

Table 7 Failure Mechanisms vs Environmental Tests

Environment	Mechanism	Reason
1. Time and temperature without power applied	Contact resistance at metal-silicon interface	With power applied, a path tends to remain open
2. Time, temperature, and power	Inversion, channeling, migration, corrosion	Proper bias collects ionic contamination; current density affects migration
3. Mechanical stress	Seal breakage, bad bonds, improper internal lead length	Mechanical stress tends to move or separate materials
4. Thermal excursions followed by mechanical stress	Die cracks, thermal mismatch	Thermal expansion/contraction propagate the cracks; mechanical stress separates
5. Overvoltage	Pinholes, improper diffusions	Voltage stress causes breakdown

In a like manner, thermal shock and mechanical stress could be performed at accelerated levels, although very little effort has been devoted to any other than electrical temperature stressing.

3. Screening

Screening consists of the lot stressing, measurements and acceptance/rejection criteria normally imposed on a supplier. Screening tests are designed to detect and reject incipient part failures before delivery. The tests usually consist of a combination of environmental, mechanical, and electrical stress that will accelerate specific failure mechanisms in the inferior part, without degrading a good part or initiating a new failure mechanism.

A typical high reliability parts screening program as shown in Fig. 5 is that defined in MIL-M-38510 (MIL-STD-883 method 5004) for class A parts.

Recent usage history has shown that performance of these tests, or the equivalent, does not provide parts satisfactory for long life assurance.[7] The major portion of escapes contain failures due to (1) particulate contamination, (2) metalization faults, and (3) surface contamination (inversion).

Because a satisfactory screen must detect the type of faults noted, it is recommended that the classical screening tests of Fig. 5 be revised as shown in Fig. 6. The revision is based on the fact that faults (1) and (2) in the preceding paragraph occur in the manufacturing sequence of wafer metal deposition or later. If a lot is defined as all parts from wafers in a common metalization run, and that commonality is maintained through all following processes, a sample test will be indicative of the quality of the lot metalization. Therefore, a lot sample test with a scanning electron microscope (SEM) for thin metalization or "waterfall" effects and a Profilometer test or other equivalent method for metal thickness measurement will minimize the faults for the entire lot.

In a like manner, analysis of test points on a wafer is indicative of surface contamination residue on the whole wafer because all parts on the wafer have been subjected to identical processing and cleaning up to that stage of manufacturing. The radioactive tracer wash is the technique recommended to detect the amount of contaminate.

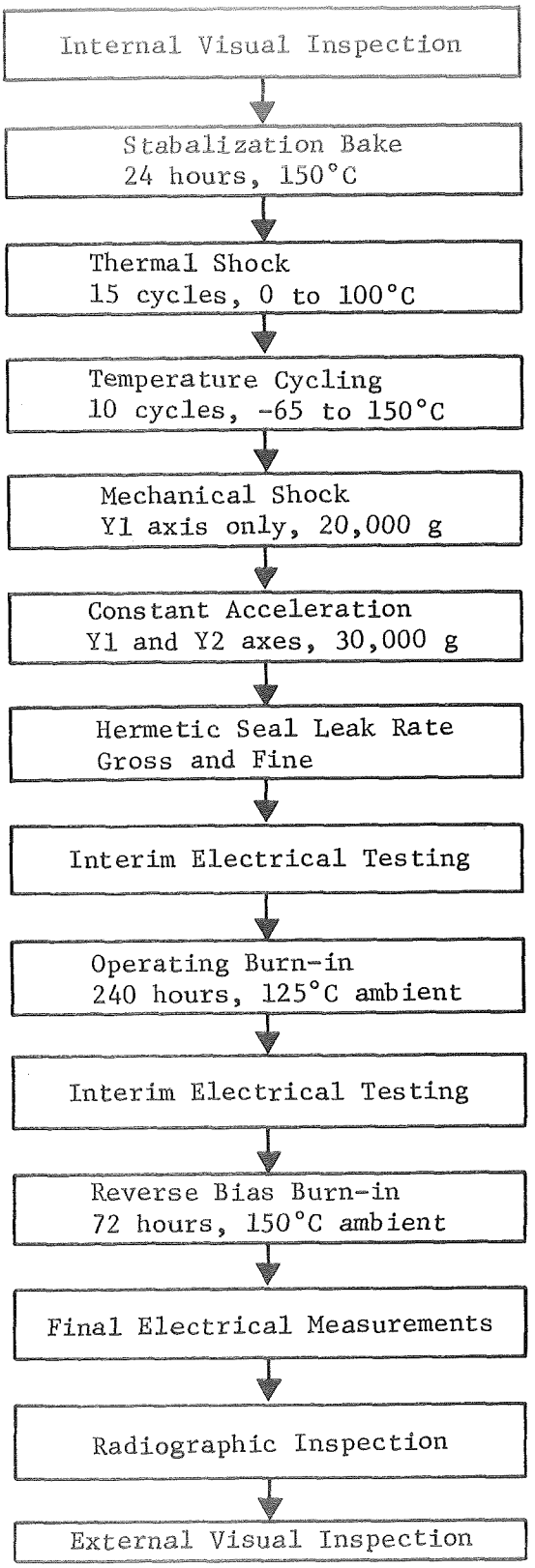


Fig 5 Classical Screening Sequence

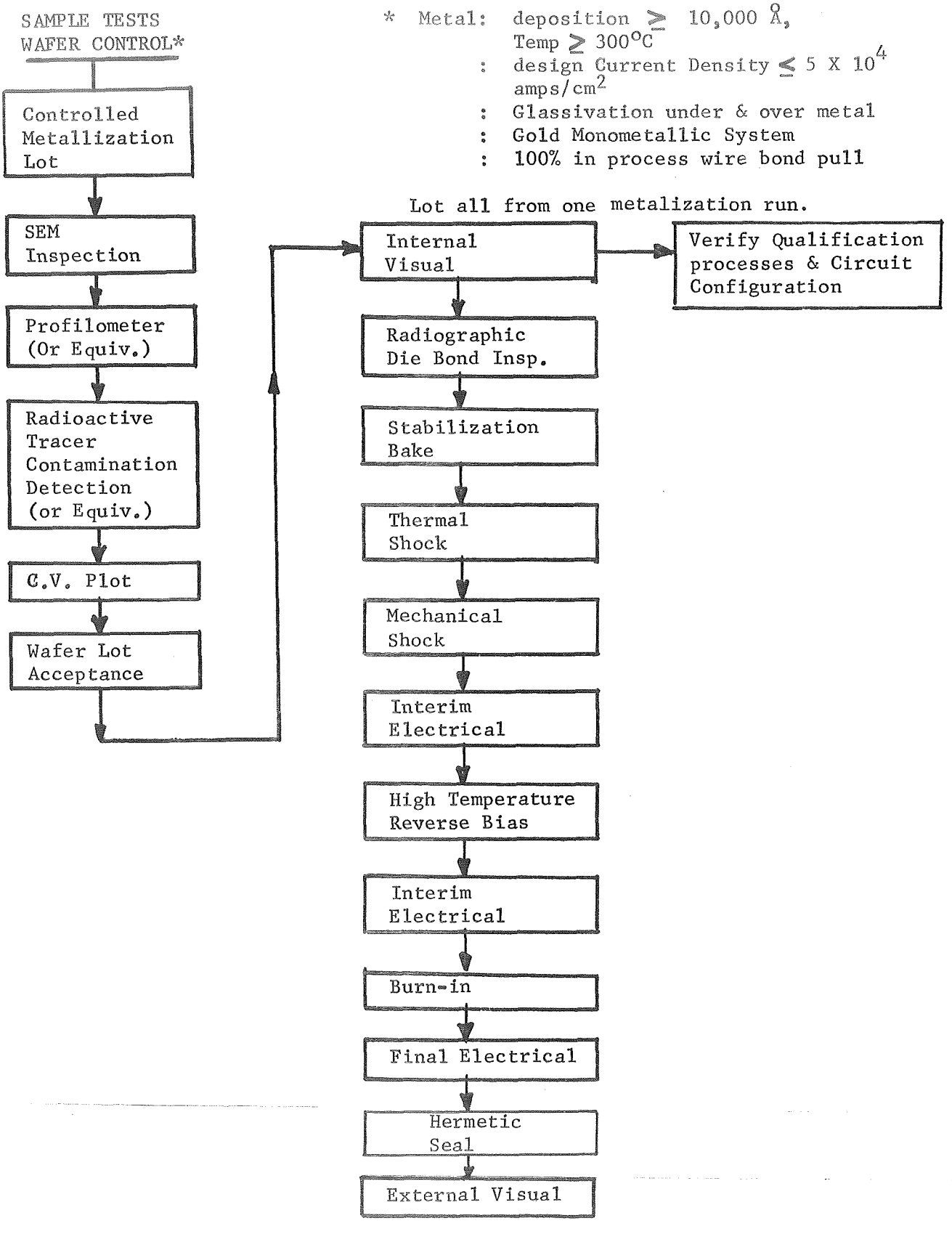


Fig. 6 Recommended Screening Tests

Presently there are no efficient and proven tests to detect particulate contamination, because the particle size is normally smaller than the resolution of X-ray equipment. Another detection method under investigation is a monitored vibration/shock screen used on the Minuteman program.[7] Note that the general solution to particulate contamination has been effort expended in *detection* techniques rather than preventive methods. In the recommended screening herein, the effects are minimized by glassivation over the metalization.

Because the recommended tests include X-ray inspection of die bond area and 100% wire bond pull, the standard mechanical shock and acceleration are no longer required. The wire bond pull test is not destructive. A survey conducted concerning the destructiveness of the pull test had two general responses. Those who employed the test (Autonetics, Fairchild and Sandia) found the pull test non-destructive. Those who did not use pull tests did not because they feared damage, but had not performed tests.

The following paragraphs summarize the MIL-M-38510 tests shown in Fig. 5.

a. Internal Visual Inspection - This test consists of visual inspection at 30 X and 100 X to check the internal materials, design, construction, and workmanship of parts before capping or sealing. If properly performed, this inspection will reject such flaws as surface metalization scratches, poor bonds, misaligned contacts, over etching, under etching, gross oxide faults, gross diffusion faults, corrosion, sagging or missing interconnect wires, particles, insufficient die mounting or improper orientation, and die cracks that may propagate into active areas.

b. Stabilization Bake - This test consists of storage at high temperature to (1) aid in stabilizing characteristics of the device, (2) accelerate the increase of any contact resistance, (3) determine the effects of storage at elevated temperatures, and (4) accelerate any corrosive actions occurring within the sealed package. If performed before sealing, this stress aids in removing contamination such as excess moisture.

c. Thermal Shock - This test consists of rapid alternating exposure to very high- and low-temperature stesses, as a test for compatible thermal coefficient of expansion at all interfaces. The test limits are selected to degrade and detect serious mismatches in seal areas between leads, glass, and ceramic or metal; delamination of multilayer material; breakage in conductor paths; propagate cracks in dice; and aid in the degradation of improper bonds. A difference in coefficient of expansion of $\geq 4 \times 10^{-7}$ in./in.°C will cause breakage at glass to metal interfaces.

d. Temperature Cycling - This test consists of alternate exposure to very high- and low-temperature stresses but at a much slower rate than thermal shock ($\geq$10 min at temperature extremes vs 5 min; 5 min stabilization at 25°C vs 10 seconds transfer time to opposite temperature extreme).

Note: Due to the very small mass and size of an integrated circuit, this test is not cost effective, and cannot be recommended. It appears to apply less stress than thermal shock.

e. Mechanical Shock - This test consists of very short pulsed acceleration (shock) such as may occur in rough handling or transportation. The tests are intended to check mechanical soundness of the part, such as the die header bond, wire bonds and possibility of internal wire deformation resulting in short circuit. Typical stress levels are 1500 g 0.5 ms for drop tests and 25,000 g, 0.2 ms for pneupactor tests.

f. Constant Acceleration - This test imposes a much longer high-g force to the mechanical structure than shock, but in a centrifugal direction rather than a straight line force. Similarly this test is intended to check mechanical soundness of the part. Typical tests are performed at 30,000 g for 1 min, although step stress testing[3] has shown that properly bonded dice and wirebonds will not separate at 150,000 g or less.

g. Seal Leak - Hermetic seal tests consist of a fine leak (10^{-5} to 10^{-8} Atm cc/s) measurement after subjecting the part to pressurized helium or radioactive Krypton 85 tracer gas. The second test, for gross leaks (10^{-2} to 10^{-5} Atm cc/s) consists of submerging the part in a pressurized Fluorocarbon to allow the liquid to enter the package if it can, then submersion in a much higher temperature Fluorocarbon to observe for bubbles from the lower temperature liquid.

h. Interim Electrical Measurements - Critical parameters that must be specified in the detail specification are then tested. The tests are designed to remove defective parts at that time and to provide a baseline in the event that maximum drift limits are imposed.

i. Burn-in - This test consists of operating the part at the maximum rated temperature of 125°C for 240 hr. Specific biasing conditions must be specified in the detail specification.

The test conditions and time are selected to impose maximum stresses on junctions to accelerate the diffusion, metalization, and bonding faults that may have escaped the precap visual inspection.

j. Interim Electrical Measurements - The same critical electrical parameters tested before burn-in are rechecked to determine if there are defective parts in the lot.

k. Reverse Bias - This test is only imposed when specified in the detail specification and consists of reverse biasing the part for 72 hr in an ambient of 150°C. The test is designed to detect surface contamination on MOS or linear circuits that are sensitive to surface leakages.

l. Final Electrical Measurements - This test consists of testing the full electrical parameters at high, low, and room temperatures as defined in the detail specification to ensure that parts are within allowable limits.

m. Radiographic - X-ray inspection is performed at this time to detect anomalies overlooked in precap visual, faults that occurred in testing and processing, such as sealing weld splatter, extraneous lead material, insufficient die bonding (voids under the die) or deformation of leads during mechanical testing. The inspection must be performed with specific accept/reject criteria, to be meaningful.

n. External Visual - A final visual inspection is performed to detect damage caused by handling and testing, gross seal failures, and improper marking.

4. Burn-In

Burn-in on high reliability parts has not been standardized. Variations range from NIMBUS I and II with up to 168 hr burn-in[28] to INTELSAT III with 1000 hr preconditioning and five-point data comparison for stability.[29] A typical example is the 10 TIROS and 5 ESSA satellites by RCA-AED. Burn-in was at 80% rated power for 300 hr in an ambient of 100°C.[30] Mil-M-38510 (MIL-STD-883), the first attempt to standardize burn-in conditions, recommends operation at rated power for 240 hr in an ambient of 125°C, plus an additional 72 hr of back-biased burn-in at 150°C, for parts that are surface sensitive. Philco[31] concludes that 168 hr was insufficient in tests performed under the referenced NASA contract and recommends that addition evaluations be performed at 340 hr burn-in (at rated power and 125°C).

It appears that considerably more evaluation and evidence of non-damage is required before elevated temperatures can be recommended as a 100% screen. Furthermore, the maximum temperatures may depend on the configuration and processes of each individual circuit type.

An evaluation aide in burn-in and screening that is gaining wide acceptance throughout industry, particularly for LSI, but just as applicable to SSI and MSI, is the use of customized test elements at critical locations on each wafer. This method has great potential for evaluation of the control in manufacturing processing such as diffusion levels, metalization thickness and grain size, oxide characteristics, mask alignments, surface cleanliness, and contact resistances. Far greater burn-in stress can be applied to the individual elements in the test chips than on the internal elements in a circuit. This provides a true accelerated evaluation of the processing.

F. PROCESS CONTROL REQUIREMENTS

All processes and materials in the manufacture of integrated circuits can be considered critical. Improper control of any of the items defined in Table 8 could have detrimental effects on the life of the part. This table does not include such critical processes and materials as purity of initial silicon pellets used in ingot melt, purity of dopant material added to the melt, seed crystal alignment and pull rate from the melt, ingot trimming, and wafer slicing, lapping, polishing, etching and oxidation, because the initial starting material at a supplier may be the purchased wafers.

Additional Process Controls Required - Although selected processes will be required, i.e., Molygold-gold metalization systems, and phosphosilicate and silicon nitride glassivation, no additional controls are required beyond those normally enforced by the supplier. Also, process limitations will be required, such as heated substrate during metal deposition, metalization thickness. These items are considered more in process selection and limitations as compared to the actual controls the supplier uses in providing a satisfactory product.

Table 8 Critical Processes and Materials

	CRITICAL PROCESS/MATERIAL	EFFECTS OF INADEQUATE CONTROL	REMARKS
1.	Resistance of basic wafer	Variation in leakage currents and breakdown voltages	
2.	Wafer cleaning	Contaminated diffusions, irregular etches and diffusions.	
3.	All mask layouts and dimensional control	Improper etches, diffusions and alignments.	
4.	Photoresist application, spin and bake, purity of photoresist.	Extraneous diffusions, contamination.	
5.	Mask alignment and exposure	Improper electrical parameters.	
6.	Resist development	Improper diffusion characteristics.	
7.	Post-development inspection	High yield loss at later stages	
8.	Oxide etch depth, rate, angle, and undercut	Change in electrical parameters, impact on metalization.	
9.	Post etch inspection	High yield loss at later stages.	
10.	Resist removal	Improper diffusions due to masking.	
11.	Prediffusion wash and dry	Contamination in diffusion.	
12.	Diffusion or deposition and drive-in, reoxidation purity of material	Electrical characteristics out of spec.	
13.	Oxide removal and epitaxial growth	Improper parameters	
14.	Oxide growth	Insufficient masking, improper diffusions.	

Steps 4 thru 13 repeated as required.

Table 8 Critical Processes and Materials (concl)

	CRITICAL PROCESS/MATERIAL	EFFECTS OF INADEQUATE CONTROL	~~REMARKS~~
15.	Metalization deposition purity of metal, grain size, thickness	Single source deposition allows shadow effect at steps, Low temperature of wafer allows small grain. Thin metal allows open oxide steps, rapid migration.	
16.	Masking, metal etch and cleaning	Shorts, opens, corrosion.	
17.	Metalization annealing	Peeling metal	
18.	Glassivation and material content	Surface instability problems	
19.	Masking, etching, and cleaning	Bond problems - opens, electrical probe problems.	
20.	Wafer electrical probe and mark	Yield loss at later stages	
21.	Application of gold-backing on wafer and purity	Separation of die-to-header	
22.	Wafer scribe, break and sort	Damaged parts	
23.	Package cleaning	Contamination on surface of die - parameter change.	
24.	Die attach and material control	Separation of die-to-header	
25.	Lead material and bonding	Improper bonds. Circuit failure.	
26.	Precap Inspection	Loss of reliability.	
27.	Package Sealing and materials	Loss of hermetic seal. Subject to contamination failure.	
28.	Packaging marking and permanency	Improper testing. Loss of identity.	

G. RECOMMENDED PARTS LIST

The following list of integrated circuits has been thoroughly investigated by the responsible parts specialists at Martin Marietta Aerospace and is recommended for high reliability applications. The generic parts must be procured to a specification control drawing that invokes the required controls noted in this report.

The specified parts have sufficient test data in existence to ensure that there are no basic faults in the part design. Furthermore, most parts on the list will be subjected to formal qualification testing for the Viking Lander space program by Martin Marietta in the near future. The remainder of the parts will be qualified by existing data or by actual test for spacecraft use by Martin Marietta on other programs.

With the basic part design well established, the imposition of requirements such as monometallic interconnect systems, glassivation, etc, will ensure the final product will satisfy long-life assurance requirements.

Unacceptable Parts - Presently, the only part types that can be considered unacceptable are those that are plastic encapsulated. Due to recent design/application problems, the 709 operational amplifier is not a recommended type.

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED

MICROCIRCUITS - DIGITAL, BIPOLAR

FUNCTION	DESCRIPTION	PARAMETERS (T_A = +25°C) AT V_{CC} = 5 ±.5 V								Comm'l Part No.		PKG. FIG.
		$\frac{T_{PHL}\ MAX}{T_{PLH}\ MAX}$	SPEED MIN	$\frac{V_{OH}\ MIN}{V_{OL}\ MAX}$	$\frac{V_{IH}\ MIN}{V_{IL}\ MAX}$	$\frac{I_{CCL}\ MAX}{I_{CCH}\ MAX}$	$\frac{I_{IH}\ MAX}{I_{IL}\ MAX}$	$\frac{I_{OH}\ MIN}{I_{OL}\ MIN}$				
MEDIUM POWER TTL NAND-NOR GATES	QUAD 2 INPUT POSITIVE NAND	15 NS / 22 NS		2.4 V / 0.4 V	2.0 V / 0.8 V	22 MA / 8 MA	40 UA / -1.6 MA	-400 UA / 16 MA		SN 5400		
	QUAD 2 INPUT POSITIVE NAND (OPEN COLLECTOR)	15 NS / 45 NS		----- / 0.4 V		22 MA / 8 MA		250 UA * / 16 MA		SN 5401		
	QUAD 2 INPUT POSITIVE NOR	15 NS / 22 NS		2.4 V / 0.4 V		27 MA / 16 MA		-400 UA / 16 MA		SN 5402		
	HEX INVERTER	15 NS / 22 NS		2.4 V / 0.4 V		33 MA / 12 MA		-400 UA / 16 MA		SN 5404		
	HEX INVERTER (OPEN COLLECTOR)	15 NS / 55 NS		----- / 0.4 V		33 MA / 12 MA		250 UA * / 16 MA		SN 5405		
	POWER HEX INVERTER (OPEN COLLECTOR)	23 NS / 15 NS		----- / 0.4 V		38 MA / 42 MA		250 UA * / 16 MA		SN 5406		
	POWER HEX (OPEN COLLECTOR)	30 NS / 10 NS		----- / 0.4 V		30 MA / 41 MA		250 UA * / 16 MA		SN 5407		
	QUAD 2 INPUT POSITIVE AND	19 NS / 27 NS		2.4 V / 0.4 V		33 MA / 21 MA		-800 UA * / 16 MA		SN 5408		
	QUAD 2 INPUT POSITIVE AND (OPEN COLLECTOR)	24 NS / 32 NS		----- / 0.4 V		33 MA / 21 MA		250 UA * / 16 MA		SN 5409		
	TRIPLE 3 INPUT POSITIVE NAND	15 NS / 22 NS		2.4 V / 0.4 V		16.5 MA / 6 MA		-400 UA / 16 MA		SN 5410		
	DUAL 4 INPUT POSITIVE NAND	15 NS / 22 NS		2.4 V / 0.4 V		11 MA / 4 MA		-400 UA / 16 MA		SN 5420		
	8 INPUT POSITIVE NAND	15 NS / 22 NS		2.4 V / 0.4 V		6 MA / 2 MA		-400 UA / 16 MA		SN 5430		
	DUAL 4 INPUT POSITIVE NAND (BUFFER)	15 NS / 22 NS		2.4 V / 0.4 V		27 MA / 8 MA		-1.2 MA / -48 MA		SN 5440		
AND-OR-INVERT GATES	DUAL 2 WIDE, 2 INPUT	15 NS / 22 NS		2.4 V / 0.4 V		14 MA / 8 MA		-400 UA / 16 MA		SN 5450		
	4 WIDE, 2 INPUT	15 NS / 22 NS		2.4 V / 0.4 V		9.5 MA / 8 MA		-400 UA / 16 MA		SN 5453		
EXPANDER	DUAL 4 INPUT	20 NS / 30 NS		----- / 0.4 V		2.5 MA / 4 MA		150 UA * / -0.3 MA		SN 5460		
FLIP-FLOPS	POSITIVE EDGE TRIGGER JK (AND INPUTS)	50 NS / 50 NS	20 MHZ	2.4 V / 0.4 V		26 MA / 26 MA		-400 UA / 16 MA		SN 5470		
	JK MASTER-SLAVE (AND INPUTS)	40 NS / 25 NS	15 MHZ	2.4 V / 0.4 V		20 MA / 20 MA		-400 UA / 16 MA		SN 5472		
	DUAL JK MASTER-SLAVE (NO RESET)	40 NS / 25 NS	15 MHZ	2.4 V / 0.4 V		40 MA / 40 MA		-400 UA / 16 MA		SN 5473		
	DUAL D TYPE EDGE TRIGGERED	40 NS / 25 NS	15 MHZ	2.4 V / 0.4 V		30 MA / 30 MA		-400 UA / 16 MA		SN 5474		
	DUAL JK MASTER-SLAVE (SEPARATE SET, CLEAR, CLOCK)	40 NS / 25 NS	15 MHZ	2.4 V / 0.4 V	2.0 V / 0.8 V	40 MA / 40 MA	40 UA / -1.6 MA	-400 UA / 16 MA		SN 5476		

*I_{CEX} OF OUTPUT TRANSISTOR

MICROCIRCUITS-DIGITAL, BIPOLAR (continued)

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED

FUNCTION	DESCRIPTION	PARAMETERS (T_A = +25°C) V_{CC} = 5 ±.5 V								Comm'l Part No.		PKG. FIG.
		$\frac{T_{PHL}\ MAX}{T_{PLH}\ MAX}$	SPEED MIN	$\frac{V_{OH}\ MIN}{V_{OL}\ MAX}$	$\frac{V_{IH}\ MIN}{V_{IL}\ MAX}$	$\frac{I_{CCL}\ MAX}{I_{CCH}\ MAX}$	$\frac{I_{IH}\ MAX}{I_{IL}\ MAX}$	$\frac{I_{OH}\ MIN}{I_{OL}\ MIN}$				
MEDIUM POWER TTL COMPLEX FUNCTIONS	QUAD 2 INPUT EXCLUSIVE OR GATE	22 NS / 30 NS		2.4 V / 0.4 V	2.0 V / 0.8 V	43 MA / -----	40 UA / -1.6 MA	-800 UA / 16 MA		SN 5486		
	8 BIT SHIFT REGISTER	40 NS / 40 NS	10 MHZ			50 MA / -----	40 UA / -1.6 MA	-400 UA / 16 MA		SN 5491A		
	4 BIT BINARY COUNTER	135 NS / 135 NS	10 MHZ			46 MA / -----	40 UA / -1.6 MA	-400 UA / 16 MA		SN 5493		
	4 BIT RIGHT-LEFT SHIFT-REGISTER (R-S)	32 NS / 27 NS	25 MHZ	2.4 V / 0.4 V	2.0 V / 0.8 V	39 MA / 63 MA	40 UA / -1.6 MA	-400 UA / 16 MA		SN 5495A		

REVISIONS				
STR	ZONE	DESCRIPTION	DATE	APPROVED

MICROCIRCUITS-DIGITAL, BIPOLAR (continued)

FUNCTION	DESCRIPTION	PARAMETERS (T_A = +25°C) V_{CC} = 5 ±.5 V								Comm'l Part No.		PKG. FIG.
		$\frac{T_{PHL}\ MAX}{T_{PLH}\ MAX}$	SPEED MIN	$\frac{V_{OH}\ MIN}{V_{OL}\ MAX}$	$\frac{V_{IH}\ MIN}{V_{IL}\ MAX}$	$\frac{I_{CCL}\ MAX}{I_{CCH}\ MAX}$	$\frac{I_{IH}\ MAX}{I_{IL}\ MAX}$	$\frac{I_{OH}\ MIN}{I_{OL}\ MIN}$				
LOW POWER TTL NAND-NOR GATES	QUAD 2 INPUT POSITIVE NAND	60 NS / 60 NS		2.4 V / 0.3 V	2.0 V / 0.7 V	2.04 MA / 0.8 MA	10 UA / -.18 MA	100 UA / 2 MA		SN 54L00		
	HEX INVERTER	↕		↕	↕	3.06 MA / 1.2 MA	↕	↕		SN 54L04		
	TRIPLE 3 INPUT POSITIVE NAND	↕		↕	↕	1.53 MA / 0.6 MA	↕	↕		SN 54L10		
	DUAL 4 INPUT	60 NS / 60 NS		↕	↕	1.02 MA / 0.4 MA	↕	↕		SN 54L20		
	8 INPUT POSITIVE NAND	100 NS / 60 NS		↕	↕	.51 MA / .33 MA	↕	↕		SN 54L30		
AND-OR-INVERT GATES	DUAL 2 WIDE	60 NS / 90 NS				1.30 MA / .8 MA				SN 54L51		
	4 WIDE 3-2-2-3 INPUT	↕				.99 MA / .8 MA				SN 54L54		
	2 WIDE 4 INPUT	60 NS / 90 NS				.65 MA / .4 MA				SN 54L55		
FLIP-FLOPS	R-S MASTER-SLAVE	150 NS / 75 NS	3 MHZ			1.44 MA / 1.44 MA				SN 54L71		
	J-K MASTER-SLAVE	↕	↕			1.44 MA / 1.44 MA				SN 54L72		
	DUAL JK MASTER-SLAVE (NO RESET)	150 NS / 75 NS	↕			2.88 MA / 2.88 MA	10 UA / -.18 UA			SN 54L73		
	DUAL D TYPE EDGE TRIGGERED	150 NS / 100 NS	↕			3.0 MA / 3.0 MA	10 UA / -.18 MA			SN 54L74		
	DUAL JK MASTER-SLAVE (COMMON CLOCK)	150 NS / 75 NS	3 MHZ			2.88 MA / 2.88 MA	10 UA / -.18 MA			SN 54L78		
COMPLEX FUNCTIONS	4 BIT MAGNITUDE COMPARATOR	150 NS / 150 NS				7.7 MA / 7.2 MA	30 UA / -.54 MA			SN 54L85		
	QUAD 2 INPUT EXCLUSIVE OR GATE	150 NS / 150 NS				6.68 MA / 4.4 MA	20 UA / -.36 MA			SN 54L86		
	8 BIT SHIFT REGISTER	150 NS / 100 NS				6.6 MA / 6.6 MA	10 UA / -.18 MA			SN 54L91		
	4 BIT BINARY COUNTER	450 NS / 450 NS	3 MHZ			6.6 MA / 6.6 MA	↕			SN 54L93		
	4 BIT RIGHT-LEFT SHIFT REGISTER (R-S)	200 NS / 200 NS	↕			9 MA / 9 MA	10 UA / -.18 MA			SN 54L95		
	4 BIT DATA SELECTORS/STORAGE REGISTERS	200 NS / 200 NS	↕			9 MA / 9 MA	10 UA / -.18 MA			SN 54L98		
	4 BIT RIGHT-LEFT SHIFT REGIATER (JK)	200 NS / 200 NS	3 MHZ	2.4 V / 0.3 V	2.0 V / 0.7 V	9 MA / 9 MA	10 UA / -.18 MA	-100 UA / 2 MA		SN 54L99		

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED

MICROCIRCUITS – LINEAR, BIPOLAR

FUNCTION	DESCRIPTION	PARAMETERS (T_A = +25°C)								Comm'l Part No.		PKG. FIG.
		$\frac{I_{BIAS}}{I_{S(MAX)}}$	$\frac{I_{INOFFSET}}{V_{INOFFSET}}$	$\frac{C_{MRR}\ (MIN)}{P_{SRR}\ (MIN)}$	$\frac{V_S\ RECM\ MAX}{V_{OUT}}$	A_V MIN	$\frac{V_{DIFF(MAX)}}{V_{IN(MA)}}$	$\frac{Z_{IN}\ MIN}{Z_{OUT}\ MAX}$				
OPERATIONAL AMPLIFIER	GENERAL PURPOSE (UNCOMPENSATED)	75 NA / 3 MA	10 NA / 2 MV	80 DB / 80 DB	±20 V / ±15 V	50 V/MV	±30 V / ±15 V	1.5 M / ---		LM101A		
	HIGH INPUT IMPEDANCE	15 NA / 3.7 MA	15 NA / 4 MV	80 DB / 80 DB	±20 V / ±10 V R_L = 2 KOHMS	100 K V/V	±12 V / ±11 V RECM	100 M / ---		HA2620		
	MICROPOWER	2.0 NA / 0.6 MA	0.2 NA / 2.0 MV	85 DB / 80 DB	±15 V / ±13 V R_L = 10 KOHMS	50 V/MV	1 V / ±15 V	30 M / ---		LM108		
	VOLTAGE FOLLOWER	--- / 5.5 MA	--- / 7.5 MV	60 DB(V+) 70 DB(V-)	±15 V / ±10 V	.999	--- / ±15 V	10 KM / 2.5		LM102		
VOLTAGE COMPARATOR	LOW CURRENT	100 NA / +6 MA -5 MA	10 NA / 3.0 MV		±15 V / 50 V 0.4 V AT I_{OUT} = 16 MA	40 V/MV TYP	±30 V / ±15 V			LM111		
	HIGH FANOUT	45 UA / +10 MA -3.6 MA	7 UA / 3.0 MV		±12 V / 24 V 2.5 V AT I_{OUT} = 400 UA 0.4 V AT I_{OUT} = 16 MA	40 V/UV TYP	±5 V / ±7 V			LM106		

MICROCIRCUITS-MISCELLANEOUS

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED

FUNCTION	DESCRIPTION	PARAMETERS							Comm'l Part No.		PKG. FIG.
VOLTAGE REGULATOR	PRECISION	STANDBY CURRENT (MA)	T.C. (AV)	V+-V- CONTINUOUS (MAX)	$V_{OUT(NOISE)}$ (MAX)	V_{IN} RANGE V_{OUT} (MIN/MAX)	LINE REG (MAX) / LOAD REG (MAX)			UA 723	
		3.5 MA	.015 PCT/°C	40 V	35 UV RMS	9.5 - 40 V / 2 - 37 V	0.2 PCT V_{OUT} / 0.6 PCT V_{OUT}				
	GENERAL PURPOSE, 5 V	10 MA TYP	.02 PCT/°C	35 V	40 UV TYP	7V - 25 V / 4.7V-5.2V	50 MV / 50 MV			LM 109	
MULTIVIBRATOR	MONOSTABLE, RETRIGGERABLE	I_{IL} MAX / I_{IH} MAX	I_{OL} MIN / I_{OH} MIN	I_{CC} MAX	V_{CC}	V_{OL} / V_{OH}	$V_{IL(MAX)}$ / $V_{IH(MIN)}$	T_{PLH} (MAX) / T_{PHL} (MAX)		UA 9601	
		-1.6 MA / 60 UA	10 MA / -7.2 MA	25 MA	5 ±.5 V	.40 V / 2.4 V	0.90 V / 2.0 V	40 NS / 40 NS			
POWER DRIVER	2 INPUT WITH EXPANDER	I_{IL} / I_{IH}	$P_{STANDBY}$ V_{CC}=28 / I_{OUT} ABS MAX PK AT V_{CC} = 10 V	V_{CC} ABSMAX CONT / V_{CC} MIN	V_{OL} (MAX) / V_{OH} (MAX) V_{CC} = 45 V	V_{IL} / V_{IH}	T_{ON} (MAX) / T_{OFF} (MAX)			NH0008	
		-1.0 MA / 5 UA	35 MW / 3.0 AMP	45 V / 10 V	0.1 V / 26.5 V	0.8 V / 2.1 V	0.4 US / 7.0 US				
MULTIPLEX CIRCUITS	DRIVER △A	$I_{CC(ON)}$ / $I_{EE(ON)}$	T_{PHL} (MAX) / T_{PLH} (MAX)	V_{OL} (MAX) / V_{OH} ABS (MAX)	V_{CC} TO - V_{EE}	I_R / I_F	I_{OL} MAX	$I_{CC(OFF)MAX}$ / $I_{EE(OFF)MAX}$		D 129AL	
		3 MA / -2 MA	250 NS / 800 NS	0.7 V / ---	38 V	.25 UA / -160 UA	10 MA	.75 MA / -10 UA			
		$R_{DS(ON)}$ (MAX)	I_S, I_D ABS(MAX) / I_{GCN}(MAX)	$I_{D(OFF)}$(MIN) (MAX)	$V_{GS(TH)}$ (MAX) (MIN)	C_{GS} MAX / C_{DS} MAX	BV_{DSS} MIN	BV_{GBS} MIN			
	GATE, 5 CHANNEL MOS	100 TO 450 OHMS	100 MA / -2.4 MA	-2.5 NA / 2500 NA	- 6 V / -2 V	3 PF / 0.4 PF	-30 V	-35 V		G116AL	
	GATE, 6 CHANNEL MOS		100 MA / -2.4 MA	- .5 NA / 1500 NA	-6 V / -2 V	3 PF / 0.4 PF	-30 V	-35 V		G119AL	

△A I_{OL} = 3 MA MAX FOR V_{OL} = .45 V MAX

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MICROCIRCUITS–MISCELLANEOUS (continued)

FUNCTION	DESCRIPTION	PARAMETERS								Comm'l Part No.		PKG. FIG.
LINE DRIVER	DIGITAL, TRIPLE	$\frac{I_{DATA(ON)MAX}}{I_{DATA(OFF)MAX}}$	$\frac{I_{CC\ MAX}}{I_{IN\ MAX}}$	$+V_{CC}$ RECOMMENDED RANGE	$\frac{V_{IN}{}^{ABS\ MAX}}{V_{OUT}}$	$\frac{T_{ON\ MAX}}{T_{OFF\ MAX}}$				HAI-245		
		5.4 MA / -100 UA	6.2 MA / -2.2 UA	5 ±.5 V	5.5 V / -30 V	10 NS / 14 NS						
LINE RECEIVER	DIGITAL, TRIPLE	$\frac{R_{IN\ MIN}}{R_{IN\ MAX}}$	$\frac{I_{OUT(ON)\ MAX}}{I_{OUT(OFF)\ MIN}}$	I_{CC} MAX AT V_{CC} = 5 V, V_{EE} = -5 V	$\frac{V_{CC}}{V_{EE}}$ RECOMMENDED RANGE	$\frac{V_{OL\ MAX}}{V_{OH\ MIN}}$	$\frac{T_{ON\ MAX}}{T_{OFF\ MAX}}$			HAI-249		
		40 OHMS / 61 OHMS	9 MA / -120 UA	2.3 MA	+5 ±.5 V / -5 ±.5 V	.45 V / 2.5 V	30 NS / 30 NS					

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III. HYBRID INTEGRATED CIRCUITS

by E. J. Sinclair

III. HYBRID INTEGRATED CIRCUITS

A. INTRODUCTION

This chapter describes failure mechanisms, test methodology, manufacturing processes and related control requirements that affect the long-life reliability of thick and thin film hybrid integrated circuits. The full temperature range, hermetically sealed type of part is addressed. The "plastic" encapsulated type part is specifically omitted due to the lack of sufficient reliability data and the "proprietary" classification of many materials used by suppliers. Furthermore, RF and other unique areas of use are avoided since the parts, materials and processes in the manufacture of those hybrids may not be common to the typical linear or digital parts. Figure 1 illustrates the materials and general areas covered.

The information herein summarizes the pertinent results of a review of available literature, discussions with manufacturers and users of hybrid integrated circuits and knowledge gained within Martin Marietta Aerospace as a manufacturer, test and failure analysis laboratory, circuit design user, and from materials and parts specialists.

A listing of failure mechanisms, basic causes, detection methods and methods to minimize the mechanisms, is presented. An attempt has been made to categorize the mechanism to thick or thin film, or common to both. Since processes are so interchangeable within the hybrid circuit concept, a portion of those listed for one type of circuitry may be just as applicable to the other.

Selection criteria are defined in detail for both thick and thin film networks. The criteria listed are those that can specifically jeopardize the long-life assurance requirements.

Test methodology, including screening, burn-in, accelerated testing and qualification, is discussed. The recommended test techniques are identified, along with justification.

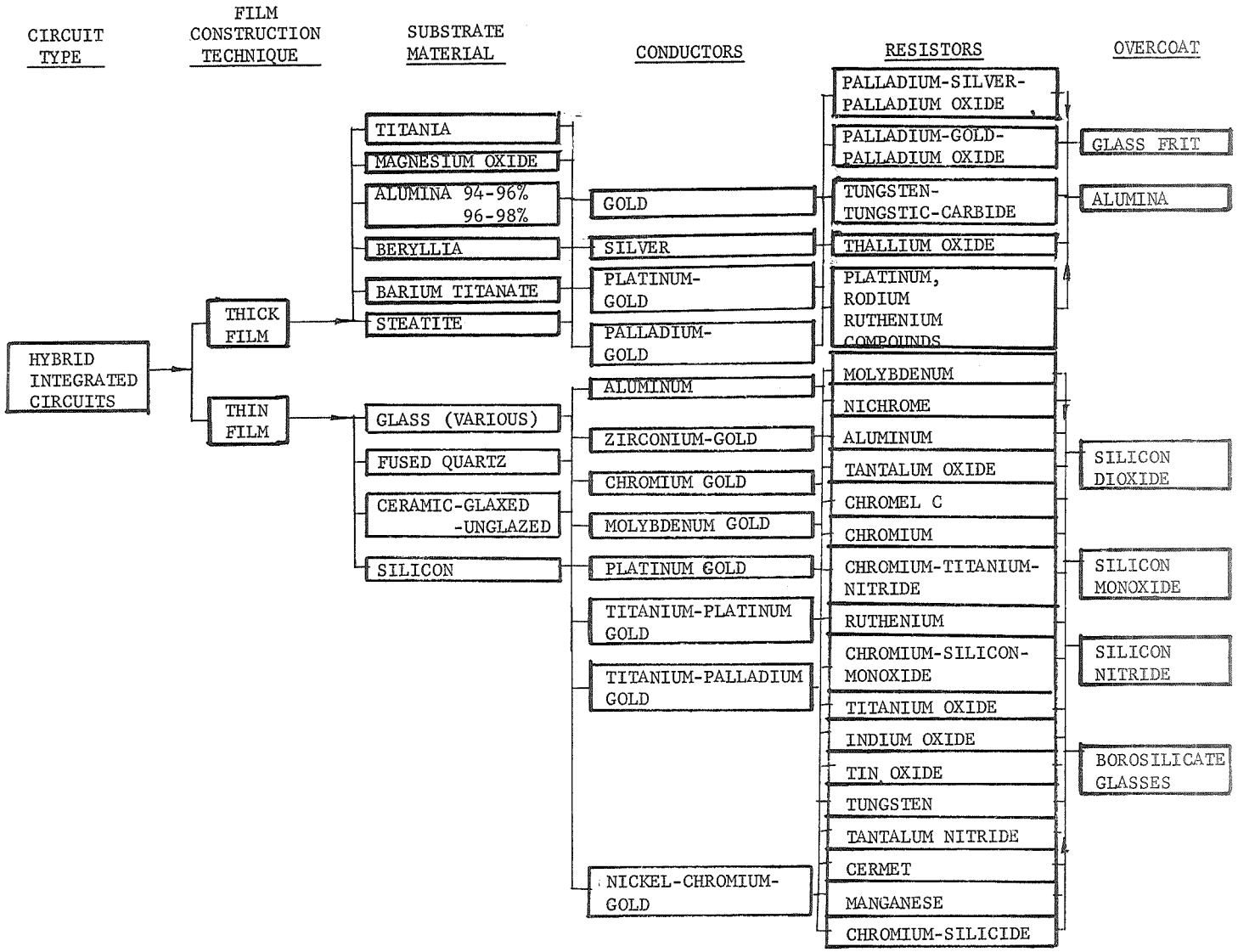

Figure 1 Manufacturing Variations

Only the general category of critical processes are identified such as masking or cleaning, as opposed to detailed process steps such as TCE wash, Freon or alcohol rinse, or dry. A complete list of processes and steps would become too complex when all variations are considered. The impact on reliability of inadequate control of each general process has also been incorporated.

Finally, those portions of other reports in this study that are directly applicable to hybrid circuits are merely referenced herein, rather than a rewrite and inclusion.

B. GUIDELINES FOR LONG-LIFE ASSURANCE

The life expectancy of properly designed and fabricated hybrid integrated circuits is greatly in excess of 10 years. Failures are caused primarily by defects introduced during fabrication as a result of insufficient process controls. An additional cause of failure is due to use of incompatible materials. Wear-out is only a minor problem which is alleviated by proper derating within the circuit design and in the application. The guidelines identified herein will enable use of hybrids with minimum likelihood of failure and maximum service life.

1. Design Guidelines

1) Use Bismuth-Ruthenium Oxide, Thallium, or Iridium as thick film resistor materials for greatest stability. Palladium and silver should be prohibited because of instability in reducing atmosphere (palladium) and migration (silver).

2) Palladium-gold or platinum-gold is preferred for thick film conductors. Silver should be prohibited to avoid migration at conductor-resistor interfaces.

3) Substrate thickness should be no less than 20 mils to avoid breakage problems.

4) Gold-silicon eutectic bonding of semiconductor chips is mandatory for highest reliability. Gold filled solder paste should only be used when eutectic temperatures cannot be used. Glass frit may fracture with thermal and mechanical stress. Epoxies, silicones, and other plastic or resinous materials have long term degradational effects.

5) Flip-chip, LID's, and beam lead devices should not be used due to limited availability of devices. The LID's cannot be thoroughly inspected and few hybrid fabricators can process flip chips reliably. Although the beam lead is extremely promising, the attachment processes are insufficiently established and practiced throughout industry at this time.

6) Use the metal lid and base type package. The ceramic package can result in photoelectric currents within active circuits.

7) Prohibit electroplating of thick film materials to avoid corrosion problems.

8) Submit each circuit to a worst case analysis. To assure long-life operation, the analysis should be based on end of life tolerances.

9) Use gold or gold on nichrome for thin film conductors because of documented life and stability capability.

10) Nichrome resistors should be coated with silicon dioxide to act as a moisture barrier.

2. Process Control Guidelines

The following processes must be reviewed and assurance obtained that they are adequate, stabilized, and under proper control by the manufacturers to minimize defects and to provide high yield, stability, and precise characteristics.

1) Substrate layouts avoiding thermal concentrations.

2) Precise mask preparation to provide resistors within acceptable trimming limits.

3) Thin film deposition control for proper film adhesion, within-tolerance resistors, and good drift and TCR characteristics.

4) Resistor trimming operation to maintain required tolerances.

5) Substrate and chip bonding processes for mechnical strength, good thermal conductivity, and minimal parametric change with age.

6) Wire bonding for mechanical strength and geometries avoiding shorts.

7) Thick film drying and baking processes to avoid outgassing and provide film stability.

8) Sealing process to provide hermeticity and prevent corrosion and drift from environments.

3. Test Guidelines

1) Individual chip families utilized such as resistors, capacitors, or semiconductors should be qualified to ensure basic capabilities of the devices used.

2) The supplier and the hybrid processes used should also be qualified for assurance of basic capability. The use of a standard "qualification model" hybrid for this use would minimize the requirements for qualification of individual circuit designs.

3) The conventional screen tests of MIL-STD-883, Method 5004 are adequate for hybrid integrated circuits.

4) Screening of individual chip devices including burn-in, thermal shock, and high temperature storage should be performed to the maximum extent possible. This will assure chip devices with a minimum probability of defects and increase yield. Semiconductor chips are not suitable for burn-in at the present time except for LID and beam leaded devices.

4. Application Guidelines

The application guidelines for monolithic integrated circuits (Chapter II) also apply to hybrid integrated circuits.

5. Special Considerations

1) Select suppliers with a successful history of fabricating similar parts. Hybrids requiring techniques and materials unique to his normal practice may be reliability risks because of the lack of experience.

2) The supplier's use of the required processes should be continuous to avoid reliability risks from start-up operations.

C. LIFE LIMITING PROBLEMS AND SOLUTIONS

1. Failure Mechanism Analysis

The failure mechanisms of hybrid integrated circuits include all the mechanisms associated with transistor, diode, and monolithic integrated circuit dice, die bonding, and wire bonding. The failure mechanism sections of those chapters are therefore related to this section, but are not repeated herein. Failure mechanisms are grouped in the following order:

1) Substrate;

2) Screening (or deposition), trimming and materials involved;

3) Chip elements, attachment, and interconnections; and

4) Packaging and miscellaneous items.

Thick film mechanisms which are applicable to thin film are not repeated in the thin film listing.

The mechanisms unique to hybrid circuits are those associated with the substrate; thick or thin film conductors, resistors, and capacitors; chip capacitors and resistors; and hermetically sealing the large package. Since tin-lead solder is used in die attach in many instances and is unique to hybrids, the failure mechanisms of that application are included.

It should be stressed that many of the failure mechanisms listed are due to manufacturing defects and will be detected by the manufacturer in normal processing and screening.

a. Thick Film Failure Mechanisms - Table 1 summarizes the predominant failure mechanisms discussed below, a description and cause of these mechanisms, methods of detecting the defects, and methods to minimize or eliminate the cause of these defects.

1) Substrate - Substrate defects are those faults occurring in the basic ceramic material on which the thick film is applied. This includes the attachment of the ceramic material within the package, impurities within the material and any stresses or cracks of that material which can affect the long-life operation of the circuit function.

Table 1 Failure Mechanism Analysis (Thick Film) (1 of 6)

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Separation of substrate bond resulting in destruction of circuitry.	Insufficient or improper bonding of substrate to base of package.	Acceleration or Mechanical shock.	Apply circuitry directly to base of package.
Cracked substrate resulting in loose chips.	High thermal stress imposed in laser trim of resistors.	Precap visual	Process control - change laser setting or trim speed.
Substrate breakage resulting in circuit destruction.	Substrate fragile due to low thickness.	Visual inspection.	Control minimum thickness to increased value.
Cracking of substrate from thermal shock.	Fracture of ceramic from thermal shock in solder dipping.	Visual inspection electrical test.	Preheat substrate prior to dipping.
Damage to adjacent resistors due to over-spray.	Deflection of abrasive trimming material to nearby elements.	Electrical test.	Require Laser trimming.

Table 1 Failure Mechanism Analysis (Thick Film) (2 of 6)

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Resistor degradation from electrostatic discharge from abrasive nozzle.	Flow of dry nitrogen carrier gas causes charge build-up on nozzle.	Electrical test.	Require laser trimming or use carrier gas of air with 600 ppm moisture content.
Change in Resistor value due to corrosion.	Incomplete removal of chemically active agents allows further reaction.	Electrical test	Process control in final wash to remove contamination.
Change in resistance due to leeching or diffusion of interface.	Leaching or diffusion at resistor - conductor interface of.	Electrical test	Change to more compatible materials.
Cracking of resistor film resulting in open.	Insufficient content of slow drying solvent, wetting agent and flow control additive in resistor ink.	Electrical test, SEM inspection.	Process control of printing ink materials.
Non-Operation of circuit due to worst case tolerance build-up.	Allowable tolerances of circuit elements great enough to cause improper operation.	Electrical test.	Perform worst case analysis. Prior to defining limits of elements.

Table 1 Failure Mechanism Analysis (Thick Film) (3 of 6)

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Short between conductors	Silver content in materials migrating across potential difference in conductors.	Electrical test, SEM inspection.	Change to gold alloy conductors or require 20 mil (minimum) spacing.
Palladium-Silver resistance change.	Change mechanism not understood - due to exposure to Hydrogen	Electrical test	Glass overcoat. Avoid Hydrogen atmosphere.
Resistor hot Spots	Current crowding at sharp corners.	Infrared thermal scanning prior to sealing.	Avoid sharp corners in resistor mask layout.
Conductor/resistor Blistering resulting in cracks.	Mismatch in thermal expansion of resistor, conductor, substrate.	Visual inspection.	Evaluation and selection of matched materials.
Transistor failure due to excessive heat from power resistors.	Centrally located power devices concentrates heat in localized area.	Electrical test, thermal plotting.	Locate larger power devices external to package containing heat sensitive elements.

Table 1 Failure Mechanism Analysis (Thick Film) (4 of 6)

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Lifting of solder pads due to low bond strength.	Adhesion of pads reduced by Leaching of silver-gold-solder combination.	Visual inspection, X-ray inspection pull test.	Change materials to more stable platinum-gold.
	Improper adhesion due to comtamination on substrate.	(same)	Process control in substrate preparation.
	Improper firing temperature for conductor material.	(Same)	Evaluation of process to determine optimum temperature.
Resistive Bond	Contamination or oxidization on surface or improper bonding.	Resistive measurement of lead to conductor.	Cleaning process control, bonding process control.
Poor conductor solderability	Contamination or oxidation on surface.	Visual inspection	Process Control
	Glass on surface	Visual inspection	———
Cracked semiconductor dice caused circuit failure.	Cracked dice not detected prior to installation or cracked in circuit assembly.	Electrical test precap visual	Require 100% visual inspection prior to die attachment and prior to capping.

Table 1 Failure Mechanism Analysis (Thick Film) (5 of 6)

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Shorted conductors at insulated crossover.	Pinhole in insulating glass allowed metal to metal short.	Electrical test	Thicker insulating layer, and visual inspection.
Shorted interconnecting wires to die or chip.	Bonding to lower level (down bonding) from element plus improper wire length.	Visual inspection, electrical test.	Process control in leadwire length and dress.
Loose semiconductor chip.	Cracking and separation of glass frit bonding material.	Visual inspection, electrical test.	Require eutectric die bond material.
Chip bond or solder-joint failure	Insufficient solder and improper bonding temperature.	Visual inspection, electrical test.	Process control, temperature controlled iron.
Circuit malfunction due to capacitive coupling.	Capacitive coupling between parallel lines provide false signals.	Electrical test	Rework to route clock lines away from sensitive circuit lines.

Table 1 Failure Mechanism Analysis (Thick Film) (6 of 6)

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Overbonding, Underbonding open wire bonds, weak bonds, lead to case short.	Refer to monolithic integrated circuit report.		Require sample bond pull test. 100% pull test not practical due to quantity of wires possible.
Loss of hermetic seal	Blow holes in solder seal.	Hermetic seal test	Improved materials and process control.
	Contaminated seal area prevented solder adherence.	Hermetic seal test	Controlled handling process, preseal wash.
	Separation of cover due to improper time-temperature in sealing.	Visual	Proper process control.
Loss of External Lead	Failure in lead fatigue due to lead damage.	Lead fatigue test	Proper handling procedures, Receiving inspection for damage on lead frames.
	Separation of external braze material	Lead Fatigue	Process control of time - temperature of brazing.
Short circuit due to internal particulate contamination.	Metal flakes and wire particles in package allowing short between conductors.	Precap visual electrical test.	Glass overcoat on conductors. Stringent precap inspection.

Separation of Substrate from Base of Package[1] - This failure, normally catastrophic, usually occurs during acceleration or mechanical shock screening test. The separation is caused by insufficient or incomplete substrate bonding or a degradation of the bond due to high temperature exposure during final sealing.

Cracked Substrate - Cracks can occur in the substrate due to high thermal stresses imposed during laser trimming of thick film resistors[2]. Ceramic chips can separate when exposed to mechanical stresses and cause further damage to the circuit. Precap visual inspection will detect this failure mechanism.

Substrate Breakage - Excessive breakage occurred when using 96% alumina substrates with a 10 mil thickness. This failure mechanism was eliminated by increasing minimum thickness to 20 mils.

Cracking of Substrate Due to Thermal Shock[3] - The thermal shock occurring in solder dipping the substrate can cause fracture of the ceramic material. This failure can be detected by visual inspection and electrical test. The mechanism can be minimized by preheating the substrate prior to solder dipping.

2) Screening, Trimming and Materials

Overspraying[4] - Overspraying is the deflection of abrasive trimming material which can result in abrading adjacent resistors and cause out-of-specification resistor values. Final electrical probing will detect these overtrimmed or damaged elements. Proper laser trimming will avoid this failure mechanism.

Electrostatic Susceptibility[4] - Electrostatic discharge through resistors will cause a change in the resistance. A damaging electrostatic charge can be built up on the abrasive nozzle when using a dry nitrogen pressure gas to drive the abrasive material. Final electrical probing will detect the out-of-tolerance resistors. The problem can be avoided by changing the gas to air containing 600 to 700 ppm of moisture, or by changing to laser trimming.

Corrosion[5,6,7] - Thick film conductors and resistors can be degraded by the incomplete removal of corrosive agents. The residual corrosive material may be traced to cleaning agents, chemically active plating solutions, solder fluxes, perspiration during handling, or environmental contamination such as sulphur in the air, or oils, or lubricants on equipment.

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[1]Superscripts refer to reference numbers in Section F.

Solder Leaching[3,8] - Leaching is the phenomena whereby a noble metal conductor dissolves into the solder coating. This can make a weak or brittle bond or, in extreme conditions, make attachment of leads or elements impossible. This mechanism can be minimized by bonding at the lowest temperature and shortest time above the alloy melting temperature, at which a satisfactory bond can be accomplished. Other ways of minimizing the problem are: 1) saturate the bonding alloy with the same noble metal used in the conductor, and 2) use flux specifically designed to reduce leaching.

Leaching or Diffusion at Resistor-Conductor Interface[9] - Leaching or diffusion can occur at the resistor-conductor interface which will result in a change in the resistance value. This problem can be minimized by selection of compatible materials used for resistors and conductors.

Open Resistor Due to Cracking of the Film[10] - The use of an ink or paste containing an insufficient quantity of slow-drying solvent, wetting agent, or flow control additive can result in open resistors due to cracks formed during curing. The open resistors can be detected by electrical probing and by SEM inspection. The problem can be minimized by a thorough test and analysis of materials prior to use.

Non-Operation of Circuit Due to Worst-Case Tolerance Buildup[11] - This failure mechanism can be avoided by requiring a worst case analysis of the circuit prior to specifying the procurement limits of elements and the trimming of resistors. Electrical test of the completed circuit will detect the mechanism.

Silver Migration[3] - Short circuit can occur between silver rich conductors with insufficient spacing. This effect can be minimized by requiring a minimum spacing between conductors of 20 mils. The problem can be avoided by use of gold alloy conductors. Electrical measurement and SEM inspection will detect the problem.

Palladium-Silver Resistor Change Due to Hydrogen Atmosphere[3] - The specific phenomena occurring is not satisfactorily explained, but it has been well established that a resistor will undergo a very drastic change after an exposure of only 24 hours in hydrogen. Application of a glass coating on the resistor will minimize the effect, but a more logical solution is to avoid the exposure to hydrogen.

Hot Spots at Sharp Corners on Resistors[3] - Sharp corners or very narrow paths will create hot spots which can affect the stability of the resistor. The hot spots can be detected by infrared scanning of the circuit prior to capping. The problem can be minimized by avoiding sharp corners in resistor patterns.

Conductor/Resistor Blistering[3,12] - The mismatch in thermal coefficient of expansion of the resistor, conductor and ceramic substrate can cause a crazing or cracking of the resistor layer.

3) Chip Elements, Attachment and Interconnection

Excessive Heating of Semiconductor Chips[11] - Non-operation can occur due to transistor failure caused by excessive heating. Hot spots due to centrally located power resistors can cause excessive heating of adjacent transistor chips. The failure mechanism can be prevented by locating all power resistors external to packages containing temperature sensitive parts. Electrical testing of the circuit or a thorough thermal analysis of the package will detect the failure.

Resistive Bonds[1] - Inoperative circuits can be caused by a high resistance in bonds due to contamination, oxidation or incomplete bonding. This failure mechanism is detectable by electrical test. The problem can be minimized by proper process controls covering contamination and bonding.

Lifting of Pads Due to Insufficient Adherence to Substrate[3,11] - This problem can be caused by any of the following: 1) Leaching of silver-gold-solder combinations; 2) incomplete bonding between contaminated surfaces, and 3) incomplete bonding due to improper firing temperature. A bonding-pad pull test will detect the problem prior to sealing or X-ray inspection after package sealing. The use of platinum-gold for conductors will eliminate the failure mechanism.

Shorted Interconnecting Wires to Die or Chip[1] - This failure mechanism typically occurs on semiconductor dice where the edges of the chip are at a different potential than the wire. The shorting of the wire is due to: 1) downbonding from a higher surface to a lower one, and 2) improper lead length, too short in length provides inadequate clearance, too long allows the wire under mechanical stress to deform and touch the edge of the chip. The failure mechanism is detectable in precap visual and electrical test. Proper wire length and dress will minimize the problem.

Shorted Conductors at Insulated Crossover[1] - Holes in the glass insulation layer or insufficient thickness allowing punch-through can result in a short circuit between conductors. Electrical test or a visual inspection prior to applying the top crossover conductor will detect the failure. A double glass insulation layer and thorough visual inspection will minimize the problem.

Loose Chip Elements Due to Glass Frit Fracture[1] - Glass frit used in chip attachment is subject to fracture and separation under mechanical or thermal stress. At times this failure may be detected by electrical test and possibly by X-ray. Eutectic or solder chip attachment eliminates this mechanism.

Chip Solder Bond Failure[11] - Insufficient solder and soldering temperature can result in solder bond separation under mechanical stress. Electrical testing will normally detect the failure. Proper process control will minimize the problem.

Capacitive Coupling[11] - Capacitive coupling due to long parallel conductors can cause circuit malfunction. Electrical testing will detect the problem. Routing clock lines away from sensitive circuitry and avoiding long parallel paths will minimize the problem.

Cracked Semiconductor Dice[11] - This mechanism can occur from installing dice previously cracked or cracking dice during assembly and wire bonding. Electrical test following thermal and mechanical stress testing will usually detect the failures. A 100% visual inspection on receiving the dice and inspection prior to sealing the package will minimize the failures.

Solder Joint Failures Due to Insufficient Heat and Solder[11] - This is corrected by pretinning leads, temperature control on soldering iron and certifying solderers. Visual inspection detects the improper joints.

Poor Solderability Due to Oxidation of the Conductors[3] - This failure mechanism can be minimized by keeping parts in a dry nitrogen box until ready for soldering.

Poor Solderability Due to Glass on Surface[3] - Glass oozing from the pores or crevices between metal grains during firing can also decrease the solderability of conductors.

4) Packaging and Miscellaneous

Separation of Cover[1] - Incomplete sealing of lid to package due to contaminated areas or improper time and temperature of seal operation. Normally detected during handling and seal leak testing, the mechanisms can be minimized by proper wash and seal process controls.

Loss of External Lead[1] - Fracture and separation of externally brazed on leads due to incomplete brazing. This fault can be detected in a non-destructive lead fatigue test. Stringent process control in brazing is required to minimize the problem. The problem can be avoided by requiring packages with continuous "through-the-glass" type lead frames.

Failure in Lead Fatigue[1] - External lead separation due to scratches, nicks, or work-hardening of the material. This failure mechanism is detectable by visual inspection for damage of lead frames prior to plating. Work hardening of material is not screenable. The problems are minimized by 100% visual inspection and by rigid specifications on materials.

External Lead Damage[1] - Although not a normal process, removal of excess glass flow on external leads has caused serious degradation of the mechanical strength of the lead due to scratches and nicks. Visual inspection prior to plating the leads will detect the damage. Process control will prevent the excess glass flow.

Particulate Contamination[1] - Particulate contamination which may result in intermittent operation or short circuit is more predominant in hybrid circuitry than in monolithic due to the increased number of chip and wire bonds and the additional thick film circuitry and materials. Detection is by precap visual inspection. Minimization is by process control through final sealing.

Loss of Hermetic Seal[13] - Incomplete hermetic seal due to contaminates that outgas within the sealing area, resulting in blowholes through the molten sealing material. Detection is by hermetic seal testing and X-ray. The mechanism can be minimized by thorough cleaning process control prior to sealing.

Photoelectrical Effects - Ceramic packages can transmit sufficient light to cause improper operation of sensitive semiconductor chips. The light striking the surface can generate false signals, particularly in high-gain amplifiers, although MSFC has experienced logic circuit switching also from this effect. Detection is by

exposing the package to a light source being switched off and on, while monitoring the output of the circuit. The problem can be minimized by shielding all packages from light during test and actual use. A more desirable solution is to eliminate the mechanism by using an all metal package for circuits containing semiconductor chips.

b. Thin Film Failure Mechanisms - Table 2 summarizes the predominant failure mechanisms discussed below, a description and cause of these mechanisms, methods of detecting the defects, and methods to minimize the cause of these defects.

1) Substrate

Cracking[14] - Cracking of substrate due to localized stresses from thermal shock or reflow soldering. These stresses occur due to random variations in substrate density and cause reflections in RF circuitry. Detection method is by substrate capacitance measurements, plating both sides and probing for capacitance variations. Minimized by using isostatically-formed alumina.

Craters or pits in Surface[14] - Due to pulling out of larger grains during lapping, buffing or polishing. The mechanism is caused by not controlling grain size to less than 6 microinches. The mechanism can be minimized by using material with extra-small grain size (0.6 microinch average) obtained by inhibiting the grain growth. Detection is by visual inspection (or SEM).

Surface Alkali Concentrations[14] - Both unglazed and glazed material can be a source of alkali contamination. The acceptable limit should be controlled by the supplier to less than 0.2%.

Uneven Surface[15] - An uneven surface can cause high local stresses in nichrome resistors, resulting in resistance change. The uneveness accelerates oxidation of the film.

2) Deposition, Trimming and Materials

Resistance Drift or TCR Change[16] - A change in resistor value and/or rate of resistance change vs temperature will shift from the initial value due to the following:

Segragation of Constituents - Separation of nickel and chromium of nichrome during deposition is due to different vaporization temperatures of the materials in the resistor mix. The mechanism is detectable by electrical test.

Table 2 Failure Mechanism Analysis (Thin Film) (1 of 3)

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Open circuit due to cracked substrate.	Internal stress due to random variations in density.	Substrate capacitance measurement.	Use isostatically formed substrates.
Variation in elements due to craters or pits in surface.	Pulling out large grains during lapping, buffing, polishing.	Visual or SEM INSPECTION.	Use extra-small grain & growth inhibiter in manufacturing substrate.
Drift of elements due to alkali ions.	Substrate or glaze contains alkali concentrations.	Electrical test, chemical analysis.	Specify acceptable limit (.200% alkali content.
Drift of elements due to local stresses.	Uneven surface of substrate.	Electrical test.	Specify acceptable limit of surface variation.
Resistor drift or change in TCR:	Segregation of materials due to differences in vaporization temperature.	Electrical test.	Use monometallic resistor material.
Drift, short or open depending on severity.	Chemical reaction with absorbed gases, encapsulants, contaminate liquids or solids.	Electrical test.	Process control on cleanliness, backfill with helium, Argon, etc.
Drift or open.	Mismatch in thermal coefficient of expansion.	Electrical test.	Limit temperature range or select compatible materials.
Drift, short or open depending on results of change.	Chemical/physical change in materials.	Electrical test.	Process control on final wash and dry.
Resistor drift, capacitor short.	Cracking or bulking of oxide.	Electrical test visual inspection.	Preheat substrate prior to deposition.
Open	Silicon monoxide dielectric reaction to oxygen or moisture resulting in fracture due to hardness or thermal mismatch.	Electrical test.	Backfill with inert atmosphere.
Drift or short in capacitors.	Embedment of silicon - monoxide or dust particles in dielectric	Electrical test.	Cleanliness process control. Dry box storage.
Drift or short.	Damage to dielectric due to explosion of gases during vaporization of chromium.	Electrical test visual inspection prior to final deposition.	Process control.
Drift	Semiconductor properties of tantalum oxides.	Electrical test.	

Table 2 Failure Mechanism Analysis (Thin Film) (2 of 3)

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Drift or open	Ionic contamination (chlorine) from organic rosin flux.	Electrical test Microprobe analysis	Cleanliness process control. Selection of non-ionic flux.
Resistor drift	Oxidation of tantalum resistors Also nitride formation.	Electrical test.	Limit temperatures to lower level.
Open resistors, open or short capacitors.	Thermal runaway due to oxidation and construction.	Electrical test.	Process control to prevent constriction.
Drift or open.	Crystallization due to diffusion at resistor-conductor interface.	Electrical test	Substitute less active diffusing material for conductor.
Drift	Ion migration of resistor material between adjacent resistors of different voltage potential		Process control - final wash and dry.
Drift	Increased or decreased current leakage due to ionic conduction in tantalum pentoxide dielectric.		Process control - final wash and dry.
Capacitor Drift	Gold counter-electrode on tantalum pentoxide dielectric lifting and allowing moisture penetration.		Backfill with inert, dry atmosphere.
Capacitor short	Tantalum carbide formation in tantalum dielectric from oil of or secondary sputtering from shielding material.		Process control - Avoid contaminating materials.
Capacitor short	Silver migration across capacitor dielectric.		Prohibit use of silver as capacitor electrode.

Table 2 Failure Mechanism Analysis (Thin Film) (3 of ~)

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Resistor drift	Alkali diffusion from substrate into resistor film.	Electrical test	Process control - spec limit on substrate contaminate contents.
Drift	Porosity of deposited films from oily residue on substrate.		Process control - cleanliness.
Open	Electrolytic corrosion due to moisture and external voltage potential or internal electrochemical potential of dissimilar metals.		Backfill with dry inert atmosphere.
Open Circuit	Improper bond due to faulty setting of bonder.	Electrical Test	100% non-destructive bond pull.
Malfunction of circuit.	Wire bond error. Connection to wrong pad.		Interconnect pattern glass screened on substrate.
Open or intermittent circuit.	Pad damage due to probing. Possible loose particles in pkg.		Proper probe-tip shape. Minimize wiping action.
Chip element parameter change.	Overbonding time or temperature. Exposure of chips.	Electrical test	Optimum selection of die bond material, optimum time/temperature process.

Chemical Reaction with Absorbed Gases, Encapsulants, Contaminant Liquids, or Solids - The newly formed compounds may have drastically different characteristics. A typical example is the reaction on resistors by amine from resin hardners.

Thermal Coefficient of Expansion Mismatch Stress Induction Between a Film and Substrate - In this instance, the problem can be minimized by heating the substrate prior to deposition.

Chemical or Physical Change of Film with Temperature - This occurs in materials in which stabilization and crystallization are at the same temperature.

Cracking and Bulking of Oxide[16] - This is due to residual stresses and can be minimized by preheating the substrate prior to deposition.

Porosity[16] - Porosity can result from contaminated oily residues on wafers. This will result in circular defects when tantalum is sputtered on the surface and anodized.

Oxidation[16,17] - Increasing resistance due to the formation of tantalum oxygen or tantalum-nitride compounds. This failure mechanism usually results in a parameter drift and typically occurs at elevated temperatures greater than 150°C. The parameter change can be detected by electrical test.

Semiconductor Dielectric[16] - TiO_2 film dielectric can exhibit semiconductor properties. This has been indicated by electrical anomalies of TiO_x films.

Thermal Runaway[16,17] - This failure mechanism in tantalum resistors results in an open and is due to a combination of two other mechanisms: (1) oxidation and (2) constriction. When current passes through an area constricted enough to cause a hot spot, local oxidation occurs. The increase in resistance due to oxidation results in further constriction. This cycle continues until the resistor either cracks or vaporizes, causing an open circuit. The thermal conductivity of the basic substrate material has a significant effect on this mechanism, i.e., poor thermal conductivity can cause or accelerate the problem. The failure can be detected by electrical test or thermal potting of the circuit prior to capping.

An equivalent mechanism occurs in tantalum capacitors. In the formation of the dielectric tantalum pentoxide (Ta_2O_5), the presence of minute contamination particles prevent complete anodization of the tantalum film. These faults in the dielectric allow small but very localized currents to start. The dielectric in the path of the current is heated which in turn lowers the resistance, allowing an increase in current. The cycle continues until failure occurs. The failure will result in an open circuit if series resistance does not sufficiently limit the current. When current limiting occurs due to large series resistors the failure mode will be short circuit.

Humidity[16] - Tantalum Pentoxide (Ta_2O_5) dielectric film has been observed to undergo a much greater change with humidity conditions when built with gold rather than with gold-nichrome film counter electrodes. This effect was due to the lifting of gold and absorption of a monolayer of moisture. Use of an organic impregnant, a polyethylene polybutylene mixture, reduced the capacitance sensitivity to moisture to a very low value.

Reaction of Silicon Monoxide to Oxygen and Moisture[16] - This mechanism results in fracture due to hardness and low thermal expansion coefficient.

Particulate Contamination[16] - Embedment of SiO or dust particles in the dielectric film yields a rough surface or pinholes.

Carbide[16] - Tantalum capacitors that failed under accelerated test conditions were found to contain Tantalum Carbide in the Ta_2O_5 dielectric film. The carbon source was assumed to be from the diffusion pump oil or secondary sputtering from stainless steel shielding in the apparatus.

Dielectric Degradation by Ionic Conduction[17] - Ionic conduction in the tantalum pentoxide dielectric can result in increased current leakage or a decreasing leakage. Stressing in the temperature range of 125 to 250°C with zero bias will result in very large increases in leakage current with eventual leveling off at a high value. A bias voltage will inhibit the leakage increase. When the bias voltage is high enough, the leakage current will decrease. This effect has occurred with 15 volt bias at 125°C and 25 volts at 175°C. The mechanism can be detected by electrical test.

Ion Migration[16,17] - Ionic migration can occur between adjacent resistor stripes where a difference in dc voltage potential exists, resulting in an increased resistance of the more positively biased portions and a corresponding decrease in the negatively biased resistor. This mechanism can occur across a U-shaped resistor or between parallel resistors. High voltage potential and elevated temperature will accelerate the mechanism. Electrical test or probing will detect the change.

Ionic Contaminate[18] - Ionic contamination in the form of chlorine has been introduced into packages with organic resin fluxes. The problem was minimized by venting the package during sealing to allow gases to escape, then plugging the vent hole.

Cations Diffusion[19] - Increasing resistance has been detected with increasing temperature cycles. It has been theorized that the mechanism is due to contamination of the film by diffusion of alkali ions from the substrate into the resistor film.

Silver Migration[19] - A major and frequent failure mode of capacitors with silver electrodes is a short circuit due to the silver migrating across the dielectric interface and through pin holes. The use of silver as electrodes should be prohibited in high reliability programs.

Electrolytic Corrosion[18] - Degradation of nichrome (NiCr) resistor and interconnecting lead wire has occurred due to electrolyte ions transported across a moist insulator surface by (1) an induced external potential, and (2) the potential developed internally in the form of electrochemical potentials of dissimilar metals in electrical contact.

Explosion of Gases[16] - Short circuit due to puncture of the SiO dielectric film resulted when an explosion of gases in chromium chips occurred during vaporization of the chromium.

3) Chip Elements, Attachment and Interconnections

Wire Bond Separation[16] - Open circuit due to improper setting of wire bonder. Fault minimized by periodic calibration of equipment. Failure mechanism detected by precap visual, thermal and mechanical stresses followed by electrical test. This problem can be minimized by a periodic lead bond pull.

Bond Wire Error[20] - Due to the increased number of wire bonds in hybrids and the possible layout of interconnecting pads, bond wire errors are more likely to occur. This problem can be minimized by careful layout of interconnect circuitry, optimum pad shapes and interconnect diagrams screened on substrate.

Probe Damage[20] - In the process of electrical probing semiconductor dice prior to separation of a wafer, some test equipment is designed to "wipe" the surface to establish good electrical contact. This wiping action will sometimes peel bits of the metal, which may interfere with the wire bond or may break loose in later testing.

Excess Bonding[20] - Changes in chip parameters have occurred due to excess die bonding times and temperatures. The problem was minimized by optimum selection of bonding materials and attachment time and temperature schedules.

4) Packaging and Miscellaneous Items - Refer to thick-film hybrid section for applicable failure mechanisms.

2. Design

a. Selection Criteria for Thick Film Hybrids - Most hybrid thick film circuits are custom designed for each specific application. Therefore, the major selection criteria of hybrids must be concentrated on the processes and materials used and the manufacturer's past history of successes or failures rather than on usage history of a specific circuit configuration as applicable to monolithic circuits.

The processes with known time-dependent failure mechanisms that can affect the life of the program must be identified and avoided or minimized. In addition, process selection and control must be imposed to minimize the failure mechanisms detailed in Section C.1 of this report. The selection criteria for individual chip elements is that portion of each individual part report that is applicable to the basic uncased element, including attachment and inter-connection criteria. The attachment and inter-connecting materials may have to be modified to be compatible with the thick film conductors and pads.

Table 3 lists the various design factors to be considered for selecting long life thick film hybrids as discussed in the following paragraphs.

Table 3 Thick Film Hybrid Selection Criteria

DESIGN FACTORS	REMARKS
Processes and Materials	Resistors: Prohibit Palladium and Silver. Use Bismuth-Ruthenium-Oxide, Thallium or Iridium series.
	Conductors: Prohibit Silver. Use Palladium-gold or Platinum-gold.
	Substrates: Use Alumina 94-96% or 96-98%, or Beryllia.
	Element or Substrate Attachment: Prohibit glass frit, epoxy, silicone and plastics, eutectic bonding preferred, solder approved.
	Beam Lead: Greatest potential but not fully established. Not recommended.
	LID's: Use only when burn-in at element level is required.
	Bump or Flip-Chip: Prohibit usage
	Ceramic Carriers: Not recommended except when chip isolation is necessary.
	Ceramic Package: Do not use ceramic lid and bottom on packages containing semiconductor chips. Use metal package.
Manufacturer's History	Usage History: Select suppliers with successful history on similar parts; both discrete elements and completed hybrids.
	Review Processes: Ensure suppliers processes do not violate this selection criteria.
	Review Failure Mechanisms: Review vendor fall-out and failure history for definition of optimum screening.
	Versatility: Investigate supplier's capability to incorporate new processes when established.
Multiple Procurement	Large Quantity: Must have multiple sources available for long term programs; sources should have similar processing for uniform reliability.
Active Production	Processes: Must be in active production to avoid reliability risks of "start-up."
External Materials	Space Environment: Ensure low outgassing, no sublimination, and no time degradation.
Design Check	Worst-Case Analysis: Require worst-case analysis performance on circuitry for production use.

1) Process and Materials Selection - Processes and materials that are known to be reliability risks must be prohibited from use where long-life assurance is required. Processes and materials that require control are identified in the following paragraphs.

Palladium - Resistor material containing palladium must not be permitted in high-reliability parts. It is a well established fact that resistors containing Palladium are subject to change by reduction or oxidation[21] when exposed to a hydrogen atmosphere, or other reducing or oxidizing environments. Since satisfactory resistor materials are available that are not so drastically affected, the specific materials must be identified and required in the production of parts. Acceptable resistor materials include Bismuth, Ruthenium, Thallium and Irridium pastes. The paste consists of combinations of the noted materials usually as oxides, in a mechanical mix of particles typically less than one micron in size, plus[10] a flux or frit to adhere the material to the substrate and a vehicle to provide screenability. Both the materials involved and the proportion of each tend to be critical. Acceptable[21] pastes include "Birox" a Bismuth-Ruthenium-Oxide (DuPont), Thallium based series (Electro-Science Lab), "Firon" (Electro Materials Corp. of America), and "BB" series Ruthenium pastes (Alloys Unlimited-Plessy, Inc.).

Silver - Material containing silver must not be permitted in applications requiring long life. Past usage history of resistors containing silver indicate a failure mechanism of migration[22,23], both at the conductor-resistor interface, and between the resistor and adjacent conductors. In addition, silver must not be used in conductors for those reasons previously noted and also due to the fact that silver will go into solution with tin-lead solders, causing a change in characteristics.[22]

Substrate Material - There appears to be no reliability risk with the 94 to 96% or 96 to 98% alumina or Beryllia except for excess breakage on thickness of less than 20 mils. Flatness of the substrate will affect manufacturing yield but does not impose a reliability risk.

Element and Substrate Attachment - Glass frit die bonding should be avoided wherever possible since it may fracture when subject to thermal and mechanical stress. Epoxy, plastic and other resinous type bonding materials must be prohibited internal to a package, since the long term characteristics are unknown and tests indicate present material combinations are degradational.[24]

Attachment of substrate to base of package and elements to substrate should be accomplished by means of a eutectic or solder paste. If eutectic bonding temperatures are degradational to the chips or elements, a gold filled solder paste may be used. Eutectic bonding is preferred for semiconductor attachment. Gold-tin and gold-germanium eutectics should not be used. Tin-lead solder is satisfactory only for capacitor and resistor chip attachment. Techniques of localized heating of the area of attachment are preferred because other elements are exposed to reduce heating.

Beam Lead - Of the numerous chip attachment methods in existence, beam lead appears to offer the greatest potential reliability. Until a full selection of elements are available with beam leads and the attachment processes are more firmly established and practiced by industry, the process cannot be recommended for long-life hybrids.

Leadless Inverted Devices (LIDS) - The use of LIDS can provide additional reliability risks such as: (1) wire and die bonds cannot be properly inspected since the element is normally covered with a drop of resinous material; (2) when attached in the normal inverted manner, the number of extra bonds required is equal to the number of pads or terminations on the element; (3) unique bonding schedules and fixtures are required; and (4) the inverted configuration prevents a thorough precap inspection of elements. Therefore, LIDS can only be recommended when it is deemed absolutely necessary to burn-in elements prior to installation and it cannot be satisfactorily performed in another manner.

Bump or Flip-Chip - In the past, the bump or flip chip has proven to be unsatisfactory for general use. Although this attachment method is presently in use by IBM, it must be prohibited on long-life parts.

Ceramic Carriers - The practice of mounting a semiconductor die on a ceramic chip then bonding this "carrier" chip to the thick film substrate should only be permitted in those instances where (1) the semiconductor must be isolated from the substrate, and (2) an isolated pad cannot be incorporated within the thick film circuitry..

Ceramic Package - Ceramic packages containing current-sensitive circuitry such as high-gain amplifiers have failed to function due to photo-electric effects.[25] The failures were due to sufficient light passing through the ceramic lid to cause photoelectric currents to be generated within a semiconductor circuit. These leakage currents were then amplified by the circuit. Therefore, a metal lid and base type package is recommended for high-reliability operation.

Electroplating - Electroplating of thick film materials should be prohibited because of the associated corrosion problems noted in paragraph C.1.a.2).

2) Manufacturer's History - In selecting monolithic circuits, a primary selection criteria is the usage history of that specific part. Since a hybrid circuit is normally a custom designed circuit, the usage history is only applicable to the elements or chips incorporated into the overall circuit. The manufacturer's capability in producing a reliable thick film network is a critical item. This capability is only reflected by the successes and failures of hybrid circuits of similar complexity and processes by the same supplier. Therefore, it becomes mandatory to not only investigate the manufacturers of the discrete elements but also thoroughly review the history of the supplier of the completed circuit. This review must include investigation and definition of the equivalent processes defined in paragraph C.2.a.1) herein, to ensure prohibited materials and processes are not being used. Determination of failure mechanisms usual to the supplier's processes should be made for optimum screening definition. The history of success or failure of similar parts on prior programs should be examined. In addition, the production must be versatile in that, as newer processes are sufficiently established to prove high reliability, those processes can be introduced into the production facility, e.g., beam lead.

3) Multiple Procurement Sources - Multiple procurement sources, for large quantities of hybrids, is important not only for discrete chips used within the package but also for the overall circuit. A minimum of two suppliers should be considered who have similar processes for uniform reliability. Additional details on the importance of multiple sources is noted in the monolithic integrated circuit report (Chapter II).

4) Active Production - The processes supplied on long life parts must be used in active production. In many instances a "learning curve" occurs in the start up of production using processes not in normal production. To avoid the reliability impact of this learning period, it is recommended that only "active" processes be approved.

5) External Materials - For space usage, materials that outgas or sublime must be prohibited. In addition external materials containing time dependent failure mechanisms must be avoided, such as those materials that degrade with age.

6) Design Check - Thick film circuits are an approach to compact packaging using film and chips elements as opposed to discrete parts. Because they are constructed of elements possessing parametric and other variations, it is important that, similar to complex discrete circuits, they be designed such that the intended function will be successfully performed regardless of these variations. Therefore, for long life applications, it is mandatory that the individual elements of hybrid circuits be derated similarly to discrete parts, and that the entire circuit be verified by a worst case analysis which includes end-of-life parameter tolerances.

b. Selection Criteria for Thin Film Hybrids - The selection criteria for thin film circuits are identical in most areas to those of thick film circuits as defined in Section C.2.a herein. Differences do occur in those processes unique to thin films. The specific criteria unique to thin film are specified in the following paragraphs and are listed in Table 4.

1) Substrate - The substrate must a) be chemically stable so that it does not interact with the deposited films, b) have a thermal coefficient of expansion that is nearly the same as any materials to be deposited or attached, c) have a high enough thermal conductivity to be effective in heat dissipation, d) exhibit good electrical insulating properties, and e) have a smooth surface. Glazed Alumina or Beryllia satisfy these requirements and are recommended.

2) Circuit Design and Layout - Similar to thick film circuits, it is necessary that Worst Case Circuit Analysis be performed on each circuit prior to designing the layout and the mask preparation. The analysis will prevent malfunction due to the worst case tolerance buildup in the finished circuitry. The circuit layout is also extremely important to prevent interaction between elements, and to assure an evenly distributed temperature from power dissipation of elements.

Table 4 Thin-Film Hybrid Selection Criteria

DESIGN FACTORS	REMARKS
Processes and Materials	Resistors: Use Nichrome 80-20, unless data on better material is available. Tantalum, Chromium, Titanium and Tungsten are potential candidates. Use chip resistors for large resistance.
	Conductors: Use gold in additive process, gold on Nichrome in subtractive process with Nichrome resistors. If other resistor materials are approved, select compatible conductor material.
	Substrates: Use Alumina 94-96% or 96-98%, or Beryllia, with glaze coating.
	Film Overcoat: Coat all Nichrome resistors with Silicon Dioxide.
	Capacitors: Thin-film capacitors are not recommended. Use chip elements.
	Interconnect Wires: Use gold wire, ball bonded only.
	Package: Use all metal package when circuit includes semiconductor dice, solder or weld lid. Prohibit use of epoxy or other plastic adhesives.

NOTE: For other design factors see Table 3.

3) Conductor Material - Although there are numerous thin film materials available, gold (or gold on nichrome) is the only one that appears to have considerable life and stability documentation available.[25,26] Therefore, gold is the recommended thin film conductor material. Other materials may be satisfactory, but should not be approved until reliability data has been reviewed.

Aluminum[27] - Due to the intermetallic growth of aluminum-nickel, and the susceptibility to electrochemical corrosion, both resulting in open circuits, this combination cannot be recommended for long-life assurance. In the event that nickel-chromium resistors in contact with aluminum conductors must be used; i.e., nichrome resistors on semiconductor surfaces containing aluminum metallization, additional process controls are required. Very careful control and clean-up of all wet chemical processes to prevent corrosive residue is an absolute necessity. In addition, the aluminum conductor and nichrome resistor *must* be covered with SiO_2 to act as a moisture barrier. Note: Silicon monoxide (SiO) is not as satisfactory as SiO_2 as a moisture barrier.

4) Resistor Material - Just as with conductors, there are several thin-film resistor materials. The most commonly used, and most-documented material, is Nichrome (80% N; 20% Cr).[28] This material is recommended for long-life assurance.[25,26] Considerable documentation may exist on the other materials, but was not found in this study.

5) Overcoat - Silicon monoxide appears to be almost universally used throughout industry and, therefore, is the recommended material. Silicon monoxide does not strongly adhere to gold, but is a necessary coating on nichrome resistors for protection and stability. Exception: see paragraph C.2.b.3).

6) Chip Resistors - The maximum resistivity of nichrome 80-20 is approximately 500 ohms per square, the maximum practical resistance is approximately 100K ohms. For resistance values greater than 100K ohms, or less when the surface area is critical, the use of chip resistors is recommended.

7) Thin-Film Capacitors - Due to the large surface area required for film capacitors, and the inherent problems in dielectric films, the use of thin-film capacitors is not recommended. A large variety of capacitor chips are available and require far less space than film elements.

8) Package - Both MSFC and Martin Marietta have noted serious effects when ceramic packages, containing transistors, diodes, or integrated circuits, are exposed to light. The translucent ceramic allows sufficient light to reach the semiconductor die to cause photo-generated currents. It is recommended that every hybrid circuit, which includes semiconductor dies, be packaged in an all metal package.

c. Results of Survey - A survey of electronic part users revealed that most aerospace agencies and companies utilize MIL-STD-883 for typical high reliability hybrid microcircuit test requirements. A notable exception[29] was reported wherein 100% non-destructive bond pull test and monitored vibration was performed. Wire bond quality on hybrids is not as uniform as on momolithic integrated circuits, and the non-destructive bond pull test provides a 100% screen as well as a check on the wide and rapid variations in bond strength that may occur. The intent of monitored vibration is to more effectively detect conductive particulate contamination within sealed packages.

d. Alternate Approaches - Alternate approaches for hybrid circuits are identical to those defined for monolithic integrated circuits and are detailed in Chapter II. Areas deserving further study are (1) investigate methods of screening and burn-in of discrete uncased parts, as applicable for hybrid use and (2) compile, in a single report, the effort and results to date, of the beam lead technology. A great number of studies and reports are in existence but no single report ties them all together and provides a detailed conclusion. It is also recommended that additional effort be expended in the design of a standard "qualification model" hybrid circuit. The standard could be designed so as to require low and high resistance film resistors with trimming to X% of some predetermined value, use of specific values of resistor and capacitor chips, and use of identified semiconductor dice. The circuit stability at designed test points, at various temperatures and lifetimes, could be then used as a quality indicator among potential manufacturers. It is further believed that this concept could provide maximum reliability information on a supplier's controls while testing a very minimum sized sample of circuits.

e. Hardware Life - Since a hybrid integrated circuit may contain monolithic integrated circuit chips, transistor and resistor dice, and resistor and capacitor chips, the life of the hybrid is that of the element having the shortest life. The actual package, substrate, and thick film elements have no verified wearout mechanisms. Properly constructed and applied hybrids have a life expectancy far in excess of ten years.

f. Application Guidelines - Application guidelines for hybrid integrated circuits are identical to those of monolithic integrated circuits (Chapter II).

D. TEST METHODOLOGY AND REQUIREMENTS

1. Qualification - Due to the fact that hybrid circuits are generally custom designed and in relatively small quantities, it is more realistic to qualify the processes and the supplier rather than each circuit configuration. Therefore, for both thick and thin film hybrid circuits the following qualification program is recommended.

a. Resistor and Capacitor Chips - Each specific chip family such as ceramic capacitors or film resistors must be qualified and listed in an approved parts list.

b. Semiconductor Dice - All semiconductors must be selected from a qualified parts list and from a qualified source, such as, JANTX and QPL-19500. The basic intent of this selection is to provide dice of proven design and long-life capability.

c. Thick or Thin Film Network - The qualification of the processes and supplier should consist of: 1) complete documentation of the processes and materials used in the circuits to be supplied, and 2) performance of qualification tests similar to those specified for monolithic integrated circuits on a "typical" circuit configuration of medium complexity.

The circuits subjected to the testing must be manufactured with the documented processes and must include thick or thin film resistors and semiconductor chips. It would also be desirable to perform the testing on circuits containing resistor and capacitor chips so as to include the attachment method in the qualification test. Use of a standard "qualification model" circuit (see para. C.2.d.) could serve as a standard of comparison between suppliers as well as a vehicle for qualification of supplier and processes.

It should also be noted that due to the larger size and mass of the hybrid circuit, qualification environmental stress levels may have to be reduced to values lower than limits imposed on monolithic circuits.

d. Accelerated Testing - As indicated in listings of failure mechanisms, the majority of failures are due to: a) internal contamination causing corrosion or migration; b) extreme mismatch in thermal expansion of joined materials; and c) reduction or oxidation due to the internal atmosphere. Since all three

failure categories are accelerated by temperature, it appears that subjecting the parts to elevated temperature can, in fact, provide an accelerated test method for detection of inherent failures.

The temperature for optimum acceleration will be dependent on the specific processes used in manufacturing the circuits. Extreme caution must be observed in determining the test temperature, to ensure that new failure mechanisms are not introduced. Typical examples of new mechanisms that can be caused by the testing are: a) destructive stresses due to thermal expansion beyond that which the circuit is specified; and b) loss of dice, chip or substrate adhesion from exceeding eutectic temperatures of the bonding material.

Prior to instigating accelerated testing it is absolutely mandatory that step-stress testing be performed on circuits with identical processes to determine the acceptable levels of stress that may be imposed and to identify those failure mechanisms introduced by exceeding the acceptable levels.

2. Screening

Screening consists of the electrical, mechanical and thermal stresses imposed on each circuit prior to delivery by the manufacturer. These tests are designed to accelerate specific failure mechanisms in an inferior part without causing degradation in a good part, or triggering new failure mechanisms.

A typical high reliability screening program for hybrids is identical to that imposed on monolithic integrated circuits, except that the maximum stress levels in mechanical testing are usually lower. The reduction in stress levels is due to the greater mass of the larger package for the hybrid. The conventional sequence of tests specified in MIL-STD-883, Method 5004, as shown in Figure 2, is more applicable to hybrid circuits than the sequence as modified and defined for monolithic integrated circuits (Chapter II). This difference in screening is due to the fact that wafer level inspections of monolithics is not applicable to hybrids. In the sequence defined in Figure 2, it is recommended that temperature cycling be deleted because thermal shock is more effective.

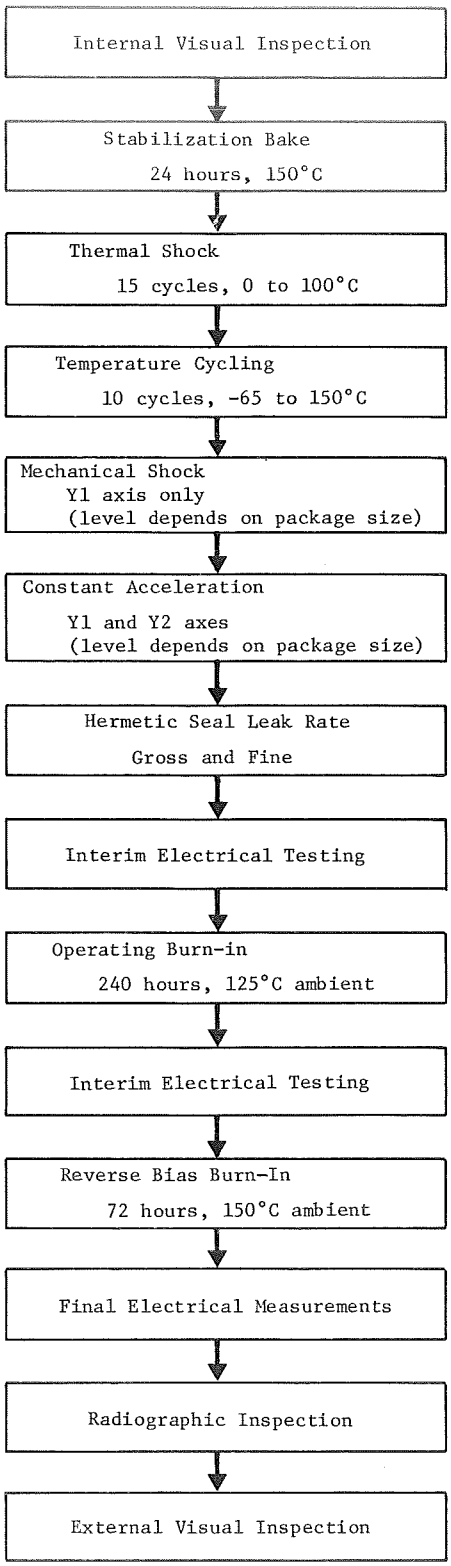

Figure 2 Traditional Screening (MIL-STD-883)

In addition to the screening required in assembly, each chip element and semiconductor die must be screened individually. It is recommended that the chip and die screening include thermal shock and high temperature storage with pre- and post-electrical measurements. The measurements should include a maximum drift limit.

Until such time that beam leaded parts are readily available and processes standardized, operating burn-in at the chip level is not economically feasible.

3. Burn-In

Operational burn-in of the completed hybrid circuit is required to ensure that no portion of the circuit will drift beyond that allowed by worst-case analysis. As recommended by MIL-STD-883, the burn-in time should be 240 hours minimum, in an ambient of 125°C. Recent investigations have determined that internal package atmosphere may contain sufficient moisture, that can condense at low temperatures, to cause corrosion. As a result of the investigation, an additional low temperature burn-in was also recommended, particularly when aluminum and nichrome fils are in contact.

Operational burn-in of all chip and die elements is highly desirable, but not absolutely necessary. The reliability of additional processes required to provide operational capability must be considered. As an example, using LID's (Leadless Inverted Devices): a) the semiconductor chip is bonded to the carrier; b) all wires are attached from chip to carrier; c) a drop of epoxy or silicone is placed on the die for protection in handling, and d) following burn-in and tests, the LID must be attached to multiple pads in the circuit. MSFC Astrionics Lab has experienced excessive failures due to bad wire bonds. It was determined that the coating of the chip was opaque and did not allow proper visual inspection of bonds, which, in turn, were substandard.

Resistor and capacitor chips may be inserted in spring-loaded holders for burn-in, and removed for attachment to the circuit. This operation should not degrade reliability unless; a) pressure is great enough to fracture the chip; b) contamination is introduced; or c) the contact pads are damaged.

Therefore, it is imperative that a user consider, not only the reliability gained by burn-in, but also the risks of degrading reliability by the manner in which burn-in is achieved.

E. PROCESS CONTROL REQUIREMENTS

All processes and materials used in the manufacture of thick and thin film hybrid integrated circuits can be considered critical. Improper control of any of the items defined in Tables 5 and 6 could have detrimental effects on the life of the part.

Table 5 Critical Process and Materials (Thick Film)

CRITICAL PROCESS/MATERIAL	EFFECTS OF INADEQUATE CONTROL	REMARKS
Circuit Design	Inoperative circuit due to design errors.	
Worst Case Analysis	Inoperative circuit due to tolerance build-up.	
Layout of Substrate	Inoperative or drift due to thermal concentration.	
Substrate Materials and Finish	Open, short or drifts due to substrate effects - contamination, roughness, thermal stresses.	
Manufacture of Screens	Tolerance beyond trimming limits.	
Cleaning Substrate	Drift due to contamination, non-adherance of films.	
Conductor Ink Selection	Drifts, migrations, leaching due to incompatible materials.	
Resistor Ink Selection	(same)	
Screening Process	Out of trimming tolerance due to thickness.	
Drying Process	Drift of resistors.	
Film Baking Process	Drift due to improper cure, outgassing.	
Resistor Trimming	Out of tolerance, damaged.	
Storing of Inks	Out of tolerance due to settlement/separation of materials.	
Screening Paste on Pads for Chips	Leaching due to incompatible materials, non-adherance of chips.	
Element Attachment Time/Temperature	Insufficient adhesion; drift of chip parameters.	
Wire Bonding	Open bonds.	

Table 5 (concl)

CRITICAL PROCESS/MATERIAL	EFFECTS OF INADEQUATE CONTROL	REMARKS
Precap Visual	Poor overall quality.	
Substrate Attachment	Insufficient adhesion.	
Package Selection	Photo effects on semiconductor chips.	
Packaging Sealing	Corrosion, drift due to environment.	

Table 6 Critical Process and Materials (Thin Film)

CRITICAL PROCESS/MATERIAL	EFFECTS OF INADEQUATE CONTROL	REMARKS
Substrate Selection and Preparation	Excessive resistor drift or TCR.	Require glazed Alumina or Beryllia. Cleaning process immediately prior to use.
Material Used as Source	Element drift, excessive TCR.	Material mixtures, such as Nichrome, tend to separate in vaporization.
Deposition Equipment Adjustment - Rate and Temperatures	Out of tolerance resistors, possibly resistive conductors. Insufficient film adhesion.	
Circuit Worst Case Analysis	Inoperative due to tolerance build-up	
Mask Layout	Interaction between elements, hot spots.	
Mask Preparation	Out-of-triming-tolerance of elements.	
Resistor Trimming	Inoperative circuit.	
Deposition of Material, Thickness Monitoring	Out-of-trimming-tolerance due to excessive thickness. Excessive drift if too thin. Change in value and TCR if exposed to atmosphere prior to coating.	
Chip Attachment	Excess mechanical stress from thermal excursions if improperly attached.	
Substrate Attachment	May separate under thermal or mechanical stress, resulting in circuit destruction.	
Bond Wire Attachment	Separation of bonds, shorting of wires.	
Package Sealing	Loss of hermeticity resulting in eventual circuit degradation.	

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IV. TRANSISTORS

by E. R. Freeman

IV. TRANSISTORS

A. INTRODUCTION

This chapter deals with the failure mechanisms, qualification, screening and process control requirements, and application guidelines for transistors intended for long-life usage. The first section is a summary of the conclusions and recommendations made in the rest of the report. Section C deals with the failure mechanisms for transistors; criteria for part and supplier selection; alternate approaches in the design, test and use of transistors; and application and derating guidelines. Section D deals with evaluation, qualification and screening testing of transistors aimed at eliminating defective devices. Section E deals with processes and materials used in transistor fabrication and needed controls. The last section lists acceptable transistor types and unacceptable constructions and designs. The types of devices discussed are bipolar, junction field effect and MOS transistors packaged as discrete elements.

Figure 1 shows a typical transistor construction and illustrates the definitions used in this report and is intended to aid those unfamiliar with terminology.

B. GUIDELINES FOR LONG-LIFE ASSURANCE

Storage and service life of a properly assembled, tested and applied transistor is virtually unlimited. Predominant in-service failures are due to surface contamination causing parametric degradation and ultimate shorting, particulate contamination resulting in shorts, and interconnect wire failure causing opens. Use of the selection, screening, application and handling guidelines included herein will enable transistors with a minimum probability of defects and practically indefinite service life.

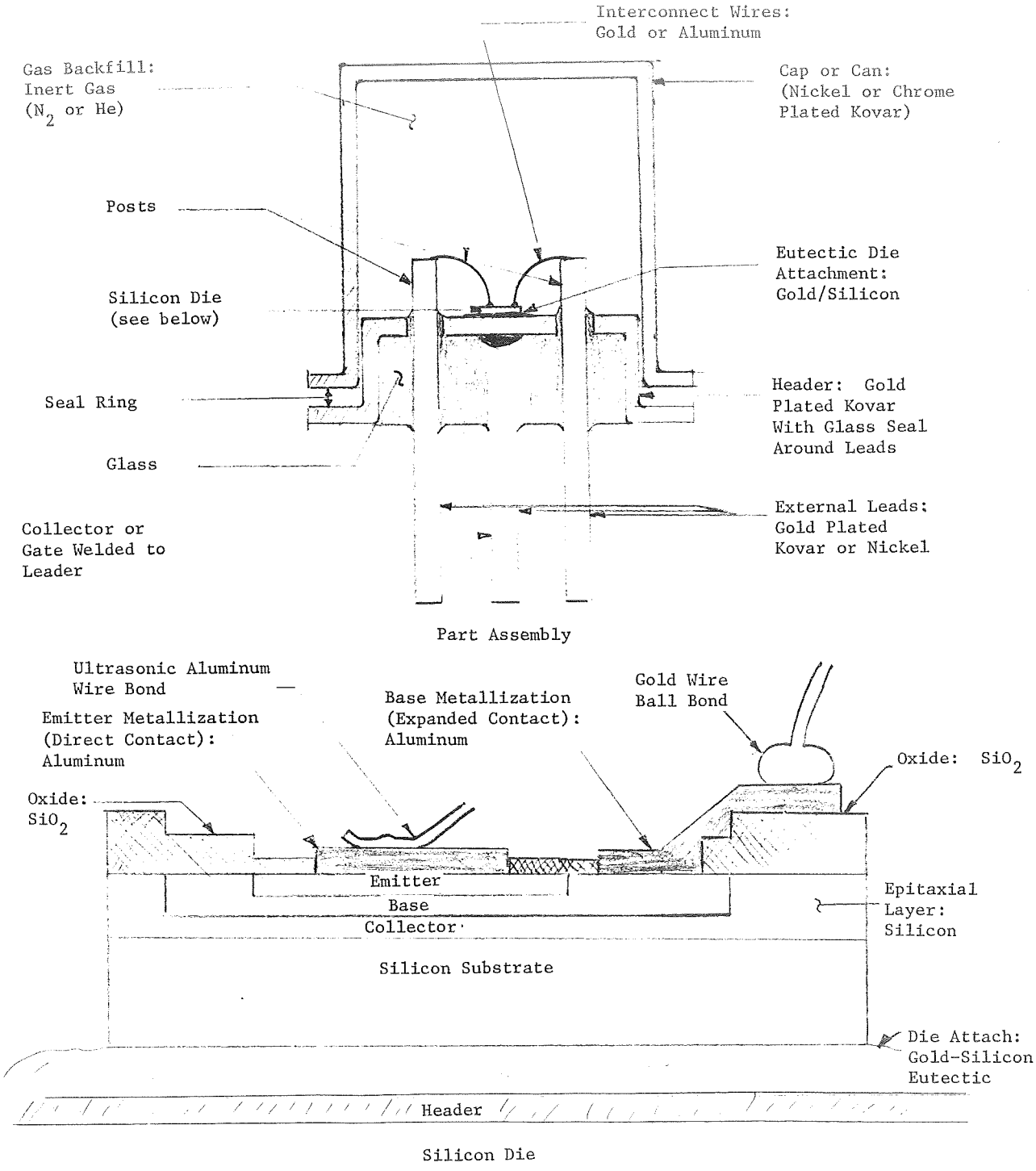

Figure 1 Typical Transistor Construction

1. Design Guidelines

1) Use silicon planar die constructions. Mesa, grown junction, alloy, or germanium types have serious life limiting problems. Mesa constructions, however, are necessary in large power, high voltage devices.

2) Use die with thermally grown oxides since silicones and varnishes introduce undesirable surface contaminants.

3) Phosphosilicate glass passivation over thermal oxides and metallization is recommended to getter surface contaminants and protect metallization.

4) Aluminum metallizations should be at least 10,000 Å thick to avoid thinning over oxide steps and be of sufficient cross-sectional area to limit current density to 5×10^4 amps per square centimeter to reduce effect of electromigration (primarily for devices with expanded contacts).

5) Do not use polymer or glass frit die attachments since they do not afford the thermal conductivity or mechanical strength of eutectic die attachment. (Soft solders for some power devices is unavoidable, but not preferred.)

6) For large die, temperature compensation phases, such as molybdenum tabs or ceramic wafers, should be employed to prevent die cracking under thermal stress.

7) Where the die is dielectrically isolated from the case, both die and isolator must be eutectically mounted to afford minimum thermal impedance and maximum strength.

8) Monometallic interconnect systems are preferred to eliminate intermetallic related bond failures. Gold-gold is the most preferred, but least available. Al-Al is acceptable only when the wire is ultrasonically bonded and 7 to 10 wire diameters slack is left between post and die. Gold-aluminum is acceptable only from suppliers who have demonstrated consistent success with this type of interconnection.

9) Hermetically sealed packages (10^{-8} ATM/cc/sec) must be used for encapsulation of the die since epoxies, plastics, and other encapsulants do not afford adequate moisture protection.

10) Dry inert back-fill gas within the package must be present to prevent interaction of the gas ambient with the die materials.

11) Inert non-reactive materials must be used for package and lead materials and platings to preclude package degradation due to corrosion or contamination and must provide sufficient mechanical strength to withstand handling, shipping and installation environments.

2. Process Control Guidelines

1) Process controls used by manufacturers are usually implied by the severity of screening and qualification tests required. Controls implemented will usually be sufficient to afford reasonably high screening yields; (i.e., 20-50% of initial lot will survive screening tests).

2) Diligence of the part manufacturer in controlling cleanliness, assembly, inspection and handling of the parts can best be monitored by the user through 100% pre-cap visual, source inspection, lot acceptance testing, and fingerprinting (construction analysis).

3. Test Guidelines

1) A 100% non-destructive interconnect wire pull is recommended to eliminate defective wire bonds. Sound bonds will not be degraded.

2) A rigorous pre-cap visual inspection of the die and header assembly is essential to eliminate common assembly defects. Perform die inspection (preferably at the wafer or die level) to eliminate defective die.

3) Screening tests on 100% of the parts, which include burn-in, HTRB, thermal cycling, mechanical shock, hermeticity, and parametric tests are essential to eliminate defective parts.

4) Qualification tests are performed once on a group of candidate parts. These tests are arranged in a manner aimed at specific failure mechanisms. The qualification also includes characterization and fingerprinting of the device to establish a baseline for validity of the qualification for future procurements. The fingerprint is performed on each successive lot to determine conditions which could invalidate qualification. Part type remains qualified as long as screening results, acceptance test results, and part performance are acceptable.

4. Application Guidelines

1) The part must be properly specified electrically and mechanically. The part must be capable of meeting the needs of the circuit without exceeding its abilities. Otherwise serious overstress of sound parts could result.

2) Maximum voltage and current ratings should be derated to 75% of rating to provide safe operating margins in the application.

3) Junction temperature should be maintained below 110°C for all silicon devices to reduce effects of thermal stresses and related metallurgical changes within the part.

4) Time/temperature dependence of part parameters should be determined and appropriate circuit derating applied to accommodate end of life drift of performance parameters; (e.g., gain, switching speed, etc).

5) Mechanical installation of the part must provide adequate thermal transfer and preclude severe mechanical stresses.

6) Low leakage devices should be protected from high voltage, low energy transients, such as electrostatic discharges to preclude junction degradation.

5. Special Considerations

1) Part types selected should be fabricated using material/process combinations that are understood and whose failure mechanisms are known. Screening can only be effective when it is aimed at known failure mechanisms.

2) Part types with established reliability afford high confidence with minimum qualification and evaluation effort; however, obsolescence and design utility are key factors in part selection. Types with limited history must be thoroughly evaluated for potential reliability problems.

3) Parts should be selected which are available from several sources to avoid procurement problems if one supplier discontinues production or has difficulty with production.

4) Sources selected should have a stable labor, facilities, and management situation. The part selected should be in reasonably continuous production and be fixed in design and characteristics. Larger volume manufacturers, although somewhat more independent, afford more lot to lot homogeneity than their smaller competitors.

5) Lot traceability back to pre-cap visual inspection is desirable to identify potential lot problems if in-service failures are encountered.

C. LIFE LIMITING PROBLEMS AND SOLUTIONS

1. Failure Mechanism Analysis

There are five failures modes for transistors: shorts, opens, intermittent operation, parametric degradation, and external mechanical degradation. Tables 1 through 4 describe the failure mechanisms for the above failure modes, the methods of detecting the failure causing defect before the parts are accepted by the user, and the method for reducing the probability of obtaining a part with such defects or causing defects in good parts. It should be pointed out, however, that a very small percentage of parts will elude detection and in-service failures will be encountered even with the most rigorous screening and process control methods.

a. Parameter Degradation - The most common and most costly to detect failure mode in transistors is degradation of part electrical characteristics. This failure mode, while usually not catastrophic to using hardware, can seriously degrade hardware performance if sufficient design margin is not allowed and is usually indicative of a part whose life is severely shortened. The mechanisms contributing to parameter degradation are shown in Table 1.

Contamination Mechanisms - Contamination and corrosion are the most prevalent causes of parameter degradation and can be categorized by the process in which they are introduced: diffusion, oxide growth, washes, and gas ambient sealed in the can. Contaminated doping materials and ambient atmospheres during the diffusion processes result in wafers with a low yield of acceptable transistor die, usually as a result of improper resistivities or channel forming ions at the $Si-SiO_2$ interface. Bad dice are normally removed by the manufacturer through electrical test.

Failure Mechanism	Description	Method of Detection	Method of Minimizing Defect
Surface Contamination	Ionic material on surface of Si or SiO_2 providing leakage paths (Cl, Fl, etc.). Alkali ions in or on oxides creating channels (Na^{+}, Ca^{++}). Precipitated dopants on surface of silicon during oxide growth.	HTRB with temperature sufficient to mobilize contaminant and field concentrations sufficient to localize it, monitor leakage and gain variations before and after test.	Proper wash/etch sequences and recycling of solutions. Practically unavoidable. Keep oxide growth temperature below diffusion temperatures.
Contaminated Gas Ambient	Non inert gases in the capping station. Non hermetically sealed cans. Evaporated contaminants from die surface.	Fine and gross leak seal tests will detect non hermetic seal. Sample residual gas analysis will detect lot problem with sealed ambient.	Sealed capping station supplied with pure, dry N_2 gas at pressure greater than 1 Atm. High temperature bake-out prior to capping.
Bulk Defects	Die cracks in active areas providing leakage paths. Inclusions, dislocations, stacking faults and other discontinuities providing localization zones for impurities. Poor geometry design leading to areas of current crowding and hot spots.	Power cycling will aggravate cracks. Power aging at high temperature will localize impurities in fault areas, increasing leakage and lowering gain and breakdown voltage. Close monitoring of gain and leakage before and after aging will detect parts with unstable characteristics.	Visual inspection of each die rejecting cracked ones. Virtually impossible to eliminate all dislocations. Careful die layout and thermal analysis using thermal microprobe on an operating device to locate hot spots in design.
Oxide Defects	Cracks, holes and thin spots providing leakage paths to exposed silicon.	HTRB with temperature sufficient to mobilize contaminant and field concentrations sufficient to localize it, monitor leakage and gain variations before and after test.	Gross defects detectable with a visual inspection after oxide growth. High temperature growth desired to form dense, uniform oxides.
Die Attachment	Voids in eutectic which results in increased thermal impedance.	X-ray normal to die lookimg for voids under die. Precap visual inspection looking for voids around die.	Proper temperature, scrubbing time, materials and cleanliness prevents voids.
Interconnect	Resistive contact of metallization to silicon due to oxide growth in the window. Intermetallic phase formations in gold wire to aluminum metallization interconnects.	High temperature storage will aggravate these phenomenon. Forward diode drop of each junction should be monitored watching for slight increases (50-100 mv).	Complete oxide cuts and proper alloy procedure. Temperature should be sufficient to form S_i-Al alloy. Use monometallic interconnects preferably gold wire, gold metallization.
Electrical Stress	Electrostatic discharges rupturing low leakage junctions. Over power and current.	Identify all devices with 1 nA leakage currents or less as susceptible and protect accordingly.	Short all leads together until part is installed. Handle in electrostatically neutral environment. Current limited, transient suppressed power supplies and adequate oscillation suppression for D. C. operation.

Table 1 Parametric Degradation

During diffusion and oxide growth, alkali (Na+, Ca++, etc) ions often are present in the diffusion ambient. These normally come from the walls of the tube, oven refractories and the diffusion gas systems. These ions can also come from handling of the wafers and storage in uncontrolled environments. Alkali ions in and on SiO_2 layers produce inversions and channels across junctions (Reference 1, 2, and 3). (Note: All part manufacturers polled indicated no significant problem in this area and that screening normally removes most defective parts.)

Contaminated washing solutions and improper washing sequences contribute greatly to part failure due to the ions they introduce on the die and header surface and between layers on the die. Degreasers such as Trichlorethylene (TCE) and etches such as hydrofluoric acid (HF) introduce negative ions (Cl- and F-) which can contribute significantly to part leakage (Reference 4) and sometimes etch Al contacts (References 5 and 6). Contaminates in, and constituents of, washing and etching solutions, such as deionized water, isopropyl alcohol, NaOH, HCL, and HNO_3 can also introduce ionic contamination or corrosive elements which can cause devices to fail.

The last of the contaminating media is the gas ambient surrounding the die. Hermetically sealed transistor packages are strongly recommended due to the degrading effects of organic solvents, catalysts, and hydrocarbons used in plastic encapsulation. In addition, water vapor, free oxygen, and hydrogen can be degrading also. The effects of H_2O are most significant in parts which have alkali ions in or on the die (References 2 and 3). H_2O tends to activate corrosive ions such as Cl and also forms conductive films with ionic contaminants causing leakage paths (References 5 and 7). While it appears to slow down the growth of intermetallic compounds in wire bonds (Reference 8), oxygen tends to contribute to growth of resistive contacts on incomplete contact windows and increases sheet resistivity of Al films due to oxidation (Reference 9).

Contamination Detection Methods - Elevated temperature bake-out for several hours in an inert atmosphere prior to capping is necessary to drive off surface contaminants. High temperature storage of sealed parts is effective in stimulating the effects of gas ambient and surface contaminants. The most effective method of detecting surface contamination is through HTRB. The temperature sufficient to activate the contaminating ion is usually 150-175°C. Reverse bias of both junctions to achieve 10^6V/cm field strengths is desired (Reference 3) to move the ions to localized areas so

they can be detected on post HTRB leakage measurements. Higher temperatures permit shorter test times, but should be carefully considered to avoid starting other time dependent mechanisms, such as "plague." Burn-in at rated junction temperature will aggravate the effects of bulk contaminants, as well as corrosive contaminants. Large increases in leakage or degradation of gain will identify devices which are contaminated.

Contamination Minimization - Use of phosphosilicate glasses or silicon nitride passivations has been shown to be effective in gettering alkalis, thereby reducing their effects (References 3, 10, 11, and 12).

The best way to avoid surface ions due to washing and etching, is a frequent change of wash and etch solutions and a proper etch/wash sequence to remove "hard to clean" ions. Deionized water in an ultrasonic wash is an excellent collector of ionic contamination and is recommended as the last step in any washing procedure. Also, the least number of steps required to manufacture the part afford a lower probability of introducing contaminants. Pure, dry N_2, He, or other inert gas backfill and a hermetic seal, are necessary to provide a stable part. Spectrographic analysis of gas backfill on a sample basis of the lot of parts is advised to discover potential lot problems.

Bulk and Oxide Defect Mechanisms - The next class of defects causing parameter degradation is somewhat related to contamination existing in the part. Contamination to some degree is inevitable so the more perfect the bulk and oxides, the lesser the effect of contaminants. Die faults and dislocations act as localization zones for mobilized contaminants during operation, resulting in breakdown, leakage, and gain failures (References 13, 14, and 15). The dislocation density in the starting material does not affect yield as much as the density of those introduced during processing (Reference 13). The ions can be the dopant material or contaminating ions, and the dislocation must be near or in a junction, and must collect ions to cause failure (Reference 13).

Another phenomenon, especially in large area die, is inclusions of polycrystalline Si during the epitaxial growth, due to particulate contamination on the prepared silicon substrate surface, which propagate through the collector base junction resulting in low breakdown voltages and high leakage currents (Reference 15).

Defective oxides (pin holes, cracks, misaligned oxide cuts, thin spots) will contribute to several mechanisms. In bipolar transistors, mobile ions can migrate through discontinuous oxide to the $Si-SiO_2$ interface depleting the base thus degrading gain (Reference 16). In FETS and bipolars the discontinuities provide leakage paths from metal connections to active areas.

Other bulk defects which affect transistor operation (especially interdigitated power types) are misalignment of base and emitter diffusions, or gradients in diffusion rate of the base and emitter diffusions leading to irregular base widths and variations in emitter resistivity. These phenomenon lead to localized secondary breakdown due to hot spot formation (Reference 17) and punch-through under reverse bias. Die cracks which propagate into diffused areas reduce breakdown voltage and increase leakage current and will ultimately produce shorted junctions.

Bulk and Oxide Defect Detection Methods - The majority of defective die fabricated are usually removed by the manufacturer prior to part assembly through wafer level electrical tests. Visual die inspection will also eliminate die with gross defects.

Thermal shock or power cycling will aggravate die cracks. HTRB and power burn-in at rated junction temperature with delta reject criteria on gain, and leakage measurements, will detect the majority of parts with time dependent failures due to oxide and bulk defects.

Bulk and Oxide Defect Minimization - Discovery of most bulk defects during die fabrication is expensive and tedious usually involving high magnification microscopy. Bulk defects seem to be tolerable to the industry provided yields are high enough. However, since transistor die with some bulk defects are unavoidable at the present state of semiconductor processing technology, they pose a life limiting failure mecahnism for a small population of parts.

Cleanliness and high temperature growth usually yield a very good grade of oxide (Reference 3). Sample SEM inspection of wafers to detect oxide defects is frequently performed on integrated circuits, but few transistor manufacturers have such a capability.

Die Attach Mechanisms - One of the most critical parameters to a power device and many small signal transistors is not electrical but thermal. Thermal impedance, junction to case θ_{jc}, affects almost all other parameters, since most parameters are dependent upon junction temperature. If too high, catastrophic part failure results. The primary interfaces affecting θ_{jc} are the silicon to eutectic, eutectic to header (or insulator), and header (or insulator) to stud. The most common defect affecting θ_{jc} is voiding of the eutectic under the die leading to hot spots on the die and localized avalanche.

Voids can be caused by oxidized or contaminated Si on the back of the die precluding the formation of a good eutectic phase, intermediate phases formed in the eutectic die from diffusion or migration, inadequate gold-Si preforms or platings, and poor die attach procedure resulting in formation of undesirable intermetallics (Reference 18).

Die Attach Defect Detection Methods - X-ray of the header, prior to capping, with X-ray axis through the die surface could be used to detect voids. Pre-cap visual inspections will detect voids around the edges of die, but not under the die. Power aging at maximum junction temperature and high temperature reverse voltage tests will detect some of these failures. A non-destructive secondary breakdown test (increasing voltage to an acceptable threshold at elevated temperature) would eliminate many parts with hot spot locations on the die contributing to premature secondary breakdown. Several suppliers employ measurement of V_{BE} (SAT) under high (twice rated) current pulse conditions to identify parts with marginal thermal conductivity.

Die Attach Defect Minimization - Clean, unoxidized surfaces and proper time-temperature controls for the attaching materials used are the only effective means for achieving proper die attachment. Gold-silicon eutectic materials afford the most reliable die attachments. Some manufacturers use low melting point (soft) solders. These are often unacceptable due to interaction with other part materials and instabilities with temperature and aging. Parts with soft solder die attachments should be carefully evaluated prior to use in long-life applications. Epoxies are not acceptable.

Interconnect Mechanisms - The last category of parameter degradation due to built-in defects is interconnect flaws. Interconnect wire degradation will be discussed later in the section dealing with opens, but their initial effect is an increase in contact resistance which increases low current voltage drop in the forward direction. Another phenomenon which increases contact resistance is the growth of SiO_2 in the contact window usually as a result of incomplete etching of the SiO_2 in the window.

Interconnect Defect Detection Methods - High temperature storage will aggravate both phenomenon. Low current forward voltage drop measurements, especially emitter to base, will usually detect parts with resistive contacts.

Excess Voltage, Current, and Power Mechanisms - The last category of parameter degradation deals with what happens to structurally and electrically sound parts due to excess power, voltage and current conditions. While most overpower and current conditions result in shorts or opens, moderate excess power or current conditions can lead to increases in leakages and decrease in gain as well as breakdown due to formation of small channels or punch-through sites in the junctions which are resistive in nature. A special case of overvoltage application is electrostatic discharge through junctions with leakages on the order of one nA. It has been observed at Martin Marietta Denver Division that junction field effect transistors and the emitter base junctions of certain bipolar devices can be degraded with electrostatic discharges on the order of 200V. (This problem has long been recognized with MOS devices.) The energy of such pulses is very low due to the limited capacitance involved, but is sufficient to cause very localized ruptures of junctions at the $Si-SiO_2$ interface. The short exhibits microplasma under reverse bias conditions and, in general, increases leakage by orders of magnitude. Devices with higher initial leakage (10 nA or more) appear to be able to bleed off the charge build-up at a high enough rate to prevent rupture of the junction. The low leakage devices have fewer leakage paths and field densities increase rapidly with time as the voltage wave propagates along the junction. Failure analysis indicates that the failure results from localized rediffusion of Si at the $Si-SiO_2$ interface. The source of the diffusant is postulated to be aluminum from the metallization migrating along the Si surface to the rupture in the same manner as "white spears" form due to overcurrent and power (Reference 19). More work is necessary to define the actual failure mechanism.

Excess Voltage, Current and Power Defect Minimization - Much work has been done in preventing damage to low leakage devices during handling, test and installation due to electrostatic damage. Leads are shorted together until part installation to prevent potential gradients from appearing across junctions; work stations where unshorted parts are handled have electrostatic precipitators, grounded work areas and, in some cases, personnel are grounded through a protective resistor. Hardware with susceptible parts are stored in foil lined bags and, in some cases, with external pins shorted. The encapsulation of cordwood modules has been a source of electrostatic charge levels sufficient to damage susceptible parts. Care is taken to keep all external leads and pins of cordwood modules at ground potential during the potting operation. The number of failures encountered is reduced considerably using the aforementioned techniques. With the advances in the industry in cleaner and better processing more devices will have to come under these controls to preclude degradation from electrostatic discharge.

Other types of degradation, due to overvoltage or current, can be avoided through careful stress and thermal analysis of the part application and care in part and system level test and conditioning.

b. Shorts - Electrical shorts and their related failure mechanisms are shown in Table 2. Most shorts are a result of poor workmanship by the part manufacturer and are easily detected by a rigorous pre-cap visual inspection. Parts which have permanent electrical shorts are rejected the first time they are electrically tested. Intermittent shorts usually occur during part test or installation and are very difficult to detect once the part is capped. These failures can be catastrophic to using hardware if proper circuit redundancy is not provided.

Failure Mechanism	Description	Method of Detection	Method of Minimizing Defect
Solid Conductive Contamination (Note: Particles smaller than the smallest interconnect separation are not considered harmful.)	Silicon chips from die scribe and break or fragments of other die. Aluminum flakes accumulated on wafer probe points and deposited on die during wafer electrical test. Fragments and smears of eutectic or steel wool slivers from tweezer clean during die attachment. Balls, pigtails, extra wires from wire bonding. Airborne material on header and in can prior to capping. Weld slug from cap weld operation.	Precap visual inspection of header assembly and can will detect most of these workmanship defects. A monitored vibration/shock test will detect particles in sealed parts. High impact shock is desired to free bound particles. X-Ray will detect dense particles (Gold, Iron, Nickel) in sealed parts (Al, Si are not visible).	Ultrasonic wash after breaking usually adequate. Probe pressure and travel must be kept to a minimum. Ultrasonic die attach scrubbers eliminating need for hand operation. Workmanship Ultrasonic clean of headers and cans prior to capping and storage in controlled environment. Die mounted on plateau above well ring or splash guard around weld ring.
Assembly Defects	Misoriented die forcing crossed wires or improper connection to external pins. Excess wire loops. Downbonding with inadequate loops allowing wire to touch edge of die. Posts touching sides or top of cap. Plating bridges or slivers on header shorting leads.	Precap visual inspection will detect most gross defects. Electrical test will detect parts with permenent shorts. Acceleration in all direction at high levels (50 Kg or better will force gold leads with excess loops to move. X-Ray will detect improper post to cap clearance.	Workmanship Workmanship Workmanship Workmanship Workmanship
Bulk Defects	Cracks and chipouts into active die areas. Inclusions, dislocations, stacking faults, and other discontinuities in or close to junctions. Inversion layers and channels due to impurities in or on Si or SiO_2. Diffusion spikes due to photolithography defects or misregistration of masks producing thinned bases.	Precap visual will detect cracked die (except under bonds). HTRB will induce the inversion layers and channels to form. Electrical test will detect parts with permanent shorts.	Sharp stylus, uniform scribe and break pressure and flat wafers yield clean fractures. Dislocation free die almost impossible. Clean washes, gases, etches help but some contamination inevitable. Channel stoppers are desired. Proper application and curing of photoresists, clean masks and prepare wafer surfaces, care in alignment.
Oxide Defects	Cracks, pin holes, thin spots under metallization, making undesired connections. Misaligned contact window cuts.	Precap visual will detect gross defects. Electrical test will detect parts permanently shorted.	Proper application and curing of photoresists, clean masks and prepare wafer surfaces, care in alignment. Proper application and curing of photoresists, clean masks and prepare wafer surfaces, care in alignment.
Metallization Defects	Metal bridge due to poor photolithography. Metal peeling introducing flakes Smears	Precap visual will detect gross defects. Electrical test will detect parts permanently shorted.	Workmanship Controlled deposition and alloy processes. Workmanship
Electrical Over-Stress	Migration of Al from one conductor to another under SiO_2 along Si surface. Punchthrough in the junction. Local thermal avalanche (secondary breakdown).	Electrical test will detect damaged part. White Spears, discolored oxides, localized or gross remelt and rediffusion zones, melted metallization are all signs of excessive bias or signal.	Proper current/voltage limiting. Heatsinking for power applications. Transient and uncontrolled oscillation supression.

Table 2 Shorts (and Intermittent Shorts)

Contamination Mechanisms - The greatest contributor to shorts is conductive contamination internal or external to the part. Aluminum flakes piled up on probe points during wafer level test which drop on the die across metallization paths and large fragments of silicon produced during scribe and break are two common forms of particle contamination introduced at the wafer level. Excess eutectic piled up over the sides of the die, fragments of eutectic either attached or loose, and fragments and slivers of steel wool from tweezer clean are common forms of contamination introduced during die attachment. Excess pigtails, extra wires and balls from the wire cutting operation are types of conductive contaminates introduced during wire bonding. Improper header fabrication and plating result in flakes and slivers of kovar or gold causing internal or external shorts. Improper storage and cleaning of die header assemblies and cans result in airborne contaminants which get sealed into the part. Weld slag balls can be introduced during the capping operation.

Contamination Detection Methods - Bound particles can often be loosened with a high impact shock test. Most free particles can be detected with an electrically monitored vibration test, but this is usually expensive. Several part users employ a technique referred to as PIND testing. Acoustic noise generated by particle impingement on the sides of the device can be monitored during random vibration coupled with a mechanical shock pulse. X-ray can detect large particles (2 mils) of gold and iron and extra wires.

Contamination Minimization - Conductive particles smaller than the smallest interconnect separation and non-conductive particles are not considered important. Acceleration of uncapped headers and ultrasonic cleaning of uncapped assemblies are methods of removing contaminants prior to capping. Glassification over metallization is the best defense against conductive particles. Beam lead die, since they are normally mounted metal side down and are passivated with silicon nitride, or other materials, provide parts which are less susceptible to shorts due to particles.

Assembly Defect Mechanisms - Assembly defects, such as improper die orientation forcing interconnect wires to cross or connection of the wrong contact to the external pins; excess wire loops; down bonding where inadequate clearance is provided between the edge of the die and the wire; misalignment of wire on bond pad; and bent or too high posts allowing them to touch the side of the can, all can cause shorts.

Assembly Defect Detection Methods - A pre-cap visual inspection eliminating parts with such defects is desired. X-ray will show crossed wires and improper post to cap clearance. Constant acceleration in all three axes will cause excess wire loops to touch other areas in the can.

Assembly Defect Minimization - Use of beam lead chips significantly reduces the number of operator sensitive assembly procedures and thereby the number of defects.

Die Defect Mechanisms - Die defects causing shorts can be categorized in three areas; bulk, oxide, and metallization. The bulk and oxide defects which cause parameter degradation, discussed previously, often produce shorts. Masking misalignment and improper diffusion depths can result in shorted junctions. Lifting and undercutting of photoresist or mask defects and misalignment can result in bridged junctions or metallization. Dislocations, inclusions, and other discontinuities located in the junctions can cause shorts. Cracks in the die as a result of scribing or improper die attach and wire bonding provide channelling paths along exposed silicon surfaces. Cracked die can also result from gross mismatches in temperature coefficient from header to die in power devices (Reference 20). Cracks, holes, and thin spots in oxide under metal paths frequently result in shorts to the active areas under the metal for expanded contact devices (wire bond at the die is made on the oxide rather than at the oxide window). Contaminants on the die surface or buried in the oxide often produce inversion layers and channels sufficient to short junctions. Smears of metallization due to improper handling, die attach, and wire bonding procedures short active areas.

Die Defect Detection Methods - A good pre-cap visual inspection will eliminate most gross die defects. High temperature storage and HTRB will aggravate oxide and bulk defects and mobilize contaminants to form shorting channels and inversion layers. Glassification of die has been successful in reducing smearing of metal. Thick eutectics or temperature coefficient matching phases such as molybdenum tabs are desired in power devices to eliminate thermally induced cracks (Reference 20). Channel stoppers are desired around outside of die to keep channels from propagating to edge of the die in single diffused epitaxial devices and guard rings or field plates around the base collector junction are often used to prevent channels in other geometries. Extension of base metallization over the base/collector junction line is a commonly used type of field plate.

Excess Voltage, Current and Power Mechanisms - The last of the shorting mechanisms is electrical overstress. The most common is excess current/voltage causing Al from one metallization path to traverse across the surface of the silicon, underneath the oxide, to a metal path of different potential, forming "white spears" (Reference 19). Bulk breakdown due to localized thermal avalanche, punch-through, and secondary breakdown are usually caused by excess temperature with bias applied. High frequency oscillations often occur during burn-in or circuit operation where degenerative feedback is not provided. Melted metallization, discolored or melted die, and vaporized bond wires are all signs of misapplication of bias and signal or improper heat sinking.

c. Opens - The failure mechanisms producing opens are displayed in Table 3. These mechanisms are frequently time dependent and often require long periods to produce failures. These mechanisms pose a considerable question to the long-life performance ability of transistors. Open transistors are generally less catastrophic to hardware failure than shorted ones because they do not load power supplies, but can still result in hardware failure due to loss of drive to succeeding stages. Redundancy is necessary where single point transistor opens can cause catastrophic hardware failure.

Interconnect Wire Failure Mechanisms - The most common cause of opens is interconnect wire failure. There are two types of metallization-interconnect wire systems used; gold wire to aluminum metallization and aluminum wire to aluminum metallizations. Each has its problem when not done properly and each historically has been a popular topic of disagreement.

Plague and Kirkendall Effect (Gold-Aluminum) - The most common interconnect system in transistors is the gold wire to aluminum metallization interconnect. Insufficient time, temperature, or pressure during the formation of the bond results in weak or incomplete bonds.

The more significant mechanism is commonly called "plague." Seemingly strong bonds grow weak with temperature and time due to intermetallic compound formation and the Kirkendall effect. Bond weakening is most severe in expanded contacts, but failures have been observed in both expanded and direct contacts.

Gold aluminum interconnects exhibit formation of five intermetallic compounds: AuAl, Au_2Al, $AuAl_2$, Au_5Al_2, and Au_4Al (References 21, 22, and 23). The growth of intermetallics is accelerated with temperature. All phases have been reported, but the most widely discussed seem to be the purple ($AuAl_2$) and the tan (Au_5Al_2, Au_2Al) phases. Purple plague has relatively good electrical and mechanical properties (Reference 22). In comparison to the tan phases its growth rate is slow, but the presence of Si in the Al film tends to increase its growth rate (Reference 21). The tan phases have relatively poor electrical and mechanical characteristics (Reference 22). Au_5Al_2 forms more easily and has fastest growth rate with Au_2Al the next fastest (Reference 21). The other two phases, AuAl (white) and Au_4Al (tan) have been observed, but grow slowly and appear to be intermediate phases for the other three.

The Kirkendall effect is the interdiffusion of two dissimilar metals at different rates producing voids at the interface. This phenomenon takes three forms; anular voids around the outer periphery of the ball, lateral voids along the entire surface of the ball, and depletion of the aluminum film. The first and last mechanisms are only a problem in expanded contacts; the second in all contacts. Depletion of the aluminum film can be attributed to the much greater bulk of gold in the ball requiring more Al atoms than the film can supply. Kirkendall voids seem to be most prevalent in parts having Au_5Al and Au_2Al phases of intermetallics. Since these gold rich intermetallics form at a faster rate than the others, require more gold than aluminum, and gold has a faster diffusion rate into Al than Al into gold, it is suggested that the voids are a product of formation of gold rich intermetallics. In addition, some parts have exhibited very stable bonds with time and reasonable temperature, suggesting some inhibitive effect on the formation of undesirable intermetallics. Since the formation of intermetallics is a function of the initial bonding parameters (time, pressure, temperature), perhaps proper combinations produce phases such as AuAl or $AuAl_2$ which retard the growth of the undesirable phases. Also, data is available which shows that oxygen retards the growth of intermetallics by reducing the amount of available aluminum through oxidation (Reference 8).

Failure Mechanisms	Description	Method of Detection	Method of Minimizing Defect
Open Interconnect Wire at the Die Note: (The most common intermittent open-normal-open failure is due to die-wire bond failures.)	Gold Aluminum: Intermetallic formations (plague) Kirkendall voids under ball. Excess pressure resulting in nicked wire exiting ball. Depletion or peeling of Al film around and under ball. Aluminum - Aluminum: Microcracking at heel of bond due to poor tooling and excess bonding pressure. Both: Insufficient time, temperature, pressure, or energy leading to incomplete bonds. Insufficient bond pad area on die.	100% bond pull (non-destructive to an acceptable threshold level) to detect weak or poorly formed bonds. Threshold for Gold-Al 2 grams min pull, Al-Al 0.7 grams min. Low duty cycle power cycling will aggravate microcracking in Al-Al wedge bonds. High temperature storage or cycling followed by mechanical shock will aggravate plague and void failures.	Use monometallic bonding system. Oxygen in gas backfill seems to retard growth. Visually inspect all bonds for improper ball dimensions and wire necking. Proper alloying (sintering) of Al film prevents peeling. Proper tool design and controlled bonding parameters. Control over bond parameters. Bond pad area must be greater than the final surface area of the bond (i.e., metallization visible around bond).
Open Interconnect Wire at the Post and Along the Wire	Insufficient weld area at the post. Burned or incomplete welds. Si inclusions in wire or greater than 1% content. (Al wire) Twists, nicks, crimps, kinks, scratches in wires reducing design diameter. Corrosion on or in the wire from drawing or cleaning operations which corrodes metallization or otherwise interferes with bonding.	Visual inspection of wires and bonds will detect gross defects. 100% bond pull (nondestructive to an acceptable threshold) will detect weak wires and bonds. Thermal shock will aggravate incomplete or improperly formed post bonds. High temperature storage followed by thermal cycling will anneal and break poor Al wire.	Use double bond at the post. Proper weld or bonding schedule. Close metallurgical surveillance of wire used, 1% Mg wire appears to be stronger. Workmanship Clean all wires before use.
Die Lifted from Header	Voids in eutectic die mount. Failure of ceramic insulation to support die under mechanical stress (for dielectrically insulated parts). Cracked die due to thermal mismatch of die and header (power devices).	Constant acceleration at high g levels will expose these failures.	Workmanship Mount ceramics directly to header. Do not support from leads. Use thick eutectics or intermediate materials to provide some stress relief.
Metallization	Photolithography defects (stained or dirty masks, lifted or underexposed photoresists, etc.) resulting in incomplete metallization. Improper annealing (sintering) resulting in peeling or lifting metallization. Scratches opening metal paths. Scratches reducing cross-sectional area of metal resulting in migration failures (expanded contact and interdigitated geometries). Insufficient design width and thickness resulting in excess current densities and burned metal or migration.	Electrical test will detect permanently open parts. Visual inspection of die will detect gross metal defects. Power burn-in at reasonably high current levels will accelerate migration failures. *Note: (Electromigration of Al is only a problem in devices with expanded contacts and is discussed more in the integrated circuit chapter.)	Clean masks, uniform photoresist deposition exposure and removal will help. Sintering temperature should be reasonably high. Glassification over metal to protect it. Glassification over metal to protect it. Maximum current densities should be 5×10^4 A/cm^2 to minimize migration effects.

Table 3 Opens and Intermittents

Microcracking and Annealing Failures (Aluminum-Aluminum) - The next most widely used bonding system in transistors is aluminum wire (with 1% silicon) and aluminum metallization. The two failure mechanisms in this system are wire breakage due to Si inclusion in the wire and microcracking at the heel of the bond due to necking of the bond by the bonding tool (References 24 and 25). Both failure mechanisms are time dependent and are a function of the thermal cycling (usually low rate) which causes mechanical movement and annealing of the wire (Reference 26).

Silicon inclusions in the wire usually results from poor manufacturing by the wire manufacturers. Annealing accelerates loss of strength due to recrystallization of the Si in localized centers along the wire (Reference 27).

Microcracking results from improper tool design and too much pressure. For ultrasonic applications, energy plays an important role in forming a sound bond while in thermal compression bonds temperature is the other variable. The effect of poor control of these parameters is a reduction of the wire diameter at the die bond as the wire exits the die.

Failure at the Post and Along the Wire - Both AuAl and AlAl interconnect systems are prone to failure if the post bond does not provide sufficient wire to post surface contact. In addition, nicks and kinks in the wire, reducing its designed diameter, could result in failure due to excessive current densities.

Interconnect Wire Failures-Detection Methods - In both AuAl and AlAl interconnect systems a 100% non-destructive wire pull is the best method for detecting improperly formed bonds, nicked, or degraded wires. Several manufacturers and users have indicated good success with such a test without degradation to sound parts. A 0.7 gram pull threshold is a sufficient pressure to break defective bonds without degradation to good bonds.

In gold-aluminum systems, several users have utilized high temperature (300°C, or better) aging of parts to detect weakening bonds due to intermetallic formation. Most, however, prefer to limit temperature exposure of gold-aluminum interconnections to 150°C to avoid inducing intermetallic growths. A low current forward voltage drop measurement is suggested pre- and post-burn-in, and temperature storage with tight delta shift criteria on voltage as a means of detecting weakening bonds due to intermetallic growths.

In aluminum-aluminum systems, large numbers of one minute on per one minute off power cycles has been used to fracture defective wedge bonds. This testing is impractical for screening programs, but could be used on a sample basis to discover a defective lot of parts. A 100% visual inspection of the bonds for severe wire necking and a sample SEM inspection of the bond heel for microcracking is advised in Al-Al bonding systems.

In both types, a 100% pre-cap visual of the die and post bonds and the wire to stringent visual criteria will remove most common interconnect defects.

Interconnect Wire Failure Minimization - The most promising development in eliminating these failures is the use of beam lead devices. This system affords a gold-gold interface thus eliminating intermetallic growth and eliminates the use of "flying" leads. However, more study into the unique frailties of beam lead devices is necessary. Also, the variety, availability, and production stability of such devices is not presently sufficient to command widespread usage.

Another alternative is the use of 1 mil gold wire thermocompression bonds to gold metallization on the die. The strength and stability of gold wire is achieved without the plague problems; however, few manufacturers have parts available with gold/gold interconnections. Where available, this system should be used.

The majority of suppliers use AuAl or AlAl interconnect schemes. Double post bonds are recommended for either system to provide good adhesion to the post. Gold ball thermocompression bonds and ultrasonic aluminum chisel bonds are the only acceptable means of bonding the wire to the die. Wire quality and material content, and metallization thickness and texture, must be controlled by the manufacturer for reliable bonding. Bond location and adequate pad size also are important controlling factors in reliable interconnects.

Some studies (Reference 27) have indicated that 1% Mg aluminum wire has significant advantages over 1% Si aluminum wire, but most users and manufacturers contacted recommended the latter.

Lifted Die Mechanisms - Excessive voids in the eutectic bond or undue mechanical stress can cause die to lift off the header. In parts with dielectrically isolated collectors or gates, ceramic insulators which do not have adequate mechanical support to the header can break die during mechanical stress and result in opens.

Lifted Die Detection Methods - Parts which have marginal die attachments can be detected usually through X-ray of the die header assembly, looking for voids. Power pulse V_{CE} (SAT) measurements will also detect such defects.

Lifted Die Minimization - Die and insulators should be firmly attached to header rather than suspended from the leads. Ceramic temperature coefficients should be matched closely to Si to preclude cracking due to thermal expansion.

Metallization Failure Mechanisms - Metallization opens are typically only a problem in expanded contacts since current is carried from the die to the wire bond by paths of metallization. Scratches due to improper die handling and missing metallization due to photolithography defects are commonly the source of open metallization paths. Migration of aluminum away from thinned areas to create voids is discussed in Chapter II. This is a problem in rf and power devices where metallization cross-sectional area and current requirements cause excessive current densities in the Al film. Improper alloying (sintering) of the Al film to the silicon and SiO_2 surfaces results in peeling and lifting of the metallization. This also can be a problem even in direct contact devices. Another mechanism is failure of the metallization to make contact with silicon due to an incomplete etch of the SiO_2 at the window, or growth of SiO_2 at the interface of the Si and Al. Molygold metallization system failures are sometimes caused by excessive undercutting of the moly during etching or inadequate alloying of the moly.

Metallization Failure Detection Methods - A pre-cap visual inspection will detect open or degraded metallization fingers in uncapped parts. Electrical testing will reveal those sealed parts having open metallization paths. Metal voiding due to migration can be discovered by a forward burn-in at rated current. Several integrated circuit users require sample SEM inspection of each wafer to determine adequate metal coverage over oxide cuts.

Metallization Failure Solutions - Use of phosphosilicate glasses retards metal migration (except gold metallization systems) and also protects the metal surfaces from scratches during die handling. High temperature storage will stimulate the growth of oxide at the contact window. The use of gold metallization significantly reduces metal migration effects because of the relative immobility of gold; however, while the gold is immobile, the moly underneath is not.

Derating maximum current limits to keep metallization current densities below 5×10^4 A/cm^2 will reduce electromigration effects considerably.

Excessive Voltage, Current, Power - Usually overpower conditions will melt interconnect wires or vaporize metallization films due to excessive current density. Shorts in the die also cause open interconnects under normal power conditions.

d. Mechanical Degradation - The last group of failure mechanisms is shown in Table 4 and deals with failures that prevent proper installation of the part. While these failures are normally discovered during and just after part installation they cause significant delay and occasionally go undetected until considerable investment is made in the using hardware. They are most easily detected prior to installation by an external visual inspection.

Degraded Leads and Packages - Corrosion of leads and cans results from a number of poor practices. Handling of parts without gloves or finger cottles and storage of parts in corrosive or oxidizing environments degrades leads preventing sound solder joints when the part is installed. Oxidized surfaces on the can where heat flow is required increases thermal impedance. Poor plating also contributes to solderability problems and reduces thermal conductivity. Improper material content and improper dimensions results in poor welds where contact resistance welding is used. Again, contamination can result in weakened joints. Scratched, bent, broken, and twisted leads make the part more difficult to install properly.

Studs - Galled or stripped threads, irregular or hollow surfaces on base of stud, and improper attachment of ceramic insulator (for dielectrically isolated devices) result in failures of stud mounted devices. The latter two usually cause a marked increase in thermal impedance of the device resulting in overheating and die failure. Damaged threads usually result in broken studs when proper torque is applied, or in insufficient torque due to added mechanical resistance.

Seals - Cracks and bubbles around the external leads result in loss of hermeticity. The effects of contaminated ambient have been discussed previously.

Part Marking - Soluble inks, smeared or smudged marking, or absence of marking afford loss of traceability of screened, qualified parts. It is essential that a part be uniquely marked to indicate that it was screened to preclude installation of an unqualified, unscreened part. Use of insoluble inks is mandatory. All part marking is to be stamped on the can. No tags on leads or cans which may outgas in the using hardware or otherwise degrade part are to be used. An external visual of all parts will eliminate parts with such external defects.

Failure Mechanism	Description	Method of Detection	Method of Minimizing Cause
Unsolderable or Unweldable Leads	Finger greases or acids on leads.	External visual inspection. Dimensional inspection. Solderability/Weldability tests.	Use of tweezers or finger cottles when handling part.
	Exposure of leads to corrosive solvents.		Control of cleaning processes and storage of parts.
	Exposure of part to O_2 and H_2O in high temperature environments.		Use of dry N_2 environments during high temperature storage.
	Poor plating.		Q. C. inspection by part manufacturer of plating integrity.
	Improper metal content.		Q. C. inspection by part manufacturer of lead metals.
	Improper dimensions.		Q. C. inspection by part manufacturer.
	Bent, broken, nicked, scratched, twisted leads due to poor handling or test equipment.		Q. C. inspection by part manufacturer.
Degraded Seals	Cracked glass due to mishandling.	External visual inspection. Hermetic seal tests fine and gross with maximum leak rate of 5 X 10^{-8} Atm/cc/sec.	Inspection of headers 100% upon receipt by part manufacturer.
	Bubbles or voids in glass.		Inspection of headers 100% upon receipt by part manufacturer.
	Improper can to header seal ring dimensions.		Inspection of headers 100% upon receipt by part manufacturer.
	Contaminated can to header seal ring.		Inspection of headers 100% upon receipt and proper cleaning.
	Improper can to header weld schedule.		Regular certification of weld schedules and welders by part manufacturer.
Degraded Part Package	Exposure to corrosive solvents or gases.	External visual inspection. Dimensional inspection.	Store and test parts in dry inert environment.
	Finger acids and greases.		Handle parts with tweezers or finger cottles.
	Improper dimensions and material content.		Q.C. inspection of headers and cans by manufacturer.
	Deformation of part can or header due to excessive mechanical stress.		Control of mechanical shock and acceleration fixtures and handling and packaging.
	Galled or stripped threads and broken studs for stud mounted packages.	External visual inspection. Thermal impedance measurement case to heatsink on installed parts.	Use of properly derated stud torque values by part user. Burn-in power parts in free air using free air ratings to achieve max T.
	Poor finish and flatness on bottom of stud surface precluding proper thermal interface.		Q.C. inspection of headers by part manufacturer and lot test of thermal impedance case to heat sink.
	Improper insulator resulting in poor mechanical support or high thermal impedance for collector or gate insulated devices.	Thermal Shock/High Impact Shock with electrical measurements prior to and post shock thermal impedance measurement junction to case.	Use ceramic insulators which are solid (unperforated or slotted) that are eutecticly mounted to part header rather than supported by lead parts.
Mismarked or Unmarked	Wrong part numbers placed on part.	External visual inspection marking,	Workmanship
	Part marking inks/paints soluble in part cleaning solutions.	marking permanency test.	Use of indelible inks/paints.
	Unintelligible marking (smears, blobs).		Workmanship
	Tags applied to leads.		No tags applied to leads. Stamp all part ID.

Table 4 Mechanical Defects

2. Design

a. Selection Criteria - Use of a transistor for long-life applications is dependent upon three factors: 1) Suitability of the part's electrical and mechanical characteristics for the intended applications, 2) Part design and construction meets environmental and life requirements, and 3) fabrication, screening and qualification of the production parts can be accomplished within the program reliability cost and schedule constraints.

It is desirable that the application of a part be tailored to the established part characteristics rather than the part to the application. In addition, to minimize effort, parts with the optimum operating characteristics out of a product family are desired as preferred parts (provided the yield of parts for such optimized characteristics is reasonable). The preferred parts should be used in the majority of designs.

Table 5 shows the part design factors desired for long-life operation. These design factors are well within the capability of the industry as most of the processes involved are currently in use by semiconductor industry. The preferred designs or processes indicated are specifically directed toward solutions to problems commonly encountered in transistors specifically oriented to life limiting problems. Beam lead constructions are currently in production and used on a limited scale and show real promise in solving many part reliability problems.

Finally, parts used in hardware intended for long-life must be screened on a 100% basis to remove improperly assembled parts, those with limited life, and to stabilize their electrical characteristics through power aging. The construction of the part and the related testing of those parts must be accomplished within the time limits of the program using the parts. The manufacturer selected to supply production parts should have a stable facility and labor situation, the design of the part fixed and a reasonably continuous production of that part. It is desired that the manufacturers used have a sufficient volume capacity to meet quantity requirements in as few lots as possible. In addition, the products of the larger volume suppliers tend to be more homogeneous. The specifications used to acquire screened and qualified parts must be negotiable by both the buyer and the part manufacturer.

b. Results of Survey - A total of twelve separate using agencies, NASA and private industry, were contacted regarding the use and test of transistors. Ten semiconductor manufacturer contacts were made in the power small signal and FET product categories regarding failure mechanisms and practical test methodology.

All part users indicated significant failure histories utilizing TX type screening and all indicated that effort beyond TX activities was required for their existing programs to obtain good parts. Table 6 shows the more unique approaches or tests used by the agencies and companies surveyed.

All manufacturers showed concern for part failures only when the numbers would significantly affect yields. All considered die fabrication and processing proprietary, but indicated the largest yield losses were rejected die during electrical check of the wafer. Most indicated that their process controls in the die fabrication area were sufficient to obtain good yields. Several indicated interest in beam lead manufacture and a few indicated actual production. Most indicated a need for market demand before committment to such a new product development. One or two suppliers indicated the availability of a "control line" concept where part users could impose in-process controls on assembly and inspection of their parts during the time of fabrication. This differs from a "captive line" approach where the user's parts are the only parts fabricated on that line for an extended period of time. A "control line" situation appears to be considerably cheaper than a "captive line" approach, but allows the user the same privileges. Such a situation would readily allow the 100% source inspection of parts built for a particular user and control of critical assembly and inspection processes which are the major sources of transistor failures.

c. Alternate Approaches - Table 7 shows the alternate approaches in the use, design, fabrication and test of transistors. Where possible, integrated circuits should be used where their dynamic characteristics and power dissipation limitations are not a problem. The use of I.C.'s greatly reduces the number of circuit connections required and affords lower weight, power consumption, and temperature contribution to the total system.

Table 5 Selection Criteria

Design Factor	Remarks
DIE	
Starting Material	Silicon should be used. Germanium has severe leakage limitations with temperature
Construction	Planar process should be used. Mesa alloy and grown junction process present limitations to performance or life not encountered in planar devices. (1)
Metallization Aluminum most common Gold-Moly/Tungsten preferred	Thickness minimum of 10,000 Å to reduce electromigration effects in interdigitated geometries (current densities should be 5 X 10^4A/cm^2 max). Large uniform grain structures are desired to reduce electromigration effects in interdigitated geometries. Wire bond surfaces should be 1.0 x the final bond area to provide adequate bond. Widths should be adequate to keep current densities below 5 x 10^4A/cm^2. Separations should be adequate to prevent corona discharge in high voltage devices.
Passivation	Thermally grown oxides most preferred and the higher the temperature during growing, the better the oxide. Glassified die (over metallization) preferred Glass immobilizes or shields out particle contamination and protects metallization from scratching and smearing. Surface passivation also reduces effects of channel forming contaminants. Paints and varnishes undesirable.
HEADER	
Posts	Height should be sufficient to prevent down - bending but not high enough to short to cap.
Insulators	In power devices, the dielectric insulator should be properly supported mechanically and provide adequate thermal interface to provide low θ_{jc}.
Weld Splatter Shields	TO-18, TO-5 type headers should be plateau type to keep weld slag and splatter off the die. Power devices should have headers which keep weld slag and splatter from reaching die.
ASSEMBLY	
Die Attachment	Eutectic bond only. Epoxy or glass frit bonds are unacceptable for long term part service.
Interconnect	Mono-metallic interconnect systems preferred. Au-Au most desirable but few vendors have this ability (also, further work required in area of process technology). Al-Al next but bonding tool, energy, pressure and duration must be controlled closely to prevent μ-cracking at die bond heel. Au-Al systems are predominant and are acceptable when temperature, pressure and duration are proper to preclude formation of undesirable intermetallics. Some manufacturers can perform a 100% non-destructive bond pull test. (2) Most manufacturers do periodic destruct bond pull on sample basis for each station/operator. Wire diameters should provide sufficient current capability margin to prevent opens. One mil dia. wire minimum.
Encapsulation	Hermetic seals only, with stiff controls over backfill to eliminate H_2O, H_2 etc. Plastic unacceptable. Beam lead and Silicon Nitride a possibility, but more work required to prove hermeticity and stability with time and temperature. Leak rates of 5 x 10^{-8} Atm/cc/sec max on hermetic seals.
PACKAGE	
Materials	Package and lead materials should be nickel or gold plated Kovar to minimize lead or case corrosion due to handling or other external environments.
Configuration	Should provide adequate mechanical integrity for handling during installation and during part tests. These are the most severe environments the part will encounter. Flight and hardware qual environments are benign compared to treatment during shipping and installation.
Studs	Stud torque strength should be adequate to provide proper interface with mounting surface. Finishes and flatness should be adequate to prevent voids increasing thermal impedance case to heat sink. T. C. mismatches between die and header should be anticipated and compensated for by thicker eutectics or T.C. matching phase such as ceramic insulators.
PART DESIGN MATURITY	Part is actively produced by more than one manufacturer and has had acceptable past usage history. Part obsolescence must not be imminent to avoid procurement problems. Production of parts must be stable and reasonably continuous to avoid startup/shutdown problems with production. Larger volume manufacturers while somewhat less cooperative, provide more stability than small houses.

(1) Mesa construction required for high voltage devices.

(2) Based upon the fact that Al has a low activation energy and Ag has a relative high activation energy. Vendors prefer to use single Al metallization because of the relatively simple processes. Gold is more expensive and the processes tedious. Although not so readily available, gold should be more reliable.

Table 6 Survey of Electronic Part Users

USER	UNIQUE TEST OR SPECIFICATION REQUIREMENTS	RATIONALE/JUSTIFICATION
JPL	100% serialization of parts and read and record all screening parameters.	Traceability of individual parts to screening data.
	1000 HTRB for FET's for burn-in.	Had some in-service failures at 720 hours due to surface contaminants.
	100% precap visual per MSFC 85M03924.	Remove cosmetic defects prior to capping.
MSFC	100% precap visual per MSFC 85M03924 and 100% source inspection.	Remove cosmetic defects prior to capping.
	240 hours of burn-in.	168 hours inadequate.
	96 HTRB on all types.	Surface effects present in NPN as well as PNP's
	Pulse power burn-in on power devices.	More effective than dc burn-in.
	Serialize parts and read and record screening parameters.	Traceability of individual parts to screening data.
	Power cycle 1 mil Al wires for qualification continuously on small samples to discover weak bending systems.	Had history of 1 mil Al wire failures for low duty cycle switching operation.
Sandia/Bendix	Radiation hardening and screening.	Applications radiation sensitive.
	Sample SEM inspection of installation and oxides.	Looking for defective metal to window interfaces and oxide defects.

Table 6 (cont)

USER	UNIQUE TEST OR SPECIFICATION REQUIREMENTS	RATIONALE/JUSTIFICATION
Sandia/Bendix (cont)	Sample wire pull to destruct, post burn-in on each lot, and 100% non-destruct pull of .8 grams.	Looking for degraded interconnects. Good interconnects survive 100% pull. Bad interconnects fail.
	Burn-in and HTRB done to achieve 300°C T_j.	Stimulates failures not detectable by T_j = 200°C.
	100% pull of collector external lead on all hot case-collector configurations.	Have had a problem with collector lead welds pulling free of case.
	Sample die push.	Looking for poor die attach.
	Do step to destruct environmental tests during qual.	Determine part's maximum environmental limitations.
	Parts fabricated on control line where all key assembly processes and materials are controlled and specified by procuring agency.	Affords parts built in a controlled manner beyond normal yield sensitive controls implemented by part manufacturer.
	Conformal coating over die and post wire attachment.	Radiation hardening and passivation to protect die from particles.
TRW Systems	Sample fingerprint of each lot procured.	Check construction and design consistency with qualification baseline.
Lockheed Missiles	Power transistors do 100% PIND testing (acoustically monitored vibration testing).	Internal particle detection.

Table 6 (concl)

USER	UNIQUE TEST OR SPECIFICATION REQUIREMENTS	RATIONALE/JUSTIFICATION
Lockheed Space	100% source inspection.	Check vendor Q.C. control and part assembly.
	Sample fingerprint of each lot.	Check construction and design consistency with qualification baseline.
	All small signal devices have glassification over metallization.	Protects metal from conductive particles and scratching.
Martin Marietta Corp./Denver	300 hours of burn-in minimum plus 48 hours HTRB.	168 hours inadequate HTRB required to discover channeling and surface phenomenon.
	100% source inspection.	Check vendor Q.C. and assembly controls.
	100% precap visual per MSFC 85M03923-Viking.	Remove cosmetic defects.
Martin Marietta Corp./Orlando	Parts fabricated on control line	Affords parts built with more stringent controls than normal yield-sensitive controls used by manufacturer.
	Using gold/aluminum interconnect	Testing shows a more dependable interconnect than Al/Al
BTL	300°C temperature soak 16 to 24 hours.	
	16 to 24 hours of forward bias at T_J of 300°C.	
	Sample test at 100 hours at T_J 300°C forward bias.	
	Thermal cycle.	
	Centrifuge	
	Selection of most stable parts.	Empirical data from past experience indicates this is an effective screen method.
	Use all Au wherever possible.	

Table 7 Alternate Approaches

APPROACH	ADVANTAGE	DISADVANTAGE
Use Integrated Circuits	Reduced number of interconnect joints for same circuit function. All circuit elements in one die. Lower power dissipation, operating temperature, and component weight.	Failure analysis of circuit more difficult.
Use Gold Metallization / Gold interconnect wire bond system.	Strength of gold thermal compression bonds and gold wire obtained without intermetallic compound formation. Gold metallization less prone to electromigration.	More expensive. Few suppliers have capability. Intermediate stages required at contact window to preclude gold migration into silicon. Molybdnum, platinum commonly used.
Phosphosilicate glass protection of metallization in interdigitated geometrics.	Protects metallization from scratches. Shields out and immobilizes particulate contamination. Getters alkali ions. Seals imperfect oxides.	Additional process steps required. May have an adverse affect on yield if process is not controlled.
Beam Lead	Die is essentially hermetic. Gold beams can be bonded to gold pads eliminating interconnect wires. Die supported by gold beams eliminating eutectic die mounts and related voiding problems.	Processes and controls more involved. Failure mechanisms not yet completely understood. Only a few suppliers actively produce beam lead devices. Power handling capability of same size die reduced because of reduction in thermal coupling to case.
Multichip devices packaged in I.C. flat packs	Better volumetric efficiency. Available from several manufacturers.	Testing more difficult. Power dissipation of each die slightly reduced.
Parameter Drift Screening	Provides visibility into part stability with time. Unstable parts can be eliminated. Parts with short predicted life can be eliminated.	Very expensive.

The use of gold molybdenum metallization with 1 mil gold wire thermal compression bonds is suggested for all transistors currently using 1 mil interconnect wires. The advantages are elimination of potential intermetallic formation and Kirkendall voiding where gold wires are connected to Al metallization, annealing and wire fatigue where aluminum wires are used, and in expanded contacts reduction in electromigration effects due to the increased density requirement to move gold atoms. Most power transistors currently use 3-5 mil Al interconnects to 10,000 Å to 50,000 Å metallization films. These are historically very stable systems and should not be changed.

The use of phosphosilicate glasses over metallization is recommended for interdigited geometries which have expanded contacts. The advantages are protection of the metallization from scratches, smears and particulate contamination; gettering of alkali ions in and on oxides; sealing of discontinuities in thermal oxides; and reduction of the effects of electromigration in the aluminum films. This technique would not significantly improve parts with direct contacts since the Al metallization is usually totally involved in the bond.

One of the promising developments in the semiconductor area is the beam lead package. Gold beams are connected to the contact windows and the die cover is silicon nitride (SiN_3) passivation. The die is attached to the external pins face down to bonding pads (Reference 28). Testing performed on this construction indicates that SiN_3 encapsulation is virtually hermetic and offers several advantages in part assembly over standard techniques. The gold beams effectively eliminate metallization on most small signal transistors and the SiN_3 acts as a getter to alkali contaminants usually present in standard diffusion techniques. More testing needs to be done to understand the potential failure mechanisms and risks involved in using this technology. The power dissipation and frequency limitations of these devices as compared to standard techniques also needs to be investigated. The industry also needs to stabilize processing and production to provide a consistent product and provide a wider variety of products.

In the area of packaging, better volumetric efficiency can be achieved by packaging multiple die in standard I.C. packages. Power dissipation for each die is reduced, but in many applications where the use of the same device is repeated in a circuit and power levels are reasonable, this packaging approach is much more efficient than individual die in one package. Several part manufacturers offer multiple die in one package as a standard product.

In the area of screening, a method of screening which is effective in detecting electrically unstable parts is parameter drift screening. This technique involves monitoring key electrical parameters for each part and plotting their variation with time. A figure of merit for each parameter is determined based on a prediction of when that parameter will fail to meet specified limits. Parts with high figure of merit are selected for use in flight hardware. Parts with unpredictable characteristics are rejected.

d. Hardware Life - There are no verified wear out mechanisms for transistors. However, there are some known failure mechanisms which are governed by time/temperature dependent chemical and physical processes which could be classified wear out mechanisms even under normal part operating conditions.

Three examples are: Accumulation of ionic contamination in bulk dislocations affecting leakage and gain, intermetallic compound formation in bimetallic bonding systems leading to weak or open interconnects, and metallization migration in expanded contact devices leading to open metal paths on the die. These three have been discussed in the previous section dealing with failure mechanisms.

The first seems to be unavoidable at the present state of semiconductor processing. The other two can be eliminated with the use of a gold-interconnect system. The transistor industry, in general, uses aluminum metallization to make contact between the interconnect wire and the silicon and few are manufacturing die with gold metallization.

e. Application Guidelines - Five things should be considered in the proper application of a transistor: 1) parameter requirements (i.e. the parameters that are specified or agreed to by the manufacturer are realistic and are adequate to meet the needs of the application); 2) maximum voltage and current ratings are not exceeded; 3) Junction temperature is kept below an acceptable maximum; 4) time/temperature dependent parameters are properly derated to account for their drift; and 5) the part is installed in a manner which will preclude damage due to undue mechanical stress.

Suitability of the part's parameters for the application is very important to obtain reliable hardware performance. All pertinent part characteristics must meet the needs of the circuit design. However, it is undesirable to tailor part characteristics beyond their normal limits to optimize circuit performance. To do so usually requires process changes by the part manufacturer which quite frequently produces poor yields and a less reliable part.

Secondly an assessment of the accuracy of the manufacturer's specification of part parameters should be made, by test, to prevent delays in delivery of parts and design changes (e.g. a common tendency by some part manufacturers is to be optimistic about switching speed capabilities for sales purposes).

Derating of part characteristics takes two forms: 1) safety factors to prevent part damage or premature failure, and 2) drift margin to compensate for natural parameter fluctuations with time and temperature. Part parameters which come under the first derating classification are the minimum or maximum current, voltage, power, and junction temperature conditions under which the part can be reliably operated. The second category deals with those parameters which influence circuit operation such as gain, leakage, current, switching characteristics, forward voltage drop, noise figure, etc.

Derating electrical and thermal limits is an advised practice to protect devices from damage and shortened life. Reverse breakdown voltages $\left(BV_{CBO}, BV_{EBO}, BV_{CES}, \text{etc}\right)$ should be derated when uncertainty exists in the exact maximum voltage levels possible at the part terminals under all operating conditions or when the actual breakdown voltage of each part installed in the hardware is known only to be above a certain specified minimum value. The values selected in the past seem to be arbitrary but appear to be reasonable and effective. Foreward breakdown $\left(BV_{CEO}, BV_{CES}, \text{etc}\right)$ should be limited by a safe operating area (SOA) curve (Acceptable Collector Current plotted versus Acceptable Collector-Emitter voltage at fixed junction temperature).

This curve should be plotted for any bipolar transistor used and the collector current and voltage applied must be below the safe limits to preclude secondary breakdown and thermal runaway. The manufacturer's rated BV_{CEO} displayed on the SOA curve should be derated if uncertainty exists in maximum applied voltage (steady state and peak) or if exact values of breakdown for each part are not known. For power transistors the secondary breakdown voltage threshold is fixed and the transistor can be protected by derating collector current at the secondary breakdown point.

Derating current, when not already influenced by the power limitations of the part, usually is done to reduce current densities in metallization films and interconnect wires and current crowding in the junction. Again, the values used in the past appear to be arbitrary but can be derived from acceptable current densities in junctions and interconnects. Such knowledge is not normally available from part manufacturers and must be obtained by actual test or analysis of part design and construction.

Power and junction temperature derating are interdependent. The junction temperature of a transistor is given by the formula $T_j = T_x + P\theta_x$ where T_j is junction temperature, P is power dissipation, T_x is either case temperature $\left(T_c\right)$ or ambient temperature $\left(T_A\right)$ and θ_x is the thermal impedance either junction to case $\left(\theta_{jc}\right)$ or junction to ambient $\left(\theta_{jA}\right)$. Thermal impedance is a constant for each transistor type and is dependent upon part construction. The desired method of controlling power dissipated is to limit the maximum junction temperature to an acceptable value, then compute allowable power by the above formula. The acceptable limit on junction temperature is fundamentally based on the activation energy for the failure mechanisms of the part and their related reaction rates. Accelerated life testing has yielded such information (Reference 29).

Variations of leakage and gain with temperature are governed by a few simple rules. Bipolar gain changes about 0.7% per °C change, increasing or decreasing with temperature over most collector current ranges. There is a point where gain has a negative temperature coefficient (TC) and it is different for each part. This point of change of TC of gain, commonly called crossover point, should be determined for each type during part evaluation. If upper bounds are not specified for gain or gain bandwidth allow adequate margin to prevent overdriving. Derating used in the past for aging seems to be arbitrary but should be provided based on data obtained in qualification. Field effect transadmittance $\left(Y_{fs}\right)$ varies about 0.4%/°C with temperature, decreasing with increasing temperature and increasing with decreasing temperature. Aging effects should be derated based on qualification data.

Leakage currents typically double for every 10°C rise in temperature but this again varies from part to part depending upon surface and bulk variations. Doubling the specified values for aging is an acceptable way of compensating for leakage increases with life.

Derating switching time is usually a practice to account for the optimism of the part manufacturers and provide adequate timing margins. Other part characteristics should be derated where life testing indicates a time dependence.

The last part application consideration is mounting and mechanical protection. In general, most part test levels far exceed the application requirements, but natural vibration modes, and stress amplification factors must be considered to preclude damaged parts. This is especially important in large mass power devices. Stud torque should be kept below the maximum value specified by the manufacturer, but at a level sufficient to provide good thermal contact. Solder temperatures during hookup should be carried away from the die when possible. Adequate thermal transfer is essential for all devices which are operating near rated junction temperature. Thermal analysis for all parts is as important as electrical analysis for reliable part operation.

Table 8 shows the current and past derating policies used by several part users. Data was obtained via survey and review of program documentation.

Table 8 Derating Practices

Company / Parameter	TIII	MMC Skylab	MMC Viking	Hughes	TRW	Grumman	Philco	JPL	NASA Ames	NASA MSFC	NASA GSFC	NASA MSC	Recommended
Breakdown Voltage	80	75	70	70	75	75	25	75	75	75	75	75	75
Collector Current	80	75	75	-	-	75	25	50 [1]	-	75	-	75	75
Junction Temperature	-	-	130°C	-	-	100°C	-	110°C	-	110°C	110°C	100°C	110°C
Power Dissipation	50	50	[2]	35	65	30	25	50	50	50	20	[2]	[2]
Leakage Current	200	200	200	-	-	200	-	-	-	-	-	-	200
Gain Bipolar	90	90	85	-	75	70	-	-	-	-	-	-	75
FET	85	85	85										
Secondary Breakdown Voltage	-	-	[3]										[3]

[1] .3A max for 1 mil Al wires

[2] Limited by max T_J and θ_j

[3] Derate I_c to 75% at Secondary Breakdown point

NOTE: All figures are percent of rated value unless otherwise noted.

D. TEST METHODOLOGY AND REQUIREMENTS

1. Qualification

Qualification of transistors is usually done to determine the ability of a part type to meet the intended stresses of the application and the life requirements of the hardware to verify the manufacturer's ability to build a sound part and to verify that screening tests can detect weak parts without degrading sound parts. There are several types of qualification; one time part and supplier qualification, lot qualification where a sample of each order of parts is qualified, periodic qualification where at regular intervals samples of each type produced within a specified period of time are put together in a lot and tested, qualification by analysis of part design and construction, and a review of past part performance and the processes used to fabricate it. Most qualification of parts and suppliers for hi-rel programs is a combination of these and usually involves direct test and use of data obtained by other using programs.

One time qualification is usually performed as a source selection and evaluation technique, where analysis of past performance and part design and construction is done to narrow the field of suppliers. Lot qualification is normally performed where quantities and frequency of buy are limited. Periodic qualification is common where quantities are large and procurement is made frequently.

Qualification tests historically have been limited to testing the life and durability of a part to specified limits, to an acceptable confidence level and tests are usually performed in parallel to save time. A better approach would be to understand the actual limitations of the part and, since many failure mechanisms are dependent upon a sequence of events, testing should be performed in a serial/parallel manner to discover such mechanisms. In addition, only those electrical limits specified by the manufacturer are tested, when a better knowledge of the parametric variations with temperature, current, voltage, and frequency is desired or even necessary for proper part application. Figure 2 shows a proposed qualification program to be performed prior to procurement of production parts as the means of selecting qualified part types and manufacturers, obtaining valuable application information about the parts to be used, and determining the effectiveness of the screening tests.

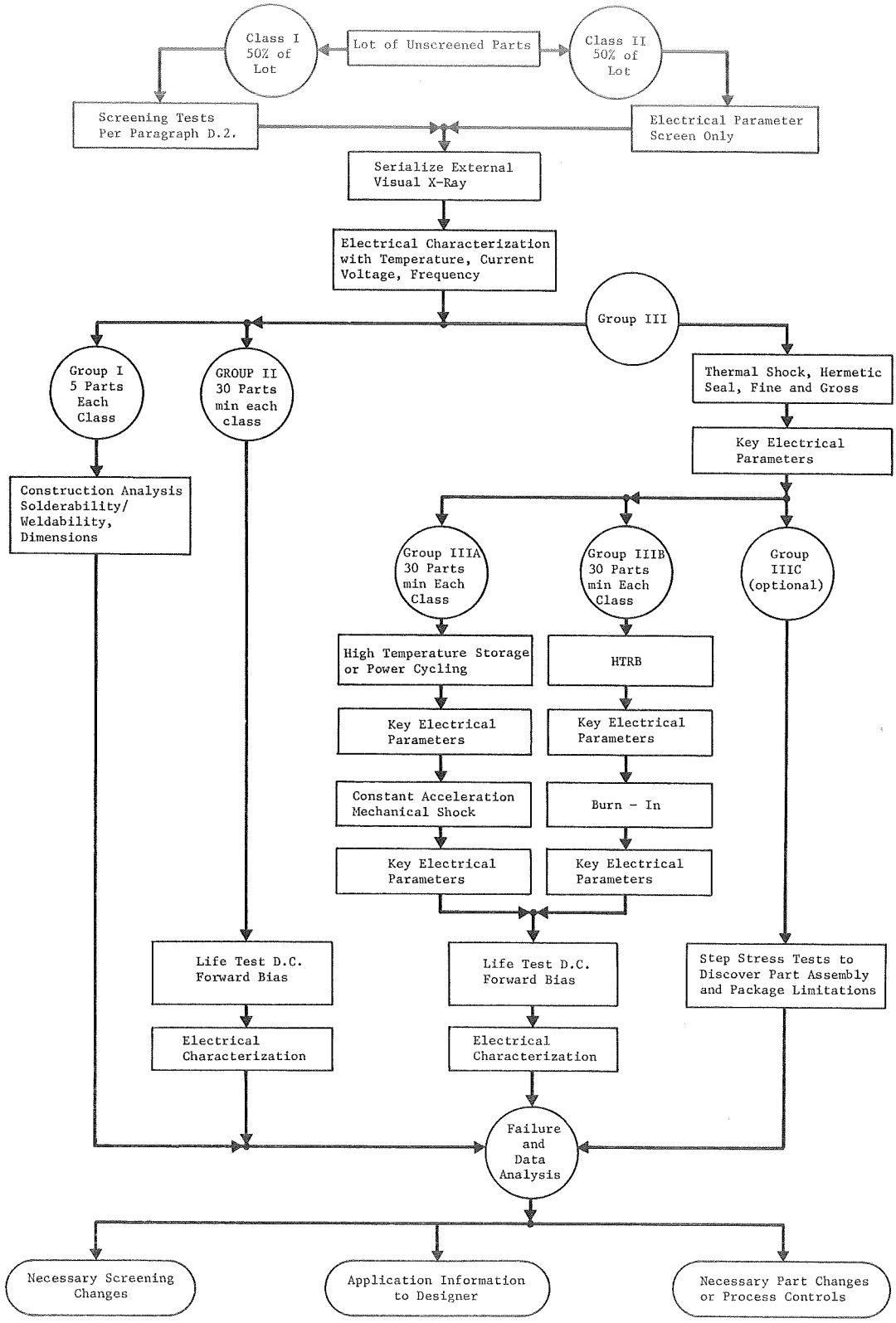

Figure 2 Transistor Qualification

The first feature of this program is the simultaneous testing of screened and unscreened parts. This is done to determine the effectiveness of the screening tests without degrading good parts and the inherent quality and soundness of the part. The second feature of this program is the combination of serial and parallel testing to discover time dependent failure mechanisms and the effects of the serial screen tests. The purposes and advantages of each leg of testing are discussed in succeeding paragraphs. A third feature of this program is characterization of the parts electrically to identify time, temperature, bias and frequency sensitivities of part characteristics for use during hardware design.

The parts procured for the qualification should be bought to the requirements of a screening specification as described in the paragraph D.2. Quantities should be sufficient to allow for replacements of rejects in the first phases of the program, particularly the unscreened parts. (Note: Here the term unscreened implies no *conditioning*. These parts should come from the same line as the screened parts and should meet the same electrical performance specifications as screened parts.) An evaluation must be made of the sources of parts prior to commitment to the qualification program. If past history and experience indicates a poor part or source, they should not be considered. A reasonable confidence must exist that the manufacturer's part will meet the requirements of the testing.

Parts are serialized with unique numbers to identify screened and unscreened parts and to provide traceability throughout the test sequence. Parts are externally inspected to remove parts which have damaged seals or leads. The parts are subjected to x-ray to remove parts with gross internal assembly defects. Substitutes should replace rejected parts to keep the sample size the same.

Next, a complete electrical characterization should be done to establish an electrical baseline for the part. Characteristics should be recorded over temperature, voltage, current and frequency ranges at the normally specified limits and at unspecified limits over a wider dynamic range. This data coupled with similar data recorded at the end of the test program is then used to identify basic time, temperature, and bias dependence of electrical characteristics for use during hardware design. In addition, a better knowledge of the part sensitivities can be obtained and areas where the part ceases to perform can be identified. This knowledge is valuable in selecting the best part for the design.

The extent of characterization of the part is greatly dependent on the scope of the design analysis and the breadth of application of a particular type in the total system. More detailed circuit analyses require more information about characteristics. More information is also required for a general purpose widely used part than one applied in only one specific application. The possible applications of the part should be assessed and coupled with the influence of the circuit analysis requirements to determine the extent of parametric characterization for the part during qualification.

Up to, and including characterization tests, parts not meeting the normally specified limits are removed and replaced. From this point, any part not meeting the specified limits are removed from the test and analyzed for cause of failure. Any failed or damaged parts in Group II, IIIA, IIIB or IIIC testing are not replaced.

Group I construction analysis involves the elements listed in Table 9. Only a few parts are necessary for this test (five or less).

The purpose of such analysis is threefold: 1) To aid in assessing the validity of the qualification tests, 2) discover any gross design or processing defects in the part, and 3) establish a fingerprint for comparison to future part procurement. It is necessary to complete at least the internal part critique phase of this testing before commencing the other test groups. If there are any gross part design defects which could eliminate a supplier, he should be removed from the qualification program before other testing begins, to reduce the risk of spending time and money on an unqualifiable part. The results of the Group I testing should be compared to similar testing done on samples of the production parts for all future procurement to identify process changes and any situations which could invalidate the original qualification (e.g., a change in die geometry).

Group II testing involves a dc forward bias life test, operating at a junction temperature of at least 200°C for a minimum of 1000 hours. A sample of 30 parts or more from each class should be subjected to Group II testing. It is desired to achieve the desired junction temperature through dissipation of power in the die rather than elevation of the ambient temperature, since several part failure mechanisms are accelerated by current and voltage along with temperature. Periodic measurements are recommended (every 250 hours of operation) to detect parts which are degraded by a test of key electrical parameters. Parts not meeting the specified values, or which have significant increases in leakage or saturation voltage, or decreases in breakdown or gain, should be removed for failure analysis. All test data should be recorded so that it can be used with initial and final characterization data to establish basic parameter life trends.

Table 9 Qualification - Group I Tests

External Package Description . Materials . Dimensions . Part Markings
Internal Part Critique . Gas Analysis of Backfill . Die Dimensions and Design . Type of Die and Wire Attachments . Type of Metallization . SEM Inspection of Metallization and Wire Bonds . Any Anomalies or Other Salient Features
Bond Wire Pull to Destruction
Cross-Section of Die, Measuring and Observing . Diffusion Depths . Oxide Thicknesses . Metallization Thicknesses . Die Thickness . Die Attachment Area (Voids, etc.) . Wire Bond Area (Voids) . Header and Wire Plating
Measure Thermal Impedance Junction to Case
Solderability/Weldability Tests

The purpose of the Group II test is to assess the influence of the Group IIIA and IIIB pre-life tests which are used for screening production parts, and to evaluate the normal variations of part parameters with life. The IIIA and IIIB test levels may be higher than the screening levels to accelerate particular failure/mechanisms, but are intended to degrade defective parts without significantly affecting good parts.

Group IIIA and IIIB testing is intended to expose time dependent failure mechanisms. The thermal shock test (10 cycles from -55°C to+150°C, 10-minute soak at each temperature, 30 seconds maximum transfer time) will aggravate poor seals, die attachments, post and die wire bonds and die cracks. Air to air is recommended over liquid to liquid.

The hermetic seal tests are both fine and gross leak with a reject level of 5×10^{-8} Atm/cc/sec. The test of key electrical parameters can be a go/no-go test to detect degradation.

Group IIIA testing is intended to expose die attachment and interconnect wire defects. High temperature storage, 200°C minimum for 100 hours, should be performed on parts with gold interconnect wires or aluminum wires greater than 1 mil to accelerate intermetallic formation and Kirkendall void formation. Shorter exposure can be used at higher temperature, but care must be taken not to induce failures in normally good bonds. A measurement of low current, forward voltage drop of each junction should be made after the temperature soak and compared to the initial readings. This test should be followed by a high impact shock, 30,000g's minimum, on top of can, 5 blows, 0.1m sec minimum duration for all TO-18, TO-5, TO-72, etc., cans (pneufactor) or 1500g's minimum in a direction to lift wire bonds and die, 5 blows, 0.5msec minimum duration for stud mounted devices. The measurement of forward voltage drop should be repeated. Finally, a constant acceleration of 30,000g's minimum in a direction to left weak bonds and die attachment should be performed followed again by a low current forward voltage drop measurement. Any part exhibiting greater than a 10% increase in forward drop should be removed for failure analysis.

The test sequence is the same for parts with 1 mil aluminum interconnect wires, except that the high temperature storage step is replaced with a power cycling test. The part is cycled at least 100% of rated power dissipation for a minimum of 20,000 cycles where one cycle is: power on for one minute, then off for one minute. This test is intended to precipitate wire failures due to nicking and microcracking at the wire bond heel.

Group IIIB testing is aimed at discovering bulk, surface, and contamination related failure mechanisms. The first step is High Temperature Reverse Bias (HTRB) performed to stimulate formations of channels and inversion layers due to surface contaminates. Temperature should be at least 175°C bias on collector-base for bipolars, or gate-source and gate-drain for FET's, with a minimum of 80% of rated breakdown voltage. The minimum time should be 96 hours, followed by a measurement of leakage currents. If leakage current values are greater than specified values, or if the initial value has doubled, the part should be subjected to failure analysis. (Note: If the initial value of leakage current was orders of magnitude below the specified value and is still within specified limits after HTRB, rejection should be based on the magnitude of the increase and not the term "doubled.") Since contaminants tend to disperse from their localization zones after bias is removed, leakage measurements should be made as soon as possible after bias removal. In addition, bias should remain on parts until they are cooled to room temperature, since higher temperatures produce faster dispersion of contaminants.

The next step is a forward biased burn-in. Ac burn-in simulates actual part use and accelerates many failure mechanisms encountered during normal part operation (Reference 30). Most part suppliers contacted, while they agreed with the concept, indicated a lack of facilities to perform ac burn-in. They also indicated that dc burn-in is perhaps a more severe test since it tends to polarize surface contaminants while ac would not.

In either case, parts should be burned in for a minimum of 300 hours at rated junction temperature. This test should be followed by an electrical measurement of gain, leakage currents, and saturation and breakdown voltages. Parts with parameters beyond specified limits should be removed for failure analysis. In addition, 20% decrease in gain or breakdown voltage, 10% increase in forward voltage drop, or 100% increase in leakage current should also be cause for removal.

The parts surviving Groups IIIA and IIIB testing are then subjected to the same life test sequence as Group II samples. Again, key electrical parameters are measured at regular intervals and the parts are electrically characterized at the completion of dc life testing. Data taken is compared to initial characterization results to determine the effects of the various screens on part parameters and their related dependence on bias and temperature.

The last group of tests (IIIC) are intended to test the mechanical integrity of the part assembly and the package. While most part capabilities far exceed the limits of test equipment capabilities, some inherently weak designs or processes in parts will be revealed during such testing. This group is recommended only where some doubt exists as to the integrity of the part assembly. All of the parts recommended in Section F have demonstrated their capabilities in each of these areas under many types of evaluation tests and by past usage so that Group IIIC testing is not necessary. A review of existing data is an acceptable substitute for actual Group IIIC tests for any part. The Group IIIC tests are recommended where uncertainty exists in the ability of the part to meet certain stress levels imposed by the application. These techniques are a means of discovering part destruct limits and discovering weak configurations or designs. The types of tests and their intent are shown in Table 10. Testing is usually stopped when 50% failures are obtained. Most of these tests (especially shock and vibration) require expensive fixtures and equipment and should only be performed where doubt exists about the part's environmental capabilities.

At the completion of the testing, the failure analysis and construction analysis results and the electrical test data is compiled and analyzed. Several possibilities exist.

If a majority of parts in the screened (Class I) and the unscreened (Class II) samples fail during qualification, the integrity of the part, screening, and qualification testing should be questioned. Severity of the qualification can be assessed if the destruct levels of the Group III Testing and the results of Group I reveal that the parts are sound. If only one manufacturer's part type exhibits high failure rates, then the integrity of that part is questionable.

If the screened parts have a low rate of failure while the unscreened parts have a high failure rate during qualification testing, it can be assumed that the screening is effective. If the bulk of unscreened past failures are of the same mechanism, particular processing controls to improve yield and stabilize part production could be suggested to the part manufacturer.

If the Class I parts have a greater incidence of failure than the Class II parts, it can be assumed that the screening is to severe or induces some time dependent failure mechanism. Changes to the screening can then be effected or derating boundaries can be changed to improve expected life.

Table 10 Qualification - Group IIIC Tests

Test	Limits and Conditions	Intent
Thermal Shock	Expanding limits from lower to higher temperature with fixed number of cycles at each set of temperature extremes. Soak time at each temperature 10 minutes minimum and 10 second maximum transfer time. Usually followed by Hermetic Seal test and functional check after each step in temperature. Typical step extremes: Step 1 -25 to +100°C Step 2 -50 to +100°C Step 3 -50 to +125°C Step 4 -50 to +150°C etc.	Checks seals, die attachment, insulator integrity (for dielectrically isolated devices), and soundness of die (cracks, etc.)
Thermal Cycling	Same as Thermal Shock except soak time at each temperature and allowed transfer times are longer. More cycles usually required.	Same as Thermal Shock but not as effective. Note this is usually a cheaper test.
Temperature Storage	Increasing time and temperature soaks. Usually followed by test of key parameters.	Accelerates chemical reactions with dissimilar metals and their related failure mechanisms.
Constant Acceleration	Increasing g levels. Number of cycles at each level and hold time at max g level constant. Usually done in 3 mutually perpendicular axes and followed by a functional check.	Tests integrity of interconnects and die attachment. Also useful in checking mechanical integrity of die support and isolation devices (ceramic tabs, discs, etc.)
Mechanical Shock	Same as Constant Acceleration with the additional variation of pulse width to simulate various energy spectra.	Same as Constant Acceleration with the addition of a check of the strength of the external package. More effective than constant acceleration.
Vibration	Variable magnitude and frequency spectra with fixed duration and number of repetitions. Can be monitored for intermittent operation. Sinusoidal excursions typical. Random more expensive.	Same as Mechanical Shock with the addition of particle detection and intermittent open interconnects when monitored.
External Lead Tensile & Twist Strength	Pull or twist leads to destruction.	Test durability of leads.
Stud Sheer Strength	Torque stud until it breaks.	Verifies manufacturer's limit.
Solder Heat	Increase heat to external leads in gradual steps from 200°C up. Keep duration of exposure at each temperature constant. Follow each step with functional check.	Check capability to withstand installation temperatures.

If the failure rates of both screened and unscreened parts is low, it can be assumed the screen and the parts are adequate (subject to process variations), or the tests are benign. Again the integrity of the qualification can be somewhat influenced by the results of Group I and Group IIIC testing.

In all cases, valuable information regarding needed process controls or screening changes can be derived from analysis of each part failure in the qualification test sequence. Characterization data from pre- and post-life testing and parameter measurements during the rest of the testing should be analyzed to determine temperature coefficients of gain, leakage, current, saturation voltage, and important A.C. parameters such as switching speed and noise figure. The data will allow determination of other items such as crossover points of the temperature coefficient of gain, the current, frequency or voltage dependence of junction capacitance, noise figure, gain, saturation voltage, leakage current, impedances, and admittances, as well as pinch-off voltage and saturation resistance for FETS and any other parameter which is necessary for circuit design analysis. In addition, derating factors for aging characteristics of gain, saturation voltage, and leakage current can be validated.

Finally, the results of construction analysis and any significant results of the qualification testing should be summarized in a report and kept for reference use during procurement, screening, lot acceptance, and failure analysis of production parts. If significant changes to the part are made after qualification, the need for requalification can then be determined.

Screening

Screening tests are performed to eliminate parts not meeting electrical performance requirements and those with built-in defects which limit their useful life. Screening tests can be categorized as 100% tests (all parts supplied are subjected to the test), sample tests (a sample of the lot of parts procured is tested with jeopardy on the entire lot if too many failures are encountered in the sample test), and lot acceptance testing performed by the part user to verify compliance with screening specification requirements.

Figure 3 shows a proposed screening test sequence aimed at discovering time dependent failure mechanisms as well as eliminating parts with workmanship and assembly defects.

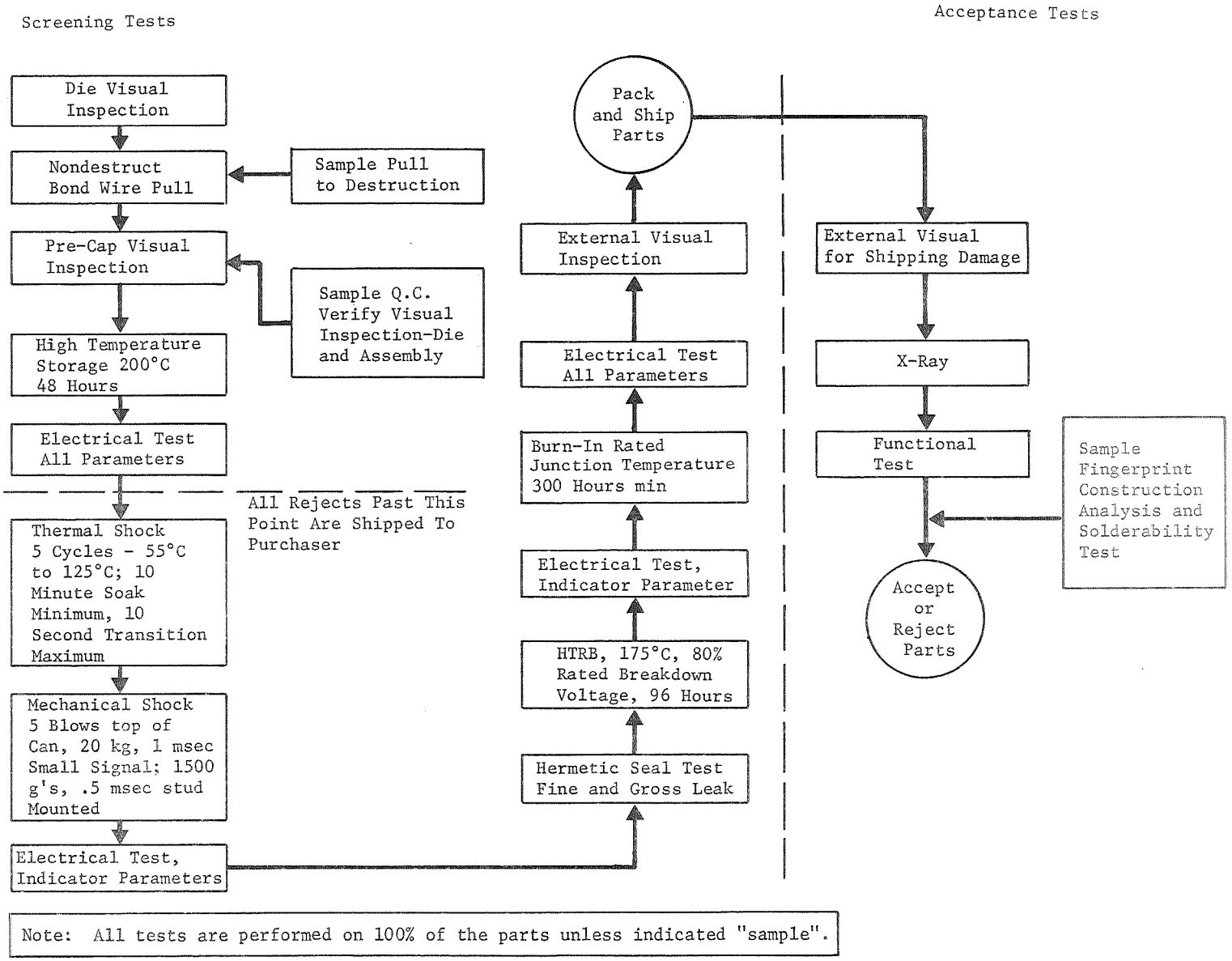

Figure 3 Screening Tests

Most part manufacturers eliminate inoperative or electrically incorrect die by use of a 100% wafer electrical test. Bad die are identified with an ink dot and these die are removed after the wafer is scribed and broken. In addition, incomplete or fractured die are also removed. At this point, it is desirable to perform a 100% die visual inspection at high magnification (dependent upon die size) to remove die with oxide and metallization defects. The visual criteria defined in Marshall Spacecraft Center specification 85M03924 "Internal Visual Inspection of Transistors, Standard For" should be met by all transistor suppliers. Most part manufacturers have internal inspection documents with visual aids to guide the inspector in accept/reject criteria. A review of a part manufacturer's internal documentation for visual inspection should be made for comparison to the MSFC standard and changes to the supplier's documentation made accordingly.

After wire attachements are made to the die and post, each interconnect wire should be tested with a non-destructive wire bond pull to a minimum threshold of 0.7 grams. The wire bond pull test is not destructive. A survey conducted concerning the destructiveness of the pull test had two general responses. Those who employed the test found the pull test non-destructive. Those who did not use pull tests did not because they feared damage, but had not performed tests. A sample wire bond pull to destruction should also be done to discover bond failure threshold and out of control bonding equipment.

Once the part is assembled, prior to capping, the header assembly is inspected at 20 to 40 power to discover common workmanship and assembly defects (extra wires, excess loops, voids in die attachment, particles, etc.) Again the criteria of 85M03924 should be met as a minimum. The problem with any visual inspection is the eye fatigue encountered by the inspector. In addition, most manufacturers emphasize speed, so the inspection may be incomplete. A rigorous QC type re-inspection of the parts on a sample basis or better yet 100% is an effective method of verifying proper visual inspection of parts especially when such re-inspection is performed by the procuring agency.

The first part conditioning step is a temperature soak for 48 hours at 200°C ambient temperature. Frequently header assemblies are "baked out" prior to capping to drive off moisture. Whether capped or uncapped, the environment must be inert to preclude oxidation or other degradation to the part. This conditioning is done to stabilize characteristics, aggravate poor wire bond and die attach failures and growth of resistive contacts between aluminum and silicon.

The first electrical test removes parts not meeting the specified electrical requirements. All specified electrical parameters are tested for all parts.

Thermal and mechanical shock tests followed by functional test and hermeticity tests are intended to destroy improperly assembled parts, break weak seals, and aggravate die cracks. Thermal shock should be per MIL-STD-750, Method 1056.1, or thermal cycling per Method 1051.1, with a maximum transfer time of one minute, with the conditions shown in Figure 3. Mechanical shock should be per the conditions indicated in Figure 3. The electrical test is a go/no-go check of gain and each junction breakdown voltage and leakage current to detect opens and shorts. Hermetic seal tests are per MIL-STD-750, Method 1071 conditions C and H, or D and H, with a fine leak rate of 5×10^{-8} atm cc/sec.

The next test is a high temperature reverse bias for 96 hours minimum at 175°C minimum with 80% rated breakdown voltage applied to collector-base for bipolar or gate-source and gate-drain for FET's. This test is intended to discover channel and inversion layer failure mechanisms. Bias is to remain on the junctions upon the completion of the test until ambient temperature is reached. Leakage current measurements are made within eight hours of removal of bias. If a leakage current increases by a factor of two from its initial value or exceeds the specified limits, whichever is greater, the part is rejected. Such increases are indicative of parts that have channels or surface inversion failure mechanisms.

The next conditioning step is a 300-hour burn-in at rated junction temperature. For bipolar devices, dc forward bias is the most commonly used method. AC burn-in is recommended where it is available and for some r.f. devices necessary. In most cases, however, part manufacturers are not equiped to perform ac burn-in. Rated junction temperature should be achieved as much as possible by power dissipated in the die rather than elevation of the ambient temperature.

Surface devices, such as MOS FET's and junction FET's, are burned in under reverse bias conditions of both junctions for 300 hours at 175°C ambient.

The last electrical measurement removes any parts which have drifted beyond the specified limits. In addition, a 15% change in gain, 100% increase in leakage currents, or a 10% increase in saturation voltages should be cause for part rejection.

The external visual inspection removes parts with corroded or oxidized part leads or packages; scratched, twisted, or broken leads; deformed packages; cracked glass seals; or unintelligible part marking. All acceptable parts are packaged in a manner to preclude shipping damage and shipped to the purchaser along with a report of screening results.

Any rejected part is removed from test and segregated from acceptable parts. All parts rejected in tests subsequent to the first electrical test are shipped to the procuring agency with identification of the nature of part failure.

Lot acceptance is intended to verify part supplier compliance with the requirements of procurement specifications, and to remove parts damaged in shipment. External visual inspection is the same as performed prior to shipment. X-ray is done in three axes to detect common assembly defects, such as extra wire, particles, posts touching can, etc. The functional go-no/go test is intended to discover shorts and opens. Any parts not meeting the requirements of the procurement documents identified to the part manufacturer are removed from the group of acceptable parts.

The sample solderability/weldability tests are performed to detect any material, plating or corrosion problems in external leads. If any part fails this test the whole lot should be suspect for such a problem and inspected. The construction analysis is the same as identified in Group I of the qualification program. It is intended to discover potential lot problems due to manufacturer errors or screening tests and changes to part design or construction which could invalidate qualification. Acceptance of the parts for use in flight hardware is contingent upon successfully passing all of the screening tests and a satisfaction by the cognizant parts specialist that the lot of parts is acceptable. If any condition is unacceptable the part or parts should not be used in flight hardware. The part manufacturer should be informed of the lot acceptance tests that will be performed and that acceptance of the parts is based on satisfactory results from the acceptance testing, including fingerprinting. This will provide impetus to the manufacturer to build a sound part.

Some of the testing and lot jeopardy conditions described may cause some manufacturers to "no bid" the procurement specification. Compromises may be made in the testing done but only if confidence gained by experienced and qualification testing exists in the particular manufacturer. Caution must be exercised in placing too much confidence in part suppliers as many are very schedule and cost conscious and place these considerations before part reliability. It is desirable that more than one supplier be available for part procurement to prevent program delays in event delivery cannot be obtained from one of the sources.

E. PROCESS CONTROL REQUIREMENTS

Critical processes and materials used to fabricate semiconductors are shown in Table 11. The processes used can be categorized as washing and etching, photolithographic, and metallurgical. The basic materials divide into starting semiconductor, dopants, metallization, die attachment, interconnect wire, cap and header, and gas backfill. The most important factors in washing and etching are cleanliness, concentration, sequence, and length of exposure. Thickness, uniformity, length of curing and exposure of photoresists, and mask cleanliness and alignment are significant factors in proper photolithography. The metallurigical processes are time, temperature, and material sensitive. Each successive step is performed at a lower temperature to prevent product degradation processed through previous steps, so the materials used for each succeeding step must interact in the desired manner without serious interaction beyond the step in which they are used.

Selection of starting material and diffusion schemes for the die is usually governed by the generic part selected. Silicon is preferred. The part manufacturer determines the dopants used based on the desired resistivities and penetration depths. Oxide growths must be done at reasonably high temperatures to achieve homogenous passivation of the silicon. Metallization must provide good electrical contact to silicon and bond well to the oxide (in the case of expanded contacts). Eutectic phases (homogenous mixtures of two dissimilar metals) are necessary for die attachment and proper fusion of bond wires to metallization and post plating is essential for sound interconnection. Cap and header materials must be relatively impervious to corrosion or degradation in the application. Gas backfill in the can should be inert and free of moisture and oxidizing or reducing agents.

Table 11 Process Control

CRITICAL PROCESS/MATERIALS	EFFECT OF INADEQUATE CONTROL	REMARKS
Die Fabrication		
Starting Silicon	Improper resistivity results in improper electrical characteristics. Too great a dislocation density results in low yield wafers.	Most poor die rejected during wafer electrical test.
Washes and Etches	Impure wash/etch solutions introduce undesired ionic contamination. Improper etch concentration and buffers resulting in uncontrolled etch rates resulting in overetching or incomplete etching. Improper wash sequences leave certain residual contaminants. Improper time/temperature for washes results in residual waxes, photoresists, etc.	
Masks	Misalignment of successive steps results in improper junction alignments, oxide windows, and metallization interconnects. Dirt, dust, stains, blobs, scratches, and holes in masks result in improper exposure of photoresist leading to pinholes, thin oxides, notched or bridged metal, diffusion anomalies, etc.	
Photoresist	Non-uniform thickness results in voids or thinning of oxides or metallization, diffusion anomalies, etc. Improper attachment of photoresist to wafer results in undercutting of oxides, metals, diffusion spiking, etc.	
Oxide growth	Alkali contamination in tube during growing introduces inversion or channel forming ions in or on oxides. Other ionic contamination on prepared surfaces. Imperfections in photoresist allows etching of oxides in undesired areas (pinholes and thin spots). Dust or blotches on masks result in incomplete exposure of photoresist in undesired areas causing pin holes and thin spots. Discontinuities in epitaxial surface (hillocks) or particles on surface prevent homogenous oxide growth (pinholes). Improper temperature - too high results in degradation of previously diffused areas, too low defective porous oxides.	
Diffusions	Improper doping levels, temperatures, and rates result in low yield wafers. Contaminants in gases or on prepared surfaces during diffusions alters doping or introduces ions providing channels, inversions, or localized breakdown sites.	

Table 11 Process Control (Continued)

CRITICAL PROCESS/MATERIALS	EFFECT OF INADEQUATE CONTROL	REMARKS
Die Fabrication (Contd)		
Metallization	Improper time and temperature during sputtering process yields too thin metal and improper grain structure leading to electromigration. Improper alloying temperature and time: too low-resistive contact at Si Al interface and peeling of Al on oxide, too high - Si migration causing voids at contact window at the step or Si, SiO_2, and Al interaction increasing film resistance. (Recrystalization of Si at grain boundaries).	Large homogeneous grains desirable. Electromigration only a problem in devices with expanded interconnects (wire attachment to die made over oxide rather than at contact window).
Back Lap and Plating	Too thick a die results in increased saturation resistance and switching times. Too thin a die increases probability for handling damage. Incomplete plating results in die attach voids.	
Scribe and Break	Ragged or non-uniform scribe results in cracks, chipouts, incomplete die attached to good die, etc. Warped wafer results in non-uniform scribe.	
Assembly		
Header and Cap	Attached slivers, burrs, or flaked plating which could cause shorts in or outside of package. Improper plating on leads or header which could interfere with proper die attach and wire interconnect. Dimensional problems of can or header or contamination which could preclude formation of hermetic seal. Cracked or imperfect glass seal resulting in non-hermeticity.	
Die attach	Insufficient or excessive preform results in voids or excess eutectic for die attach. Poor operator procedure results in voids under die, particles of eutectic on or around die, cracked or scratched die from mishandling.	
Wire bonding	Improper time, temperature, pressure schedule, and task design for thermo-compression bond results in incomplete bonds, undesirable intermetallic formations, wire necking and tearing, cracked die. Improper time, pressure, energy, and tool design for ultrasonic bonds results in incomplete bonds, wire necking and tearing. Insufficient weld or bond area at post. Poor operator procedure results in excess pigtails; extra wires; bent, twisted, scratched, kinked or nicked wires; excess wire loop; wrong hookup, crosssed wires. Balls introduced as result of wire cut operation.	

Table 11 Process Control (Continued)

CRITICAL PROCESS/MATERIALS	EFFECTS OF INADEQUATE CONTROL	REMARKS
Assembly (Contd)		
Washes and Cleans	Impure cleaning solvents and wash sequences leaves residual surface ions resulting in increased leakage, inversions, etc. Corrosive solvents degrading plating, metallization, etc. Excessive energy at ultrasonic cleans introduces excess mechanical stress to die and wire interconnects.	
Capping	Insufficient bake out to remove surface contaminates. Contaminated gas ambient in capping station. Wrong weld schedule for materials to be used results in incomplete seals. Slug introduced internally.	
Test, Storage, Shipping, and Accountability	Coorosive environments during storage results in degraded packages and leads (especially during high temperature storage or operation). Finger acids and greases degrades leads and packages. Poor sockets scratch, mar, and gouge part leads. Mishandling results in lost, broken, or damaged parts. Poor shipping materials and practices result in lost or damaged parts in transit from manufacturer to user. Improper marking results in loss of traceability.	

1. Die Fabrication Processes

Die fabrication is the most sensitive process to part manufacturers, and cleanliness controls in this area greatly influence the long-life performance of a part. The degree of control exercised by the manufacturer in this area is extensive to prevent poor die and wafer yields. Most semiconductor manufacturers consider their wafer processes proprietary and will not submit to part user participation in some cases. The user may specify minimum metallization thickness and require phosposilicate glass protection for the die surface in the procurement specification. Ohterwise the extent of control of die processes by the part user is implied by screening and selection of the best manufacturer rather than by direct documentation.

Manufacturers with the most stable parts historically and by qualification test usually have adequate wafer processing controls. The screening tests described in the previous section will reject almost all of the products with poor die fabrication process control.

2. Assembly Processes

These processes involve a significant human element, since many assembly techniques involve operator judgements. Some manufacturers have incorporated automated assembly tools which eliminate some of these factors, but most rely on assembler skill. Control in this area is achieved through several routes.

The most common form of assembly process control is a Quality Control surveillance of manufacturing production, where Quality and Manufacturing are separate organizations. The Quality function monitors equipment set-up (wire bonder temperature and pressure settings, die attach stage temperature settings, etc.). Quality also monitors wire bond work via periodic sample bond pull tests of each operator's work. Weak bonds indicate need for tool check or operator retraining. Visual inspections for workmanship defects is another method frequently used to effect assembly process control.

The part user can effect control of assembly processes by such Quality surveillance using his own Source Inspection on the assembly line. Some manufacturers have available a "control line" where the assembly line produces parts under the cognizance and monitoring of personnel employed directly by the user. This approach is somewhat more costly than the normal manufacturer/user situation, but allows the user a greater degree of participation in part assembly and inspection.

Precap visual inspection of the die and header assemblies is perhaps the most effective screening method for eliminating assembly defects, especially if the inspection of all parts is monitored by a user employee prior to capping. Any parts not meeting visual standards defined in the procurement specification are removed from the lot. Again, selection of manufacturers with a stable part, historically and by test, will afford parts manufactured in a controlled manner. Screening will eliminate most improperly assembled parts.

3. Materials

Control over the materials used is achieved by selection of the desired generic part and through specification in the procurement documents. Parts with undesirable die, metallization, interconnect, die attachment, and package materials can be eliminated during evaluation and qualification.

The criteria set forth in Section C should be applied when selecting parts types for use. Changes to materials can be discovered during lot acceptance testing of the production parts. Undesirable changes would result in a rejected lot. Knowledge of such lot acceptance requirements will stimulate the part manufacturer to inform the user of such changes at the time of procurement.

External lead and case materials are normally defined in the procurement specification and by the type selected. The die, metallization, and interconnect wire materials and the gas backfill can also be specified in the procurement document.

4. Handling, Storage, Test, and Shipment

Once a good part is produced, control of test, storage, handling, and shipment is needed to preserve the part integrity. All high temperature exposure should be in an inert environment. All parts should be handled with gloves or finger cottles to keep acids and greases off leads and packages. Parts should be stored and tested in non-corrosive environments. When shipped, parts should be packaged in containers which will survive handling environments in transit. Test sockets should not scratch or bend leads. Parts sensitive to electrostatic discharge damage should be protected by shorting all external leads together until installation.

Shipping instructions are usually defined in the procurement specification. Control over the test and storage environments and handling of the part is usually achieved by approval of the manufacturers test plan and procedures. Well defined controls in these documents is necessary to avoid degradation to good parts. Handling and installation control requirements by all users of parts should be well defined and stringently enforced to preclude damage to good parts.

F. PARTS LIST

1. Acceptable Parts

Table 12 is a list of transistors which have considerable successful usage history. Much conventional circuit design can be done using these devices. These parts are preferred because of the amount of qualification and evaluation data available and because their design and construction meets most of the desired criteria discussed in Section C. In some applications, parts with better performance characteristics are available, but do not have as much accummulated data and history, consequently involve more qualification efforts.

2. Unacceptable Parts

Non-hermetically sealed devices are unacceptable because of the contamination involved in plastic encapsulation. Mesa, grown junction, and alloy constructions have serious drawbacks over planar types and are not recommended. Germanium has temperature limitations not encountered in silicon and consequently should not be used. Certain new technologies such as ion-implantation, and other semiconductors (GaAs, CdS, etc.), do not have proven stabilities, either in manufacture or application. MOS transistors pose some unique handling problems and their use should be restricted to special applications where very high input impedance preclude use of junction devices. Beam lead appears to offer several solutions to common semiconductor problems, but a better understanding of its unique failure mechanisms and problems must be obtained before it is widely used. Mesa constructions are generally necessary for high voltage devices $\left(300\text{V } BV_{CB} \text{ or more}\right)$. The technique for passivation must be carefully evaluated to understand its influence on part life.

Table 12 Acceptable Parts

TYPE	NPN	PNP
Bipolar		
Small Signal		
Amplifier	2N2484	2N2605 (2N3799 [1])
General Purpose	2N2222A,	2N2907A,
Switching	2N2369A	2N3546, 2N3251A
Clipper	2N2432A	2N2946A
R.F.	2N918 (2N3700)	2N4957 [2]
Medium Power		
General Purpose	2N2219A, 2N3019	2N2905A, 2N4405
Switching	2N3501	2N3467
R.F. Driver	2N3866	
High Power		
Amplifier	2N2880, 2N2814	2N4399
R.F.	2N3375	
Switching	2N5659	
	2N5330	
Multiple		
Dual Diff. Amp	2N2060, 2N2920	2N3350, 2N3811
	N-CHAN	P-CHAN
Field Effect		
Amplifier	2N3685	2N2608
Switch	2N4391	
Dual	2N5196	

[1] 2N3799 has much better operating characteristics than 2N2605 but not as much history.

[2] Limited number of suppliers.

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V. DIODES

by C. W. Riss

V. DIODES

A. INTRODUCTION

This chapter is addressed to diodes in general rather than directed towards specific kinds with respect to function. The die fabrication techniques are fundamentally the same, with variations in geometries used to achieve the varying functions. This chapter addresses three fundamental kinds of package construction. These are:

1) Voidless monolithic.

2) Double slug whiskerless.

3) Whisker (whisker includes all connections with the die that are not made directly to a slug/heat sink or an external lead).

There are many variations with respect to packages. These include microwave pill types, TO-5 types, DO-7 types, DO-4 types, and other types that have no common designation. Regardless of the variations, the die attachment and electrical interconnections utilized can be discussed as a variation of the three fundamental package constructions.

The information is further addressed to kinds of parts that have historically demonstrated a capability of operating in the military and space type environments. An example of these can be found by referring to the list of acceptable parts contained in Section F.

B. GUIDELINES FOR LONG-LIFE ASSURANCE

Storage life of diodes is estimated to be greater than ten years for present day parts. The service life of a diode that is well constructed and properly applied is also estimated to be greater than ten years. Life limitations are due to failures caused by defects rather than life limiting wearout mechanisms.

Part screening techniques normally restrict part failures to the part manufacturer's facility. Better wafer scribing techniques, in-line checks for bulk silicon defects, oscilloscope display tests, parameter drift detection, and accoustical noise tests will minimize the probability of receiving defective parts.

The part user must also contribute to part long-life by proper application of the part. Packaging is as much a part of proper application as is the circuit application.

1. Design Guidelines

1) Use phosphosilicate glass for glassivation of die surfaces. The phosphosilicate is desired because of its characteristic to act as a gettering agent for sodium.

2) Use silicon nitride (Si_3N_4) as it protects junctions from degradation from the mobile ions such as sodium. Si_3N_4 alone is insufficient as process control is difficult and demonstration of control is as much a requirement as the presence of the Si_3N_4.

3) Utilize laser, chemical or ultrasonic scribing techniques to prevent cracks that occur during diamond scribing.

4) Use scanning oscillator techniques (SOT) to aid in detecting bulk failures, such as dislocations, that occur during the processing stages.

2. Process Control Guidelines

1) *Demonstration* - The part manufacturer should demonstrate process control effectiveness. This should be in the form of records that show increasing or stable yields for the processes in question or in the form of test data (from periodic testing) that shows decreasing or stable reject rates. Data of this nature will demonstrate that the processes are being controlled effectively. Other results may indicate inadequate process control.

2) *Check Points* - The part manufacturer should have in-line check points that verify that the process is in control. An example of this is a lead bond pull test of a sample of units taken from the line in a periodic manner. Consisted or increasing bond pull values would be indicative of lead bond process control. Varying or decreasing values would be indicative of inadequate process control or personnel variations.

3. Test Guidelines

Testing must be based on the results of the evaluation of the part. Tests may vary from part to part depending on construction and function.

1) The qualification testing in section D herein should be performed on each procurement lot. These tests will verify part fabrication process control that could vary from lot to lot. The stress levels will be governed by the system requirements.

2) The screen tests in section D herein should be performed on all parts to be used in the fabrication of production hardware. These tests will detect gross mechanical defects and defects that result in electrical parameter variations and early life failures.

3) Use oscilloscope display tests since they are more effective than automatic test equipment in detecting parts with anomalies. The oscilloscope display will aid in detecting unstable parts by exhibiting the breakdown characteristics.

4) Electrical parameter measurements must be made before, during and after burn-in or life testing to determine which parts are stable. Parameters may drift initially and then stabilize at a new level. Measurements of this kind would preclude rejection of stable parts.

5) Tests designed to detect particles such as weld splatter or solder balls must be implemented. Monitored vibration or a Particle Impact Noise Detection (PIND) test would be effective.

6) High temperature bias must be performed on planar type diodes. The exposure to voltage or current and temperature will detect inversion or accumulation defects.

7) Burn-in for all parts is recommended.

4. Application Guidelines

1) Current and voltage derating must be required. This derating will maintain lower junction temperatures and protect against spurious surges. Current and voltage must be derated 50%.

2) Stud torque and seating plane flatness must be controlled to prevent excessive stresses in the die/header interface and to promote better heat transfer.

3) Limit operating junction temperature to 110°C to achieve longer life.

4) Provide stress relief of leads and interconnecting wires to prevent damage to the hermetic seal of the part.

5. Special Considerations

1) Current ratings in terms of lead temperature versus lead length must be established. This kind of information is useful to a designer for calculating heat sinking requirements and will standardize current ratings.

2) A manufacturer selection must be performed. Selection criteria consists of a history survey, process maturity verification, and part evaluation. This will aid in selecting the best part.

C. LIFE LIMITING PROBLEMS AND SOLUTIONS

1. Failure Mechanism Analysis

Diode failure modes consist of shorts, opens, and parameter degradation. Mechanisms for these modes, which are precipitated by electrical overstress or mishandling, are not discussed. The failure mechanisms discussed in the following paragraphs are summarized in Tables 1 through 5. They are classified as follows:

1) Bulk Defects - Failures due to faults in the silicon wafer;

2) Surface Defects - Failures due to faults in the oxide or passivation;

3) Wire/Bond Defects - Failures due to faults in lead interconnects (internal or external);

4) Contamination Defects - Failures due to contamination on the die or in the package;

5) Mechanical Defects - Failures due to faults in the package or die attachment.

a. Bulk Defects - Bulk faults result from defects in the silicon wafer (Table 1). Failures of this nature are limited and are usually detected during electrical testing at the part manufacturer's facility. Dislocations, if present during processing, provide nucleation centers that are conducive to the formation of metal precipitates (Ref 1). This occurrence causes soft breakdown characteristics or high leakage currents. Failures due to dislocations are considered to be minor with respect to surface-related failures. Dislocations in wafers can be detected by the use of the scanning oscillator technique (Ref 2). This is a nondestructive technique and can be utilized as an in-line check after each processing step. Dislocations may be present during electrical testing, but located such that electrical testing does not detect them. This is particularly true when the test is performed by short pulse techniques or with digital readouts. Because of stresses during use, dislocations may propagate to the junction area and degrade breakdown or leakage current.

Table 1 Failure Mechanism Analysis-Bulk Defects

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Metal precipitation	Gold precipitates during manufacturing operations such as glass sealing resulting in soft breakdown characteristics.	Power cycling with electrical test (Breakdown voltage)	Not known. Possibly related to dislocations.
Dislocations	Imperfections in the silicon that provide nucleation centers for metal precipitates that result in soft breakdown characteristics.	Power cycling with an electrical test (Breakdown Voltage).	Monitor wafer processing with a scanning oscillator (SOT).
Cracked Die	Scribe crack propagates into the junction.	Internal visual. Electrical test.	Ultrasonic or laser scribing.

Cracked die are usually detected during a visual or an electrical test. However, it is possible that cracks considered to be acceptable during the visual examination could propagate, due to temperature cycling, and penetrate the junction. The time involved could be such that failure occurs during service. The use of laser, chemical, or ultrasonic scribing techniques could eliminate or minimize the possibility of this mechanism occurring.

b. Surface Defects - Surface faults, as discussed herein, are applicable to both mesa and planar parts (see Table 2). These failures result from defects in the oxide layer and surface passivation or cleanliness of the die surface at the junction. Defects on planar construction result in inversion, accumulation, or shorts. Failures on mesa construction result in high leakage currents or premature voltage breakdown.

Inversion is a phenomenon accentuated by a high temperature reverse bias (HTRB). It occurs when a P-type region forms on the cathode surface, resulting in an extension of the anode region and causing high leakage current (Ref 3).

Shorts are caused by pinholes in the oxide. Pinholes that go through the oxide are relatively easy to detect during electrical test. Pinholes that do not go completely through the oxide are a potential problem that can result in breakdown voltage and leakage current degradation.

Accumulation is a phenomenon brought about by a high temperature forward bias (HTFB). It occurs when donor states in the oxide become positively charged, resulting in an n+ layer that results in high leakage currents (Ref 3).

c. Wire/Bond Defects - Diodes come in a variety of packages. Some of them are similar to the transistor TO-5 types. For these types the wire/bond failures will be of a similar nature (see Table 3).

Gold-aluminum systems experience failures caused by intermetallic formations or voids under the bond. Aluminum - aluminum systems experience failures in the wire adjacent to the bond area due to excessive pressure during bonding causing cracking in the wire.

The gold-to-gold thermal compression type of interconnect is the preferred technique. This is because of the compatibility between the wire metal and bonding pad metal. In addition, the gold wire has better long-life characteristics with respect to temperature cycling caused by current switching.

Table 2 Failure Mecahnism Analysis - Surface/Defects

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Ion Migration through and across the Oxide.	Inversion of the n region near the anode contact. Surface contamination and lack of an oxide sealant.	High Temperature Reverse Bias Reverse Current Deltas	Improved control of surface cleanliness. Application of phosphosilicate glass over the oxide.
Hole Trapping in the Oxide.	Donor states in the oxide becomes positively charged resulting in an accumulation layer and premature break-down.	High Temperature Forward Bias Reverse Current Deltas	Improved control of surface cleanliness. Application of phosphosilicate glass over the oxide.
Holes in Oxide.	Pinholes in the oxide result in shorting paths from anode to cathode.	Electrical test.	Improved process control.

Table 3 Failure Mechanism Analysis - Wire Bond Defects

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Open Wires.	Improper bond schedule. Bond separates or wire necks down too much.	Internal visual. Mechanical/thermal stress with electrical test.	Process control. Study to determine feasibility of performing a 100% non-destructive bond pull.
	Intermetallic formation.	Mechanical/thermal stress with electrical test.	Monometallic interconnects.
	Nicks in wires cause high current densities that melt wires.	Power cycling electrical test.	Internal visual.
	Improper or out of control weld schedule resulting in poor weld to post.	Visual, thermal shock, electrical.	Process control, internal visual.
Shorted Wires.	Large relief loops touching during shock or vibration.	Monitored shock and vibration. Internal visual.	Internal visual.

Established, verified, and controlled bond schedules are a requirement for reliable bonds. The part manufacturer should have evidence of bond schedule parameter combinations that were used in developing his bond schedule for each kind of part. He should have test data to show the stress levels that the various bond schedules are capable of withstanding. He should have in-line control to assure that bond quality is being maintained.

Most of the S or C bend type of interconnect defects are easily detected by a visual inspection of the completed package prior to painting. These are the misplaced, excessive bend or touching die type of defects. A more difficult type of defect to detect is insufficient pressure against the die contact or mechanical contact only.

Power stud diodes use a variety of interconnect techniques. Some use an ultrasonic bond, some use an alloy type and some use solder. The solder type of interconnect would be the least desirable because of a thermal fatigue problem. The alloy or eutectic type has proven to be an acceptable method. The ultrasonic bond is a reliable technique if properly established and controlled. Some parts may have either an alloy and an ultrasonic bond or an ultrasonic bond and an electronic weld.

The prime concerns should be that the process has been established, verified, is controlled, and uses materials that are compatible.

Some double slug type diodes depend on the glass case to provide the compression to maintain electrical contact between the die and the leads. This can result in parameter variation during temperature cycling. After a stabilization period, the parameters are within specification limits. The change occurs during the temperature change because of a difference in thermal coefficient of expansion between the glass and the heat sink materials.

Some double slug diodes use a construction technique that forms a monolithic structure of the heat sinks and the die. This is achieved by plating the die and the heat sinks with compatible materials and elevating them to a high temperature (1000°C) to form the bond. The bond interface is across the total die surface.

Methods of external lead attachment to the diode heat sinks vary. One method is to form the lead attachment directly to the heat sink using only the heat sink plating and the lead material to form a eutectic bond. This results in a bond that is as strong as the tensile strength of the wire. The bond is formed at about 700°C

and is relatively void free. Another method is to utilize a third metal as the eutectic. This method has a tendency to have voids similar to those encountered in eutectic die mounting. Severe voiding could result in a weak lead connection that could fail in shock or vibration during service.

d. Contamination Defects - Contamination discussed in this paragraph refers to any material in the package, loose or attached, that is not part of the design. Examples are weld splatter, silicon chips, solder balls, and pieces of internal lead wire. These are summarized in Table 4.

Sealing of metal packages by welding causes a weld splatter. These particles of weld splatter may or may not be located so as to be detected during electrical testing. Those that are not may relocate during shock or vibration in usage and cause a shorting condition at that time.

Silicon chips can result from diamond wafer scribing. Scribing may cause cracks in the silicon that will propagate in a manner that will cause a chip of silicon to separate from the die. The propagation rate is dependent on time, temperature and environment exposure. The chip could cause a short or mechanical damage during shock and vibration in usage.

Some diodes are assembled using solder to attach the die to the header. During the soldering process, solder balls may be formed. This introduces a potential failure mechanism of the same type as weld splatter. The balls may break loose during environmental stress and cause shorts.

Diodes assembled with internal lead wires are exposed to potential failure mechanisms similar to transistors and integrated circuits. Wire particles and pieces may remain in the package to cause shorts or mechanical damage. These kinds of diodes lend themselves to internal visual inspections that will remove many of the defects.

e. Mechanical Defects - Mechanical defects discussed in this paragraph are related to the package defects that prevent the part from performing its intended function. Examples are loss of hermetic seal, die separation, and poor solderability. These are summarized in Table 5.

Table 4 Failure Mechanism Analysis - Contamination Defects

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Contamination	Weld splatter from package sealing of metal cans causes shorts.	X-ray, acoustical noise test, monitored vibration.	Glassivation, weld splatter ring.
	Die chips cause shorting.	Internal visual electrical test.	Internal visual, glassivation monolithic construction.
	Bonded lead wire tail broken off causing shorting.	Internal visual, electrical, monitored vibration.	Internal visual, glassivation, monolithic construction.

Table 5 Failure Mecahnism Analysis - Mechanical Defects

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
A. Double Slug Contruction			
Loss of Hermetic Seal.	Fracture of glass case.	Visual; dye penetrant.	Handling techniques; mounting techniques; 100% visual inspection.
	Seal fracture due to insufficient sealing area low heat, short time, contamination.	Visual.	100% visual; better controls on pre-seal and seal operations.
Poor Solderability.	Contamination of plating or base metal during plating.	Hot oil dip of solder coated leads on sample basis. Visual.	Control of cleaning and plating operation. 100% visual.
Intermittent	Variation of conductivity during temperature cycling. Lack of control of assembly process.	Monitor V_f during temperature cycling.	Process Control. Use monolithic double slug construction.
B. Whisker (TO-5 Type) Construction			
Loss of Hermetic Seal.	Fracture of the glass to seal.	Hermetic seal test.	Handling techniques, mounting techniques.
Die Lifted.	Excessive voids in the eutectic bond.	X-ray, thermal impedence test.	Vacuum during eutectic bonding.
Poor Solderability	Contamination of plating or base material prior to or during plating.	Hot oil dip of solder coated leads on a sample basis. Visual inspection.	Control of cleaning and plating operations.
	Oxidation or contamination of the plated metal due to handling.	Visual.	Application of a protective coating that is compatible with normal fluxing and soldering operations.

Table 5 Failure Mechanism Analysis - Mechanical Defects

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
C. Whisker Contruction			
Loss of Hermetic Seal.	Fracture of glass case.	Visual; seal test.	Handling techniques; mounting techniques.
	Seal fracture due to insufficient sealing area, low heat, short time, contamination.	Visual; seal test.	100% visual; better controls on pre-seal and seal operations.
Poor Solderability	Contamination of plating or base metal during plating.	Hot oil dip of solder coated leads on a sample basis.	Control of cleaning and plating operation. 100% visual.
D. Voidless Monolithic Construction			
Loss of Hermetic Seal.	Fracture of the glass case.	Visual; dye penetrant; electrical	Handling techniques; mounting techniques.
External Lead Separation	Poor braze.	Visual; pull test.	Single element metallurgical bond; better control of brazing operation; vacuum brazing.
Poor Solderability	Contamination of plating or base metal prior to or during plating.	Hot oil dip of solder coated leads on sample leads on sample basis. Visual.	Control of cleaning and plating operation; use of single element leads 100% visual.

Loss of hermetic seal is caused by cracked glass, bubbles or voids in the glass or poor adhesion of the glass to the metal. These defects are detected by hermetic seal tests or a visual inspection. Cracks are caused by improper handling or mounting in usage.

Die separation occurs when excessive voids are present in the die bond material or the die bond material deteriorates with time or temperature. Failures of this nature are related to constructions that do not contain the die by some means; e.g., double slug with a glass sleeve as a structural member; C or S whisker with spring pressure. They also occur in TO-5 or DO-4 type case where the die bond relies on a eutectic or similar type bond.

Poor solderability results from contaminated plating, poor adhesion of plating, or plating that fundamentally has poor solderability characteristics. Contaminated plating is caused by handling with bare hands and leaving finger oils or acids on the leads, inadequate cleaning of corrosive solvents, or oxidation of the lead plating. There are protective coatings available that are compatible with standard fluxing and soldering techniques. These coatings protect the leads from oxidation or contamination due to handling.

Poor adhesion of plating is caused by contamination of the base metal prior to plating, improper cleaning of the base metal, plating that is not compatible with the base metal, or plating directly over the base metal without an intermediate metal to aid in adhesion. Adhesion problems affect long life because they are a time dependent mechanism. The best means of prevention is a review of the processes to be used to determine if sound metallurgical practices are followed.

Platings that have poor solderability characteristics tend to cause more problems than failures. Some plating materials have characteristics that do not lend themselves to ease of soldering. Nickel is an example. Connections can be made to nickel if proper preparation is performed. This preparation is more complex than when preparing a tin plated lead for soldering. Poor solder joints of this type are usually detected in lower assembly levels and do not cause system failures because of poor solder joints. However, effects of rework on the system reliability could be significant.

2. Design

a. Selection Criteria - Developing the selection criteria for parts for long-life applications is a critical phase in the total effort. The purpose of a pre-use evaluation is to determine what part types would be best to use and for each part type which one is best and which manufacturer would be best. The criteria should be established and implemented as early as possible so that all phases can be completed in a time frame that is compatible with the needs of design engineering, procurement, and manufacturing. The criteria should include a history survey, process maturity verification, part evaluation, manufacturer evaluation, and presence of desired construction features.

1) History Survey - The history survey is necessary to determine the success that candidate parts have had in previous space applications. Failures that have occurred should be checked to verify the failure mechanisms. (This information will serve as a guide for qualification or screen test activity.) Information obtained on the history survey can be used to modify preliminary preferred parts lists. Data from various lots should be evaluated to determine stability from lot to lot.

2) Process Maturity Verification - Process maturity verification is necessary in order to keep part evaluations and design parameters from fluctuating. The user should review processes to determine when changes were made and what the change was. Too many changes or vascillations may be indicative of unestablished or out of control processes. Each change will have to be judged on its own merits. Test data should be available to verify that the changes do what was intended and do not cause reactions that are detrimental to the life of the part.

3) Part Evaluation - Part evaluation is necessary to determine which part has features most conducive to long-life. The evaluation should include electrical tests, including step stress testing; short-term life (1000 to 2000 hours) stability; long-term life (10,000 or more hours) stability. This may be satisfied by existing data or analysis of prestressed parts to be compared to construction analysis of environmentally and electrically stressed parts. Evaluations of this nature are time consuming, costly, and are usually performed in a manner that yields inadequate results. A check of other users may reveal evaluations in the processes of being performed or already completed. Such results could be used if their integrity can be verified.

The construction analysis should be performed on more than one or two parts and should concentrate on the soundness of the design, apparent process control, and the presence of desired features.

4) Manufacturer Evaluation - An evaluation of the manufacturer should also be performed to determine his philosophy toward high reliability parts, process controls, his reaction to failure analysis corrective action recommendations, his ability to deliver when promised, his quality control policies and records, his manufacturing areas and test facilities, his predictions on how long production of the parts will continue, and the back log of orders for the parts being considered.

5) Presence of Desired Features - The desired features for long-life of diodes can be covered only in a general sense because of the variety of constructions used. What is ideal for one is not necessarily ideal for another. The items to be considered include construction features, stability of parameters, and specific features. The construction features are summarized in Table 6.

Construction - Consideration must be given the soundness of construction with respect to the kind of diode being considered and the application conditions that will be encountered.

When a choice can be made between a monolithic double slug and other kinds of construction, the monolithic construction is the desirable technique; between a whisker switching diode and a double slug switching diode, the double slug diode is the desired technique; between a solder die bond and a eutectic die bond, the eutectic die bond is the desirable technique; between lead attachment methods to double slug diodes, first choice is single element eutectic, second choice is dual element eutectic, third choice would be soldered.

Epoxy die bonds have been considered to be undesirable. Generally speaking, this may be true. Some manufacturers have used a form of an epoxy to achieve a die bond. Parts of this nature have been used on high reliability programs with no die bond failures or parameter degradation attributed to epoxy. If epoxy die bonding is the only fault noted, its other features may outweigh the features of a part with a eutectically bonded die.

It is not sufficient to select a bonding technique without giving consideration to process control or success history. A good technique by itself does not assure long-life. Evaluation is necessary to select the best part.

Table 6 Design Factors for Long-Life Assurance of Diodes

DESIGN FACTORS	REMARKS
1. CONSTRUCTION	
a. Monolithic double slug	This construction is limited to rectifiers and some general purpose diodes.
b. Die bond	The preferred method is a gold eutectic.
c. Lead attachment	The best method is a single element eutectic. Second choice is a dual element eutectic. Soldering is the third choice.
2. DIE CONSTRUCTION	
a. Passivation	Phosphosilicate glass should be used.
b. Planar	Planar type construction should be used rather than mesa.
c. Scribing	Laser, chemical or ultrasonic scribing should be used.

Use of the double slug type package eliminates some of the failure mechanisms common to whisker type packages. In some instances, it may introduce failure mechanisms that are non-existant in whisker type diodes. The monolithic double slug is an improvement in construction over the double slug.

The monolithic double slug is not "the" solution. Certain diode characteristics are achieved by techniques that do not lend themselves to the monolithic or non-momolithic double slug construction. For example, characteristics that are necessary for high frequency microwave applications are achieved by etching the silicon to form a mesa. The etching reduces the strength of the silicon in the junction area, resulting in an inability to support a bond to the slug.

Parameter Stability - Parameter stability is a function of passivation materials and techniques. Opinions vary as to the ideal passivation. Most agree that a glassivation offers the most significant protection. The glass should be a phosphosilicate type that will act as a gettering agent for impurity ions.

Silicon Nitride (Si_3N_4) has characteristics that are desirable for a passivating material. Some manufacturers are using it now. Others have tried it in the past and found that it did not offer significant advantages over a phosphosilicate glass at that time. Theoretically, Si_3N_4 would enhance the life of semiconductors because of its resistance to diffusion by many elements, high dielectric constant, chemical inertness, and mechanical durability (Ref 4). Process control is critical in the application of Si_3N_4. Although its use may be desirable, the manufacturer's ability to control the application should be verified. A part, with Si_3N_4, from a manufacturer that has recently implemented it may not be as reliable as a part from a manufacturer that does not use it. Part evaluation will help to select the best part. Parameter stability is the prime consideration.

Specific Features - There are some specific features that should influence the selection *if all other items considered are equal*. These are:

a) Die or Geometry Size - The larger the junction, the greater the current carrying capability. Conversely, this means that for the same current, the junction will be cooler.

b) Die Shape - A round die will have better high voltage characteristics than a die that has square corners.

c) Die Scribing - Die scribing with a diamond will cause more cracks than a laser, chemical etch or ultrasonic technique.

d) Depletion Region Thickness - A wider depletion region will have lower voltage gradients (volts/mil) than a narrow depletion region.

b. Results of Survey - A telephone survey of diode users was conducted to determine what special or unique controls or tests were imposed and what they were intended to control or detect. The results are summarized in Table 7.

Seven users were contacted. Most users were performing standard Mil-S-19500 type testing. Three were performing tests that were not standard Mil-S-19500 tests. The special tests were monitored mechanical shock, power cycling, parameter stability, bond pull after mechanical shock and vibration, monitored thermal cycle, surge current, and monitored breakdown voltage.

The monitored mechanical shock is performed to detect particles that may cause shorting. Another method, not mentioned by the users contacted for detection of particles, is the Particle Impact Noise Detection (PIND) test. The PIND test is performed by vibrating the parts and listening for noise caused by loose particles. The PIND test could be used only on metal can, cavity type parts.

Power cycling is performed as a qualification test to detect poor interfaces in lead bonds and die bonds. The cycling is performed by forcing current through the diode to cause the junction to heat up to its rated value. The current is then turned off until the junction cools to about +25°C. Current is reapplied and removed in the same makner for the necessary number of cycles.

Parameter stability testing is performed on parts that are subjected to a life test. Parameters monitored or checked are parameters that are key parameters for the part; e.g., reverse recovery time $\left(t_{rr}\right)$, capacitance, minority carrier lifetime, etc. The key parameters are not to be confused with the standard quality indicating parameters, such as leakage current $\left(I_R\right)$ and forward voltage $\left(V_F\right)$, that are normally measured before and after life testing.

Table 7 Survey of Electronic Part Users

PART TYPE (CATEGORY)	USER	UNIQUE TEST OR SPECIFICATION REQUIREMENTS	RATIONALE/JUSTIFICATION
Diode	Bell Telephone	Monitored shock	Particle test
	Martin Marietta Denver	Power cycling for qualification	Die bond/lead bond check
		Reverse recovery time stability during life	Detect drift during 1000-hour life test
		Bond pull after mechanical shock and vibration	Detect effects of shock and vibration on bonds
		Monitored thermal cycle	Detect poor bonds
	TRW Systems	Surge current for double heat sink nor metalurgical bonds	To detect intermittents during temperature excursions
		Monitored breakdown voltage tests (oscilloscope display)	To detect unstable junctions

Bond pull test is performed as a part of qualification testing after the parts have been subjected to mechanical shock and vibration. The purpose of the test is to determine the effect of mechanical shock and vibration. The purpose of the test is to determine the effect of mechanical shock and vibration on leads and lead bonds.

The monitored thermal cycle is performed to detect weak lead bonds and die interface bonds. The electrical tests performed before and after thermal cycling may indicate that the part is acceptable. However, an intermittent could occur during the temperature excursion that could result in erroneous system operation. The monitored thermal cycle test would detect any intermittent, or open, condition.

The surge current test is performed to detect poor lead bond or die bond interfaces. When used to detect poor lead bonds, the amplitude should be small, about 50 or 100 ma, so that a welding operation is not performed that will tend to cure the weak bond interface. When the surge is used to detect poor die bond interfaces, the amplitude should be large enough, close to the part rating, to cause heating due to the high resistance of the poor contact. The V_F is checked prior to the surges and after the surges to determine the transient thermal impedance. The test limits for the transient thermal impedance are determined from a gaussian distribution. The high contact resistance parts fall outside of the distribution. A part manufacturer is presently performing a transient thermal impedance test. The total test time per part is about 60 milliseconds.

The monitored breakdown voltage test is performed to detect instabilities in the junction. Parts that exhibit discontinuities or dynamic instabilities are removed from the lot. An oscilloscope is used to monitor the breakdown. Instabilities in the trace are indicative of junction impurities and defects.

c. Alternate Approaches - Alternate approaches possible are the use of other part types or development of new processes or tests.

The use of other part types is a possibility for some applications. Integrated circuits could be used for low power applications. The advantages would be fewer interconnects, higher reliability and greater component density. The disadvantages would be a greater degree of difficulty in failure analysis and limited usage because of power limitations.

Another approach would be to use hybrid circuits with beam lead diodes. Hybrid circuits offer a higher power dissipation capability. The use of beam lead parts would eliminate the problems of die bonding, and interconnect wire bonding. Beam lead parts have poorer transfer characteristics because of lower heat conduction of the beam leads.

Disadvantages with hybrid circuits are limited manufacturers and more process controls. These are not considered to be major disadvantages, but they should be a part of the decision to use, or not to use, hybrid circuits.

It is recommended that further study be conducted to determine if the "Ideal Diode" approach is an effective and practical means of selecting long life diodes. (Ref 5).

d. Hardware Life - The majority of diode failures occur as a result of defects during manufacturing and improper handling and application. A properly assembled and applied diode will not wear out.

Two environments that have the greatest impact on life are high temperature and temperature cycling. It is estimated that a junction temperature of +150°C would increase the life by an order of magnitude over a junction temperature of +200°C. The real effects of temperature cycling on life are unknown, but experience indicates that it is an effective technique to accelerate die and lead bond failures

e. Application Guidelines - Proper application of a part is as important as proper assembly and test. The purpose of all effort prior to application is to obtain the best part possible. Misapplication will tend to nullify that effort.

For proper application, considerations should be given to stud torque, mounting surface flatness, voltage and current ratings, junction temperature, derating of parameters that are known to drift with time or temperature, stress relief in leads or interconnecting wires, and mechanical stresses such as shock and vibration.

1) Stud Torque - Assure that the stud torque in the application does not exceed the rated value. It is advisable to keep it at a value below the rated value since the rating is based on what the threads will withstand. To exaggerate a point, any amount of torque will tend to cause stresses in the header material. These

stresses will be passed on to the semiconductor die where heating and cooling will amplify them. The difference in tensile stress on a 1/4-20 stud torqued to 15 inch pounds and one torqued to 12 inch pounds is approximately 2000 pounds per square inch. This additional stress could contribute to a shortened life for the part.

2) Mounting Surface Flatness - For good heat transfer to a heat sink, the flatness of the mounting surface should be equal to or better than that of the seating plane of the part. Uncontrolled mounting surfaces may also cause additional stresses to be transmitted to the semiconductor die.

Stud torque and mounting surface flatness are closely related factors. A flatter surface will have a lower thermal impedance for a given torque value. Conversely, a flatter surface will have the same thermal impedance for a lower torque value.

3) Voltage Ratings - The user must understand the voltage ratings and apply the part such that the voltages in the application do not exceed 50% of the Peak Inverse Voltage (PIV) rating of the part. PIV is the maximum allowable voltage, transients and all, that the part should be exposed to.

4) Current Ratings - Current ratings on manufacturer's data sheets are sometimes vague. There is no standard for specifying current ratings. Some ratings are based on a heat sink mounting. Others specify a current value, give a derating based on power and do not give forward voltage versus forward current data that is sufficient to apply proper derating. Current derating would seem to be the preferred method as the current is something the designer can realize.

The rms current rating determines power dissipation and is independent of temperature. In other words, regardless of case temperature, the rms current rating must not be exceeded. The rms current is not normally specified on manufacturer's data sheets. Currents usually specified are average rectified current $\left(I_o\right)$ based on 60 Hertz, sine wave, operation , DC forward current $\left(I_F\right)$, and surge current. Surge current ratings are usually given for both repetitive and non-repetitive conditions.

Maximum current through the diode should not exceed 50% of the rated value being considered. The derated value will reduce junction temperatures for the same ambient temperatures and will allow

for unforeseen surge currents.

5) Junction Temperature - Junction temperature is normally the limiting factor on how much current a diode can conduct. The life of a diode is related directly to the junction temperature. Herr and Fox (Ref 3) showed a reliability improvement of about 16 to 1 for junction temperatures of +100°C as compared to temperatures of +200°C. It is advisable to keep the junction temperature below 110°C for silicon.

In order to achieve the lower junction temperature T_j the derating curve must be adjusted to the desired T_j limit. The slope of the curve is the thermal impedance of the part and is fixed by the part design. Therefore, the slope of the derated curve has to be parallel to the slope of the manufacturer's derating curve. Often, the slope of the curve is changed to achieve the desired derating. When this is done, any derating that may occur is less than the percentage desired.

6) Parameter Derating - Derating applied to electrical characteristics is usually arbitrary with respect to life. There is little information available to show what degradation occurs with life. What is available may not be applicable to the parts being considered. Qualification data can be used to aid in the derating, but it is usually limited to 1000 hours.

Leakage currents will vary with temperature. However, they do not always follow the text book rule of doubling every 10°C. Evaluation test results should be used to establish leakage current variation with temperature for design use. Leakage current variation with life can vary from lot to lot in production. Practice has been to double the specification limit for an end of life design limit.

Forward voltage has proven to be stable with respect to life. Therefore, no derating is recommended.

There have been discussions about a drift occurring in reverse recovery time $\left(t_{rr}\right)$. There has been nothing documented to substantiate the t_{rr} stability. It is recommended that a drift of ten to 20 percent be allowed for unless the stability can be verified.

7) Stress Relief - It is important to allow for stress relief in leads or interconnecting wires to account for variations in lead length due to temperature changes or flexing of printed circuit boards. Stresses of this nature will damage glass-to-metal seals or cause fracturing of glass cases.

Stress relief in interconnecting wiring is necessary to prevent bending stresses on stud rectifier terminals which can result in damage of glass-to-metal seals. These terminals should not be used as terminal blocks, as shock or vibration coupled with the extra loading of multiple wires can result in damage of glass to metal seals. The appearance of the top terminals on stud rectifiers is deceiving. The terminal is hollow. Bending of this kind of terminal is more degrading to glass seals than is bending of solid terminals of the same size. It is advisable to utilize a terminal block for multiple wire connections rather than the terminal of a diode.

8) Shock and Vibration - For most applications, the parts can meet the shock and vibration levels. However, the levels to be encountered in the application are not always known, and for large power diodes, the rating may be exceeded. Levels may be such that failure does not occur at the time of exposure, but the part is weakened enough to cause a shortened life.

D. TEST METHODOLOGY AND REQUIREMENTS

1. Qualification Testing

The purpose of the qualification test is to determine if the part is capable of operating in the environment that it is to be exposed to in the application.

The tests should also be relevant to the kind of construction being tested; e.g., acceleration testing of a monolithic double slug diode is not a worthwhile test. A shock test would be more meaningful. Furthermore, data showing that the part is capable of passing the desired levels should be used. If process control is the concern, it should be verified by lot qualification.

The test sequence is important from the standpoint of detecting the effect of an environmental exposure; e.g., hermetic seal should be performed after a temperature cycling exposure rather than the reverse order to determine the effects of exposure to environments. Conventional qualification tests perform tests in parallel and as such do not determine the deleterious effect of one environment on the part's capability to withstand a different environmental exposure. For example, one group of parts is exposed to thermal shock while another group is exposed to mechanical shock. The part's ability to withstand both has not been determined. It is quite probable that the part will be exposed to both environments in the application. A more effective sequence is proposed in Figure 1.

Some of the tests shown in Figure 1 may not be applicable to all parts. The procedure should be modified to exclude those kinds of tests.

A possible modification could be made to the conventional thermal cycling test. This would be to put the parts in a cold chamber (-65°C) and force the rated current through the junction, to cause heating, until the part has stabilized. Then turn the current off until the part stabilizes at the ambient temperature. Repeat the cycle 1000 or more times. This kind of test would be more realistic of what the part would experience in the application with respect to thermal cycling. A test of this type would also require less handling because the parts would not have to be transferred between hot and cold chambers. Other temperature options could be used.

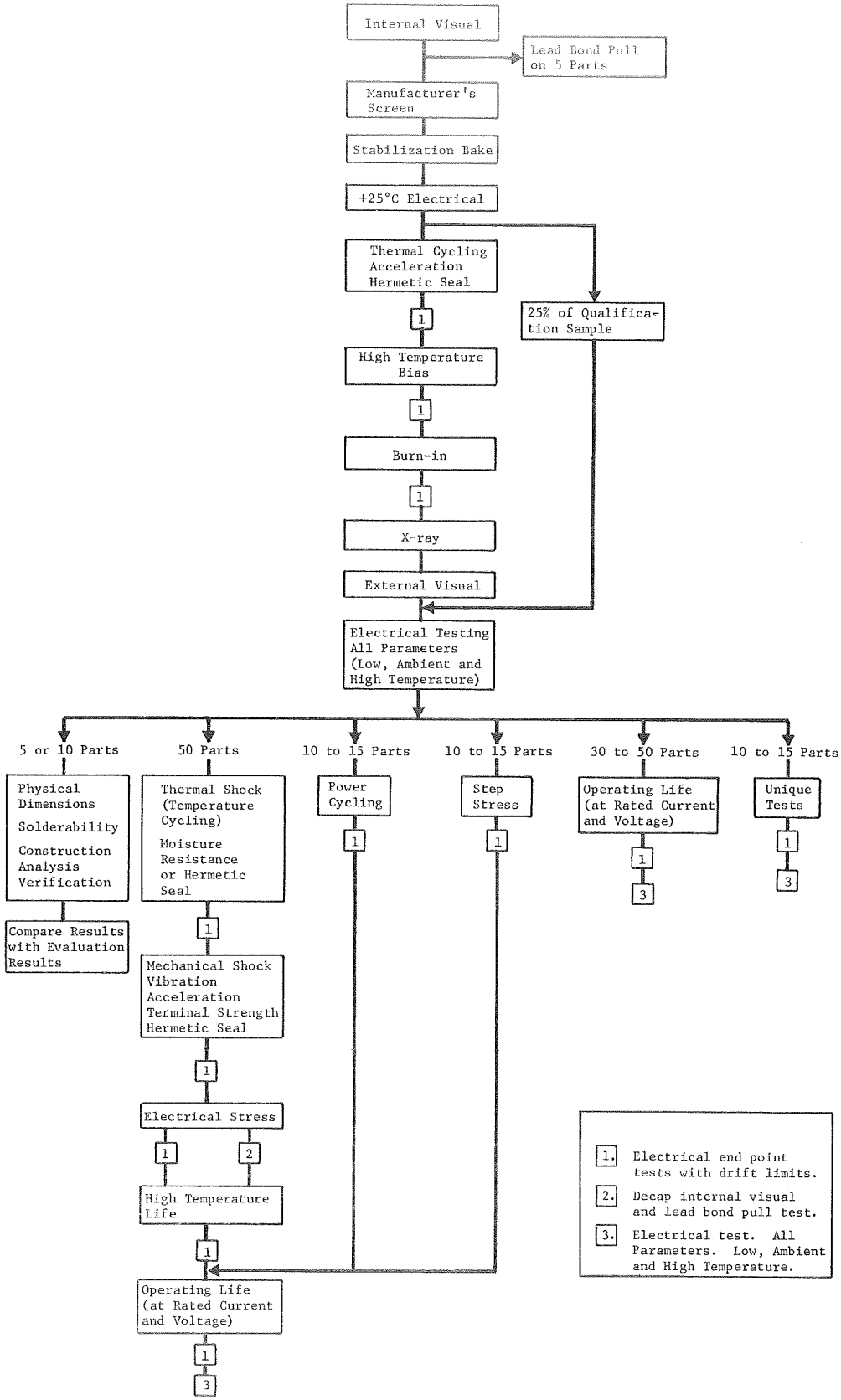

Figure 1 Qualification Test Sequence

The purpose of bypassing 25% of the qualification sample around a portion of the screen tests is to verify the effectiveness of the acceptance tests.

The qualification sample size is critical only from the standpoint of having enough parts to assure a meaningful distribution. Generally, any amount over 100 through a test or a series of tests would not yield any more information than the first 100. If the part evaluation has revealed potential problem areas, a larger sample size, larger than 10 or 15, could be subjected to those tests to give a higher confidence that the production parts will survive.

Electrical testing of all parameters should be performed before and after qualification to assure stability. End point tests of two or three quality indicating parameters is acceptable for in line tests. The testing of all parameters before and after is advised.

A construction analysis should be performed to verify that the qualification parts are similar to the evaluation parts. This will also aid in failure analysis activities.

The moisture resistance or hermetic seal test will have to be selected for optimum effectiveness in detecting non-hermetically sealed parts. The monolithic double slug parts have no cavity internally, so trying to force a tracer gas into the part for leak detection is not an effective test. A detergent pressure bomb test with an electrical drift test afterwards has proven to be an effective test. The pressure bomb test may be effective for cavity type parts when the cavity volume is small.

The serial arrangement of the thermal shock and mechanical shock is to stress bond interfaces thermally, then to test their integrity by a mechanical stress. The hermetic seal test afterward verifies the capability of the package to maintain a hermetic seal.

The terminal strength test is more effective if V_F is monitored during the test when testing non-monolithic double slug diodes.

The electrical stress is normally a current surge exposure. It could be a single surge or a combination of surges but should not exceed the rating of the part. If thermal or mechanical shock has degraded die or lead bonds, the surge current can cause heating that can crack the die or cause melting of contact materials.

High temperature life will reveal weaknesses in die and lead bonds. Contact resistance at the metal silicon interface will increase if a defective bond exists.

Operating life at rated current and voltage will verify part ratings. When performed in series with thermal, mechanical, and electrical stress, it will verify the part's ability to perform its intended function in the application. Comparison of test results from the series life test to the parallel life test will aid in determining the effects of the stresses on the life of the part.

Power cycling is performed to determine the ability of the part to operate in an on-off mode. This causes heating and cooling that stress the die and lead bonds. The cycle length can be determined empirically and is not critical. The prime concern is to have as large a temperature excursion as possible while heating the junction to its rated temperature. The number of cycles should be adequate to allow a prediction as to the total capability. Periodic testing of the quality indicator parameters is required for a meaningful prediction.

The step stress tests are performed to determine the margin between the part's ratings and its capability. This is important when derating for design.

The Unique Tests are performed to detect potential problem areas that are unique to a type of construction. For example, non-monolithic double slug parts should be subjected to a monitored thermal shock test to verify that intermittents will not occur during temperature excursions, and welded packages should be subjected to particle impact noise detection (PIND).

a. Accelerated Testing - Accelerated testing is beneficial in that it allows the tester to obtain results in a short period of time. Caution should be exercised so as to not induce failures because of the test conditions.

1) High Temperature Storage - This method is used to check contact and bond interface quality. Temperatures used should be established empirically to verify that failure modes due to the high temperature are known, considered, and are not allowed to influence the test results.

2) High Temperature Bias - This method is used to check surface problems such as inversion and accumulation. Bias levels should be 80% for voltage, 100% for current, and a temperature of +150°C.

3) Stress Testing - Step stress testing is a means to determine part capability and to accelerate failure mechanisms. The capability must be determined first or the step stress could introduce new failure mechanisms. The determination of capability is necessary for each part and each manufacturer.

2. Screen Tests (100%)

The purpose of the screen tests is to remove parts that do not meet the electrical and fundamental mechanical integrity requirements, and parts that have built-in defects and infant failures. Screen tests are performed on all parts and are usually a part of acceptance testing. Screen test all parts.

Screen tests could contribute to the effort of obtaining parts with long-life by screening out parts with a short life. The tests have to be designed with that in mind rather than what method is most convenient or economical. Many tests are performed on automated test equipment using pulsed forcing conditions and yielding digital outputs. Test techniques of this sort will not show soft or unstable breakdown characteristics.

Schenk (Reference 6) observed a phenomenon described as walkout. This occurred in some parts that had been exposed to a forward bias stress. Briefly, it is gradual stabilization in leakage current with a gradual increase in voltage. The leakage current will be low and stable up to a value of reverse voltage. Increasing the reverse voltage by a volt or two causes a temporary instability in leakage current. When the current stabilizes for a given voltage, it remains stable for voltages equal to or less than that voltage. Automated test equipment does not detect this kind of fault. It is detectable by viewing the characteristics on an oscilloscope.

It is possible that the breakdown voltage meets the specification value, as shown by automatic test equipment readout, but the part is unstable. If the part is used in a rectifying application, it may never fail because it becomes unstable only after a continuous voltage bias. The applied voltage on the rectifier is such that it will keep the fault from developing to the failure stage.

Walsh (Reference 5) suggests an "Ideal Part" approach to screening. Fundamentally, it involves establishment of ideal characteristics from theoretical and empirical data, selecting levels of voltage, temperature, and current that are most likely to indicate the presence of extraneous series, parallel or changing charge conduction mechanisms, performing evaluation tests to determine the level and rates of change of the conductivity constants of the various charge generation and transport mechanisms, and comparing parts to these values. Parts that compare to the ideal curve have proven to remain stable for 2500 hours. Parts that do not conform to the ideal curve show degradation and failure during the 2500 hour life test. The test results show enough consistency to warrant further study.

A suggested screen test sequence is shown in Figure 2. Test details should be modified to the part being screened. For example, no acceleration on double slug diodes, high temperature bias for silicon controlled rectifiers may be dropped, and the burn-in modified to be an AC blocking voltage exposure. A discussion of each screen test follows.

a. Internal Visual Inspection - The purpose of this test is to detect contamination, misplaced bonds or whiskers, scratches in metallization, sagging or missing internal leads, cracked die, etc. This inspection may be performed before or after the package sealing operation depending on the package construction. A wafer or die inspection prior to assembly would eliminate some of the defects found at the assembly level.

Internal visual inspection of some monolithic double slug parts is impossible in that the package is opaque. Defects that the internal visual inspection were meant to detect are eliminated by this method of construction.

b. Stabilization Bake - This step is inserted to do what the name implies, stabilize the part, primarily the junction. The shortness of the exposure does not allow much else to happen. It is possible that it may tend to accelerate defects in the die and lead bonds.

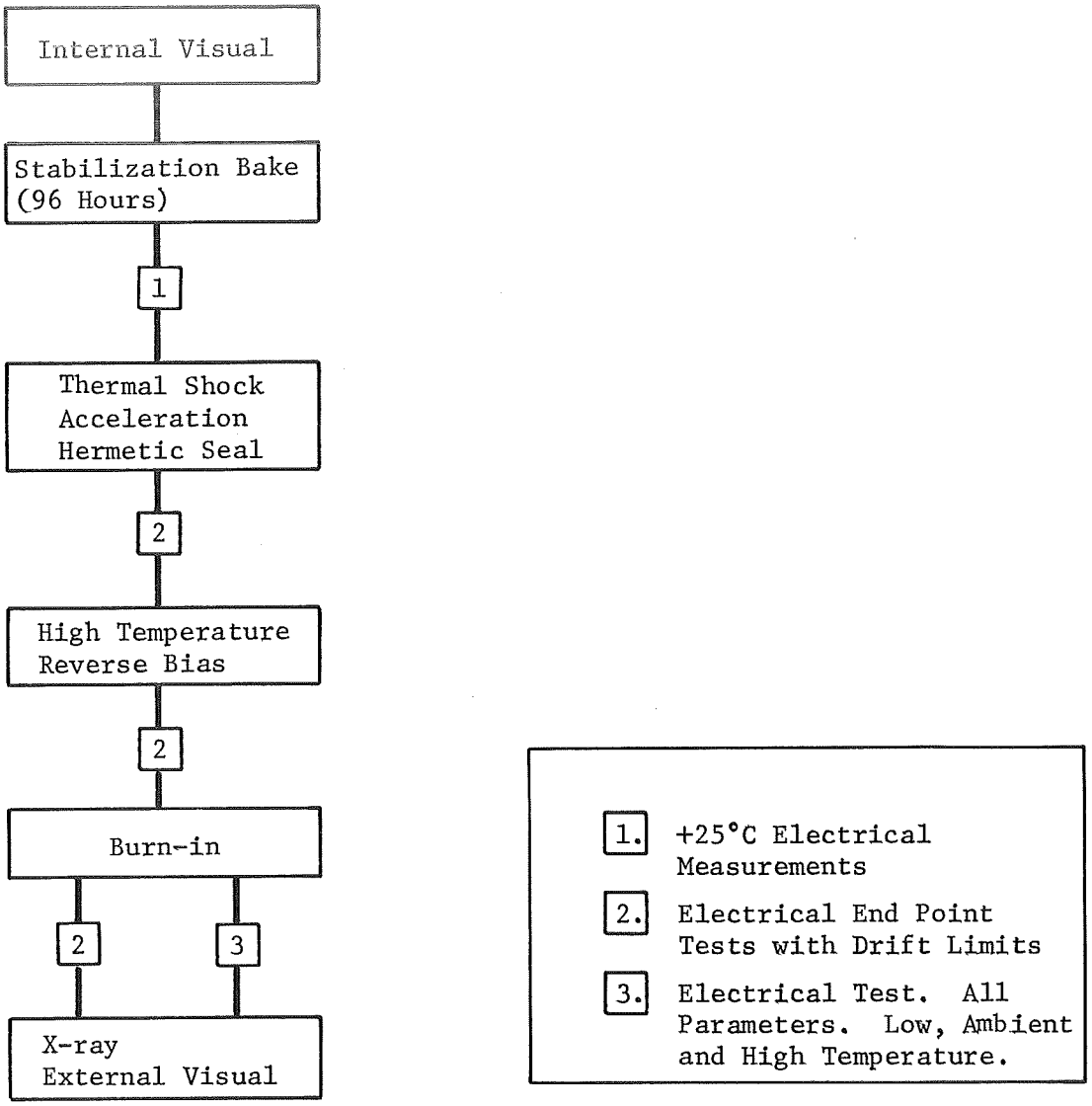

Figure 2 Screen Test Sequence

c. Thermal Shock - Military specifications; e.g. MIL-STD-750, attach the term "Thermal Shock" to two tests. One is a hot liquid/cold liquid exposure. The other is a cold chamber/hot chamber with a gas ambient (usually air) exposure.

The liquid test is considered to be more severe because of the rapid change in temperature that causes larger temperature differentials, and is the recommended test for detecting mechanical defects. The liquid used is normally water, which tends to limit the temperature excursion to 100°C compared to about 250°C for air.

Some parts are capable of exposure to liquid nitrogen (-195°C) with immediate transfer to boiling water (+100°C) and back to the liquid nitrogen without damage. This exposure is severe because of the temperature differentials encountered.

The purpose of the thermal shock is to detect poor glass-to-metal seals, poor die bonds, or cracked dice.

d. Constant Acceleration - The purpose of this test is to detect weak contacts or bonds. It is effective for whisker type parts only. Acceleration testing of double slug parts, monolithic or otherwise, cannot be considered a wasted effort, but there are better tests to perform for the money and time.

e. Hermetic Seal - This test should be performed after thermal shock so as to detect defective seals caused by the thermal shock. The actual technique of detecting the defects is dependent on the package construction. Tracer gas is effective for cavity type parts. A detergent bomb test is preferred for non-cavity or small cavity parts. (A DO-35 package is considered a small cavity.)

f. High Temperature Bias - The purpose of this test is to detect surface contamination defects. On planar construction, a reverse bias can cause an inversion and a forward bias can cause an accumulation (Reference 3). Both of the phenomena are detected by soft breakdown and an increase in leakage current. An oscilloscope display would be an effective way of detecting parts that have inversion or accumulation defects. The display would reveal the soft breakdown and instability in the breakdown region. Instability of the breakdown voltage or increases in leakage current would be indicative of potential problems that could cause a shortened life.

The high temperature bias test is most effective on the planar construction. Its worth on the mesa type construction has been questioned. The data on previous lots that have been subjected to the bias should be reviewed to determine the effectiveness of the test. If it detects defective parts, it should be retained. The burn-in may have detected the same defective parts. If so, a redundant test is being performed.

Manufacturers of silicon controlled rectifiers are of differing opinions on the effectiveness of the high temperature bias. Some use it, others claim that an ac blocking voltage exposure is more effective. It would seem that further study in this area is needed.

g. Burn-In - The purpose of the burn-in is to simulate actual operation conditions to eliminate infant failures. There are arguments for ac burn-in and there are arguments for dc burn-in. If the application is known, the burn-in should be structured toward simulation. Otherwise, rectifiers should have an ac burn-in and parts used as diodes (dc or blocking applications) should have a dc burn-in. If the application is not known, it is recommended that a dc burn-in be performed. A 100% burn-in is recommended

Whichever technique is used, the junction temperature should be close to the rated value. This could be achieved by a high ambient temperature and a low current or a low ambient temperature and a high current. The high current is the preferred approach because it will be more likely to detect weaknesses in the junction, lead bonds, or die bonds than a low current.

h. Radiographic Inspection - This inspection will supplement the internal visual inspection or, if an internal visual inspection could not be performed, it will take the place of it.

Defects that it can detect are weld splatter, extraneous lead material, voids under the die, whisker or lead deformation, misalignment of heat sinks, and whiskers.

X-ray inspection on some parts may be ineffective because of the case material. Some glass case parts use glass that contains lead. X-rays on these parts yield only a good silhouette. X-ray of stud rectifiers are more effective if they are taken on an angle to the stud.

i. External Visual Inspection - This inspection will remove parts that have defective leads (e.g., corroded, bent or scratched), deformed cases, and poor markings.

3. Parameter Drift Detection

Parameter drift detection is accomplished by applying a drift limit to a critical parameter, measuring that parameter, exposing the part to a particular environment (e.g., burn-in), remeasuring the parameter, and comparing the two values. Any difference between the two values will indicate that a change has occurred, but it does not indicate when the change took place. It is possible that a parameter may drift at a point in time early during the exposure and then remain stable during the remainder of the exposure time. The drift may have exceeded the allowed limit and as such is rejected as an unstable part.

Zierdt (Reference 7) discusses a possible fault with drift limits. The argument is that the parts may have an inherent offset tendency in the measured characteristics. The effect itself may be larger than a characteristic drift. If the offset magnitude is not considered in establishing the drift limits, good parts may be rejected. It is also noted that parts may drift initially and then stabilize. Unless intermediate measurements are made, the stabilization will go undetected, the drift will be noticed and the part rejected. Care should be taken to make certain that an attempt is made to verify part stability.

The drift limit may be established by the mission and part requirements. Missions that are long-term should use parts that exhibit the most stability. The limit should be based on life test results. There must be a correlation between drift limits and stability during life tests.

The quality indicator parameters used depend on the kind of part. Diodes and rectifiers traditionally use reverse current and forward voltage drop. Zeners use reverse current and breakdown voltage. Reverse current is considered to be the best quality indicator parameter.

Some manufacturers use a scope display of the breakdown voltage to determine stability. The scope display is a time consuming test that has to be performed manually. As such, it is not performed by many manufacturers, but is a good test to select stable parts.

It is recommended that additional studies be performed to determine if the "Ideal Diode" screening technique could be developed and used to select long-life parts. The results of the study by Walsh (Reference 5) indicate that his approach is sound.

4. Failure Mode Detection

Internal visual inspection will aid in detection of some of the mechanisms shown in Table 1. However, some diodes do not lend themselves to an internal visual inspection. Of these, some may be inspected for certain mechanisms during the manufacturer's fabrication processes.

Others, such as some monolithic double slug types, do not lend themselves to an internal visual inspection. These parts were designed to eliminate the kinds of problems that an internal visual inspection detected. Electrical test and x-ray are tests that will detect remaining failure mechanisms.

Internal visual inspection may or may not be an effective failure mechanism detector. The user of the part must make that judgment and act accordingly.

E. PROCESS CONTROL REQUIREMENTS

Most defects caused by lack of control will be detected during normal screening procedures. The defects that are not detected will be those that are time dependent such as corrosion due to chemicals that have not been cleaned off the die, lead bonds that are good enough to endure screen testing, but weak enough to cause early life failure, and cracks in the die that propagate due to temperature cycling caused by on and off operation. Because these defects cannot be detected during testing and can affect the part life, they are considered to be the critical processes.

Scanning Oscillator Techniques (SOT) should be used as a means of in-line process control for detecting dislocations in the silicon (Ref 2).

This SOT is based on diagnostic X-ray charts. These charts are obtained through correlation of SOT topograph and final device yield maps. The topographs are recorded through the use of the scanning oscillator technique of x-ray diffraction microscopy. The technique is nondestructive. Use of the SOT as an in-line control will also help to determine where, in the process flow, problems are occurring.

It is recommended that the use of the SOT as a means of rejecting dice be investigated. Dice with dislocation defects could be removed at the time the wafer is broken up into dice.

A review of the manufacturer's records and data should be performed to determine if he has process control. The data could be that compiled at in-line check points. If the data shows increasing or stable yields, the processes in question are being controlled effectively.

Lot to lot test data for parts is another means of detecting process control effectiveness. Decreasing or stable reject rates would be indicative of effective process control.

The manufacturer should have in-line check points to verify process control. Electrical wafer probing and lead bond pull tests are examples of check points. Results of these checks would aid in early detection of process problems.

F. PARTS LIST

1. Acceptable Parts

The parts shown in Table 8 are parts that have been used on space programs at Martin Marietta Corporation and other manufacturers of space hardware. The parts have sufficient history to demonstrate the soundness of their design. They have been in production long enough to have achieved a high degree of process maturity, while also maintaining a popularity that will tend to assure long-term production.

The section on Selection Criteria in this chapter must be considered when using this, or any other list. The presence of a JEDEC or commercial number from this list on a part does not necessarily put it in the category of a high reliability part. The manufacturer and part evaluation results should be the major determining factor.

Table 8 Recommended Parts List Diodes

Application	Description	Parameters							Commercial Part Number
		P_D (Watts)	BV_Z ±5 PCT (Volts)	I_{ZT} (MA)	Z_Z (Ohms)	T.C. (PCT/°C)	I_{ZM} (MA)	T_j MAX (°C)	
Regulator Diode General Purpose	Semiconductor Device, Diode, Zener, 400 MW	.4	3.3	20	26	-.052/-.087	120	-65 to +175	IN3506
			3.6	20	23	-.045/-.078	110		IN3507
			3.9	20	22	-.040/-.067	100		IN3508
			4.3	20	19	-.030/-.060	90		IN3509
			4.7	20	17	-.010/-.050	85		IN3510
			5.1	20	15	+.015/-.030	75		IN3511
			5.6	20	8.5	+.009/+.035	70		IN3512
			6.2	20	4.0	+.010/+.047	65		IN3513
			6.8	20	4.3	+.024/+.055	60		IN3514
			7.5	10	5.0	+.028/+.059	50		IN3515
			8.2	10	6.0	+.030/+.065	45		IN3516
			9.1	10	7.5	+.030/+.068	40		IN3517
			10	10	8.5	+.054/+.075	38		IN3518
			11	10	12	+.058/+.080	35		IN3519
			12	10	13	+.060/+.087	32		IN3520
	Semiconductor Device, Diode, Zener, 1 W	1.0	3.3	76	10	-.075	276	-65 to +175	IN3821A
			3.9	64	9	-.060	238		IN3823A
			4.7	53	8	±.025	194		IN3825A
			5.6	45	5	+.040	162		IN3827A
			6.8	37	3.5	+.057	140		IN3016B
			8.2	31	4.5	+.065	115		IN3018B
			10.0	25	7.0	+.071	95		IN3020B
			12	21	9.0	+.076	80		IN3022B
			15	17	14	+.082	63		IN3024B
			18	14	20	+.085	52		IN3026B
			22	11.5	23	+.087	43		IN3028B
			27	9.5	35	+.090	34		IN3030B
	Semiconductor Device, Diode, Zener, 5 W	5.0	6.8	175	1	.05	700	-65 to +175	IN4954
			8.2	150	1.5	.06	580		IN4956
			10.0	125	2.0	.07	475		IN4958
			12.0	100	2.5	.07	395		IN4960
			15.0	75	3.5	.08	315		IN4962
			18.0	65	4.0	.085	264		IN4964
			22.0	50	5.0	.085	216		IN4966
			27.0	50	6.0	.09	176		IN4968
			33.0	40	10.0	.095	144		IN4970
			39.0	30	14.0	.095	122		IN4972
			47.0	25	25.0	.095	100		IN4974
			56.0	20	35.0	.095	84		IN4976
			68.0	20	50.0	.100	70		IN4978
Regulator Diode General Purpose	Semiconductor Device, Diode, Zener, 10 W	10	6.8	370	1.2	+.057	1500	-65 to +175	IN2970B
			8.2	305	1.5	+.065	1180		IN2972B
			10.0	250	3.0	+.071	980		IN2974B
			12.0	210	3.0	+.076	820		IN2976B
			15.0	170	3.0	+.082	640		IN2979B
			18.0	140	4.0	+.085	525		IN2982B
			22.0	115	5.0	+.087	435		IN2985B
			27.0	95	7.0	+.090	340		IN2988B
			33.0	75	9.0	+.092	300		IN2990B
			39.0	65	11.0	+.094	240		IN2992B
			47.0	55	14.0	+.095	200		IN2995B
			56.0	45	16.0	+.096	170		IN2999B
			68.0	37	18.0	+.097	137		IN3001B
			82.0	30	25.0	+.098	115		IN3003B
			100.0	25	40.0	+.110	91		IN3005B
			120.0	20	75.0	+.110	77		IN3008B
			150.0	17	175.0	+.110	62		IN3011B
			180.0	14	260.0	+.110	52		IN3014B
	Semiconductor Device, Diode, Zener, 400 MW	.4	15	8.5	16	+.082	26	-65 to +175	IN965B
			18	7.0	21	+.085	21		IN967B
			22	5.6	29	+.087	17		IN969B
			27	4.6	41	+.090	14		IN971B
			33	3.8	58	+.092	12		IN973B
			39	3.2	80	+.094	9.1		IN975B
			47	2.7	105	+.095	7.9		IN977B
			56	2.2	150	+.096	6.9		IN979B
			68	1.8	230	+.097	5.5		IN981B
			82	1.5	330	+.098	4.6		IN983B
			100	1.3	500	+.110	3.7		IN985B

Table 8 (cont)

Application	Description	Parameters							Commercial Part Number
		P_D (Watts) MAX	BV_Z ±5 PCT (Volts)	I_{ZT} (MA)	Z_Z (OHMS)	T.C. (PCT/°C)	I_{ZM} (MA)	T_J MAX (°C)	
Temperature Compensated Reference Diode	Semiconductor Device, Diode T.C. Reference Diode	250 MW	6.2	7.5	15	.001 -55 to +100		-65 to +175	IN827
	Semiconductor Device, Diode T.C. Reference Diode	500 MW	9.0	7.5	20	.001 -55 to +150		-65 to +175	IN938B
	Semiconductor Device Diode T.C. Reference Diode	500 MW	11.7	7.5	30	.001 -55 to +150		-65 to +175	IN944B

Application	Description	P_D (MW)	BV (Volts)	I_R AT +25°C NA / +150°C UA	V_F AT I_F (Volts)	I_F (MA)	$I_R = \frac{T_{RR}}{I_F \text{ at } X \text{ MA}}$	C_O (PF)	I_F MAX (MA)	T_J MAX (°C)	Commercial Part Number
Switching											
High Speed High Conductance	Semiconductor Device, Diode Silicon, Computer	500	100	25 / 50 V_R = 75	1.0	10	4 NS / 10 MA	4.0	400	-65 to +175	IN4148
Low Leakage, Controlled V_F (1-200 MA)	Semiconductor Device, Diode Silicon, Computer	500	150	1.0 / 3.0 V_R = 125 V	.52-.68 . 6-.75 .74-.88 .83-1.0	1 5 50 200	3 US / 10 MA	8.0	200	-65 to +150	IN3595
High Conductance High Speed High Breakdown	Semiconductor Device, Diode Silicon, Computer	250	200	100 / 100 V_R = 175 V	1.0	100	50 NS / 30 MA	5.0	220	-65 to +175	IN4938
Controlled V_F (1-200 MA) High Speed	Semiconductor Device, Diode Silicon, Computer	500	75	100 / 100 V_R = 50 V	.54-.62 .66-.74 .82-.92 .87-1.0	1.0 10 100 200	4 NS / 10 to 200 MA	2.5	400	-65 to +200	IN4150
Controlled V_F (.1-20 MA) High Speed	Semiconductor Device, Diode Silicon, Computer	500	75	50 / 50 V_R = 50 V	.49-.55 .59-.67 .70-.81 .74-.88	.1 1.0 10 20	4 NS / 10 MA	2.0	400	-65 to +200	IN4153

Application	Description	V_R Volts Peak	$V_{RM(WKG)}$ Volts Peak	I_O AT T_A Amp	°C	I_R MAX AT +25°C UA / +150°C MA	V_FMAX AT I_F Volts	Amp	T_{RR} NS	T_J MAX °C	Commercial Part Number
Rectifier Fast Recovery	Semiconductor Device, Diode, Silicon Fast Recovery, Stud	400	400	12	100	25 / 3	1.5 V (PK)	38 A (PK)	200 MAX	-65 to +150	IN3893
Fast Recovery	Semiconductor Device, Diode, Silicon Fast Recovery, Axial Lead	600	600	1.0	55	1.2 / 0.2	.6-1.3	1.0	150 MAX	-65 to +175	IN4946
Fast Recovery	Semiconductor Device, Diode, Silicon Fast Recovery, Axial Lead	400	400	3.0	55	1.0 / 20 UA AT +100°C	.6-1.3	3.0	150 MAX	-65 to +175	IN5418

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VI. TANTALUM CAPACITORS

by R. A. Homan

VI. TANTALUM CAPACITORS

A. INTRODUCTION

This chapter discusses the following types of tantalum capacitors:

1. Solid Electrolyte, Sintered Slug
2. Wet Electrolyte, Foil
    a. Plain Foil
    b. Etched Foil
3. Wet Electrolyte, Sintered Slug

Tantalum electrolytic capacitors provide large values of capacitance per unit volume, but they are less reliable than other types. For example, Reference 1 reports that six tantalum capacitor failures occurred in the Mariner Venus 67 spacecraft program. The total capacitor usage was 4622 parts of which 1301 were tantalums. No failures occurred in the other capacitor types.

The construction of each of the tantalum capacitor types is reviewed and an analysis of the associated failure mechanisms is made. From these considerations, and an industry survey, guidelines are derived for design criteria, process control, test, and application requirements which will enhance their reliability.

B. GUIDELINES FOR LONG-LIFE ASSURANCE

The life expectancy of properly constructed, tested, and applied tantalum foil and solid electrolyte capacitors is in excess of 100,000 hours. The quality of these parts is due largely to good control of critical materials and complex processes. However, many failures have occurred from errors such as lead welding, slug soldering, insulation sleeve defects, etc. The wet slug tantalum capacitor is not recommended for long-life applications at this time. The preferred choice for long-life applications is the solid electrolyte capacitor. Wet slug capacitors should be permitted only if their use has been specifically justified. When used, the electronic packaging design should permit their replacement without damage to other parts.

The guidelines presented herein will enable use of tantalum capacitors with minimum probability of defects and maximum service life. Guidelines for wet electrolyte slug capacitors have been included even though the solid electrolyte slug capacitor is the preferred choice for long-life applications.

1. Design Guidelines

1) Use only hermetically sealed capacitors to provide maximum stability and reliability, and prevent outgassing during low pressure operations.

2) For foil and wet slug capacitors, the leads should be welded to anodized tantalum risers external to the hermetic seal so as to provide a completely insulated structure within the seal.

3) The tantalum riser wires should not extend more than 1/4 inch beyond the seal to minimize the possibility of bending and therefore damaging the riser and its oxide, particularly at the seal area.

4) The cathode lead of wet slug capacitors in silver cans should be of a material which is weldable to silver without causing crystallization or punch-through. For this purpose, silver or oxygen free copper is superior to other materials such as nickel.

5) Gelled electrolyte is preferred over liquid sulfuric acid electrolyte in wet slug capacitors because of lesser mobility.

6) The proper high temperature solder must be used in fabrication to prevent reflow during assembly operations.

7) The attachment of slugs into solid electrolyte capacitor cases must utilize silver bearing solder to prevent silver paint dissolving into the solder.

8) Plain foil capacitors are preferred over the etched foil, since the etched foil is somewhat more prone to manufacturing process errors.

2. Process Control Guidelines

In general it is not necessary nor desirable for the user to control the processes of the tantalum capacitor manufacturer. Variations in processes, equally successful and equally proprietary, exist. Each manufacturer, however, must have his particular processes under strict control. The lack of control will usually be reflected in wide product variations and poor yield. As a guideline, however, the user should not wait for these effects to manifest themselves, but should obtain maximum supplier cooperation and monitor him as closely and continuously as possible.

3. Test Guidelines

1) Tantalum capacitors should be qualified to the requirements of MIL-C-39003 or MIL-C-39006 level P, as a minimum. Additional program-peculiar requirements should be added as required.

2) Radiographic inspection on 100% of the devices should be made in accordance with more comprehensive inspection criteria such as in MSFC-STD-355 to detect anomalies more effectively.

3) Burn-in should be increased to a minimum of 240 hours at rated voltage at 85°C with tight delta limit criteria. Stability is an indication of reliability and present durations are not sufficiently long to detect all parts with instabilities. Read and record measurements of capacitance, dissipation factor, and leakage should be made before and after burn-in on 100% of the devices.

4) Seal test should be performed on 100% of the devices to verify every seal. In addition, if acid electrolyte is used, a litmus paper or thymol blue test should be added to the usual leak test.

5) Accelerated tests are applicable to solid tantalum capacitors. Caution is required in applying these techniques to foil or wet slug capacitors as electrolyte breakdown may occur at relatively low voltages creating a new failure mechanism.

4. Application Guidelines

1) For highest reliability, polar capacitors should be applied so that voltage reversal never occurs, including the conditions of combined ac and dc voltage.

2) When capacitors are used in series, balancing resistors should be used to assure proper division of voltage.

3) When capacitors are used in banks, they should be assembled in easily removable modules to facilitate replacement and test.

4) Solid electrolyte capacitors should be applied with a limiting series resistor of 3 ohms per volt minimum so that scintillation effects do not precipitate catastrophic breakdown.

5) When solid electrolyte capacitors are used in banks, the series limiting resistor should be installed with each capacitor to prevent discharge of the entire bank into a scintillation fault.

6) The ripple current in all capacitors should be limited to values which do not bring the temperature above the derated rating. When capacitors are used in banks it is cautioned that the capacitor with lowest ESR will carry the largest ripple current.

7) The largest possible case size should be used for a given capacitor voltage rating as this provides thicker oxide dielectric, lower ESR, lower dissipation factor, better heat dissipation, and greater capacitance stability.

8) To minimize silver particle generation, the ripple current for wet slug capacitors should be derated as follows:

   T_1 Case Size - 35 ma RMS

   T_2 Case Size - 120 ma RMS

   T_3 Case Size - 300 ma RMS

9) For long life high reliability usage, the peak voltage including surges and transients should be limited to 50% of the manufacturer's derated ratings for all tantalum capacitors.

10) For foil and solid electrolyte capacitors, the allowable ripple current should be derated to 70% of the manufacturer's derated rating for high reliability.

11) The temperature of solid electrolyte capacitors should be limited to 50°C including internal temperature rise. For long life, the foil and wet slug types should be held to 70°C.

5. Special Considerations

1) When purchasing tantalum capacitors, the lowest failure level available should be used.

2) Flight hardware should use the freshest product available to avoid degradation that may have occurred during shelf life and to take advantage of improved processes and techniques.

3) Whenever wet slug capacitors are used, they should be operated a minimum of 240 hours in the actual use condition. Dissection should then be made and the device observed for silver deposits on the anode and cathode. Evidence indicates that ripple current can plate and deplate silver.

4) Select parts with high volume continuous production and acceptable past history with no likelihood of product line obsolescence to obtain products with maturity.

5) For highest assurance, reject all parts with absolute or delta parameter outlier values. Analyze parameter delta shift data and use only the most stable parts in flight hardware. Perform litmus or thymol blue test on parts containing acid just prior to installation in assembly.

6) Avoid non-standard sizes, ratings, and lead materials to avoid risks associated with manufacturer's lack of experience with such parts.

C. LIFE LIMITING PROBLEMS AND SOLUTIONS

1. Failure Mechanism Analysis

a. Construction Features - The heart of the sintered tantalum capacitor is a porous tantalum anode fabricated by forming small particles of high purity tantalum into a compact mass and then sintering at high temperature under a vacuum. Camphor, stearic acid, or similar organic compounds are added to the powder prior to pressing into pellets of the desired shape in a die (Reference 2). The problem is to fabricate a porous tantalum body of high purity, uniform porosity, optimal density, high volume efficiency, and high mechanical strength. The binders are driven off during a part of the sintering operation known as the pre-sintering step. Both sintering and pre-sintering are batch processes with cycle times of about 4 to 10 hours. Sintering temperatures are approximately 2000°C. The sintering process yields a porous pellet which has a large surface area relative to its volume. The volumetric efficiency is dependent on the size of tantalum powder used in forming the pellet, typical pores having diameters on the order of 10 microns, with lengths as much as 1/8 inch. Typical surface area achieved is from 110 to 200 cm^2 per gram. (Reference 3).

The porous tantalum pellet is then anodized to form the dielectric Ta_2O_5 film which is the active part of the anode capacitance. The electrochemical oxidation of the pellet is performed in an anodizing solution such as phosphoric acid. A current is passed between the tantalum anode and a suitable cathode material in the acid solution. The current is kept constant as shown in Figure 1, while the voltage is increased. This is necessary because the amorphous Ta_2O_5 is growing on the pellet. At a predetermined voltage (called the forming voltage) the voltage is held constant while the current decreases due to the oxide thickness approaching a limiting value proportional to the forming voltage used. The forming voltage is typically between four and eight times the voltage rating of the finished capacitor.

To complete the capacitor, a contact must be made to the oxide. The two contact methods used are wet electrolyte and solid electrolyte, which is the derivation of the terms for these capacitors.

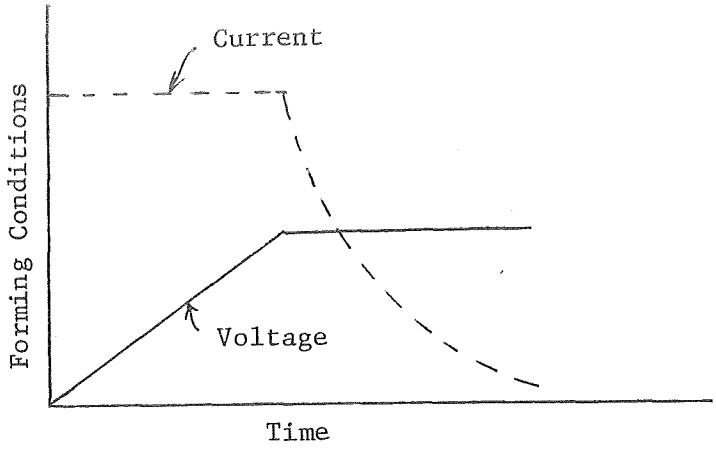

Figure 1 Anodization Curves

The terms wet-slug and solid-slug distinguish the type of electrolyte used in sintered tantalum capacitors. The porous anode structure imposes a limitation in that the cathode surface cannot be brought in close proximity with the anode surface such as in conventional wound foil capacitors. The cathode area is restricted severely because it cannot conveniently exceed the outer surface of the anode. Also, the electrolyte must have low resistivity because the resistance of electrolyte in the pores is in series with the capacitor, adversely affecting the power factor. The most suitable electrolyte in common use for wet slug capacitors is 30-40% sulfuric acid solution. It may be in a liquid or gelled form. This electrolyte has an acceptable temperaure coefficient of resistance to -55°C and can be operated at 125°C in a pure silver container. The container is the cathode and the sulfuric acid solution is the conductor between the tantalum oxide surface and the silver cathode. The capacitance of a wet slug electrolytic capacitor is not determined entirely by the area and thickness of the Ta_2O_5 dielectric and its dielectric constant. This is due primarily to the capacitance of the cathode which acts in series with the anode capacitance. This capacitance is polarization capacitance due to a Helmholtz double layer at the cathode surface. This double layer consists of space charge created by a layer of ions absorbed on the silver surface and an oppositely charged layer in the electrolyte interface separated by a distance of a few angstroms. This small charge layer separation results in capacitance on the order of 10 microfarads per cm^2 of surface for silver in sulfuric acid (Reference 3). This capacitance is a function of the metal and the electrolyte. As it is desirable to have

infinite cathode capacitance, the interior of the silver case is usually treated (such as platinizing) to increase this capacitance. A great deal of effort has been made in determing combinations which have the highest capacitance per unit cathode area. Any chemical or electrochemical reactions between the electrolyte and cathode usually lead to the formation of dielectric films that greatly reduce the polarization capacitance and give rise to aging effects in the capacitor. The polarization capacitance decreases with frequency and accounts for the poor frequency characteristics of wet tantalum capacitors. The poor low temperature characteristic is due to decrease in the polarization capacitance and the large increase in electrolyte resistivity.

Figure 2 shows one type of construction of a hermetically sealed wet slug tantalum capacitor. The elastomer support pads are used to isolate the anode from the case and provide support as an anti-vibration spacer. The solder should be high temperature solder so that reflow does not occur due to assembly operations in circuit fabrication. In other designs, an eyelet is provided in the header and the lead weld is buried in the eyelet as opposed to being external to the case. Some designs provide a crimp in the can over the top elastomer pad to minimize capillary action and confine the electrolyte to the slug area. Theoretically there should be no chemical degradation of the device. However, the possibility of impurities being in the electrolyte or other materials always exists, as well as defects caused by handling, welding, sealing, etc. The electrolyte does not dissolve the tantalum oxide.

The resistance of the tantalum oxide-electrolyte interface is very low in the reverse direction. The permissible reverse voltage is theoretically determined by the potential required to cause an evolution of hydrogen at the silver cathode. With sulfuric acid electrolyte and a silver cathode, the reverse voltage is thus theoretically limited to about 1.2 volts. However, any reverse current in this type of capacitor will cause silver ions in the electrolyte to plate out on the anode slug. This plating is preferential at high conductivity sites (defects) on the oxide. As silver does not anodize, the high conductivity sites remain so and may cause a short between the tantalum and the electrolyte. With forward voltage applied at all times, high conductivity sites have a tendency to heal themselves. The mechanism of self-healing is electrolysis in much the same manner in which the capacitors were originally formed. Any fractures or weak spots in the oxide (if not catastrophic) would heal themselves by reforming with applied voltage. This also occurs in the phenomenon known as "scintillation" or "flicker." The oxide breaks down suddenly under

voltage stress, a high current flows momentarily, the breakdown site is self-healed. However, even when there is no breakdown, electrolysis is continuously in operation and weak spots in the oxide are in a dynamic state of repair. As a result, the leakage current at constant voltage gradually decreases in time. This action operates only under voltage application. When wet slug capacitors are dormant, the oxygen accumulated is diffused away and leakage currents will increase.

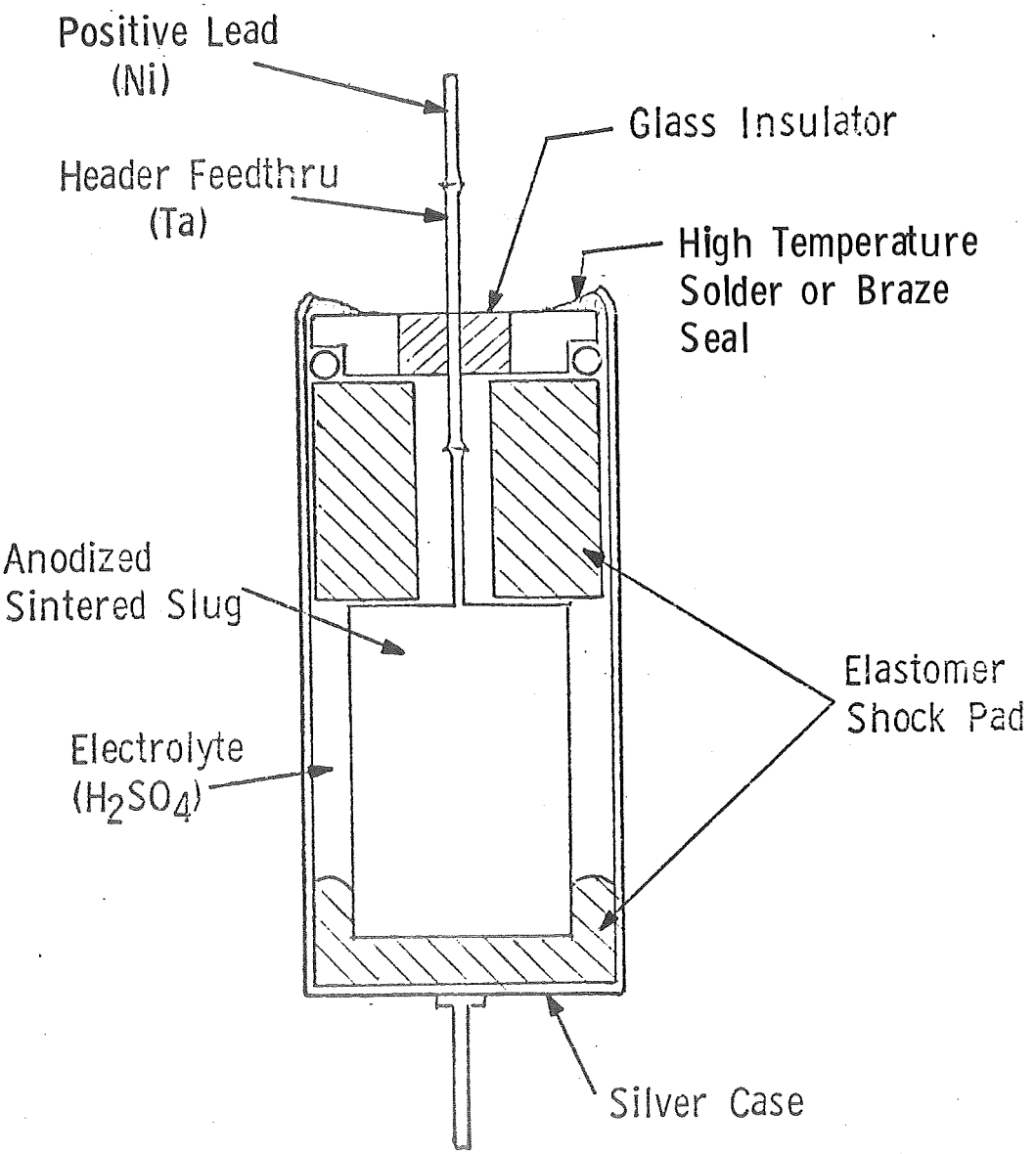

Figure 2 Wet Slug Tantalum Capacitor

Figure 3 shows the typical construction features of a hermetically sealed solid slug capacitor. The basic sintering and anodizing processes are similar to the wet slug capacitor except that the safety margin between forming voltage and working voltage is usually greater in the solid slug capacitor. Because of the generally thicker oxide film and the difficulty in assuring full impregnation of the porous slug with the solid electrolyte, the volumetric efficiency of solid electrolyte capacitors is not as high as the wet slug. However, the solid electrolyte capacitor does not have the problem of sealing a liquid electrolyte and also exhibits improved performance characteristics, particularly at low temperatures. Semiconducting oxides, such as PbO_2, MnO_2, and NiO have been used, with manganese dioxide in common use today. This electrolyte has a low resistivity and can be produced readily from decomposition of manganese salts. The MnO_2 is produced *in situ* in the pores of the anode because it cannot be manufactured in a liquid form.

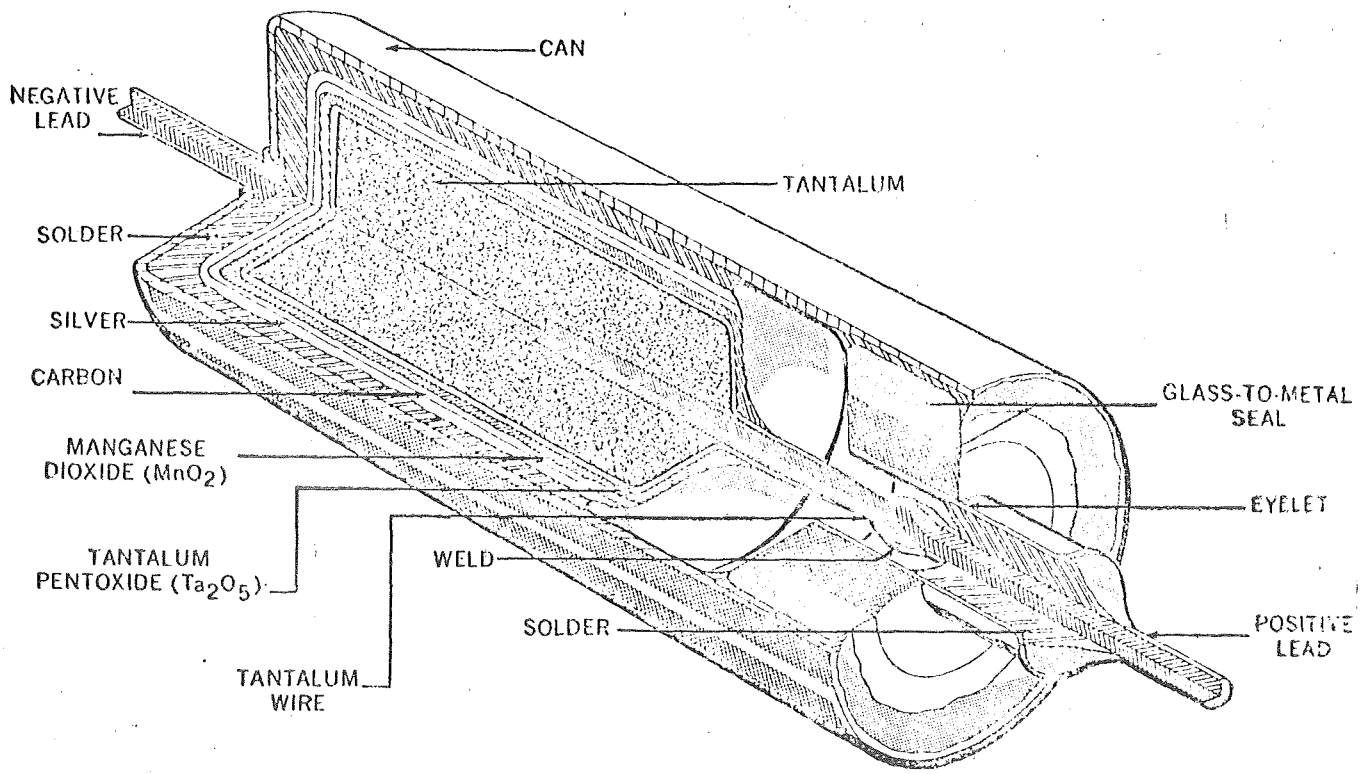

Figure 3 Solid Slug Tantalum Capacitor

Heating the oxide above 450°C decomposes it to highly insulating lower oxides. The pores of the anode are impregnated with a concentrate of maganese nitrate, which is then pyrolyzed. The solubility of the nitrate is limited so the solution is about 50% water. The reaction is carried out at approximately 400°C to prevent formation of lower oxides. However, the water is converted to steam and is forced out of the pores at high pressure. A gaseous product, N_2O_4, is also evolved in the process and must also escape from the pores. The result of gassing is such that the MnO_2 electrolyte is deposited as a very fine foam, but a single impregnation only partly fills the pores. The process needs to be repeated approximately nine times for satisfactory results. Even at the end of nine pyrolyses, the pores are not solidly filled with MnO_2 because each successive deposit restricts the impregnation of the pores with additional solution. The tantalum oxide is under severe stress during pyrolysis (Reference 4). After completion of this process, with many of the pores and passageways blocked by the manganese dioxide, the device must be returned to an electrolytic bath and "reformed". The reformation voltage is less than the formation voltage, but still appreciably higher than the operating voltage. In order to make a good ohmic contact to the electrolyte, it has been found necessary to apply a layer of graphite (aquadag) to the MnO_2. This is done by dipping the anode coated with MnO_2 in a colloidal graphite suspension, which is then dried. The graphite coated anode is then dipped in a silver paste with an organic binder. The silver paste (sometimes called paint) is cured to produce good contact with the graphite.

The use of the semiconducting electrolyte produces some significant changes. First, the metallic cathode becomes a purely ohmic contact. The wet solution-to-metal interface is eliminated which means that the Helmholtz double layer and cathode polarization capacitance is eliminated. The resistance of the electrolyte is no longer strongly dependent on temperature since it is not governed by the viscosity of the liquid. The frequency dependence of the capacitance is much less due to elimination of the polarization capacitance. The capacitor retains its rectifying properties and it is assumed that the rectifying junction is located at the Ta_2O_5-MnO_2 interface. The reverse voltage characteristics are very much improved since there is no electrolytic release of hydrogen. The reverse current is less, due to the electrolyte resistance which is higher than the liquid electrolyte resistance.

The self-healing process and scintillation are also observed in the solid capacitors. One explanation is that the manganese dioxide is broken down into lower oxides by local heating at defect sites. At about 500°C oxygen will be released which may be available to form new tantalum oxide at the defect site. Another explanation is that the increased resistivity of the lower oxide plugs the leakage site with a high resistive plug (References 5, 6, and 7). Indeed, evidence of fused tantalum at failure sites has been observed, indicating that the local temperature during low impedance faults can be as high as 3000°C. However, the evidence presented in References 5 and 6 has led these writers to believe that formation of new tantalum oxide is not the correct explanation for self-healing, but that high resistivity (10^6 ohm-cm) lower oxides of manganese isolate the fault with insulation. The ability of tantalum to anodically grow oxide when in contact with MnO_2 rather than a wet electrolyte has shown that there is some oxide growth. The rate, however, is several orders of magnitude below that for liquid electrolytes. Thus, the self-healing mechanism in solids depends on defect sites reaching a temperature of about 500°C, but the current flow should be limited to prevent excessive heat which would make the fault propagate or go catastrophic. Thus, the general rule for limiting the current to approximately 300 milliamps when applying solid tantalum capacitors.

After completion of the aquadag and silver paint application, the slug is soldered into a brass can to make a solid assembly. The can, as with wet slug capacitors, is at cathode potential. High temperature solder should be used throughout. For ac applications, solid capacitors are available which essentially consist of two slugs connected back-to-back, the external leads being the anode lead of each slug.

Figure 4 shows the construction features of the tantalum foil capacitor, this unit having a hermetically sealed case. As with all tantalum electrolytic capacitors, the dielectric is tantalum oxide and the capacitive action is achieved by a tantalum-tantalum pentoxide-electrolyte interface. The foil type capacitor has a volumetric efficiency which is lower than the solid and wet sintered slug types. High capacitance per unit volume is obtained by anodizing thin sheets of tantalum foil. The foil may be plain or etched prior to anodizing. The etched foil provides more effective surface area and a higher capacitance per unit volume. Two foils are prepared, one for the anode and the other for the cathode. The cathode foil is anodized to a very thin layer of oxide while the anode foil is anodized to achieve the desired voltage rating. The anode and cathode foils are assembled into a sandwich, with a cross-section as shown in Figure 5.

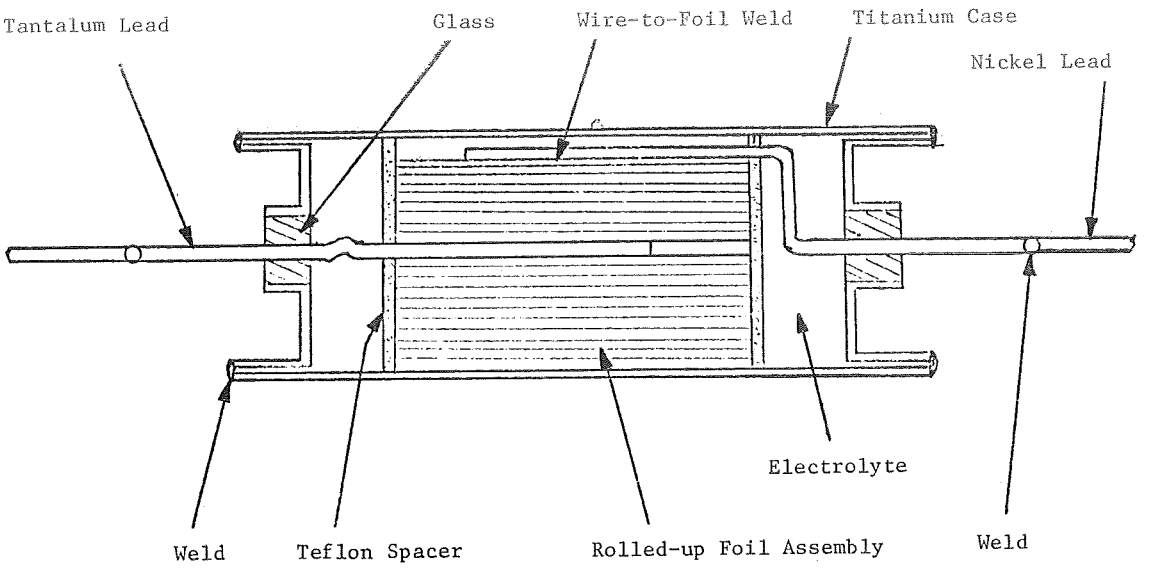

Figure 4 Tantalum Foil Capacitor

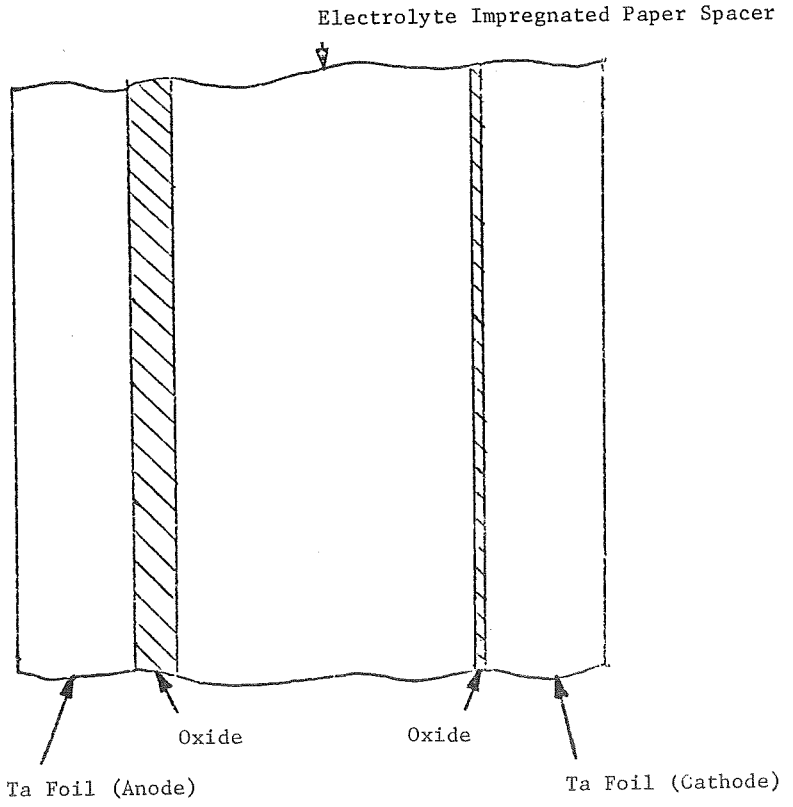

Figure 5 Cross Section of Foil Assembly

The two foils are separated by an electrolyte impregnated paper spacer. The oxide on the anode foil determines the capacitance and voltage rating of the device. The two oxides are facing each other. The oxide on the cathode foil prevents high leakage currents with up to 3.5 volts reverse voltage. The electrolyte impregnated paper provides a conduction path between anode and cathode. The foil sandwich is rolled into a cylindrical shape and assembled in the case. In this assembly, identical hermetic seals are used at both ends. Tantalum feed-through leads are welded to the cathode and anode sides of the foil and extend outside the case via tantalum to glass seals. The seals are welded to the titanium case around the edges of these feed-throughs. Nickel extension leads are welded to the tantalum feed-throughs outside the case. In this construction, both the anode and cathode are isolated electrically from the case.

b. Wet Tantalum Capacitor Failure Modes - Short circuits, high dc leakage, and electrolyte leakage have been the major problems associated with wet slug tantalum capacitors (Reference 8). The major problem has been electrolyte leakage as is evidenced by the fact that more than half of the Alerts on wet capacitors are addressed to this problem. However, improved manufacturing controls and development of hermetically sealed designs have alleviated this problem to a large extent. Table 1 summarizes the predominant failure mechanisms for wet tantalum capacitors, a description and cause of these mechanisms, methods of detecting the defects, and methods to minimize or eliminate the cause of these defects.

Electrolyte Leakage - In addition to an increase in dissipation factor and a decrease in capacitance, the corrosive sulfuric acid electrolyte can be damaging to neighboring components if leaked out. The standard elastomer seal design, regardless of the number of crimps placed on the can, is prone to breathing. Although the seal materials have sufficient resistance to the electrolyte, mass spectrometric experiments and weight loss tests have shown that water vapor and gases such as hydrogen, oxygen, and nitrogen diffuse through the seals during electrical bias and storage. However, most part failures due to seal leakage have been caused by faulty crimping or the tantalum riser wire has defects such as abrasions, scratches, or is out of round and provides a path for the electrolyte. Glass seals were cracked during conformal coating cure cycling of hermetically sealed capacitors (Alert F3-72-02).

Table 1 Failure Mechanism Analysis Wet Tantalum Capacitors

FAILURE MECHAMISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Electrolyte Leakage	Faulty crimping of elastomer seals, riser wire out of round or has scratches and abrasions.	Thymol blue or litmus paper test. Increase in dissipation factor or decrease in capacitance. Temperature cycling, burn-in, seal test, insulation resistance.	Use of hermetically sealed capacitor design, use gelled electrolyte to minimize mobility.
	Overetching of seals when removing silica from leads.	Thymol blue or litmus paper test. Temperature cycling, burn-in, seal test.	Improved process control, keep etchant from seal area on hermetically sealed capacitors.
	Cathode leakage at nickel lead weld to silver case.	Thymol blue or litmus paper test, sample lot dissection of lead weld area for examination of grain structure and detection of thin silver. Temperature cycling, burn-in.	Careful control of critical lead weld schedule, thicker silver can bottom.
	Leakage past inner seal causing electrolyte to bridge anode lead to cathode.	Increased leakage current or short circuit. Temperature cycling, burn-in.	Use of hermetic capacitors having fully anodized anode riser through the seal and external nickel lead attachment.
Oxide Defects	Impurities in starting tantalum impede oxide growth at sites during anodization.	High leakage currents or outlier leakage currents. Temperature cycling, burn-in, surge test.	Use of high purity starting tantalum powder and handling to avoid contamination.
	Abrasions of sintered pellets expose impurities prior to anodization.	High leakage currents or outlier leakage currents. Temperature cycling, burn-in, surge test.	Improved process control to minimize handling damage.

Table 1 (concl)

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Oxide Defects (cont)	Binder or die impurities on sintered pellet.	High leakage currents or outlier leakage currents. Temperature cycling, burn-in, surge test.	Proper binder composition to provide die lubrication and thorough removal of binder in pre-sintering.
	Handling damage during anodization processes and assembly.	High leakage currents or outlier leakage currents. Temperature cycling, burn-in, surge test.	Improved process control to minimize handling damage.
	Crystalline tantalum pentoxide.	High leakage currents or outlier leakage currents. Temperature cycling, burn-in, surge test.	Processing to avoid surface irregularities causing high fields, minimization of contamination which serves as nucleation sites.
Silver Deposition on Anode	Reverse voltage on capacitor.	High leakage current.	Application must insure voltage is never reversed during use or test. Minimize ripple current. Use of designs utilizing titanium or tantalum cases.
Silver Dendrites	Reverse voltage on capacitor.	High leakage current, lower ESR, short circuit.	Voltage must never be reversed. Use of designs utilizing titanium or tantalum cases.
Mechanical Defects	Warped slugs, slugs cocked in case, canted seals, bent or improper length risers, etc.	Radiographic inspection.	Improved process control.

This was traced to overetching of the seals in a process of removing silica from the tantalum leads. The etching weakened the seal and allowed mechanical and thermal stresses to fracture the glass. There may be a considerable time lag between the occurrence of a seal failure and the appearance of electrolyte. If fracturing occurs from temperature, the seal may remain tight, as glass has a higher coefficient of expansion and the cracks are under compression. The cracks may open up completely or return to a lower temperature at a later time. If the hermetic seal is properly made, electrolyte leakage should be eliminated. Although the hermetically sealed capacitor will alleviate the seal leakage, cathode leakage of electrolyte at the lead weld has also occurred. Where nickel lead wires are required, reliable welds are easily made to the anode tantalum riser. The cathode lead weld to the silver case is another matter. Preformed leads are required and the weld schedule is critical in regard to heat, time, and pressure. The nickel lead has a tendency to penetrate the silver case, and a very thin layer of silver may be separating the lead from the electrolyte. The nickel is readily susceptible to attack from the sulfuric acid, which may reach the lead along grain boundaries. Copper leads are very compatible with silver and can be attached by automatic welders utilizing wire spool feeds very reliably. Thicker silver can bottoms and careful control of the welding process is required for nickel leaded wet tantalum capacitors.

Electrical Leakage - Oxide defects appear to be a major contributor to high electrical leakage. It is generally assumed that defects originate at sites where a minute impurity is present either on the surface or just under the surface. Apparently the sintering process serves to reduce the surface impurities. Efforts are made to use very pure tantalum as starting material. When two finished anode slugs are rubbed together prior to anodization, defects are profusely produced in the end product. These defects are more pronounced in the regions of abrasions where there are no sharp peaks. Thus, abrasions appear to expose impurities which, after anodization, produce defect sites. High field spots (peaks, irregularities, etc.) promote the transformation of amorphous Ta_2O_5 to crystalline Ta_2O_5. It has been proposed that impurities can act as nucleation sites for generation of crystalline Ta_2O_5. The crystalline form is more conductive than the amorphous form and behaves like a defect except that the crystalline form may spread to adjacent areas. Sources of contamination which may contribute to defect sites are inherent in the manufacturing processes. First, it is desirable that the starting material be of high purity. The binders which are used to form the

pellets also serve to lubricate the die, and their removal in presintering must be performed carefully to minimize possible contamination with carbon. Besides binder related impurities, the transfer and pickup of impurities from the die material itself occurs due to wear and are not readily removed in the sintering step. These may lead to lasting contamination of the outer surface of the sintered anode. During sintering, the pellets are usually stacked in crucibles, which causes a degree of sintering between pellets and between pellets and the cruicible wall (Reference 2). This bond has to be broken forcibly after sintering with the consequence of some physical damage to most anodes. In some cases the anode leads are pressed into the pellet before sintering and other manufacturers weld the tantalum lead to the pellet after sintering. No problem has been noted for either method of lead attachment to the pellet (Reference 6). After sintering, all operations require that the pellets be suspended from their leads for anodization and that each anode be connected to a power source. The leads are commonly spot welded to fixtures which enable batch processing either manually or at varying degress of mechanization. The fixturing step is a manual operation which requires handling of each pellet again with the possibility of physical damage. After anodization, the pellets must be removed from the fixtures and again handled individually. Careful insertion in the can is required to avoid abrasion again. In some cases (Reference 8), warped anodes have been noted in the finished product. The tantalum riser lead must also be trimmed and the external anode lead welded to the riser. The complex and critical procedures, with the many handling steps, all contribute to sources of contamination and defects in an erratic and unpredictable manner. Batch to batch variations, as well as rather wide variations of electrical parameters in a given batch, can readily occur. In Reference 7, visual evidence of the harm which can result from improper handling of the anodized pellet has been demonstrated. Anodized pellets were purposely damaged by striking one against the other and then immersing the samples into a copper salt solution and applying a cathodic potential. Copper metal plated out preferentially on the damaged area since it was the site of high leakage currents. Photographs were taken, the copper removed by dissolving in nitric acid, and the pellets processed into finished capacitors of the solid type. Sufficient current was allowed to pass to cause discoloration of the tantalum oxide. Analysis of the units purposely damaged revealed the failure site to correspond exactly to the area on which the copper had plated.

In Reference 8, the integrity of the tantalum oxide dielectric was investigated in a similar manner with electrochemical methods. One of the more successful methods was the anodic deposition method using benzedrine hydrochloride electrolyte. The pellet is operated in this solution for a few minutes and then examined for black reaction products of the benzedrine on the slug surface. Again, deliberately scratched or damaged pellets showed the reaction product at the damage sites, definitely indicating that these were sites of high leakage current. Self-healing experiments have shown that the presence of silver or copper ions in the electrolyte play no significant role in determining the rate at which an oxide defect heals. However, where these metals were intentionally plated onto the anodes, the time required to heal defects was increased. Not all the silver on the anode had to be deplated before healing could proceed. Apparently, just the silver in the defect area of the oxide needed to be deplated. Erratic healing surges were noted during the deplating even though available current was limited. On a well-formed defect-free pellet, the silver adheres poorly to the oxide. However, good adherence is observed on a defect area. Very small amounts of reverse bias can cause silver to plate onto the tantalum oxide. In one example, silver was visible after exposure to 0.3 millivolts for 150 hours.

In Reference 9, ripple life tests showed that silver deposits occur on both the anode and the silver case cathode even without reverse bias voltage. The deposits are unlike the large whiskers which result from negative anode bias. It appeared that the mere presence of silver on the anode does not automatically lead to higher leakage currents. However, it is unclear what the long-term effects of large ripple currents and anode silver deposits are. As it is clear that reverse bias silver deposits are definitely a reliability hazard, it appears that ripple current should also be limited to prevent anode silver deposits until the long-term effects are understood.

Shorts - Silver ions in the electrolyte will migrate through the electrolyte and plate out on the oxide preferentially at oxide defects. After the defect is coated, plating will still tend toward the high conductivity site and dendrites will form extending out into the electrolyte. These dendritic bridges promote shorting of the capacitor in two ways. In the first case, when a breakdown is initiated at defects which are coated with silver, the silver may bridge the oxide and short the tantalum to the electrolyte. Since silver does not anodize, the short is a

permanent one. Second, the effect is a type of bootstrap operation in that the dendrite reduces the series resistance of the electrolyte and increases the leakage current. The reduced electrolyte resistance lowers the applied voltage at which breakdown in the oxide occurs. In the extreme case, as reported in Alert MSFC-70-13B, the silver dendrite may reach the silver can producing direct contact between the slug and cathode. Several construction variations have been developed to eliminate this effect. In Reference 10, a platinized gold cathode device is discussed. It is stated that such devices, using cases drawn from gold-clad silver, will tolerate up to one volt reverse bias for extended periods of time. Catalytic recombination of most of the hydrogen and oxygen released under this reverse bias condition is stated to occur in this design. The electrical characteristics are similar to capacitors with platinized silver cathodes. In Reference 11, the silver cathode has been eliminated altogether by using titanium case metal. The titanium and the material used for cathode capacitance do not plate out, therefore, the shorting mechanism caused by silver dendritic growth is eliminated. The capacitor is stated to be capable of reverse voltage applied continuously at 1.0 to 1.5 volts.

Another type of short is associated with leaking electrolyte. If the seal is leaking, the conductive electrolyte can bridge the glass between the anode lead and case causing a short. In some designs, leaking electrolyte between the elastomer and the glass seal can cause the same effect without evidencing external leakage. Sealing the tantalum riser directly to the glass eliminates this possibility.

c. Solid Tantalum Capacitor Failure Modes - High electrical leakage currents, open and short circuits, and increase in dissipation factor have been the major problems associated with solid tantalum capacitors. Increases in dissipation factor are generally due to increases in equivalent series resistance (ESR), but occasionally an increase in capacitance may occur also. Table 2 summarizes the various failure mechanisms for solid tantalum capacitors, a description and cause of these mechanisms, method of detecting the defects, and methods to minimize or eliminate the cause of these defects.

Table 2 Failure Mechanism Analysis Solid Tantalum Capacitors

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Oxide Defects	Impurities in starting tantalum impede oxide growth at sites during anodization.	High leakage currents or outlier leakage currents. Temperature cycling, burn-in, surge test.	Use of high purity starting tantalum powder and handling to avoid contamination.
	Abrasions of sintered pellets expose impurities prior to anodization.	High leakage currents or outlier leakage currents. Temperature cycling, burn-in surge test.	Improved process control to minimize handling damage.
	Binder or die impurities on sintered pellet.	High leakage currents or outlier leakage currents. Temperature cycling, burn-in, surge test.	Proper binder composition to provide die lubrication and thorough removal or binder in pre-sintering.
	Handling damage during anodization processes and assembly.	High leakage currents or outlier leakage currents. Temperature cycling, burn-in, surge test.	Improved process control to minimize handling damage.
	Crystalline tantalum pentoxide.	High leakage currents or outlier leakage currents. Temperature cycling, burn-in, surge test.	Processing to avoid surface irregularities causing high fields, minimization of contamination which serves as nucleation sites.
	Oxide shorts due to excessive power surges under flicker or scintillation conditions.	Short circuit, surge test.	Voltage derating, use of current limiting resistors, processing and material control to avoid defect sites, temperature derating, healing of defect sites with controlled application of power.
	Thin MnO_2 or silver paint penetrating MnO_2 and preventing healing of defect sites.	High leakage currents or outlier leakage currents. Temperature cycling, burn-in, surge test. High dissipation factor.	Adequate processes to provide proper MnO_2 thickness, sample dissection to examine MnO_2 layer.

Table 2 (concl)

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Poor Slug Adhesion	Inadequate wetting of solder to silver paint.	Temperature cycling, burn-in, capacitance decrease, dissipation factor increase, radiographic inspection.	Proper temperature, time, and solder quantity control in bonding slug in the case.
	Silver paint dissolving into the solder.	Temperature cycling, burn-in, capacitance decrease, dissipation factor increase.	Use of silver solder to bond slug to case.
	Low solder level, poor anchorage of slug to case, flux between solder and paint.	Radiographic inspection, temperature cycling, burn-in, dissipation factor.	Control of solder quantity in bonding process as well as time and temperature.
Solder Reflow	Excessive heat applied during assembly of capacitor into circuit.	Radiographic inspection for excessive solder, improper solder distribution, and solder balls.	Use of high temperature solder in capacitor case and in eyelet. Careful control of temperature during assembly operations.
Mechanical Defects	Solder distributions, voids, slugs canted in case, bent risers, etc.	Radiographic inspection.	Improved process control.

1) Leakage Current - Increases in leakage current are usually associated with defect sites in the dielectric. In Reference 5, it is shown that with low circuit resistance, capacitors failed catastrophically at breakdown. The voltage was deliberately increased to breakdown levels. However, with the current limited with a 100-ohm resistor (current less than two amperes) the capacitors apparently healed themselves by the production of lower forms of manganese oxide. When the voltage was again increased to breakdown, the level was found to have significantly increased, indicating that the dielectric strength was improved. However, significant increases in leakage current at rated voltage occurred after each breakdown. The increased leakage is attributed to the plug of MnO formed at the breakdown site. Although it has a higher resistivity than the MnO_2 from which it was derived, it has a much lower resistivity than the tantalum oxide. Also, under the test conditions used, apparently sufficient energy was provided to cause propagation of flaws in the dielectric under subsequent breakdowns. Scintillation or flicker as observed in normal service of solid capacitors is the operation of this same phenomenon. The amount of healing or damage occurring during scintillation is a function of applied voltage, temperature, limiting circuit resistance, and capacitor size. Figure 6 illustrates the possible changes in leakage current occurring from scintillation.

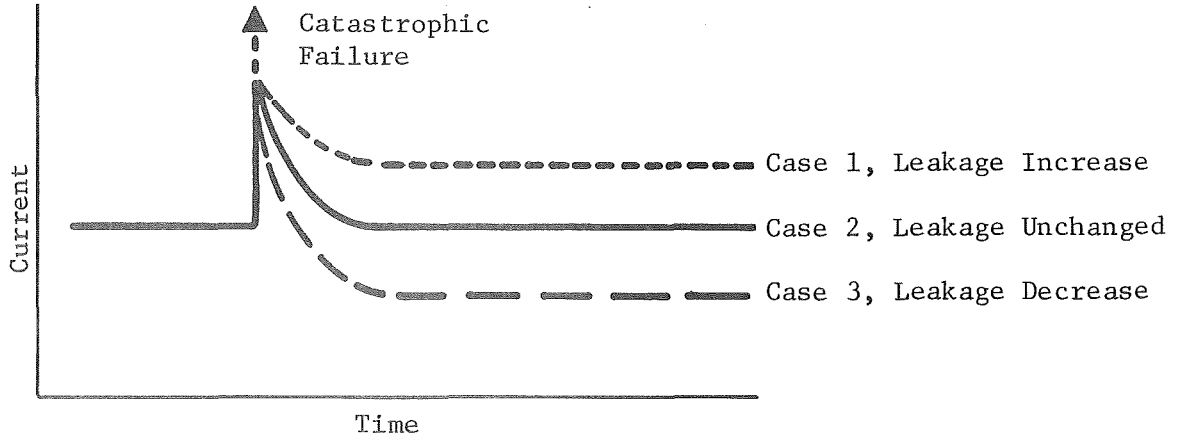

Figure 6 Scintillation Effects on Leakage Current

The capacitor may exhibit an increase, a decrease, no change, or go catastrophic. In Reference 7, it is stated that with the series limiting resistance value of three ohms per volt, catastrophic failures are virtually eliminated, but the leakage current can increase on successive scintillations. The ideal situation would be to supply just sufficient energy to the defect site to accomplish healing without generating more damage. In Reference 12, it is shown that temperatures at the defect site must be in excess of 600°C to achieve proper healing. The manganese dioxide showed a negative temperature coefficient of resistivity below this temperature and a positive coefficient above this temperature. The resistivity changes are permanent once the temperatures are reached and reactions allowed to occur. The investigation was performed to determine a method of supplying minimum energy to fault sites and reduce leakage currents to acceptable values in thin film tantalum capacitors. An approach of slowly increasing the applied voltage while rapidly and continuously cycling 26 current limiting resistors was used. This approach provides a vast number of power levels for clearing faults, and presumably clearing will occur at optimum levels without damaging the dielectric further. Multiple clearings commonly occur, indicating either multiple defect sites or more than one clearing of a single site occurring. It is interesting to note that clearing currents in this particular product were as low as 20 microamperes and ranged to 300 milliamperes. As these levels presumably were capable of generating temperatures greater than 600°C, it is very probable that fault propagation temperature levels could easily be reached in normal service where only a single power level determined by the circuit configuration is available. Also, the capacitor itself is a source of energy which could contribute to healing or possibly damage. In Reference 13, it is noted that the energy in a 35-volt, 6.8 microfarad capacitor may be in excess of observed scintillation energies.

An adequate uniform thickness of MnO_2 is also apparently necessary to prevent increase in leakage current. In Reference 6, it is pointed out that when the MnO_2 layer is very thin or when, equivalently, the silver paint penetrates the MnO_2, effective healing is unlikely at these locations. This condition has been found to be associated with many failures of capacitors due to high leakage. In view of this discussion, it may be expected that capacitors with few defects in the tantalum oxide, with adequate MnO_2, and with proper aquadag, silver paint, and solder connection to the case, would heal themselves in time. The scintillations should cease and, with proper current limiting, the leakage current should decrease. However, solid capacitors in both operating and dormant

conditions are apparently undergoing some gradual internal change which is not fully understood. Thus, after periods of dormancy, parts taken off the shelf exhibit higher leakage currents as reported in IDEP Report No. 347.20.00.00-S6-02. Here it is reported that 40 capacitors exhibited high dc leakage after five years of shelf life. Even under operating conditions, capacitors may remain stable for thousands of hours and suddenly exhibit scintillation which may precipitate a catastrophic failure or increase in leakage current.

The effect of moisture on leakage current is usually negligible. In Reference 4, it is reported that units have been operated in wet air for several months with no change. In Reference 3, uncased units were exposed to 50% relative humidity air at room temperature and were also immersed in water. The results were not uniform, with most capacitors showing no significant change, but some showing a leakage current increase. It is postulated that the leakage current increase is caused by residual unpyrolized manganese nitrate which is ionized by the water. Thus, moisture would not significantly affect a unit where pyrolysis is complete.

2) Shorts - When insufficient circuit series resistance allows large power surges to occur during scintillation, gross Joule heating can occur at the breakdown site and fuse the tantalum so that a metallic-like agglomerate shorts the dielectric. Local temperatures may reach 3000°C. At times the continued application of power under this shorted condition may further heat the capacitor to melt the solder which then can flow and create further shorts.

Excessive heat applied during circuit assembly operations has also caused solder reflow which can cause solder balls or shorted devices from the reflow. Excessive solder, improper distribution in the can, excess fillet in the eyelet, and improper positioning of the slug can aggravate the situation. High temperature solder should be used within the capacitor, and carefully controlled assembly operations performed to avoid excessive heat. Internal solder conditions of the slug and tubelet are easily inspected by X-ray. Alert MSFC-71-3B details acceptance and rejection criteria for such X-ray inspections.

3) Opens - The conditions which create shorts can also lead to opens. For example, the lead wire within the can may fuse open under short circuit conditions. The main defects leading to opens are poor welds from the tantalum riser to the external lead and poor slug anchorage to the can (Reference 6). Poor adhesion of the slug to the solder can be caused by the silver dissolving into the solder. Silver solder should be used to prevent silver migration. Low solder level may result in an intermittently open unit. If the canning operation is performed at too low a temperature, adequate wetting to the silver paint may not be achieved which may result in an open circuit under mechanical stress. The degree of wetting may be observed by examining the solder meniscus in X-ray pictures.

4) High Dissipation Factor - High dissipation factor can be caused by increases in ESR or capacitance, or increases in both. Capacitance and ESR both increase in the presence of moisture (Reference 7). The capacitance in a humid atmosphere increased until it approached the value obtained in an acqueous electrolyte wet check. It is assumed that the wet check indicates the total capacitance available, and the difference between the wet and dry capacitance indicates the area not covered by MnO_2. In Reference 3, it is indicated that a cathode capacitance exists in the solid capacitor and that the capacitance increase is largely due to an increase in cathode capacitance. The change in ESR, and therefore dissipation factor, is caused by a change in resistance of the manganese dioxide. The resistivity increases dramatically in the presence of moisture. The effects of moisture on the solid tantalum capacitor are reversible, as units return to their original values after being dried out. Apparently moisture has no permanent damaging effects to solid tantalum capacitors. However, for highest stability of characteristics, a hermetic seal is necessary.

Heat exposure will also increase dissipation factors by increase in ESR. In Reference 14, chip components subjected to temperatures in excess of 200°C experienced deterioration of the graphite or silver layers. In hermetically sealed solid tantalum capacitors such temperatures would also deteriorate the solder integrity.

A reverse bias on a heated tantalum capacitor (Reference 7) will decrease the effective dielectric thickness thereby increasing the capacitance and therefore the dissipation factor.

Poor solder contact between the capacitor and the inside of the can, due to non-wetting of either the silver paint or the can, will increase dissipation factor because of the high resistance contact. Also, when there is flux between the silver paint and the solder, the increased resistance will cause a high dissipation factor, particularly at low temperature, even if a high solder level exists.

d. Tantalum Foil Capacitor Failure Modes - Decrease of capacitance, decreased insulation resistance, and increase of dissipation factor are the major problems associated with tantalum foil capacitors. High leakage current occurring at the spots where anode and cathode leads are welded to the foils has been a manufacturing problem in the past. This is easily detected in 100 percent screening. Table 3 summarizes the various failure mechanisms for tantalum foil capacitors, a description and cause of these mechanisms, method of detecting the defects, and methods to minimize or eliminate the cause of these defects.

1) Low Capacitance - An example of low capacitance is reported in ALERT No. J5-68-01. After burn-in, more than half of the capacitors exhibited approximately 2% of the initial capacitance. This was caused by faulty welds at the anode lead to the foil. Electrolyte leakage may also cause a decrease in capacitance, but this is virtually eliminated in hermetically sealed units. Another potential source of capacitance decrease is caused by separation of the foils. This may occur if reactive impurities were in the electrolyte or paper, and gas bubbles form between the foils.

2) Low Insulation Resistance - Insulation resistance problems and their causes are closely related to part design. In ALERT No. GSFC-71-6, an insulating mylar sleeving between an internal and external case contained a metallic contaminant. Also, the internal epoxy potting compound was poorly cured. A one-hour bake at 125°C raised the insulation resistance to 1000 megohms. This condition is easily detected by a terminal-to-case insulation resistance measurement.

3) High Dissipation Factor - Separation of foil or leakage of electrolyte will cause an increase in dissipation factor in addition to a decrease in capacitance. This is caused by an increase in ESR. The problem of gas bubbles forming between the foils from reactive contaminants is not a severe problem and has not received much treatment in the literature.

Table 3 Failure Mechanism Analysis Tantalum Foil Capacitors

FAILURE MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Electrolyte Leakage	Leakage past center of seal causing electrolyte to bridge between internal nickel wire and case.	Temperature cycling, burn-in, seal test, capacitance, dissipation factor, leakage current, insulation resistance.	Use of hermetically sealed capacitors having fully anodized lead wires through the seal and external nickel lead welds.
Insulation Defects	Metallic contamination in mylar sleeving, improperly cured epoxy compound.	Burn-in, temperature cycling, seal test, dissipation factor, insulation resistance, leakage current.	Improved handling and process control to avoid contamination and assure cure of insulating materials.
Foil Separation	Reactive impurities in electrolyte or in paper spacer.	Temperature cycling, burn-in, capacitance. dissipation factor.	Good material and process control to insure purity of materials and lack of contaminants.
Faulty Lead to Foil Welds	Machine and operator errors cause inadequate welds.	Temperature cycling, burn-in, capacitance insulation resistance. leakage current, dissipation factor.	Process control of materials and welding equipment and weld schedules.

2. Design

Selection Criteria - Table 4 lists various design factors to be considered for selecting long-life tantalum capacitors. It is recommended that the wet slug tantalum capacitor be avoided wherever possible. Although they can be obtained with reliability levels equivalent to solid slug capacitors, it must be considered that these levels are achieved gradually from numerous tests of relatively short duration. The long-term effects of operation are generally not revealed in these tests. The wet slug types are extremely sensitive to reverse voltage with an unknown long-term effect of ripple current even when the voltage never reverses. The corrosive electrolyte generally makes catastrophic failure more hazardous to other equipment. Also, defects in hermetic seals may not become apparent until after long periods of operation, thermal cycling, or power cycling. The hermetically sealed capacitor should be used regardless of type selected.

For a given voltage rating, it is generally believed that the higher capacitance values are more prone to failure. In Reference 15 it is pointed out that the average number of flaws in dielectrics should increase as the square root of the dielectric area or, equivalently, the square root of the capacitance. In selecting capacitor sizes then, it would be preferable, from a reliability standpoint, to use the smallest possible value of capacitance. However, some applications may be more reliable with one large capacitor as opposed to the use of two smaller capacitors in parallel.

The nature of tantalum capacitors is such that the quality and reliability is highly dependent on the maturity, dependability, and uniformity of the processes and materials utilized. It is extremely important that the manufacturer have a stable, mature, and well-controlled facility with a history of successful experience in ability to perform the critical processes involved. It is preferable that standard sizes and ratings, which are in continuous high volume production, be selected. Start-up problems associated with intermittent production may adversely affect quality. Any requirement which may cause a perturbation to normal producton practices should be carefully considered for the possible impact on product quality.

Table 4 Selection Criteria

Design Factor	Remarks
Seal	For highest stability and reliability, the hermetically sealed type capacitors only should be considered. Elastomer sealed devices should not be used.
Lead Attachment	External leads should be welded to anodized tantalum risers external to the hermetically sealed area. Lead materials non-standard to the suppliers normal product should be avoided to eliminate attachment problems arising from inexperience with such materials.
Solder	High temperature solder should be used throughout in the fabrication of solid tantalum capacitors to prevent reflow during assembly operations. Silver solder must be used for attachment of slugs into cases in order to prevent silver paint dissolving into the solder.
Foil	As fewer anomalies are likely to exist with plain foil, these are preferred over the etched foil capacitors.
Size & Ratings	Standard production sizes and ratings only should be selected. Non-standard sizes and ratings unique to the supplier are a greater reliability risk because of his inexperience with these items. A single large value capacitor is preferred over utilization of two capacitors in parallel.
Electrolyte	If wet slug capacitors are utilized, the gelled electrolyte is preferred over the liquid because of lesser mobility.
Product Maturity	Select parts with high volume continuous production and acceptable past usage history, with no imminent likelihood of obsolescence in product line.

b. Results of Survey - Aerospace users of electronic parts were surveyed in regard to their procurement practices in obtaining high reliability tantalum capacitors. In general, the requirements of MIL-C-39003 and MIL-C-39006 were used as is, or were used with some additional or more stringent requirements. Table 5 lists the various users who have reported tantalum capacitor tests or other specification requirements which are unique to the requirements of the Established Reliability specifications. The rationale provided for each requirement is also listed. It is noted that the most common unique requirement was an increase of burn-in duration.

The users were also queried as to their preference of tantalum capacitor type for long-life space missions. The consensus, in order of preference, was: 1) solid electrolyte; 2) tantalum foil; and 3) wet slug. No specific application requirements were considered; merely preference based on probable relative life expectancy as biased by their experience. The solid electrolyte and tantalum foil capacitors ranked close together. A few users even preferred the foil to the solid. However, without exception, the wet slug capacitor ranked last, considerably below the solid and the foil types.

c. Alternate Approaches - The historical problems with wet slug tantalum capacitors have been associated with corrosive electrolyte leakage and silver electrochemical action. The desire to use this capacitor, with the attendant advantage of highest volumetric efficiency, is tempered by these problems. The hermetic seal has been a development to solve the electrolyte leakage problem. Other developments to solve the silver electrochemical problem have been the platinized gold cathode approach (Reference 10) and the titanium cased capacitor with lithium chloride electrolyte (Reference 11). However, the use of lithium chloride adversely affects the low temperature capability. Another approach currently under development is the tantalum cased capacitor with sulfuric acid electrolyte. This is being developed by Transitor for NASA-MSFC. All of these capacitors can withstand some reverse voltage without the danger of silver plating out on the cathode. In the tantalum cased capacitor, the cathode capacitance is formed to provide approximately a 2-1/2 volt reverse rating. At the present time, the dissipation factor of this capacitor is high as compared to silver cased types. The tantalum cased capacitor development may solve most of the problems associated with wet slug types and should be followed closely.

Table 5 Survey of Electronic Part Users

PART TYPE (CATEGORY)	USER	UNIQUE TEST OR SPECIFICATION REQUIREMENTS	RATIONALE/JUSTIFICATION
Wet Slug Tantalum Capacitors	MSFC	Radiographic inspection per MSFC STD-355.	Detailed guidelines for interpretation of radiographs provide more definitive and comprehensive inspection criteria. Problems identified in Alert MSFC-71-3 indicated need for guidelines.
	JPL	Parametric data is reviewed for outlier detection.	Parts with characteristics that differ significantly from the rest of the lot are reliability suspects and should not be used in flight hardware.
	TRW Systems	Burn-in increased to 250 hours.	Experience has indicated that longer burn-in is necessary to detect all parts with instabilities.
	Martin Marietta, Denver	Qualification includes 600 hours storage at 135°C, 1880 G 0.4 ms half sine shock, 80 G 22 ms half sine shock, 75 G sine vibration to 2000 hz, and 36.6 G rms random vibration.	Qualification levels imposed to meet Viking sterilization and environmental requirements.
	G. E. Pittsfield	Burn-in increased to 96 hours.	Longer burn-in is necessary to detect all parts with instabilities.
		Nickel to tantalum lead weld must be made external to seal.	Internal electrolyte leakage can otherwise cause increase in electrical leakage and attack nickel lead.
	LMSC	Nickel to tantalum lead weld must be made external to seal.	Internal electrolyte can otherwise cause high dc leakage.
		Burn-in increased to 96 hours.	Longer burn-in is necessary to detect all parts with instabilities.

Table 5 (cont)

PART TYPE (CATEGORY)	USER	UNIQUE TEST OR SPECIFICATION REQUIREMENTS	RATIONALE/JUSTIFICATION
Wet Slug Tantalum Capacitors (cont)	LMSC (cont)	100% high temperature surge test at 85°C for 100 cycles, each consisting of 30 sec. rated 85°C surge voltage followed by 30 sec short.	This test is believed to be able to detect weak spots in dielectric while non-damaging to good parts.
	Hughes	Burn-in increased to 100 hours, tightened delta limits on capacitance, leakage, and dissipation factor.	Longer burn-in is necessary to detect all parts with instabilities, tight delta limits assure highly stable parts.
Solid Tantalum Capacitors	MSFC	Radiographic inspection per MSFC STD-355.	Detailed guidelines for interpretation of radiographs provide more definitive and comprehensive inspection criteria. Problems identified in Alert MSFC-71-3 indicated need for guidelines.
	JPL	Parametric data is reviewed for outlier detection.	Parts with characteristics that differ significantly from the rest of the lot are reliability suspects and should not be used in flight hardware.
	TRW Systems	Point of manufacture is controlled.	Assurance is obtained that parts are made in qualified facility.
	Martin Marietta, Denver	Qualification includes 600 hours storage at 135°C, 1880 G 0.4 ms. half sine shock, 80 G 22 ms. half sine shock, 75 G sine vibration to 2000 hz, and 36.6 G rms random vibration.	Qualification levels imposed to meet Viking sterilization and environmental requirements.

Table 5 (cont)

PART TYPE (CATEGORY)	USER	UNIQUE TEST OR SPECIFICATION REQUIREMENTS	RATIONALE/JUSTIFICATION
Solid Tantalum Capacitors (cont)	Martin Marietta, Denver (cont)	Burn-in increased to 250 hours at 85°C and 1.3 times rated voltage.	Longer burn-in is necessary to detect all parts with instabilities. Accelerated voltage provides burn-in equivalent to 3000 hours or more.
	G. E. Pitsfield	Burn-in increased to 96 hours.	Longer burn-in is necessary to detect all parts with instabilities.
	Hughes	100% Weibull testing at 85°C and 150% to 200% voltage for 100 hours minimum.	Determine that lot is within failure rate limits and demonstrate a decreasing failure rate.
	Autonetics	Burn-in increased to 96 hours at 125°C.	Longer burn-in is necessary to detect all parts with instabilities.
		Delta leakage after burn-in at 25°C is 120% maximum of initial value.	Tight delta limits assure highly stable parts.
		Dissipation factor performed at 1000 hz.	Data for each lot is reviewed, and items with D.F. values beyond a 3 sigma limit are discarded. These items are considered to differ significantly from the lot and are reliability suspects.
	McDonnell-Douglas (West)	Burn-in increased to 240 hours at 85°C.	Longer burn-in is necessary to detect all parts with instabilities.
	Philco-Ford	Burn-in increased to minimum of 100 hours at 85°C.	Longer burn-in is necessary to detect all parts with instabilities.
	LMSC	Burn-in increased to 250 hours and 10 temperature cycles performed instead of 5.	Longer burn-in and more temperature cycles is necessary to detect all parts with instabilities and weaknesses.

Table 5 (concl)

PART TYPE (CATEGORY)	USER	UNIQUE TEST OR SPECIFICATION REQUIREMENTS	RATIONALE/JUSTIFICATION
Tantalum Foil Capacitors	MSFC	Radiographic inspection per MSFC STD-355.	Detailed guidelines for interpretation of radiographs provide more definitive and comprehensive inspection criteria. Problems identified in Alert MSFC 71-3 indicated need for guidelines.
	JPL	Parametric data is reviewed for outlier detection.	Parts with characteristics that differ significantly from the rest of the lot are reliability suspects and should not be used in flight hardware.
	TRW Systems	Burn-in increased to 250 hours.	Experience has indicated that longer burn-in is necessary to detect all parts with instabilities.
	LMSC	Burn-in increased to 96 hours.	Longer burn-in is necessary to detect all parts with instabilities.
	McDonnell-Douglas (West)	Two cycles, each consisting of 24 hours at 85°C with applied voltage and 24 hours at -55°C with no voltage.	Mechanical/thermal stress at temperature extremes and with voltage applied will detect weaknesses within foil detectable by changes in capacitance.
	Philco-Ford	Burn-in increased to minimum of 100 hours at 85°C.	Longer burn-in is necessary to detect all parts with instabilities.

The solid electrolyte capacitor has a higher volumetric efficiency than the tantalum foil type, but has the disadvantage of lesser surge voltage capability. Minimum circuit impedance is usually imposed to assure that power surges during scintillation lead to healing rather than propagation of damage in the dielectric. The effectiveness of solid electrolyte capacitors would be greatly enhanced if the requirement for circuit impedance could be eliminated and surge capability increased.

The technique successfully used on thin film solid electrolyte capacitors to optimize healing (Reference 12), should theoretically be applicable to discrete solids. This technique consists of slowly increasing the applied voltage while rapidly and continuously cycling 26 current limiting resistors with values from zero ohms to one megohm. This provides a vast number of power levels for clearing faults, the available power increasing in small increments. The weakest spots in the dielectric should break down at the lowest voltages and clear themselves first. As the voltage and power levels are extremely low at the start of the voltage ramp, the energy supplied is intended to be sufficient to convert manganese dioxide to manganese oxide, but not sufficient to propagate the defect. The defect is healed by the insulating effect of manganese oxide. Theoretically, it should be possible, with optimized healing, to obtain a capacitor with surge voltage capability close to the anodization reforming voltage. Voltages above this level may result in a completely insulated capacitor or a shorted capacitor.

It is recommended that research be conducted to develop an optimized healing approach for solid electrolyte discrete capacitors utilizing controlled step application of power and voltage. The purpose is to utilize fully the potential capability of existing capacitor types by both eliminating devices not capable of sufficient healing, and providing optimum healing of superior devices with fewer defects in order to advance the long-life assurance of solid tantalum capacitors. It is recommended that this research include:

1) Determination of approach to obtain optimized healing.

2) Determination of optimized healing effects on characteristics of capacitance and dissipation factor.

3) Determination of improvement in surge current and voltage capability, together with feasibility of decreasing circuit resistance requirements.

4) Comparison of optimized and non-optimized capacitor reliability by means of Weibull accelerated life tests.

The capacitor which is optimally healed should be more reliable and longer lived in any given application, as the capability to withstand unexpected stresses should be improved. In an unpublished report by H. W. Holland, of Kemet, surge testing of solid electrolyte capacitors was investigated for the purpose of screening to obtain capacitors capable of reliable operation with a series impedance of zero ohms per volt. Even without optimized healing, it was concluded that operation with series impedances below 0.1 ohm/volt can be used successfully when devices were screened with surge current testing. Of 40,000 capacitors subjected to 15 current surges, a decreasing failure rate was observed on repeated surges. Ninety-one percent of all rejects (leakage current out of specification) occurred during the first three surges. The decreasing failure rate is in accordance with accelerated Weibull life test data such as that obtained in Reference 16.

Normal burn-in testing does not adequately screen solid electrolyte capacitors in regard to capability for operation under transient conditions. Use of an optimized healing technique has potential for application as a screen or a conditoning test to improve the capability of solid capacitors, to increase the long-life reliability, and to improve their usefulness by reduction of the series limiting impedance requirement.

d. Hardware Life - The expected life of tantalum capacitors is closely related to the application and environment. Operation of well-screened capacitors under moderate conditions of temperature, mechanical environment, with derated voltage, derated ripple current, and with no transient or reverse voltages would have the greatest expected longevity. Wet slug tantalum capacitors with elastomer seals would have little trouble meeting a design life of three to four years (Reference 8), while the hermetically sealed device is expected to be considerably longer. Weight loss of wet slug devices may be one indication of longevity, although many other factors must be considered. In Reference 11 it is reported that weight loss from electrolyte decomposition and water loss through elastomer seals was more than 12 times greater

than through "hermetic" devices. During a 7000-hour test at rated voltage at 85°C, the elastomer devices showed more than 6% weight loss while the hermetic devices showed less than 1/2% weight loss. Some unknowns, which exist in the truly hermetic devices, are the rates and dispositions of electrochemical gaseous products, pressure build-up, and effects of cycling and periods of dormancy on these effects. It is generally believed (Paragraph C.2.b) that tantalum wet slug capacitors in their present state are not suited for long-life space missions. In Reference 17, it is stated that wet slug tantalum capacitors are judged to be unsuitable for a 100,000-hour mission due to the corrosiveness of the electrolytic medium and the resulting long-term aging effects that are possible.

Solid slug and tantalum foil capacitors are capable of meeting 100,000-hour mission life requirements. The useful life of these capacitors is enhanced by derating, benign environments, and circuit tolerance to parameter change. Test data beyond 10,000 hours of life is scarce. For example, in IDEP report No. 152.75.40.40-E9-02, 520 solid capacitors were tested at rated voltage at 85°C for 10,000 hours. Four failures due to leakage were observed.

In accordance with other experiences of decreasing failure rate, two failures occurred during the first 2000 hours of test and the other two during the remaining 8000 hours of test. In IDEP Report No. 152.75.40.40-H6-01, 40 pieces of solid slug capacitors were operated for 18 months at 25°C at 80% voltage in vacuum. No failures occurred. The nature of the solid electrolyte tantalum capacitor leads many to view the device as a semiconductor. In Reference 17, the relative failure rate factor of solid capacitors is the same as for low power bipolar transistors. The relative failure rate factor for tantalum foil capacitors is somewhat better than high power density diodes.

e. Application Guidelines - The tantalum electrolytic capacitors are used where large values of capacitance in a small volume are required. They are suitable for use primarily in by-passing, coupling, filtering, and applications requiring energy storage. In general, they are not suited for precision timing or oscillator circuits because of parameter changes during life and at temperature extremes. All types should be applied so that the peak voltages experienced by the capacitor do not exceed the derated voltage. Sufficient dc polarizing voltage should be applied to polar types to prevent any reverse voltage on the capacitor by ac components at any time. When used in banks or in parallel

operation, consideration must be given to the manner in which ripple current is shared throughout the applied life. The highest ripple current, in the capacitor with the lowest ESR, should not exceed the derated ripple current rating. The total temperature, including the temperature rise from self-heating, should not exceed the derated temperature rating. Tantalum capacitor banks should be potted into an easily removable module to facilitate replacement and periodic test.

1) Wet Slug Tantalum Capacitors - The advantage of the wet slug is that it has the highest volumetric efficiency. The leakage is low and may continue to improve under steady state operation. The disadvantages are a comparatively poor temperature characteristic and high dissipation factor. The corrosive electrolyte, the extreme susceptibility to reverse voltages, and the use of silver on the cathode, are other undesirable features. There is evidence that ripple current on these capacitors can cause silver to plate on the anode slug, in addition to the normal capacitor heating (Reference 9 and Alert No. MSFC-70-13). Although the impact of plating on the anode due to ripple is not fully known, the possibility of increased leakage at oxide defect sites and the freeing of these particles under mechanical environments exists. Plating also occurs on the cathode, which can be another source of particulate generation under shock or vibration. Quantitative data on minimum ripple currents required to cause plating over extended periods of time does not presently exist. Levels of vibration or shock required to free the plated particles from the anode or cathode are also unknown. Thus, in addition to the possibility of seal leakage and the susceptiblity to reverse voltage, the particulate contamination possibility makes the wet slug capacitor a reliability risk in long-term missions, particularly if high shock and/or vibration levels are involved. The limiting value of ripple is probably determined by the plating effect rather than the self-heating effect. The following derated ripple current levels are therefore recommended for the CLR65 type capacitors:

T_1 Case Size - 35 ma RMS

T_2 Case Size - 120 ma RMS

T_3 Case Size - 300 ma RMS

These values are for 120 hz. Ripple current at other frequencies should be controlled such that the heating effect at higher frequencies does not exceed that at 120 hz, allowing for the decrease in ESR with increasing frequency and temperature. Operation of these capacitors back-to-back is not recommended. Operation in series connection should utilize balancing resistors in parallel to assure proper division of voltage. After periods of dormancy or storage, the leakage current may be expected to rise because the self-healing effect during operation is absent and oxygen barriers at weak dielectric spots diffuse away. The capacitors will return to normal if operated near rated voltage for approximately 48 hours. It is preferable that the voltage be applied in a ramp fashion rather than in a step fashion under these conditions.

2) *Solid Electrolyte Capacitors* - The solid tantalum capacitor is superior to the wet slug and the tantalum foil capacitors in high frequency characteristics, particularly at low temperatures. Although this capacitor is capable of reverse voltages of approximately one volt, it is recommended that voltage reversal be avoided for maximum reliability, particularly where capacitance stability is required. Reverse voltage tends to increase the capacitance and adversely affect the high frequency characteristics. The scintillation effect may cause undesirable circuit noise in some applications. This effect is minimized at reduced temperatures and voltages. This effect also makes the capacitor sensitive to voltage and current surges and is therefore not preferred for pulse applications. Transient voltages must be limited to the derated voltage rating. A series resistance of 3 ohms per volt minimum is recommended to prevent scintillation derived damage. If these capacitors are used in banks, the series resistance should be used with each capacitor. Otherwise, the self-healing breakdown may become a catastrophic failure because of the low impedance discharge of the paralleled capacitors into the breakdown site.

When used in series, balancing resistors should be used to ensure proper voltage division. The polar solids may be used in non-polar applications connected back-to-back if derated peak voltages and temperatures are not exceeded and the series limiting resistance recommendations are implemented. Both polar and non-polar capacitors, when used in ac applications, should be insulated from ground. The ripple or ac current should be controlled such that the heating effect does not cause the derated temperature rating to be exceeded, allowing for the decrease in ESR with increasing frequency.

3) Tantalum Foil Capacitors - The tantalum foil capacitor has the advantages of availability of non-polar types, the use of tantalum for both anode and cathode giving the least electrochemical action, higher voltage ratings, and ability to take unexpected overloads. The polar types have the capability to withstand voltage reversals up to 3 volts, but for highest reliability it is recommended that reverse voltage be avoided wherever possible. The principal disadvantages are that they have greater tolerances than the solids, higher dissipation factor than the solids, and poorer temperature characteristics than the wet slugs. The foil type is prone to failure in the open mode as opposed to the shorted mode and is therefore more suitable than the solid capacitor in some applications, such as in filter banks. The plain foil is preferred over the etched foil because of greater stability and the lesser possibility of having anomalies. However, greater capacitance in smaller size is available with the etched foil type. The surge voltage should never exceed the derated voltage rating. Ripple or ac current should be controlled such that the heating effect does not cause the derated temperature rating to be exceeded, allowing for the decrease in ESR with increasing frequency. When used in series, balancing resistors should be used to assure proper division of voltage.

4) Derating - For long-life high reliability usage, the peak voltage of any tantalum capacitor should not be allowed to exceed 50% of the manufacturer's derated ratings. The ripple current for wet slug capacitors should not exceed the values tabulated above. For solid slug and tantalum foil capacitors, the allowable ripple current should be limited to 70% of the manufacturer's derated ratings. The temperature of tantalum foil and wet slug capacitors should not be allowed to exceed 70°C including the effects of internal heating. The temperature of solid electrolyte capacitors should not exceed 50°C. These derating values are recommended as the result of a derating survey reported in Volume IV.

D. TEST METHODOLOGY AND REQUIREMENTS

1. Qualification

The qualification and retention of qualification requirements of MIL-C-39003 and MIL-C-39006 are excellent and entirely adequate for most high reliability applications. Parts should be procured to the highest reliability level available, never below level P. Additional qualification requirements should be imposed only when unusual program-peculiar needs, such as higher environmental levels, arise. Although the presently available tantalum foil and solid electrolyte capacitors are deemed suitable for 100,000 hour applications (properly applied and derated), it may be desirable at times to select, from available qualified products, those with the greatest expected longevity. In this event, it is recommended that an evaluation approach, as opposed to qualification, be implemented in accordance with Subsection D.2.

2. Life Test

It is impractical to perform a real time test under normal operating conditions to verify 100,000 hour life capability. However, it may be extremely desirable, even necessary, to obtain confidence in, or an estimate of, long life capability when a new tantalum product is being considered for such usage. This condition would apply both to the new sources of conventional products and to new product developments. When necessary under these conditions, it is recommended that an accelerated test approach be utilized using the Inverse Power Rule identified in "A Study of Accelerated Testing Techniques" included in Volume IV. These tests should be performed at constant temperature (either rated or use conditions) but at accelerated voltages. A two step approach is recommended consisting of: 1) determination of maximum usable voltage stresses and; 2) performance of the accelerated life test. The first step utilizes a small number of samples (approximately 5 to 10) and consists of increasing the voltage in small increments for short durations (10% of rated voltage, one hour each increment), starting at 110% of rated voltage, and progressing until failure occurs. The failure criteria could be the occurrence of a catastrophic failure or a permanent change in a desired parameter such as leakage. The desired parameter measurements should be made after each increment under a set of standard conditions. The trends in the parameters following each increment should be observed carefully to detect changes indicative of damage occurring within the capacitor. When catastrophic failures or sudden parametric shifts occur, dissection analysis of the capacitors involved should be made

for determination of failure mechanism. In this manner, the maximum voltage level which does not initiate new failure mechanisms can be estimated in approximately one week or less. From this data, voltage levels to be used in the second step can be selected, preferably less than the maximum estimated in Step 1. Data on accelerated tests of capacitors indicates that the value of the exponent "n" in the Inverse Power Rule will be between 10 and 20. For solid electrolyte capacitors tested in Reference 16, the value was estimated to be 9.6. The simplest manner to perform Step 2 is to assume an exponent "n" of 10, which is probably conservative, and perform a constant high voltage test for a given length of time. For example, if 160% of rated voltage is well within the maximum usable level determined in Step 1, then a 1000 hour test at this voltage is equivalent to a minimum 100,000 hours at rated voltage. If the value of "n" is greater than 10, then it is equivalent to a correspondingly greater number of "real time" hours. (With "n" = 20, a 1000 hour 160% voltage test is approximately equal to ten million hours at rated voltage.) Rather than attempting extremely high acceleration factors, it is recommended that more moderate voltages be used requiring about 1000 hours of test time to acquire the needed information. Since a minimum value of "n" is assumed, this is a purely qualitative approach. No information is obtained on failure rate estimates. However, it is an economic approach in both time and money to obtain some assurance that the product evaluated is capable of performance for the required time. The minimum quantity of parts tested should be thirty pieces. The number can be increased for greater confidence. If failures occur during the 1000 hour test, Weibull analysis of the data can be made. The slope will indicate if the part has an increasing or decreasing failure rate. With assumptions to the value of "n", failure rate or hazard estimates can be made for usage or derated conditions.

If more precise results are required, a minimum of two groups of parts should be used, each subjected to a different accelerated voltage. For practical test times and moderate accelerating factors, the voltages chosen should be such that the lower voltage group has approximately 50% (or more) failures within 2000 hours. The higher voltage group should be tested at a level which provides approximately 50% failures between 100 and 1000 hours. With two groups of parts and two Weibull analyses, the regression curve shown in Volume IV for the Inverse Power Rule can be made, hazard rates for any reasonable derated voltage condition estimated, and the exponent "n" for the part determined.

For a given part, Step 1 need not be performed each time it is desired to perform Step 2. Once the valid upper limit of voltage is established, accelerated tests on that part can be performed economically to determine qualitatively the capability for the required life time. If desired, the capability of a particular production lot can be verified. Step 1 need only be performed when the valid upper limit is unknown, and repeated only if a significant change in design, processes, or materials is made.

The qualitative approach, using one group of parts for Step 2, can also be valuable in comparing the relative reliability or longevity of two or more available products. Weibull analyses of tests performed on samples of each product would show the relative reliability in comparison with one another.

3. Screening

The screening requirements of MIL-C-39003 and MIL-C-39006 (Level P or greater), are considered adequate for most high reliability applications. However, for highest quality, it is recommended that a 100% radiographic inspection of all parts purchased to these specifications be made in accordance with comprehensive inspection criteria such as exists in MSFC STD 355. In addition, it is recommended that analysis of all lot parametric data be reviewed against a suitable outlier criterion. Parts having parameters significantly different from the others within the same lot are suspects, even if they are within specification limits. They must be considered abnormal if they exhibit abnormal characteristics. There is no sound outlier criterion established on the basis of test data relating degree of abnormality to reliability. A subjective approach of reviewing data and rejecting parts by judgment is not recommended. Statistical data analysis by computer is more accurate and faster. One criterion used is to reject all parts having values beyond three sigma limits of the lot mean value, based on assumption of normal distribution. An outlier criterion based on the probability that the tested part does not belong to the group is preferred. Such a criterion was used by JPL and is described in their Reliability Engineering Document No. 15-1, "Program Specifications for Component Parts Screening Data Reduction Systems".

4. Burn-In

The survey results listed in Table 5 indicate that many users of tantalum capacitors have increased their burn-in (or voltage conditioning) requirements beyond those existing in MIL-C-39003 and MIL-C-39006. It is recommended that for long life programs, the

burn-in requirement for all tantalum capacitors be 240 hours minimum, at rated 85°C voltage, at 85°C. Consideration should be given to increasing the voltage, and thereby reducing the time, but this should be based on data obtained from tests such as those described in Para D.2. If such data is obtained, Weibull analyses may then be possible from accelerated burn-in tests on each lot. In Reference 15, a relationship is brought out between reliability of tantalum capacitors and the delta changes in capacitance and leakage during life tests. Many of the users surveyed have also imposed tight delta limits. It is recommended that tightened delta limits during burn-in be imposed on all capacitors applied in long-life missions. As there is no quantitative data relating burn-in delta limits to failure rate, the absolute values required cannot be presently defined. The delta limits should be chosen in coordination with suppliers to establish values which are reasonable and assure procurement of the most stable parts. Further, of the parts received, it is recommended that those with the highest stability be used in flight hardware, while those with lowest stability be used in development, breadboard, and qualification hardware.

E. PROCESS CONTROL REQUIREMENTS

1. Starting Material

The tantalum powder used in processing of sintered slug devices should be of the highest purity. Contaminants will lead to oxide defects. Much attention has been paid to this problem in the past, and the suppliers of tantalum powder have been providing adequate purity for some time. Spherical shaped grains were thought at one time to be superior to irregularly shaped grains, but investigations have shown this not to be significant. Care must be taken during subsequent processing of both foil and sintered type devices to prevent contaminants on the surface and just under the surface where anodization is to take place. In foil capacitors, contaminants in electrolyte or paper separator could cause gassing resulting in foil separation.

2. Green Pellet Formation

The type and consistency of binder used in mixture with the tantalum powder can contribute to contamination-caused oxide defects. Contaminants in the binder itself are one source, and can be particularly troublesome if they are nonvolatile. The binder and tantalum mixture should provide proper lubrication of the forming die so that contamination by die wear products is minimized. Various binders and formation processes are used with equal success. The anode lead may be inserted at this time or welded to the slug in a later step after sintering. Both procedures are equally acceptable.

3. Sintering

The first step in the sintering process (pre-sintering) drives off the binder. The temperature, temperature rates, vacuum, and duration should be such that the binder is removed in such a fashion that the slug is not physically disturbed and is homogenous in density and porosity. The second step consists of the actual sintering, and again the temperatures, rates, and durations should be such that a homogeneously porous but a mechanically sound structure results. The sintering should also provide complete removal of remaining binder as well as any other contaminants that may be on the surface of the slug.

4. Anodization

Most of the defects originating during the anodization process are mechanical damage in handling the slugs and welding to fixtures. There is considerable latitude in rates, solutions, temperatures, etc. When the final forming voltage is reached, the slug should be retained at that voltage sufficiently long to allow thorough and complete oxidation throughout the porous body.

5. Pyrolysis

The preparation of MnO_2 on the slug should be performed a sufficient number of times to assure complete impregnation. This will provide maximum capacitance and assure availability of dioxide for healing. There should be adequate MnO_2 on the surface of the slug also to assure availability of dioxide to heal surface defects. Handling during reforming must be performed carefully to prevent damage and thin spots in the manganese dioxide. After carbon coating and application of the silver paint, any fluxes or binders should be thoroughly cured out.

6. Handling

In addition to the requirement for careful handling to prevent contamination defects as noted above, careful handling is required to prevent physical damage. Even small abrasions prior to anodization could cause oxide defects. Sharp projections could cause high field stresses resulting in crystalline oxide which could spread. After anodization, the oxide itself is susceptible to physical damage. Therefore, the processes such as forming foil into rolls, inserting rolls and slugs into cans, etc, must be carefully performed to avoid dielectric damage.

7. Assembly

The operation of attaching the solid slug to the can requires proper temperatures and solder quantities to provide reliable adhesion. Excess solder and heat can lead to solder balls and conditions leading to short circuits. Insufficient solder or heat will create poor wetting, poor mechanical strength, and/or high resistance contact. The other assembly operations such as sealing and lead attachment can lead to early failures if not properly performed.

8. General

Many of the processes critical to performance of tantalum capacitors are proprietary. It is necessary that they be under good control by the manufacturer to assure repetitive and continued production of reliable products. Most of the processes result in easily detectable characteristics changes when out of control and generally affect yield. A summary of critical process/materials and the effects of inadequate control is presented in Table 6.

Table 6 Process Control

Critical Process/Materials	Effect of Inadequate Control	Remarks
Starting Material	Contaminants in tantalum cause oxide defects. In foil capacitors, contaminants in electrolyte or paper separator could cause gassing resulting in foil separation.	The results of inadequate process control are generally detectable by excessive scintillation, leakage current, dissipation factor, low capacitance, seal tests, and visual inspection.
Green Pellet Formation	Improper die lubrication by binder causes die wear products to contaminate slug.	
Sintering	Inadequate control of sintering can result in low mechanical strength and slug surface contamination.	
Anodization	Insufficient or non-uniform anodization results in inadequate voltage margin and high leakage currents.	
Pyrolysis	Inadequate pyrolysis results in high dissipation factor, lower capacitance, and inadequate healing capability.	
Handling	Improper handling can cause contamination or damage to the capacitor. Contaminants can lead to oxide defects.	
Assembly	Improper assembly can result in poor lead attachment, leaky seals, conductive particulates, or inadequate bonding of slug to case.	

F. PARTS LIST

1. Acceptable

The tantalum foil and solid electrolyte capacitors made to specifications MIL-C-39006 and MIL-C-39003 are acceptable for long life applications. Screening should be modified per the guidelines in Para B.4. All capacitors must be hermetically sealed. The acceptable tantalum foil capacitors are listed in Table 7, and the solid electrolyte capactors in Table 8. These parts are identical to the Preferred Parts for Space Shuttle listed in MSFC specification 85M03936.

2. Unacceptable

Wet slug tantalum capacitors are not acceptable for long life applications at this time. Nonhermetic tantalum capacitors and all tantalum capacitors not meeting the minimum P level requirements of MIL-C-39003 and MIL-C-39006 are not acceptable. Wet slugs may become acceptable on development of the tantalum cased capacitor.

Table 7 Acceptable Tantalum Foil Capacitors

Type Part No.	Electrical Characteristics			Specification	QPL	Remarks
	w Vdc @ 85°C	Capacitance (μF) Min.	Max.			
Polarized, Etched Foil, CLR 25	15	60	580	MIL-C-39006/1B	QPL-39006	Note - Both hermetic and non-hermetic seals are available to the applicable detail specifications. Only the hermetic seal types are approved. Order to failure rate "P" or better.
	25	40	350			
	30	32	300			
	50	18	150			
	75	12	100			
	100	8	70			
	150	4	36			
Non-Polarized Etched Foil, CLR 27	15	40	350	MIL-C-39006/2B		
	25	20	200			
	30	18	170			
	50	10	80			
	75	6	50			
	100	4	35			
	150	2	18			
Polarized, Plain Foil, CLR 35	15	18	160	MIL-C-39006/3B		Tantalum capacitors are are limited as a function of temperature, voltage and ripple current.
	25	12	100			
	30	10	85			
	35	--	68			
	50	6	55			
	75	4	40			
	100	3	30			
	150	2	20			
	200	1.5	15			
	250	1.2	12			
	300	1.0	10			
	375	0.82	8.2			
	450	0.56	5.6			
Non-Polarized Plain Foil, CLR 37	15	10	100	MIL-C-39006/4B		
	25	6.0	60			
	30	5.5	45			
	50	3.0	30			
	75	2.0	20			
	100	1.5	15			
	150	1.0	10			
	200	0.75	7.5			
	250	0.60	6.0			
	300	0.47	4.7			
	375	0.39	3.9			

Table 8 Acceptable Solid Electrolyte Tantalum Capacitors

Type Part No.	Electrical Characteristics			Specification	QPL	Remarks
	w Vdc @ 85°C	Capacitance (μ F) Min.	Max.			
CSR 13	6	5.6	330	MIL-C-39003/1B	QPL-39003	Order to failure rate level "P" or better. These parts must be X-rayed per MSFC-STD-355. These parts must have an effective series limiting resistance of 3 ohms per volt.
	10	3.9	220	↓	↓	
	15	2.7	150			
	20	1.2	100			
	35	5.6	47.0			
	50	0.0047	22.0			
		0.1	15.0			
		0.0047	2.7			
	75	0.1	15.0			
	100	.0047	2.7			

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H. PERSONS CONTACTED

1.	Mr. Abraham Spector, Grumman Aircraft	(516) 575-1132
2.	Mr. Bruce Evans, Martin Marietta	(303) 794-5211, X3251
3.	Mr. Dick Scott, JPL	(213) 354-5750
4.	Mr. Sam Baugh, JPL	(213) 354-2013
5.	Mr. Fred Laracuente, MSFC	(205) 453-3987
6.	Mr. Ben Vizzier, MSFC	(205) 453-3987
7.	Mr. Ed Thornley, TRW Systems	(213) 535-2621
8.	Mr. John Stevens, G.E, Pittsfield	(413) 494-2863
9.	Mr. George Reeder, NAD	(812) 854-1866
10.	Mr. Cliff Montgomery, Boeing	(206) 773-1738
11.	Mr. Jim Stamper, LMSC	(408) 742-2629
12.	Mr. Dan Maciejczak, Hughes	(213) 391-0711, X3317
13.	Mr. Ed W. Nieckula, Autonetics	(714) 632-4792
14.	Mr. Jack Levin, McDonnel-Douglas	(714) 896-3511
15.	Mr. Dave Clamp, Philco-Ford	(415) 326-4350, X4437

VII. ELECTROMECHANICAL RELAYS

by R. E. Cole

VII. ELECTROMECHANICAL RELAYS

A. INTRODUCTION

Electromechanical relays (EMR) have not reached the level of reliability of solid-state devices. If that level of reliability is required, solid-state relays must be used. Circuit design, power systems, thermal systems, weight, etc., must be adjusted for SSR use.

Electromechanical relays can be made more reliable. This chapter will present the best methods in use today and suggest methods which can be used in the future. The emphasis is on long calendar life, although most methods apply to long cycle life as well.

A typical electromechanical relay is shown in Figure 1. The legend or parts list for Figure 1 is presented in Table 1.

B. GUIDELINES FOR LONG-LIFE ASSURANCE

The following guidelines are intended to produce the most reliable relay possible. Single thread reliability for any given time is low. Relay redundancy must be used for high-rel applications.

The chief obstacle to single relay reliability is contamination. Even if cleaning processes could eliminate all outgassing and all particulates, the problem of internal generation of particles, due to mechanical and electrical wear, is still there. The other major obstacle is the vacuum environment of space with which electromechanical devices are inherently incompatible. The fact that this is a secondary problem points to present success in technique to maintain earth environment in space.

1. Design Guidelines

Design criteria are both application independent and application dependent. The criteria are presented under these two groupings.

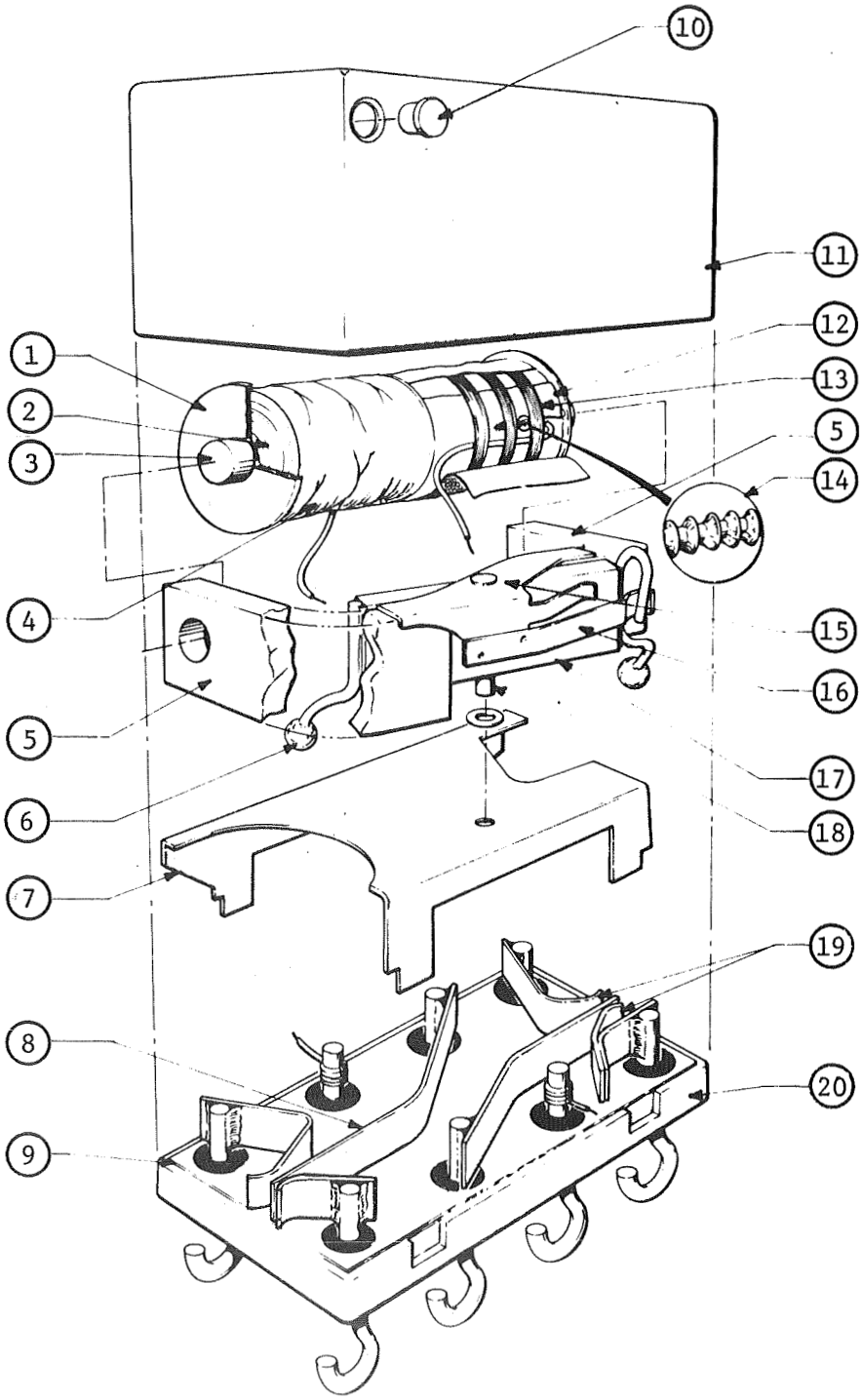


Figure 1 Typical Armature Relay (1/2 Crystal Can)

Table 1 Parts List for Figure 1

Typical Armature Relay Design

ITEM	ITEM NAME
1	Bobbin
2	Magnet Wire
3	Core
4	Insulating Wrap
5	Pole Piece
6	Pusher
7	Frame
8	Movable Contacts
9	Insulation Pad
10	Plug
11	Case
12	Insulating Film
13	Insulating Thread
14	Reinforcing Lead
15	Back Stop
16	Return Spring
17	Armature
18	Pivot
19	Stationary Contacts
20	Header

a. Design Guidelines Application Independent

1) Hermetic Seal - Relays should be hermetically sealed for minimum leakage. Electron beam welding should be used. This type seal has the least leakage and introduces practically zero contamination.

2) Arcing - Minimize arcing in design by increasing contact gap and opening/closing speed. This design requirement takes precedence over miniaturization.

3) Contact Action - Contacts should be designed for a partial wiping action. Partial wiping (0.003") will clean the contacts of small particles, polymers and oxides.

4) Motor Force - The motor should be designed with a 20% force margin at minimum operating conditions. Force margin above 20% does not increase reliability.

5) Getter - Do not use a getter. If cleaning processes and material selection require a getter, the relay is not a high-rel relay. In addition, getters are a source of particulate contamination.

6) Pin Seal - Use compression glass for pin seal. To minimize susceptibility to cracking, undercut the front and back side of header. This will puddle the glass and prevent miniscule creep.

7) Built-In Devices - Do not use built-in devices for ac rectification (coil) or induced voltage suppression. These additional components decrease reliability through particle contamination and outgassing.

8) Armature - Use balanced clapper armature design. Although other designs appear to have higher reliability possibilities (suspended, rotary, diaphragm), each exhibits a weakness which results in less reliability (shock/vibration, particulate susceptibility, hydrocarbon outgassing).

b. Design Guidelines Application Dependent

1) Contact Material

a) For dry circuit to intermediate loads, use gold plating on contacts. The softness and inertness of gold reduces susceptibility to film contamination, which is the primary problem in this load range.

b) For intermediate to high loads, use palladium for contact material. The hardness, high melting point and relatively inert properties reduce the susceptibility to material transfer, erosion and carbon generation which is the primary problem at higher loads.

(Note: Load application (resistive, motor, lamp) and the number of cycles which will be required must be analyzed carefully before the choice is made for highest reliability. The cut-off point is approximately two amperes.)

2) Arcing - Arc suppression circuit design will affect gap, closing/opening speed, contact material and physical size of relay. This must be considered in parallel with relay design parameters.

3) Dual-Chamber Relays - The dual-chamber relay is recommended because it isolates relay contacts from polymers. As polymers primarily affect light circuits, and therefore small relays, their use is limited to this application range, i.e. less than 5 amperes. The cost of dual chamber relays versus parallel relays may be prohibitive.

4) Bifurcated Contacts - Bifurcated contacts are recommended at low and intermediate current ranges since the contact pressure tradeoff is more reliable. Also, certain circuit applications are sensitive to contact bounce. The dual contact can be adjusted for separate resonances, and virtually eliminate energy fluctuation.

5) Spark Arrester - The spark arrester is useful in high load, many cycle applications. However, it is a particle and gaseous contaminant generator; and the reliability tradeoff must be made for contamination failure versus contact to case shorting failure. It is recommended for a large number of cycles and not recommended for a low number of cycles. Approximately 100,000 cycles is the cut-off point (life).

6) Backfill Gas - The tradeoff involved with backfill gas is: inert gas versus a gas with some oxygen for lubrication. Unfortunately, oxygen enhances polymer formation in addition to being an oxidizer. Small-ultra-clean-single-cavity-relays should use oxygen. Small dual-chamber relays should use oxygen in the contact chamber. These relays are more susceptible to sticking from self-adhesion due to the small motor forces and the noble metals used on contacts. There is some evidence that oxygen in larger relays is effective in reducing wear and particle contamination, but it is not conclusive.

2. Process Control Guidelines

a. Coil - Coil wire lubricant is a major cause of hydrocarbon contamination. Wind the coil, using dry wire. This can be done by immersing the spool in a bath of trychlorethylene and wiping the strand during winding.

b. Winding - Coil wire should be pretensioned during winding operations at just below the elastic limit. Scramble wound is preferred, as space factor is just under layer wound, and it is easy.

c. Component Cleaning - All subassembly components (armature, frame, can, contacts, header, pins, bobbin, springs and pins) should be cleaned prior to assembly. The recommended cleaning process is ultrasonic trychlorethylene, GN_2 drying, ultrasonic alcohol, GN_2 drying, ultrasonic distilled water followed by GN_2 drying.

d. Handling - All handling/moving of components and subassemblies should be done with the components sealed in a plastic bag.

e. Degassing - All relays should be subjected to a high temperature, high vacuum degassing process. The vacuum should be less than 5 mm Hg, and the temperature at 200°C for 4 hours minimum. At least one GN_2 purge cycle is recommended. The hydrocarbon outgassing which condenses on the chamber walls should be cleaned after each batch processing.

f. Sealing - The evacuation hole should be sealed with a plug, electron beam welded into place BEFORE REMOVING FROM BACKFILL CHAMBER.

g. Plating - Plating is a major source of metallic contaminants. Avoid plating, if possible. The plating material, electrolyte, temperature, time, etc., should be very precisely controlled. In addition, samples should be analyzed from EVERY plating lot to assure uniformity, adhesion and porosity of plating.

h. Raw Materials - All incoming raw materials shall be subjected to quantitative and qualitative analysis to assure conformity. Do not hesitate to reject incoming materials.

3. Test Guidelines

a. Qualification Testing - Qualification testing should subject the relay to 25% environmental overstress condition, while monitoring relay parameters for out-of-limit conditions and uniformity. Qualification testing limits are established by user application.

b. Screening Tests - Standards for screening tests of all relays have been established. Since many documents describe these in detail, they are listed below without additional description.

1) Pre-Adjust Run-In - 5000 cycles with no contact load prior to contact, contact spring, armature gap, armature spring adjustment.

2) Pre-Can Visual - 100% inspection for particulates prior to canning at 10X magnification.

3) Parameter Tests -

- Contact resistance
- Coil current
- Dc coil resistance
- Pickup and dropout voltage (ambient, 23°C)
- Operate and release times
- Dielectric strength (voltage)
- Insulation resistance
- Leak test, gross and fine
- Miss test (run-in test)
- Mechanical tests (shock, vibration, acceleration)
- Visual inspection

c. Additional Recommended Tests

1) Shock, Vibration and Acceleration - 100% shock, vibration and acceleration at specified levels.

2) *Lot Sampling*

- 5% of each lot be subjected to qualification level (destructive) testing

- 5% of each lot be subjected to long shelf life testing

3) *Particle Detection Test(s)* - Two basic tests exist to detect particulates. Both require the relay to be mechanically agitated. In one, the relay is cycled, and the particulate is captured by the armature or contacts which produces a parametric anomaly. In the other, the energy released by the particulate striking the relay or can is sensed. A variation of either method is to apply a high potential to the case and monitor for a case to relay short.

4. Application Guidelines

a. Determine Type of Load

Resistive

Inductive

Capacitive

Motor

Lamp

b. Determine Type of Power, Coil and Load

Dc

Ac, frequency and number of phases

c. Analyze Load Level

Low level (dry circuit)

Intermediate level

High load level

Worst case load level

d. Define Switching Requirement

Open

Close

Transfer, Form C or D

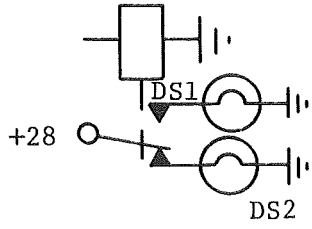
Transfer, center off

Double contact arrangements of above

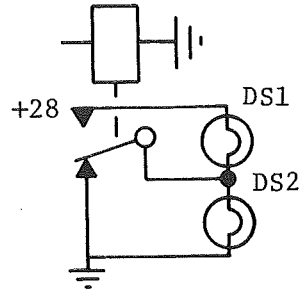
e. Assure circuit in design allows minimum stress on contacts. Consider detailed operation of relay for this. See examples in f below.

f. Application Circuit Examples

Lamp Loads

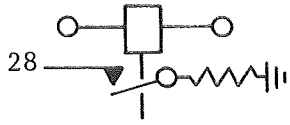


Conventional High Inrush

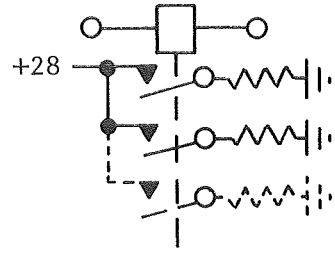


Recommended Low Inrush Circuit

Resistive DC

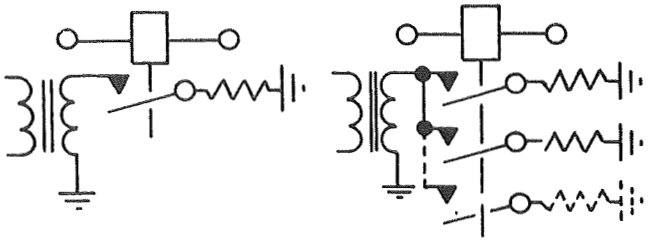


Recommended Single Pole



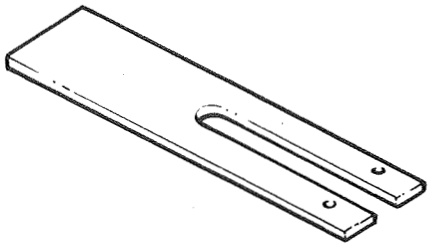
Recommended Multiple Pole

Resistive AC, Single-Phase



Recommended On-Off Switching 115Vac

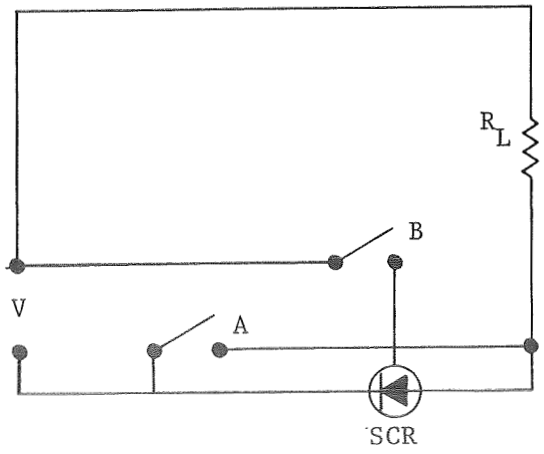
Use Bifurcated Contacts to Reduce Bounce



Bifurcated Contact

g. Hybrid Circuits

Example: Reduce opening and closing contact transients, and subsequent arcing.



B Closes Before A

A Opens Before B

C. LIFE LIMITING PROBLEMS AND SOLUTIONS

1. Failure Mechanism Analysis

The failure modes are fail open, fail closed, intermittent operation and premature. The mechanisms causing these failure modes are presented in Table 2.

a. Non-Metallic Particulate Contamination - There are two sources of non-metallic particulate contamination; those introduced in the manufacturing process, and those produced by the relay itself.

Class 100 clean room conditions will minimize particles introduced from assembly processing. Periodic cleaning during assembly will further reduce these particulates. A final pre-can visual inspection, conducted at 10X magnification, should reduce the quantity to essentially zero.

Internal sources are the bobbin, header seal, spark arrester (arc shield), coil wrap, lead wire insulation, bobbin wire insulation and armature head. The majority of these particles are loose prior to canning. They may be eliminated by cleaning and pre-can inspection. Material selection to reduce susceptibility to particle generation must be accomplished in the initial design.

After canning, screening tests should be used to eliminate relays which still retain loose, non-metallic particulates. It is recommended that these screening tests be the last performed in the entire sequence of acceptance tests.

b. Metallic Particulate Contamination - The primary sources of metallic particulates are the relay itself and in the final canning process. Canning process sources are soldering, welding and sealing. These particulates are solder balls or splash, welding intrusions, or slag.

The relay can produce particles from almost any internal feature; armature, pivot, backstop, frame, springs, contacts, linkage, can and header. Plating from any of these components are also large contributors to metallic particulate contaminations. Design and process control must be the major corrective actions to eliminate this defect.

Table 2 Failure Mechanism Analysis - Electromechanical Relays

Failure Mechanism	Failure Mode	Failure Description/ Functional Response	Method of Detection	Method of Minimizing Defect
a. Non-Metallic Particulate Contamination	Fail Open Fail Close Intermittent	A. Bobbin, header seal, coil wire insulation, arc shield, coil wrap, armature bend. B. Lint, dust, dandruff, hair, etc. High resistance or open contacts, failure to operate.	1. Contact miss during run in and parameter tests. 2. Particle detect tests (variety). 3. Final visual inspection. 4. Failure to operate (large particles).	A. Proper material selection, design clearances, in process cleaning, final visual inspection screening tests. B. Laminar flow benches, clean rooms, "clean" clothing, employee education, in process cleaning, final visual inspection, screening tests.
b. Metallic Particulate Contamination	Fail Open Fail Closed Intermittent Premature	A. Armature, pivot, linkage, frame. B. Solder, weld, can material. High contact resistance (from arcing), failure to operate, failure to de-energize.	1. Contact miss during run-in and parameter tests. 2. Particle detect tests (variety). 3. Failure to operate. 4. Final visual inspection.	A. Material selection and plating processes control. B. Hermetic seal process, restraining design.
c. Gaseous Contamination	Fail Open Fail Closed Intermittent	A. Non-metallic material outgassing. B. Backfill gas impurities. C. Leakage (atmosphere). D. Sealing process (resin).	1. Multi-measurement of pull in parameters for variability. 2. High-low temperature tests to hasten condensation of impurities during run-in tests. 3. Gas analysis.	A. Temperature-vacuum bake-out. B. Backfill gas analysis and meticulious chamber cleaning. C. Leak test and seal process. D. Use EB weld only.

Table 2 (cont)

Failure Mechanism	Failure Mode	Failure Description/ Functional Response	Method of Detection	Method of Minimizing Defect
c. Gaseous Contamination (cont)		E. Contact self-adhesion, motor self-adhesion, high resistance of open contacts, variable contact resistance, variable pull-in parameters (current and time), failure to operate, failure to open.	4. Gross and fine leak tests.	E. Screening test, discrete and statistical.
d. Spring Force Relaxation	Intermittent Premature	Weakened contact springs due to mechanical fatigue or temperature. Contact chatter, transfer, high and/or variable contact resistance.	1. Contact chatter/ transfer during mechanical testing (vibration, shock, acceleration). 2. Lower transfer time. 3. More contact bounce. 4. Lower pull in voltage.	Material selection of spring. Reduced requirements, temperature and/or cyclic Temperature screening.
e. Arcing	Fail Open Fail Closed	Contact opening causes an arc. Contact closure causes an arc. High contact resistance, failure to open or close.	1. Contact resistance measurement. 2. Pull-in voltage measurement. 3. Drop-out voltage measurement.	Assure correct circuit application. Arc suppression devices. Contact material selection. Contact opening/closing speed (snap action). Contact derating.
Shorted Coil	Fail Open	Adjacent coils on bobbin short.	1. Coil resistance measurement.	Quality control of coil wire-insulation.

Table 2 (concl)

Failure Mechanism	Failure Mode	Failure Description/ Functional Response	Method of Detection	Method of Minimizing Defect
Shorted Coil (cont)		High pull-in current, longer pull-in time, can lead to hot spots in coil which open coil. Failure to operate.	2. High potential coil test. 3. Operate time measurement. 4. Operate current measurement.	Screening tests. Process control of winding.

Screening tests should be performed after all other acceptance testing is done. Do not assume screening tests detect *all* the particulates since more will be generated if the design and/or process controls do not first produce a component that is not prone to generation.

c. *Gaseous Contamination* - Contamination of the internal atmosphere of the relay may be produced by a variety of sources: (1) the non-metallic materials used in the relay construction may continue to outgas, (2) hydrocarbons may not be completely cleaned (coil wire oil, body oil, rosin) and will outgas after canning, (3) the backfill gas chamber may not be clean, and may contaminate the backfill gas, (4) the backfill gas itself may contain obnoxious constituents, and (5) either the final sealing process may introduce gaseous contaminants, or the sealing may be done outside the chamber with some atmosphere exchange taking place.

The failures caused by gaseous contamination are: (1) polymer deposit on contacts causing high resistance or open condition, (2) contact oxidation causing high resistance or open, (3) contact or motor parts self-adhering (cold welding) due to lack of appropriate lubricating gas, (4) wear particulates generated by motor parts as a result of lack of lubricating gas, (5) variable contact resistance, (6) variable operate parameters, (7) failure to operate, and (8) failure to open.

d. *Relaxation of Spring Force* - Mechanical fatigue and high temperature cause this problem. Proper design is the only prevention, assuming material control screens unacceptable material. Loss of contact pressure may result in contact failure due to high resistance. The operating failure mechanisms are excessive contact bounce, contact chatter and transfer. Pickup and dropout time and power changes are symptoms of this problem.

e. *Arcing* - Some arcing is desirable for cleaning contacts. Severe arcing will cause complete contact failure, or even welding of contacts in the open (double throw) and closed conditions. Proper design is the only cure, but it *must* be accompanied with complete circuit analysis. Derating of the relay may cure the problem, but the cost in weight and power may be excessive.

Where arcing cannot be eliminated or minimized, the application of a solid-state relay (SSR) or hybrid device should be seriously considered.

2. Design

a. Selection Criteria - Those design factors which contribute to long-life are enumerated in the design guidelines. Prior to choosing an EMR for a switching circuit, SSR versus EMR should be analyzed. An excellent tradeoff criteria discussion is presented by R. Stuart Gibbs in the 19th Annual Relay Conference Proceedings of the NARM. A brief list of these parametric comparisons follows:

1) Life, Calendar and Cycle - Definitely favors the SSR in a properly designed circuit;

2) Reliability - Favors the SSR, but SSR must be built to high-rel guidelines; and the circuit properly designed;

3) Isolation - EMR contacts have highest isolation, and is the largest "plus" for EMR's;

4) EMI and RFI - SSR has the edge, although circuit design and relay design (bifilar coils) can be made comparable;

5) Speed of Operation - SSR;

6) Operate Power - SSR;

7) Shock and Vibration - SSR;

8) Environment - Hermetically sealed EMR's are equal to SSR's, but EMR's have a slight edge in temperature range below -55%C and above +125°C;

9) Contact Voltage Drop - EMR, very large "plus" for EMR's;

10) Transient Effect - EMR; coil on a relay is practically impervious to transients;

11) TTL, RTL, DTL Compatibility - SSR's lend themselves to direct interface with digital circuits;

12) Thermal Power Dissipation - EMR is much better. Largest weakness of SSR's are their inability to dissipate heat;

13) Economics - Today, the EMR is more cost effective in a given application;

14) Size - SSR in microcircuits, the EMR in power circuits. The crossover is about 5 amps today (1972);

15) Human Engineering - EMR: SSR use must be accompanied by considerable circuit knowledge. The EMR is flexible, and more forgiving to mistakes. This adds a large measure of reliability to EMR's.

Specific relay particulars are shown in Table 3, Selection Criteria.

b. Survey Results - The user survey indicated (Table 4) that all relay users are using essentially the same design (see guidelines) and the same screening tests as those described in STR-0001A. The areas of controversy are:

1) Inert backfill versus some oxygen, and;

2) Particle detection screening tests.

As a result, the survey concentrated on these two areas.

Most users are experimenting with oxygen in the backfill gas today (Sandia, North American, Radiation Incorporated, Martin Marietta, McDonnell Douglas, and Grumman). Good results have been obtained (decreased contact and motor self-ahesion), but the long range effects have not been determined. Oxygen is known to contribute to polymer formation (and, of course, is an oxidizer); but if the relays are extremely clean, this effect may take a long calendar time to detect.

Self-adhesion itself will only occur in an extremely clean environment. The question is whether this environment is clean enough to "withstand" a percentage of oxygen. To date, the data is favorable. Oxygen does not seem to be required for larger relays.

For particle detection tests, the two basic types are parameter degradation detection due to particulates, and the direct detection of particulates themselves.

Figure 2 is a schematic of the test setup used to detect parameter degradation. Figure 3 is a schematic of the test setup used to detect particles directly.

Table 3. *Selection Criteria*

ITEM	ADVANTAGES	DISADVANTAGES
Contacts, Gold	Excellent for intermediate circuit levels.	Power circuits, above 2 amps, will erode the gold immediately.
Contacts, Palladium	Excellent for power circuits, resistant to arcing and mechanical wear.	Cannot eliminate films. It is not good for low level circuit application.
Coil, Bifilar	Excellent for inductive suppression.	Weight, additional wire (and oil), slows the dropout time of relay.
Hermetic Seal	Contains atmosphere, seals out contamination.	Seals in any contamination initially present, and prevents any generated contamination from escaping
Getter	Absorbs hydrocarbon gasses and moisture.	Can be a gas generator, and is a particle generator. Generally cannot withstand booster level shock and vibration requirements.
Built-In Devices (Diodes)	Eliminates external wiring and components, therefore, weight.	Source of particulate and gaseous contamination.
Dual-Chamber	Seal the contacts from all non-metallics, which are gas generators.	Larger relay, larger motor, more complicated build and processing.
Bifurcated Contacts	Higher contact reliability, bounce reduction.	Susceptable to film, lower contact pressure, generally large relay; weight and power consumption.
Spark Arrester (Arc Shield)	Prevents material build-up between case (header) and pins.	Source of gaseous contamination and particulate contamination.
Oxygen in Backfill	Acts as lubricant for contacts and motor.	Contact oxidation and polymer forming enhancement.

Table 4 User Survey

PART TYPE	USER	UNIQUE REQUIREMENTS	RATIONALE/JUSTIFICATION
Potter & Brumfield HL & HC, 1/2 Crystal Can Deutsch Blue Ribbon 1/2 Crystal Can General Electric 3 SAM Crystal Can Size, 3 SAV 1/2 Crystal Can Leach, J, K & L, Crystal Can	Lockheed Space Systems Division	Backfill Oxygen - Yes Backfill Moisture - Yes PIND Test - Yes Particle Detect Miss Test - No Bobbin Material - Kel-F Radiflo Leak Test - Preferred Mass Spectrum Leak Test - O.K. Dual-Chamber - No Armature Plating - Chrome Calendar Life - Indefinite	Relays require moisture and oxygen for contact and motor lubrication. Percentages are proprietary. PIND test is excellent, particle miss test is not worth the money. Kel-F is preferred, but Diallylphthallate is okay in some relays. Radiflo leak test is preferred because it detects smaller leaks, but mass spect. method is adequate. Dual-chamber relays not worth the expense. Chrome or bronze plating on armature is okay, depends more on process conyrol. Relay should operate indefinitely in space, until cycle life is exceeded.
Babcock All	Lockheed Missile Systems Division	Backfill Oxygen - No Backfill Moisture - No PIND Test - No Part. Det. Miss Test - Yes Bobbin Material - Kel-F Radiflo Leak Test - Yes Mass Spect. Leak Test - No Dual-Chamber - No Armature Plating - Chrome Calendar Life - Unlimited	Relays should have 100% dry nitrogen for backfill. Definitely no oxygen or moisture. PIND test definitely no good. Particle detect test using sinusoidal vibration is best. Kel-F is a requirement, cannot use Diallylphthallate, reason classified. Radiflo leak check much better than mass spectrometer. Dual-chamber relay is not used, too few of them made. Chrome is best for armatures. Relay life should be indefinite, up until cycle life.

Table 4 (cont)

PART TYPE	USER	UNIQUE REQUIREMENTS	RATIONALE/JUSTIFICATION
None named specifically	NASA Reliability	Backfill Oxygen - No Moisture - No PIND Test - No Particle Detect Miss Test - Yes Bobbin Material - No opinion Radiflo Leak Test - Yes Mass Spectrum Leak Test - O.K. Dual-Chamber - Not enough data Armature Plating - No opinion Calendar Life - No opinion	Relays should have 100% dry nitrogen for backfill. Definitely no oxygen or moisutre. PIND test too subjective, good for large metallic particles only. Particle detect miss test best with random vibration Radiflo leak test definitely superior to mass spect., but mass spect. probably good enough for 5 years. Best plating is no plating. Always subject to flaking.
None named specifically	Federal Electric (NASA)	Backfill Oxygen - No opinion Moisture - Probably need PIND - Yes, reservations Particle Detect Miss Test - Yes Bobbin Material - Kel-F Radiflo - O.K. Mass Spect - O.K. Dual-Chamber - No Armature Plating - No Calendar Life - No opinion	No opinion on oxygen, but probably need some moisture. PIND may be okay if article is quiet and good baseline established, but probably not very good. Particle detect miss test is best. Random vibration quite expensive, sinusoidal correctly chosen for article is quite adequate. Radiflo and mass spect. both accurate enough for space. Dual-chamber relay is good idea, but state-of-the-art not good enough yet. Do not plate at all if can be avoided. Kel-F is best if properly deburned using dry ice (CO_2) in a tumble.
None named specifically. Has used all in last 15 years.	North American Space Systems Division	Backfill Oxygen - No Moisture - No PIND Test - No Particle Detect Miss Test - Yes Bobbin Material - Kel-F Radiflo - No preference Mass Spectrum - No preference Dual-Chamber - No need Armature Plating - O.K. Calendar Life - Indefinite	Relays should use 100% dry nitrogen unless using mass spectrum, then 90% dry N_2 and 10% helium. No oxygen or moisture. PIND test not required, particle detect miss test is best with sinusoidal vibration. But best method to eliminate particles is a thorough pre-can visual inspection. Radiflo and mass spect. Both sensitive enough. Armature plating is okay if right process is used. Regeneration

Table 4 (cont)

PART TYPE	USER	UNIQUE REQUIREMENTS	RATIONALE/JUSTIFICATION
	North American Space Systems Division (cont)		plating (patented) should be investigated. Calendar life should be indefinite as cycle life not exceeded and relay is load cycled occasionally (once a week).
Potter & Brumfield All	TRW Systems Group	Backfill Oxygen - Yes Moisture - Yes PIND - Some Particle Detect Miss Test - No opinion Bobbin Material - Kel-F Radiflo - No preference Mass Spect. - No preference Dual-Chamber - No opinion Armature Plating - O.K. Calendar Life - 8 yrs spec.	TRW specifies 100% dry N_2, but allows some % moisture and oxygen. These percentages are proprietary. Feels the relays need moisture and oxygen for lubrication. PIND test is used on some relays. Feel pre-can visual hurts and does not use it.[1] Bronze, nickel and chrome okay, depends on manufacturer. Minimum life specified at 8 years; three shelf and five space.
Babcock largely uses others. Also Deutsch Dual-Chamber	Sandia	Backfill Oxygen - Yes Backfill Moisture - No PIND Test - No opinion Part Detect Miss - Prefers Bobbin Material - Kel-F Radiflo - O.K. Mass Spect - O.K. Dual-Chamber - Yes, qualified Armature Plating - Chrome Calendar Life - No comment	Oxygen is required if relays are ultra-clean. Moisture not required. Particle detect miss test with sinusoidal vibration probably best test. Kel-F is recommended bobbin material. Radiflo and mass spectrum okay, but both have drawbacks. Experimenting with other backfill gas because of a whisker growth on contacts which requires Radiflo. Dual-chamber relays are more reliable, but cost is very high. Armature plating should be chrome.

[1] TRW believes pre-can visual does more harm than good, allowing potential contaminants to enter. Also, TRW sampling approach is 11% destructive testing.

Table 4 (concl)

PART TYPE	USER	UNIQUE REQUIREMENTS	RATIONALE/JUSTIFICATION
Babcock, Deutsch, Teledyne, Leach	Martin Marietta	Backfill Oxygen - No Moisture - No PIND Test - No Part Detect Miss Test - Yes Bobbin Material - Kel-F Radiflo - Yes Mass Spect - O.K. Dual-Chamber Relays - No opinion Armature Plating - No opinion Calendar Life - Indefinite	Martin specifies 100% pure dry N_2, and does not have any adhesion problems. Experience with the PIND test, to date, has been negative, but possibilities are intriguing and experimenting is proceeding. The particle detect miss test with sinusoidal vibration is considered excellent and mandatory. Kel-F is presently used, although Diallylphthallate is under consideration. Diallyl outgasses more, but has less fiber contamination. Radiflo method is preferred, as it is more sensitive. Calendar life should be indefinite.

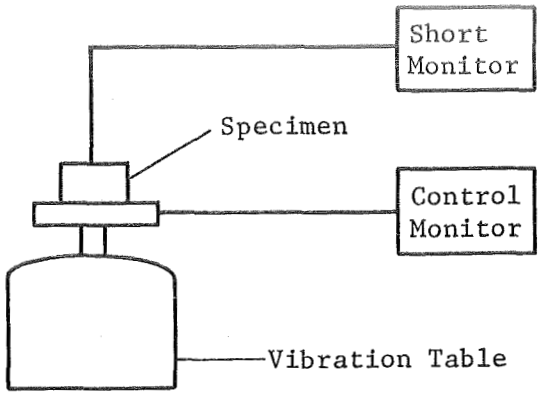


Figure 2 Test Setup to Detect Parameter Degradation

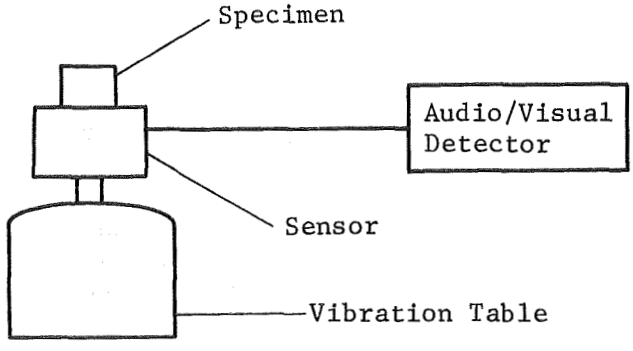


Figure 3 Test Setup to Detect Particles Directly

The following references are recommended for more detailed information:

R. W. Pfeil: "Detection of Loose Particles Within Electric Component Cavities." *Proceedings 1971 Annual Symposium on Reliability*, Lockheed Missiles and Space Company,

Lou Nardo: *Pre-Installation Test Procedure for LM Relays*. Grumman Aircraft Engineering Corporation, #LTP390-103.

Lou Nardo: *Pre-Installation Test Procedure for LM Relays*. Grumman Aircraft Engineering Corporation, #LTP815-31001.

B. T. French and J. E. Mann, North American Rockwell; and G. E. Erickson, Naval Electronics Laboratory Center: *Prediction of IC and LSI Performance by Specialized Vibration/Detection Test for Presence of Conductive Particles*.

Specification for Monitored Vibration/Shock Testing of Integrated Circuits. TR 72-244-043-STFA-30, North American Rockwell.

D. R. Howard: *Attachment 3, Relay Procurement and Control Requirements*. Aerospace Corporation.

c. Alternate Approaches - Presently, the alternate approach to relays is solid-state devices. The primary problem with EMR's is susceptibility to contamination. An area which holds promise for EMR's is the mercury wetted contact design. This would be practically impervious to both particulate contamination and gaseous (chemical) contamination. Mercury wetted contacts have been developed which can sustain some environmental stresses, but an order of magnitude lower than the stresses required for space usage. Research into the area of mercury wetted contacts is needed, as the advantages of EMR's will always be required.

d. Hardware Life - The hardware life specified for today's relays is three to five years usage in space with a shelf life of one to three years. General consensus is that relays not overstressed or overcycled should last indefinitely.

e. Application Guidelines - A primary application guideline is to assure that the relay dielectric strength is sufficient to withstand circuit dynamic voltages. During transient conditions with arcing, the static dielectric strength is considerably reduced.

The circuit application should be thoroughly analyzed for worst case dynamic transients. These voltages, with safety factors, should be applied during *dynamic* testing of the dielectric strength.

The environmental conditions of the application should be used to determine the operate characteristics. The required operate specifications should include the minimum and maximum temperature.

A common misapplication is to use a single-phase multipole relay in a multiphase application. Assure the contacts are rated for multiphase, or use double the single-phase peak voltage to qualify the dielectric under *dynamic* conditions.

For detailed high reliability relay applications, the reader is directed to *Guidelines for Reliable Relay Application and Selection*, compiled in 1969 by L. W. Wendling, Naval Air Systems Command, and E. U. Thomas, Grumman Aircraft Engineering Corporation.

The use circuit is the starting place for relay application. Once the required loads and switching application have been defined, the ratings of Table 5 should be used, as required by MIL-R-6106, as a minimum. For long life application, derating as identified in Volume IV Chapter V is recommended.

D. TEST METHODOLOGY AND REQUIREMENTS

1. Qualification

Qualification tests are performed either to verify a design (Design Development) or to qualify an existing design for usage not specified. Acceptable qualification tests for high reliability parts are identified and described in:

1) *General Specification for Acceptance Testing of Electromagnetic Relays for Use in High Criticality Manned Space Flight Applications*. MSC, Houston, Texas. ST-R-0001;

2) *Screening Requirements for Non-Preferred Electrical and Electronic Parts*. MSFC, Huntsville, Alabama. 85M03876;

3) *Engineers Relay Handbook*. NARM; Scottsdale, Arizona;

4) *Relay Engineering*. Struthers-Dunn, Inc., Pitman, New Jersey.

Table 5 Derating Table

TYPE OF LOAD	LIFE OPERATING CYCLES x 10^3	RATED CONTACT LOAD (AMPERES PER POLE) CASE GROUNDED												See Appropriate Notes
		28 VDC				115 VAC, 1 PHASE				115/200 VAC, 3 PHASE (2)				
		MAIN		AUX		MAIN		AUX		MAIN		AUX		
		NO	NC	NO	NC	400Hz	60Hz	400Hz	60Hz	400Hz	60Hz	400Hz	60Hz	
RESISTIVE	100	10	10			10	5			10	5			
INDUCTIVE	20	8	8			8	2.5			8	2.5			
INDUCTIVE	100	4	4			4	1			4	1			
MOTOR	100	4	4			4	2			4	2			
LAMP	100	2	2			2	1			2	1			
TRANSFER, LOAD														(3)
MECHANICAL LIFE REDUCED CURRENT	400	2.5	2.5			2.5				2.5				
MIN CURRENT		APPLICABLE PER SPECIFICATION												

NOTES, APPLICATION (Note provision for two inductive values.)

(1) Over temperature range.
(2) 115/200 VAC for 60 Hz ratings, absence of value indicates relay is not rated for 3 phase applications
(3) Transfer load indicates relay suitable for transfer between unsynchronized AC power supplies at rating indicated.
(4) Dielectric rating may be improved by suitable insulation of terminals and wiring after installation

There are two test methods which could be applied to qualification testing which are not in general use. One is the force margin measurement which is a measurement of the actual motor force versus the contact force (see Figure 4). This tedious measurement can be simplified to a current versus time measurement (see Figure 5) after the force margin data in Figure 4 have been determined. Qualification of a given relay design would then depend on close tolerance adherence to the N.C. contact opening time and the amount of current recorded at that time. If a given sample exhibits variances of these parameters after other qualification tests (shock, temperature, vibration, life cycle), the relay must be redesigned. Close adherence to designed force margin is required for high reliability.

The second method is based on contact resistance, but utilizes the variance technique to indicate a less reliable design. Two forms of variance should be tested for. One is the spread of contact resistance over a given number of cycles. The spread should be subjected to random analysis, sigma computed. If this exceeds a specified sigma value, a redesign is called for (contact pressure, contact material, contact "wiping", etc.).

The other form of variance is an extra lump, or two peaks in the random distribution curve. This is caused by foreign material of some sort at the contact (polymers, hydrocarbons due to arcing, or burn through to base metal). The variances are small, thus the cause of variance is small, and is probably not detectable by other means.

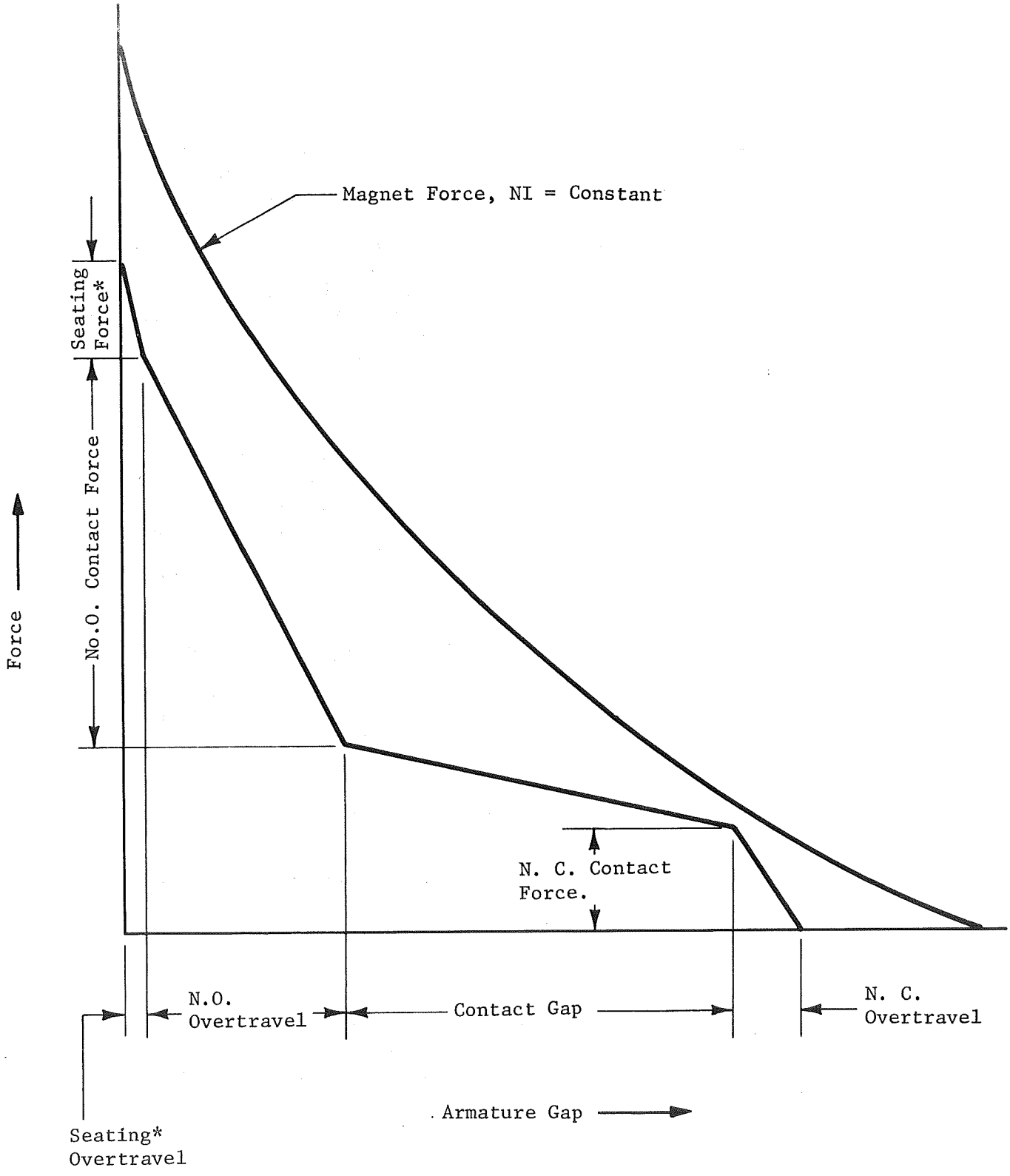
Both of these methods lend themselves to effective screening tests, and are recommended.

a. Accelerated Testing - There is no recognized method for accelerated calendar life testing being used in industry today.

2. Life Test

Relays are subjected to two types of life tests. One, the cyclic life test, consists of cycling the relay under load until failure. The failure mode is almost always contact failure. The other test is a lot sample, subjected to parameter tests at discrete time intervals. This is a "real time" life test, and normally is conducted in parallel with relay usage.

Sampling techniques for both of these tests are identified in MIL-STD-105, MIL-R-6106, and ST-R-0001A.



*should be reduced to 0 after wear-in.

Figure 4 Force Margin Measurement Test

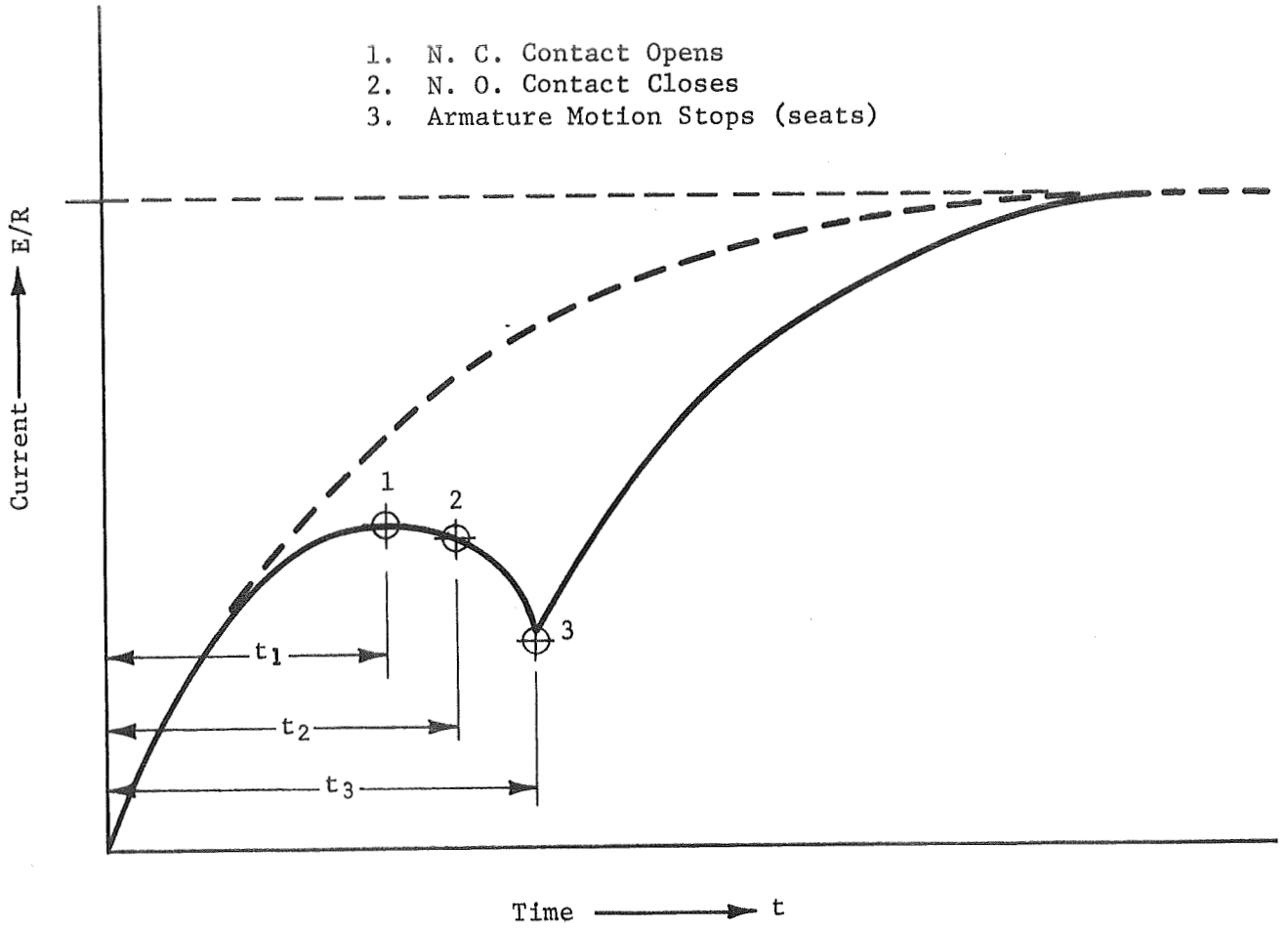


Figure 5 Current vs Time Measurement

3. Screening Tests and Failure Mode Detection

Standard screening tests are identified in ST-R-0001A, *Engineers Relay Handbook* and *Relay Engineering Handbook*.

Several techniques not in popular use today, which have potential, are the two qualification methods described earlier, and neutron radiography for detection of non-metallic particles.

Two techniques, sporadically used throughout industry, are methods for particle detection. One method enhances conditions to detect the failure mode, the other detects the mechansim which would lead to a failure.

Particles are detected by operating the relay until a particle either becomes lodged and causes a motor jam or lodges between contacts and causes a "miss" (failure mode). The controversial area is the method used to agitate the relay to cause the particulates to move. Random vibration, cyclic sine wave vibration and cyclic sine wave vibration with periodic shock pulses to enhance particle motion are all in use at present. (Shock is presently used on canned IC's only, not on EMR's, but is under investigation for EMR's.) This particle detect test is further enhanced by placing a potential (200V dc) on the relay can/header and monitoring for a short which would be caused by a conductive particle. This method is in use by at least two companies - Grumman Aircraft and Martin Marietta Corporation.

Martin Marietta Corporation investigated radiation as a means to discharge electrostatically charged particles. Gamma radiation of 1500 milliroengtens and beta radiation at 0.005 milliroengtens were used. Samples were acrylic particles (0.0005" - 0.015") clinging to a metallic plate with electrostatic charge. No dropping of particles occurred with 3 hours of continuous radiation. Higher levels of radiation and/or longer time periods may have some effect, but these approaches are not practical.

Another method is to place a high potential on the contact in the open position only. (This would be reduced to the contact monitor voltage just prior to closure.) The increased potential should assist attraction of electrostatically charged particles to the contacts, if the particles exist. Martin Marietta Aerospace is presently investigating the feasibility of this approach.

Particles can also be detected by agitating the relay and sense particle impact energy (failure mechanism). The method in use today was perfected by Rod Pfeil at Lockheed Missiles and Space

Company. This method uses a microphone to detect ultrasonic acoustical energy released as the particle impacts. This energy is translated to the audio range and broadcast while being simultaneously displayed on a cathode ray oscilloscope. This combination of information enables an experienced operator to detect a particle.

The above test, called the "Particle Impact Noise Detection" test (PIND), has two weaknesses. One, if the relay has loose parts, the noise generated by the parts tends to mask any particle noise; and two, the test is sensitive to metallic particles only.

The user survey indicates mixed feelings about the test in the area of operator subjectivity. A survey preference yields:

MSC	- Particle Detect
MSFC	- Particle Detect
LMSC	- PIND
Grumman	- Particle Detect
Martin	- Particle Detect
Sandia	- Neither
North American	- Particle Detect
Aerospace	- PIND
TRW Systems	- Neither

E. PROCESS CONTROL REQUIREMENTS

(See Process Flow Chart, Figure 6, example.)

1. Existing

The process controls identified in the accompanying flow chart are used by all high-reliability relay manufacturers. Precise sequences, cleaning fluids, vary, but in principal they are the same.

Needed

The most urgent need today in relay manufacturing is a total Class 100 environment. Particulate contamination is the major cause of failures. Pre-can visual and post-can screening tests have reached a limit. Very little more can be done practically.

Another factor which appeared frequently during the user survey is a concern with the manufacturers, and manufacturing personnel. As Aerospace and Military high-rel relay contracts have fluctuated, experienced personnel have been lost. In one instance, a ground equipment circuit had to be redesigned, as a specific relay could not be obtained. The manufacturer could not produce it as "the personnel with the capability to adjust that relay" were no longer with the company.

The other factor was the reduced quantity of high-rel relays being used. This is due to more SSR application, and the reduced number of contracts. In short, a "need" in the area of process control is steady, long run production contracts. Small, infrequent orders for high-rel relays are inconsistent with high-rel requirements.

PARTS LIST

The following is a partial list of acceptable part numbers. A considerable number of Military/Aerospace relays are made-to-order, and are not listed in vendor catalogs.

Acceptable:

Number	Manufacturer
BRJ26CD1H6A5-1	Deutsch
ER-WKJR-6D-26.5	Allied Control
814C2	Leach
49-3179	Cutler-Hammer
A410-151171-01	Guardian Electric

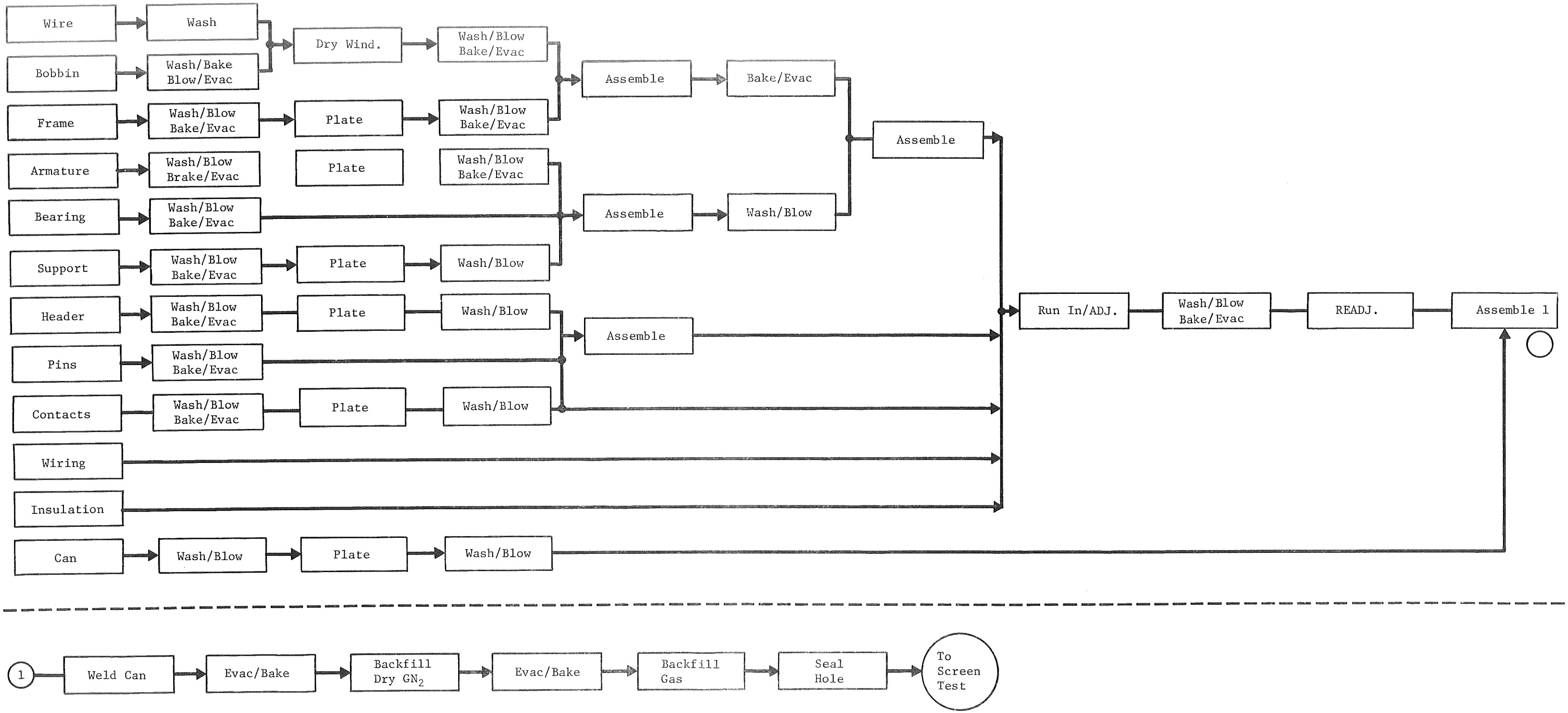


Figure 6 Typical Relay Assembly Process Flow

GRY-14-410-4001	Giannini Voltex
PTZ-1034-XXX	Potter-Brumfield
FCM-410-60	Struthers-Dunn
CR2791G121AT1	General Electric
5715-184PX	Price Electric
PR9405	Phaostron Company
A-711JC	Hartman Electric
1904B2-4-A-110(1)	Electronic Speciality
585	Piqua Engineering

2. Not Acceptable:

Most companies carry a commercial product line. None of those relays are acceptable.

G. BIBLIOGRAPHY AND CONTACTS

1. Bibliography

1) *Pre-Installation Test Procedure* LTP390-103, Grumman Aircraft Engineering Corporation.

2) R. W. Pfeil: *Detection of Loose Particles Within Electric Component Cavities*, Lockheed Missiles and Space Company.

3) G. E. Ereckson, B. T. French and J. E. Mann: *Prediction of IC and LSI Performance by Specialized Vibration/Detection Test for Presence of Conductive Particles*, Naval Electronics Laboratory Center and North American Rockwell.

4) NARM Proceedings, 1st through 20th Symposium papers.

2. Persons Contacted

1) Hal Block, North American Rockwell, Autonetics.

2) Bell Steward, NASA-MSC.

3) Tom Hooper, Federal Electric, MSFC.

4) Jack Mann, North American Rockwell, Autonetics.

5) Rod Pfeil, Lockheed Missiles and Space Company.

6) Ed Freirria, Lockheed Missiles and Space Company.

7) Hugh Heritage, Aerospace Corporation.

8) A. B. Oden, Aerospace Corporation.

9) Charles Murphy, Boeing, MSC.

10) Lou Nardo, Grumman Aerospace.

11) Edgar Jones, North American Rockwell.

12) Jack Brown, Babcock Relay Corporation.

13) Harold Greenberg, TRW Systems.

14) C. Bates, Sandia Corporation.

15) C. Schumaker, Martin Marietta

VIII. SWITCHES AND CIRCUIT BREAKERS

by R. Q. Jackson

VIII. SWITCHES AND CIRCUIT BREAKERS

A. INTRODUCTION

This chapter presents the guidelines and rationale for reliable, long-life switches and circuit breakers. A major concern with switches is contamination, both particles and contaminant films on contacts. Circuit breakers are less prone to failure from contamination, but are more prone to mechanical failure due to the complexity of some actuation mechanisms. The storage life of switches and circuit breakers exceeds 10 years when the devices are hermetically sealed and internal non-metallic materials are eliminated, or if very stable materials are used. The state-of-the-art cycle life is about 100,000 actuations for switches and 10,000 actuations for circuit breakers. Switches and circuit breakers with less cycle life capability are acceptable when the mission requirement is significantly less than the cycle life capability.

Current developments in solid-state circuit breakers should be continuously reviewed and solid-state circuit breakers used when permitted by availability and application, since they are not subject to wear out or the failure modes inherent in complex mechanical devices.

B. GUIDELINES FOR LONG-LIFE ASSURANCE

1. Design Guidelines

1) Use hermetically sealed, metal enclosed switches. Accomplish the seal by electron-beam welding. Soldering or non-metallic sealers introduce both particulate and gaseous contaminates.

2) Use either a metal bellows or metal diaphragm for the seal around the activation mechanism. Do not use an elastomer seal. This metal seal should also be accomplished by electron-beam welding.

3) Circuit breakers are, typically, not hermetically sealed, but sealed devices should be used if and when available.

4) The contacts should be alloys of nickel, silver or palladium for loads greater than 500 milliamperes. For loads less than 500 milliamperes, the contacts should be gold plated to minimize oxide films and maintain low contact resistance.

5) The minimum thickness for gold plating is 0.000100 inch. Thinner platings may burn through. Thicker platings are neither necessary nor cost effective.

6) The contact gap should be sufficient to extinguish the maximum designed power arc. This consideration is most applicable to very small switches, such as reed switches.

7) Snap-action switching of contacts should be designed in the mechanism to minimize arcing time which increases contact life.

8) Contacts should have a partial wiping action (.300" to .005") to disrupt oxide films. Greater wiping lengths will introduce excessive wear.

9) External electrical terminals should be sealed with glass with a matched thermal expansion coefficient for strength, dielectric and gas seal qualities. Other methods such as alumina, ceramic sleeves, and brazing are under development but should not be used until the process is developed and proven.

10) Solid-state circuit breakers, currently under development, are preferable to mechanical circuit breakers since they are not subject to wear-out or the failure modes inherent in complex mechanical devices.

11) Solder hook external contacts are required to provide stress relief to the glass seal. Plug-in units are not recommended because the glass seal may be stressed.

12) Getter devices should not be used. They may break or move and interfere with switch operation. Switches must be clean enough without a getter or they are not reliable parts.

13) Avoid plating of internal parts. Plating is a major source of metal particle contamination.

14) Minimize the use of non-metallic materials because they are prone to outgas, are a source of particulate contamination, have a normally lower mechanical strength, are more temperature sensitive, and do not have the long term stability of metals.

2. Process Control Guidelines

1) All switch assembly should take place in a Class 100 clean room environment to preclude particulate contamination; an extremely serious problem.

2) The transfer of switch components between assembly stations should be accomplished in sealed plastic bags to reduce contamination.

3) Vacuum bake-out of switches should be conducted at 200°C, 1 mm pressure for a minimum of four hours to prevent subsequent contaminating films of non-metallic materials. Some components may require as much as 16 hours, two cycles. One purge cycle with dry GN_2 is recommended as a minimum.

4) The out-gassing hole in the switch enclosure should be sealed in the backfill chamber, or an adjacent chamber common to the back-fill chamber to prevent contamination.

5) The back-fill and bake-out chamber should be cleaned after each operation to remove hydrocarbon (oil) condensate from chamber walls.

6) During assembly, each mechanism piece should be checked against the installation print for proper installation. A go/no-go test should be made for every clearance specified, with no hindrance of motion.

7) Plating of piece parts should be avoided. Where unavoidable, the plating process (temperature, raw metal purity, bath cleanliness, voltage stability, etc.) should be continually monitored and controlled. In addition, destructive parts analyses should be conducted on 5% of the piece parts to verify plating adherence, absence of cracks, and the achievement of a fine-grained structure.

8) Cleaning baths should be constantly filtered and recirculated with approximately a 20% replacement after each cleaning process.

9) Incoming material inspection should be on a sample basis as a minimum and should verify materials, dimensions and tolerances as well as workmanship. Materials should be stored in contamination protected containers or bags.

3. Test Guidelines

1) Qualification and acceptance (screening) testing should be accomplished using MIL-S-8805 for switches and MIL-C-39019 for circuit breakers as a minimum. Additional program peculiar requirements should be added as required.

2) For acceptance testing of production hardware, the above specifications are inadequate in certain areas and, therefore, must be supplemented with the following inspections and tests.

3) Radiographic inspection on 100% of the devices should be accomplished in accordance with more comprehensive inspection criteria such as MSFC-STD-355C to detect contamination, bent parts, and misaligned parts.

4) For switches, an operational run-in (2000 cycles of operation at -65°C, 2000 cycles at +125°C, and 500 cycles at +25°C) should be conducted as a 100% screening test. The voltage drop across the contacts should be monitored during cycling and the electrical characteristics measured after the test. For circuit breakers, the run-in should be performed using 200, 200, and 50 cycles at the applicable temperatures, and with verification of calibration consistency. The values of 2000, and 200, are upper limit values which should be reviewed for reduction to avoid wear-out of some shorter-life devices.

5) Seal tests should be performed on 100% of the devices to verify the seal integrity.

6) A sinewave vibration test of 30g's, 5-2000 Hz, should be conducted as part of 100% screening with contact resistances monitored during the test to insure the absence of contact chatter and transfer. During vibration, both switches and circuit breakers should be monitored for a short to case condition, as well as other parameters.

7) A particle contamination test should be performed as a 100% screening test. The (PIND) test per LMSC specification 1420833 is recommended. The Raytheon developed particle detection test has some technical advantages, such as better detection of smaller non-metallic particles. However, this test is more time consuming and costly and, therefore, most part specialists consider the PIND test as more cost-effective.

8) Accelerated testing is basically accomplished by the run-in testing described above. However, one variant which should be considered for selective application is the exposure of the non-operating device to high temperature followed by operation under a very light load to establish that outgassing of inorganic material has not produced a contamination film on the contacts. This accelerated test approach is aimed at a final verification of the adequacy of the bake-out processes.

4. Application Guidelines

1) Current should be derated as follows:

Type of Load	Percent of Manufacturers Rating
Resistive	75%
Inductive	40%
Motor	20%
Filament	10%
Capacitor	75%

2) When estimating life cycle requirements, avoid a false life assessment. Count the total cycles to be accrued in acceptance testing and prelaunch checkouts, in addition to the mission usage cycles.

3) Switch applications in digital circuits must be carefully reviewed to assure that contact bounce or chatter will not be interpreted as a circuit interruption which will produce logic errors.

4) Switches and circuit breakers are subject to contact chatter in high shock and vibration environments, and these environments may dictate the use of solid-state devices. The mounting of switches and circuit breakers should be designed to minimize vibration and shock amplication or to provide the necessary isolation.

5) Where a circuit breaker hang-up or failure to trip can jeopardize the mission, redundant circuit breakers should be used. On the Skylab Program, this is accomplished by having circuit breakers in the various branches of the power distribution tree.

6) Contacts may be paralleled to reduce the effects of contact bounce and vibration, and for redundancy. This purpose has been achieved using bifurcated contacts. NOTE: Do not parallel switch contacts to increase current breaking and making capability. One set of contacts will close first and carry excessive load.

C. LIFE LIMITING PROBLEMS AND SOLUTIONS

1. Failure Mechanisms Analysis

The failure mechanisms of switches and circuit breakers are listed in Table 1. The failure modes are opens, shorts, intermittants, and failure to operate. The failure mechanisms most frequently encountered are discussed as follows:

1) Deformed Contacts

Deformed or misadjusted contacts found in a complete assembly are a result of poor manufacturing and inspection practices. The manufacturing production line should be operated so that periodic inspection stations are employed as a part of each switch build cycle. Each inspection station should:

Verify piece part design conformance.

Verify assembly fit, placement and interface tolerances.

Verify subassembly and assembly mechanical function to closure.

2) Loose or Broken Contacts

Loose or broken contacts are caused by inadequate welding to the header, frame or support bracket, excessive shock and vibration during handling, or lack of assembly controls. Good process control, inspection, and controlled handling will eliminate these failures.

3) Termination Separation

Termination separation is a result of inadequate wire or terminal routing clearances which can result in actuation mechanism interference, sharp bend radii which can result in

Table 1 Failure Mechanism Analysis - Switches and Circuit Breakers

FAILURE MODE/MECHANISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Open/Short			
Deformed Contacts	Poor process control.	Visual inspection, x-ray, electrical parameter deviation.	Improved process controls.
Loose or Broken Contacts	Poor process control.	Visual inspection, x-ray, electrical parameter deviation.	Improved process controls.
Termination Separation	Defective welds or solder joints. Poor wire stress and routing.	Visual inspection, electrical parameter deviation.	Improved process control, soldering and welding.
Contamination	Solder flux, film on contacts, loose particles, oxides sulfides, sealing cement, cleaning residue.	Particle detection tests, x-ray, electrical parameter deviation.	Clean room assembly, electron beam welding, particle detection and x-ray screen testing, controlled cleaning methods, internal visual inspection, use of materials that do not outgas.
Contact Corrosion	Sulfides, sulfates, chlorinates, impurities, moisture, salt-laden atmosphere.	Electrical parameter deviation.	Outgas by baking at high temperature, use hermetic seal. Use contact materials that are resistant to oxidation, such as gold, platinum, palladium and their alloys.
Parameter Deviation			
Operating and Release Force Incorrect	Mechanical misalignment, contamination, loose or defective parts, wear.	Visual inspections, functional tests, x-ray.	Improved production control, inspections, and tests.

Table 1 Failure Mechanism Analysis - Switches and Circuit Breakers (cond)

FAILURE MODE/MECAHNISM	DESCRIPTION/CAUSE	DETECTION METHOD	METHOD TO MINIMIZE OR ELIMINATE CAUSE
Parameter Deviation (cont)			
Operating Displacement of Activating Mechanism Improper	Loose or defective parts, inadequate heat treatment.	Visual inspections, functional tests, x-ray.	Improved production control, inspection, and tests.
External Failure Mechanisms			
	Poor terminal plating, incorrect case dimensions or termination spacing, encapsulant on terminals, damaged or loose terminals, defective hermetic seal, cracked terminal beads.	Visual inspections, functional tests, physical measurements.	Improved production control, inspections, and tests.

breakage of wire, defective solder joints, overstressed solder joints, or defective welds, due to contaminated parts, or lack of weld schedule control.

Routing clearances and bend radii must be established by design and enforced through control inspection stations. Cold solder joints will be prevented by employee education (NASA Solder Certification), and inspection. Stressed solder joints are prevented by incorporating lead stress relief. Weld adhesions will be obtained by empirically determining the precise weld schedule, and maintaining continual control of the weld schedule. Use of power regulation inside the factory to minimize the effect of line variations, and thorough cleaning of individual piece parts by ultrasonic baths is desirable.

4) Contamination

Contamination is the major problem in switches. Films and oxides can form on contacts' surfaces and create a high resistance. Loose metal particles can become lodged between linkage members and render the switch inoperative or adhere to open contacts and create a short. The control of contamination must be a consideration in every step of the production process and should include cleaning baths, visual inspection stations and incoming materials control. Contamination can be minimized in the switch assembly by performing the assembly in a Class 100 clean room. Neither the Raytheon developed particle detection test nor the Lockheed PIND test are 100% effective as screening tests and; therefore, every practical means should be employed in initially fabricating switches which are clean.

5) Contact Corrosion

It is a failure mechanism due to external sulfides, sulfates, chlorinates, moisture and salt, and internal impurities from outgassing of non-metallic materials, solder resin, body oils, and wire lubricants. The failure mode is high contact resistance and opens. The enclosure must be sealed by electron beam welding to reduce external corrosive contamination. The cavity must be cleaned, vacuum baked, and back-filled with GN_2 to minimize internal corrosive contaminates. Contacts must be made of materials impervious to chemical oxidation and reduction for further resistance to corrosion. Gold, platinum, silver, nickel, pelladium, and their alloys are successful contact material deterrents to corrosion.

6) Incorrect Operating and Release Forces

Incorrect operating and release forces are failure mechanisms that cause false switch operation or failure of the switch to operate. This mechanism is caused by mechanical misalignment of actuation mechanism members, contamination, loose or defective parts, excessive wear on parts improperly installed, and corrosion. The methods to detect this mechanism is through functional testing and measurements. The most effective means to eliminate this mechanism is by improved production controls.

7) Improper Operating Displacement of the Activating Mechanism

Examples of these failure mechanisms are, a toggle lever that has improper travel, a push button that does not move under its designed load, a rotary switch with no detent or stops, or a rocker that does not actuate its switch. These anomalies are caused by the use of incorrect parts, omitting a spring member, failing to captivate the actuation spring, or particles which become lodged in the mechanism and render it inoperative. Improper heat treatment of actuation parts will cause premature failure due to breaking or bending of parts when stressed during operation. Switches built using the incorrect parts can cause excessive force and wear on contacts which will reduce their useful life. These causes are detected by functional testing and measurements. The actuating force, lever travel, pre-travel, overtravel, changes in contact resistance, loss of insulation resistance are effective detection methods. The method to eliminate the causes is improved production control, especially of the production build cycle which is to include periodic inspection stations to assure correct and proper build schedules.

8) External Failure Mechanisms

The failure mechanisms associated with the external portions of a switch follows. These failure mechanisms can be detected by visual examination, physical measurements and electrical parameter tests. These mechanisms may be eliminated by employing improved production controls, inspections, in-line testing and stringent final acceptance testing.

Poor terminal plating causing loss of electrical continuity.

Incorrect case dimensions causing operational interference with the actuation mechanism.

Binding of the movable contacts causing excessive force to operate the actuation mechanism and breakage of internal parts.

Terminal spacing that is too close that will make terminating of leads difficult and can cause damage to the adjacent terminal or create a shorted condition between leads.

Damaged, loose, corroded or dirty terminals are contributing causes of electrical discontinuity.

2. Design

a. Selection Criteria for Switches - General guidelines for the selection of reliable, long-life switches are presented in Table 2. There is an enormous variety to choose from which may be used in many different ways. It is necessary to be familiar with the principal types and the considerations guiding switch selection in order to optimize system design. Many switch types are custom designed for specific applications. Particular attention must be directed toward the switch application and its environment.

Special switches and RF switches are not considered in this report. Examples of these types are: Mechanical-actuated switches, temperature-actuated switches, proximity-actuated switches, and pressure-actuated switches.

The design considerations for the switch enclosure, contacts, and actuation mechanism are discussed in the following paragraphs.

1) Enclosure - Switches may be purchased either open, enclosed for shielding, enclosed for dust and moisture protection, or enclosed using a hermetic sealing technique which provides the maximum switch protection. In applications where long-life and higher reliability are required, the hermetic sealed enclosure is recommended.

Hermetic sealing should be accomplished by electron beam welding to eliminate the introduction of solder balls, solder flux, or other contaminants. The enclosure materials should be a durable metal/alloy such as nickel alloy, tin plated. Metals of cadmium or zinc are not to be used in parts for space applications because they sublimate under vacuum conditions.

Table 2 Design Factors for the Long-Life Assurance of Switches and Circuit Breakers

Design Factor	Remarks
Enclosure	Use hermetically sealed switches where the seal has been accomplished by electron beam welding to eliminate solder and solder flux contamination; backfill the cavity with a dry, inert gas. Hermetically sealed circuit breakers are desirable, but may not be available.
	Use corrosion resistant metals. Do not use cadmium or zinc.
Contacts	Switch contacts for loads less than 500 milliamperes should be gold plated. Contacts for greater loads should be alloys of nickel, platinum, silver, or palladium. The contact gap should be sufficient to extinguish the arc. Contact operation should have a wiping action to clean the contact surfaces.
	In circuit breakers, the arc path should not be on the mating surfaces.
Actuation Mechanism	Teaseable switches should not be used.
	Spring members should be securely captivated.
	Spring members should have a low hysteresis and adequate fatigue life.
	Use snap action mechanisms to decrease arc time and increase contact life.
	The design should not be sensitive to mounting direction. In high vibration environments, center-of-gravity mountings are preferred.
	Internal connections and wires should be placed to prevent possible interference with moving parts.
	Non-metallic materials and lubricants should be minimized to the maximum extent practicable.
	Lubricants and non-metallic materials should be reviewed to assure that they will not outgas and contaminate the contacts.
	Select circuit breakers with the simplest mechanisms. Avoid complex mechanisms.
General	Avoid plating on internal parts.
	Avoid getter devices.
	Select designs least susceptible to contamination.

Some hermetically sealed switches are back-filled with an inert gas, usually nitrogen, depending on the switch requirements and the manufacturer, to provide a more controlled environment that aids in providing a longer switch life.

Terminals should be adequately spaced and designed to reduce strain on the glass header. Coefficients of thermal expansion between glass and metal should be matched.

There are many applications where a numerical letter or written display is needed with a switch operation, such as on a display panel. These switches may be enclosed with either an environmental seal or the basic switch unit may be hermetically sealed and the display and actuation mechanism attached to the switch as the application dictates.

Careful attention should be directed to the vibration and shock requirements the switch may experience to avoid chatter and transfer problems. In high vibration environments, highly cantilevered designs can have a high vibration amplification.

In some cases it is desirable to locate the mounting hardware at the center of gravity of the switch to lower vibration amplification.

2) Contacts - Contact materials are an important concern, especially for extended life applications. The metals commonly employed are platinum, palladium, silver, nickel, and gold. Many manufacturers consider their contact material and controls proprietary; therefore, a specific contact material is not recommended. The harder alloys that provide long wear characteristics and reduced oxidation properties are the most suitable. Gold plated, or gold alloy contacts, are preferred for low current (dry circuit) switching applications. Self-cleaning designs are recommended. Self-cleaning is achieved by a wiping or sliding action of one contact over the other during the switching operation. An extreme example of this action would be a knife-blade type switch. Overtravel can provide the necessary wiping action to aid in contact cleaning. This type action helps break through films and oxide layers on the contact surfaces. The film may be sulfides, sulfates or chlorinates of the contact material, as well as impurities, such as water/oil vapors dust, dirt and other contaminants.

Contact bounce is associated with the switch mechanism design rather than the contact design. It should be carefully considered, especially in those circuits where digital logic pulses are involved. Contact bounce can easily appear as a switching operation, depending on circuit response time. Proper switch selection for the intended application is required.

3) Actuation Mechanisms - The actuation mechanism (the assembly, or part which maintains and changes the movable contacts' position) should be of simple design and provide for mechanical advantage, especially if the switch is hand operated. The snap-action actuation is preferred. Snap action provides a fast break and fast make operation. This decreases the contact arc time and yields longer contact life. Switches which have "teaseable" actuation should not be used. Teaseable action is where a set of contacts may be opened and closed again without completing a switch operation. A switch operation is, for example, where a toggle lever is moved from "normally open" to "normally closed", or from "off" to "on." This teaseable action is not to be confused with a momentary action switch.

For long-life, spring members should be designed to work well below the yield strength. Precise values were not established in this study, but it appears that less than 50% of yield is desirable.

All internal parts should be designed and installed so there is little possibility of becoming detached. Internal parts should be positioned to eliminate any possible interferences, either initially, or with aging and wear. Non-metallic materials such as plastics and lubricants should be eliminated to the maximum extent practicable since such materials lack the long-term stability of metals and they are potential sources of outgassing that could produce a contaminating film on the contacts. Plating of internal parts is a source of contamination and should be avoided.

Rotary switches should have a detent or spring locking device to maintain the selected position. The moving mechanism, and contacts, should be constructed such that bridging from one pole to the next on a break-before-make design does not occur with normal wear. When accessories, such as boots, mechanical locks or levers, identification, knobs, linkages, shields, etc., are used, they should be assembled such that they do not inhibit or alter the switch operation.

b. Selection Criteria for Circuit Breakers - General guidelines for the selection of reliable, long-life circuit breakers are presented in Table 2.

Electromechanical circuit breakers are, for the most part, of three basic types. The thermal circuit breaker is actuated by a temperature change of a bimetallic element. The thermalmagnetic circuit breaker type operates the same way up to the point of opening. At this point, a magnet assists the bimetal element in tripping the contacts open. The hydraulic-magnetic circuit breaker type has a solenoid with a dashpot time-delaying element. Changes in current changes the magnetic field which, with an increase, moves the trip lever. If the current increase is slow, the iron core in the solenoid moves against the damping fluid and increases the magnetic field to cause the trip lever to close which opens the contacts.

The thermal and thermal-magnetic breakers depend upon heat for tripping and, therefore, there is very little difference in their characteristics when used on 60 Hz or direct current. The hydraulic-magnetic breaker has a different ampere-turn ratio for ac than for dc, and therefore they should be used with their respective types of current. The typical response, short time, is at approximately 100-200% of rated current. However, time-delay breakers may not respond until over 1000% of rated current, depending on the design.

A valuable feature for circuit breakers is a contact arc damping or arc interruption. One system uses a contact breaking system such that the arc drawn does not take place on the contact mating surface. Another system uses an arc breaking device to break the arc up into a series of small arcs.

Where a breaker is used in switch applications, arc protection is of significant value. The snap action decreases arc time and thus increases contact life. Also, the wiping action or self-cleaning of the mating surfaces as the contacts mates, is recommended to keep the contacts clean and break up the films and oxides that form on the contacts from impurities. Environment resisting circuit breakers and their parts are necessary for long-life applications. Breakers should have fungus-resistant materials, explosion-proof sealed enclosures and be resistant to vibration, shock, moisture, salt spray, sand, dust, heat and altitude.

The selection criteria previously discussed for switches, is for the most part, applicable to circuit breakers. However, one significant distinction should be made. As compared to switches,

circuit breakers are less susceptible to failure due to contamination, since they usually handle much higher current levels and are normally closed. On the other hand, they are much more susceptible to failure of the actuating mechanism, since the mechanisms are not only much more complex, but wear and fatigue from high impact loads becomes a factor.

There is a large variety of circuit breaker actuation mechanisms. They vary from the simple series trip mechanism to remote operated and special transient overvoltage-overcurrent mechanisms. For long-life use, the least complex mechanism that will do the required job is recommended. Because of the failure risk inherent in the actuating mechanism, the preferred design is the design which can still operate satisfactorily with some wear, and despite tolerance stack-up problems, or nominal variations in the dimensions of the many parts and linkages. A selected circuit breaker should have the reliability of the mechanism already well established by test programs and by successful prior usages on other programs.

c. Results of Industry Survey - An industry survey failed to identify any new or unique test approaches for switches and circuit breakers. The practices of vibration screening and x-ray inspection, listed in Table 3, are conventional, not new or unique, approaches.

d. Alternate Approaches - Solid-state circuit breakers do not have wear out failure modes, and have a much greater potential for long-life and high reliability. Hence, the use of a solid-state device is preferred whenever an appropriate device has been developed and proven. The interest for using solid-state circuit protection or power control has created recent activity in aircraft and spacecraft applications.

There are several development projects presently under way to design solid-state power control systems and power sensing systems with remotely variable sensing and control. Westinghouse and Spacecraft have developed solid-state power controllers for evaluation; however, they are not producing the devices at this time. The Leach Corporation has developed a remote power controller capable of handling 1 ampere to 35 amperes dc and are in the process of qualifying it to MIL-P-81653. Flight Systems, Inc. has a solid-state circuit breaker rated from 0.5 to 1.5 amperes and which weighs less than 3 ounces.

Table 3 Survey of Part Users

Part Type	User	Recommended Specification Requirements	Rationale
Rotary and Toggle Switches	North American Martin Marietta Grumman	100% screening by 30g sine vibration, 20-2000 Hz. X-ray inspection.	Verifies absence of contact chatter and transfer. Verifies no internal anomalies or large metallic particles.
Circuit Breakers	North American Martin Marietta Grumman	100% screening by 30g sine vibration, 20-2000 Hz. X-ray inspection.	Verifies absence of contact chatter and transfer. Verifies no internal anomalies or large metallic particles.

An application for the A-7 aircraft to use a multiplex system, incorporating solid-state circuit breakers, has increased data capability and decreased the amount of cabling previously required.

There are some applications of solid-state circuit breakers that are noteworthy. They can be programmed to trip or override predetermined levels, they can be used as on-and-off switches, they can be automatically and remotely reset, their programmed function can be changed approximately every 4 milliseconds if desired, they can incorporate magnetic sensors, and they can provide status of load; i.e., an indication if the load exceeds a predetermined value, or if there is no current flow. The flexibility of solid-state circuit breakers is a design convenience. The replacement of the electromechanical circuit breaker with a solid-state circuit breaker offers one exceptional advantage: the elimination of the failure modes associated with the mechanical linkage of the actuation mechanism. One disadvantage is the relatively low upper temperature limit. A typical value is 70°C.

An alternate approach to mechanical switches is the proximity actuated solid-state switch. However, factors of cost, weight, power and size dictates against their use, except in specialized applications.

e. Hardware Life - Solid-state circuit breakers have no life limitation. Mechanical switches and circuit breakers are subject to wear-out failure modes. The state-of-the-art cycle life is about 100,000 actuations for switches and 10,000 actuations for circuit breakers. Devices of lower capability are acceptable whenever the cycle life capability significantly exceeds the mission requirement plus the ground fabrication, test, and checkout requirement.

The storage life of switches and circuit breakers is mainly influenced by the long-term stability of the non-metallic materials and when these are eliminated, or only very stable materials are used, the storage life exceeds 10 years.

f. Application - The first consideration in selecting a switch or circuit breaker is the type and magnitude of load the switch is to control. The next consideration is that the part should be derated from the maximum rated temperature. Hermetically sealed switches should be used, and hermetically sealed circuit breakers should be used whenever available. The following current derating has been successful and is suggested:

Type of Load	Percent of Manufacturer's Rating
Resistive	75%
Inductive	40%
Motor	20%
Filament	10%
Capacitor	75%

A circuit analysis of the loads, transients and other inputs should be performed and carefully reviewed to verify that the limits are not exceeded. The packaging must be reviewed to show that proximity to temperature, magnetic, vibration, and shock sources will not affect the switch or circuit breaker's operation.

The criticality of the circuit breaker application should be reviewed to determine if redundant circuit breakers can be justified.

The shock and vibration requirements should receive close attention because both switches and circuit breakers are subject to contact chatter.

The following factors must be considered when selecting a switch: The voltage and current to be interrupted (ac, dc, high frequency), inrush current, contact current rating, voltage drop across the contacts, temperature rise within the switch, the heat dissipation, physical size, type of load; i.e., resistive inductive, lamp, capacitive or motor, the contact arrangement, make-before-break, break-before-make, etc. If redundant circuitry is used, the effect of make-before-break of the redundant contacts must be reviewed carefully. For example, when using a multipole switch, it is assumed that all contacts move (open/close) together, or that some will open and close before others. The closing of a set of contacts, connected in parallel with another set of contacts, could cause a shorted condition or make-before-break operation where break-before-make is needed.

The switch actuation mechanism must be determined. The application of the switch will require a toggle lever, push button, rotary, rocker button or lever, or leaf actuation. The switch will be mechanically operated by a rotating cam, a sliding wedge or other actuating mechanisms, or be manually operated with a lever, knob or push button.

Circuit breakers should be electrically located as close as possible to the protected circuit to offset the influence of other components.

The time-current curve of the circuit breaker should be matched to the circuit to be protected to embody normal circuit transients, i.e., motor start up, inductive switching, BUS E.M.I.

Life cycle estimates should include the actuations encountered, not only during the mission, but during ground tests and checkouts.

Switch applications in digital circuits must be carefully reviewed to assure that contact bounce or chatter will not be interpreted as a circuit interpretation which will produce logic errors. Switch contacts should not be paralled to increase current capability, since one set of contacts will close first and carry an excessive load.

D. TEST METHODOLOGY AND REQUIREMENTS

1. Qualification and Acceptance Test Screening

Tables 4 and 5 outline qualification and screening test programs. These basic tests may be augmented by program peculiar requirements as appropriate.

The qualification sample should be parts which have been first subjected to the screening tests. The qualification testing is a one time manufacture and part design capability level verification to demonstrate the ability of the part type to meet a determined stress level. Any change in part design or process control which affects form, fit or function requires requalification of the altered part type. Periodic tests and inspections (quality conformance on sample lots of parts produced) provides an indicator of how well the qualification and level of integrity is being maintained.

The 100% screening tests most important for the achievement of reliable devices are the operational run-in test (from 100 to 2000 cycles, depending on mission requirements and device capability) in which contact resistance is monitored; x-ray inspection for contamination and internal anomalies; and in the case of switches, the Lockheed-developed PIND test per LMSC Specification 1420833 is recommended for detection of contamination. Vibration screening to verify the absence of contact chatter is a good test for workmanship defects. During vibration, both switches and circuit breakers should be monitored for a short to case condition as well as other parameters.

Table 4 Switch Test and Inspection Requirements

100% Screening	Quality Conformance on Each Lot	Qualification on Each Part Type
Electrical Parameters	Group A	
Operational Parameters	Sample per MIL-S-8805	Qualification Inspection per MIL-S-8805 Table 6
Dielectric With standing Voltage		
Insulation Resistance	Group B	
Operational Run-in (Monitor Voltage Drop)	Sample per MIL-S-8805	
Vibration		
Contamination Detection		
Electrical Parameters		
Seal Leakage		
External Visual X-Ray		

Table 5 Circuit Breaker Test and Inspection Requirements

100% Screening	Quality Conformance on Each Lot	Qualification on Each Part Type
Electrical Parameter		
Operational Parameters	Group A	
	Sample per MIL-C-39019	Qualification Inspection per MIL-C-39019
Dielectric Withstanding Voltage		
Insulation Resistance	Group B	
	Sample per MIL-C-39019	
Calibration		
Vibration		
Contamination Detection		
Electrical Parameters		
Seal Leakage		
External Visual		
X-Ray		

2. Life Tests

The cycle life of switches and circuit breakers should be verified by life cycle tests, but taking care that the actuation rate is not high enough to cause secondary effects from excessive internally generated heat.

The margin between the life test demonstration and the mission requirement varies widely between users, varying from a factor of two to a factor of 10. For maximum reliability, the conservative margin is recommended, primarily because the test sample size is statistically small, and the variation of demonstrated life from one switch to another can be appreciable.

3. Accelerated Testing

Accelerated tests in the form of power burn-in, high speed life or excessive power pulsing are not normally a part of switch and circuit breaker testing. There have been tests where switches or circuit breakers were exposed to their maximum rated power, temperature and cycle rate, all at the same time. This maximum stress testing is used to find weak or failure prone parts and is recommended for use in development programs, and for devices that have been developed, but have not had prior successful program usage.

Another application of an accelerated test, which should be considered for selective application to switches, is the exposure of the non-operating device to high temperature followed by operation under a light load at ambient temperature to verify that any outgassing of inorganic materials is insufficient to condensed as a contamination film on the contacts.

E. PROCESS CONTROL REQUIREMENTS

Process controls and handling are considered critical. Improper control of any element of a part assembly, handling, cleaning and sealing can have detrimental effects on the life and reliability of the part. Table 6 lists critical processes and the effects of inadequate controls. For switches, based on recent Aerospace experiences, a very critical problem is particle contamination and the need for ultra clean conditions cannot be over-emphasized. It should be emphasized that x-ray inspection does not detect non-metallic particles, and the PIND test does not detect very small

Table 6 Critical Processes

Critical Processes	Effect of Inadequate Control
Fabrication of Detail Parts	Out-of-tolerance parts, damaged parts, improper heat-treat, improper materials.
Weld Schedule	Loss of seal, loose parts, shorts, open, parameter deviation, poor wire bonding.
Cleaning	Contamination, out-of-tolerance, operational interference.
Handling	Loose parts, seal loss, contamination, parameter deviation, shorts, opens.
Assembly	Our-of-tolerance, contamination, operational interference, parameter deviation, seal loss.
Sealing	Contamination, corrosion, shortened life due to varying atmosphere, inadequate protection, seal loss.

particles, and therefore the primary control of contamination must be the exclusion of contamination by clean rooms and clean benches. Class 100 conditions are desirable.

On those part types required for long-life application, the production build sequence and sealing methods need to be reviewed to verify that maximum control is used to provide minimum contamination and maximum process and schedule control.

F. PARTS LIST

1. Acceptable

Table 7 is a partial list of parts which have demonstrated reliability. These parts have been qualified and used in systems requiring high reliability for long durations.

2. Unacceptable

For long-life applications, switches that are not hermetically sealed are unacceptable. A circuit breaker which is not hermetically sealed should be deemed unacceptable if a hermetically sealed equivalent is available. Parts with soft or corrodable contracts such as copper are undesirable. Parts containing plated internal perts, or non-metallic materials which may outgas are undesirable. Circuit breakers with complex actuation mechanisms of unproven reliability are unacceptable. Circuit breakers that require solder or metal melting to operate are unacceptable. Devices produced by a supplier with an uncorrected or uncontrollable history of contamination failures are unacceptable. A mechanical circuit breaker is unacceptable when a solid-state equivalent is available which satisfies the application.

Table 7 Acceptable Parts (Partial List).

Type	Manufacturers Resistive Load Rating Maximum Current	Contact Description	Operating Temperature Range	Notes
A. Switches				
MS27216-1 Lever	5 amperes	SPDT	-85°C to +125°C	Per Mil-S-8805/8, Hermetic sealed, leaf actuated.
MS24594-1 Push Button	5 amperes	DPDT	-65°C to +315°C	Per Mil-S-8805/41, Hermetic sealed, plunger actuated.
Mil-S-81551 Toggle	Open	Per Mil-S-81551	Per Mil-S-81551	Hermetic sealed toggle actuated, source/manufacturer to be determined.
Rotary	See North American Rockwell Corporation Specification ME452-0093 and MC452-0049			Hermetic sealed rotary actuated, source/manufacture to be determined.
B. Circuit Breakers				
Bimetallic Circuit Breaker	See North American Rockwell Corporation Specifications ME454-0010, ME454-0011, and ME454-0012			

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IX. ELECTRONIC PACKAGING

by R. W. Burrows

IX. ELECTRONIC PACKAGING

A. INTRODUCTION

This study addresses multilayer printed circuit (PC) boards, printed circuit board-electronic part assemblies, conformal coating, and encapsulated modules. The basic life terminating factor is temperature cycling. In multilayer P. C. boards, temperature cycling produces failures of the plated-through-holes. In P. C. board assemblies, it produces cracked solder joints; and in encapsulated assemblies, it causes failures of both parts and electrical connections. It is not the objective of this report to encompass the total subject of electronic packaging, but to highlight the most important factors and guidelines for preventing these temperature-induced, life-limiting problems, and to place great emphasis on the importance of this subject to long-life assurance. This subject is also important as an economic consideration, since the solution to one, single, solder joint problem required an expenditure estimated at $7,000,000.

It is anticipated that problems will continue to occur in the future until the fundamental electronic packaging hazards and solutions are well understood, not just by the assigned packaging engineer, but by program managers and all the personnel directly involved in the design and testing of electronic hardware. This report was written with this education-oriented objective in mind.

B. GUIDELINES FOR LONG-LIFE ASSURANCE

1. Guidelines for Multilayer Printed Circuit Boards

Achievement of long-life multilayer printed circuit boards mainly depends on achieving plated-through holes which are capable of withstanding temperature changes without cracking and electrical failure. Heavy deposits of ductile copper are necessary, and verification by temperature cycling coupons from production boards is mandatory.

a. Design Guidelines

1) The thickness of the through-hole should be not less than 0.0015 inch for good resistance to thermal induced cracking.

2) Heavy layer copper (2 ounce) is preferable to 1/2 and 1 ounce circuits, and the thickness of the layer copper and PTH copper should be approximately matched for good resistance to thermal induced cracking.

3) Thinner boards, in which the volumetric proportion of glass epoxy to copper is minimized, are preferable.

4) The standard land, plated-through connection is superior to both functional land and landless designs, from the standpoint of thermal induced cracking.

5) For severe thermal applications, resin-glass systems of low thermal expansion should be developed and used to minimize thermal induced cracking.

b. Process Control Guidelines

1) The two processes critical to the life of multilayer printed circuit boards are the hole drilling process and the electroplating process, both of which require very close control to insure clean holes and ductile copper.

2) Brighteners should not be used in the electroplating bath since they may cause brittle copper.

3) The electroplating bath should be very closely controlled to avoid both brittle copper and hard copper.

4) Rockwell B hardness of 50 or less is recommended to assure the ductility necessary for long-life.

c. Test Guidelines

1) A test coupon from each production board containing 80 to 100 plated-through holes, connected in series, should be temperature cycled between -65° and 110°C, and increased electrical resistance should be cause for rejection of the production boards.

2) For programs with a nominally mild temperature environment 50 temperature cycles are recommended. For more severe applications, 200 temperature cycles are recommended.

3) Acceptance tests should also include temperature shock tests simulating the wave, or the hand soldering operations, since thermal induced warping of the boards tends to cause cracks between the inner copper planes and the plated-through hole.

d. Application Guidelines - Multilayer printed circuit boards should not be used in a very severe temperature cycling environment. An example is exposed hardware (not temperature controlled) on a spacecraft in a 150 nautical mile orbit where a temperature cycle is experienced every 1½ hours. However, from the wider viewpoint of overall electronic equipment reliability, electronic equipment should be protected from a severely fluctuating temperature environment by the use of a passive or active environmental control system.

2. Guidelines for Printed Circuit Boards Assemblies

In a printed circuit board assembly, the principal failure mode (excluding part failures) is cracked solder joints from temperature fluctuations which cause fatigue failures in solder joints not provided with adequate stress relief in the packaging design. (Failures of electronic parts are treated in the other sections of this volume.) The solution to the problem is to design an adequate stress relief. Other factors, such as solder application technique, amount of solder, type of solder alloy, etc., influence solder joint cracking, but are secondary to the factor of stress relief.

a. Design Guidelines

1) The parts mounting techniques should be controlled by specification. The specification "Standard Parts Mounting Design Requirements" MSFC-STD-136, is recommended.

2) Plated-through holes provide a much stronger solder joint than bare holes. Bare holes should not be used.

3) The pad size, hole diameter, and all other geometric factors influencing the shear strength of a given solder joint should be kept to the conservative side of MSFC-STD-136 to insure the strongest practicable solder joints.

b. Process Control Guidelines

1) NHB 5300.4 (formerly NASA 200.4) is oriented towards the process of producing high quality solder joints. This specification, however, does not provide detailed guidelines on the stress relief of solder joints and, therefore, it should be augmented by the use of MSFC-STD-136.

2) The maximum amount of solder allowed by NHB 5300.4 (formerly NASA 200.4) should be used, since temperature cycling tests have shown that the amount of solder significantly influences solder joint cracking.

3) The gold embrittlement problem should be avoided by removal of the gold-on-gold plated leads prior to the final soldering operation.

c. Test Guidelines

1) Verification of the packaging design should be accomplished on *early* prototypes, or on test samples representative of the design, by subjecting the hardware to temperature cycling between -55°C and 100°C, and inspecting for cracked solder joints.

2) The nominal value of 200 cycles required by MSFC-STD-136 is recommended. The actual mission environment should be reviewed to determine if this value should be adjusted.

d. Application Guidelines

Printed circuit board assemblies are not suitable for use in very high vibration and shock environments. For vibration levels of 0 to 5g rms, no particular effort to reduce vibration fatigue effects are usually necessary. From 5 to 20g rms, vibration resistance can usually be acheived through proper use of clamping, dampening, and conformal coating. Above 20g rms, the use of encapsulants to prevent fatigue failures from excessive board flexure will usually be required. The above estimates are gross; and each printed circuit board application requires a careful review for compatibility with the dynamic environment, and to establish mounting and dampening provisions.

e. Special Considerations

The requirement to withstand 200 temperature cycles may seem excessive, but it should be emphasized that earth-based equipment not stored in a temperature controlled environment could acquire 1826 cycles, with about a 15°C daily excursion, in a period of five years, and that some spacecraft equipment may experience a temperature cycle every 1-1/2 hours. The correlation of accelerated temperature testing with field service conditions has not been clearly definitized. However, IBM, on one program, determined from actual failure data that 46 temperature cycles from -20°C to 85°C was equivalent to two years of field service life.

3. Guidelines for Conformal Coating

Conformal coating, necessary for environmental protection and mechanical support on long-life hardware, is a major cause of both part and interconnection failure when not properly selected and applied. The problem is that heavy coatings, heavy filleting, or bridging under flat bottom parts produce or aggravate stress on parts and solder joints in a fluctuating temperature environment, and cause cracked solder joints and damaged parts.

a. Design Guidelines

1) A flexible polyurethane coating less than 4 mils in thickness is recommended.

2) Fragile parts such as glass diodes should be sleeved to prevent damage from thermal expansion stresses.

3) Coatings of the above thickness do not provide ultra high insulation resistance because 100% coverage cannot be achieved. When ultra-high insulation resistance (10^{10} ohms, and above) is required, a deposited coating such as Parylene C is recommended.

4) When both ultra-high insulation resistance and mechanical support is required, a deposited coating such as Parylene C followed by a sprayed 1- to 2-mil flexible polyurethane coating is recommended.

b. Process Control Guidelines

1) The application of conformal coating should be closely controlled by the packaging specification to prevent heavy coatings, heavy filleting, and bridging under flat-bottom parts. Application by spraying and removal of excess filleting by centrifuging (spinning) is recommended.

2) Bridging of conformal coating under flat-bottom parts usually has catastrophic consequences and must be completely avoided.

c. Test Guidelines

1) Verification of the packaging design, with the conformal coating applied, should be accomplished by the temperature cycling program described for printed circuit board assemblies.

2) Assure that the specific polyurethane selected has been tested under high humidity and temperature conditions to assure chemical reversion will not occur.

d. Application Guidelines

1) Conformal coating should be used only when specifically required for humidity protection and/or mechanical support.

4. Guidelines for Encapsulated Modules

Encapsulation (potting), employed with cordwood packaging, and sometimes with printed circuit board construction, is used for increased mechanical support. All potting materials, as a result of temperature changes, impose stresses on parts, connections, and many materials. Stresses in the thousands of pounds per square inch are produced. To prevent failures of parts and connections, the

potting material must be carefully selected and then tested using temperature cycling to verify that damage to parts and connections will not occur. Encapsulated modules generally do not have the temperature cycle capability of well-designed printed circuit board assemblies.

a. Design Guidelines

1) Solid, rigid materials, such as solid polyurethane or epoxy, should not be used as they impose excessive stress on the encapsulated parts.

2) Microballoon filled epoxy and low density polyurethane foam are usually satisfactory materials.

3) Very low density materials, such as polyurethane foam with a density of 2 lbs/cubic foot, may be required for increased temperature cycling capability.

4) Low density materials are good heat insulators and the module design must allow the conduction and dissipation of self-generated heat.

5) Potting stresses are reduced by a low ratio of potting volume to hardware volume.

6) In encapsulated modules, welded joints are preferred to solder joints since they are not subject to the problem of fatigue cracking.

7) Resilient pre-coats should be employed to achieve lower stress on parts and connections. A thin pre-coat (0.001 inch) hydraulically distributes the stress on a part, while a thick coat (0.008 inch) will reduce the stress.

b. Process Guidelines

1) The curing temperature should be as low as practicable, since a zero stress condition is present at the curing temperature, and stress progressively increases as the module cools.

2) Proper allowance must be made for the fact that the manufacturer's recommended curing process will probably not result in a 100% complete cure and subsequent temperature cycling will cause further hardening and aggravate the stress problem.

c. Test Guidelines

To verify that the encapsulating material and process will not damage parts, electrical connections, or cause performance shifts of sensitive parts, it is mandatory that the design be subjected to temperature cycling as described in the section of this report on printed circuit board assemblies. A prime difficulty in such testing is the difficulty of removing the potting to inspect the electrical connections visually. This difficulty is largely alleviated if the recommended, very low density, materials are used since these can usually be removed by mechanical, if not chemical, means.

C. MULTILAYER PRINTED CIRCUIT BOARDS

1. Introduction

This study addresses the long-life aspects of the copper clad, epoxyglass, etched circuit board with plated-through holes (PTHs) for layer interconnections.

The multilayer board (MLB) evolved from the single and double-sided boards with the development of the process to produce a plated-through-hole (PTH) to interconnect the copper planes. Because of problems with the plated-through holes, a number of investigations, including enhanced-defect-test-programs, have been accomplished since 1966, primarily by Rome Air Development Center and IBM. This study summarizes this work and provides consolidated guidelines for Long-Life Multilayer Boards.

2. Life Limiting Problems and Solutions

a. Thermal Coefficients of Expansion - The Basic Failure Mechanism

Since copper, glass, and epoxy are very stable materials, the Multilayer Board (MLB) has a potential life, at a constant temperature, of much greater than ten years. However, in an environment of changing temperature, the life of a poorly designed and constructed board may be terminated after a very few temperature changes. The underlying problem is the difference in the thermal coefficient of expansions between copper, epoxy, and glass.

This incompatibility produces copper cracking, usually within the PTH, with certain designs, or with incorrect or out-of-control processes. This cracking can produce electrical failures after several temperature cycles, but if designs and processes are optimized, the MLB can withstand several hundred severe temperature cycles over a range of -65°C to 110°C.

An investigation by R. N. Wild of IBM (Reference 1), conducted on the epoxy-glass laminate, alone, using G-10 material, found that due to the restraining effect of the glass fabric, the expansion of the epoxy-glass laminate in the Z direction (perpendicular to the MLB) is six to ten times greater than in the X and Y directions. A marked increase in the coefficient of thermal expansion in the Z axis after about 60°C was also established, as shown in Figure 1. The discontinuity in the curve is now attributed to the measuring technique. Later data (Reference 2) showed continuous curves and confirmed the high expansion in the Z axis. This phenomena accounts for the basic cause of PTH cracking.

b. RADC Industry Survey of MLB Failure Trends

In 1967, John E. McCormick of RADC reported a survey of 26 organizations, including both users and manufacturers (Reference 3). This survey was addressed to failures of *assembled* boards after the final screens and inspections. McCormick reported that in 40-odd failures, over 20 were electrical opens, mostly in the plated-through-holes; about eight were shorts, mostly due to solder bridging; five failures were internal shorts in the board; and five failures were defective solder joints. Since solder bridging is detectable by good visual inspection and the solder joint failures were not germane to the MLB problem, this survey focused increased attention on the plated through-holes.

c. Enhanced-Defect-Test Program Results

In 1970, McCormick and Donald W. Calabrese reported (Reference 4) the results of a three-phase RADC investigation. In the first phase, the causes of internal opens were determined to be epoxy smear, hole breakout caused by drilling, weak plated through-holes and chemical entrapment. The causes of internal shorts were foreign particle inclusions, partially etched copper, entrapped processing solutions, voids in the insulation, and layer misregistration. In the second phase, RADC used the above information to plan and conduct an enhanced-defect-test program during which many boards were fabricated with various "controlled" defects and then life tested using different environmental exposures including temperature-humidity tests and temperature cycling tests. The two most significant results of this test program are:

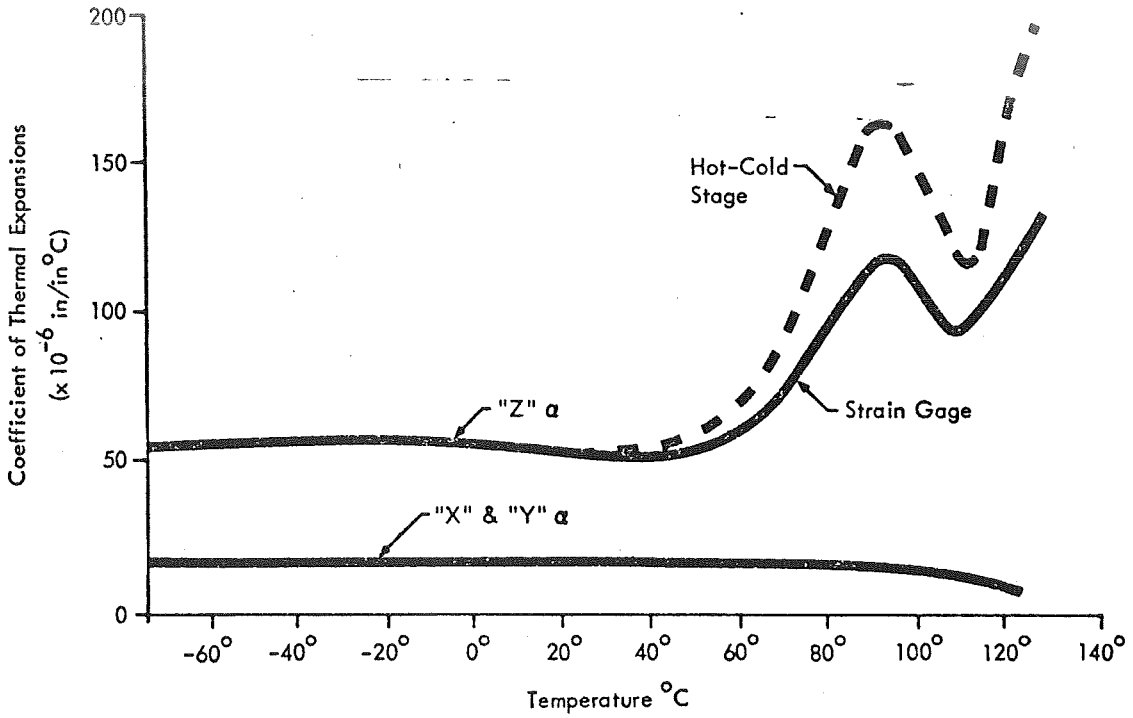


Figure 1 Coefficient of Thermal Expansions (G-10 Mat'l)

1) Plated-through-hole (PTH) failures are a much more serious problem than the other problems, such as entrapped chemicals, voids, and particles which may cause shorts.

2) Hole drilling, cleaning, and plating processes are extremely critical and must be closely controlled and monitored.

In the third phase, RADC temperature cycling results were compared with temperature cycling programs by the Institute of Printed Circuits (Reference 5) and by RCA (Reference 6). The three tests compared were:

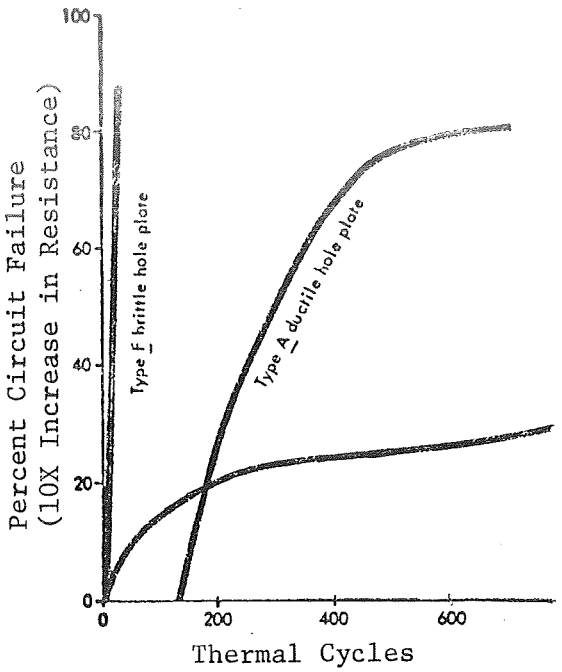
RADC - three-hour cycle, -65°C to 115°C.

IPC - 50-minute cycle, using thermal shock, 25-minute dwells, and progressively increasing the ΔT until -65°C to 150°C is reached.

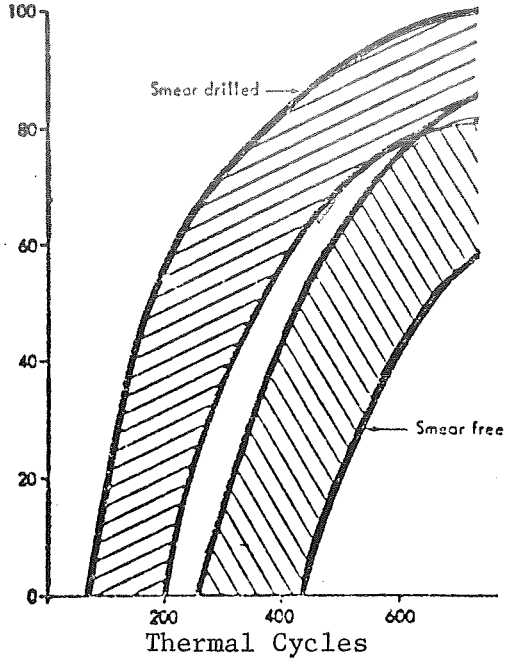
RCA - 30-minute cycle, using thermal shock, and 15-minute dwells.

In spite of the difference in these test cycles, McCormick concluded that there was good correlation between the results of the three programs, and recommended a thermal shock (in air) screening test for MLBs of 50 cycles using -65°C and 125°C with a 15-minute dwell at each extreme. This test can be performed in 25 hours, and provides data much faster than the 150 hours required by the three-hour cycle. The test was proposed to be conducted on a special test coupon containing 80 to 100 plated-through-holes in series. During temperature cycling, electrical resistance would be monitored. Increased, out-of-spec, resistance would constitute a failure.

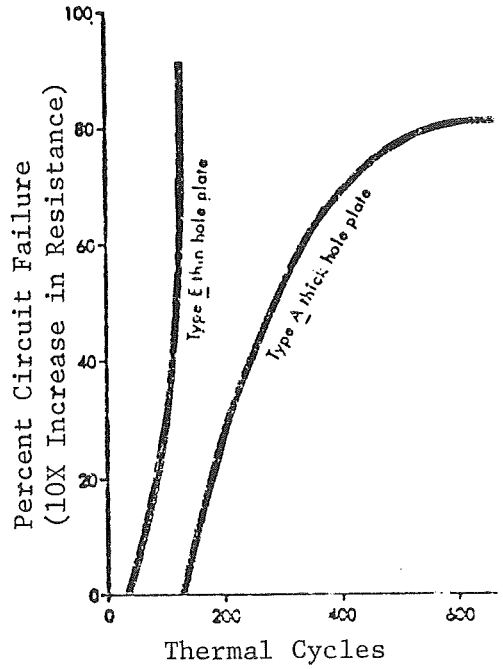
An investigation conducted by IBM, under contract to RADC, supplied most of the data reported in 1970 by H. C. Hurley in Reference 7. This enhanced-defect-test program established the effects of poor lamination, poor drilling causing epoxy smear in the holes, ductile versus brittle electro-plated copper, three thicknesses of layer copper, two thicknesses of the plated through-holes, and landed versus landless PTH/conductor interconnections. Multilayer boards were fabricated with the above variables and subjected to three different temperature cycling tests; a "hot" cycling test, a "cold" cycling test, and a test involving both hot and cold extremes. The results from this latter test, employing a three-hour cycle from -65°C to 110°C, are summarized in Figure 2. The failure mechanisms are illustrated in Figure 3.



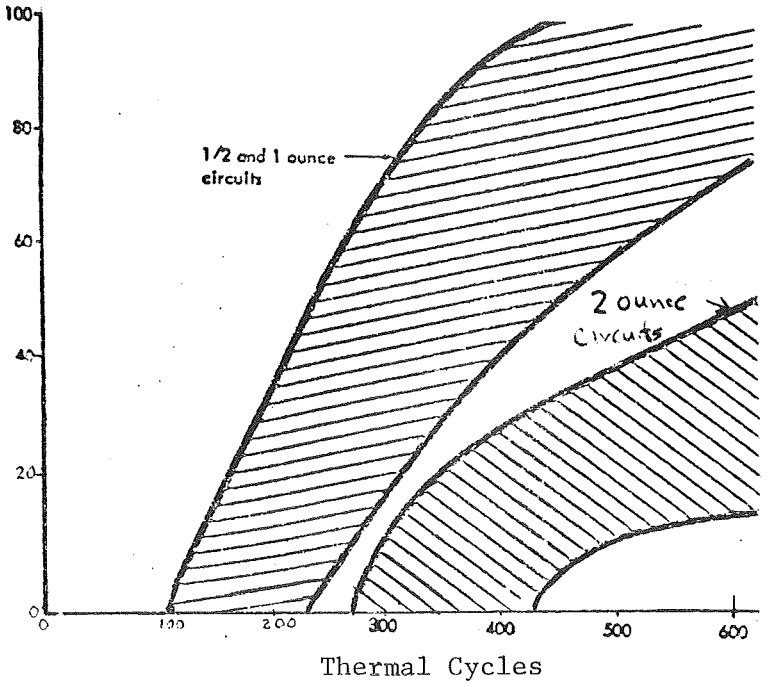
Brittle versus ductile hole plate.



Hole drilling evaluation.

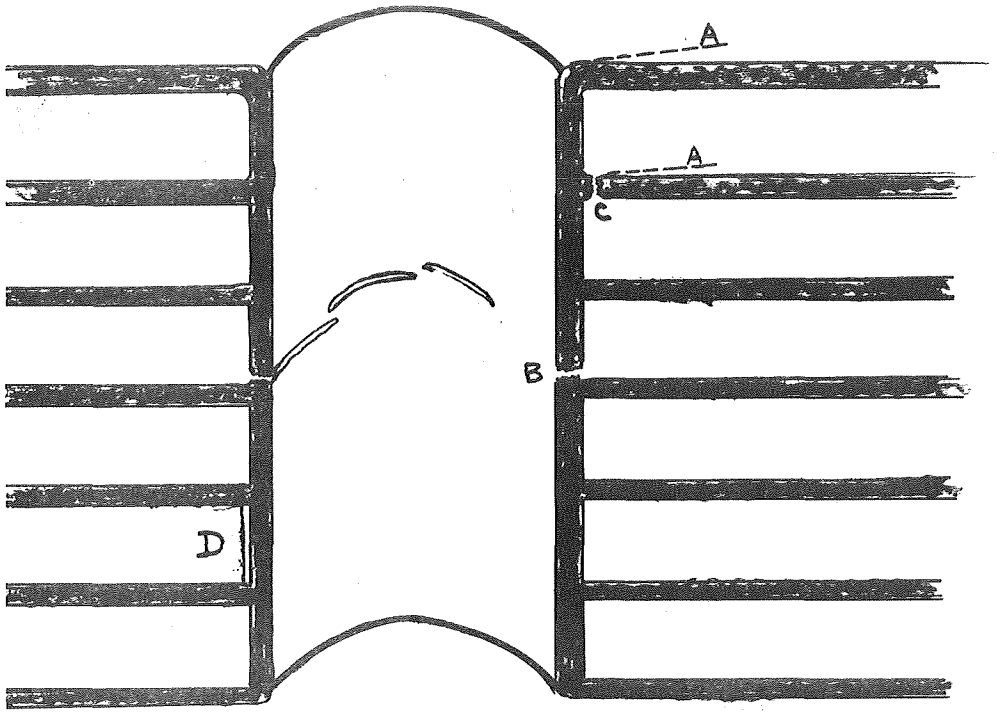


Thin versus thick hole plate.



Layer copper weight effects.

Figure 2 Temperature Cycling Data From Reference 7



1. The first indication of damage is bowing of the epoxy glass between the PTHs and deflection of the surface and internal bands (A).

2. Greater than 98% of the electrical opens resulted from 360° barrel fractures, usually located in the center half of the board near a land connection (B).

3. Interplane fractures represented about 2% of the failures and occurred only on planes near the surface (C) and within the interplane, and not at the PTH interface.

4. Loss of adhesion between the glass-epoxy wall and the PTH was also noted (D).

Figure 3 Cross-section of Multilayer Printed circuit Board Showing Failure Mechanisms as Determined by H. C. Hurley (Reference 7)

From this investigation, Hurley concluded that:

1) Brittle hole plate was the most serious defect, causing 50% circuit failure by 20 cycles, versus 300 for the control product.

2) Smear-drilled circuits, as compared to smear-free circuits, halved the life. Board opens were about three times as prevalent in smear-drilled circuits than smear-free circuits, and interplane opens about twice as prevalent.

3) MLB reliability is maximized by using thick hole plate and thick layer copper and the two thicknesses should be matched.

4) Landless designs are considerably inferior to landed designs.

Ennanced Defect Testing by R. N. Wild (Reference 1) established the superiority of a thick, 1.5 mil, copper plating for the PTH and the desirability of a low coefficient of expansion in the resin-glass systems.

Some results of Wild's temperature cycling tests using a four-hour cycle and -62°C to 115°C are shown in Figure 4. Wild also found that lowering the upper temperature only 20°C (from 115°C to 95°C) markedly extended the life. This can be explained in terms of the significant reduction of thermal expansion in the Z axis in this temperature.

In 1971, H. C. Hurley reported further findings (Reference 8). This program, using G-10 MLBs, evaluated the effects of three PTH diameters, two resin systems, and three PTH connection geometries. These variable were evaluated in three thermal environments; thermal cycling, soldering, and hand soldering. A three-hour 125°C and -65°C thermal cycle was used. The low expansion resin gave superior results; the reliability increased with increasing hole diameter; and the normally-used standard land plated hole connection was superior to both the functional land and the landless designs.

In the wave soldering tests, examination, after ten exposures, showed plated hole degradation typified by a separation of the copper board from the epoxy-glass wall, and a permanent stretching of the barrel. Boards manufactured from resin system No. 2, while superior in the thermal cycling tests, showed a higher incidence of barrel-to-wall separation and more warpage (would not lay flat). The standard land PTH's were significantly superior to the other configurations because of their anchoring effect. Through-hole

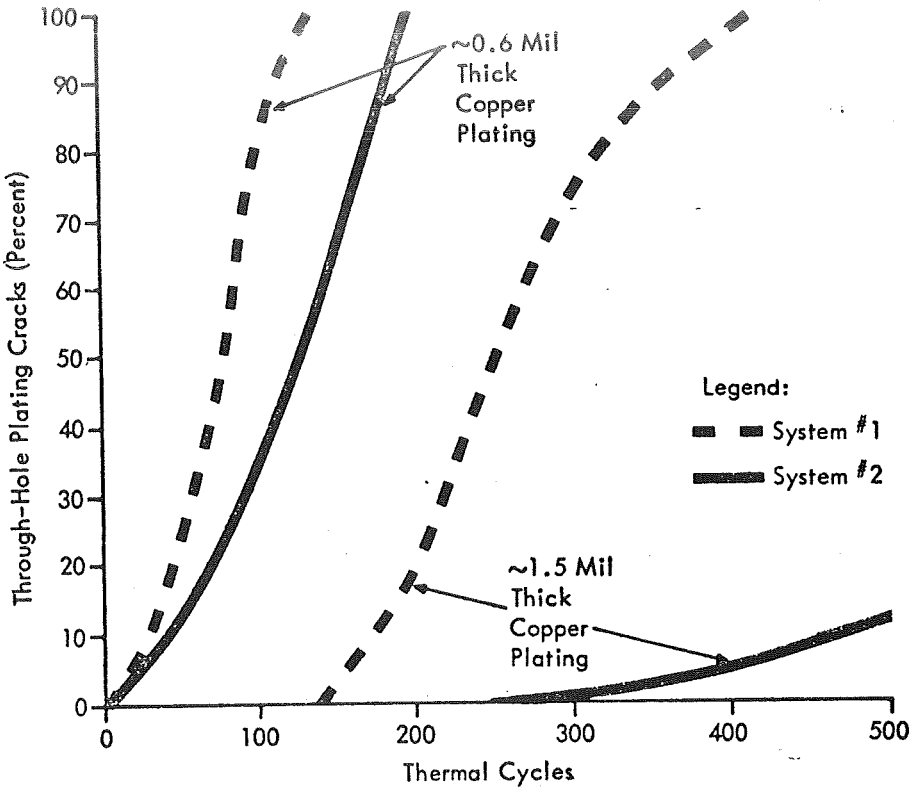


Figure 4 Through-Hole Plating Cracks vs Thermal Cycling (360° Cracks) (Reference 1)

diameter did not have a measurable effect. No electrical failures were detected in the boards after 20 exposures to the wave solder environment. It should be emphasized that an "accelerated", wave soldering, test was performed in which the contact time was increased from a normal two seconds to nine seconds.

In the hand soldering tests, barrel stretch and epoxy-glass separation from the barrel were more severe than in the wave solder tests. The test consisted of soldering and unsoldering a wire six times, allowing the joint to cool between each step. As with the wave soldering tests, resin No. 1 and the standard lands, again showed the least amount of barrel-to-wall separation, but through-hole diameter influenced the results with the 0.022 inch hole showing more degradation than either the 0.16 inch or the 0.31 inch diameter holes. In addition, severe bowing of the surface eyelets and internal lands was noted.

3. Processes and Associated Failure Mechanisms

This section describes MLB fabriaction processes and the related failure mechanisms. Process control requirements are summarized in Table 1.

a. Artwork

From the circuit schematic, a designer lays out the required parts as templates to locate holes or mounting pads, usually at four times size (4X), and then begins the pad/hole and trace placement. He also lays up ground/voltage planes and clearance holes or connection on inner layers, as well as inner circuitry layers as required. The "tape-up", as it is called, is the master drawing and, as such, sets the trace width, conductor spacing, pad size, hole size, board dimensions, tooling hole positions and all other sizes, locations and dimensions. From the master, a contact "second original" is made. Which is used to make the final "working Tool" by photoreduction to 1:1 scale (1X). Working with care, on a .100" x .100" grid at 4X, a highly competent designer can nearly match the accuracy of the modern computer artwork generation systems. He has the advantage of reducing his errors by 4:1 on photoreduction, but he has several disadvantages working against him. First, the tendency of Mylar drafting film at 30" x 40" to expand and contract with temperature changes reduces accuracy. Use of 7-mil instead of 4-mil Mylar improves dimensional stability as does care in handling, transporting and storing the master and second original. Second, the tape-up tapes and shapes have some tolerances in their manufacture and third, the photoreduction step depends on a very accurate camera, accurate measurement from master to film, temperature control and highly skilled personnel to keep additional dimensional errors to a minimum.

Table 1 Process Control Requirements

Critical Process/Material	Relative Impact on Long-Life	Effects of Inadequate Control	Method of Control
1. Art Work	Minor	Dimensions out-of-tolerance	Skilled draftmen and checking of tolerance.
2. Clad Material Preparation	Minor	Insignificant	Careful process control.
3. Cleaning of Clad Material	Minor	Lifting of photoresist; etch away conductor.	Careful process control; mechanization/automation.
4. Application of Photoresist (Inner Layers)	Minor	Bubbles under dry film resist or in liquid resist - same mechanism as above	Use machine designed specifically for type of resist being used.
5. Exposure of the Photoresist	Minor	Underexpose; not all photoresist washed away upon development (next step); unwanted copper after etch.	Post-proper exposure schedules. Visual inspection.
6. Development of Photoresist	Minor	Not all photoresist "strings" completely removed; unwanted copper after etch.	Replenish or replace developer accoring to manufacturers recommendations.
7. Etching of Circuitry and Stripping of the Exposed Photoresist	Minor	1) Overetch; 2) corrosion later from entrapped etchant in holes. 1) Underetch unwanted copper binding; 2) contamination between conductors (entrapped etchant).	Periodic Q.C. Lab analysis/test of etchant. Maintain specified etching temperature and time. High pressure water rinse for a time (plus margin) determined by Q.C. Lab or Engineering. Minor bridging may be carefully removed.

Table 1 Process Control Requirements (cont)

Critical Process/Material	Relative Impact on Long-Life	Effects of Inadequate Control	Method of Control
8. Lamination	Major	Delamination from: contamination, mishandling, improper storage or improper laminating cycle, causing possible cracking of holes or conductors. Delamination from above causing: voids, possible moisture or solution entrapment. Inclusions (conductive contamination).	Operator training. Post-operation instructions. Periodic calibration of press platen temperature and pressure by Q.C. Lab. Analysis of incoming prepreg (and periodic analysis thereafter) by Q.C. Lab for gel time, percent flow and percent resin and volatile. Maintain process operations log.
9. Hole Drilling	Major	Incorrect feeds or speeds; dull drills. Causes tear-out of epoxy or copper, "nailheading, " drill wander and glass fiber projections, all of which can cause weak spots in plating and increased susceptibility to cracks.	Operator training. Post-schedules for all feeds and speeds for materials and drill sizes.
10. Deburring and Cleaning the Holes	Major	Small copper particles from sanding can cause nodules during plating. Nodules usually cause weak spots in hole wall plating.	High pressure air blow-out.
11. Removal of Epoxy Smear	Major	Epoxy smear not removed; no contact of inner layer with plated hole wall. Etchback is to cause small projection of inner layer for better bond to plated hole wall	Periodic Q.C. analysis of sulfuric acid (water content)
12. Sensitization and Deposition	Critical	Carelessness or out-of-control process can cause voids, resulting	High pressure/ultrasonic rinse. Adequate cleanliness. Daily

Table 1 Process Control Requirements (cont)

Critical Process/Material	Relative Impact on Long-Life	Effects of Inadequate Control	Method of Control
12. (cont) of Electroless Copper		in weakness to plated hole - or no continuity at all. Soft or non-adherent deposits contribute to shoulder cracking of PTH	(or more often) Q.C. Lab check of electroless copper. Bi-weekly Q.C. Lab analysis of catalyst. Schedule for replenishment/replacement of all solutions.
13. Deposition of Electrolytic Copper	Critical	Out-of-control bath (or inattention to process documents) can cause: 1) Nodulation - weak spots in hole walls. 2) Brittle copper - cracked holes. 3) Low tensile copper - cracked holes.	Minimum twice-a-week analysis of bath by Q.C. Lab. Post-schedules for time and current density to give required thickness of plating. Accurate measurement of board (and rack) area to calculate current density. Maintain mandatory plating logs for each tank. Log bath additions and time, current and area for each bath.
14. Application of Photoresist to Outer Surfaces, Exposure and Development	Minor	See Steps 4, 5, and 6.	See Steps 4, 5, and 6.
15. Deposition of Tin-Lead	Minor	"Bridging" (after hot oil reflow) from too thick tin-lead deposit.	Weekly analysis of tin-lead bath by Q.C. Lab. Posted schedules for time and current density. Visual inspection.

Table 1 Process Control Requirements (concl)

Critical Process/Material	Relative Impact on Long-Life	Effects of Inadequate Control	Method of Control
16. Stripping Exposed Photoresist and Etching, Using Tin-Lead as the Etch Resist	Minor	See Step 7.	See Step 7.
17. Reflow of Tin-Lead	Minor	Bridging from too thick tin-lead solder.	Visual inspection. Minor bridging may be carefully removed.

Computer-generated artwork, on the other hand, has none of these three problems. The process starts with the layout which the designer has produced, or in some systems with the electrical schematic. In the former instance, the hole or pad positions are digitized, a wiring list is generated and the computer, through a plotter, interconnects parts and routes lines (traces) with minimum specified spacing. The output is a glass 1:1 master, fragile, but dimensionally stable. From it, the 1X working tool is made on contact printed on film. Computer generated artwork should be used for boards of four layers or more, to achieve adequate layer-to-layer registration accuracy. Artwork tolerances should be kept to the best attainable level. Using the latest targeting and registration techniques, and with one of the methods of "stacking" the final 1X artwork to check position and alignment, the first step in the production of a reliable multilayer PCB has been accomplished.

b. Clad Material Preparation

The shearing-to-size of the clad material very seldom contributes to an MLB failure.

c. Cleaning of Clad Material

Inadequate cleaning may result in non-adherence of the photoresist, resulting in the etching away of part of a pad or trace, ultimately showing up as an open circuit.

d. Application of Photoresist (Inner Layers Only)

Bubbles in the liquid resist may cause thin spots and unwanted etching away from conductors. With dry-film resists, an improperly controlled "laminating" machine or the wrong machine may cause air pockets under the resist to give the same result as non-adherence.

e. Exposure of the Photoresist

When the artwork is overlayed and exposed, underexposure of the photoresist will cause unwanted copper resulting in short circuits.

f. Development of Photoresist

There are two basic kinds of photoresist. One polymerizes and becomes less soluble where it is exposed to light (through the clear part of the working artwork). When is is "developed", the unexposed portion washes away in solvent. The other becomes more soluble where it is struck by light and that exposed portion washes away in development. The former is most commonly used. If this resist is underexposed, or the "strings" of unwanted photoresist are not washed away, short circuits of unwanted copper will result after etching.

g. Etching of Circuitry and Stripping of the Exposed Photoresist

Overetching can cause open circuits. Shorts can be caused from poor rinsing resulting in corrosion from the entrapped etchant or contamination between conductors. Underetching can also cause shorts. If the above defects are not detected by visual inspection, they will be "buried" inside the board by the next operation.

h. Lamination

Material prep and storage operations and the layup must be done under reasonably clean room conditions to prevent metallic particles from falling onto the layup creating potential shorts.

Once the layup is in the press, the laminating schedule depends on the parameters of the prepreg, gel time, flow and resin content. The schedule is usually set empirically by making "dummy" layups. Lamination may be done "cold press" or "hot press", but while the former gives more control, the latter is the more common process. Too high a pressure can cause "swimming" or breaking of circuitry. The principle failure mechanisms caused by poor lamination are resin starvation (too thin glue line) or pregellation and air bubbles (too thick a glue line). Either may cause a short circuit failure mode if solutions are entrapped. Martin Marietta has determined that warping or flatness of the board can be improved by special lay-up techniques, which are now under investigation for the Viking program.

i. Hole Drilling

In drilling an inhomogeneous material, layers of copper, requiring one set of drill feeds and speeds, and layers of epoxy-impregnated fiberglass, requiring a different set, the process is a compromise and not optimum for either.

While for many years a drill speed of 20,000 rpm was considered adequate, the current practice is 80,000 to 100,000 rpm. Too fast a *feed* can cause deformation of the copper foil and epoxy glass tear-out, while a dull drill not only also causes the above defects, but causes "nailheading" of the inner layers and drill wander as well. Too slow a *speed* will also cause nailheading. Rough, torn, or smeared hole walls significantly degrade the quality, uniformity, and bond of the subsequently plated through-hole.

j. Deburring and Cleaning the Holes

Most manufacturers use a Clair sander or equivalent to debur the drilled holes. The debris from sanding catches in the rough holes and, without adequate cleaning, particles will remain to cause problems in through-hole plating.

k. Removal of Epoxy Smear and Etchback

In drilling, epoxy is softened and smeared across the inner copper layers. If not removed, it will cause an open circuit after platings. Either sulfuric acid or a "liquid honing" process will remove epoxy smear.

Etchback is a controversial subject. Originally, it was considered essential to good PTH-internal layer joints. The etchant was a mixture of sulfuric and hydrofluoric acids to remove about 1 mil of both epoxy and glass.

Moreover, if the sulfuric/hydrofluoric acid mixture picks up too much water, or the hydrofluoric acid concentration gets too high, deposits of powdery, insoluble fluosilicates can form to cause voids later during the plating process. The consensus process is the use of sulfuric acid alone.

l. Sensitization and Deposition of Electroless Copper

This process involves 10 to 15 tanks in series, depending on whether or not a common rinse tank or separate rinse tanks are used. Prior to plating, the boards are thoroughly cleaned, preferably with a mechanized scrubber and rinser, since pumice cleaning may leave particles in the holes to become nodules after plating. Unremoved pumice may also contaminate the plating line solutions. After a near-boiling anodic clean comes a brief etch in ammonium persulfate (and a rinse at the end of each step) followed by catalyst, sensitizer, accelerator and into the electroless copper solution itself. Upon completion of the electroless

deposition, boards are kept wet and electroplated as soon as possible. If the boards are left to dry or stand too long in sulfuric acid, the adhesion of electrolytic copper may be poor, contributing to the shoulder cracking of the plated through-holes. Common plating racks that can be used in both electroless and electrolytic plating are recommended.

m. Deposition of Electrolytic Copper

The boards are immersed in the electrolytic copper bath and, after a few minutes at a low current density (copper strike), the operating current density is then adjusted for the area to be plated and continued for the time specified in the plating schedule. The most difficult part of electroplating is the chemical control of the bath itself. It should be analyzed for PH, copper content, pyrophosphate content and ammonia content at least once a week depending on the stability of the bath parameters and the volume of circuit boards being processed. An analysis for orthophosphate should be performed at least bi-weekly and temperature monitored every few hours.

The copper pyrophosphate bath is considered here because it is today the consensus bath; it has good throwing power and it is easier to control than other baths, especially copper fluoborate. Throwing power is the ratio of thickness of surface plating to the thickness of plating in the hole. A lower value in the holes arises from the lower current density inside the holes and is partly a function of the board thickness, t, versus the hole diameter, d. The ratio t/d should always be less than five to one and preferably three to one or less.

If minute metal particles from sanding are not completely removed by air blow-out, or subsequent rinsing, nodules will result upon electroplating and may reduce hole size below minimum tolerance or cause weak spots in the hole walls. Rough drilling will be accentuated by electroplating and large nodules may be formed.

Organics, including the breakdown products of brighteners, if used, cause pitting and worse, brittle copper. Periodic tests with a Hull cell will indicate the level of organic contamination, which can be removed by treating with finely divided carbon.

Continuous filtration through a one-micron filter to remove fine particles, is mandatory.

n. Application of Photoresist to the Outer Surfaces, Exposure and Development

The previous discussion (d thru g) is applicable.

o. Deposition of Tin-Lead

Tin-lead is co-deposited from a tin and lead fluborate bath. Currently, it is almost always pattern plated; that is, deposited in the holes and the areas of copper that will be traces, the tin-lead later acting as an etch resist. The bath is relatively easy to control. Too much tin-lead on the traces and pads can cause shorts after reflow.

p. Stripping Exposed Photoresist and Etching, Using Tin-Lead as the Etch-Resist

The same kinds of problems exist here as in Step 7.

q. Reflow of Tin-Lead

The tin-lead, as deposited, is not solder; it must first be reflowed above the melting point of solder to convert it to eutectic tin-lead solder (63-37). Originally, peanut, or other oils capable of 400°F, were used for reflow, but currently Carbowaxes, polyoils, and other non-oil materials are frequently used. Excess tin-lead on the circuit traces can cause bridging and shorts upon reflow.

It is concluded that the electroplated copper of high ductility is the most important single factor for long life multilayer printed circuit boards. Very close control of the electroplating both is necessary.

Organics, including the breakdown products of brighteners, if used, cause pitting and worse, brittle copper. Periodic tests with a Hull Cell will show, semiquantitatively, the level of organic contamination, which may be removed by treating with finely divided carbon.

Continuous filtration through a one-micron filter to remove fine particulates is mandatory.

The pyrophosphate plating bath is reportedly capable of as high as 9% ductility (Reference 9), measured as elongation at break. Good process control should provide adequate ductility and prevent cracking of plated through holes. Fluhman and Saxer (Reference 10) have reported that by using very fine (down to 0.6 micron) molecular sieve type filtration for all materials in making up the pyrophosphate bath plus 0.8 micron continuous filtration, they could achieve 20% elongation plated copper. However, no matter how ductile the copper plate is (to the maximum of the above process limitation), at some finite number of temperature cycles, depending on the temperature excursion, cracking will start to occur because of metal fatigue.

The foregoing descriptions of process and workmanship-dependent defects emphasizes the importance of Process Control to the Long-Life Assurance of MLBs. Process control comprises a set of process specifications or documents which detail the process operations and controls (both in-line and quality control) *and* a rigorous, vigilant, continuing quality audit and monitoring to ascertain that the process documents are being followed to the letter. Well-designed, mechanized or automated processes are easier to control than those which depend on human operators. This applies whether the MLBs are procured in-house or out. Another important adjunct to process control is an alert process engineering organization (may be *one* man) to trouble-shoot and solve anomalous problems that do not respond to the normal procedures for keeping the process in control.

4. Summary

The life of multilayer printed circuit boards depends on the capability of the boards to withstand the temperature-induced stresses resulting from the soldering process and the subsequent temperature cycling experienced during the service life as a result of both ambient temperature changes and the temperature changes induced when the equipment is energized. The failure mode is cracking at, or in, the plated through holes, and is the result of the difference of thermal expansion of copper and glass-epoxy. The life of an MLB electroplated with brittle copper, and thin plate in the plated through holes, is extremely short since failure will occur after a few temperature cycles. The life of MLB, through good design and process control, can be extended to greater than 200 temperature cycles between -65°C and 110°C.

The prime long-life is the ductility of the copper plate in the plated through-hole. To achieve ductile copper and to avoid brittle, or hard copper, extreme process control is required during the electroplating process to insure high ductilities in the region of 5 to 10% elongation. It does not appear feasible to insure ductility by requiring a ductility test on a test sample as deposited in the bath, because the thinness of the sample (only several copper grains thick) yields unreliable results. IBM prefers a hardness test. Rockwell B hardnesses of 50 have given good results, while hardnesses as high as 80 to 90 may give trouble. While electroplating is a critical process to long-life, the hole drilling and cleaning processes are almost as critical and they also require very close process control.

The design of the board also markedly influences the life. The most significant design factors for achieving long-life in a fluctuating temperature environment are listed:

1) The thickness of the hole plate should not be less than 0.0015 inch.

2) Resin-glass systems of low thermal expansion should be developed and used when the temperature environment is severe.

3) Thinner boards are preferred, since the effect of the high expansion of the resin is proportionally minimized.

4) The normally used standard land, plated hole connection is superior to both functional land and landless designs.

5) Heavy layer copper (2 ounce) is preferable to 1/2 and 1 ounce circuits.

6) The thickness of the inner plane layers should be approximately matched to the thickness of the plated through holes.

As final verification of both the design and the process control, a test coupon from each production panel should be subjected to temperature cycling between -65°C and 110°C. The special test coupon should contain 80 to 100 plated through holes in series. The test coupon being used by Martin Marietta Aerospace on the Viking program is shown, as an example, in Figure 5. During temperature cycling, increased, out-of-spec, electrical resistance would constitute a failure. The number of temperature cycles should be determined from an analysis of the particular program

Figure 5 Multilayer Printed Circuit Board Test Coupon Used on the Viking Program

or mission. For mild conditions, 50 temperature cycles are recommended, while 200 cycles are recommended for more severe applications. Since the state-of-the-art in MLBs is approximately 200 cycles, multilayer printed circuit boards should not be used in long-life hardware which will experience a great number of temperature cycles. An example is exposed hardware (not temperature controlled) on a spacecraft in a 150 nautical mile earth orbit, where a temperature cycle is experienced every 1-1/2 hours.

D. PRINTED CIRCUIT BOARD ASSEMBLIES

1. Introduction

The majority of the technology on the prevention of solder cracking problems on PC boards was developed as a result of solder cracking problems on the Saturn Program. The solution to these problems was undertaken by a Solder Committee established at MSFC in February 1967, and chaired by Mr. E. Ray Van Orden.

Exhaustive studies of solder cracking have been performed since 1967, and sufficient knowledge exists to produce long-life hardware, providing the lessons learned by these investigations are understood and followed. The approach of this section is to concisely summarize these investigations and reference the source data.

Four MSFC documents and five reports from Westinghouse, IBM, and Martin Marietta Corporation are briefly abstracted herein.

These nine documents provide the essential background information and guidance for any program with the goal of long-life assurance.

The mechanism of failure is the result of mismatches in the coefficients of thermal expansion. Temperature changes fatigue the solder joint producing stress lines and bulges, and then small cracks which become progressively severe until, finally, electrical failure occurs.

The variation in solder joint life ranges from 1 accelerated temperature cycle to more than 4000 cycles, and mainly depends on the stress relief inherent in the design.

2. Life Limiting Problems and Solutions

a. Abstracts of Source Data -

1) The mechanism of solder joint failure is described in a recent report by R. N. Wild (Ref 11).

This report describes the primary cause of solder joint failure as a slow cycle fatigue phenomena and emphasizes that a solder joint seldom fails because its ultimate strength has been exceeded. Relatively low stresses (from inadequate stress relief) cause rapid creep and relaxation of the stress and, after a number of cyclic

repetitions (from temperature changes), a crack forms and progresses to the point of electrical failure. The first visual evidence of cyclic damage is a dulling of the normally bright shiny surface, appearing as an annular crazing or frosty condition. As the solder is work hardened, grain growth and recrystallization occurs. The slip will then occur in a slightly different (non-strain hardened) position within the solder joint. This produces several slip bands until one is weakened due to Pb rich-phase alignment to a point where fracturing occurs and subsequently progresses to an electrical failure. Using a cyclic strain testing machine developed by IBM, it was discovered that when the strain cycles were applied slowly, a solder joint would fail after much fewer cycles than when the cyclic strains were applied at a more rapid rate. This is attributed to the greater plastic deformation that occurred on each cycle when slower cycling was employed.

2) A NASA Technical Memorandum by M. J. Berkebile (Ref 12) describes the causes and solutions of some of the cracked solder joint problems which occurred on the Saturn Program. The part mounting techniques did not allow for the stresses caused by thermal expansion of the boards that occurred in normal operation. Particular problems discussed include: (1) the solder joint cracking which tends to occur when a feed-through is soldered to both sides of a bare (not plated-through) hole, (2) the solder joint cracking that results from the typical transistor mounting using a plastic spacer, and conformal coating, and (3) problems with relays and modules. Several flight hardware items were reworked to provide strengthened solder joints. The techniques employed were the flanged tubelet, copper tubelet, and redundant soft copper wire. Such rework techniques are avoided when stress relief is provided by the design. The report contains numerous guidelines and diagrams, and emphasizes that high confidence in the life capability of any packaging design can only be obtained by verification testing employing temperature cycling and vibration.

3) An investigation by Barnes Beasley of MSFC is reported in Reference 13. In this investigation, calculations were first made to derive the solder joint loads resulting from various part mounting techniques as a result of exposure to temperatures of -20°C to 85°C. The results, summarized in Table 2, illustrate the seriousness of the problem that can be expected with the standard mounting of transistors on nylon spacers, and with larger components such as transformers and modules. Table 2 also illustrates the benefits of low modulous (resilient) pads and spacers. Various hardware configurations were fabricated and subjected to temperature cycling between -30°C and 100°C, using a three-hour cycle with

with one-hour soak times at high and low temperature. The test results, summarized in Table 3 illustrates the problem that exists with transistors and large modules.

4) A NASA Technical Memorandum by E. Ray Van Orden (Ref 14) presents many techniques of strain relief, including a basic design concept on mounting components with heavy leads to a solid structural base and then soldering the leads to a thin, *flexible*, board which is free to yield under stress. This report presents a very comprehensive set of guidelines, an example of which are presented as Figure 6. One of the most significant items is that a basic policy was on verifying the *packaging design* by testing was established by the Solder Committee. This verification policy has, subsequently, been implemented by many NASA contractors. This testing should be accomplished as long *before* formal Qualification Testing as possible, to enable adequate opportunity for timely corrective action on the basic packaging. This policy, entitled *Basic Design Verification*, is as follows:

> "It is anticipated that many more packaging configurations, some of which may be more complex than the fundamental concepts discussed herein, will become evident. In order to establish confidence in the reliability of new packaging configurations, the following tests have been standardized by the Solder Committee. New packaging configurations should have been successfully tested prior to implementation.
>
> "1. Temperature cycling - The subassemblies should be temperature cycled in an air circulating oven from room temperature to -55°C to 100°C and back to room temperature at a rate not to exceed 5°C per minute. Soak time at each temperature extreme should be 15 minutes, minimum. The duration of each cycle should average 2 hours. An inspection of each joint under 15X magnification should be performed prior to test and after 10, 25, 100 and 200 cycles.
>
> "2. Vibration - After completing the temperature cycling test, the subassembly should be subjected to vibration equivalent to the requirements, plus a safety factor, dictated by design that the subassembly will see in usage or acceptance testing.
>
> "3. Complete assurance is established if there are no cracked solder terminations found after 200 thermal cycles and vibration testing when examined under a minimum of 15X magnification."

Table 2 Summary of Solder Joints Loads from MSFC Report No. 53824

CONFIGURATION	SOLDER JOINT LOAD
TRANSISTOR CONFIGURATION	
Nylon Spacer	1.9 lb
XCU-A308 Spacer	0.07 lb
Sleeve Spacer	0.02 lb
TRANSFORMER CONFIGURATION	
Transformer with Conformal Coating	6.8 lb
Transformer W/O Conformal Coating	14.2 lb
Transformer with XCU-A308 (Pad)	0.18 lb
Transformer with XCU-A308 (Gasket)	0.14 lb
WELDED MODULE CONFIGURATION	
Welded Module with Conformal Coating	9.4 lb
Welded Module with XCU-A308 Pad	0.27 lb

Table 3 Summary of Temperature Cycling Testing of Solder Joints from MSFC Report No. 53824

Parts and Mountings Tested	Number of Temperature Cycles	Total Number of Solder Joints	Number of Cracked Solder Joints	Percent Cracked Solder Joints
Standard Mounted Transistors	1000	3072	566	18
Transistors Mounted Using Vinyl or Teflon Lead Sleeving as Standoffs	813	300	0	0
Transistors Mounted on Resilient Pads	200 to 1000	1080	7	0.7
Standard Mounted Transformers on Test Boards	455	12	7	58
Standard Mounted Transformers in Two Hardware Packages	397	1397	122	9
Standard Mounted Modules on Test Boards	455	230	186	82
Standard Mounted Modules in Two Hardware Packages	397	1343	846	63
Standard Mounted PC Connectors	397	3416	199	6
PC Connectors Mounted on Resilient Pads	200	1428	3	0.2
Free (Unstressed) Kovar Transistor Leads	1000	60	0	0

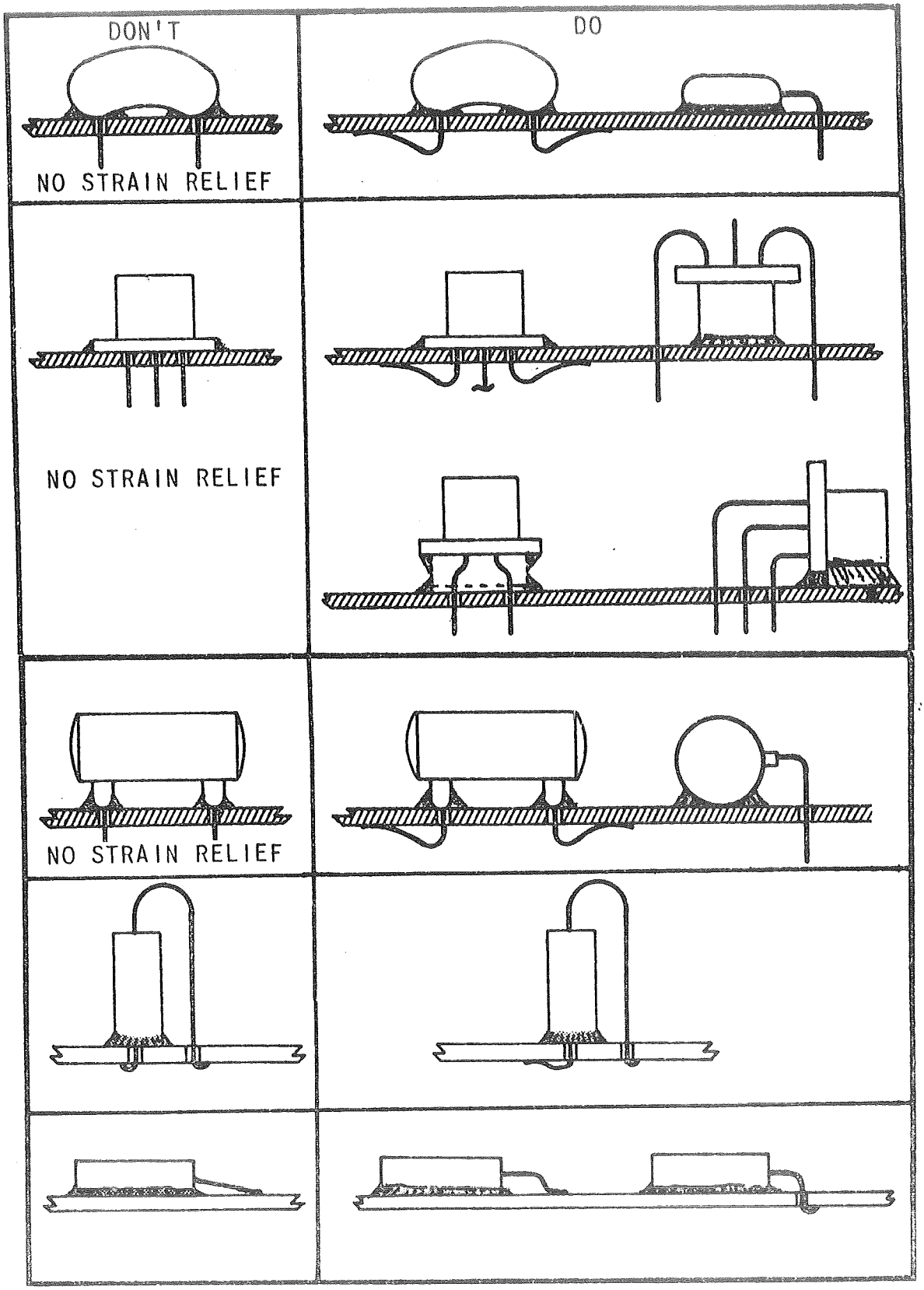


Figure 6 Parts Mounting Guidelines from Reference 14

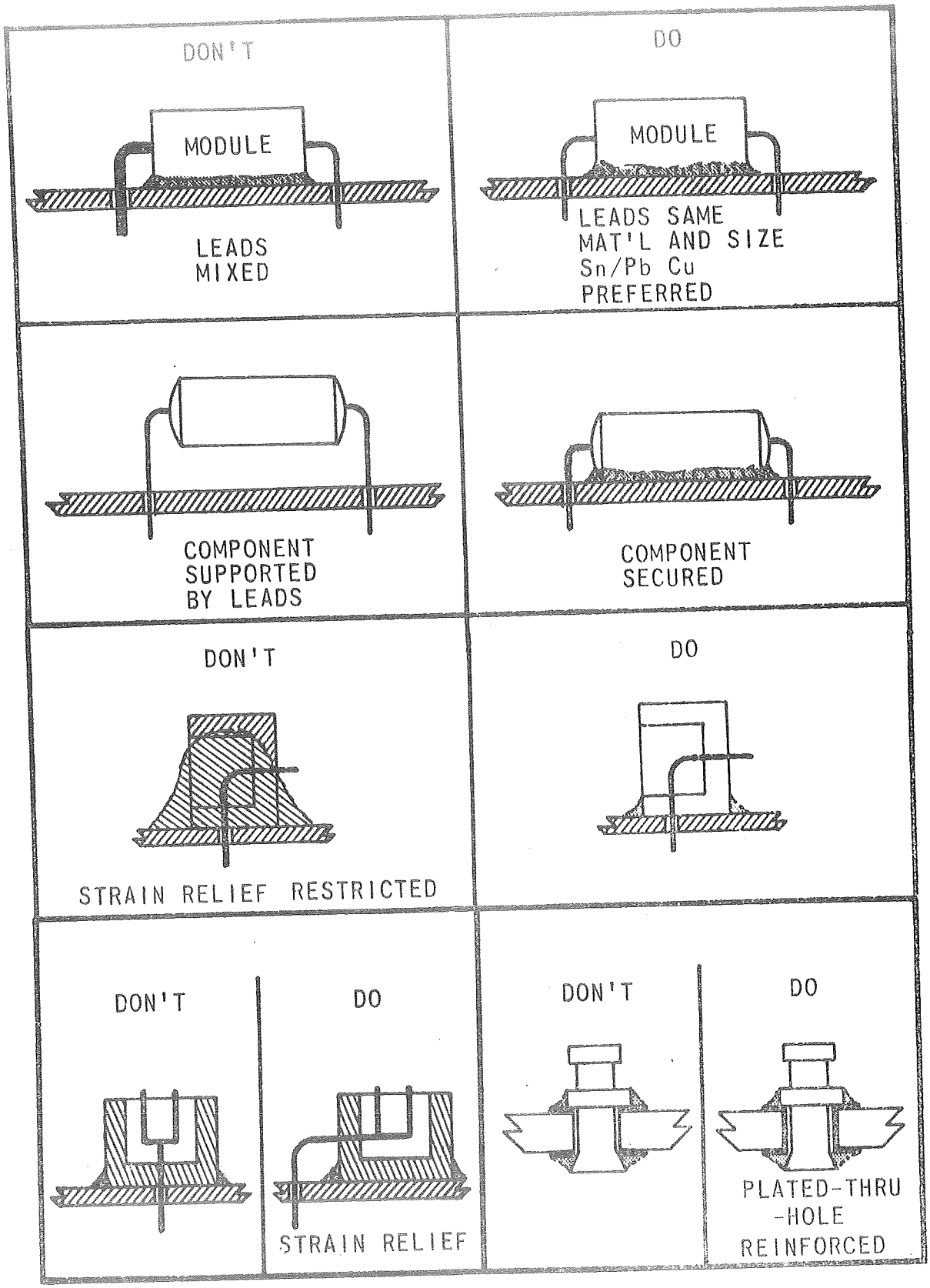


Figure 6 Parts Mounting Guidelines (Continued)

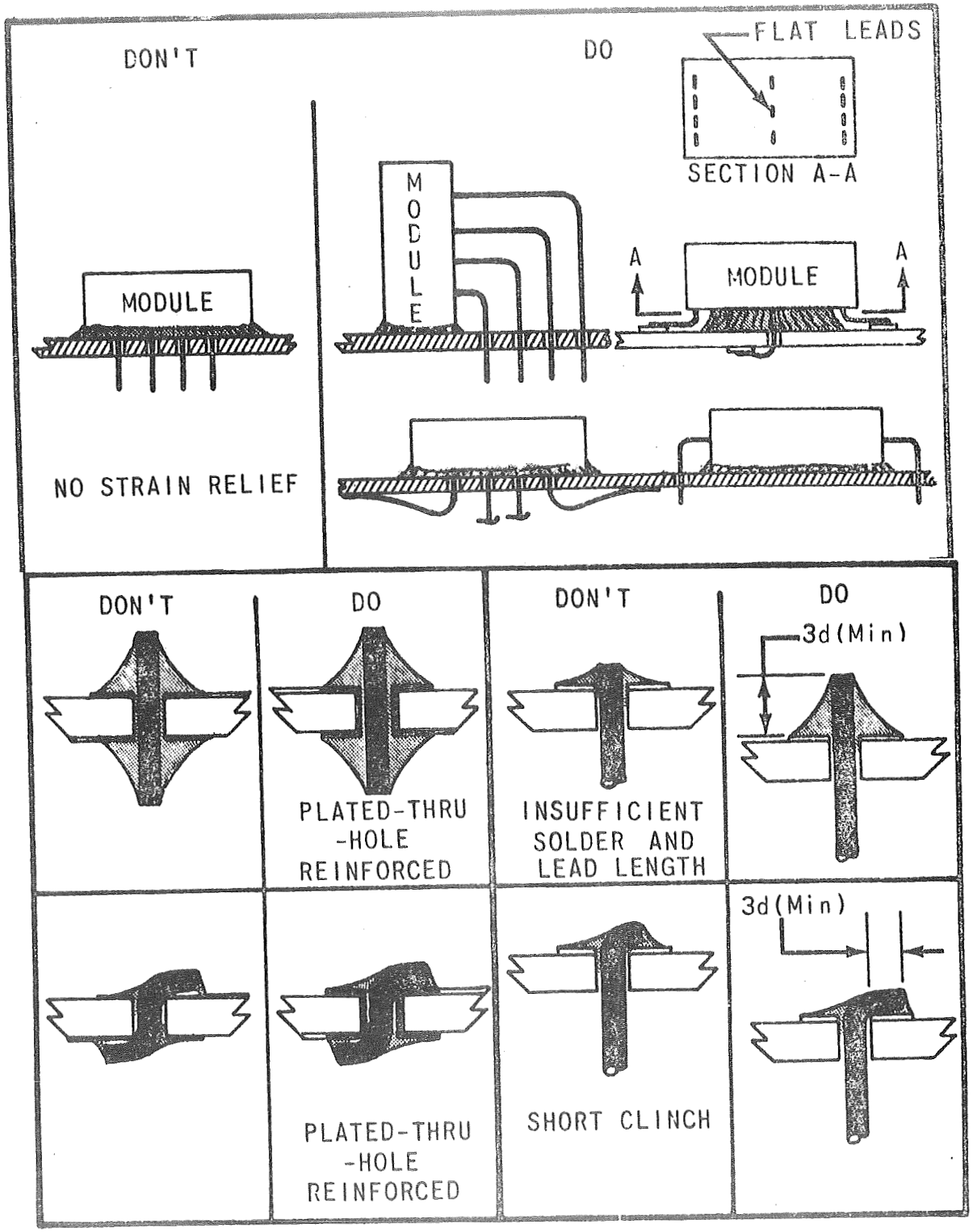


Figure 6 Parts Mounting Guidelines (Continued)

Table 4 Susceptability of Various Types of TO-5 Transistor Solder Joints to Cracking During Thermal Cycling

Type of Solder Joint	Approximate Cycles to Cracking
Standard joint	less than 100
Plated-through holes, lead free on one end	150
Standard joint, jumper wire, soldered both ends	300
Standard joint, 0.005 inch maximum hole/lead diameter	300
Eyelet, funnel, split, brass	300
Standard joint, silicone foam rubber spacer	350
Standard joint, lead free on one end	500
D loop, standard solder	500
Extra heavy solder, silicone foam rubber spacer	600
Extra heavy solder, 0.115 inch DAP spacer	600
Extra heavy solder, no spacer	700
52 percent nickel/48 percent iron lead, standard joint, free on one end	800
Extra heavy solder, D loop, silicone foam rubber spacer	800
Extra heavy solder, D loop, no spacer	850
Extra heavy solder, D loop, 0.078 spacer	900

Unless otherwise noted, all joints are Kovar leads, 60/40 tin-lead solder, TO-5 transistors mounted on 0.078 inch thick DAP spacers with 0.017 to 0.019 inch diameter gold plated Kovar through 0.026 inch diameter holes formed over and soldered per NPC-200-4.

5) A Westinghouse Report (Ref 15) describes an extremely comprehensive program investigating almost every aspect of solder joints for printed circuit boards. This work was undertaken under the technical direction of E. Ray Van Orden, of MSFC. The scope of this work included industry surveys, failure mechanism analyses, test of different solder alloys, and comprehensive test programs to evaluate the many variables involved.

The approach used by Westinghouse was to establish the relative influence of the many variables by building them into basic configurations intentionally selected as having a very low resistance to temperature cycling. These configurations were 1 inch square modules with nine pins, soldered into various types of printed boards, with different solder alloys, conformal coatings, solder joint designs, and application techniques.

Again, it was evident from the extreme complexity of the solder joint cracking problem that actual verification by temperature cycling testing is mandatory.

6) A report by Martin Marietta Orlando Division (Ref 16) describes an investigation of solder joint cracks in a Control Signal Processor and to develop solder joints capable of withstanding a goal of 1000 temperature cycles. This study mainly addressed the transistor mounting problem. The endurance of various transistor solder joints tested are summarized in Table 4. The profound benefits of stress relief and extra heavy solder is evident by the fact that 100 temperature cycles (-55 to +125°C) cracked over 50% of the standard solder joints, but with the incorporation of "D" loops and extra heavy solder, only one minor crack had developed by 900 cycles.

7) A report by Martin Marietta Orlando Division (Ref 17) describes a program to develop solder joints capable of withstanding a 12,000 thermal cycle goal on the Apollo Telescope Mount Gyro Processor. In this program, an "accelerated" thermal cycle was used in which 4000 test cycles were approximately equivalent to the 12,000 cycle goal. The benefits of lead stress relief, resilient spacers, heavy solder joints, and solder joints strengthened with tubelets, were clearly established.

8) A report by IBM (Ref 18) describes investigations resulting from a cracked solder joint in a Flight Control Computer. The goal was to implement solder joint fixes to enable the computer and other hardware to withstand 60 temperature cycles between -20°C and 85°C. The 60-cycle requirement was derived as equivalent to

2 years normal operations, plus a safety factor. The various hardware items were reworked utilizing the various different corrective actions depending on the practicality of implementation on each hardware item. The types of corrective action implemented were:

Offset pads;
Strain relief loops;
Tear-drop pads to permit heavy solder fillets;
Rubber spacers;
Tublets;
Crimped and soldered microlets;
Plated-through holes;
Percussive welding.

For the design of future production, 200 temperature cycles were used, and IBM selected offset pads, plated through holes, and resilient pads as the primary solutions.

A review of this report shows that transistors, and larger parts such as transformers, relays, and inductors constituted the majority of the problems.

9) The foregoing investigations and the salient conclusions of the Solder Joint Committee are reflected in the specification MSFC-STD-136, "Standard Parts Mounting Design Requirements" dated June 11, 1971 (Ref 19). This specification is recommended for Long-Life Assurance, and it should be particularly noted that the specification requires verification, by 200 temperature cycles, for all configurations which deviate from the specification. From past experience, it can be stated that on any large space program this approach will save many dollars in solder joint failure investigations, and corrective action programs to rework or redesign and rebuild hardware. Some of the diagrams from this specification are reproduced herein as Figures 7 through 13, but the entire specification should be obtained and directly implemented on long life programs, or used as a basis for establishing the packaging specification for a specific program.

10) On the Viking Lander Program, Martin Marietta Aerospace imposed rigid control on packaging techniques. Some features of this program are presented. For the mounting of transistor cans, a spacer was developed using berylia, a low coefficient of expansion material. This spacer, shown in Figure 14, is used as its own tool for accomplishing the first stress relief bend. The second bend is accomplished using an auxiliary tool which slips over the bottom of the spacer. Another interesting approach was the

approach used on axial lead parts such as resistors and capacitors. The concern was that on axial lead parts of small diameter, the solder fillet might envelop the 90°stress relief bend and, therefore, a special criteria was established when the distance of the axial lead to the board was less than 1.5 times the part lead diameter. This criteria is shown in Figure 15.

b. Other Factors Affecting Solder Joint Life - The factor of lead stress relief is the primary factor influencing solder joint life. Other factors, of secondary to no importance, are briefly described.

1) Effect of Solder Alloy - When cracked solder joints were investigated on the Saturn program, many solder alloys were researched and a number of selected alloys were tested in an attempt to solve the problem by an alloy significantly more resistant to temperature cycling.

Martin Marietta-Orlando tested six alloys (Ref 16) and concluded that 60/40 solder was optimum (Figure 16).

Westinghouse tests (Ref 15) showed that 97.5 percent lead, 1.5 percent tin solder had improved cracking resistance. However, the higher melting point (588°F) caused delamination of the copper on the printed circuit board. Also, variability in solder joint appearance created an inspection problem. A 50 percent indium, 50 percent lead solder exhibited somewhat improved crack resistance, melted at an acceptable temperature (400°F), but difficulty was experienced with maintaining a tinned tip on the soldering iron.

On the Viking Program, Martin Marietta Aerospace, concerned with the high temperature sterilization requirement, investigated other solder alloys. Again, no significant improvement was found.

A current investigation on different solder alloys, being conducted by R. N. Wild of IBM, will be completed in early 1973.

While certain solder alloys do appear superior to conventional 60/40 solder in some specific applications, it has been generally concluded by industry that the solder joint cracking problem must be mainly solved by packaging designs which remove external stress from the solder joints. Past, current, and new developments in solder alloy technology should be considered for possible application to a specific, and particularly difficult, problem, but the vast majority of potential problems of solder joint cracking are solvable, and should be solved, by the proven techniques of stress relief.

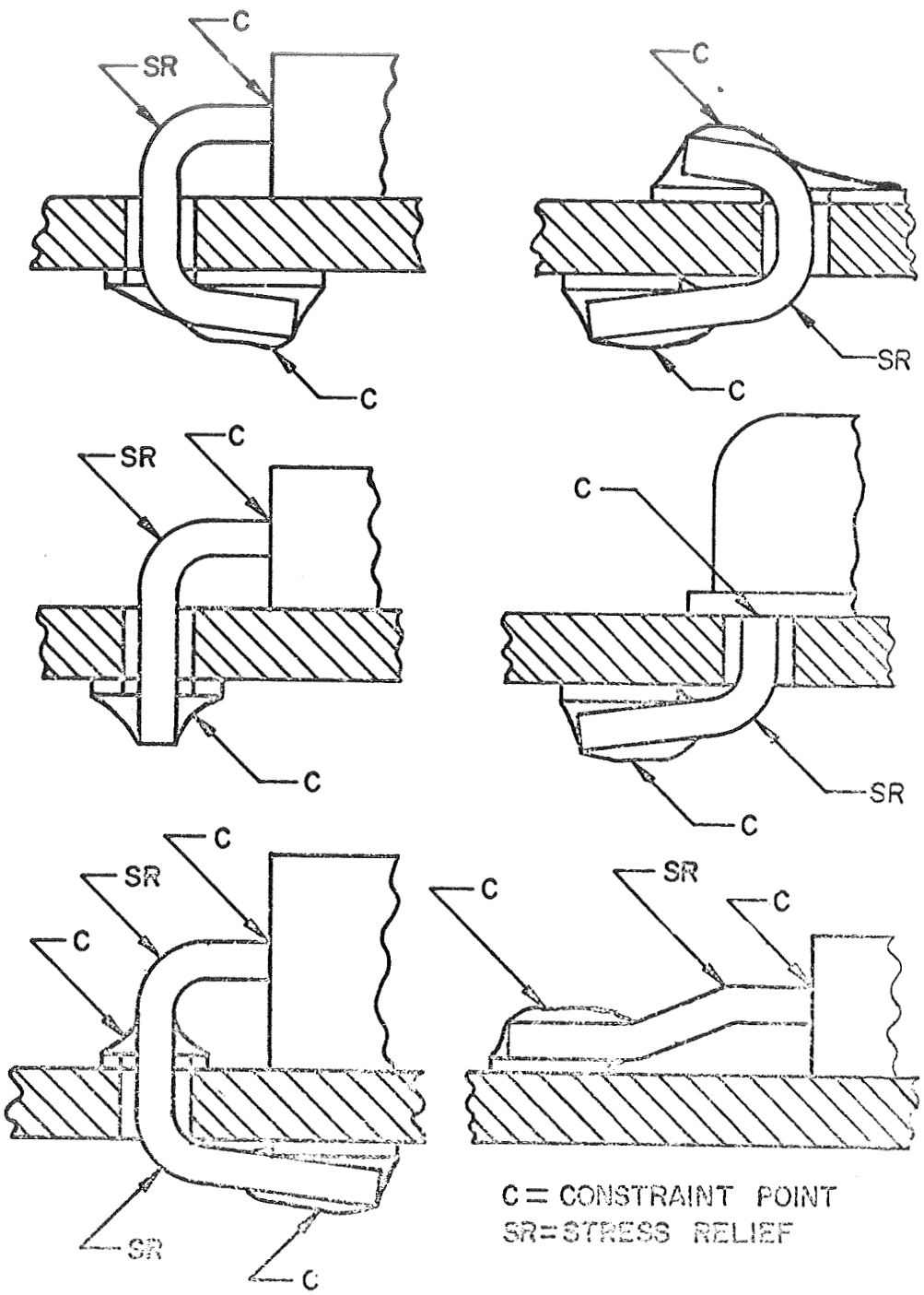


Figure 7 Parts Mounting

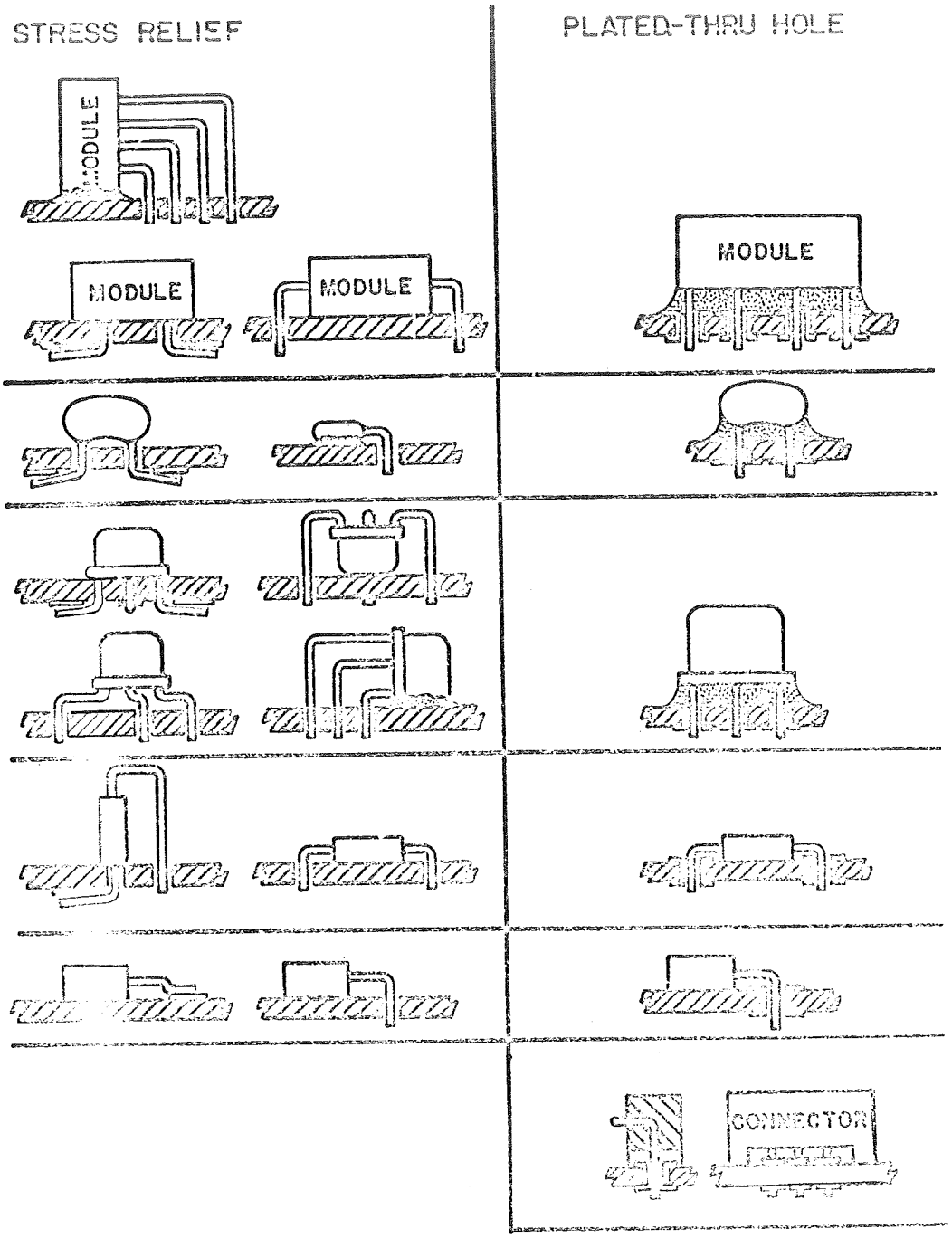


Figure 8 Mounting Configurations

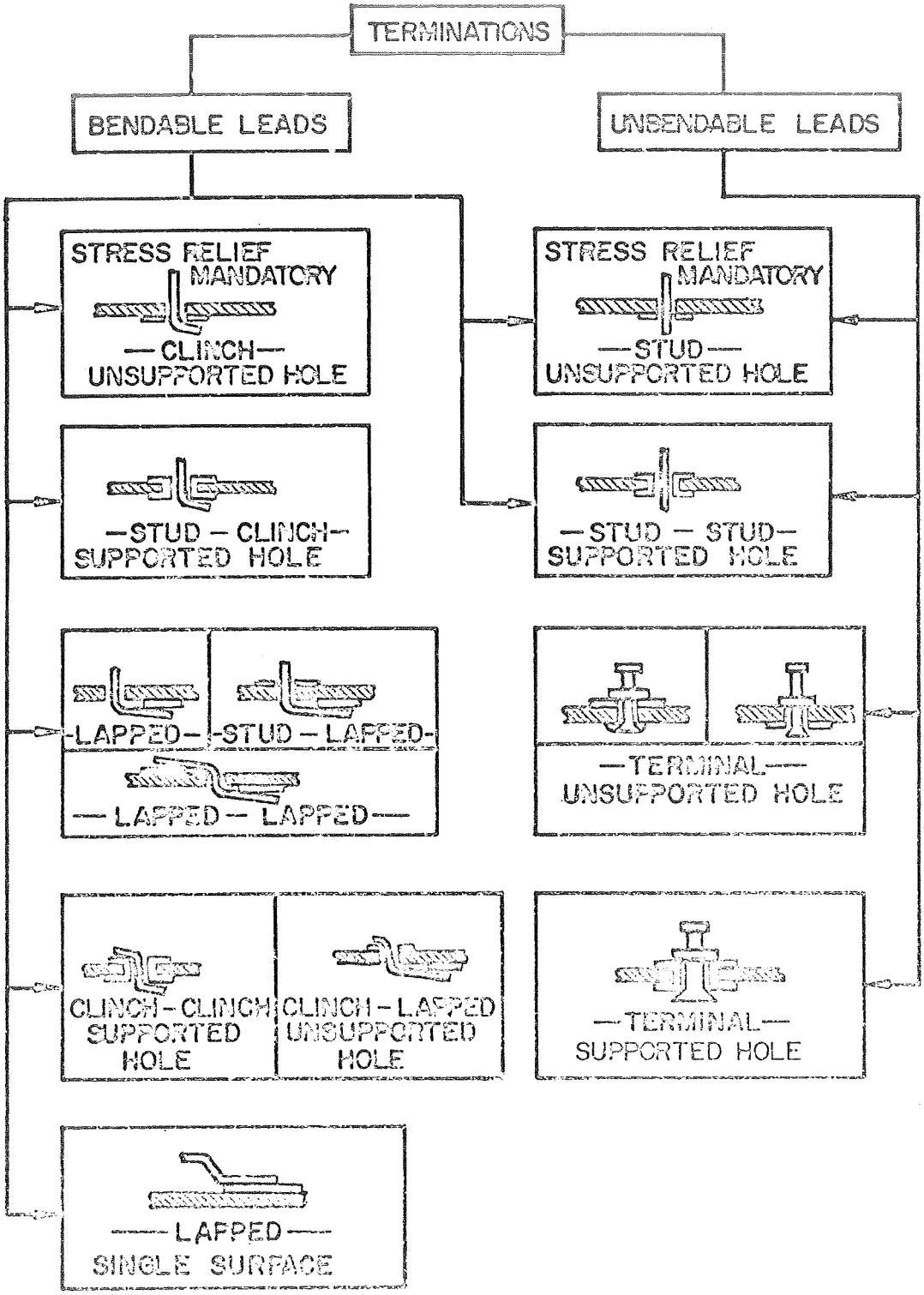
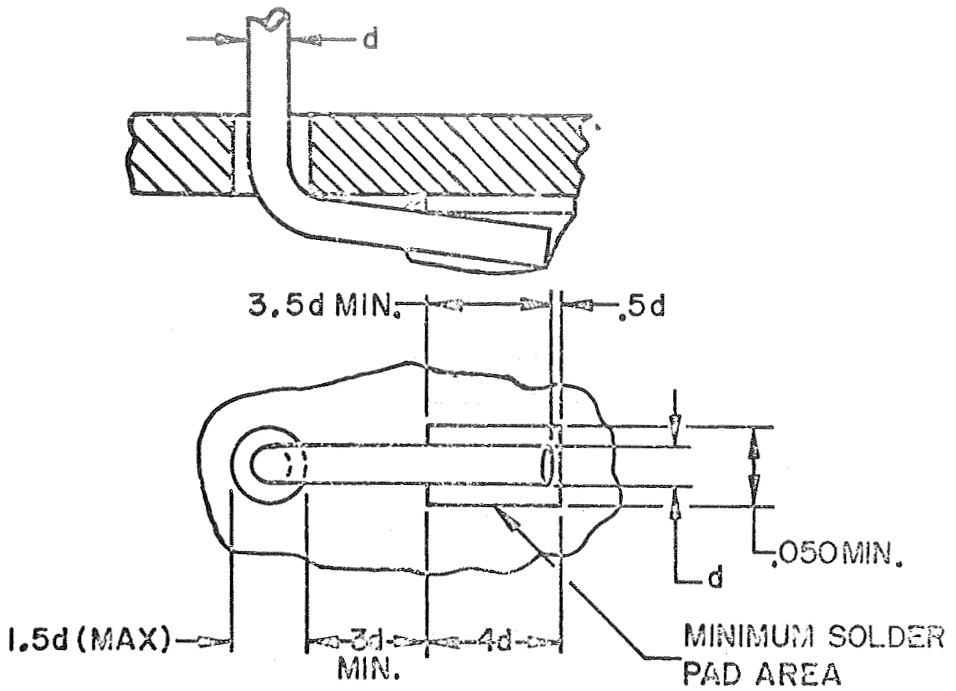
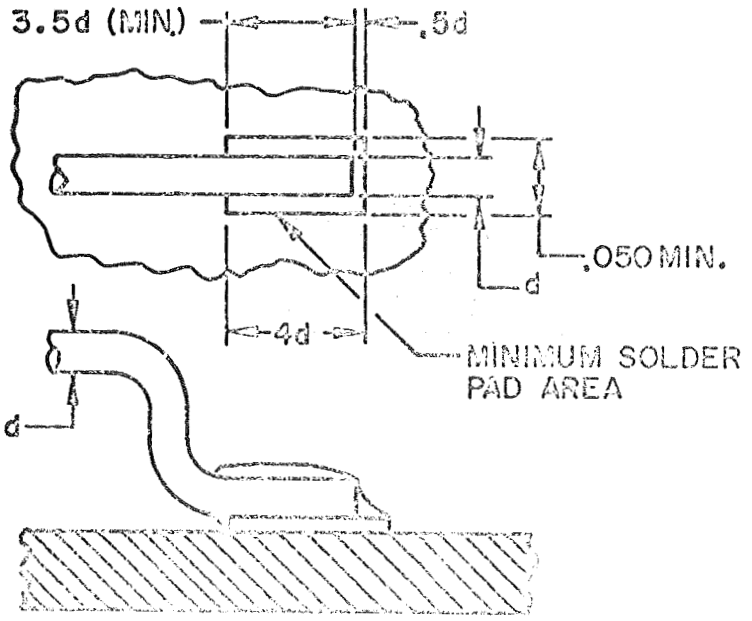


Figure 9 Acceptable Terminations



a. THRU-HOLE LAPPED TERMINATION



b. SINGLE SURFACE LAPPED TERMINATION

Figure 10 Round Lead Lapped Terminations

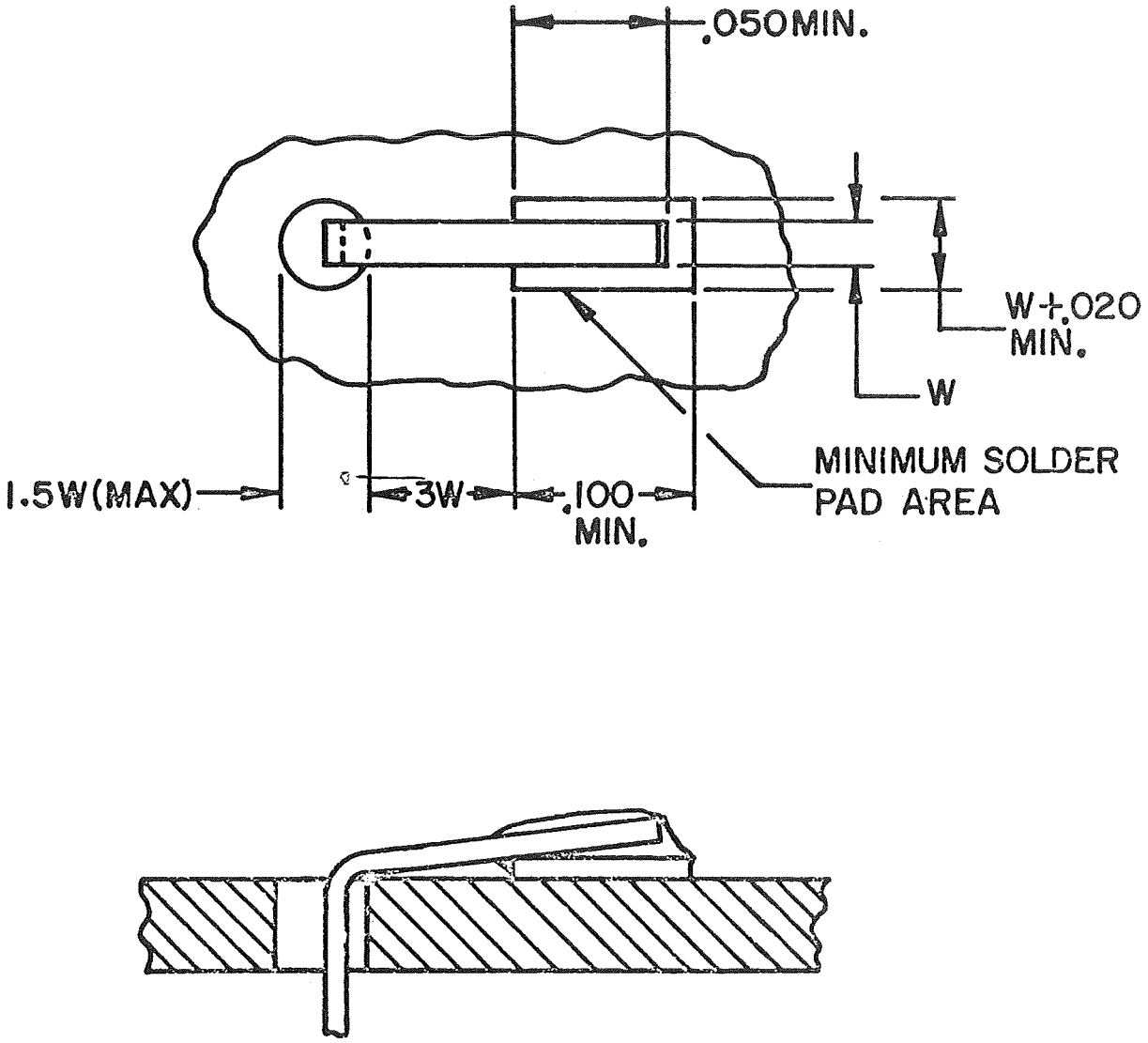
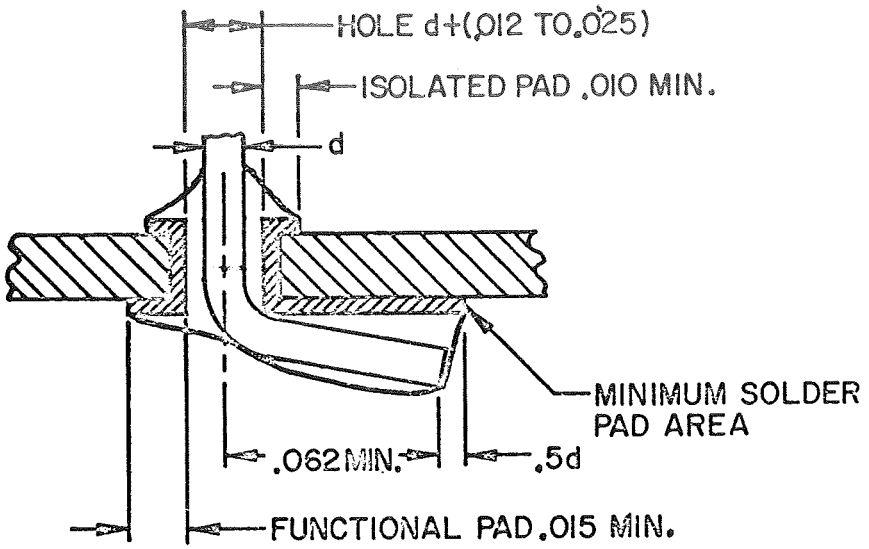
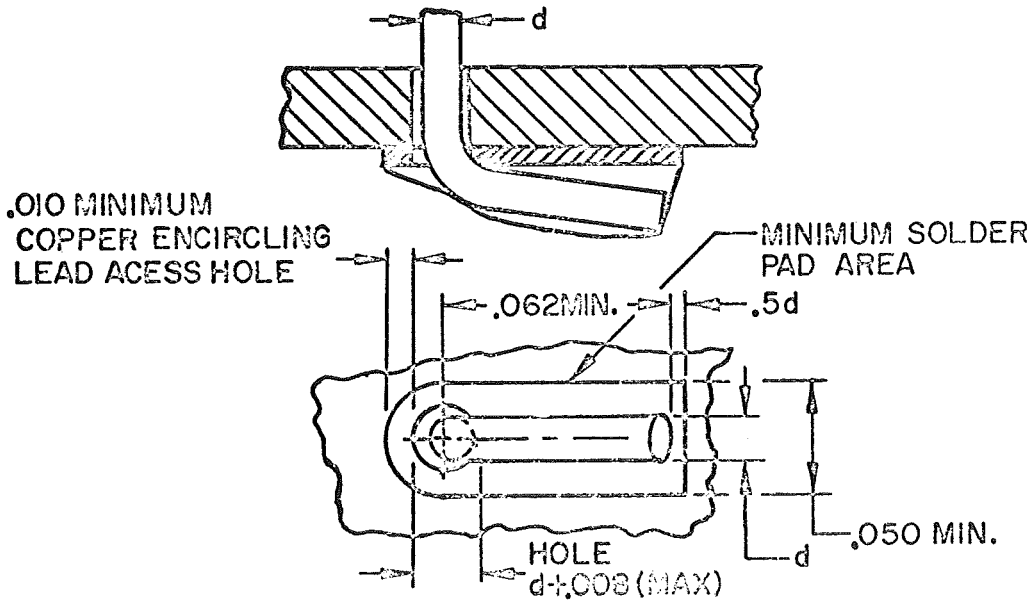


Figure 11 Ribbon Lead, Through-Hole Lapped Termination



a. PLATED THRU HOLE, TERMINATION



b. UNSUPPORTED HOLE TERMINATION

Figure 12 Clinched Termination

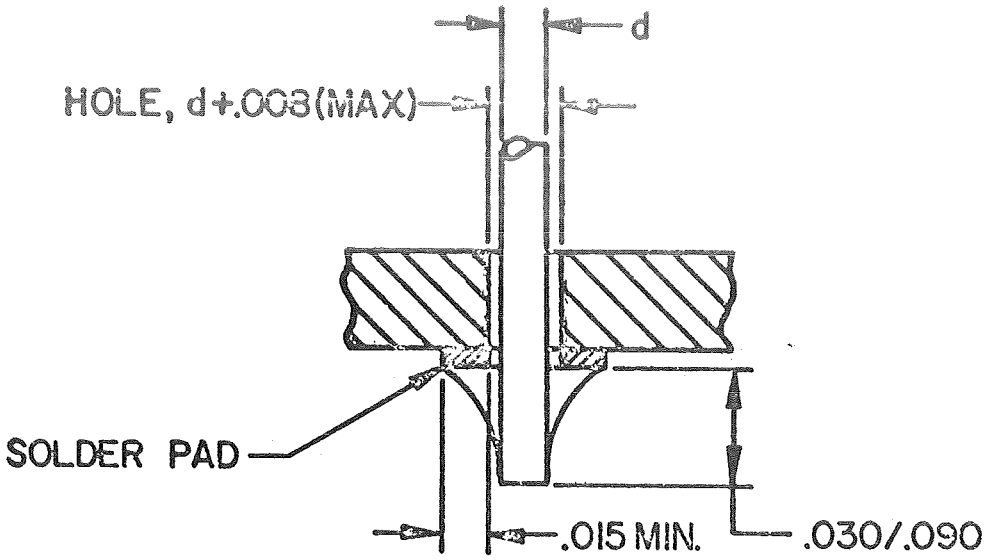


Figure 9. Stud termination.

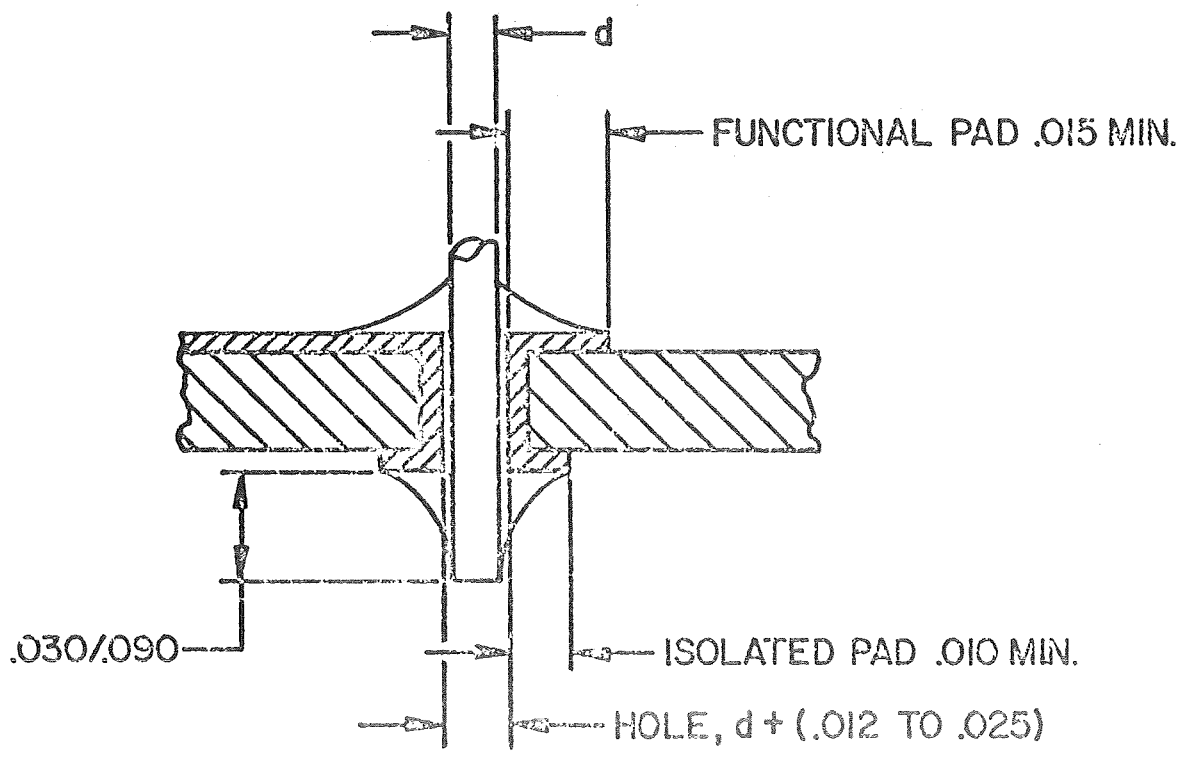


Figure 13 Plated-Through-Hole, Stud Termination

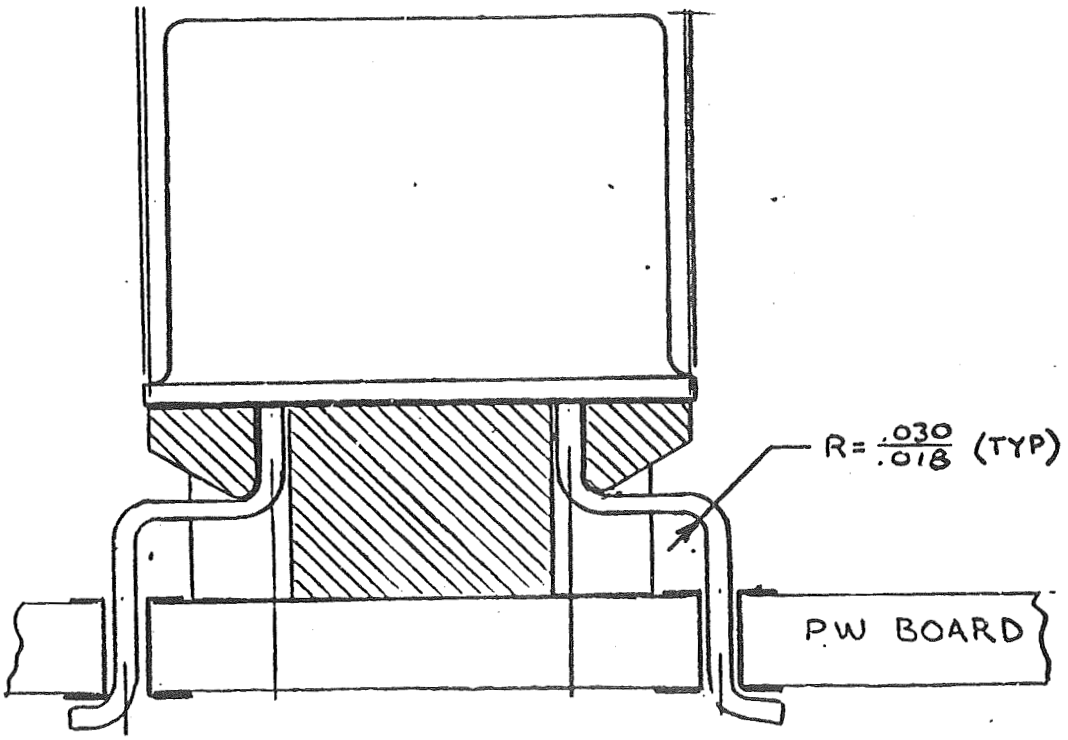


Figure 14 Berylia Spacer Developed for the Viking Program

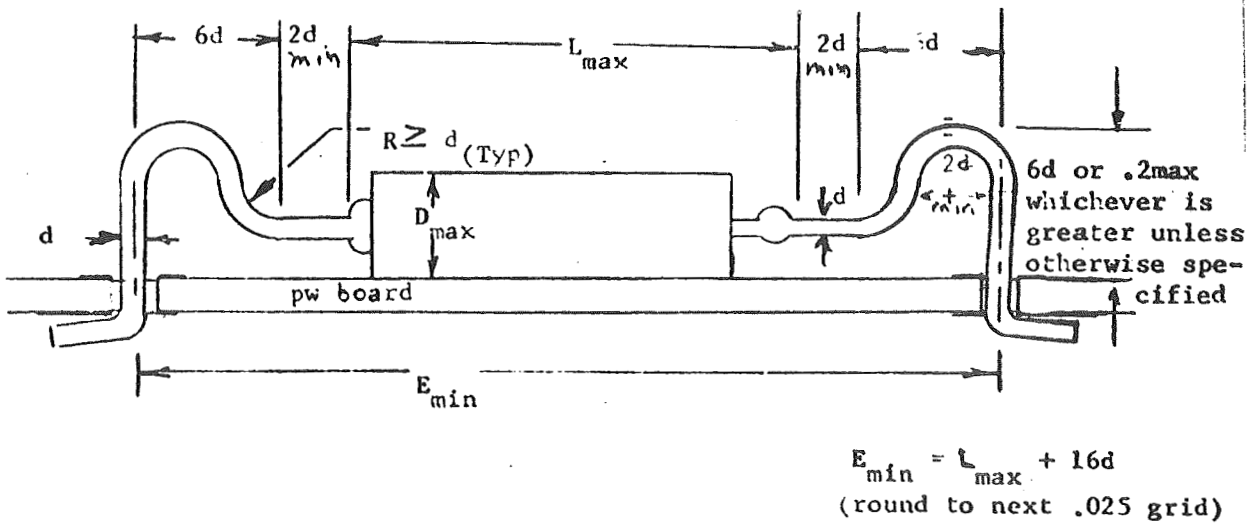


Figure 15 Viking Criteria for Small Axial Lead Parts

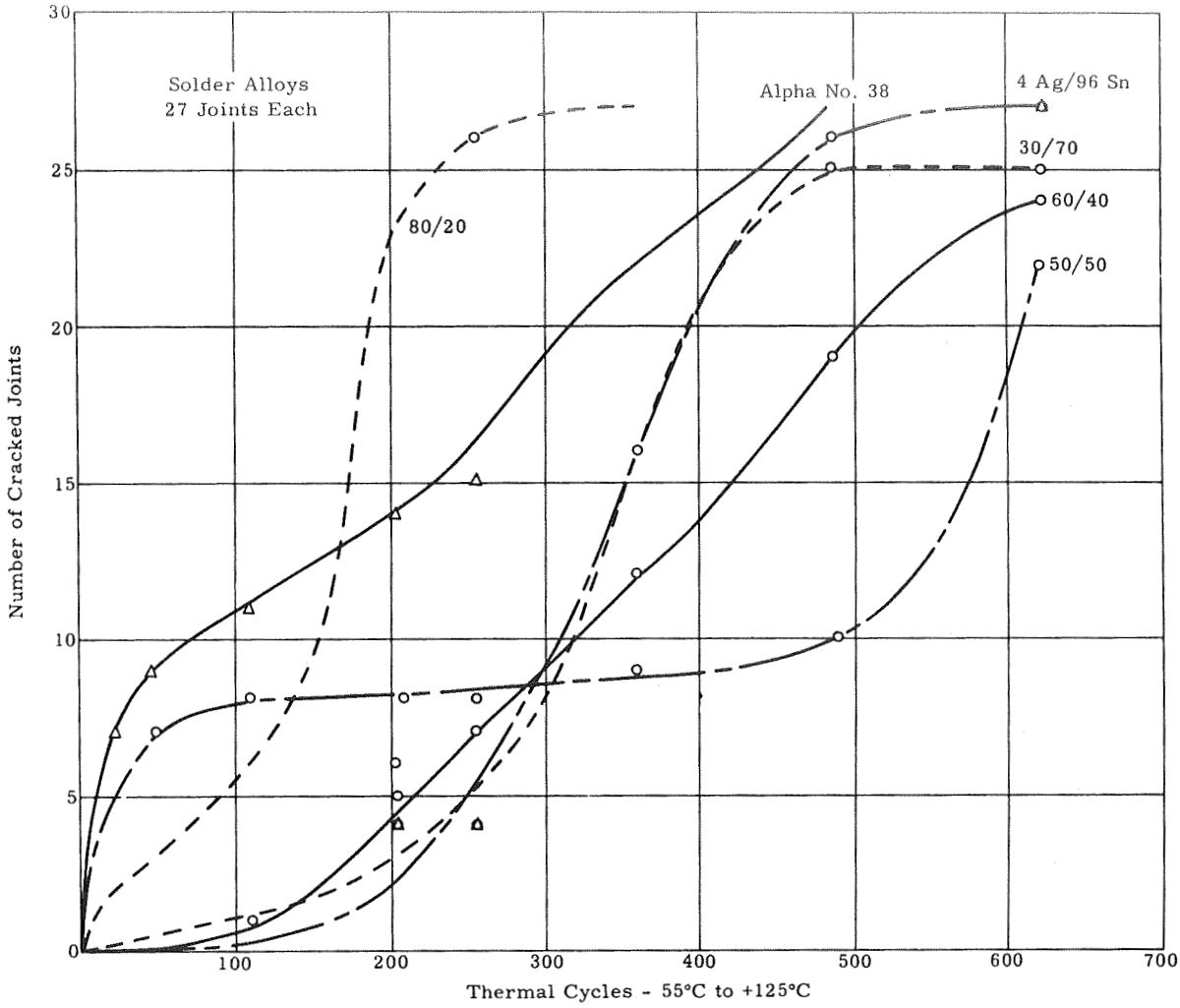


Figure 16 Effect of Different Solder Alloys in Solder Joint Cracking

2) Effect of Solder Embrittlement - In soldering gold plated leads, the gold dissolves in the solder and may form brittle intermetallic compounds and a joint more prone to cracking when stressed. This is less likely to occur with thin plated (50 micro inches) component leads in a large circular solder joint, than with the thin faying surface layers of solder such as under I.C. flat-pack leads.

Avoidance of the gold intermetallic problem has been accomplished by specifying pre-tinned leads, by successive wicking-off of the solder during hand soldering, or by pretinning the leads by a wave soldering machine or by immersing the leads into a solder pot and insuring a washing effect by moving the lead through the bath or by ultrasonic agitation.

MSFC-STD-136 requires that all terminating surfaces shall be solder-tinned *prior* to soldering.

Solder baths used for tinning must be periodically replaced to prevent a dangerous accumulation of gold. The specified limit, on the Viking program, was established at 0.1%. This value appears conservative, when compared to an investigation by R. N. Wild, (Ref 20), who concluded that there was no detrimental changes in the physical properties of solder joints with up to about 1% gold.

Large solder tanks require periodic chemical analyses of the solder to determine when the solder should be discarded, but, with small solder pots, it is usually more economical to frequently replace the solder than to incur the higher expense of frequent chemical analyses.

3) Effect of Lead Material - Solder joint cracking due to temperature cycling can occur from the internal stresses within the joint itself, when all external loads have been removed. Reference 17 quotes the temperature cycle life of clinched leads with 60/40 solder on single sided PC boards as follows:

	No. of Temperature Cycles (-100 to 185°F) to	
Lead Material	First Crack	10% Cracked
Kovar	250	700
Nickel-iron	--	800
Dumet	1000	1700
Copper	>4300	>4300

These results are the effect of the differences in the coefficient of thermal expansion between solder and the lead materials, as shown:

Material	Coefficient of Thermal Expansion in/in/°C x 10^{-6}
Solder	24
Kovar	5
Nickel	13
Copper	17

This thermal incapability of kovar transistor leads and solder, coupled with externally applied loads on the solder joint, has caused serious solder joint cracking problems. The preferred solution is the elimination of all external loads through stress relief techniques, and the use of plated-through-holes to provide a stronger solder joint. This approach is adequate for most programs. However, on one program (Ref 17), where the goal was 12,000 thermal cycles, testing revealed that heavy solder and copper tubelets over the end of the transistor leads were necessary.

4) Effect of Lead Flexibility - "Strain relief to a solder joint is best accomplished by mechanically fastening the component and using a flexible electrical link between the component and the solder joint. The ideal approach to strain relief is to use components having small, stranded or ribbon leads for flexibility. Unfortunately, the present concept of packaging electronic hardware is to have component leads strong enough to support the component. As a result, manufacturers provide large lead sizes and a variety of lead materials. These are usually overrated, electrically. To use components that are available today, lead configurations must be created that minimize stresses to the joint. This is accomplished by permitting the leads to flex." (Ref 14).

5) Effect of Solder Application Techniques - Westinghouse performed a series of tests (Ref 15) in which P.C. boards were dip soldered with 60-percent tin, 40-percent lead solder at temperatures of 425, 500, and 550°F and for times of 5, 10, and 30 seconds. Thermal cycling tests were then conducted and the results show no significant differences. Also, there were no significant differences between dip soldered, wave soldered, and hand-soldered joints.

When a crack is produced in a solder joint, metallographic examinations showed that the failure began and propagated in the solder matrix, and the solder remained bonded to the surfaces, except in a few cases which were found to be lead preparation problems. Westinghouse concluded that the failures were occurring in the solder and the properly executed practices in regard to fluxes, solders, temperature, time, and solderability of lead materials as called out in NHB/5300.4 (formerly NASA 200-4) gives solder joints which will not fail at the interface.

The amount of solder in the joint was found to have a most significant reduction on cracking rate, as described in the next paragraph.

6) Effect of Amount of Solder - Figure 17 from Reference 15, illustrates the marked improvement resulting from increasing the amount of solder on the joint. This test was conducted on nine-pin modules soldered into a single sided board with a 0.008 inch clearance which was bridged by PC 22 polyurethane conformal coating. With hand soldering, the amount of solder can be reasonable controlled. However, as the amount of solder increases beyond that amount necessary to give a contour joint, as specified in NHB 5300.4, the possibility of an operator piling solder on a nonwetted joint becomes a concern. Proper training of operators to assure that they observe wetting of surfaces before adding additional solder becomes important. Also, Westinghouse concluded the assurance of properly prepared surfaces so that wetting or alloying can take place is a must. A proper guideline is to use the maximum allowable solder permitted by NHB 5300.4 providing that this approach is not considered or used as a substitute for stress relief techniques.

7) Effect of Solder Joint Geometry - The resistance to cracking is influenced by the strength of the solder joint, and specifically the area of the shear planes through a cross-section of the joint. To insure good shear strength, geometric factors such as the lead diameter, hole diameter, and the distance that stud type leads project above the printed circuit board are important. A complete treatise on this subject is presented in Reference 15. The criteria of Figures 10 through 13 address this important factor.

8) Effect of Plated-Through-Holes - In a plated-through-hole, as compared with a bare hole, the solder flows into the hole and provides a solder joint with substantially increased shear strength. The use of plated-through-holes as a solder joint reinforcement technique is highly recommended. The superiority of the plated-through-hole is shown by Figure 18 from the Westinghouse data of

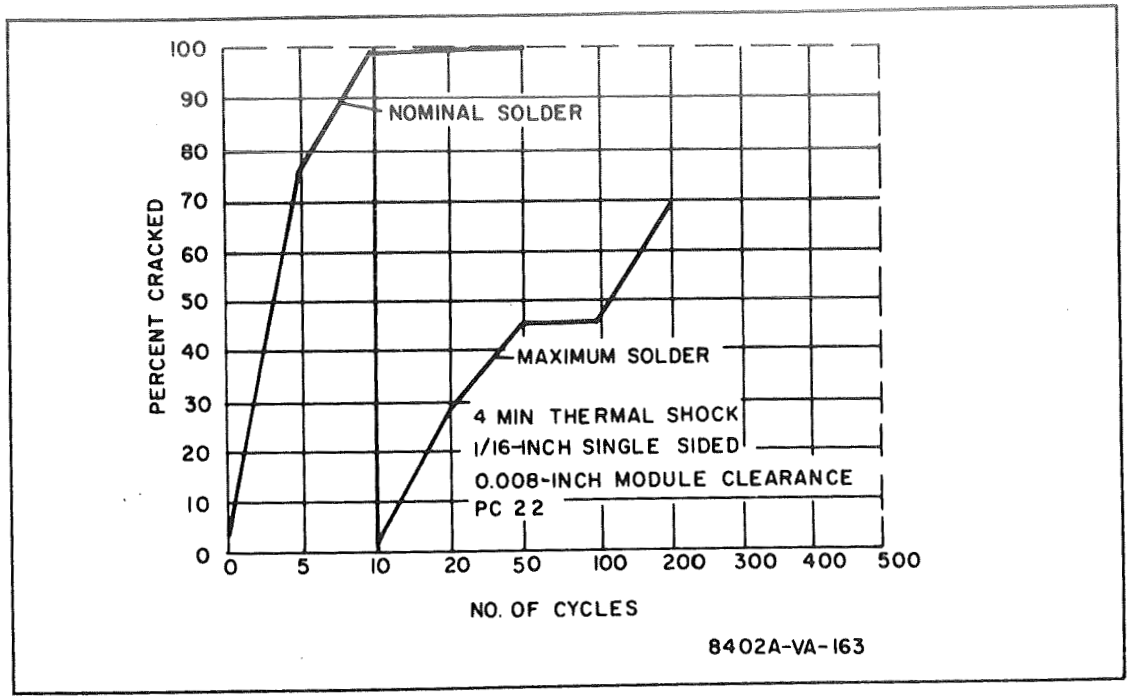


Figure 17 Effect of Solder Amount on Cracking Rate (Ref 15)

Reference 15. This data also shows that the thicker board was advantageous. MSFC-STD-136 encourages the use of plated-through-holes but cautions that this method of joint reinforcement is insignificant for boards 0.032 inch thick or less.

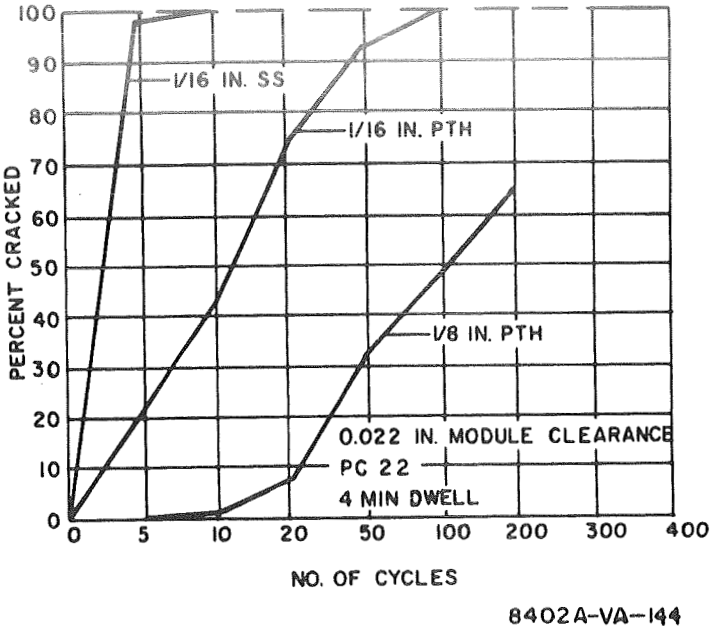
It should also be stated that since the high expansion of PC boards in the vertical axis is a primary source of stress, the use of thicker PC boards with bare holes can aggravate a solder joint problem. This, however, becomes somewhat academic if the proper techniques of stress relief are employed.

9) Effect of Type of Parts - The major problems of solder joint cracking have been encountered with transistors and larger parts such as modules and relays. The most serious transistor problems have been the result of several factors working in combinations: The low expansion of Kovar, the use of tall spacers with a high coefficient of thermal expansion, the use of bare-hole PC boards, and the use of heavy coats of conformal coating. This combination is absolutely catastrophic to solder joints and cracking may occur in a very few temperature cycles.

With large modules, the leads are sometimes not ammenable to easy stress relief solutions and, in additional, loads are imposed on solder joints from *lateral* expansion and contraction effects as well as the vertical loads.

10) Effect of Conformal Coating - This subject is discussed in a following section of this report. Minimum thickness should be used. In particular, the bridging of conformal coating between flat bottom components and the PC board must be avoided unless the particular strain relief technique removes all stress from the solder joints in spite of the very adverse effects of such bridging. Also, bridging can actually break weak ceramic or glass parts such as ceramic dual-in-line integrated circuits.

11) Spacers and Resilient Pads - Rigid spacers under transistors contribute to solder joint stress when lead stress relief bends are not employed. Some problems have been solved with resilient spacers or pads. When employing this solution, a material must be selected that retains its resiliency at low temperatures and is acceptable in the applicable vibration environment. Reference 17 concludes that resilient spacers under transistors should have a Shore Hardness of below 45 on the A scale, and that larger parts should have softer spacers.



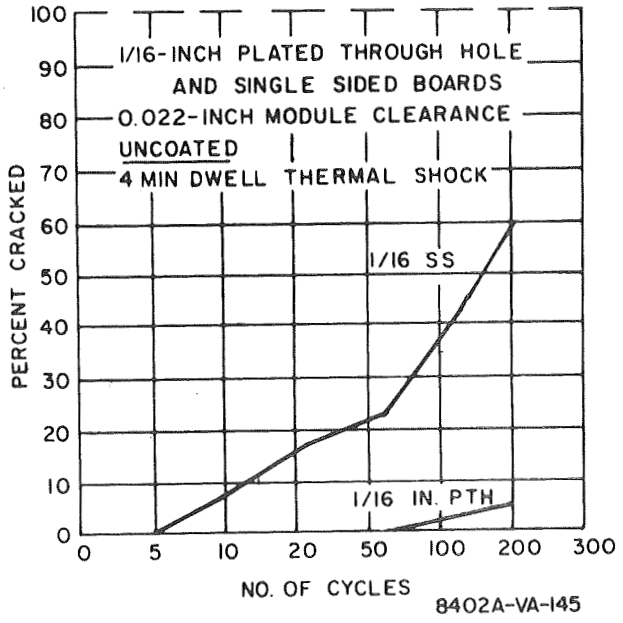


Figure 18 Comparison of Plated-Through-Holes and Single-Sided Boards (Ref 15)

3. Summary

The majority of cracked solder joint problems are caused by external stress on solder joints resulting from inadequate stress relief in the design, rather than defects in the original solder joint itself. Transistors (Kovar leads) and large modules represent the greatest threats. The problem cannot be adequately solved by the selection of the solder alloy, or improvement of soldering technique, but must be solved by employing stress relief features in the design such as those specified in MSFC-STD-136. The problem can be alleviated by the use of flexible part leads, as opposed to heavy rigid leads; by using the maximum permissible amount of solder; and by using plated-through-holes, since these provide a significantly stronger solder joint. Verification of the packaging design should be accomplished on early prototypes or on test samples representative of the packaging design, by subjecting the hardware to temperature cycling between -55°C and 100°C, and inspecting for cracked solder joints. The nominal value of 200 cycles required by MSFC-STD-136 is recommended, although actual mission or program requirements should be reviewed to determine if this value should be adjusted. It should be remembered that equipment (on earth) not stored in a temperature controlled environment may experience a daily temperature cycle of 15 to 20°C, and could acquire 1826 cycles in 5 years.

Precise data correlating the severity of actual in-service temperature cycling with the severity of accelerated temperature cycling could not be identified in this study, but it seems reasonable that a 15°C temperature excursion would be about one-tenth or more probably, less than one-tenth as severe as the 155°C temperature excursion specified by MSFC-STD-136. On this premise, 1826 daily temperature cycles over a five year period would equate to about 183 accelerated cycles. This conclusion is in rough agreement (but on the conservative side) with the IBM work reported in Reference 18. This report concluded, from actual field failure data, that 46 accelerated cycles from -20° to 85°C was equivalent to 2 years of field service life. It should also be remembered that the temperature environment in spacecraft, in orbit is often more benign and constant than while the same equipment is on the earth. However, it is important that the equipment not have cracked solder joints at the time of insertion into orbit, and therefore the above guidelines are still applicable even though the orbital environment is benign.

E. CONFORMAL COATINGS

1. Introduction

The use of conformal coatings on long-life hardware for environmental protection and mechanical support is generally still a valid design requirement; however, experience on present programs has identified problems so serious as to cause consideration of its elimination. These problems concern primarily thermally induced stresses on parts and interconnections. It has been established that the major cause of solder joint failures is thermal fatigue due to stresses induced by the differences in thermal expansion of the materials in a solder joint configuration; i.e., printed circuit board, conformal coating; part lead, part body, solder, etc. Conformal coating, especially if improperly used, can be a great contributor to solder joint stresses, as well as to part stresses and breakage.

2. Life Limiting Problems and Solutions

a. Part Stressing - Numerous studies have dealt with the problems of conformal coating induced stresses on part bodies causing breakage of brittle ceramic or glass parts, such as glass diodes. These studies have established the major cause to be thermally induced bending stresses on the part body due to heavy application, uneven application, heavy fillets of conformal coating around the part body, or bridging under the part body.

An example of the adverse effects of bridging of conformal coating was encountered on the Skylab program with ceramic dual in-line integrated circuits. During temperature testing it was observed that the glass frit bond between the two halves of the package developed cracks. Further testing showed that devices from all manufacturers tested were affected in this manner and that bridging of conformal coating under the devices was a principle contributor to the cracking. It was necessary to replace many cracked devices and install the new devices without bridging of the conformal coating.

Manufacturers have minimized these problems by:

1) The protection of fragile parts such as glass diodes by flexible plastic tubing or heat shrinkable sleeving such as polyethylene terephalate, covered by MIL-I-23053/7. Also, a soft

flexible coating is sometimes applied prior to the conformal coating. This technique has been used when heavy, rigid conformal coatings are used. However, heavy rigid coatings should not be used.

2) The use of flexible conformal coatings and the use of application techniques to provide their uniform thicknesses with minimum fillets around part bodies, and with no bridging under flat bottom components. The flexible polyurethane, such as PR1538 and Solithane 113, applied by spray, spin and cure techniques are examples of this solution. This technique is recommended where both environmental protection and mechanical support are required.

3) The development of very thin, deposited coatings such as Parylene C, which result in negligible thermal stresses during thermal cycling. However, this type of coating is expensive and provides no mechanical support. However, it can be applied to a board, and then followed by a thin flexible polyurethane coating for mechanical support.

b. Solder Joint Cracking - Many investigations (two of which are summarized) show an increase in solder joint failures when conformal coating is entrapped between a part body and solder joints on printed circuit boards.

1) The Westinghouse study (Reference 15) showed that all coatings tested caused a decrease in the number of thermal cycles to 100% failure over uncoated boards when the coating was allowed to bridge or fill the gap between the test module and the PCB solder joint. The test modules were one inch square with nine leads soldered directly through the printed circuit board. Figure 19 plots a comparison of the results from an uncoated assembly with three assemblies where the module was bridged with a polyurethane (PC-22), a filled polyurethane, and RTV 3140. This comparison indicates the catastrophic effect of the entrapment of conformal coating between part body and printed circuit board.

2) A report by Teledyne Ryan Aeronautical (Reference 21) presents a very comprehensive investigation of solder joint stressing and the role played by conformal coating. This investigation was initiated by a solder joint failure on the Apollo LM Landing Radar. Exhaustive investigations, both theoretical and experimental were conducted. The solder joint failure

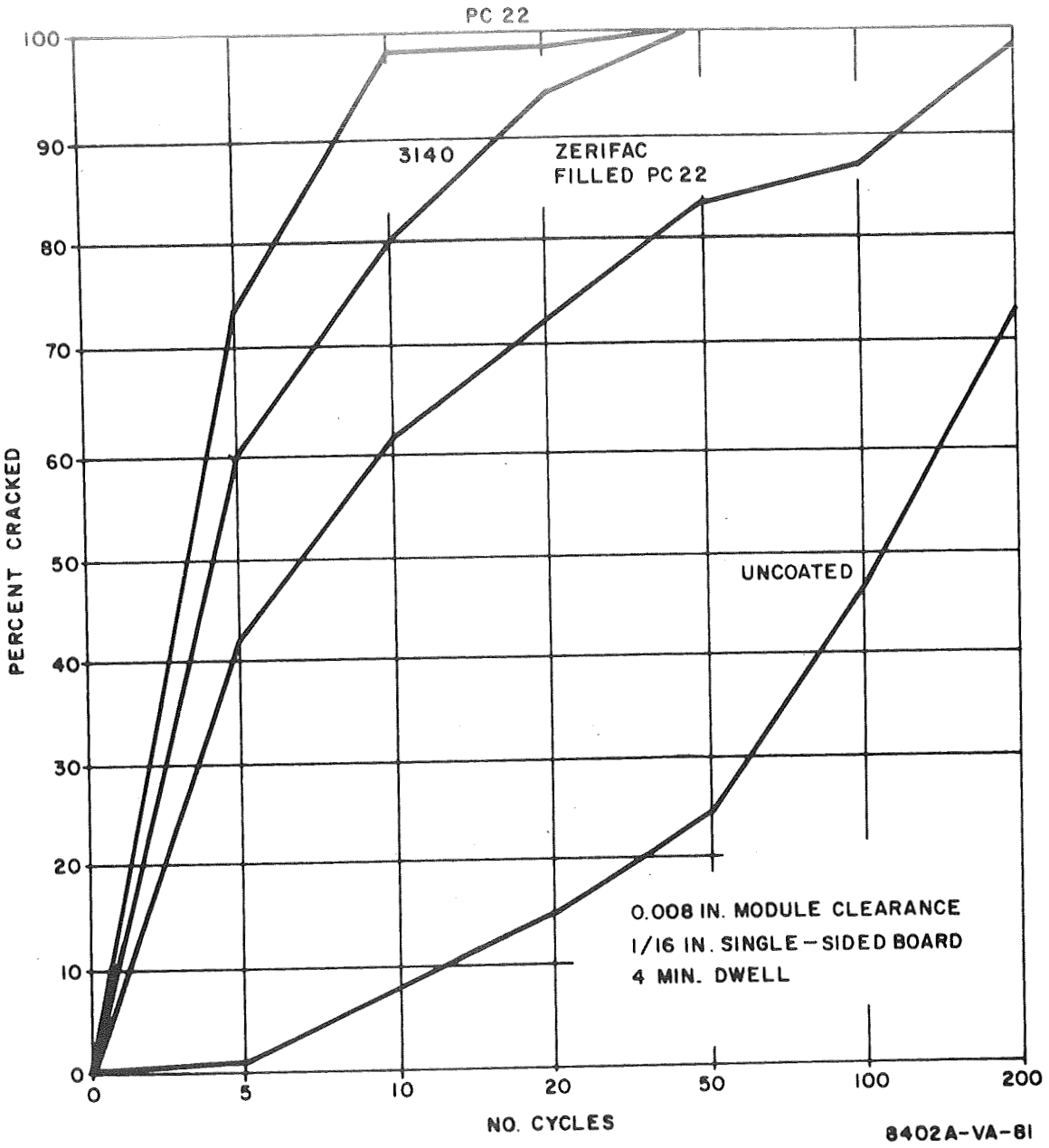


Figure 19 Effect of various Conformal Coatings on Soldered Joint Cracking Rate (Coatings Completely Under Modules) (Reference 15)

was caused by the bridging of polyurethane conformal coating between an I.C. carrier and the printed circuit board. Figures 20 through 22 show the effect of the conformal coating on solder joint loads. Intensive studies made to find a method of removing the conformal coating concluded that no acceptable method existed. Studies of solder joint strengthening techniques were performed. Final trade-off studies on whether to rework or build new assemblies for units not completed resulted in the decision to build new assemblies.

c. Coating Coverage - Conformal coatings as used in aerospace electronics are generally epoxies or polyurethanes conforming to MSFC-PROC-257A or 293A, or MIL-I-46508A applied so as to conform to the contour of the assembly being coated. There generally exists a specification requirement for 100% coverage of all surfaces; however, without excessive coating thickness, or spot build-up, actual complete coverage of the underside of leads, or high points, is seldom accomplished in production. Table 5 is an assessment of typical conformal coating coverage from a Hughes Aircraft Company report (Reference 22). This report concludes that conventionally applied epoxy or polyurethane coatings do not provide the complete coverage required for ultra high reliability humidity protection without the undesirable coating thickness discussed previously. It can be concluded that when high resistivity (10^{10} ohms and above) under humidity is required for long-life hardware, the conventional epoxies and polyurethanes are not adequate. A thin (.001 inch and less) coating with complete coverage of the deposited Parylene C type must be developed and used. In addition, the expense and lack of mechanical support of these thin coatings require that more serious consideration must be given to the actual environmental requirements of the design before 100% coverage is specified. If the design requires both 100% coating coverage and mechanical support, a composite of a deposited and conventional polyurethane must be developed and used.

3. Summary

Conformal coating, necessary for environmental protection and mechanical support on long-life hardware, is a major cause of both part and interconnection failure when not properly selected and applied. The following guidelines should be of major consideration in the design of long-life hardware:

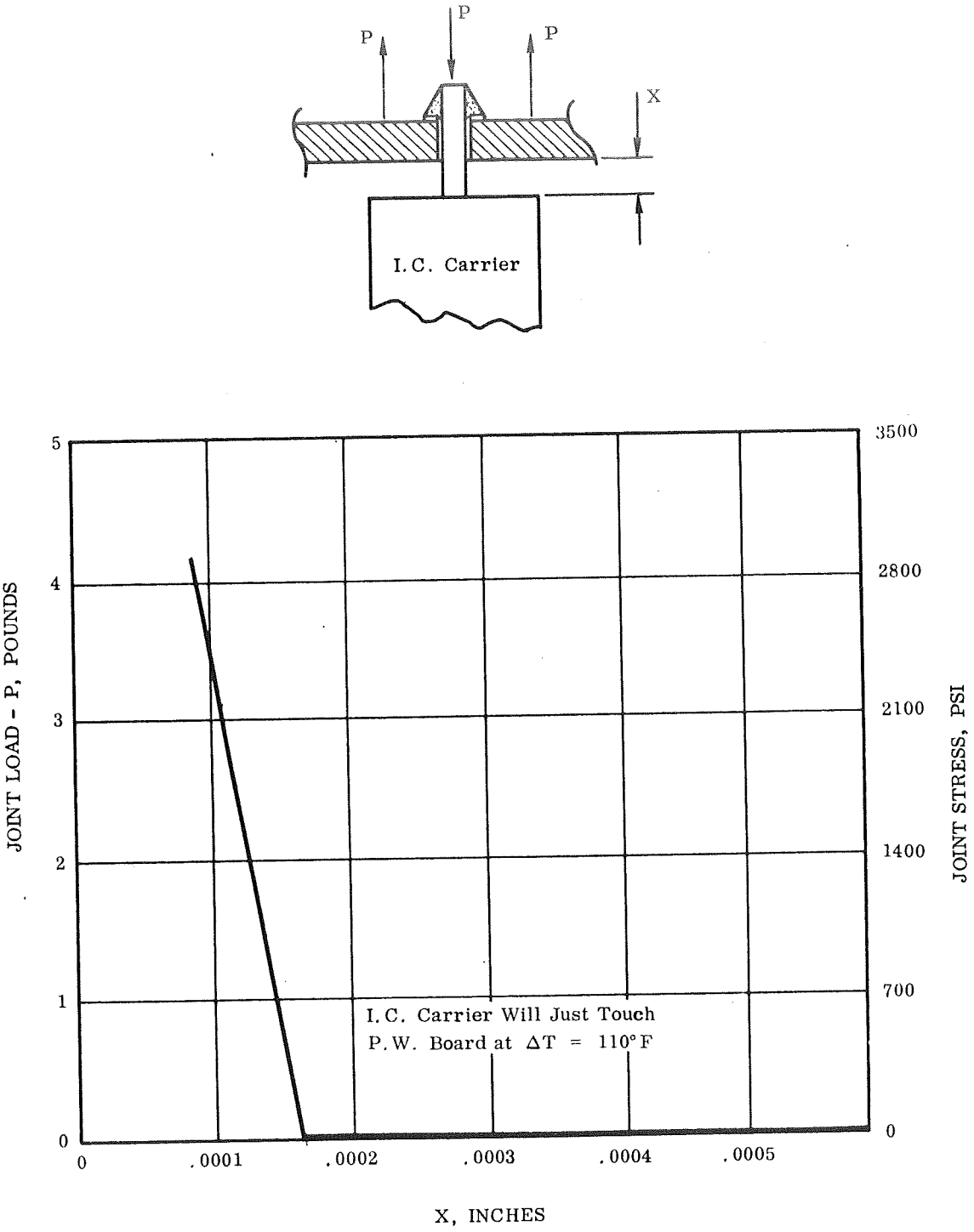
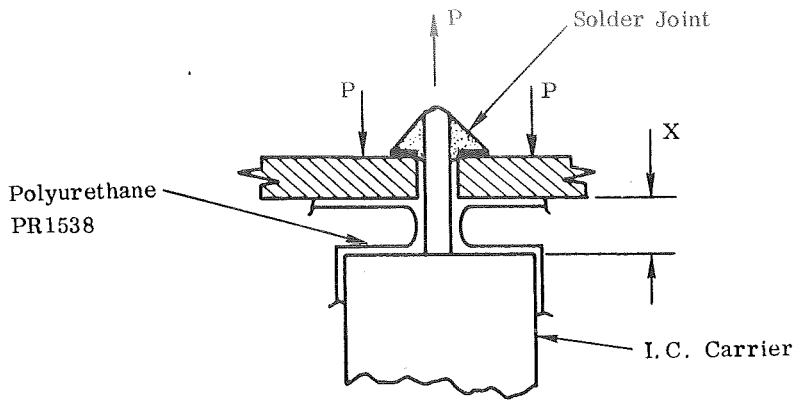


Figure 20 No Conformal Coating (Reference 21)



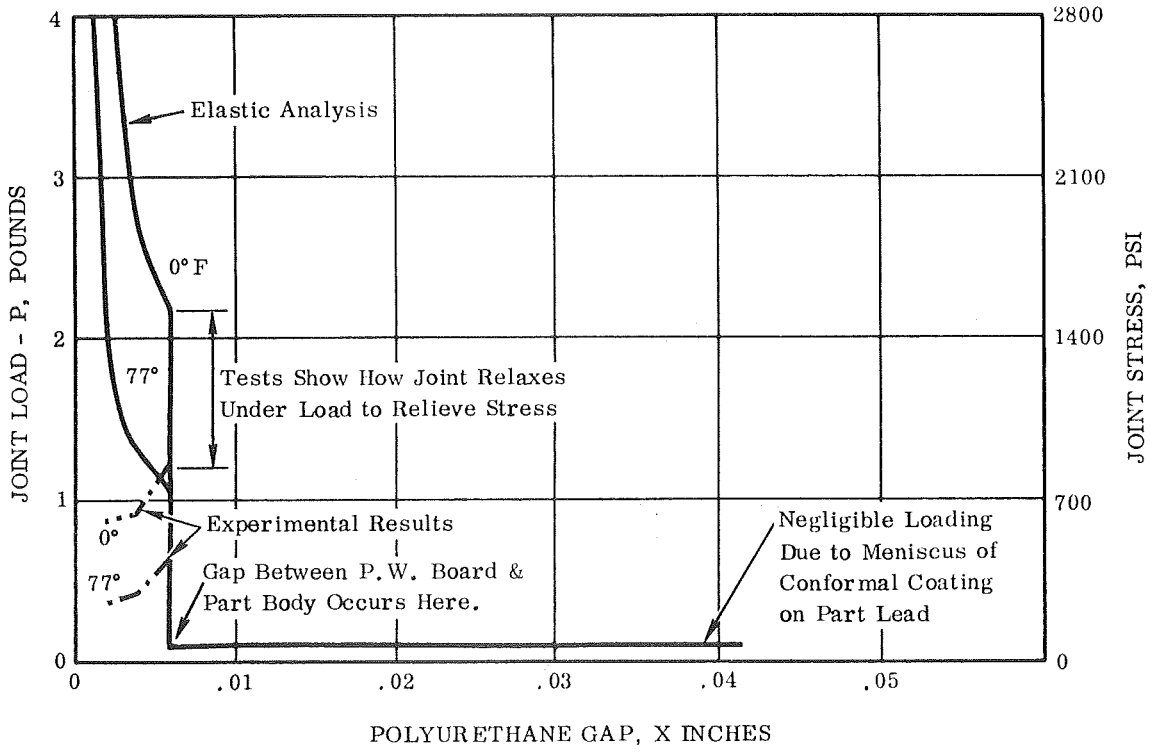


Figure 21 No Bridging of Conformal Coating for Gaps X Greater Than 0.006 Inch (Reference 21)

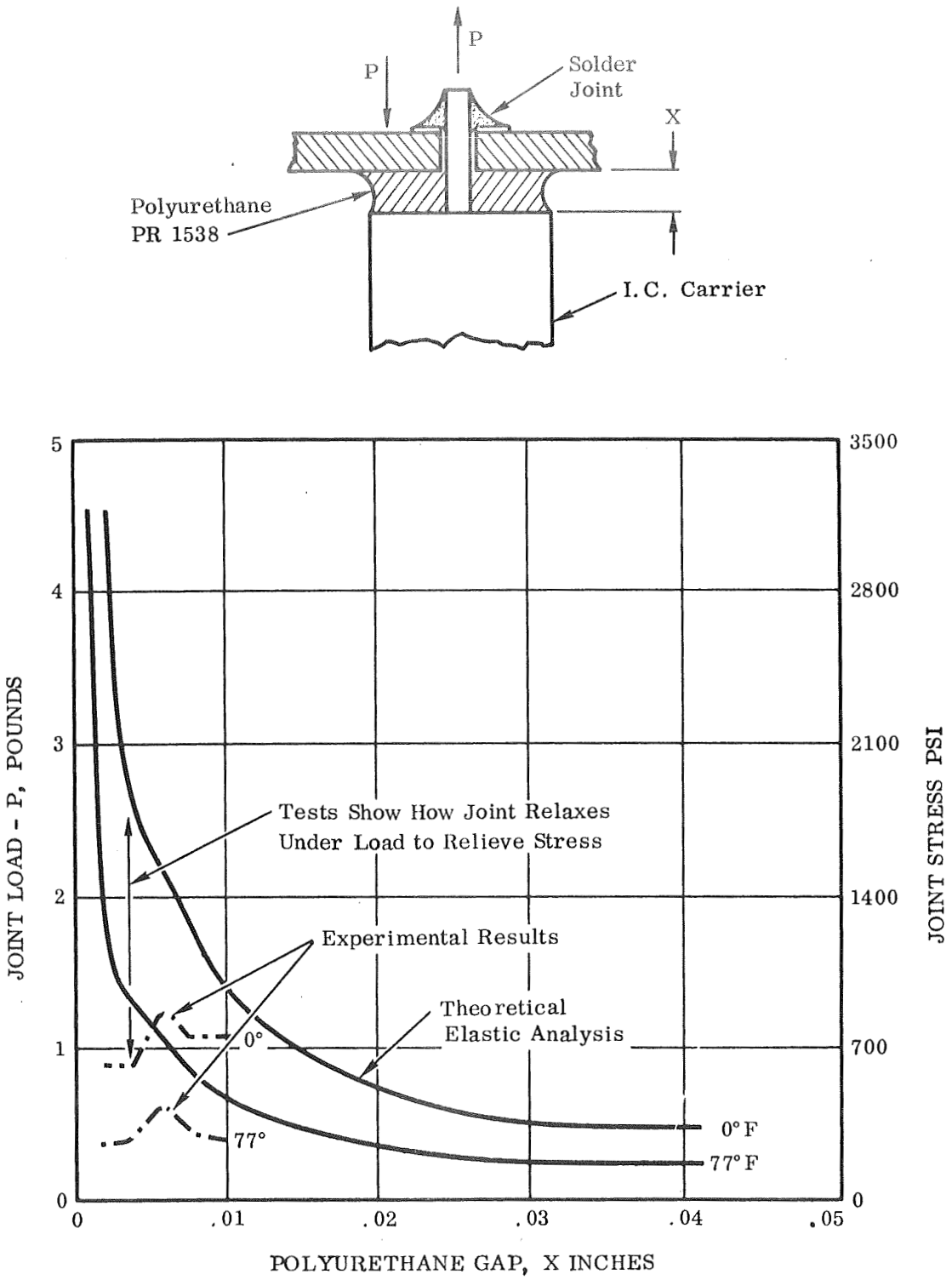


Figure 22 Light Bridging of Conformal Coating (Reference 21)

Table 5 Degree of Circuitry Coverage Provided by Conformal Coatings, in Percent of Items Coated

Coating	Printed Circuit Board Traces	Solder Points and Terminals	Tangent Points (Circuitry Beneath Components)	Component Leads	Chances of High Humidity Survival in Un-Sealed Units
None	0	0	0	0	0
Epoxy or Poly-urethane Varnish, 0.001 inch Thickness	85	10	20	10	30
MIL-I-46058, Types ER and PUR, 0.002 Inch Thickness	100	50	95	50	75
Composite Poly-urethane, 0.005 Inch Thickness	100	99	99	90	97
Parylene Type, 0.001 Inch Thickness	100	100	100	100	99.9+

a. Coating Coverage - Careful consideration of the electrical and environmental requirements of the system must be given to determine the actual need for 100% coverage of the assembly. If the actual operating conditions of the equipment require very high resistivity, under adverse humidity conditions, then 100% coverage provided by a deposited coating of the Parylene C type is recommended. Otherwise, the coating provided by a sprayed and spun flexible polyurethane should be adequate. Where mechanical support, as well as ultra humidity protection is required, a 1 to 2-mil sprayed flexible polyurethane over the deposited coating is recommended.

b. Coating Thickness - The minimum thickness for mechanical support is recommended. Flexible polyurethane coatings less than 4 mils in thickness with no entrapment of coating under part bodies and minimum fillets is recommended, except as discussed where maximum humidity protection is necessary.

c. Coating Application - Application of the coating by spraying and spinning to prevent fillet build-up as the coating tends to flow down and around the part is recommended. The coating must be applied in a manner to prevent bridging under slot components such as multi-pin modules. Fragile glass and ceramic parts require sleeving prior to coating.

F. ENCAPSULATED MODULES

1. Introduction

The vibration, shock, or acceleration capability of electronic hardware can be substantially increased by encapsulating the parts, usually with an epoxy or a polyurethane potting material. However, the potting system must be selected with the utmost care to prevent failures from the high internal stresses resulting from temperature changes. This section summarizes nine investigations and develops guidelines for encapsulated modules.

2. Life Limiting Problems and Solutions

a. Abstracts of Source Data

1) An investigation reported by Herbert Dorfman (Ref 23) clearly establishes the profound influence of the potting material on electrical connections in an environment of temperature cycling. In this investigation, a matrix of Dumet wire and nickel ribbon were welded to intentionally produce weak welds of 5.4 and 7.7 lb. These welded assemblies were flow-coated with a flexible epoxy, cured and then encapsulated with five different potting compounds, with the properties shown in Table 6. The modules were then subjected to 10 temperature cycles from -30°F to +165°F.

The results, shown in Table 6 show that the filled and unfilled epoxy potting produced many weld failures. The microballoon filled epoxy and the 10-lb polyurethane foam markedly lowered the incidence of weld failures and the 2-lb polyurethane foam produced no weld failures, even though the welds were weak. It was also determined that the weld failure rate depended on the spacing between the welds; the higher the spacing.the greater the failure rate.

2) The microtransducer developed by LMSC to measure external stresses in encapsulated modules reveals, per Ref 24, the temperature induced stresses in a number of encapsulants. Samples of material were thermally cycled from -55°C to +100°C allowing the sample to stabilize before recording each reading. Figure 23 illustrates the variation and magnitude of the stress transition associated with these encapsulants.

Table 6 Weld Failures Due to Temperature Cycling

(a) Material Characteristics

Resin No.	Type of Material	Specific Gravity gm/cm^3	Shrinkage %	Coefficient of Thermal Expansion
1	Microballoon Filled Epoxy (Pigmented Black)	0.7	0.3	10.5×10^{-6}/°F
2	Filled Epoxy (Pigmented Black)	1.30	0.78	37×10^{-6}/°F (Range R.T. to 150°F and 69×10^{-6}/°F (Range 150° to 200°F)
3	Unfilled Epoxy	1.08	0.95	56.3×10^{-6}/°F (Range 80° to 120°F)
4	Polyurethane Foam (10-lb/cu ft density)	0.16	0.3	0.14 to 0.20 $\times 10^{-6}$/°F
5	Polyurethane Foam (2-lb/cu ft density)	0.03	Not available from vendor	17×10^{-6}/°F

(b) Summary of Failures

Resin No.	Type of Material	Number and Percentage of Weld Failures in Each Module*			
		Nominal Weld Strength: 5.4 lb		Nominal Weld Strength: 7.7 lb	
		No.	%	No.	%
1	Microballoon Filled Epoxy (Pigmented Black)	3	3.6	0	0
2	Filled Epoxy (Pigmented Black)	9	10.7	10	11.9
3	Unfilled Epoxy	23	27.3	14	16.7
4	Polyurethane Foam (10-lb/cu ft density)	4	4.8	0	0
5	Polyurethane Foam (2-lb/cu ft density)	0	0	0	0

*Each module contained 84 welds (14 welds/circuit x 6 circuits).

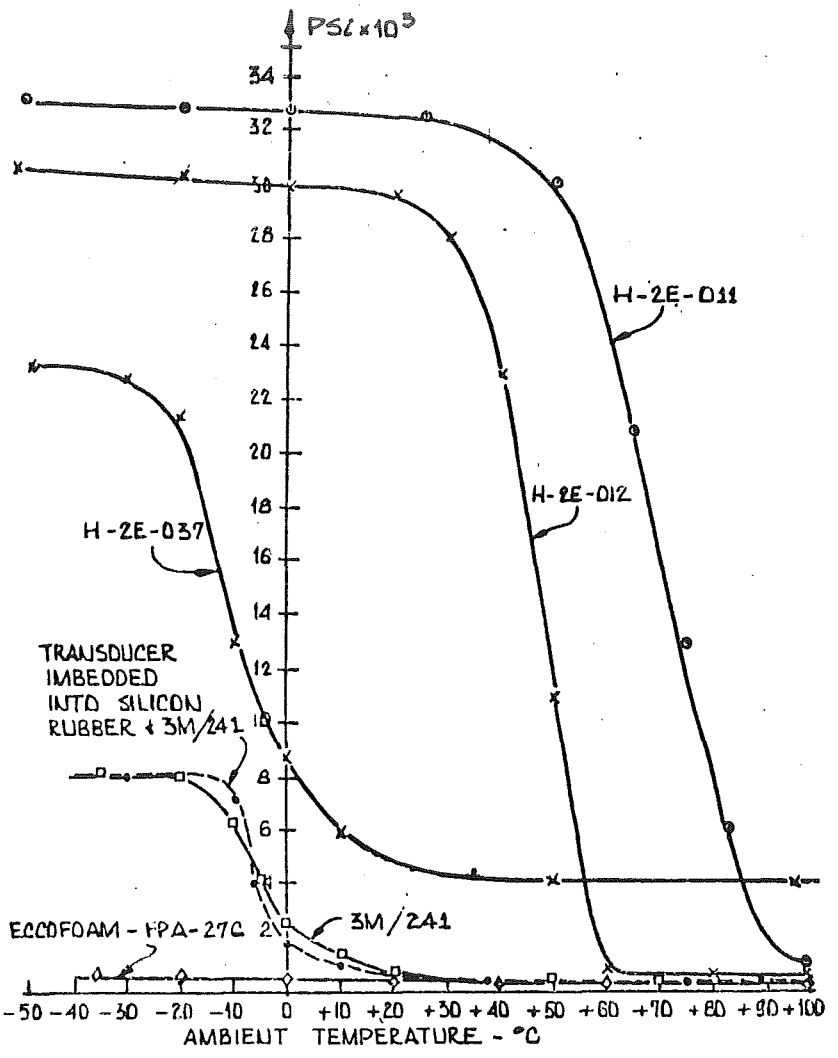


Figure 23 Stress Characteristics of Encapsulants (Ref 24)

The stress transition temperature range for Epocast H-2E-011 is between 90°C and 50°C. For Epocast H-2E-012, a rigid encapsulation, the internal stresses increase 30 times. The structural characteristics of Epocast H-2E-037 remain quite constant and high in the temperature range above +10°C. 3M/241 Scotchcast reflects a 15 times increase in internal stress. No stress transition was found in Eccofoam FPH-276, thereby showing its use to isolate electronic components from the stress characteristics of rigid and semiflexible encapsulants. The effects of coating a

component with an isolation material prior to encapsulation in a semiflexible encapsulant resulted in a slight shift in the transition range. This data raises the question as to the value of isolation coatings on components encapsulated in semiflexible materials.

The large change in internal stresses that occurs within a small ambient temperature range, indicated by the microtransducer measurements, can result in degradation of electronic circuit performance if the change in the parameters of pressure sensitive components cannot be tolerated.

3) A paper by C. E. Brown (Ref 25) stated that modules consisting of hybrid circuit assemblies, power transistors, a printed circuit card, and a motherboard, were encapsulated with a semiflexible epoxy to offer structural support yet permit necessary thermal expansions and contractions of the components.

This module form was subjected to a 16-cycle thermal test with each cycle consisting of a 30-minute exposure at +150°C followed by the same exposure at -65°C. Following this test, problem areas were noted with solder cracks, encapsulant softening, and ballooning effects in the encapsulation material.

The encapsulant (3M CRP-241) was too soft at temperatures above +125°C for use around output pins. Solder cracks resulted from thermal stresses due to insufficient relief provisions. The ballooning effects in the semiflexible epoxy resulted from too thick an application of silicone rubber on the module prior to its encapsulation.

Corrective measures included looping the interconnection leads and using a light coating of silicone rubber on all stress relief points without causing the module case to balloon. Subsequent testing evidenced lack of further problems incorporating these measures plus output pins, tinned instead of gold plated, and soldered on the underneath side of the motherboard. Also, the shoulder of the pins was encapsulated in a rigid header of 2850 GT epoxy and the remainder of the module was encapsulated with semiflexible epoxy.

The redesigned modules revealed no discrepancies after being exposed to 48 thermal cycles.

4) A report by Carter and Burkhardt (Ref 26) describes a problem currently under investigation by Sandia Corporation. On one program, Sandia encapsulates P.C. boards with a glass microballoon filled epoxy. However, prior to encapsulation, the boards, with parts, are first precoated with a semiflexible polyurethane to provide higher insulation resistance and to reduce electrical performance shifts due to potting pressures on the parts. A solder joint failure was encountered and it was postulated that the problem might be solved by coating only the parts and then soldering the parts to the boards. The test program conducted to investigate this is described:

Three samples of each of three different configurations of PC boards were fabricated and subjected to 40 temperature cycles between -40°F and 160°F. The three configurations are described.

a) Direct encapsulation - The component parts were soldered to the PC board, cleaned, encapsulated, and cured at 150°F for 24 hours.

b) Total dip - The component parts were soldered to the PC board and then the entire system was cleaned, dip coated in the polyurethane and cured at 160°F for 24 hours, encapsulated and cured at 150°F for 24 hours.

c) Custom dip - The component parts were cleaned and individually dip-coated in the polyurethane and cured at 160°F for 24 hours. The components were then soldered to the PC board, cleaned, encapsulated and cured at 150°F for 24 hours.

The test results, summarized in Table 7, show that the addition of the polyurethane precoat seriously aggravated the solder joint problem, and that precoating the parts, only, reduced the electrical performance problem to a level below that of the directly encapsulated parts, but the solder cracking problem was much worse than the directly encapsulated hardware. Sandia is continuing their testing to determine the effects of lead stress relief, spongy precoats, and other factors.

This case history illustrates the very insidious nature of embedment problems and emphasizes that the verification of the packaging by temperature cycling is the only certain method of proving out a packaging design.

Table 7 Encapsulation/Thermal Cycle Test Results

	Solder Joints Cracked	Electrical Performance Shifts
Direct Encapsulation	0.8%	1 serious abnormality 1 minor abnormality
Total Dip	43.9%	1 failure 1 serious abnormality
Custom Dip	13.8%	Slight deviations

5) A report by L. H. Fanelli (Ref 27) describes a problem with the F-111 power supply. The failure was an intermittent open circuit traced to the capacitor in a potted cordwood module. Nineteen of 24 solder joints were found cracked in a module cured at 266°F and 12 out of 24 cracked in a module cured at 165°F. Investigation determined the cracks to be caused by stresses in the solder joint which exceeded the strength of the solder. Stresses were developed by the differences in thermal expansion of the epoxy and capacitor leads upon cooling during the potting cycle and subsequent thermal cycling.

Evaluation indicated two approaches to the problem solution, lowering the elastic modulus of the potting compound and/or increasing the strength of the solder joint.

Canadian Marconi (F-111 Program), encountering the same problem, used a softer potting material consisting of a loose aluminum oxide filler in the module and retaining the previous potting compound as a containing shell only. The loose powder provided a low modulus media.

Autonetics investigated strengthening the solder joint by use of silver solders with superior stress-rupture characteristics. The best solder found for this purpose consisted of 3.5% silver, 1% cadmium, balance tin (Alpha Metals No. 38 Alloy). However, this material was not used because of anticipated manufacturing problems. Instead, the solder joints were strengthened by the easiest improvement to implement which was incorporation of large bifurcated solder posts which increased the lead-to-solder bond area by a factor of four.

6) A report by Gore and Lane (Ref 28) describes a problem of solder joint and part failures in cordwood modules during an acceptance test of five temperature cycles from -55°C to +85°C. The module was potted with a silica-filled epoxy resin. The stresses from the potting caused both electronic part and solder joint failures.

This problem was solved by: (1) kinking the part leads to permit extension and compression of the lead with a minimum of force transmitted to the joint, (2) by coating the unencapsulated assembly with DC-271 to prevent adherence of the potting compound to the leads and the parts, and (3) by the use of two-sided printed circuit boards with plated-through holes to provide stronger solder joints.

After this corrective action, 485 modules passed the five temperature cycle acceptance test with one solder joint failure, and with no evidence of damage to the electronic parts.

7) Burton S. Levin, of the General Electric Company, describes (Ref 29) the failure of an epoxy encapsulated electronic module in which a nickel ribbon moved during potting and subsequently shorted a resistor. As corrective action, an epoxy coating was applied to the module which prevented movement of the ribbon during encapsulation.

8) A report by R. R. Prudhomme (Ref 30) describes the embedment pressures within modules potted with six different materials. In the program, carbon composition resistors were mounted in an array and potted. The measurements of pressure were based on the fact that the resistance of a carbon composition resistor varies with pressure in a repeatable manner. The resistor modules were embedded using the six materials and curing procedures shown in Table 8. The modules were then subjected to six 24-hour temperature cycles from ambient to 135°C. The embedment pressures, all measured at ambient temperature, are shown in Figure 24. The pressures using Scotchcast 5090 and RTV 602 were low and were not plotted. One rather startling finding was that the pressures increased during the first two temperature cycles showing that complete curing of the potting was not achieved by using the manufacturers' recommended curing times. This was confirmed by hardness measurements. The very high pressures measured illustrates the fundamental problem with potted modules.

Table 8 Material Mixing and Curing Procedures

Material	Mixing Ratio	Cure Time & Temp
EPON 828	100 PBW Epon 828 to 100 PBW MICA to 10 PBW CAT. (DTA).	Room Temp 24 hr
Stycast 1090/9	100 PBW Resin 9 PBW CAT. No. 9 De-gassed for 10 min.	Room Temp 24 hr
Stycast 1090/11	100 PBW Resin to 12 PBW CAT. No. 11 De-gassed for 10 min.	218°F 2 hr
Stycast 2850	100 PBW Resin to 4 PBW CAT. No. 11. De-gassed for 10 min. Heated material to 165°F to lower viscosity prior to mixing, de-gassing, and pouring.	214°F 2 hr
ScotchCast 5090	7 PBW Part "A" to 3 PBW Part "B" De-gassed for 10 min.	166°F 3 hr
RTV 602	100 PBW Resin to 0.25 PBW CAT. De-gassed for 10 min.	Room Temp 36 hr

The lower pressures measured on Resistor No. 1 are attributed to the fact that this resistor was more closely surrounded by other resistors and this reduced the stress. This effect has been observed by other investigators.

Resistors No. 1 and 3 were not precoated, while Resistor No. 2 was precoated, and the benefits of the precoat are evident in Table 9.

The maximum pressures measured in the modules between 75°C and -65°C are plotted as a function of temperature in Figure 25, where it is shown that the pressures increase with a decrease in temperature further emphasizing the need of precoating to minimize stresses.

9) A report by Dr. Frank Swanson (Ref 31) describes pressure measurements within silica-filled rigid epoxy modules and the effect of RTV precoats of various thicknesses. Pressures were measured by using a thermometer bulb, which had been pressure calibrated using hydraulic pressure. The measurement was temperature-compensated. In this program, thermometer bulbs were coated with Dow Corning RTV-731 and then encapsulated in a methylene dianiline cured, 75% (by weight) silica filled rigid epoxy. The encapsulating compound was cured at 170°F, resulting in a peak

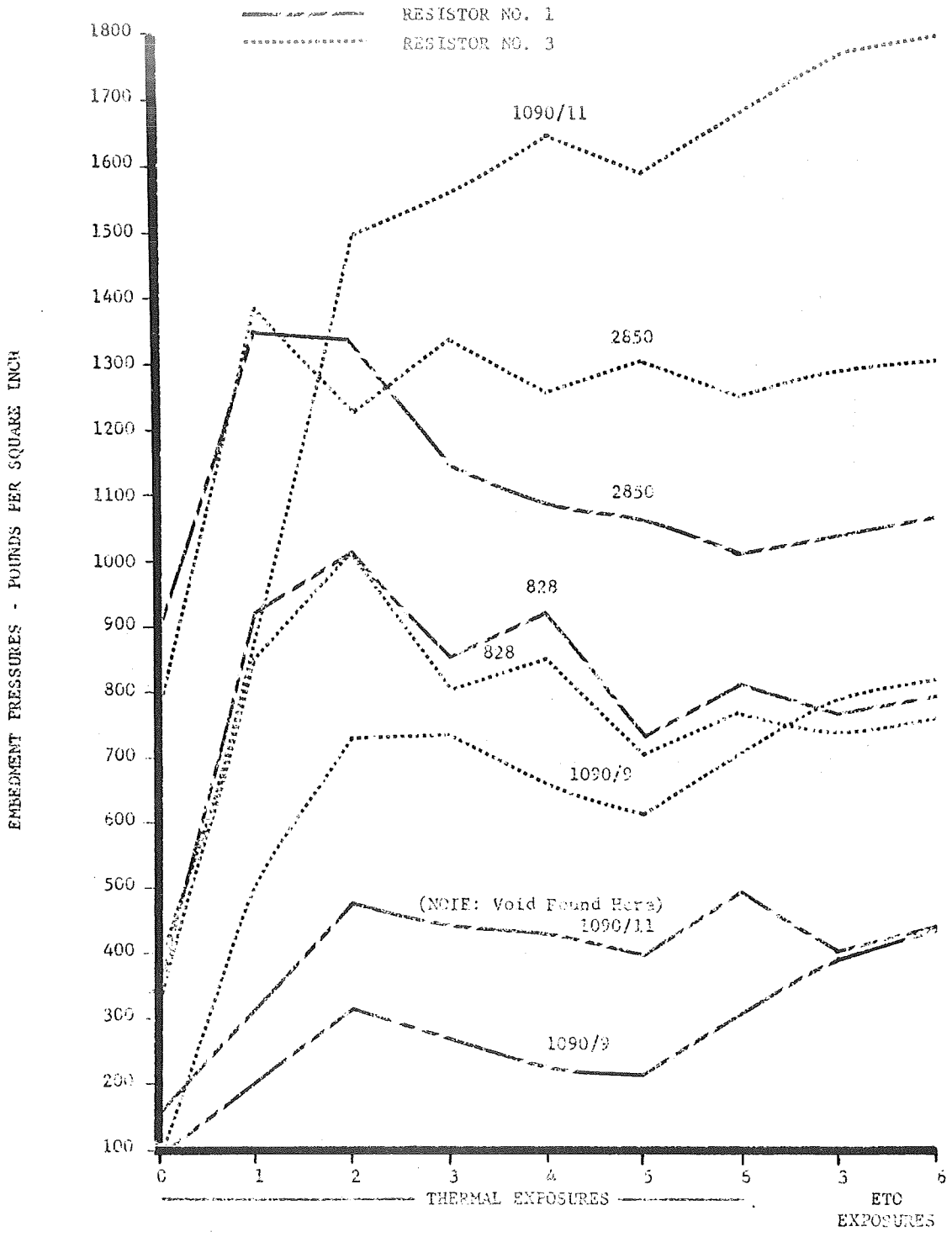


Figure 24 Effects of the Sterilization Procedure on Embedment Pressures

exotherm of approximately 200°F, which is the minimum pressure point. Pressure readings were taken at temperatures of 160, 130, 100, 70, 30, 0, and -30°F. The measured pressures are plotted in Figure 26. This data shows that the stress relief on the component is directly proportional to the coating thickness, and the conformal coating must be quite thick to significantly reduce the stress.

Table 9 Effect of Potting Material, Precoating, and Temperature Cycling on Embedment Pressure

Material	Resistor No.	After Cure	Thermal Exposures; Pressure (psi)					
			1	2	3	4	5	6
EPON 828	1	335	926	1007	855	915	731	809
	2	181	18	--	--	--	--	--
	3	310	858	1015	801	851	705	762
Stycast 1090-9	1	101	202	318	270	221	210	303
	2	53	--	168	140	154	133	211
	3	95	514	729	732	651	613	708
Stycast 1090-11	1	161	308	477	440	432	395	485
	2	92	234	290	216	206	142	184
	3	360	676	1497	1559	1648	1591	1688
Stycast 2850	1	876	1349	1138	1145	1084	1065	1011
	2	208	283	230	264	238	287	242
	3	778	1387	1230	1339	1258	1306	1250
Scotchcast 5090		Pressure data not included. Refer to body of report for explanation.						
RTV 602	1)	Negligible						
	2)	Negligible						
	3)	Negligible						

While the above data suggests that 8 or 9 mils is required to eliminate stress, Dr. Swanson reports that a thin layer is beneficial in that it has the effect of converting localized stress into a distributed hydraulic stress, and his experience has shown that for many devices a 1-mil conformal coating is sufficient to prevent the component from changing electrical characteristics. He reports that conformal coating, prior to encapsulation of a capacitor, and glass diodes eliminated device failure by converting localized stresses to distributed hydraulic stresses, not by eliminating stresses. Low modulus conformal coatings are necessary since high modulus conformal coatings transmit localized stresses.

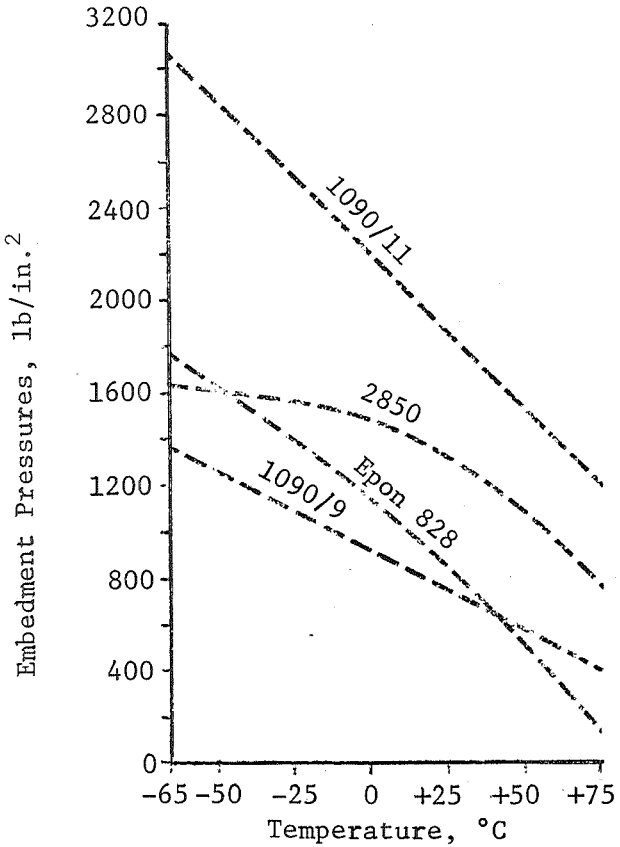


Figure 25 Low Temperature Embedment Pressures

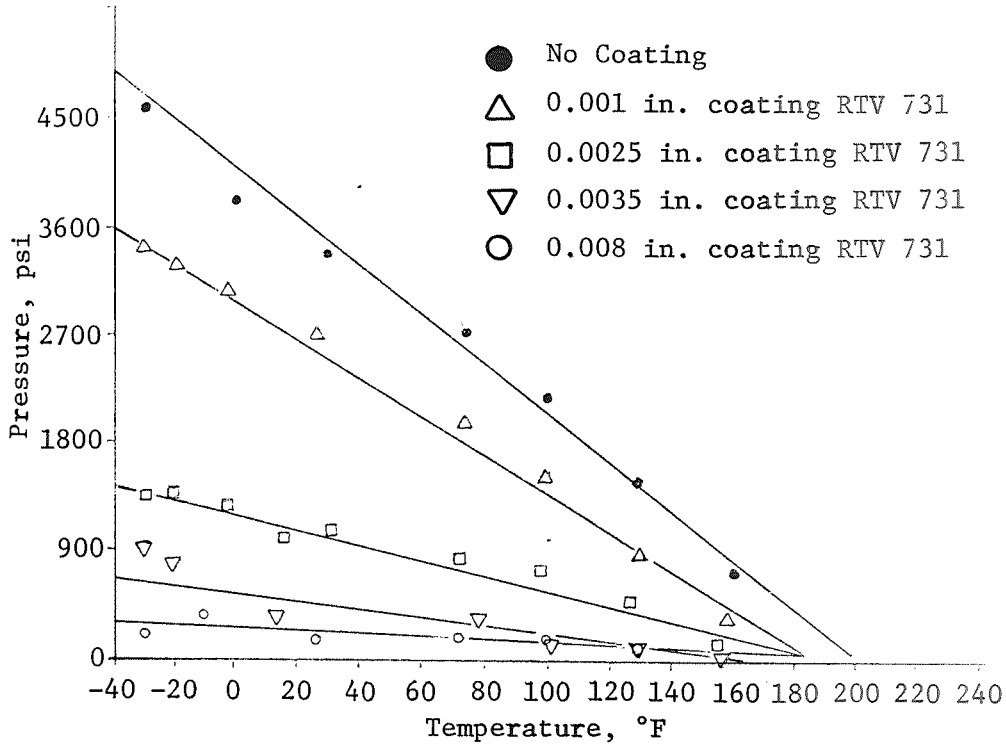


Figure 26 Pressure-Temperature Curves for Conformally Coated Thermometer Bulbs (Ref 31)

3. Summary

The thermal induced stresses imposed on parts and electrical connections as a result of the encapsulating material and process can frequently exceed thousands of pounds per square inch. Solid polyurethanes and epoxies cannot be safely used. The encapsulating material must be a low density, high modulus, material with a low coefficient of thermal expansion. In a sense, it should be a physically weak material incapable of imparting high stress to components, but rigid enough to provide the desired mechanical support. This dictates the use of materials such as microballoon-filled epoxy or low density polyurethane foams. However, even these materials can cause weld failures where the weld strengths are less than 7 or 8 pounds.

In severe temperature cycle environments it may be necessary to use polyurethane foam with a density as low as 2 pounds per cubic foot.

Low density materials are good thermal insulators and the module must be designed to conduct self-generated heat out of the module.

In encapsulated modules, welding is preferred to soldering since welded joints are not subject to the problem of fatigue cracking as are solder joints.

In evaluating and testing a candidate potting material, it must be remembered that the material will probably not be completely cured after the manufacturer's recommended cure cycle, and during subsequent temperature cycling, the material may *increase* in strength and hardness, to the detriment of the encapsulated parts.

When a module is cured, a zero stress condition exists at the curing temperature (plus the exotherm) and when the module cools to room temperature, internal stresses are generated. Accordingly, it is usually desirable to cure at the lowest practicable temperature.

Thin (0.001 inch) coatings of a resilient precoat, such as RTV 731, do not reduce the total stress on an electronic part, but aid in hydraulically distributing the stress over the part. Thick coatings (0.008 inch) appear to reduce the stress. Such coatings should be considered, and they have an added advantage of precluding electrical shorts if component leads move during the final encapsulation process.

Attempting to stress relief parts by kinking the component leads is ineffective unless resilient precoat is also applied to prevent a bond between the lead and the potting material.

To verify that the encapsulating material and process will not damage parts, electrical connections, or cause performance shifts of sensitive parts, it is mandatory that the design be subjected to temperature cycling as described in the section of this report on printed circuit board assemblies. A prime difficulty in such testing is the difficulty of removing the potting to visually inspect the electrical connections. This difficulty is largely alleviated if the recommended, very low density, materials are used since these can usually be removed by mechanical, if not chemical, means.

It is concluded that while there is existing test data showing that multilayer boards and their solder joint configurations can be designed and fabricated to withstand more than 200 severe temperature cycles, there is no corresponding proof showing that encapsulated modules have an equivalent capability. Therefore, extreme attention should be given to encapsulated modules, and all proposed designs should be thoroughly verified by temperature cycling prior to the start of production.

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