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A SLOW-SPEED MULTIPLE-CHANNEL ANALOG-TO-DIGITAL DATA LOGGING SYSTEM

T. C. Lloyd
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ABSTRACT

This work discusses an analog-to-digital data logging system. The system was developed to record from one up to a maximum of sixteen channels of analog data onto magnetic tape. Each analog channel of data can be sampled at rates of 1, 2, 6, 12, or 60 times per minute.

The system is divided into three subunits: a digital clock, an incremental magnetic tape recorder, and a sequential converter. The interfacing requirements of these subunits are presented. The majority of this report is devoted to the operation and design of the sequential converter. Its design is presented in sufficient detail to allow for the duplication or adaptation of the system using a different digital clock or magnetic recorder.

A final summary of the system's capabilities completes the work. Major system concepts and methods of improving the system's hardware design are presented, and the present application of the system is discussed.

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CHAPTER I

INTRODUCTION

1.1 The Old Data Collection and Reduction System

A major bottleneck in the experimental work of the Ionosphere Radio Laboratory is the collection and processing of satellite data. In the past, this data, existing as slowly varying voltage channels, was continuously recorded using strip chart recorders and manually reduced and logged to provide the required computer inputs. Although the electromechanical recording equipment provided adequate resolution, the mechanical reduction process, which involved scaling and logging the continuous channel records at predetermined time intervals, was extremely slow and inefficient. Since this manual method required the generation of punched cards with time references and data channel information, available manpower, money and sheer data bulk, severely limited maximum sampling rates and channel capacity. Additionally, the chart recorder required frequent maintenance and changing of paper, making the scheme impractical for recording data at remote unmanned stations.

To overcome the limitations of the present system, a flexible and reliable data logging system was required. Several basic design parameters were determined by considering present as well as future processing needs. Some of the major system design parameters are discussed in Section 1.2.

1.2 Design Requirements for a New Data Logging System

The initial system requirements decided upon were the number of input analog voltage channels and the data sampling rates. A sixteen channel input capacity was determined as adequate to provide for any foreseeable increase in data recording capability. To conserve the recording medium and to minimize computer processing time, it was deemed necessary to provide a simple method of varying the number of channels sampled. Selected data sampling rates of one sample per minute, two samples per minute, six samples per minute, twelve samples per minute, and one sample per second were required. The slower speeds would be sufficient for most data recording while the fastest rate would provide an input channel bandwidth of .5 Hertz.

To simplify the interfacing of the new system with existing systems, it was determined that the existing voltages would become the inputs to the new system. A valid input voltage range of +1.9999 volts to -1.9999 volts with a resolution of 100 microvolts was deemed adequate. In the new system, sequential sampling of the input channels and analog to digital conversion of the channel voltages would replace continuous strip chart records and manual data scaling.

Since most instruments that would provide digital data to the system use a Binary Coded Decimal (BCD) output format (Hewlett-Packard, 1972) it would be desirable to use a BCD format for all system numeric data. This implied that the analog-to-digital (A/D) conversion device would provide BCD outputs. An existing programmable digital clock (Chalasani

and Flaherty, 1967), which provided time information in a BCD format, was available for use as part of the system.

An additional obvious design requirement was the determination of the recording medium. Since all data would be reduced on an IBM 360 computer, the medium should be compatible with exiting IBM 360 facilities. Paper tape, one obvious choice, was rejected because of its decreasing use at the University of Illinois, its limited recording density, and its slow processing speed. Magnetic tape was determined to be the most desirable recording medium. This medium would allow a high recording density and it would be compatable with most computer hardware. Additionally, incremental magnetic tape recorders have the inherent mechanical simplicity and ruggedness required by a system designed for unattended operation. The selection of magnetic tape would require that the data logging system output would have to provide scan separation characters and inter-record gaps, in addition to voltage data and time information. The system would also have to provide for the inputting of manual data in the form of a tape header. This header would include information such as the date, number of channels sampled, sample rate, and any other information required by the software programs.

Since the output tape was to be compatable with an IBM-360 computer, the tape code and format were chosen to maximize the efficiency of the associated software programs. The use of an Expanded Binary Coded Decimal Information Code (EBCDIC) format, easily processed by the IBM-360 and many other computers, was decided upon. (Kennedy, 1972)

Finally, the system should also include its own power supplies so that it would operate from existing commercial power (110 volt ± 10%, 60 Hertz). The system should operate reliably over an ambient temperature range of 0°C to 50°C.

1.3 Description of the Text

A data logging system was designed and built to meet the above requirements. In the following chapters the system's operation, design and construction are discussed.

In Chapter II an overall view of the system is presented in a very simplified form. Operation of the system in its two operational modes (manual, sample) are discussed in terms of the three main system subunits: the digital clock, the sequential converter, and the magnetic tape recorder.

In Chapter III the EBCDIC code and the magnetic tape format is discussed. The EBCDIC characters that are used in the system are given in their binary level form, i.e., level inputs to the magnetic tape recorder. The blocking of data into records of a fixed length, a data compression code, and a sample of one data record is presented.

In Chapter IV system operation is discussed in detail. The sequential converter, treated as a system subunit in Chapter II, is separated into its functional circuits. The circuits are designated as to their function and they are briefly defined. System manual/sample mode formatting and sequencing operations are discussed with the aid of two block diagrams.

Chapter V is devoted to the development of the logic and its symbolic notation. The Boolian symbolic notations and the digital logic elements used in the system are defined. The schematic representations of these elements are also given.

Chapter VI is devoted to the operation and logic of the individual functional circuits. The logic requirements for the operation of the commercial subunits are described. The circuit board layouts, the schematic diagrams and the interconnection diagrams for all of the system circuits are included. These diagrams are presented in sufficient detail to enable the system to be duplicated.

Chapter VII is the concluding chapter. In it, the system's characteristics and capabilities are discussed. Tables listing the system's hardware are included; additionally, major system concepts and methods of system improvement are discussed.

The appendix presents a Fortran IV program capable of decoding and unpacking the data recorded on the magnetic tape.

CHAPTER II

BASIC SYSTEM OPERATION

This chapter presents a very basic overview of the system. Like any system, the data logging system has a set of inputs and outputs. In this system, the inputs are of three types: analog voltages, time and manually generated alpha-numeric characters. The output of the system is the IBM 360 compatible magnetic tape record of these inputs. A simplified block diagram of the system is shown in Figure 1.

Three major subunits comprise the data logging system. These subunits are the digital clock, the incremental magnetic tape recorder, and the sequential converter.

The digital clock provides the time information required by the system. Additionally, this clock contains a master clock pulse source and a sample command circuit.

The incremental magnetic tape recorder (Kennedy, 1972) generates the magnetic tape output of the system. It records the level states that exist at its inputs when commanded by externally generated write pulses. This recorder also contains circuitry to record internally generated inter-record gaps (IRG) when commanded by a pulse on its IRG input. Additionally, this recorder contains write error detection circuitry, providing a write error output pulse when a write error (failure of the tape head to write a character) occurs.

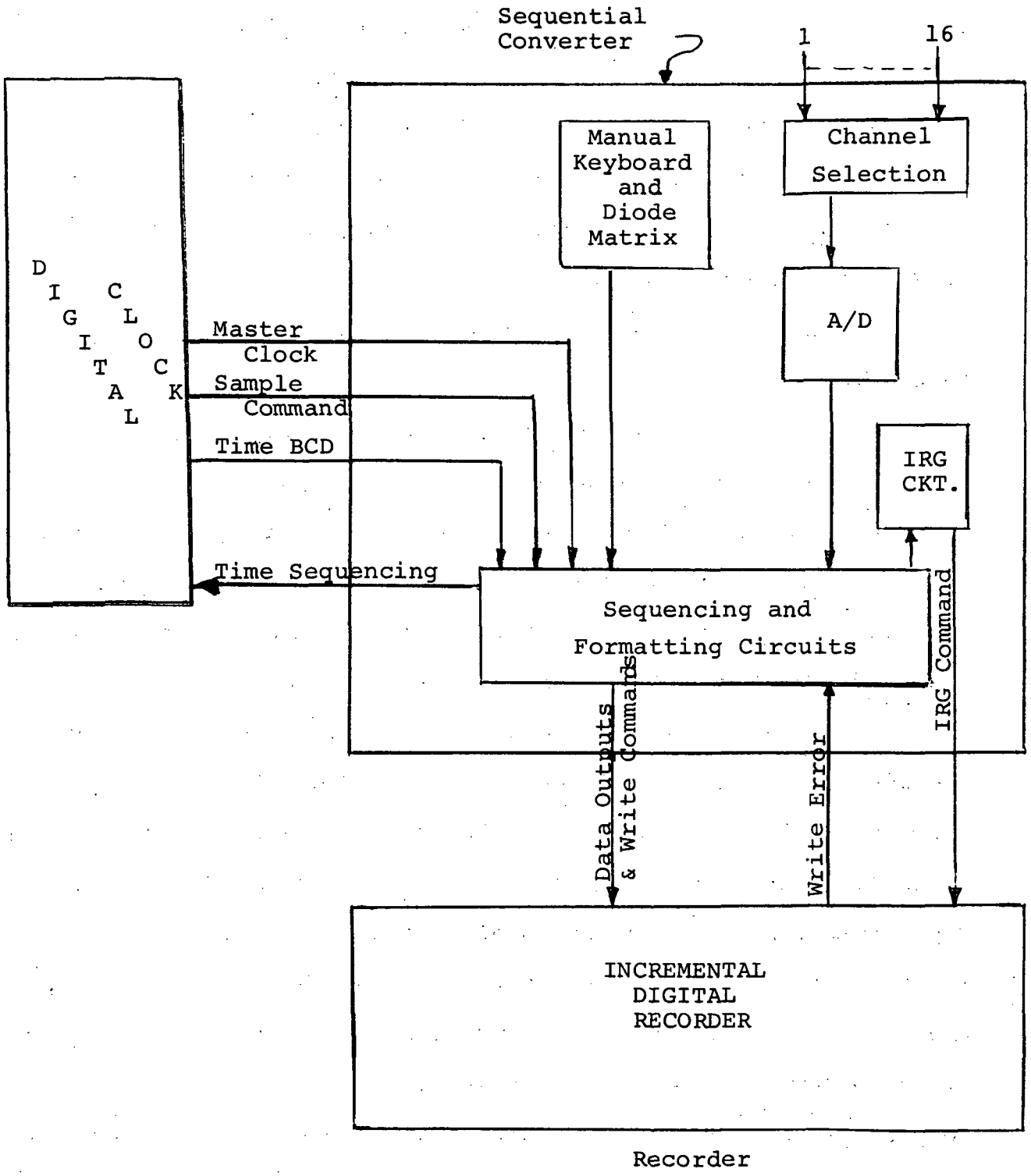


Figure 1. A Basic System Block Diagram

The third subunit in the data logging system is the sequential converter. It provides all the conversion, sequencing, and formatting operations required by the system. Digital clock inputs to this unit are the master clock pulses, sample command, and time BCD information. Other inputs are the analog channel voltages, and the write error output from the incremental magnetic tape recorder. Its outputs are the level states, write pulses, and IRG pulses required by the tape recorder.

Two modes of operation are used in the data logging system. The manual mode provides for the inputting of manually keyed characters that are used for generating the tape header. The sample mode records time information and channel voltages. The maximum recording speed is 16 characters/second in the manual mode and 166 characters/second in the sample mode.

In the manual mode the manual keyboard and matrix circuits provide digital logic information for the formatting and sequencing circuits. The formatting circuits provide the level state outputs to the tape recorder. These level states are the EBCDIC code representation of the alpha-numeric character to be recorded. In this mode, the sequencing circuits provide write pulses that are coincident with key depressions to allow the recording of these level states. In this way characters are written to provide the tape header. Since this header must include an IRG, the manual keyboard contains a key that enables the IRG circuit. Since the sample commands and the write error input are effectively disabled in the mode, no other sequencing and

formatting operations are involved.

Sample mode operation is more complicated. In this mode, manual inputs are disabled. The sample command, time information, channel voltages, and write error inputs are used. As in the manual mode, write pulses are generated coincident with the level state outputs that are to be recorded. A sample command pulse (reoccurring at selectable time intervals) initiates sequencing operations. Upon this command, scan separation characters, required by the system software, are outputted as level states from the formatting circuits. The presence or absence of a write error in the previous scan determines the scan character format (see Section 3.2). The recording of scan separation characters is followed by the recording of time information. This time information is outputted from the digital clock as serial BCD data. (Parallel to serial conversion operations in the clock are not explicitly shown in the block diagram.) This BCD data is coded by the formatting circuits and serially recorded by the tape recorder. After time is recorded, channel selection circuits sequentially connect input channels (analog voltages) to the analog-to-digital (A/D) converter. Recording stops while A/D conversion of an input channel voltage is in progress. Completion of an A/D conversion initiates other sequencing and formatting operations that provide for the serial recording of the BCD output of the A/D converter. A scan is complete and all sequencing operations end when a selected number of input channels have been sampled and recorded. The separation of the sampled data into record blocks is

accomplished by the IRG circuit. This circuit counts scans and provides an IRG pulse to the tape recorder after a predetermined number of scans. The format in which the data is recorded on the tape and the record blocking are explained in the next chapter.

CHAPTER III

MAGNETIC TAPE CHARACTER CODING AND FORMATTING

3.1 Introduction

Any data system output is useful only if the output record is in an easily processed form. In general, the magnetic tape reading equipment, computer system capabilities, and associated system software must all be considered in determining the most desirable output data format.

A serial format utilizing one byte per data character is used in the system. A serial format simplifies system software to the extent that it minimizes the required number of program changes that will be needed as the number of input data channels is varied from tape to tape. A "packed code" (two or more data characters per byte) would result in a more efficient utilization of the tape, but at the anticipated data rate this increased tape density is not needed.

3.2 EBCDIC Character Code

The most logical character code to use is one whose numeric representations most closely resemble the system's BCD information. The Expanded Binary Coded Decimal Information Code (EBCDIC) is an obvious choice (Kennedy, 1972). This code is readily accepted by most computers, including the IBM 360, with a minimum of software programming.

The EBCDIC code is an eight level (level 0 thru 7) binary code. In this system only fifteen alpha-numeric EBCDIC characters

are used. These characters and their binary level states (representing the level inputs to the incremental magnetic tape recorder) are given in Table 1.

Table 1

System Characters and Their EBCDIC Representation

Character	Levels							
	0	1	2	3	4	5	6	7
E	1	1	0	0	0	1	0	1
G	1	1	0	0	0	1	1	1
S	1	1	1	0	0	0	1	0
+	0	1	0	0	1	1	1	0
-	0	1	1	0	0	0	0	0
0	1	1	1	1	0	0	0	0
1	1	1	1	1	0	0	0	1
2	1	1	1	1	0	0	1	0
3	1	1	1	1	0	0	1	1
4	1	1	1	1	0	1	0	0
5	1	1	1	1	0	1	0	1
6	1	1	1	1	0	1	1	0
7	1	1	1	1	0	1	1	1
8	1	1	1	1	1	0	0	0
9	1	1	1	1	1	0	0	1

3.3 System Formatting of the Magnetic Tape Record

In the manual mode, all of the characters with the exception of "G" can be generated by key depression as required for use in the tape header. The actual header format is determined by computer software requirements and will not be discussed in detail. At present, the characters "E" and "S" precede all numeric manual data. An IRG is manually generated upon completion of manual data inputting.

In the sample mode the magnetic tape is blocked into records of thirty-two scans or samples. Each record is separated by an IRG generated upon completion of the thirty second scan. Each scan or sample is in turn divided into three unique parts. These parts are the scan separation characters, time information, and input channel voltage information.

Two scan separation characters are recorded at the beginning of each scan. These characters separate scans and identify the beginning of each scan. The first character recorded is either an "E" or a "G". Normally an "E" is recorded. However, if a flux error occurred during the recording of the previous scan, this first character will be a "G". The second scan separation character is always an "S".

Following these scan separation characters, time is recorded as a five digit number N_1 N_2 N_3 N_4 N_5. In this scheme, N_1 is the ten-hour digit, N_2 is the hour digit, N_3 is the ten-minute digit, N_4 is the minute digit, and N_5 is the ten-second digit.

After time is recorded, input channel voltages are sequentially recorded. Software requirements make it desirable that each of these voltages be recorded as a five digit number. However, the valid input voltage range of the system's A/D converter is +1.9999 volts to -1.9999 volts. Recording the sign character and all voltage digits in sequence would require a six digit number. Compression of the voltage data into a five digit number is accomplished by using a unique numeric code for polarity and range information. This scheme

allows any input voltage $\pm N_1\ N_2\ N_3\ N_4\ N_5$ to be recorded as "C" $N_2\ N_3\ N_4\ N_5$, where "C" is the polarity-range digit as defined in Table 2.

Table 2

The Voltage Polarity-Range Digit "C" for all Possible Input Channel Voltages

First Data Bit (C)	Input Voltage Polarity	Input Voltage Magnitude
+	Positive	< 1.0000 v.
-	Negative	< 1.0000 v.
1	Positive	> 1.0000 v. and < 2.0000 v.
3	Negative	1.0000 v. and > 2.0000 v.
5	Positive	> 2.0000 v. Invalid (exceeds A to D converter range)
7	Negative	2.0000 v. Invalid (exceeds A to D converter range)

Table 3, using hypothetical input data, illustrates the salient feature of the sample mode format. (Two input voltage channels are recorded and the sample rate is once per minute.)

In writing the software program for use with the system output tape, the programmer needs to know the number of characters (bytes) per record. This is given by the following relation

$$W = 32(7 + 5M)$$

Table 3

An Illustration of the Sample Mode Format Using Hypothetical Data

Scan No	Time	Voltage		Tape Record (EBCDIC-Code)	Write Error
		Chan #1	Chan #2		
1	1400:00	+0.1114	-0.1114	ES14000+1114-1114	No
2	1401:00	+0.1120	-0.1120	ES140100+1120-1120	Yes
3	1402:00	+0.1426	-0.1185	GS14020+1426-1185	No
4	1403:00	+0.9615	-1.1050	ES14030+961531050	No
5	1404:00	+1.0170	-1.1042	ES140401017031042	No
.					
.					
.					
.					
31	1430:00	+2.4756	- .1167	ES1430050000-1167	No
32	1431:00	+1.0176	-2.2150	ES143101017670000	No
IRG					

where M is equal to the number of channels sampled and W is the number of bytes per record.

Chapters I and II and this chapter have provided a basically non-technical description of the system. System requirements, operation, and coding and formatting have been presented in sufficient detail to allow a computer programmer to utilize the system. The following chapters describe the system's operation.

CHAPTER IV

DETAILED SYSTEM OPERATION

4.1 Introduction

The data logging system's basic characteristics have been presented in previous chapters. In this chapter the system's subunits, discussed in Chapter II, are further divided into operational units and functional circuits. These units and circuits are of three basic types:

1. Commercially obtainable units such as the digital voltmeter, the analog multiplexers and the incremental magnetic tape recorder.
2. An existing unit, the digital clock, expanded and adapted by adding additional circuitry.
3. Circuits within the sequential converter that were specifically designed and built for the data logging system.

In this chapter each of these units or circuits is treated as a system building block, performing a unique logic function.

In Section 4.2 the functional circuits in the sequential converter are given. These circuits are used in Sections 4.3 and 4.4 to explain system operation in its two operating modes (manual and sample).

4.2 Sequential Converter Circuit Designations and Their Descriptions

Physically, the sequential converter consists of several circuits and units. Below are listed their names and their brief functional descriptions. They are listed at this time to aid the reader in following the system block diagrams (see Figures 2 and 3), and to introduce the system logic design in an orderly way. Generally speaking, these circuits each provide one or more logic functions. Unless it is stated otherwise, these units were specifically designed and built for the data logging system.

DVM - The Digital Voltmeter. This commerical unit encodes input voltages, outputting them as parallel BCD data. As a function of an external logic input, the unit either "free runs", repetitively updating BCD output data, or operates in a hold mode, maintaining a constant BCD output after initial encoding of an input voltage is complete. It also provides an "end of encode" output upon the completion of encoding.

MUX #1 - MUX #2 - The Analog Multiplexers. These commercial units each contain eight MOSFET logic controllable switches that connect a particular channel input to the DVM analog voltage input.

"M=0", "M=1" - Mode Switching Circuit. This circuit provides logic outputs used to switch the system from manual mode to sample mode operation or vice versa. Since separate block diagrams are used for each mode of operation this circuit is not explicitly shown.

SW #1 - The Manual Channel Selection Switch. This switch is a seventeen position (0-16), single-pole, rotary switch. It selects the input analog channel that is monitored by the DVM in the manual mode.

SW #2 - The Number of Channels Sampled Switch. This switch is also a seventeen position (0-16), single-pole, rotary switch. It determines the number of input analog channels that are sequentially scanned and recorded when the system is in the sample mode.

Keyboard - The Manual Keyboard. This keyboard provides single-pole switch closures to ground when the system is in the manual mode. The individual keys provide for the manual recording of alpha-numeric characters.

IRG Key - The Inter-Record Gap Key. Physically located on the manual keyboard, this key generates an inter-record gap command for manual mode recording.

ERR Key - The Error Key. Also located on the Manual Keyboard, this key simulates a write error condition when the system is in the sample mode.

Diode Matrix - The Diode Matrix Board. This board converts single level outputs from the manual keyboard into the eight level EBCDIC outputs. It also outputs an enable command for the Master Sequencer.

Board #1 - The Recorder Pulse Generator. This board provides write command and IRG command pulses to the recorder.

Board #2 - The Master Sequencer. This board is the clock source for all the sequencing circuits. Each cycle of this

board consists of six unique output state combinations. Each cycle is associated with the recording of a single character.

Board #3 - The Time Sequencer. This board provides sequencing inputs for time parallel to serial conversion in the digital clock. It also controls the coding and sequencing circuits for time recording.

Board #4 - The Scan Separation Character Generator. This board initiates sample mode recording upon command of the digital clock and provides coding outputs for scan separation character generation. It also contains the end of scan flip-flop.

Board #5 - The Voltage Data Sequencer. This board provides sequencing inputs for the Voltage Data Parallel to Serial Converter. It also controls the coding and sequencing circuits for voltage data recording.

Board #6 - The EBCDIC Encoder. This board converts BCD data and other coding information into EBCDIC outputs for the recorder.

Board #7 - The BCD Coupler. This board receives serial BCD data from four sources and couples it to the EBCDIC Encoder.

Board #8 - The Voltage Data Parallel to Serial Converter. This board converts the DVM parallel BCD outputs into serial BCD outputs.

Board #9 - The Channel 1 thru 8 Selector. This board provides switching commands to the first eight analog multiplexer channels.

Board #10 - The Channel 9 thru 16 Selector. This board provides switching commands to the rest of the analog multiplexer channels. Additionally, this board provides a write error coding output.

4.3 Manual Mode Operation

A block diagram for manual mode operation is given in Figure 2. In the manual mode time is not recorded, hence, the digital clock is shown only as a 100 PPS clock source.

Sequential operation in the manual mode involves only the recording of alpha-numeric characters using the keyboard. Depression of a keyboard key outputs a ground to the Diode Matrix. This in turn, provides level outputs to Board #6 directly and via Board #7. Board #6 outputs the level states to the recorder. Upon key depression, an additional output from the Diode Matrix enables Board #2 for one cycle. An output pulse from Board #2 triggers a monostable multivibrator in Board #1 to provide the write command for the recorder.

No other sequencing operations occur in the manual mode. However, two other features, IRG pulse generation and DVM operation are included in the block diagram. The IRG key, connected to Board #1, provides an IRG command pulse for use in writing the header. The "Gap in Process" output from the recorder resets logic in Board #1. BCD outputs from the DVM are not used in the manual mode, but the visual indication can be used either to monitor any channel input or to adjust the DVM. Switch #1 causes a single true state register bit output from

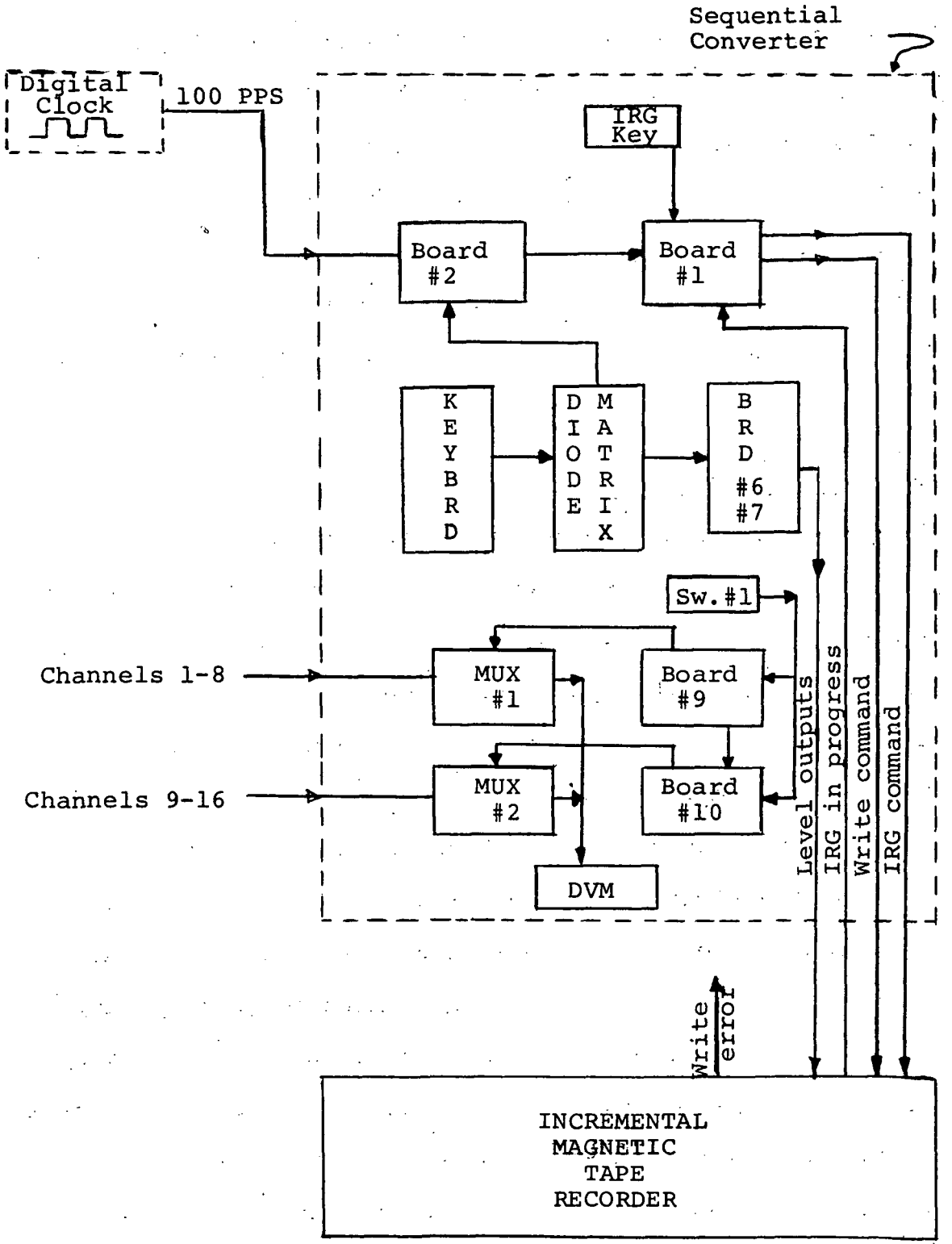


Figure 2. A Block Diagram of Manual Mode Operation

either Board #9 or #10, to close a MOSFET switch on either MUX #1 or MUX #2. Alternatively, in the 0 channel position, no MOSFET switch is closed. In the manual mode the hold input of the DVM is not enabled and the DVM "free runs".

Although write errors could occur in manual mode recording, the software program has no way of detecting an error character so the write error output of the recorder is not used in this mode.

4.4 Sample Mode Operation

A block diagram for system operation in the sample mode is given in Figure 3. The circuits added to the digital clock are not explicitly shown in this figure (only the clock's outputs and inputs to the system are shown.

The recording of data in the sample mode is initiated by a sample command pulse from the digital clock. A command pulse is outputted by the clock when its time (minutes and seconds) coincides with the rate selector setting. This command pulse triggers flip-flops on Boards #3 and #4. One flip-flop on Board #4 disables a clear input for a flip-flop on Board #9. Board #4 enables Board #2 for two cycles and outputs coding information to Board #6. If a write error indication was outputted from the recorder during the previous scan or if the Err Key was depressed during the previous scan, an output from Board #10, clocked by Board #4, provides a write error coding output to Board #7. The output is coincident with the recording of the first scan's operation character.

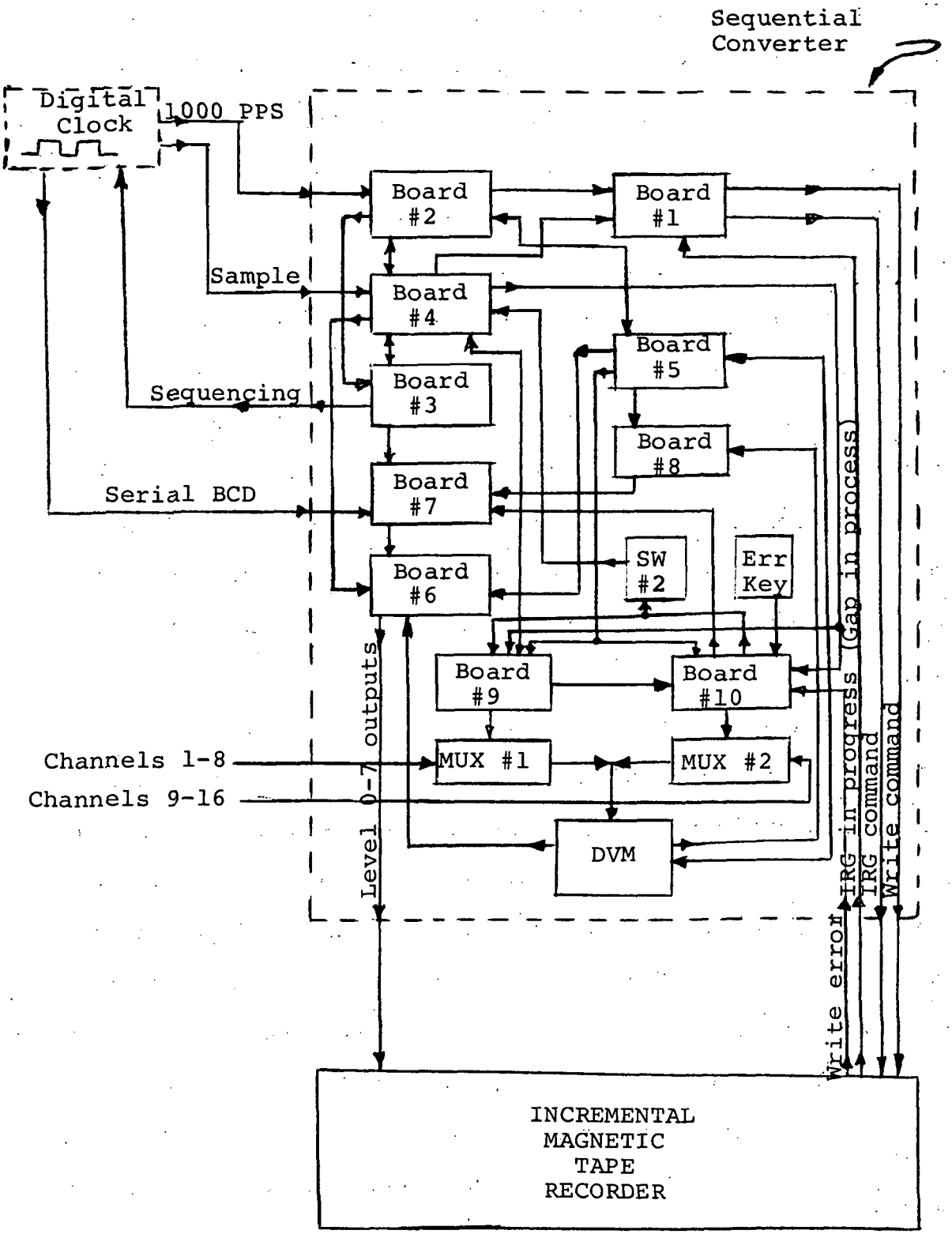


Figure 3. A Block Diagram of Sample Mode Operation

After the two scan separation characters are recorded, an output from Board #4 inputs a true state into the first bit position of the Board #3 shift register. Right-shifting of this state provides inputs for parallel to serial conversion of time BCD data. The serial BCD data is inputed to Board #7 which couples the data to Board #6. Board #3 also provides the output to Board #4 which enables Board #2 for an additional five cycles. After time is recorded, Board #5 provides a clock pulse to Board #9. This board, which now contains a true bit state in its shift register, outputs a logic command to MUX #1, connecting the voltage at channel 1 to the DVM. A flip-flop on Board #9, whose clear input was disabled by Board #4, is triggered at this time to allow the data sequencing and recording operation to begin.

The data sequencing operations are as follows: First, the DVM is released from the hold condition by an output from Board #5 and encoding of the first input channel voltage begins. When Board #5 receives an end of encode command from the DVM, the hold is reapplied (to prevent changes in the BCD outputs during recording). Outputs from Board #5 enable Board #2 for five cycles, provide coding commands to Board #6, and provide sequencing for Board #8. Range and polarity outputs from the DVM are connected to Board #6 for first data character recording. The parallel BCD data to Board #8 is serially outputed to Board #7 and then coupled to Board #6.

After all five characters of voltage data are recorded, a clock pulse from Board #5 right-shifts the true bit state in

the Board #9 shift registers. MUX #1 connects the second input channel voltage to the DVM and the sequencing operation is repeated as described in the previous paragraph. This process repeats until the preselected (SW #2) number of input channels are sampled. SW #2 provides for the ending of a scan as follows: With SW #2 in the nth channel position, an output pulse from Board #9 or Board #10 is inputed to Board #4 after n channels are recorded. This pulse clears the end of scan flip-flop on Board #4 which, in turn, clears the flip-flop on Board #9 that originally enabled data sequencing. All sample mode flip-flops are cleared and all shift registers contain only false bit states at this time. The sequential converter is idle until another scan command pulse is received.

Clock pulses for the shift registers on Boards #4, #3, and #5 have not been discussed above. These pulses are obtained from Board #2. Each board receives a single clock pulse input for each cycle of Board #2 and each board, in turn, enables Board #2 as long as it contains a true bit state in any shift register. Board #4 is electrically equivalent to a two-bit shift register. Therefore, two scan separation characters are recorded. Board #4 utilizes a five-bit shift register. Hence, five time characters are recorded. Board #5, which also utilizes a five-bit shift register, similarly causes five voltage data characters to be recorded for each voltage channel.

Only one board, Board #1, remains to be discussed. Write commands for the recorder are generated as in the manual mode. The end of scan output from SW #2 is used to trigger a

divide-by-thirty-two counting chain on Board #1. After thirty-two scans, an IRG command is generated by this board. The "Gap in Process" output from the recorder resets the counter-circuit.

This completes the operational description of the system. A detailed description of the system's individual circuits remains. Before they are discussed, a brief summary of the logic symbolism and its schematic representation is presented. This aids the reader in following the system logic design by showing the relationship between the physical components and their digital logic functions.

CHAPTER V

BOOLIAN SYMBOLISM AND DIGITAL LOGIC ELEMENTS

5.1 Introduction

The board wiring and logic diagrams in Chapter VI are essentially schematic wiring diagrams that not only provide detailed logic information but also sufficient information to allow duplication of the circuitry. For this reason, a set of digital logic element symbols must be used and they are defined in this chapter. These logic elements are broadly classified into two types, arithmetic elements and nonarithmetic elements. These elements are described by using Boolian algebraic notation, where "v", "·" and "$\overline{A}$" are used for the "or", "and", and "inverse of A" Boolian algebraic operations. The logic state of a digital logic element input or output "a" will be written as $\underline{a}$. Similarly the "true" state will be $\underline{1}$ and the "false" state, $\underline{0}$. Where no ambiguity can exist, such as in truth tables, a, 1 and 0 may replace $\underline{a}$, $\underline{1}$, $\underline{0}$.

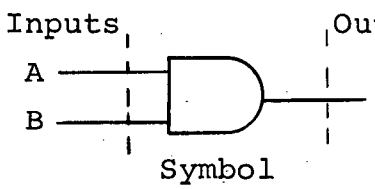
5.2 Arithmetic Elements

An arithmetic element is a digital logic element whose output state(s) at time τ are uniquely determined by its input state(s) at the same time τ (ignoring propagation delay). Six arithmetic elements are used in the sequential converter and the added digital clock logic. These six elements are the two input NAND gate, the open collector two input NAND gate, the multiple input

NAND gate, the NOR gate, the Inverter, and the open collector Inverter. Boolian algebraic functions required by the system are generated by using two or more of the above elements.

The symbols and functions for these elements are given in the following paragraphs. Gate power connections (V_{CC} and signal or logic ground) are not explicitly shown on the symbolic diagrams. The board logic schematic diagrams which are given in Chapter VI will also delete these power connections.

5.2.1 The Two Input NAND Gate

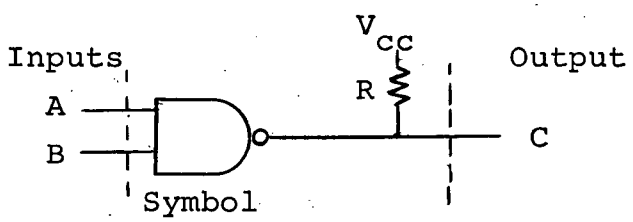


$\underline{C} = \overline{\underline{A} \cdot \underline{B}}$

Function

In many of the system's circuits the two input NAND is used as an Inverter ($\underline{C}=\overline{\underline{A}}$) by connecting the B input to $\underline{1}$ (V_{CC} or open circuit) or by connecting the A & B inputs together if the device loading considerations permit.

5.2.2 The Open Collector Two Input NAND Gate



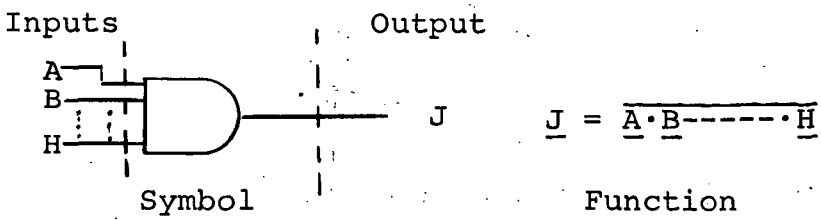
$\underline{C} = \overline{\underline{A} \cdot \underline{B}}$

Function

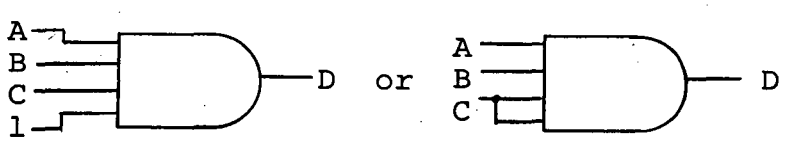
The external pull up resistor "R" (1K-2K) that is connected between the output & V_{CC} is required when open collector logic is used. This resistor is explicitly shown on all board wiring and logic diagrams.

Like the conventional NAND gate, the open collector NAND gate is sometimes used as an Inverter. "Wired output" logic, using the open collector NANDS as open collector Inverters is discussed as a part of the open collector Inverter description.

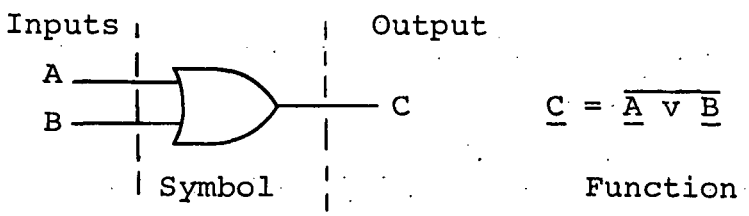
5.2.3 Multiple Input NAND Gate



In the system unused inputs (actual element inputs in excess of those required for a realization of a particular Boolian function) are connected to 1 or to other inputs as determined by wiring and device loading considerations. For example, the function $D = \overline{A \cdot B \cdot C}$ could be realized using a four input NAND by either of the following two wiring schemes.

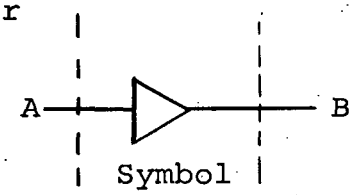


5.2.4 The Two Input NOR Gate



The two input NOR gate is sometimes used as an Inverter to generate the function $\underline{C} = \overline{\underline{A}}$. This is accomplished by connecting B to $\underline{0}$ (logic ground) or by connecting the A & B inputs together if device loading considerations permit.

5.2.5 The Inverter

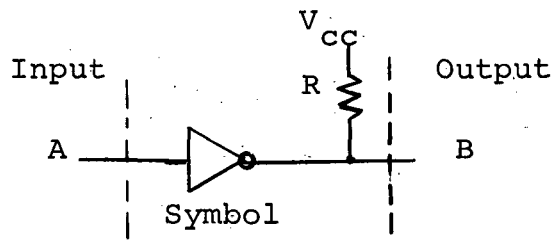


$\underline{B} = \overline{\underline{A}}$

Function

The Inverter provides the most efficient realization of the inverse operation since no additional wiring (to fixed logic levels $\underline{0}$ or $\underline{1}$ or to unused inputs) is required. However, unlike the NAND and NOR gates which can be used in combinations to derive the Boolian "and" and "or" functions, only the inverse function can be generated with the Inverter.

5.2.6 The Open Collector Inverter



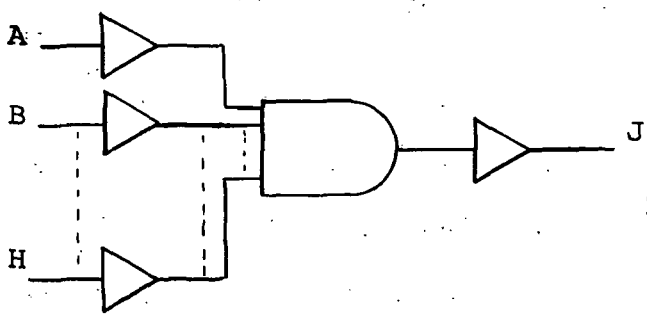
$\underline{B} = \overline{\underline{A}}$

Function

Like the open collector NAND gate, the open collector Inverter requires the use of an external pull up resistor "R" (1K-2K).

The open collector Inverter (and the open collector NAND gate wired as an Inverter) can also be used in a "wired output" configuration to simplify the realization of some functions.

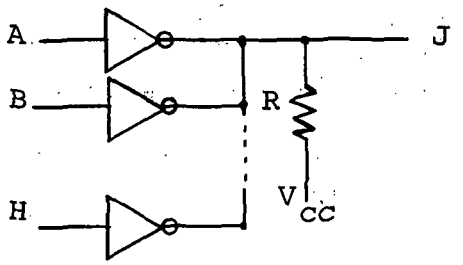
For example, the function $J = \overline{A \vee B \vee C \vee \cdots \vee H}$ is realized by the three schemes shown below.



$J = \overline{A \vee B \vee C \vee \cdots \vee H}$

SCHEME #1

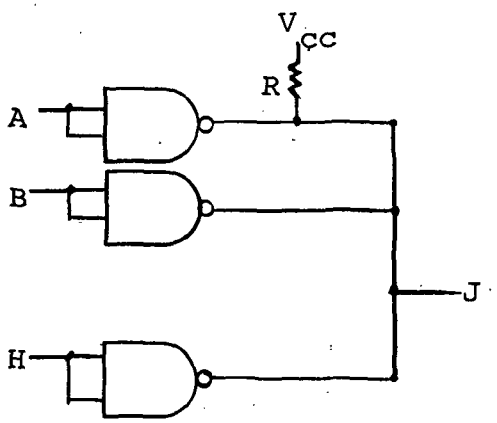
Conventional Logic Realization



$J = \overline{A \vee B \vee C \vee \cdots \vee H}$

SCHEME #2

Open Collector Inverter Realization



$J = \overline{A \vee B \vee C \vee \cdots \vee H}$

SCHEME # 3

Open Collector NAND Gate Realization

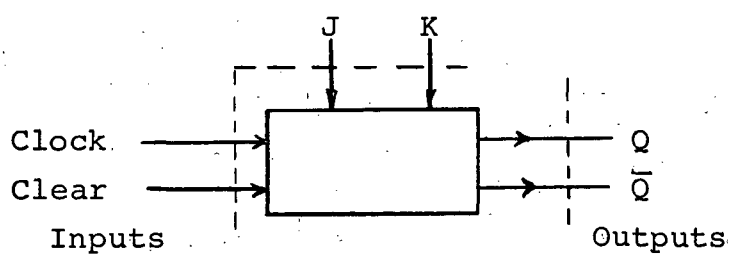
Scheme # 1, using conventional logic obviously requires a greater number of elements and more interconnect than scheme # 2 and # 3 where the "wired output configuration" is used.

5.3 Nonarithmetic Elements

A nonarithmetic element is a digital logic element that contains one or more storage devices. Its output state(s) at time τ is not uniquely determined by its input state(s) at time τ. Five nonarithmetic elements are used in the sequencing converter and added digital clock logic. These elements are the flip-flop, or binary, the shift resistor, the decade counter, the divide-by-twelve counter, and the monostable multivibrator. A brief description of these elements, their symbols and their functions follow. The symbols do not include power connections (V_{CC} & ground). Salient features of the elements that are not necessary for the understanding of the circuitry presented in Chapter VI are not included. (Signetics, 1971)

5.3.1 The J-K Flip-Flop

Only one type of flip-flop, the master slave J-K flip-flop, represented by the symbol below, is used.



SYMBOL FOR THE MASTER SLAVE J-K FLIP-FLOP

This particular flip-flop is clocked by the trailing edge (1 to 0 clock state transition) of the clock input pulse and is cleared to the Q equals 0 ($\overline{Q}$ = 1) state by clear equals 0. Since the master-slave principle is used, clocking and clearing operations are independent. For example, the flip-flop can be cleared by clear equal to 0 regardless of the simultaneous state or transition existing on the clock input.

Four unique output equations are possible with this flip-flop during any time interval when the clear input is disabled (clear is 1). The output equations are determined by the J and K input states existing prior to a trailing edge transition and they are summarized in Table 4. In this table Q_n is the output state prior to clocking and Q_{n+1} is the output state after clocking.

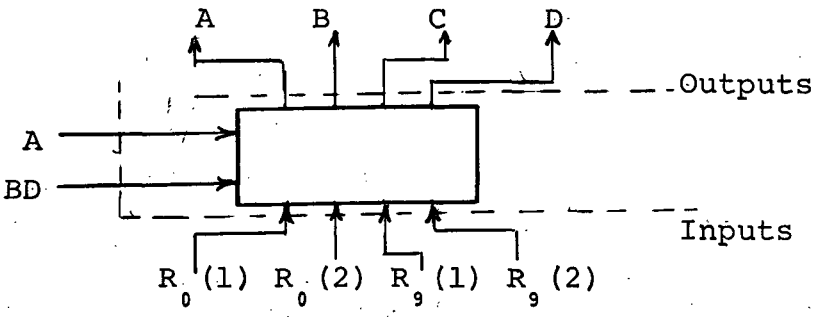
Table 4

The Truth Table for a J-K Flip-Flop

J	K	Q_n	Q_{n+1}	Output Equation
0	0	0	0	$Q_{n+1} = Q_n$
		1	1	
0	1	0	0	$Q_{n+1} = 0$
		1	0	
1	0	0	1	$Q_{n+1} = 1$
		1	1	
1	1	0	1	$Q_{n+1} = \overline{Q}_n$
		1	0	

5.3.2 The Decade Counter

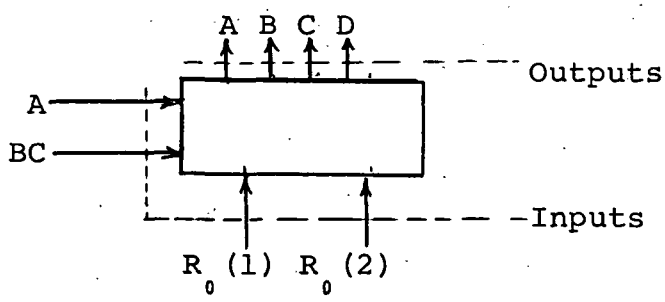
A decade counter (divide-by-10 counter) which "counts" on the trailing edge of the input clock pulse, is used in the digital clock to generate sample commands. The symbol for this device is shown below



Since the one application of this device in the data logging system involves its use as a divide-by-5 counter followed by a divide-by-2 counter, its operation will be described only in terms of this application. In the decade counter used in the system, the $R_9(1)$ and $R_9(0)$ inputs are connected to ground [$R_9(1) = 0$, $R_9(2) = 0$] and the output "D" is connected to the input "A". When $R_0(1)$ is 1 and $R_0(2)$ is 1 the counter resets all outputs to 0. Counting begins when $R_0(1)$ is 0 and $R_0(2)$ is 0. Output D provides a divide-by-5 count of the input BD pulses, and output A provides a divide-by-10 count.

5.3.3 The Divide-by-Twelve Counter

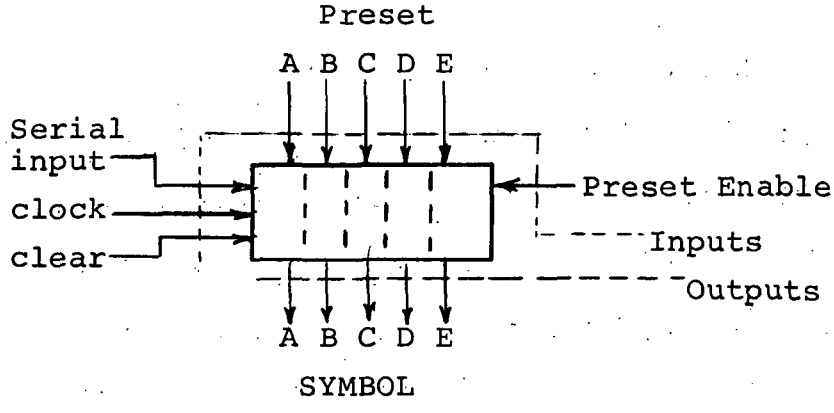
A trailing edge logic divide-by-12 counter that counts trailing edge transitions of an input pulse train is also used to generate sample commands. This counter consists of separate divide-by-6 and divide-by-2 counters that can be interconnected.



When used as a divide-by-6 counter only, (the application in the data logging system) input A and outputs A and B are not used. The input to the counter is connected to BC and the outputs C and D provide a divide-by-3 and divide-by-6 count respectively. Reset (all outputs = 0) is accomplished when $R_0(1)$ is 0 and $R_0(2)$ is 0. Counting requires that $R_0(1)$ and/or $R_0(2)$ equal 1.

5.3.4 The Five-Bit Shift Register

The five-bit shift register is the primary sequencing element in the sequencing converter. This device employs leading edge logic (shifting on the 0 to 1 transition of the input clock pulse) and its bit states may be preset independently of its clock and clear states. The following symbol will be used for this shift register.



SYMBOL

The outputs A-E represent the states of the 1st, 2nd, 3rd, 4th, and 5th bits of the shift register. When clear is 0, all bits assume logic state 0 and the clock and serial inputs have no effect. When clear is 1, right-shifting of bit states occurs on the leading edge of the input clock pulse. The serial input is used to input 0's or 1's into the first bit of the shift register.

Presetting of any bit state to 1 is accomplished by providing a 1 input to the preset enable input and the corresponding preset bit input. If clear is 0 when bit "x" is preset to 1, "x" will return to 0 when either preset enable or preset "x" becomes 0. If clear is 1, "x" will remain 1 after preset enable or preset "x" returns to 0. Further changes in "x" will be determined by the right-shifting operation of the shift register.

In actual sequencing operation the five-bit shift register is cleared and then provided with a 1 bit in the first bit position. This 1 bit is then right shifted by clock pulses. Since only a single 1 is "loaded" into the first bit position, a maximum of one bit in the shift register is 1 at any time. Completion of a particular sequencing operation occurs when all five bits return to 0.

Two possible sequencing operations, differing only in the method used to "load" a 1 into the 1st bit position, are used in the system. These operations are illustrated in Tables 5 and 6. In these tables t-n is the time before the nth leading edge of the clock pulse and t+n is the time after this leading edge.

Table 5

Serial Input "loading" of the Five-Bit Shift Register

TIME	INPUT STATE	OUTPUT STATES				
	serial input	A	B	C	D	E
t-1	0	0	0	0	0	0
t+1	1	0	0	0	0	0
t-2	1	0	0	0	0	0
t+2	1	1	0	0	0	0
t-3	0	1	0	0	0	0
t+3	0	0	1	0	0	0
t-4	0	0	1	0	0	0
t+4	0	0	0	1	0	0
t-5	0	0	0	1	0	0
t+5	0	0	0	1	0	0
t-6	0	0	0	0	1	0
t+6	0	0	0	0	0	1
t-7	0	0	0	0	0	1
t+7	0	0	0	0	0	0
t-8	0	0	0	0	0	0
t+8	0	0	0	0	0	0

Note: In this table other shift register inputs are:

Preset enable = 0, Preset A,B,C,D,E = 1 or 0,

Clear = 1

Table 6

Preset A "loading" of the Five-Bit Shift Register

TIME	INPUT STATE	OUTPUT STATES				
		A	B	C	D	E
t-1	0	0	0	0	0	0
t+1	1	1	0	0	0	0
t-2	0	1	0	0	0	0
t+2	0	0	1	0	0	0
t-3	0	0	1	0	0	0
t+3	0	0	0	1	0	0
t-4	0	0	0	1	0	0
t+4	0	0	0	0	1	0
t-5	0	0	0	0	1	0
t+5	0	0	0	0	0	1
t-6	0	0	0	0	0	1
t+6	0	0	0	0	0	0
t-7	0	0	0	0	0	0
t+7	0	0	0	0	0	0

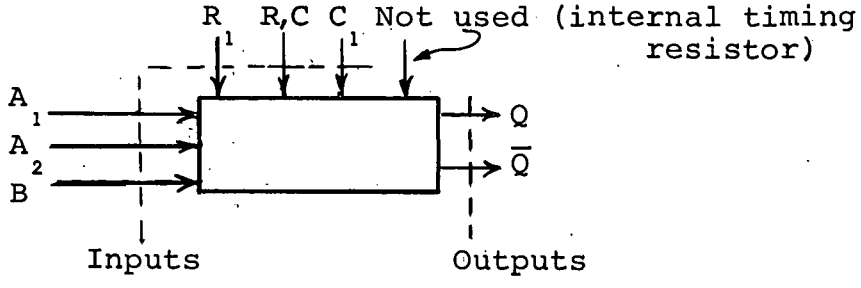
Note: In this table other shift register inputs are:
Serial input = 0, Preset enable = 1 and
Preset B,C,D,E = 0

It should be noted that the output states given in Table 6 are also the same if the preset A and the preset enable inputs are interchanged. They would also be the same if the preset A

and the preset enable inputs are simultaneously pulsed. These two variations are also used in the system.

5.3.5 The Monostable Multivibrator

The monostable multivibrator provides a single output pulse of fixed time duration upon command of trigger input. The symbol for this multivibrator is given below.



Either leading or trailing edge triggering may be used. If B is 1 and A_2 is 1, triggering will occur on the trailing edge of an input pulse connected to A_1. The pulse width is determined by an external timing resistor and capacitor. The resistor is connected between inputs R_1 and R,C and the capacitor is connected between R,C and C_1. The pulse width is defined by the approximate formula: $T = RC\ln 2$

5.4 The Selection of TTL Logic

The digital elements described in this chapter are also used in the data logging system. For these elements, the SN 7400 series of transistor-transistor logic (TTL) was chosen (Morris and Miller, 1971). This logic series is very versatile, economical, and reliable. Further, the use of TTL logic was selected to simplify present and future interface requirements. The

wide acceptance of TTL logic have made it a near standard in the electronics industry. Most of the instruments that would be used with/in the data system are available with TTL logic interfaces.

CHAPTER VI

OPERATION AND DESCRIPTION OF THE INDIVIDUAL FUNCTIONAL CIRCUITS

6.1 Introduction

The previous chapters described the interrelation of the various functional circuits in the data logging system. In this chapter, the individual functional circuits will be discussed. This will be accomplished by dividing the three system subunits into their logic functional circuits and analyzing them in detail. Section 6.2 describes the existing digital clock and specially designed circuits added to the clock. Section 6.3 describes the input/output requirements of the incremental magnetic tape recorder. The remaining section, Section 6.4, describes the sequential converter circuitry. Specifically, Section 6.4.1 and 6.4.2 describe commercially manufactured units, the digital voltmeter and the analog multiplexer. Section 6.4.3 describes the Mode Switching Circuit and Section 6.4.4 describes the Diode Matrix. Finally, Sections 6.4.5 through 6.4.14 describe the TTL circuit boards 1 through 10. These are the boards that are listed by their circuit function in Chapter 4.

Since detailed operational descriptions of commercial units are available from the manufacturers, only those characteristics that pertain to this data logging system are presented. However, detailed descriptions are given for the specially designed and constructed circuits. For each of the TTL circuit

boards in the system, three figures or diagrams are given. They are a power wiring and device layout diagram, a logic schematic diagram, and a socket wiring diagram.

The power wiring and device layout diagrams show the physical placement of the TTL integrated circuit devices on the circuit boards. They also show the power supply connections (V_{CC} and ground) to the devices. The devices, even if they contain more than one logic element, are assigned a unique number. For example, on Board #1 (see Figure 25), device number 16 is a SN 7402 (a quadruple 2-input NOR gate). On the logic schematic (see Figure 26) for this board, the four NOR gates that are included in device number 16, are shown with this number inside of the NOR gate symbol. Also the device number, 16, indicates that it is the sixth device on board number one.

The logic schematic diagrams show the complete logic wiring of circuit boards. The numbers adjacent to the logic symbols are the device input/output connections. The numbers or letters in parentheses are the board socket pin designations.

The socket wiring diagrams show all of the interconnections between the various functional circuit boards. Also included in the diagrams are power supply connections, and all discrete components that may be associated with a particular board.

6.2 The Digital Clock

The digital clock is one of the three subunits in the system. This subunit supplies clock pulses to the Master Sequencer board in the sequential converter for manual and sample

mode recording. It also supplies BCD time information and sample command pulses for sample mode recording. The digital clock contains both previously designed circuitry and newly designed circuits specially required for the system logic. To better explain the digital clock circuitry, this subunit is divided into four parts, an existing programmable digital clock, a Clock Pulse Switching Circuit, a Time Parallel to Serial Converter, and a Sample Rate Selector. These parts are individually discussed in sections 6.2.1 through 6.2.4.

6.2.1 The Existing Digital Clock

The major part of the system's digital clock subunit is a solid state programmable digital clock. This clock was originally designed to provide a visual time readout, a time marker output for strip chart recording of data, and four programmable (preset times) digital outputs. A detailed description of this clock is presented in Technical Report No. 30, Ionosphere Radio Laboratory (Chalasani and Flaherty, 1967). This clock uses TTL devices to provide time information by dividing down the frequency of a highly accurate internal 200 KHz oscillator signal. Parallel BCD outputs from decade counters are used to drive the Nixie tubes that provide the visual time readout, and NAND gates are used to provide time marker and programmable digital outputs. In the data system, the parallel BCD outputs provide time BCD information for the sequential converter and visual readout information. Time marker and programmable digital outputs remain available for use with auxillary recording devices.

The existing, or original, digital clock could have been left unmodified for use with the data logging system. However, the availability of circuit board mounting space in the clock housing and a desire to minimize the number of digital logic input/output connections to the sequential converter dictated that additional circuitry be added to this subunit. Obviously, the person who wishes to duplicate the system will not have access to the particular digital clock described here. Any commercially available digital clock providing TTL compatible parallel BCD outputs could be used with the system. In this case, square wave oscillators, added to the sequential converter, would replace the Clock Pulse Switching Circuit and associated counters that are described in section 6.2.2. The Time Parallel to Serial Converter and Sample Rate Selector, described in Sections 6.2.3 and 6.2.4 would have to be physically located within the sequential converter.

6.2.2 The Clock Pulse Switching Circuit

Two square (rectangular) wave, periodic clock pulse sources are required to provide the clock input to the Master Sequencer shift register in the sequential converter. One clock pulse source is required for each mode of operation. In the sample mode the clock pulse frequency must be less than 3 KHz. This upper frequency limit is set by the maximum writing speed of the recorder (500 characters/sec) and the number of clock pulses for each cycle of the Master Sequencer (6 clock pulses per cycle). Since writing one character requires one complete cycle of the

Master Sequencer the recorder writing rate is given by the following equation:

$$\text{Writing rate (characters/sec)} = \frac{\text{Clock Pulse frequency (Hz)}}{6}$$

In the manual mode of operation, the clock pulse frequency should be about an order of magnitude slower than above. This restriction is imposed by contact bounce, or sluggish action of the manual data keys.

Although various TTL devices could be used to generate these clock pulses, the data system circuitry is simplified by utilizing the 1000 Hz, and 100 Hz clock pulses generated by the original digital clock. Cabling and input/output interface requirements are simplified by adding a circuit to the digital clock that switches between the two clock sources as required. The output frequency of the Clock Pulse Switching Circuit is determined by the control input "M=0" whose state is a function of the sequential converter's mode of operation. This switching circuit, consisting of one quad 2-input NAND gate (SN 7400) added to an existing digital clock counter board is shown in Figure 4.

In the sample mode "M=0" is 1 and the input A, wired directly to a 1 KHz decade counter output, is inverted by NAND gate 1A. The output state of NAND gate 1B is 1 in this mode. NAND gate 1D performs a second inversion so that CP is A. In the manual mode "M=0" is 0 and the input B, wired directly to a 100 Hz decade counter output, is inverted by NAND gate 1B. The output state of NAND gate 1A is 1 in this mode. As in the sample mode, 1D functions as an inverter so that CP is B.

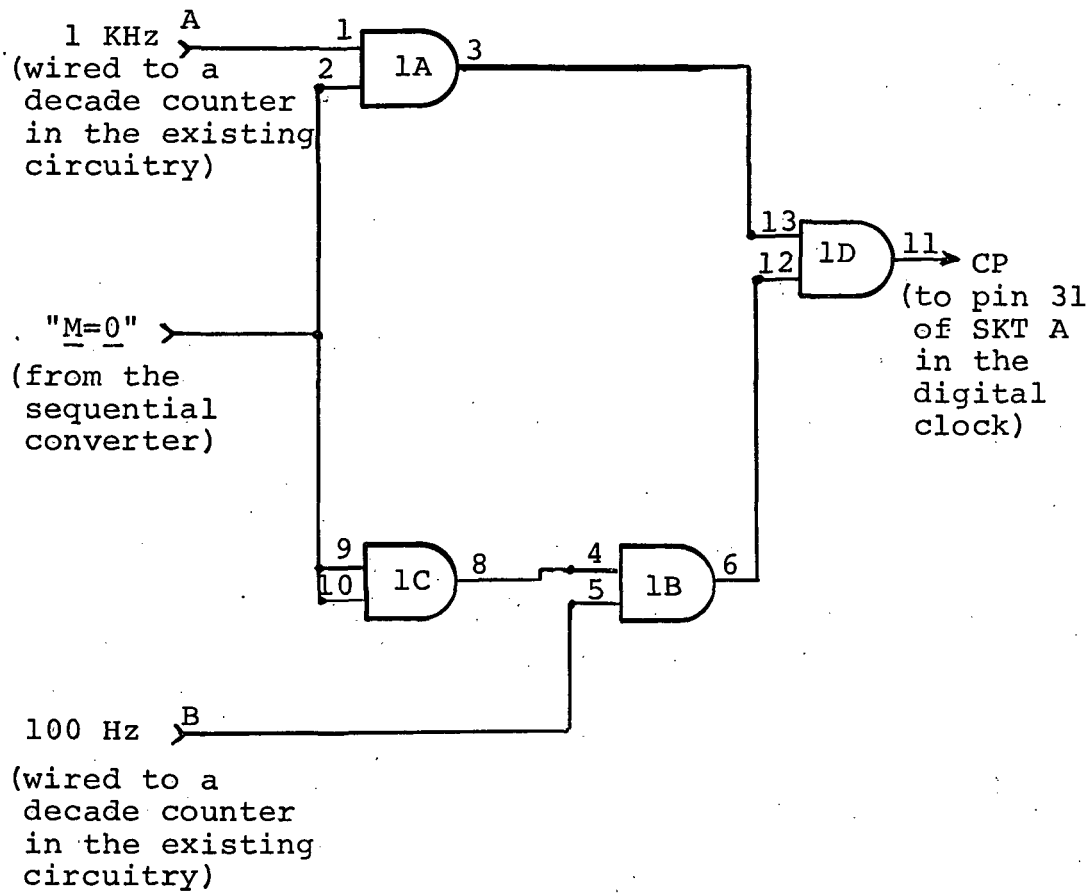


Figure 4. The Clock Pulse Switching Circuit

CP is not connected directly to the digital clock-sequential converter cable. Rather, CP is connected to the inputs of a two input NAND gate on the Time Parallel to Serial Converter discussed in Section 6.2.4. The output of this NAND gate ($\overline{CP}$) is then connected to the cable.

6.2.3 Time Parallel to Serial Converter

Decade counter outputs in the original digital clock provide parallel BCD time information. Since time is recorded as a five digit number using the serial format outline in Chapter III, a parallel to serial conversion operation is required. This operation could be performed within the sequential converter by outputting the BCD 1, 2, 4 and 8 states of each digit to be recorded. A total of twenty outputs from the digital clock would be required. Performing parallel to serial conversion within the digital clock by utilizing an added circuit board requires only four outputs and five inputs. The Time Parallel to Serial Converter also contains circuitry to invert the clock pulse output from the Clock Pulse Switching Circuit and to generate a one minute re-synchronizing pulse for the Sample Rate Selector discussed in Section 6.2.5.

Each of these functions is individually discussed in the remainder of this section. Figures 5, 6, and 7 show the power wiring and device layout, logic schematic, and socket wiring of this circuit board.

Time parallel to serial conversion is the simultaneous outputting of BCD1, 2, 4 and 8 level states for the particular

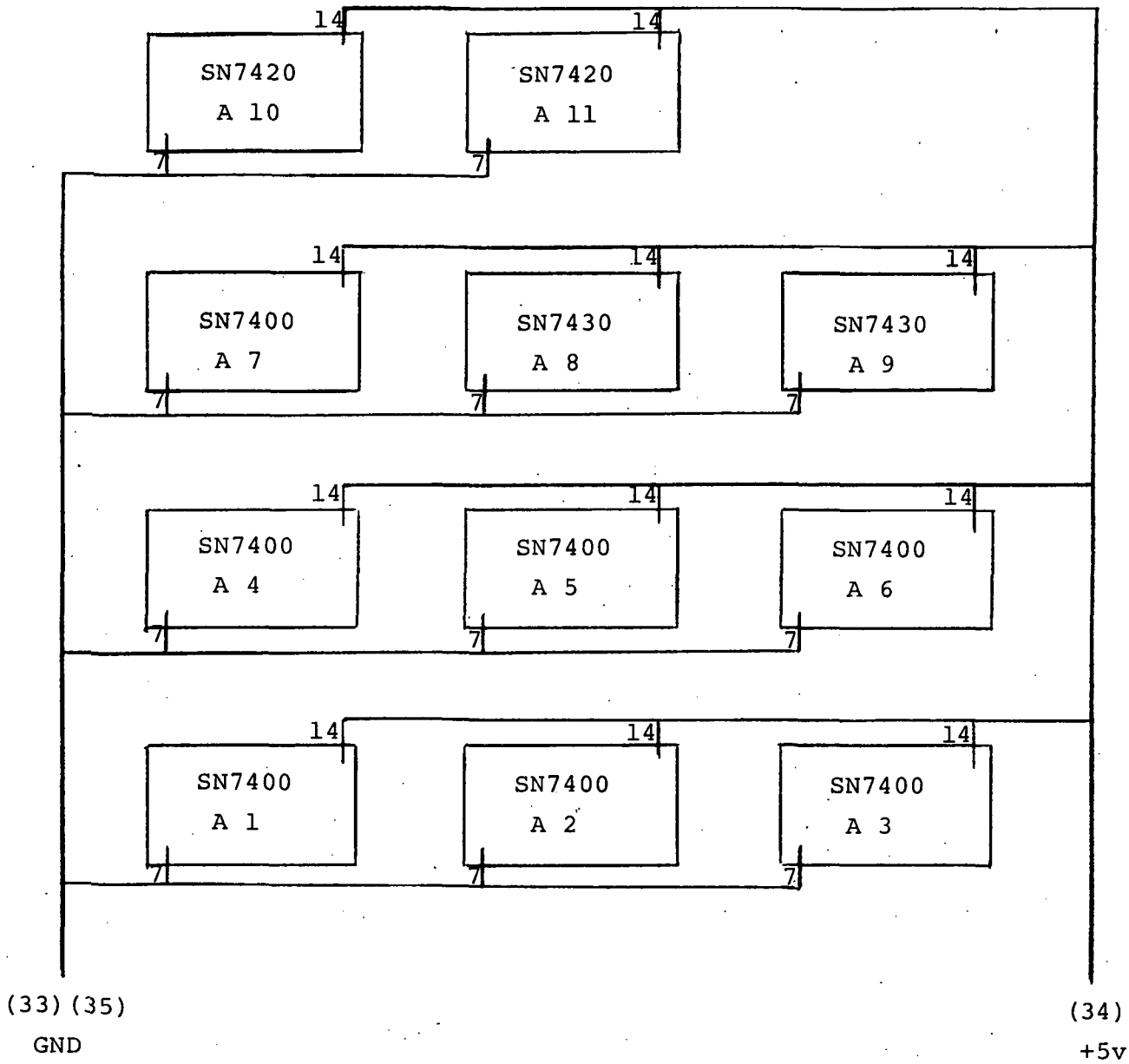


Figure 5. The Time Parallel to Serial Converter - Power Wiring and Device Location Diagram

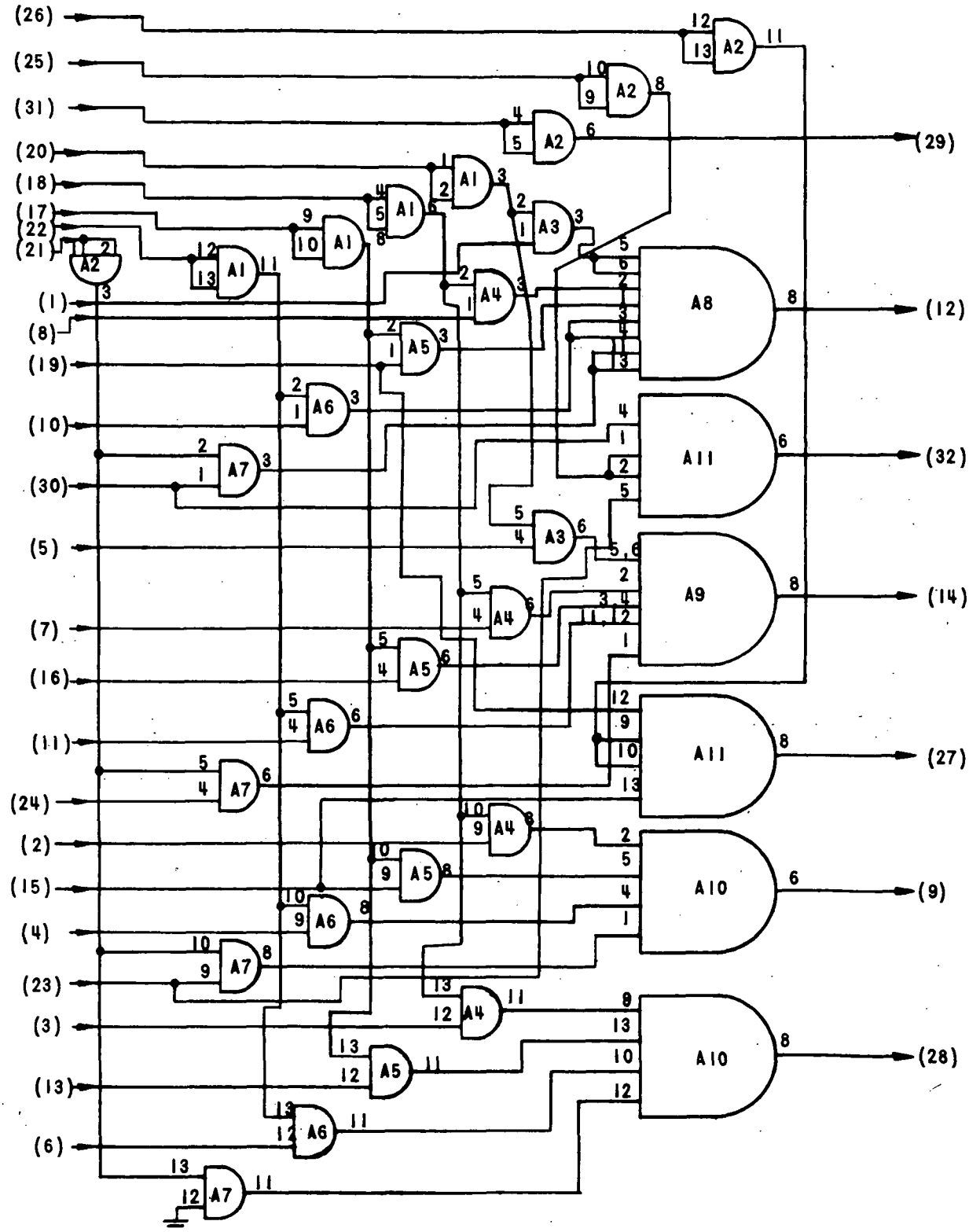
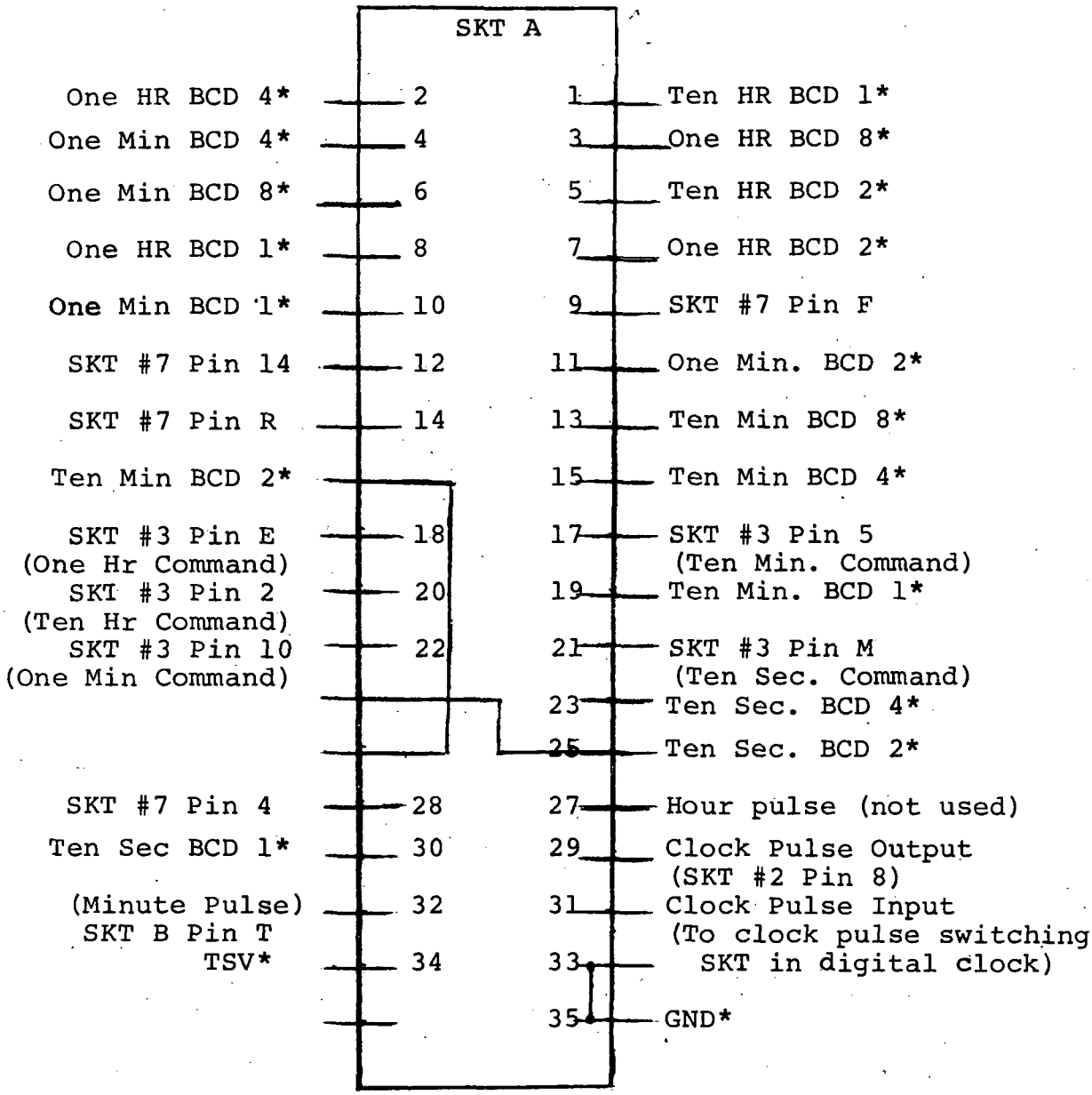


Figure 6. The Time Parallel to Serial Converter Logic Schematic



*To existing digital clock logic (explicit pin connections not shown).

Figure 7. Connections to the Time Parallel to Serial Converter

time digit to be recorded. These simultaneous outputs (for a particular digit) are provided serially so that the first time digit recorded is the ten hour digit and the last is the ten second digit. The operation of the conversion circuitry is easily understood by referring to Figure 8. This figure is a partial schematic showing only the circuitry for one BCD level (BCD1). In this figure, pins (20), (18), (17), (22), and (21) are connected to the ten hour, hour, ten minute, minute, and ten second time commands from the sequential converter. On the circuit board, these inputs are connected to 2-input NAND gates wired as Inverters. Pins (1), (8), (19), (10), and (30) are connected to the BCD1 outputs of each of the time output decade counters. That is, the ten hour BCD1 output is connected to pin (1), the hours BCD1 output is connected to pin (18), and so forth for the other counters. Pin (12), providing the serial BCD1 output to the sequential converters is the output of an 8-input NAND gate, wired as an equivalent 5-input NAND gate. The five inputs are labeled A, B, D, D, and E on the figure. Hence, (12) is $\overline{A \cdot B \cdot C \cdot D \cdot E}$.

When the first time digit (ten hour digit) is to be recorded, the ten hour time command input, (20), is 0 and all other [(18), (17), (22) and (21)] inputs are 1. The output of NAND gate A3, A, is $\overline{\text{ten hour BCD1} \cdot 1}$ or $\overline{\text{ten hour BCD1}}$. Gates A4, A5, A6, and A7 each have an input whose state is 0. Therefore, B, C, D, and E are 1, regardless of the states of the other inputs to A4, A5, A6, and A7. The output of NAND gate A8 is $\overline{A \cdot 1 \cdot 1 \cdot 1 \cdot 1}$ or $\overline{A}$. Therefore, (12) is $\overline{\overline{\text{ten hour BCD1}}}$ or ten hour BCD1.

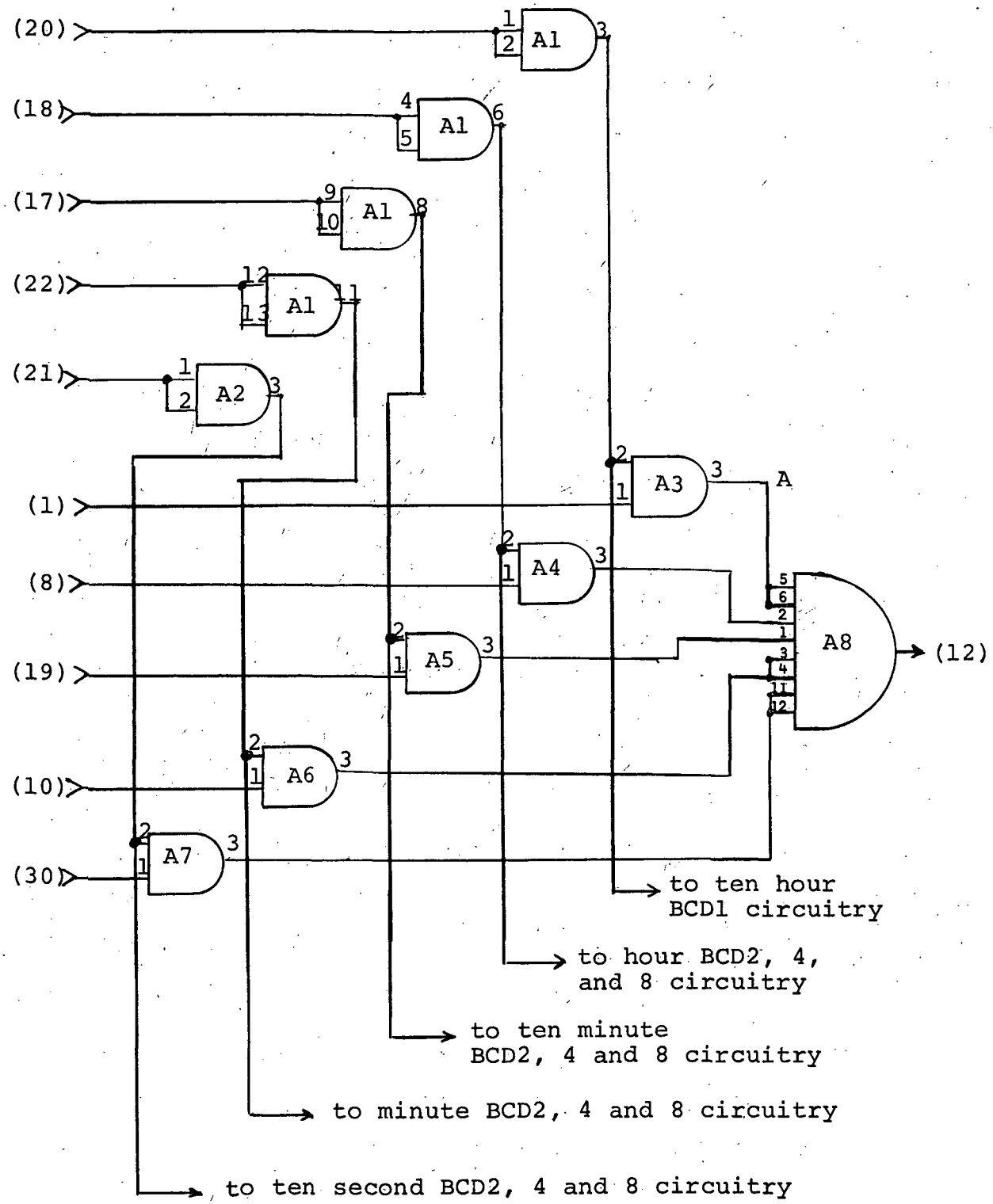


Figure 8. Simplified Time Parallel to Serial Converter Logic Schematic

When the second time digit (hour digit) is to be recorded, the hour time command input, (18), is 0 and all other time command inputs are 1. Similar equations result, specifically, B = $\overline{\text{hour BCD1}}$ and (12) = $\overline{1 \cdot B \cdot 1 \cdot 1 \cdot 1}$ = hour BCD1. Parallel to serial conversion of subsequent digits occurs in the same manner. As each digit is to be recorded, its corresponding time command input is 0 and all other time command inputs are 1. When no time digit is to be recorded, all time command inputs are 1 and (12) is 0.

Comparing Figure 6 to Figure 8, the similarity of BCD2, 4 and 8 circuitry to the BCD1 circuitry is apparent. The same time commands are used for all the BCD levels. Therefore, while BCD1 is being converted, BCD2, 4 and 8 conversions are also being performed. [BCD2, 4 and 8 outputs appear in Figure 6 on pins (14), (9), and (28) respectively.] The two 4-input NAND gates, A10, are sufficient for BCD4 and 8 outputs because in some decade counters BCD4 and 8 outputs are always 0. Not providing circuitry or inputs for these fixed state BCD levels allows the inclusion of the reamining two circuit functions on this circuit board. These two circuit functions, clock pulse inversion, and the generation of a one minute re-synchronizing pulse, are discussed in the following paragraphs.

A single 2-input NAND gate, A2, is used for the clock pulse inverting function. In Figure 6 input (31) is connected to the Clock Pulse Switching Circuit. This gate provides an inverse clock pulse output on (29) for the sequential converter.

The remaining NAND gates (A1, A2) in Figure 6 provide the one pulse per minute and one pulse per hour outputs. Since the

present data logging system format requires time recording every scan, not every hour, the one pulse per hour output (27) is not used. The one pulse per minute output (32) provides the re-synchronizing pulse required by the Sample Rate Selector. The output state of All, (32), is 1 except when the BCD outputs of the ten second counter are BCD1 is 1, BCD2 is 0, and BCD4 is 1 (10 second digit = 5). The 0 to 1 transition of this output, coincident with the ten second and second digits of time becoming zero, synchronizes the Sample Rate Selector. This will be explained in Section 6.2.4. It is important to note that this pulse is not affected either by the reset time of the existing digital clock counters or the brief digit six condition that exists in the ten second decade counter as time changes from 59 to 00 seconds.

6.2.4 Sample Rate Selector

The second logic board added to the existing digital clock is the Sample Rate Selector. This circuit generates the sample command pulses required by the sequential converter for sample mode recording. Scan rates of 1 scan/sec, 1 scan/5 sec., 1 scan/10 sec., 1 scan/30 sec., and 1 scan/minute are provided. The diagrams pertaining to this circuit are shown in Figures 9, 10 and 11.

This board uses the 1 PPS pulses generated by the existing digital clock circuitry and sequentially divides it by 5, then by 2, then by 3 and finally by 2. Output rate selection is accomplished by a 5 position rotary switch which cases the

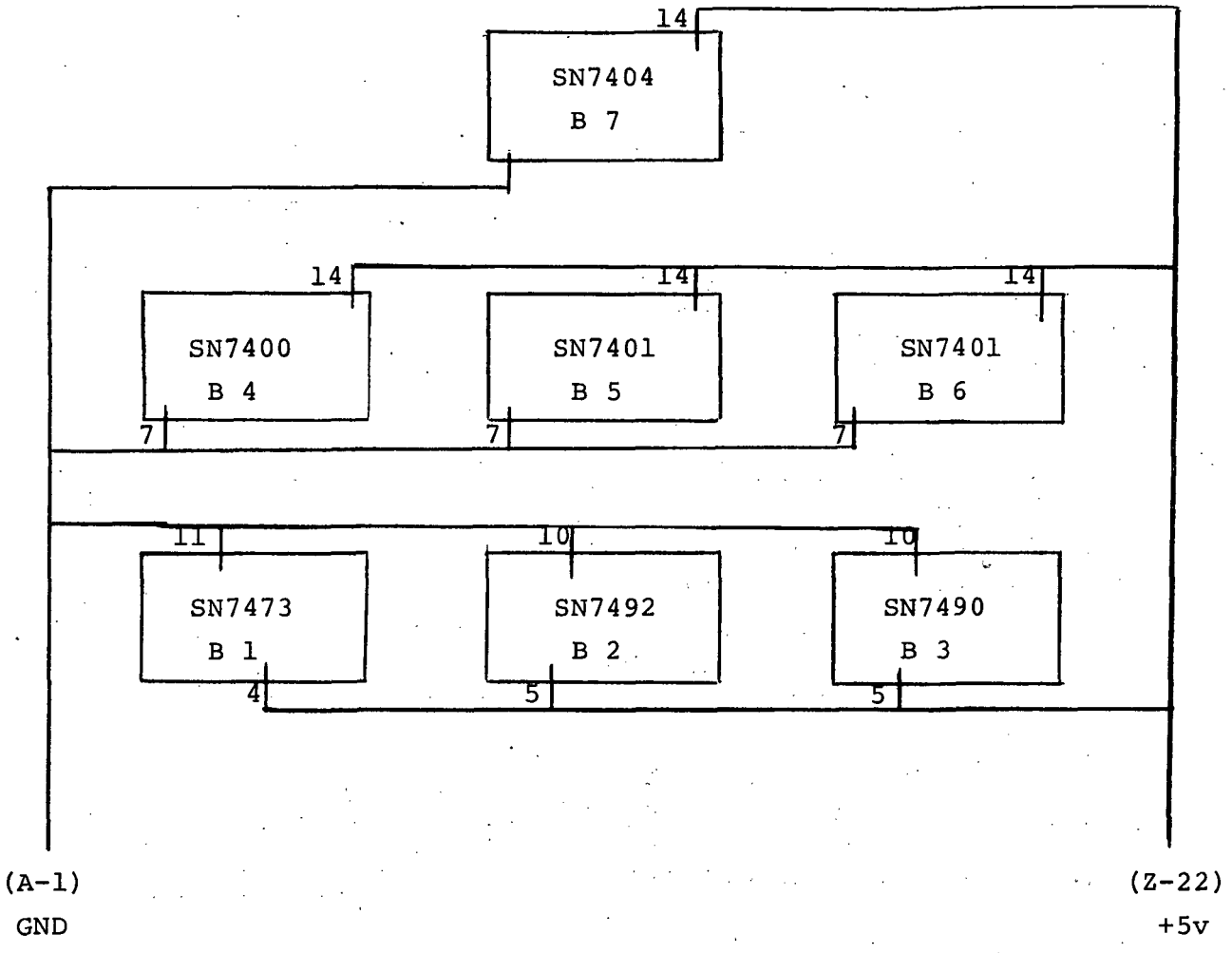
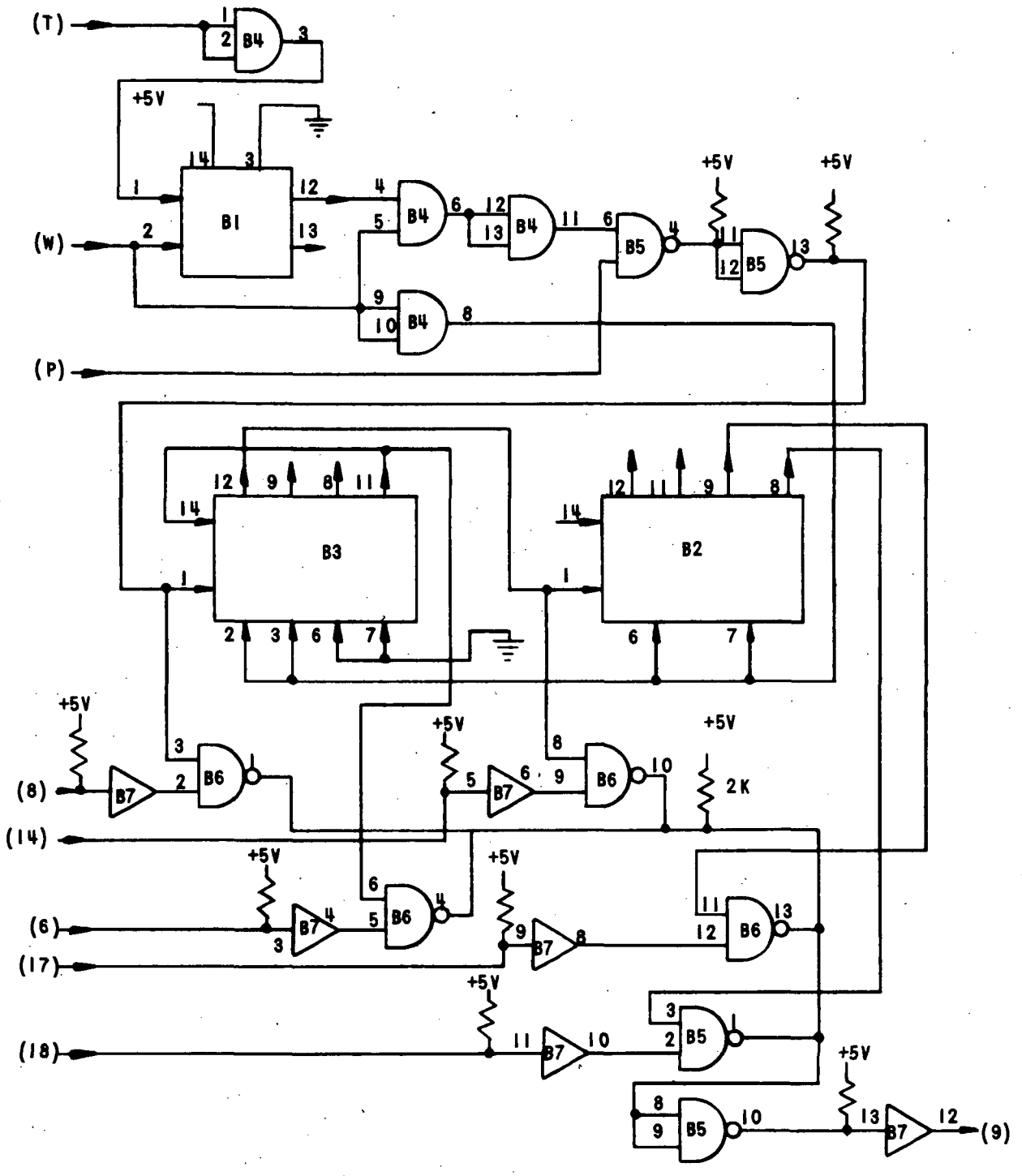


Figure 9. Sample Rate Selector - Power Wiring and Device Location Diagram



ALL DISCRETE RESISTORS IK UNLESS OTHERWISE NOTED

Figure 10. Sample Rate Selector Logic Schematic

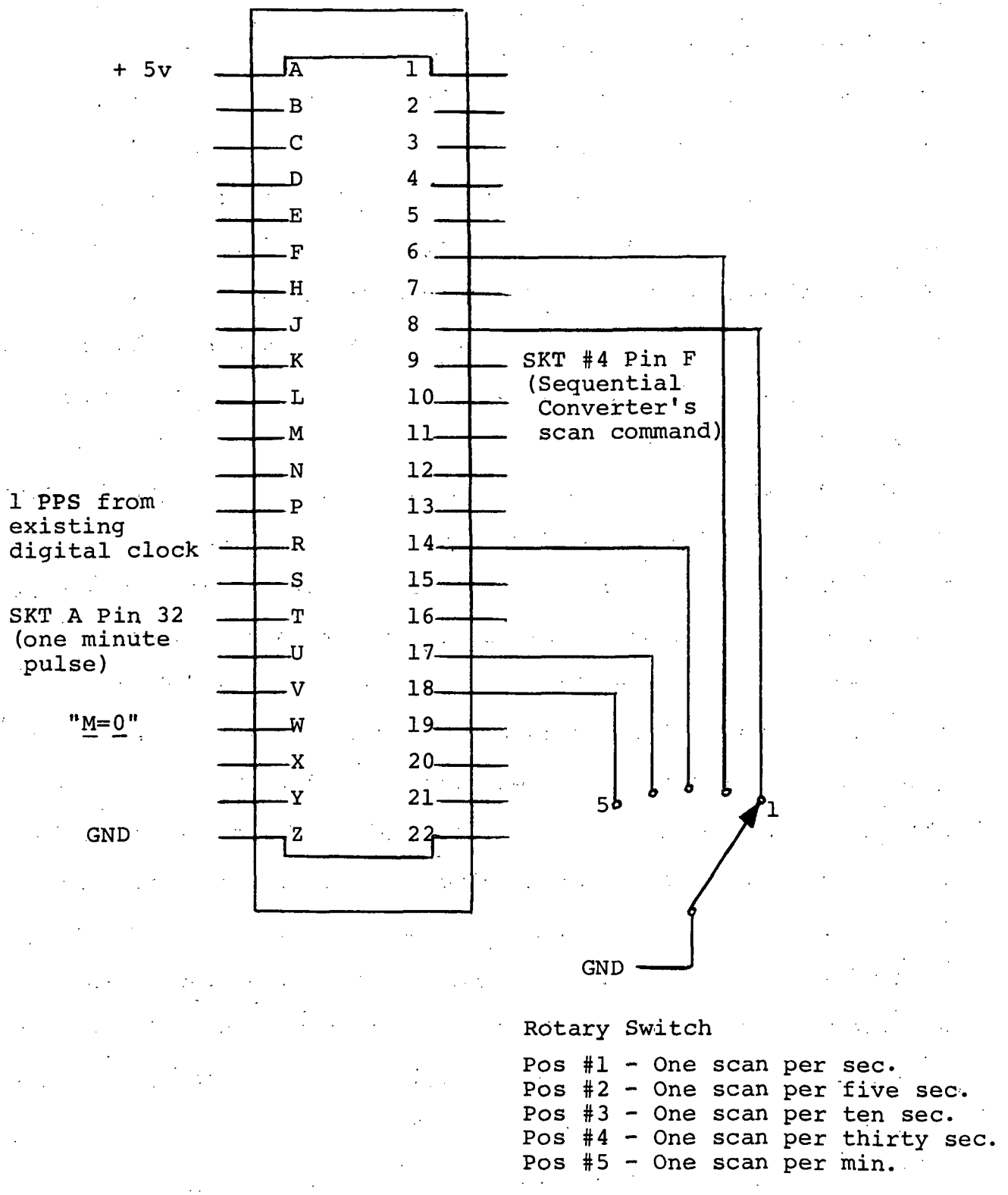


Figure 11. Connections to the Sample Rate Selector

desired rate enable input pins (8), (6), (14), (17) or (18) in Figure 10 to be in the 0 state. Note that wired output logic using open collector elements is used for rate selection.

The "M = 0" input, (W), and the one minute pulse input, (T), are used to synchronize the counters to the real time output of the digital clock. When "M = 0" is 0 (the system is in the manual mode), all counters are cleared by the J-K flip-flop (B1) circuitry. When "M = 0" becomes 1 (the system is in the sample mode), this J-K flip-flop continues to disable all counting until the first 0 to 1 transition of input (T) occurs. Since this transition occurs when the existing digital clock ten second counter and one second counter outputs correspond to BCD 0, the sample command pulse output (9), is synchronized to the real time output of the digital clock. Re-synchronization occurs whenever the system is returned to the sample mode from the manual mode.

Technically, re-synchronization would be required only after the digital clock is manually reset. However, the scheme described here provides a known start time for sample data recording. The first scan recorded by the system will be recorded at a real time that is one scan interval after the minute transition of the digital clock. For example, assume the digital clock time is ABCD.xy, and xy are any combination of digits other than 00. If the mode switch is placed in the sample position at this time and the sample rate is one sample every 5 seconds, the time of the first scan will be ABC(D+1).05.

6.3 Incremental Magnetic Tape Recorder

The incremental magnetic tape recorder is the second system subunit. This recorder is a Kennedy Model 1600/360. It is a nine track IBM 360 compatible recorder provided with a TTL compatible interface and write error checking circuitry. The recorder packing density is 800 bits per inch, and its maximum write rate (recording speed) is 500 characters per second. Since the detailed circuitry and the operational description of the recorder is available from the manufacturer (Kennedy, 1972), only those inputs and outputs that are used in the data logging system will be discussed here.

The required inputs for the recorder are of two types, level inputs and command pulses. Nine level inputs, whose states are expressed in binary form as a zero or one, are required for the recording of each character. Eight of these levels (level 0 thru 7) are provided by the sequential converter. (These levels correspond to the EBCDIC character code mentioned in Section 3.2.) The ninth level, level P, is the parity level. This level is generated by circuitry within the recorder, and its state is determined by the states of the other eight level inputs. The two command pulse inputs are the write command and the IRG command. These command pulses must have a one state time duration of greater than 10 microseconds but less than 100 microseconds (40 microseconds is used). The write command is required to enable the writing of each character on the tape. While this command is in the one state, the eight level input states must remain constant. The IRG command is required by

the tape recorder to insert the correct gap (IBM-360 compatible) on the magnetic tape.

Only two of the recorder outputs are used. They are the gap in process and write error outputs. Both of these outputs have a normal state of 0. When a IRG is being written, the gap in process output becomes 1. This output is used to reset the IRG command circuitry in the sequential converter. When the recorder senses that a write error occurred, the write error output becomes 1. This output is used in the sequential converter to flag the next data scan indicating that the previous scan was in error (see Section 3.3).

6.4 The Sequential Converter

The sequential converter is the third, and final, system subunit. Since this subunit was totally designed and constructed for use with the data logging system its physical layout is presented here.

The converter is built in a 12 inch high by 17 inch wide by 14 inch deep aluminum housing with a 12 1/2 x 19 inch front panel. The front panel of the unit (see Figure 12) is used for mounting power and mode switches and indicators, the Digital Voltmeter and associated adjusting potentiometers, and the Manual Keyboard. The rear of the housing (see Figure 13) is used for mounting the Manual Channel Selection and Number of Channels Sampled Switches, BNC connectors for voltage inputs, "Blue Ribbon" connectors for cabling to the digital clock and the incremental magnetic tape recorder, and power line fusing.

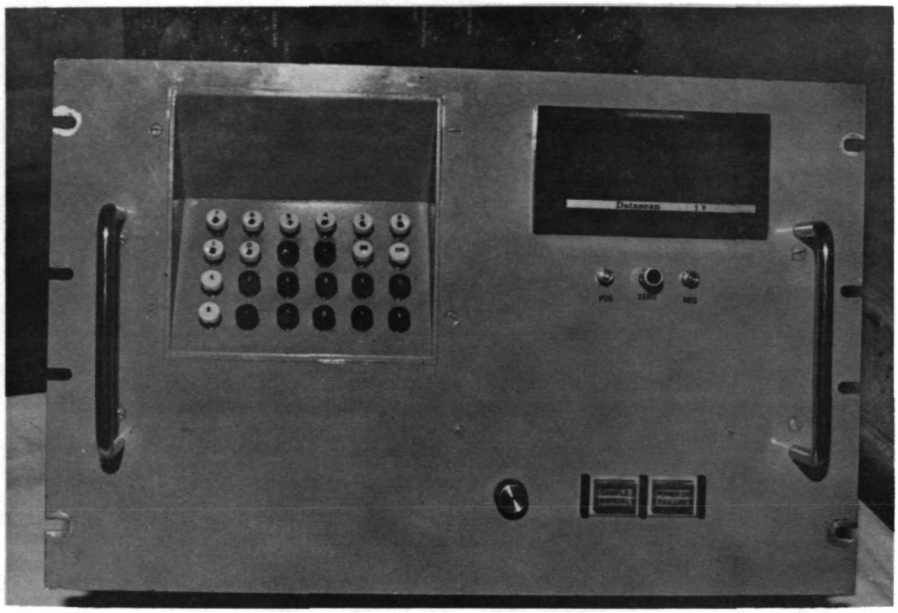


Figure 12. Front View of the Sequential Converter

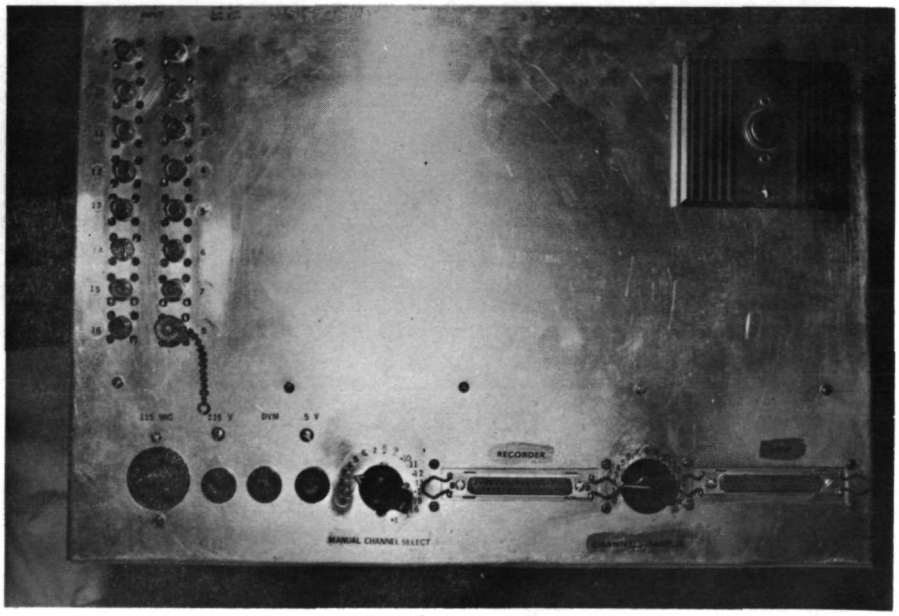


Figure 13. Rear View of the Sequential Converter

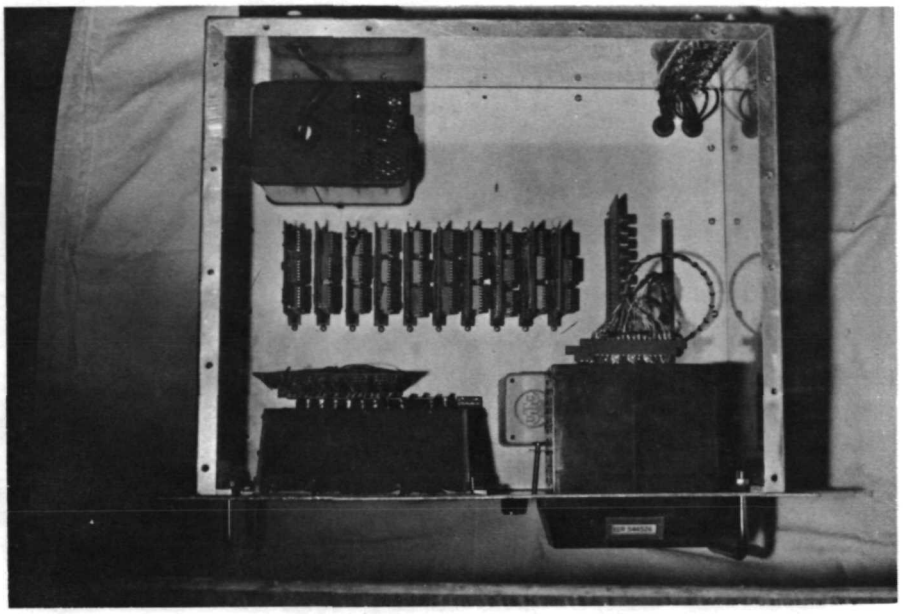


Figure 14. Top View of the Sequential Converter

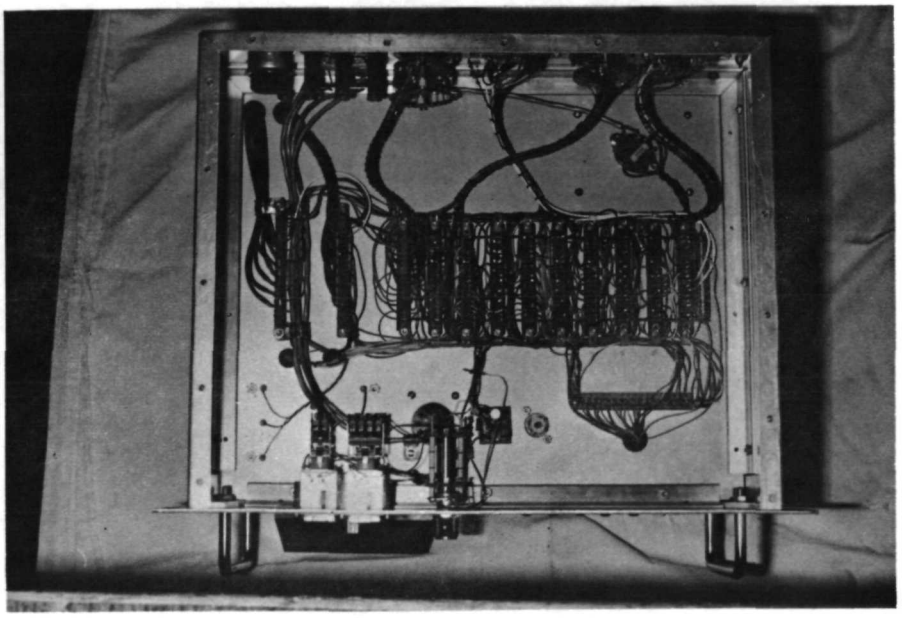


Figure 15. Underside View of the Sequential Converter

A solid horizontally mounted aluminum plate (see Figure 14) within the sequential converter housing provides mounting for the 5 volt logic and ±15 volt analog multiplexer power supplies, an indicator lamp transformer and circuit board sockets. Upright mounting of the circuit boards in the various sockets eliminates the need for guide rails or other board mounting hardware. Socket layout is logically arranged to correspond, as close as possible, to the order of sequencing operations of the system.

Convential wiring (see Figure 15) is used to interconnect sockets, switches, and other major functional parts of the convertor. The relatively slow speed of the system, the logical socket layout, and the large horizontal ground plane (mounting plate) allow logic cables to be neatly harnessed without encountering pulse coupling problems. Only a few critical sequencing leads (such as the clock pulse from the digital clock and the encode pulse from the Digital Voltmeter) require shielded cable.

As mentioned in the introduction of this chapter, the following sub-sections will describe the individual circuits within the sequential converter. With these circuits, layout diagrams, logic schematic diagrams, and socket wiring diagrams are presented. Together these diagrams describe the complete sequential converter wiring.

6.4.1 The Digital Voltmeter

The Digital Voltmeter (DVM) is used as the voltage analog-to-digital (A/D) converter in the system. Besides providing

the BCD levels representing the input channel voltages, it also provides a visual output that is useful in checking the system's operation.

The DVM is a Data Scan Autopolar Model 720-4 1/2 digit panel meter. It has an input impedance of one megohm, and provides a TTL logic interface for all inputs and outputs. Its valid encoding range is +1.9999 v to -1.9999 v. Two circuit boards within the DVM contain all of the analog and digital circuitry. The DVM's internal zero adjustment, and full scale adjustments have been modified to provide external trim adjustments. These trim potentiometers are shown on the analog board socket wiring diagram in Figure 16. The socket wiring diagram for the second board, the power and logic board, is shown in Figure 17. Since the DVM is a commercial unit, its detailed operation will not be discussed. Its operation will be discussed only in terms of its logic input and output commands. It is assumed that any analog-to-digital converter could be used in place of the DVM, and the system's operation would remain unchanged. However, as an aid to the reader, all pin designations, descriptions, and functions of these boards are presented in Tables 7 and 8.

As in any A/D converter, a logic input or command is required to start the conversion process (encoding) and a logic output is required to indicate when this conversion is completed. With this DVM, the start command is designated the "Hold Command", and the output is called the "End of Encode". Encoding of an input voltage starts when the Hold Command becomes 1. Upon completion of the initial encoding of the voltage, the

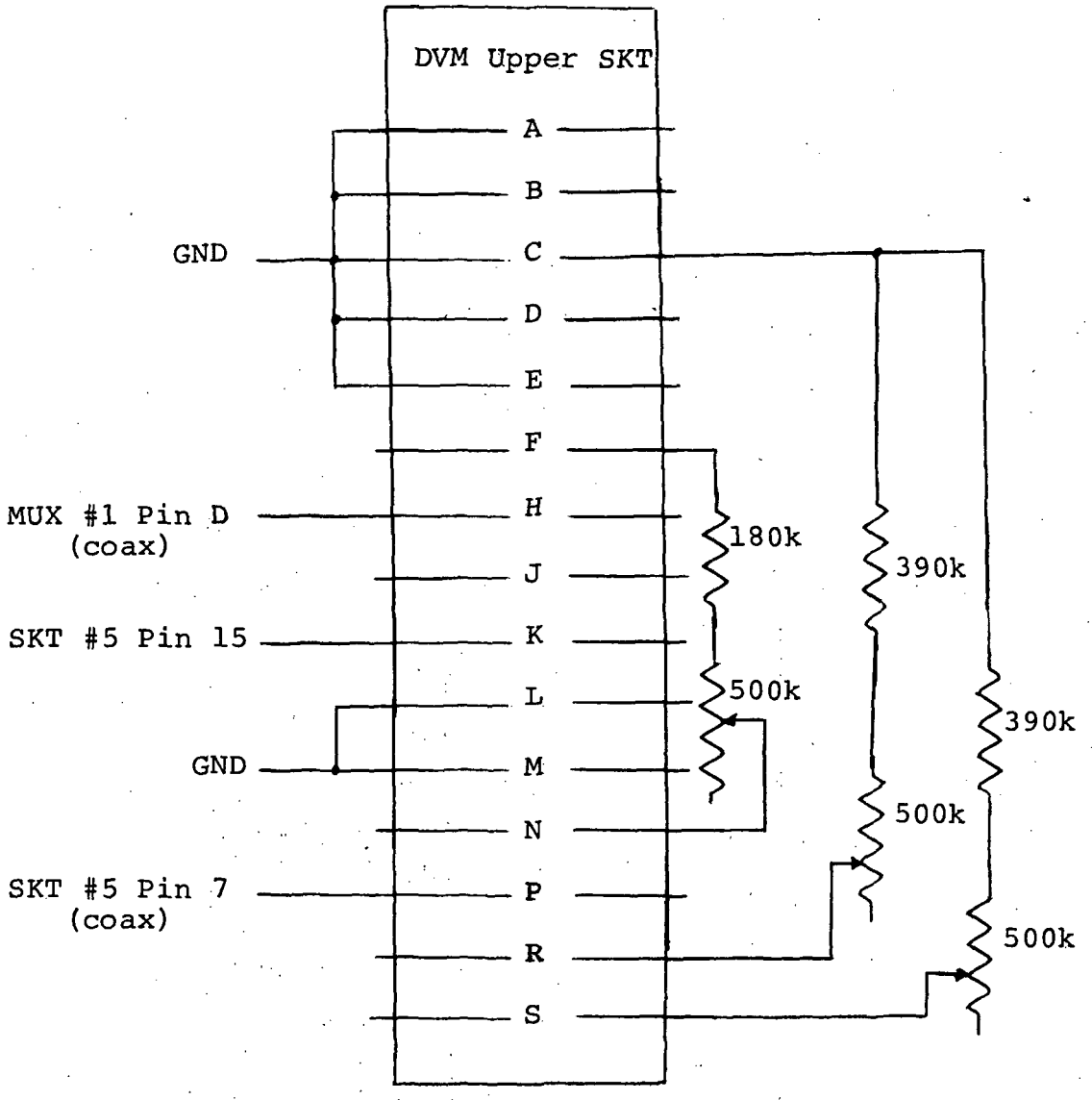


Figure 16. Connections to the DVM Analog Board Socket

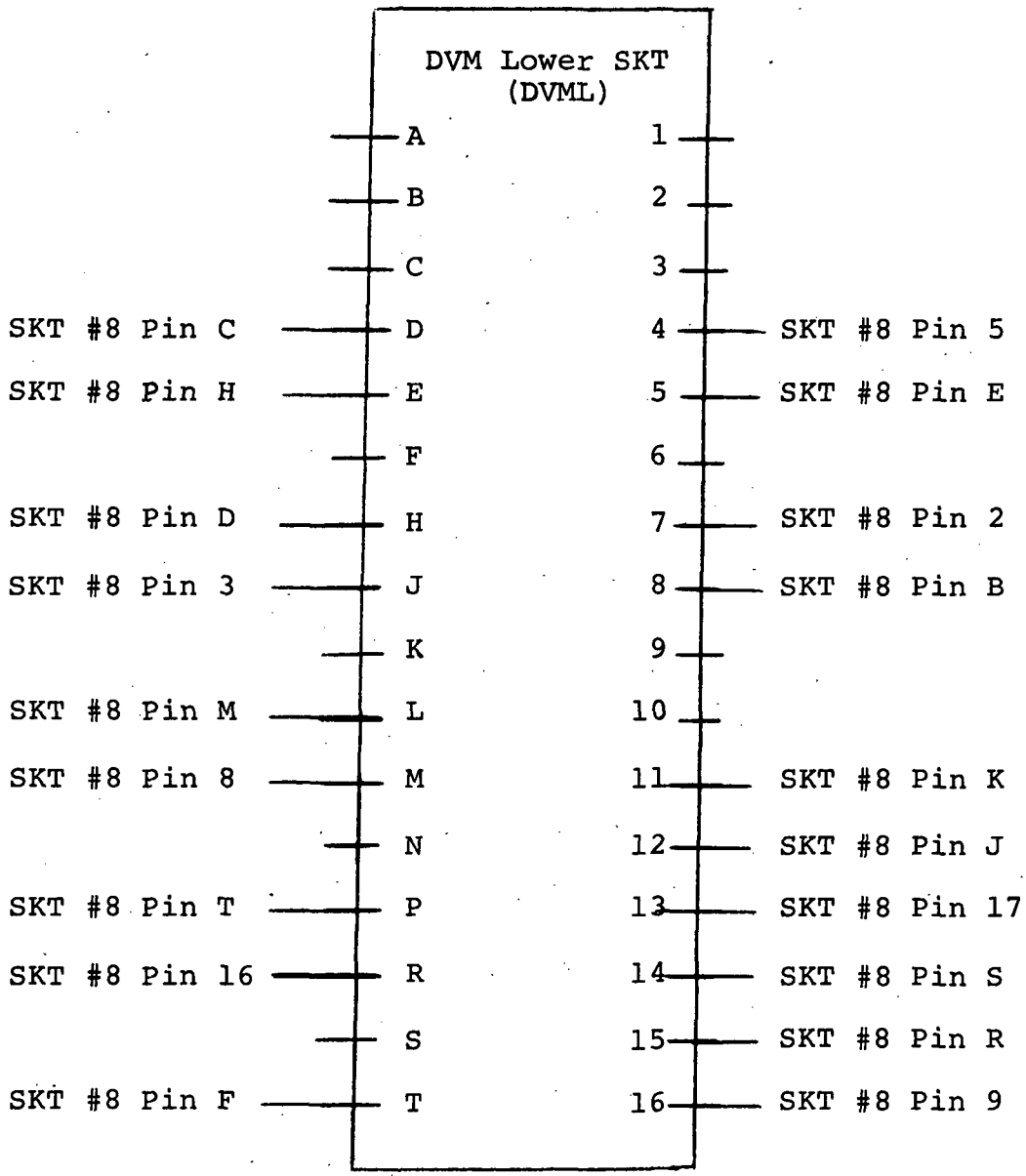


Figure 17. Connections to the DVM Power and Logic Board Socket

Table 7

Inputs and Outputs to the DVM Analog Board

Pin Designation	Description	Function
A		Not connected
B		Not connected
C	Logic Ground	Ground for TTL Logic
D	Input Low	Used for input analog voltage
E	Input Low	
F	Zero Adjust	"Zero adjust" potentiometer
H	Input High	Used for input analog voltage
J	Input High	
K	Hold Command	Input = 0, DVM stops encoding, Input = 1, DVM starts encoding
L	Signal Ground	Connected to System ground
M	Signal Ground	
N	+6v Reference	Used for external "zero adjust" potentiometer
P	End of encode	Output = 1 when DVM is encoding input voltage or Hold = 0. Output = 0 when DVM encoding is complete. Additional 1 to 0 transitions when DVM updates data.
R	Negative Adjust	Used for external "full scale negative adjust" potentiometer.
S	Positive Adjust	Used for external "full scale positive adjust" potentiometer.

Table 8

Inputs and Outputs to the Power and Logic Board

Designation	Description	Function
A	AC High	to 110v AC
B	AC Low	to 100v AC
C	Power Ground	System Ground
D	BCD Units 2	BCD Output
E	BCD Units 8	BCD Output
F	unit decimal point	Not used
H	BCD tens 4	BCD output
J	BCD tens 8	BCD output
K	Tens decimal point	Not used
L	BCD hundreds 4	BCD output
M	BCD hundreds 8	BCD output
N	Hundred decimal point	Not used
P	BCD thousands 4	BCD output
R	BCD thousands 8	BCD output
S	Thousands decimal point	Not used
T	Overange bit	Output=0 when 1.9999v $\geq$ |input voltage| $\geq$ 1.0000v Output=1 otherwise
U	Not connected	
V	Not connected	
1	AC high	Same as pin A
2	AC low	Same as pin B
3	Power Ground	Same as Pin C
4	BCD units 4	BCD output
5	BCD units 1	BCD output
6	Not connected	
7	BCD tens 2	BCD output
8	BCD tens 1	BCD output
9	Not connected	
10	Not connected	
11	BCD hundreds 2	BCD output
12	BCD hundreds 1	BCD output
13	BCD thousands 2	BCD output
14	BCD thousands 1	BCD output
15	Outrange bit	Output=0 when |input voltage| > |1.9999v| Output=1 otherwise
16	Polarity bit	Output=0 when input voltage is negative Output=1 when input voltage is positive
17	Not connected	
18	Not connected	

End of Encode makes a 1 to 0 transition. In the sample mode this transition is used to trigger a flip-flop on the Voltage Data Sequencer, Board #5, that initiates recording logic, and also causes the Hold Command to become 0. When the Hold Command is 0, the A/D converter outputs remain fixed (held), the End of Encode returns to 1, and the voltage is recorded. While the A/D is being held, its analog input is switched to the next channel voltage. Upon completion of the recording sequence, the Hold Command again becomes 1, and the process is repeated until all of the channel voltages are recorded. When the system is in the manual mode, the Hold Command is fixed to logic 1, and the A/D converter repeatedly encodes the manually selected input channel voltage (the End of Encode output is ignored).

Since the system processing time of an analog input (the time required to sample the input, perform the required A/D conversion, and record the digital data on magnetic tape) is equal to the DVM encoding time plus the system recording time (30 ms using a 5 digit format and a 166 bps recording speed), the long encoding time (500 ms) of the DVM severly limits the system's capability. Replacement of the DVM with a faster unit is straightforward and would involve few changes to the existing sequential converter logic.

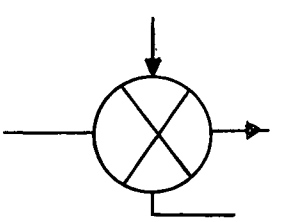
6.4.2 The Analog Multiplexer

Input voltage switching to the DVM is provided by two commercial circuit board configured analog multiplexers. Designated "Multiplexer #1" and "Multiplexer #2" (or "MUX #1"

and "MUX #2") these multiplexers, MOSES-8, are manufactured by Analog Devices Incorporated. Socket wiring for Multiplexer #1 and Multiplexer #2 is in Figures 18 and 19.

These multiplexers each contain eight TTL logic controllable MOSFET switches. A common signal gound is utilized for all inputs and outputs. Hence, all input channel voltages are supplied to, and measured by, the system with respect to ground. Each multiplexer provides eight separate analog outputs, permitting simultaneous measuring of more than one input voltage if a corresponding number of A/D conversion devices are available. In this system, using only one A/D conversion device, all multiplexer outputs are connected together to form a single analog output. Further, the analog output of MUX #1 is connected to the analog output of MUX #2. The resultant circuitry provides an equivalent sixteen port input and one port output electronic switch. (The switch position is determined by the sequential converter logic.)

A block diagram, illustrating multiplexer analog and digital circuitry is shown in Figure 20. In this figure the symbol shown below is used to denote a single MOSFET switch.



MOSFET SWITCH

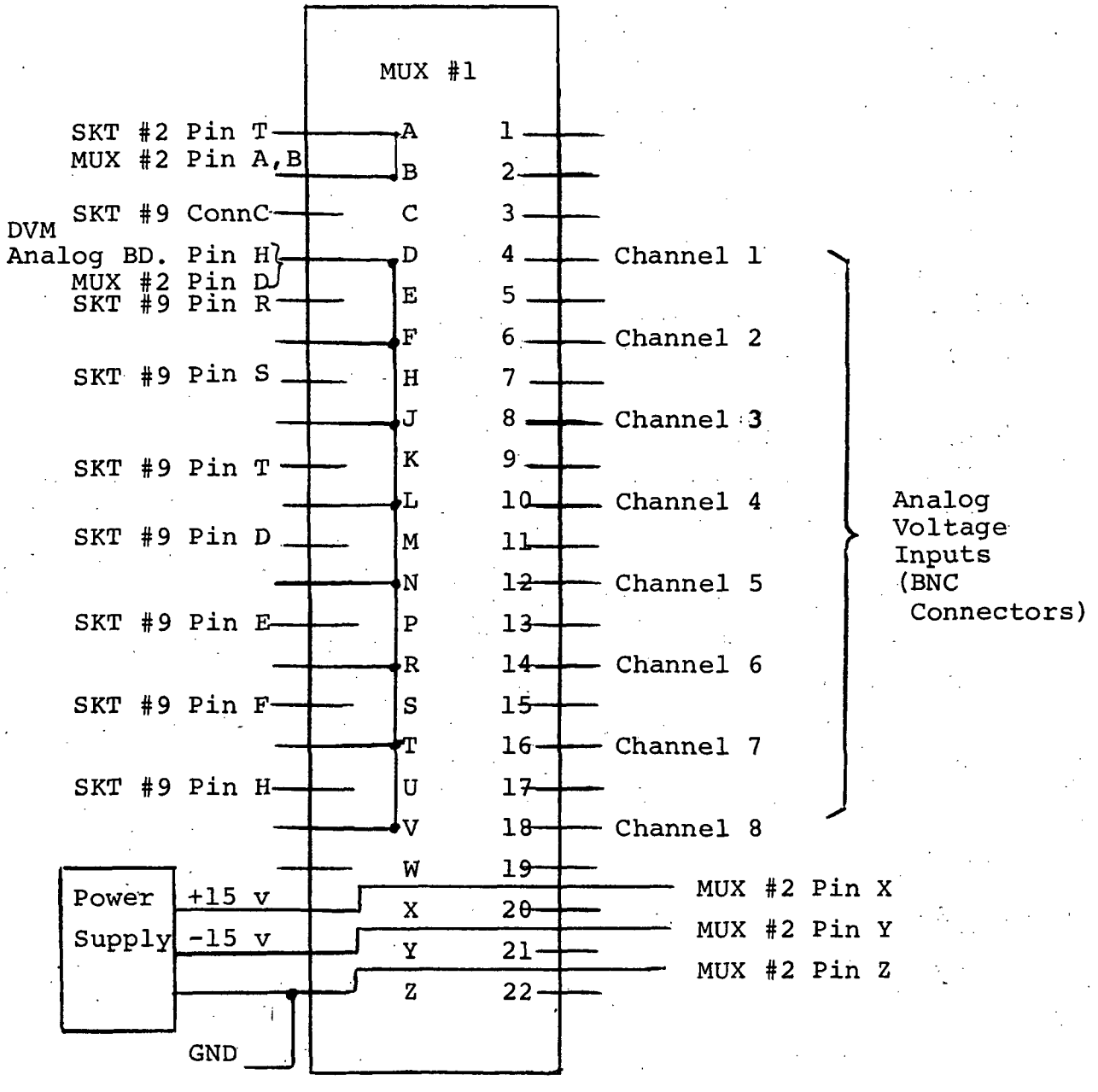


Figure 18. Connections to the First Analog Multiplexer Socket

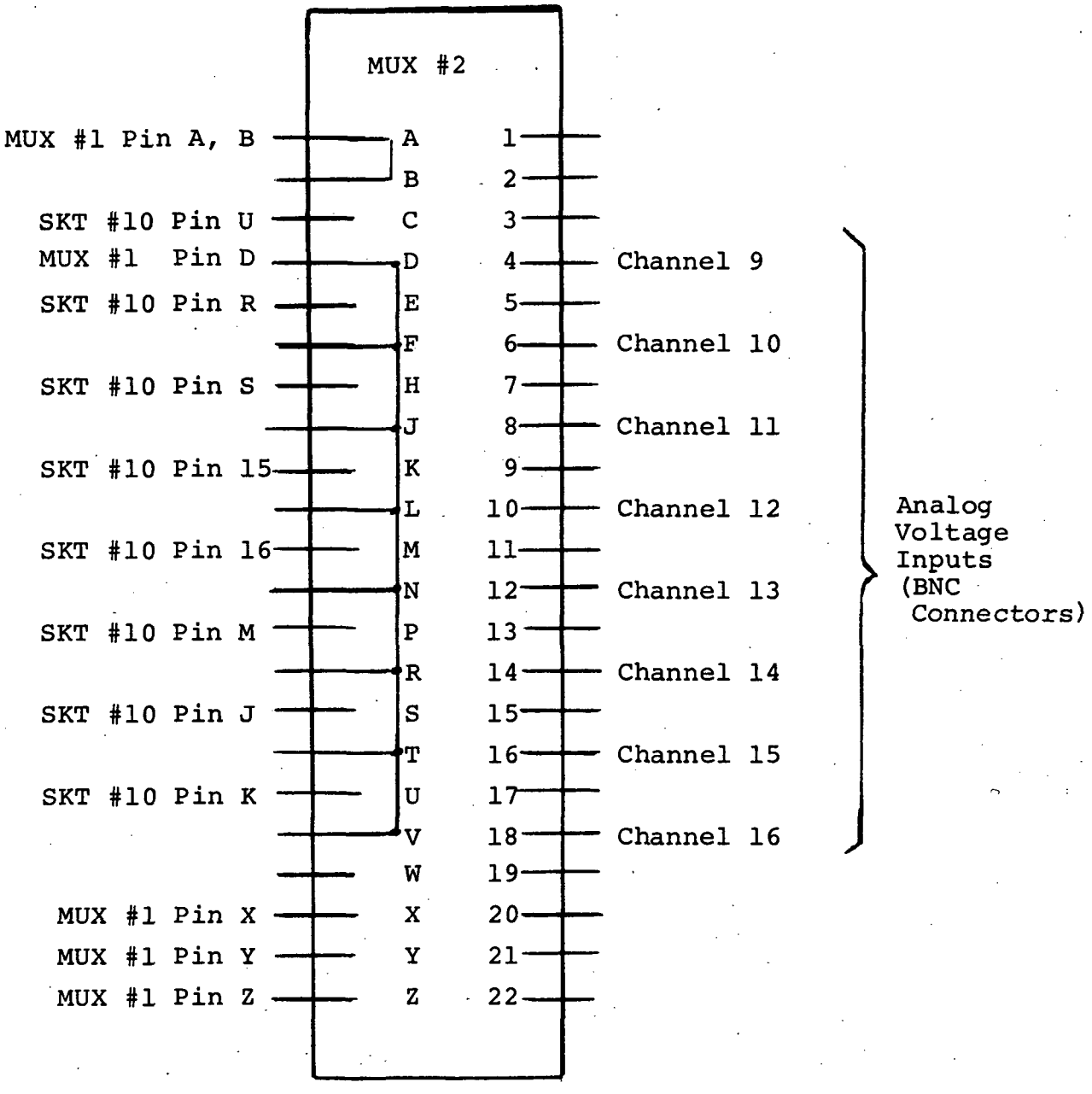


Figure 19. Connections to the Second Analog Multiplexer Socket

The lines without the arrows are the digital inputs, and the lines with the arrows are the analog input and output of the switch. (The maximum analog input voltage is ±5 volts.) The switches have two well defined analog states, an On state and an Off state. In the On state the switch is equivalent to a low impedance connection (a virtual short) between its analog input and output. Conversely, in the Off state, this switch is equivalent to a high impedance connection (a virtual open) between its analog input and output. In both states, the open circuit input and output impedances (with respect to signal ground) approach infinity. In Figure 20 the channel 1 through 8 inputs are (4), (6), (8), (10), (12), (14), (16), and (18) and the corresponding outputs, connected in parallel at the socket, are (D), (F), (J), (L), (N), (R), (T) and (V), respectively.

Two digital control inputs are associated with each MOSFET switch on the multiplexer. A common logic input for all switches is connected to the output of a 2-input NAND gate. Inputs to this gate are (A) and (B). In this system these inputs are connected together providing a single override input to an equivalent inverter. Each switch has a separate logic input that is driven by an inverter. The inputs of these inverters, individual control inputs for channels 1 through 8, are (C), (E), (H), (K), (M), (P), (S), and (U). Any MOSFET switch is in its On state only when the override input is 1 and its control input is 1.

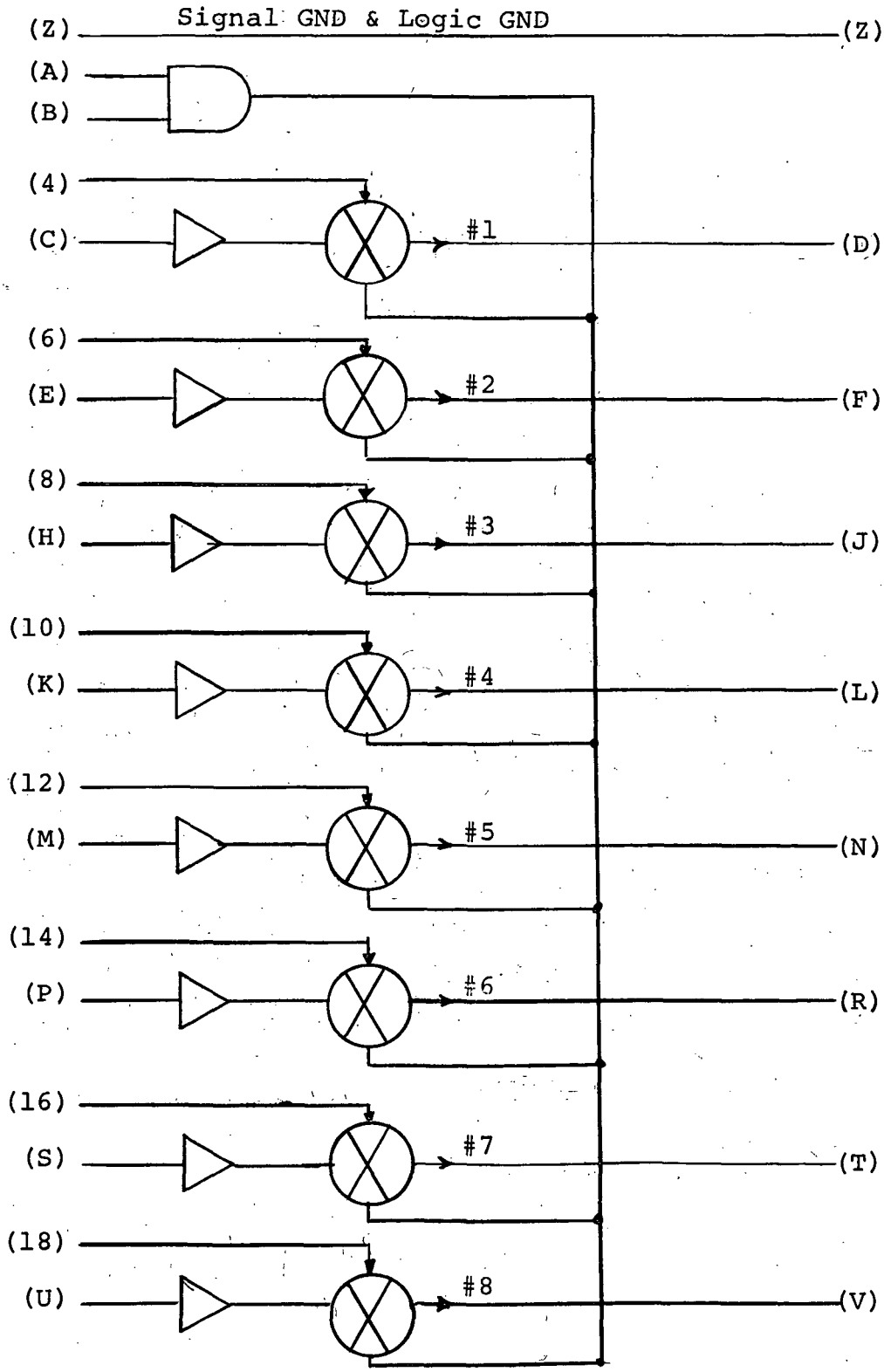


Figure 20. An Equivalent Circuit for the Analog Multiplexer

In the manual mode the override input is normally 1. A single-pole rotary switch is used to fix the state of a single control input to 1. The associated MOSFET switch is turned On and its analog input is connected to the DVM. There is one position on the switch for each of the input channels. This switch has break-before-make contacts to prevent turning On two of the MOSFET switches at the same time. (See Section 6.4.13 and 6.4.14)

In the sample mode, the state of the override input is determined by the output of the Master Sequencer (Board #2). The states of the control inputs are determined by the bit states of four shift registers connected in cascade on Boards #9 and #10. Except during switching transitions associated with the shift registers, one and only one of the control inputs may be 1. The switching from channel N to N+1 involves the right-shifting of a 1 bit in the shift register. During this shifting operation, the states of both channel N and channel N+1 control inputs are briefly 1. (The overlap time is less than one microsecond.) If the override input is 1 when this overlap occurs, a momentary input short would occur between the two adjacent channel inputs. This short circuit is prevented by connecting the override input to the Master Sequencer circuitry. Right-shifting of the 1 bit in the channel selector shift registers occurs when the state of the last bit position in the Master Sequencer shift register becomes 1. In Section 6.4.6 it will be shown that Master Sequencer output (T), connected to the override inputs of the multiplexers, assumes a state of 0 when any one of the Master Sequencer's

shift register bits is 1. On the next clock pulse into the sequencer, the shift register has all bit states equal to 0 and output (T) becomes 1. Thus, the override inputs are 0 for one clock pulse (one millsecond) after the start of the transitions of the control inputs. This time separation prevents the momentary shorting of two input channels.

6.4.3 Sample/Manual Mode Switching Circuit

As mentioned in previous chapters, the data logging system has two modes of operation: the sample mode and the manual mode. Mode switching is accomplished using a two position rotary switch and discrete components.

Two outputs, labeled "M=0" and "M=1", are generated by the mode switching circuitry. As the name suggests, the "M=0" output is 0 when the mode switch is in the manual mode and is 1 when the mode switch is in the sample mode. The "M=1" output is the inverse of the "M=0" output.

The "M=0" and "M=1" outputs are used as inputs for many of the system circuits. Primary uses of these outputs are:

1. Enabling the diode matrix logic for manual data recording.
2. Disabling or clearing of shift registers and flip-flops when the system is in the manual mode.
3. Controlling encoding circuitry.
4. Changing the clock pulse frequency from the digital clock.

The individual functions of these outputs will be explained as a part of the operational description of the other circuits.

Figure 21 is a schematic drawing of the mode switching circuit. A single-pole, single-throw switching arrangement using a rotary switch with little "contact bounce" reduces switching noise and extraneous pulse generation during switching transitions. This discrete component inverter provides the high fanout capability required for the "M=1" output. Additionally, use of an inverter, as opposed to a multiple-pole switching scheme, prevents both outputs ("M=0", "M=1") from simultaneously having the same state during switching.

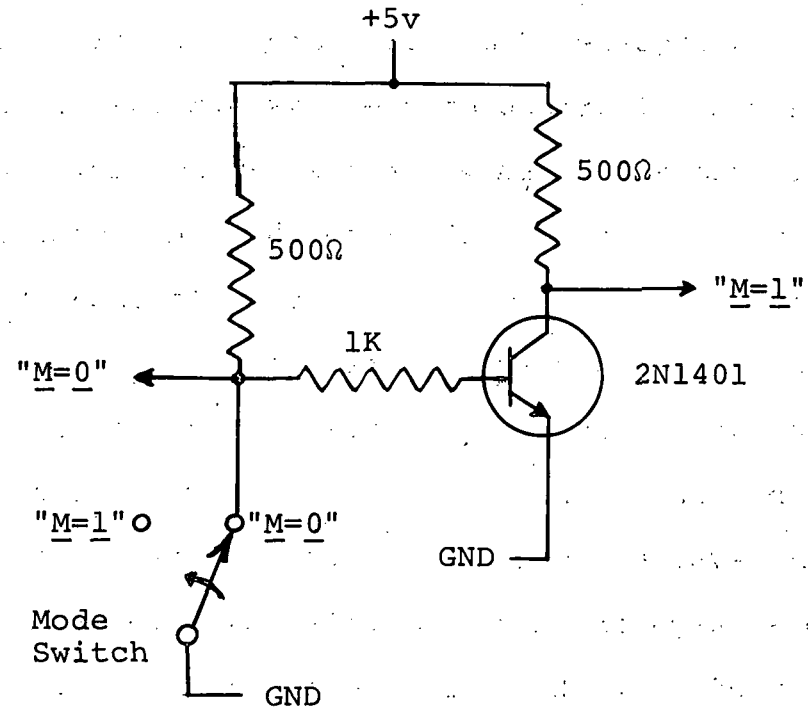


Figure 21. The Sample/Manual Mode Switching Circuit

6.4.4 The Diode Matrix and Manual Keyboard

The Diode Matrix is a twenty-two by ten matrix used to provide encoding information and sequencing commands for manual data recording. The circuit contains 11 resistors and 79 diodes hand wired on a fiberglass-epoxy, perforated circuit board. The schematic drawing for this circuit board is shown in Figure 22.

Twenty-two keys, wired as shown in Figure 23, provide for manually inputting data into the Diode Matrix. All of the keys have a common connection to "M=0". The physical layout of these keys on the keyboard is shown in Figure 24. Parentheses above each key (in Figures 23 and 24) denote its pin connection to the Diode Matrix. Fourteen of the keys are used to generate the alphanumeric characters shown in the EBCDIC table in Section 3.2. (No key is provided for "G" since this character is used only in the sample mode.) Eight other keys, labeled "0" - "7" in Figures 23 and 24, are used to generate single level 1's on the magnetic tape as an aid in hardware trouble shooting and software debugging. The two remaining keys on the keyboard, the IRG and ERR keys, are marked with an asterisk on Figures 23 and 24. These keys are not associated with the Diode Matrix. The IRG key is used to write an inter-record gap when the system is in the manual mode (see Section 6.4.5). The ERR key is used to duplicate a write error condition when the system is in the sample mode (see Section 6.4.14).

The Diode Matrix outputs are "Record Enable", "$\overline{\text{Level 0}}$", "$\overline{\text{Level 1}}$", "$\overline{\text{Level 2}}$", "$\overline{\text{Level 3}}$", "$\overline{\text{Level 4}}$", "$\overline{\text{Level 5}}$", "$\overline{\text{Level 6}}$",

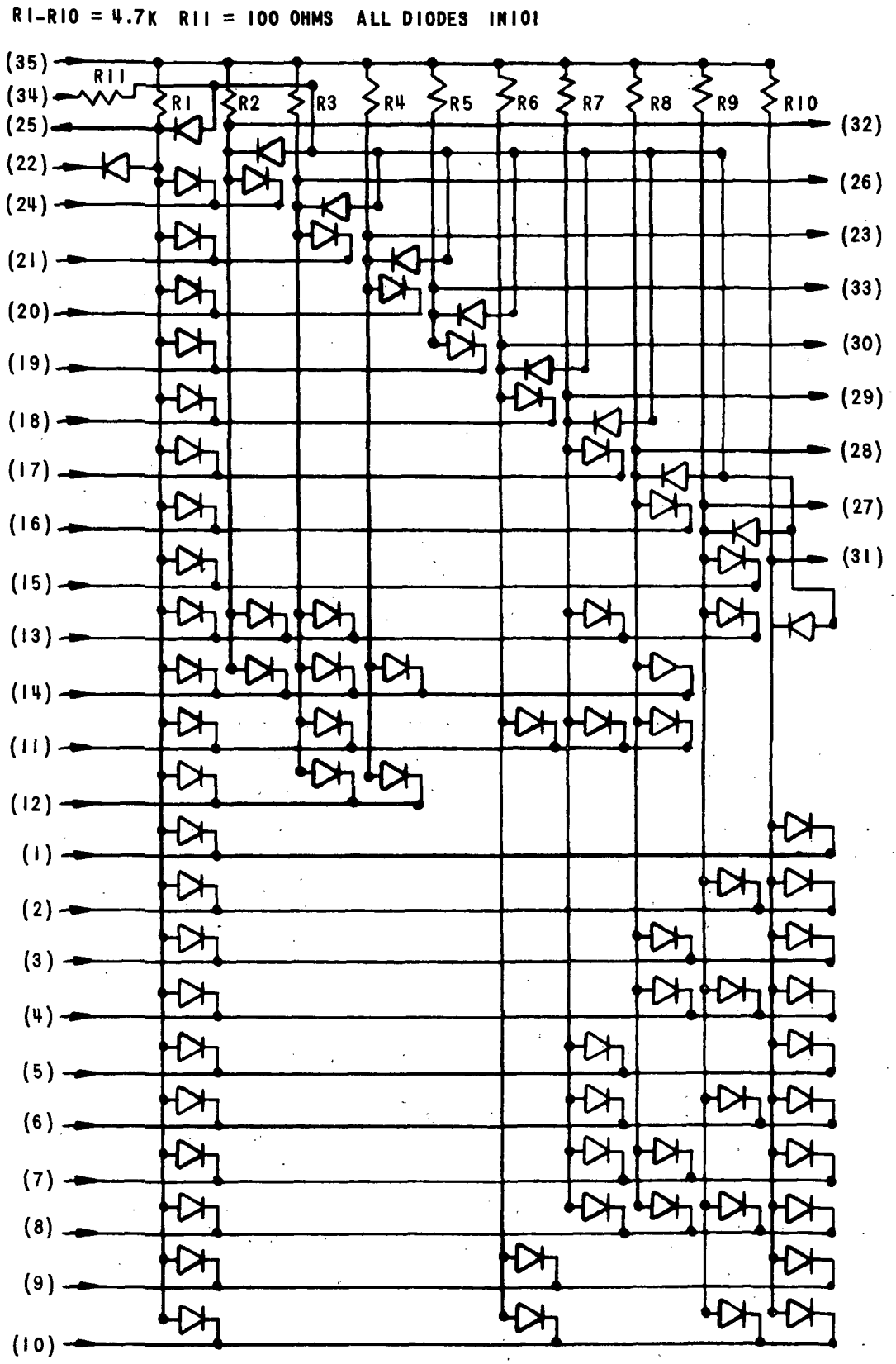


Figure 22. The Diode Matrix Schematic

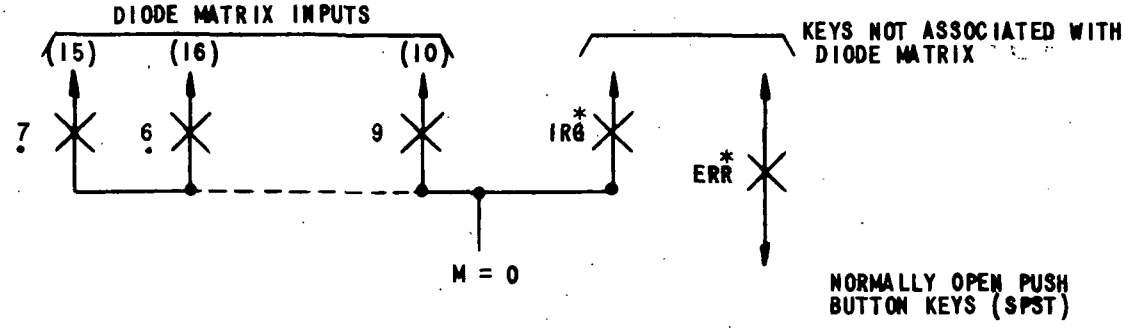
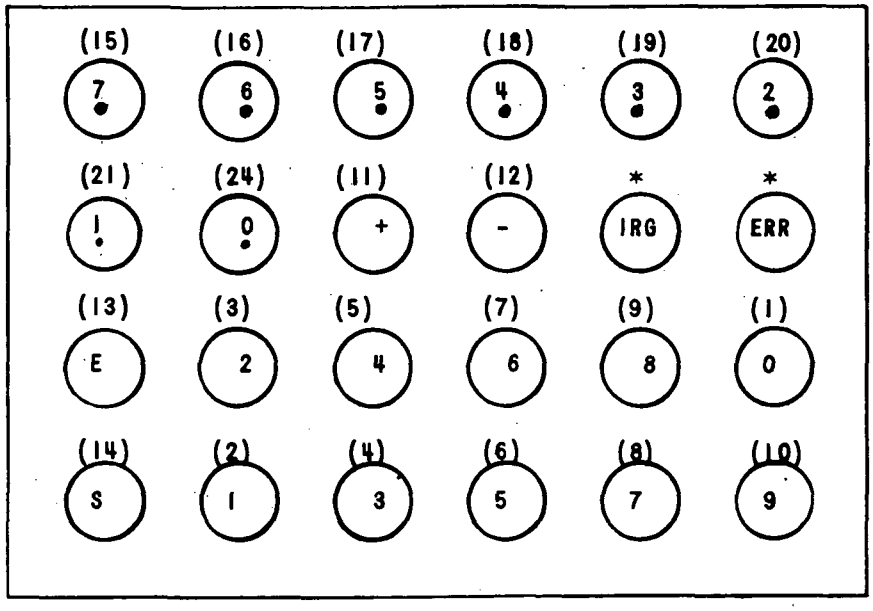


Figure 23. The Manual Keyboard Wiring



KEYS MARKED * ARE NOT USED TO GENERATE MANUAL CHARACTERS. THEY WILL BE DISCUSSED IN OTHER SECTIONS

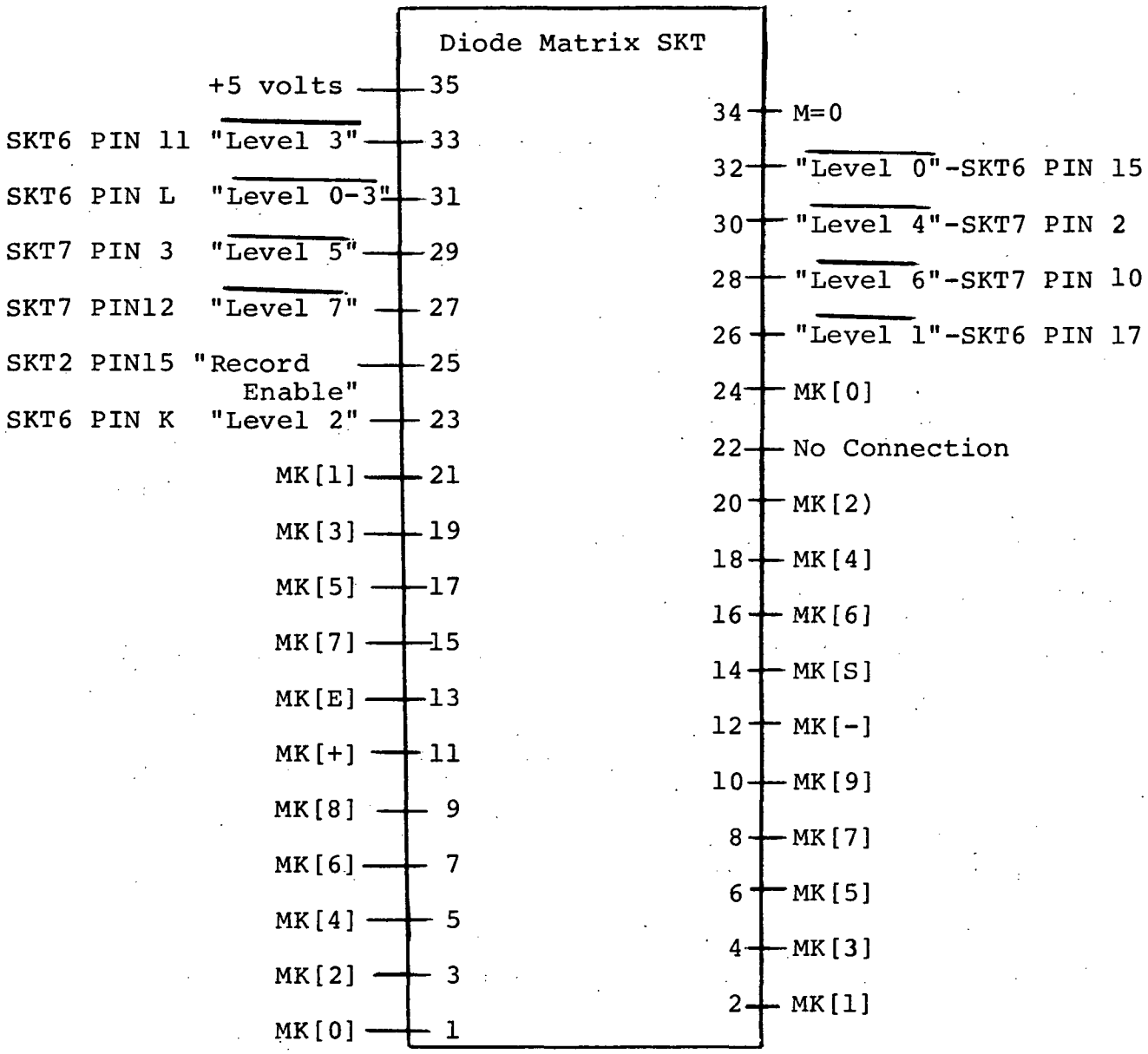
( ) INDICATES PIN NUMBER ON DIODE MATRIX BOARD SOCKET

Figure 24. The Manual Keyboard Layout

"Level 7", and "Level 0-3". The pin designations for these outputs are shown in Figure 25. In the manual mode, the "Record Enable" output provides a 1 to 0 transition when any manual key is depressed. This transition enables the Master Sequencer, providing a single write command pulse to the incremental magnetic tape recorder (see Section 6.4.6). The eight single level outputs, "Level 0" through "Level 7", provide output states that are the inverse of the eight levels that are shown in the EBCDIC coding table. For example, when the "-" key is depressed (and the system is in the manual mode) "Level 1" and "Level 2" outputs become 0 while all other outputs remain 1. The tenth output, "Level 0-3", is used for numeric characters. The use of one output to represent four levels simplifies encoding circuits and greatly reduces the number of diodes in the matrix. The output condition "Level 0-3" = 0 is logically equivalent to "Level 0" = 0, "Level 1" = 0, "Level 2" = 0, and "Level 3" = 0. Since the level 0 through 3 states of all numeric characters are 1, this output becomes 0 when a manual key is depressed.

In the manual mode, closing a key causes some diodes in the matrix to conduct. Since these diodes, germanium diodes, are forward biased into their high conductanic region, their forward voltage drop is less than .35 volts. A current sink with a voltage drop of less than .8 volts is a valid TTL Logic 0 output. Hence, the states of the outputs associated with the conducting diodes will be 0.

Circuit operation of the Diode Matrix and associated manual keys can best be described by using a partial schematic diagram



MK[ ] INDICATES CONNECTION TO THE MANUAL KEY GENERATING [ ] CHARACTER

" " INDICATES OUTPUT FUNCTION

Figure 25. Connections to the Diode Matrix Socket

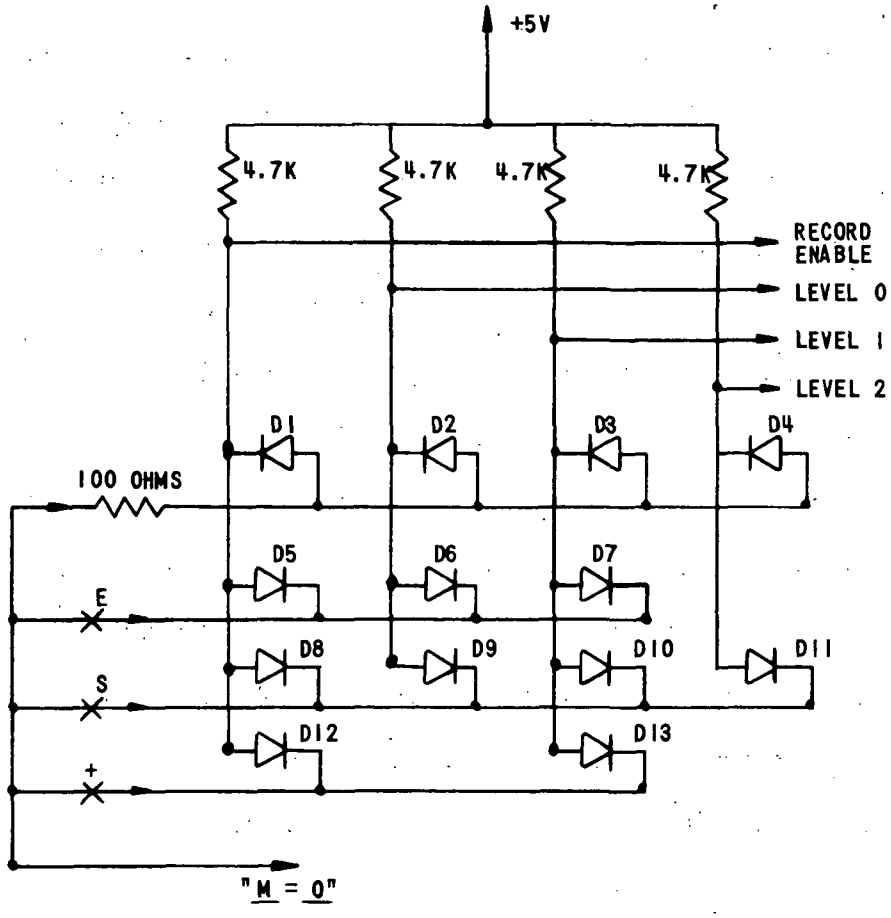


Figure 26. A Partial Diode Matrix Schematic

of the Diode Matrix, Figure 26. In this figure, some of the diodes, D5 through D13, are used to generate the 0 output states that are required to record a particular manual character. Since this recording is accomplished with the system in the manual mode, the "M=0" input is connected to ground and D1 through D4 are reverse biased. When the key "E" is depressed diodes D5, D6, and D7 conduct to ground. The states of the associated outputs, "Record Enable", "$\overline{\text{Level 0}}$", and "$\overline{\text{Level 1}}$", are 0. Similarly, diodes D8, D9, D10 and D11 conduct when the "S" key is depressed, causing all of the output states shown to be = 0. As each manual key is depressed only those outputs associated with conducting diodes are 0 and all other outputs are = 1. Hence, all of the outputs will be equal to 1 in the manual mode if none of the keys are depressed. When the system is in the sample mode the "M=0" output is connected to +4.5 volts, and all diodes, except D1 through D4, will be nonconducting. Hence, all matrix outputs will be 1. (Key closures do not affect this output.) Diodes D1 through D4, are slightly forward biased and they are used to lower the output impedance of the Diode Matrix outputs when it is in this mode.

6.4.5 The Record Pulse Generator

The Recorder Pulse Generator, Board #1, is a dual purpose board consisting of eight TTL devices with both arithmetic and nonarithmetic elements. A device layout diagram, a logic schematic diagram, and a socket wiring diagram for this board are given in Figures 27, 28, and 29.

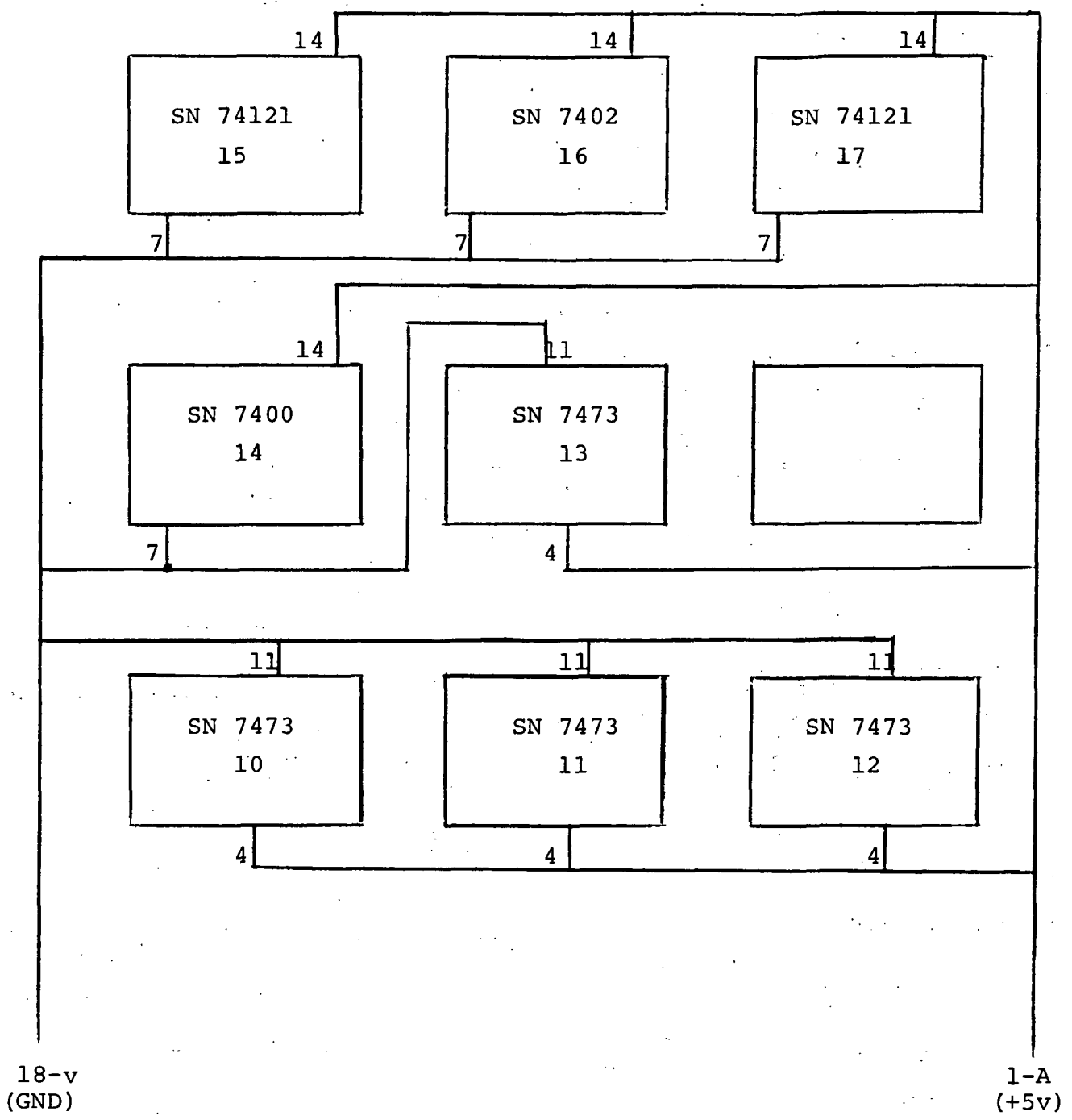


Figure 27. The Recorder Pulse Generator - Power Wiring and Device Location Diagram

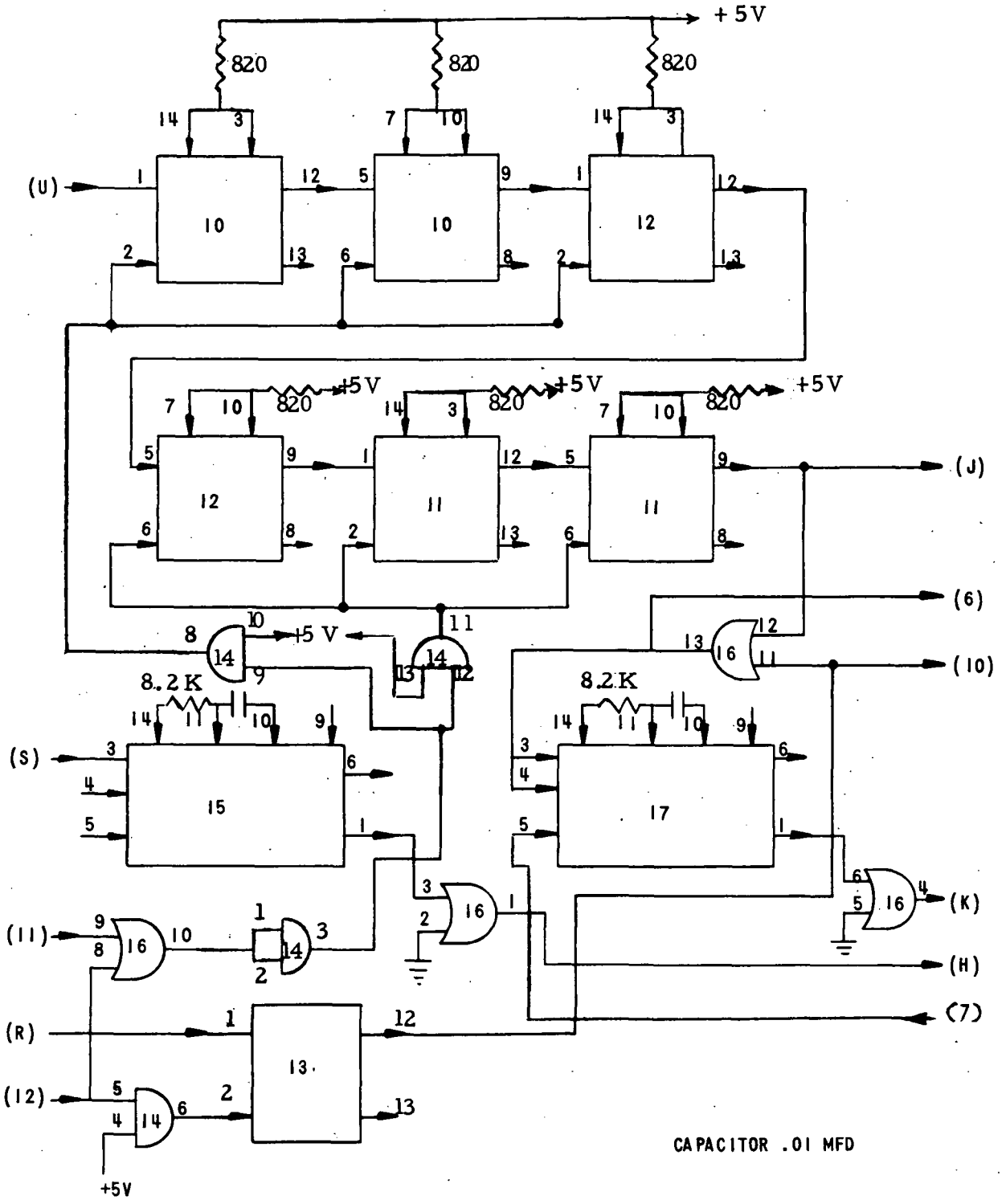


Figure 28. The Recorder Pulse Generator Logic Schematic

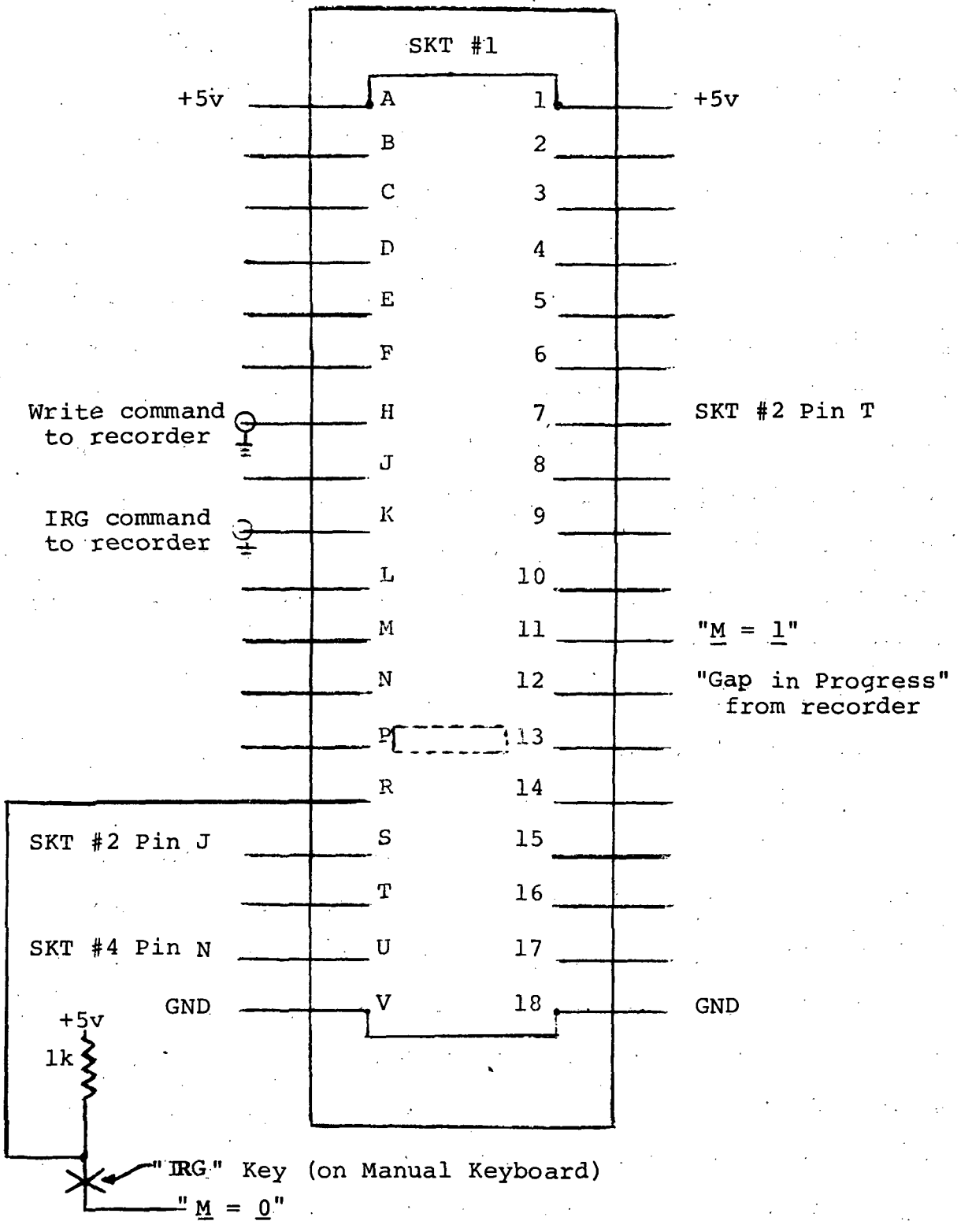


Figure 29. Connections to the Recorder Pulse Generator Socket

The first circuit contained on this board is the write pulse generator. This circuit provides a single write pulse to the tape recorder for recording each character. The input to this circuit is (S) and the output is (H). The input (S), connected to the first bit output of the Master Sequencer shift register (discussed in the next section) makes a 1 to 0 state transition each time a character is to be recorded. This transition triggers a one-shot multivibrator, device 15, providing a $\overline{Q}$ equals 0 output pulse of approximately 40 miscroseconds. The $\overline{Q}$ output of this multivibrator is connected to an input of a NOR gate used as an Inverter. The gate output is connected to (H), therefore (H) equals Q. The use of this buffering arrangement (also used for the IRG pulse output) prevents electrical damage to the multivibrator if a failure in the recorder or its connecting cable occurs.

The second circuit on this board provides the IRG command to the tape recorder. The inputs to the circuits are (11), (7), (12), (R), and (U). The output (K), a buffered 40 microsecond pulse, is used to command the IRG circuitry in the recorder.

Input (U), connected to Board #4, makes a 1 to 0 state transition upon completion of each sample mode scan. With the system in the sample mode, J-K flip-flops (devices 10, 12 and 11) provide a divide-by-thirty-two counting chain. (Since binary counters are used in the counting chain, a change in the number of scans between record blocks can easily be accomplished.) The Q output of the last counter in the chain (pin 9 Device 11) makes a 0 to 1 transition after the thirty-second scan is complete.

The inverse of this transition and (7) equal to 1 triggers a monostable multivibrator, device 17, providing the IRG pulse to the tape recorder. While the IRG is being written by the recorder, the recorder's "Gap in Process" output has a state = 1. This output is connected to (12) to clear the counting flip-flops through NOR gate 16 and NAND gate 14.

In the manual mode, input (11) is 1, and the counting flip-flops are cleared. Depressing the IRG key on the manual keyboard causes input (R) to become 0, triggering a flip-flop, device 13, and changing its Q output state to 1. Triggering of the multivibrator is again accomplished through a NOR gate operating as an Inverter. The same "Gap in Process", output used to clear the counting chain in the sample mode, clears this flip-flop through NAND gate 14.

6.4.6 The Master Sequencer

In the sequential converter, all sequencing operations must be performed in a definite order. The system must generate a set of synchronized clock pulses that will satisfy the timing requirements for all sequencing operations. The circuit that does this is called the Master Sequencer, Board #2. It is the brain of the sequential converter. Just as the human brain governs the body's operation, the Master Sequencer governs the data system's operation.

The Master Sequencer generates the required synchronized clock pulses by using the outputs of a ring counter circuit. This counter employs a logic-controllable feedback loop. This loop enables the counter circuits and causes the counter

to recycle. This counter provides the synchronized outputs to the other circuits as they are required. The operation of this sequencer is discussed below with the aid of Figures 30, 31, and 32.

All of the outputs of the Master Sequencer can be expressed in terms of the five-bit shift register's bit outputs (device 24 in Figure 31). To simplify the Boolian algebraic equations for these outputs, A_2 is defined as the first bit output, and B_2, C_2, D_2, and E_2 are the second, third, fourth, and fifth bit outputs. Using these definitions, the outputs at the board socket are:

$$\underline{(J)} = \underline{A_2} \qquad \underline{(H)} = \underline{A_2} \vee \underline{B_2} \vee \underline{C_2} \vee \underline{D_2} \vee \underline{E_2}$$

$$\underline{(K)} = \underline{(11)} = \underline{A_2} \vee \underline{B_2} \qquad \underline{(16)} = \overline{\underline{C_2}}$$

$$\underline{(U)} = \underline{C_2} \qquad \underline{(9)} = \underline{(14)} = \overline{\underline{A_2} \vee \underline{B_2}}$$

$$\underline{(M)} = \underline{D_2} \qquad \underline{(R)} = \overline{\underline{D_2}}$$

$$\underline{(12)} = \underline{(E)} = \underline{E_2} \qquad \underline{(3)} = \overline{\underline{E_2}}$$

$$\underline{(F)} = \underline{D_2} \vee \underline{E_2} \qquad \underline{(4)} = \overline{\underline{D_2} \vee \underline{E_2}}$$

$$\underline{(T)} = \overline{\underline{A_2} \vee \underline{B_2} \vee \underline{C_2} \vee \underline{D_2} \vee \underline{E_2}}$$

The pulsing of these outputs generates the required synchronized clock pulses. This pulsing is determined by the control inputs to the feedback circuitry and by the master clock input. The control inputs determine the number of continuous ring counter cycles that occur for each sequencing operation, and the master clock input determines the time required to complete a cycle of the ring counter. The operation of the sequencer is discussed below using these inputs.

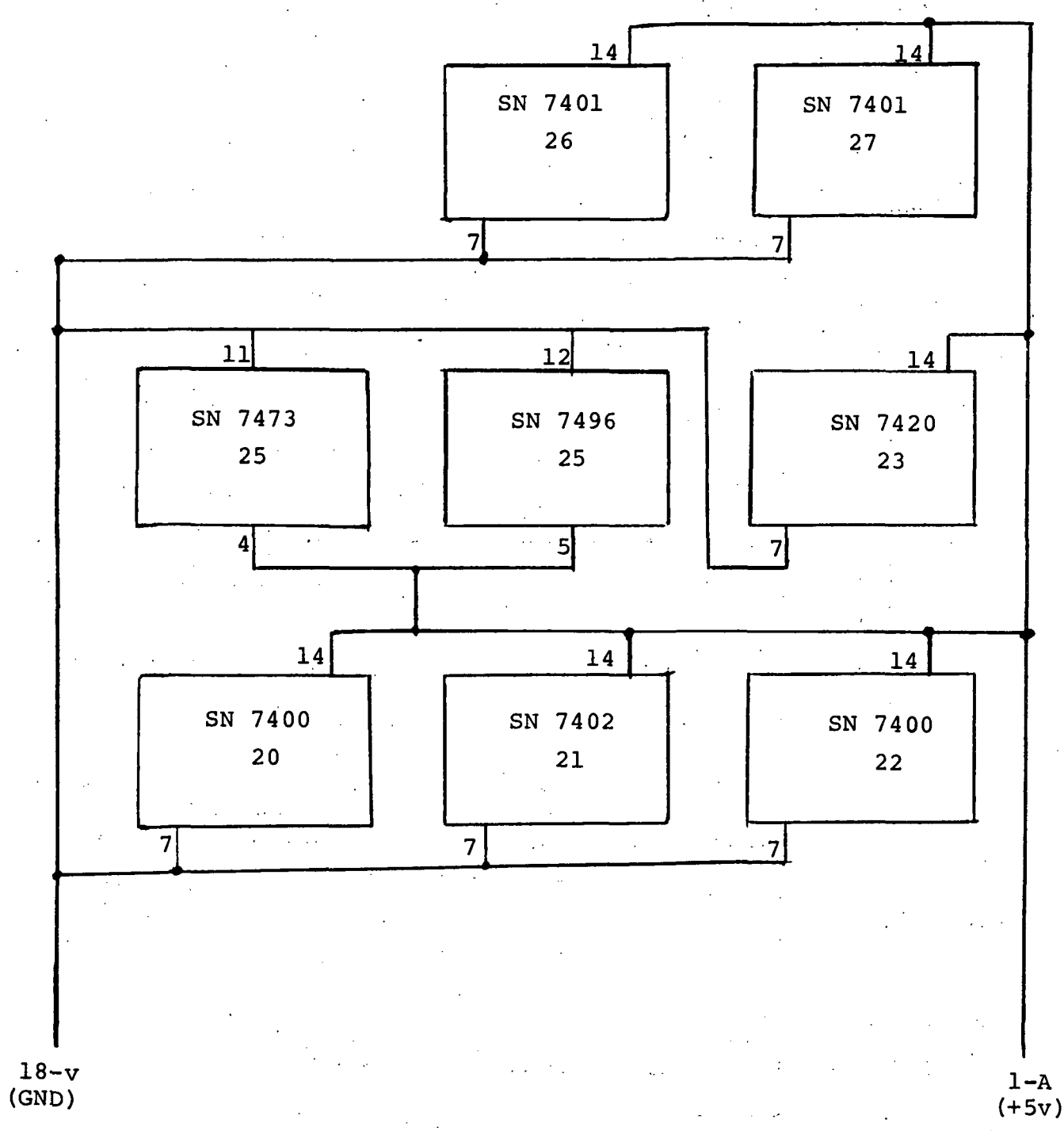


Figure 30. The Master Sequencer - Power Wiring and Device Location Diagram

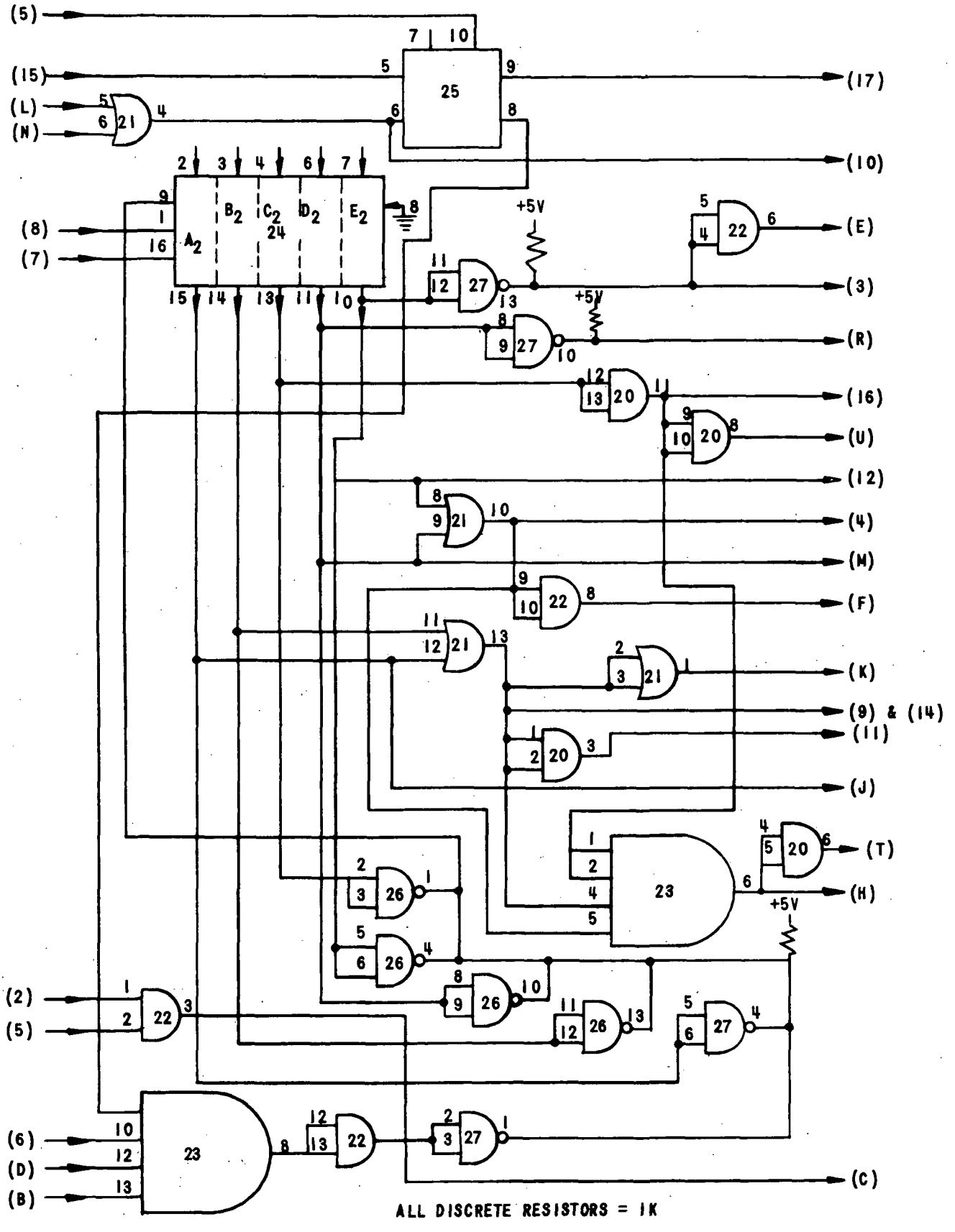
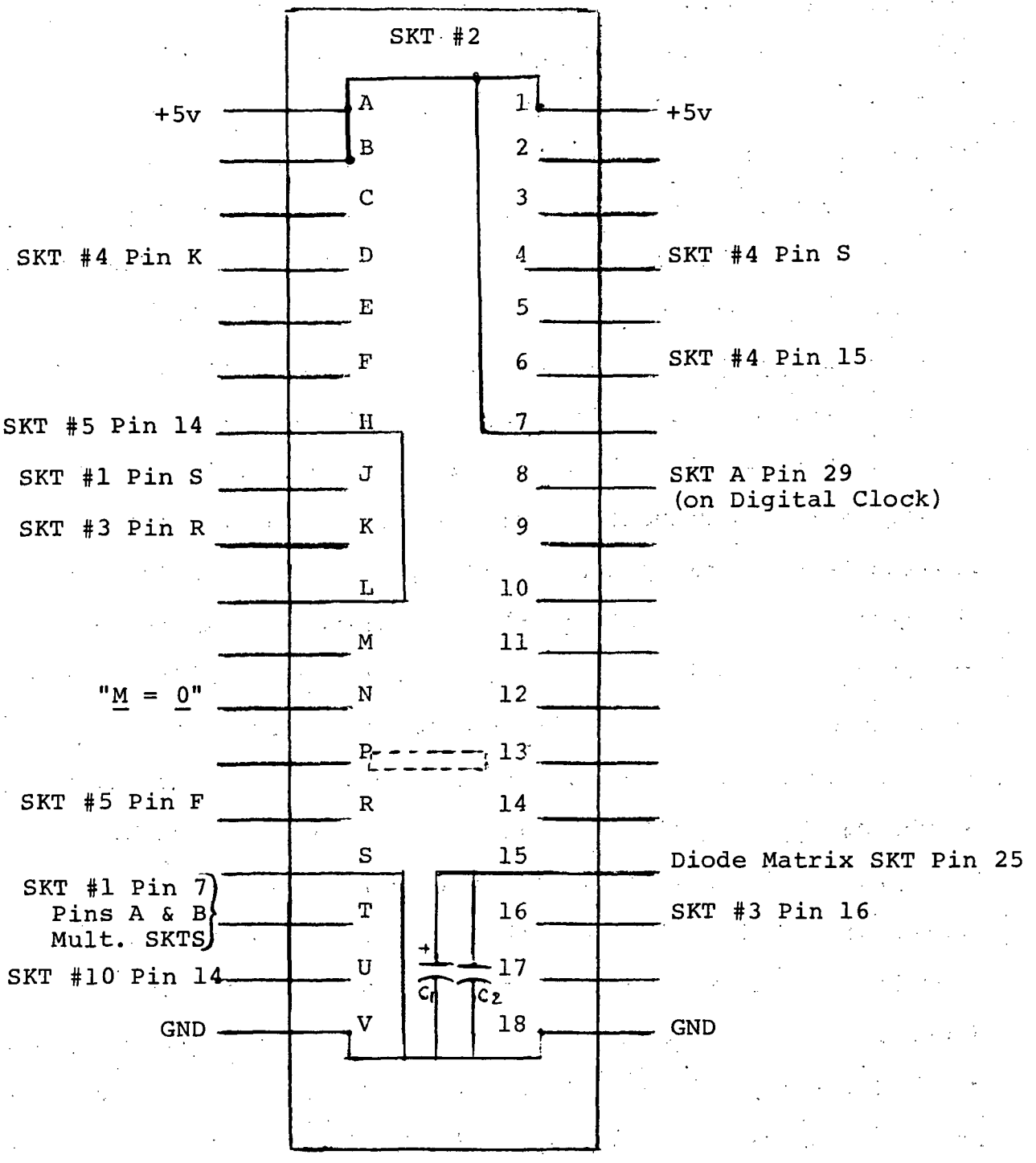


Figure 31. The Master Sequencer Logic Schematic



C1 = 47 MFD, 50 volt

C2 = .01 MFD, 200 volt

Figure 32. Connections to the Master Sequencer Socket

The ring counter uses a five-bit shift register to sequentially output bit states equal to 1. Specifically, the serial input, pin 9, of the shift register is connected to the output of a feedback loop circuit (open collector NAND gates wired as Inverters to provide an equivalent multiple input NOR gate). With all shift register bit outputs equal to 0, and Pin 8 device 23 equal to 1, the serial input will be equal to 1. The leading edge of the input clock pulse, (8), (1 KHz or 100 Hz) causes this serial input of 1 to be loaded into the first bit position of the shift register. However, when the shift register has any bit state equal to 1 the serial input will return to 0. Consequently, subsequent clock pulses will load 0's into the register's first bit position and right-shift a single 1 from the first to the last bit position. A ring counter cycle thus consists of six unique bit output conditions. The first five of these conditions occur when one bit state is equal to 1 and all other bit states are equal to 0 (first condition, A_2 = 1, B_1 through E_2 = 0, fifth condition A_2 through D_2 = 0, E_2 = 1). The sixth condition, the idle condition, occurs when all bit states are equal to 0. Once the register is in the idle condition, recycling can only occur as a function of the logic control inputs. The logic control inputs (see Figure 31) are (6), (D), (L), (N), (15), and (B). Inputs (L), (N), and (15) determine manual mode operation and inputs (6), (D), and (N) determine sample mode operation. Note, in Figure 32, the state of (B) is presently fixed to logic 1. If, in the future, an external source of digital data is to be recorded, control input (B)

can be used for that purpose.

In the manual mode, depression of any manual character key causes a 1 to 0 transition of input (15), the clock input of flip-flop 25. This transition causes the output state, ($\overline{Q}$), of the flip-flop to become 0. Hence, one of the inputs to NAND gate 23 is 0. (The other inputs to this gate, (D), (6), and (B), have states equal to 1 in the manual mode.) This 0 input forces the serial input of the idling shift register to become 1. The next clock pulse to the shift register causes the state of its first bit output to become 1. Since one of the shift register bits is now 1, output (H) will become 1, and flip-flop 25 is cleared. This flip-flop is cleared because (L) = (H) (connected together at the board socket in Figure 32), and the other input, (N), to NOR gate 21 is 0 in the manual mode. Subsequent clock pulses into the shift register will right-shift this 1 bit until the register completes its cycle (all bit states are 0). Output (H) then returns to 0, and retriggering of flip-flop 25 is now possible. The system is now ready to record a new manual character.

In the sample mode (N) is 1 and the clear input to flip-flop 25 is 0. This is done to prevent accidental triggering of the flip-flop, thereby holding $\overline{Q}$ to 1. Hence, only control inputs (6) and (D) are used to recycle the counter in this mode. Control input (D) is used for the recording of scan separation characters and time data. Control input (6) is used when recording each input channel voltage. For each character written on the magnetic tape, the Master Sequencer must complete one cycle.

Hence, for each scan, (D) has a state equal to 0 for seven sequencer cycles (two scan separation characters and five characters of time) and then it returns to state equal to 1. The first channel voltage is then encoded. When the encoding is complete (6) becomes 0 and remains 0 for five sequencer cycles (five voltage data characters). Subsequent 1 to 0 transitions of (6) occur for each channel voltage that is to be recorded. After the last channel is recorded, (D) = (6) = 1 and the shift register idles until the next scan begins.

The Master Sequencer outputs have been described only in terms of their defining equations. The use of these outputs will be described in later sections as inputs to the other sequencing circuits.

6.4.7 The Time Sequencer

The Time Sequencer, Board #3, provides the sequential outputs required for the parallel to serial conversion of time BCD data. Outputs from this board also provide an enabling command to the BCD coupler, Board #7, and a command that initiates voltage data recording. This board enables the feedback loop in the Master Sequencer causing it to recycle five times. The pulsed outputs from C_2 of the Master Sequencer are used as clock inputs for the Time Sequencer. The circuitry and the sequential operation of the Time Sequencer is discussed in the following paragraphs. Figures 33, 34 and 35 aid in this discussion.

Like the Master Sequencer, the Time Sequencer utilizes a five-bit shift register, device 35 in Figure 34, to provide sequential outputs. These outputs can be defined solely in

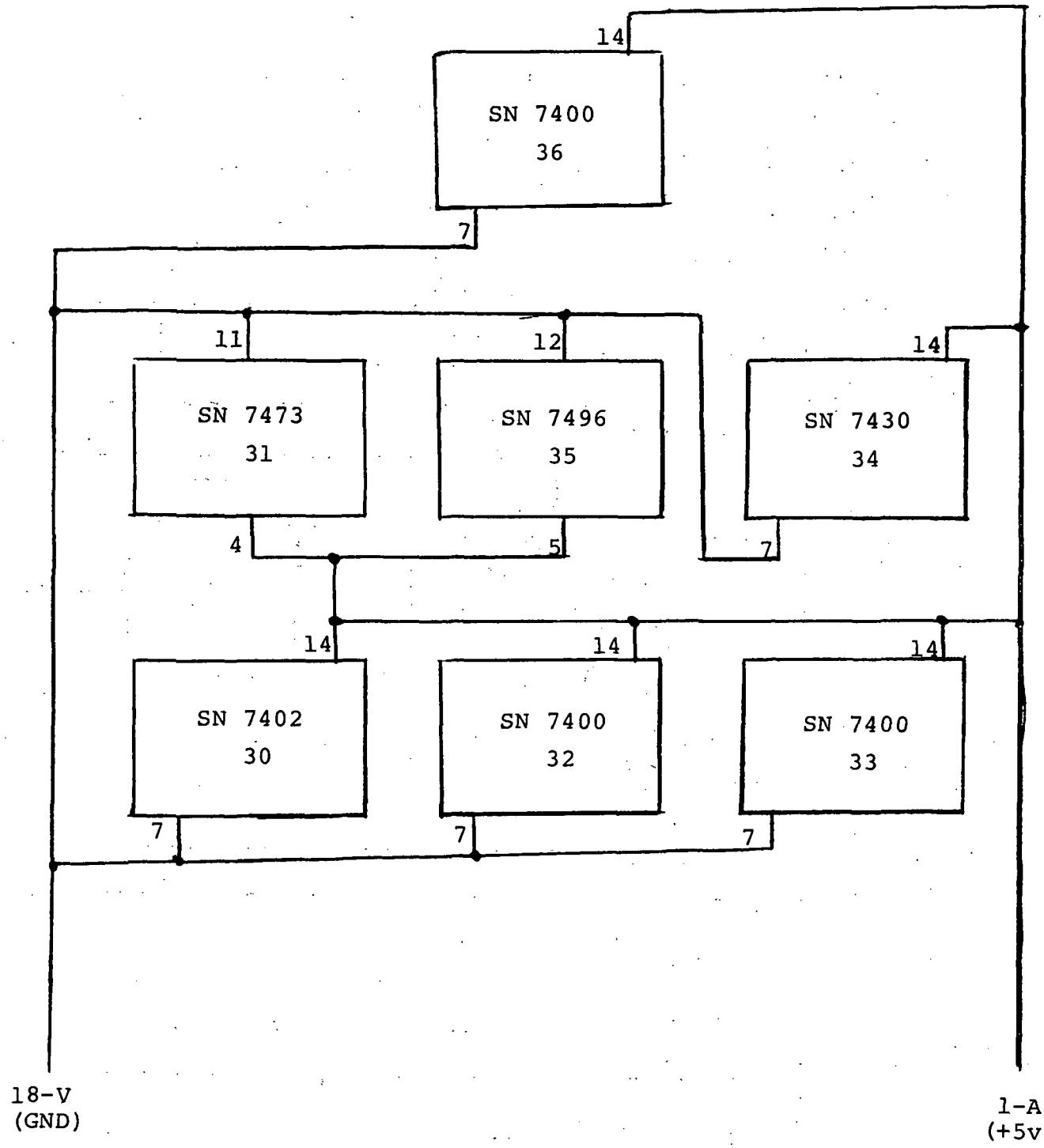


Figure 33. The Time Sequencer - Power Wiring and Device Location Diagram

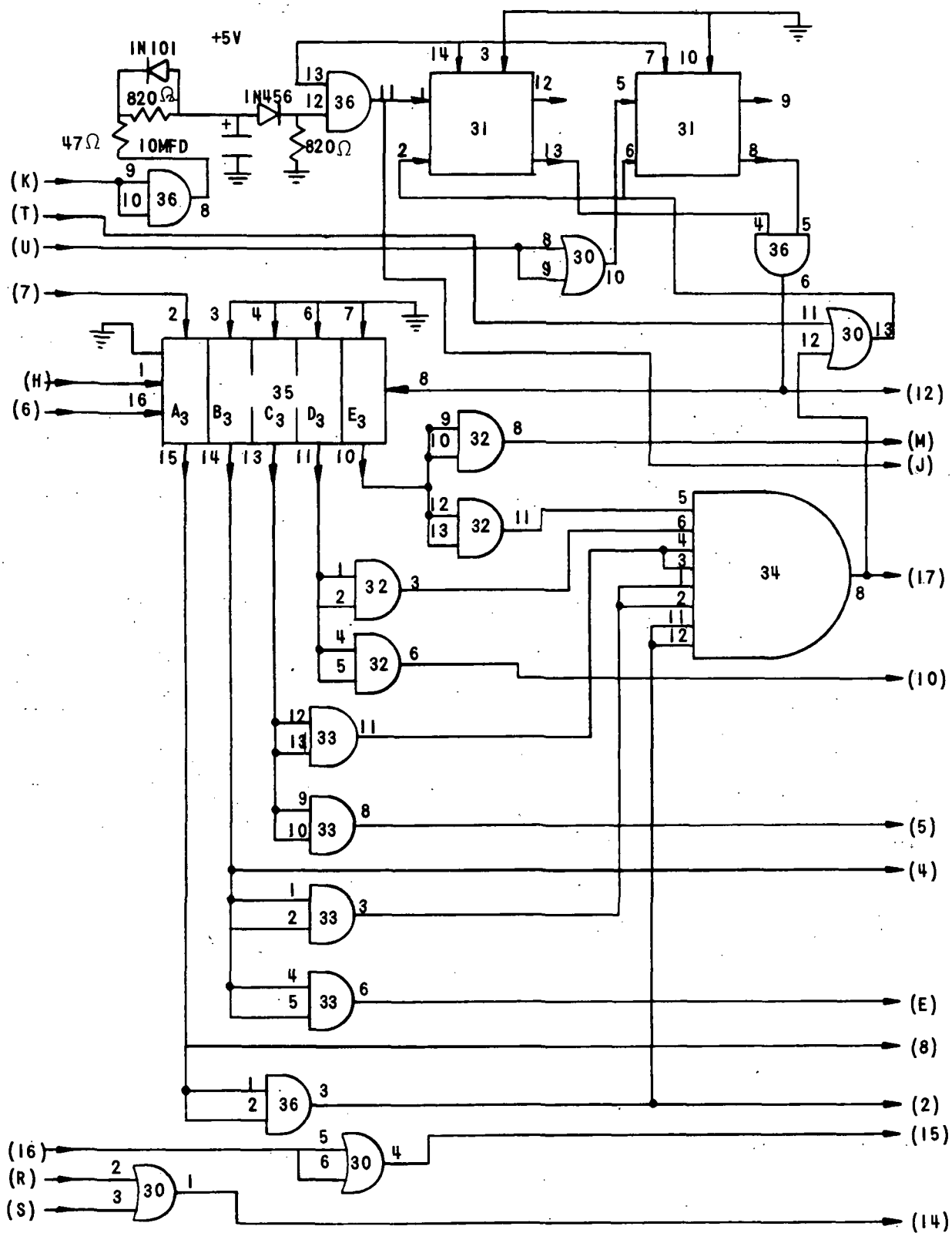


Figure 34. The Time Sequencer Logic Schematic

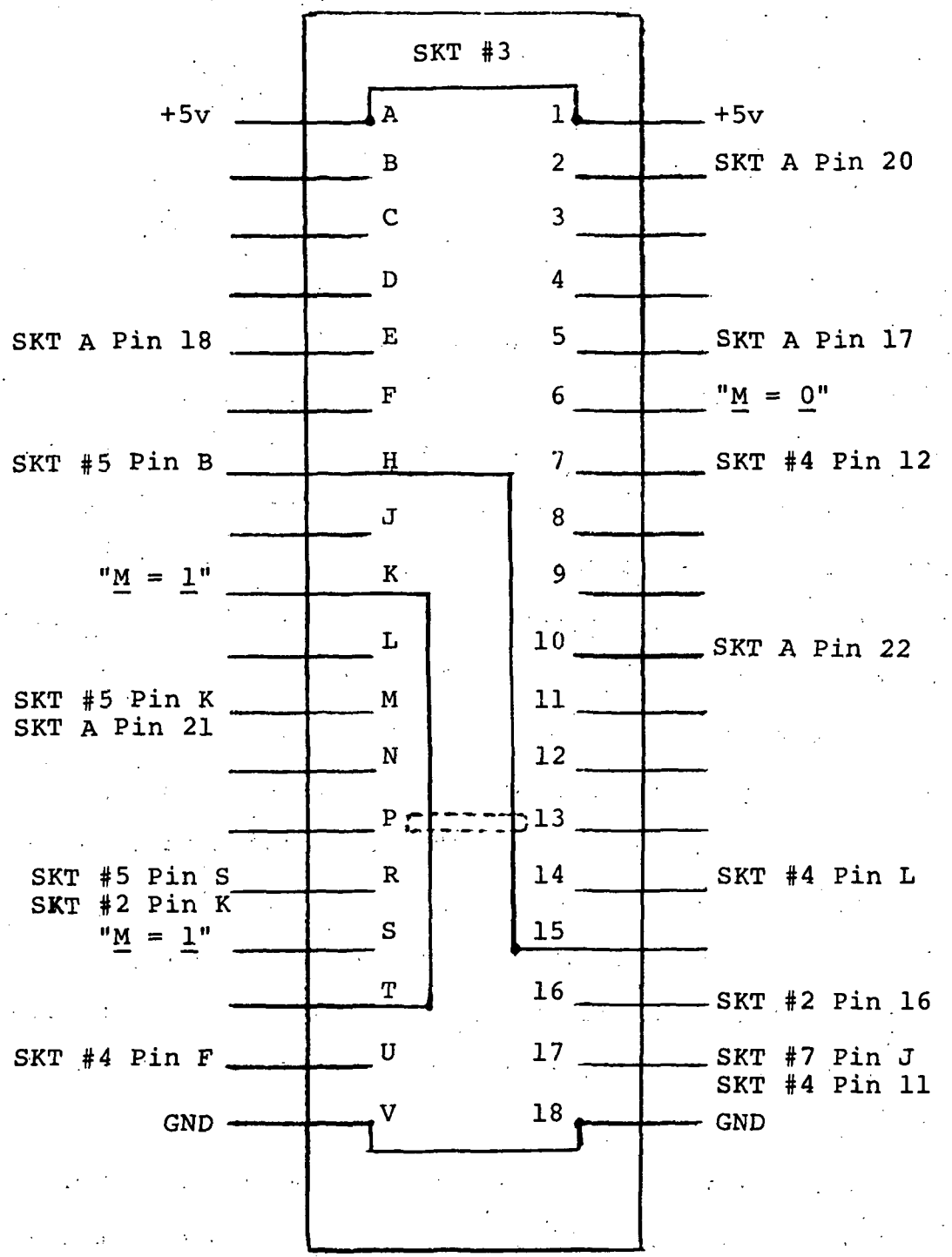


Figure 35. Connections to the Time Sequencer Socket

terms of the shift register's bit outputs, A_3 through E_3, (analogous to A_2 through E_2 for the Master Sequencer). These output equations are:

$$\underline{(8)} = \underline{A_3} \qquad \underline{(E)} = \overline{\underline{B_3}}$$

$$\underline{(4)} = \underline{B_3} \qquad \underline{(5)} = \overline{\underline{C_3}}$$

$$\underline{(17)} = \underline{A_3} \vee \underline{B_3} \vee \underline{C_3} \vee \underline{D_3} \vee \underline{E_3} \qquad \underline{(10)} = \overline{\underline{D_3}}$$

$$\underline{(2)} = \overline{\underline{A_3}} \qquad \underline{(M)} = \overline{\underline{E_3}}$$

The outputs (2), (E), (5), (10), and (M) provide the ten hour through ten second commands for the parallel to serial conversion of time data in the digital clock. The functions of these outputs have been presented in Section 6.2.4. Additionally, (M) initiates the system's processing of voltage data. This latter function will be discussed in Section 6.4.9. Output (17) performs two functions. First, it recycles the Master Sequencer when time is to be recorded. This output is connected to input (11), a NOR gate input, on Board #4. The output of this gate (K), is connected to the control input (D) of the Master Sequencer (one of the feedback loop logic control inputs). $\underline{(D)}$ is $\underline{0}$ when $\underline{(17)}$ is $\underline{1}$. (Other logic on Board #4 also affects (D).) The second function of (17) is the enabling of the BCD time outputs from the digital clock. This function will be discussed in Section 6.4.11.

The four inputs that are related to the sequencing operations of the Time Sequencer will be first discussed as to the function they perform in the Time Sequencer. These inputs and the previously defined outputs will then be used to describe the Time Sequencer in its sequential operation.

The four inputs are (K), (U), (7), and (16). Input (K), connected to "M=1", provides for the recording of time on the first scan of a new tape. If time is recorded on every scan, this input is redundant. When the system is switched from the manual mode to the sample mode, (K) clocks a flip-flop, device 31, causing pin 8, device 35, to become 1. Input (U) determines if time is to be recorded on a particular scan. If (U) makes a 0 to 1 transition at the beginning of a scan, time will be recorded. The transition of (U) clocks the other flip-flop, device 31, again causing pin 8, device 35, to be equal to 1. The present system format requires that time is to be recorded on every scan. Hence, input (U) is connected to the digital clock's sample command output. Inputs to (K) and (U) determine that time will be recorded at some interval during the scan. Where in the scan it is actually recorded is determined by input (7). This input becomes 1 after the scan separation characters are recorded. This is discussed in detail in Section 6.4.8. To start time sequencing operations, both conditions, pin 8 equal to 1 and (7) equal to 1, must exist simultaneously. This will load a 1 into the shift register. This 1 can then be right-shifted in the register by the clocking of the input (H). Input (H) is connected at the socket to output (15). This output is the inverse of input (16). Input (16) is the $\overline{C_2}$ output of the Master Sequencer. Hence, the equation for (H) is:

$$(H) = \overline{(16)} = \overline{\overline{C_2}} = C_2$$

and right shifting occurs when C_2 becomes 1.

The discussion of the sequential operation of the Time Sequencer begins with its shift register, 35, in the idle state (all bits equal to 0), and flip-flops, 31, in their cleared states with clear inputs equal to 1. At the beginning of a scan, the sample command output from the digital clock becomes 1. This means that (U) becomes 1. Hence, pin 8 of shift register 35 is 1. Also the Master Sequencer is cycled for the recording of the scan separation characters as described in Section 6.4.8. While the scan characters are recorded, (7) is 0, and the clock pulses at (H) have no effect on the shift register's output states (all states are 0). Two milliseconds after the second scan separation character is recorded (7) becomes 1 (when D_2 becomes 1). A 1 will now be loaded into shift register 35, and A_2 is equal to 1. Since one of the outputs of the shift register is 1, the output (17), of NAND gate 34, is 1 and flip-flops 31 are cleared. This returns pin 8 of the shift register to 0. Parallel to serial conversion of the ten hour BCD data is now performed, (2) is equal to $\overline{A_3}$ which is equal to 0. Output (17) is now used as a control input for the Master Sequencer. (Control input (D) of the Master Sequencer is 0 when (17) is 1.) The Master Sequencer recycles, recording the ten hour character when B_2 becomes 1. When C_2 becomes 1, the time sequencer shift register right-shifts a single 1 from A_3 to B_3. Parallel to serial conversion of the hour BCD data is now performed. Subsequent recycling, the recording of a time digit, and the right-shifting of register 35 continues until the last time digit is recorded. At this time, E_3 will be equal to 1 and B_2 is 1.

On the next clock pulse of the Master Sequencer, C_2 becomes 1, causing all bit states of register 35 to become 0. When all states of the register are 0, (17) becomes 0, and the cycling of the Master Sequencer is no longer controlled by control input (D). The flip-flops, 31, again have their clear inputs set equal to 1, and the Time Sequencer stays in this idle state until the start of the next scan.

In the manual mode no time sequencing operations are performed. Clock and preset inputs to the Time Sequencer are disabled by inputs (T) and (16). (T) is 1 and (16) is 0, causing all clear inputs on devices 31 and 35 to be 0.

The remaining NOR gate, part of device 30, on the Time Sequencer Board is not used in the Time Sequencer logic, but its output equations will be given here for completeness.

$$(14) = \overline{A_2 \vee B_2} \quad \text{. . . in the sample mode}$$

$$(14) = 0 \quad \text{. . . . . in the manual mode}$$

6.4.8 The Scan Separation Character Generator

The Scan Separation Character Generator, Board #4, provides the sequential outputs for the encoding of the scan separation characters. This board also provides outputs that start the Time Sequencer and stop the Voltage Data Sequencer (Section 6.4.9). This board enables the feedback loop in the Master Sequencer, causing it to cycle two times. The pulsed outputs from D_2 of the Master Sequencer are used as clock inputs for the shift register on this board. The outputs and inputs of this board will be defined below with the aid of Figures 36, 37, and 38. After they are defined, they will be used to

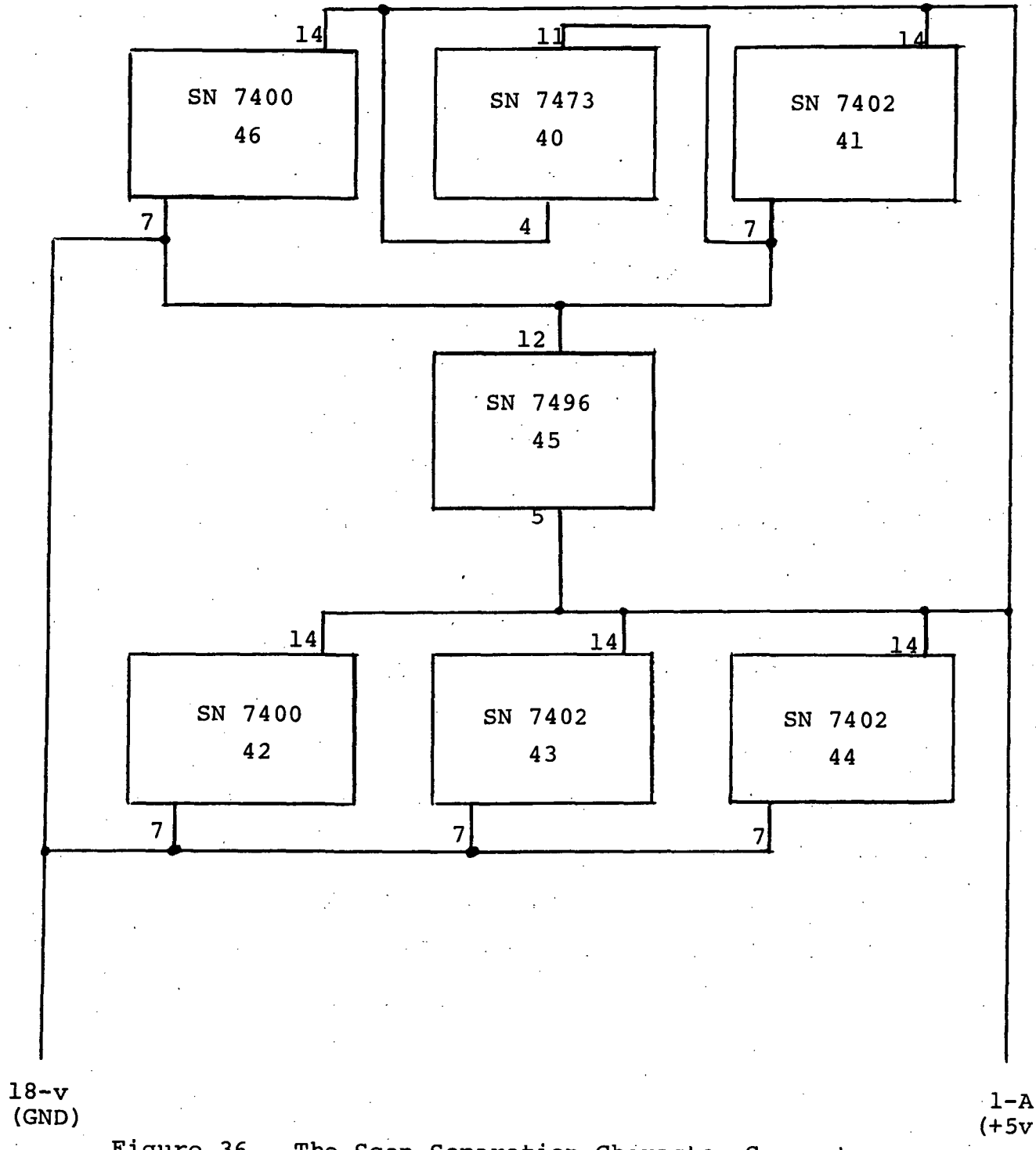


Figure 36. The Scan Separation Character Generator - Power Wiring and Device Location Diagram

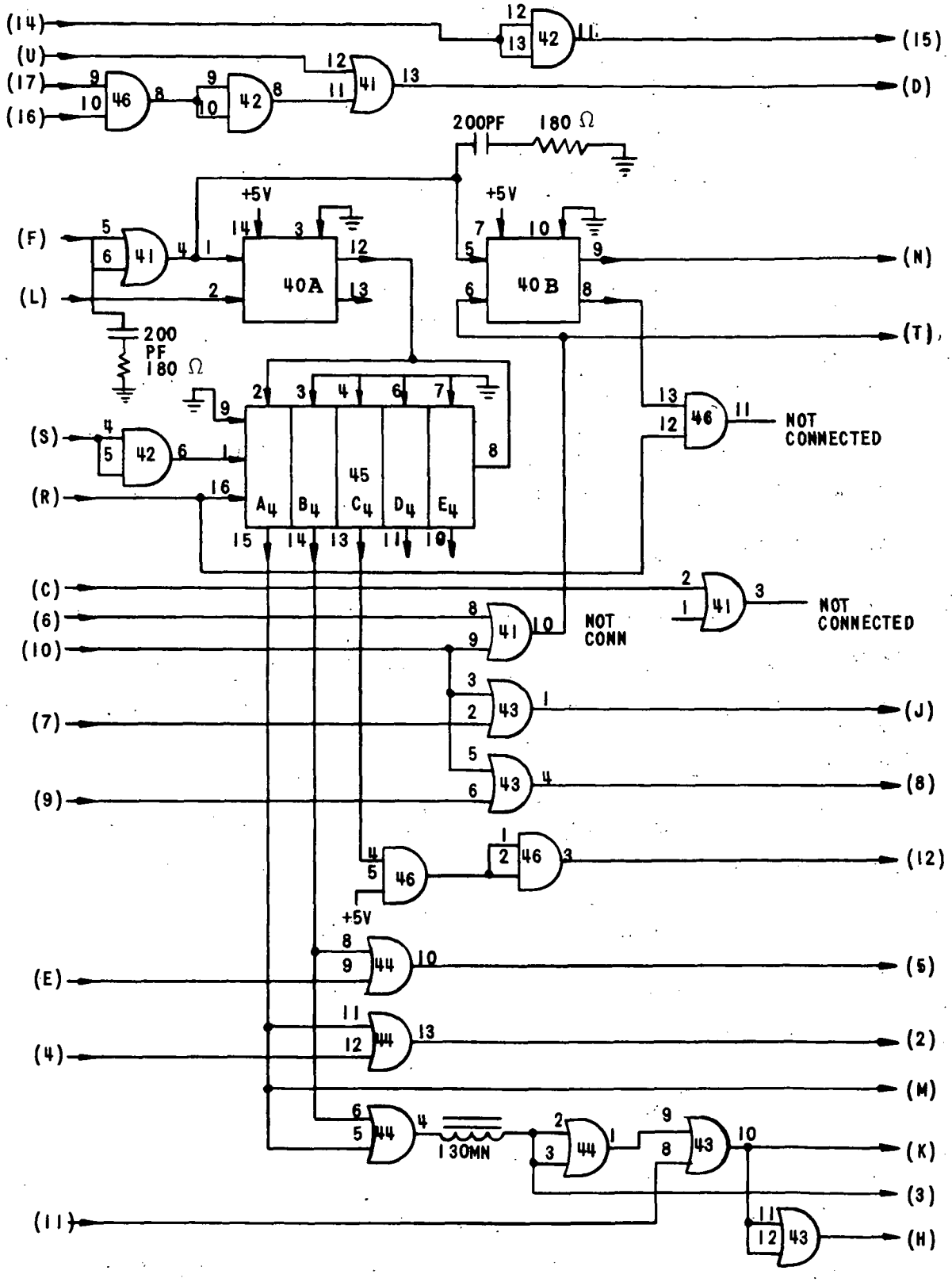


Figure 37. The Scan Separation Character Generator Logic Schematic

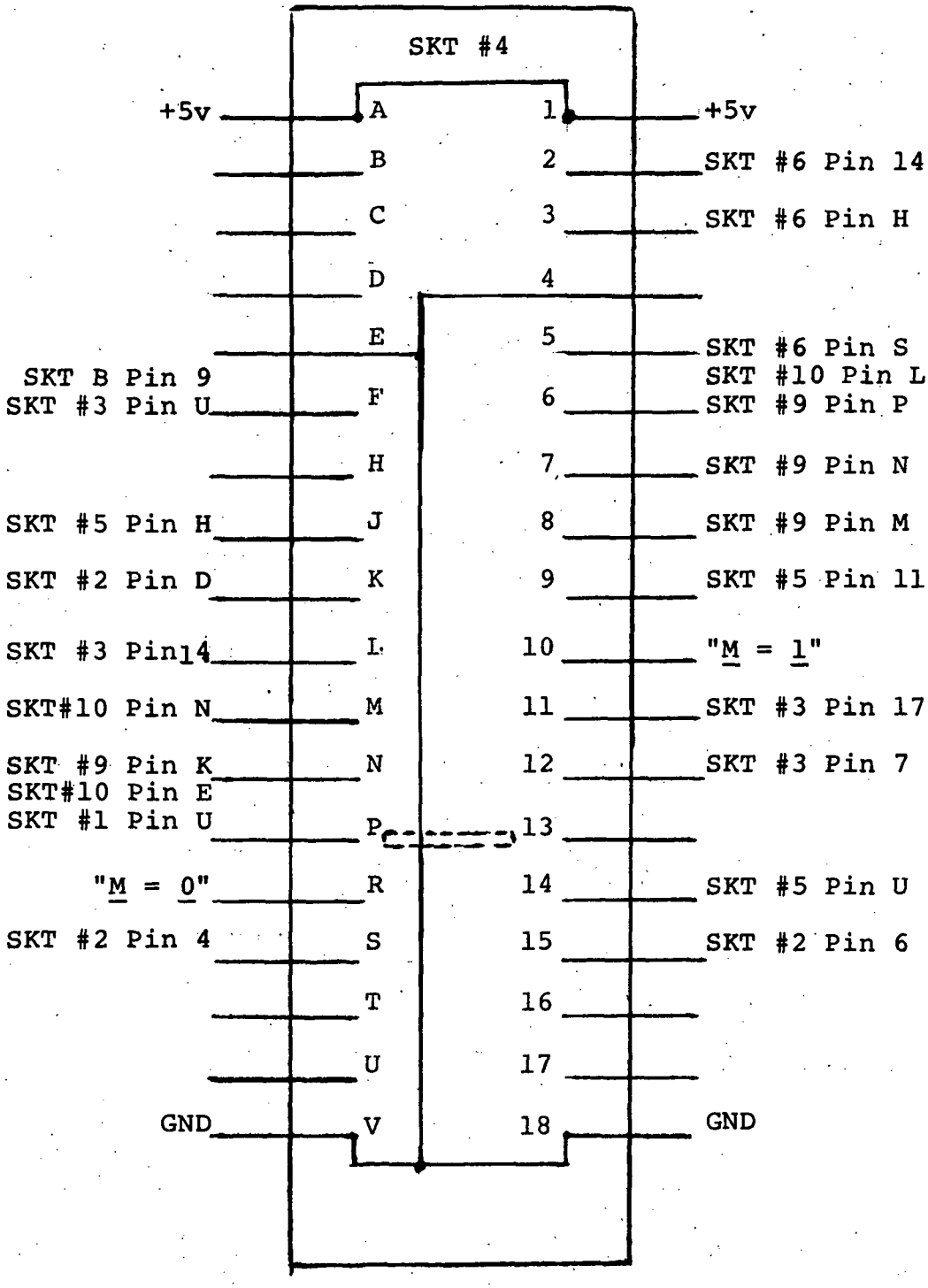


Figure 38. Connections to the Scan Separation Character Generator Socket

describe the generator's sequential operations.

A five-bit shift register, device 45, provides the sequential outputs associated with the recording of the scan separation characters. However, only the first three bit outputs, A_4 through C_4, are used. The outputs that can be expressed in terms of these shift register outputs are:

$$\underline{(M)} = \underline{A_4}$$

$$\underline{(2)} = \underline{A_4} \qquad \underline{(5)} = \overline{\underline{B_4}}$$

$$\underline{(12)} = \underline{C_4} \qquad \underline{(K)} = \overline{\underline{A_4} \vee \underline{B_4} \vee \underline{(11)}}$$

$$\underline{(3)} = \underline{A_4} \vee \underline{B_4} \qquad \underline{(H)} = \underline{(\overline{K})} = \underline{A_4} \vee \underline{B_4} \vee \underline{(11)}$$

The outputs (5), (2), (3), and (M) are used to command the EBCDIC Encoder to output the EBCDIC level states for the two scan separation characters. Output (12) is used to initiate the Time Sequencer through its input (7). Output (K) is connected to control input (D) of the Master Sequencer. This output is 0 when either scan separation characters or time data are to be recorded (see Section 6.4.7). (H), the inverse of (K), is not used.

One other output, (N), connected to flip-flop 40B is used for sequential converter operations that occur after all of the voltage channels have been recorded. Output (N) stops the Voltage Data Sequencer after a preset number of voltage channels has been recorded. This output also provides a clock input pulse for the IRG counter on the Recorder Pulse Generator board and provides a clear input for the write error circuitry on the Channel Nine through Sixteen Selector board. The remaining outputs on this board perform logic functions associated with other boards.

The inputs associated with the above outputs are (L), (S), (F), (6) and (11). Input (L) is the clear input to flip-flop 40A. This flip-flop is cleared by the first cycle of the Master Sequencer. From Section 6.4.7, $\underline{(L)}$ is equal to $\overline{\underline{A_2} \vee \underline{B_2}}$ in the sample mode. Input (S) provides the clock input for shift register 45. The equation for this input is:

$$\underline{(S)} = \overline{\underline{D_2}}$$

(Note, however, that the shift register input is actually $\overline{\underline{(S)}} = \overline{\overline{\underline{D_2}}} = \underline{D_2}$.) Input (F) clocks flip-flops 40A and 40B, initiating sample mode sequencing. This input is pulsed by the sample command output from the digital clock. Input (6) is used to clear flip-flop 40B, changing the state of output (N), to stop voltage data sequencing.

A sequential description of the Scan Separation Character Generator follows. The Master Sequencer is idling, shift register 45 is idling, and flip-flops 40A and 40B are in their cleared states with clear inputs equal to 1. That is, the sequential converter has completed a scan and it is waiting for a sample command from the digital clock. A 0 to 1 transition of the sample command output clocks flip-flops 40A and 40B. Output (N) becomes 1. This is a necessary, but not sufficient, condition for voltage data sequencing. Pin 2 and pin 8 of shift register 45 become 1 loading a 1 into the first bit of the shift register. That is, $\underline{A_4}$ is 1. Outputs (2) and (3) are equal to 0, and output (M) and (5) are 1. These output states command the EBCDIC Encoder, Section 6.4.10, to output level states for the first scan separation character. Output

(K), (K) now equal to 0, initiates the first cycle of the Master Sequencer. When A_2 of the Master Sequencer becomes 1 flip-flop 40A is cleared by input (L). Hence, only a single 1 bit will be right-shifted in the register. The first scan separation character is recorded when B_2 of the Master Sequencer becomes 1. Nothing further happens until D_2 becomes 1. At this time, the A_4 bit is right-shifted to B_4 (B_4 = 1, A_4 = 0). Outputs (3), (5), and (M) are equal to 0, and output (2) is 1. The EBCDIC Encoder now outputs the level states for the second scan separation character. (F) remains 0 and the Master Sequencer recycles. When B_2 becomes 1 the second scan separation character is recorded. On the next clock pulse to shift register 45, C_4 becomes equal to 1 (A_4 = 0, B_4 = 0). Output (M) is 0, and outputs (2), (5) and (3) are equal to 1. These output states remain unchanged throughout the rest of the scan. These states condition the EBCDIC Encoder to recognize future BCD data inputs as numeric data. Output (12) becoming equal to 1 will load a 1 into the first bit of the Time Sequencer shift register (see Section 6.4.7). Since (K) is equal to $\overline{A_4 \vee B_4 \vee (11)}$ and A_4 and B_4 both now have states equal to 0, (K) will be equal to $\overline{(11)}$. The Master Sequencer's feedback loop is now under the control of the Time Sequencer. Further right-shifting of shift register 45, while time is being recorded, has no effect on the system's sequential operation. After time is recorded shift register 35 returns to its idle state. Output (K) then becomes 1 (It remains in this state until the next scan is begun.). Output (H) also becomes 0 at this time to enable voltage data

sequencing. Voltage data will now be recorded. After the preset number of voltage channels has occurred a 0 to 1 transition of input (6) will occur. This transition provides an output to the IRG counter via output (T), and it clears flip-flop 40B. When flip-flop 40B is cleared, (N) becomes equal to 0. Hence, a necessary condition for voltage data sequencing is no longer satisfied, and the system has now completed recording data for this scan. Output (6) is returned to (0) to allow retriggering of flip-flop 40B. Since the Master Sequencer is idling, input (L) is 0, and flip-flop 40A is ready to accept new sample commands from the digital clock.

In the manual mode the Scan Separation Character Generator is effectively disabled. Inputs (L) and (R) are 0, clearing flip-flop 40A and shift register 45. Input (10) is 1, clearing flip-flop 40B.

The remaining logic functions on this board are not related to other functions on this board. Their outputs are defined in terms of board inputs, but their use will be described as they are required in the following sections. These equations are:

$$(15) = \overline{(14)}$$

$$(J) = \overline{(7)} \quad \text{. . . . . in the sample mode}$$

$$(J) = 0 \quad \text{. . . . . in the manual mode}$$

$$(8) = \overline{(9)} \quad \text{. . . . . in the sample mode}$$

$$(8) = 0 \quad \text{. . . . . in the manual mode}$$

6.4.9 The Voltage Data Sequencer

The Voltage Data Sequencer, Board #5, provides sequential outputs to the Voltage Data Parallel to Serial Converter, Section 6.4.12, and to the EBCDIC Encoder, Section 6.4.10. The logic on this board determines the DVM's mode of operation, and it enables the Master Sequencer to recycle five times after each analog voltage has been converted to digital form. The outputs, inputs, and operation of the Voltage Data Sequencer will be discussed in this section with the aid of Figures 39, 40 and 41.

A five-bit shift register, device 55, provides most of the sequencer's outputs. The bit outputs of this shift register, shift register #5, are A_5 through E_5, as shown in Figure 40. The Voltage Data Sequencer outputs that can be defined in terms of these bit outputs are:

$\underline{(C)} = \underline{A_5}$ $\qquad$ $\underline{(T)} = \overline{\underline{(F)} \vee \underline{(U)}}$

$\underline{(8)} = \underline{B_5}$ $\qquad$ $\underline{(3)} = \overline{\underline{A_5}}$

$\underline{(10)} = \underline{(C_5)}$ $\qquad$ $\underline{(9)} = \overline{\underline{B_5}}$

$\underline{(E)} = \underline{E_5}$ $\qquad$ $\underline{(4)} = \underline{(16)} = \underline{D_5}$

$\underline{(U)} = \underline{A_5} \vee \underline{B_5} \vee \underline{C_5} \vee \underline{D_5} \vee \underline{E_5}$ $\qquad$ $\underline{(R)} = \overline{\underline{E_5}}$

$\underline{(J)} = \overline{\underline{D}} \vee \underline{(U)} = {}^{*}\overline{\{\underline{(14)} \cdot \underline{(5)} \vee \underline{(17)}\}} \vee \underline{(U)}$

*Note, on diagram 41, (D) is connected to (15)

The outputs (C) and (3) are connected to the EBCDIC Encoder. $\underline{(C)}$ equals $\underline{1}$ and $\underline{(3)}$ equals $\underline{0}$ enables encoding of the Voltage polarity-range bit (see Section 6.4.10). The outputs (8), (10), (4), and (E) are the command inputs for the Voltage Data Parallel

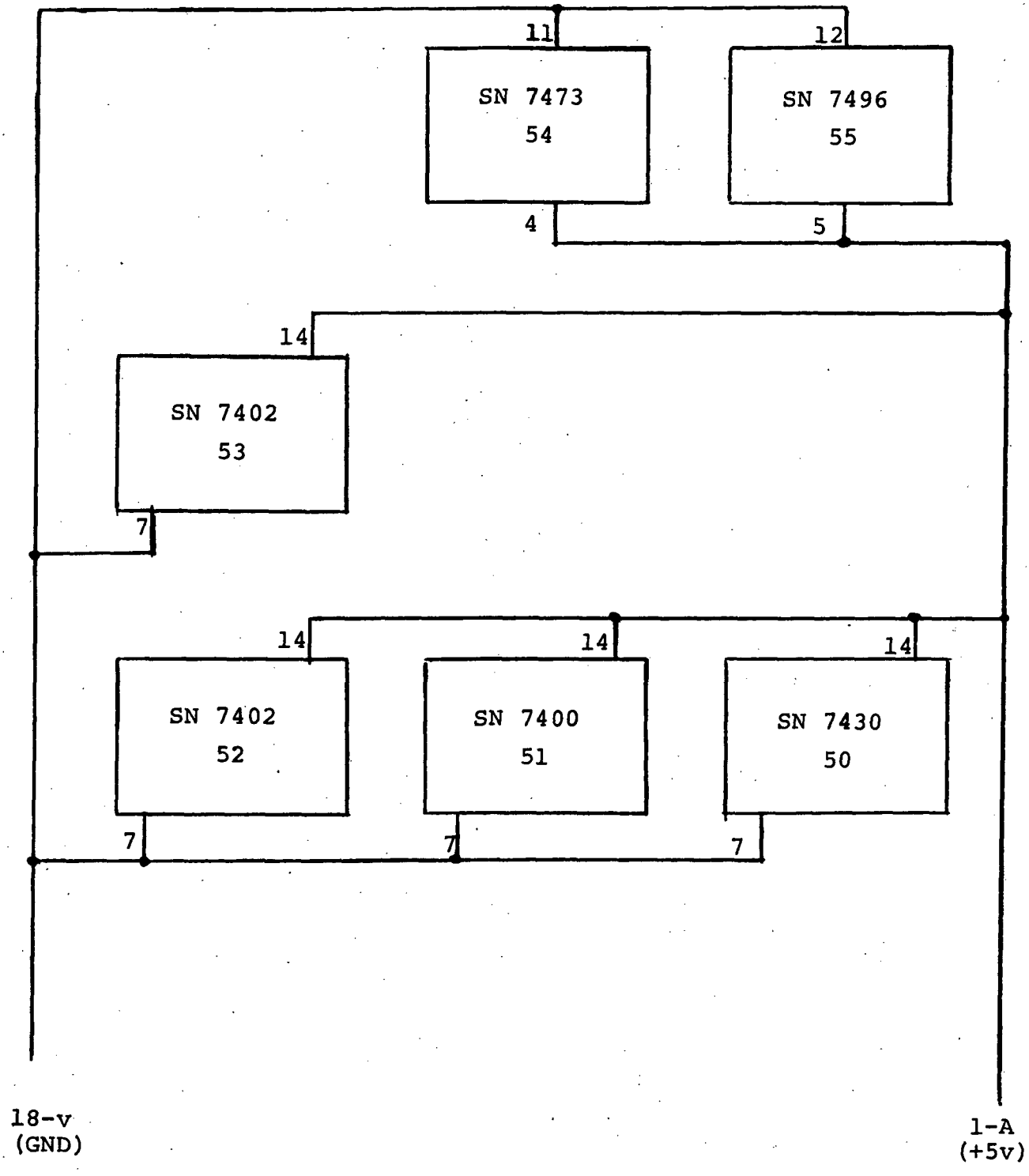


Figure 39. The Voltage Data Sequencer - Power Wiring and Device Location Diagram

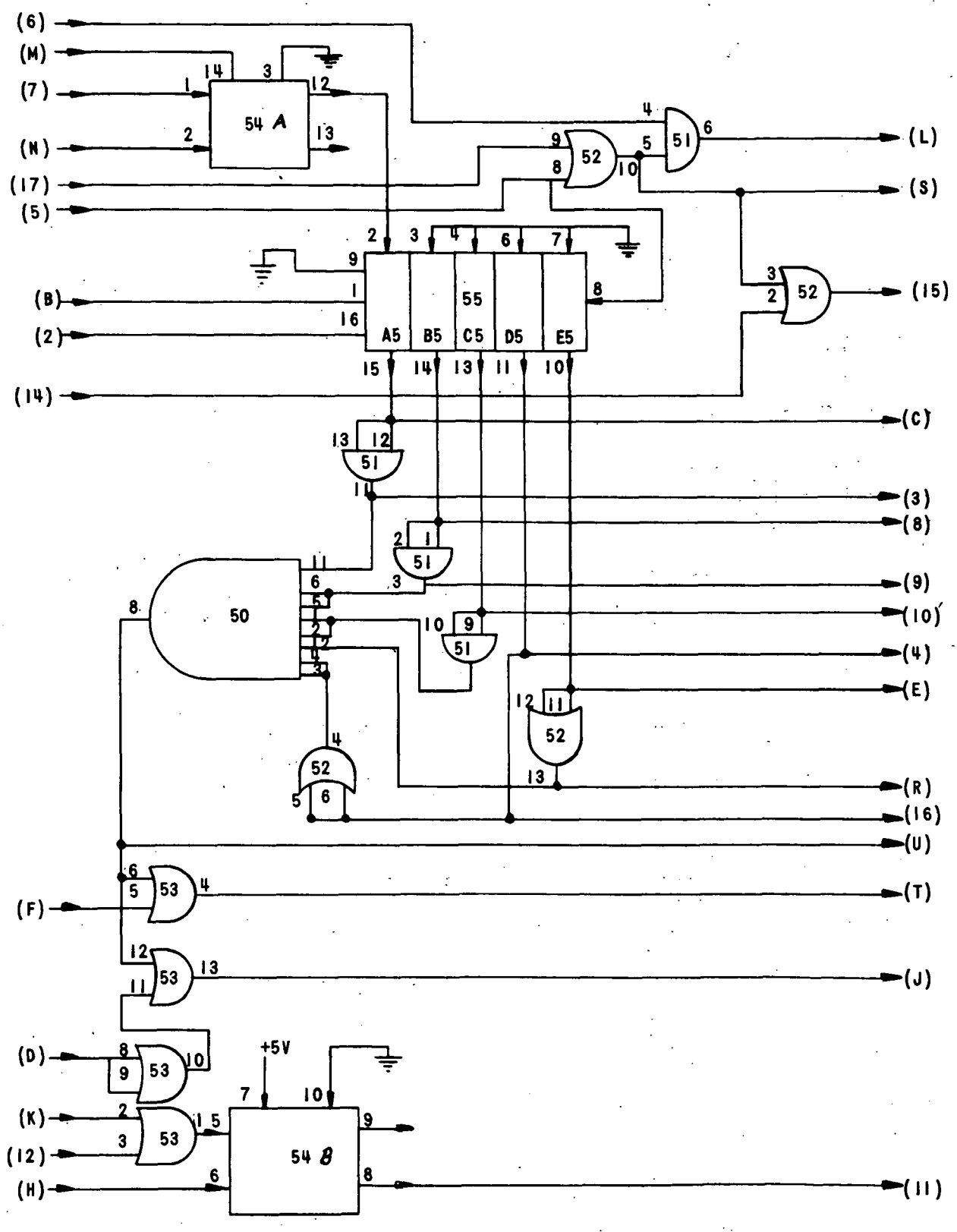


Figure 40. The Voltage Data Sequencer Logic Schematic

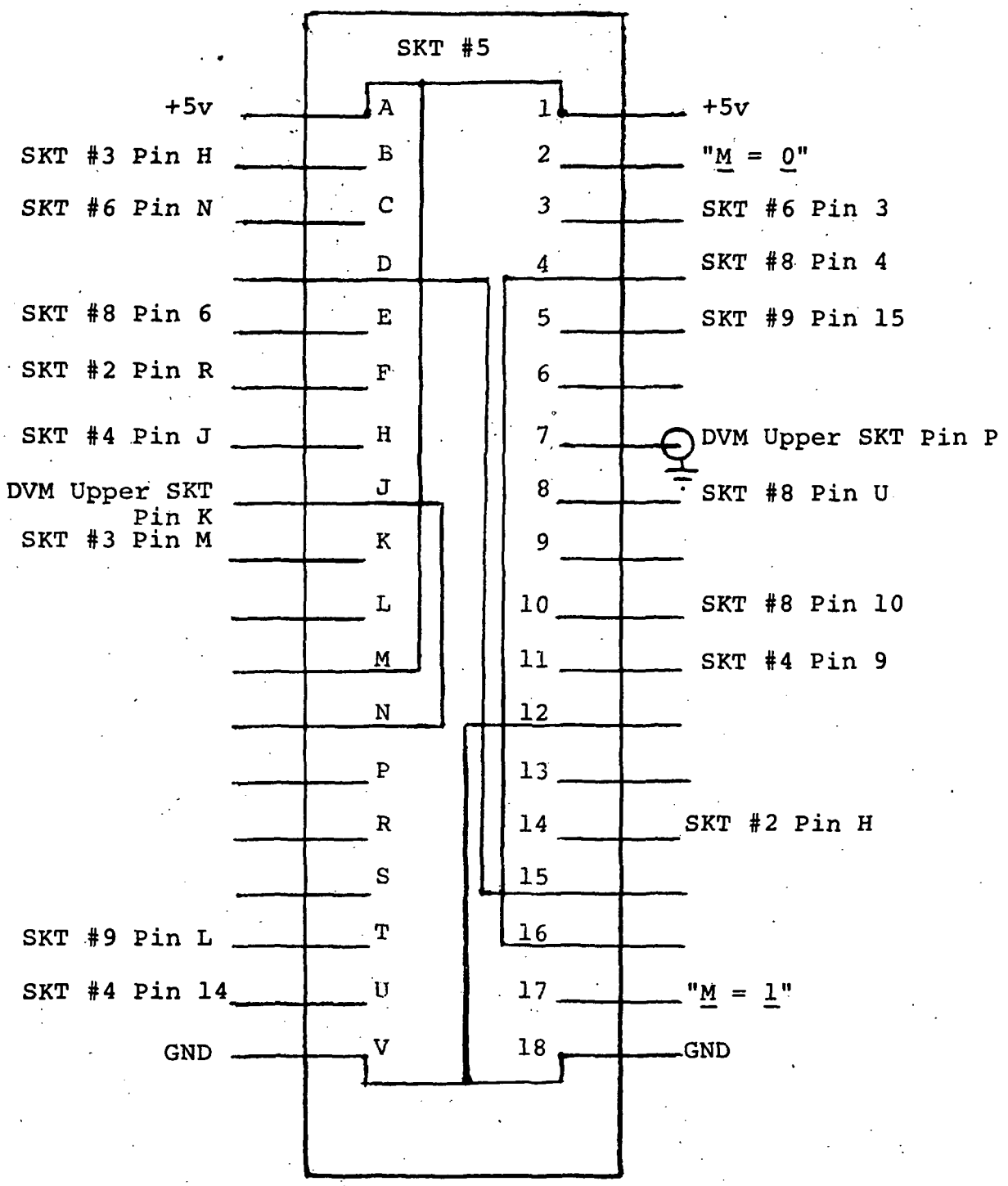


Figure 41. Connections to the Voltage Data Sequencer Socket

to Serial Converter discussed in Section 6.4.12. Output (U) is used to control the recycling of the Master Sequencer. This output, inverted by a NOR gate on Board #4, determines the state of the logic control input (6) of the Master Sequencer. The control input condition, (6) equal to 0, that causes recycling of the Master Sequencer is satisfied when any one of the shift register's #5 bit states is 1. Output (T) provides the clock pulse input to the shift registers on the channel selector boards, Board #9 and Board #10. These boards are discussed in Section 6.4.13 and 6.4.14. Output pulses at (T) are provided whenever D_2 becomes 1, and all of the shift register's #5 bits are 0 [(U)= 0]. Output (J) is connected to the DVM's hold command input and to the clear input of flip-flop 54A. The condition that (J) equals 1 enables the A/D conversion of an analog voltage. When (J) is (0), the DVM's outputs are held.

Of the remaining Voltage Data Sequencer outputs, only output (11) is used. The inverse of this output, the $\overline{Q}$ output of flip-flop 54B, is connected to the preset A input of the Channel One through Eight Selector shift register (see Section 6.4.13).

The inputs to the Voltage Data Sequencer that are associated with the shift register are (B), (2) and (5). The inputs to flip-flop 54A and B are (M), (7), (K), (12), (N), and (H). Input (B), the shift register's clock input, is connected to C_2. (B) is equal to C_2, and right-shifting of the register occurs when C_2 becomes equal to 1. Input (2), the shift registers clear input, clears the shift register in the manual mode and has no effect in the sample mode. Input

(5), the shift register's "preset enable" input, is connected to a flip-flop on Board #9. When (5) is 0, the Voltage Data Sequencer is disabled. Input (5) becomes 1 prior to the A/D conversion of the first channel voltage and remains 1 until a preset number of channels have been recorded. Input (7), the clock input for flip-flop 54A, is connected to the DVM's end of encode output. Since input (M) is fixed to 1, a 1 to 0 transition of input (7) will load a 1 into the shift register whenever input (5) is 1. Input (K) is one of the clock inputs to flip-flop 54B. This input is clocked by $\overline{E_3}$ of the time sequencer shift register. Since the other clock input, (12), is 0 (see Fig. 41), the flip-flop is triggered when E_3 makes a 1 to 0 transition. Input (H), the clear input of flip-flop 54B, is connected to Board #9 via a spare NOR gate on Board #4. Input (H) is equal to 0 when A_9, the first bit of the Channel One through Eight Selector shift register, has a state of 1.

Only two other inputs, associated with output (J), are presently used. Input (14) is connected to the Master Sequencer. In the sample mode when (14) is 1 (any Master Sequencer shift register bit = 1), output (J) is equal to 0. Input (17) is connected to "M=1", allowing the DVM to continuously encode in the manual mode.

The above defined outputs and inputs will now be used to describe the sequential operation of the Voltage Data Sequencer.

In the sample mode, voltage data sequencing operations begin after time data has been recorded. Prior to this time, flip-flop 54B and shift register #5 are in their cleared states

with clear inputs equal to 1. Input (5) is equal to 0; hence output (J) is 0, and the clear input of flip-flop 54A and the DVM's hold command input have states of 0. When the last time digit is recorded, (E_3) is 1, and (B_2) is 1. When C_2 becomes 1, E_3 makes a 1 to 0 transition, triggering flip-flop 54B. Output (11) becomes 0 loading a 1 bit into A_9. This 1 bit forces (H) to become 0, clearing flip-flop 54B. (Only a single 1 bit can exist in shift register #9.) No further triggering of this flip-flop occurs during the rest of this scan. When D_2 becomes 1, a clock pulse occurs at output (T). This clock pulse right shifts the 1 bit in A_9, and causes input (5) to become 1. (5) will remain 1 until the preset number of voltage channels is recorded. The control input (6) of the Master Sequencer is 1 [(U) = 0]; therefore, recycling of the Master Sequencer does not occur immediately after E_2 becomes equal to 0. When the Master Sequencer becomes idle, the First Analog Multiplexer connects the first voltage channel to the DVM's analog input. Input (14) is now 0 which forces (J) to 1. This output state commands the DVM to begin A/D conversion and allows flip-flop 54A to be triggered.

When the DVM's end of encode output makes a 1 to 0 state transition, flip-flop 54A is triggered, and loads a 1 into shift register #5. This 1 bit forces output (U) to 1. (J) then returns to 0 to hold the DVM's outputs and to clear flip-flop 54A. Output (C) equals 1 and output (3) equals 0, enabling the encoding of the voltage polarity-range character. The control input (6) of the Master Sequencer now has a state of 0, and the next clock pulse input to the Master Sequencer causes A_2 to become equal

to 1. When B_2 becomes 1, the polarity-range character is recorded. C_2 then becomes 1. This causes right-shifting of the 1 bit in shift register #5. (C) returns to 0; (3) returns to 1; and output (8) is 1 to initiate parallel to serial conversion of the DVM's thousands digit BCD output. When D_2 becomes 1, no clock pulse occurs at output (T); since (U) is 1. Sequential recording of the parallel to serial converter's BCD outputs, right-shifting of shift register #5, and parallel to serial converting of the next DVM digit, continues until all five voltage data characters are recorded (E_5 = 1 and B_2 = 1). When C_2 becomes 1, shift register #5 returns to its idle state, and (U) becomes 0. Output (J) remains 0 because a 1 bit still exists in the Master Sequencer shift register. A clock pulse occurs at (T) when D_2 becomes 1. This clock pulse causes right-shifting of the channel selector's shift register. When the Master Sequencer returns to its idle state, the second channel voltage is connected to the DVM, and (J) returns to 1. A new channel voltage is now encoded and recorded as described above. The cyclic operation of the Voltage Data Sequencer continues until a preset number of channels have been recorded. After the last character of the last voltage channel is recorded, the output (T) clock pulse forces (5) to become 0 (see Section 6.4.13 and 6.4.14). The DVM's hold command input remains 0. Therefore the DVM holds the reading of the last channel sampled until the first channel of the next scan is to be sampled.

In the manual mode, input (2) equals 0 to clear shift register #5. Input (17) equals 1, forcing the DVM's hold command input to assume a state of 1. This allows the DVM to continuously

encode its analog input voltage. In this mode, the DVM may be connected to any desired voltage channel. This is a desirable feature since it aids in system testing and DVM calibration.

6.4.10 The EBCDIC Encoder

The EBCDIC Encoder, Board #6, encodes special character commands and all serial BCD data into the EBCDIC representation of the alphanumeric character that is to be recorded on the tape. The encoder uses only arithmetic elements. Therefore, no sequencing operations are performed by its circuits. That is, ignoring propagation delays, its output states at time T are uniquely determined by its input states at this same time T. Since no input can change state until one millisecond after the encoder's outputs are recorded, digital storage is not required. (Recording occurs when B_2 becomes 1, and no input changes state until C_2 becomes 1.) Similarly, propagation delays do not effect the encoder's operation because all inputs have been preset since A_2 became 1, and they are not recorded until B_2 becomes 1. This two millisecond interval, (time between A_2 becoming 1 and C_2 becoming 1) is a direct result of using a multiple-output ring counter, the Master Sequencer described in Section 6.4.6, as the clock pulse source for all sequencing circuits.

The EBCDIC Encoder is described in the following paragraphs with the aid of Figures 42, 43 and 44. The encoder's outputs and their determining inputs are defined.

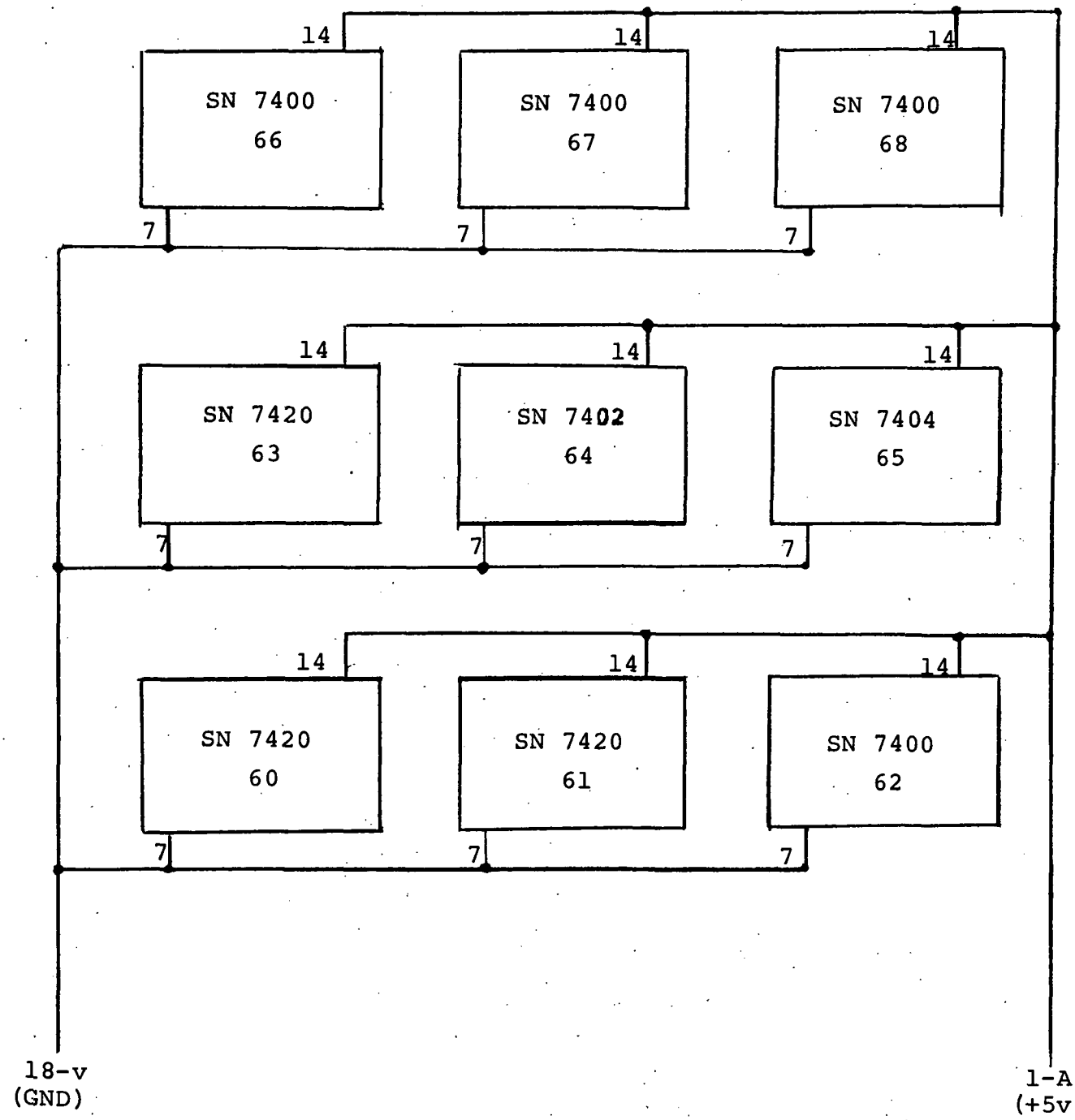


Figure 42. The EBCDIC Encoder - Power Wiring and Device Location Diagram

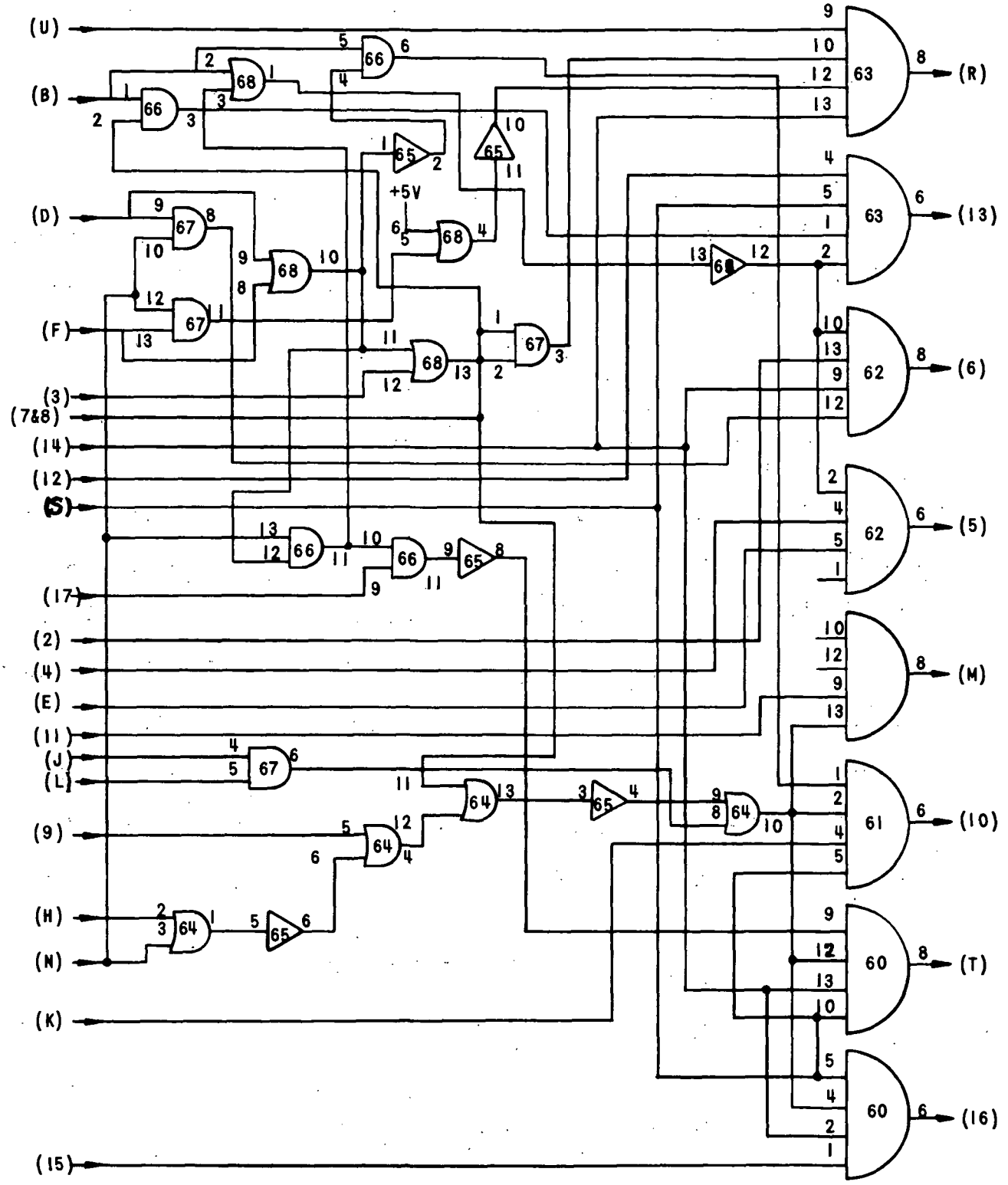


Figure 43. The EBCDIC Encoder Logic Schematic

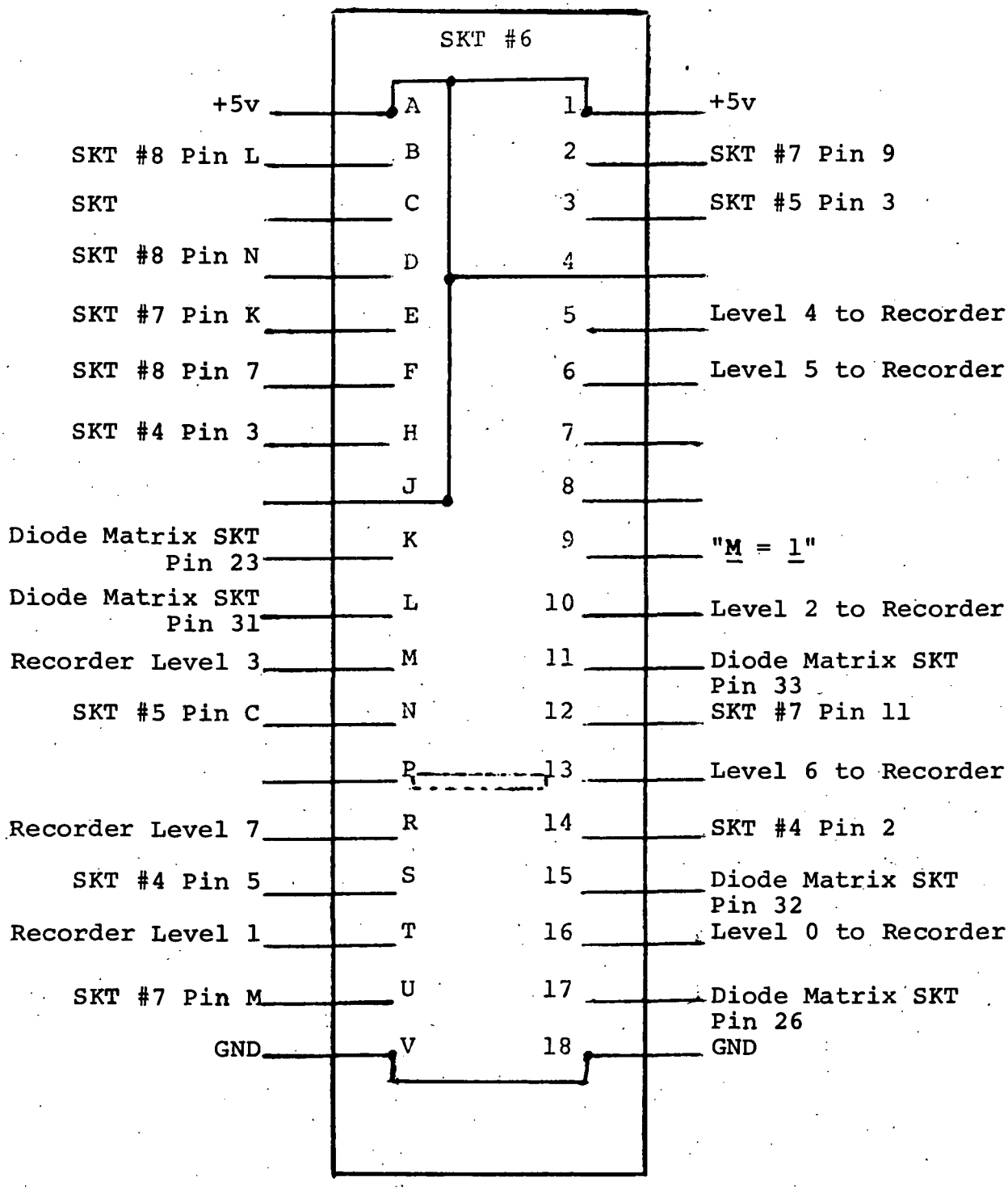


Figure 44. Connections to the EBCDIC Encoder Socket

The outputs of the EBCDIC Encoder are the eight EBCDIC levels, Level 0 through Level 7, that are the required inputs for the tape recorder (see Table 1 in Section 3.2). These outputs on Figures 43 and 44 are (16), (T), (10), (M), (5), (6), (13) and (R).

Inputs to the encoder are divided into two types. The first type are the serial BCD data inputs generated by the sequential converter. The second type are the special character inputs that command special encoding operations within the EBCDIC Encoder.

The BCD inputs are used primarily to record numeric data. These inputs (U), (12), (2), and (E) are the outputs from the BCD Coupler described in the next section (Section 6.4.11). To simplify encoder and coupler circuits, these inputs are the inverse of the BCD states. They are defined by the following equations:

$$\underline{(U)} = \overline{\underline{BCD\ 1}} \qquad \underline{(12)} = \overline{\underline{BCD\ 2}}$$

$$\underline{(2)} = \overline{\underline{BCD\ 4}} \qquad \underline{(E)} = \overline{\underline{BCD\ 8}}$$

Since most of the characters recorded on the magnetic tape are numeric characters whose BCD code representation is inputted into the encoder, it is important to understand the similarities between the BCD code and the EBCDIC code. These similarities are exploited to simplify the encoding circuitry. The BCD code is a four level code, BCD 8, BCD 4, BCD 2 and BCD 1, which is defined for decimal digits. Table 9 lists the BCD representation of these digits.

Table 9

The BCD Code

Digit	BCD Levels 8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Comparing this table with the numeric portion of the EBCDIC code table, Table 1 in Section 3.2, the following similarities are noted:

1. The EBCDIC Level 4 through Level 7 states are the same as the BCD 8, 4, 2, and 1 level states.
2. The EBCDIC Level 0 through Level 3 states are the same for all numeric characters (their states are all 1).

Thus, if the BCD inputs to the Encoder represent numeric digits, the following equations are used to define the encoder outputs.

Level 0 = 1 Level 1 = 1

Level 2 = 1 Level 3 = 1

Level 4 = BCD 8 Level 5 = BCD 4

Level 6 = BCD 2 Level 7 = BCD 1

Although the BCD code is not defined for other alphanumeric characters, the equivalence of BCD levels to EBCDIC level is exploited. For example, the inverse level outputs of the Diode Matrix are EBCDIC level outputs. However, $\overline{\text{Level 7}}$ through $\overline{\text{Level 4}}$ outputs are defined as the equivalent inverse BCD levels. They are inputted to the BCD Coupler as though they represented the BCD level states of numeric digits.

The functions of the special character inputs could be explained in terms of a set of eight output equations. For example, the output equation for Level 0 output state is given by:

$$\underline{(16)} = \overline{\underline{(15)} \cdot \underline{(14)} \cdot \underline{(5)} \cdot [\{\underline{(H)} \vee \underline{(N)} \vee \underline{(9)}\} \cdot \{\underline{(3)} \vee \underline{(F)} \cdot \underline{(D)}\} \cdot \underline{(L)}]}$$

However, such a presentation would present little insight into the system's encoding operations. Rather, the various inputs and their states for the sample and the manual modes of operation are listed in Tables 10 and 11. The effects of these inputs on the encoder's outputs are then discussed.

The effects of the inputs in Table 10 on sample mode encoding can best be described in the sequence in which the characters are recorded. When the first scan separation character is to be recorded, (U), (2), and (E) are 1. (H) is equal to 0, this signifies that the character to be recorded is a nonnumeric character. Thus, (H) equal to 0 disables encoder circuitry that normally causes Level 0 through Level 3 outputs to be 1. When (14) is 0 and (H) is 0, the outputs are determined by the following equations:

(16) = Level 0 = 1	(T) = Level 1 = 1
(10) = Level 2 = 0	(M) = Level 3 = 0
(5) = Level 4 = 0	(6) = Level 5 = 1
(13) = Level 6 = (12)	(R) = Level 7 = 1

If (12) is 0, a write error on the previous scan did occur, and the EBCDIC character "G" is outputted from the Encoder. If (12) is 1, a write error did not occur, and the character "E" is outputted. (The reader is advised to compare the output level states with those given in Table 1 for the "E" and "G" characters.) The circuitry that determines the state of (12) is discussed in the next section (6.4.11). When the second scan separation character is to be recorded (N) is 0, (H) is 0, (14) returns to 1, and all inverse BCD inputs are 1. The encoder then outputs the level states representing the EBCDIC character "S". Next, time is recorded. Since the five characters recorded are numeric digits, Level 0 through Level 3 outputs are 1. Level 4 through Level 7 are the BCD levels. The system now starts to record the voltage channels. The first voltage character for each channel voltage, the polarity-range characters, may (may not) be numeric. At this time (3) is 0, (N) is 1, and all inverse BCD inputs are equal to 1. This enables the circuitry associated with inputs (B), (D), and (F). The state of these three inputs then determine the EBCDIC character that the encoder outputs. (See Table 4, Section 3.3 for the compression code characters.) The remaining four characters of the voltage are numeric digits, and Level 0 through Level 3 outputs are 1. Level 4 through Level 7 are the BCD levels.

Table 10

The EBCDIC Encoder Inputs for Sample Mode Operation

Inputs	States	Remarks
(9)	$\underline{0}$	Connected to "$\underline{M}=\underline{1}$"
(15), (17), (K), (11), and (L)	$\underline{1}$	Diode Matrix outputs
(14)	$\underline{0}$ when $\underline{A_4} = \underline{1}$ $\underline{1}$ otherwise	Used to generate 1st scan separation character
(S)	$\underline{0}$ when $\underline{B_4} = \underline{1}$ $\underline{1}$ otherwise	Used to generate 2nd scan separation character
(H)	$\underline{0}$ when $\underline{A_4} v \underline{B_4} = \underline{1}$ $\underline{1}$ otherwise	Identifies a non-numeric character
(3)	$\underline{0}$ when $\underline{A_5} = \underline{1}$ $\underline{1}$ otherwise	Identifies first voltage character and enables (B), (D) and (F)
(N)	$\underline{1}$ when $\underline{A_5} = \underline{1}$ $\underline{0}$ otherwise	Identifies first voltage character and enables (B), (D) and (F)
(B)	$\underline{0}$ Channel Voltage pos. $\underline{1}$ Channel Voltage neg.	Inverse of DVM's polarity output
(D)	$\underline{0}$ $\lvert$Channel Voltage$\rvert$ < 2.0000 $\underline{1}$ $\lvert$Channel Voltage$\rvert$ ≥ 2.0000	Inverse of DVM's out of range output
(F)	$\underline{0}$ $\lvert$Channel Voltage$\rvert$ < 1.0000 $\underline{1}$ $\lvert$Channel Voltage$\rvert$ ≥ 1.0000	Inverse of DVM's overrange output
(U)	$\overline{\underline{\text{BCD 1}}}$	Output of BCD Coupler
(12)	$\overline{\underline{\text{BCD 2}}}$	Output of BCD Coupler
(2)	$\overline{\underline{\text{BCD 4}}}$	Output of BCD Coupler
(F)	$\overline{\underline{\text{BCD 8}}}$	Output of BCD Coupler

Table 11

The EBCDIC Encoder Inputs for Manual Mode Operation

Inputs	States	Remarks
(9)	1	Connected to "M=1"
(14), (5), (H) and (3)	1	No sequencing of Board #4 and #5
(N)	0	No sequencing of Board #5
(B), (D), and (F)	See Sample Mode	No effect because (3) = 1 and (N) = 0
(15)	Level 0	Output of Diode Matrix
(17)	Level 1	Output of Diode Matrix
(K)	Level 2	Output of Diode Matrix
(11)	Level 3	Output of Diode Matrix
(E)	Level 4	Output of Diode Matrix via BCD Coupler ($\overline{\text{BCD 8}}$)
(2)	Level 5	Output of Diode Matrix via BCD Coupler ($\overline{\text{BCD 4}}$)
(12)	Level 6	Output of Diode Matrix via BCD Coupler ($\overline{\text{BCD 2}}$)
(U)	Level 7	Output of Diode Matrix via BCD Coupler ($\overline{\text{BCD 1}}$)
(L)	Level 0-3	Output of Diode Matrix Numeric characters only

The effects of the inputs in Table 11 on manual mode encoding are separated into two conditions. They are nonnumeric character recording and numeric character recording. When a nonnumeric key is depressed, (L) becomes equal to 1. The only other valid inputs to the encoder are the Diode Matrix inverse level outputs. The encoder outputs are now the inverse of inputs (15), (17), (K),

(11), (E), (2), (12) and (U). When a numeric key is depressed (L) becomes equal to 0. This forces Level 0 through Level 3 outputs to 1. The remaining outputs are now the inverse of inputs (E), (2), (12) and (U).

6.4.11 The BCD Coupler

The BCD Coupler, Board #7, provides BCD data information to the EBCDIC Encoder. The BCD Coupler receives data from three primary sources: Level 4 through Level 7 outputs of the Diode Matrix, the BCD outputs from the Voltage Data Parallel to Serial Converter, and the BCD outputs from the Time Parallel to Serial Converter (located in the digital clock). Device location and power wiring, the logic schematic, and socket connections are shown in Figure 45, 46 and 47.

Of all the outputs brought out of this board, only (M), (11), (9), and (K) are used. These outputs provide BCD information to the EBCDIC Encoder in the previous section. Since all of the elements on this board are arithmetic (see Figure 46), all outputs can uniquely be defined in terms of the inputs. These output equations in simple form are:

$$\underline{(M)} = \overline{\underline{(14)} \cdot \underline{(J)} \vee \underline{(16)} \vee \underline{(12)}}$$

$$\underline{(11)} = \overline{\underline{(R)} \cdot \underline{(J)} \vee \underline{(T)} \vee \underline{(10)} \vee \underline{(L)}}$$

$$\underline{(9)} = \overline{\underline{(F)} \cdot \underline{(J)} \vee \underline{(C)} \vee \underline{(3)}}$$

$$\underline{(K)} = \overline{\underline{(4)} \cdot \underline{(J)} \vee \underline{(5)} \vee \underline{(2)}}$$

The reader will note that inputs tied to a fixed logic level as indicated on Figure 47, are a part of the above equations but are not explicitly shown. For example, in the first equation

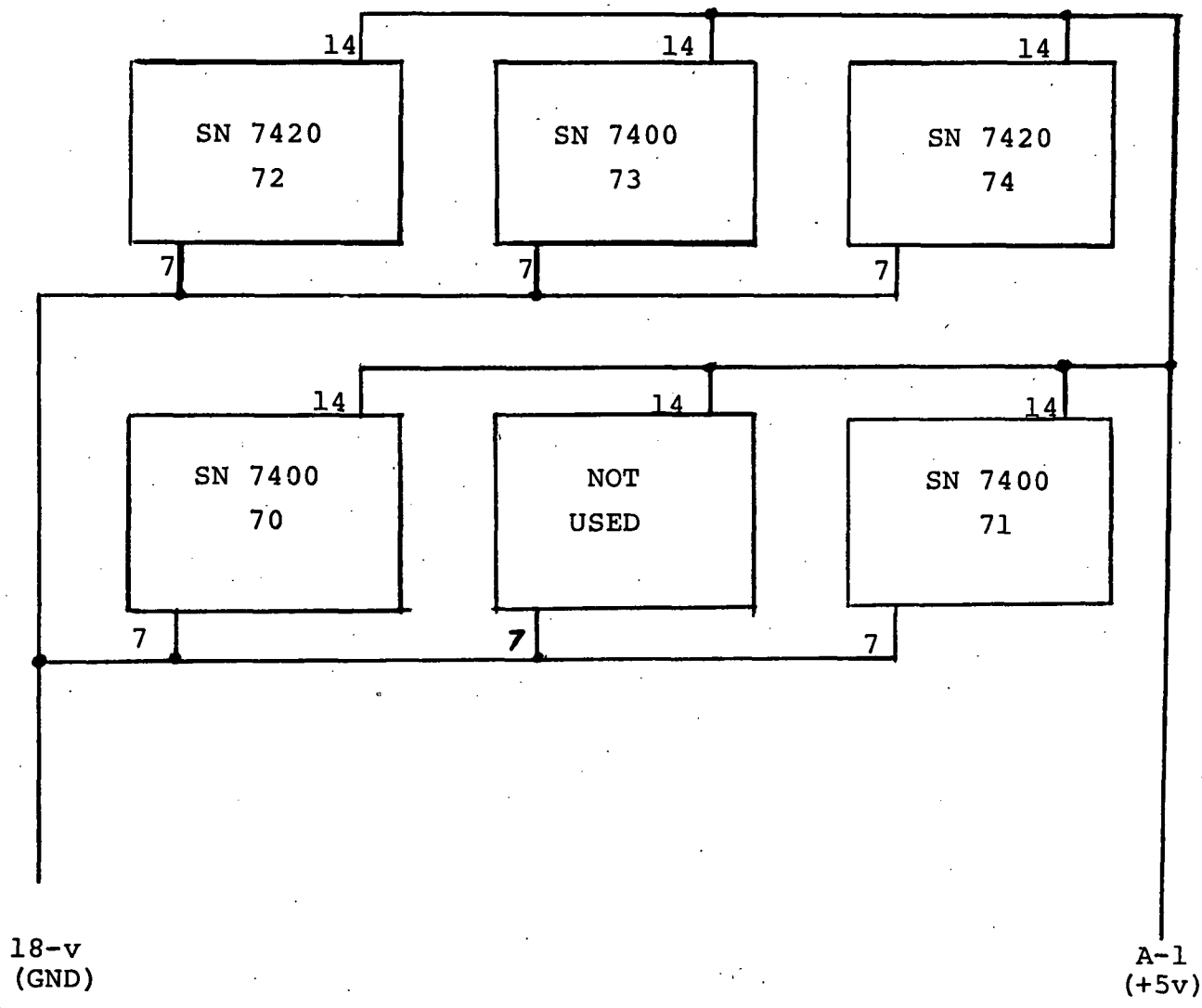


Figure 45. The BCD Coupler - Power Wiring and Device Location Diagram

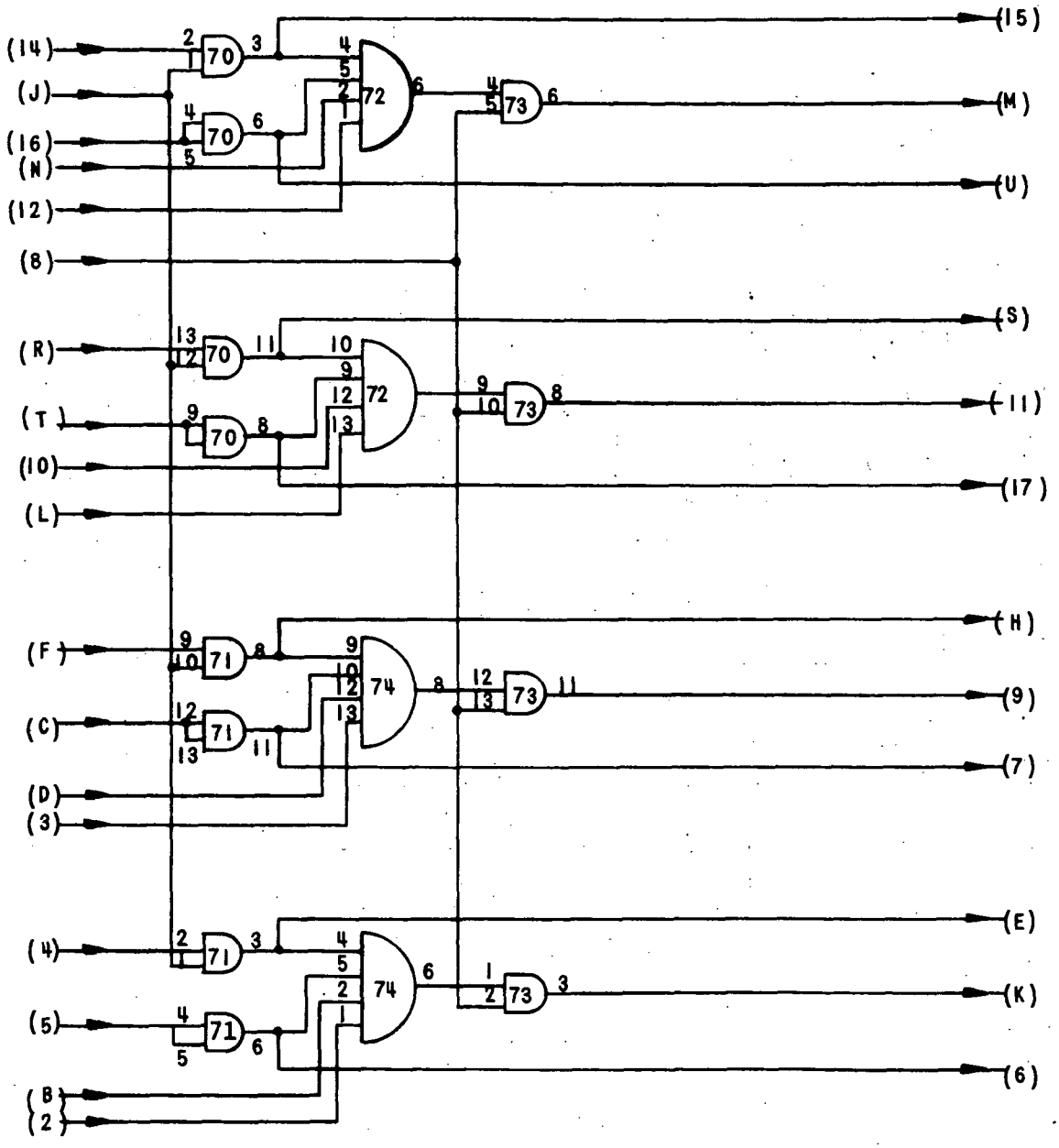


Figure 46. The BCD Coupler Logic Schematic

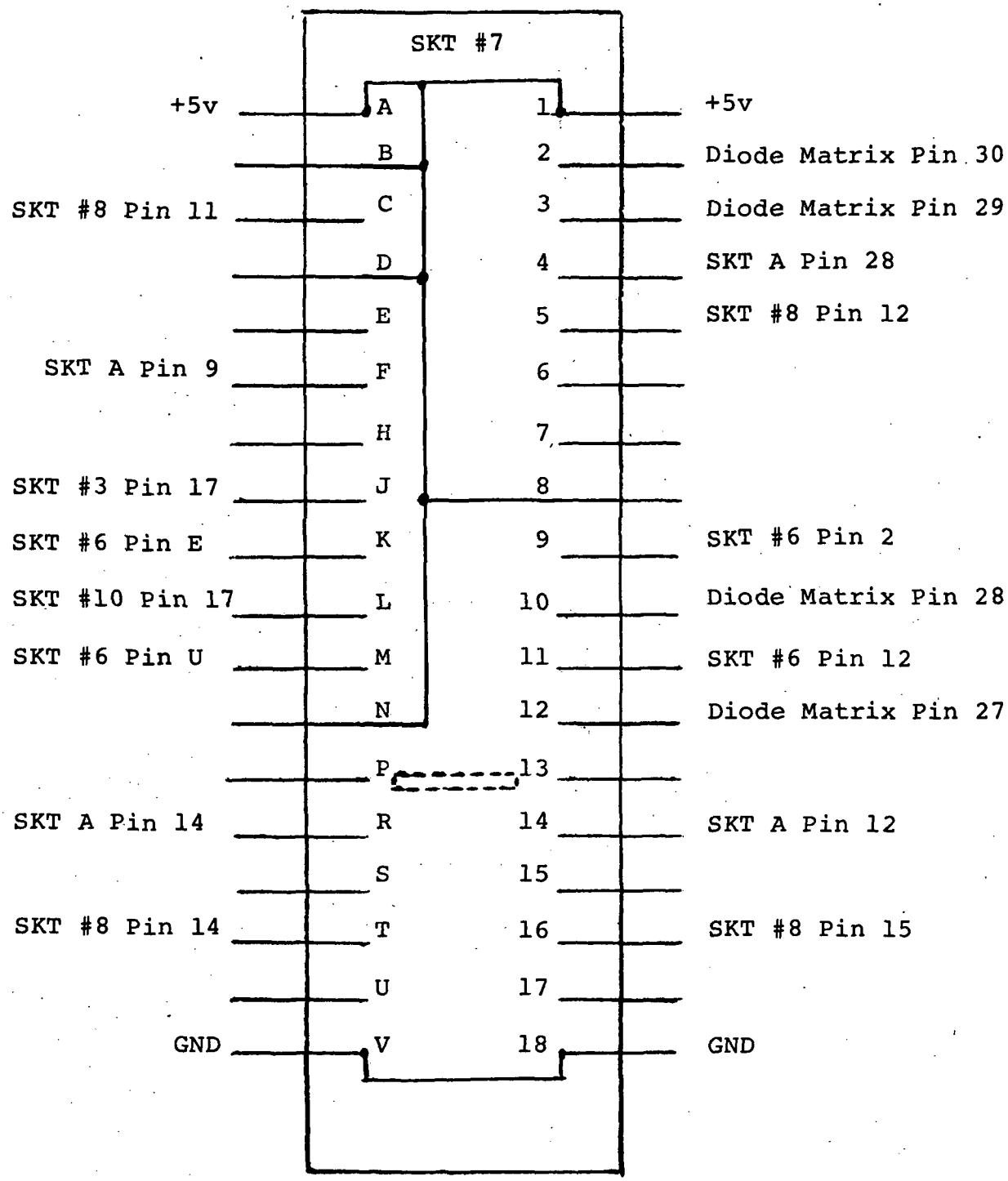


Figure 47. Connections to the BCD Coupler Socket

$$\underline{(M)} = \overline{\underline{(14)} \cdot \underline{(J)} \vee \underline{(16)} \vee \underline{(12)} \vee \underline{(N)} \vee \underline{(8)}}$$

Since $\underline{(N)} = \underline{(8)} = \underline{1}$ this reduces to

$$\underline{(M)} = \overline{\underline{(14)} \cdot \underline{(J)} \vee \underline{(16)} \vee \underline{(12)}}.$$

The inputs (14), (R), (F), and (4) are the BCD 1, 2, 4, and 8 outputs of the Time Parallel to Serial Converter. Inputs (16), (T), (C), and (5) are the BCD 1, 2, 4, and 8 outputs of the Voltage Data Parallel to Serial Converter. Inputs (12), (10), (3), and (2) are the equivalent inverse BCD 1, 2, 4 and 8 outputs from the Diode Matrix. The remaining two inputs are (J) and (L). Input (J) enables the coupler to accept BCD time data. Input (L) is used to change one of the BCD levels in the coupler when an error is detected in writing the data on tape.

The operation of the coupler in the sample mode is described in the order that sequencing events occur; i.e., the order in which characters are written on the tape. In the sample mode (12), (10), (3), and (2) are 1. (see Section 6.4.4) During the recording of the scan separation characters, inputs (14) (R), (F), (4), (J), (16), (T), (C) and (5) are 0. The output equations reduce to the following:

$\underline{(M)} = \underline{1}$, $\underline{(11)} = \underline{(L)}$, $\underline{(9)} = \underline{1}$, and $\underline{(K)} = \underline{1}$.

When the first scan separation character is to be recorded (L) will be 1 if no write error was detected on the previous scan. If an error was detected (L) is 0. After the first scan separation character is recorded, (L) is equal to 1. This state does not change throughout the rest of the scan. Before the coupler can accept time BCD data inputs, (J) must become equal to 1. (J) equals 1 only when the Time Sequencer shift register contains

a 1 bit and time is to be recorded. This input prevents failures associated with the Time Parallel to Serial Converter (or cable failures) from affecting other recorded characters. During the recording of time (J) is 1, and (16), (T), (C), and (5) are 0. The output equations reduce to the following:

$$(M) = \overline{(14)}, \quad (11) = \overline{(R)}, \quad (9) = \overline{(F)}, \quad (K) = \overline{(4)}$$

Thus, the outputs of the BCD coupler are the inverse of the serial BCD time data outputs. These outputs are then inputted in serial form to the EBCDIC Encoder for recording on tape. After the recording of time BCD data, (14), (R), (F), (4), and (J) are 0. The outputs of the BCD Coupler are now determined by the outputs of the Voltage Data Parallel to Serial Converter. The output equations are now as follows:

$$(M) = \overline{(16)}, \quad (11) = \overline{(T)}, \quad (9) = \overline{(C)}, \quad (K) = \overline{(5)}.$$

Thus, the outputs of the BCD Coupler are the inverse of the Voltage Data Parallel to Serial Converter outputs. Voltage parallel to serial conversion does not begin until the first voltage is encoded and its polarity-range character is recorded. Previous to this time the converter's outputs are all 0. Therefore,

$$(M) = (11) = (9) = (K) = 1.$$

After the polarity range bit is recorded, the serial BCD voltage data is outputted in serial form to the EBCDIC Encoder for recording on tape. The above process is then repeated for each channel voltage. After all channels are recorded, all the BCD data inputs are 0, and the outputs remain 1 until the next scan.

In the manual mode all BCD data inputs and (J) are 0. (L) is equal to 1, and the output equations are as follows:

(M) = (12), (11) = (10), (9) = (3), (K) = (2).

Thus, the BCD Coupler connects the four inverse BCD outputs from the Diode Matrix to the EBCDIC Encoder.

6.4.12 The Voltage Data Parallel to Serial Converter

The Voltage Data Parallel to Serial Converter, Board #8, accepts the parallel BCD voltage data from the DVM and outputs this data in serial form to the BCD coupler. This board also provides outputs that are the inverse of the DVM's polarity and range outputs. The outputs, inputs, and operation of this board will be discussed with the aid of Figures 48, 49 and 50.

The serial BCD outputs are (15), (14), (11), and (12). When a particular DVM digit, digit X, representing the DVM's thousands, hundred, tens or units digit, is to be encoded; the outputs equations are

(15) = BCD 1 of digit X

(14) = BCD 2 of digit X

(11) = BCD 4 of digit X

(12) = BCD 8 of digit X

Inputs to the parallel to serial conversion circuitry are command inputs, and the parallel BCD outputs from the DVM. The command inputs (U), (10), (4), and (6) have the following input equations:

(U) = B_5 (10) = C_5

(4) = D_5 (6) = E_5

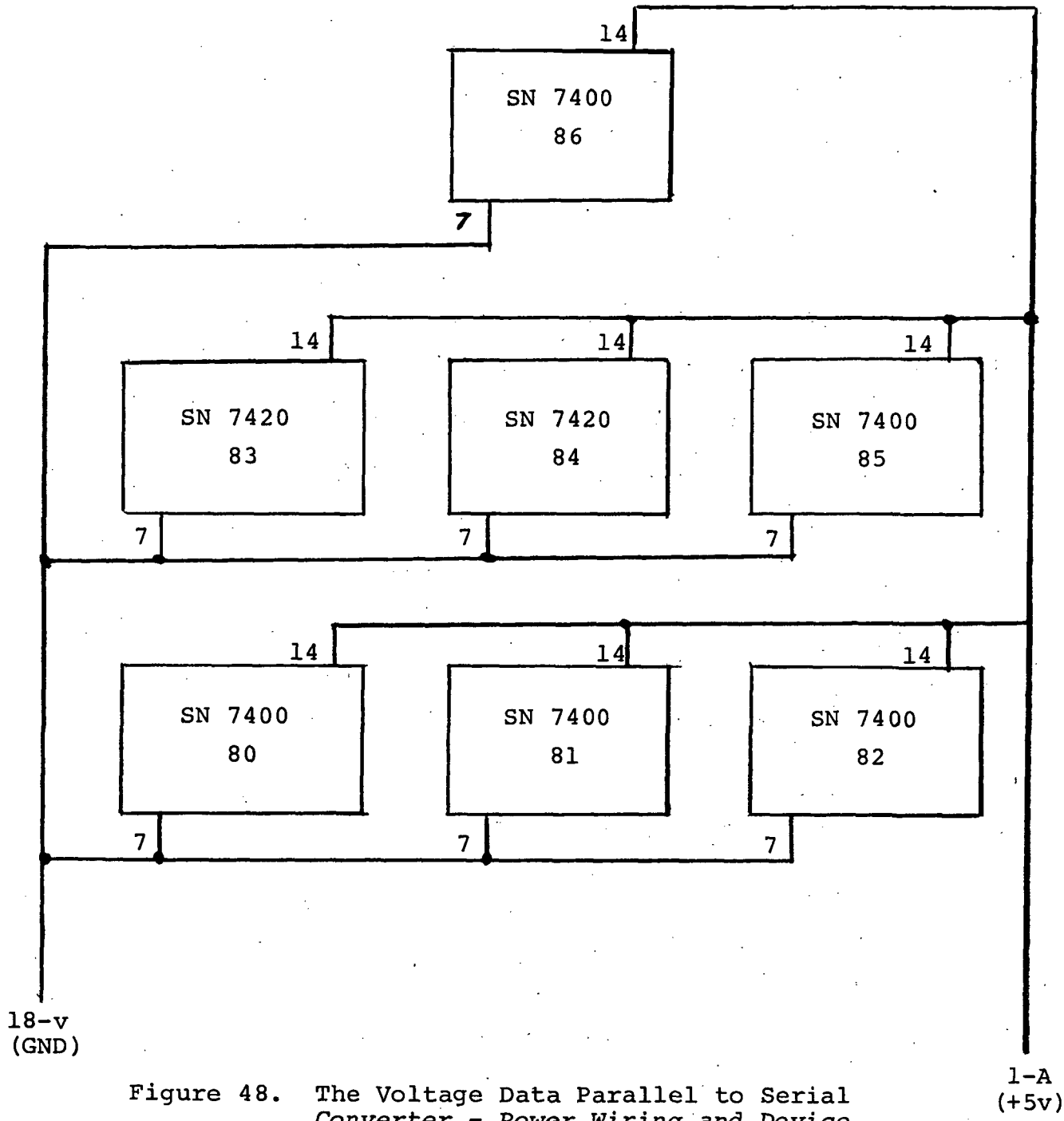


Figure 48. The Voltage Data Parallel to Serial Converter - Power Wiring and Device Location Diagram

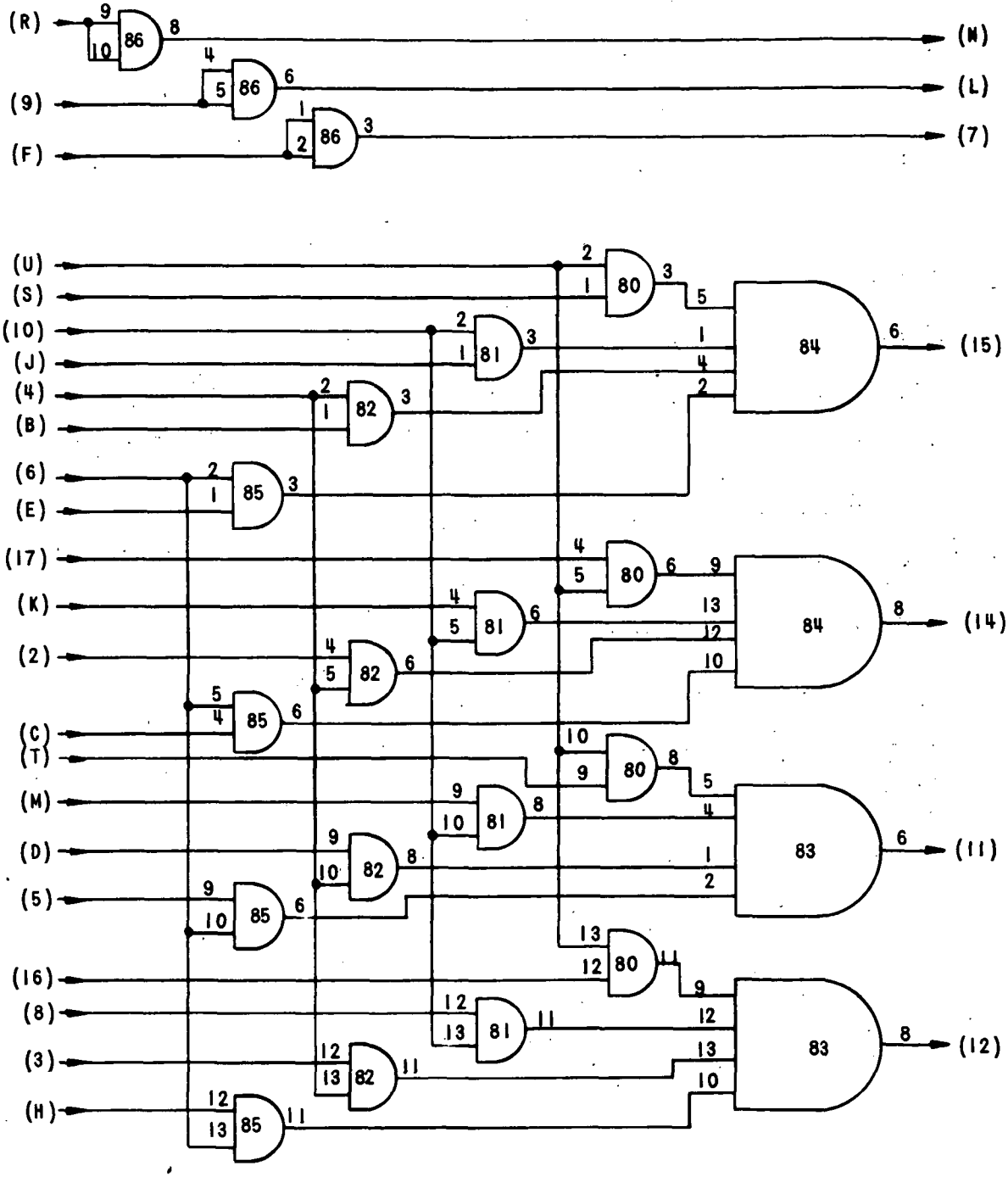


Figure 49. The Voltage Data Parallel to Serial Converter Logic Schematic

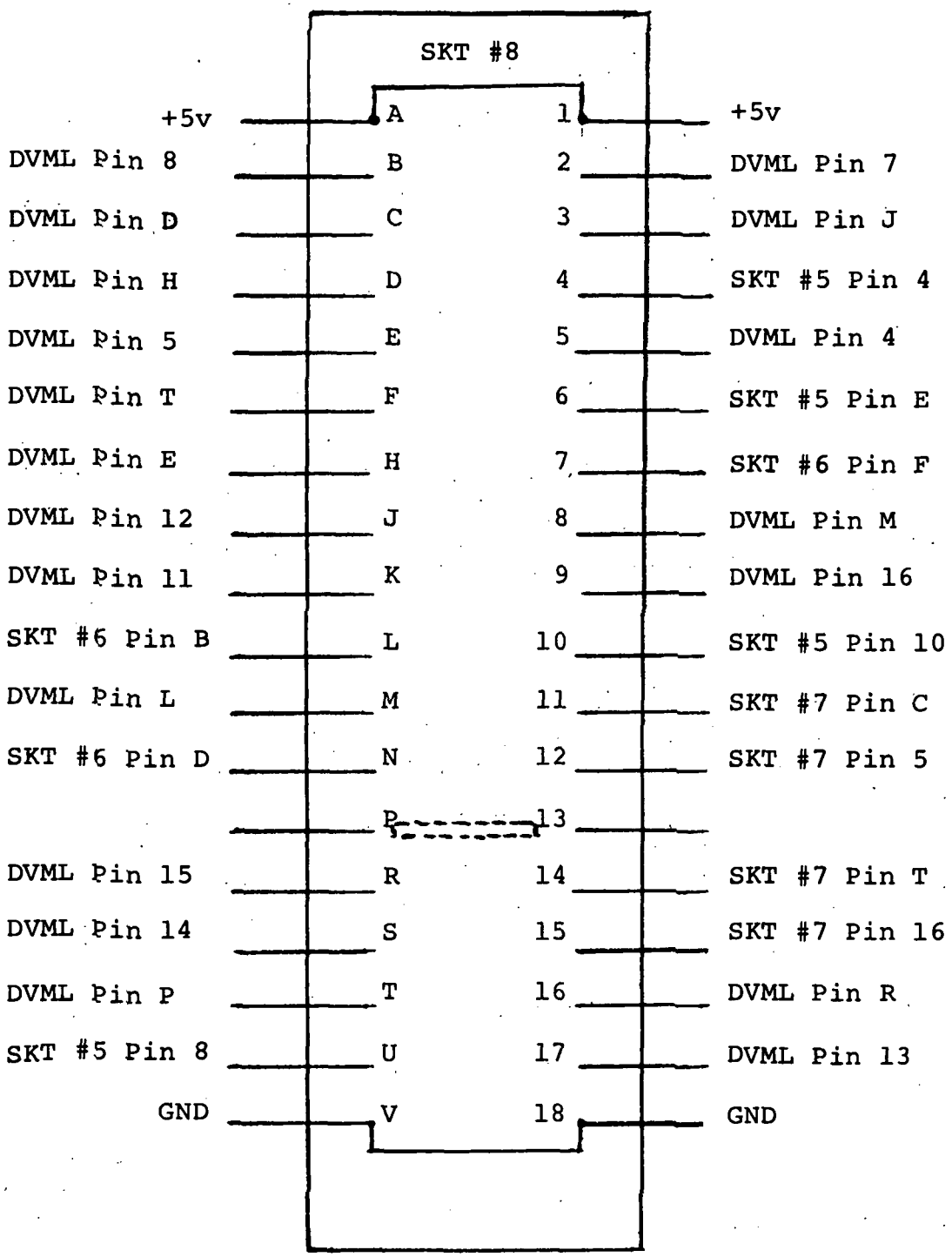


Figure 50. Connections to the Voltage Data Parallel to Serial Converter Socket

Only a very brief description of the Voltage Parallel to Serial Converter circuit will be presented here. Its operation is very similar to the time parallel to serial conversion discussed in Section 6.2.2. Since only a single 1 bit can exist in shift register #5 at one time, only one of the command inputs defined above will ever be 1. When the DVM's thousands bit is to be encoded, (U) is 1, and (10) equals (4) equals (6) equals 0. Similarly when another DVM digit is to be recorded, one of the other control inputs becomes 1 and the rest are 0.

The three outputs shown in Figure 49 that are not associated with serial BCD data are (N), (L), and (17). These outputs are connected directly to the EBCDIC Encoder. They are used by the encoder to encode the first voltage data character (see Section 6.4.10). These outputs are defined by the following equations

$$(N) = \overline{(R)} \qquad (L) = \overline{(9)}$$

$$(7) = \overline{(F)}$$

The inputs (R), (9), and (F) are the DVM's out of range, polarity, and overrange outputs, respectively.

6.4.13 The Channel One through Eight Selector

The Channel One through Eight Selector, Board #9, provides logic control outputs for the First Analog Multiplexer, MUX #1. This selector also contains a flip-flop circuit that determines that state of the preset enable input of shift register #5 (see Section 6.4.9). The shift registers on this board (and the next board) are operated in a slightly different manner than the other shift registers. After a brief discussion of these differences, the selector's outputs, inputs and operation will

be presented. Figures 51, 52, 53 and 54 will be used in this presentation.

The sequencing circuits that have been discussed prior to this have all used single five-bit shift registers. Their outputs were all 0 when no sequencing operations were occurring. However, the Channel One through Eight Selector (Channel Nine through Sixteen Selector) uses two five-bit shift registers, devices 91 and 92 (devices 101 and 102). These two devices employ common preset enable, clock, and clear inputs. Moreover, the bit number five output from the first register is connected to the serial input of the second register. In this configuration, the two five-bit shift registers are logically equivalent to a single ten-bit shift register, shift register #9 (shift register #10). The bit outputs of this ten-bit shift register are A_9 through J_9 (A_{10} through J_{10}) and the preset inputs are preset A through preset J. Note, in figure 52 and 54, that with these ten-bit shift registers, all of the preset inputs can be used to load the register. In the manual mode of operation, these preset inputs are used to load a single 1 bit into either register #9 or #10.

Selector outputs are the bit outputs of shift register #9 and the output of flip-flop 90. The outputs associated with the shift register are given by the following equations:

$\underline{(N)} = \underline{A_9}$ $\quad \underline{(C)} = \underline{B_9}$ $\quad \underline{(R)} = \underline{C_9}$

$\underline{(S)} = \underline{D_9}$ $\quad \underline{(T)} = \underline{E_9}$ $\quad \underline{(D)} = \underline{F_9}$

$\underline{(E)} = \underline{G_9}$ $\quad \underline{(F)} = \underline{H_9}$ $\quad \underline{(H)} = \underline{I_9}$

$\underline{(J)} = \underline{J_9}$

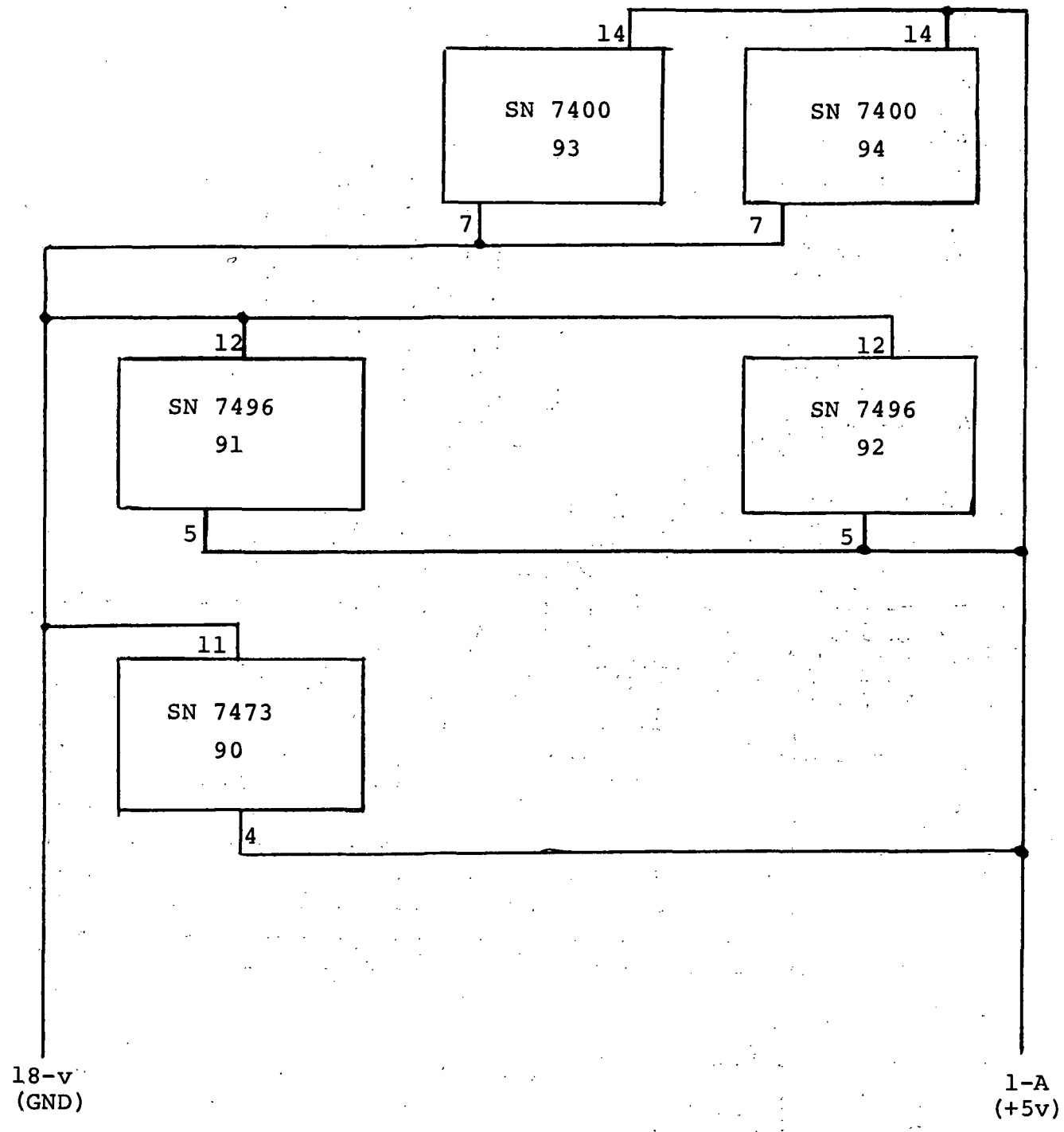


Figure 51. The Channel One through Eight Selector - Power Wiring and Device Location Diagram

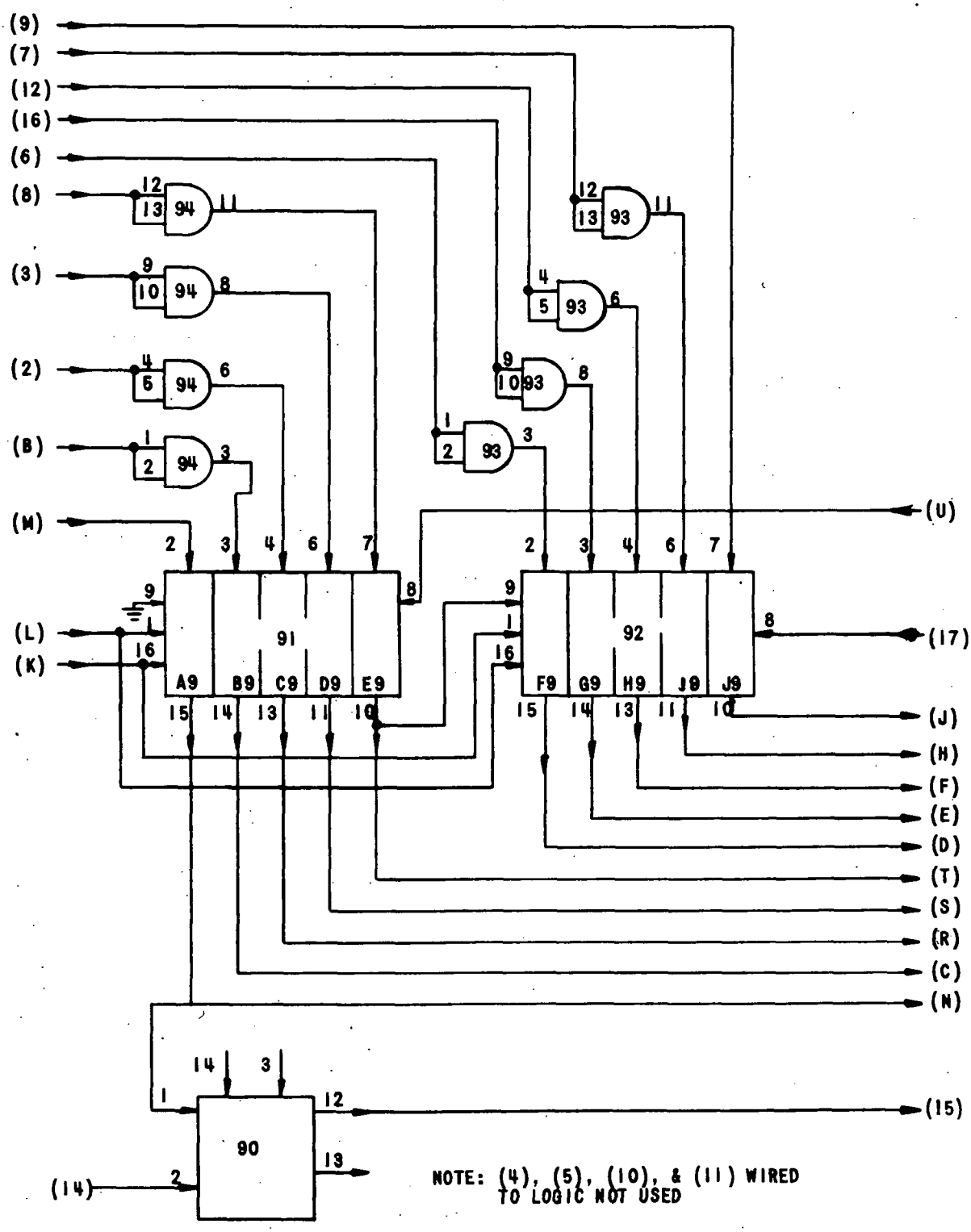


Figure 52. The Channel One through Eight Selector Logic Schematic

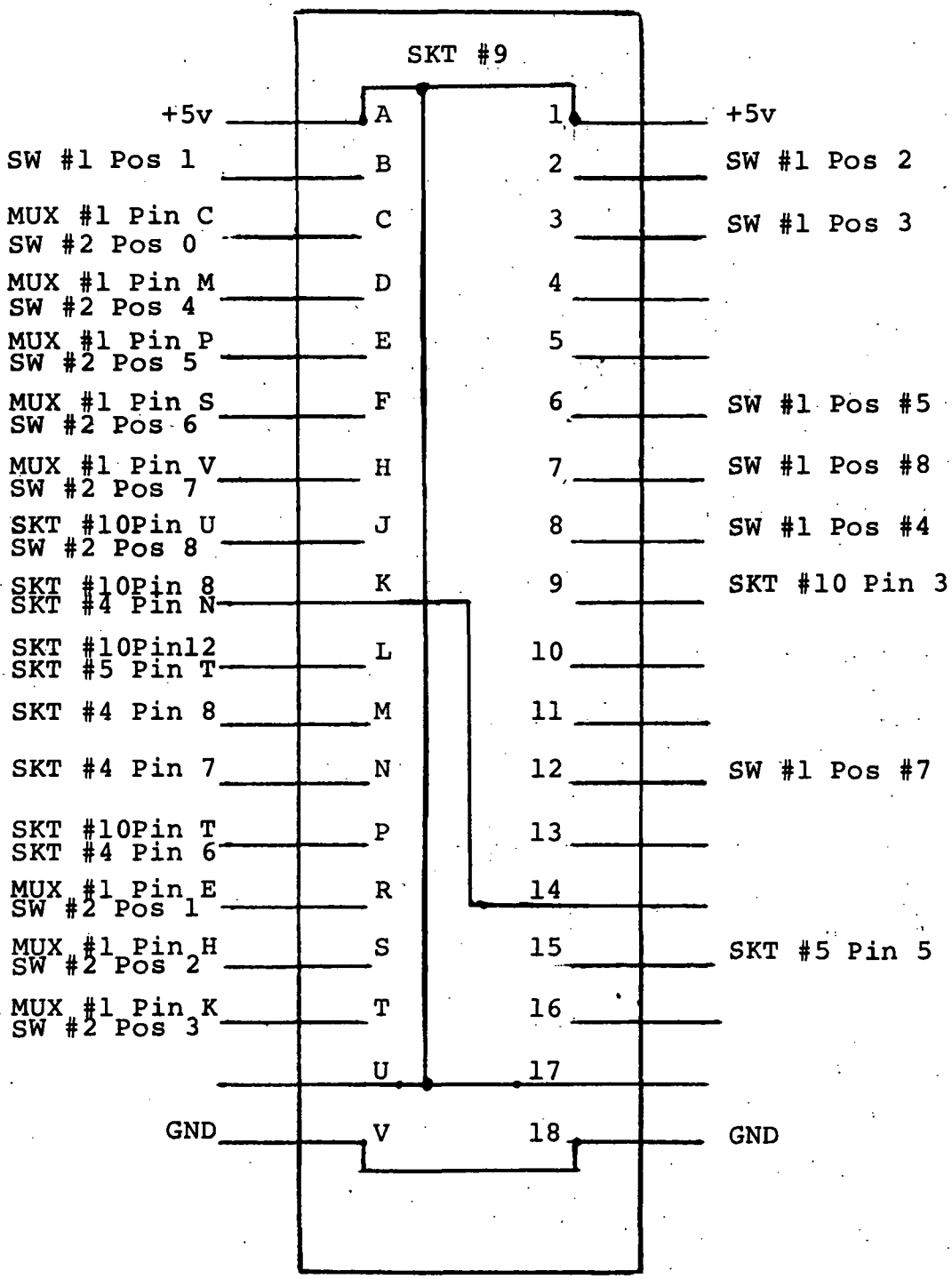


Figure 53. Connections to the Channel One through Eight Selector Socket

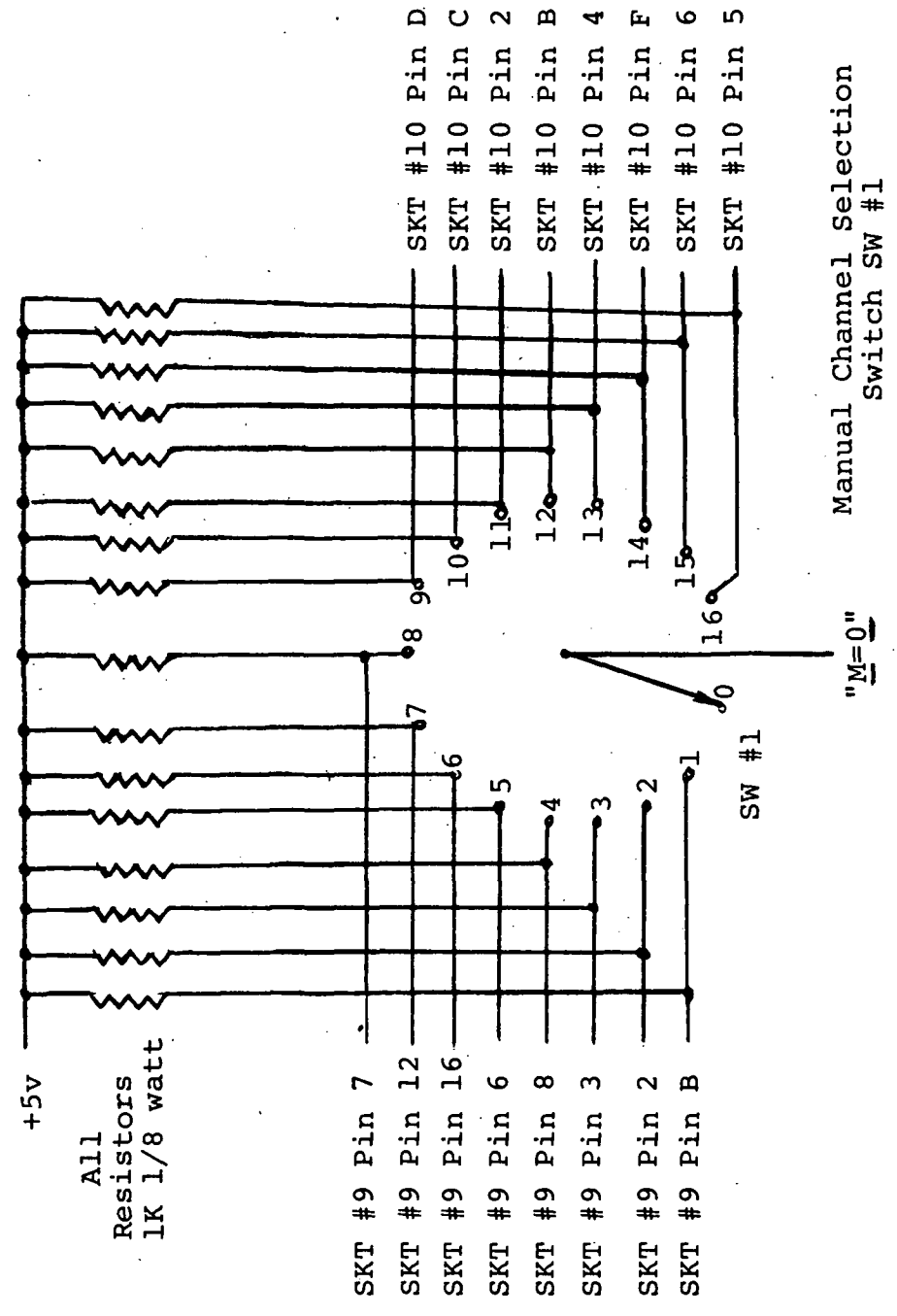


Figure 54. The Manual Channel Selection Switch

Output (N) is used to clear flip-flop 54B on the Voltage Data Sequencer via a NOR gate used as an Inverter on Board #4. Outputs (C) through (H) are connected to the control inputs of MUX #1. These outputs determine which voltage channel (1 through 8) is connected to the DVM's analog input. Output (J), the remaining shift register output, is connected to board #10. It is the serial input for shift register #10, and it is a logic control input for MUX #2. All of the above shift register outputs, except (N), are connected to the Number of Channels Sampled Switch, SW #2, discussed in detail in the next section. The remaining output, (15), the Q output of flip-flop 90, is connected to the Voltage Data Sequencer described in Section 6.4.9. Output (15) becomes 1 when A_9 makes a 1 to 0 transition. (15) remains 1 until flip-flop 90 is cleared.

Selector inputs are associated with shift register #9 and flip-flop 90. Inputs (U) and (17), shift register #9 preset enable inputs, have a fixed state of 1 (see Figure 53). Input (M), the preset A input of shift register #9, is connected to the Voltage Data Sequencer via a NOR gate on Board #4. This input is used to load a 1 into the first bit position of register #9. Input (L), the clock input of shift register #9, is connected to the Voltage Data Sequencer. A clock pulse occurs at (L) when D_2 becomes 1 and shift register #5 is idle. Inputs (K) and (14) are the clear inputs for shift register #9 and flip-flop 90. They are both connected to the Q output of flip-flop 40B on Board #4. (K) and (11) become 1 when a scan command is generated by the digital clock. After a preset number of channel

voltages are recorded, these inputs return to 0 to clear the shift register and flip-flop. The remaining selector inputs, (B), (2), (3), (8), (6), (16), (12), (7), and (9), are associated with the Manual Channel Selection Switch, SW #1, shown in Figure 54. Inputs (B) through (7) are connected directly to the switch and input (9) is connected via an equivalent Inverter on Board #10 (see Figures 56 and 57).

The outputs and inputs described above will now be used to describe the Channel One through Eight Selector's sample and manual modes of operation. Both modes of operation are dependent upon the First Analog Multiplexer and upon circuitry on Boards #2, #3, #4, and #5. In the following descriptions, a familiarity with these other circuits is assumed.

In the sample mode, all of the outputs of SW #1 are fixed to a logic state of 1, independent of the position of the switch. (Note, "M=0" has a logic state of 1 in the sample mode.) Therefore, all of the shift register #9 preset inputs B through J have states of 0, and the corresponding bit output states, B_9 through J_9, are determined only by the shift register's right-shifting operations. Sequential operations do not occur until time data recording is complete, E_3 equals 1 and B_2 equals 1. At this time, flip-flop 90 and shift register #9 are in their cleared states with clear inputs equal to 1; and input (M) is 0. When C_2 becomes 1 after the last time digit is recorded, E_3 makes a 1 to 0 transition, triggering flip-flop 54B on the Voltage Data Sequencer. Input (M) becomes 1, forcing A_9 to 1. Hence, output (N) is 1 which clears flip-flop 54B and returns (M)

to 0. The result of this operation is the loading of a single 1 bit into shift register #9. The next clock pulse to the Master Sequencer causes D_2 to become 1. The D_2 clock pulse appears at input (L) and the first bit of register #9 is right-shifted. (Now, A_9 = 0 and B_9 = 1.) The 1 to 0 transition of A_9 triggers flip-flop 90, forcing output (15) to 1. Output (15), connected to Board #5 input (5), now enables voltage data sequencing as described in Section 6.4.9. Output (C) is equal to 1, satisfying one of the necessary conditions to connect channel one to the DVM. When the Master Sequencer shift register idles the other condition is satisfied, and the DVM begins A/D conversion of the first channel's voltage. The Voltage Data Sequencer causes the Master Sequencer to recycle after A/D conversion is complete. While the channel one voltage is being recorded, D_2 clock pulses do not appear at (L) since they are held off by the Voltage Data Sequencer. After the Voltage Data Sequencer idles, a clock pulse at (L) again right-shifts a bit in shift register #9 to allow the second voltage channel to be connected to the DVM. The process is repeated until the preset number of channel voltages are recorded. If nine or more channels are to be recorded, output (J) provides a serial input to shift register #10 (Board #10). This serial input (a single 1 bit) is right shifted through register #10 to provide logic control outputs for MUX #2. When the preset number of channels have been recorded, flip-flop 40B on Board #4 is cleared via SW #2. (The operation of SW #2 is discussed in the next section.) The clear inputs (K) and (14) are returned to 0. All shift register #9 bits become

0 and (15) returns to 0 to prevent further voltage data sequencing operations (see Section 6.4.9). Clear inputs (K) and (H) remain 0 until the next scan command pulse is generated by the digital clock (see Section 6.4.8).

In the manual mode, clear inputs (K) and (14) are 0, and input (M) is 0. Clock pulses on input (L) will therefore have no effect, and A_9 is equal to 0. The other bit output states of shift register #9 are determined by the Manual Channel Selection Switch, SW #1. With SW #1 in position "0" or any position "10" through "16", all of register #9 bit outputs are 0. In any other position, a single preset input will be forced to 1 ("M=0" is connected to ground), and its corresponding bit output will be 1. Thus, one of the associated MOSFET switches (channels 1-8, MUX #1 or Channel 9, MUX #2) will be closed (ON) when the Master Sequencer shift register idles. This connects the DVM analog input to the ON channel, and its voltage is continuously read. With SW #1 in the "0" position no MOSFET switch on MUX #1 or MUX #2 is closed. With SW #1 in one of the positions "10" through "16", similar logic on Board #10 causes an associated MOSFET switch closure.

An alternate method for manual mode channel selection, would be to use a switch to connect a channel's voltage directly to the DVM's analog input (thereby bypassing the multiplexers and the selection circuits). Such a scheme would not provide as much useful troubleshooting information as the method that was employed. Using the selector and multiplexer circuits in both modes of operation, allows a technician to quickly verify and

locate a suspected failure. With the mode switch in the manual mode position and with different fixed voltages inputted to each of the channels, the DVM's analog input can be switched to the various channels using SW #1. If all the voltages at this point are correct, then shift register #9, #10, MUX #1, and MUX #2 are operating correctly.

6.4.14 The Channel Nine through Sixteen Selector

The Channel Nine through Sixteen Selector, Board #10, is the last circuit board in the sequential converter. This board, and its associated circuitry, have three functions. First, it provides the logic control outputs to MUX #2 for voltage channel selection. Second, this board provides the end of scan pulse used to stop voltage data sequencing and to reset associated flip-flops and shift registers. Third, the selector contains a write error circuit that changes the first scan separation character of a new scan if a write error was detected by the tape recorder during the recording of the previous scan. To simplify the discussion of the selector's outputs, inputs, and operation, each circuit function will be discussed separately. Figures 55, 56, 57 and 58 will be used in these discussions.

The first selector function, channel selection, is associated with the two five-bit shift registers shown in Figure 56. These two shift registers, devices 101 and 102, are wired as an equivalent ten-bit shift register, shift register #10. The bit outputs are A_{10} through J_{10}, and the preset inputs are preset A through preset J. Selector outputs that can be defined in terms of

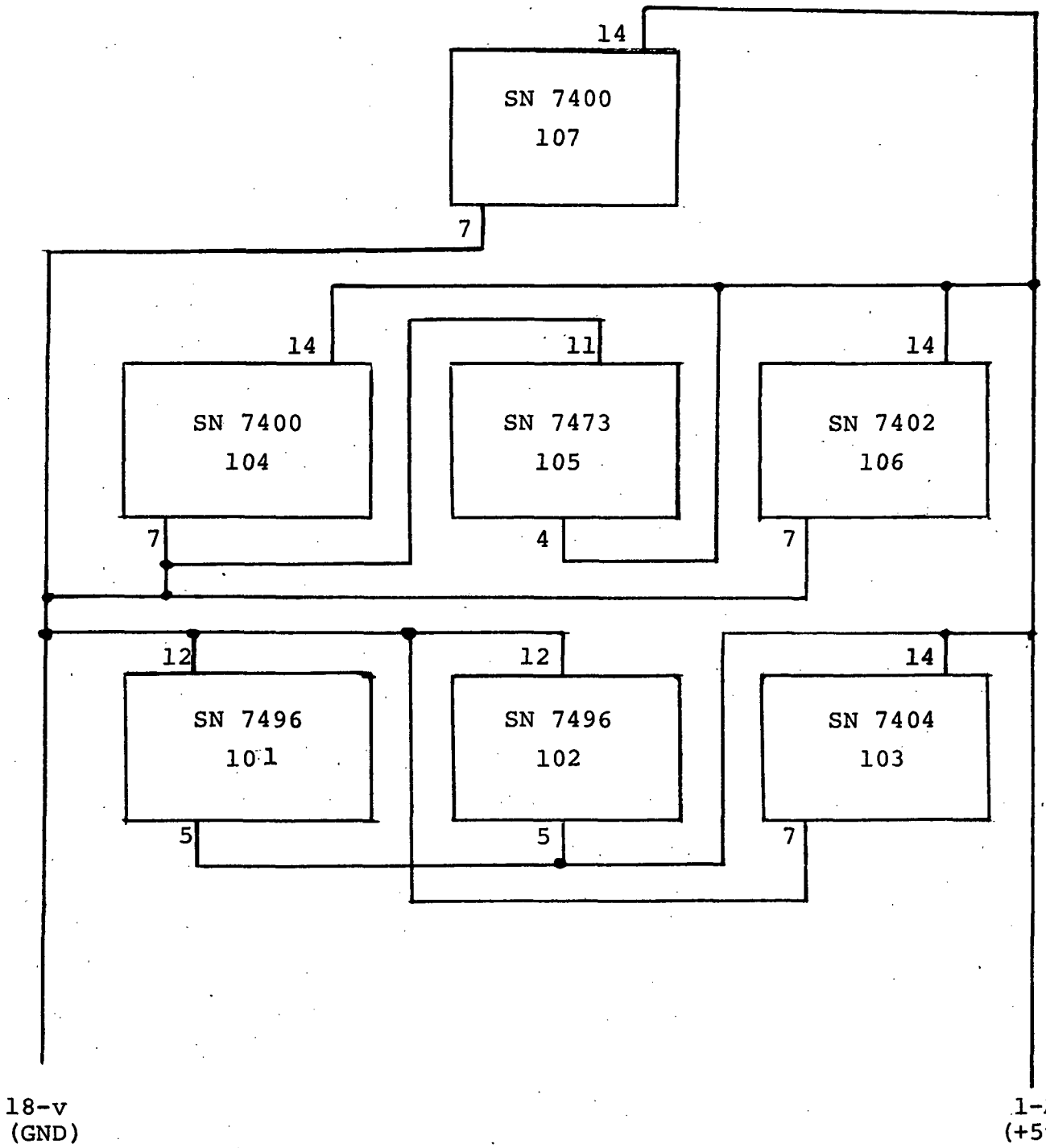


Figure 55. The Channel Nine through Sixteen Selector - Power Wiring and Device Location Diagram

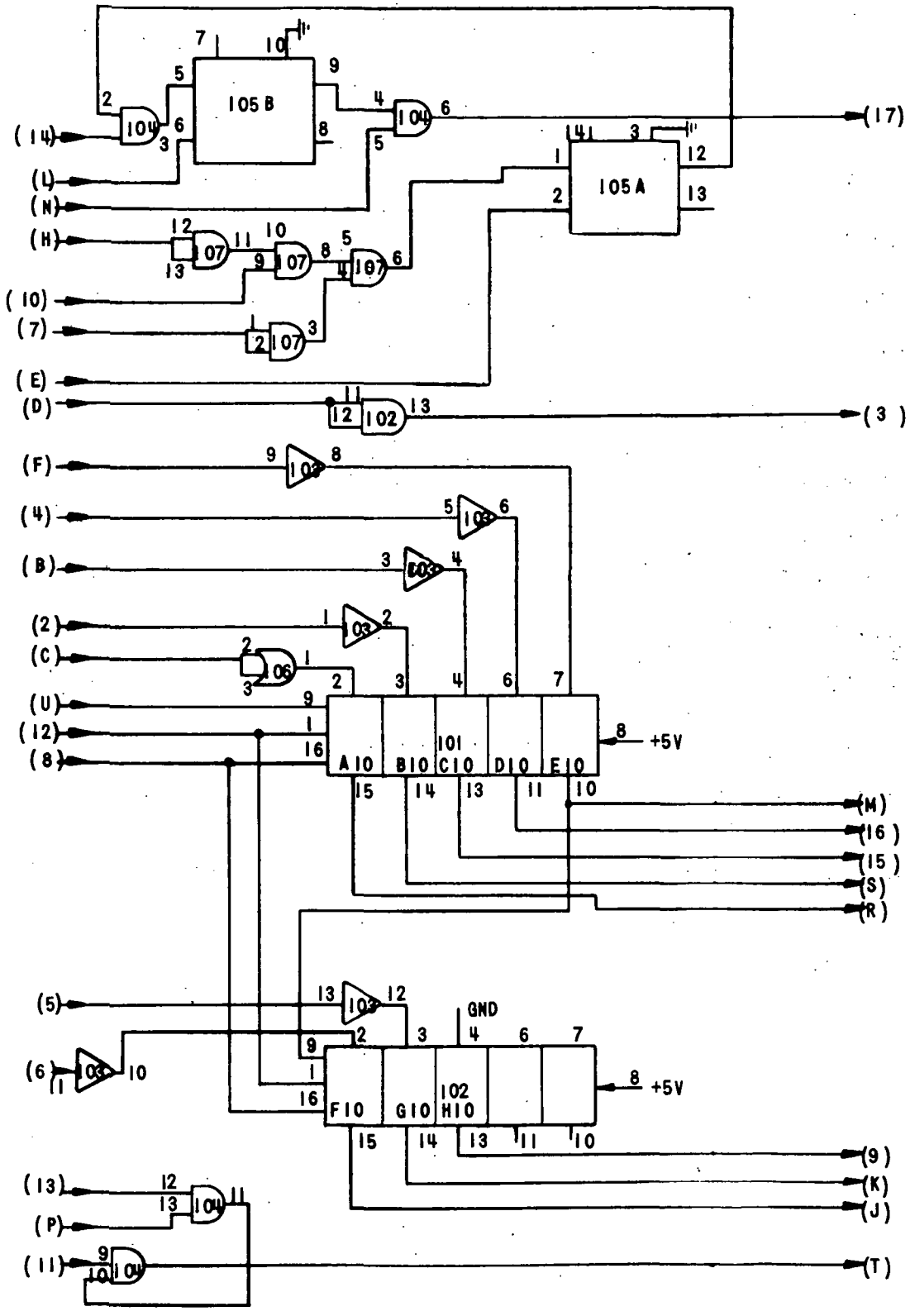


Figure 56. The Channel Nine through Sixteen Selector Logic Schematic

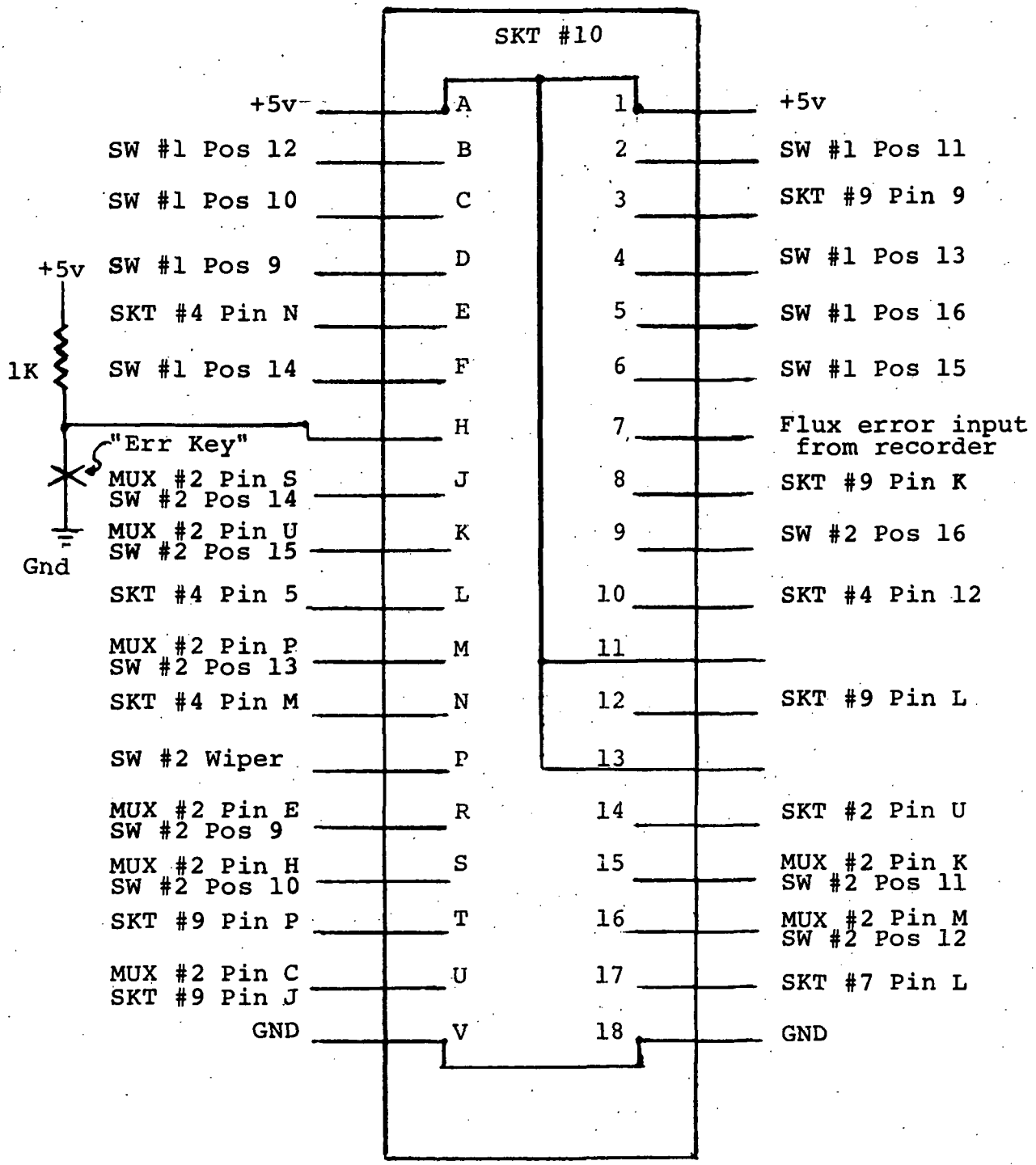


Figure 57. Connections to the Channel Nine through Sixteen Selector Socket

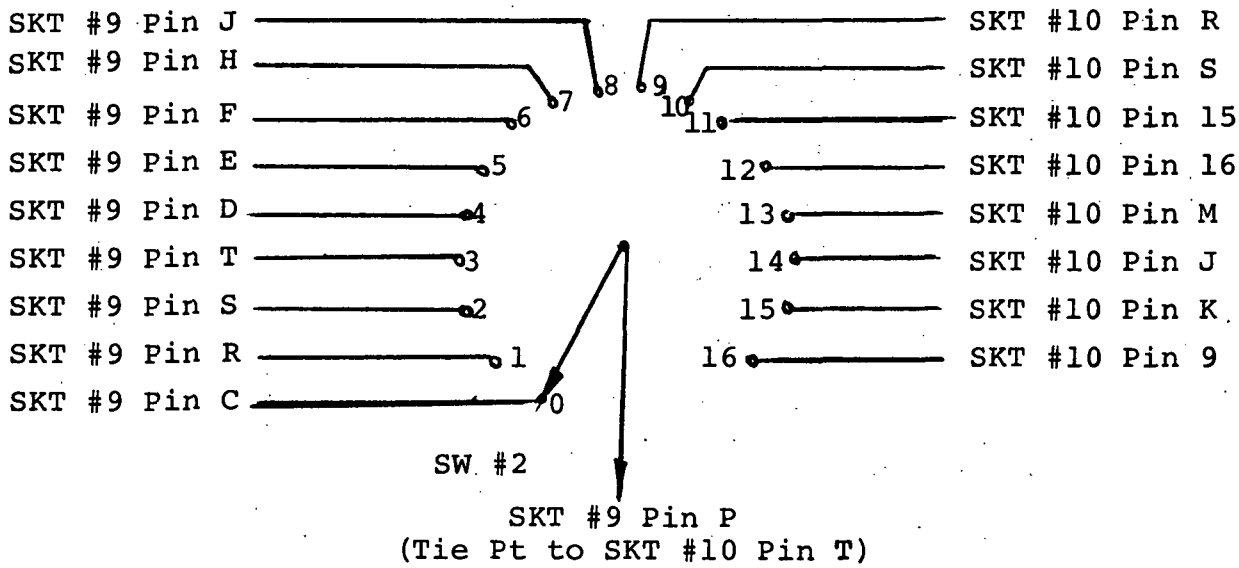


Figure 58. The Number of Channels Sampled Switch

this shift register's bit outputs are:

(R) = A_{10}	(16) = D_{10}	(K) = G_{10}
(S) = B_{10}	(M) = E_{10}	(9) = H_{10}
(15) = C_{10}	(J) = F_{10}	

As shown in Figure 57, bit outputs A_{10} through G_{10} are used to provide MUX #2 logic controls, and A_{10} through H_{10} are associated with the Number of Channels Sampled Switch, SW #2.

Inputs to the channel selector circuitry are the clock, clear, and serial inputs of shift register #10; and the inputs associated with the preset inputs of shift register #9 and #10. Input (R), the clock input, and input (8), the clear input, are connected to the clock and clear inputs of shift register #9 on Board #9. Input (U), the serial input, is connected to the tenth bit output of shift register #9. Shift register #10 is thus an extension of shift register #9. Together those two equivalent ten-bit shift registers are equivalent to a twenty-bit shift register.

The remaining channel selection circuit inputs are (D), (C), (2), (B), (4), (F), (6), and (5). These inputs are all connected to SW #1, described in the preceding section. Input (D) provides the preset J input for shift register #9 [via output (3) and socket wiring]. The remaining inputs determine the states of the preset A through G inputs of shift register #10. Operation of this selector's channel selection circuitry is identical to that described in the previous section. It will not be described here.

The second circuit board function is provided by the Number of Channels Sampled Switch, SW #2, shown in Figure 58 and by selector output (T) and inputs (13), (11), and (P).

Output (T) is connected to input (6) of the Scan Separation Character Generator (Board #4, discussed in Section 6.4.8) via socket #9 wiring (see Figure 53). When (T) becomes 1 flip-flop 40B on Board #4 is cleared. This results in the clearing of shift register #10, flip-flop 90, and shift register #9 on Board #9. Voltage data sequencing stops when flip-flop 90 is cleared (see Sections 6.4.9 and 6.4.13). To allow retriggering of flip-flop 40B when the next sample command pulse is generated by the digital clock, it is necessary that output (T) return to 0 after the above clearing operations are completed.

Inputs (11) and (13) are provided solely to allow the system's recording to be stopped by some future external control circuit. Presently, (11) and (13) have fixed states of 1 (via socket wiring). Output (T) is equal to input (P), and the condition for stopping voltage data recording is given by (P) equal to 1. (P) is connected to the wiper of SW #2. The position inputs of this switch are the bit outputs of shift registers #9 and #10. In any switch position the state of (P) is determined by the state of a particular shift register's bit output. Specifically, with the switch in the 4th position (4 channels to be recorded) the state of (P) is the state of the bit output, (F_9) associated with channel 5 (the bit output that controls the 5th MOSFET switch).

The operation of this circuit is most easily understood by assuming that SW #2 is in position "N". In this case, (P) is 0 until recording of the Nth channel voltage is complete. Upon completion of recording, a D_2 clock pulse right-shifts a 1 bit in either shift register #9 or #10. The channel N + 1 bit output becomes 1 and input (P) equal to output (T) becomes 1. Flip-flop 40B clears, clearing shift registers #9, #10 and flip-flop 90. Clearing of these shift registers will return (P) to 0. Thus the condition that (T) return to 0 to allow retriggering of flip-flop 40B is satisfied. From the above discussion, it is obvious that the (P) equal to 1 or (T) equal to 1 condition exists only momentarily. This time is approximately 100 nanoseconds (the combined propagation delay of three gates, one shift register, and one flip-flop).

The remaining selector output, output (17) and selector inputs, inputs (7), (N), (L), (14), (E), (H), and (10), are associated with the final circuit function, flagging the first scan separation character.

Output (17) is connected to the BCD Coupler described in Section 6.4.11. Normally, (17) is 1. If, during the previous scan, a write error was detected by the tape recorder, this output is equal to 1 when the first scan separation character is to be recorded [(17) = 0 when A_4 = 1]. If no error occurred, (17) remains at 1. The effect of (17) on the first scan separation character is described in Section 6.4.10.

Input (7), a clock input for flip-flop 105A, is connected to the tape recorder's write error output. Input (7) makes a

1 to 0 transition when a write error is detected. Since all tape recorder writing of data characters is initiated by B_2 becoming 1, this transition, if it occurs, will occur after B_2 becomes 1, but before C_2 becomes 1.

Input (N), connected to Board #4, is used to force output (17) to 1 if a character other than the first scan separation character is being recorded. [(N) = A_4] Input (L), also connected to Board #4, clears flip-flop 105B after the scan separation character is written, and (L) equals B_4. Input (14), connected to the Master Sequencer, allows the Q equal 1 output from flip-flop 105A to trigger flip-flop 105B. Input (14) is equal to C_2. Inputs (7), (N), (L), and (14) are all associated with the normal functions of the write error circuit.

Additional inputs (E), (H), and (10) provide added features. Input (E), from Board #4, clears flip-flop 105A when the system is idling or is in the manual mode. Therefore, write errors detected during manual data recording will not affect the first scan separation character when the system is switched to the sample mode. In typical system operation, write errors seldom occur. To allow software debugging, it is necessary to be able to duplicate a write error condition on a particular scan. This is accomplished by the Error Key on the manual keyboard, its associated input (H) and input (10). Input (H) is equal to 0 when the Error Key is depressed and Input (10) is equal to C_4.

In the normal sample mode operation of the write error circuit, (E) is 1, (H) is 1 and (10) has no effect. When

each scan begins flip-flop 105A is in its cleared state with the clear input equal to 1 (This flip-flop is cleared by the input (E) equal 1 condition described previously in section 6.4.8). When A_4 is 1, (17) is equal to $\overline{Q}$ of flip-flop 105B. If a write error pulse occurred during the previous scan, Q flip-flop 105B is equal to 1, (17) is 0, and a "G" is written as the first scan separation character. Otherwise, Q is 0, (17) is 1 and a "E" is written. In either case, when A_4 is no longer 1, (17) is forced to 1. When B_4 becomes 1, (L) becomes 0, clearing flip-flop 105B. When B_4 returns to 0, (L) returns to 1. A write error output from the tape recorder associated with the first character or any succeeding character on the scan triggers flip-flop 105A, causing its Q output to become 1. Once this Q output becomes 1 subsequent write error output pulses in the same scan do not affect its state. After each character is recorded, the Q output of flip-flop 105A is clocked to the clock input of flip-flop 105B in input (14). If this Q output is 1, flip-flop 105B is triggered when C_2 becomes 1. As in the case of flip-flop 105A, once the Q output of flip-flop 105B becomes 1 additional clock pulses do not affect its state. An exception to the above sequence occurs if the first write error pulse is associated with the first or second scan separation character. An error on the first character causes Q flip-flop 105A to become 1. When C_2 becomes 1, Q flip-flop 105B becomes 1. Although (17) is 0 until B_4 becomes 1, this output does not affect the character just recorded. (Recording is complete before C_2 becomes 1.) Since flip-flop 105A is then

cleared when B_4 is 1, the Q equal 1 output of flip-flop 105A does not retrigger flip-flop 105B until A_3 is 1 and C_2 becomes 1. Similarly, a first write error pulse associated with the second scan separation character does not trigger 105B until A_3 is 1 and C_2 becomes 1. The last character of a scan is recorded when B_2 becomes 1. When C_2 becomes 1 the Q output of flip-flop 105A is clocked to flip-flop 105B. D_2 becoming 1 clears flip-flop 105A momentarily. At this time the Q output of flip-flop 105B is 1 if a write error occurred in the scan just completed and is 0 otherwise. The sequential operation described above is repeated for each scan.

If an "artificial" write error condition is required for software debugging, the ERR Key is depressed before a scan begins. This forces (H) to 0, allowing the C_4 clock pulse to trigger flip-flop 105B. After C_4 returns to 0, (H) has no effect and the key may be released. To assure that the required time interval has elapsed it is suggested that the key be depressed until the first voltage channel is encoded (the DVM visual readout changes). The next scan will begin with a first character "G" just as if a write error pulse occurred.

No sequencing operations of this circuit occur in the manual mode. Flip-flop 105A is cleared in this mode and flip-flop 105B cannot be triggered.

All of the system's functional units, their interconnections, and their operations have been described. The concluding chapter will review the system's capabilities and features. Additionally, possible methods of improving the system to reduce hardware

requirements and to increase system capabilities will be presented.

CHAPTER VII

CONCLUSION AND SUMMARY OF RESULTS

7.1 Introduction

The previous chapters have described a data logging system designed for use by the Ionosphere Radio Laboratory (IRL) at the University of Illinois. Chapter I presented system requirements and design parameters. Chapter II described the basic inter-relationships between the three system subunits. Chapter III discussed the data system's code and format. Chapter IV introduced the individual functional circuits that comprise the system. Chapter V defined the logic elements used to realize the system's functional circuits. Chapter VI provided a detailed description of the system's individual functional circuits and their interconnections. In this chapter the system's development and its present capabilities will be summarized. Major design concepts and system improvements will also be discussed. Finally, the data system's present applications will be presented, illustrating its usefulness.

7.2 The Development of the System

The present data logging system is the final result of an evolutionary process. When data collection and reduction capabilities of the Ionosphere Radio Laboratory were first analyzed, a slow speed, fixed scan rate, and eight channel capacity was decided upon. Project funding and the possibility of using existing equipment were important considerations in this

development. A first generation system that would meet initial system requirements was constructed. This system utilized a digital clock, a sequential converter, and a paper tape punch and its associated power supplies and solenoid driver circuits. This system utilized the ASCII paper tape code to represent all output data. The system format included start characters, a five character time record (time recorded every hour), and voltage data groups consisting of five characters (a voltage polarity-range character and four decimal numbers). Manual data recording was a part of this original system's capabilities. The system had a recording speed of 16 characters per second, and a single sample rate of one scan per minute. A single Analog Multiplexer and a single channel selector circuit resulted in an eight channel voltage input capability.

Although this original system was used for almost a year, its weaknesses were painfully apparent. The low recording density (10 characters per inch) required frequent changing of the system paper tape. Additionally, computer processing of the paper tape was a slow and inefficient process. Virtually all of the failures in the first system were traceable to the mechanical recording device, the paper tape punch although the reliability of the sequential converter was very satisfactory.

When future data needs of the IRL were considered, it was decided to expand the existing data system and to replace the paper tape punch with an incremental magnetic tape recorder. Since few problems had been encountered with the digital clock or the sequential converter both of these subunits were modified

and retained. Additional circuits were added to the digital clock to allow a choice of scan rates and to provide a higher frequency clock pulse, increasing the system's recording speed to 166 characters per second. The modifications to the sequential converter are discussed below.

A change of encoders and some modifications to the Diode Matrix were required to provide the EBCDIC encoding necessary to simplify system software. The concept of using five character groups for time and voltage data was maintained to reduce sequencing circuit changes. Scan separation characters for the magnetic tape format were generated in the same manner as they were in the paper tape system. Time sequencing was changed to record time on each scan. Additional circuits were added to satisfy some requirements unique to the magnetic tape processing equipment. Specifically, a circuit was added to provide for the generation of inter-record gaps after each thirty-two scans. A circuit was added to flag the first scan separation character to indicate any errors detected by the recorder write error circuitry. The addition of a second Analog Multiplexer and a second selector circuit expanded the input voltage capacity to sixteen channels. The present system uses the same slow A/D converter that was used with the paper tape system. Replacement of this unit in the future is straightforward and should not result in a lengthy loss of the data system's availability. The substitution of a faster unit (an A/D converter with a shorter encoding time) will be necessary to permit multiple channel recording at the highest scan rate

(1 sample per second).

7.3 Present System Capabilities

The present data logging system provides two modes of operation. In both modes IBM 360 compatible EBCDIC coding of the output tape is used. A manual mode, with a recording speed of 16 characters/sec., is used to write characters associated with the tape header. A sample mode, with a recording speed of 166 characters/sec., serially records time and voltage information in five character groups. One to sixteen channels of analog voltage data may be recorded. Selectable sampling rates of one scan per second, one scan per five seconds, one scan per ten seconds, one scan per thirty seconds, and one scan per minute are provided. Blocking of the output tape record and flagging of the tape's output to indicate the presence of write errors are also performed by the system in this mode.

Since the sequential converter was totally designed and constructed to be a system subunit, its power supplies must be mentioned. A ±15 volt supply, manufactured by Analog Devices, provides power for the Analog Multiplexers. The DVM contains its own internal line powered supplies. The remaining logic circuits in the sequential converter derive power from an Acopian regulated 5 Volt, 2 ampere supply. Since this supply is operating near its rated capacity, its regulator pass transistor was externally mounted on a large heat sink at the rear of the sequential converter (see Figure 13).

As an aid to the reader who wishes to duplicate all or part of the system's circuitry, a listing of the TTL devices

added to the digital clock and used in the sequential converter is presented in Table 12. A total of 87 devices are shown in this table. These devices contain a total of 233 arithmetic elements and 34 nonarithmetic elements. Since the present system is a prototype, the listing in Table 12 does not represent optimum system design.

Table 12

A Listing of the System's TTL Devices

Device	Description	Number Used
SN 7400	Quad 2-input NAND gate	34
SN 7401	Quad 2-input open collector NAND gate	4
SN 7402	Quad 2-input NOR gate	10
SN 7404	Hex inverter	3
SN 7420	Dual 4-input NAND gate	10
SN 7430	8-input NAND gate	3
SN 7473	Dual J-K master-slave flip-flop	11
SN 7490	Decade counter	1
SN 7492	Divide-by-12 counter	1
SN 7496	5-bit shift register	8
SN 74121	Monostable multivibrator	2

Certain basic concepts are used in the system's design and construction. Four of these concepts, applicable to many serial recording systems, are discussed below.

The first concept is the use of the Master Sequencer as a clock pulse source for all sequencing circuits. In any data logging system involving more than one sequential operation, a major problem is timing. Typically, flip-flops and shift registers are clocked by a common source. Completion of a particular sequencing operation occurs when certain of these nonarithmetic elements return to their cleared states. Other operations are then initiated. Propagation delay times are often critical, since they affect the required time interval between completion of one operation and the initiation of the next operation. The Master Sequencer replaces the single common clock pulse source with six synchronized sources. The six output pulses are each separated by known time intervals (multiples of the input clock pulse) that are independent of device parameters. By judiciously choosing the correct shift register #2 bit output as the clock pulse source for each sequencing circuit's clock inputs, and by assuring that the constant time interval is greater than any propagation delays encountered, sequencing or timing errors are eliminated.

The second concept is the use of an intermittent recording scheme involving sequential encoding and then recording of each data channel. With this scheme analog data storage (sample and hold circuits) and digital data storage are not required. In cases where exact time correlation between the various input channels recorded on each scan is not required, this scheme greatly simplies the system's hardware. An additional feature of this scheme is of particular value to a research group with

limited present data requirements and an expectation of larger future requirements. Since the system recording speed is not determined by analog voltage encoding speed (recording speed is defined as the speed at which available digital data is recorded on tape), a relatively slow and inexpensive A/D converter can be used initially. The system capabilities are then easily increased by replacing the A/D converter with a faster unit.

The third concept is concerned with the recording of manual data. In this particular system, as in many data logging systems whose output tape is used directly as a computer input, manual recording consists of generating a few characters at the beginning and at the end of the tape. Sophisticated keyboards and associated circuitry are of dubious value due to their limited use. In order to use an existing keyboard, originally designed for a much slower recording system, the system incorporates a special manual recording speed of 16 characters/sec. The keyboard operates a flip-flop enabling circuit that prevents the generation of false characters due to contact bounce. The Diode Matrix associated with the keyboard provides the necessary character flexibility at reasonable cost. In this system, no attempt is made to provide for manual recording of characters that might be required in the future. Rather, the Diode Matrix was designed to premit rapid changing of any key character by the addition or deletion of a maximum of eight diodes. Removal of the Diode Matrix can be accomplished while the system is recording data in the sample mode.

The fourth and final concept is related to the physical layout of the functional circuits in the digital clock and sequential converter. These physical schemes are described here and their advantages are given in the following paragraph. All TTL elements in the system are socket mounted on fiberglass-epoxy circuit boards. The circuit boards in the sequential converter are identical 36 connector, plug-in boards providing copper pad mounting for up to nine, fourteen or sixteen pin dual-in-line integrated circuits. Larger circuit boards, compatible with the existing mounting arrangement, are used for added circuitry in the Digital Clock. Conventional wiring, using teflon insulated stranded hook up wire and cold drawn solid wire with teflon spagetti, is employed on all boards. Finally, each board is designed to provide only one major circuit function.

There are several advantages to the physical schemes described. The use of integrated circuit sockets and conventional wiring provides the necessary flexibility required in prototype construction. Additionally, certain TTL gates used for circuit buffering and protection are purposely subject to failure during testing and "turn-up" of the system. Replacement of the gates, after initial faults are corrected, must be a simple procedure. The demarcation of circuit functions provides many desirable advantages. An obvious advantage of this arrangement is a minimization of input-output connections to each board. Since the mechanical board socket connections are a weak link in any system, this minimization cannot be overemphasized. This feature also allows the physical layout of circuit boards to

correspond to the logical order of the sequencing operations. The resultant sequential converter layout is simplified and interboard wiring cross coupling is reduced. One of the most important advantages of this arrangement is related to system trouble shooting. In spite of the high reliability of the TTL elements, logic failures will occur. Isolating a failure to one or two boards or their associated wiring is possible when each board provides only one major function. For example, if a computer dump of the output tape indicates that a particular level is always being recorded as a 1 or a 0, a problem exists in the encoding circuitry (as opposed to sequencing circuitry). If a BCD level (Level 4-7) is affected, either the BCD Coupler or the EBCDIC Encoder is suspect. If level 0, 1, 2, or 3 is affected, the failure is most likely in the EBCDIC Encoder. Similarly, extra or missing time or voltage data characters are most likely the result of Time Sequencer or Voltage Data Sequencer failures.

Virtually all system shortcomings are the result of the historic development of the system and not design errors. They are discussed here for the benefit of those who desire to build a similar system. The use of a slow speed A/D conversion device is an obvious weakness if high speed recording of multiple channels is required. Replacement of the device in the present system is anticipated. Other shortcomings are related to the sequential converter's board layout and TTL logic devices. These shortcomings do not affect the system's capabilities and will not be corrected in the foreseeable future.

The use of many circuit boards each providing a single function is a valid concept. However, this concept may have to be compromised if the circuit boards provide for the mounting of too few integrated circuits or if they do not have an adequate number of pin connections. Compromises have been made in the present system because gates required to complete a particular Boolian function or a sequencing operation could not be physically located on the correct circuit board. Larger boards with more pin connections would alleviate this problem.

An obvious design criteria was the minimization of TTL devices. Unfortunately, this goal was not always achieved due to the historical development of the sequential converter. More extensive use of Hex Inverters and open collector logic would reduce the total number of TTL devices in the system. Additionally, parallel to serial conversion circuits could be duplicated by using newer types of TTL devices such as the 4-line-by-1-line digital multiplexer.

7.4 The Present Use of the Data System

The data system is presently being used to continuously record Faraday rotation data (Titheridge, 1966) from two synchronous satellites. The system is in operation 24 hours a day. During most of this time, the receiving station is unattended. Four input analog channels are sampled once per minute and outputted onto the magnetic tape. The system output tape and a Fortran II program is inputted into a Bendix G-20 computer. (This is done about once per week for convenience.) The G-20

computer outputs the data as continuous values of Faraday rotation. The data is outputted as a printed list, written on another magnetic tape, and plotted on a Calcomp plotter in the form of diurnal curves. A copy of one of these plots is shown in Figure 59. In this figure, three days of continuous data are shown. It is important to note that this plot was obtained directly from the data system's output tape. No other processing was required. To get the data in this form using the older, manual data reduction methods of the IRL, would have taken approximately 10 man hours for each day plotted. The data would first have to be scaled from the strip chart recordings, then the values would have to be punched on IBM cards, and finally the cards would have to be inputted to the computer. The computer would then output the data in the same fashion. This is the procedure that would have to be followed for reducing one type of data. In the future the IRL will be recording several different types of data. The number of man hours that the data logging system will save is quite obvious.

A copy of the IRL's Faraday reduction, and Calcomp plotting programs are not included with this work. They may be obtained from the IRL. A Fortran IV program is given in the appendix. This program will unpack the data recorded on the magnetic tape and arrange the data into individual channel arrays. This data may then be manipulated by other computer programs for further processing.

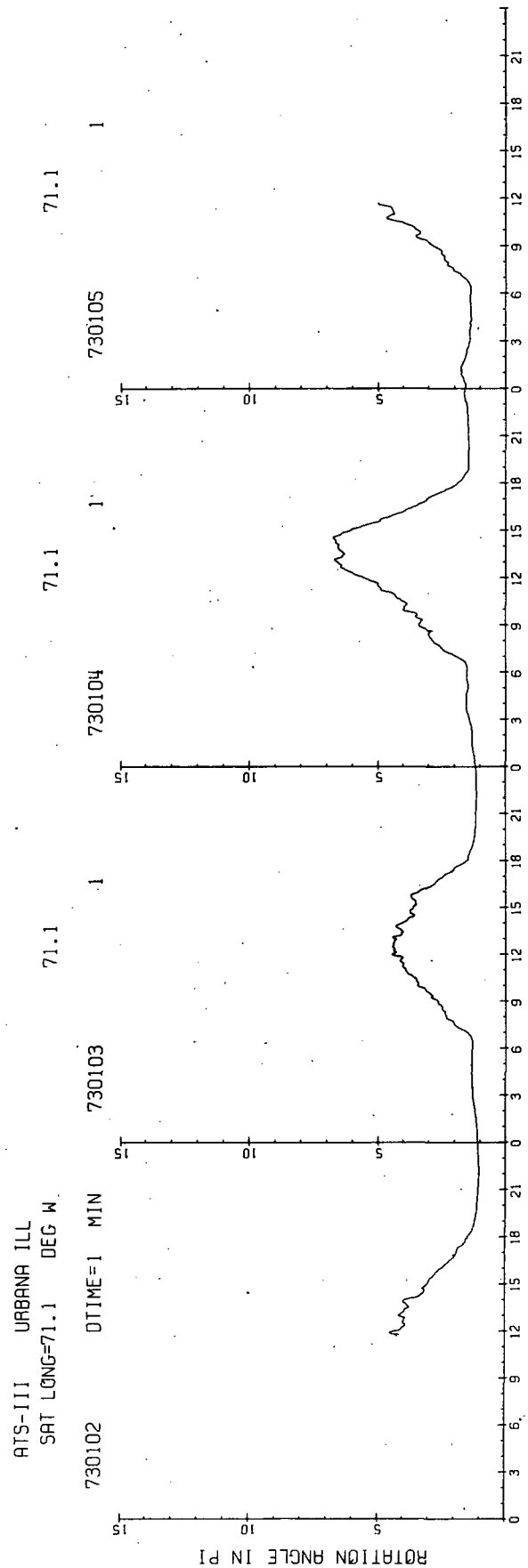


Figure 59. A Calcomp Plot of the relative Faraday rotation of a VHF signal from the ATS III satellite at Urbana, Illinois.

APPENDIX A

```
C     THIS PROGRAM READ THE TAPE INFORMATION IN 'A' FORMAT,DECODES,AND
C     PACK THE DATA
      LOGICAL*1 IE(2784)
      DIMENSION DATA(37)
C     PRINT HEADER INFORMATION
      WRITE(6,1)
    1 FORMAT(1H1,36X,'NUMBER OF',11X,'SAMPLING RATE')
      WRITE(6,2)
    2 FORMAT(1H ,7X,'CONTROL',14X,'YEAR',16X,'MONTH',15X,'DAY',16X,
     1'CHANNELS',11X,'IN SECONDS')
C     READ HEADER INFORMATION,'3' IS A TAPE READER UNIT
      READ(3,3)  (IE(I),I=1,24)
    3 FORMAT(24A1)
C     DECODE INFORMATION
      J=1
      DO 4 I=5,24,4
      CALL DECODE (J,DATA,I,IE,3,1)
    4 J=J+1
      WRITE(6,5)  IE(3),IE(2),(DATA(I),I=1,5)
    5 FORMAT(1H ,10X,2A1,9X,5(F12.0,9X))
C     READ AND DECODE THE DATA ACCORDING TO HEADER INFORMATION
      WRITE(6,6)
    6 FORMAT(1H ,'CON',' TIME ',' CHL  1',' CHL  2',' CHL  3',' CHL  4'
     1,' CHL  5',' CHL  6',' CHL  7',' CHL  8',' CHL  9',' CHL 10',
     2' CHL 11',' CHL 12',' CHL 13',' CHL 14',' CHL 15',' CHL 16')
      NCHAL=DATA(4)
C     CALCULATE NUMBER OF BYTES IN EACH SCAN
      KKK=1
      NBYTE=NCHAL*5+7
C     CALCULATE TOTAL NUMBER OF BYTES IN 32 SCANS
      NTOT=NBYTE*32
C     TOTAL NUMBER OF POINTS IN A RECORD
      IF=NCHAL+3
      ITOT=IF*32
   20 READ(3,7,END=80)  (IE(I),I=1,NTOT)
C     FORMAT STATEMENT 7 DEPENDS ON NUMBER OF CHANNELS RECORDED. THIS
C     PARTICULAR ONE IS FOR TWO CHANNELS. THE FORMULA IN GENERAL IS
C     32*(# OF CHANNELS*5+7)
    7 FORMAT(255A1,255A1,34A1)
C     CHECK END OF DATA
      IF(.NOT.IE(1))  GO TO 80
C     DECODE AND PACK DATA OF EACH RECORD
      DO 8 I=1,NTOT,NBYTE
      J=1
      LJ=I+2
      CALL DECODE(J,DATA,LJ,IE,4,1)
      KK=I+7
      DO 9 M=1,NCHAL
      J=J+1
      CALL DECODE(J,DATA,KK,IE,3,2)
    9 KK=KK+5
      WRITE(6,10)  IE(I),IE(I+1),(DATA(K),K=1,J)
   10 FORMAT(1H ,1X,2A1,1X,F6.0,16F7.4)
    8 CONTINUE
      WRITE(6,11)  KKK
   11 FORMAT(1H ,1X,'END OF RECORD NUMBER',I4)
      KKK=KKK+1
      GO TO 20
   80 CALL EXIT
      END
```

```
      SUBROUTINE DECODE(J,DATA,IB,IE,II,I)
      LOGICAL*1 IE(2784)
      LOGICAL*4 DUMY
      INTEGER   ICONV
      DIMENSION DATA(17)
      EQUIVALENCE (DUMY,ICONV)
      GO TO (10,20),I
   10 XNUM=0.0
      IF=IB+II
      DO 1  K=IB,IF
      DUMY=IE(K)
    1 XNUM=XNUM*10.0+(ICONV-240)
      DATA(J)=XNUM
      RETURN
   20 DUMY=IE(IB)
      A=ICONV
      JB=IB+1
      XNUM=0.0
      IF=JB+II
      DO 2  K=JB,IF
      DUMY=IE(K)
    2 XNUM=XNUM*10.0+(ICONV-240)
      XNUM=XNUM/10000.0
      IF(A.EQ.78.0)  DATA(J)=XNUM
      IF(A.EQ.96.0)  DATA(J)=-XNUM
      IF(A.EQ.241.0)  DATA(J)=1.0+XNUM
      IF(A.EQ.243.0)  DATA(J)=-(1.0+XNUM)
      IF(A.EQ.245.0)  DATA(J)=0.0
      IF(A.EQ.247.0)  DATA(J)=-0.0
      RETURN
      END
```

Note, this subroutine decodes the magnetic tape header information and the data. The data is packed into words that are five bytes long. The first byte is the voltage compression code character (see Section 3.3).

OUTPUT DATA FORMAT

CON	TIME	CHL 1	CHL 2	CHL 3	CHL 4	CHL 5	CHL 6	CHL 7	CHL 8
ES	12220.	0.3640	0.1747						
ES	12230.	0.3624	0.1731						
ES	12240.	0.3666	0.1768						
ES	12250.	0.3673	0.1782						
ES	12260.	0.3725	0.1825						
ES	12270.	0.3769	0.1870						
ES	12280.	0.3825	0.1921						
ES	12290.	0.3866	0.1957						
ES	12300.	0.3921	0.2013						
ES	12310.	0.3950	0.2045						
ES	12320.	0.3999	0.2090						
ES	12330.	0.4005	0.2097						
ES	12340.	0.4019	0.2108						
ES	12350.	0.4042	0.2129						
ES	12360.	0.4038	0.2125						
ES	12370.	0.4064	0.2148						
ES	12380.	0.4090	0.2176						
ES	12390.	0.4102	0.2187						
ES	12400.	0.4033	0.2119						
ES	12410.	0.4022	0.2101						
ES	12420.	0.3985	0.2069						
ES	12430.	0.3972	0.2055						
ES	12440.	0.3946	0.2031						
ES	12450.	0.3912	0.1990						
ES	12460.	0.3868	0.1952						
ES	12470.	0.3851	0.1939						
ES	12480.	0.3831	0.1917						
ES	12490.	0.3834	0.1913						
ES	12500.	0.3836	0.1918						
ES	12510.	0.3828	0.1907						
ES	12520.	0.3842	0.1931						
ES	12530.	0.3884	0.1973						
END OF RECORD NUMBER 1									
ES	12540.	0.3902	0.1992						
ES	12550.	0.3949	0.2039						
ES	12560.	0.4007	0.2106						
ES	12570.	0.4053	0.2160						
ES	12580.	0.4081	0.2193						
ES	12590.	0.4134	0.2244						
ES	13000.	0.4197	0.2311						
ES	13010.	0.4250	0.2374						
ES	13020.	0.4287	0.2410						
ES	13030.	0.4341	0.2461						
ES	13040.	0.4342	0.2464						
ES	13050.	0.4347	0.2471						
ES	13060.	0.4332	0.2459						
ES	13070.	0.4308	0.2434						
ES	13080.	0.4299	0.2427						
ES	13090.	0.4288	0.2414						
ES	13100.	0.4238	0.2367						
ES	13110.	0.4203	0.2331						
ES	13120.	0.4174	0.2291						

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13. ABSTRACT

This work discusses an analog-to-digital data logging system. The system was developed to record from one up to a maximum of sixteen channels of analog data onto magnetic tape. Each analog channel of data can be sampled at rates of 1, 2, 6, 12, or 60 times per minute.

The system is divided into three subunits: a digital clock, an incremental magnetic tape recorder, and a sequential converter. The interfacing requirements of these subunits are presented. The majority of this report is devoted to the operation and design of the sequential converter. Its design is presented in sufficient detail to allow for the duplication or adaptation of the system using a different digital clock or magnetic recorder.

A final summary of the system's capabilities completes the work. Major system concepts and methods of improving the system's hardware design are presented, and the present application of the system is discussed.

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14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
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