

INVESTIGATE OPTIMUM WAY OF
ADDING WIDEBAND CAPABILITY AND
RECOMMEND A DESIGN FOR MODIFICATION
OF ONE GOVERNMENT FURNISHED
AM BASEBAND DEMULTIPLEXER

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FINAL REPORT

CONTRACT NAS8-29039, MODIFICATION 1

PREPARED FOR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GEORGE C. MARSHALL SPACE FLIGHT CENTER
HUNTSVILLE, ALABAMA 35812

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APRIL 1973

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FOREWORD

This report is submitted in response to NASA/MSFC contract NAS8-29039, Modification 1. The report, in conjunction with Martin Marietta Aerospace report numbers MCR-72-198 and MCR-73-15, details the study phase, the hardware modification phase, and the test program required under Contract NAS8-29039 to prove the feasibility of wideband operation of one government furnished AM Baseband Demultiplexer, Adcom Model G-146.

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I. INTRODUCTION

The following report describes the hardware design and implementation and the test results of the accommodation of two wideband channels, 8 kHz DSB/QDSB located at 44 kHz and 16 kHz SSB, lower sideband, located at 104 kHz in a government furnished FDM demultiplexer unit, Adcom Model G-146. The Acceptance Test Plan for the demultiplexer, modified to wideband operation, is contained in Martin Marietta Aerospace Corporation Report No. MCR-73-15.

Originally the demultiplexer unit provides 1 kHz bandwidth operation in the DSB/QDSB mode and 10 Hz to 2 kHz operation in the SSB mode. The channel locations are from 4 kHz to 176 kHz with 4 kHz spacing, and a maximum of 24 channels can be utilized simultaneously. The pilot tone may be located at 4, 8, 16, 32, 64 or 128 kHz, and the reference or ambiguity channel may be at any odd multiple of 4 kHz. Two different demodulation techniques are employed in the demultiplexer. The lower channels, 4 kHz through 36 kHz, are up converted with a 160 kHz carrier, filtered and then down converted to baseband. Channels located at 40 kHz through 176 kHz are demodulated directly. The demodulation methods chosen require in-line filtering in all data channels, and filter matching is employed between the pilot channel and each individual data channel to reduce the effect of frequency modulation (FM) of the input signal caused by tape recorder wow and flutter.

Phase I of this contract was a study to analyze and test the Teledyne/Adcom Model G-146 demultiplexer to determine the feasibility and optimum method(s) for modifying the unit for broadband operation. The results of this study are contained in Martin Marietta Aerospace Corporation Report No. MCR-72-198, referred to as Reference 2, summarized as follows:

(a) A comparison of actual tape recorder wow and flutter and the ability of the demultiplexer pilot and carrier phase-locked loops to track the wow and flutter led to the conclusion that the performance would be suboptimum, especially in the QDSB mode, without extensive rework of all loops. Testing with frequency modulation of the input signal was therefore not proposed.

(b) The general conclusion was that the demultiplexer was not designed in such a way as to be easily converted to a high performance wideband system, however, to prove the feasibility of such conversion two approaches were outlined. Additionally two alternate approaches, both requiring breadboarding efforts rather than system rework, were presented.

The approach to be hardware implemented during Phase II of this contract includes the demodulation of the input signals by shorting the demultiplexer's in-line filters on the 44 kHz and 104 kHz channels, and also the 64 kHz pilot filter. No other channels can be demodulated during the demodulation of the two wideband; however, other channels may be demodulated by reinserting the pilot and reference filters and rerunning the input composite signal. Some higher channels may be demodulated simultaneously with the wideband channels by shorting their in-line filters. These channels are 148 kHz to 176 kHz. 4-28 kHz cannot be demodulated on the same tape run as wideband channels since filtering is always required for the up converted channels.

Channel modifications include:

- (i) New 16 kHz polyphase network
- (ii) Two 8 kHz lowpass output filters for the 44 kHz channel
- (iii) 16 kHz lowpass output filter for the 104 kHz channel

It should be noted that this system deviates from the design principles of the Adcom demultiplexer in the respect that channel-to-pilot filter matching is not employed. This modification, however, is useful to prove wideband operation in general.

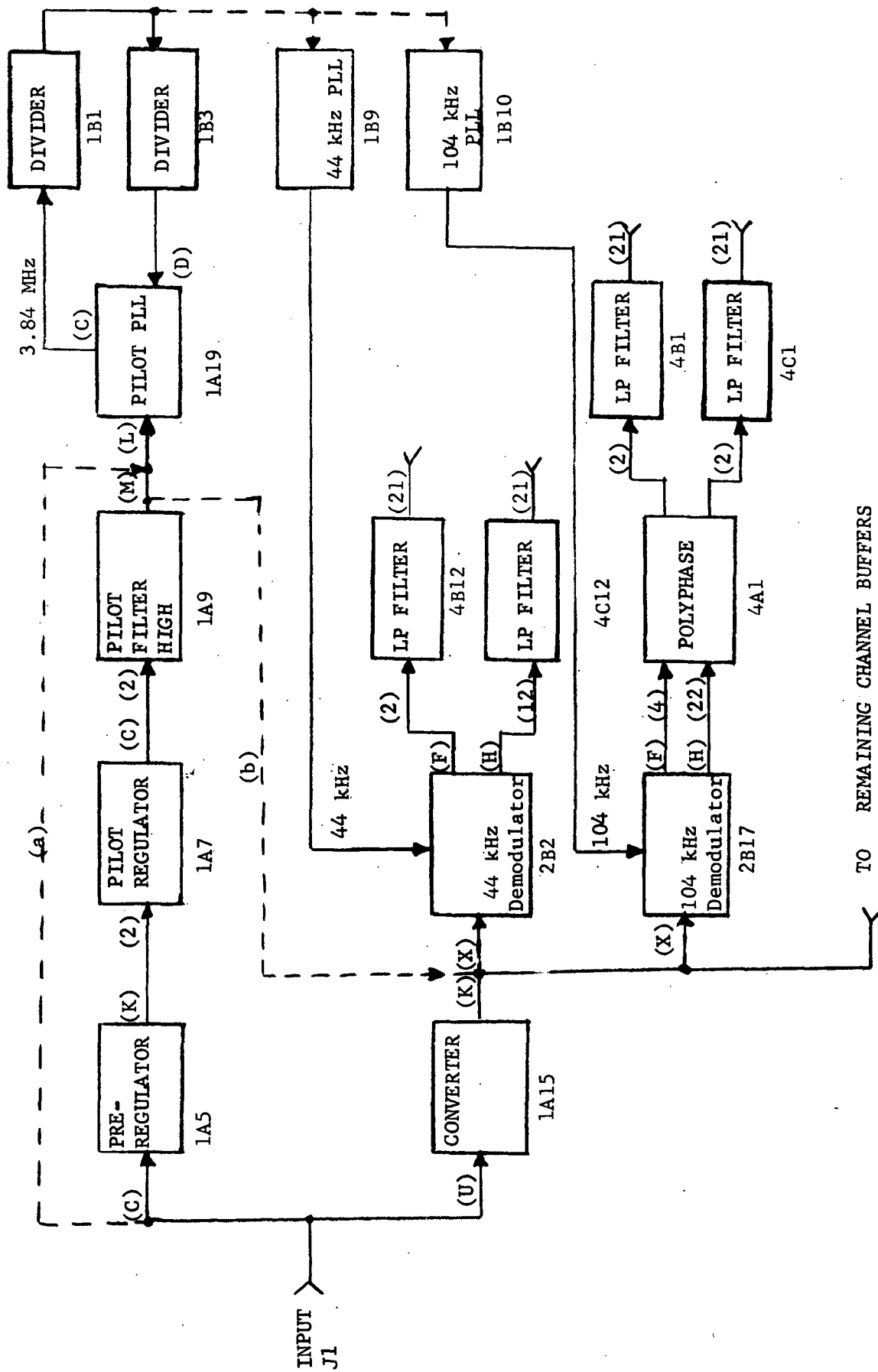
II. WIDEBAND MODIFICATIONS

A. GENERAL

Figure 1 shows the block diagram of the system circuits involved in the 8 kHz DSB/QDSB operation on the 44 kHz channel and the 16 kHz SSB operation on the 104 kHz channel. Circuit details for the original narrow band operation are described in Reference 1, Operation Manual for FDM demultiplexer Teledyne ADCOM Model G-146, Final Report Contract NAS8-30138, May 1970.

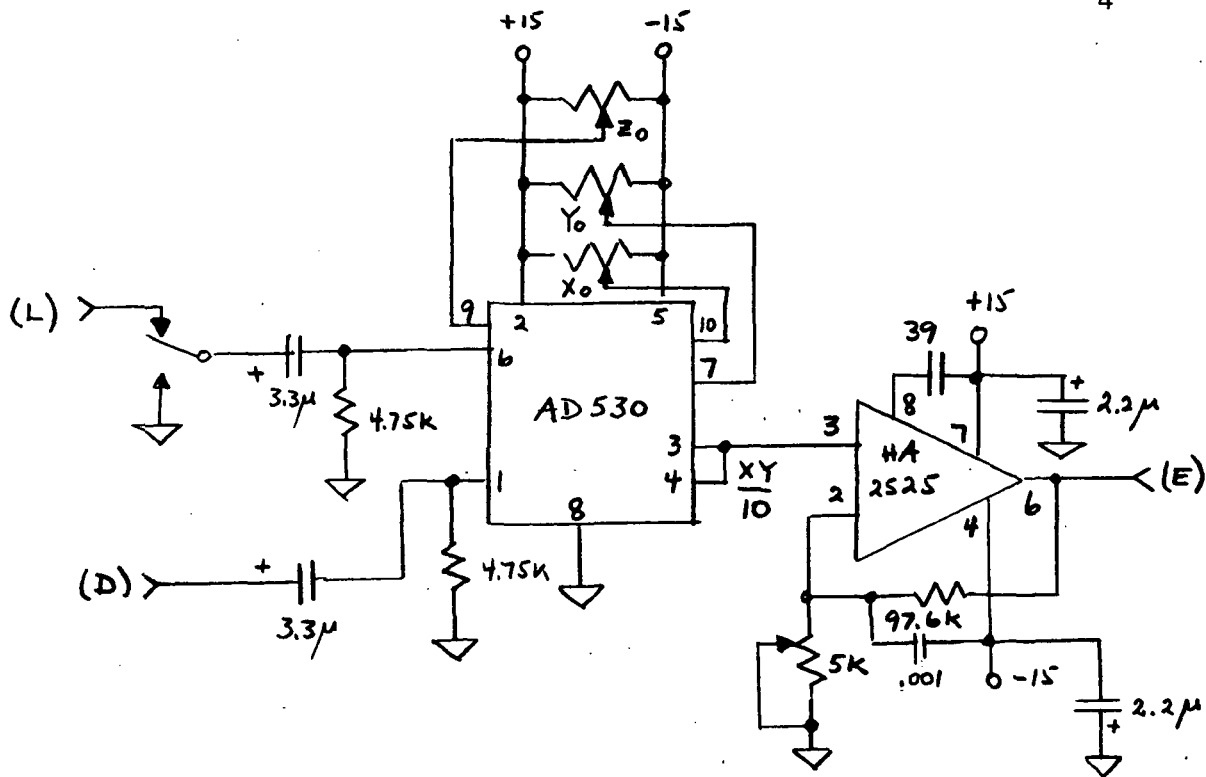
The pilot signal at 64 kHz is routed through the preregulator, pilot regulator and the pilot filter board to the pilot phase locked loop. The only modification in this path is the shorting of the 64 kHz pilot filter on the 1A9 board. Referring to Reference 1, this short is applied between the L1/L2 junction and the L4/L5 junction in Figure 5-6. Alternatively the pilot could be routed directly from the system input, J1, to the pilot PLL as shown by the dotted line (a) in Figure 1.

During wideband operation the pilot phase locked loop is modified as shown in Figure 2. A new, linear, nonsaturating, phase detector/driver is used in place of the saturating amplifiers and exclusive "OR" type phase detector shown in Figure 5-8 of Reference 1. The reason for this substitution lies in the fact that the pilot is no longer filtered, and the pilot signal will, therefore, not be dominant at the input of the phase detector. The input signal actually consists of seven signals at



Block Diagram of the 44 kHz and 104 kHz Wideband Channels

FIGURE 1



The New Phase Detector on the 1A19 Board

FIGURE 2

NOTE: The pin numbers of the phase detector in Figure 2 refer to the actual numbers on the 1A19 pilot PLL board. The pilot input is on pin L, the synthesized pilot input is on pin D, and the output is fed to the loop amplifier/filter via pin E.

To operate the 1A19 board with its original phase detector the following simple modifications should be made:

- (a) disconnect the red wire between pin E and pin 6 of the HA2525 amplifier.
- (b) replace jumper wire between pin E and the Q3-R23 junction (Figure 5-8 in reference 1).

approximately the same level as the pilot. These signals are two cophase and two quadrature sidebands in the 44 kHz channel, a single sideband in the 104 kHz channel and the reference signal at 68 kHz. The pilot is, therefore only about 1/7 of the total signal. The old squaring circuit will deteriorate this pilot-to-"noise" ratio an additional 6 dB by the capture effect, and the exclusive "OR" type phase detector output signal-to-noise ratio is so poor that the loop has difficulty locking on the control signal. The new AD530 phase detector operates on an input signal of approximately 2 vpp with a gain of -68 dB with respect to the pilot. Since both the detector and the drive amplifier operates in a nonsaturating mode, the capture effect will no longer reduce the control signal, and less uncertainty will exist in the loop. The gain of the amplifier is set to 47 dB giving a total dc loop gain of 119 dB, which is equivalent to that of the old loop. The 800 Hz roll-off on the HA2525 amplifier replaces that of the Q3 in Figure 5-8 of Reference 1. Since all "interference" signals on the input will be outside the pilot loop bandwidth, they will be attenuated, and the FM sidebands on the pilot output caused by these signals will be negligible with respect to system performance.

The loop performance with the new phase detector will therefore be identical to that of the original loop.

The input composite signal to be demodulated is routed through the buffer on the Converter board directly to the subcarrier filter and detectors of Figure 5-24 in Reference 1. Because of rather substantial gain on the detector board the maximum input level must be kept below 150 mV to prevent saturation. With this low signal level it was determined that the transient buffers, located at boards 2A11, 13, 15 and 17, must be bypassed because these drivers have output noise levels of the order of 1 mV, and if used, the signal-to-noise ratio at the detectors would be of the order of 40 dB rather than about 50 dB as is the level on the converter output. The bypassing of the buffer board is accomplished through a jumper wire from pin K on the 1A15 board to the unused pin X on the 44 and 104 kHz detector boards 2B2 and 2B17. Pin X on these boards are jumpered to the transient input contact on the board input switch in lieu of the jumper from the original transient signal input pin.

Wideband modifications to the 44 and 104 kHz demodulator/detector boards also include shorting of the in-line channel filters. This short is located between the L1/L2 and the L4/L5 junctions on Figure 5-24 of Reference 1.

The remaining wideband modifications are as follows:

(i) New polyphase network board in the 104 kHz channel, located in the 4A1 slot.

(ii) Two new 8 kHz low pass filters in the 44 kHz channel, located in the 4B12 and 4C12 slots.

(iii) New 16 kHz low pass filter, located in the 4C1 slot. The 4C1 path corresponds to the lower sideband in the 104 kHz channel.

Finally it should be pointed out that alternatively the composite signal could be routed through the regulator portion of the system rather than the transient data converter as shown with the dotted line (b) in Figure 1.

The reason this is not done is that the pilot AGC circuit employs synchronous demodulation of the pilot to provide the AGC control signal. With the above wideband modifications the pilot is no longer filtered on the AGC input, and interference from the remainder of the composite signal will be present on the AGC control signal causing amplitude modulation of the in-line signal. The amount of interference is dependent upon the time constant in the AGC circuit; however, the level of AM interference will not exceed -40dB, and the AGC'd composite signal may therefore be used for demodulation purposes and still meet the system requirements as stated in the Acceptance Test Plan, MCR-73-15.

B. DSB/QDSB OPERATION

The 44 kHz channel has been modified to handle DSB and QDSB modulation from dc to 8 kHz. The only new boards in the signal path are the output lowpass filters located in slots 4B12 and 4C12. The filters are identical 7 pole Chebychev with 0.1 dB ripple. The circuit schematic is shown in Figure 9. Amplifiers U1 and U5 are buffer stages, and U2 through U4 and associated components comprise the actual filter. Minor adjustments R6, R10, R14, and R17 are provided for minimum ripple tuning. Since the filter contains high Q stages, four pads are reserved for each filter capacitance. This is done to achieve high accuracy of the capacitance values without extensive measurements, by paralleling capacitors.

C. SSB OPERATION

The 104 kHz channel has been modified to handle SSB modulation from 80 Hz to 16 kHz. Since the contemplated input signal will be the lower sideband, only the lowpass filter in the LSB location, 4C1, required a new filter. This filter is similar to the new 44 kHz channel filters. The only difference is resistance values as shown in Figure 9. The polyphase network board, 4A1, has been redesigned to accommodate the 80 Hz to 16 kHz bandwidth. The circuit schematic of this new board is shown in Figure 10. Amplifiers U1 and U7 are input buffers, and U2 through U6 and U8 through U12 comprise the polyphase network. The polyphase network is composed of two separate all pass networks as shown in Figure 3.

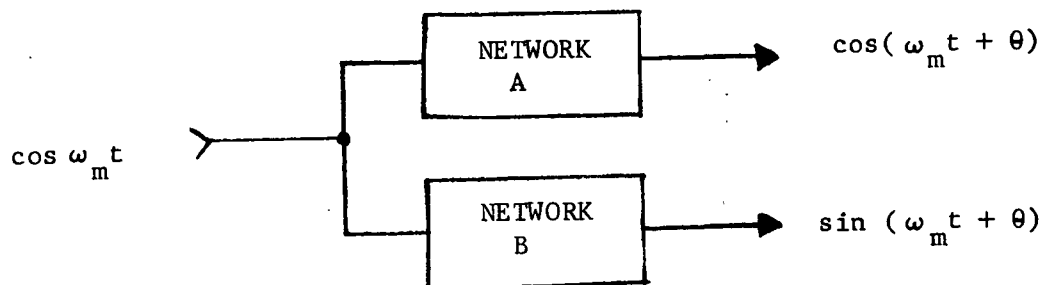
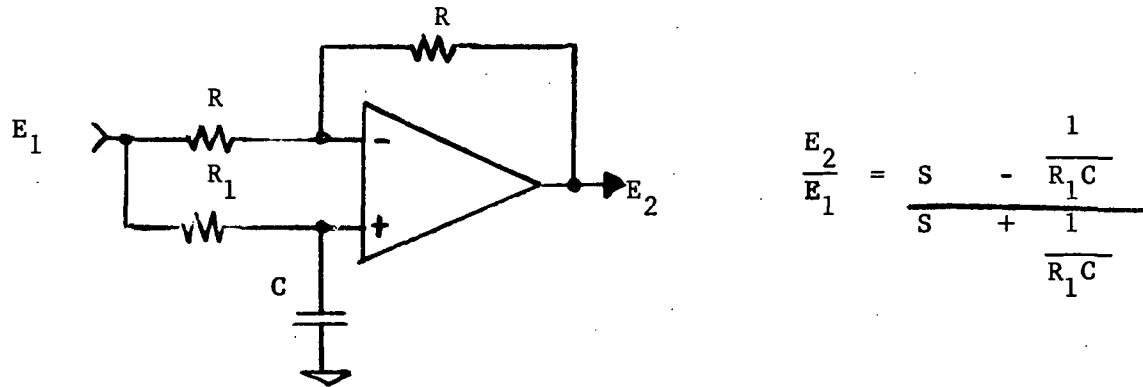


FIGURE 3. PHASE DIFFERENCE NETWORK

The networks A and B are Chebychev equal ripple type approximations. The phase difference on the output of the two networks is controlled to $90 \pm 0.16^\circ$ over the bandwidth 80 Hz to 16 kHz, corresponding to better than 50 dB suppression of the unwanted sideband within this bandwidth. The networks are implemented using the amplifier in Figure 4 to synthesize the pole frequencies required by the overall transfer function.



POLE-ZERO ALL-PASS PHASE SHIFTER
FIGURE 4

The pole-zero locations were determined using a computer program developed under contract NAS8-24682, and are as follows with respect to Figure 10:

AMPLIFIER	POLE FREQUENCY (HZ)
U2	27.31
U3	205.25
U4	808.27
U5	3113.40
U6	13546.70
U8	94.49
U9	411.12
U10	1583.62
U11	6236.16
U12	46867.30

The remaining circuits in Figure 10 perform addition and subtraction of the polyphase network outputs. U13 is an adder, and its output is the lower sideband in the channel. U15 performs the subtracting function, and its output would be the upper sideband in the channel, if present. Switches S1 and S2 are, as in the original channel, performing DSB, QDSB and SSB signal routing into the two channel output filters depending on the channel mode of operation.

D. TEST TOOL

During the performance of the functional testing of the wideband modified demultiplexer unit as outlined in the Acceptance Test Plan. The input signals will be supplied by the airborne FDM unit, Code 04236, Serial No. 001, as modified for wideband operation in contract NAS8-25987, Modification 5, with the addition of a 44 kHz QDSB test tool as shown in Figure 5 and 6. The FDM airborne unit, as modified to wideband operation, is described in Reference 3. Prior to testing, the test tool must be verified operational as follows:

- (a) Verify that the 44, 64, 68 and 104 kHz carriers in the FDM unit are locked to the system comb signal.
- (b) Set the FDM 44 kHz audio input to 2.5 vdc.
- (c) With 5 vpp audio inputs at A1, A2 and A3 adjust output levels to the values shown in Figure 5.
- (d) Adjust the test tool phase shifter to exactly 90° with R1 in Figure 6.
- (e) Adjust feedthrough signals in the 104 kHz channel and at the outputs of the AD422 multipliers to a minimum.

III. ALIGNMENT OF THE WIDEBAND CHANNELS

A. GENERAL

To insure proper operation of the demultiplexer the following steps should be undertaken:

- (a) Connect the 68 kHz subcarrier output to the ambiguity input.
- (b) Verify pilot PLL lock-in condition by adjusting R14 in Figure 5-8 of Reference 1.
- (c) Verify lock-in of the 44 and 104 kHz subcarrier PLL's at the test points on boards 2B2 and 2B17. The lock-in phase adjustments are on boards 1B9 and 1B10 respectively.

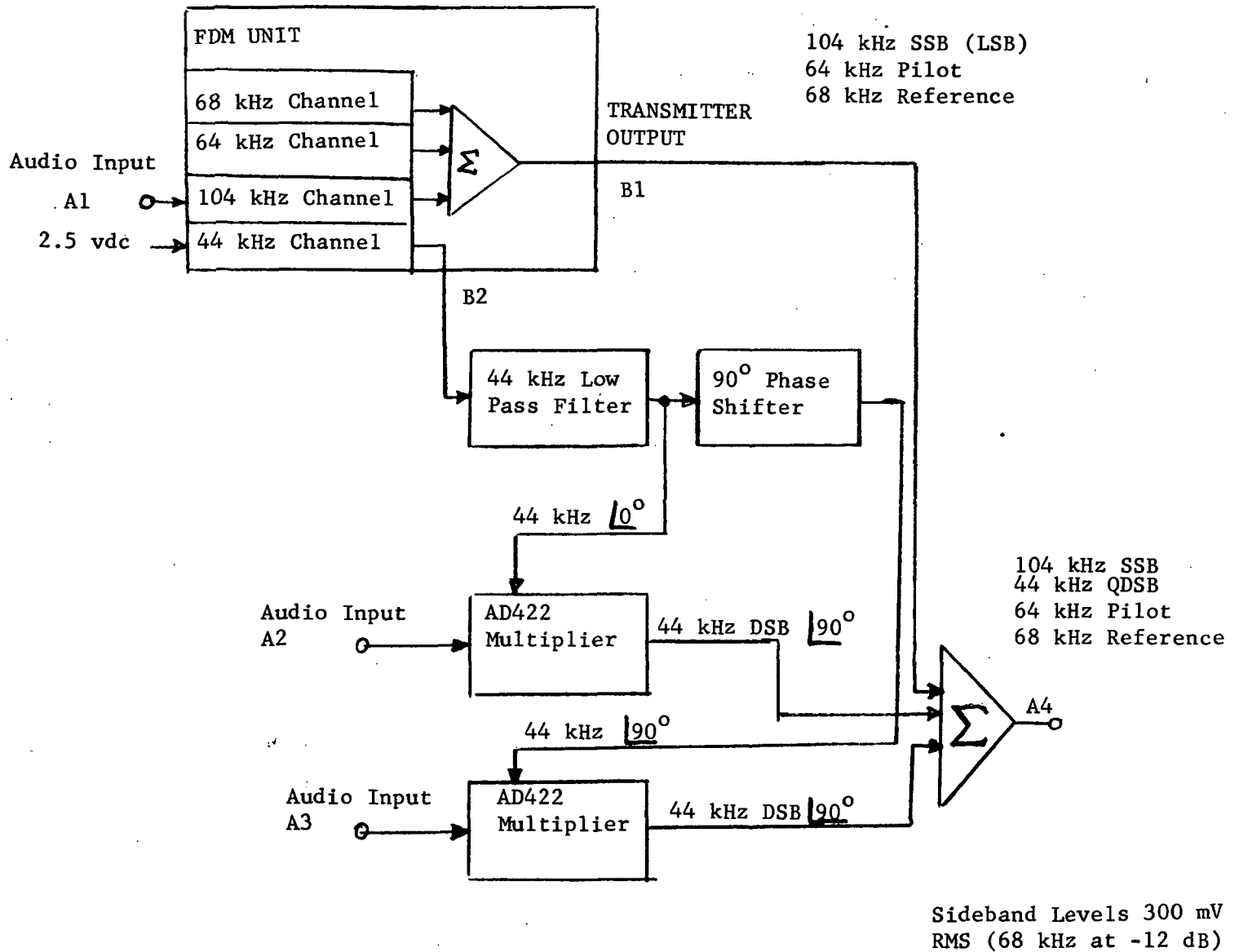


FIGURE 5
INPUT SIGNAL TEST TOOL

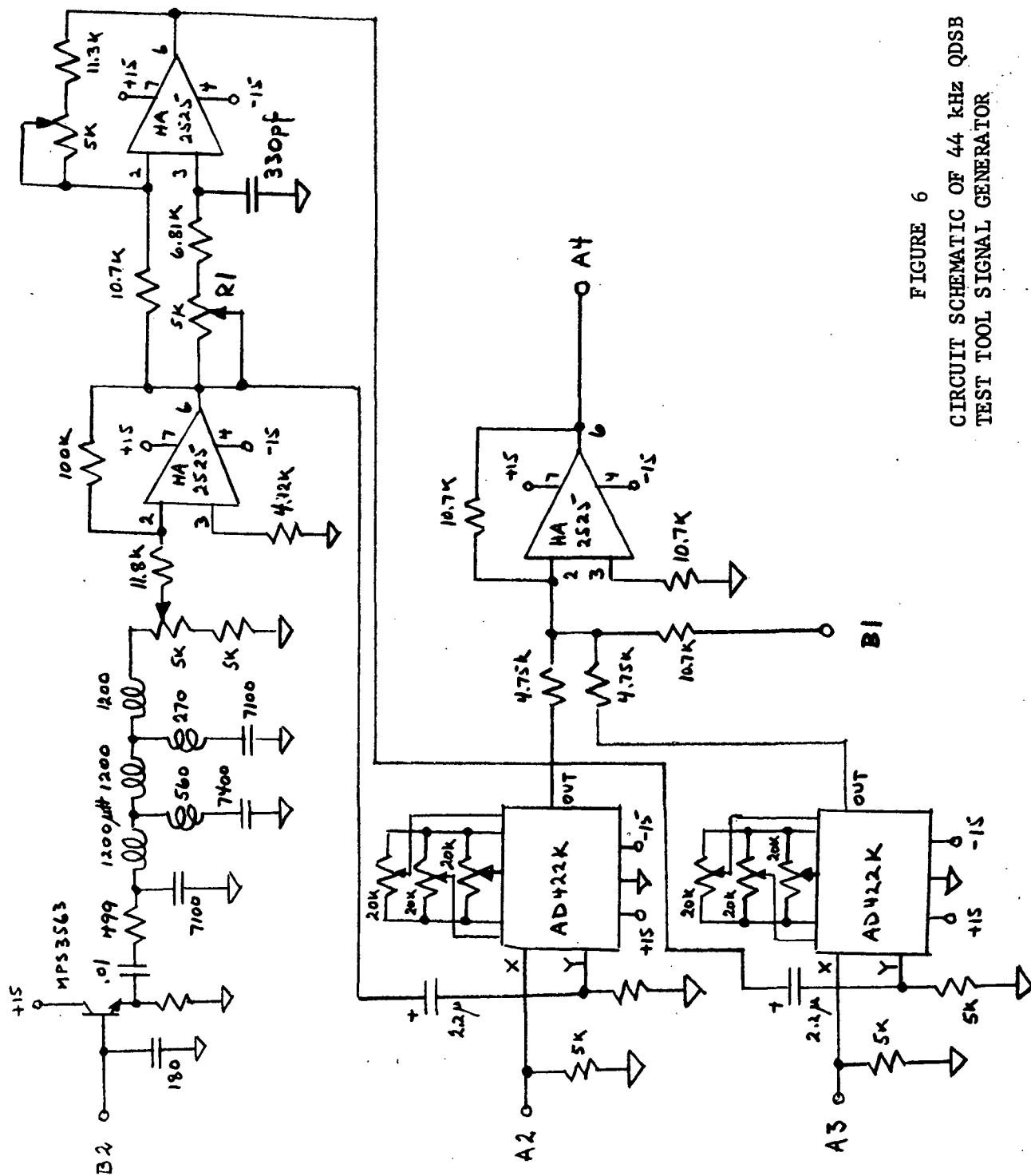


FIGURE 6
CIRCUIT SCHEMATIC OF 44 kHz QDSB
TEST TOOL SIGNAL GENERATOR

(d) The MODE switch on 4A1 shall be in the SSB position, and the BW SELECT switch shall be in the LSB - 16 kHz position.

(e) The MODE switch on the polyphase board, 4A12, shall be in the DSB position, and the BW SELECT switch shall be in the DSB - COPHASE - 8 kHz position.

(f) Adjust R6 on the 1A15 Converter board to a maximum level of about 50 mV per sideband to prevent saturation on the subcarrier detector boards.

(g) Adjust R10 and R19 on the 1A7 Pilot Regulator board for approximately 2 vpp amplitude of the composite signal at the pilot PLL input (the pilot sideband level at 64 kHz should be approximately 150 mV.)

B. DSB/QDSB ALIGNMENT

The alignments in the 44 kHz channel are as follows:

(a) The gain on the 2B2 is determined by R19. This potentiometer is adjusted to prevent signal saturation at the emitters of Q7 and Q8.

(b) The balance resistor, R25, is adjusted to give maximum quadrature suppression.

(c) Resistors R39 (course) and R42 (fine) is the COPHASE phase adjustment to be adjusted for maximum signal in the COPHASE channel.

(d) R45 is the quadrature or 90° phase adjustment to be adjusted for maximum quadrature suppression. The adjustment varies the symmetry of the carrier at the test point on the 2A2 board.

(e) Finally the output amplitude can be adjusted on the 4B12 and 4C12 boards by gain adjustments on U5 in Figure 9.

C. SSB ALIGNMENT

The polyphase network on the 4A1 board has been prealigned as shown in Figure 7.

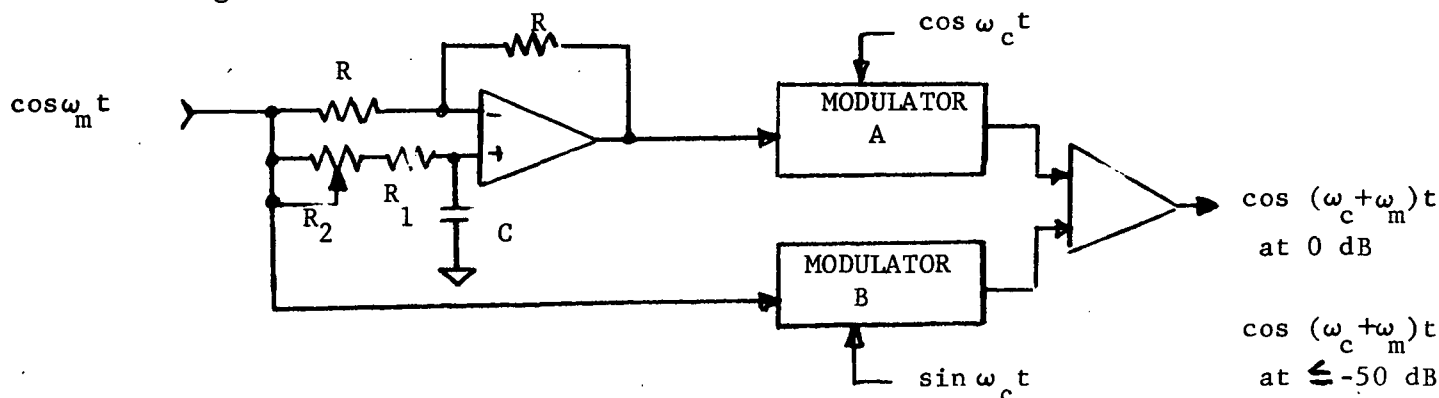


FIGURE 7. POLE-ZERO ALL-PASS PHASE SHIFTER ALIGNMENT
CIRCUIT

Each pole in the network is aligned individually by applying the precise pole frequency, as listed in paragraph II.C, to the phase shifter and to modulator B. The modulators A and B operating with quadrature carriers are summed to produce single sideband. When the phase shift across the phase shifter is adjusted to exactly 90° , the unwanted sideband will exhibit maximum suppression. Therefore, by monitoring the output of the summer with a wave analyzer, R2 of the phase shifter can be adjusted to exactly 90° at the pole frequency.

The functional alignments in the 104 kHz channel are similar to those of the 44 kHz channel as follows:

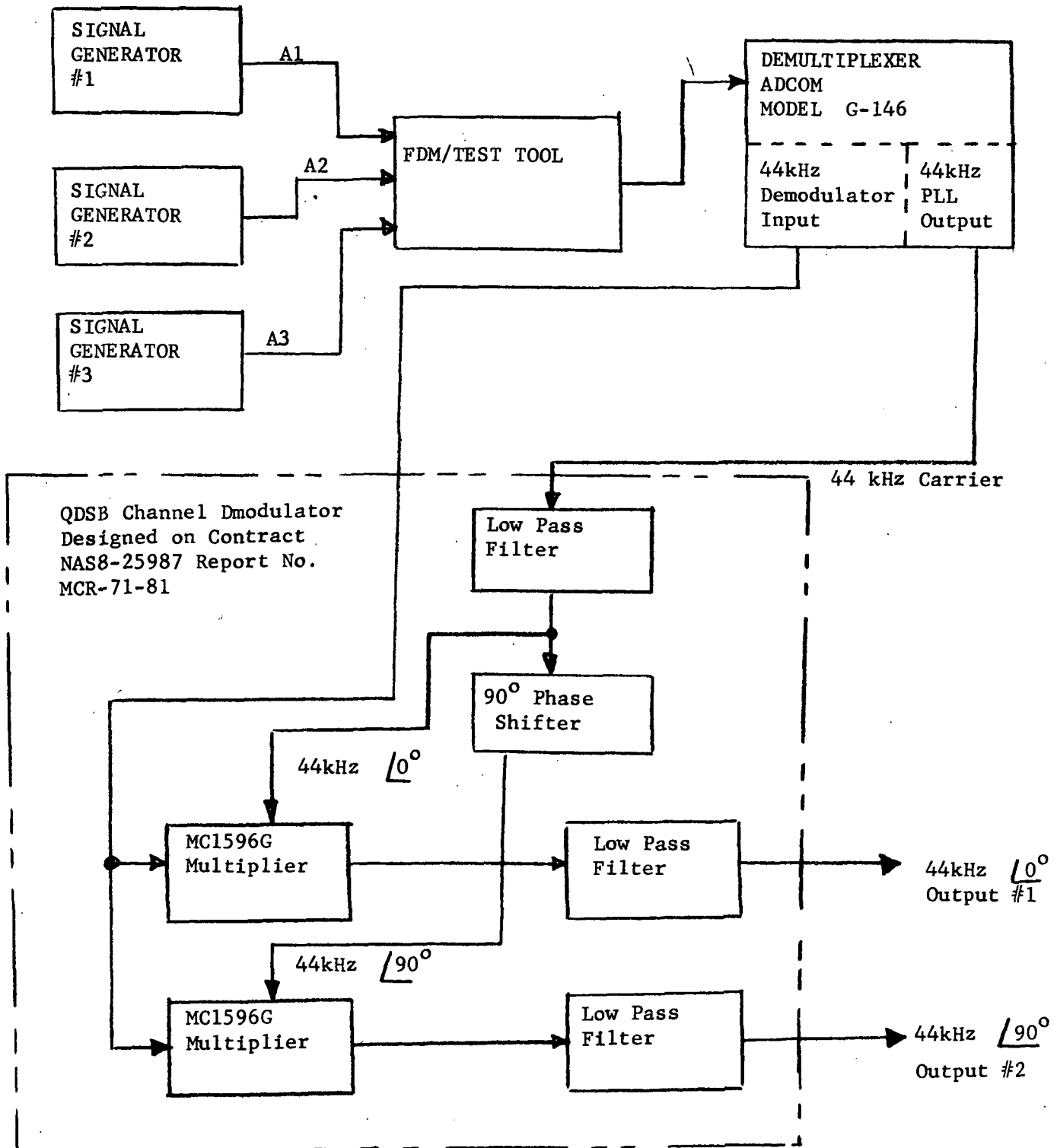
- (a) R19 on the 2B17 board is adjusted to prevent channel saturation.
- (b) R25 and R45 are adjusted for maximum suppression of the unwanted sideband.
- (c) R39 and R42 need not be adjusted since these will only cause phase shift of the audio in the SSB mode.
- (d) In Figure 10 R56 and R67 adjust high and low sideband rejection respectively. R61 and R72 are channel gain potentiometers, and R59 and R70 adjust the channel dc offsets.

IV. TEST PROGRAM

Due to some unexpected discrepancies which became apparent during the initial functional testing of the demultiplexer unit, some additional testing using a breadboard type demodulator in place of the 2A2 detector board was performed. The breadboard demodulator is shown in Figure 8, and consist of QDSB balanced demodulators with associated 90° carrier phase shifter and output low pass filters. This breadboard was designed on a previous NASA/MSFC contract, NAS8-25987, and was available for use during this contract.

The unexpected results obtained using the 2B2 board for demodulation of the 44 kHz QDSB signal are commented upon in Paragraph VI of this report.

FIGURE 8

44 kHz QDSB BREADBOARD
CHANNEL DEMODULATOR

V. TEST RESULTS

The frequency division demultiplexer Teledyne/Adcom Model G-146, with wideband modifications as described in previous sections of this report, was tested in accordance with Acceptance Test Procedure MCR-73-15. The acceptance test was performed by Martin Marietta Aerospace, Denver Division, to show compliance with the requirements of contract NAS8-29039, Modification 1. The tests proved the performance of the wideband modified FDM demultiplexer unit to exceed all requirements as stated in MCR-73-15.

The acceptance test results are summarized in the following section, and are referenced with paragraph numbers corresponding to those found in Acceptance Test Procedure MCR-73-15. The actual laboratory test data sheets are in Figures 11 thru 35.

The functional tests of the input signal test tool, as outlined in Section II of MCR-73-15, were performed, and proper operation of the test tool was verified prior to the execution of the Acceptance Test.

1. Distortion Products - 104 kHz Channel

All harmonics and unwanted frequency were suppressed 40 dB, or more, with respect to the desired audio frequency as verified by attached plots, Figures 11 and 12, corresponding to procedure steps B and D respectively.

2. Distortion Products - 44 kHz Channel

Using the breadboard channel demodulator of Figure 8 all output amplitudes other than the desired audio signals were suppressed by 40 dB or more. The suppression of the quadrature channel audio exceeded the 35 dB test requirement. Those results are verified by the output spectra shown in Figures 17 thru 20.

The data shown in Figures 13 thru 16 are commented upon in Section VI of this report.

3. Quadrature Suppression - 44 kHz Channel

Using the breadboard channel demodulator of Figure 8 the quadrature suppression for the 44 kHz channel exceeds 35 db for all frequencies between 100 Hz and 8 kHz, as verified by Figures 23 and 24.

The data shown in Figures 21 and 22 are commented upon in Section VI of this report.

4. Amplitude Linearity - 104 kHz Channel

The linearity of the 104 kHz channel was within the ± 0.1 dB test requirement. The actual data is presented in Figure 31.

5. Amplitude Linearity - 44 kHz Channel

The linearity of both the cophase and the quadrature channels was within the ± 0.1 dB test requirement. The actual data is presented in Figure 32.

6. Frequency Response and Upper Sideband Rejection - 104 kHz Channel

The frequency response of the 104 kHz channel was flat to within 0.2 dB from 80 Hz to 16 kHz, and the upper sideband rejection exceeded 35 dB over the full frequency range as verified by Figures 25 and 26.

7. Frequency Response - 44 kHz Channel

Using the breadboard channel demodulator of Figure 8 the frequency response from DC to 8 kHz of both the cophase and the quadrature channels were found to be flat within 0.2 dB as verified by Figures 29, 30, and 34.

The data shown in Figures 27 and 28 and 33 are commented upon in Section VI of this report.

8. Output Impedance

The output impedance of all relevant demodulator outputs were found to be below 10 ohms. The actual data is shown in Figure 35.

VI. TEST RESULT COMMENTS

During the preliminary testing of the Adcom G-146 demultiplexer with wideband modifications two unexpected discrepancies became apparent. The acceptance test plan were written such that these effects would be documented, while at the same time wideband performance of the demultiplexer would be proven.

Both discrepancies are related to the operation of the original equipment subcarrier detectors shown in Reference 1, Figure 5-24, and the effects show up in Acceptance Test Plan Procedures III.2,3 and 7.

During the Harmonic Distortion Test, paragraph III.2 and the Quadrature Suppression Test, paragraph III.3, a 7 kHz spurious response at -20 dB was present at the output of the 44 kHz channel, as can be seen in Figures 13 through 16 and 21 and 22 of this report. This spurious response is a direct effect of the 9 kHz audio applied to the 104 kHz channel during these tests in the following way: The 9 kHz SSB audio will cause a sideband at 95 kHz in the 104 kHz channel. This sideband will be present at the 44 kHz subcarrier detector input, and will be detected as $(95-88)$ kHz = 7 kHz by a peculiar second harmonic effect of the half wave rectifier/chopper type detector. From this it is evident that if the original equipment detector is used in the wideband modified channels the restrictions on input signals, as described in the study report of this contract, Reference 2, must be expanded to include the band 88 ± 16 kHz.

During the Frequency Response Test, Paragraph III.7 of the Acceptance Test Plan, a 4 dB discrepancy was found between the dc and ac responses in the 44 kHz channel when using the original equipment subcarrier detector as evident from Figure 33. The cause of this discrepancy again is the detector itself. As mentioned above the detector is a synchronous half wave rectifier/chopper, however, the drive voltage to the chopping field effect transistor (2N3819) is ± 2.5 volts, and depending on the pinch-off voltage of the transistor and the instantaneous value of the in-line signal the FET WILL NOT ALWAYS BE NONCONDUCTING WHEN REQUIRED TO. The chopper will sometimes operate in a semi-off condition and thereby attenuate the channel output signal. From this it follows that the detector operation will be slightly different with dc and ac modulation in the channel, since the actual subcarrier signals versus time will be different for dc and ac modulation.

It should be noted that the above discrepancies are inherent in the original equipment design, and that the frequency response effect will also be present in the original narrowband operation of the demultiplexer.

To prove proper operation of the demultiplexer the above three tests were performed using MC 1596 balanced modulators in place of the chopper type detectors with the result that all spurious signals were suppressed more than 40 dB, and the frequency response was flat to within 0.2 dB as required.

VII. REFERENCES

1. Operation Manual for FDM Demultiplexer Teledyne/ADCOM Model G-146, Final Report Contract NAS8-30138, May 1970.
2. Investigate Optimum Way of Adding Wideband Capability and Recommend a Design for Modification of One Government Furnished AM Baseband Demultiplexer, Study Report Contract NAS8-29039, Phase I, MCR-72-198.
3. Linear Modulator, Contract NAS8-25987 Modification 5, MCR-73-91 (Wideband Modifications to Airborne FDM Unit Code 04236, Serial No. 001).

VIII CONCLUSIONS

As pointed out in Paragraphs I, II.A and VI of this report and Paragraphs II.B, C, D, and E of Reference 2, the Adcom Mode G-146 demultiplexer has not been designed in such a way that high performance data can be readily processed neither in a narrowband nor in a wideband configuration. The wideband modifications performed under this contract have proven the wideband operation of the demultiplexer to be of similar quality to that of narrowband operation. Generally, spurious suppression exceeds 40 dB and quadrature suppression is in excess of 35 dB. The main reasons for this suboptimum performance lie in inadequate phase-locked loop performance with respect to tape recorder wow and flutter; the management of signal levels in the sense that at some points in the system the data levels are too close to the noise floor; and in inadequate shielding and routing of cables/wires so as to cause pick up problems.

However, the wideband modification exercise has been useful in as much that the final problems associated with high quality frequency division multiplexing or demultiplexing systems have been pin pointed, and the solutions to these problems are well understood.

IX. RECOMMENDATIONS

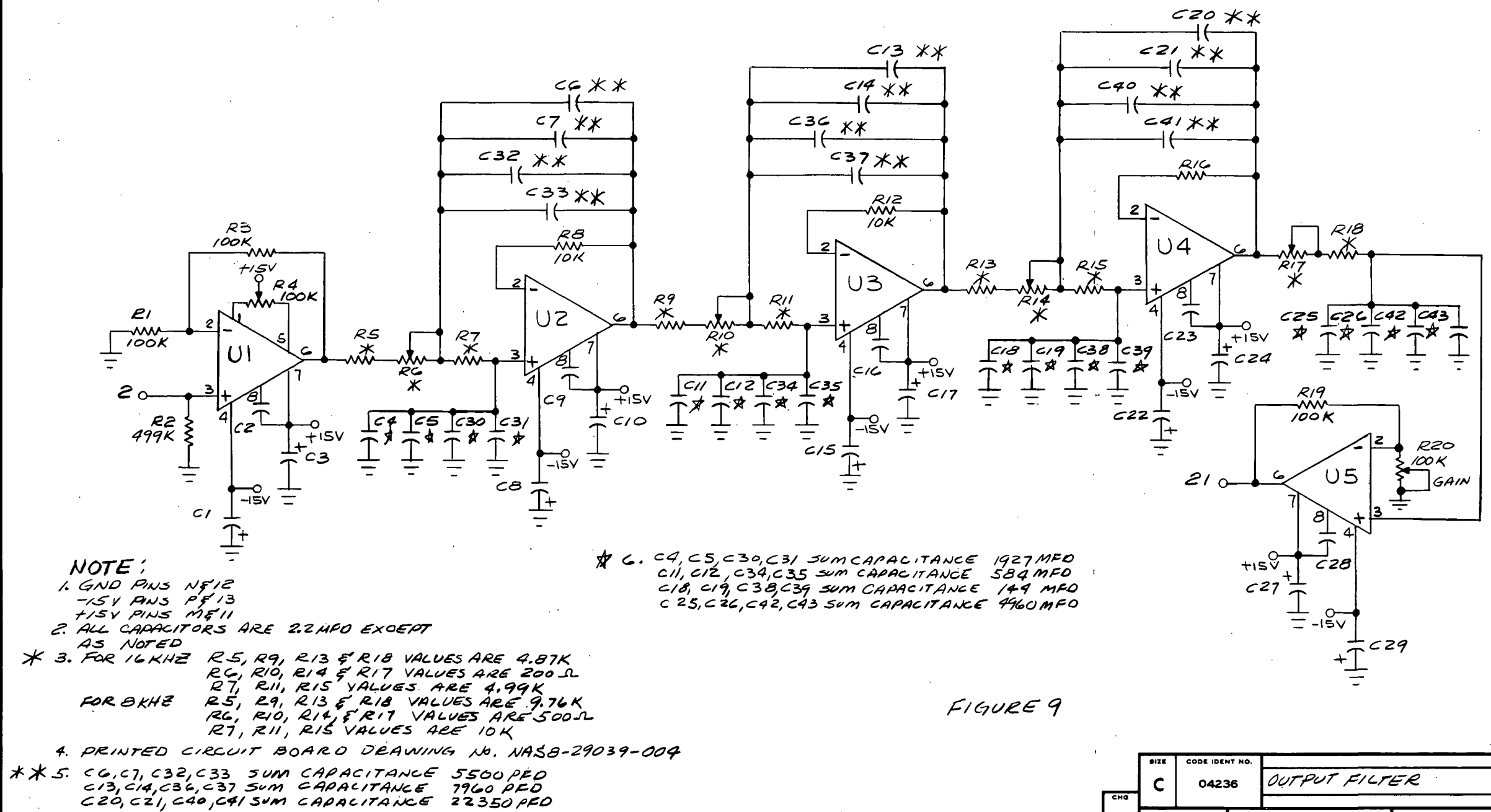
During the last three years the Martin Marietta Aerospace Corporation has been continuously involved in AM-FDM work in collaboration with MSFC on contracts NAS8-24682, NAS8-25987 and NAS8-29039. In summary this effort has produced the following conclusions.

(a) 50 dB spurious suppression systems are feasible in both DSB, QDSB and SSB with up to 16 kHz channel bandwidth.

(b) System accuracies of the order of 1% is feasible, even when a tape recorder is used in the link between the modulator and the demodulator.

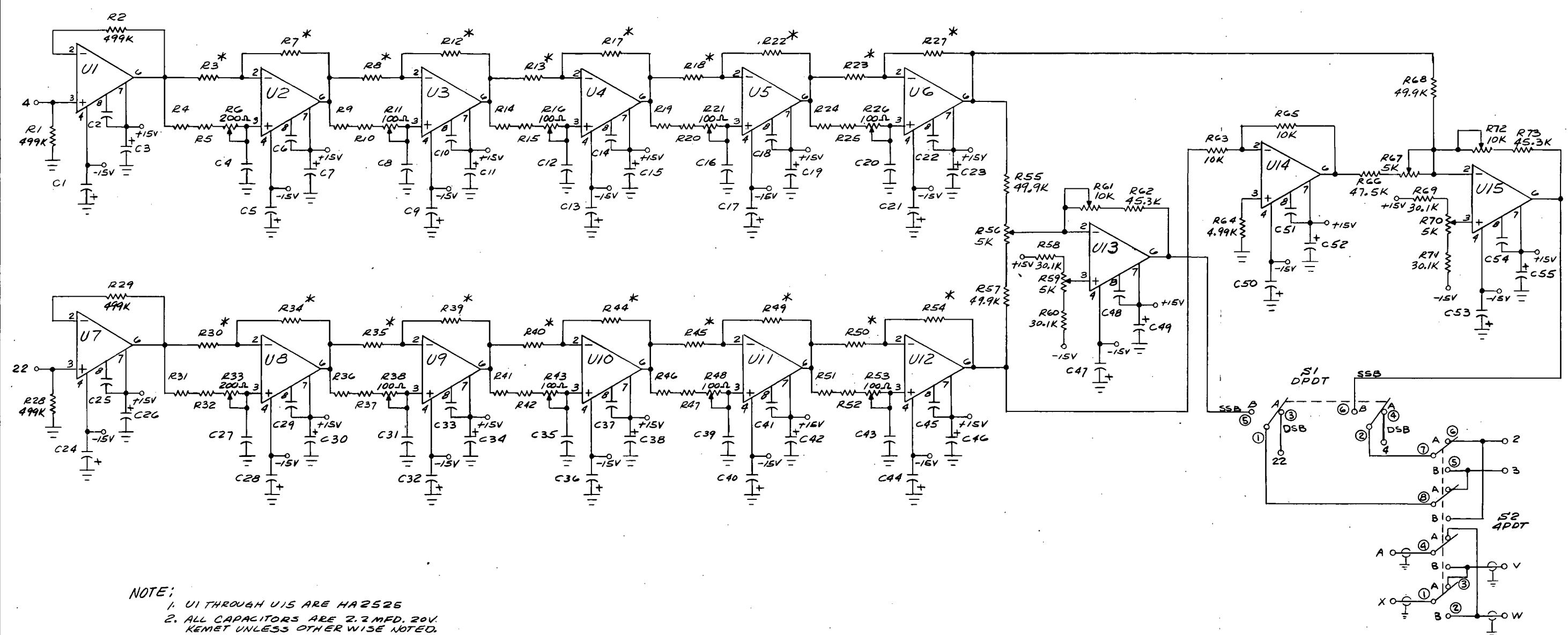
The recommendations based upon the total MMA effort is to utilize DSB in a multichannel FDM system with respect to cost, quality and performance. QDSB is recommended for higher channel density systems.

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED



SIZE	CODE IDENT NO.	
C	04236	OUTPUT FILTER
CHG		
SCALE	NASB-29039-002	SHEET 1 OF 1

REVISIONS			
SYM.	ZONE	DESCRIPTION	DATE

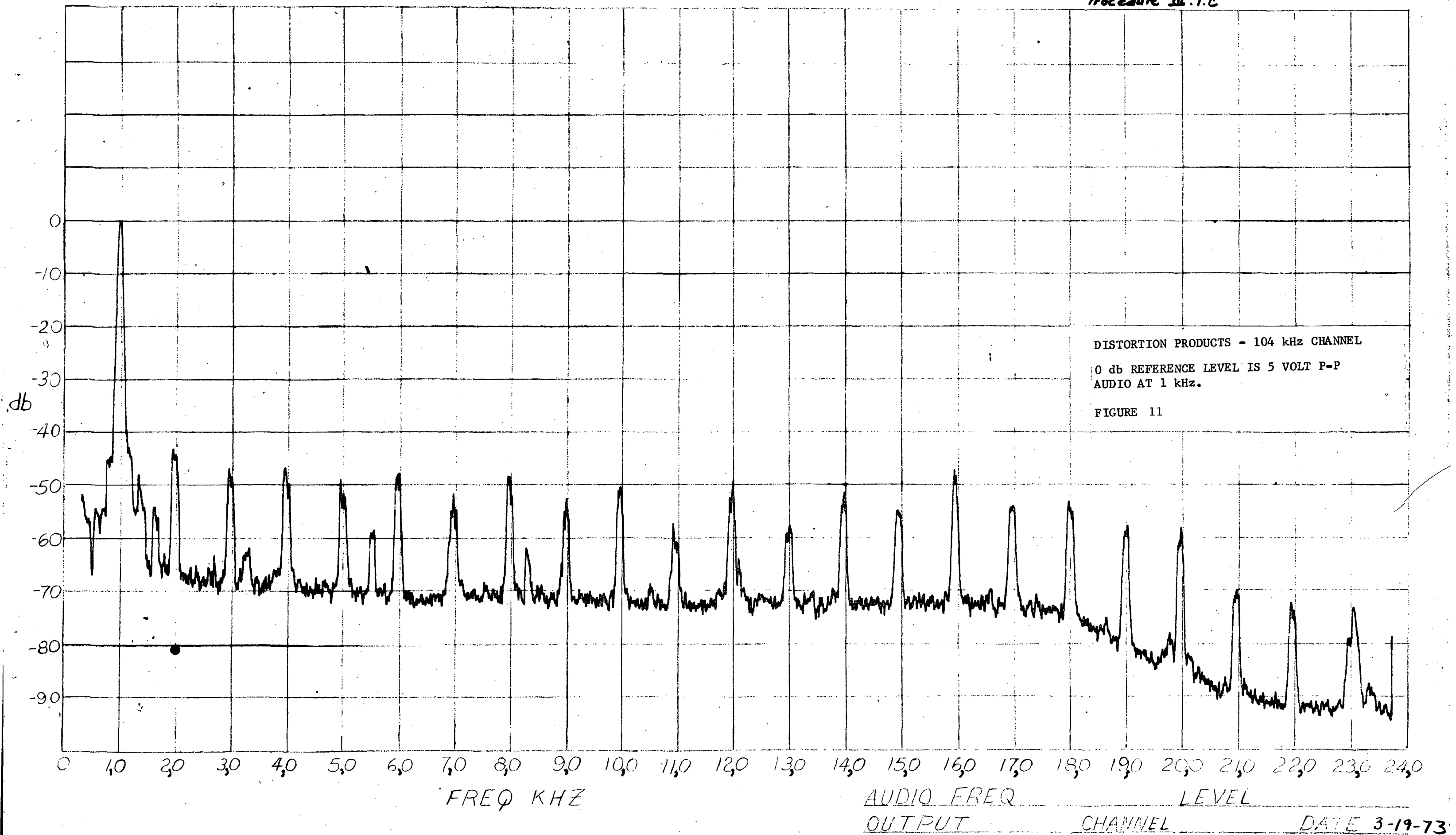


- NOTE:
1. U1 THROUGH U15 ARE HA2525
 2. ALL CAPACITORS ARE 2.2MFD. 20V. KEMET UNLESS OTHERWISE NOTED.
 3. LAST R NO. 73
C NO. 55
U NO. 15
S NO. 2
 4. * ALL 10K PAIRS MATCHED
 5. ○ INDICATES NUMBER TERMINAL ON P.C. BOARD
 6. ○ USE SHIELDED CABLE FROM NUMBERED TERMINALS TO EDGE CONNECTOR
 7. +15V PINS P & 13
-15V PINS M & 11
GND PINS N & 12
 8. PRINTED CIRCUIT BOARD NO. NASB-29039-003

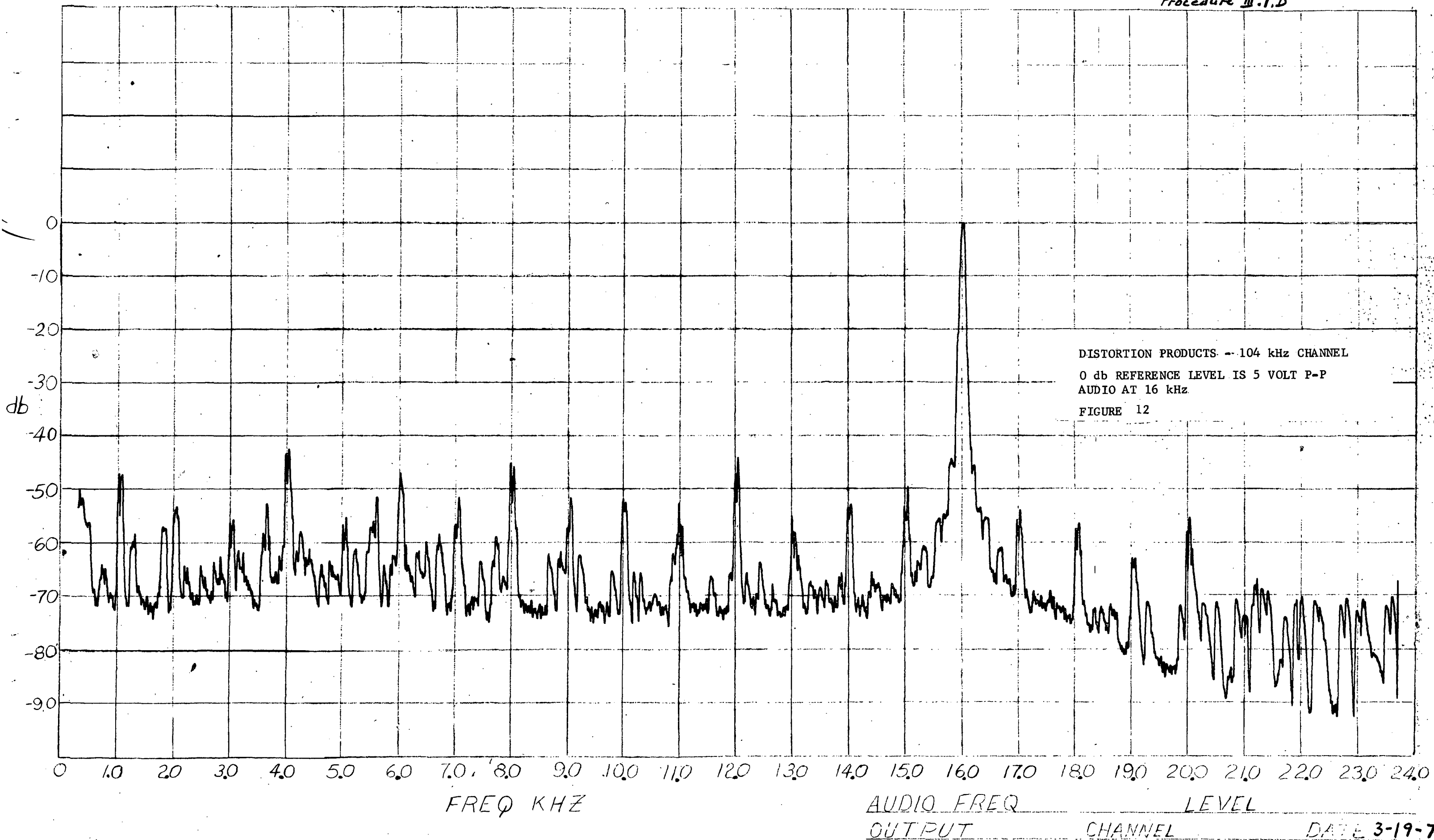
FIGURE 10

SIZE	CODE IDENT NO.	16KHZ SSB
D	04236	
SCALE	NAS 29039-001 SHEET 1 OF 1	

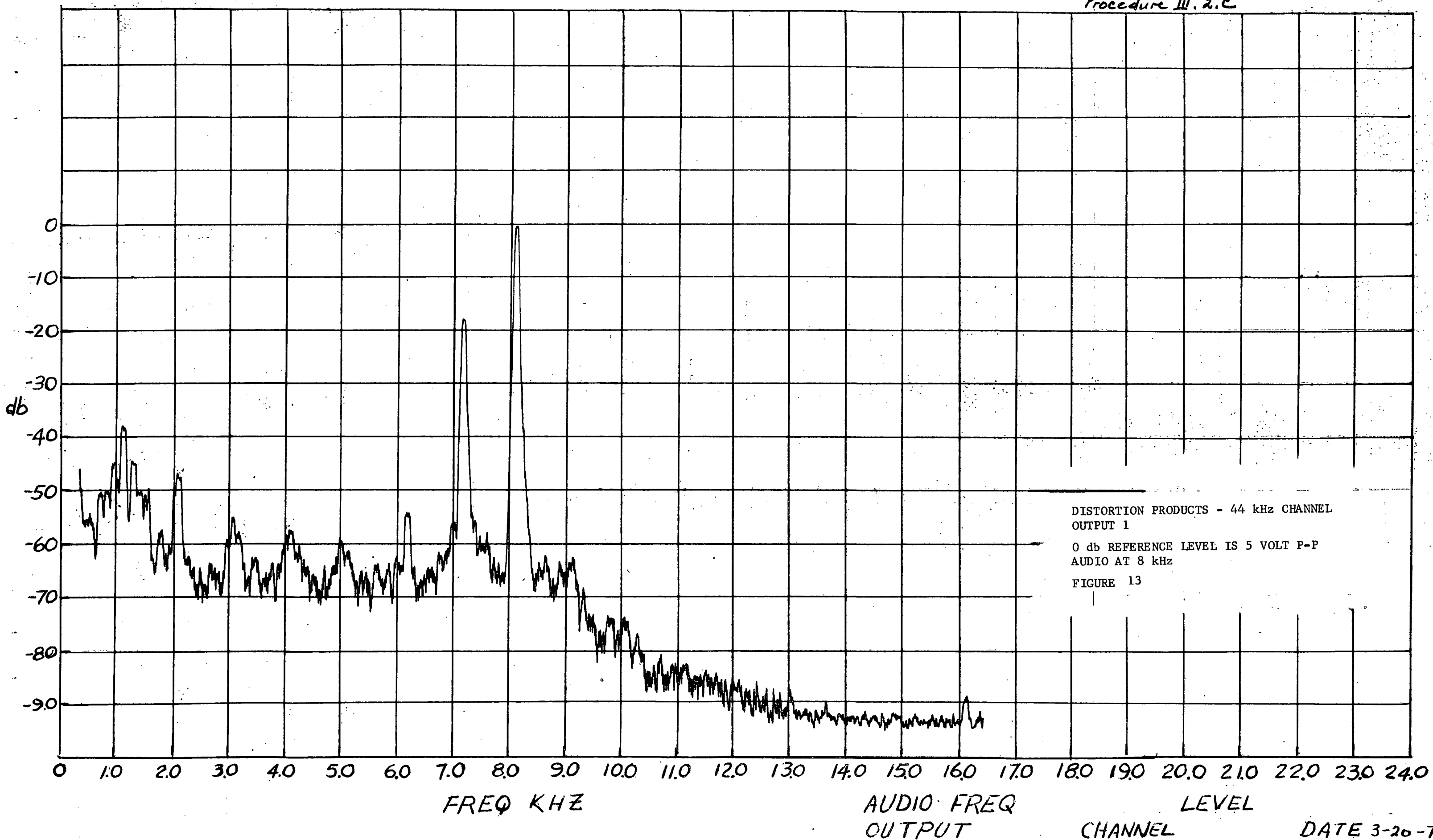
Procedure III.1.c



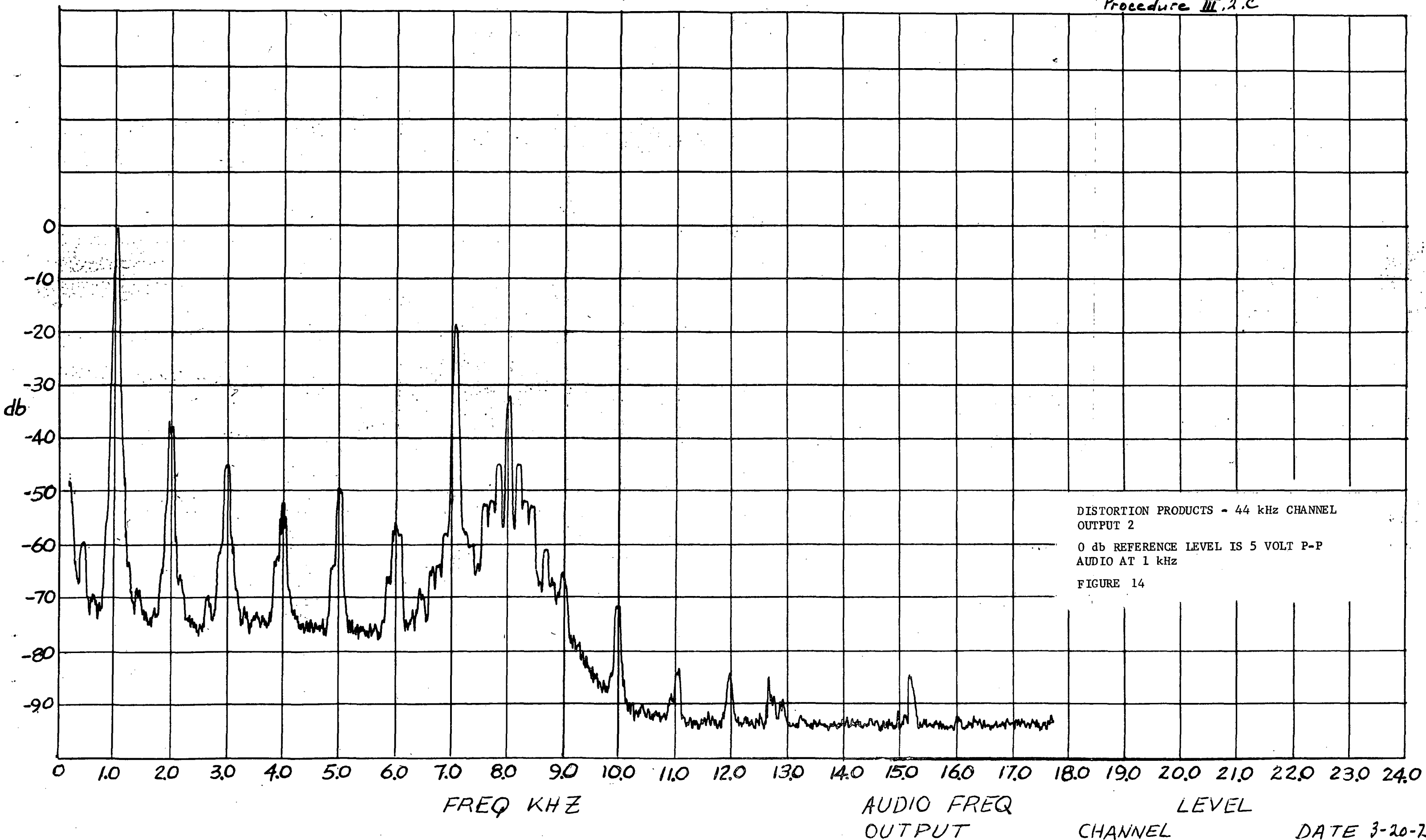
Procedure III.1.D



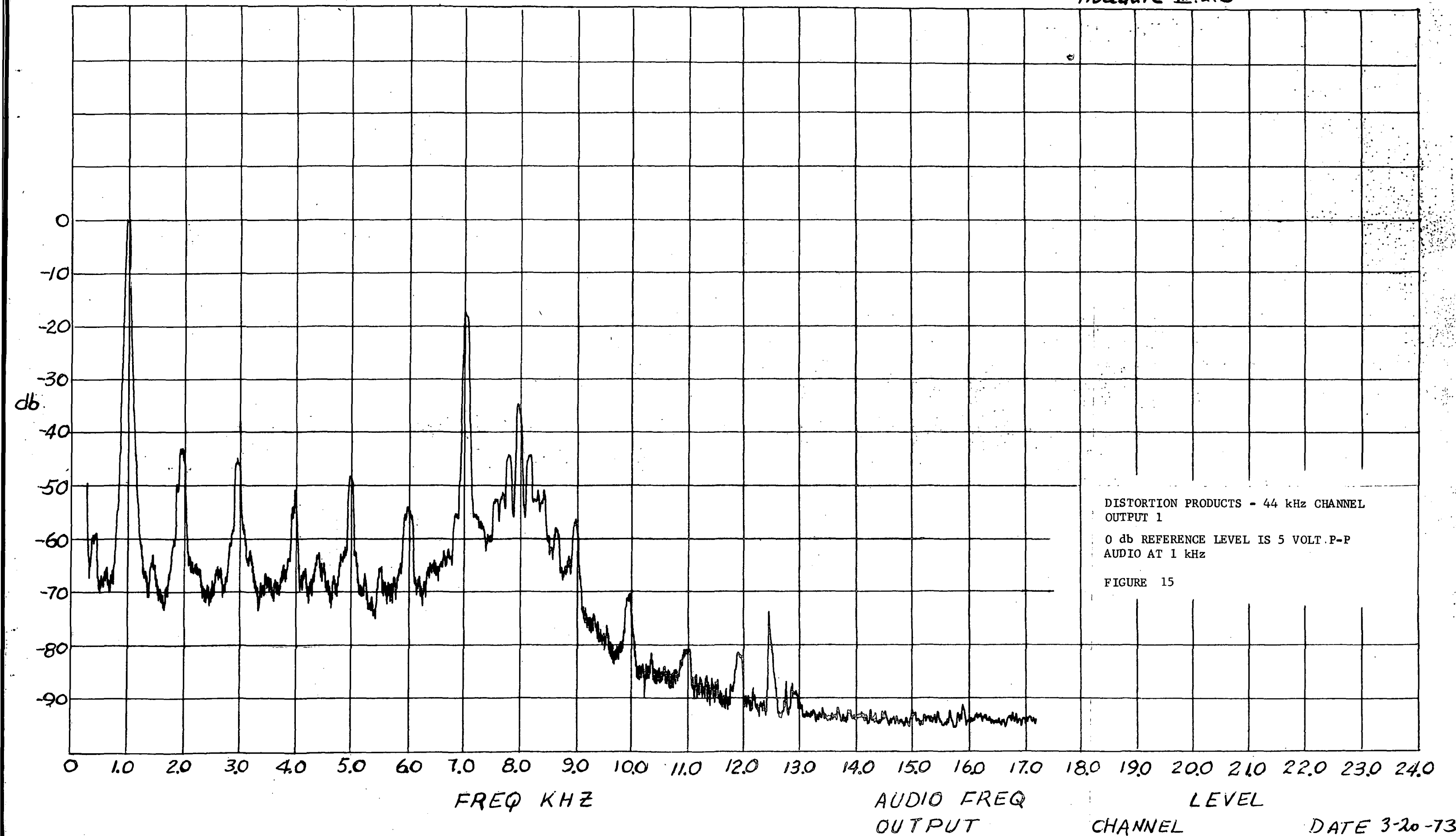
Procedure III. 2.C



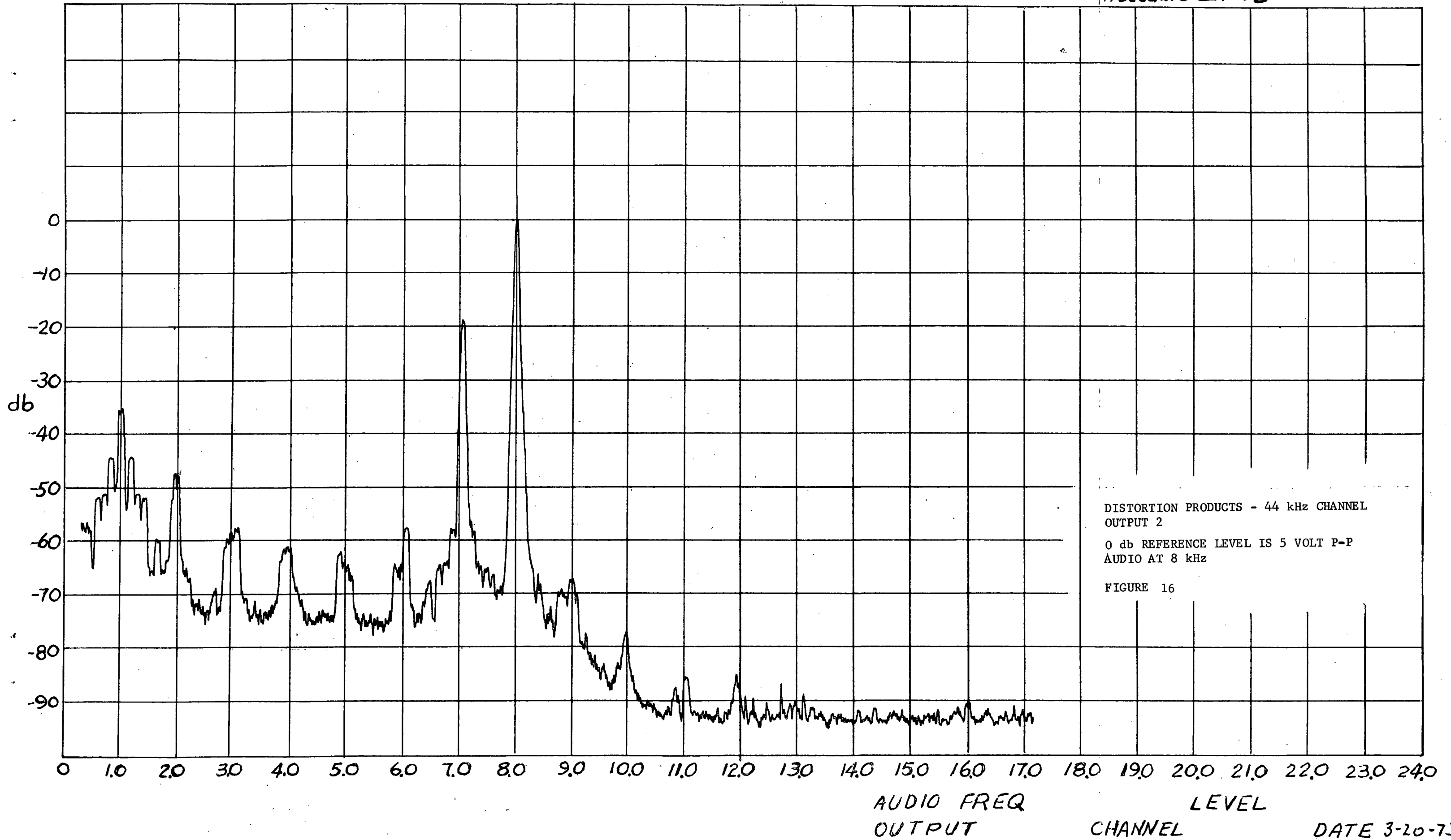
Procedure III.2.C



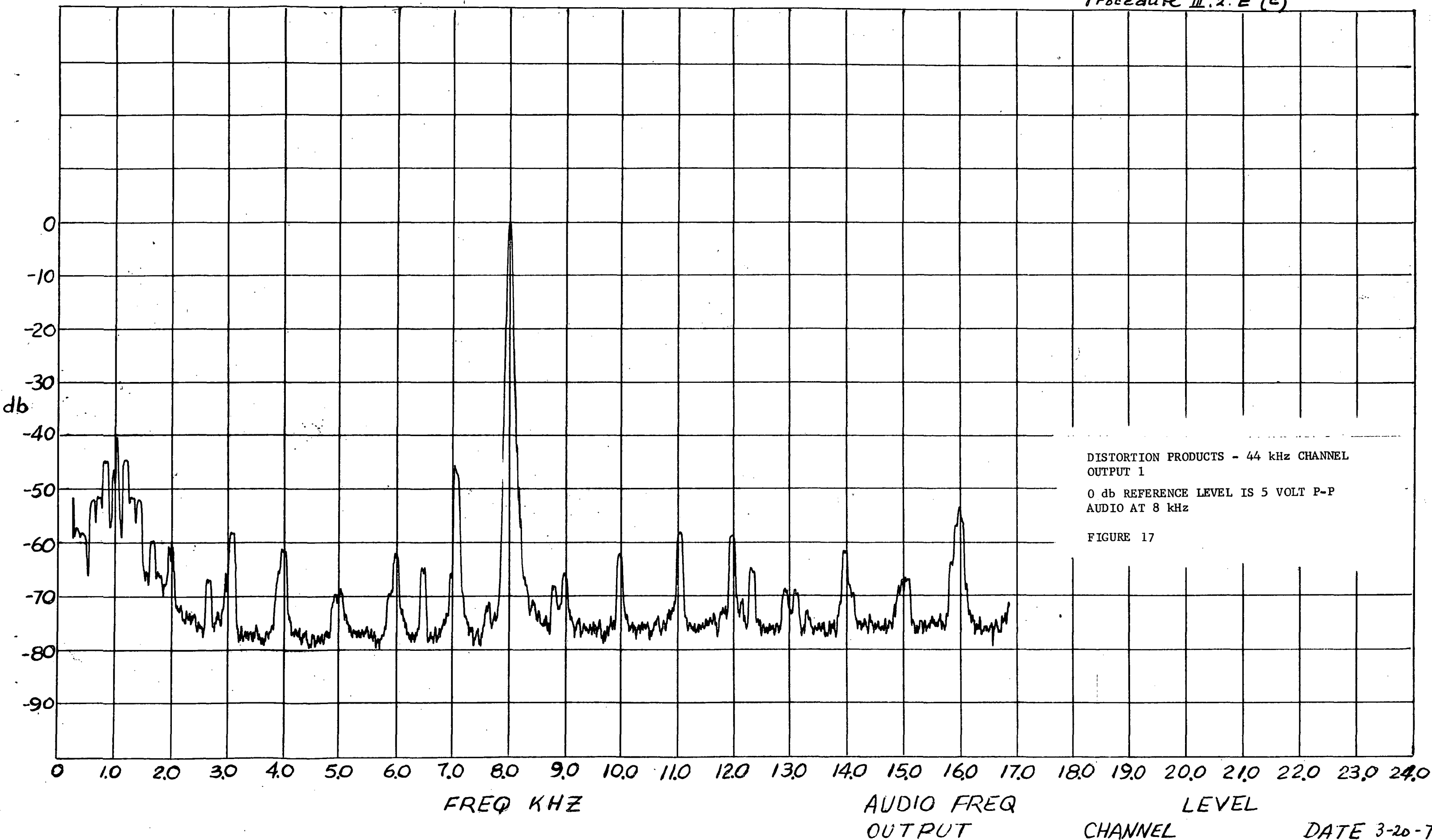
Procedure III.2.D



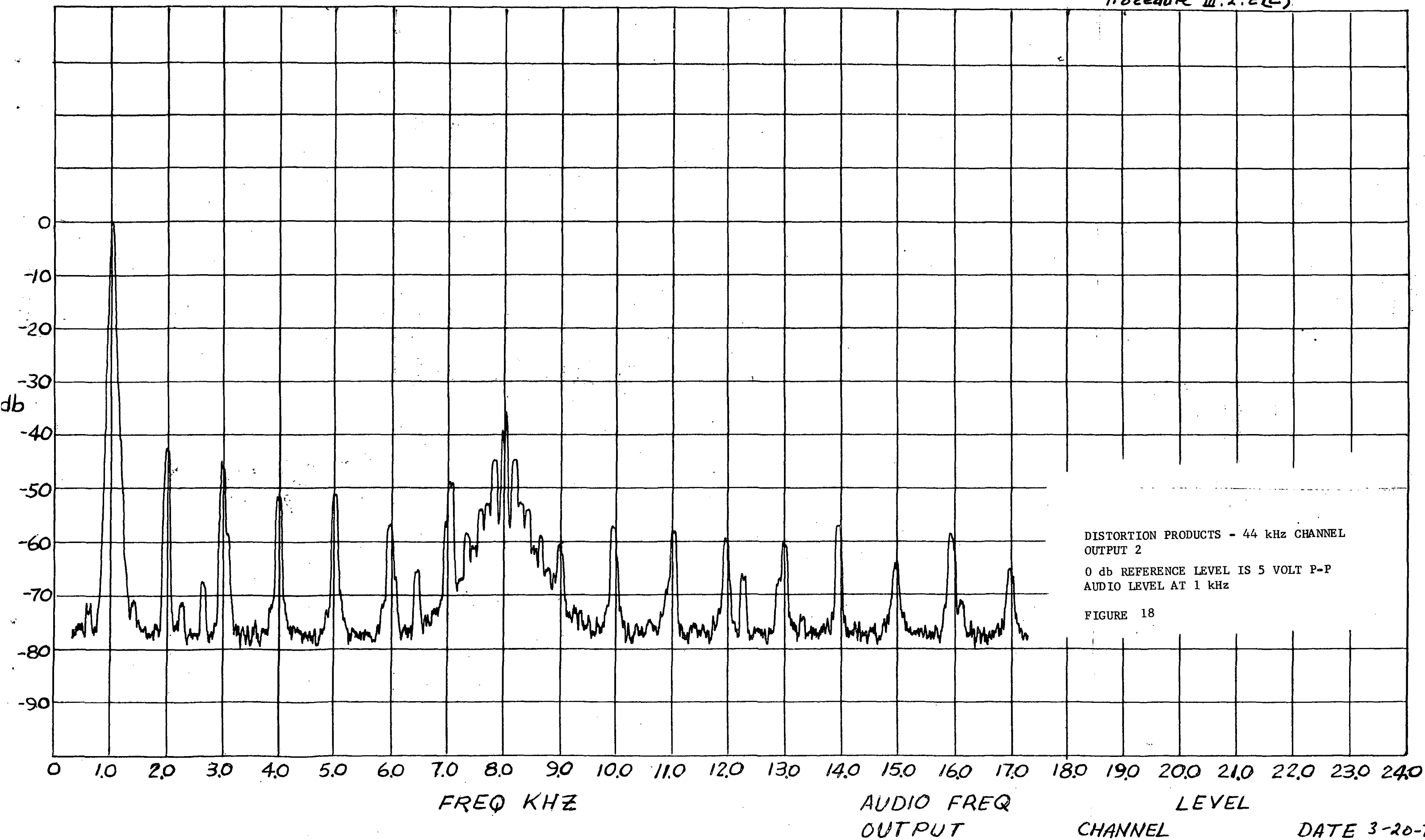
Procedure III.2.D



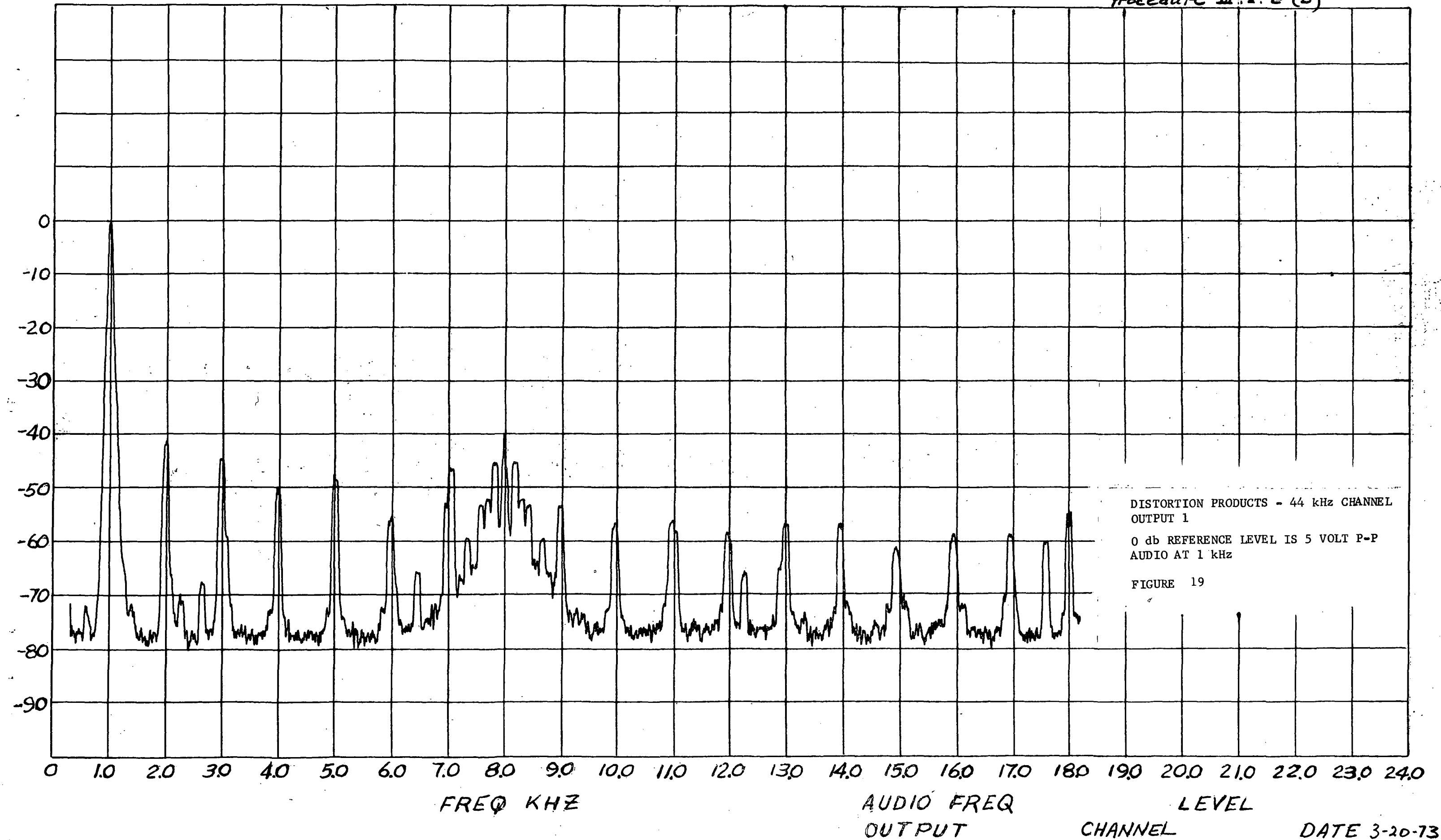
Procedure II.2.E (c)



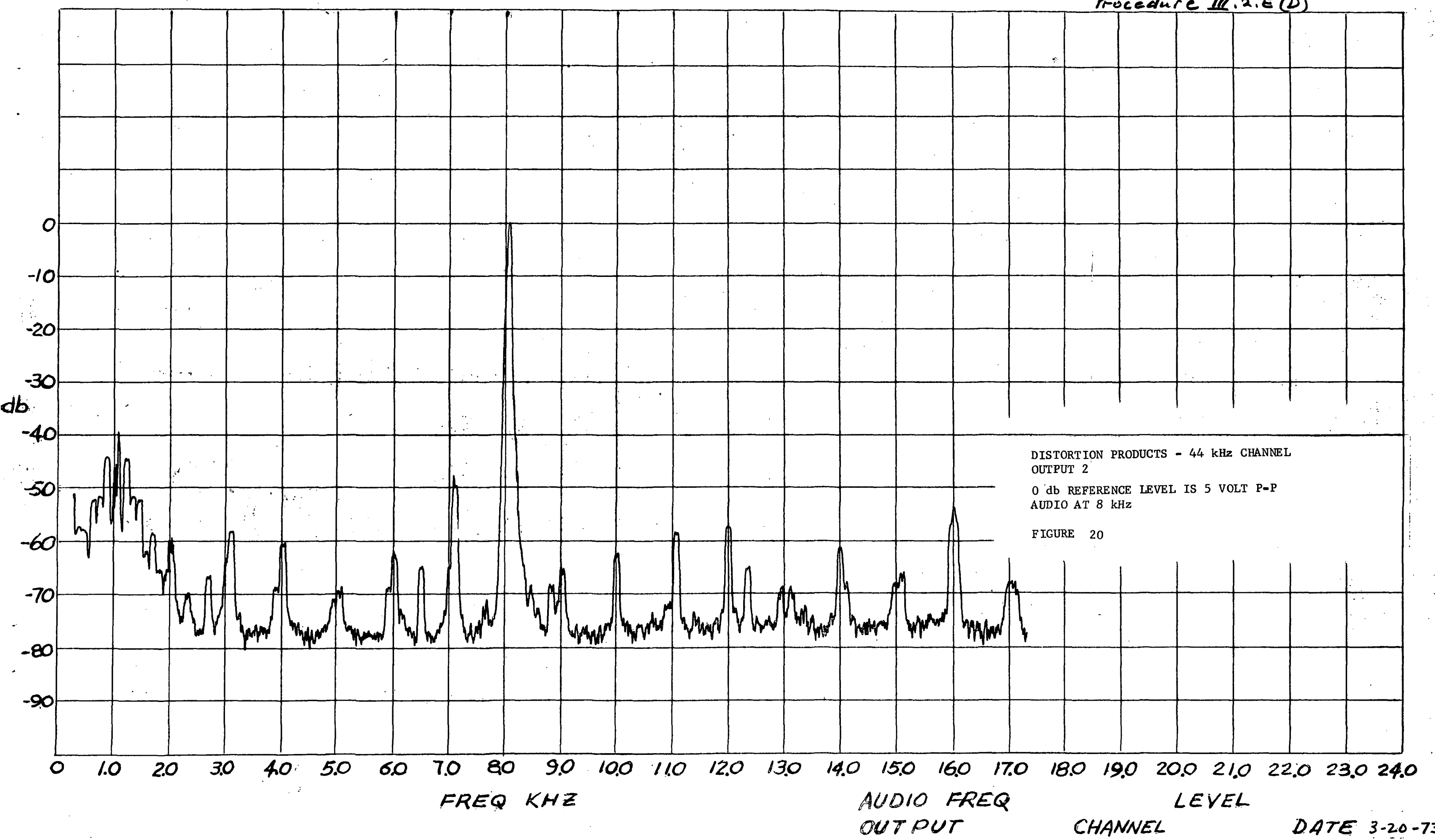
Procedure III.2.E(c)



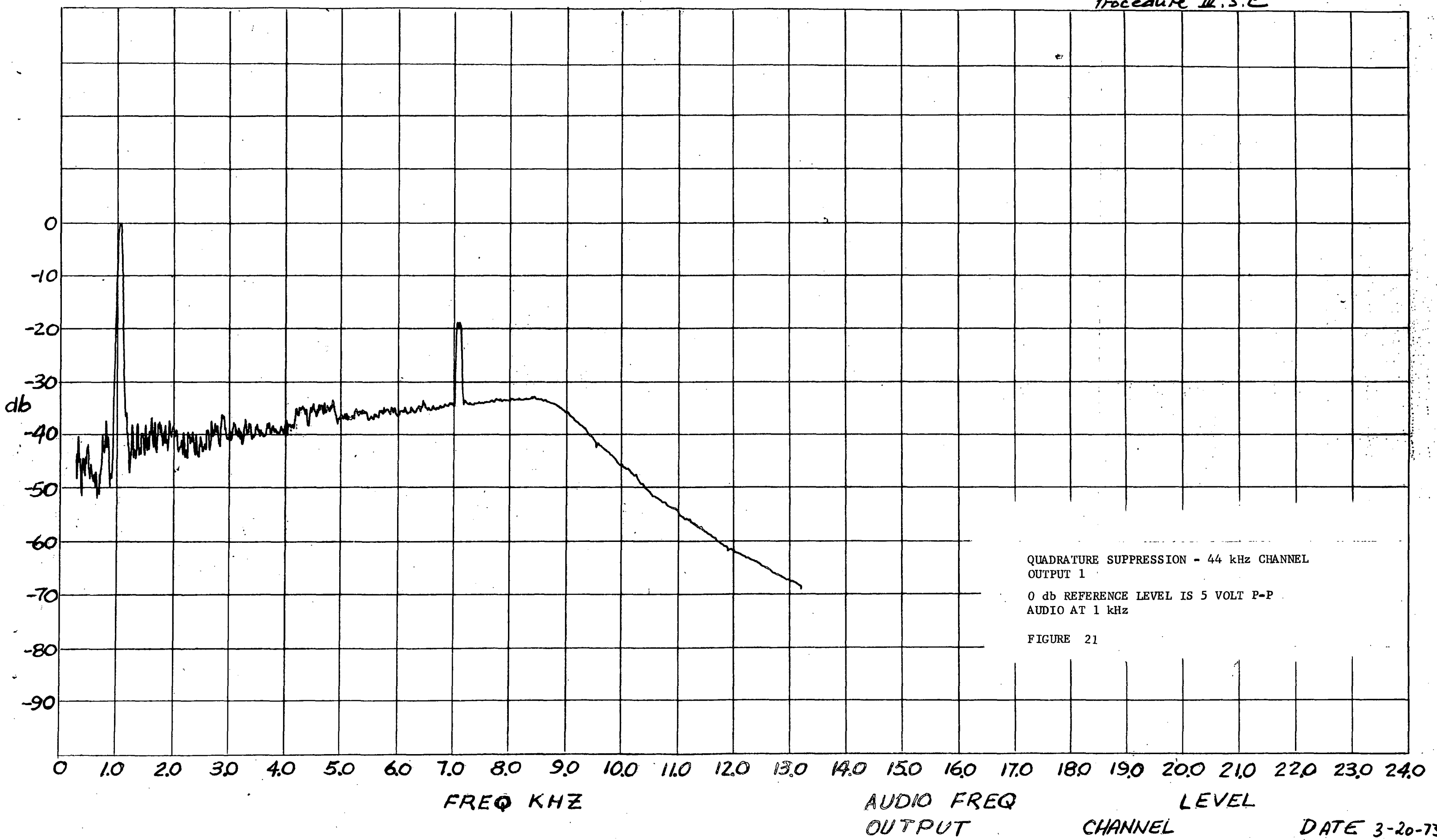
Procedure III. 2. E (D)



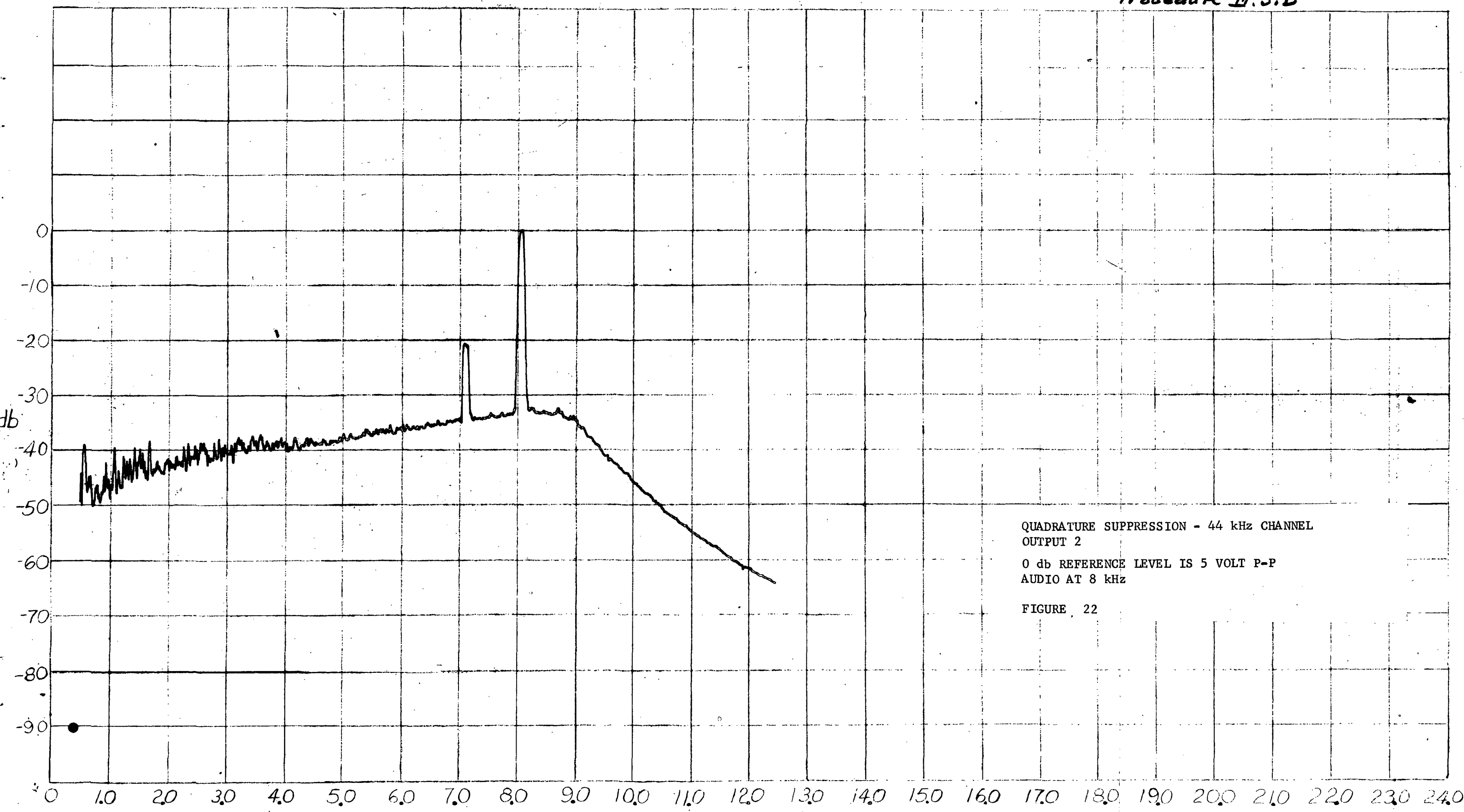
Procedure III.2.E (D)



Procedure II.3.C

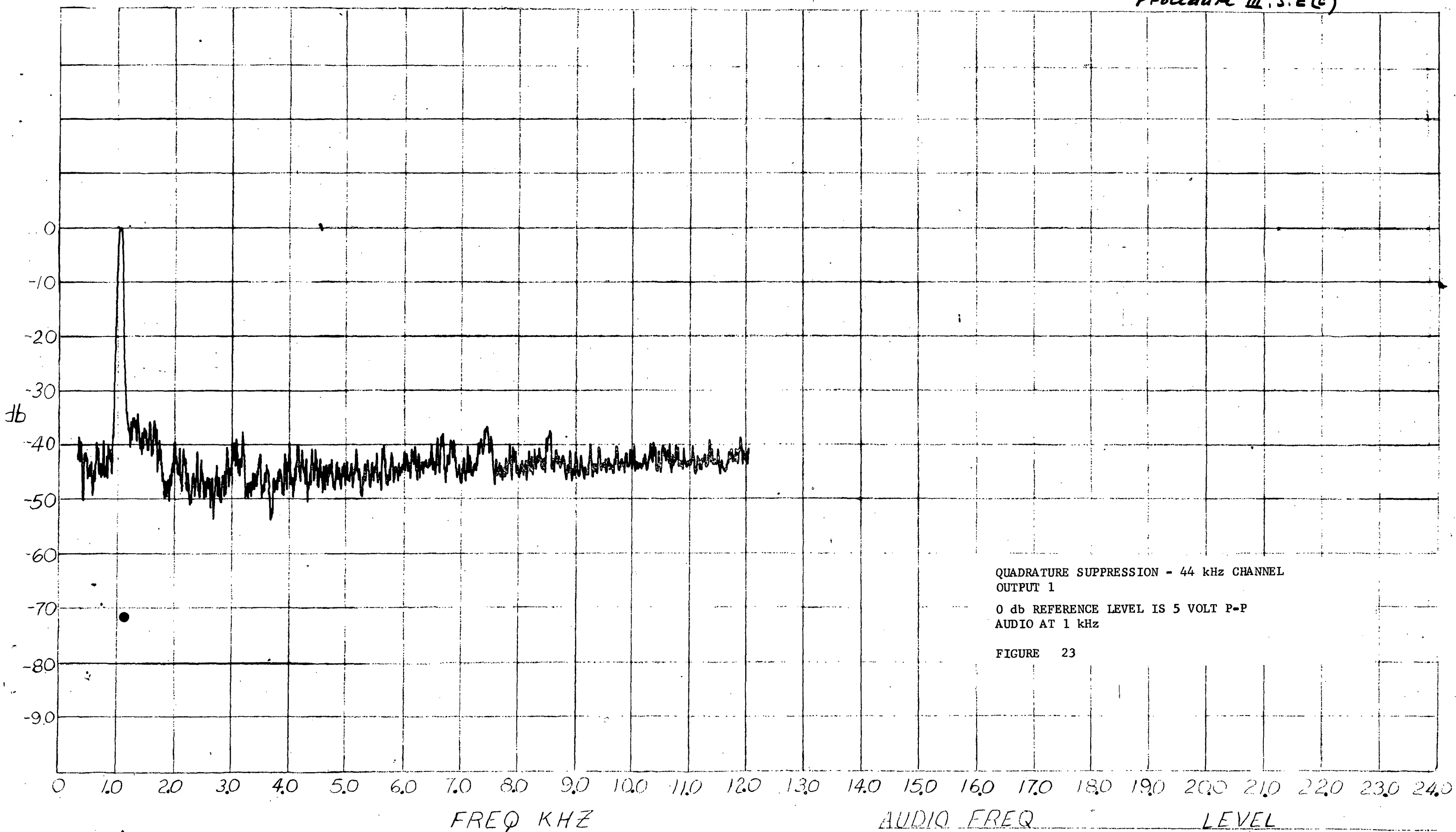


Procedure IV.3.D



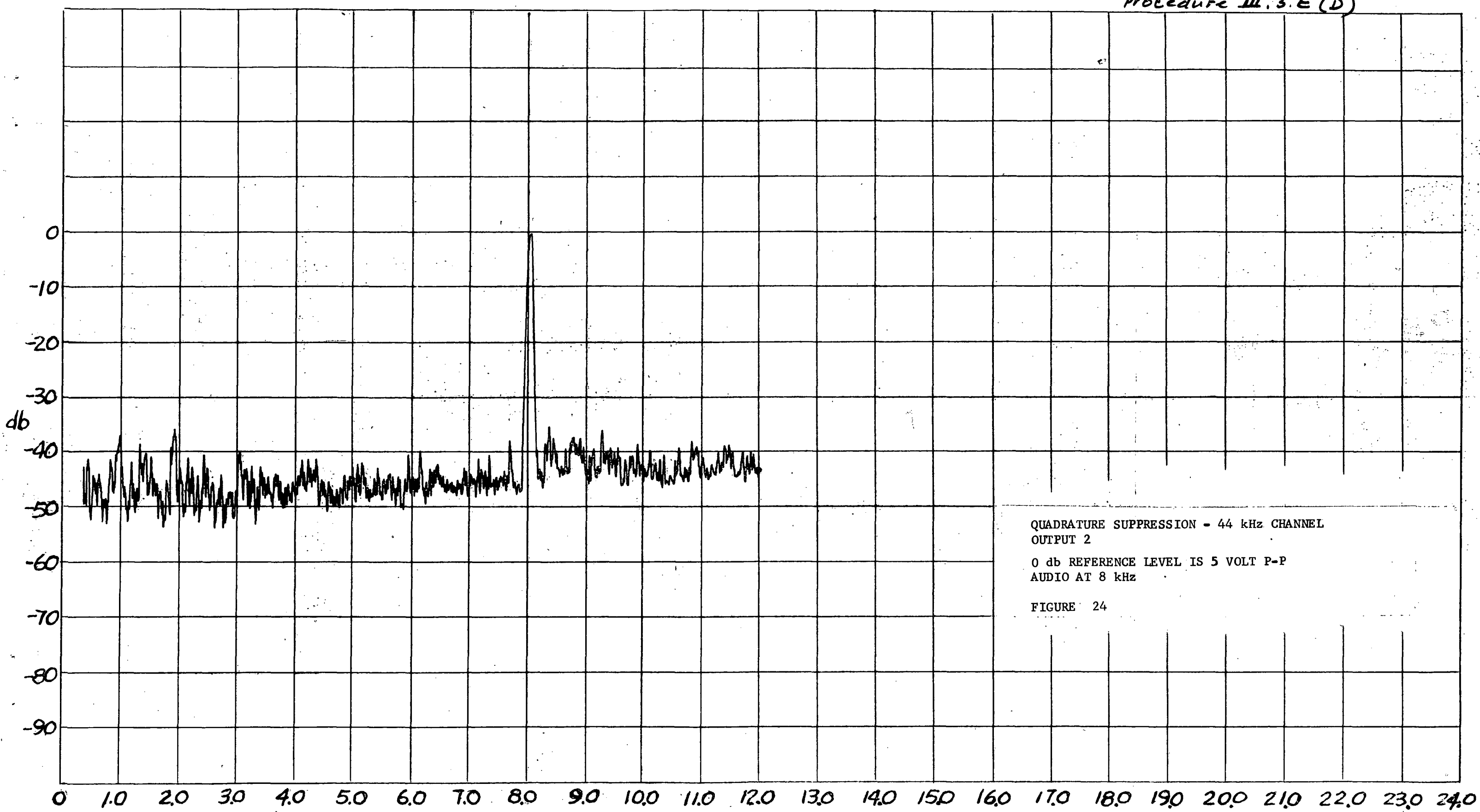
QUADRATURE SUPPRESSION - 44 kHz CHANNEL
OUTPUT 2
0 db REFERENCE LEVEL IS 5 VOLT P-P
AUDIO AT 8 kHz
FIGURE 22

Procedure III.3.E(c)



AUDIO FREQ	LEVEL
OUTPUT	CHANNEL
DATE 3-20-73	

Procedure III.3.E (D)



QUADRATURE SUPPRESSION - 44 kHz CHANNEL
OUTPUT 2

0 db REFERENCE LEVEL IS 5 VOLT P-P
AUDIO AT 8 kHz

FIGURE 24

FREQ KHZ

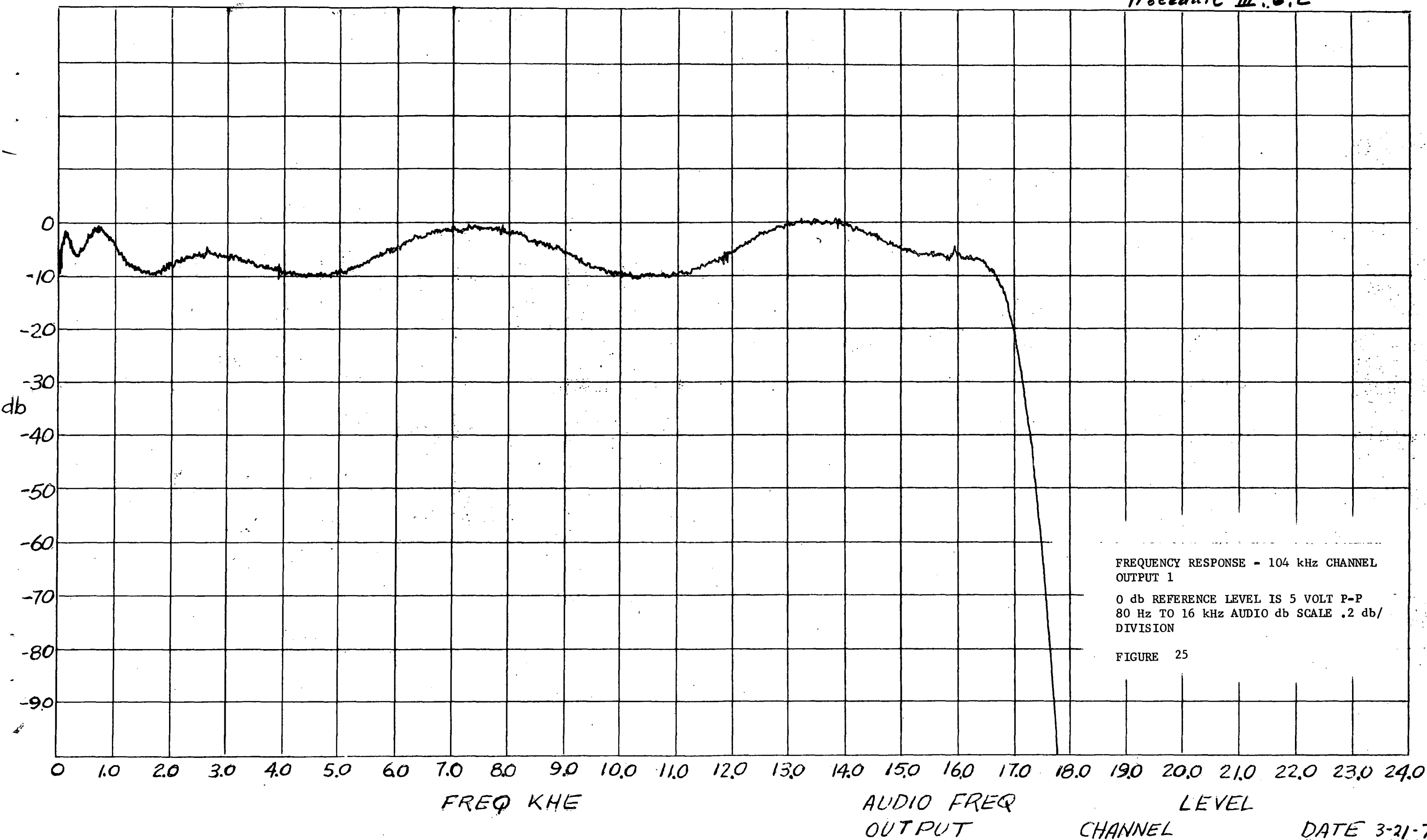
AUDIO FREQ
OUTPUT

LEVEL

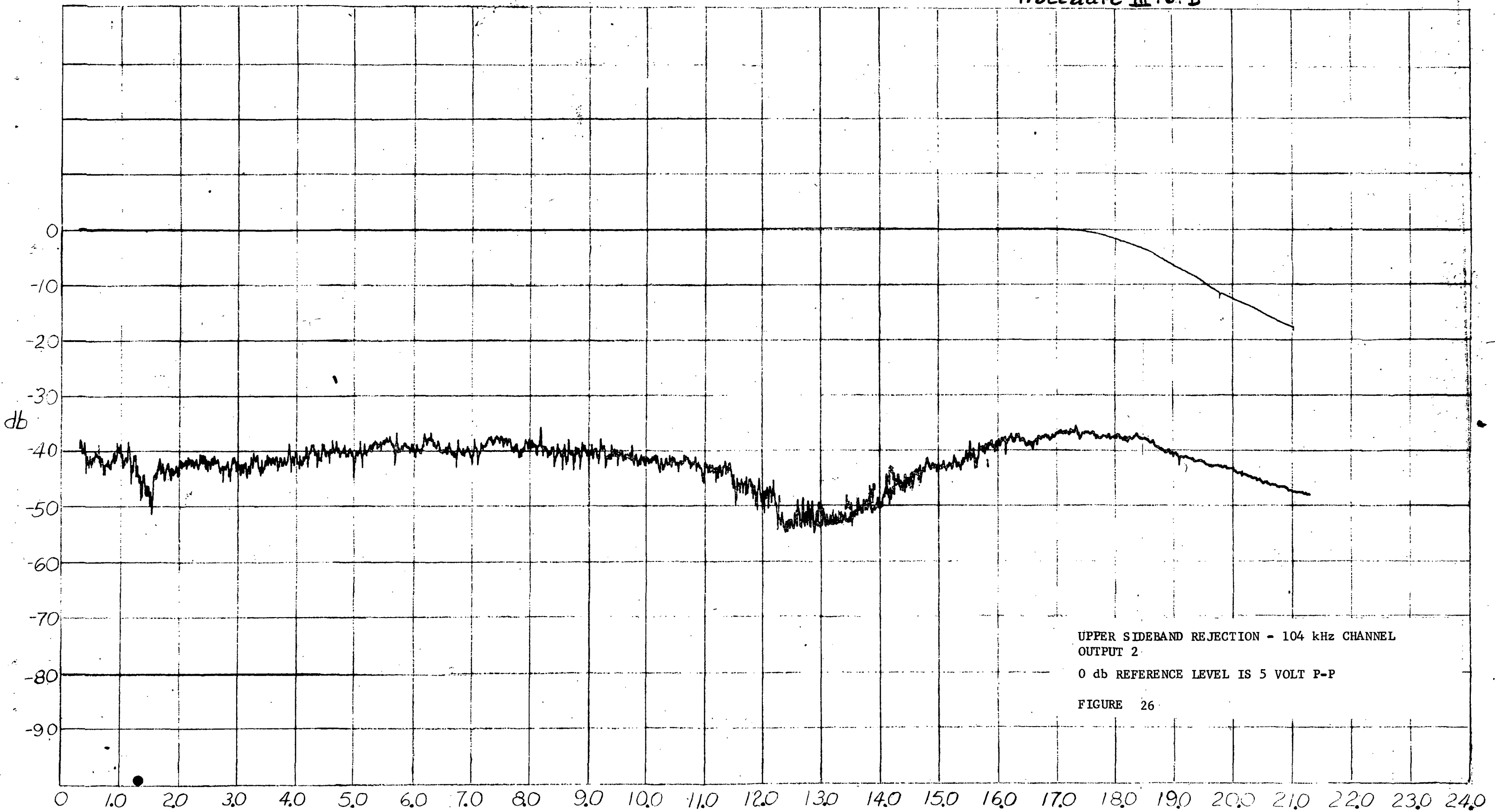
CHANNEL

DATE 3-20-73

Procedure III.6.c



Procedure III.b.D



UPPER SIDEBAND REJECTION - 104 kHz CHANNEL
OUTPUT 2

0 db REFERENCE LEVEL IS 5 VOLT P-P

FIGURE 26

FREQ KHZ

AUDIO FREQ

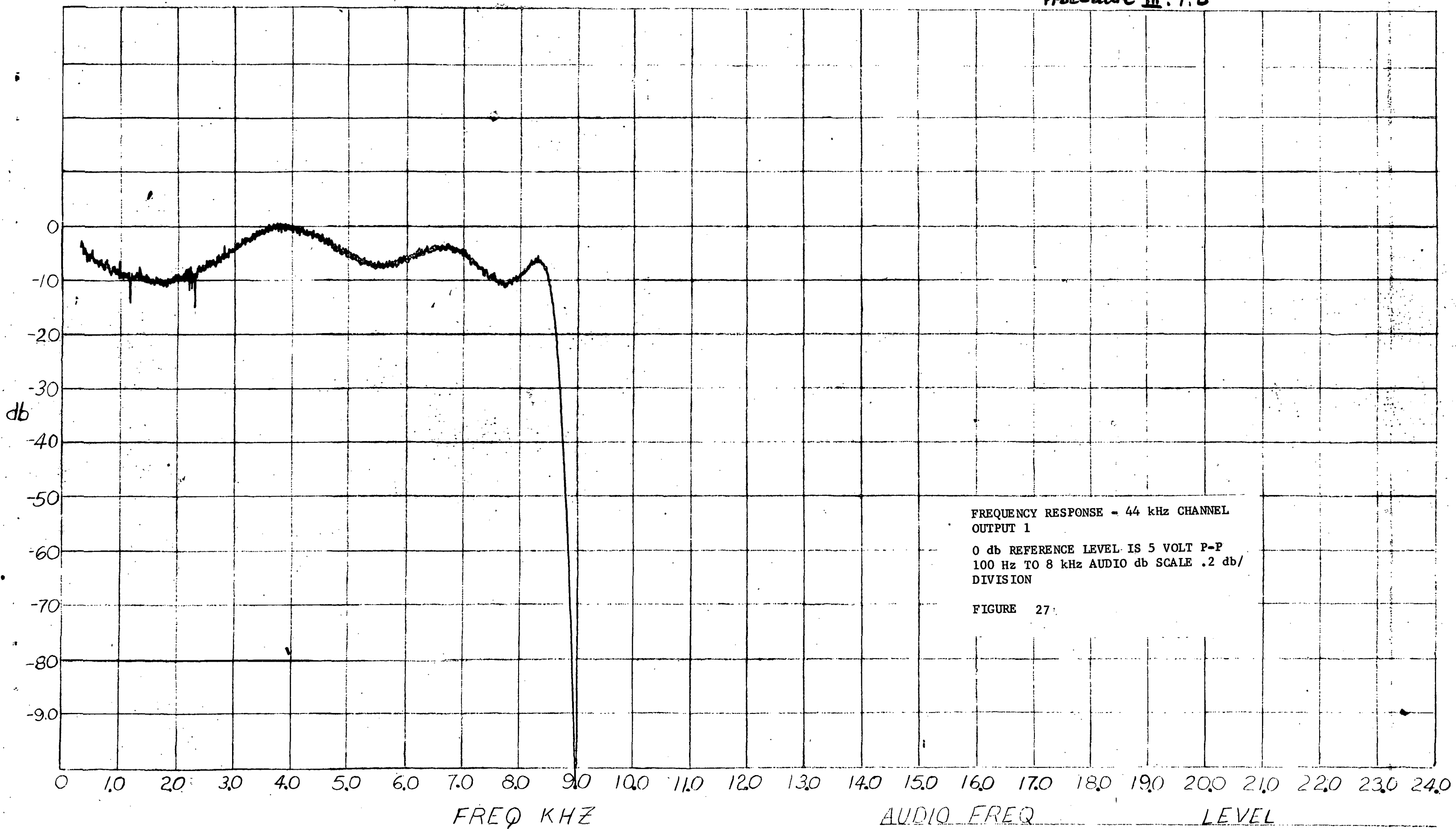
LEVEL

OUTPUT

CHANNEL

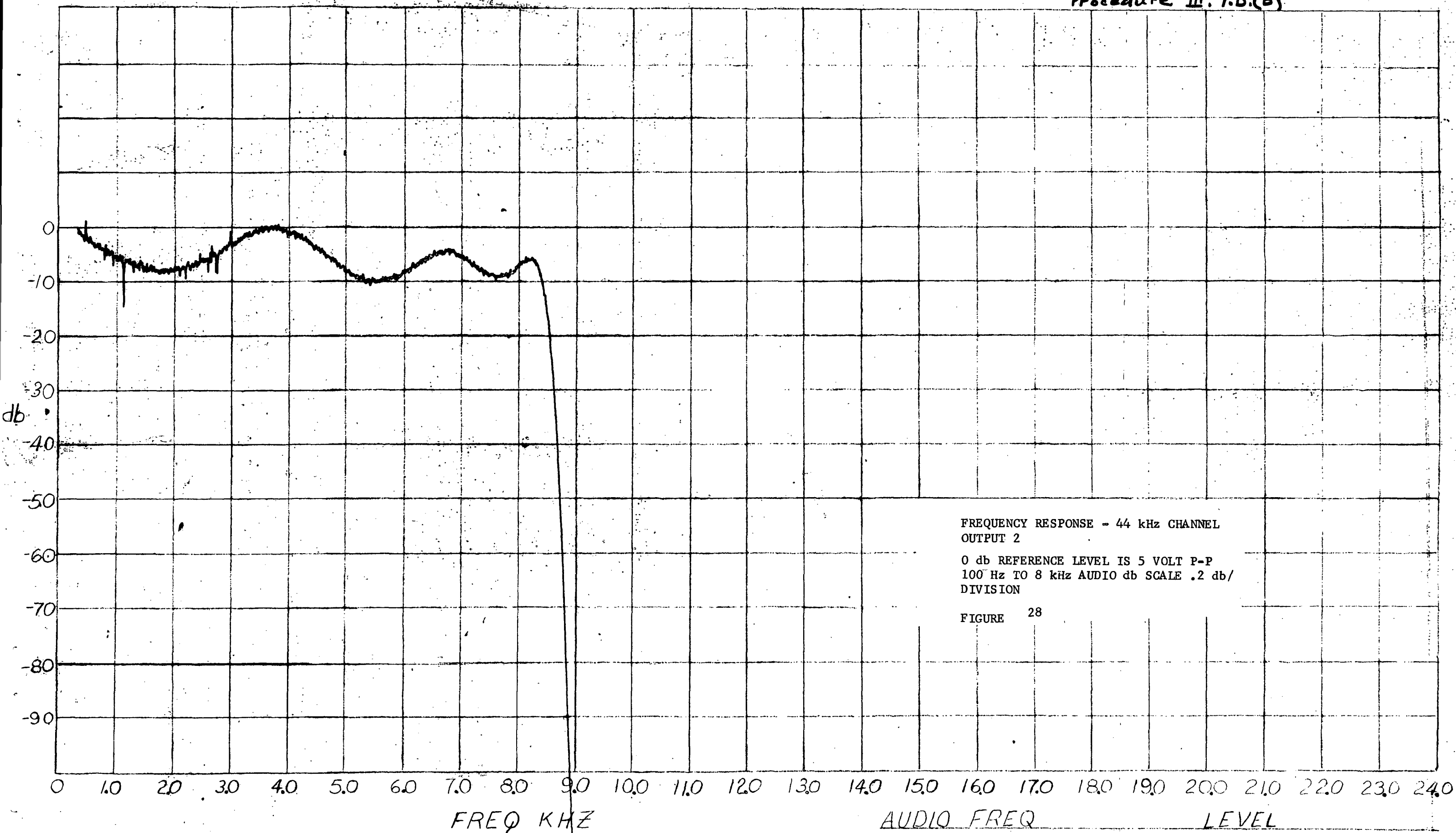
DATE 3-21-73

Procedure III.7.B



AUDIO FREQ	LEVEL
OUTPUT	CHANNEL
DATE 3-21-73	

Procedure III.7.D.(B)



FREQUENCY RESPONSE - 44 kHz CHANNEL
OUTPUT 2

0 db REFERENCE LEVEL IS 5 VOLT P-P
100 Hz TO 8 kHz AUDIO db SCALE .2 db/
DIVISION

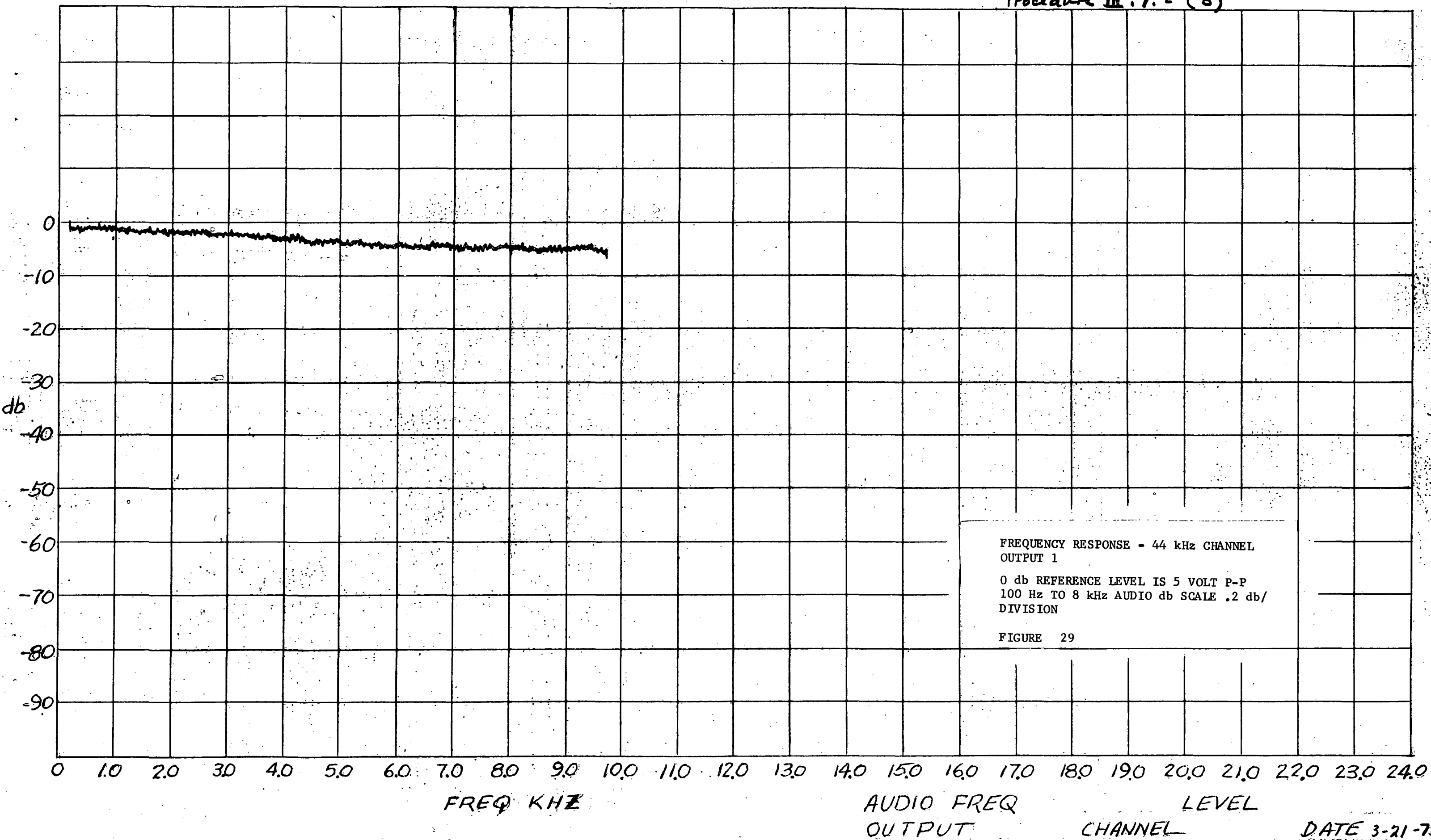
FIGURE 28

AUDIO FREQ
OUTPUT

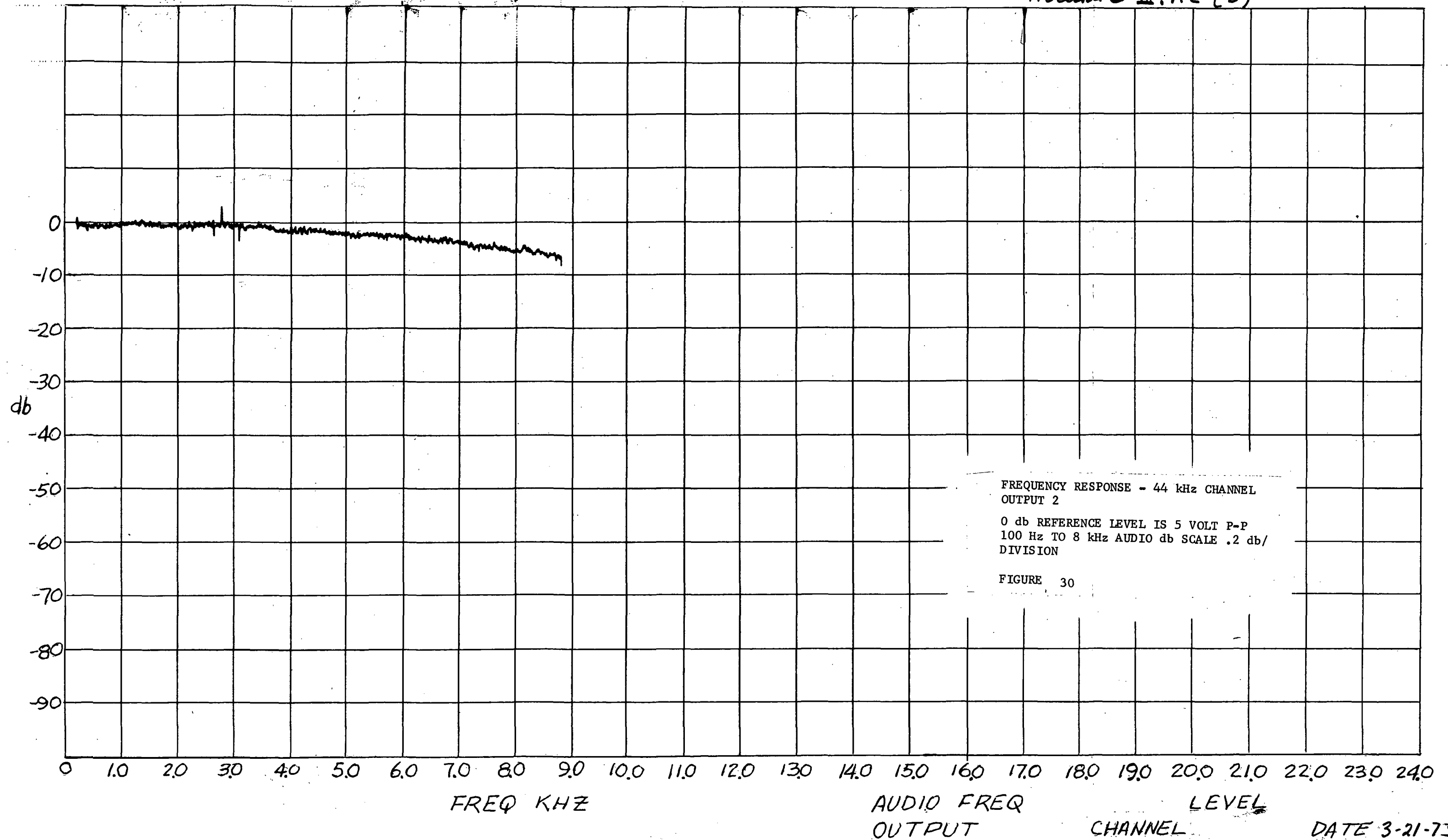
LEVEL
CHANNEL

DATE 3-21-73

Procedure III.7.E (B)



Procedure III.7.E (D)



PROCEDURE III.4
AMPLITUDE LINEARITY - 104 kHz CHANNEL

INPUT mV RMS	OUTPUT V RMS	db GAIN
50	0.303	15.6494
100	0.606	15.6494
150	0.908	15.6394
200	1.212	15.6494
250	1.518	15.6666
300	1.820	15.6594

The linearity of the channel is better then 0.03 dB.

FIGURE 31

PROCEDURE III.5
AMPLITUDE LINEARITY - 44 kHz CHANNEL

INPUT V RMS	OUTPUT #1 V RMS	db GAIN
.353	.355	+ .0520
.707	.709	+ .0260
1.060	1.068	+ .0606
1.060	1.068	+ .0606
1.414	1.416	+ .0086
1.767	1.768	+ .0042
INPUT V RMS	OUTPUT #2 V RMS	db GAIN
.353	.353	.0000
.707	.704	- .0037
1.060	1.060	.0000
1.414	1.413	- .0002
1.767	1.762	- .0246

The linearity of both the cophase and the quadrature channel is better than 0.06 dB.

FIGURE 32

PROCEDURE III.7.C
FREQUENCY RESPONSE - 44 kHz CHANNEL

INPUT	OUTPUT #1	
AC 5V PP (1.769 RMS)	1.767 RMS =	2.500 Vpeak
DC + 2.50	+4.660	
DC - 2.50	-3.870	
	2) 8.530 =	4.265 Vpeak
	$20 \log \frac{4.265}{2.500} =$	4.6396 db
AC 5V PP (1.769 RMS)	OUTPUT #2	
AC 5V PP (1.769 RMS)	1.769 RMS =	2.500 Vpeak
DC + 2.50	-4.502	
DC - 2.50	+3.778	
	2) 8.280 =	4.140 Vpeak
	$20 \log \frac{4.140}{2.500} =$	4.381 db

FIGURE 33

PROCEDURE III.7.E(C)
FREQUENCY RESPONSE - 44 kHz CHANNEL

INPUT	OUTPUT #1		
AC 5V PP (1.769 RMS)	6.500 RMS	=	9.191 Vpeak
DC + 2.50	+8.797		
DC - 2.50	-9.487		
	2) 18.284	=	9.142 Vpeak
	$20 \log \frac{9.191}{9.142}$	=	0.0434 db

INPUT	OUTPUT #2		
AC 5V PP (1.769 RMS)	5.620 RMS	=	7.947 Vpeak
DC + 2.50	-8.110		
DC - 2.50	+7.870		
	2) 15.980	=	7.990 Vpeak
	$20 \log \frac{7.990}{7.947}$	=	.0434 db

The DC response corresponds to the AC response reference reading to within 0.05 dB for both the cophase and the quadrature channels.

FIGURE 34

PROCEDURE III.8
OUTPUT IMPEDANCE

		NO LOAD	1K LOAD
104 kHz	#1	1.820	1.819
104 kHz	#2	1.820	1.819
44 kHz	#1	1.768	1.767
44 kHz	#2	1.762	1.761

OUTPUT IMPEDANCE BASED ON FORMULA

$$R_S = \frac{R_L (E_O - E_{RL})}{E_{RL}}$$

where E_O = no load voltage

E_{RL} = load voltage with 1 k ohm load resistor

R_L = 1 k ohm

Output impedance of 104 kHz channel is 0.55 ohm.

Output impedance of 44 kHz channel is 0.56 ohm.

FIGURE 35