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HIGH VOLTAGE AND CURRENT, GATE-ASSISTED, TURN-OFF THYRISTOR DEVELOPMENT

by

T. P. Nowalk, J. B. Brewster and Y. C. Kao

WESTINGHOUSE ELECTRIC CORPORATION
Semiconductor Division
Youngwood, Pennsylvania 15697

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Julian F. Been

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16. Abstract

An improved high speed power switch with unique turn-off capability was developed. This gate assisted turn-off thyristor (GATT) was rated 1000V and 100A with turn-off times of 2μs. Fifty units were delivered for evaluation. In addition, test circuits designed to relate to the series inverter application were built and demonstrated. In the course of this work it was determined that the basic device design is adequate to meet the static characteristics and dynamic turn-off specification. It was further determined that the turn-on specification is critically dependent on the gate drive circuit due to the distributive nature of the cathode-gate geometry. Future work should emphasize design modifications which reduce the gate current required for fast turn-on, thereby opening the way to higher power (current) devices.

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I. INTRODUCTION

1.1 Power Processing and the Series Inverter

A broad area of the field of power processing technology deals with the conversion of dc power from one voltage level to another. In some systems, the prime power is supplied by relatively low voltage energy converters which provide outputs too low and too variable to be used directly. In others, the dc source is derived from the rectified output of an ac line which must be adjusted to the desired voltage level and then regulated at that point.

A considerable amount of technology has been generated in this area, making possible a solution to almost any reasonable system problem. However, when examined critically from the standpoint of equipment cost, size, weight, reliability and efficiency, each circuit solution represents a certain compromise of desired properties. It is always desirable, therefore, to advance the art with new technology which offers an improved compromise of the system evaluation criteria described.

Circuits for the conversion of dc power from one level to another must of necessity interrupt dc currents. This can be done by inserting an active switching device in the dc line or, alternately, by utilizing a series energy storage device. No solid-state dc switch is commercially available at present for use at high power levels; thus the technique normally used for the former is force commutation of a thyristor. However, this approach results in high energy transients which are detrimental to efficiency and reliability, and contribute significantly to undesirable electromagnetic interference. Circuits of this type also suffer disadvantages in size and weight and are limited in internal operating frequency by the recovery times of the thyristors.

A more desirable circuit solution employs relatively lossless energy storage devices, such as inductors and capacitors, to effectively interrupt dc currents by natural commutation. In these circuits, standard thyristors may be employed without the need for commutating circuitry. Because commutation takes place naturally, no large voltage or current transients need occur, thereby increasing reliability and efficiency. Circuits of this type work well and exhibit all of the previously discussed advantages. However, they are limited in size and weight by the maximum realizable internal carrier frequency, which is in turn limited by the recovery times of the thyristors used.

A considerable improvement in dc power conversion circuit performance results from the use of a solid-state switching device which permits rapid recovery of forward blocking voltage capability after current interruption by external means. The gate assisted turn-off thyristor (GATT) is such a device. It was initially developed under Contract NAS12-2198; the performance capability and manufacturability has been extended significantly under Contract NAS3-14394. The GATT device is useful in applications where high frequency thyristor operation is needed. However, a circuit application of particular interest is the series inverter.

The specific series inverter circuit under consideration is that developed by Dr. F. C. Schwarz. The principal function of the circuit is to convert dc power at one voltage level to another, where the voltage is then regulated against changes in input voltage and output loading. The circuit performs this function with minimum size and weight owing to the use of a high internal carrier frequency. It also performs this function with maximum efficiency and reliability, owing to the reduction of component dissipation and stress resulting from the use of natural commutation.

A schematic diagram of the circuit employing conventional thyristors is shown in Figure 1. Theoretical voltage and current waveforms which occur during circuit operation are shown in Figure 2. Just prior to time t = 0 of the time reference for the waveforms shown, the transformer primary current i_1 is zero and both thyristors are nonconducting. Capacitor C_1 is charged to a voltage slightly in excess of supply voltage e_s, and capacitor C_2 is charged slightly negatively.

At time t = 0, thyristor Th_1 is triggered on causing it to conduct. The flow of current i_1 through thyristor Th_1, transformer T_1, and inductor L_1, causes capacitor C_1 to discharge and capacitor C_2 to become charged. When current i_1 naturally commutates to zero, thyristor Th_1 ceases conduction and becomes slightly reverse biased. At time $t = t_1$ after a time interval T_k, capacitor C_1 is charged slightly negative and capacitor C_2 is charged to a voltage slightly in excess of the supply voltage e_s.

At time $t = t_2$, after an additional interval of time T_D, thyristor Th_2 is triggered on causing it to conduct. The primary current i_1 of transformer T_1 now flows in the opposite direction charging capacitor C_1 and discharging capacitor C_2. When current i_1 naturally commutates to zero, thyristor Th_2 ceases to conduct restoring all circuit components to their conditions which prevailed at time t = 0.

In order to obtain a circuit with minimum size and weight, the period of the carrier frequency at which the circuit operates should be minimized. It can be seen in Figure 2 that the period of the carrier frequency is equal to $2(T_K + T_D)$. The minimum value of T_D approaches the thyristor turn-off time which limits the minimum period and thus the maximum operating frequency. Therefore, in order to increase the operating carrier frequency to reduce system size and weight, thyristors with shorter turn-off times are needed.

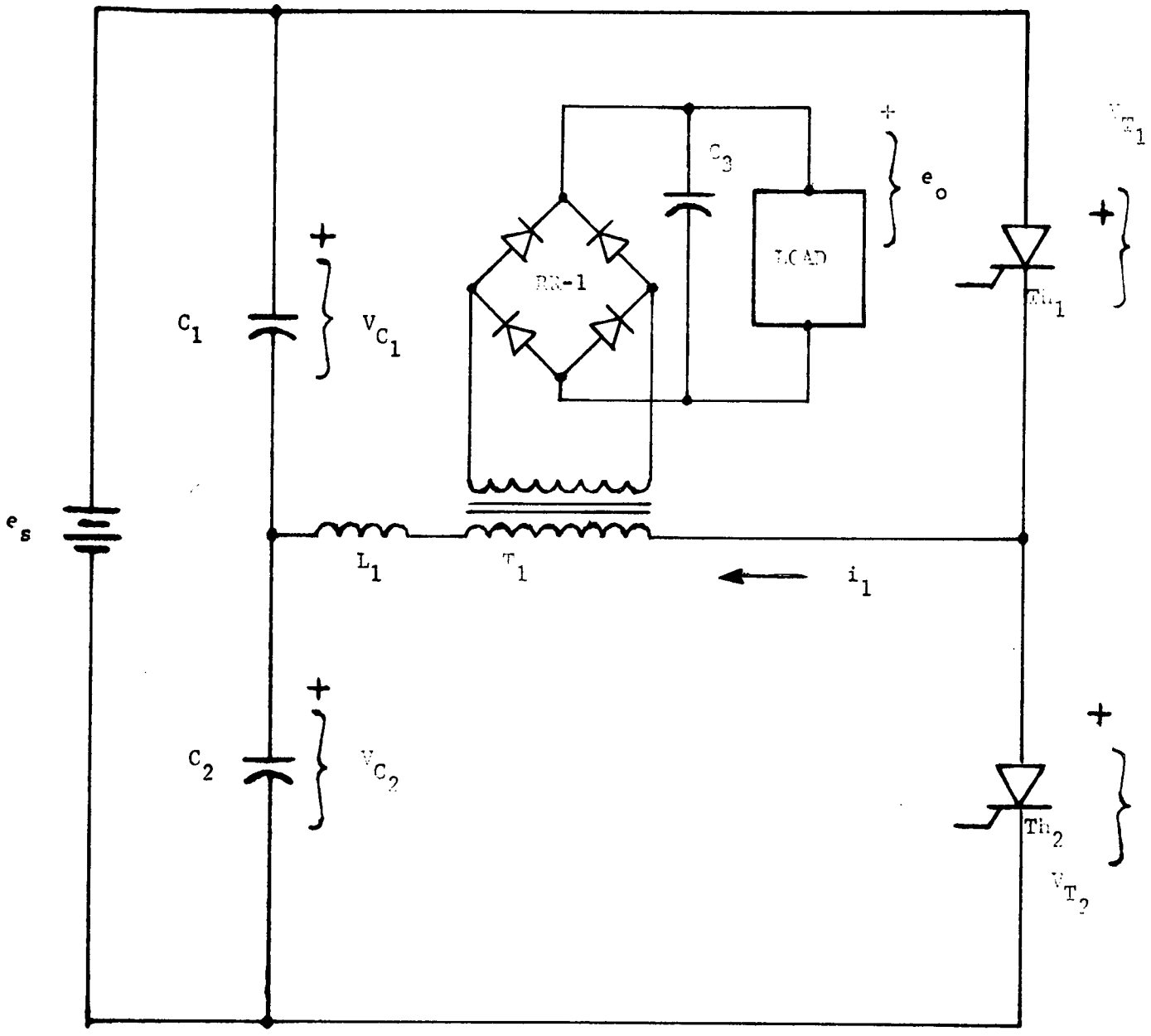


Figure 1 - Load Insensitive Series Inverter

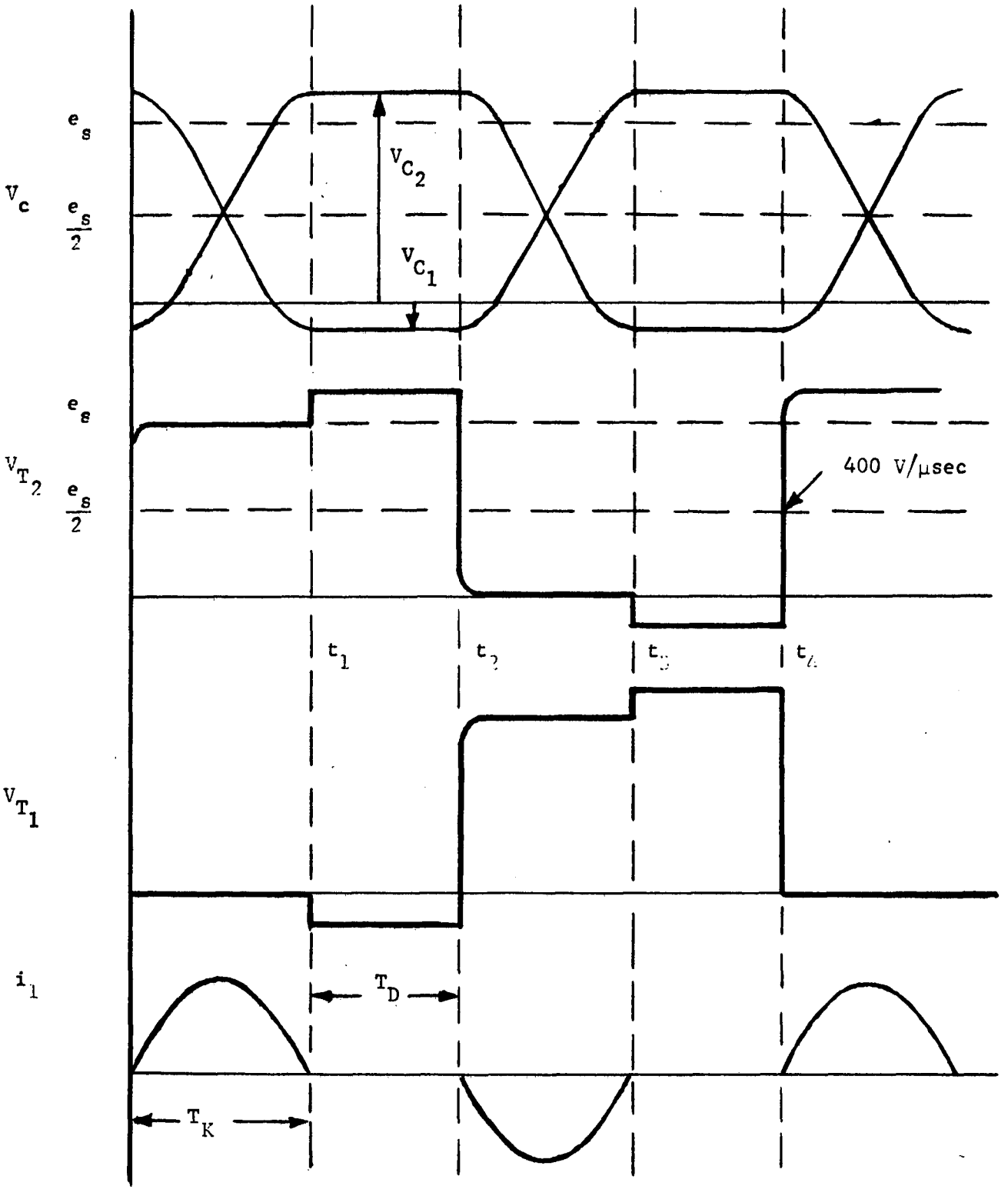


Figure 2 - Load Insensitive Series Inverter Waveforms

According to the analysis made by Dr. Schwarz, the efficiency of the circuit at high power can be expressed approximately as follows:

$$n = 1 - \rho^2 \frac{R_S}{R_L' + R_S} \qquad (1)$$

where n = circuit efficiency

ρ = form factor

R_S = equivalent series resistance

R_L' = equivalent load resistance reflected into the primary of the transformer

The form factor is related to the timing intervals and component values as follows:

$$\rho = \frac{\pi}{2\sqrt{2}} \left(1 + \frac{T_D}{\pi \sqrt{L_1 C_p}}\right) \qquad (2)$$

where L_1 = series inductance (see Figure 1)

$C_p = C_1 + C_2$ (see Figure 1)

T_D = delay time (see Figure 2)

From equation (1), it can be seen that for a given power level of operation, which fixes the values of R_S and R_L', circuit efficiency may be increased by minimizing the form factor ρ. From equation (2), form factor ρ can be minimized by minimizing delay time T_D because L_1 and C_p are fixed when the operating power level is established. As was noted previously, the minimum value of T_D approaches the turn-off time of the thyristors and, as a result, circuit efficiency can be increased for a given power level of operation by reducing turn-off time. It is assumed that no new effects are introduced in the process.

Utilizing the circuit shown in Figure 1, Dr. Schwarz reports the construction of a power conditioner using conventional thyristors with turn-off times of 10μs operating at a carrier frequency of 20 kHz. The circuit constructed controlled a 2 kW load and exhibited an efficiency of 95% with a specific weight of 2.5 kg/kw.

The GATT devices developed during the course of this program and the preceding one exhibit conventional thyristor characteristics, except that their turn-off times can be decreased by the proper application of gate drive. They may be substituted directly for the thyristors in the power circuit shown in Figure 1. However, the gate drive circuitry which is not shown requires modification.

The effect on circuit performance by the use of the GATT device will be to reduce T_D from its present value to several times smaller. On the basis of a device characterization comparison, the thyristors used by Dr. Schwarz had turn-off times of 10μs; the GATT devices developed under this contract and its predecessor have typical turn-off times of 2μs. It would be unrealistic to expect to realize an increase in operating frequency by a full factor of five because other effects do enter in. It is anticipated, however, that the internal carrier frequency can be increased from the 20kHz level used by Dr. Schwarz in his earlier work to perhaps 50 kHz with an accompanying increase in efficiency and decrease in circuit size and weight.

1.2 GATT I Program Results

As noted in Section 1.1, the subject program extends the work performed under the GATT I Contract, "Development of a High Speed Power Thyristor - The Gate Assisted Turn-Off Thyristor", NAS12-2198. The objective of the earlier effort was specified to be the development of a thyristor type of switch that would recover its forward blocking capability within two microseconds when used in a series inverter. The design objectives included blocking voltage capability of 600 volts, maximum forward current of 50 amperes and forward drop of two volts at 50 amperes. In addition, it was required to design and build test circuits for evaluation of the switching characteristics of these new devices. All of the prescribed objectives were met and a final sample delivery of twenty-two (22) GATT I devices completed the development effort.

The earlier contract revealed several process technique problems which would have to be resolved if the GATT device were to become a production reality. Paramount among these was the manner in which the cathode junction was formed and contacted. The GATT I device employed a mesa type cathode-emitter structure. Uniformity of cathode-gate junction characteristics was sufficiently lacking that each discrete cathode mesa had to be go-no go tested on the basis of junction leakage. A bus bar was then ultrasonically bonded to each acceptable finger thereby raising the contact plane above the original level. This automatically open circuited all unacceptable fingers. The structure in that particular form was simply not a manufacturable configuration; suitable modifications in design and/or process had to be made such that all fingers were acceptable.

Although the aforementioned fabrication/processing problems did impact the device design, the net effect was a reduction in overall yield of good devices; in other words, devices were fabricated which met specifications. Therefore, it was possible to project with a high degree of confidence improvements in electrical parameter performance based on established principles of PNPN switch design and the knowledge gained in the course of the GATT I development.

1.3 GATT II Contract Objectives

The subject contract design objectives are outlined in Table 1 for the GATT II device. A comparison with the earlier GATT I contract specification indicates an increase in blocking voltage capability from 600 volts to 1000 volts and a doubling in current rating from 50 amperes to 100 amperes. Most significant, too, is the fact that forward drop remains unchanged even though specified at the higher current level. And the all important turn-off time, as measured in the GATT mode, remains at two microseconds.

Equally important to the substantial increases specified for electrical ratings of the GATT II device is that of improvements in fabrication/processing technology. The contractor assumed the responsibility to answer to the problems inherent to the GATT I device which are referenced in the last section. In other words, the need to develop a manufacturable device of reasonable yield and cost was recognized as an objective of the program as well.

1.4 Contract Work Plan

A work plan was established early in the program as prescribed by the contract. The essence of this plan is outlined below. The sequence of tasks is not significant; tasks were performed in parallel where there was no strict dependency and it was advantageous to the overall progress schedule to do so.

Task 1: Device, Design and Develop Thyristor

1 - Establish the design parameters of silicon resistivity, junction depths, basewidths and profiles to attain 1000V blocking capability based upon established PNPN switch theory.

2 - Determine the cathode junction area required to meet the 100 ampere current design and associated current density sensitive parameters, notably forward drop.

3 - Design the required size element (fusion in Westinghouse parlance) assuming a fixed cathode emitter stripe width and planar-passivated cathode-gate junctions.

4 - Conduct experimental studies to determine the optimum n^+p junction relationship relative to overall device performance.

5 - Evaluate the effect of lifetime degradation on such parameters as forward drop and switching characteristics.

6 - Develop an internal contact scheme which provides a convenient means of effectively joining the element with its encapsulation.

Stud temperature = 100°C

Symbol	Description	Specification
V_{DRM}	Minimum forward blocking voltage	1000 volts
V_{RRM}	Minimum reverse blocking voltage	1000 volts
I_T	Maximum RMS forward current	100 amperes
V_{TM}	Maximum steady state forward voltage drop for conduction of 100 amperes	2 volts
t_{on}	Time required to reach V_{TM} after initiation of current conduction with a rate of rise of 100 amperes per microsecond and application of a gate signal of 2.5 amperes for two microseconds.	2 μsec
I_{DRM}	Maximum forward leakage current at 1000 volts	10 ma
I_{RRM}	Maximum reverse leakage current at 1000 volts	10 ma
I_G	Typical gate current to fire at V_{FB} = 5 volts	200 ma
V_G	Maximum gate voltage to fire at V_{FB} = 5 volts	4 volts
I_h	Minimum holding current	25 ma
t_R	Maximum time after anode current has reached zero before anode voltage can be reapplied at the maximum rate of rise of voltage (dV/dt) as stipulated below.	2 μsec
dV/dt	Maximum rate of rise of anode voltage.	400 volt per μsec
di/dt	Maximum rate of rise of current concurrent with and after a gate signal of not more than 2.5 amperes for one (1) microsecond.	400 amperes per μsec

GATT II DEVICE TARGET SPECIFICATION

TABLE 1

7 - Establish a tentative process flow designed to yield working samples which provide sufficient knowledge and understanding to determine the Phase II design and process. This is to be used for fabrication of fifty (50) samples for delivery to NASA.

8 - Determine the appropriate quality assurance measures required to ensure that the device design, fabrication process and test procedures are established (documented) and implemented in a reproducible and controlled manner.

9 - Demonstrate and document the achievements attained under this Task to the NASA Project Manager and obtain approval to proceed with Task 2.

Task 2: Fabrication of Deliverable Items

Fabricate fifty (50) GATT devices in accordance with the results and agreements effected through Task 1.

Task 3: Provide, or Develop, Test Circuits

1 - Develop the necessary equipment and techniques for performing electrical parameter tests according to the specifications outlined in Table 1.

2 - Study other aspects of device performance as they relate to actual applications, particularly the series inverter circuit.

Task 4: Data Recording

1 - Perform the required electrical measurements on finished GATT devices in accordance with the specifications outlined in Table 1.

2 - Provide an Applications Note to assist the circuit designer in proper use of the GATT device.

Task 5: Identify Research Problems Related to Improved Device Rating

Provide recommendations for future developments of the GATT device which project improved device ratings and identify existing device limitations.

II. GATT II DESIGN AND DEVELOPMENT

The fundamental notion here is that of extending the capability of the GATT I device to higher voltage and current levels. In addition, the desirability of expressing this improved version in a design which is manufacturable, i.e. capable of being produced at reasonable yields, was considered to be of equal importance.

2.1 Element Design

2.1.1 Blocking Voltage

The resistivity and basewidth of the n-base region are fundamental internal structure design parameters which determine the blocking voltage capability. Higher voltage requires higher resistivity silicon and a wider basewidth. However, the latter will lead to a higher forward voltage drop and moreso when the lifetime is reduced to achieve fast turn-off to minimize the transient and steady state power losses. These physical design parameters must be carefully selected to provide the narrowest basewidth capable of supporting the required voltage. The initial design parameters specified were: resistivity - 25 to 44 ohm-cm; basewidth - 170 μm (6.6 mils). These values are designed to meet the blocking voltage specification of 1000 volts given in Table 1.

The junction passivation system must also be considered, otherwise the device might be surface rather than bulk limited with respect to blocking voltage. However, present day technology and experience with surface problems at the one-kilovolt level are adequate to relegate it to a secondary role. This is confirmed by results attained in the subject development as will become obvious in later sections of the report.

2.1.2 Current Rating and Forward Drop

The initial review was based on the GATT I descrete cathode emitter design. Although the latter was rated to fifty (50) amperes, it was known that the current density was well below the usual standards for fast switching PNPN devices. The subject specification, Table 1, calls for a capability of 100 amperes maximum RMS forward current. The forward drop is given as 2.0 volts at 100 amperes. Furthermore, the turn-off time specification of 2.0 microseconds immediately thrusts the device into the forefront of the category of fast switch devices. This implies additional restraints on forward drop due to the need for reduction of minority carrier lifetime in the n-base region.

2.1.2 Current Rating and Forward Drop (Cont.)

A comparison was made to the existing Westinghouse T507 thyristor of the 1000 volt category. The latter is a fast-switching thyristor employing lifetime control techniques as part of the fabrication process which are equivalent to that projected for GATT II. An abbreviated table of values expresses the similarities.

	T507	GATTS
Blocking Voltage (volt)	1000	1000
RMS Current (amp)	110	100
Forward Voltage (volt) @ 100 amperes	2.0	2.0
Cathode Emitter Area (cm^2)	0.89	0.86

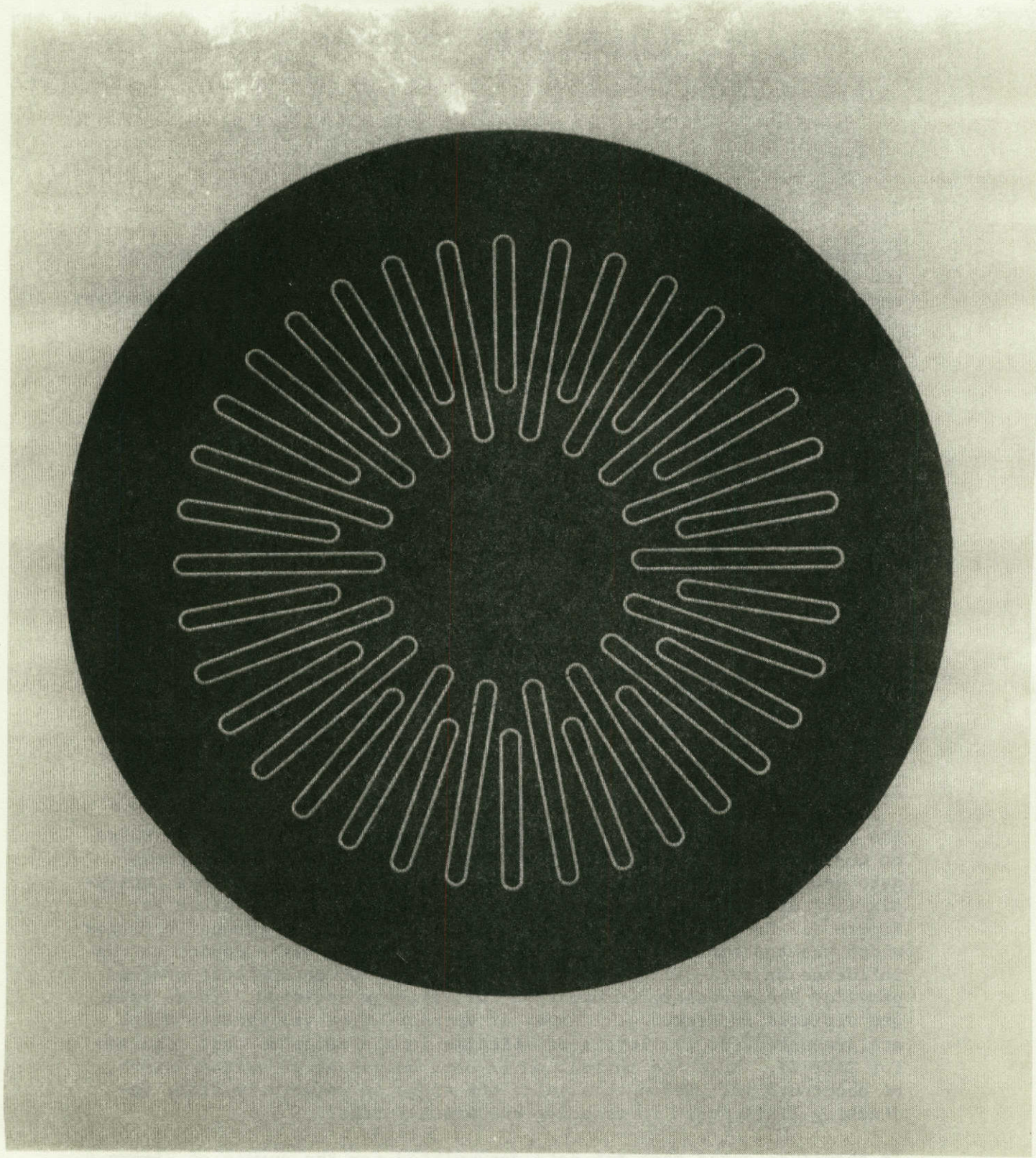
The values indicate a virtual one-to-one correspondence for all parameters listed. Thus it is concluded that the original GATT I device is sufficiently large to meet the specifications for RMS current and forward drop. This decision, too, is confirmed by the test results on actual devices which are presented later in this report.

2.1.3 Plan View Design

The acceptability of the GATT I design for rating to 100 amperes based on current density leads directly to a consideration of the cathode-gate geometry or plan view design. The earlier version employs thirty-six (36) discrete fingers arranged in a radial pattern as shown in Figure 3. Each finger is 0.5 mm (0.020 inch) wide. A change in finger width was contemplated and variations were studied with respect to the influence on turn-off capability. The results of an in-house program provided the necessary information for making a decision. These data are depicted in Figure 4. Curves of turn-off time vs. emitter width are presented for two levels of lifetime in the range of that required for GATT II. Note the inflection in both curves at an emitter width of about 0.5 mm. Below this value the slope is relatively flat, indicating little gain in reducing the width further.

It should be noted that the data accumulated for the curves of Figure 4 were taken with the devices operated in the gate controlled switch turn-off mode.

Based on the aforementioned studies, it was decided to design about the 0.5 mm finger width, thus retaining the GATT I plan view.



GATT Device Plan View

Figure 3

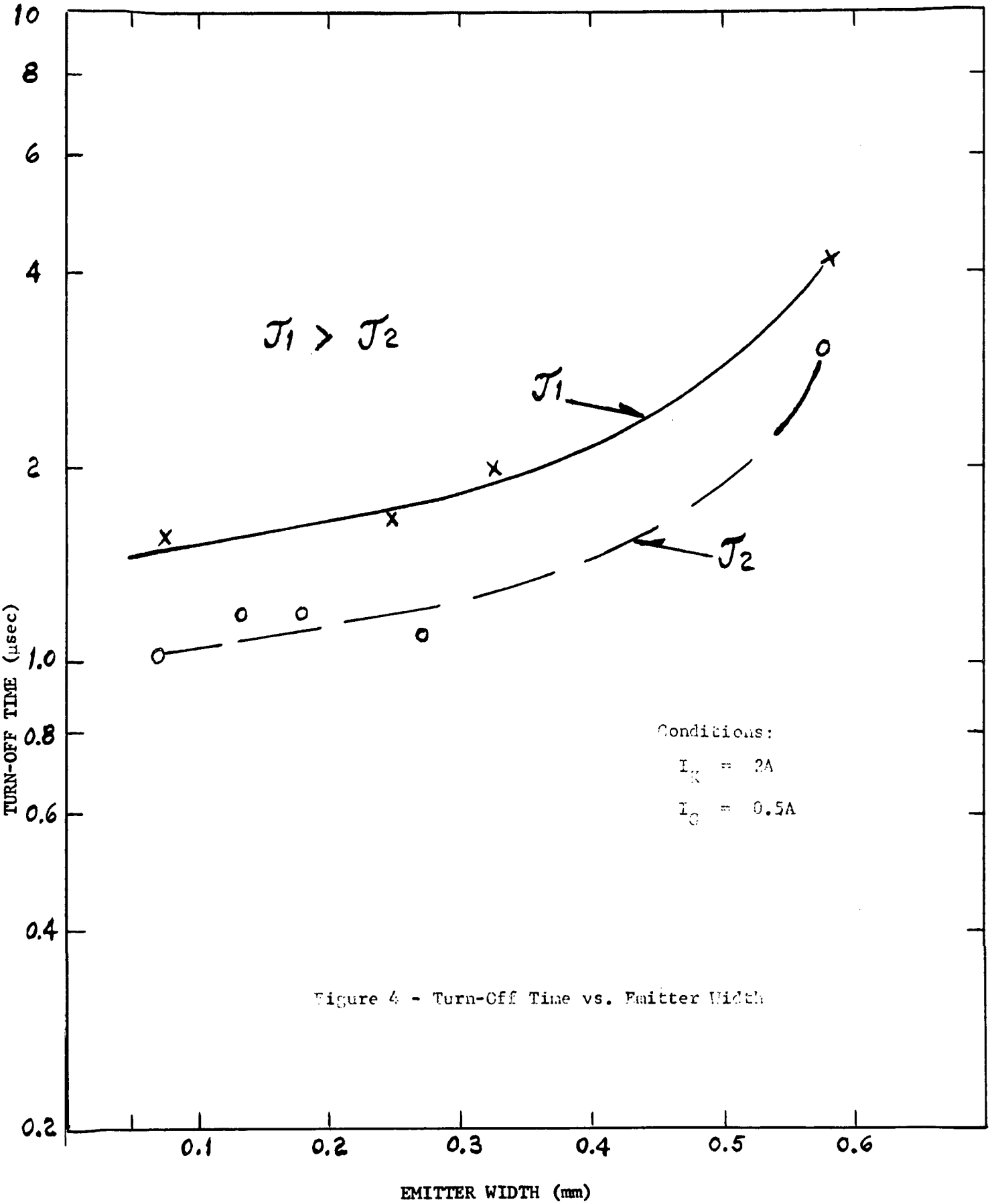


Figure 4 - Turn-Off Time vs. Emitter Width

2.1.3 Plan View Design (Cont.)

A very important facet of the design which is not obvious from the plan view shown in Figure 3, is the employment of planar passivated cathode-gate junctions. This modification in structure, in comparison to the mesa configuration of GATT I, provides the basis of achieving the objective emphasized in Section 1.2, viz. the means of fabricating sets (all thirty-six fingers) of acceptable discrete cathode junctions. This concept is coupled with an inventive scheme for contacting described in Section 2.4 to yield a complete solution to the problem which plagued GATT I.

2.1.4 Profile Design

The increase in blocking voltage capability has been discussed and the need to optimize the overall device structure was indicated such that forward drop and turn-off time are not unduly compromised. This optimization required careful design of the complete PNPN concentration profile. Parameters of concern (note Figure 5) include surface concentration, gradient, junction depth and base width. Equally important is the so-called working point, i.e. the peak concentration in the p-base which is further defined by the cathode junction depth. This latter parameter determines the sheet resistance under the cathode emitter which is particularly significant for turn-off devices such as the GATT and GCS. The AGE experimental series discussed in Section 2.3 addresses this matter directly.

2.1.5 General Considerations

The silicon wafer with junctions formed therein and oxide passivation formed across the cathode-gate junction has been discussed thus far. The complete element (fusion in Westinghouse terminology) further incorporates metal contacts to the cathode, gate and anode regions and an appropriately treated blocking junction periphery. Standard Westinghouse construction is used for these and is briefly described in the following.

The anode contact consists of a molybdenum disc which is attached to the anode diffused region by high temperature alloying with aluminum. Molybdenum provides a suitable backing plate for the device element in that it closely matches the silicon in expansion characteristics yet provides good thermal and electrical conductivity. Aluminum is an acceptor atom and effects an efficient non-rectifying contact to the p^+ anode region.

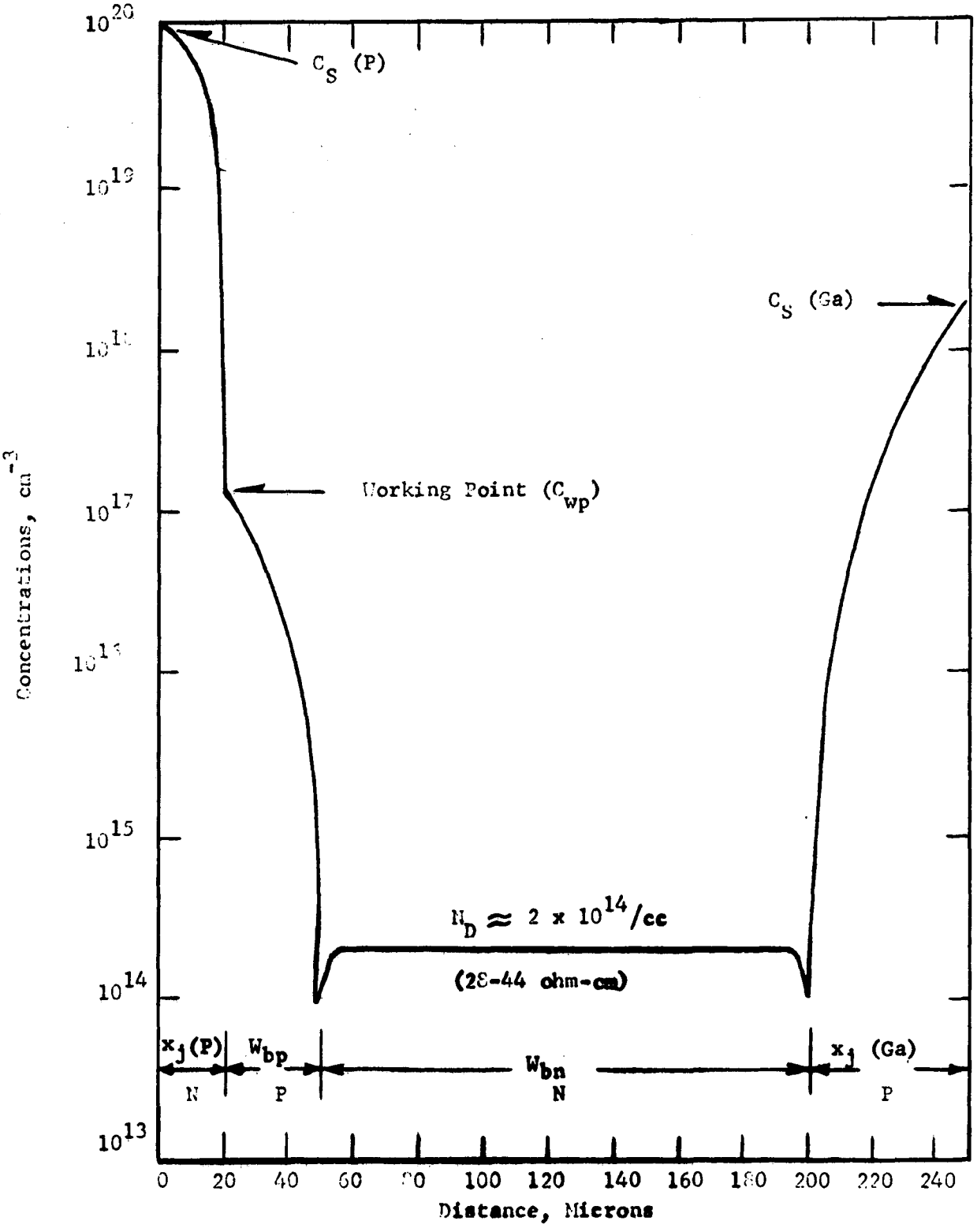


Figure 5 - Sample PNPN Concentration Profile

2.1.5 General Considerations (Cont.)

The cathode and gate regions employ evaporated aluminum as the contact material. Mask and etch processes are used to remove the aluminum between adjacent cathode and gate regions; the metallization pattern is then sintered at a relatively low temperature. The latter effects a good non-rectifying contact to the p^+ gate and the n^+ cathode regions. The low temperature sintering is required to avoid forming a spurious p^+n junction near the surface of the n-type cathode region.

The junction periphery of the metallized element is angle beveled, etched, and coated with an organic material.

The result of the contact and junction treatment steps yield the finished element as shown in the cross-section view of Figure 6.

2.2 Process Developments (Element)

The fabrication process for a power semiconductor device can be divided into a sequence of six major process centers:

1 - Silicon Preparation

2 - Junction Formation

3 - Contacting

4 - Junction Passivation

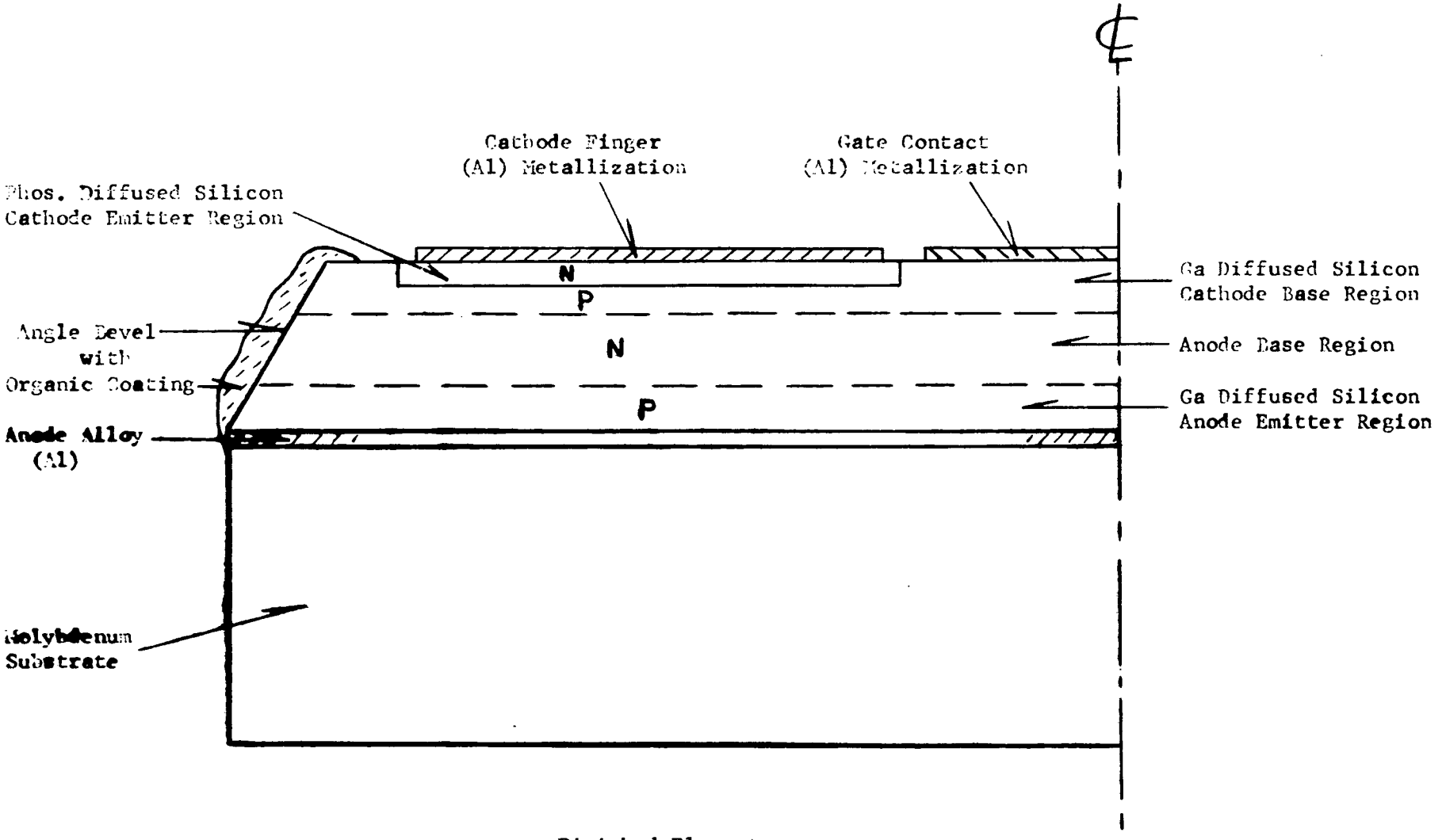
5 - Encapsulation

6 - Test

The first four are included in the fabrication of the element or fusion. The latter two are discussed elsewhere in later sections of this report.

Process development relative to silicon preparation was limited to establishing the single side etch process. Wafers are masked with apiezon wax on one side and etched twenty-five at a time in a large beaker containing 7:1:1 $HF:HNO_3:HAc$. Uniformity of etch is ensured by applying a swirling motion by mechanical means.

The junction formation process center includes oxidation and photomasking steps in addition to the p- and n-diffusions. Studies pertinent to this program included anode reinforcement diffusion and oxide passivation of the cathode-gate junctions.



Finished Element
Cross-Sectional View Schematic

Figure 6

Anode reinforcement was attempted by performing a selective boron diffusion into the anode region. The forward drops of these devices were compared with controls which had the normal p^+ diffusion only. The comparison yielded no statistical difference in V_{TM} measured at 625 amperes and 1500 amperes, respectively. Other parameters were generally within ten percent of the control devices. Thus the reinforcement diffusion was not added to the process since it implied an extra step in the process with no observable gain as a result.

Oxidation per se has been part of the GATT process insofar as it serves to mask the gate region during phosphorous diffusion of the cathode junctions. A photochemistry operation to open windows in the oxide prior to metallization was introduced. Thus the SiO_2 is retained over the cathode-gate junction for the express purpose of passivation.

The contacting and blocking junction passivation steps are standard operations and required no change.

In summary, process developments were limited to several particular areas under the subject program. More focus and attention was placed on adjusting the design parameters to optimize the balance of device characteristics in accordance with the Table 1 specifications. The experimentation to this end is detailed in the next section.

2.3 'AGE' Experiment

The second generation GATT development was enhanced by the existence of in-house programs which were directed toward analogous objectives for other device structures. For example, the results achieved in gate controlled switch studies provided the data for selection of the cathode finger width of GATT II (see Section 2.1.3). In addition, a large scale experiment, denoted by the acronym AGE, was designed to evaluate a number of parameters which relate to the PNPN profile design. It was the purpose of this study to provide basic design information for a variety of devices, including GATT, GCS and conventional fast switching thyristors. Thus the levels of parameters selected are not necessarily peculiar to GATT II devices.

The AGE experiment design is presented in Table 2. In each of the six runs (AGE I through AGE VI) there were about forty slices built to the GATT II plan view illustrated in Figure 3. An equal number of standard production thyristors were included in each run for purposes of comparison and control.

	PARENT SILICON			P-TYPE DIFFUSION						N-TYPE DIFFUSION		
	Resistivity (ohm-cm)	Lap Thk. (μm)	Etch Thk. (μm)	Step 1	Step 2	Anode P++	C_s (cm^{-3})	X_j (μm)	W_{bn} (μm)	C_{wp} (cm^{-3})	X_j (μm)	W_{bp} (μm)
AGE I	41-59	365	325	Al	Ga	---	10^{18}	70	185	$5x10^{16}$ $1x10^{17}$ $3x10^{17}$	-- 15 --	-- 55 --
AGE II	41-59	340	300	Ga	--	B	10^{18}	50	200	$5x10^{16}$ $1x10^{17}$ $3x10^{17}$	-- 15 --	-- 35 --
AGE III	41-59	315	275	Ga	--	---	10^{18}	40	195	$5x10^{16}$ $1x10^{17}$ $3x10^{17}$	-- 13 --	-- 27 --
AGE IV	28-44	315	290	Ga	--	B	10^{18}	60	165	$5x10^{16}$ $1x10^{17}$ $3x10^{17}$	-- 15 --	-- 45 --
AGE V	28-44	340	315	Al	Ga	---	$4x10^{17}$	70	170	$5x10^{16}$ $1x10^{17}$	-- 12-15	-- 55-58
AGE VI	28-44	340	315	Ga	--	B	10^{17}	60	165	$5x10^{16}$	--	--

AGE Experiment Design
Table 2

As seen in Table 2, there were two different ranges of n-base resistivities used: 28 through 44 ohm-cm and 41 through 59 ohm-cm. These values correspond to two blocking voltage ranges: 800 to 1000 volts and 1000 to 1200 volts, respectively. Both aluminum-gallium (Al-Ga) and single gallium (Ga) diffusion sources were used to form the blocking junctions. Phosphorous was then diffused to different working points which yielded variations in base resistance. Carrier lifetime was also varied. The interactions of these fundamental design parameters were reflected in the shift of electrical characteristics as measured on the completed fusions. This information was an invaluable aide in optimizing the trade-offs to best-fit the Table 1 GATT II specifications.

AGE I and AGE IV experimental runs yielded especially pertinent data from which the design center of the final sample runs was established. Table 3 presents the test data on AGE I for both control and GATT II devices. Two working points were investigated. Due to a relatively low surface concentration out of the gallium diffusion, it was not feasible to make devices with a working point of 3×10^{17} atoms/cc as per the original design. Three levels of lifetime were evaluated.

Table 4 presents the test data on AGE IV, again for both control and GATT II devices. In this case, all three working points were realized. And three levels of lifetime equivalent to these in AGE I were employed. AGE I devices were higher voltage as expected from the slice thickness/resistivity combination. In similar predictable fashion, the forward drop is lower for AGE IV devices with approximately equivalent working point and the same level of lifetime degradation. Similarly, the narrower basewidth AGE IV devices yielded the better turn-off performance - measured both conventionally and in the GATT mode. In summary, AGE I yields a combination of high voltage, reasonable forward drop and high turn-off time devices; AGE IV yields lower voltage, reasonable forward drop and low turn-off time devices. The conclusion, for purposes of formulating the design of the final GATT II devices, is to modify the AGE IV design to compensate for the lower voltage yet retain the combination forward drop and turn-off time.

2.4 Contacts and Encapsulation

Section 2.1 described the basic element or fusion which constitutes the heart of the GATT device. Figure 3 presents a plan view of the fusion; Figure 6 presents a cross-sectional view of the fusion. What remains in the fabrication cycle of a complete, usable GATT device is that of packaging this fusion. Contacts are required to provide low resistance paths for current flow, electrical and thermal. And the somewhat delicate fusion must be insulated from undue mechanical stress and the surrounding chemical environment.

			V_{DRM}[3] (volt)		V_{RRM}[3] (volt)		V_{TM} (volt)			I_{GT} (ma)	V_{GT} (volt)	Turn-On Current	Turn-Off[4] Time
			25°C	125°C	25°C	125°C	@ 100A	625A	1500A	25°C	25°C	(A)	(μs)
Standard Thyristor (Controls)	C_{wp}	$\tau 0$	1350	1390	1410	1400	0.94	1.27	1.70	100	0.95		
		$\tau 1$					1.06	1.42	1.89	120	1.26		
		$\tau 2$					2.11	2.68	3.70	330	1.95		
	C'_{wp}	$\tau 0$	1440	1410	1210	1000	0.90	1.27	1.71	40	0.75	N/A	N/A
		$\tau 1$					0.99	1.41	1.94	44	0.93		
		$\tau 2$					1.46	2.42	3.61	70	1.05		
GATT Device	C_{wp}	$\tau 0$	1250	---	1400	1360	1.08	1.83	2.28	6	0.85		
		$\tau 1$					1.12	2.04	3.34	11	1.03		
		$\tau 2$					1.80	3.58	6.05+	33	0.82	14	6
	C'_{wp}	$\tau 0$	1380	---	1420	1280	1.06	1.88	2.40	4	0.84		
		$\tau 1$					1.10	1.94	3.16	2	0.96		
		$\tau 2$					1.42	3.11	5.44	4	0.98	10	11

Note 1 - $C_{wp} > C'_{wp}$ (atoms/cc)

2 - $\tau 0 > \tau 1 > \tau 2$ (lifetime in microseconds)

3 - $I_{DRM} = I_{RRM} = 7$ ma (25°C), = 13 ma (125°C)

4 - GATT mode

AGE I Test Data

Table 3

			V_{DRM}[3] (volt)		V_{RRM}[3] (volt)		V_{TM} (volt)			I_{GT} (ma)	V_{GT} (volt)	Turn-On Current	Turn-Off[4] Time
			25°C	125°C	25°C	125°C	@ 100A	625A	1500A	25°C	25°C	(A)	(μs)
Standard Thyristor (Controls)	C_{wp}	τ_0	850	900	990	1100	0.95	1.22	1.58	165	0.86		
		τ_1					1.10	1.41	1.85	180	1.04		
		τ_2					4.25	4.56	4.59	660	1.30		
	C'_{wp}	τ_0	920	990	1070	1110	0.88	1.16	1.51	79	0.92		
		τ_1					0.93	1.25	1.69	85	0.89	N/A	N/A
		τ_2					1.78	1.96	2.59	169	1.01		
	C''_{wp}	τ_1	910	930	1090	1150	0.84	1.11	1.43	60	0.90		
		τ_2					0.89	1.22	1.63	61	0.76		
		τ_3					1.35	1.66	2.23	95	0.87		
GATT Device	C_{wp}	τ_0	790	800	970	1120	1.06	1.71	2.10	9	0.96		
		τ_1					1.05	1.83	2.84	3	1.23		
		τ_2					2.00	3.44	5.65	209	0.92		2.5
	C'_{wp}	τ_0	750	980	600	660	0.98	1.53	1.85	4	0.85		
		τ_1					1.03	1.63	2.47	2	0.88		
		τ_2					1.39	2.51	4.01	8	0.82	25	4.0
	C''_{wp}	τ_0	740	820	820	850	0.96	1.48	1.79	2	0.91		
		τ_1					1.01	1.58	2.38	2	1.05		
		τ_2					1.28	2.32	3.62	4	0.97	15	6.0

Note 1 - $C_{wp} > C'_{wp} > C''_{wp}$ (atoms/cc)

2 - $\tau 0 > \tau 1 > \tau 2$ (lifetime in microseconds)

3 - $I_{DRM} = I_{RRM} = 7$ ma (25°C), = 13 ma (125°C)

4 - GATT mode

AGE IV Test Data

Table 4

GATT II contact and encapsulation development focused on the need to provide a means of selectively contacting the cathode and gate regions. This was straightforward in the case of GATT I since the cathode plane of contact was raised above the gate plane of contact due to the mesa-type construction. The bonding of cathode bus-bars simply amplified this concept. However, the subject program assumed the fusion to present to its encapsulation a singular planar array of cathode and gate contact areas. This resulted from the incorporation of the planar oxide-passivated system into the GATT II fusion. Thus, a means of selective contacting was no longer inherent to the fusion but rather had to be supplied by the mating contact system.

Again, the subject program benefited from parallel in-house Westinghouse programs. A technique for contacting interdigitated patterns was developed about the use of metal preforms chemically milled to match the pattern of concern. Upon attachment to the fusion, the plane of the cathode contact areas is raised above that of the gate contact areas by the thickness of the preform. Figure 7 illustrates the preform used for the GATT II devices. The only modification required of the original fusion design was to substitute silicon dioxide for the gate metallization in the area below the rim of the preform. Otherwise, the cathode contact would short to the gate. This presents no problem since the gate metallization in that region is virtually non-functional. The resultant plan view of the fusion is shown in Figure 8.

The matter of maintaining the contact preform in alignment with the cathode metallization pattern was resolved by "spot gluing" with silicone varnish at the preform outer periphery to the underlying fusion. The same material used for junction coating served this purpose quite well.

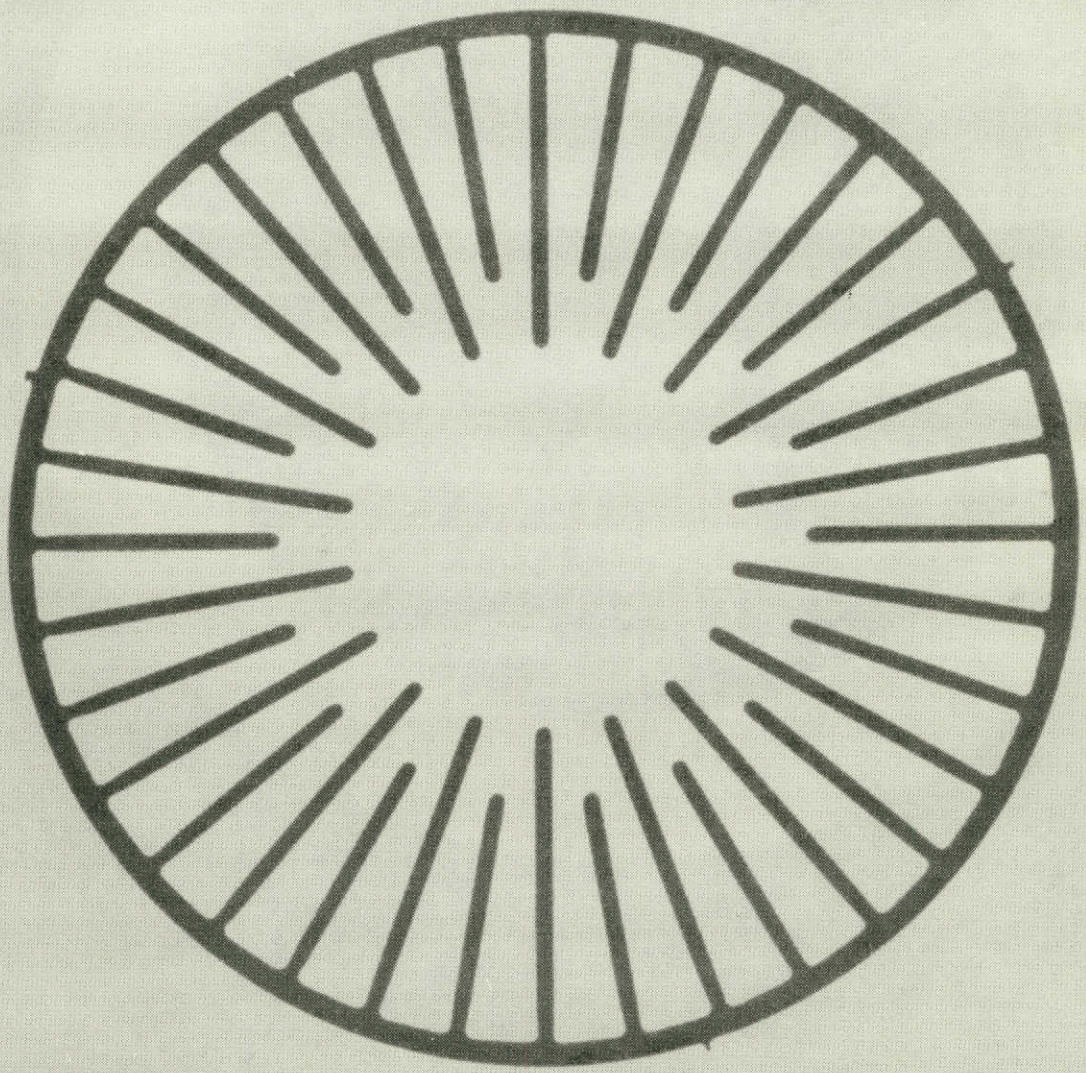
Final encapsulation of the device is achieved by assembling the fusion-plus-contact into a standard Westinghouse CBE (compression bond encapsulation) package. Figure 9 illustrates the package before the ceramic seal is assembled and welded to provide the hermetic seal. As noted, this system is standard and is identical to that used for GATT I. Figure 10 is a photograph of a finished device.

2.5 Quality Assurance Controls

Quality assurance controls are routine practice throughout the manufacture of power semiconductor devices. These consist mainly of incoming materials inspection, process and test equipment calibration and product inspection per se through the fabrication process and final test sequence.

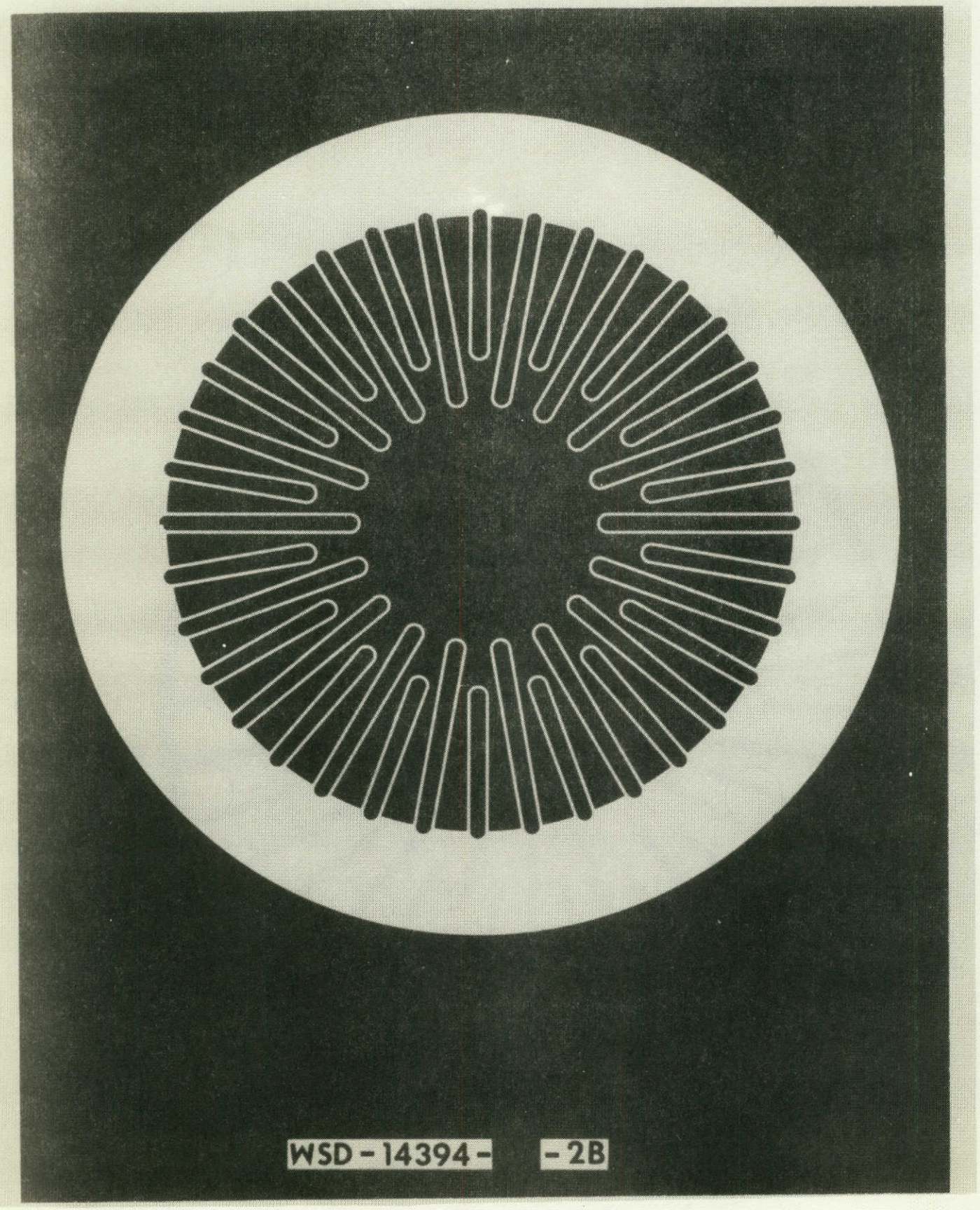
The subject development leaned heavily on production quality control measures. This resulted from the use of standard materials and parts where possible, as well as the fact that a number of the fabrication steps were performed in the manufacturing area. The latter implies the use of production services, equipment and (sometimes) personnel.

Operations performed in the Engineering Pilot Line were subjected to strict quality control measures. These will be further detailed in Section 4.



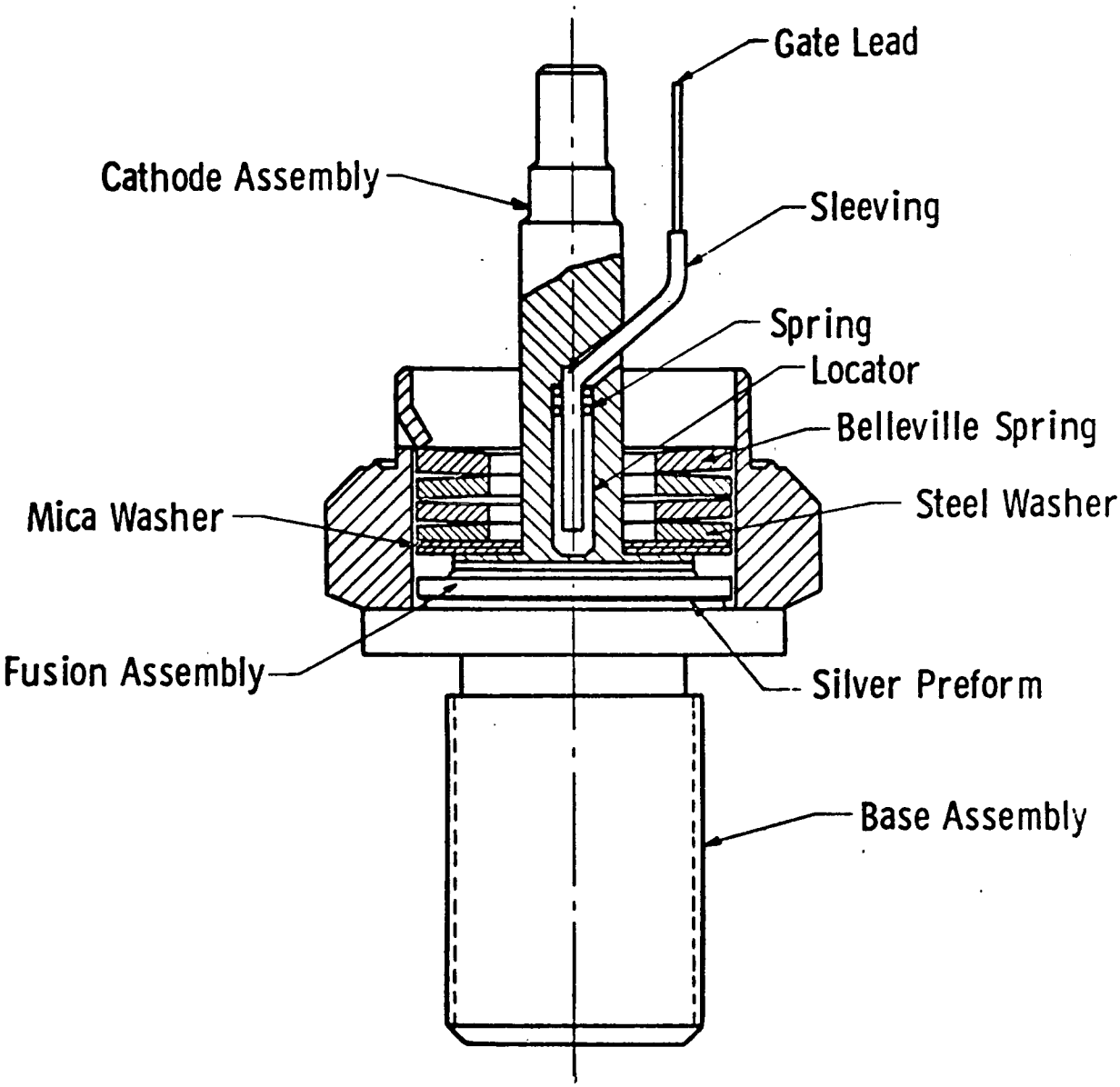
Cathode Contact Preform

Figure 7



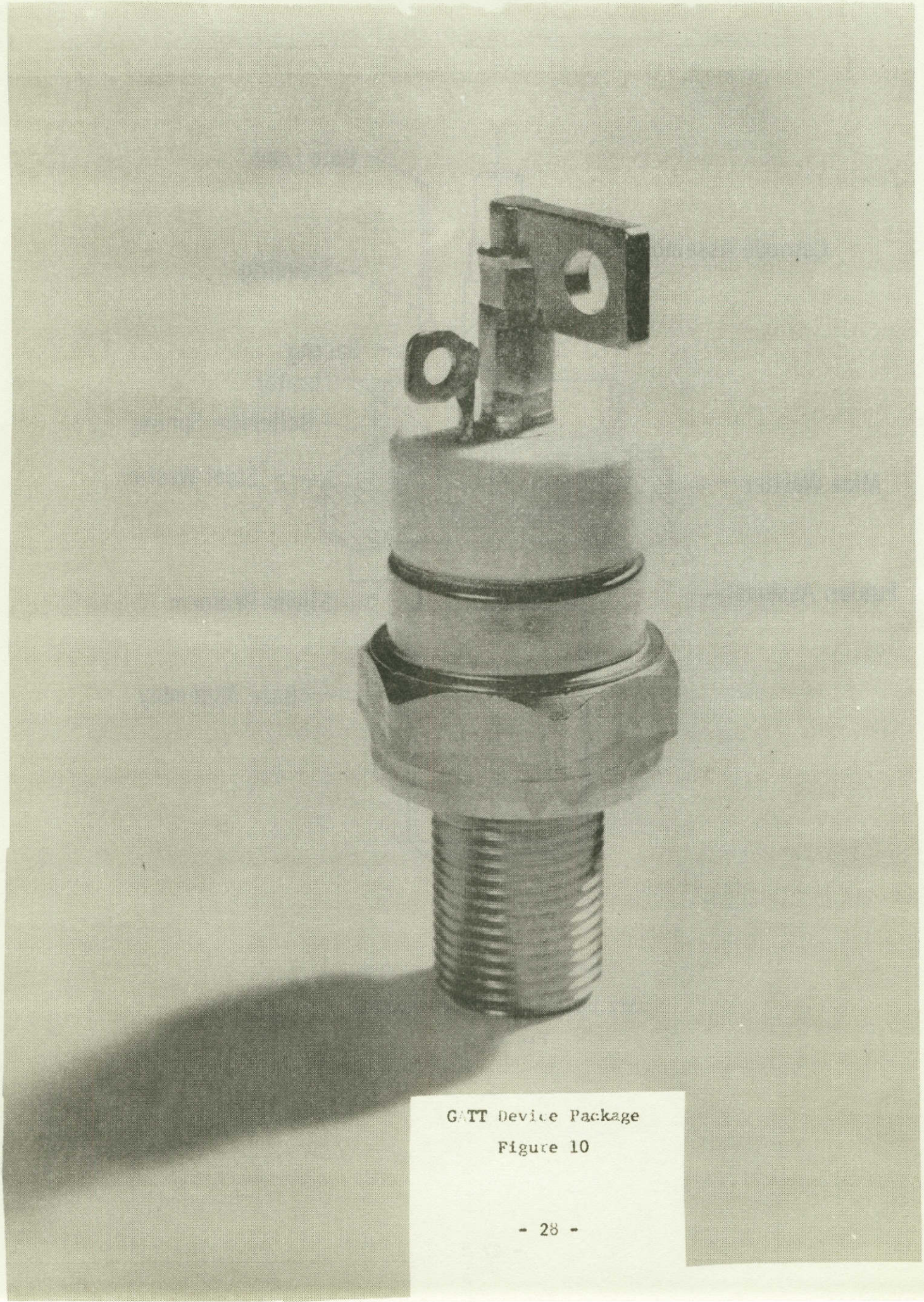
GATT II DEVICE, FINAL PLAN VIEW

Figure 8



GATT DEVICE PRE-ENCAPSULATION

Figure 9



GATT Device Package

Figure 10

III. TEST CIRCUIT DESIGN AND DEVELOPMENT

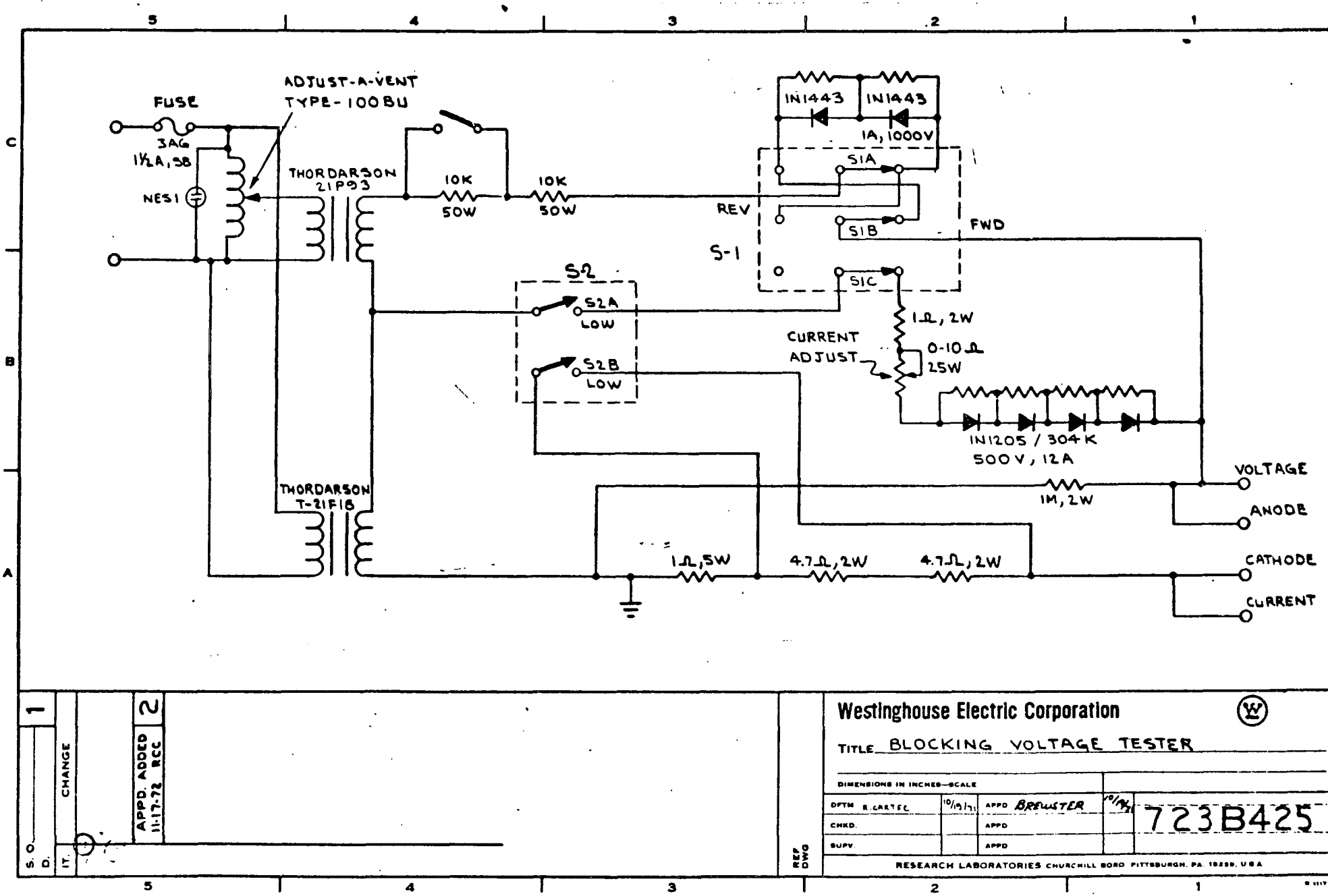
The test functions available in the Device Evaluation Group at the Research Laboratories consisted of standard thyristor parameter evaluation facilities. Only two additional test units had to be built in order to provide circuitry appropriate to test the GATT device in its unique dynamic mode of operation. The first additional test unit was envisioned to be a load simulator designed to generate half-sinusoidal load current pulses peculiar to the intended usage of the GATT, viz. application in a 50 kHz series type inverter. The load simulator did not include its own load current power supply; but it did include a self-powered timing unit and gate driver system. The second additional test unit reproduced the self-powered timing unit and gate driven system, and served to apply proper turn-on and gate-assisted turn-off drive when used in conjunction with an in-house standard turn-off time tester. During the time period from initial fabrication of the GATT II device and finalization of its design, the intended usage of the load simulator was changed. This revision is discussed under the final subject category in this section.

3.1 Standard Thyristor Test Circuits

3.1.1 Blocking voltage characteristics

The circuit diagram for the blocking voltage (V_{DRM}, V_{RRM}) tester is given in Figure 11. To determine device blocking voltage tolerance, voltage is applied under variac control, through an isolation transformer and half-wave rectifier, across the anode-cathode of the test device. Two 10,000 ohm resistors are positioned in series with the half-wave rectifier, one of which may be shorted out by a switch. These resistors supply current limiting action such that when the avalanche point of a device is exceeded, leakage current will not increase in an uncontrolled fashion but will be limited by the preselected 10,000 or 20,000 ohm series resistance. Switch S1A and S1B are provided to reverse the sense of voltage applied to the test device. Switch S-2 in conjunction with the FWD position of S1C may be used to supply a large current to a test device after turn-on by voltage switching. GATT devices are not normally tested in this fashion. The voltage and current impressed on the test device are viewed at the vertical and horizontal input terminals of a Type 503 Tectronics Oscilloscope, yielding the familiar I-V characteristic.

The maximum voltage range of this system and a 503 oscilloscope with a X10 multiplier is 1800 volts and 5 ma. When devices near 1000 volts are tested, well over 15 ma peak is available. The measured device leakage current is viewed across a 10 ohm resistor. The 503 oscilloscope may then be calibrated at 10 ma/milli-volt in the horizontal direction. Typical photographs of I-V traces for sample GATT devices are presented in the test result presentation.



Blocking Voltage Tester, Circuit Diagram

Figure 11

3.1.2 Gate Forward and Reverse Characteristics

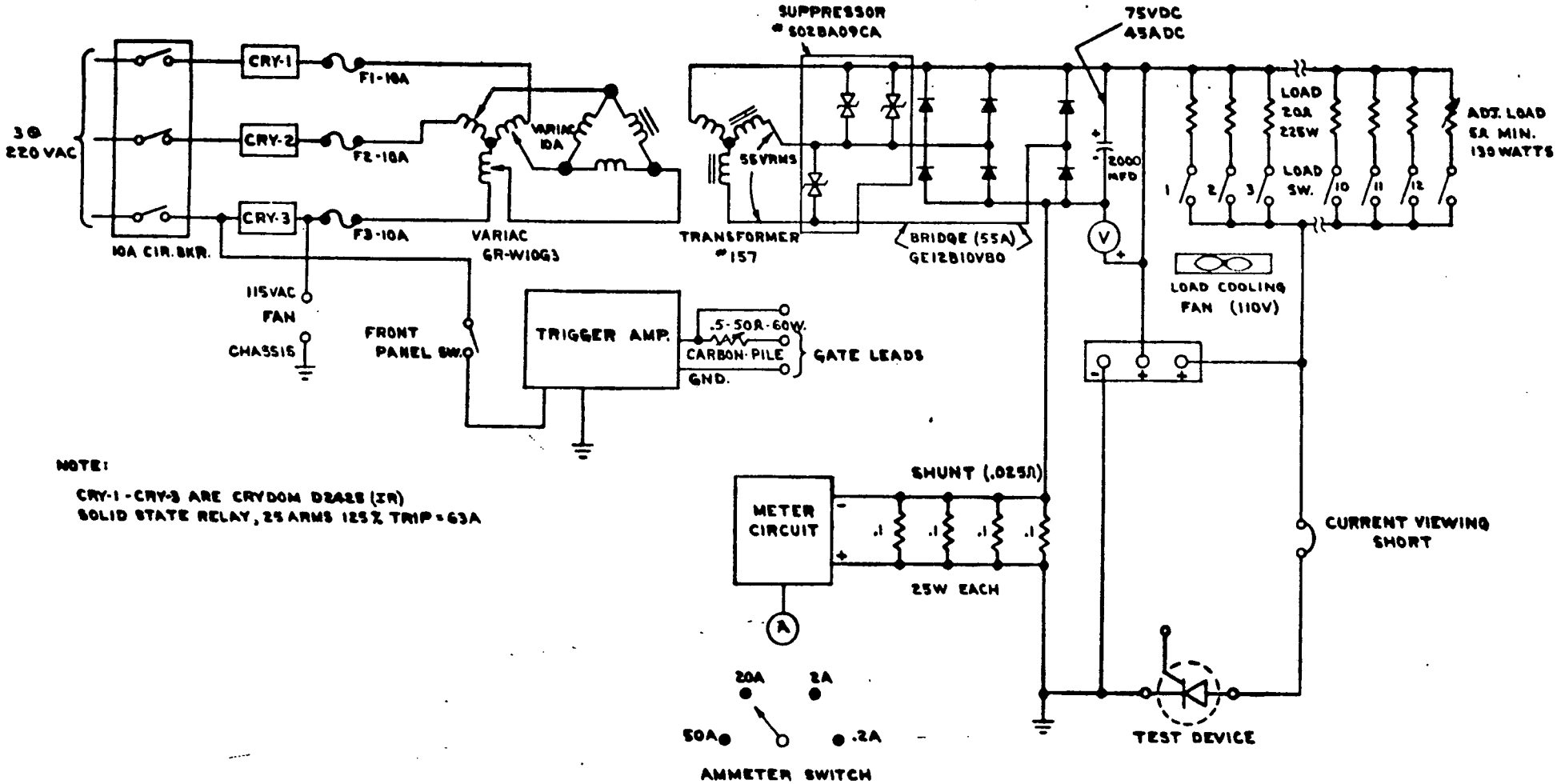
Oscilloscope measurements of device forward and reverse I-V gate characteristics are measured with a standard Tecktronix Type 575 transistor curve tracer.

3.1.3 Gate Trigger Sensitivity Characteristics

The circuit diagrams for the gate trigger sensitivity (V_{GT}, I_{GT}) tester are given in Figures 12 and 13. These parameters determine the minimum gate current and gate voltage required to cause turn-on of a thyristor switch. The tester is designed to study holding and latching current characteristics as well. To determine gate sensitivity parameters, a known load is applied to the anode of the test device. The considerations of the load are (1), that anode current be greater than the known latching current of the device under test, and (2), that anode voltage be large enough to reduce the effect of gate forward potential on the conducting load current. As an example of the second condition, some early thyristor gate sensitivity testers were designed with anode supplies of 6 volts dc. A thyristor under test which was characterized by a conducting forward voltage drop of several volts meant that the available supply with which to drive anode current was more nearly 4 volts rather than 6 volts. As a consequence, the built-in thyristor device parameters could affect load current and the validity of the measurement itself. To eliminate these effects, the supply voltage of the subject tester is available up to 75 volts dc and actual tests are generally run at 50 or 75 volt anode supply levels.

The power circuit (Figure 12) consists of an adjustable three phase ac source which is full-wave rectified and capacitively filtered to produce up to 75 volts at 50 amperes dc. Provisions are made to vary the load resistance in discrete steps, or a fraction of rated load may be continuously adjusted with a carbon pile variable resistance. As noted above in condition (1), load current is set to a value of no less than the minimum known latching current.

For convenience sake and protection, the ac input to the power circuit is under control of a solid state relay. By simple push button control, supply output can be shut down; or in the event of overload, it will automatically shut down. Load current is monitored with a metering circuit designed such that the meter range is adjustable without interrupting anode current. This circuit is given later and will be further explained under the discussion of holding current tests.



I_{LX}, I_{HO}, V_{GT} and I_{GT} Tester, Power Circuit Diagram

Figure 12

WESTINGHOUSE ELECTRIC CORPORATION

TITLE $I_{LX}, I_{HO}, V_{GT}, I_{GT}$ TESTOR POWER CIRCUIT

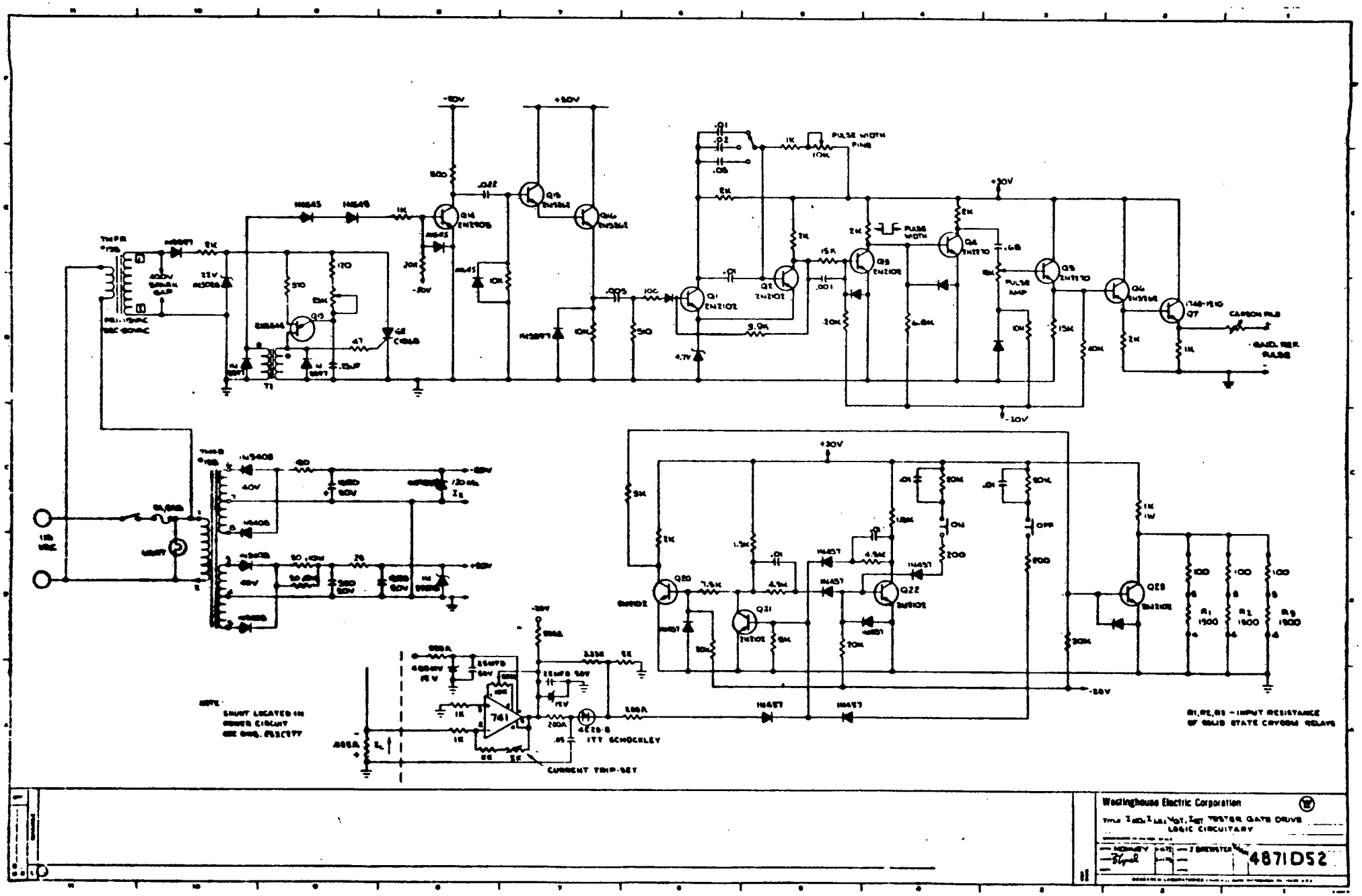
DIMENSIONS IN INCHES—DO NOT SCALE DRAWING | SUB. 1

DRTH R.C.CRAMER 3/4/76 APPD J.BREWSTER 3/4/76

CHKD APPD

255C277

1 CHANGE



I_{LX}, I_{HO}, V_{GT} and I_{GT} Tester, Logic Circuit Diagram

Figure 13

3.1.3 Gate Trigger Sensitivity Characteristics (Cont.)

The power circuit diagram of Figure 12 shows the gating circuit in simple block diagram form. This is expanded in detail in Figure 13, the logic circuit diagram. The upper portion of Figure 13 is a 100 Hz timing oscillator with additional pulse forming and amplification to produce the controllable gate pulse for turn-on sensitivity test. The thyristor trigger pulse is formed by one-shot Q_1 and Q_2 which includes coarse and fine pulse width controls. Pulse amplitude control is inserted in the base of Q_5, and output transistors Q_6 and Q_7 provide final current amplification.

The conventional thyristor gate sensitivity test should use a gate trigger of at least 50 microseconds to avoid changes in apparent trigger sensitivity which can be due to insufficient pulse width. For normal testing, the output of the gate driver is set at 50 microseconds duration and 25 volts open circuit. The carbon pile current adjustor may then be used to increase gate drive current until turn on is achieved. Thyristor gate voltage is viewed on an oscilloscope with a voltage probe, and gate current to fire is measured on an oscilloscope with a current probe. V_{GT} and I_{GT} are then easily determined for the particular thyristor under test. However, the current rise-time available from this driver of only one microsecond is inadequate to perform special GATT turn-on tests. Other test equipment has been devised for gate drives with fast rise time requirements and will be covered later in this report.

The remaining circuitry of the logic circuit diagram of Figure 13 includes push button on-off control for the solid state circuit breaker, as well as an overcurrent sensor and a trip circuit. Transistor Q_{21} and Q_{22} make up a standard flip-flop, whose state is determined by appropriate on and off controls. Transistor Q_{20} and Q_{23} condition the logic of the flip-flop to drive solid state relay gates R_1, R_2 and R_3. The flip-flop logic may also be set by the output of a 741 amplifier overcurrent trip. The input to the 741 amplified is taken across a .025 ohm resistor through which full load current flows. When load current reaches 63 amperes, or 130% of rated load, a Shockley diode discharges a small capacitor to trip the logic flip-flop to the off condition.

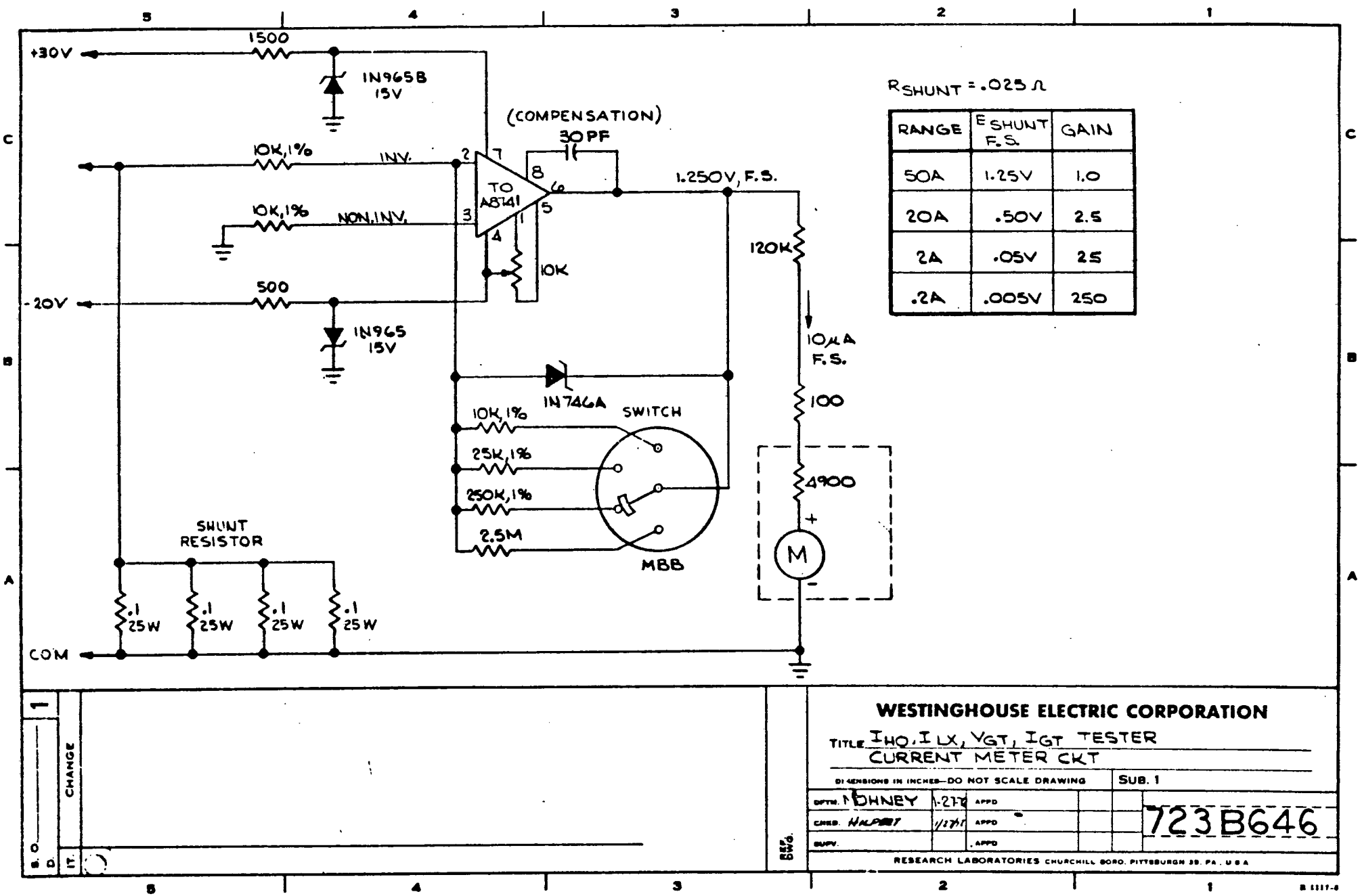
3.1.4 Latching and Holding Current Characteristics

Measurements of latching current (I_L) and holding current (I_H) parameters are made with the equipment described in the preceding section and given in Figure 12 and 13.

3.1.4 Latching and Holding Current Characteristics (Cont.)

The latching current measurement is made first. Gate drive for the measurement is chosen at some increment in excess of the measured minimum gate current to fire. For GATT devices, the conditions selected are two amperes of gate drive, a pulse width of 50 microseconds, and an open circuit gate voltage of 25 volts. Anode load resistance is made as small as possible, and anode voltage is set to 50 volts. The adjustment carbon pile resistor serves best as the singular load resistor for this test. The test is started with insufficient load current for latching and has a unique response. Anode current will exist prior to latch, but only during the period in which gate drive is being applied. Also, anode voltage will collapse only during the period in which gate trigger current is being applied. Otherwise, anode current will return to zero, and anode voltage will rise up to full applied voltage. To measure latching current, the pulsating anode current is viewed with a current probe, and the magnitude just prior to complete turn-on is recorded. This should agree with the current measured on the d.c. metering circuit just after turn-on. As long as gate current is applied, the anode current may be varied above and below the latching value and in general the test device will latch or return to the non-latch condition dependent upon the magnitude of the anode current. The best indication of latching will be a complete collapse of anode voltage, or a sudden rise of the load current ammeter to the level of current at latching, or the disappearance of signal from the current transformer output since the current at latch will rise to a d.c. value.

If gate drive is removed by turning gate voltage to zero after latching, then further variation of load current will not cause return of the switch to the pre-latch condition. Complete control of anode current by the gate will have been lost and true latch will have been sustained. Load current may then be reduced below the latching level with restoration of the blocking state. This condition is that needed for measurement of holding current. With gate drive removed and latch sustained, load current is decreased till blocking voltage once again is supported by the test device. The current at which this occurs is termed holding current; it is generally less than the latching current value. For holding current measurement the load current monitoring ammeter is used and this portion of the tester is described in the current metering circuit of Figure 14. (It is the meter circuit portion of Figure 12). The meter circuit is designed to meet the holding current measurement requirements. The technique for measurement of holding current is described in the following. Anode voltage is set at 50 volts and the latching state is sustained with open circuit gate voltage set to zero. Load resistance is increased and load current decreased. Anode current is measured at the point just prior to restoration of the blocking state. In order to accurately measure the holding current, which is some small fraction of rated device current, it is necessary to change ammeter range without interruption of load current. This is done with the ammeter circuit of Figure 14. Here the current signal, taken from a .025 ohm shunt, is amplified by a type TO-A8741 operational amplifier. The required range



I_{LX}, I_{HO}, V_{GT}, and I_{GT} Tester, Current Metering Circuit Diagram
Figure 14

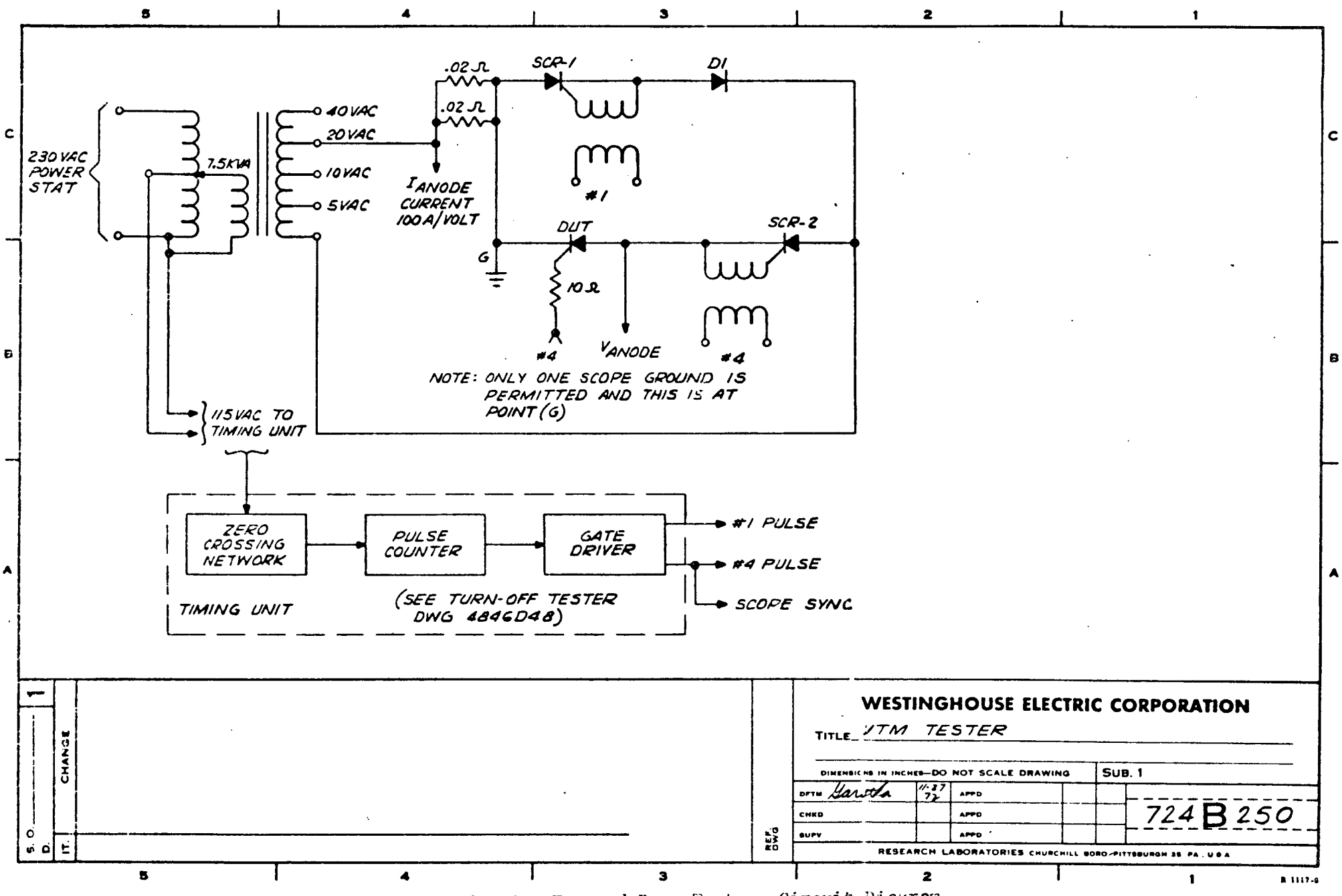
3.1.4 Latching and Holding Current Characteristics (Cont.)

of the meter circuit is 100 ma and 1.250 volts full scale; different ammeter ranges are secured by changing the gain of the amplifier to suit the range. A satisfactory procedure is to start a holding or latching current measurement on the 20 ampere range, and then decrease the range until the current measurement is made on the smallest possible thus achieving the highest accuracy.

3.1.5 Conducting Forward Voltage Drop Characteristic

The circuit diagram for the conducting forward voltage drop (V_{TM}) tester is given in Figure 15. Conducting forward voltage drop is measured with a device current of a 60 Hz half sine-wave of low duty cycle. The 60 h_z half-sine wave provides a long turn-on time which conforms to the classical technique for measuring conducting drop. The length of the pulse allows complete turn-on of the wafer to its most lateral extremes, and hence should be easily reproducilbe. The low duty cycle of the pulse is selected to provide a test result which is as independent of thermal impedance or cooling as possible. A device under test (DUT) such as shown in Figure 15 which conducts on every pulse would rise in temperature and produce a conducting drop measurement as a function of temperature of the particular cooling system selected for the test. The test system shown only triggers the test device on every eightieth pulse, or some even multiple thereof. This technique keeps self-heating to a minimum so that it may be ignored. During the time the half-sine wave of current is applied to the test device, junction temperature is known to follow the current excursion. The reading of V_{TM} is taken at the peak of the half-sine wave, and all comparative readings should be under the same conditions. Readings of forward voltage drop for short rectangular current pulses or phase controlled half-sine waves with peaks equal to full half-sine waves will, in general, read higher by some small increment.

The test current pulse is generated by using the device under test in a low voltage-high current rectifier system. Both forward and reverse direction current pulses are produced in order to provide load balance to the 7.5 KVA isolation-transformer as well as the input power system. Although not used here, a balanced load pulse also provides opposing reset flux for current sensors such as toroidal current transformers. In Figure 15, the forward load current pulse flows through SCR-1 and D-1, while a reverse half cycle pulse flows through DUT and SCR-2. DUT only conducts a reverse half-sine wave of conduction. Thyristor SCR-2 is used to provide current switching if DUT is a rectifier; thyristor SCR-1 controls the presence of forward current, and rectifier D-1 provides a balancing forward voltage drop. The two control SCR's are rated 200 amperes RMS, with single cycle surge ratings of 3300 amperes. In conjunction with the front end variac rated at 7.5 KVA, a current of



Conducting Forward Drop Tester, Circuit Diagram

Figure 15

3.1.5 Conducting Forward Voltage Drop Characteristics (Cont.)

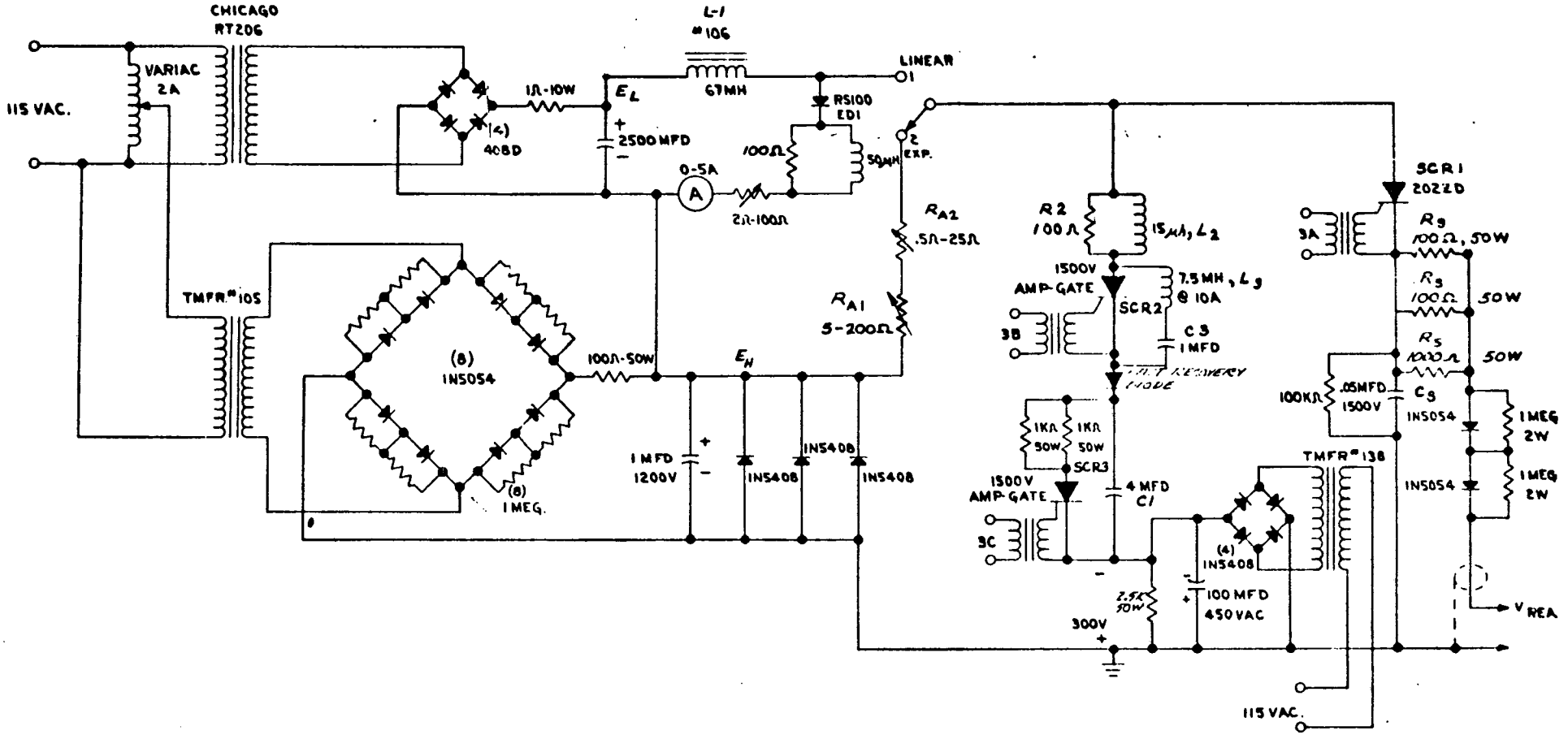
1000 to 1500 ampere may be sustained by the DUT with this test system. The control SCR's then operate at one-half their single cycle surge rating; this is a tolerable operating point which could be sustained indefinitely. Higher test currents would require higher rated control SCR's. The only current limiting resistance in the V_{TM} tester are two .02 ohm, 250 watt resistors connected in parallel. The high wattage is selected to tolerate the high peak dissipation present during the load test pulse without affecting the value of the resistor, also used as the current measuring shunt. The most important condition which must be met in the V_{TM} measurement system is that the measuring device only connects to the shunt resistance common point at a single point. If an oscilloscope is used as the measuring device, in normal mode or X-Y mode, it should only connect to the common point (G) of the shunt resistor at a single point. Scopes are frequently double grounded by an inadvertant power line ground, resulting in an erroneous reading.

3.1.6 Transient Susceptability Characteristics

The circuit diagram for the dv/dt tester is given in Figure 16.

Thyristors exhibit sensitivity to changing wavefronts of voltage. The standard test conceived to measure this sensitivity is a non-destructive dv/dt test whereby a change in voltage from zero to 80% of rated forward blocking voltage is applied to a device and a test conducted to see if the transient will cause the device to turn-on. If turn-on occurs, it should not cause destruction, although limits to "non-destructability" do exist. The voltage transient range of interest varies from 5 volts per microsecond to 1000 volts per microsecond and the useful functional transients are either linear or exponential. The standard definition of exponential dv/dt is to divide 63% of the exponential transient excursion by the time taken to reach that value.

The circuitry of Figure 16 generates both linear and exponential transients. The exponential range is one volt per microsecond to 800 volts per microsecond. The linear range is one volt per microsecond to 50 volts per microsecond. The exponential pulse is generated as follows. Incoming 60 Hz power is stepped up by transformer TMFR #105 and full wave rectified, developing an output dc voltage of 0-1000 volts across a one microforad, 1200 volt filter capacitor. This output supply voltage is applied through two carbon pile resistors to the anode of SCR-1. When SCR-1 is triggered by pulse 3A, capacitor C_S is charged exponentially through the mentioned carbon pile resistors. The size of C_S may be changed to generate slower transients as desired.



dv/dt Tester, Circuit Diagram

Figure 16

1	CHANGE	WESTINGHOUSE ELECTRIC CORPORATION	
0		TITLE DV/DT TESTOR	
		DIMENSIONS IN INCHES DO NOT SCALE DRAWING	SUB 1
		DRFR R.C.CRAMER 6 14 71 APPD J BREWSTER 6 15 71	254C791

3.1.6 Transient Susceptability Characteristics (Cont.)

To maintain a nondestructive character to the tester, C_S should be as small as possible. At times, devices connected across C_S show conductive tendencies such that the set dv/dt rate is altered by the device. To avoid this, C_S should be increased in size. To maintain the same charging rate i/C_S, the charging current i must also be increased, thus minimizing tendencies of leaky devices to change the preset dv/dt. Higher charging currents, however, can cause some devices to destructively fail.

The charging capacitor is never connected directly across the test device. Connection to the anode of the test device is made through an isolation resistance R_S, as well as several isolation diodes in series. The output voltage is labeled V_{REA}, a term originating from the use of the transient dv/dt signal as reapplied voltage signal used in a turn-off time measurement. For standard tests, resistor R_S should be 1000 ohms; but for GATT turn-off time testing, R_S should be reduced to about 50 ohms.

A simple dv/dt test circuit with only the components described would have one flaw. If a device under test turned-on while C_S was being charged through SCR-1, then SCR-1 would latch-up or remain on by current supplied from the high voltage power supply. The latch-up of SCR-1 is prevented by forcing the anode of SCR-1 negative when SCR-2 is turned-on by pulse 3B, 500 microseconds after SCR-1 is pulsed.

The anode of SCR-1 is forced negative by connection through SCR-2 and C_1 to a minus 300 volt power supply. Inductance L_2 slows the commutation rate, and R_2 swamps transients caused by L_2. Thyristor SCR-2 is turned off by the ringing of L_3 and C_3 in a self-commutation scheme. Thereafter SCR-3 is fired 500 microseconds after SCR-2 and causes discharge of C_1. Use of this circuitry allows a short circuit to be placed across the output, with subsequent recovery of the generated waveform when the short is removed. This test may be performed with the high value carbon pile resistor shorted and the low value carbon pile current limiter set to 0.5 ohm.

Linear dv/dt is obtained by switching the linear-exponential switch to linear. In this mode a predetermined constant current flows from a low voltage floating supply through L_1, RS 100 diode, current determining resistor, ammeter and back to supply. When SCR-1 is now triggered, diode RS 100 is back biased by the full high voltage supply and the current through RS 100 is instead forced to flow from the high voltage supply, through the low voltage supply through L_1, SCR-1, C_S and back to the high voltage supply. Capacitor C_S then charges at the constant rate of I_O/C_S. When C_S reaches near the level of the high voltage output, the charging current will transfer back through RS 100 and charging will cease. The initial commutation of RS 100 is important. Other rectifiers are now available with better reverse recovery characteristics which allow higher charging currents and higher linear voltage rates of rise.

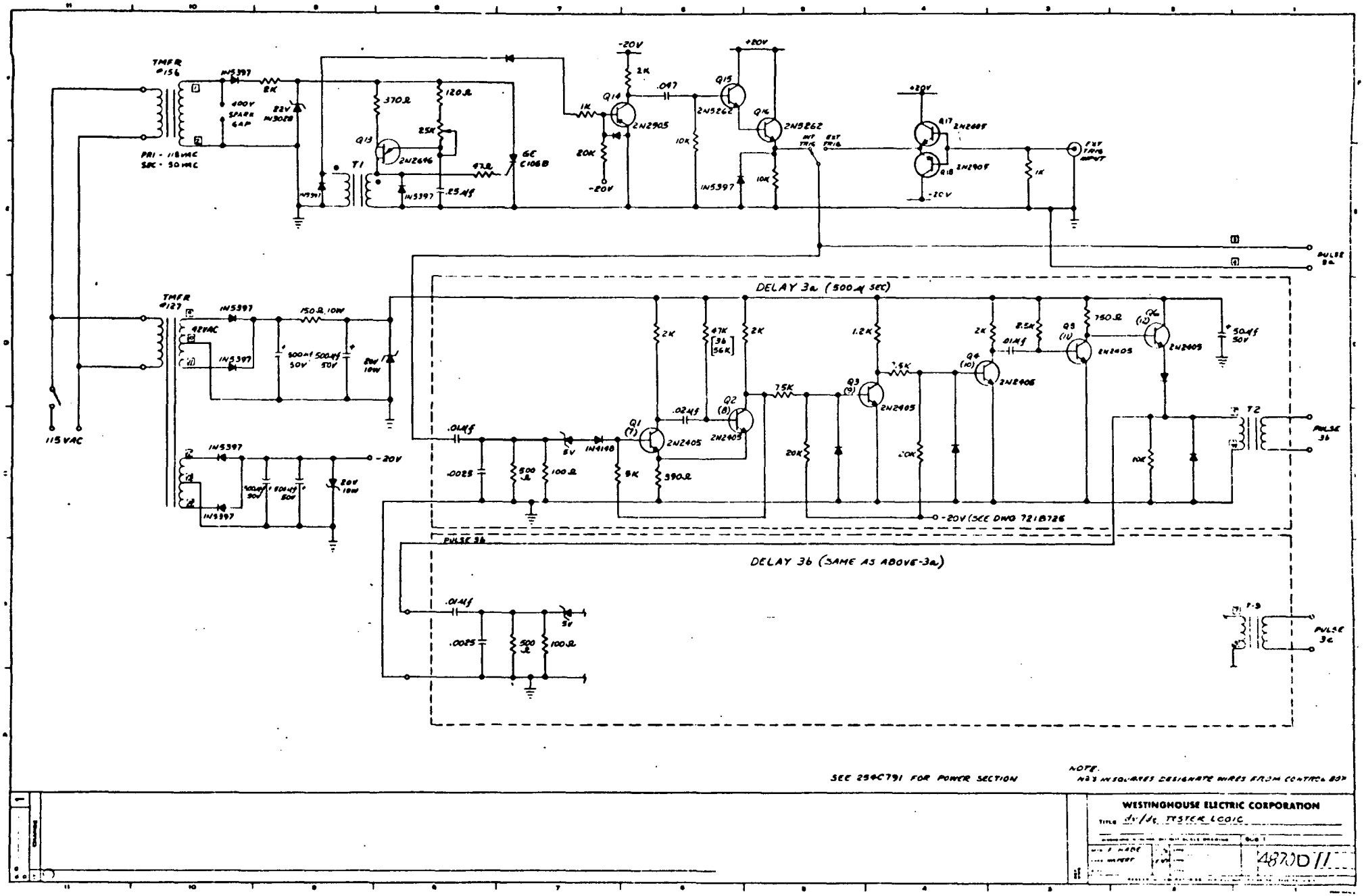
3.1.6 Transient Susceptability Characteristics (Cont.)

Timing for the dv/dt tester is shown in the circuit of Figure 17, dv/dt Tester Logic. The system includes an internal oscillator and provisions for external triggering. The generation of the three timing pulse 3A, 3B, and 3C is straightforward and needs no further explanation.

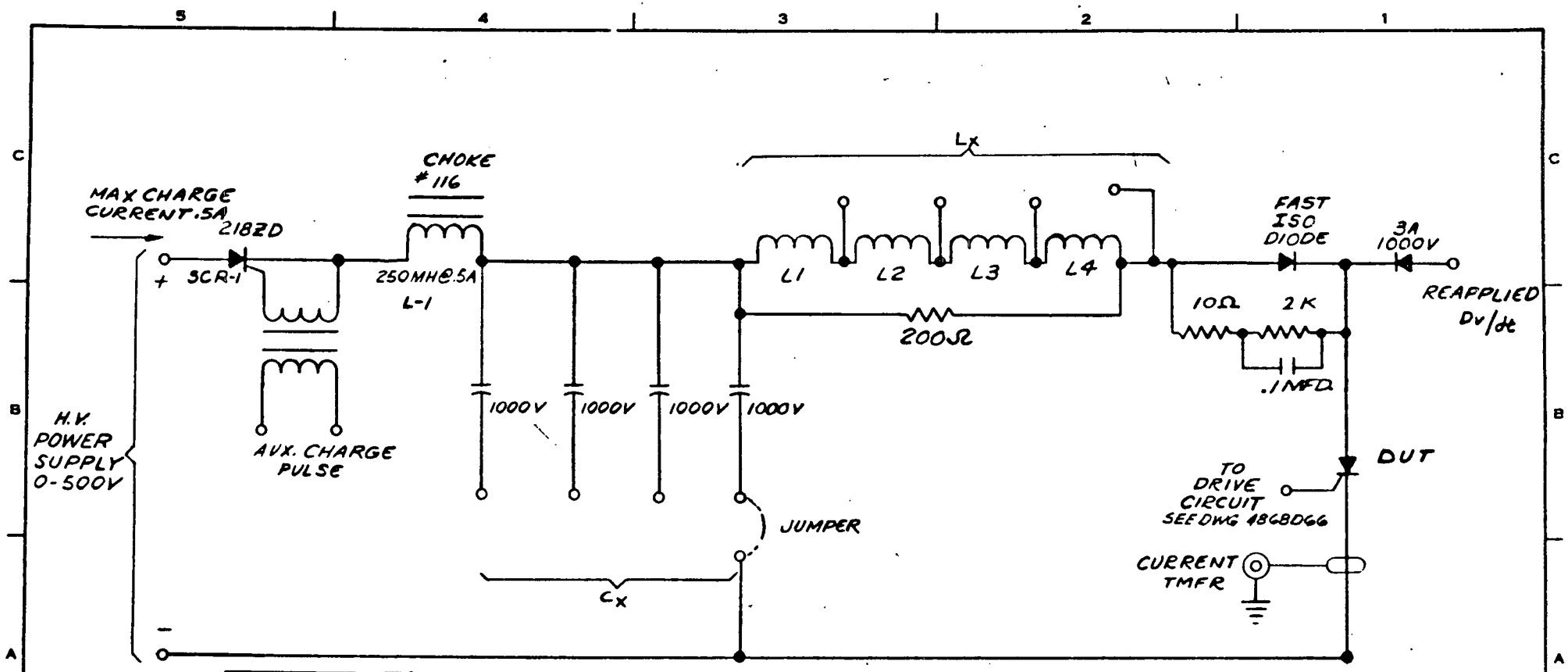
3.2 Turn-On Test Circuits

The initial thinking at the beginning of the subject GATT II contract envisioned (and ultimately resulted in) the turn-on test circuit shown in Figure 18. The intent of the test circuit was to generate four test pulses of 100 ampere peak amplitude, but with different rates of rise. The current rates of rise available are 35, 50, 75, and 100 amperes per microsecond. The pulses are generated as follows. An external power supply is connected to the circuit and used to charge capacitor C_X through SCR-1 and resonant charging choke L-1 to twice the input supply. Thereafter, the device under test is triggered, and C_X discharges through inductor L_X, which may be preselected to generate the 100 ampere peak pulse with di/dt and pulse width as shown in Figure 18. By calculation and test with a proven switch, the circuit is determined to provide the indicated response. A GATT test device is then inserted in the place of the proven switch and tests are made to determine if the known circuit response can be obtained with the chosen test device. If it is observed that for a particular selection of L_X and C_X that the predetermined response does not occur, then it may be said that the switching speed of the test device is insufficient to produce the indicated response. Under these conditions it may be said that "device limiting" occurs. In this case, current response is determined by the test device rather than the circuit. If the current response is reproduced faithfully, it may be said that the device switching speed is sufficient to pass the circuit determined current. Circuit di/dt may then be increased by change of C_X and L_X and another switching speed analysis made. Ultimately a di/dt and peak current will be reached which cannot be passed by the switch, and the di/dt switching speed range of the switch will be known. To produce the current responses of the circuit in Figure 18, anode voltage of the DUT is set to 600 volts, or the input supply is adjusted to 300 volts.

A second technique exists for checking turn-on with a slightly different perspective than the current response reproduction technique. The second technique also uses the components of the Figure 18 circuit with substitution of some items. Capacitor C_X is replaced by a pulse forming network, (PFN), made up of 10 capacitors of 0.5 microforad each, plus some small inductors. The characteristic impedence (Z_0) of the PFN is one ohm and the generated pulse has a width of 10 microseconds. As a load, L_X is replaced by a one ohm non-inductive resistor which matches Z_0 of the PFN. With this system, the following circuit determined characteristic responses may be obtained:



dv/dt Tester Logic, Circuit Diagram
Figure 17



PW	Cx	Lx	Ip	di/dt
10 USEC.	.58 MFD	20 uA	100 A	35 A/USEC
6.25 USEC	.35 MFD	12 uA	100 A.	50 A/USEC
4.2 USEC	.23 MFD	8 uA	100 A	75 A/USEC
3.2 USEC	.18 MFD	6 uA	100 A.	100 A/USEC

S.O. 1 CHANGE IT.

REF DWG

Westinghouse Electric Corporation

TITLE GATT II TEST CIRCUIT
1) di/dt 2) GATE ASSIST

DIMENSIONS IN INCHES—SCALE ~

DFTM F. HABE	11/14/74	APPD	723B485
CHKD HALPERT	11/15/74	APPD	
SUPV		APPD	

RESEARCH LABORATORIES CHURCHILL BORO. PITTSBURGH PA 15235 U.S.A.

GATT II di/dt and Gate Assist Tester, Circuit Diagram
Figure 1

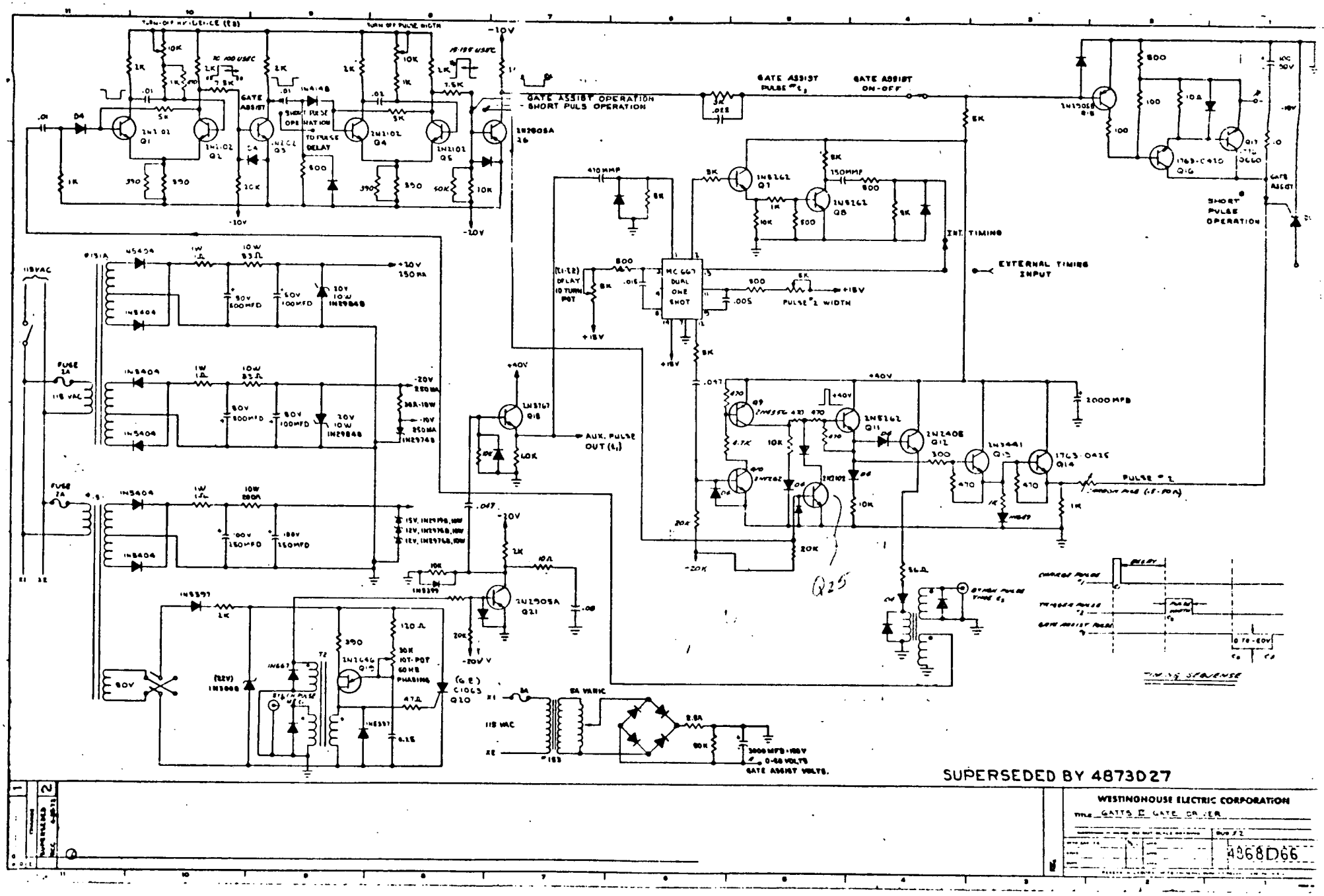
Pulse Forming Network Responses

	Input Supply (volts)	DUT Switching Voltage (volts)	Circuit di/dt (amps/ microsec.)	Pulse Amplitude (amps)	Pulse Width (microsec.)
1.	100	200	200	100	10
2.	200	400	400	200	10
3.	300	600	600	300	10

Response number one was chosen for application to the GATT since it fell within the range of device performance. The test technique is to subject the test device to a known circuit response in excess of device capability, and measure the let through di/dt. For response one, the known response is 200 amperes per microsecond to one-hundred amperes peak. The resultant switching speed of the GATT device for a variety of ranges of gate drive allowed di/dt's of 30 to 150 amperes per microsecond, speed increasing with increasing amplitude of gate signal. It is concluded from the let-through di/dt test that if a switch produces a given di/dt less than a circuit di/dt with a given drive, then it will switch all circuit di/dt's up to and equaling the let-through value. At a later point in this report, let-through di/dt is plotted as a function of gate drive.

The second function of the tester described in Figure 18 was to generate the current pulse close to the type of pulse actually to be used by the device, and then measure turn-off time using this load current pulse. As may be seen from the drawing, terminals are available to add a standard re-applied voltage pulse for turn-off time measurements (See Figure 16, dv/dt Tester). Two items are added to the GATT II test circuit of Figure 18 to facilitate turn-off time tests. An isolation diode is placed between the re-applied voltage source and the anode of the device under test, and a fast isolation diode is placed between the load current power source and the anode of the device under test. The purpose of each diode is to isolate the load current source from the re-applied dv/dt source and vice-versa. Thus the load current source is high-current, and the re-applied voltage source is low current; each should not influence the other. During generation of the forward current pulse, a natural reverse voltage causes the DUT and the fast isolation diode to conduct reverse current. By its very character, the fast diode determines the duration of reverse current which is small and flows through L_X. At the instant of reverse current recovery, a trapped current exists in L_X which causes a high voltage spike to occur across the fast diode. A suppressor is placed across the fast diode to suppress the recovery spike; the suppressor now destroys the isolation character of the fast diode. Since completion of the test work associated with this contract, fast isolation diodes have been obtained with very superior reverse recovery characteristics which could near eliminate the troublesome reverse recovery voltage transients. However for this contract, a second means of turn-off time testing was available and used. The circuit just described was used almost exclusively for turn-on time testing, and that almost exclusively with the PFN - one ohm load resistor circuit.

A logic-gate drive circuit was built to drive the power circuit just described. The GATTS II tester, gate driver circuit, is given in Figure 19. The essentials of the logic are shown on the timing sequence diagram. An internal oscillator generates a starting-charge pulse at time t_1. The charge pulse triggers SCR-1 of the power circuit causing charge of C_X or a PFN, whichever is used. After a suitable delay the device under test is triggered by a pulse generated at time t_2. At time t_3, which is adjusted to occur at load current zero after conduction, a gate assist pulse is generated which terminates at time t_4. The timing for the system begins with line synchronized oscillator Q_{19} and Q_{20}. The output pulse is amplified by Q_{21} and Q_{18}. The charge pulse for SCR-1 of the power circuit is available at the emitter of Q_{18}, at time t_1. This pulse feeds dual one shot MC 667, the first half of which determines the pulse width of the output pulse at time t_2. The one shot output drives Q_{10} and Q_9, turning on each. The drive pulse for the GATT, with 35 volt amplitude and pulse width determined by Pulse #2 width, appears on the base of Q_{11}. Transistor Q_{11} is an emitter follower, which drives darlington connected emitter followers Q_{13} and Q_{14}. The thirty-five volt pulse at the emitter of Q_{14} drives the gate of DUT through an adjustable carbon pile resistor which can be used to adjust the peak gate current from several hundred milliamperes to 20 amperes. The pulse from Q_{11} also drives Q_{12} and an isolation pulse transformer in its emitter. The isolation transformer output provides a sync pulse at time t_2, as well as a source trigger feeding transistor Q_1 and Q_2. These form a one-shot delay which determines the time interval between time t_2 and t_3. The delay is adjustable with the turn-off incidence control. The signal from Q_2 is processed by transistor Q_3, and the lagging edge (t_3) triggers one-shot Q_4 and Q_5. These two transistors determine the duration of the gate assist pulse, which is adjusted by the turn-off pulse width control. The pulse at the collector of Q_5 is inverted by Q_6 and is used to drive Q_{15} through the Gate-Assist On-Off switch. During the gate assist interval, Q_{15} turns on, then turning on darlington connected Q_{16} and Q_{17}. The voltage at point A, the emitter of Q_{17}, is an adjustable, filtered dc voltage of 0-50 volts which is variac controlled. When transistor Q_{17} is turned-on at time t_3, the gate assist voltage is directly applied to the gate of the DUT at the desired present level. The mode of operation of the gate drive just described is that necessary for gate assisted testing. As has been previously explained, it was found necessary to test gate-assisted turn-off time with a second test system and the gate driven-power circuit combination was instead modified for evaluation of device turn-on performance. Turn-on performance required a PFN and one-ohm resistive diode used with the power circuit, and only the turn-on drive pulse of the GATTS II gate driver. Although the voltage rise time of the gate-drive pulse was only 50-100 nanoseconds, the distance of the test device from the gate driver was several feet, such that gate current rise times of much as several microseconds were possible. To overcome the effects of connecting line inductance, a set of emitter follower transistors were built and operated in close proximity to the test device. In effect, output transistors Q_{13} and Q_{14} were duplicated at the gate of the DUT.



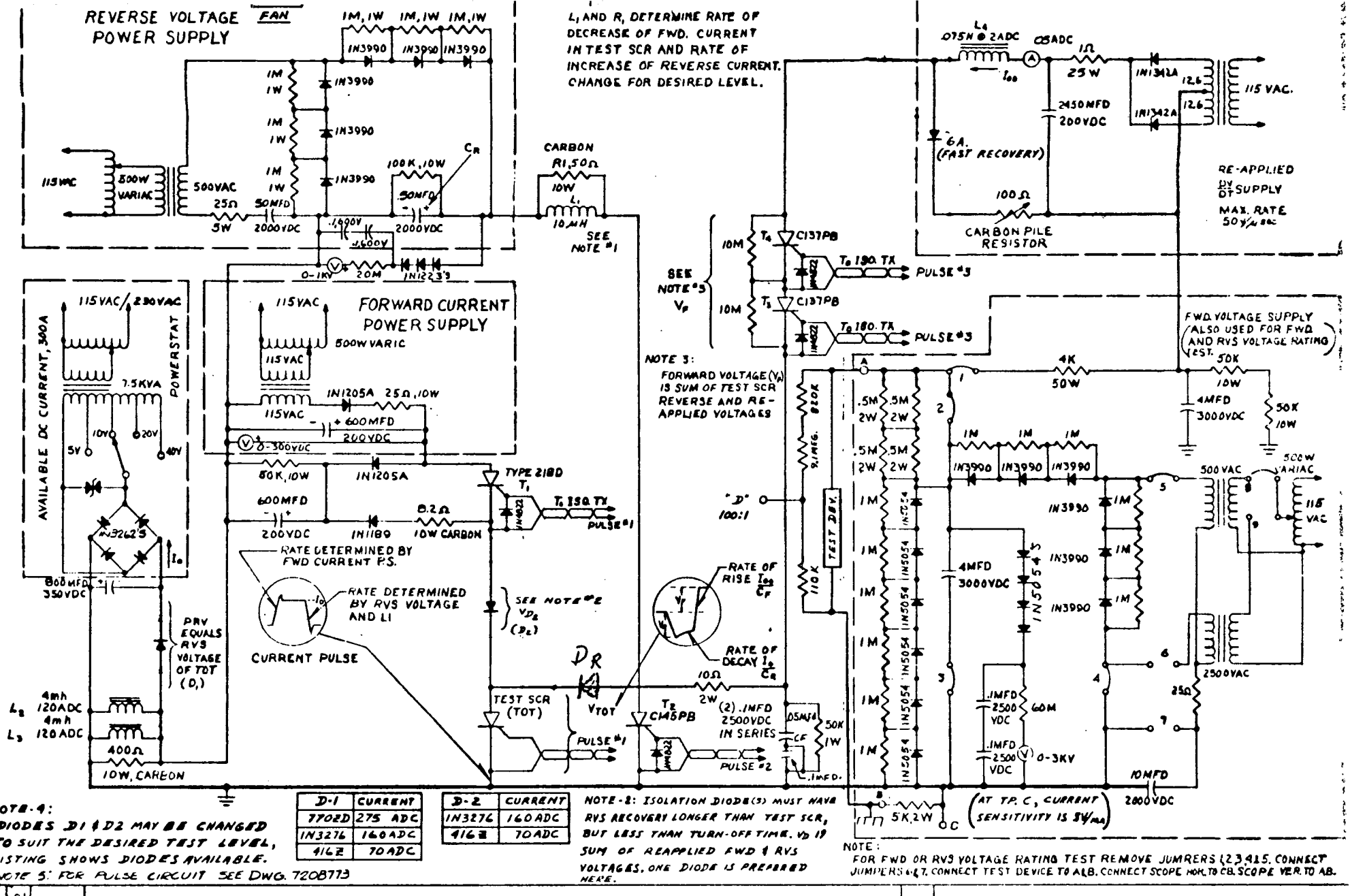
GATT II Tester, Gate Driver Circuit Diagram
Figure 19

This included a several thousand microforad power supply bypass capacitor. The new gate rise time with local pulse amplifiers was no more than 150 nanoseconds for a 30 ampere pulse. (A 30 ampere output pulse was possible by changing the local equivalent of Q_{14} from a 25 ampere peak current transistor to a 60 ampere transistor, Westinghouse 1776-0660). While the local pulse current amplifier gave good rise time, the pulse width control furnished by one-half of MC 667 could not yield pulse widths of only several microseconds. This was primarily due to the turn-off time of the switch transistors Q_9, Q_{10}, and Q_{11}. Even though the input drive pulse to these transistors could be made only several microseconds, the termination of the input drive did not result in the turn-off of Q_9 and Q_{10}. As a result, it was necessary to terminate the turn-on pulse by brute force crowbar of base circuit of Q_{11} at the appropriate instant. The appropriate pulse to turn-on the crowbar transistor Q_{25} should occur as early in the timing as possible, but not as early as time t_1. The earliest possible pulse with which to switch the crowbar must originate at pulse time t_2 and this pulse is found at the input to the one-shot used to form the DUT trigger pulse. The pulse here, pin 13 of MC 667, may originate internally from Q_8, or may be provided by an external generator. The pulse is sent to a delay circuit which provides a several microsecond delay. The delay is external to the gate-driver and has not been shown. The delayed t_2 pulse is fed back into one-shot Q_4 and Q_5 with the input switch in the short pulse operation position. The output of the one-shot, with the output switch in the short pulse position, is used to drive the base of pulse crowbar Q_{25}. A resume of this sequence is as follows: the output pulse is delayed, formed into a gate, and then used to terminate its own duration by turning on crowbar Q_{25}.

The final turn-on pulse, available at the emitter of the local amplifier, has good rise time and pulse width in the 1.5 - 5.0 microsecond range. An adjustable carbon pile is no longer used to vary gate drive current, but instead non-inductive resistors are used. Small capacitors, across their current limiter resistors, are necessary to speed up the leading edge of the current drive.

3.3 Turn-Off Test Circuits

GATT turn-off time testing was performed with the system given by the circuit diagram of Figure 20. This tester simulates test conditions and measures turn-off time in a non-destructive manner. The test system always operates at a low duty cycle such as 3 pulses per second. The focal point of the system is a dc current established in inductors L_2 and L_3 by a low voltage power supply originating from a large variac, step down transformer, and full wave rectifier. The current established in the inductors also flows through D-1. Two other floating supplies exist in the circuit and they are the low voltage forward current power supply, and a relatively high reverse voltage supply. Three current paths exist, one of which has already been pointed out:



D-1	CURRENT
7702D	275 ADC
IN3276	160 ADC
4162	70 ADC

D-2	CURRENT
IN3276	160 ADC
4162	70 ADC

NOTE-4: DIODES D1 & D2 MAY BE CHANGED TO SUIT THE DESIRED TEST LEVEL, LISTING SHOWS DIODES AVAILABLE.
NOTE 5: FOR PULSE CIRCUIT SEE DWG. 7208773

NOTE-2: ISOLATION DIODE(S) MUST HAVE RVS RECOVERY LONGER THAN TEST SCR, BUT LESS THAN TURN-OFF TIME. VD IS SUM OF REAPPLIED FWD & RVS VOLTAGES, ONE DIODE IS PREFERRED HERE.

NOTE: FOR FWD OR RVS VOLTAGE RATING TEST REMOVE JUMPERS (2) 3, 4, 5. CONNECT JUMPERS 6 & 7. CONNECT TEST DEVICE TO A & B. CONNECT SCOPE HOR. TO C & SCOPE VER. TO A & B.

CHANGE	
1	CAT REVISED AS PER MARKED PRINT.
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GATT Turn-Off Time Tester Circuit Diagram
Figure 20

WESTINGHOUSE ELECTRIC CORPORATION
TITLE TURN-OFF TIME TESTER
DIMENSIONS IN INCHES DO NOT SCALE DRAWING
SUB # 2
182C286

the variac controlled dc supply, L_2 and L_3, D_1 and back to supply. The second current path consists of current through L_2 and L_3, the forward current power supply, thyristor T_1, isolation diode D_2, thyristor under test TOT, and back to L_2 and L_3. The third current path consists of current through L_2 and L_3, the reverse voltage power supply, thyristor T_2 and back to L_2 and L_3. To establish a current pulse through test thyristor TOT, the current commutes from the first path, to the second, and the second to the third in the order given, and finally back to path one. The current through the test device is established as follows. The desired test current is circulated in L_2 and L_3, and D-1. With a line synchronized pulse but at low pulse rate, thyristor T_1 and TOT are simultaneously triggered. This causes the forward current supply voltage minus the high current supply voltage to appear across D-1. Since the forward current supply is longer, D-1 will be back biased. The current through L_2 and L_3 continues to flow, through the forward current supply, T_1, D_2, and TOT. If allowed to continue in this fashion without further action, this current in the TOT thyristor loop would flow until the filter capacitance at the output of the forward current supply were discharged. When this voltage falls below that of the high current supply, the current in TOT would harmlessly commutate both to the D-1 loop. Before this can happen, thyristor T_2 is triggered, forcing the current of L_2 and L_3 to loop 3. The difference voltage of the reverse voltage power supply and the remaining voltage of the forward current supply appears across D_2 in series with TOT, effectively back biasing these devices. Under these conditions, current must transfer to loop 3. The rate of transfer is directly related to the magnitude of the reverse voltage power supply and the size of inductor L-1. The constant current of L_2 and L_3 now discharges the filter capacitor in the output of the reverse voltage power supply. When this voltage reaches the magnitude of the high current power supply output, current will begin to transfer from loop three back to loop one and the initial starting condition. The net result is the generation of a trapezoidal load current pulse through thyristor TOT. The front end or rising edge of this pulse is determined by the magnitude of the forward current power supply and distributed wiring inductance. Practically, front end load current pulse rate-of-rises of no more than 50 amperes per microsecond were achieved, and higher rates of rise put undue stress on the reverse current sweep out interval of D-1. Although the magnitude of the forward current supply may be used to have direct control of the linear rate of rise of the load current pulse, it should not be attempted to generate on excessive rate of rise on the front end of the pulse since failure of D-1 will be imminent. This control function finds excellent usage for testing latching effects at 1-10 amperes per microsecond rise, but should not be considered useful for a switching speed test since useful front end rate of rise is limited. The magnitude of the load current pulse is continuously adjustable over the full range of the high current power supply. It is always assumed that for a selected load current pulse width and amplitude, the forward current supply is always of sufficient

magnitude to maintain the constant current level of the load current pulse until commutation to loop 3. The indication of insufficient forward supply voltage will be a definite drop or trailing off of the normally flat load pulse as pulse amplitude or pulse width is increased. This indicates that current is beginning to self-commutate from loop 2 back to loop 1 before the forced transfer from loop 2 to loop 3. When this occurs, a simple elevation of the forward current power supply will eliminate the drop.

The duration of the load current pulse is determined by the triggering incidence of thyristor T_2. As has been mentioned, the decay rate of the load pulse is continuously variable with the reverse voltage power supply, and in discrete steps with the size of L-1. The load current pulse decay rate is important and should always be specified for a turn-off measurement. As an example of the rates of decay available with the system of Figure 20, a rate of decay of 100 amperes per microsecond with reverse voltage of 600 volts and L-1 equal to zero is easily obtainable.

The trapezoidal load current pulse flows in the loop of L_2 and L_3, forward current power supply, thyristor T-1, isolation diode D-2, and test device TOT. Thyristor T-1 is present such that if the test device is a rectifier or a short circuit, the load pulse will still be maintained. Isolation diode D-3 isolates the forward high current load pulse from the re-applied dv/dt source. Isolation diode D-R isolates the re-applied dv/dt source from the forward current power source. The requirements of isolation diode D-2 are strict; diode D-2 should recover reverse blocking capability after the test device recovers, but before the occurrence of the minimum turn-off time which is to be measured. These requirements are easily met for turn-off time measurements in the 15 microsecond and greater range, but become progressively more critical as turn-off time is shortened. For turn-off times in the range of 5 to 15 microseconds, it is sufficient to match the reverse recovery characteristics of the test device to the isolation diode. This means that for identical load current conditions, and current rate of decay, the reverse current recovery characteristics of isolation diode and test device should be as near identical as possible. For turn-off times greater than 15 microseconds, the reverse recovery current of the test device will not be influenced by the reverse current of the test device, since the isolation diode is selected to recover after the test device. Reverse current of the test device will have great influence on turn-off time but for the greater than 15 microsecond device no alteration of the measurement should be expected. For turn-off times between 5 and 15 microseconds, with the recovery of the isolation diode and test device selected as near a match as possible, the reverse current of the test device should only be slightly affected by the isolation diode, and turn-off time measurement should still be good. For times under 5 microseconds, the only possible technique will be to select the isolation diode with ultra-short recovery times such that the reverse current of

the test device is highly altered, or near eliminated. A non-destructive turn-off time measurement may still be made, with the down-grading effect of turn-off time being lengthened because of the drastic effect of eliminating test device reverse sweep-out current. Nevertheless a measurement may be made and then a conclusion drawn that for a conventional device, turn-off time would actually be better if full device reverse current were present. With the GATT device, the under five microsecond measurement can be made, even within the limits of the test spec, and without the aiding benefit of most of device normal sweep out current. Hence non-destructive measurements of turn-off time may be made under five microseconds which show turn-off times of only several microseconds duration. GATT test results of this character require some adjustment before applications. The problem is restated as follows: because of semiconductor limitations and to achieve non-destructive testing, an isolation diode is used in the forward current loop serially with the device under test. To test turn-off times of several microseconds, the isolation diode, which blocks or isolates the re-applied voltage from the high current forward loop, must recover within 500 nanoseconds. As a consequence, the normal reverse current flow experienced by a test device is over-ridden by the necessary fast recovery characteristics of the isolation diode. Nevertheless, the turn-off measurement can be made, and GATT devices can be shown to recover within the contractual 2 microsecond period under these conditions. This turn-off time is measured from the moment forward current, in process of decreasing, passes through zero.

Under actual conditions, GATT devices exhibit reverse current recovery times of at least 1.5 microseconds, after which reapplied forward voltage may be applied. Reapplied forward voltage may not be applied during the reverse current recovery interval; hence an actual turn-off time measurement must include the time for reverse junction blocking recovery, as well as the time for forward blocking junction recovery. A turn-off time measurement under these actual conditions would then be the sum of the 1.5 microsecond reverse recovery time, plus the normal forward junction recovery time which was measured as less than 2 microseconds for all devices when measured without the benefit of reverse current. With reverse current, it may be safely assumed that the forward junction recovery time is reduced from 2 microseconds to half this value. Hence, the true usable recovery time is the sum of 1.5 microseconds reverse recovery plus an assumed 1.0 microsecond forward recovery yielding an actual time of 2.5 microseconds.

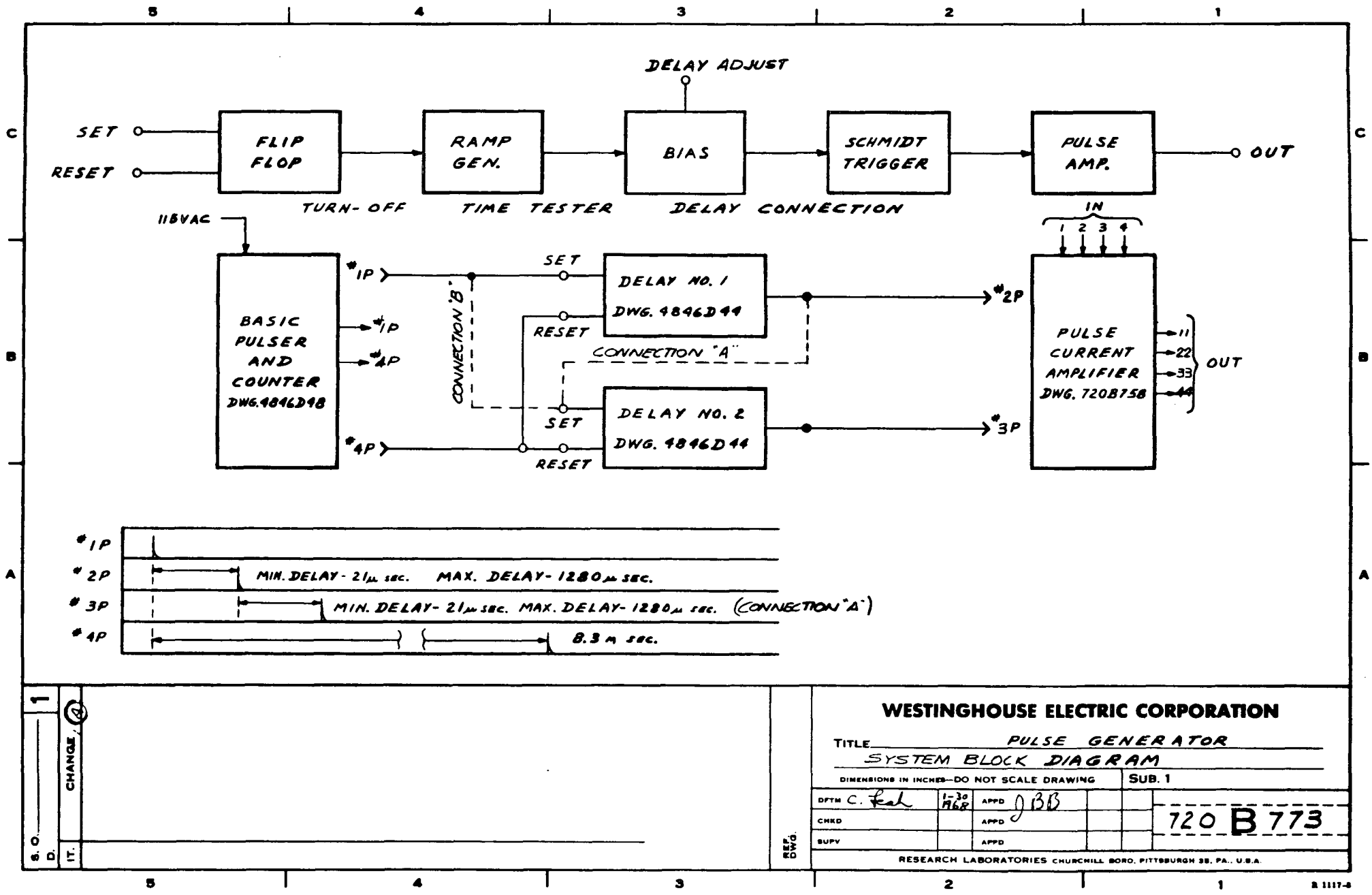
Other peculiarities of the serial combination of isolation diode D2 and test device TOT exists. These do not alter test results but should be mentioned. When two devices are connected in series, the tendency is to share voltage according to leakage level, except immediately following conduction. Just after conduction, two devices in series will share voltage dependent upon which device achieves blocking junction recovery first. Voltage will not distribute according to leakage until all charge in each device

achieves equilibrium condition. Hence a fast device in series with a slow device will see the fast recovery device assumes all the reverse blocking voltage, while the slow recovery device will assume none until the charges in the slow device are annihilated by the slow process of recombination rather than the fast process of current sweep out. These factors are noticeable under the unusual conditions required for not only ultra-fast non-destructive turn-off time testing but the complete range of non-destructive testing as well.

The reapplied voltage source of Figure 20 connected to the anode of the test thyristor (TOT) through D_R did not achieve the 400 volt per microsecond required of the GATTS contract. In its stead, the dv/dt generator of Figure 16 is used to generate the 600 volt, 400 volt per microsecond reapplied signal. The generator of Figure 16 has already been covered under Section 3.1.6. The dv/dt generator shown in Figure 20 is of a similar type to the linear ramp generator portion of Figure 16. In the turn-off time tester a floating current is established in a choke L4 and rectifier D3. When T_4 and T_3 are turned on, rectifier D3 is commutated and the current through L4 changes C_F at the rate of I_{00}/C_F. The maximum linear ramp rate available is but 50 volts per microsecond. In this circuit thyristors T_3 and T_4 are not protected against latch up when the test device turns on by application of reapplied voltage in an interval less than rated turn-off time of the device under test. Because of the latch up problem and also the insufficient range problem the more advanced dv/dt generator is used for turn-off time testing. The high voltage power supply feeding the unused ramp generator has a double usage. The normal output of the supply is simple voltage doubling of a 500 volt source voltage. By changing connection through jumpers, the doubler rectifiers may be connected in series to rectify the output of a 2500 volt ac transformer, generating a test potential which is useful for blocking voltage measurements to 3000 volts dc.

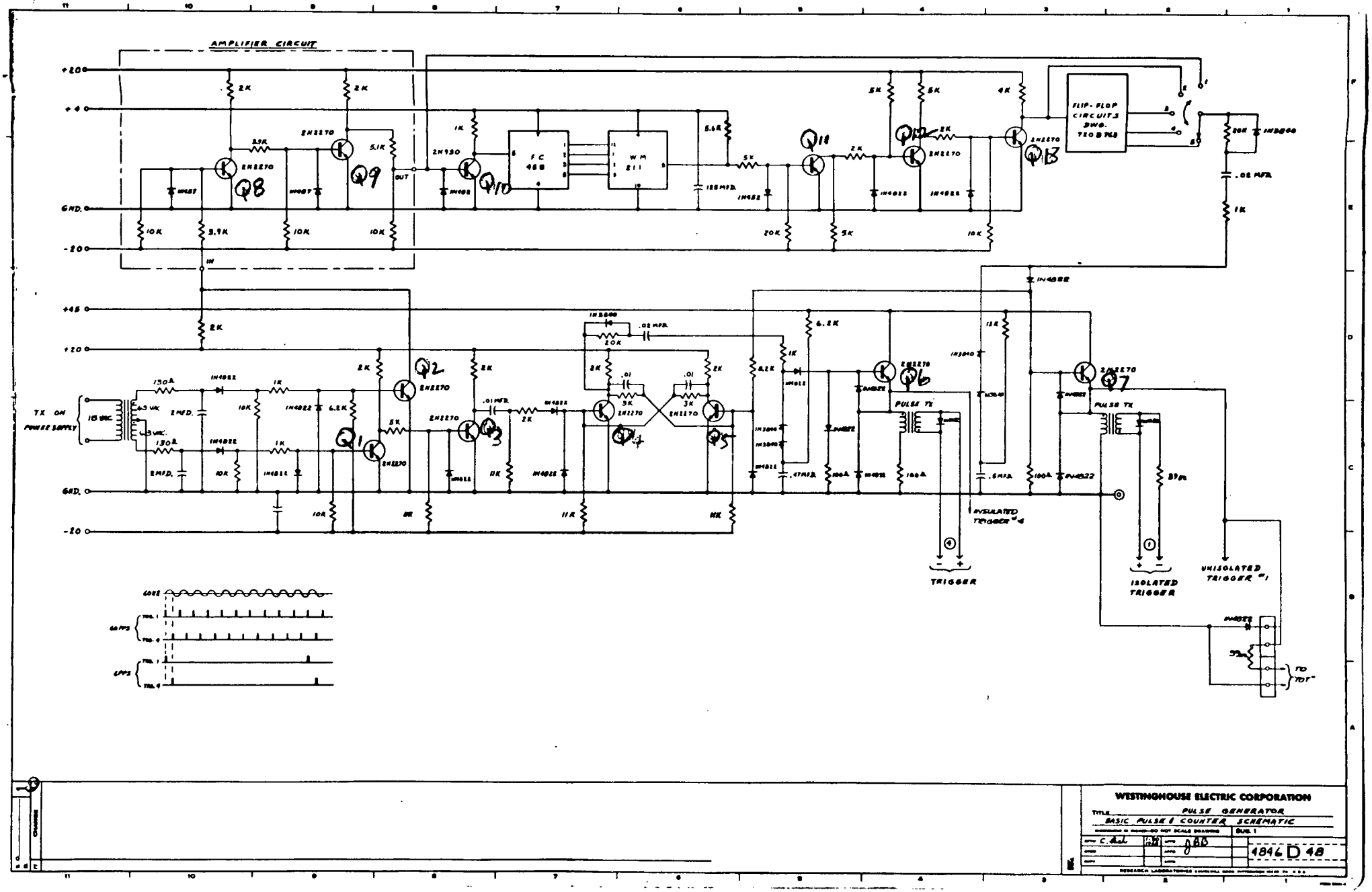
3.3.1 Turn-off Tester Logic

The logic system used to supply the gate firing pulses for the turn-off time tester are shown in block diagram form in Figure 21. Through conventional zero crossing detectors and associated circuitry, two pulses are developed at each crossing of a 60 Hz wave, and these are labeled pulse #1 and pulse #4. The details of this pulse formation are given in Figure 22. Line voltage is stepped down to 6.3 Vdc and then filtered to eliminate sharp line disturbances. Each line voltage half cycle drives two successive voltage squaring stages, Q1-Q3 and Q2-Q8. The signal from Q8 is twice inverted by Q9 and Q10, at the same time being reduced to a four volt excursion. These four volts are compatible with a scale of ten IC counters, consisting of Fairchild 488 counter and Westinghouse 211 and gate. The output of the counter achieves proper sense and is returned to the 20 volt level in stages Q11, Q12, and Q13. This signal is made available at pin two of a selector switch. Pin one of the selector is a square wave of the original 60 Hz line rate, pin two is a rectangular pulse of 6 Hz rate or the line rate divided by ten. The remaining pins consist



CATT Turn-Off Time Tester, Pulse Generator Circuit Diagram

Figure 21



GATT Turn-Off Time Tester, Pulse Generator, Basic Pulse and Counter Circuit Diagram

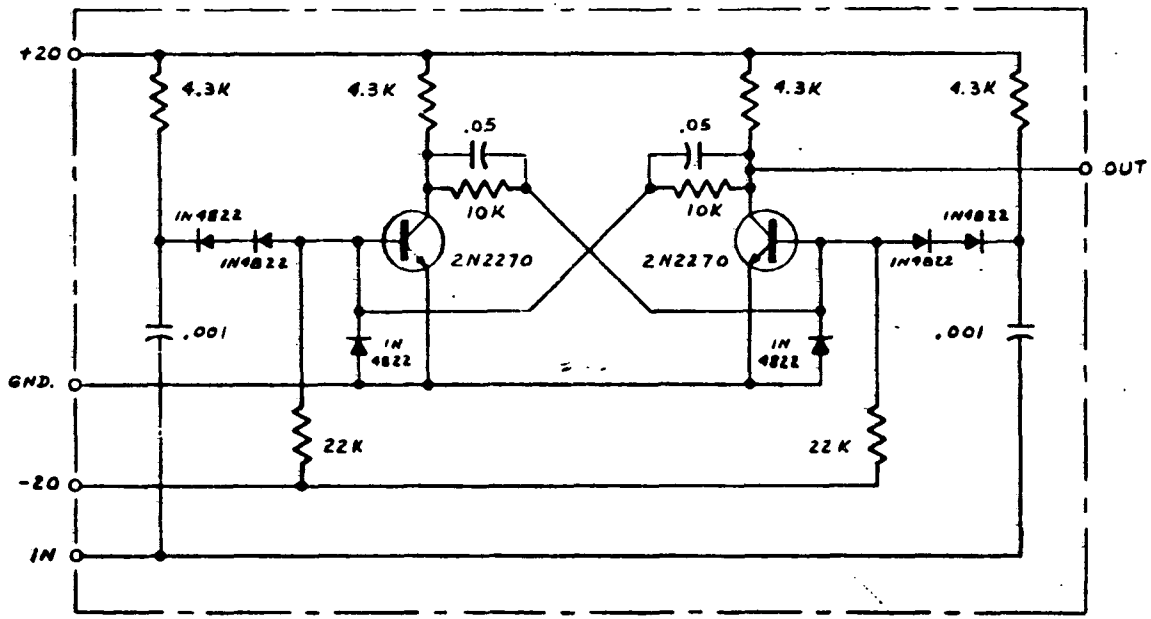
Figure 22

3.3.1 Turn-off Tester Logic (Cont.)

of the 6 Hz output divided by two, four, or eight. The additional counting originates with the basic flip-flop arrangement shown in Figure 23 and Figure 24. The output of the count selector switch allows selection of pulse rates of 60, 6, 3, 1.5, and .75 Hz. These signals trigger two serially connected Schockly diodes, discharging a capacitor across the base of Q7 producing either a common referenced trigger or isolated trigger for timing usage. The rate is, of course, dependent upon the counter selector switch. This particular referenced pulse is labeled pulse #1 and is the timing signal used to produce the delayed pulses, pulse 2 and pulse 3. The alternate zero crossing pulse available at the output of squarer Q3 drives flip-flop Q4 and Q5. The flip-flop will not toggle, however, unless it has been preset by the action of pulse one, available at the base of Q5 from the count selector switch. Hence, the flip-flop toggles only at the selected count rate of pulse one. The flip-flop output drives two Schockly diodes in series which discharge a preset capacitor across the base of Q6. A sharp trigger, coincident with the second zero crossing, is available at the emitter of Q6, referenced to common or transformer isolated. As diagramed in the logic system block diagram of Figure 21, pulse 1 is sent to a pulse delay and used to generate pulse 2. The incidence of pulse 2 determines the width of the trapezoidal current pulse of the turn-off time tester. Pulse two may be used to originate a second delay to produce pulse three or pulse one may originate the second delay. Pulse three determines the incidence of the reapplied voltage pulse. Details of the pulse delay circuits are shown in Figure 25. In this circuit, an input flip-flop, Q1-Q2, is set by the pulse to be delayed. This action causes Q4 to turn-off, allowing a charging current furnished by current source transistor Q3 to charge a small capacitor. The ramp voltage at the base of Q5 is current amplified by that stage, and is used to trigger Schimdt trigger circuit Q6 and Q7. The output from Q7 is shaped, amplified, and given proper sense by Q8 and Q9, and finally current amplified by Q10 to yield delayed pulse two at its emitter. Delay is accomplished by varying the ramp bias level in the emitter of Q5. This varies the incident point at which the Schmidt trigger fires. Ramp rate of rise is determined by adjustment of the charge current provided by Q3. This gives a measure of range control. The ramp charge capacitor across Q4 may be switched for course range control. Final reset of the input flip-flop is provided by pulse four. The delay circuit provides linear delay control of from 20 microseconds to several thousand microseconds. By special design, minimum delays of two microseconds are possible. All output pulses are emitter follower current amplified by transistor stages shown in Figure 26.

3.4 Equipment Calibration Schedule

All equipment used for measurements of data in this report was maintained on a 90-day calibration schedule against standards at the Research Laboratories, which are traceable to the National Bureau of Standards.



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	IT.		

REF. DWG 7208763

WESTINGHOUSE ELECTRIC CORPORATION

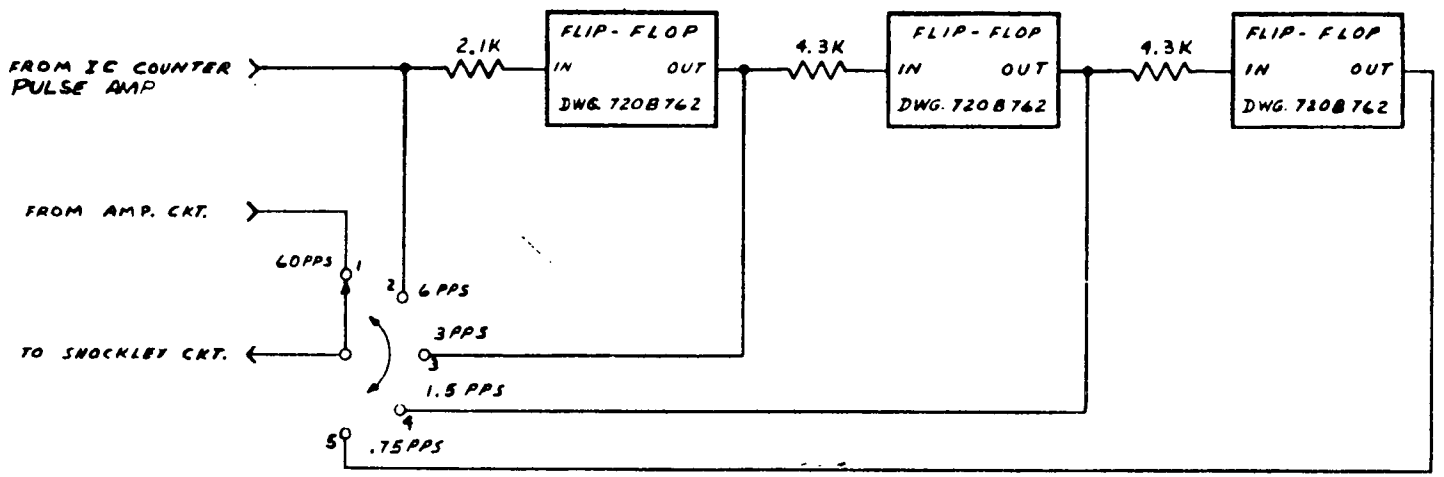
TITLE PULSE GENERATOR
FLIP-FLOP SCHEMATIC

DIMENSIONS IN INCHES. DO NOT SCALE DRAWING — SUB. 1

DFTM C. Fink	1-25-1948	APPD JBB	720 B 762
CHKD		APPD	
SUPV		APPD	

RESEARCH LABORATORIES CHURCHILL BORO PITTSBURGH 35 PA., U.S.A.

GATT Turn-Off Time Tester Pulse Generator, Flip-Flop Circuit Diagram
Figure 23



WESTINGHOUSE ELECTRIC CORPORATION

TITLE PULSE GENERATOR
FLIP-FLOP CIRCUIT DIA.

DIMENSIONS IN INCHES DO NOT SCALE DRAWING | SUB. 1

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CHRD | APPD
SUPV | APPD

RESEARCH LABORATORIES CHURCHILL BORO PITTSBURGH 35 PA U.S.A.

REF DWG 4846048

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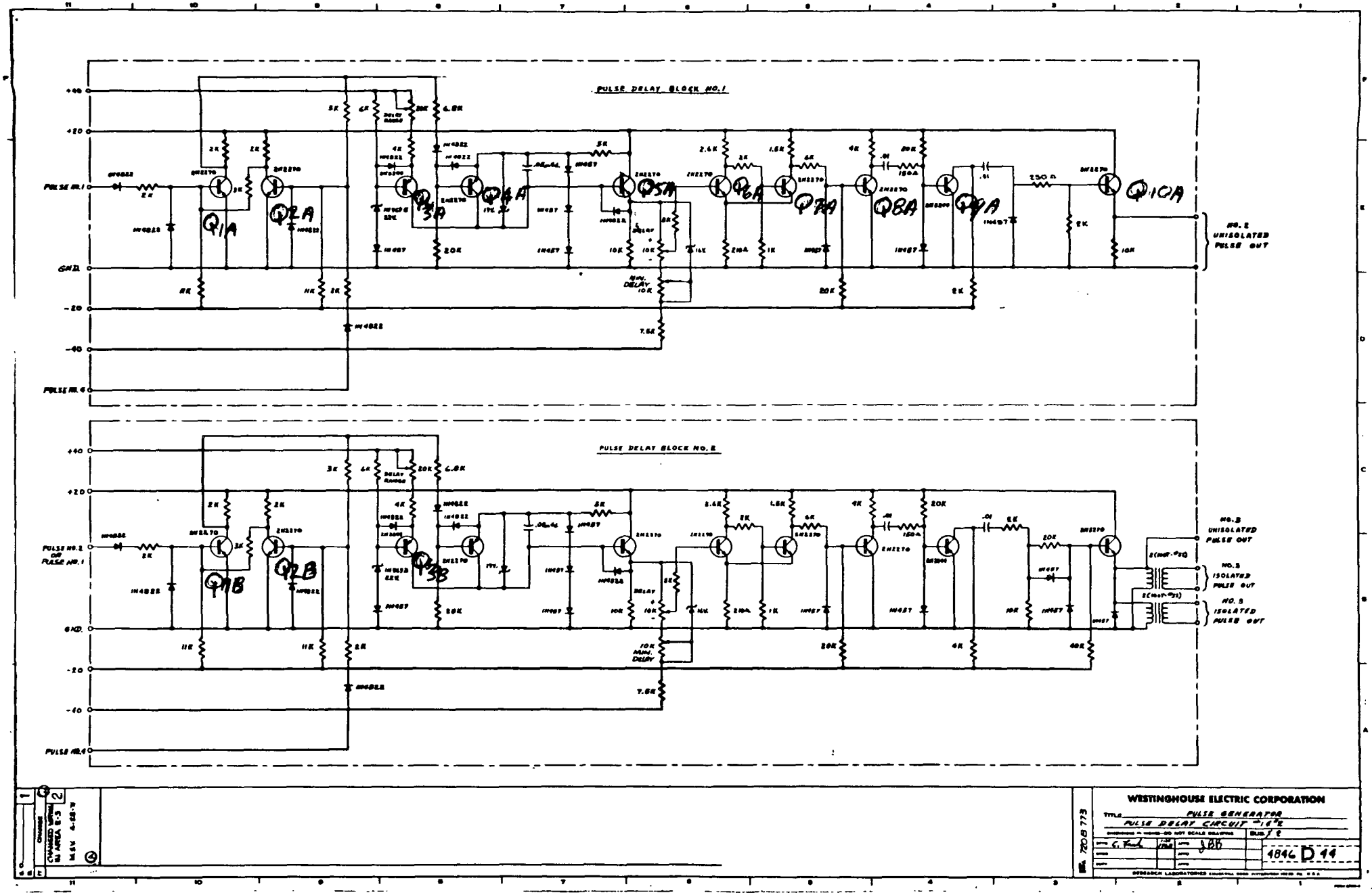
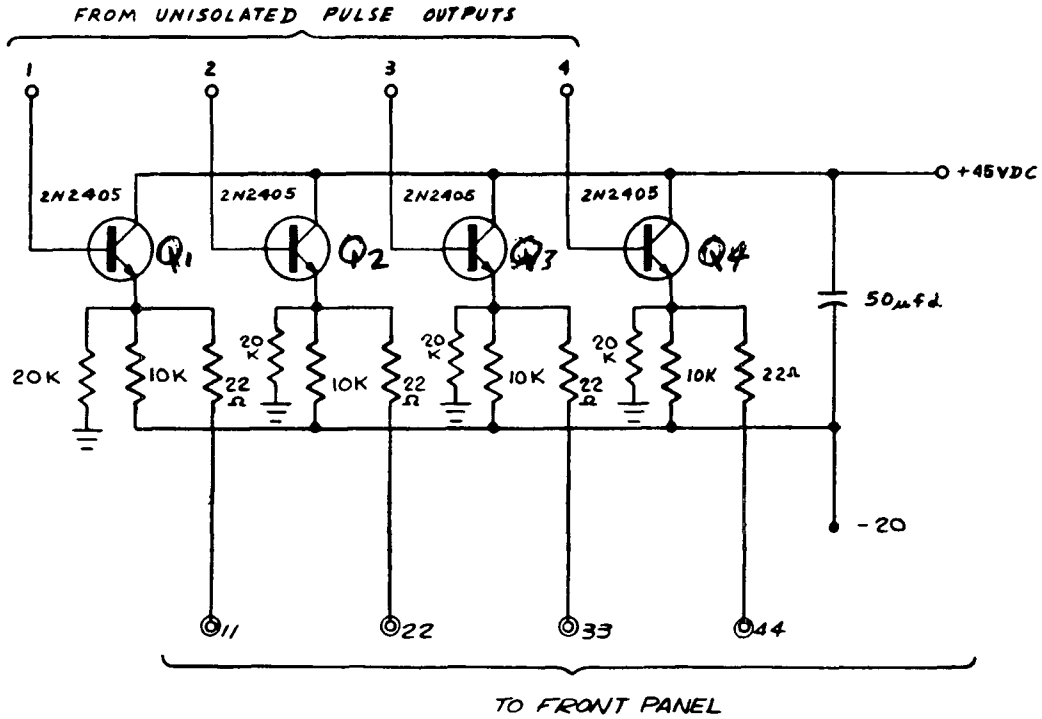
GATT Turn-Off Time Tester Pulse Generator, Flip-Flop Block Circuit Diagram

Figure 24



GATT Turn-Off Time Tester Pulse Generator, Pulse Delay Circuit Diagram

Figure 25



S.O. / D.	IT.	CHANGE		REF. DWG.
1 (A)	2	ADDED 4 20K RES. AND GNDS. DELETED 2 GNDS AND ADDED -20. M.S.V. 4-28-71		7208773

WESTINGHOUSE ELECTRIC CORPORATION

TITLE PULSE GENERATOR
PULSE CURRENT AMPLIFIER

DIMENSIONS IN INCHES—DO NOT SCALE DRAWING — SUB. # 2

DFTM C. Fink	1-15-1968	APPD	BB
CHKD		APPD	
SUPV		APPD	

720 B 758

RESEARCH LABORATORIES CHURCHILL BORO PITTSBURGH 35 PA. U.S.A.

R 1117-8

GATT Turn-Off Time Tester Pulse Generator, Pulse Current Amplifier Circuit Diagram
Figure 26

IV. FABRICATION OF GATT II DEVICES

The device design information generated during the first phase of the subject contract was sufficient to establish a second generation device design specification. The simultaneous implementation of the planar passivated cathode-gate configuration in concert with the cathode preform idea provided a manufacturable system in the strategic area of contacting and encapsulation. And, finally, the establishment of a complete device evaluation test facility in parallel with the device development tasks finished the work of the first phase of the contract effort.

The above achievements were reviewed in depth with the contracting agency. It was agreed to initiate work on the second phase which was designed to yield the deliverable items, fifty (50) finished GATT II devices. It was agreed that the specification for these devices would be as given in Table 5.

4.1 Design

Basic fusion design parameters were determined as a result of the analysis of AGE I and AGE IV experimental runs discussed in Section 2.3 and in conjunction with the voltage and current considerations developed in Section 2.1. These specified design parameters will be detailed in the discussion of pilot runs which follows in Section 4.3. The fusion structure as shown in Figure 8, i.e. with contact preform attached, was adopted. And, the standard Westinghouse T600 CBE (compression bonded encapsulation) package construction with flag-type terminals was adopted. The latter is illustrated in Figure 10.

4.2 Process

The fabrication process for the pilot runs follows closely that employed in the earlier experimental runs. The process flow is outlined in Figure 27. Quality assurance controls were introduced in accordance with the requirements of this process flow.

4.3 Pilot Runs

In order to insure success in meeting the requirements of the contract in terms of numbers of finished devices as well as performance, two pilot runs were made. These were designated as AGE X and AGE XI.

Stud temperature = 100°C

Symbol	Description	Specification
V_{DRM}	Minimum forward blocking voltage	1000 volts
V_{RRM}	Minimum reverse blocking voltage	1000 volts
I_T	Maximum RMS forward current	100 amperes
V_{TM}	Maximum steady state forward voltage drop for conduction of 100 amperes	2 volts
t_{on}	Time required to reach V_{TM} after initiation of current conduction with a rate of rise of 75 amperes per microsecond and application of a gate signal of 15 amperes (with a rise time of 100 ns) for three microseconds.	2 μsec.
I_{DRM}	Maximum forward leakage current at 1000 volts	10 ma
I_{RRM}	Maximum reverse leakage current at 1000 volts	10 ma
I_G	Typical gate current to fire at V_{FB} = 5 volts	400 ma
V_G	Maximum gate voltage to fire at V_{FB} = 5 volts	4 volts
I_h	Minimum holding current	25 ma
t_R	Maximum time after anode current has reached zero before anode voltage can be reapplied at the maximum rate of rise of voltage (dV/dt) as stipulated below.	2 μsec.
dV/dt	Maximum rate of rise of anode voltage, gate bias 10 volts/10 ohms	400 volt per μsec.
di/dt	Maximum rate of rise of current concurrent with and after a gate signal of 15 amperes for three microseconds.	75 amperes per μsec.

GATT II Device Final Specification

TABLE V

1 - Silicon Preparation	Lapping
	Cleaning
	Etching
2 - Junction Formation	Gallium Diffusion
	Gallium Drive & Oxidation
	Photomasking
	Phosphorous Diffusion
	Phosphorous Drive
	Photomasking
3 - Contacting	Anode Alloying (Mo + Al)
	Aluminum Evaporation
	Photomasking
	Aluminum Sintering
4 - Junction Passivation	Angle Bevelling
	Spin Etching
	Organic Coating
5 - Encapsulation	Cathode Preform Attachment
	Fusion Testing
	Pressure Mounting (Pre-Encapsulation)
	Ceramic Seal Welding
	Lead Swaging
6 - Test	Static Testing
	Dynamic Testing

Process Flow Chart

Figure 27

Start-up details are as follows (quantities are approximate figures):

	AGE X	AGE XI
Number of slices	450	450
Slice resistivity	44-60 ohm-cm	33-39 ohm-cm
Slice etch thickness	280-290 μm (11.0-11.4 mils)	270-280 μm (10.6-11.0 mils)

In order to accommodate the large number of starts in the pilot line, it was necessary to split each run into two parts. This occurred prior to the gallium drive and oxidation step early in the junction formation process. Each of the four subgroups was then processed as an independent unit throughout the balance of the fabrication process.

The gallium deposition process conditions were constant for both runs. The process was performed in an evacuated sealed quartz ampoule at 1175°C for 16 hours, followed by slow cooling. The furnace was calibrated for temperature prior to use as quality control check. This practice is repeated throughout the junction formation process and will not be mentioned further. Junction depths were 22 μm and 23 μm for AGE X and AGE XI, respectively. Surface concentration was the same for both runs, approximately 3.7×10^{18} atom/cc. The notable difference was carrier lifetime measured to be 5.5 μs for AGE X and 15 μs for AGE XI. These values were obtained using the open circuit junction voltage decay technique as described by Lederhandler and Giacolletto.[3]

Gallium drive for AGE X was done in an open tube at 1235°C for 16 hours. Without removing the charge, oxidation was then performed for an additional three hours, followed by slow cooling. Junction depths for subgroups A and B were 49 μm and 47 μm, respectively. Surface concentration slumped back to a somewhat lower level. Carrier lifetime increased to 8 μs and 12 μs, respectively, for the two subgroups.

Gallium drive for AGE XI was also done in an open tube furnace at 1235°C for 16 hours. Slow cooling ensued. (Oxidation was performed as a subsequent operation at 1200°C for three hours). Junction depths for subgroups A and B were 46 μm. As in AGE X, surface concentration slumped back to a somewhat lower level. Carrier lifetime measured between 8 μs and 11 μs on subgroup A; the measurement was inadvertently not recorded for subgroup B.

Phosphorous deposition was done in an open tube furnace using $POCl_3$ as the source, for one hour at 1200°C. These conditions were constant for all four groups.

Phosphorous drive was done in an open tube furnace at 1200°C for all runs. AGE X was driven for 13.5 hours, yielding junction depths of phosphorous of 18 μm and 19 μm for subgroups A and B, respectively. Carrier lifetime was about 5 μs in both cases. The gallium junction depths after this final high temperature step were 57 μm and 60 μm, respectively.

AGE XI was driven for 16 hours, yielding junction depths of phosphorous of 23 μm and 20 μm for subgroups A and B, respectively. Carrier lifetime was measured to be 3 μs and 4 μs, respectively. The gallium junction depths after this final high temperature step were 60 μm and 57 μm, respectively.

In summary, the differences between subgroups within each run were small. This indicates excellent process control and reproducibility. A further comparison between AGE X and AGE XI reveals the designed-in difference in the phosphorous junction depth/working point parameters. AGE XI was driven longer, thus the working point is lower than that of AGE X. Specifically, $x_{w.p.}$ for AGE XI is 1.7×10^{17} atoms/cc; $x_{w.p.}$ for AGE X if 4.8×10^{17} atoms/cc.

The balance of the fusion fabrication process, contacting and junction passivation, are standard as far as process conditions can be measured, and therefore a constant. This also includes the attachment of the cathode preform.

At this point the fusion can be tested. Fixturing is employed which simulates conditions which will exist in the final package. Assuming the fusion is not rejected during testing, it is forwarded to the assembly line for packaging. Again, standard processing is employed with the singular exception of the retaining force applied. In order to accommodate the smaller cathode contact relative to a "standard" thyristor fusion of the same nominal size, the force was reduced to 75% of standard.

Devices so packaged are ready for final test and evaluation.

4.4 Results

The numbers of fusions available for test were: AGE X ... 289; AGE XI ... 296. Referring to the 450 starts per run, the raw yield is about 65%. This figure is not adjusted for the relatively large number of sample slices which are used in performing the various quality control and monitoring steps; nor does it take into account the number of standard thyristor control devices processed in parallel with the GATT II devices.

V_{DRM} and V_{RRM} are the first tests performed in order to classify the product and screen out the obvious rejects. The data generated is presented in Table 6.

	AGE X-A	AGE X-B	AGE XI-A	AGE XI-B
> 1000V	66	3	3	--
800-1000V	59	56	41	73
600-800V	9	29	30	28
400-600V	--	18	40	38
< 400V	34	15	29	14
	168	121	143	153

AGE X and XI Fusion Voltage Distribution

Table 6

The AGE X run yields the higher voltage distribution. This is expected since the starting silicon was thicker and higher resistivity (see Section 4.3).

The remainder of fusion tests performed were designed to determine the character of the run as a whole. Thus they consisted of sampling the run for, notably, forward drop and turn-off combination relative to lifetime control. It was early determined that AGE X was not suitable for producing devices to the required specifications. A decrease in carrier lifetime in order to reduce turn-off to the two microsecond level resulted in the forward drop increasing well beyond the two volt limit at 100 amperes.

Emphasis shifted to the AGE XI run. Again, samples were tested for the V_{TM}/t_{off} combination for several levels of carrier lifetime. In this case it was determined that the combination was in reach. The balance of the run was processed accordingly.

It was determined to be necessary to perform screening tests on reverse gate characteristics. Leakages were found to run too high in some cases, resulting in catastrophic failure in turn-on test of the packaged device. Fusions were then screened to several leakage limits at 15 volts: 100 ma, 500 ma, 1500 ma and > 1500 ma. It was determined that leakages in excess of 1500 ma were prone to failure. All fusions were screened accordingly. Rejected fusions could be reworked in a number of cases by stripping the oxide.

V. CHARACTERIZATION OF GATT II DEVICES

A tabulated summary of GATT II performance is presented in this report. This section deals with the details of that summary. The characterization data covers both static and dynamic response under well defined conditions. These conditions originate from several sources. A large number relate to the thyristor-like properties of the GATT switch. Other conditions originated with contract specifications for well defined performance requirements. Finally, some conditions evolved during the contract growth period due to usage requirements.

5.1 Static Parameter Test Results

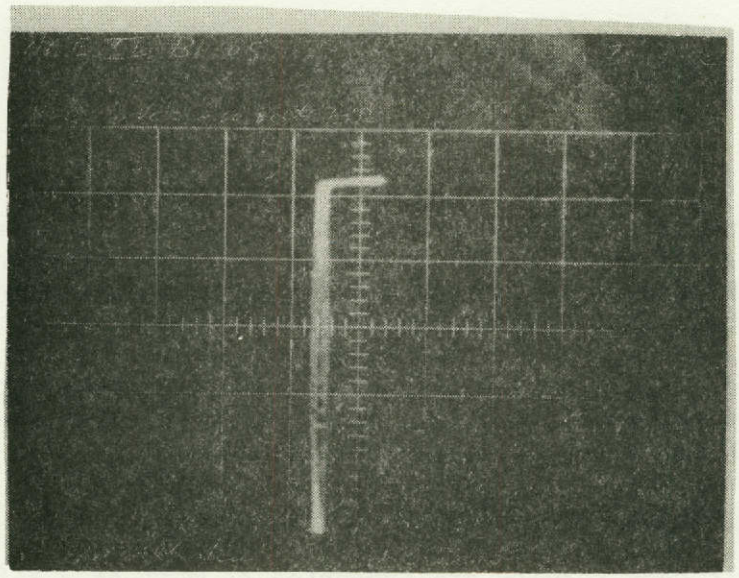
Static test results are presented as well as a definition of the test condition. This is followed by an explanation of the techniques employed for taking measurements and concludes with photographs or typical data presentations. In some cases, data is presented in graphical form to show characteristic spread or trends.

5.1.1 Forward Blocking Voltage

Blocking voltage is applied across the test device with anode positive and cathode negative. The voltage point at which the leakage current reaches 10 ma is defined as the forward blocking voltage.

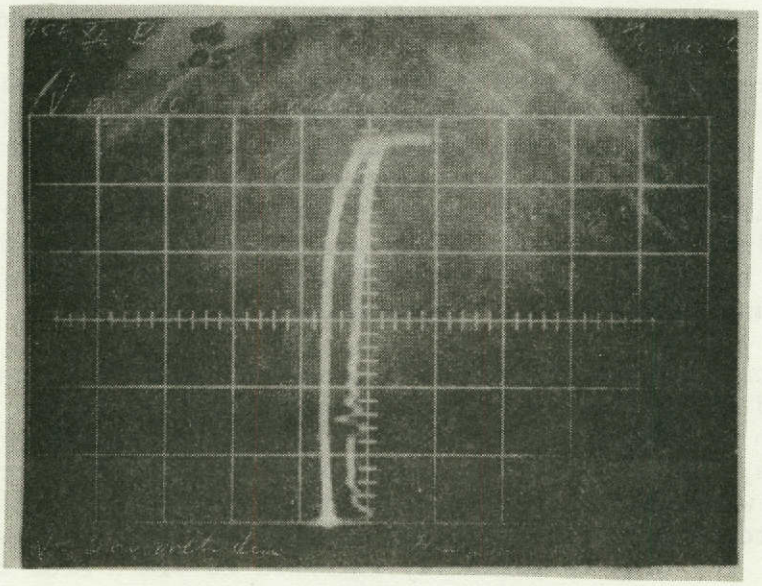
This parameter indicates forward blocking junction avalanche level, and possesses a positive temperature coefficient. Hence, if device surface passivation techniques are well under control, the forward blocking voltage level will increase with temperature. Nearly every GATT device tested exhibits this characteristic. Sample V-I trace plots of blocking voltage are shown in Figures 28 and 29 at case temperature of 25°C and 100°C. The avalanche function is sharp, and increases with temperature.

In the case of the GATT devices, forward blocking voltage is always measured for a fixed gate condition. This is that the gate-cathode junction be biased with a negative ten volts serially with ten-ohms. In usage, the GATT switch should never support and block forward voltage without the benefit of a biased gate. The bias is not intended to enhance forward blocking ability, but it does have this effect. The bias is primarily intended to drain from the gate displaced carriers generated by transient (dv/dt) positive anode voltages. In standard thyristors, these carriers bypass the gate-cathode junction by traversing small carrier channels called shunts.



Forward Blocking VI Trace, T_c = 25°C
Hor. - 2 ma/div, Vert. - 200 volts/div
Device B1-05

Figure 28



Forward Blocking VI Trace, T_c = 100°C
Hor. - 2 ma/div, Vert. - 200 volts/div
Device B1-05

Figure 29

5.1.1 Forward Blocking Voltage (Cont.)

Shunts are low resistance paths formed across the gate-cathode junction. Thus, dv/dt induced currents are shunted around the gate-cathode junction and do not cause injection from this junction which could turn a device on. Since a GATT possesses no shunts, dv/dt induced currents are extracted from the gate region by a negative biased gate and the purpose of shunts is thereby accomplished.

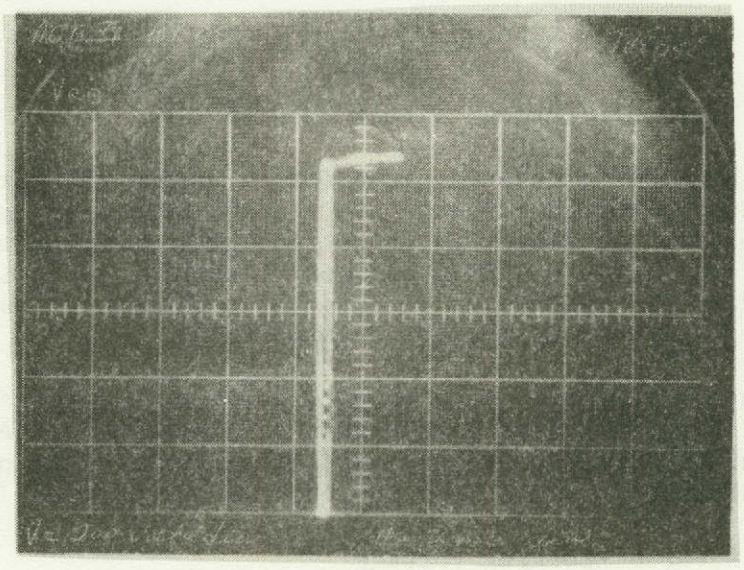
The secondary benefit of a shunted gate, or a reversed biased gate, is that of bypassing leakage currents originating in the anode. Hence, the leakage currents are not multiplied by the gain of the NPN equivalent transistor and forward blocking voltage is improved.

5.1.2 Reverse Blocking Voltage

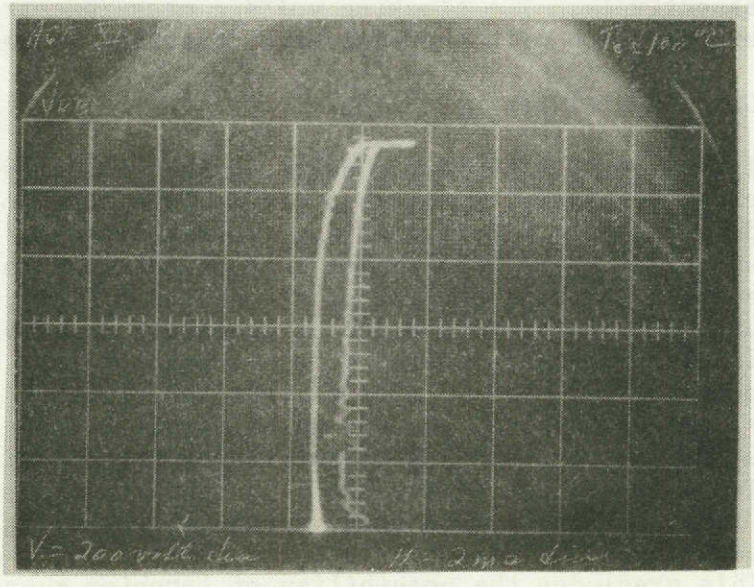
Blocking voltage is applied across the test device with anode negative and cathode positive. The voltage point at which the leakage current reached 10 ma is defined as the reverse blocking voltage. Reverse blocking voltage is measured with the gate-cathode junction open circuited, since negative gate biases will not influence the reverse blocking voltage junction. Sample reverse blocking voltage V-I traces are shown in Figure 30 and Figure 31 for case temperatures of 25°C and 100°C respectively. The blocking voltage measurements, all of V-I character, are made with the equipment described in Section 3.1.

5.1.3 Gate Sensitivity

Gate trigger sensitivity is a measure of the minimum gate voltage and gate current necessary to switch a device from the blocking state to the conducting state. Before making the measurement, the anode current to be switched for the measurement must be adjusted to a value greater than the known latching current of the device. Also the turn-on gate pulse must be adjusted to a width large enough to eliminate the effects of insufficient charge supplied by the trigger pulse. Driving pulses equal to or greater than 50 microseconds satisfy this requirement. Also, the rise time of the load current pulse should be considerably less than the gate pulse width. This eliminates the possibility that the gate pulse will end before the anode current rises above the latching current level. Finally, the anode current level being switched should be at least twice the measured latching current for the device under test. This precludes the possibility of latching current effects interfering with trigger sensitivity. All of these conditions may be met by the tester described in Section 3.1.3.



Reverse Blocking VI Trace, T_C = 25°C
Hor. - 2 ma/div, Vert. - 200 volts/div
Device B1-05



Reverse Blocking VI Trace, T_C = 25°C
Hor. - 2 ma/div, Vert. - 200 volts/div
Device B1-05

Figure 21

5.1.3 Gate Sensitivity (Cont.)

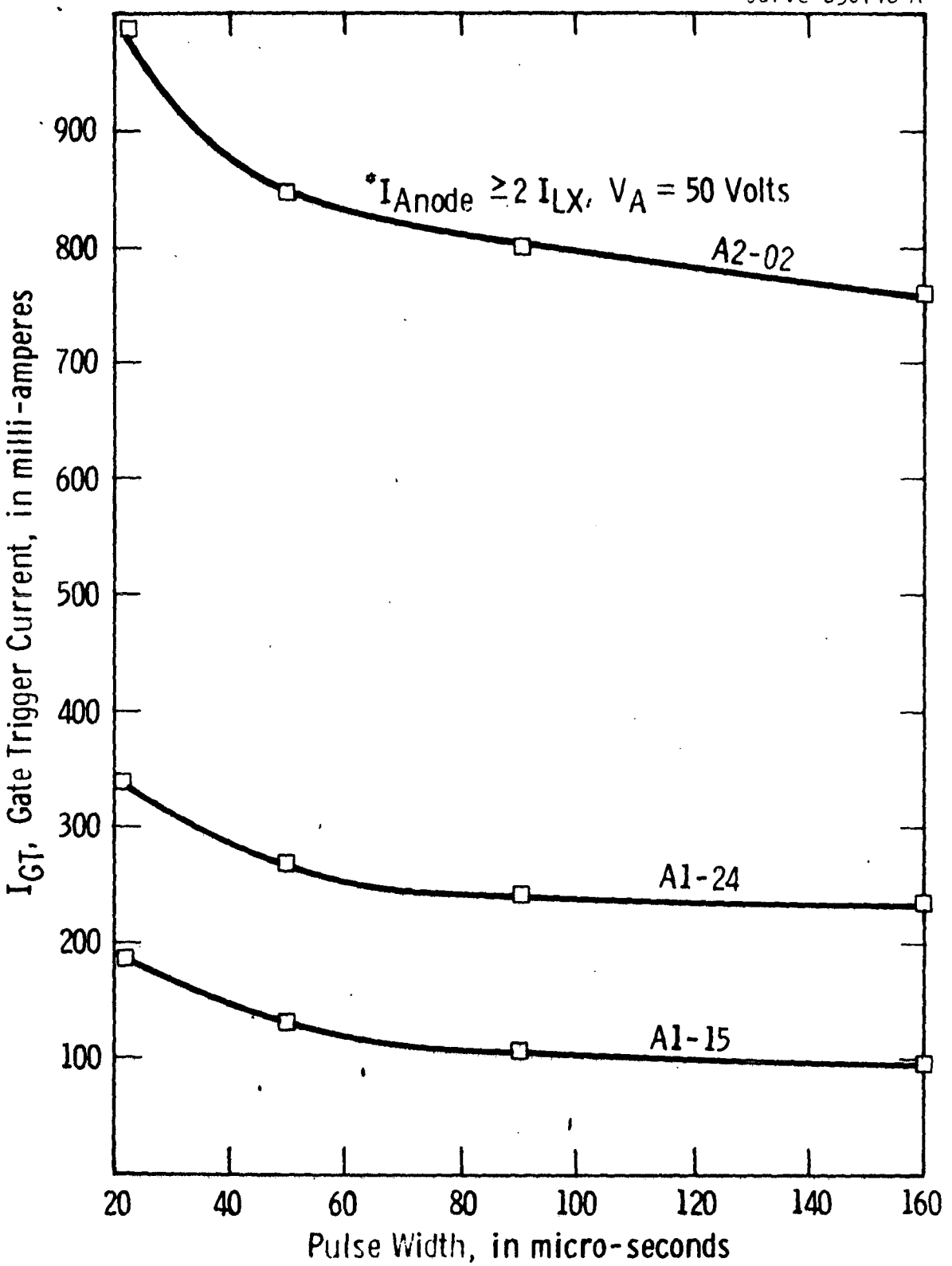
A sample of the manner in which gate trigger pulse width affects gate current to trigger is given in Figure 32. At gate trigger pulse widths less than 50 microseconds, considerable decrease of sensitivity occurs. The trend is identical for several samples of different trigger sensitivity levels. The spread of I_{GT} among devices from a common lot is attributed to normal process variations, compounded in the subject case by the long cathode gate periphery. The reproducibility of the data of Figure 32 is a moderate function of device temperature and the tendency is for sensitivity to increase with increasing temperature. The temperature sensitivity is further amplified in Figure 33 where the trigger sensitivity is plotted for a single device at case temperature of 25°C, 75°C, and 100°C. The increasing sensitivity of Figure 33 is only of academic interest since the specified negative bias of the GATT device must first be overdriven before false triggering can occur, and the available bias supply current of one ampere is large compared to the gate trigger sensitivity at high temperature.

Trigger sensitivity measurements for all devices are given in tabular form at the conclusion of this section. All measurements are given for anode voltage of 50 volts, gate pulse width of 50 microseconds, and load current set to greater or equal to twice the latching current for the device under test. Test data is presented for case temperature of 25°C. All devices, following the trend of Figure 32, fall well within the gate trigger sensitivity spec at 100°C. Gate trigger voltage sensitivity measurements, also in tabular form, vary in value from 0.6 volts to 1.3 volts. These values are less than 4 volts; all are within specification.

5.1.4 Latching and Holding Current Test Results

5.1.4.1 Latching Current (I_{LX})

Latching current is the minimum value of anode current for which gate drive may be removed from a device and forward conduction will be maintained under dc conditions. Latching current is tested with the equipment described in Section 3.1.3. The technique is to switch a device from a moderately high supply voltage such as 50 volts and continuously increase anode current until a complete collapse of anode voltage occurs. Prior to latching, the device will support anode voltage at all intervals except during the application of the gate pulse. During the gate drive periods, anode voltage will be low, but switching to the post-latch condition will not occur. This pre-latch condition shows the transistor character of the GATT device. Both PNP and NPN transistor equivalents of the GATT function, but gain is insufficient to force transfer to the mode in which gate current



-Gate current to trigger, I_{GT}, versus gate trigger pulse width

Figure 32

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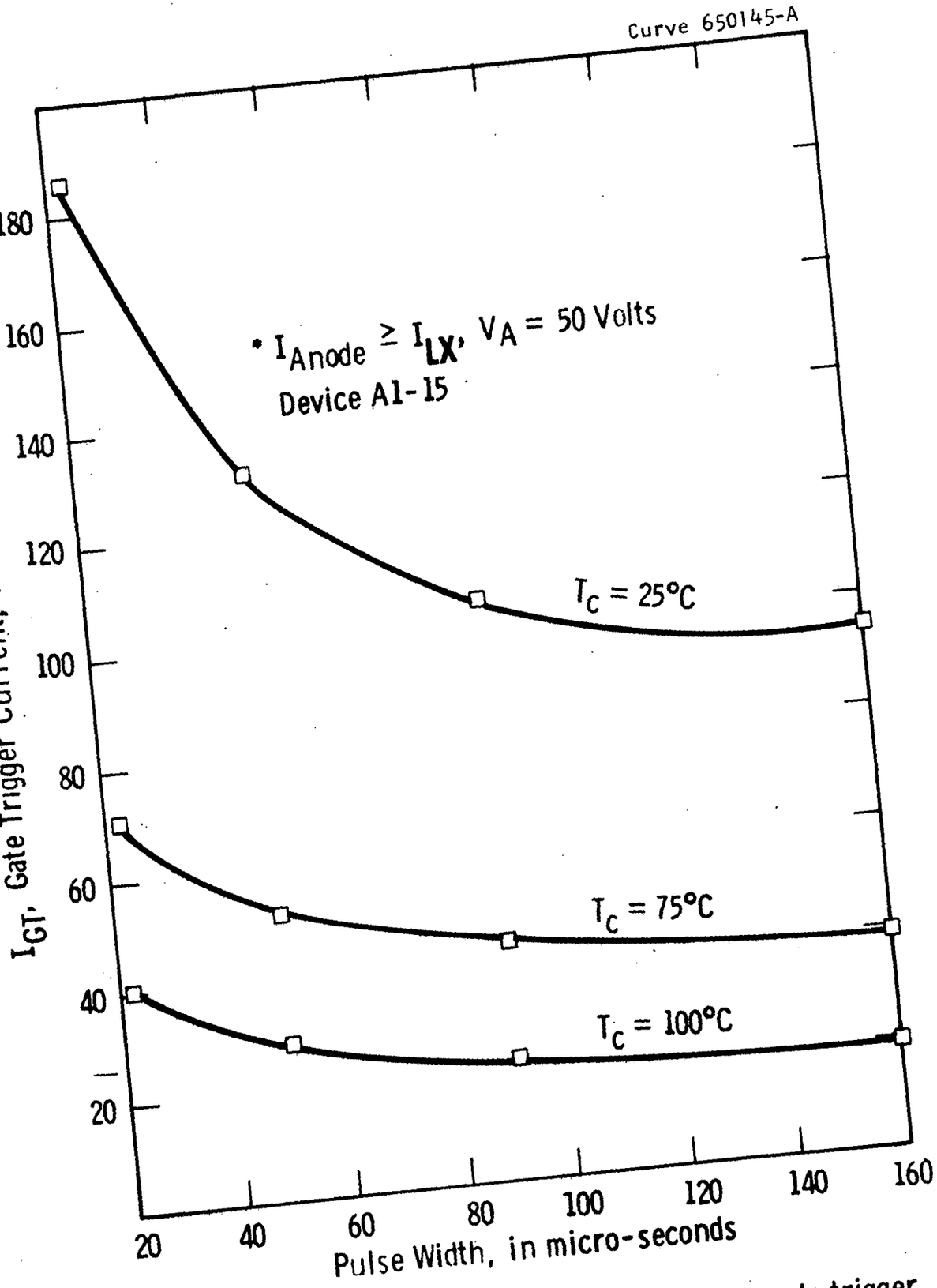
650146-A



Gate current to trigger, I_{GT}, versus gate trigger pulse width

Cur # 650145-A

Figure 33

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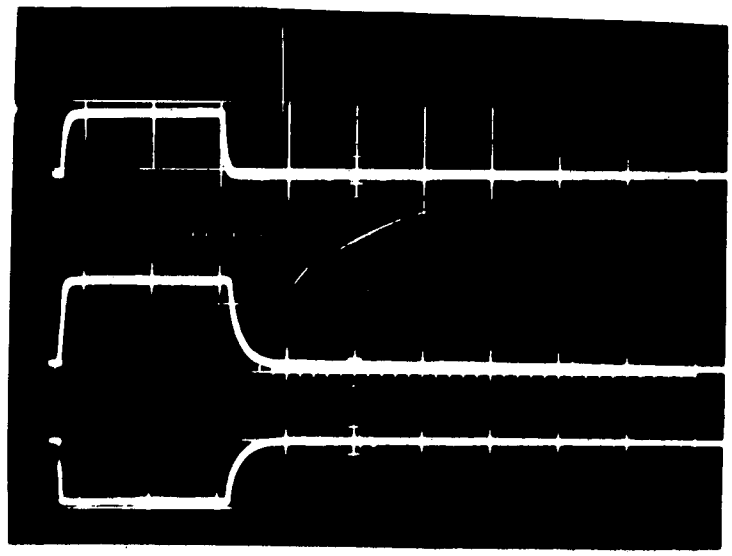
. - s.l. 12-11-72

5.1.4.1 Latching Current (I_{LX}) (Cont.)

control is lost. The pre-latch condition is shown in Figure 34; the parameters are gate current, anode current, and anode voltage. During the interval in which gate drive is applied, anode voltage is only several volts, allowing current to build up to a constant value. When gate drive decreases to zero, voltage blocking action is restored, very similar to the manner in which a transistor responds to a removal of gate drive. The anode current of Figure 34 is observed with a pulse transformer; the true latching current may be measured as the value of the anode pulse amplitude just prior to the point it turns to a dc value.

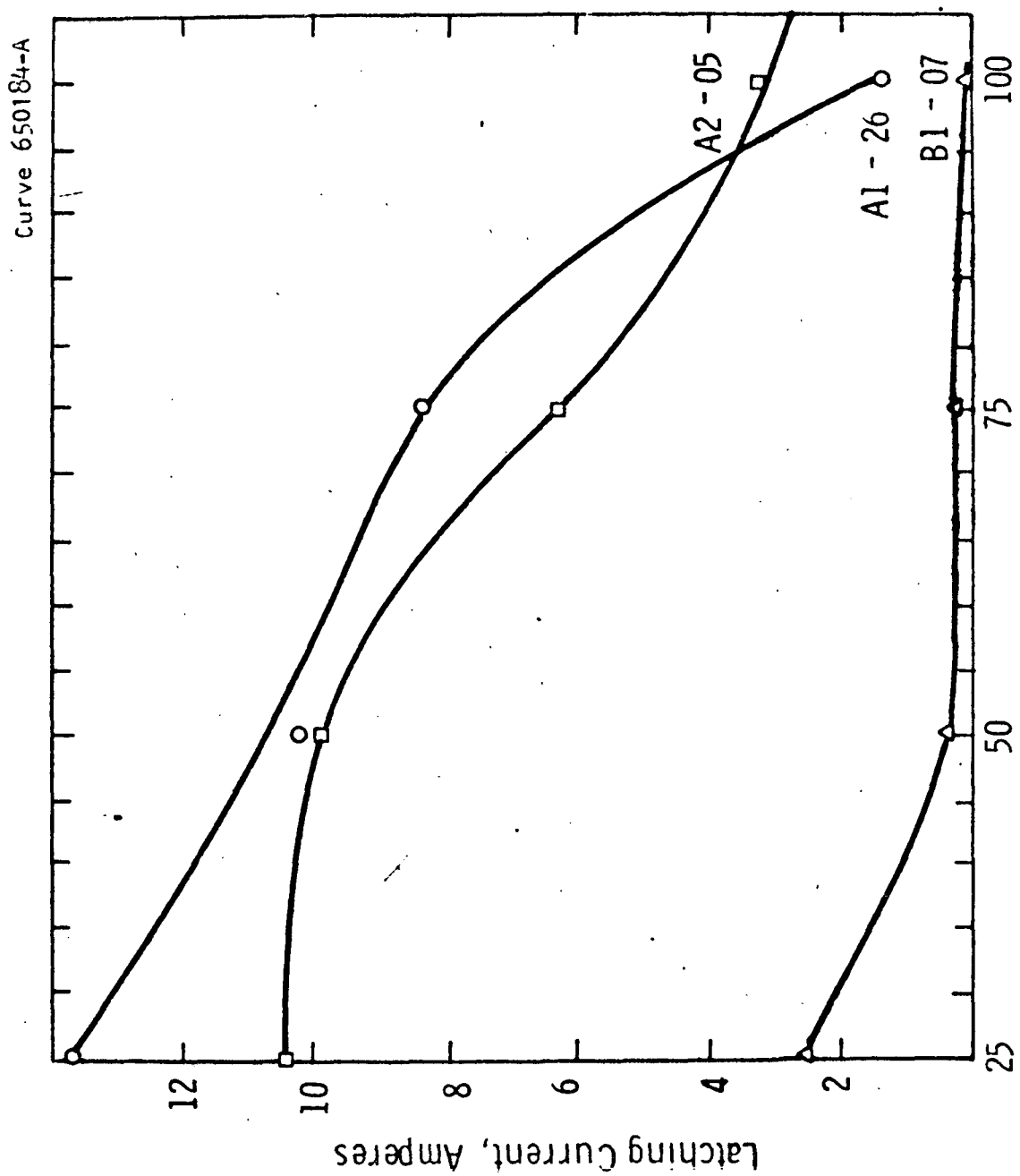
The tabulated latching current in this report is measured for an anode voltage level of 50 volts, gate drive pulse width of 50 microseconds, and gate current amplitude of two amperes. Data is presented to show temperature effects. For gate drive pulse widths of greater than 20 microseconds, a change of latching current with pulse width was not noticed. This assumes the anode current rise time is fast enough to reach latching level before gate drive terminates. A sample of anode current rise time may be seen in Figure 34. Figure 35 presents latching current temperature trend data of several devices. The temperature relationship is strong, tending to rapidly reduce latching current at above 50°C.

The most critical latching current effect is a dynamic one, related to the minimum gate pulse width recommended for maximum switching performance. Through testing, it has been determined that a gate pulse of 15 amperes amplitude, 150 nanosecond rise time, and no less than three microseconds duration is necessary to achieve maximum turn-on performance of the GATT thyristor. Maximum performance is taken to mean ability to switch a predetermined rate of change of anode current (di/dt) with least anode and gate power loss. The rated di/dt under rated gate drive conditions is 75 amperes per microsecond. Latching current effects are noticeable when switching di/dt's are low, 10 amperes per microsecond and below. The devices used for these final tests are part of the group of deliverable samples required by the contract. Performance with a short three microsecond gate pulse and low di/dt anode current is illustrated in Figures 36 - 38. The same response variables are noted in each photo, beginning with the gate current which is shown at the top of the group. The lower section of the photo shows a combined anode voltage and anode current response; zero point



Pre-Latch Anode Voltage and Current Response
Device A2-05

Figure 34



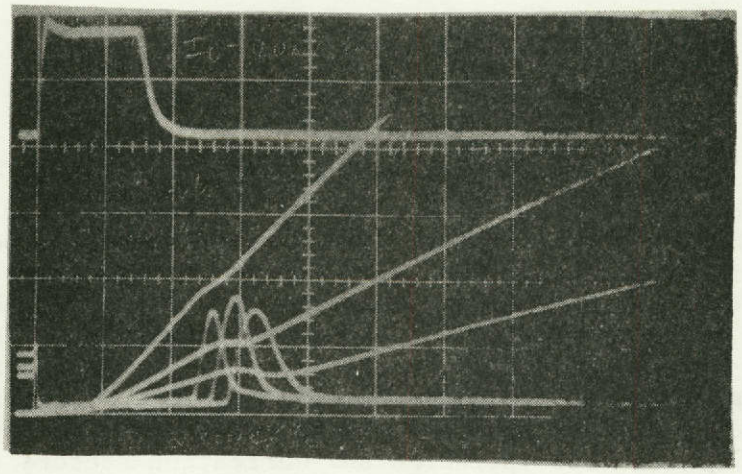
Latching current, I_{LX}, vs junction temperature

Figure 35

J. B. Brewster
J.m.s. - a.c. 12/12/72

Curve 650184-

Device A1-23, Low $\frac{di}{dt}$ Latching Test



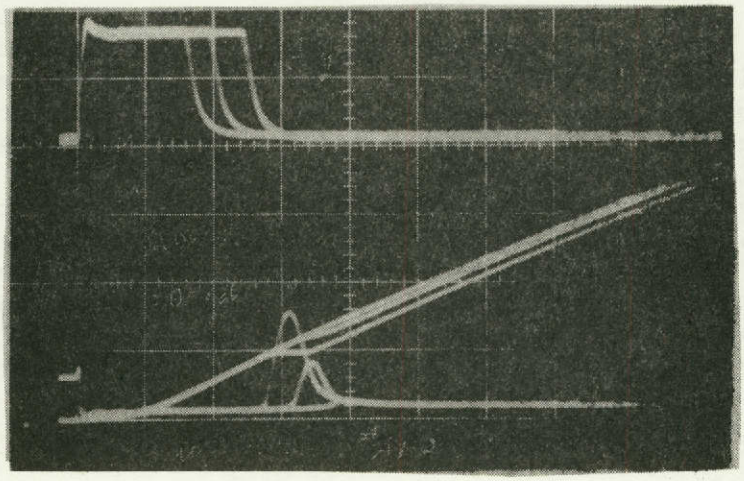
I_g - 10 amps/div

V_A - 20 volts/div

I_A - 20 amps/div

Hor. 2 μsec/div

Figure 36



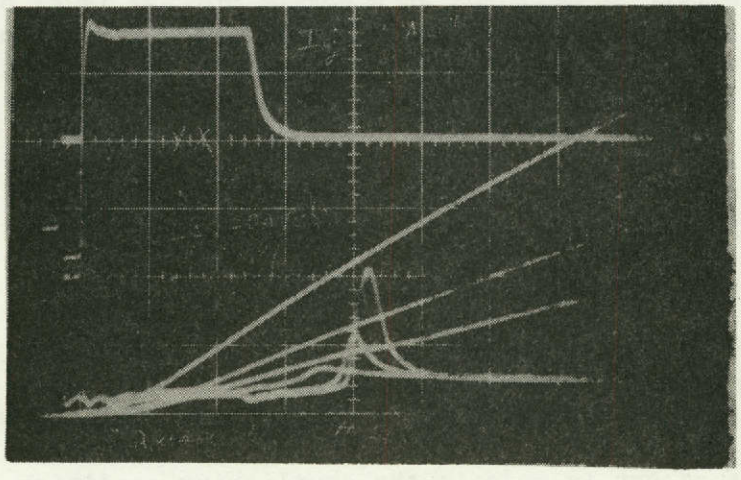
I_g - 10 amps/div

V_A - 20 volts/div

I_A - 20 amps/div

Hor. 2 μsec/div

Figure 37



I_g - 10 amps/div

V_A - 5 volts/div

I_A - 20 amps/div

Hor. 2 μsec/div

Figure 38

5.1.4.1 Latching Current (I_{LX}) (Cont.)

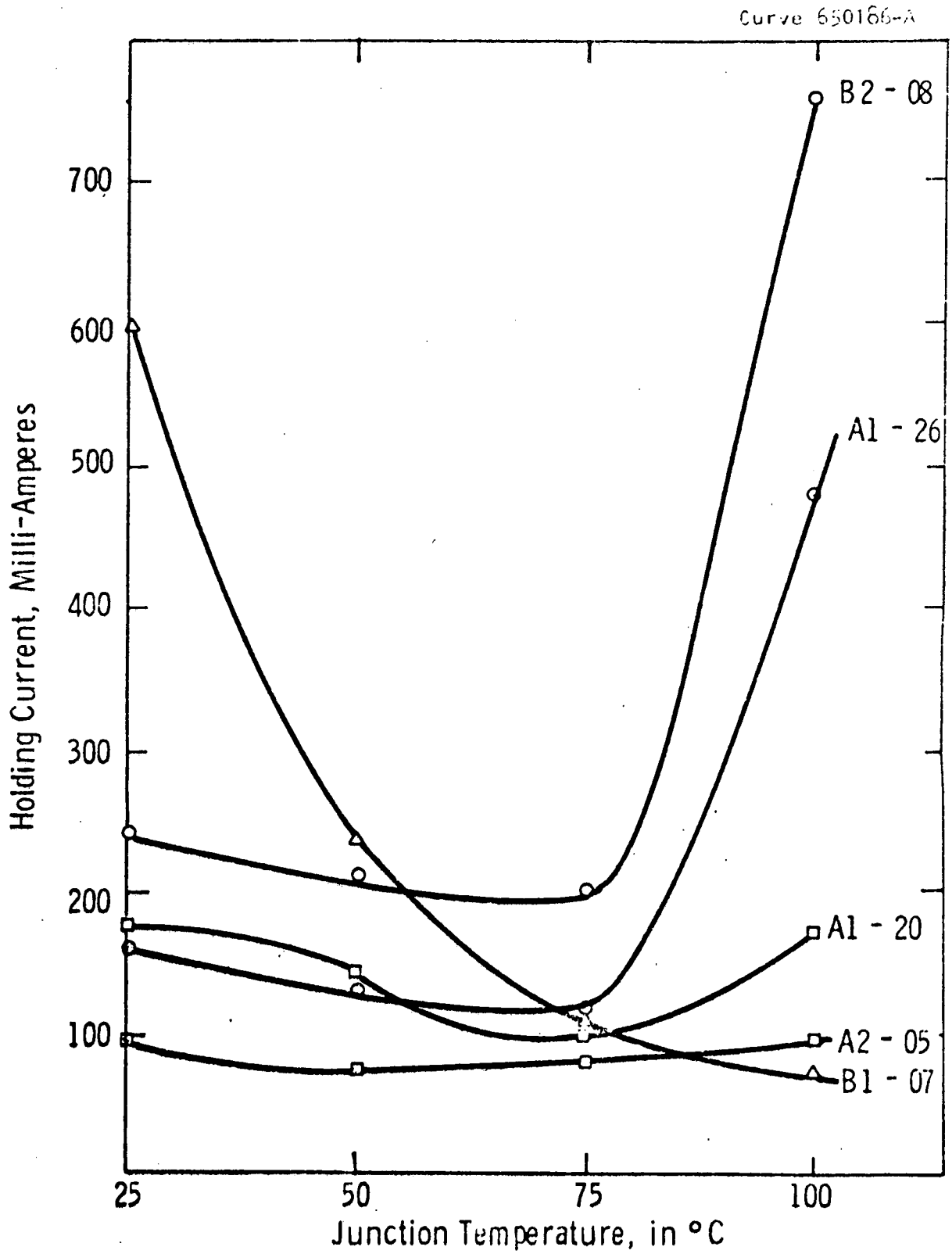
for both is adjusted to the bottom graticule. Figure 36 shows anode voltage and anode current response for the recommended gate pulse drive. The current rate of rise progressively increases from 2.5 amperes per microsecond. The switching is inadaquate since the anode voltage takes a 30 volt, two microsecond rise after the gate pulse ends, indicating only a near latch condition. The narrowing of the anode rise pulse occurs with increasing di/dt. The problem may be dealt with by increasing gate pulse width, shown in Figure 37. Here all variables and deflection factors are the same as Figure 36. The switched di/dt for all gate pulse widths is four amperes per microsecond, and this may be successfully latched with a 15 ampere drive pulse, but of five microsecond width. The progressive decrease of anode voltage rise after the gate pulse ends occurs for increasing gate pulse width. Finally, Figure 38 illustrates the switching performance of the same device for several di/dt's. These are 2.5, 4.0, and 6.6 amperes per microsecond. Again, the anode voltage increase after the gate pulse ends tends to deminish with progressively higher di/dt levels of anode current. The severity of the anode voltage deflection factor has been changed to five volts per division. In all cases, it may be interpreted that the rise in anode voltage following the end of the gate drive is near failure to switch due to insufficient turn-on charge supplied by the gate. With progressively increasing rates of rise of anode current, the effect diminishes and switching improves.

5.1.4.2 Holding Current (I_{HO})

Holding current is determined by latching a switching device, removing gate drive, and then diminishing anode current until current suddenly drops to zero and forward blocking is restored. Holding current is measured at blocking voltage level of 50 volts and is measured with the equipment described in Section 3.1.3. Holding current is presented in tabular form when measured at 25°C, and the open circuit gate current condition. The variation of holding current with temperature for several devices is shown in Figure 39. These variations are reasonably consistent and indicate the minimum holding current at 100°C will always be greater than the specified 25 milliamperes.

5.1.5 Conducting Forward Voltage Drops (V_{TM})

The specification of V_{TM} is defined as no greater than two volts when conducting 100 amperes, with case temperature of 100°C. This particular specification is quasi-static, in that the voltage is measured after conduction has spread to the extreme lateral regions of the device. The measurement is made in the equilibrium condition, i.e. after the device has achieved full conduction. A long conducting current pulse is easily achieved with a 60 Hz, half sine wave current pulse, of 100 ampere peak amplitude. The pulse is long in terms of



Holding current, I_{HO}, vs junction temperature

Figure 39

J. B. Brewster
d.m.s. - a.c. 12/12/72

Curve

5.1.5 Conducting Forward Voltage Drops (Cont.)

the time required for a thyristor to achieve the full "on" condition. The conducting forward drop is measured when the current pulse reaches its peak. At the current peak, rate of change of current is zero, and any errors due to induced voltages will also be zero. Induced voltage errors are small with 60 hz pulses, but become progressively larger as measurements are made with pulses of shorter width. The tabulated data at the end of this section gives the conducting forward drop under the conditions described, with the exception that stud temperatures are maintained at 25°C for the measurement. Since the forward voltage coefficient is negative for currents up to several hundred amperes, the 25°C measurement represents a worst case value and improves as junction temperature increases.

A second factor which affects the conducting forward drop of a GATT device is gate bias. In the class of devices such as the GCS or GATT type, the borderline character of the gainfulness of the switches will be evident by the tendancy for gate bias to have some influence on forward conducting voltage drop. This is best indicated by trend information such as in Figure 40. Here is shown the effect of gate current upon forward drop for several representative devices. The effect is shown for both the condition of current driven into the gate of the conducting device, and a negative gate current of one ampere. This latter effect should be only done with care, since all GATT devices have some measure of Gate Controlled Switch action and any attempt to operate a GCS-type device beyond its capability will result in quick failure. This applies directly to application of a modest negative bias to a GATT device conducting one hundred amperes, as is the test condition of Figure 40.

For the sake of comparison, the gate bias condition of tabulated forward drop data is zero, while the stud temperature of Figure 40 was 25°C. It might be assumed that the tabulated conducting drop information should agree with the zero bias measurement of Figure 40. In practice, some variation was observed, which was attributed to the heating character of the two different types of pulses used for each test. Tabulated data uses a half-sinewave, 60 hz pulse of 100 amperes peak, while Figure 40 uses a near constant 100 ampere pulse of 500 microseconds length. This trapezoidal pulse consistently gave V_{TM} measurements which were 100-200 millivolts greater than the 60 hz pulse. It was finally attributed to the junction heating effect of the long 8000 microsecond pulse, compared to the lesser heating of the shorter, trapezoidal 500 microsecond current wave.

Forward conducting voltage (V_F) vs gate bias current

Figure 40

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Curve 650

5.1.6 Transient Susceptability

Transient measurements are reported under static parameter test results because the measurements are made under conditions remote from prior current conduction. Junction conditions before the test are at equilibrium and the charges associated with current conduction have long since recombined. The conditions of the test are to apply a transient between anode and cathode of the device and determine if a turn-on can be achieved. This is presumed to be done non-destructively. The gate condition for a standard thyristor dv/dt test is that of open gate, but the conditions for the special GATT device is a specific gate bias condition. The gate bias condition is minus 10 volts through 10 ohms between gate-cathode. The purpose of the gate bias is to provide a path for dv/dt induced currents which would ordinarily flow across the gate-cathode junction, thus causing further conduction and finally turn-on. By flowing out the gate instead of across the gate-cathode junction, full forward blocking ability may be maintained for the most severe anode transient changes. The bias effect in a standard thyristor is achieved provided by small shunting resistance judiciously distributed across the gate-cathode junction. Shunts cannot be used with the GATT device since the gate-assist voltage would be effectively "shunted out" by the low impedance paths.

All test devices supported an exponential 400 volts per microsecond transient at stud temperature of 100°C. The amplitude of the transient was 600 volts, and the gate bias condition was as prescribed. No devices turned-on to indicate inability to tolerate a transient, and devices were not driven to higher test values to determine excess dv/dt margin since dv/dt tests become progressively more destructive at rates in excess of 400 volts per microsecond. For the GATT units, any device turned-on by voltage transient in excess of 400 volts per microsecond does so destructively. This occurs in a range of values greater than 800 volts per microsecond, but contract delivered devices were not subjected to this extreme transient.

5.2 Dynamic Parameter Test Results

Dynamic test results are those responses occurring for non-equilibrium junction conditions and basically originate when a change of device state occurs. Turn-on conditions involving a change of state from off to on, and turn-off conditions, involving the reverse condition, are considered dynamic. In both cases, current densities are changing either up or down, seriously affecting device response. Also, related factors, such as rate of change of current, magnitude of current, and gate drive have large influences.

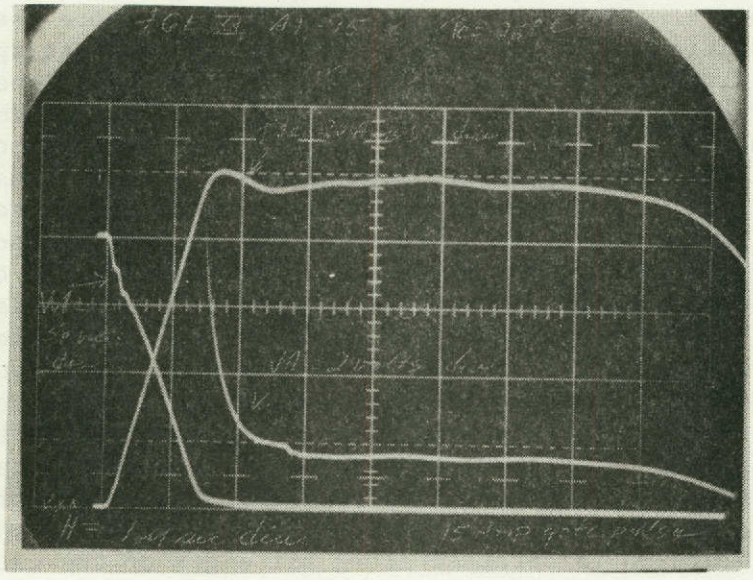
5.2.1 Turn-on Test Results

The turn-on test specification was initially two microseconds, with turn-on defined as "the time required to reach V_{TM} after initiation of current conduction with rate-of-rise of 100 amperes per microsecond and application of a gate signal of 2.5 amperes for two (2) microseconds". Conducting forward drop is defined as not more than two volts for conduction of 100 amperes. This particular test specification is more stringent than most standard thyristor test specifications in that by definition, it demands 100% turn-on of the test device in two microseconds. Although more stringent, the specification is also very precise. This is compared to most thyristor definitions of turn-on time which require measurement of an anode switching voltage fall time between 10% and 90% of the switched voltage, and into some unspecified rate of rise of load current. In most cases, the thyristor relationship between dynamic forward drop and conducting area is ignored, as well as the relationship of anode voltage fall time to rate of rise of current. Hence, standard definitions are somewhat confusing. The GATT turn-on time definition circumvents this confusion by not considering the interim periods of the dynamic switching event, but only the end points; i.e. to measure the time between start of switching and the achievement of complete conduction. By computation, it is possible to show that achievement of the desired switching speed is possible if turn-on is obtained along all edges of the cathode periphery. By measurement, it is shown that the turn-on specification has been attained; however, the gate signal required for two microsecond turn-on must be increased to 15 amperes or more.

Dynamic turn-on measurements have been made with a specially designed system. The main problem is that of observing a signal of several volts after anode voltage decreases from a level of 200 volts in but a few microseconds. All oscilloscope pre-amplifiers, when set to view deflection factors of several volts per dimension, are driven hard into saturation by the initial switching level of several hundred volts. The general amplified recovery from the overdriven condition could require 100 microseconds, thereby making it impossible to measure a small voltage only two microseconds after the thyristor switches. A single pre-amplifier made by Tektronix recovers from the overdriven condition in 150 nanoseconds; this is the Type 1A5 unit. When used with recommended oscilloscopes, adequate response is present to overcome the dynamic conducting voltage measurement problems.

Typical sample measurements are shown in Figures 41 and 42. Anode current is presented for one deflection factor, and anode voltage is shown for two. The zero level for all measurements is the bottom graticule. Anode current is developed from a 200 volt signal formed by discharging a one ohm PFN into a one ohm resistive load. (See Section 3.2 for test circuit description). The circuit speed has been proven to be at least two hundred amperes per microsecond or at least 0.5 microsecond rise time. The response of Figure 41 was generated by

Switching Transient Anode Voltage and Current vs
Gate Drive, Device A1-15

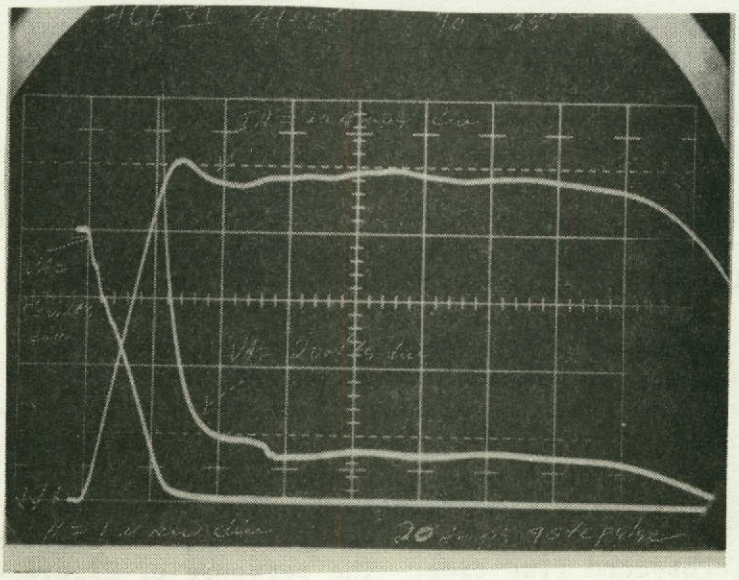


Anode Current
20 amperes/div

Anode Voltage
50 volts/div;
2 volts/div

Peak Gate Drive - 15 amperes

Figure 41



Anode Current
20 amperes/div

Anode Voltage
50 volts/div;
2 volts/div

Peak Gate Drive - 30 amperes

Figure 42

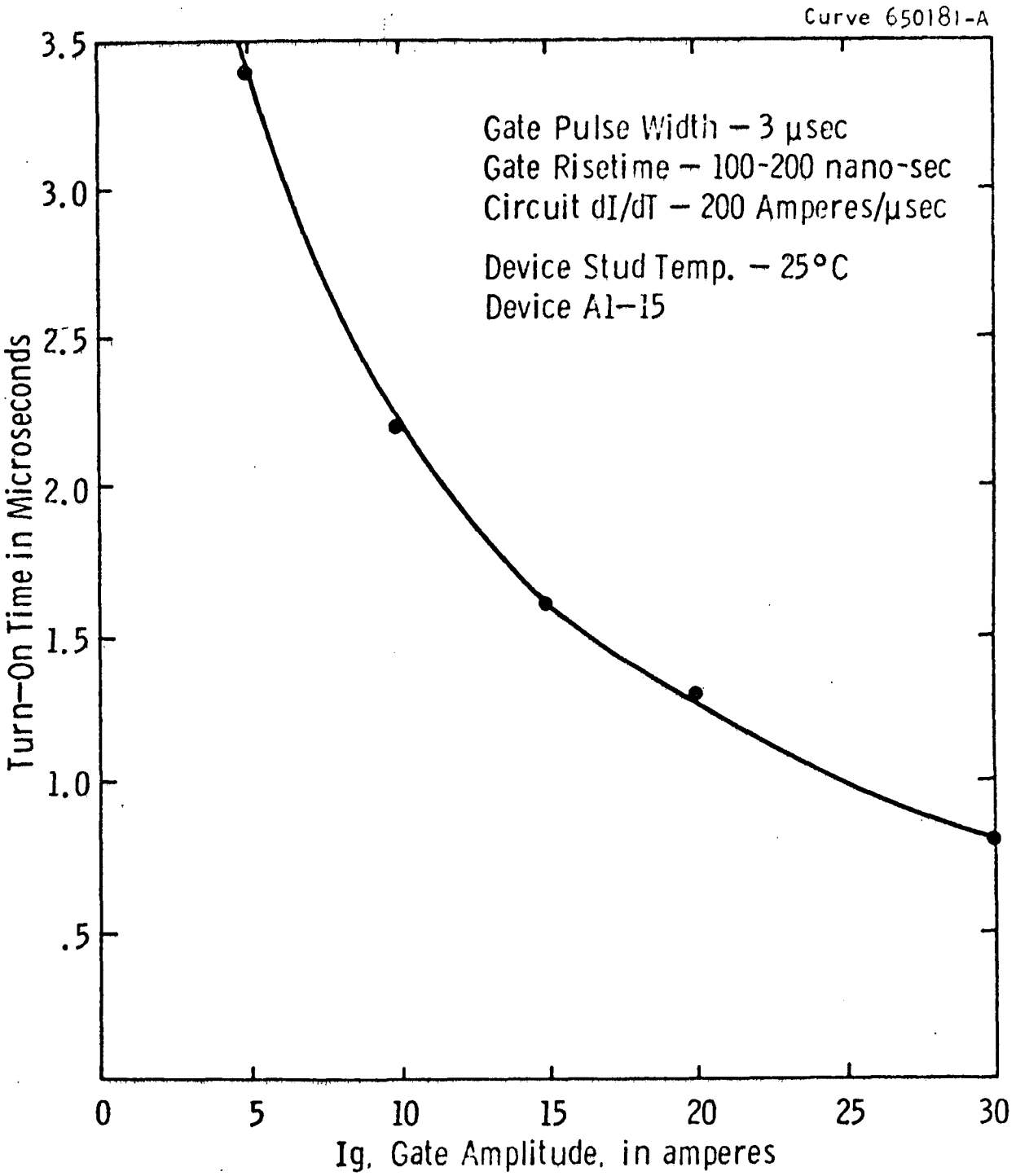
5.2.1 Turn-on Test Results (Cont.)

driving the gate with a three microsecond long gate pulse of 15 amperes peak and 150 nanosecond risetime. The response of Figure 42 was generated by driving the gate with a three microsecond gate pulse of 20 amperes peak and 175 nanosecond risetime. The figures show anode voltage fall and anode current rise at deflection factors of 50 volts per division and 20 amperes per division, respectively. In addition, anode voltage is shown for an expanded vertical deflection factor of two volts per division, with the same timing as the low deflection factor anode voltage response. For the two volts per division scope deflection factor signal, it can be assumed that the response is obtained within 0.15 microsecond after the anode voltage signal passes below 12 volts, or within the linear non-saturated range of the Type 1A5 pre-amplifier. In Figure 41, several features of the response are shown at once. 1) The linear anode voltage fall time, equal to the current rise time, is 1.6 microseconds. Since it is known that circuit rise time is at least 0.5 microseconds, the device under test is limiting the current. 2) Under device limiting, the anode current rate of rise, or "let through di/dt" may be measured to be 70 amperes per microsecond. 3) Anode voltage falls to the two volt level in 2.5 microseconds. The same responses are repeated in Figure 42 for a peak gate drive of 20 amperes with all other conditions remaining the same. As a result, linear anode voltage falltime, equal to current rise time, decreases. Device limiting still exists, but let through di/dt increases to 90 amperes per microsecond. Also, a two volt forward drop is achieved in 1.8 microseconds. The second figure shows the definite benefits of increased gate drive. Other data points for this same device of the previous two figures were taken, and there results are shown graphically in Figure 43. Also, Figure 44 shows linear voltage fall time, also equal to anode current rise time to 100 amperes, as a function of peak gate drive current. The parameter relationship appears to be an inverse one, such as $t_{on} = K/I_g$ with rate of change of turn-on time decreasing for higher and higher drives. A diminishing returns effect become obvious. Figure 44 shows let through di/dt as a function of peak gate current, and here the functional relation is linear. This follows from the aforementioned expression for t_{on} since in the case of device limiting, it can be said that

$$\frac{di}{dt} = \frac{I_{peak}}{t_{on}} \qquad (3)$$

Substituting for turn-on yields

$$\frac{di}{dt} = \frac{I_{(peak)}}{K} \times (I_g) \qquad (4)$$



Turn-on time vs gate drive amplitude

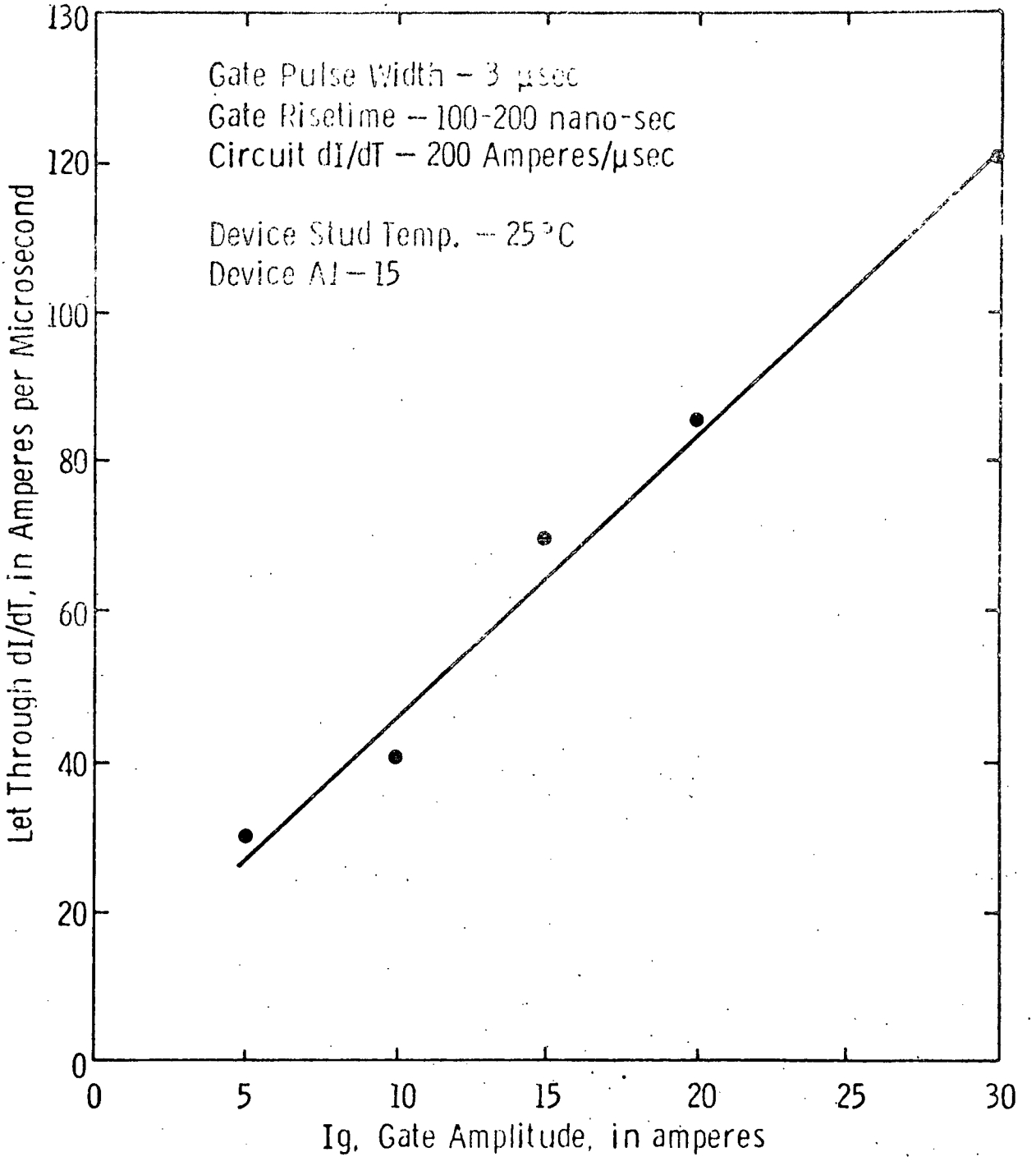
Figure 43

Brewster

c. - m.m. 12/12/72

Curve 650181

Curve 650182-A



Let through dI/dT vs gate drive amplitude

Figure 44

rewster
- m.m. 12/12/72

Curve 650182-A

5.2.1 Turn on Test Results (Cont.)

Continuing the development, the relationship between switching losses and switching speed is obtained. For linear voltage fall and linear current rise (device limiting), switching power is: given by

$$P_{sw} = \frac{1}{6} (E_{peak}) (I_{peak}) \quad (5)$$

and switching energy is: given by

$$E_{sw} = \frac{1}{6} (E_{peak}) (I_{peak}) (t_{on}) \quad (6)$$

Hence power dissipation rate remains constant regardless of switching time, but energy loss is directly related to speed. These energy relationships apply only for the unique circumstances shown in Figure 43 to 44. These are all device limiting conditions and produce the largest possible switching loss conditions. Switching GATT devices at less than device limiting levels results in lower switching losses. This reduction is a function of di/dt.

All devices were given turn-on tests according to the conditions of Figure 41. These results are presented in tabular form at the end of this section. The turn-on time data represents time measurements of points at which dynamic anode voltage crosses through the two volt level, measured from initiation of turn-on. Although some readings exceed the two microsecond specified turn-on time, the dynamic V_{TM} can be shown to be within 2% of switched voltage within the specified turn-on time. This is presumed well within the accuracy limitations of the Type 1A5 pre-amplified accuracy limitations.

Additional measurements were made at stud temperatures of 100°C. These tests show that switching speed changes with temperature are insignificant.

One additional turn-on test not covered by the standard turn-on test circuit composed of PFN and one ohm load resistor is that which shows turn-on performance as circuit speed increases. The circuit speed may be expressed as a di/dt, or that which would exist if rise time were uninhibited by the circuit switch. This was done for some different ultra-fast switches such that a circuit rise time was known before use with a typical GATT switch. Then the GATT is used to switch a preselected circuit speed, and the anode voltage and current response is measured. Under these conditions, the measured current response may not be that of the original current rate-of-rise determination. This indicates onset of device current limiting. A typical series of such responses is shown in Figure 45 to Figure 50. The gate drive for the photographs is that recommended for the GATT, 15 amperes for three microseconds duration, and 150 nanoseconds rate of rise. As

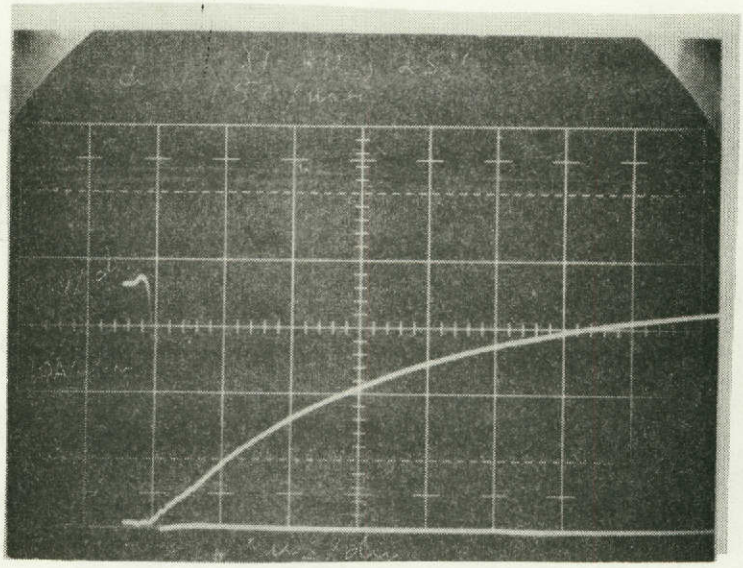


Figure 46

Anode Voltage
200 volts/div

Anode Current
10 amperes/div

Hor. - .5 μs/div

Circuit $\frac{di}{dt}$

15 A/μs

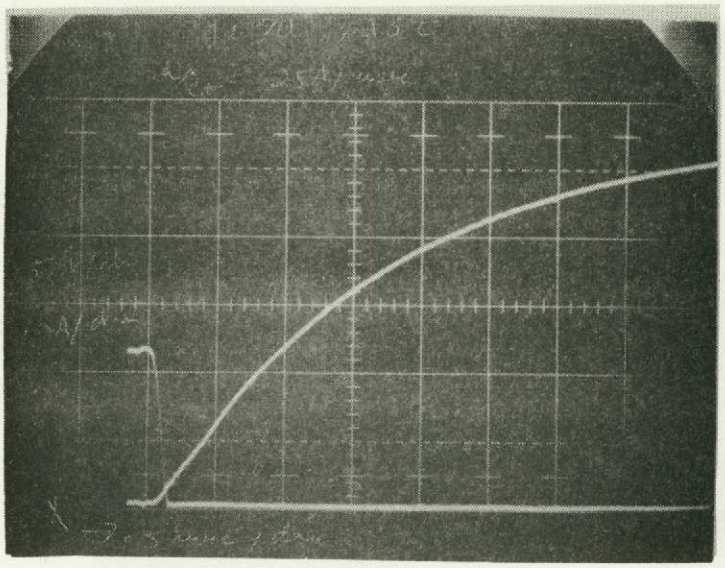


Figure 46

Anode Voltage
50 volts/div

Anode Current
10 amperes/div

Hor. - .5 μs/div

Circuit $\frac{di}{dt}$

25 A/μs

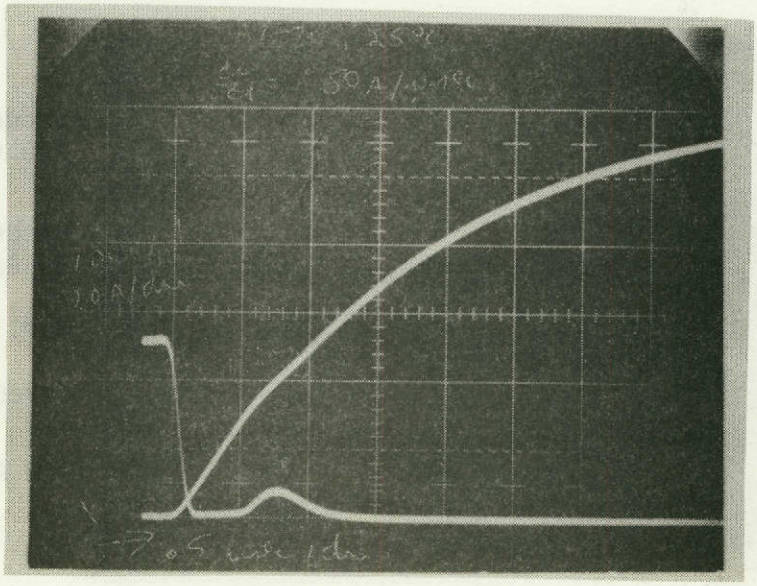


Figure 47

Anode Voltage
100 volts/div

Anode Current
20 amperes/div

Hor. - .5 μs/div

Circuit $\frac{di}{dt}$

50 A/μs

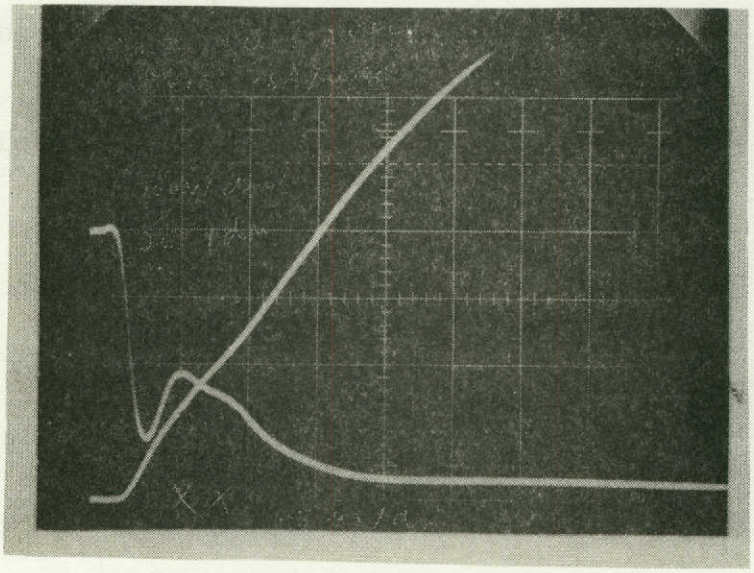


Figure 48

Anode Voltage
100 volts/div

Anode Current
20 amperes/div

Hor. - .5 μs/div

Circuit $\frac{di}{dt}$

75 A/μs

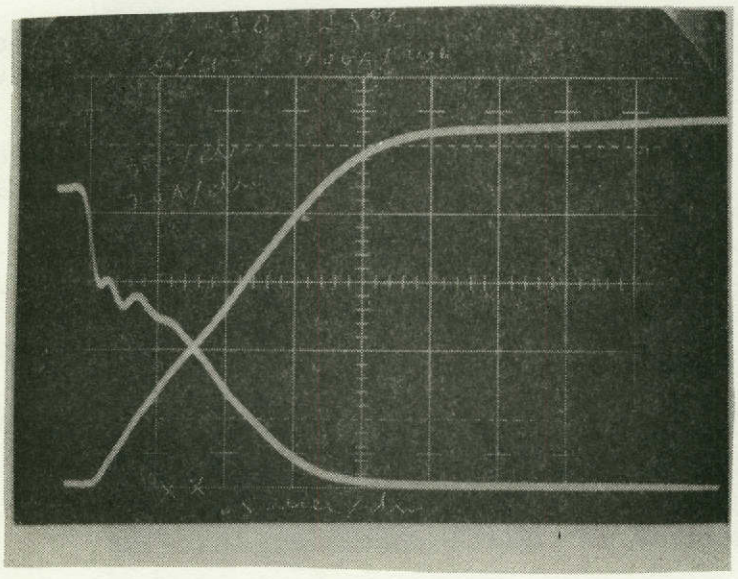


Figure 49

Anode Voltage
50 volts/div

Anode Current
20 amperes/div

Hor. - .5 μs/div

Circuit $\frac{di}{dt}$

100 A/μs

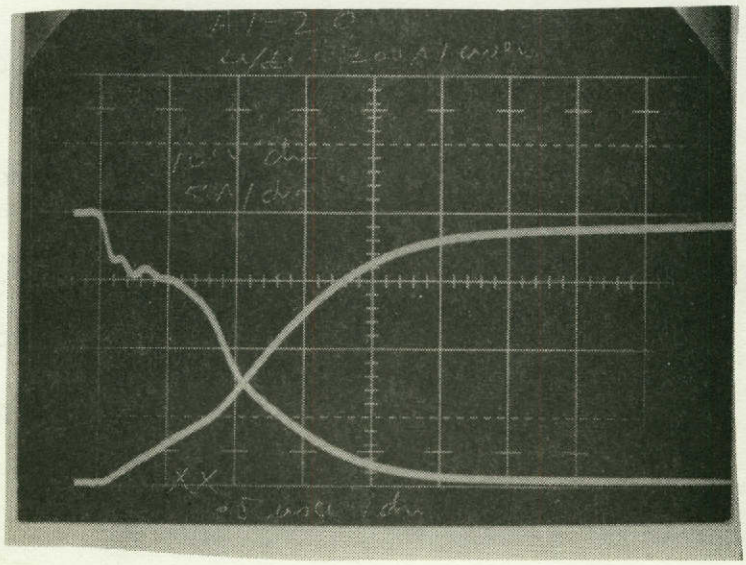


Figure 50

Anode Voltage
100 volts/div

Anode Current
50 A/div

Hor. - .5 μs/div

Circuit $\frac{di}{dt}$

200 A/μs

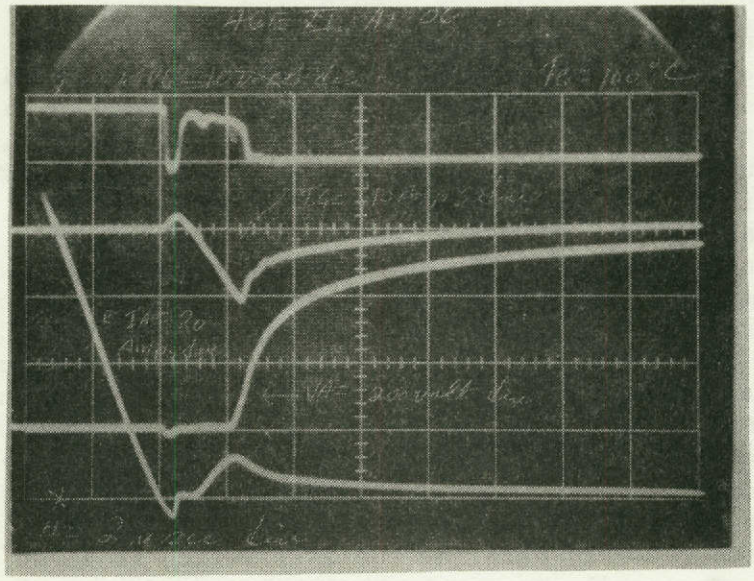
5.2.1 Turn on Test Results (Cont.)

circuit rate of rise increases, some difficulty begins to appear in Figure 47. This becomes more pronounced in Figure 48, where the circuit rate of rise of 75 amperes per microsecond has been reduced by the device speed to only 50 amperes per microsecond. For the highest circuit di/dt of 200 amperes per microsecond, the current limiting action is most significant allowing only 75 amperes per microsecond. The device under test for this series was A1-20.

5.2.2 Turn Off Test Results

Maximum contracted turn off time of two microseconds is defined as "the maximum time after the anode current has reached zero before anode voltage can be reapplied at the maximum rate of rise of 400 volts per microsecond". This is to occur at 100°C stud temperature. The specification is achieved by forcing a conductive anode current of 100 amperes, and after current is well established and "on" equilibrium is established, current is forced to decay at the rate of minus 25 amperes per microsecond. After current passes through zero, reapplied voltage, rising to 600 volts, is applied at the 400 volt per microsecond rate within two microseconds. To assist the forward blocking recovery, a gate assist voltage is switched across the gate cathode at the current zero period. The gate assist voltage is minus 20 volts, with source impedance much less than 1 ohm. A typical response, showing several GATT response functions simultaneously, is shown in Figure 51 The functions are (from top to bottom) gate voltage, gate current, anode voltage, and anode current. All the variables are time coincident. As anode current decreases to zero, the gate assist transistor switch is turned on at the point of zero crossing. A small reverse recovery current is shown; this previously explained in Section 3.3 to be due to the reverse recovery of the isolation diode, rather than the GATT device. Reverse recovery data for the GATT switch is given in the next section. The small reverse recovery current does avalanche the gate-cathode junction, since reverse current flows through the switch from cathode to anode. In this case, the reverse current drives the gate more negative than the gate assist supply, actually forcing some current into the gate for an instant. After the reverse recovery interval ends, reapplied voltage is applied to the device under test. The open circuit reapplied voltage rises only 0.4 microsecond after reverse current recovery, but is not supported by the anode immediately because the anode has not achieved forward blocking junction recovery. The reapplied voltage does promote a current flow into the anode and out of the gate, and this current is the forward junction recovery current. The flow of recovery current forces the negative gate voltage to increase towards zero and actually prevents the anode voltage from rising.

GATT Turn-Off Time Response Showing 2 μsec
Recovery Time with Gate Assist



Gate Voltage
10 volts/div

Gate Current
10 amperes/div

Anode Voltage
200 volts/div

Anode Current
20 amperes/div

Figure 51

C2

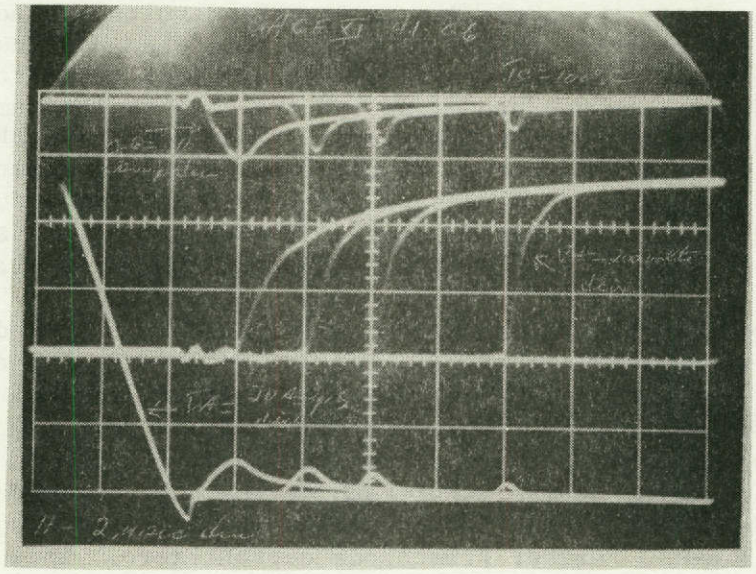
5.2.2 Turn off Test Results (Cont.)

The current into the anode due to reapplied voltage reaches a 10 ampere peak, and is plainly visible in Figure 51. When peak current is reached, the device begins to support reapplied voltage; thereafter, a tail current flows into the anode and out the gate at the same time anode voltage rises to full blocking level. The forward blocking junction recovery is nearly identical to the familiar reverse junction recovery process. Gate assist voltage is maintained until the duration of the reapplied voltage transient decays. Thereafter, bias is present across the gate as long as the GATT device blocks forward voltage.

The information present in Figure 51 is further expanded in Figure 52, but gate voltage is not shown. The new information is obtained by photographing various instants of reapplied voltage, including the minimum. It is then possible to observe the decrease in recovery current, either that flowing into the anode or out the gate. Figure 53 repeats this test for a second device. For each device, the forward junction recovery current decreases in peak and duration as the incidence of reapplied voltage is moved further from anode current zero. This phenomena is characteristic of carrier lifetime effects. As time progresses from current extinction, larger numbers of carriers are annihilated by recombination and less are available to be swept out as charge in the sweep out current. By ten microseconds after current zero, the charge available from forward sweep out appears equal to that available from reverse current sweep out. As has been mentioned, the reverse recovery current of Figures 51 to 53 is dependent upon the recovery characteristics of the isolation diode in series with the test device. The isolation diode was specially processed for very fast reverse recovery, without regard for balanced characteristics otherwise. Reverse recovery characteristics of the GATT switch are presented in the next section. The turn off characteristics of the remaining switches, all similar to those of the photographs are presented in the tabulated data section.

The test conditions of the photographic data of turn-off response must include the fact that the turn off conditions were sustained at low pulse rate. Average heating effects due to forward junction recovery were small, but the loss factors obvious in Figures 51 to 53 are not small. Afterforward recovery, several amperes flows into the anode while the device supports a blocking voltage of 600 volts. The decay of forward recovery current occurs in six to eight microseconds, such that 600 to 1200 watts are dissipated for that interval of time if the forward supply voltage is 600 volts. A dissipation of this magnitude will have heavy impact upon derating at ultra-high pulse operating rates.

GATT Turn-Off Time Response Showing Variation of
Forward Recovery Current With Recovery Time

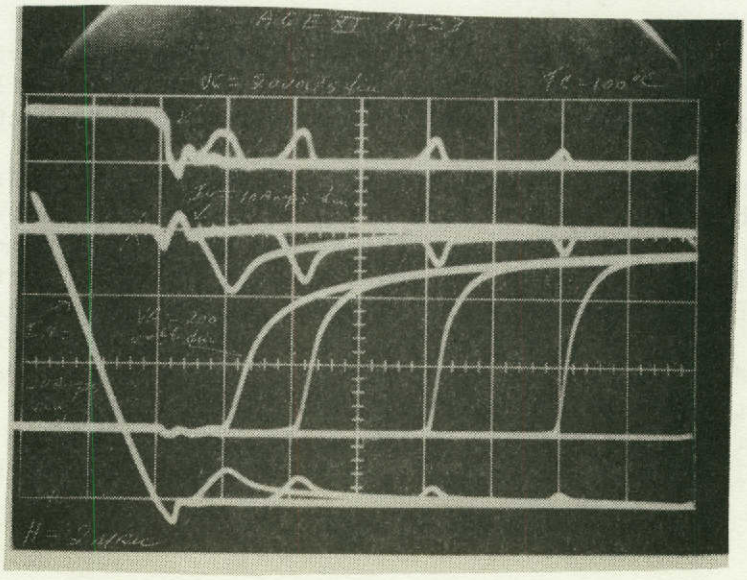


Gate Current
10 amperes/div

Anode Voltage
200 volts/div

Anode Current
20 amperes/div

Figure 52



Gate Voltage
20 volts/div

Gate Current
10 amperes/div

Gate Voltage
200 volts/div

Anode Current
20 amperes/div

Figure 53

5.2.2 Turn off Test Results (Cont.)

As a concluding comparison of turn-off, it is possible to measure turn-off time with an allowed reverse recovery current near equal to that normally seen by the test device. Under normal test conditions, a fast isolation diode is used in series with the test unit to isolate the forward current generating loop from the reapplied voltage loop. The reapplied voltage loop may be made high impedance and the turn-off test can be non-destructive. To measure turn off times near two microseconds, an isolation diode is used which isolates the high current supply from the reapplied voltage in about 0.5 microsecond. This allows a turn-off time measurement down to the two microsecond level, but does not indicate true response under normal sweep out conditions. An example of a single device recovering forward blocking when using a fast isolation diode is shown in Figures 54 and 55. The variables shown are anode current just decaying to zero from 100 amperes at -25 amperes per microsecond, and reapplied anode voltage recovering in four microseconds in Figure 54 and recovering in two microseconds in Figure 55 The reapplied signal rises at the rate of at least 400 volts per microsecond to 600 volts. A turn-off time test is also shown in Figure 56 under the same test conditions, but with reverse recovery current about equal to the normal recovery current of the device under test.

It is clear that forward blocking recovery cannot occur in two microseconds because the reverse junction recovery is at least this long. The turn-off time recovery is shown at a reasonable four microseconds. One obvious feature of this action is that the rise of forward anode voltage actually begins about 0.5 microseconds at the source before it rises across the anode of the test device. During this time, the anode is conductive, and forward recovery current flows until it peaks, at which time forward blocking junction recovery occurs, and anode voltage rises in a positive direction. The rate of rise of forward recovery current is determined by the reapplied voltage source impedance. As with reverse recovery, the simultaneous incidence of forward recovery current and voltage is lossy, and subjects the device to high dissipation for short time periods. Excessively low reapplied source impedance will cause the forward junction recovery to be faster, with a greater peak recovery current than in Figure 56. The coincidence of high peak recovery current and reapplied forward blocking voltage will cause device failure.

5.2.3 Reverse Recovery Measurements

All devices were given tests to determine the character of the reverse recovery current. These tests were made at 25°C and at 100°C. Each device was tested when anode current decayed from 100 amperes at the rate of 5, 12.5, and 25 amperes per microsecond.

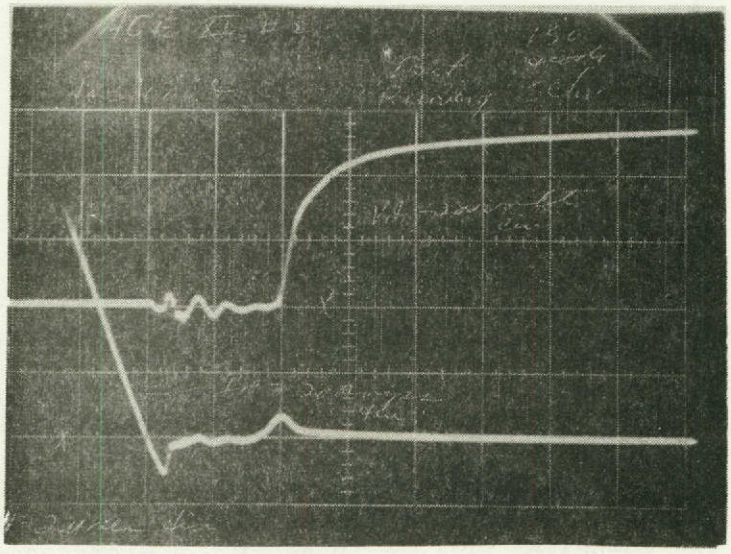


Figure 54

Anode Voltage
200 volts/div

Anode Current
20 amperes/div

Hor. - 2 μs/div

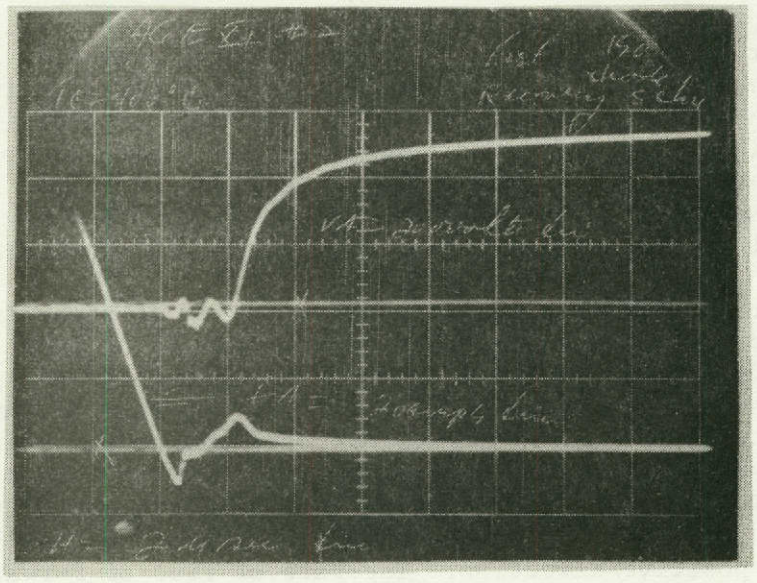


Figure 55

Anode Voltage
200 volts/div

Anode Current
20 amperes/div

Hor. - 2 μs/div

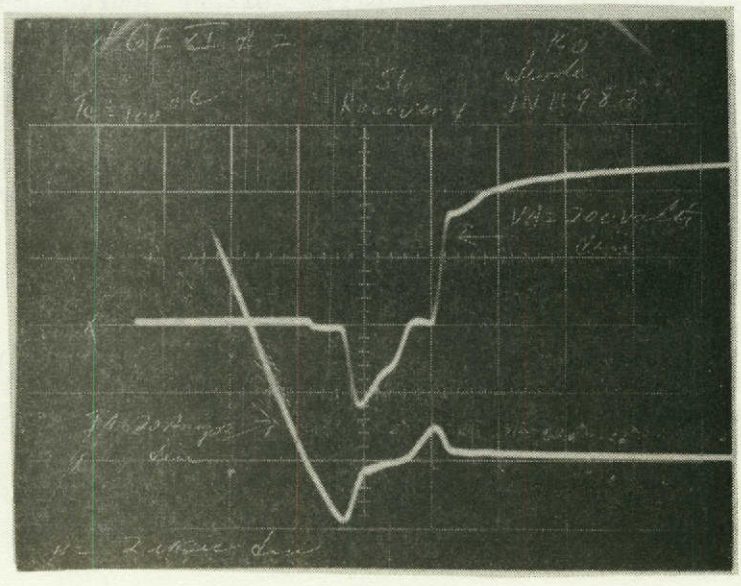


Figure 56

Anode Voltage
200 volts/div

Anode Current
20 ampers/div

Hor. - 2 μs/div

5.2.3 Reverse Recovery Measurements (Cont.)

Three parameters were measured:

1) I_{RP} - Peak reverse recovery current.
2) t_{rp} - Time in microseconds to reach I_{RP} from current zero.
3) t_{rr} - Reverse recovery time measured from current zero to decaying value of 10% of I_{RP}.

Test results are very similar and data of several sample units are given in Table 7 and 8 to show the typical trends.

	$-di/dt = 12.5\ A/\mu s$			$-di/dt = 25A/\mu s$		
Device	I_{RP} Amps	t_{rp} Microseconds	t_{rr} Microseconds	I_{RP} Amps	t_{rp} Microseconds	t_{rr} Microseconds
A1-05*	10	1.2	1.6	20	1.1	1.6
A2-03	9.0	1.2	1.6	20	1.2	1.6
B1-06	10	1.4	2.0	22	1.3	1.9
B3-12	9.0	1.2	1.7	19	1.0	1.6

Reverse Recovery Data (25°C)

Table 7

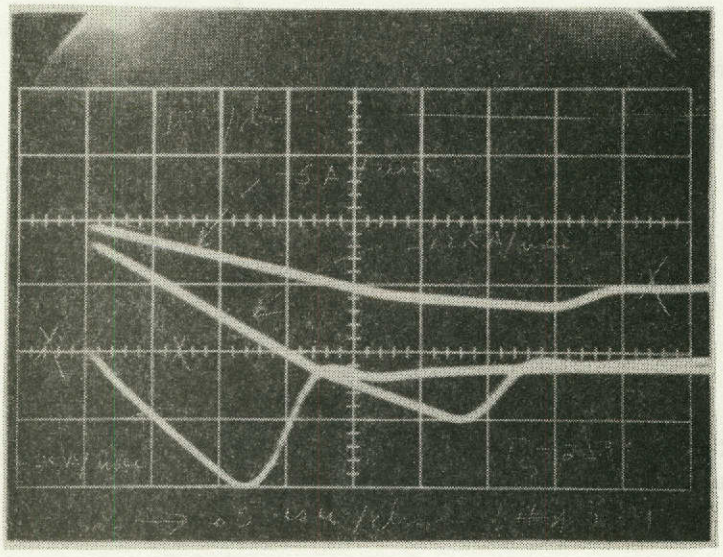
	$-di/dt = 12.5A/\mu s$			$-di/dt = 25A/\mu s$		
Device	I_{RP} Amps	t_{rp} Microseconds	t_{rr} Microseconds	I_{RP} Amps	t_{rp} Microseconds	t_{rr} Microseconds
A1-05*	13	1.8	2.6	26	1.5	2.3
A2-03	12	1.6	2.3	24	1.4	2.2
B1-06	14	2.0	2.8	28	1.7	2.5
B3-12	12	1.6	2.4	25	1.4	2.2

Reverse Recovery Data (100°C)

Table 8

Several photographs of reverse recovery for device A3-01 are shown in Figures 57 and 58. Reverse recovery is shown at 25°C in Figure 57 and at 100°C in Figure 58. An increase of swept out charge is obvious at higher temperature.

Reverse Recovery Response, Device A3-01

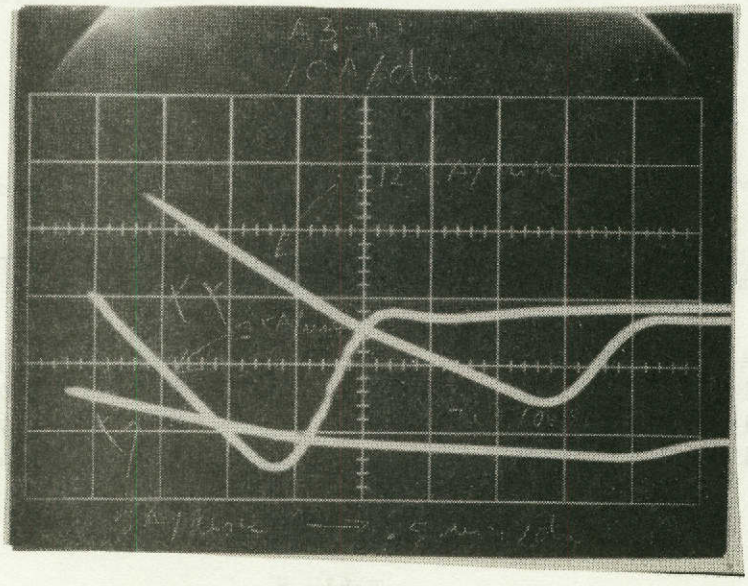


← zero

← zero

Figure 57. T_C = 25°C

$-\frac{di}{dt}$ = 5 A/μs, 12.5 A/μs, 25 A/μsec



← zero

← zero

Figure 58. T_C = 100°C

$-\frac{di}{dt}$ = 5 A/μs, 12.5 A/μs, 25 A/μs

5.3 Final Device Sample Parameters

Data of the fifty (50) final device samples delivered to NASA are tabulated in Table 9. Preceding sections have detailed the test conditions and techniques which prevailed in performing the various parameter measurements.

The incomplete data noted for Nos. 1 - 4 was the result of a need to deliver four 'best effort' devices on short notice early in the pilot production activity. Time did not permit a complete characterization.

I was recognized that the unique balance of static and dynamic characteristics of the GATT II devices might give rise to improper application by circuit design engineers unfamiliar with this class of solid state switch. Ergo, an application note was devised which provides some basic guidelines for use of the device. The appendix, GATT II Application Note, presents the information.

NO		V_{DRM} (1) (volt) 25°C	V_{DRM} (1) (volt) 100°C	V_{RRM} (1) (volt) 25°C	V_{RRM} (1) (volt) 100°C	V_{TM} (2) (volt) 25°C	I_{GT} (ma) 25°C	V_{GT} (volt) 25°C	I_H (ma) 25°C	I_L (A) 25°C	V_{RG} (volt) 25°C	I_{RG} (ma) 25°C	t_{on} (3) (μs) 25°C	t_{off} (4) (μs) 100°C	
1	6	1050	1100	1150	1300	<2.0							3.1	4	
2	7	1000	1100	1150	1200	<2.0							25	2	
3	9	1100	1200	1100	1150	<2.0							4.6	4	
4	17	1100	1200	1200	1300	<2.0							3.2	3	
5	A1-05*	1000	1100	1000	1210	1.78	310	0.70	150	7.2	20	700	3.2	2.0	
6	A1-06*	1000	1150	1200	1120	1.64	350	0.70	120	7.1	20	270	3.3	2.0	
7	A1-18	1020	1050	1150	1220	1.80	400	0.90	96	0.4	20	400	2.8	2.0	
8	A1-20	950	1040	980	1090	2.12	900	1.0	154	7.0	20	1500	2.8	2.0	
9	A1-21	900	1000	940	1000	1.90	420	0.85	160	5.2	20	900	2.8	2.0	
10	A1-23	920	1060	1080	1180	1.72	400	0.90	130	5.2	21	500	2.8	2.0	
11	A1-24	920	1020	980	1040	1.68	300	0.85	100	4.8	22	1000	2.4	3.0	
12	A1-25	1080	1120	920	840	1.40	50	0.75	700	0.8	20	600	2.0	2.0	
13	A1-26	1000	1050	1160	400	2.16	1100	0.90	160	8.0	20	400	3.0	2.0	
14	A2-01	1000	1100	1080	820	1.76	410	0.85	100	6.2	20	500	3.0	2.0	
15	A2-02	920	1000	500	400	1.96	800	0.85	300	6.2	20	2000	3.3	2.0	
16	A2-03	960	1040	930	1020	1.96	620	0.85	130	5.2	20	300	5.0	2.0	
17	A2-05	900	960	1040	760	1.96	800	0.90	70	5.0	21	500	3.0	2.0	
18	A2-07	1060	1140	1040	720	1.80	700	1.0	90	7.2	20	900	3.0	2.0	
19	A3-01	1080	1100	1120	1180	1.64	300	0.85	168	4.1	21	1300	2.5	2.0	
20	A3-02	1080	1100	1020	1100	1.68	330	0.85	80	4.2	20	350	2.8	2.0	
21	B1-02	980	1040	480	400	1.68	600	0.80	115	8.5	20	110	3.0	2.0	
22	B1-04	960	1040	1040	1140	1.80	500	0.90	310	7.2	19	1100	3.5	2.0	
23	B1-04*	900	1060	1000	580	2.00	1200	0.90	320	10.4	20	3000	6.0	2.0	
24	B1-05*	1000	1180	1000	1160	1.68	280	0.65	210	7.6	20	1200	3.0	3.0	
25	B1-06	920	980	1040	1130	1.68	380	0.85	140	7.6	19	190	3.2	2.5	

(1) $I_R = I_{RRM}$ 10 ma (2) T =100 A (3) to 100 A (4) 100 v/μ to 600 v t 100 25v/μ d

Table 9 (Cont.)

DELIVERABLE ITMES

NO		V_{DRM} (1) (volt) 25°C	V_{DRM} (1) (volt) 100°C	V_{RRM} (1) (volt) 25°C	V_{RRM} (1) (volt) 100°C	V_{TM} (2) (volt) 25°C	I_{GT} (ma) 25°C	V_{GT} (volt) 25°C	I_H (ma) 25°C	I_L (A) 25°C	V_{RG} (volt) 25°C	I_{RG} (ma) 25°C	t_{on} (3) (µs) 25°C	t_{off} (4) (µs) 100°C
26	B1-07*	900	960	1000	1120	1.52	120	0.60	140	5.8	20	140	3.2	4.0
27	B1-08*	1000	1120	1000	1140	1.60	360	0.60	200	7.0	20	1000	3.2	3.0
28	B2-02*	1000	1080	1000	1100	2.04	1400	0.70	500	11.4	19	620	8.0	2.0
29	B2-04	950	1040	1000	1100	1.80	1500	0.90	180	11.0	20	300	3.6	2.0
30	B2-05	940	1040	1100	1200	2.00	1200	1.0	200	12.0	20	600	4.0	3.0
31	B2-06*	1000	1170	1000	1160	1.84	800	0.65	220	11.0	19	830	8.0	3.0
32	B2-08	960	1060	1000	1080	2.16	1300	1.0	200	9.0	20	1200	4.5	2.0
33	B2-11	1040	1140	900	980	2.24	1200	1.3	220	8.6	19	320	4.5	2.0
34	B3-03	1030	1120	1060	1160	1.80	600	0.90	200	6.1	20	2000	3.2	2.5
35	B3-08	1000	1080	1090	1180	2.04	1200	1.0	380	12.5	20	1500	3.2	2.0
36	B3-09	1040	1210	1130	1320	1.44	1200	0.80	180	3.4	20	1500	2.3	2.5
37	B3-12	1060	960	1160	1030	1.90	700	0.90	200	6.2	20	1800	45	2.0
38	G6-42	1000	1000	1000	1060	1.50	50	0.70	620	0.7	20	800	2.5	3.0
39	G6-63	1000	1040	980	1000	1.70	50	0.70	100	2.0	19	600	2.6	3.0
40	G4-18	1040	1160	1080	1160	2.15	300	0.90	220	5.6	21	2000	2.8	3.8
41	A90-6	1000	1060	1080	1090	3.10	1600	1.0	240	10.4	20	790	3.0	3.0
42	G6-18	1000	1100	960	1020	2.30	650	0.90	100	9.8	20	20	2.6	3.4
43	NO-1	920	1000	1000	1070	2.38	500	0.80	160	4.2	21	1500	2.6	3.5
44	G4-12	1000	1120	1120	1240	1.85	500	0.90	160	6.0	21	700	3.0	3.6
45	G4-20	1100	1200	1120	1200	2.15	1200	1.0	250	7.3	20	1000	3.0	3.8
46	NO-2	980	1010	1000	1000	2.20	1100	0.90	140	9.0	22	900	3.0	2.0
47	NO-5	1040	1100	1090	1000		1500	1.0	220	13.6	21	700	3.0	2.0
48	NO-11	1030	1120	1090	1160	2.00	750	1.4	200	12.4	20	600	3.0	2.1
49	NO-14	1090	1150	1000	920	1.62	380	1.0	240	7.0	21	1200	2.8	2.0
50	NO-18	1040	1160	800	920	1.83	500	12	115	8.2	21	350	2.9	2.0

(1) $I_{TV}=I_{RM}$ 10 ma (2) I_{TM}=100 A (3) to 100 A (4) 400 v/µs to 600 v at 100 A, -25A/µs decay

VI. CONCLUSIONS AND RECOMMENDATIONS

The basic performance objective outlined for this contract effort was met in that the ability to produce an increased voltage (600 volts to 1000 volts), higher current (50A to 100A) gate assisted turn-off thyristor while maintaining forward drop and turn-off time at equivalent levels was demonstrated. Of equal importance, the objective to improve the fabrication/processing technology was met as evidenced by the introduction of the planar passivated cathode gate structure in conjunction with the contact preform/pressure encapsulation package.

In the course of the Phase I development, it became apparent that the fast turn-off capability which characterized GATT II devices was attained at some expense of turn-on convenience. The trade-off was mutually recognized by Westinghouse and NASA. Table 10 is a succinct presentation of actual test data. This was recorded for the same group of devices under, first, the condition of high lifetime yielding the "standard speed" set of characteristics and, second, the condition of low lifetime, yielding the "fast switch" set of characteristics.

	Fast Switch	Standard Speed
V_{DRM}/V_{RRM}	1000V	1000V
I_{GT}	0.5 to 1.0A	< 100 ma
I_H	100 to 200 ma	< 100 ma
I_L	5 to 10A	< 100 ma
V_{TM}	1.7 to 2.0V	1.1 to 1.3V
t_{on} time	3μs to 3V	3μs to 2.0V
t_{off} time	< 2μs	12 to 15μs

Fast Switch vs. Standard Speed GATT:
A Comparison of Parameter Trade-Offs

Table 10

Note the increased insensitivity of the fast switch devices for both dynamic turn-on and full-on conditions. I_{GT} and I_H increased about an order of magnitude; I_L increases up to two orders of magnitude; both steady state and dynamic V_{TM} appear to increase about 50%. The benefit received is a decrease in turn-off time of about an order of magnitude. In conclusion, one is faced with the necessity to seek the compromise which best fits the system (application) requirements. The turn-off time in particular, should be carefully scrutinized, and specified as high as possible since one sacrifices considerably in other characteristics if turn-off is required to be very low, of the order of several microseconds.

Recommendations for future development in the area of gate assisted turn-off thyristors should include an in depth study of turn-on. The GATT II requires a minimum 15 ampere gate firing current and fast rise time of 100 ns. Reduction by about an order of magnitude is desired. This obviously involves consideration of, e.g., dynamic gate type structures.

Further recommendations concern the approach to specification of an improved device. If one is to achieve the best balance of device characteristics, it is necessary to exercise as much freedom of choice in the area of parameter trade offs. For example, the specification should give top priority to the frequency and energy loss per cycle. The device design engineer has the option then of trading off switching losses and steady state losses as he see fit - as long as total dissipation does not exceed the specified value.

In summary, further development of GATT II should be performed on structures designed for the same voltage level (one kilovolt). Emphasis should be directed to the area of turn-on and power dissipation. A resolution of these matters should readily permit a scale-up of the device to higher current ratings.

VII. NEW TECHNOLOGY

The principle item of new technology resulting from this work was the demonstration that the contract objectives as defined in Table 5 were feasible. Devices meeting the specification were produced.

A second item of New Technology was the demonstration of the practicability of the composite device structure and configuration of the GATT II. The mating of oxide passivated cathode-gate junctions and cathode contact preform, in the CEE pressure contact encapsulation, was shown to be a viable construction which circumvents some of the objectionable features of the GATT I Device.

Accordingly, a New Technology Reportable Item Report was submitted per contract requirements. The report related specifically to the innovative structure and design features of the GATT II device which yielded the performance specification noted above.

APPENDIX

GATT II APPLICATION NOTE

GATT II APPLICATION NOTE

A. Turn-On Requirements

1. Gate drive: current - 15A
   pulse width - 3μs
   rise time - 150 ns

2. Maximum swtiched circuit speed: 75A/μs

3. Maximum forward current for two (2) microseconds turn-off time - 100A

4. Maximum rate of decay of forward current from 100 amperes for two (2) microseconds turn-off time - -25A/μs

B. Turn-Off Requirements

1. Gate assist source voltage (maximum open circuit) - -20 volts

2. Gate assist source impedance (maximum) - 1 ohm

3. Earliest incidence of gate assist - current zero
   Note: gate assist not to be applied while positive anode current flows

4. Maximum rate of reapplied voltage - 400V/μs

5. Maximum peak forward recovery current - 15A

C. Gate Bias Requirements

1. Source voltage (open circuit) - -10 volts

2. Source impedance - 1 ohm
   Note: gate bias is applied at all times that the gate assisted thyristor is not conducting.

REFERENCES

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3. **Lederhandler and Giacoletto, "Measurement of Minority Carrier Lifetime and Surface Effects in Junction Devices", Proc. I.R.E., vol. 43, pp. 477-483; April, 1955.**