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NASA TECH BRIEF

Marshall Space Flight Center

Error-Correcting Codes for High-Speed Digital Computers

A document has been published which discusses a method for the correction of errors in high-speed digital computers. These errors result from the occasional failures within the computer hardware. According to this method, the computer operation becomes fault-tolerant, i.e., its operation is error-free in spite of a single hardware element malfunction.

A logic circuit operates according to a prescribed matrix to generate a code vector derived from parity bits according to the information bits processed. Each row of the matrix corresponds to one partition of the code vector which, in turn, corresponds to one segment of the hardware. The parity bits are set when the vector is created, to establish even parity for each matrix column. Bit inversions which occur, due to hardware failures, will cause a unique pattern when parity checks are reconstructed, permitting the logic circuit to restore the original vector.

The error corrector circuit may be contained on a single integrated circuit chip. The chip will reconstruct parity, analyze the pattern formed, and correct any erroneous information bits.

Notes:

1. The method provides for the detection and correction of repetitive and spurious processing and transmission errors.
2. Requests for further information may be directed to:
   Technology Utilization Officer
   Marshall Space Flight Center
   Code AT01
   Marshall Space Flight Center, Alabama 35812
   Reference: B74-10147

Patent status:

NASA has decided not to apply for a patent.

Source: R. D. Campbell of
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Category 02