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# NASA TECH BRIEF

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## Advanced-Priority Interrupt Module

The advanced-priority interrupt module (APIM) fabricated on a single wire-wrap circuit board provides minicomputers with an interrupt structure comparable to that found on larger and traditionally more sophisticated computers. The module contains a mask register, a line register, a primary sync register, a secondary sync register, a push-pop stacking register, a control section, and an interrupt address generator. The APIM operates in conjunction with the logic found in the majority of minicomputers to provide fully-vectored interrupt capabilities.

The APIM contains an array of approximately 140 IC's, the majority of which are registers which receive, synchronize, and process the interrupt signals from external sources. The APIM scans the interrupt lines at approximately 900-ns intervals. If signals occur on more than one interrupt line during any 900-ns scan period, the highest priority signal is acknowledged. The remaining interrupt requests are stored in the line register until each has been acknowledged. At the end of each 900-ns period, a request is sent to the control logic which in turn generates a request for an interrupt from the computer. The priority level of a device connected to the interrupt module is determined by channel selection at the time of installation.

The push-pop stacking register of the APIM dynamically stores information that allows the scheduling of interrupts without extensive software overhead. Minimal masking and no enabling or disabling of interrupts are required by the stored software program. An arriving interrupt of high priority causes a lower priority subroutine to cease operations. After the higher level routine is processed, information stored within the stacking logic permits a return to the lower priority subroutine. A lower level interrupt is precluded from interrupting higher priority processing.

The circuit board also includes control logic circuits which vary slightly in format with the make and model of minicomputer. The modification of these circuits will adapt the module to specific minicomputers. Although the module provides 16 levels of priority, the design permits expansion to 128 channels.

### Note:

Requests for further information may be directed to:

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Reference: TSP74-10165

### Patent status:

Title to this invention has been waived under the provisions of the National Aeronautics and Space Act [42 U.S.C. 2457 (f)], to the California Institute of Technology, Pasadena, California 91109.

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Category 02