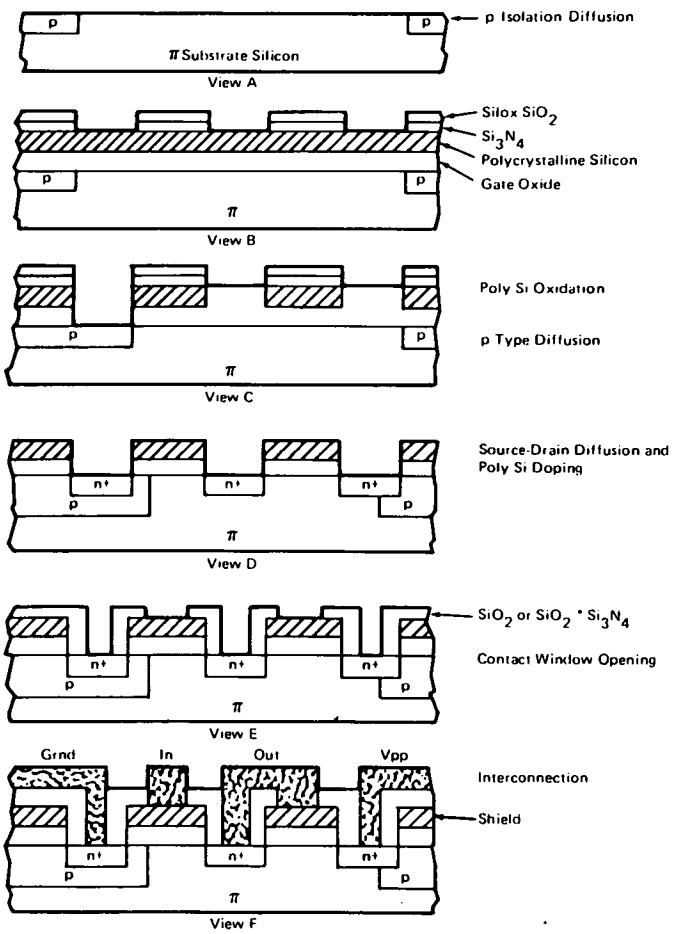
NASA TECH BRIEF

Langley Research Center

A Method for Polycrystalline Silicon Delineation Applicable to a Double-Diffused MOS Transistor

The use of this method permits polycrystalline silicon layers to be delineated into discrete, electrically-isolated areas without removing polysilicon material. Also, an insulating support can connect adjacent thinly isolated areas, forming a smooth substrate for overlying metal interconnect patterns. This method is simple and eliminates the requirement for unreliable special etchants.

The illustration shows the steps used in the fabrication of a double-diffused metal-oxide-silicon (MOS) transistor and integrated circuits. In this case, it is desired to fabricate an enhancement-mode n-channel transistor as the switching device and a depletion transistor as the load device. The enhancement-mode switching transistor is fabricated by diffusing an additional p-type layer into the same window as the n-type source of the switching transistor.



(continued overleaf)

The π-type wafer is first p-diffused for isolation (View A). Gate oxide, polycrystalline silicon, silicon nitride (Si_3N_4), and pyrolytic oxide silox are sequentially grown on the wafer and windows are opened through the silox and Si_3N_4 for the outlines of source and drain (View B). Another photoetching step is exercised to open a window for the first p-diffusion into the source window. During the drive-in step, the exposed polycrystalline silicon becomes oxidized as shown in View C. This oxide layer is thick enough (approximately double the poly-Si thickness) to mask against the next diffusion and can be removed readily by standard oxide etch, such as buffered HF. After the drive-in diffusion, all the oxide on top of the polycrystalline silicon and that covering the drain region is removed and n+ type dopant is diffused into the source and drain regions as shown in View D.

After the fourth masking, the polycrystalline silicon is selectively etched to isolate the gate, leaving the rest of the polycrystalline silicon to serve as an electrostatic shield. Another layer of glass is then grown over the structure. Contact windows are opened in the fifth masking step and, after aluminum evaporation and sintering, the last masking step is applied to delineate the interconnection.

The structure thus fabricated is graded in resistivity to prevent punch-through and has a very narrow channel length to increase the frequency response. The contacts are on the top to permit a planar integrated circuit structure. The polycrystalline shield will prevent the creation of an inversion layer in the isolation region.

Note:

Requests for further information may be directed to:

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Patent status:

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