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BINARY SELECTABLE DETECTOR HOLDOFF CIRCUIT: DESIGN, TESTING, AND APPLICATION

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16. ABSTRACT

A very high speed switching circuit, part of a laser radar data acquisition system, has been designed and tested. The primary function of this circuit was to provide computer controlled switching of photodiode detector preamplifier power supply voltages, typically less than ±20 volts, in approximately 10 nanoseconds. Thus, in actual use, detector and/or detector preamplifier damage can be avoided as a result of sudden extremely large values of backscattered radiation being detected, such as might be due to short range, very thin atmospheric dust layers. Switching of the power supply voltages was chosen over direct switching of the photodoide detector input to the preamplifier, based on system noise considerations. Also, the circuit provides a synchronized trigger pulse output for triggering devices such as the Biomation Model 8100 100MHz analog to digital converter.

A point by point description of the circuit operation is presented, with actual signal waveforms shown. In addition, printed circuit board layouts and a parts listing are given to assist implementation of the circuit by interested individuals.

Finally, further applications of this device are discussed and summarized.

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INTRODUCTION

The application of laser radar systems to the systematic study of the lower atmosphere has been severely hampered by the very large dynamic range of the backscatter signal return. There have been basically two approaches to this problem. The first approach has been to utilize multiple detectors, wherein each detector has a different linear amplifier signal gain factor. The second approach has been to utilize fixed gain logarithmic amplifiers to compress the dynamic range of the returned signal. Although each of these approaches is applicable, neither addresses itself to the problem concerning the overexposure of sensitive detectors to sudden extremely large values of backscattered radiation as might result from short range atmospheric dust layers or low level clouds entering the laser radar field of view. Normally when such a target appears, data acquisition is suspended to prevent detector and/or detector preamplifier damage. Conceivably, the problem of detector and/or detector preamplifier damage might be avoided if the detector system could be "turned off" in the space interval between detector and target. Also, the detector system should be able to be "turned on" only in the space interval between the detector and target. This would allow detailed atmospheric studies up to a cloud base without need for concern of the large signal that would be subsequently returned from the cloud base itself. Thus, the design of a binary selectable detector holdoff circuit was undertaken and successfully accomplished. Figure 1 illustrates the role of this circuit in a laser radar data acquisition scheme. Reference 1 contains a more detailed description of the entire laser radar system concept and application.

The application of a detector holdoff circuit is not restricted only to laser radar. Luminescence phenomena (i.e. gas breakdown due to giant pulse laser-gas interactions) generally has lifetimes in the microsecond range. This circuit could be used to measure the luminescence time history and allow the maximum signal gain to be utilized. For example, by profiling the luminescence time history from end to beginning rather than beginning to end.

CIRCUIT DESCRIPTION

A schematic of the binary selectable detector holdoff circuit is shown in Figures 2 and 3. Basically the circuit functions shown in Figure 4 are as follows:

a) At voltage (V_{cc}) turn on, the circuit is initialized.

b) When a high-low-high (HLH) or low-high-low (LHL) remote in pulse is applied, the $\overline{Q}$ output of the 9601 one-shot integrated circuit (IC1) is triggered. The combination of C_2 and R_2 establishes the longest time delay of the entire circuit to prevent circuit retriggering.

c) Since the $\overline{Q}$ output is a HLH pulse, the second 9601 (IC2) triggers immediately on the HL pulse edge (negative edge triggered). C_s is simply stray capacitance and R_{min} should be chosen to provide an output pulse width greater than 100 nanoseconds. The Q output (LHL) pulse provides the true laser trigger and the $\overline{Q}$ output (HLH) pulse presets one flip flop of the 9S112 (IC3).

d) The 100 nanosecond laser trigger pulse is sent through the hex inverter pairs to provide for a delay of the laser trigger output pulse. Hex inverter pairs are used as delay lines since various speed logic (i.e. 3, 6, 8, 10 or 20 nanosecond chip propagation time) is commercially available. Also, each hex inverter (IC4, IC5 and IC6) contains three hex inverter pairs and thus the maximum delay allowable is a function of the chosen logic speed mix. In this case, 3 IC s or 9 hex inverter pairs were used, thus allowing a delay range of 9[2(3)] = 54 nanoseconds to 9[2(20)] = 360 nanoseconds.

e) When the 9S112 (IC3) is preset, the nand gate clock, i.e. the 9S00 (IC7), is synchronized and clock pulses are passed through the 9S20 four input nand gate (IC8).

f) The clock pulses are counted by dual 93S16 counters (IC9 and IC10). Note, the counters had been reset previously by the initialize pulse. The counters serially count and the counter outputs are being constantly compared to the sense line settings by the 9014 exclusive or (IC11, IC12, IC13 and IC14).

g) When a <u>true</u> comparison is achieved, the resulting 9S20 four input nand gate (IC8) issues a HLH pulse. This HLH pulse presets the second flip flop of the 9S112 and <u>turns on</u> the detector preamplifier power supply switch,

as well as stopping the nand gate clock output, resetting the counters, and initiating the retrigger time delay 9601 one shot IC s.

h) C_3 and R_3 determine the retrigger time delay. This time delay is typically less than half of the C_2 and R_2 combination. The output of this 9601 one shot (IC16) is a Q output, a LHL pulse. Again, on the HL transition, the second 9601 one shot (IC17) is triggered.

i) When the second 9601 one shot is triggered (C_S is stray capacitance and R_{min} is five ohms), the $\overline{Q}$ output, a HLH pulse, resets both flip flops on the 9S112. Thus, following the remote in delay (para b) the entire circuit can be retriggered.

CIRCUIT IMPLEMENTATION

The circuit shown in Figures 2 and 3 was breadboarded to determine operational characteristics. A fast rise pulse generator, operating at a 2000 pulse/second rate, was used as the remote input.

Figure 5 shows synchronization of the laser trigger LHL pulse positive going edge with the positive going edge of the detector preamplifier power supply switch signal. The laser trigger pulse is shown after passing through a delay of seven hex inverter pairs. The power supply switch signal is the output of pin 9 of the 9S112 flip flop. The synchronization was achieved for a sense switch setting of 1 (1 to 256 is possible), which is the minimum setting since a setting of zero creates an ambigious circuit state. As can be seen from Figure 5, synchronization was achieved within 4 nanoseconds for a 10 nanosecond/division time base. Figure 6 indicates the change in synchronization using eight inverter pairs and Figure 7 indicates the change using all nine hex inverter pairs. Figure 8 illustrates, in a multiple exposure, the use of seven, eight, or nine hex inverter pairs as delays. The quality of the delays generated by each set of hex inverter pairs is amazingly uniform. Each pair of hex inverters is thus equivalent to 16 nanoseconds (8 nanosecond logic). Therefore, the total circuit propagation delay is $7(16) \approx 112$ nanoseconds.

Figure 9 illustrates the output of pin 6 of the 9S20, the clock output. The sense switch setting indicated a decimal count of 17 clock pulses, though 18 clock pulses are shown in the figure. This means that one extra clock pulse occurred due to the circuit propagation time delay from the time of the

true comparison and shut off the clock via pin 6 of the 9S20. The second signal (lower trace) in Figure 9 is the remote in trigger pulse. Figure 10 is simply a repeat of Figure 5 for a time base of 100 nanoseconds/division. Figure 10 is shown for comparison to Figures 11 and 12. Figures 11 and 12 are multiple exposures wherein Figure 11 shows sense switch settings of 1, 3 and 9 decimal counts and Figure 12 shows settings of 1, 5, and 17 decimal counts. Note, the sense switch settings are actually binary in nature, base two, whereas the resultant number of clock pulses are base ten or decimal in nature. There are a total of 256 decimal counts (2^8 binary) possible.

Figure 13 shows the laser trigger pulse and the +20 volt output of the detector preamplifier power supply switch. The time base is 20 nanoseconds/division. The laser trigger pulse width has been increased in comparison to Figures 5, 6, 7, and 8. The synchronization of the +20 volt output and the laser trigger pulse was achieved within 4 nanoseconds. Figure 14 illustrates, in a multiple exposure, the effects of three different hex inverter pair delays. Again, each hex inverter pair delay equals typically 16 nanoseconds. Figure 15 shows that the synchronization of the -20 volt output and the laser trigger was achieved within 4 nanoseconds. Apparently, the -20 volt output switches faster than the +20 volt output. Figure 16 illustrates this clearly, since the lower trace is the -20 volt output and the upper trace is the +20 volt output.

Figure 17 is simply a repeat of Figure 13 for a time base of 400 nanoseconds/division. The excellent uniformity of +20 volt output is self evident. Figure 18 shows both the ±20 volt output for a time base of 2 microseconds/division. The uniformity is achieved by the proper use of decoupling capacitors in the circuit, such as between the switch case and common ground.

The printed circuit board layouts, doublesided with plated through holes, are shown full sized in Figures 19, 20, and 21. It should be noted that two grounds are employed to minimize possible stray triggering effects. These ground systems are maintained throughout the laser radar data acquisition electronics and are labeled common and chassis ground.

Finally, Figures 22 and 23 show the complete binary selectable detector holdoff circuit module. One four-pin connector provides +5 volts, +28 volts, -28 volts and common ground. The cable shield of the four-conductor cable provides chassis ground. One triaxial connector is the delayed laser trigger pulse output and the second is the remote in trigger pulse input. The multiple pin (14 conductor) connector provides the computer interface capability, such as the sense switch settings. The two triaxial

connectors on the opposite end of the module provide the ± 20 volt detector preamplifier power supply output.

Component listing and component layout are given in the appendix.

CONCLUSIONS

A binary selectable detector holdoff circuit has been designed and tested. This type of device is applicable wherever very high speed variable time delay switching of detector systems, under computer control, must be accomplished. The speed of the device is controlled by the choice of the nand gate clock (i.e., 20, 10, 8, 6 or 3 nanosecond logic). Also, a 50MHz clock rate is the maximum allowed due to the speed limitations of the 93S16 binary counters. The use of Silconix DG 187AA ±20 volt power supply switches was shown to be an excellent choice for the intended application. In actuality, the timing difference in the circuit (between the laser trigger pulse and the +20 volt supply output) is negligible since for most laser radar data acquisition applications, plus or minus 10 nanoseconds is an acceptable error in range measurement.

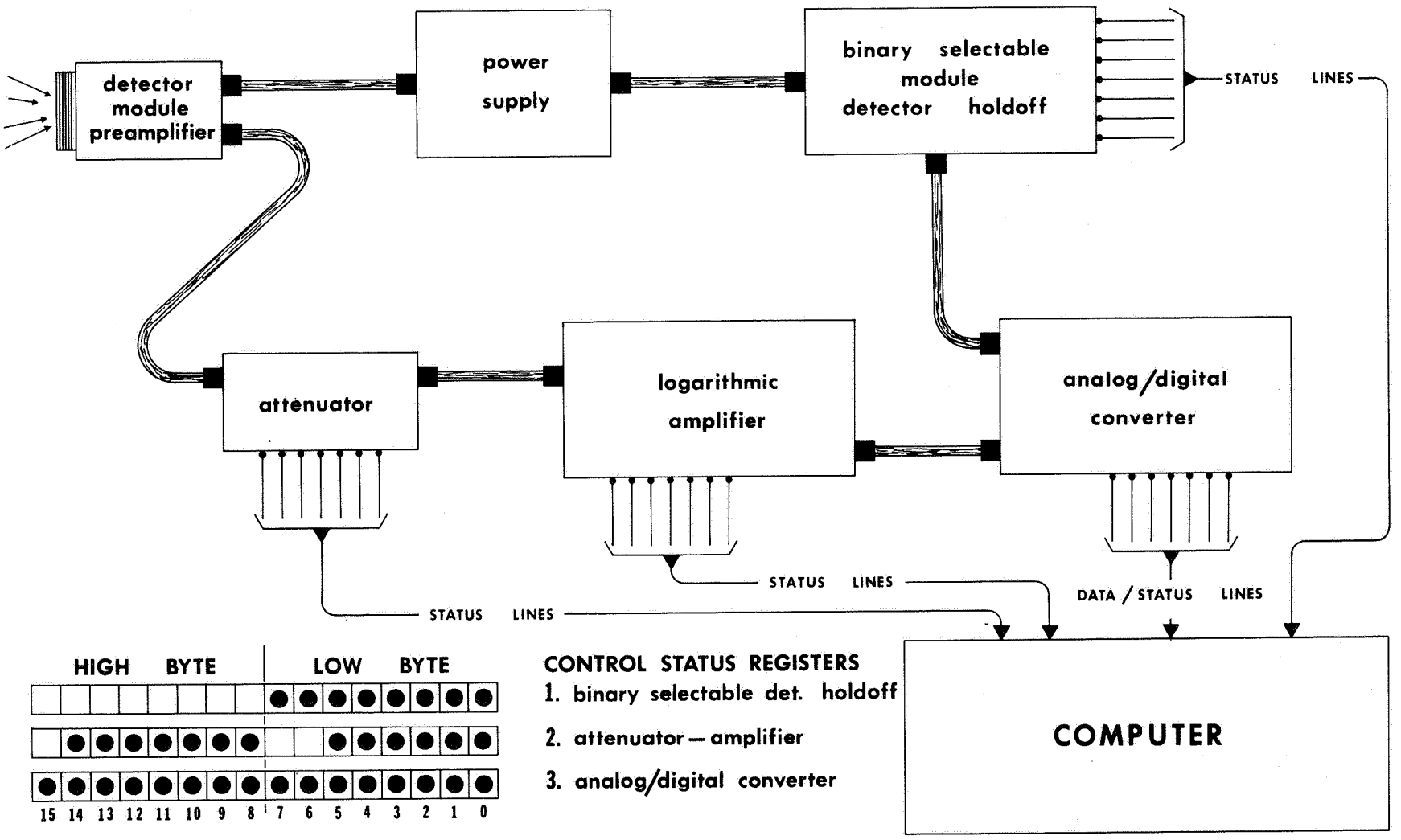


Figure 1. Signal detection and data acquisition electronics.

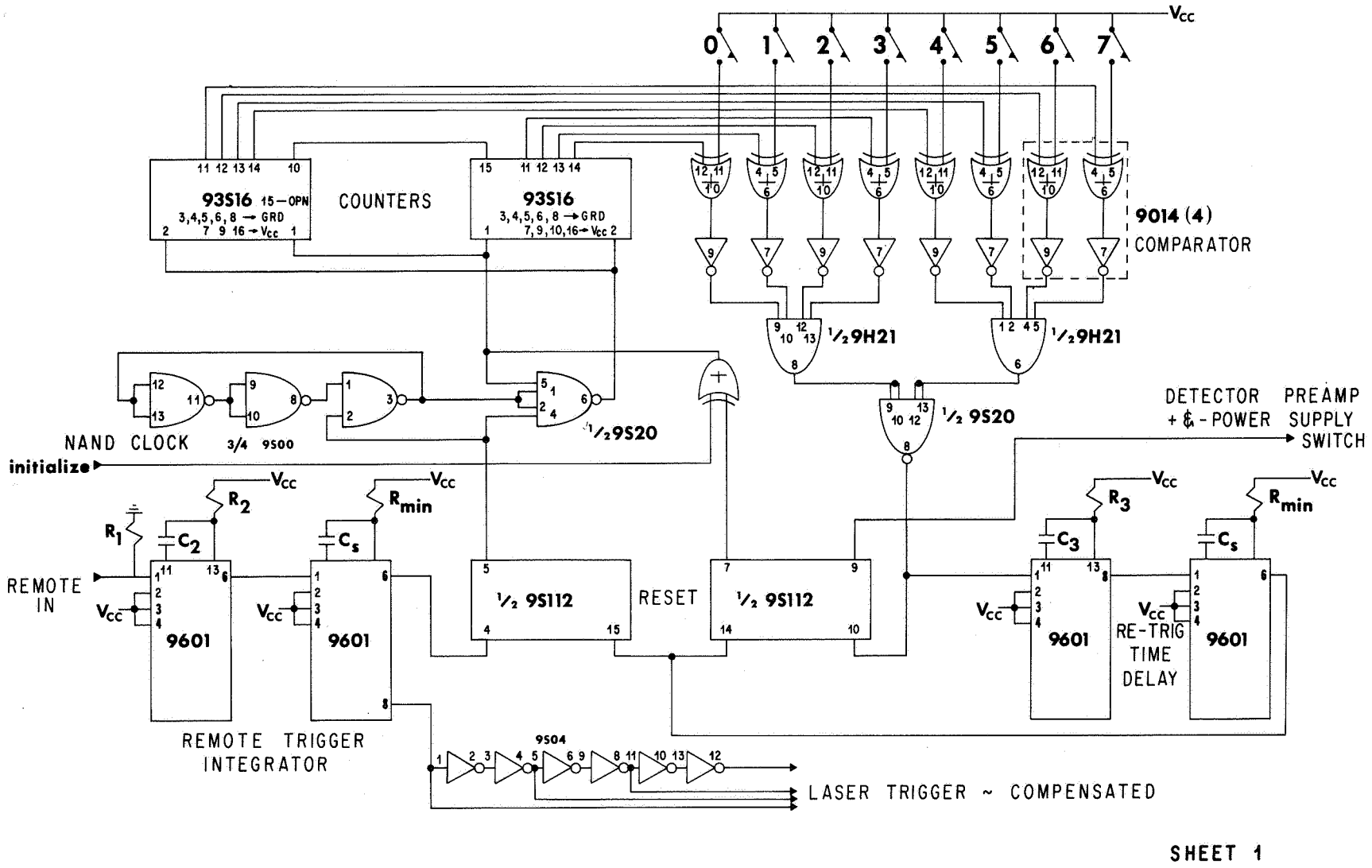


Figure 2. Binary selectable detector holdoff circuit.

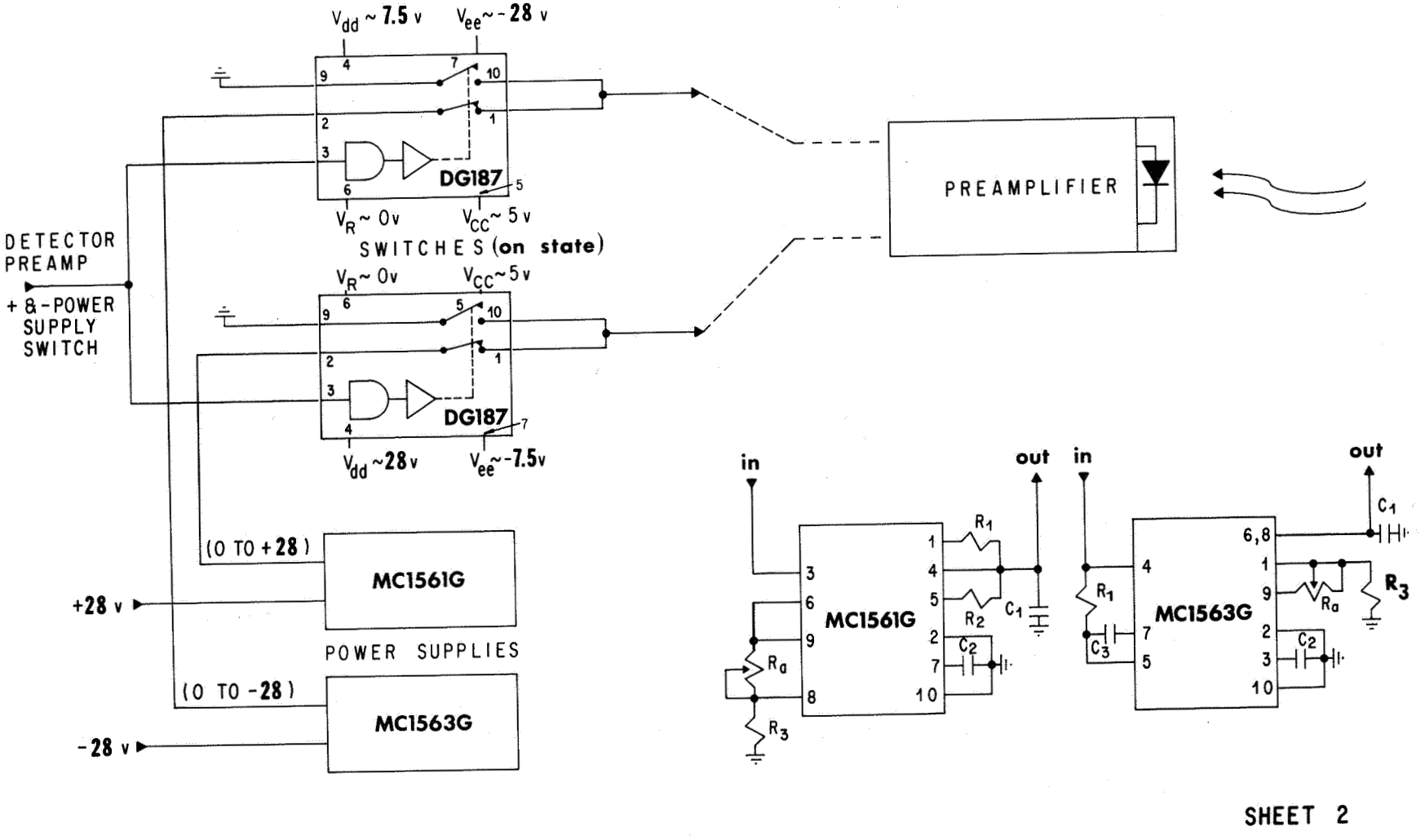
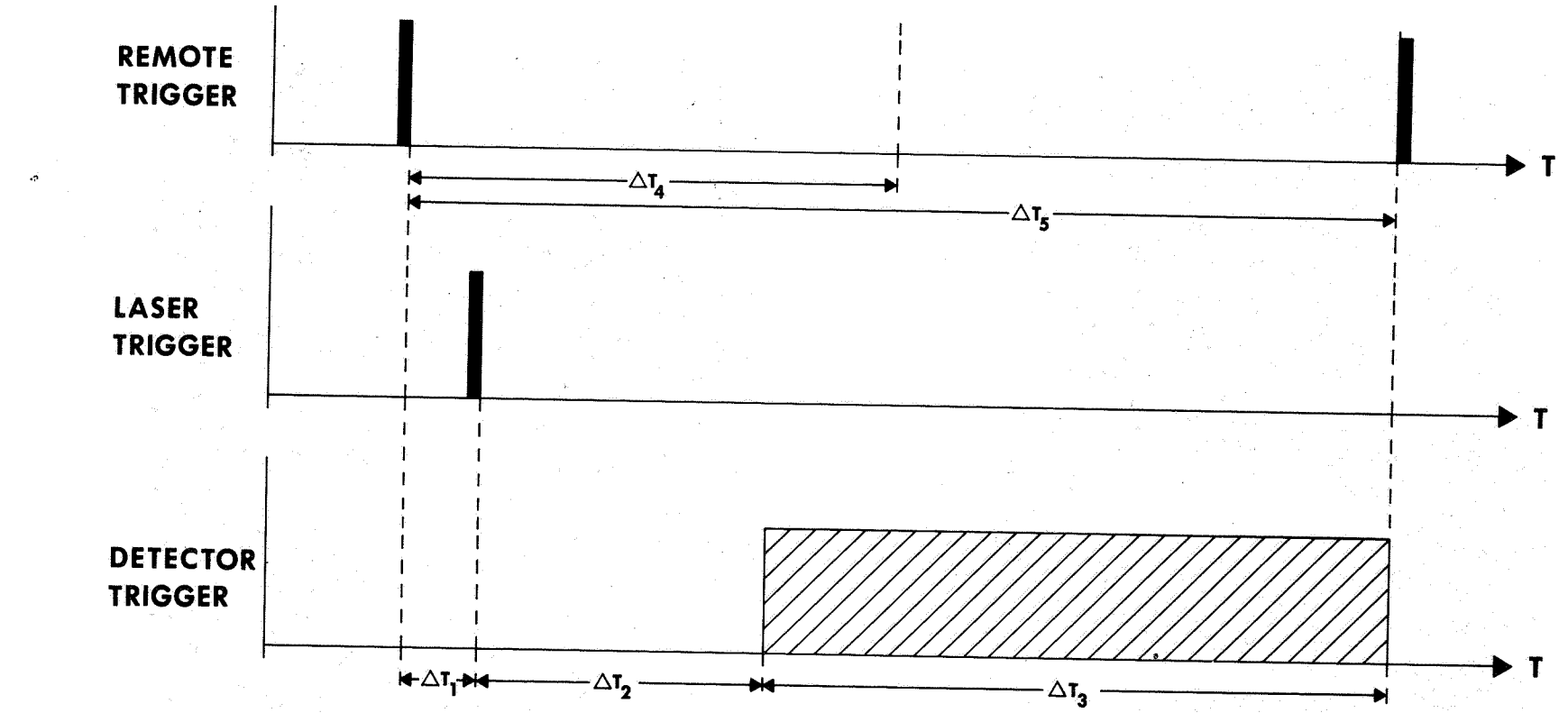


Figure 3. Binary selectable detector holdoff circuit.



CLOCK	RATES
9S00	100MHz
9H00	50MHz
9N00	30MHz
9L00	15 MHz

ΔT_1 – Inherent Circuit Pulse Propagation Delay
ΔT_2 – (Clock Rate) x (Binary Code)
ΔT_3 – Adjustable Detector Reset Delay
ΔT_4 – Remote Switch Contact Bounce Integrater
ΔT_5 – System Cycle Period

Figure 4. Timing diagram — binary selectable detector holdoff circuit.

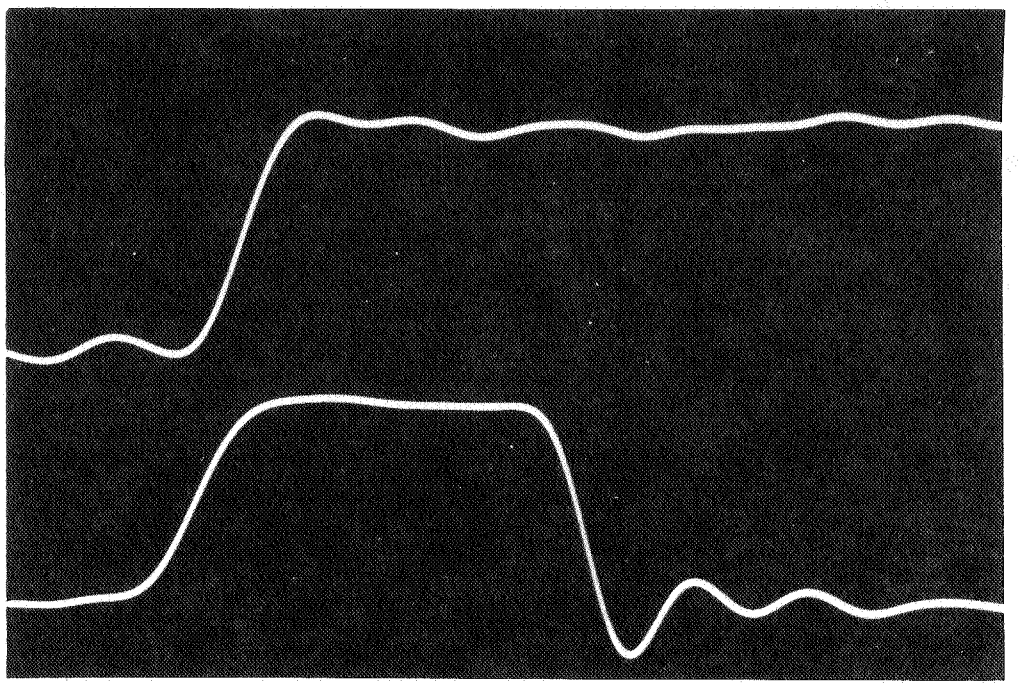


Figure 5. Comparison of the power supply switch signal with the delayed laser trigger pulse for seven hex inverter pair delays.

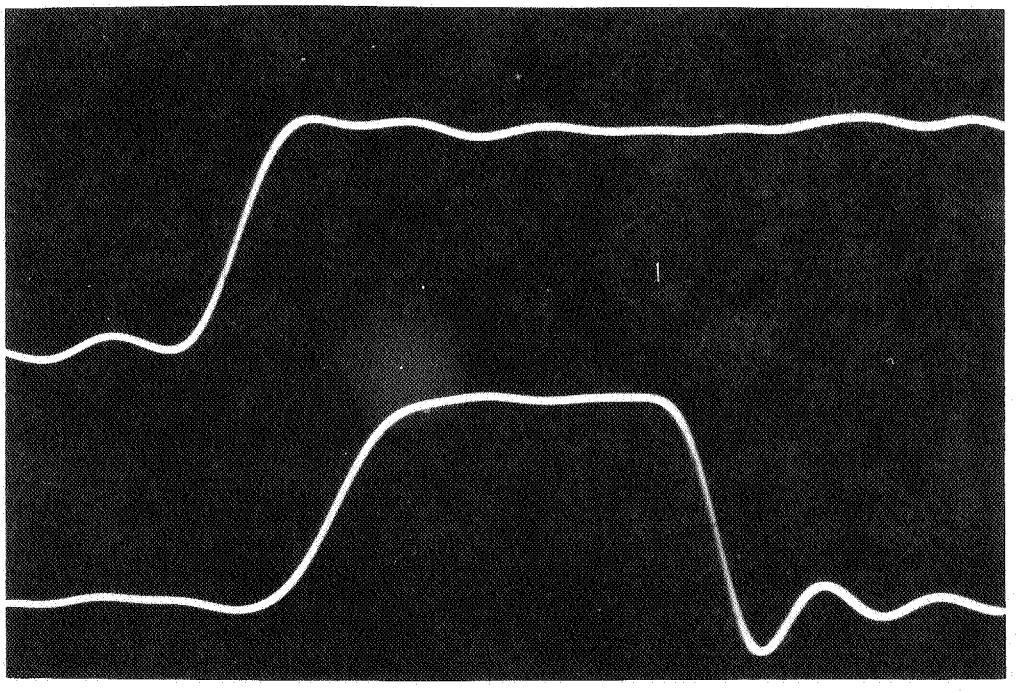


Figure 6. Comparison of the power supply switch signal with the delayed laser trigger pulse for eight hex inverter pair delays.

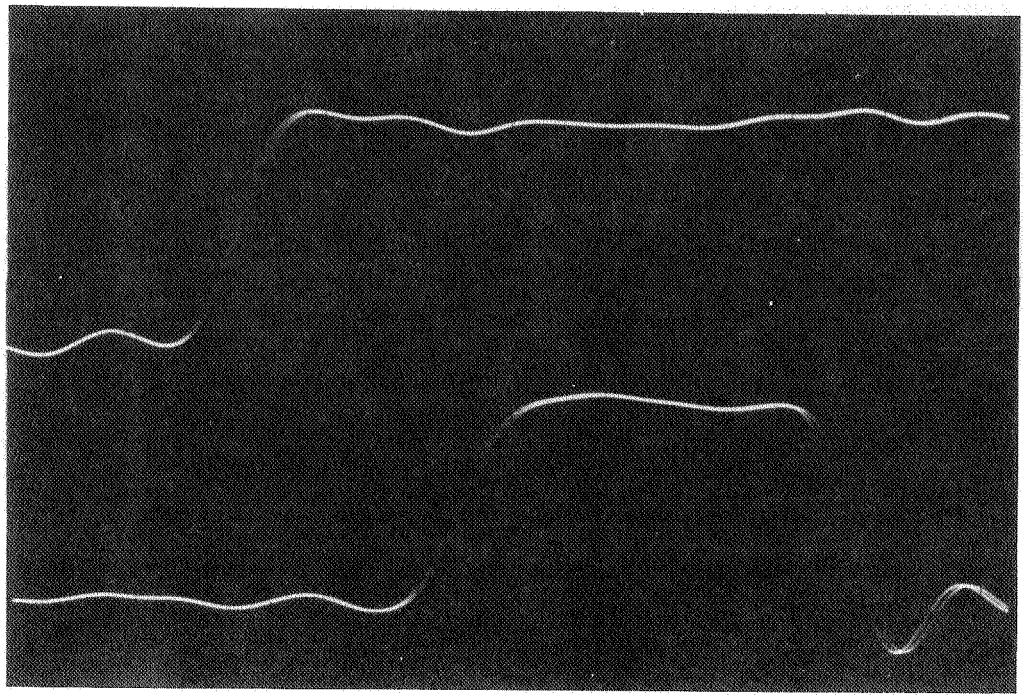


Figure 7. Comparison of the power supply switch signal with the delayed laser trigger pulse for nine hex inverter pair delays.

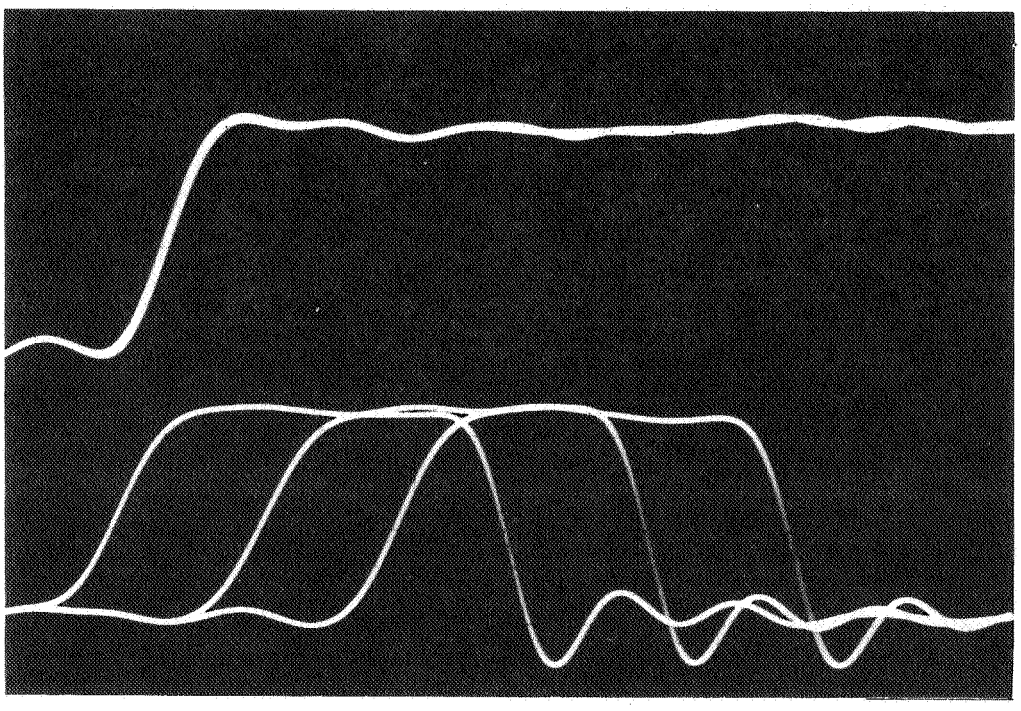


Figure 8. Multiple exposure comparison of the power supply switch signal with the delayed laser trigger pulse for seven, eight and nine hex inverter pair delays.

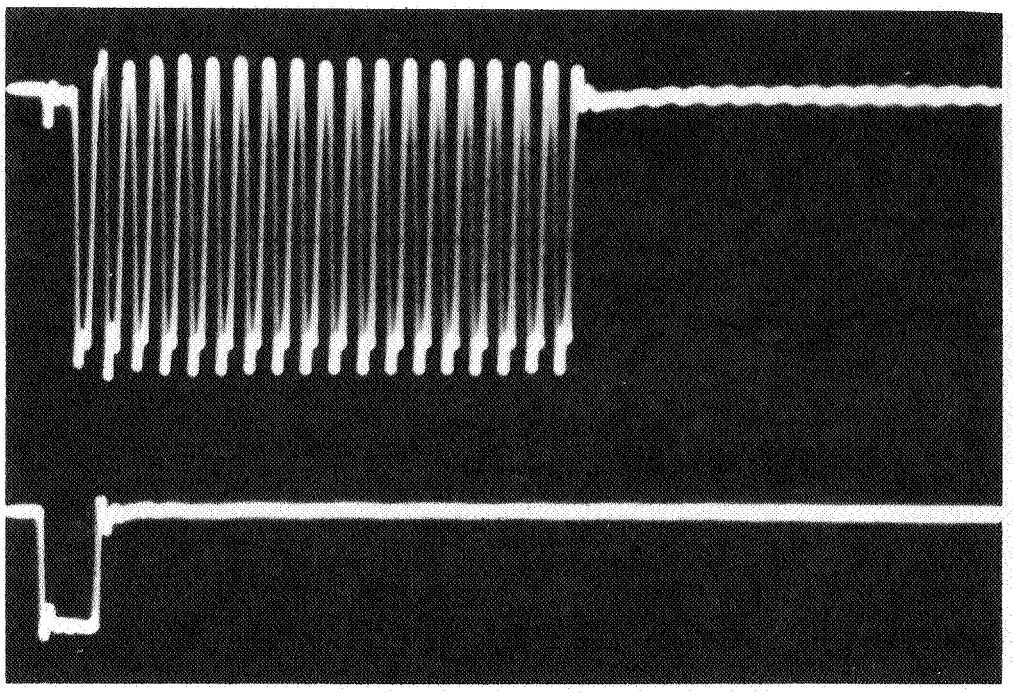


Figure 9. Comparison of the nand gate clock output with the remote in trigger pulse.

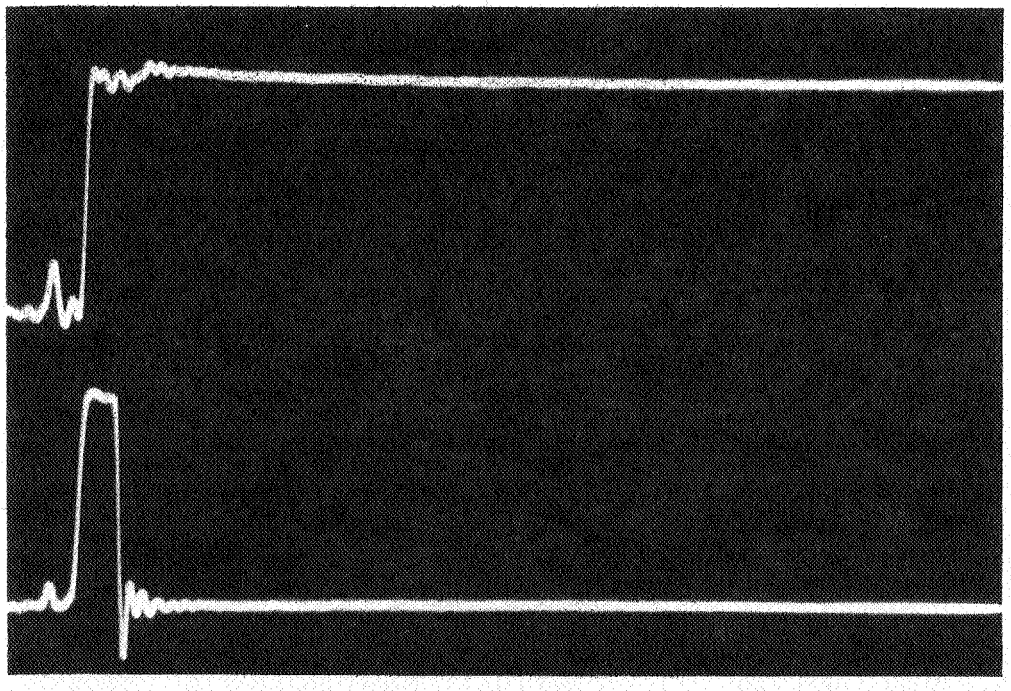


Figure 10. Synchronization of the power supply switch signal with the delayed laser trigger pulse for a sense switch setting of one decimal count.

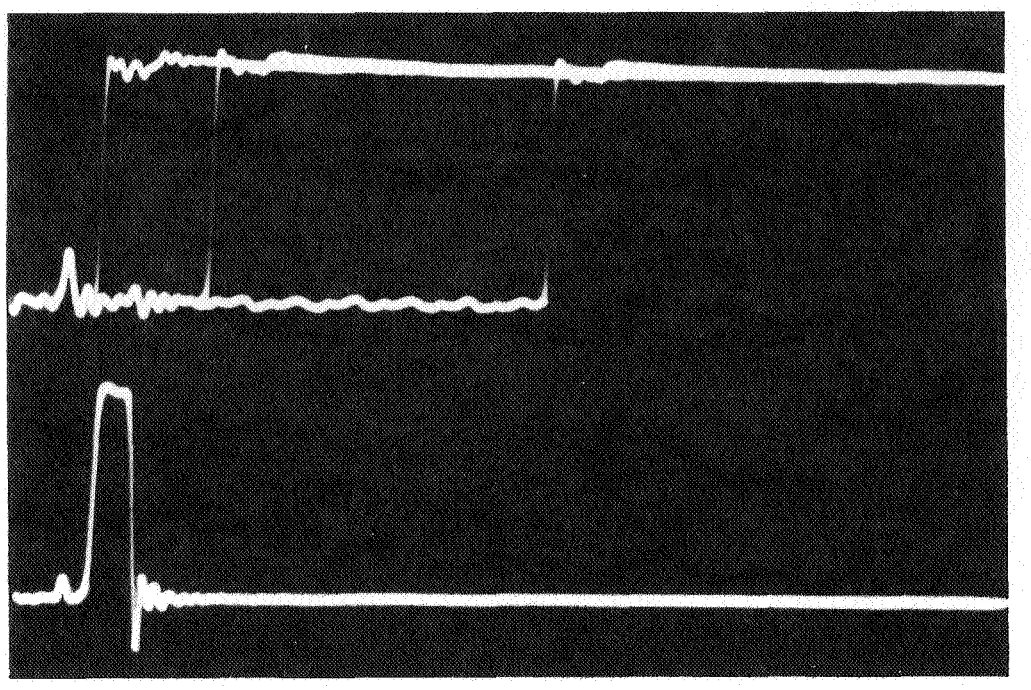


Figure 11. Multiple exposure comparison of the power supply switch signal with the delayed laser trigger pulse for sense switch settings of 1, 3, and 9 decimal counts.

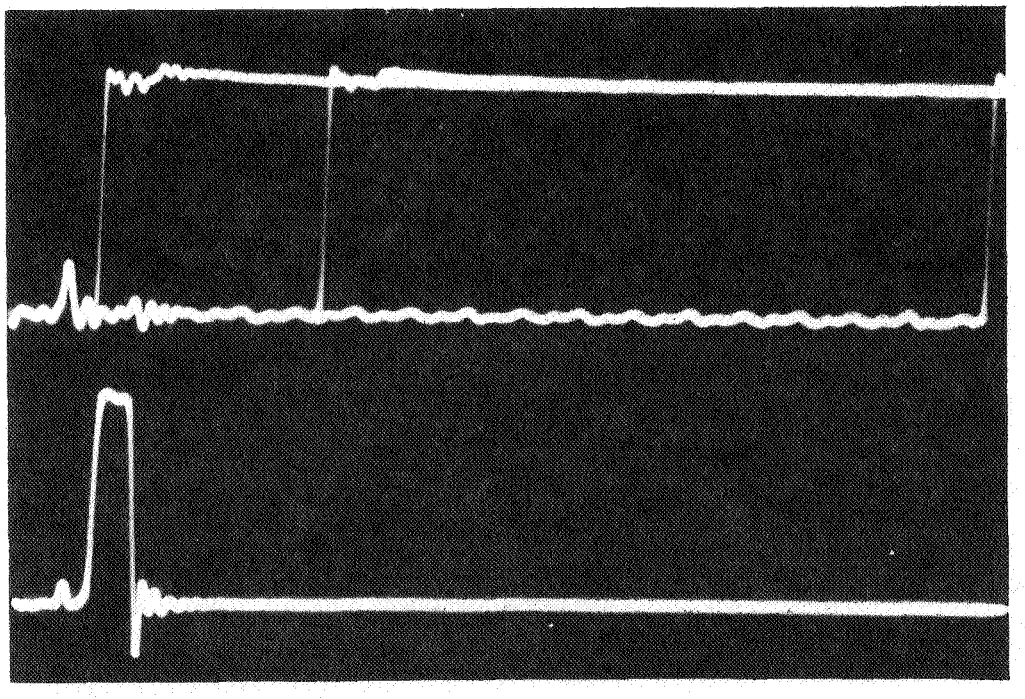


Figure 12. Multiple exposure comparison of the power supply switch signal with the delayed laser trigger pulse for sense switch settings of 1, 5, 17 decimal counts.

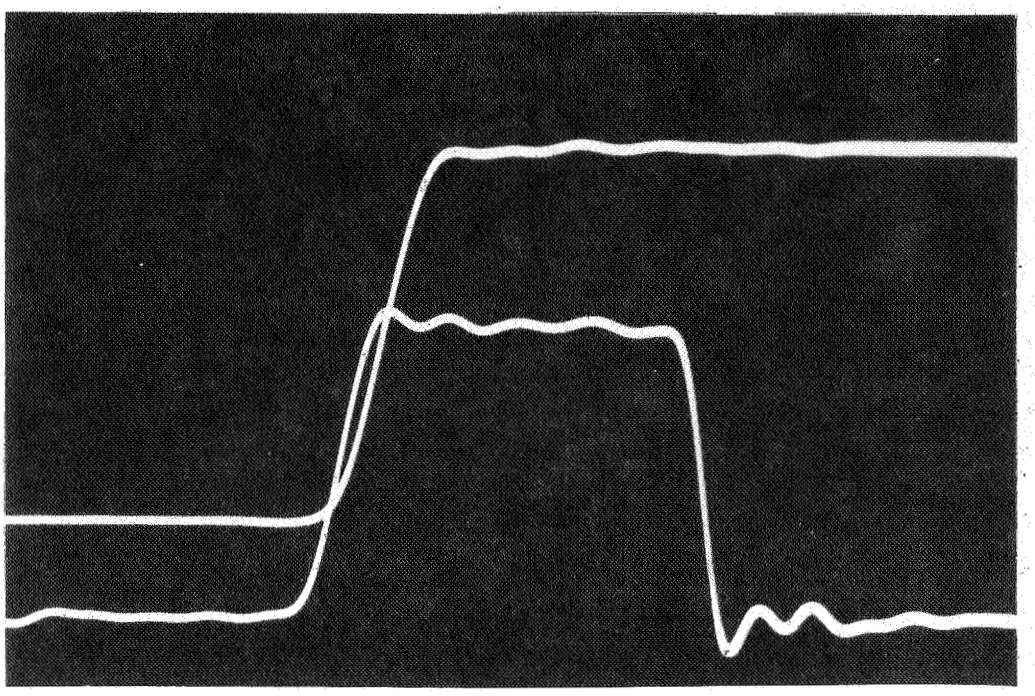


Figure 13. Synchronization of the power supply +20 volt output with the delayed laser trigger pulse.

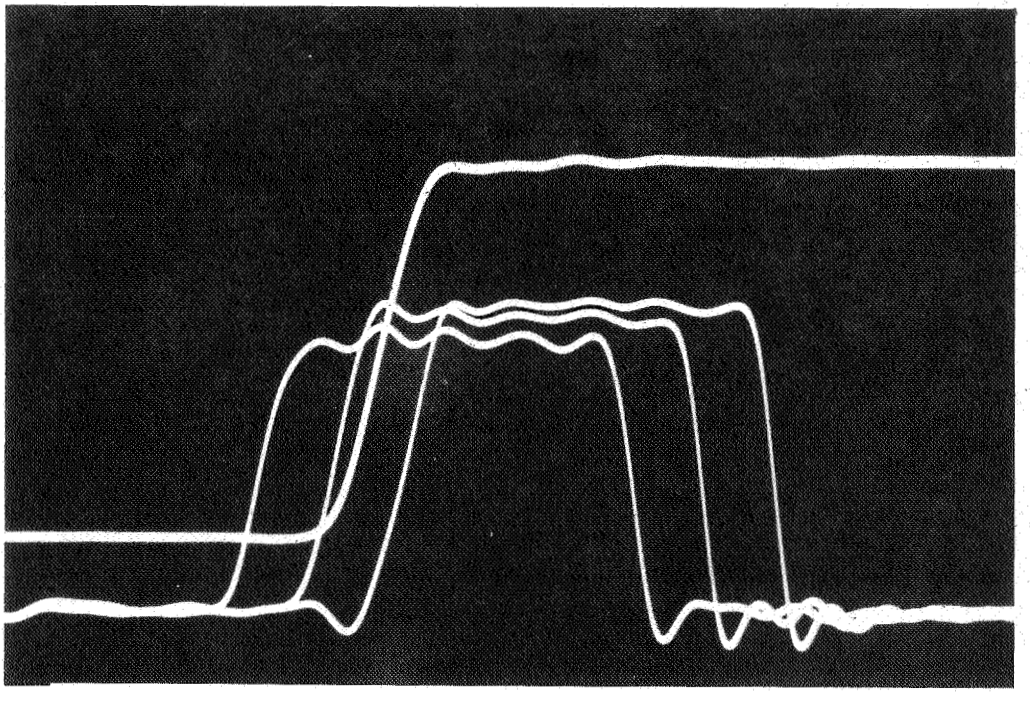


Figure 14. Comparison of the power supply +20 volt output with the delayed laser trigger pulse for one more and one less hex inverter pair delay.

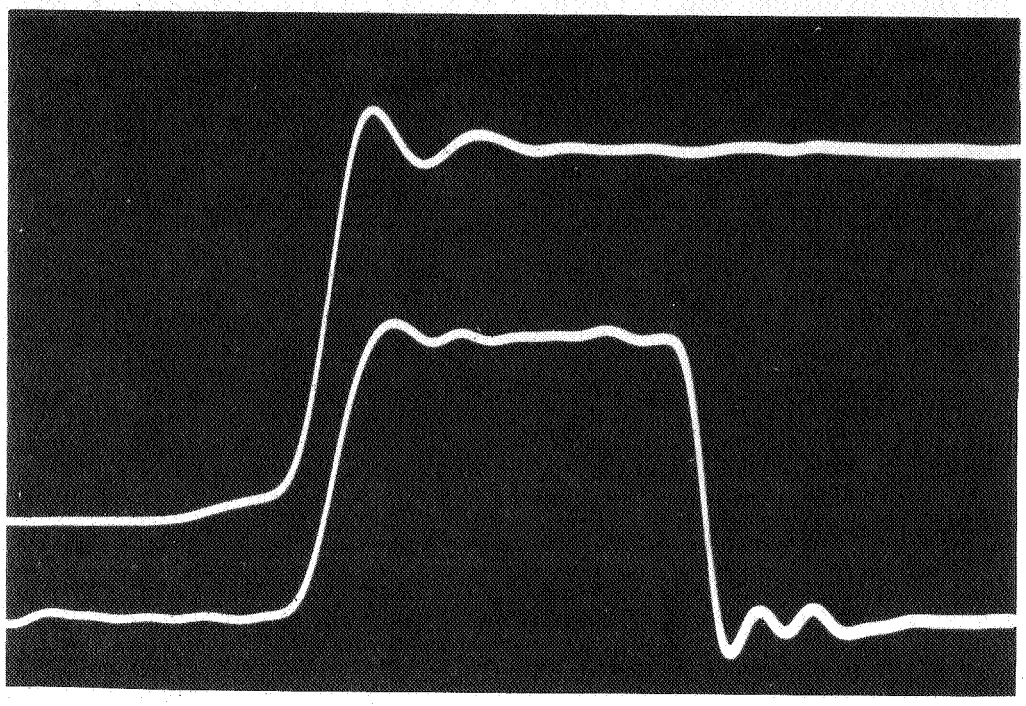


Figure 15. Synchronization of the power supply -20 volt output with the delayed laser trigger pulse.

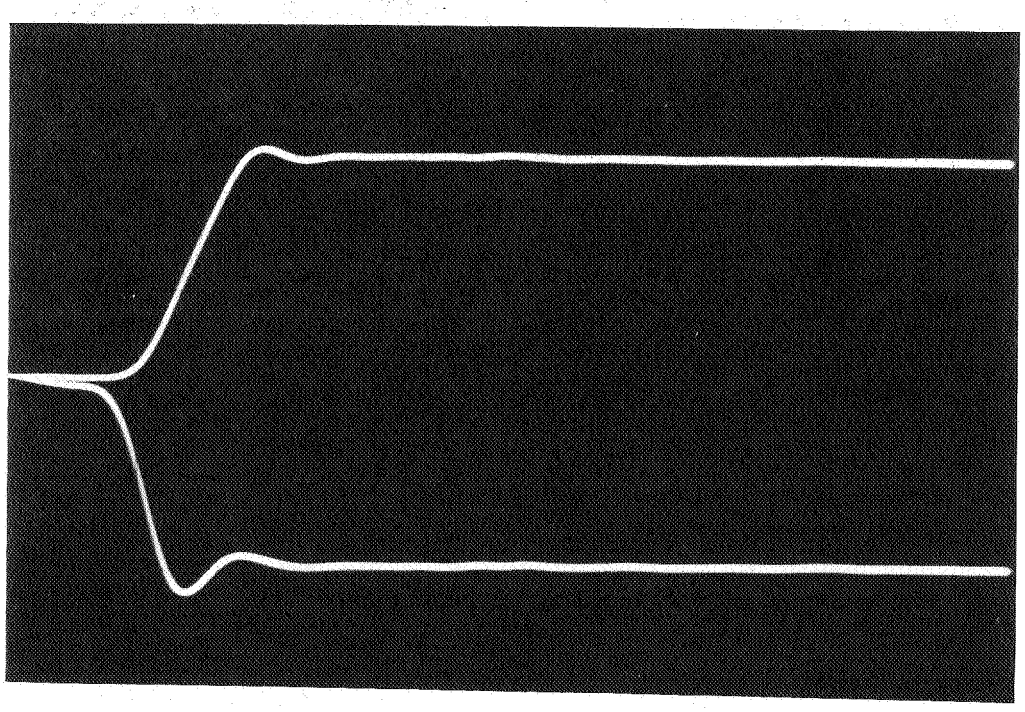


Figure 16. Comparison of the synchronization of the power supply +20 volt (upper trace) and -20 volt (lower trace) outputs.

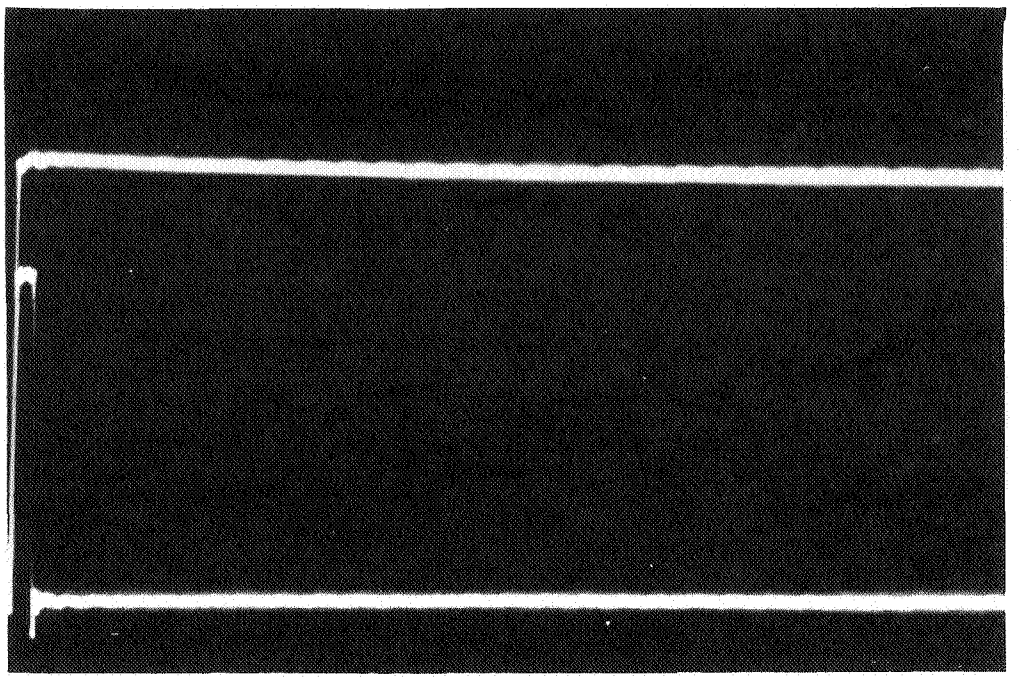


Figure 17. Comparison of the power supply +20 volt output with the delayed laser trigger pulse indicating high speed response, damping and stability.

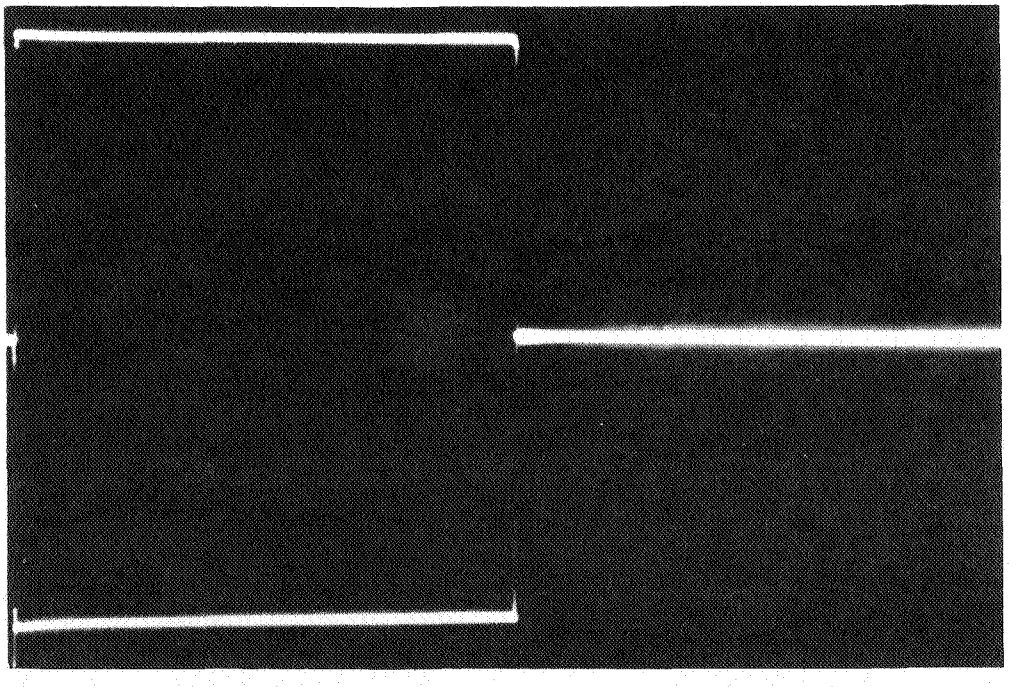
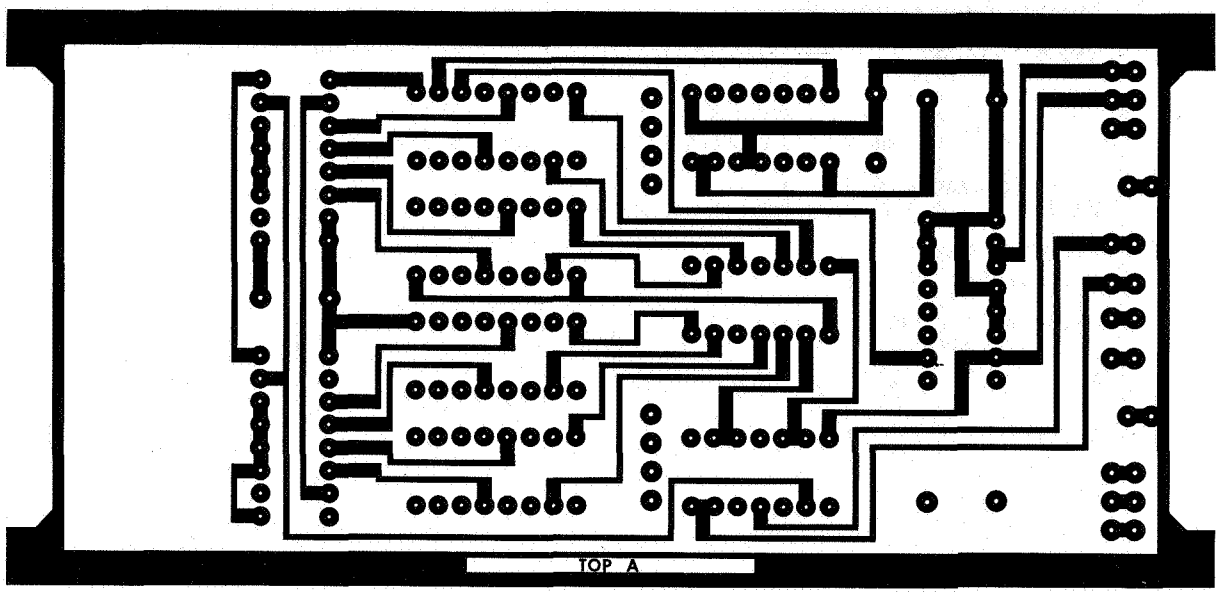
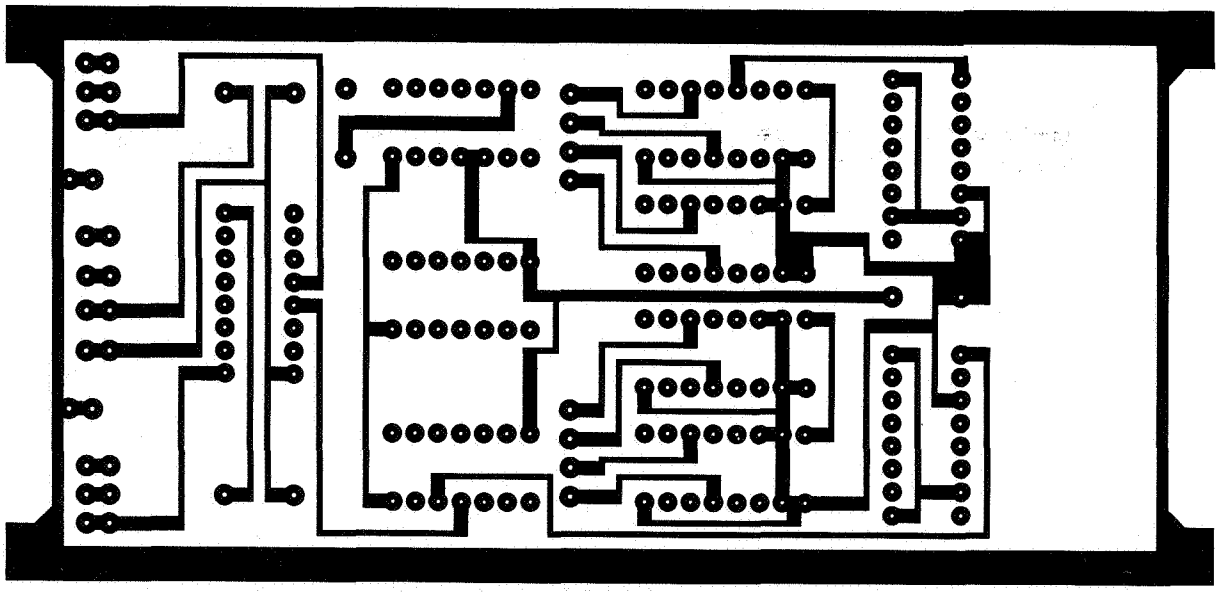


Figure 18. Comparison of the long term stability of the power supply +20 volt and -20 volt outputs.

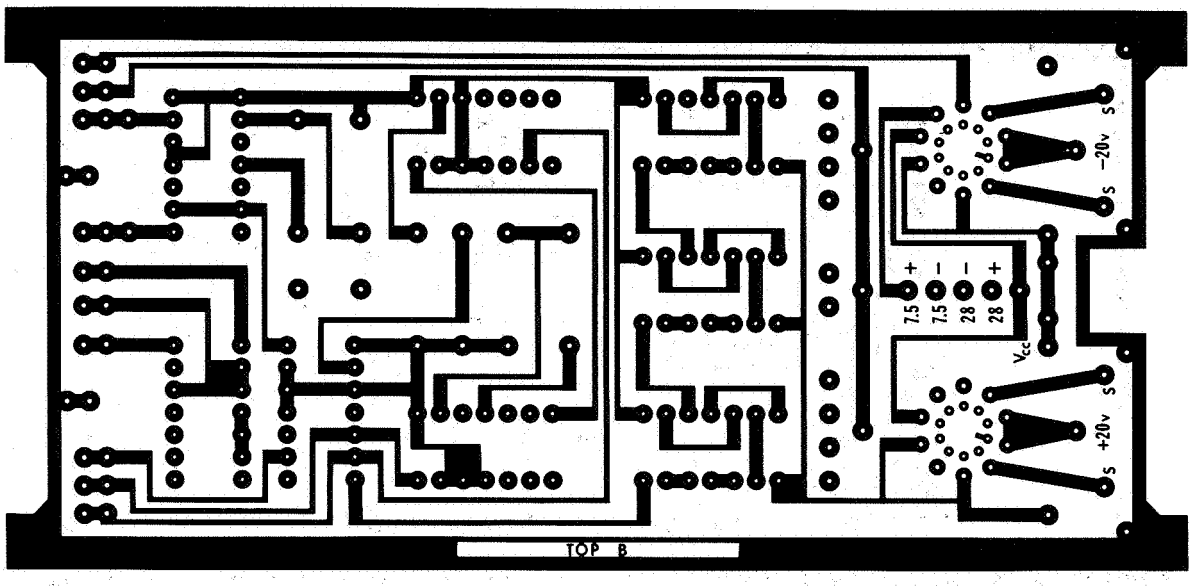


INTEGRATED CIRCUIT SOCKET SIDE



SOLDER SIDE

Figure 19. Printed circuit board A



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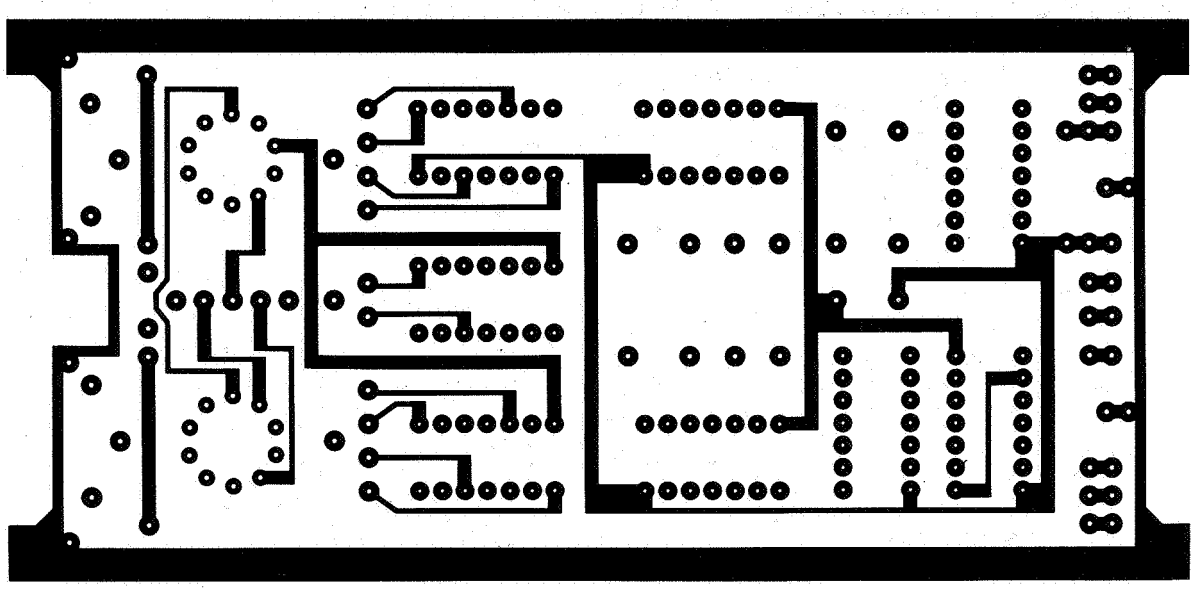
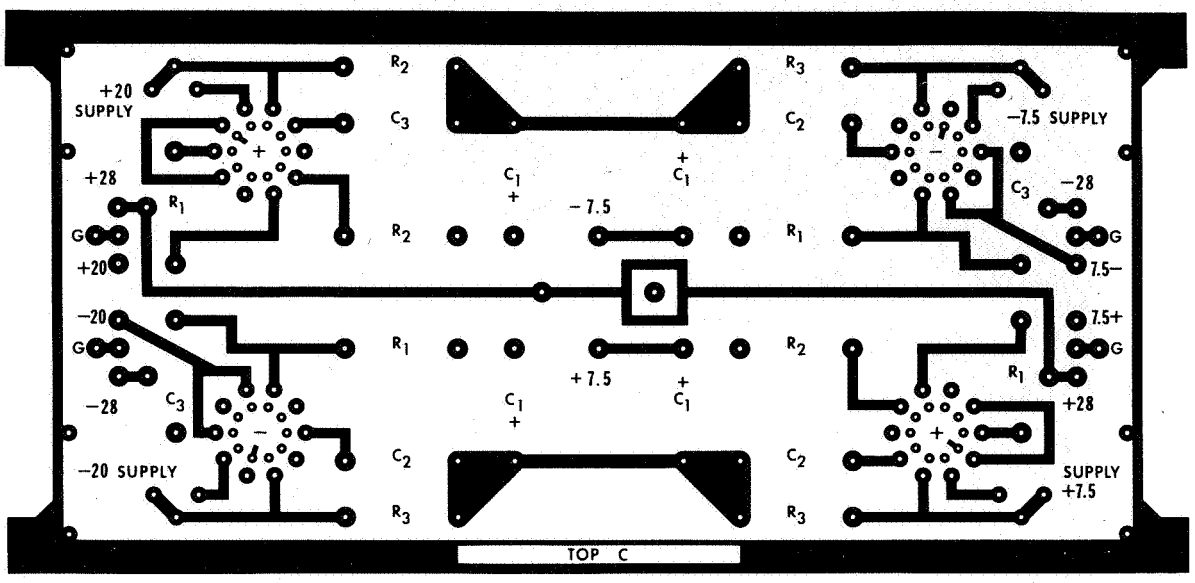
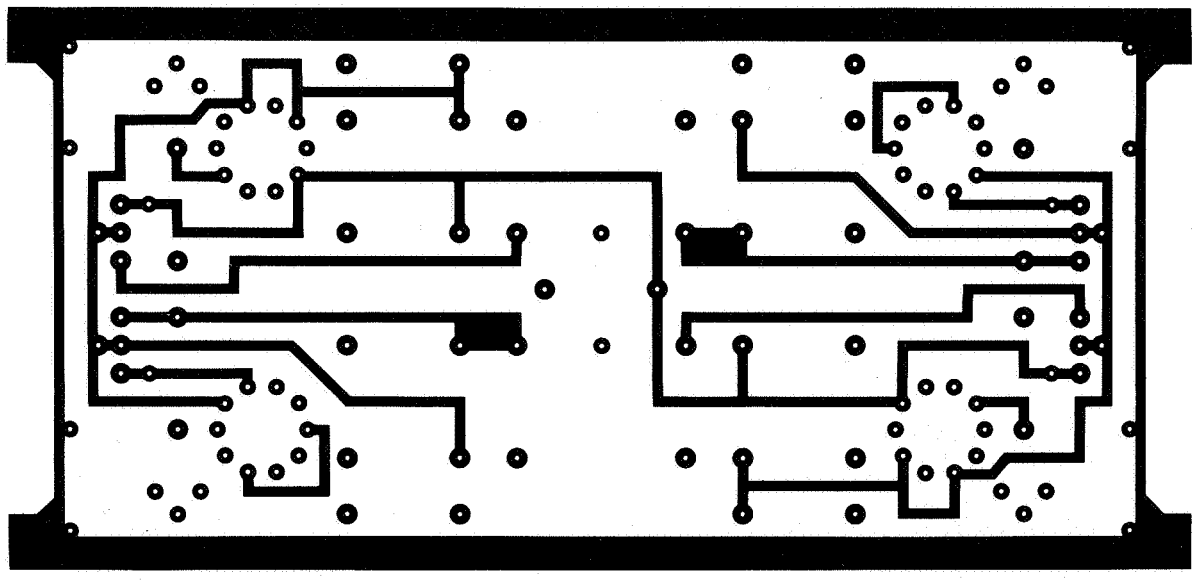


SOLDER SIDE

Figure 20. Printed circuit board B



INTEGRATED CIRCUIT SOCKET SIDE



SOLDER SIDE

Figure 21. Printed circuit board C

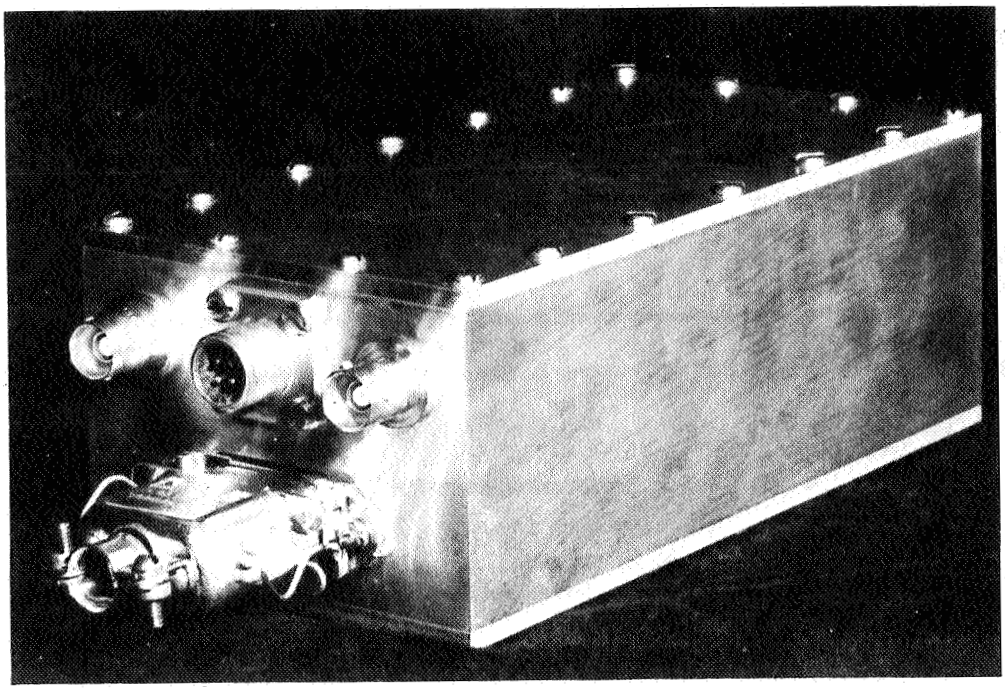


Figure 22. Circuit module, input end view.

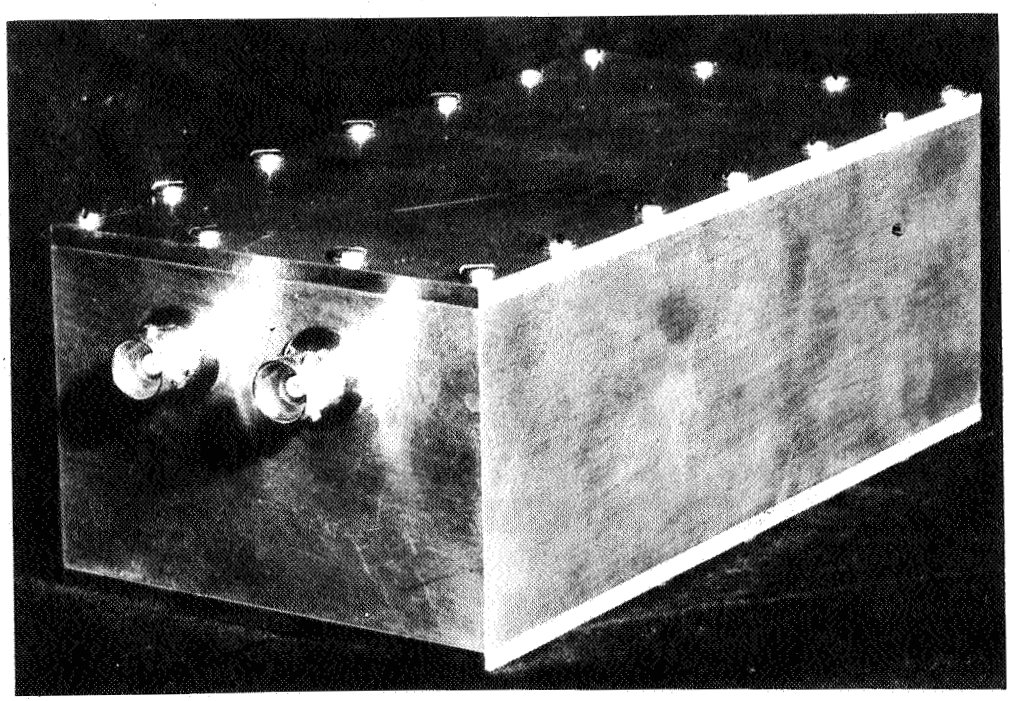


Figure 23. Circuit module, output end view.

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1. Kadrmas, K. A.: Phased-array Laser Radar: Concept and Application. NASA TM X-64753, June 8, 1973.

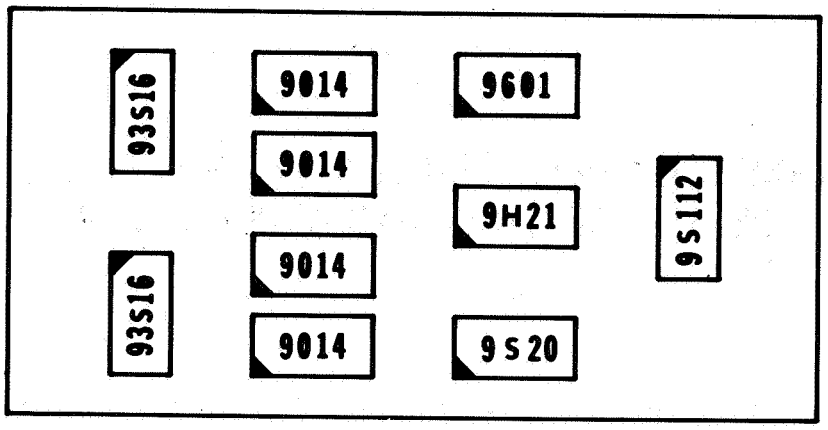
2. Fairchild Industries, Inc.: Fairchild Semiconductor Digital Logic Handbook. 1972.

APPENDIX

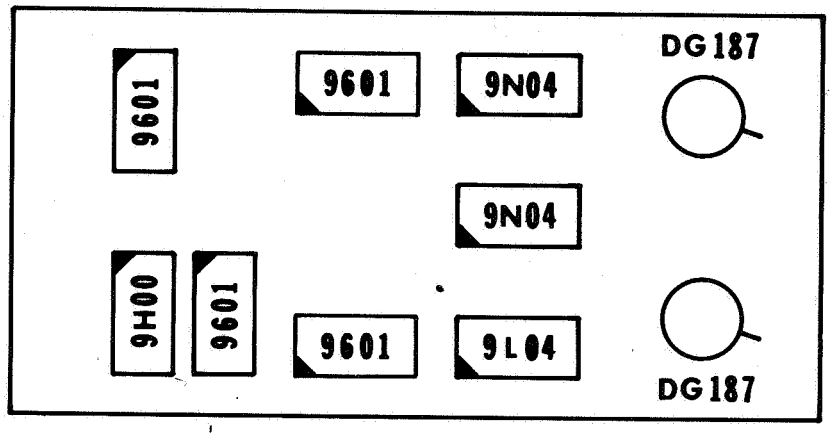
COMPONENTS AND COMPONENT LAYOUT

TABLE A-I. COMPONENT LISTING

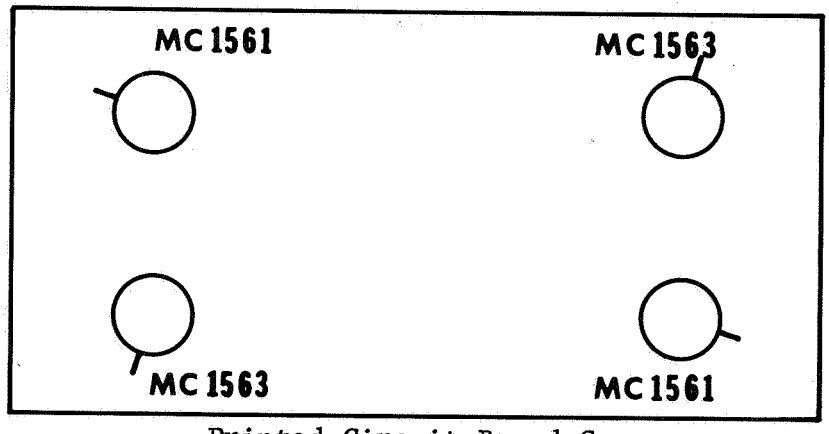
Type of Function	Component Type	No. Required
binary counters	93S16 9316	2 ea. 2 ea.
one shot	9601	5 ea.
flip flop	9S112	1 ea.
exclusive or with inverters	9014	4 ea.
four input and gate	9H21	1 ea.
four input nand gate	9S20	1 ea.
two input nand gate	9L00 9N00 9H00 9S00	1 ea. 1 ea. 1 ea. 1 ea.
hex inverter	9L04 9N04 9H04 9S04	3 ea. 3 ea. 3 ea. 3 ea.
switches	Silconix Corp. DG187AA	2 ea.
positive voltage regulator	Motorola Corp. MC1561CG	2 ea.
negative voltage regulator	Motorola Corp. MC1563CG	2 ea.
misc. resistors & capacitors	N/A	N/A



Printed Circuit Board A



Printed Circuit Board B



Printed Circuit Board C

Figure A-1. Component layout.

APPROVAL

BINARY SELECTABLE DETECTOR HOLDOFF CIRCUIT: DESIGN, TESTING, AND APPLICATION

By K. A. Kadrmas

The information in this report has been reiewed for security classification. Review of any information concerning Department of Defense or Atomic Energy Commission programs has been made by the MSFC Security Classification Officer. This report, in its entirety, has been determined to be unclassified.

This document has also been reviewed and approved for technical accuracy.

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Chief, Aerospace Environment Division

for E. D. Geissler
Director, Aero-Astrodynamics Laboratory

MSFC—RSA, Ala