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DRL LINE ITEM # 2
DRD # MA-129T

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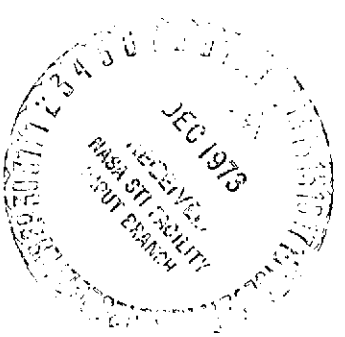
SOLID STATE POWER CONTROLLERS

FINAL REPORT
DATE 30 AUG 1973



TELEDYNE RELAYS

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ABSTRACT

The report is comprised of the rationale, analysis, design, breadboarding and testing of the incremental functional requirements that led to the development of prototype 1 and 5 Amp DC and 1 Amp AC Solid State Power Controllers (SSPC's). The SSPC's are to be considered for use as a replacement of electro-mechanical relays and circuit breakers in future spacecraft and aircraft. They satisfy the combined function of both the relay and circuit breaker and can be remotely controlled by small signals, typically 10 mA, 5 to 28 vDC.

They have the advantage over conventional relay/circuit breaker systems in that they can be located near the utilization equipment and the primary AC or DC bus. The low level control, trip indication and status signals can be circuited by small gauge wire for control, computer interface, logic, electrical multiplexing, unboard testing, and power management and distribution purposes. This results in increased system versatility at appreciable weight saving and increased reliability. Conventional systems require the heavy gauge load wiring and the control wiring to be routed from the bus to the load to other remote relay contacts, switches, sensors, etc. and to the circuit breaker located in the flight engineer's compartment for purposes of manual reset. Solid state switching reduces the conducted EMI substantially. The SSPC is intended to protect itself, the load, and the systems wiring against overload, short-circuit and voltage transients.

SUMMARY

Following analysis, design and breadboard testing, 1 and 5 Amp DC and 1 Amp AC prototype Solid State Power Controllers were produced and delivered to NASA MANNED SPACECRAFT CENTER/Houston. The specifications of the Statement of Work were satisfied with a few exceptions. These exceptions were due to compromises in arriving at optimum design with respect to weight, size, reliability and cost. Many options in design were evident and are discussed.

Due to the small quantity of units contracted and problems of high density packaging of discrete components, some optional features of the SSPC's were not included in the delivered articles, particularly "status indication". Circuits for this feature were analyzed, breadboarded and tested. Production requirements would utilize hybrid microelectronic manufacturing techniques, and the inclusion of many optional functions can be realized.

In addition to meeting functional requirements, the design objective was simplicity for reasons of reliability, weight, size and cost. The design leading to the prototype units met this requirement. Relaxation of some specification parameters without sacrifice to overall performance could lead to further optimization of design and are discussed.

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CONCLUSIONS

Solid State Power Controllers can be made in the envelope proposed, satisfy the functions and meet the environmental conditions. This makes possible a fully automatic electrical control system with built-in safety factors to protect the SSPC, the load and wiring against overload, short-circuit and voltage transients.

RECOMMENDATIONS

Since the efforts of the study and the production and testing of functional SSPC's proves the concept, final specifications for production flight SSPC's should be generated. Efforts should be made between NASA, cognizant military services, aircraft manufacturers and potential suppliers to arrive at a mutual agreement concerning basic packaging, functional requirements, control voltage levels, trip indication, status indication, etc. To meet functional requirements in optimum packaging, hybrid microelectronic manufacturing techniques will be required. Poor economics as well as reliability exist in relatively small quantity of hybrid microelectronic production. Standardization of basics would encourage more multiple and universal usage with resulting improvements in economics and reliability. Economy, rather than design or production, appears to be the only obstacle to widespread practical usage of SSPC's. An advanced system utilizing SSPC's would be cost-competitive with conventional systems if reasonable production could be anticipated.

Although the contract requested study and development in the 1 Amp to 5 Amp range, higher current SSPC's are being considered. For the high DC current range, 10 Amp to 50 Amp, the availability of transistor chips with good secondary break-down characteristics are limited and only available at considerable cost. Encouragement to the semi-conductor industry to produce an acceptable chip at reasonable cost is highly recommended.

Industry has recently reported on some SSPC failures in switching into transformer loads where core saturation can occur. Teledyne has not experienced this failure mode. Since reported failures have been catastrophic in nature, further study of the problem is suggested and resulting specifications derived to protect against this possible failure mode.

INTRODUCTION

It was suggested that a study be made of DC and AC Solid State Power Controllers (SSPC's) with respect to each of the functional requirements such as control voltage, trip indication, status indication, and isolation. Teledyne Relays was to analyze optional circuitry for each function and to weigh the results with respect to size, cost, weight and reliability. Optimum packaging was to be a main consideration. The final objective was to fabricate and test prototype units incorporating the analysis and breadboard testing results. Although the guiding specification was MIL-P-81653, "General Specifications for Power Controller, Solid State", deviations were allowed to optimize the design. The basic functions and switching characteristics were to be satisfied in principal. The following functions and points of design analysis were considered for both the DC and AC SSPC's.

DC SOLID STATE POWER CONTROLLERS
- Power Output Termination
- Power Chip Selection
- Power Dissipation
- Isolation
- Current Limiting and Short-Circuit Protection
- Control Voltage Selection
- Trip Indication
- Status Indication
- Reset
- Transient Voltage Protection
- Fusing
- Foul-up Protection
- Circuit Schematic
- Packaging
- Reliability
- Specifications
- Test Results

AC SOLID STATE POWER CONTROLLERS
- Zero Axis Switching
- Power Output Termination
- Power Chip Selection
- Power Dissipation
- Isolation
- Short-Circuit Protection
- Control Voltage Selection
- Trip Indication
- Status Indication
- Waveform Distortion
- Reset
- Transient Voltage Protection
- Fusing
- Foul-up Protection
- Circuit Schematic
- Packaging
- Reliability
- Specifications
- Test Results

In analysis and design, the axiom was taken that reliability was inversely proportional and cost-, weight- and size-proportional to total component count of the circuit. Emphasis was on simplicity.

DC SOLID STATE POWER CONTROLLERS

POWER OUTPUT TERMINATION

MIL-P-81653 solid state power controller specification requires the functional circuitry illustrated in Fig. 1, requiring three terminals in the output section. The ground terminal is used for establishing an internal power supply for switching and status function. This current arrangement has distinct disadvantages in that the base current necessary to drive the power switching transistor must be established for the minimum load voltage, resulting in excessive power dissipation at maximum load voltages. Circuitry for the isolation and control function requires a relatively high component count. The principle objective of the study was to reduce the component count for reasons of size, weight, cost and reliability. Transformer coupling is required to obtain the necessary base drive to saturate the power transistor, introducing probable RFI elements unless elaborate filtering is employed.

A 2-terminal design was investigated and the functional circuitry is illustrated in Fig. 2. This arrangement has the advantage that no power is taken from the load supply for the switching function. The base drive is independent of the load voltage, resulting in the controller having uniform switching capabilities from .5 volts to 30 volts. The 2-terminal design allows for location of the power switching transistor on either the supply or ground side of the load voltage. In the case of the 3-terminal design, the load is dedicated to the ground side. The disadvantage is that the power for the base drive of the switching function must be derived from the control signal. The current required for low control voltages is appreciably more than that required for the 3-terminal controller. With a 28 volt control voltage current, drain is not excessive for 1 and 5 Amp controllers. For higher ratings, control current requirements may be excessive. RFI problems will also exist for the 2-terminal controller, as transformer coupling is required for isolation. The induced power of the RFI element is considerably less for the 2-terminal controller. Status indication requirement is more complex for the 2-terminal controller without the ground reference. It can be accomplished by sensing current in the load line versus sensing voltage at the load in the 3-terminal controller.

An alternate 3-terminal design was investigated, as shown in Fig. 3. For 1 Amp loads a PNP transistor may be used for Q1, with Q2 omitted. For higher currents, PNP transistors are not readily available with sufficient Beta for efficient drive. The NPN power transistor, driven by a PNP transistor, allows for efficient switching. The only disadvantage is the increased voltage drop across the combined switching transistors. Fig. 4 shows load current vs voltage drop. It might appear that the larger voltage drop would cause considerably more power dissipation resulting in a less efficient power distribution system. However, calculations taking

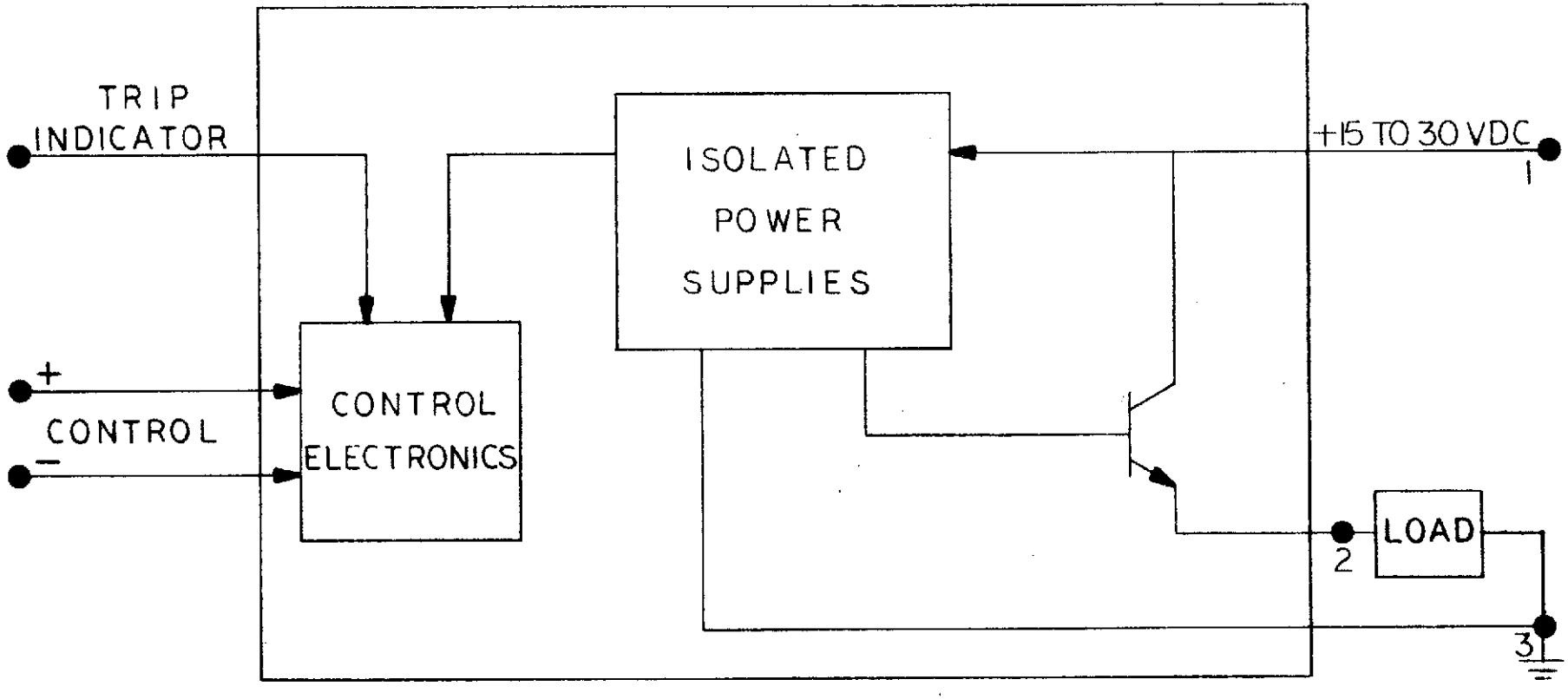


FIG.1 MIL-P-81653 3 TERMINAL CONTROLLER

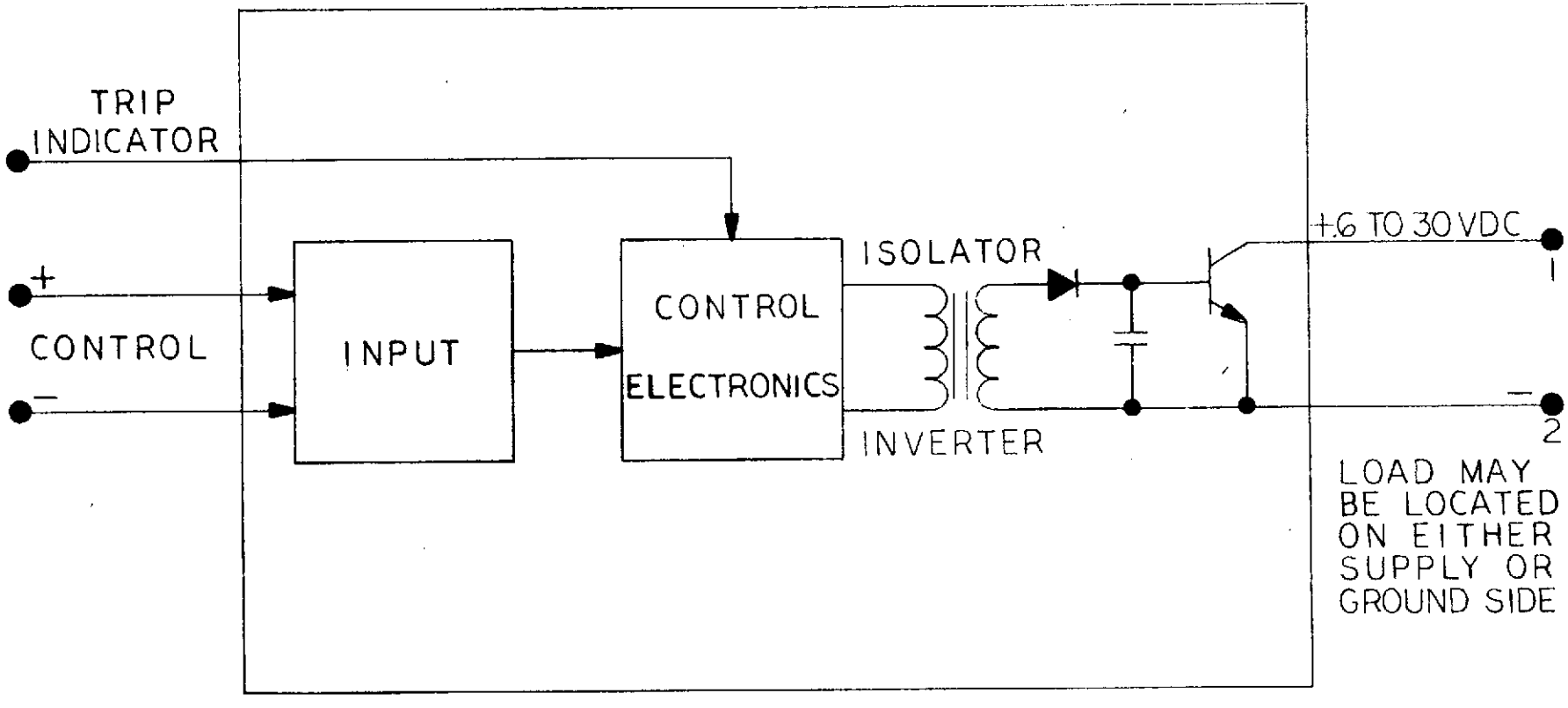


FIG. 2 TELEDYNE 2 TERMINAL CONTROLLER

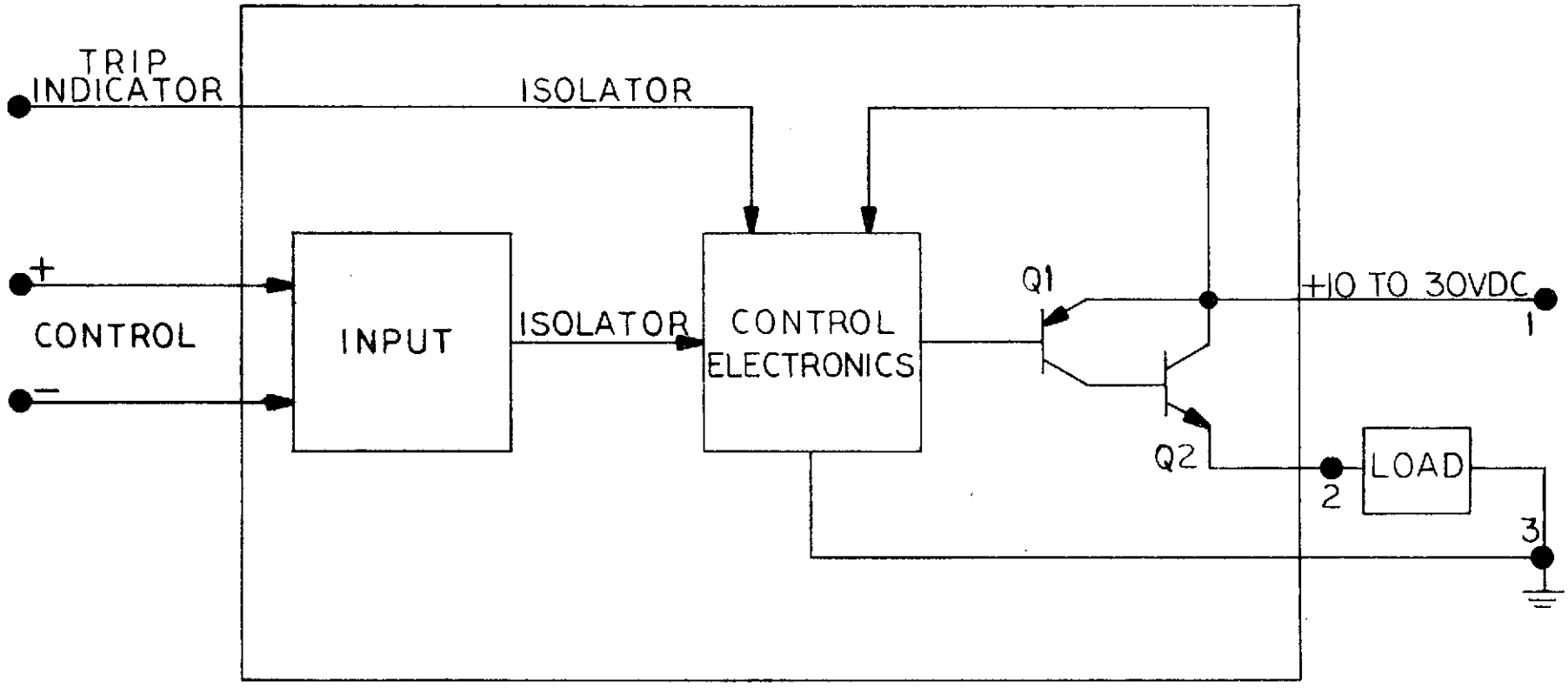


FIG.3 3 TERMINAL EMITTER FOLLOWER CONTROLLER

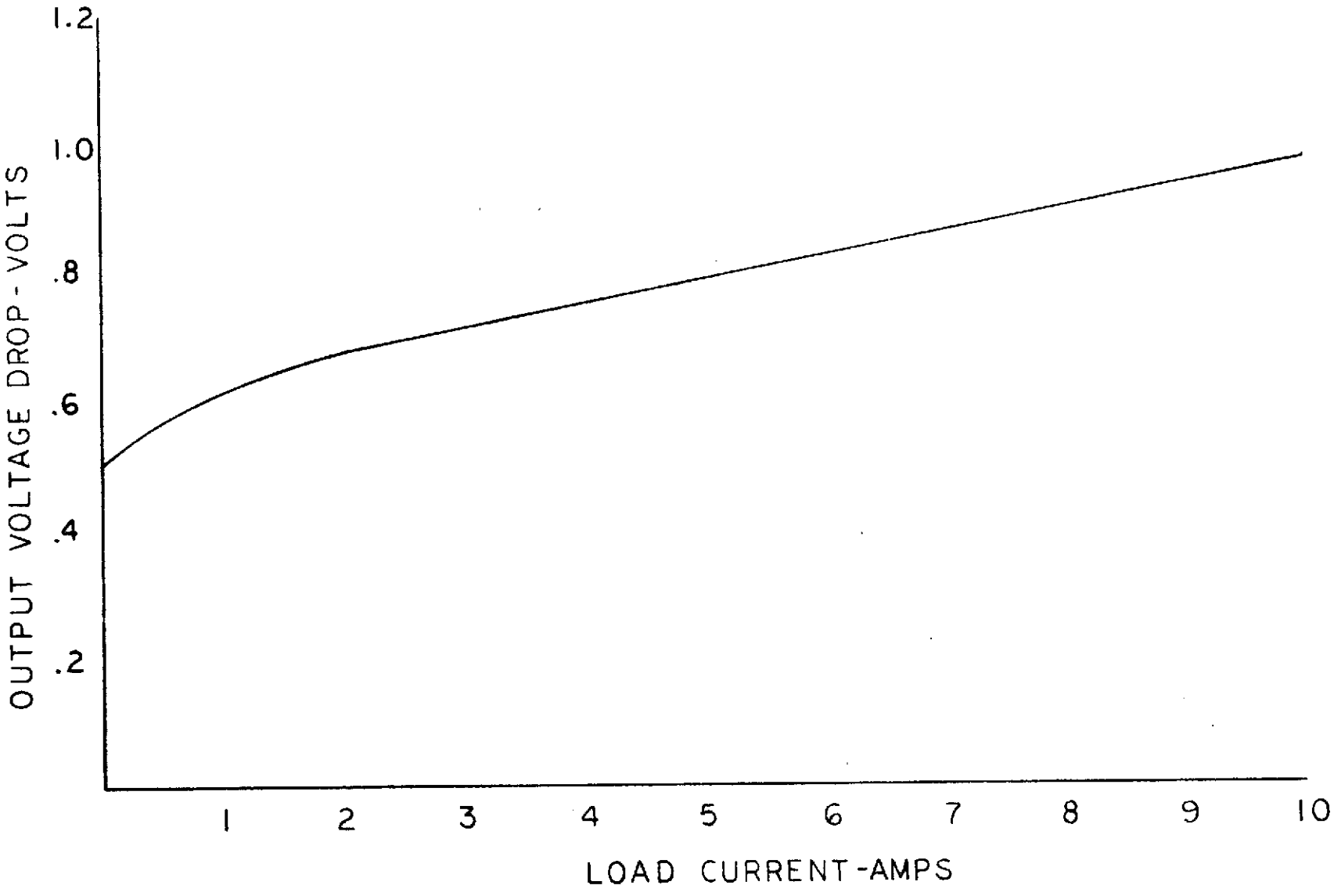


FIG. 4 OUTPUT VOLTAGE DROP VS. LOAD CURRENT - EMITTER FOLLOWER CONTROLLER

into consideration the internal power requirements for drive as well as the power dissipation of the power switching transistor, indicate that this 3-terminal arrangement is more efficient for loads up to 7.5 Amps. Above 7.5 Amps, a MIL-P-81653 controller is more efficient. It has been estimated that from 76% to 90% of controllers on actual aircraft systems (A-7, F-14, SST, etc.) are for loads of 7.5 Amps or less. There may be loads which suffer in performance due to the slightly reduced output voltage. Trade-off studies are required to isolate the areas. Another major advantage of the 3-terminal controller illustrated in Fig. 3, is that isolation can be accomodated by opto-electro means, resulting in elimination of RFI-induced elements, reduced weight, size, cost, and improved reliability.

The design used for prototype units incorporated the 2-terminal configuration, Fig. 2, because of the 1 and 5 Amp rating specified and the available 28 volt control voltage. The 3-terminal controller, Fig. 3, should be considered in future studies if the resulting slight increase in output voltage drop is acceptable.

POWER CHIP SELECTION

The output power switching transistor is the only highly stressed component in the entire circuit. In the current limiting mode, it must dissipate at a minimum 105% of rated load X 37.5 volts, or 195 watts for a 5 Amp controller. The chip failure mode is determined by secondary breakdown characteristics. Power transistor chips with 75 Amp rating failed for the 5 Amp rated controller in the current limiting mode due to secondary breakdown characteristics. Chip size and geometry, rather than rating, determine the secondary breakdown characteristics. Power Tech MT-1010 was selected after comparison evalution with several other manufacturers' power chips. Power Tech discrete equivalent to the MT-1010 is their P/N PT-7501.

POWER DISSIPATION

While the controller is in short-circuit or current limiting mode, it is necessary to dissipate the heat generated in the power chip to the heat sink as rapidly as possible to limit the transistor maximum junction temperature to a safe value. The problem is complicated by the need to isolate the power chip from the controller case to meet the 1000V dielectric test. Further complications arise in that the temperature rise is rapid in the event of a short-circuit, and a temperature gradient develops from the heat sink to the isolator to the power chip. This develops mechanical stresses due to differences between coefficients of thermal expansion of the different materials involved. Large power chips are required for reasons of secondary breakdown characteristics, thus making thermal expansion problems more acute. Two methods of power chip mounting were investigated. One was to mount the chip with hard solder directly to a copper surge block of sufficient size to rapidly absorb the heat generated under fault conditions, in turn isolating the copper surge block from the controller case, Fig. 5. This procedure proved efficient. Another approach was to mount the power chip to the metalized Beryllia (BeO), which acts both as an insulator and a thermal conductor. The power chip and BeO assembly is in turn mounted to the copper header making up the case, which acts as an additional heat sink, Fig. 6. This method allows for appreciable weight saving and would be adequate for the 1 Amp controller. However, the heat problems are critical for the 5 Amp controller, and copper surge blocks were used for both the 1 Amp and 5 Amp controllers.

ISOLATION

A dielectric withstanding voltage of 1000 vAC (RMS) with a maximum leakage of 1.0 mA is required between all input terminals and output terminals. This applies for control (on-off and reset), short-circuit and current limiting interface,and trip indication. Isolation between control, short-circuit and current limiting, and trip indication is not required since all of these functions have a common DC ground in most applications. They can be isolated at the expense of additional componentry, cost, size and weight. Wherever applicable, opto-electro couplers are more efficient with respect to cost, size, weight, RFI and reliability than DC-DC converters utilizing transformers. Care is taken in the use of opto-electro couplers to allow for leakage currents at elevated temperatures and exposures to radiation.

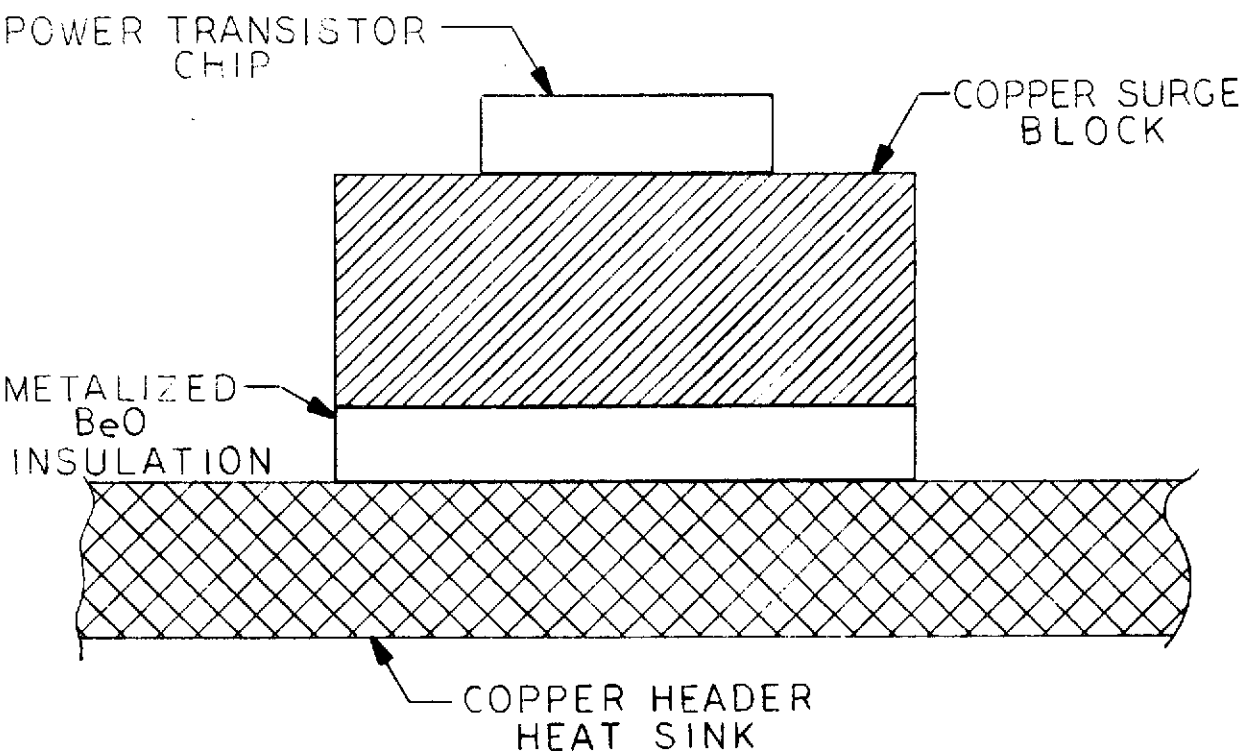


FIG. 5 POWER TRANSISTOR CHIP MOUNTED DIRECTLY TO COPPER SURGE BLOCK

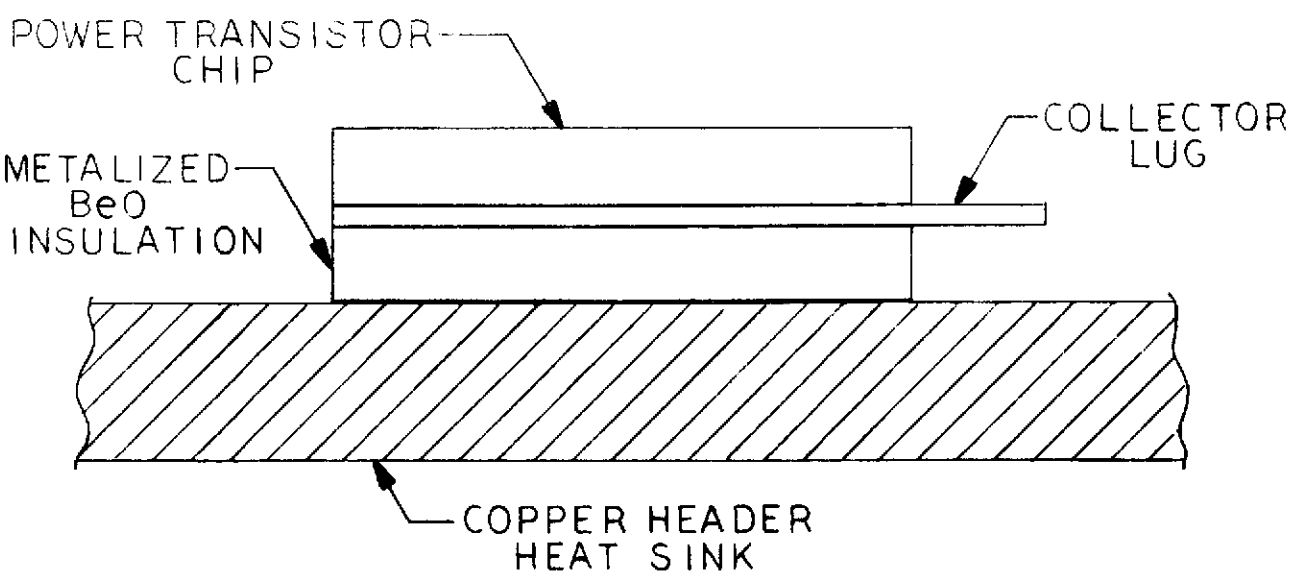


FIG. 6 POWER TRANSISTOR CHIP MOUNTED TO BeO INSULATOR TO COPPER HEADER HEAT SINK

CURRENT LIMITING

The characteristics and mounting of the power transistor chip determine the current limiting capabilities. It is believed that the optimum available chip has been selected. Its safe operating characteristics are illustrated in Fig. 7. Fig. 8 shows the voltage drop across the collector and emitter, with an 80 volt supply voltage for the 5 Amp rated controller. A locus of points for 105%, 110%, 120%, 130% and 140% current limiting conditions vs their respective voltage drops across the collector-emitter are superimposed on Fig. 7. These points are in a marginal region of the Safe Operating Region curves. The current limiting characteristics of MIL-P-81653 are shown in Fig. 9, which dictates fold-back current limiting. This is not recommended as it does not allow for full rated load to be applied under transient voltage conditions. Also, fold-back current limiting has a negative resistance characteristic which may cause serious instability (oscillation) with many reactive loads.

Analysis of the overvoltage problem yielded the following conclusion. The object is to protect the power transistor chip from excessive power dissipation and secondary breakdown. The most efficient method of doing this is to monitor the voltage across the power chip itself, rather than the supply voltage. With up to 37.5 volts across the controller, full current is delivered to the load. Above that voltage, the controller switches off if it is in a current limiting mode. (see Fig. 10) The 37.5 volt value was selected in order that with an 80 volt line surge, the controller would still deliver full rated current to the load. This system protects the power chip only when needed and does not interfere with normal operation. If the voltage surge (above 37.5 volts) occured simultaneously with a short-circuit, the actuator would trip-out immediately. If required, a 100 msec delay could be implemented before trip-out and still remain within the safe operating range of the power transistor chip. The controller will not trip-out under the increased load currents resulting from the voltage transients of MIL-STD-704 (Fig. 11). The time delay of 2 to 3 seconds is fixed for all conditions except the combined condition of overvoltage and short or near-short conditions, in which case the trip-out is immediate (or delayed for 100 msec if desired). Fig. 12 block diagram shows the basic function. The controller will be tripped after a 2 to 3 second delay if the overvoltage indication is not present. In the event of overvoltage, the trip-out is immediate. An overvoltage condition can not trip the controller by itself. It must be AND functioned with the controller in the current limiting mode for trip-out.

Schematic shown in Fig. 13 for the 1 and 5 Amp DC controller illustrates how current limiting and overvoltage projection are accomplished. Voltage across current sensing resistor R16 is supplied to operational amplifier U4. When over current exists, voltage is applied through emitter diode of opto-isolator U2, initating a timing circuit comprised of C1, R1, and R2. The output voltage through diode of U2 continues through R19, R20 and R17, providing feedback to operational amplifier U4 with Q7 being

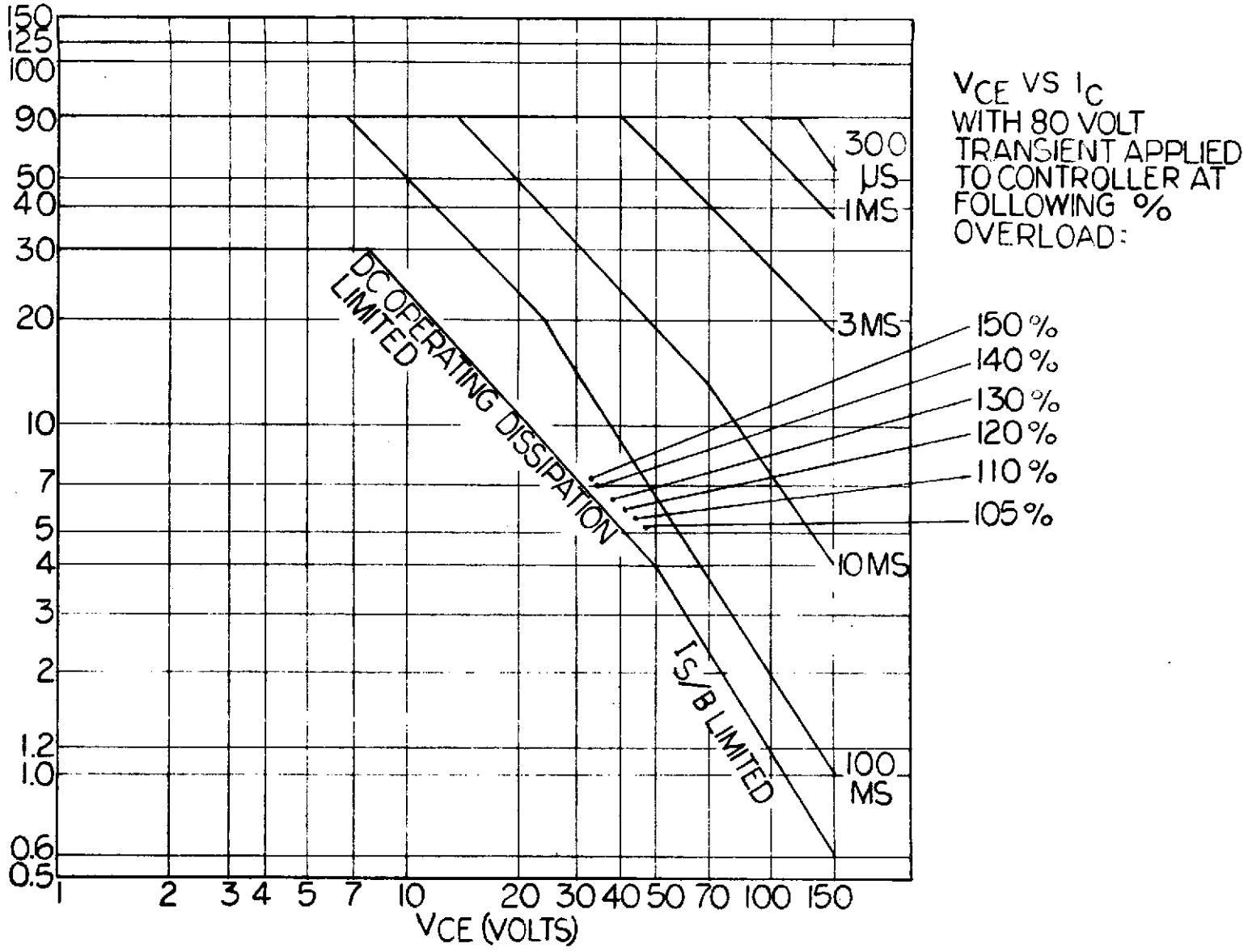


FIG.7 SAFE OPERATING AREA POWERTECH MT-1010 POWER TRANSISTOR CHIP

% OVER LOAD TRIP POINT	I_L AMPS	R_L OHMS	$I_L R_L$ VOLTS	V_{CE} VOLTS	$V_{CE} I_L$ WATTS
150	7.5	6	45	35	262.5
140	7.0	6	42	38	266.0
130	6.5	6	39	41	266.5
120	6.0	6	36	44	264.0
110	5.5	6	33	47	258.5
105	5.25	6	31.5	48.5	254

I_L = LOAD CURRENT

R_L = LOAD RESISTANCE

V_{CE} = VOLTAGE DROP ACROSS CONTROLLER

FIG. 8 EFFECT OF 80 VOLT TRANSITENT ON 5 AMP CONTROLLER SWITCHING INTO RATED LOAD

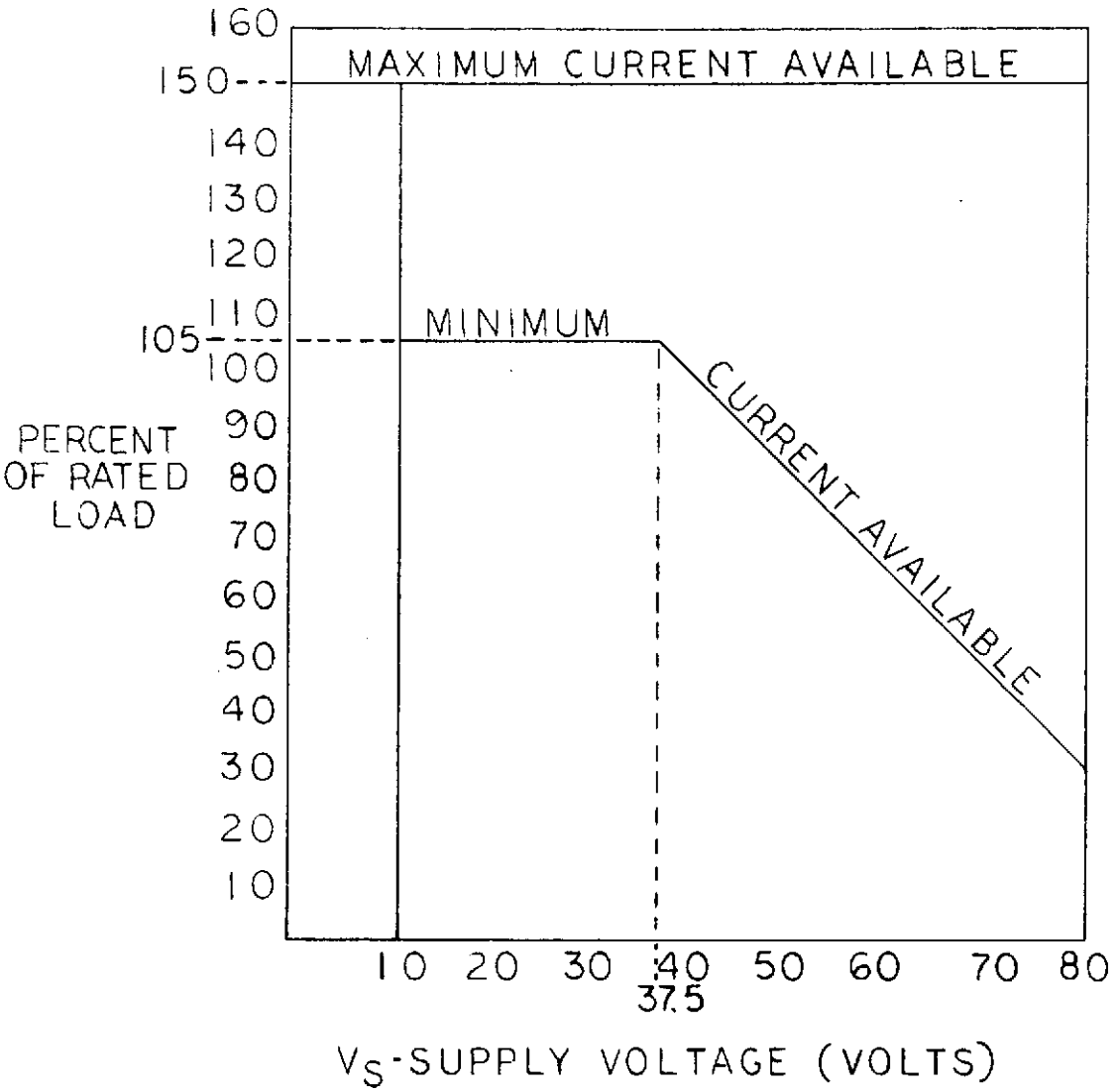


FIG. 9 MIL-P-81653 CURRENT LIMITING CHARACTERISTICS OF DC CONTROLLERS

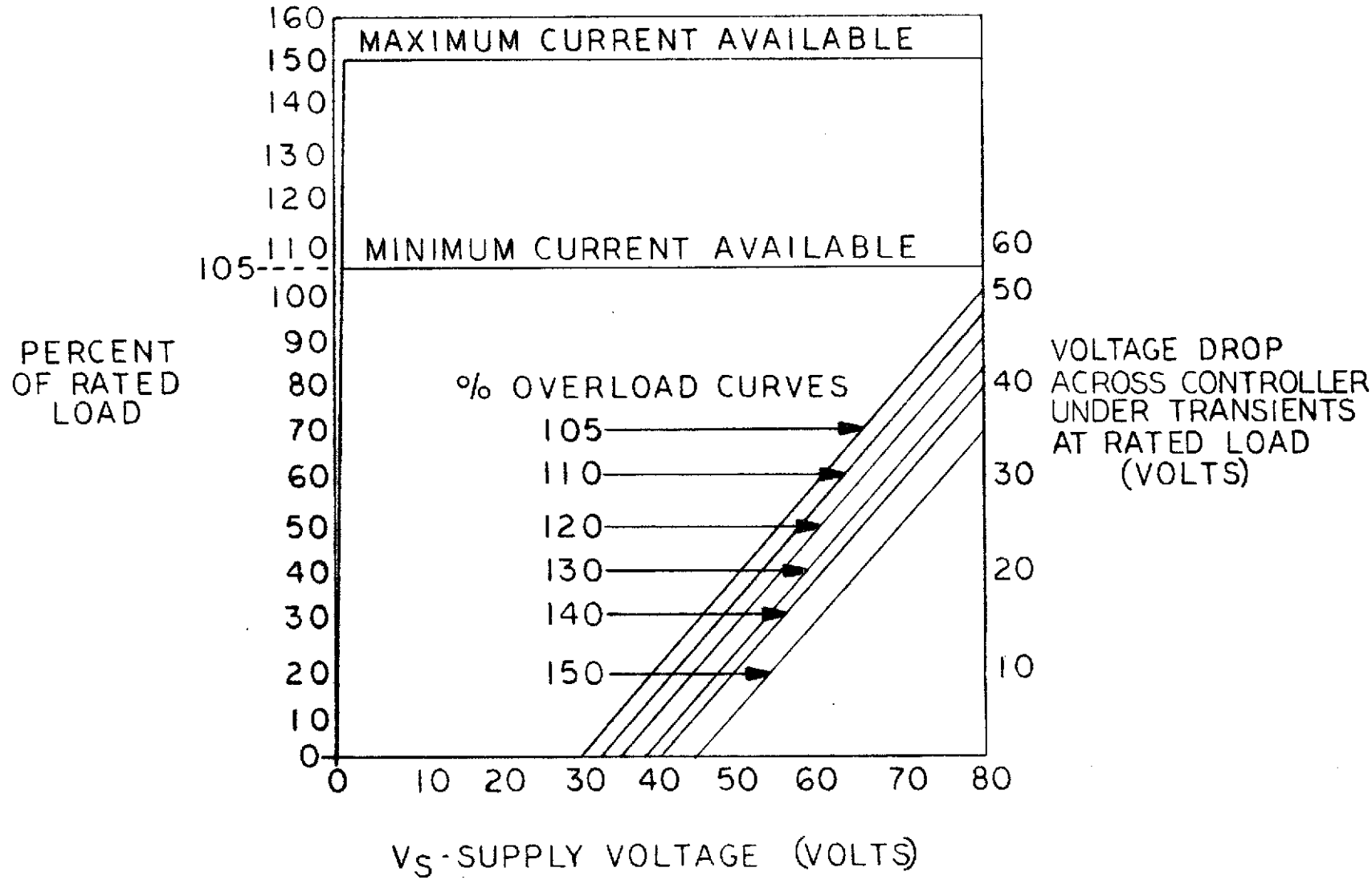


FIG. 10 CURRENT LIMITING CHARACTERISTICS TELEDYNE DC CONTROLLER AND VOLTAGE DROP ACROSS CONTROLLER UNDER TRANSIENTS

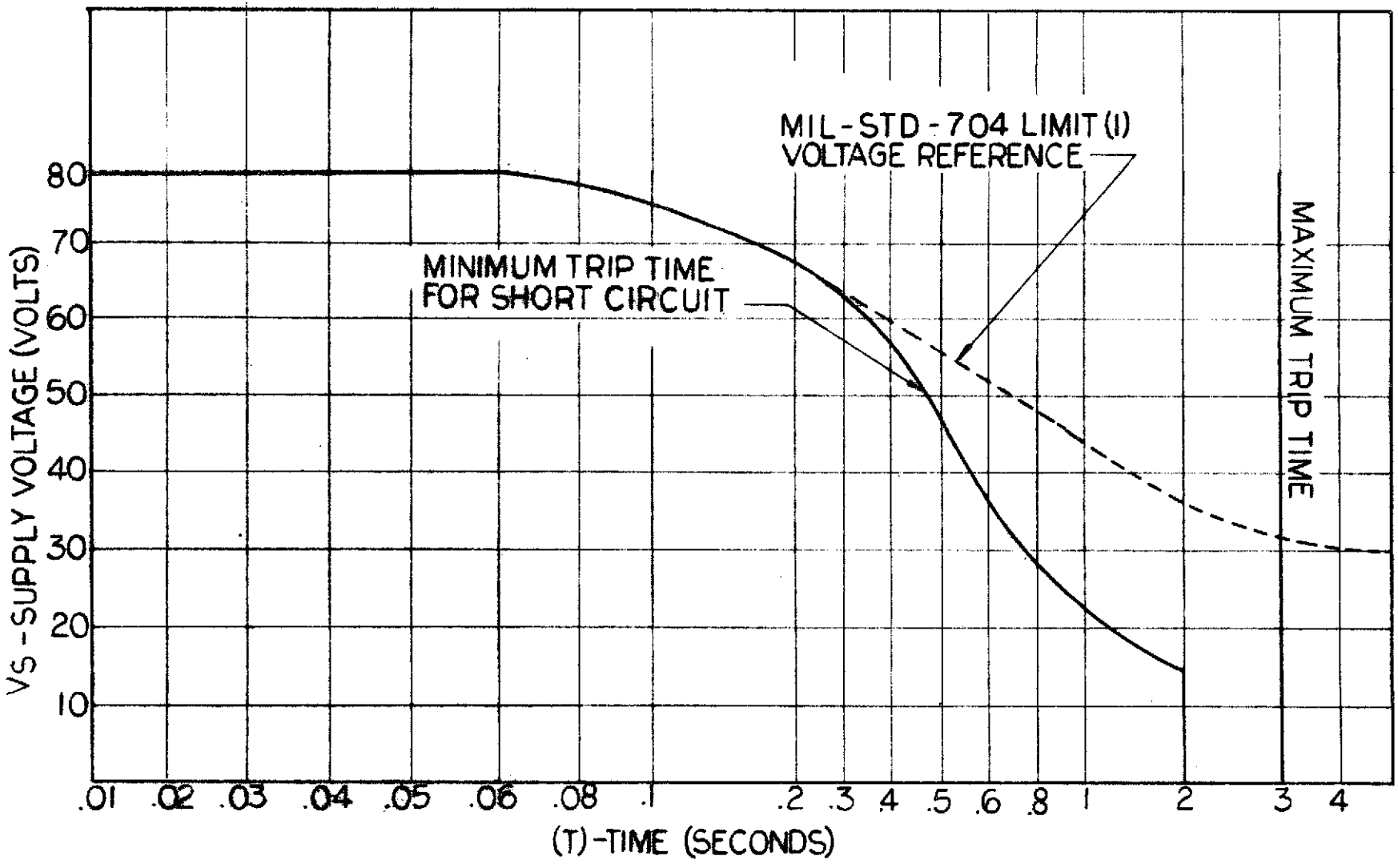


FIG. 11 MIL-P-81653 TRIP CHARACTERISTICS FOR DC CONTROLLERS IN CURRENT LIMIT MODE

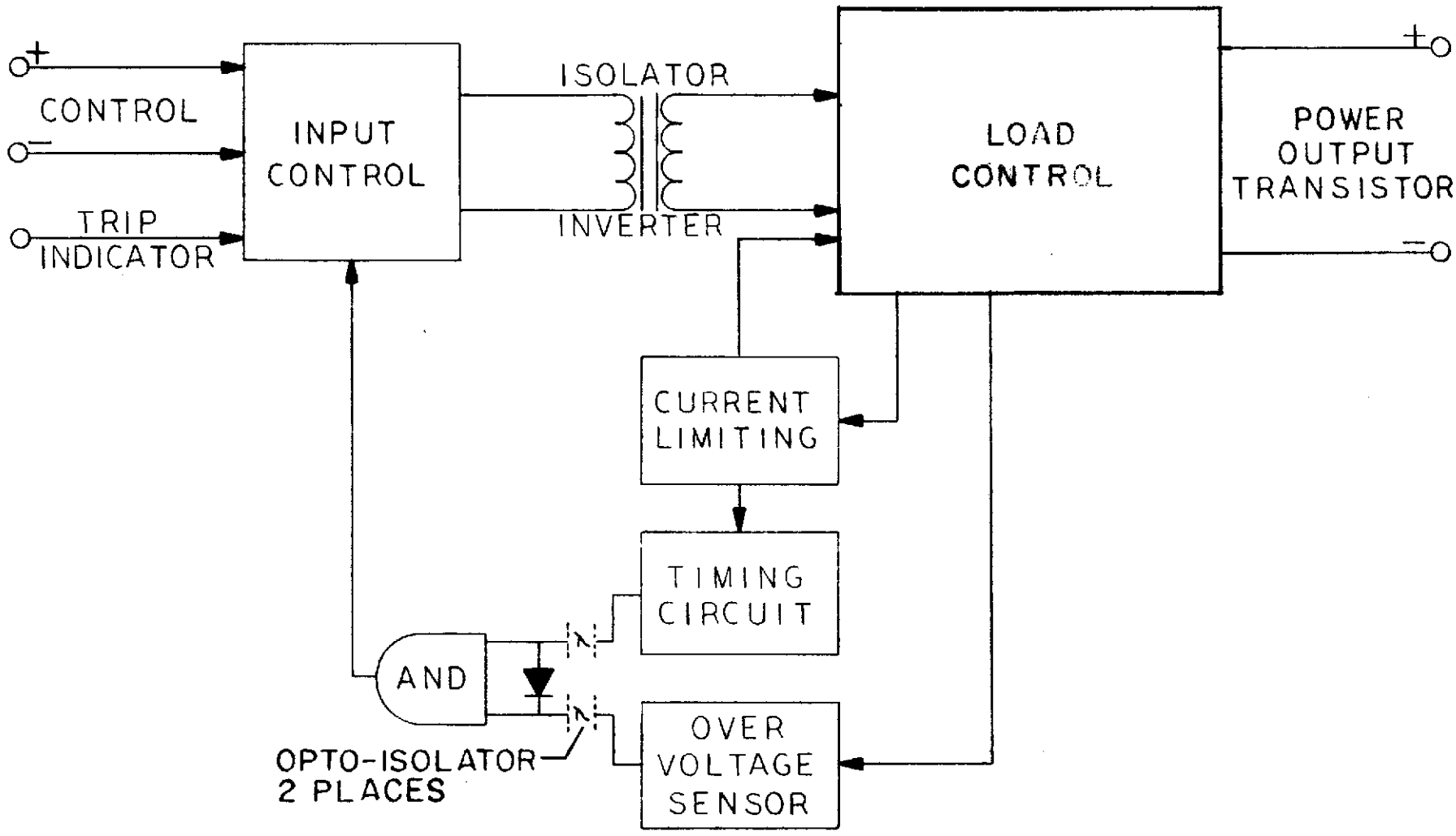


FIG. 12 FUNCTIONAL BLOCK DIAGRAM DC CONTROLLER

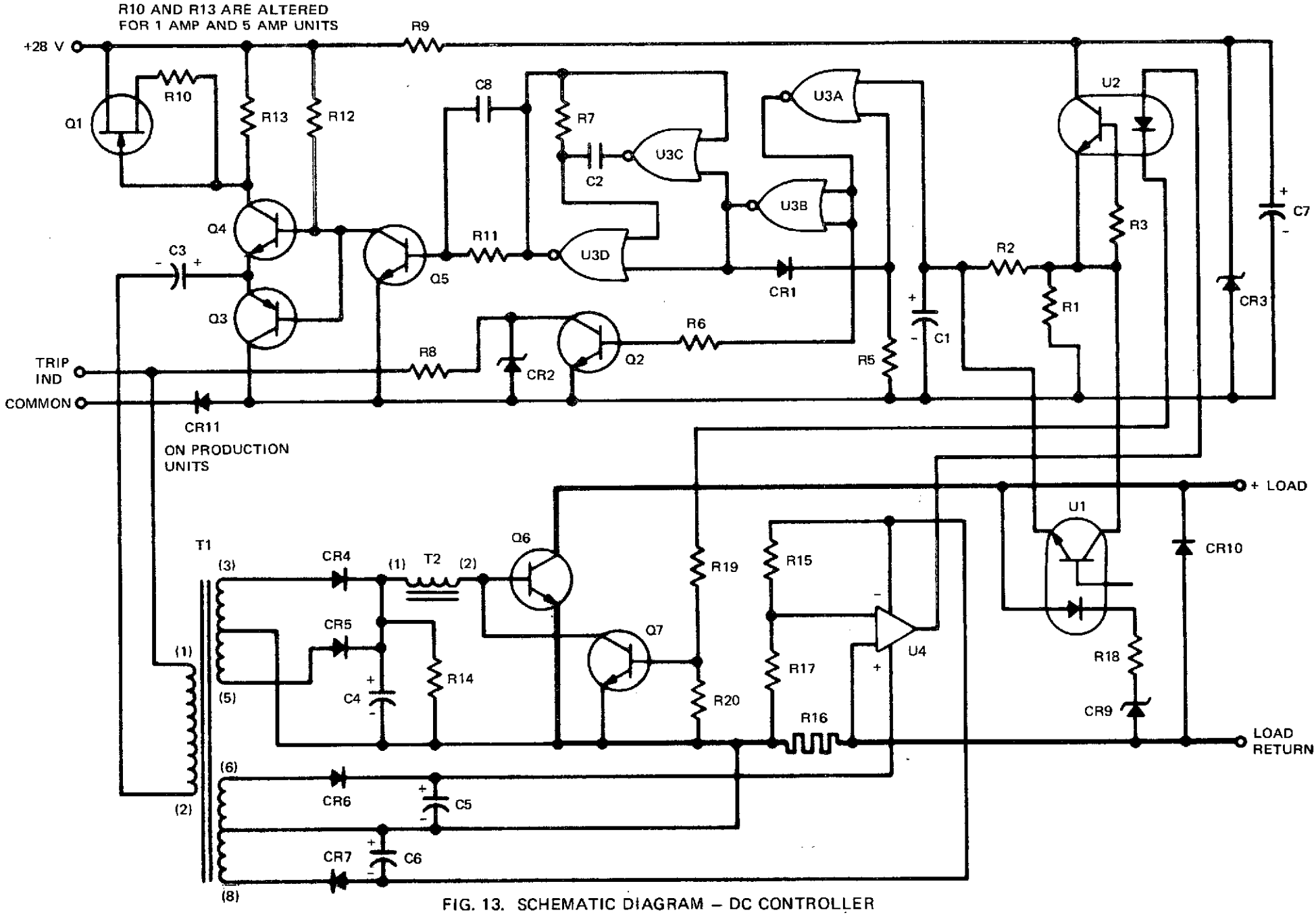


FIG. 13. SCHEMATIC DIAGRAM – DC CONTROLLER

biased to put Q6, the power transistor, in a constant current mode by virtue of the above-mentioned feedback. After the time delay of 2 to 3 seconds the gate of U3A goes to logic 1, inhibiting the oscillator consisting of U3C, U3D, C2, C8, R11 and R7, and the push-pull amplifier consisting of Q5, Q3, Q4, R13, R12 and C3. The trip-out is latched by virtue of feedback via CR1.

The overvoltage sensing circuit consists of opto-isolator U1, R18 and CR9. With 37.5 volts (36 volts zener and 1.5 volts diode drop of U1), current flow through diode of U1 with the transistor of U1 effectively short-circuiting R2 of the timing circuit allowing for immediate inhibition of the oscillator if the controller is in the current limiting mode. Remember the 37.5 volts is the voltage across the controller and not the supply voltage.

This circuit offers power transistor chip protection for overload and overcurrent conditions. It is protected against short-circuits in normal and overvoltage conditions. It allows the controller to supply full rated loads from 1 to 30 volts, and through transients to 80 volts with a wider margin against nuisnace trips. It deviates from MIL-P-81653 controller in that trip-out is faster under the combined conditions of overvoltage and short-circuit. In some schools of thought this is an attribute. Regardless, the overall advantages far outweigh the disadvantages of the above-mentioned current fold-back systems.

MIL-P-81653 allows for current limiting within 150% maximum and 105% minimum. Current limiting can be accomplished within a 20% band through temperature anywhere within the 105% to 150% range. Its location is optional. Prototype units were fixed at a 110% to 130% band. A band of 130% to 150% would provide greater pass current capabilities without effecting nominal load conditions.

CONTROL VOLTAGE SELECTION

MIL-P-81653 control voltage refers to Para. 3.1 , making control voltage a specification requirement for a specific controller. A 5 volt TTL compatible control voltage has been generally specified. It is considered that this control voltage is too low for aircraft and spacecraft use. The 2.5 volt threshold between "ON" and "OFF" conditions of the controller would be susceptable to voltage-induced noise. The 5 volt level increases the current requirements for transformer isolation and power transistor base drive.

The most efficient voltage to use would be the existing 28 volt bus. Transients can be readily suppressed and voltage levels reduced for internal logic functions. The 28 volt supply would prove most efficient for transformer coupling and opto-isolation. The controller would also be compatible with existing 28 volt systems. The 28 volt control system was employed in the prototype DC controllers after weighing size, cost, weight and reliability.

The purpose of the 5 volt TTL control is to have the controller operated directly from the computer. If direct computer control is essential, then HTL (High Threshold Logic) control voltage levels should be considered. HTL was specifically developed for the purpose of noise immunity for systems with far less hostile noise environment than aircraft or spacecraft. HTL has a minimum of 5.0 volt noise immunity and operates from a 15 volt supply which would be adequate for transformer coupling and opto-isolators.

TRIP INDICATION

Trip indication can be readily satisfied by either current sinking or voltage indication. Current sinking can be performed in either one of two conditions, light indication when controller is tripped or light off when controller is tripped. The latter method has the advantage in that it also gives positive indication that control voltage has reached the controller by having the light "ON" in the untripped condition. It has the disadvantage that a light turning off is not as distinct a visual indicator of a change in condition as a light turning on. This method was used in the prototype controllers since the current sinking method of trip indication was to be investigated, and this method does afford the dual function of trip indication and wiring integrity to the controller. The circuit schematic, Fig. 13, shows how trip indicating transistor Q2 is forward biased from NOR gate output of U3A. By connecting the base of Q2 to NOR gate output of U3B, trip indication with the light going on rather than off would be accomplished.

Trip indication by means of voltage indication can be readily performed by connecting the collector of Q2 through a resistor to the 28 volt control supply, and Q2 forward biased as an indication of trip; that is, connecting the base of Q2 to the NOR gate output of U3B. This system would give both trip indication and control voltage wiring integrity indication. By simple circuitry at the receiving point of indication, a lamp could be turned on when trip occurs. Voltage indication would be 28 volts no trip and .4 volts tripped.

STATUS INDICATION

An ideal status indicator would show flow of current to the load with the controller on. This would indicate wiring integrity to the controller and from the controller to the load. A pure voltage indication at the controller output does not indicate voltage to the load, only voltage to the controller output. It does not indicate wiring integrity from the controller to the load. A status indicator based upon current flow to the load was developed. The principal was similar to the current limiting approach described earlier, ie. a voltage differential was detected across a current sense resistor in the power line and fed into an operational amplifier which biased a signalling transistor. The gain of the amplifier was set to detect current flow of 50 mA or more. A simplified schematic is shown in Fig. 14. Supply voltages for the operational amplifier were from the same source as for the operational amplifier used in the current limiting function. Because of the limited number of prototype units contracted which eliminated hybrid-microelectronic manufacturing concepts, it was impossible to package this status indicating circuit in the size package established for the prototype units. This status indicating feature could be incorporated in production warranting hybrid-micorelectronics.

If it is desirable to fully isolate a fault to the load, to the controller, to control wiring, to load wiring (from the load supply to the controller and controller to the load), a load voltage sensor would be required at the controller load input and controller load output. This would mandate a 3-terminal output configuration.

RESET

After the controller has tripped, resetting is accomplished by removal of control voltage and re-application of control voltage. A seperate reset circuit could be implemented by forward biasing through a coupling capacitor, a transistor located between output of U3B NOR gate and input to U3A NOR gate, Fig. 13. This would remove the latch voltage applied to input of U3A through diode CR1.

The time for re-applying control voltage for resetting is 80 msec minimum. This time is dictated by capacitor C7 of Fig. 13. In addition, the capacitor must be of sufficient capacity to filter high voltage transient spikes. The 80 msec interval requested before re-applying control voltage following a trip-out should not be detremental to circuit function.

TRANSIENT VOLTAGE PROTECTION

Control Input Transients as specified in MIL-P-81653 will not damage the controller. The Operating Voltage Transients as specified in MIL-P-81653 can be satisfied. The requirements of Transient Spike Overvoltage ($\pm$ 600 volts) of MIL-P-81653 cannot be satisfied. The controller will not be damaged by these transients. A $\pm$ 600 volt transient applied to the power input terminal will be passed to the power output terminal for the duration of the transient (.6μsec.). Power transistors suitable in chip form that would satisfy all the requirements of the power chip are not available with a 600 Vceo rating.

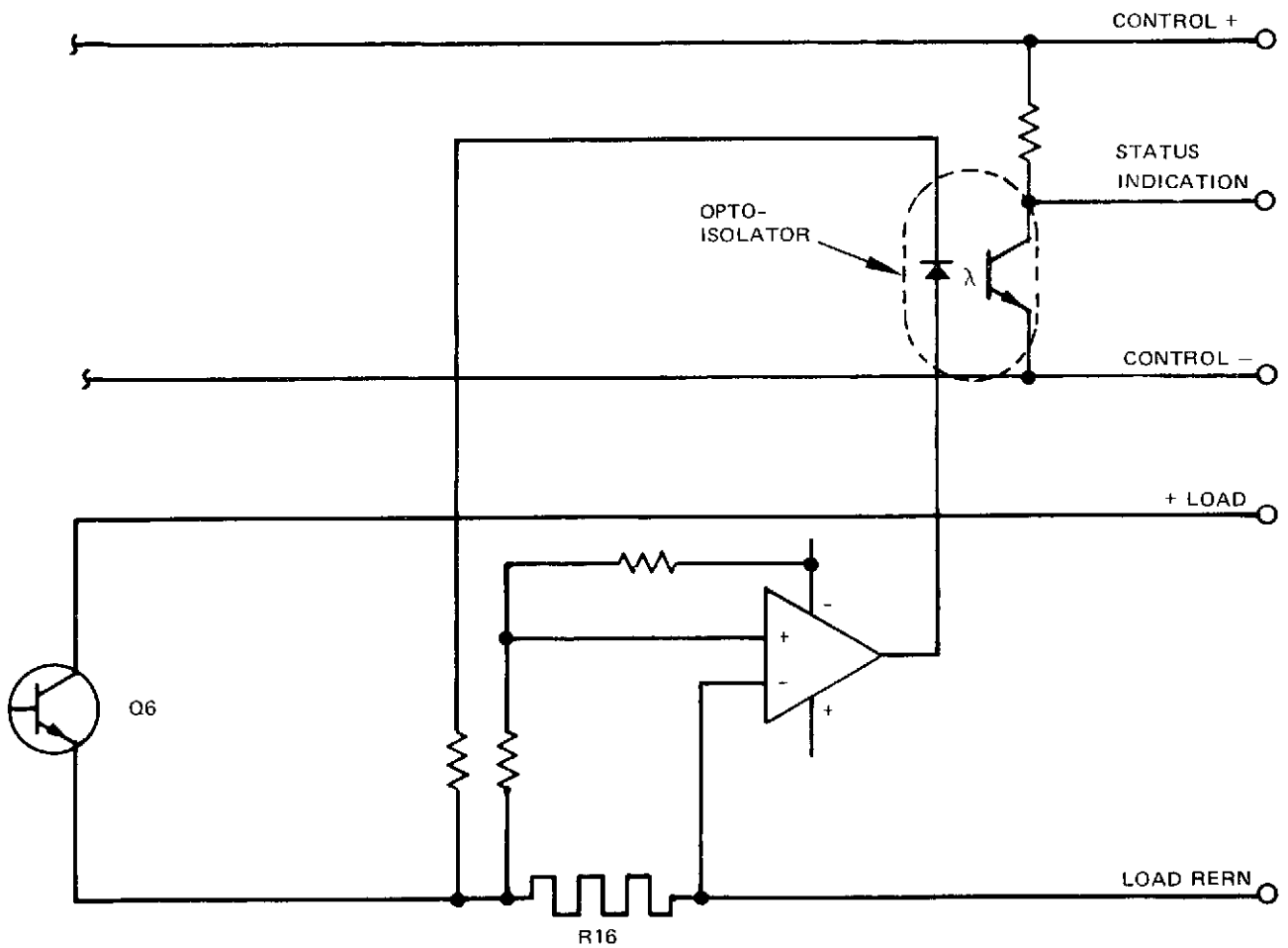


FIG. 14. STATUS INDICATOR SIMPLIFIED SCHEMATIC

FUSING (FAIL SAFE)

The fusable link requirement is met by insuring that the bond from the emitter of the power transistor is the smallest cross-section conductor in the power system. MIL-P-81653 specifies that in the event of a failure of the controller in a shorted condition, the controller shall fail open within 4 seconds when a current corresponding to 50% of the square root of the specified I^2t value is applied, namely 18 Amps for the 1 Amp controller and 32 Amps for the 5 Amp controller. The fusable link requirement was included in the prototype controllers. Tests were not conducted to determine exact current/time limits. In flight hardware, this specification can be met.

The fuse link raises problems of arc extinction and other phenomenon in high current fuses, to ensure the desired protection of the spacecraft. The proposed method of controlling this is with the use of a stable liquid such as silicone oil or a flourocarbon. There has been previous experience using these types of fluid for purposes of controlling arcing. There are other benefits to be derived from fluid filling. One is the additional heat paths due to conduction and convection that tend to equalize temperatures within the package and minimize hot spots. This would be particularly beneficial to solid state switches. There are also proven benefits of fluid-filled devices with respect to mechanical shock and vibration conditions. Under short duration mechanical shock, the fluid acts as a solid and gives support to all the components it surrounds. Under mechanical vibration, the oil acts as a viscous damper for any resonant conditions. Considerations are made for fluid expansion under differentials to atmospheric pressure and temperature. Fluid filling is proposed for flight controllers, and the possibilities of a replaceable fuselink should be considered in future studies.

FOUL-UP PROTECTION

Since the controller is polarity-sensitive, it can be destroyed in test and installation by improper wiring, ie. not observing polarities. Diodes could be used to protect against this condition, but would constitute a .7 plus additional voltage drop in the power circuit. Diode protection can be used in the control and trip-indicating circuits without difficulty. They were omitted in the prototype units and can be included in flight units as indicated in the schematic, Fig. 13.

The controller is intended to operate on bi-level control voltages. Slow ramp or gradual increase or decrease of control voltage could destroy the controller. This possible problem area could be eliminated by snap-action on turn-on and turn-off, however this feature would be at the expense of size, weight, cost and reliability due to the additional components.

Rapid sequential switching of reset with the controller switching into a short-circuit, could be damaging. The controller can be reset once within the 80 msec minimum. No positive protection against damage from repetitive rapid cycling can be incorporated without extensive circuitry. Functionally, repetitive recycling is not required. Caution should be exercised in testing and computer programming of the reset function of the controller.

FOUL-UP PROTECTION (Continued)

The controller is designed for considerable abuse. Properly wired, tested and installed, it should prove trouble-free. With the theory, "If something can be fouled-up, it will be", the above possible areas of concern are noted.

CIRCUIT SCHEMATIC

The circuit schematic of the 1 Amp and 5 Amp DC controller is shown in Fig. 13. The two units are identical except for input impedance and gain of the operational amplifier for current limiting. The functions of the schematic have been discussed under each individual function heading.

PACKAGING

The prototype 1 Amp and 5 Amp DC controllers delivered to NASA Manned Spacecraft Center consisted of discrete component packaging, with the exception of the power transistor chip. The outline drawing of the 1 Amp and 5 Amp DC controller is shown in Fig. 15. The method of internal assembly is shown in Figs. 16, 17 and 18.

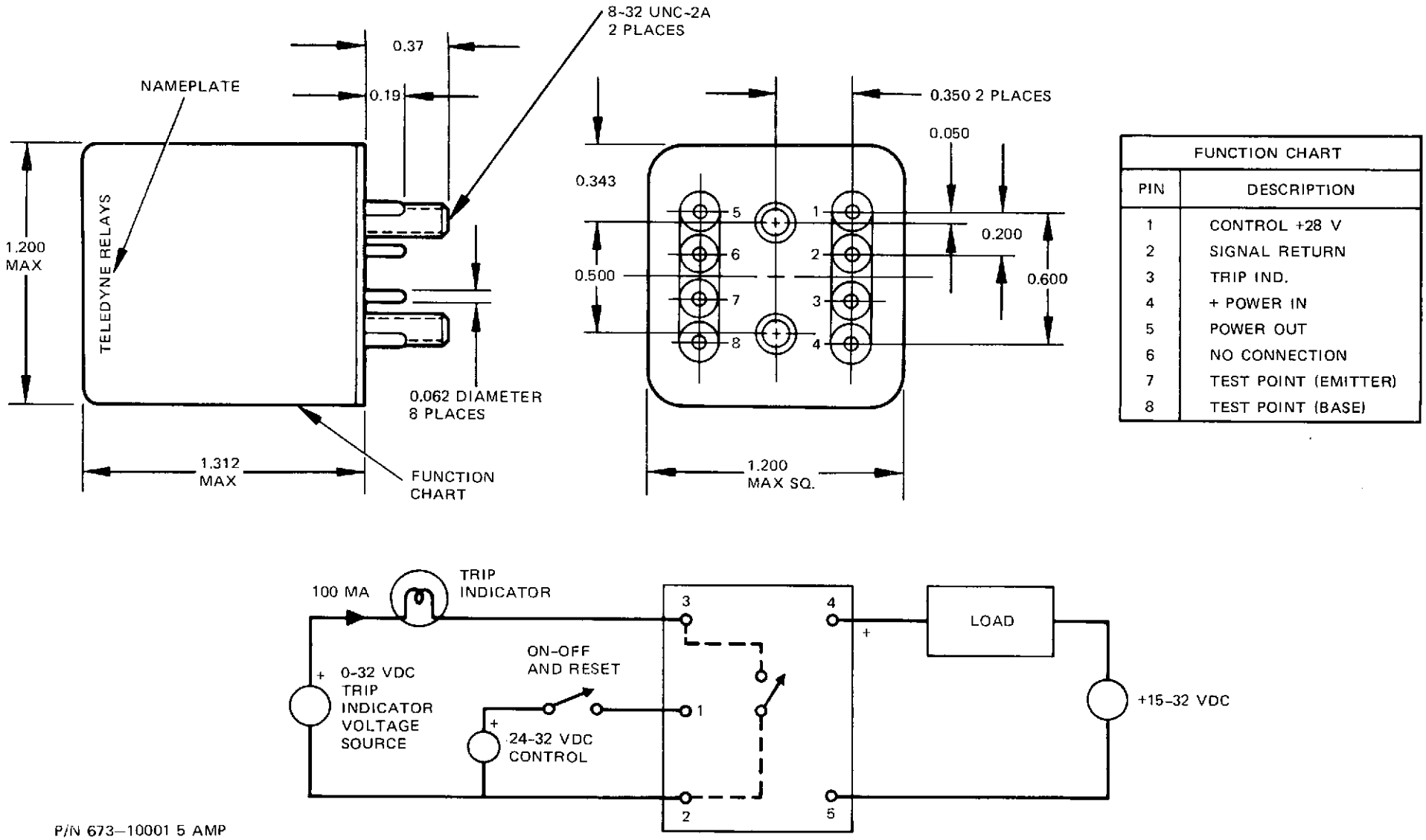
Intensive study was made of packaging for flight hardware controllers utilizing hybrid-microelectronic principals. Based on an analysis of the circuit complexity and the thermal and environmental considerations, the following was established as reasonable size and weight targets.

Size: 1 cu. in. max.
Weight: 2.5 oz. max.

The control circuitry will be in one hybrid-microelectronic package.

Teledyne, through its Microelectronic Operations, has been engaged in the development and production of hybrid-microelectronics for the past nine years. Over 500 different configurations have been designed and produced, with a total quantity of over 400,000 packages delivered. Teledyne pioneered in the technology of manufacturing and testing of these devices in large-scale economic production. These hybrid packages have been used in numerous high reliability aerospace systems. This has demanded the development of extensive 100% screening procedures that in some cases exceeded the requirements of MIL-STD-883 to ensure the necessary reliability.

The circuits involved are both analog and digital and the circuit components include bipolar integrated circuits and transistors, FET devices, diodes, resistors and capacitors. For digital applications, a package typically houses 25 integrated circuits, with some as high as 32. For analog applications, a typical package may contain up to 70 components with a mix of integrated circuits, transistors, resistors and capacitors. The range of power densities has been from 6 watt/in to 32 watts/in and all package designs have provided for heat sinking in the system application. Since some system applications have used from 200 to 1000 of these packages in an extremely



FUNCTION CHART	
PIN	DESCRIPTION
1	CONTROL +28 V
2	SIGNAL RETURN
3	TRIP IND.
4	+ POWER IN
5	POWER OUT
6	NO CONNECTION
7	TEST POINT (EMITTER)
8	TEST POINT (BASE)

P/N 673–10001 5 AMP
P/N 673–10004 1 AMP

FIG. 15. OUTLINE DWG – DC CONTROLLER

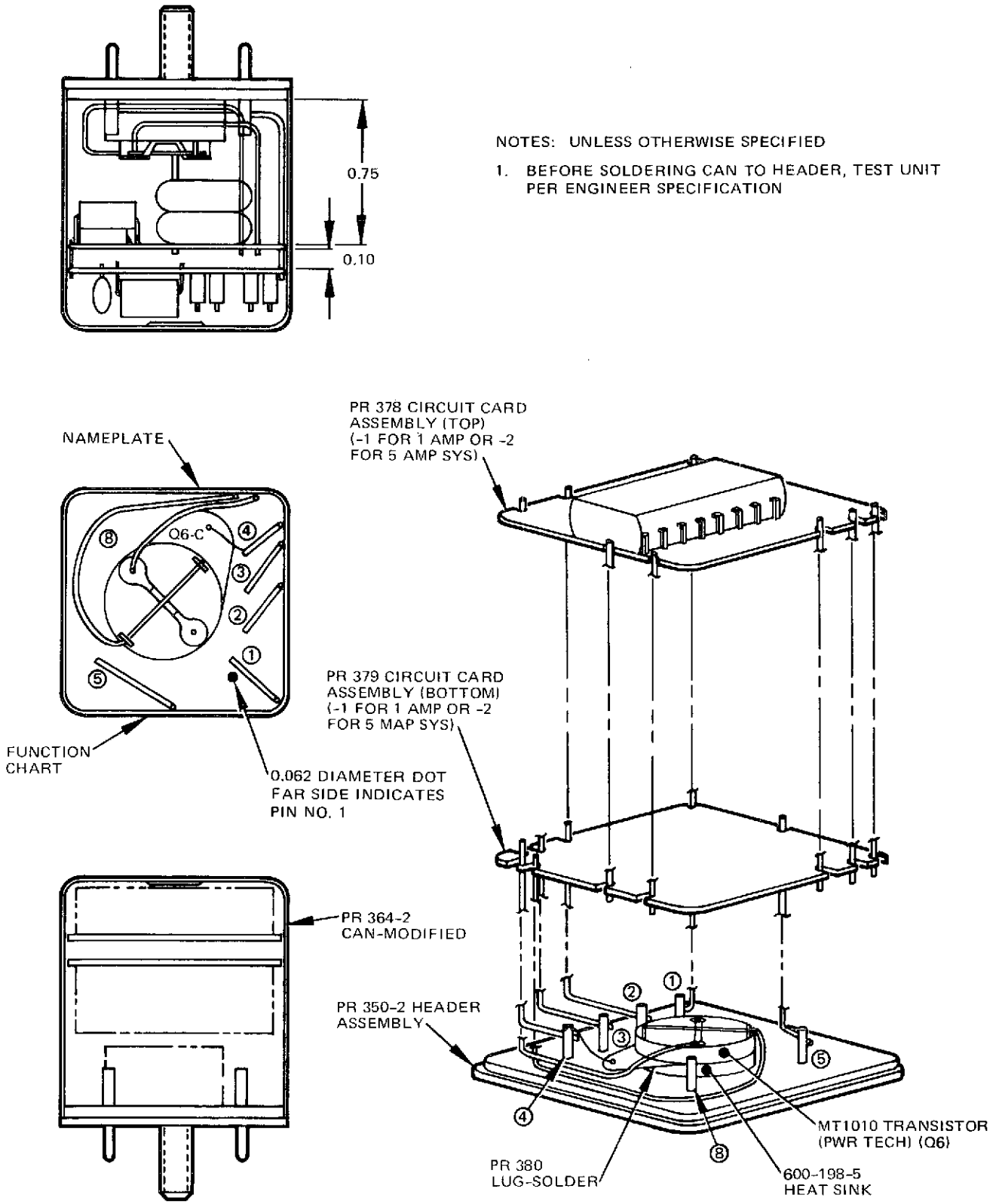


FIG. 16. ASSEMBLY LAYOUT 1 AMP AND 5 AMP DC CONTROLLERS

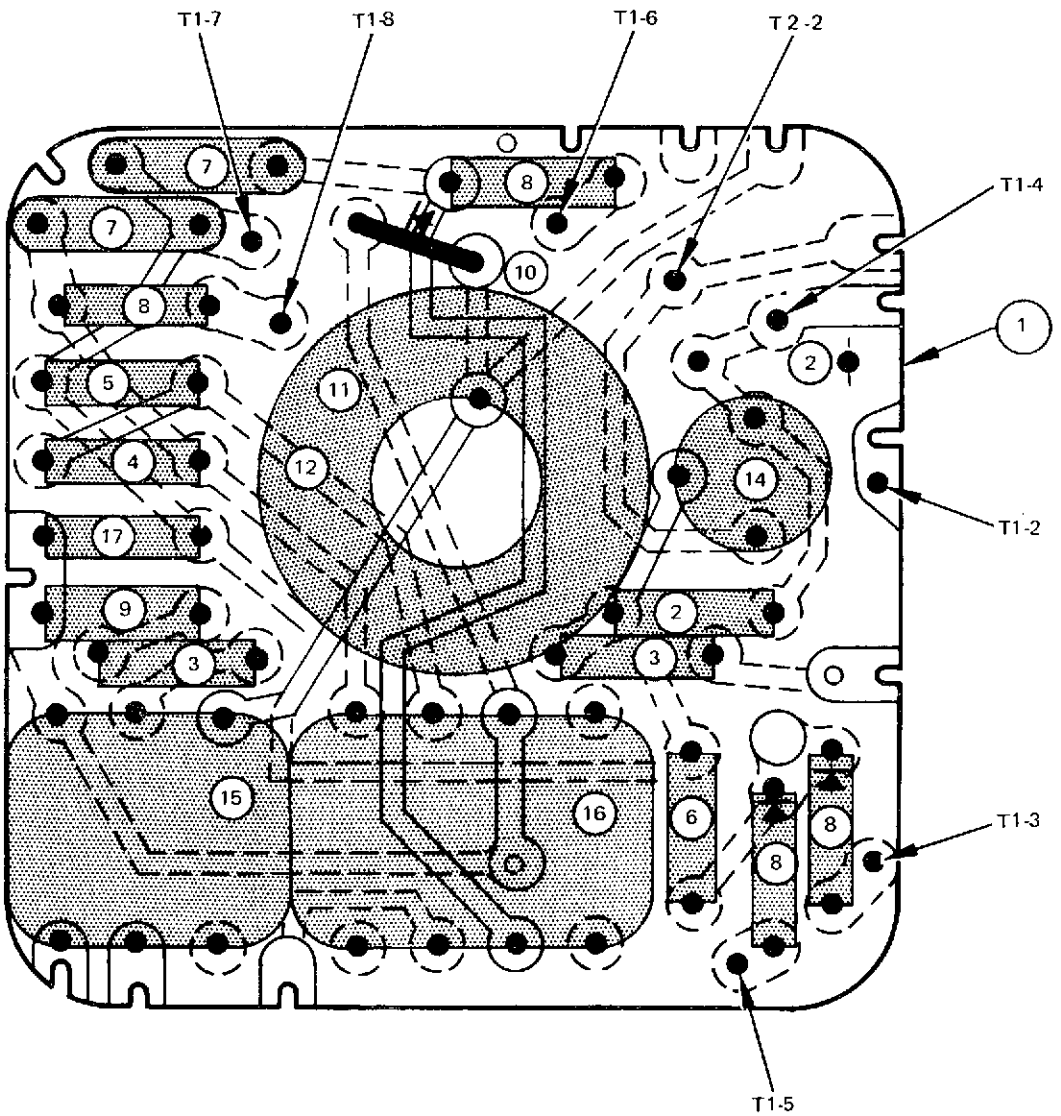


FIG. 17. CIRCUIT BOARD ASSEMBLY – BOTTOM, DC CONTROLLERS

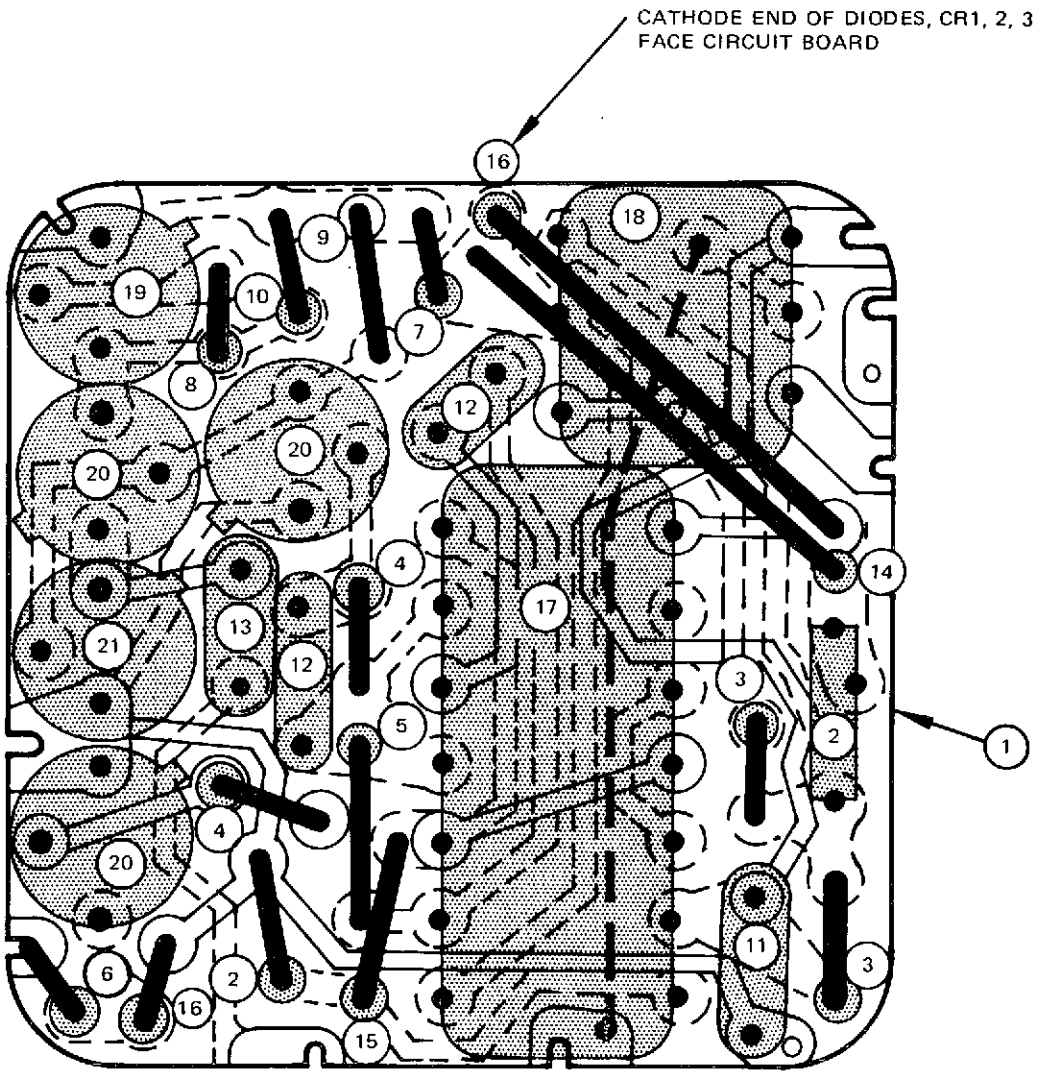


FIG. 18. CIRCUIT BOARD ASSEMBLY – TOP, DC CONTROLLER

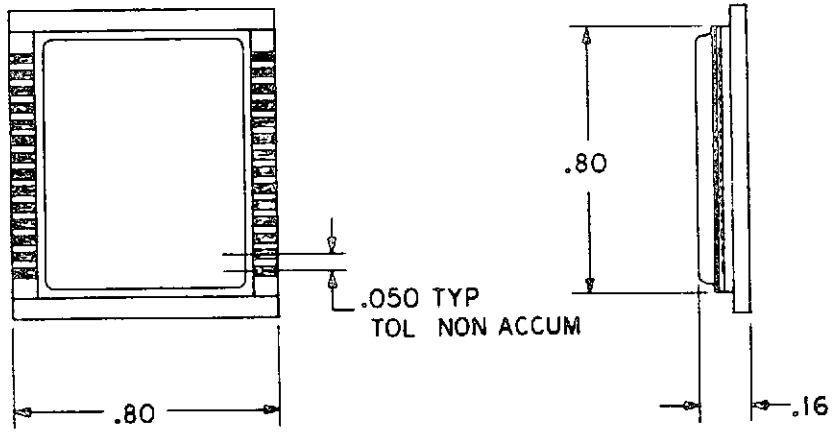
dense array, the thermal problem has received considerable attention. This extensive background is directly and ideally applicable to the specific problems of the solid state power controllers.

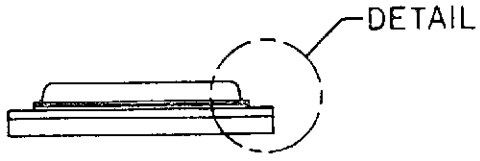
Some of the control circuitry will be in the form of MSI integrated circuits and it appears the component count to be packaged will be in the order of 40. This would exclude the optical isolators and a few additional power devices. The mechanical dimensions of the end item power controller establishes the size of the hybrid package, but from preliminary estimates it appears that a package size of approximately 0.8 inch X 0.8 inch X 0.160 inch would result. This size package could reasonably accommodate the components mentioned above, and therefore there would be one hybrid control package per power controller. The substrate power dissipation is estimated to be in the range of ½ watt.

The key factors determining the hybrid package design for this application are the reasonably high power dissipations mentioned above and the maximum heat sink temperature. This dictates that this hybrid package must have the lowest possible thermal resistance from the components to the heat sink, and rules out any simple mechanical contact interfaces between the substrate and the heat sink. The substrate will be beryllium oxide ceramic which has the highest thermal conductivity of any known electrical insulating material (2.6 watts/CM/°C). The ceramic will be 0.025 inches, which will give adequate strength for this size substrate. To implement the maximum thermal conductivity rule, a copper strip in the order of 0.025 inch thick would be brazed to the bottom of the ceramic substrate, providing the best possible thermal path to the heat sink. This copper would equal the width of the ceramic in one dimension, and extend beyond it in the other dimension to engage a support structure for mechanical mounting in the power controller, which is also the heat path. This is shown in Fig. 19.

The ceramic metallization required to provide a base for this copper braze operation can be either moly manganese or thick film gold-palladium. The advantage of gold-palladium metallizing is that its firing temperature of 900°C causes no warping or introduction of camber to the ceramic, as opposed to the 1540°C firing temperature for moly manganese which can reintroduce cambers in the order of 1 mil/inch, which are acceptable but less desirable.

Therefore, the program would proceed with the thick film gold-palladium approach for ceramic metallization. The exit pads for the package, as shown in Fig. 19, would be thick film stripes emerging from under the cover seal area, appearing as exposed pads on the ceramic surface along two edges. They would be on 0.050 inch centers, which is industry standard, and leads can be bonded by either welding or reflow solder techniques. The insulation for the cover seal land area is provided by silk-screened and fired glass inks or fired glass preforms, to give adequate insulation path to the cover to meet the electrical requirements of the specification. Gold-palladium metallization on the top of this glass insulation provides the solder base for cover seal. The proposed metallization system for the active portion of the substrate is a dual system. Gold-palladium ink would be screened on and fired to form the component mounting pads. This would actually take place at the





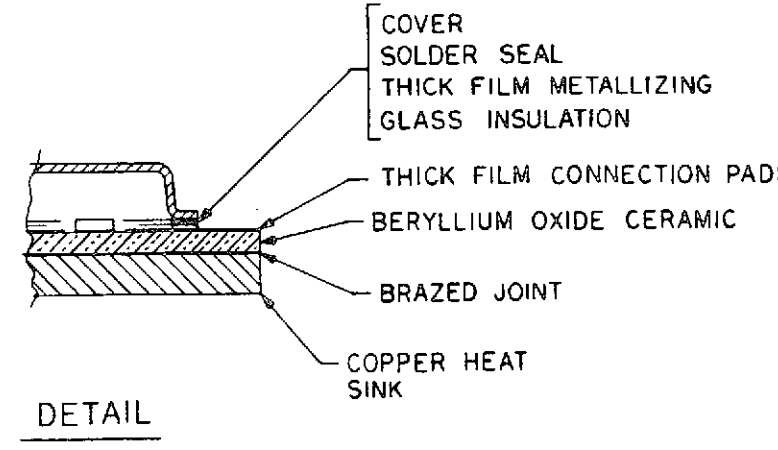


FIG. 19. CONCEPTUAL PACKAGING LAYOUT FOR HYBRID CONTROL CIRCUIT ASSEMBLY

same screening operation as the package exit pads. Aluminum would be evaporated with an undercoat of nichrome over the entire active area. The aluminum thickness would be 250 microinches, which gives the desired resistivity of 5 milliohms per square. The surface would then be coated with photo resist and exposed with the desired substrate wiring pattern.

After developing and processing, the aluminum is protected by resist, where the conductive pattern is desired, and the aluminum is bare where it is to be removed. The substrate is immersed in an etch bath and the aluminum is removed from between the desired conductive strips in the circuit pattern, and also from the component bond pads to re-expose the bare gold-palladium surface.

The aluminum system was chosen to allow a monometallic bonding system with aluminum dice pads, aluminum wire and aluminum substrate bond areas. The advantage of this is the total elimination of potential intermetallic problems. This is particularly important in this application since the temperatures will be in the region of 125°C or slightly higher, and long life at these temperatures is required.

The dual system with gold-palladium is necessary to provide a solderable metallization for component attach, since aluminum is not wettable by solders on a practical basis. The role of the evaporated film of nichrome under the aluminum is twofold. First, it is routinely used as an intermediary to strengthen the bond between evaporated metal films and either glass or ceramic substrates. In this case it serves an important secondary role of acting as an effective diffusion barrier between the aluminum and gold-palladium where they are in contact. Engineering tests involving thousands of hours at 200°C indicate that the nichrome is an excellent diffusion barrier, and no evidence of intermetallics have ever been found in the proposed metallurgical system.

Component attach technology will follow standard production procedures. The component wire bonding will use aluminum wire with ultrasonic welding, which is standard procedure. Circuit analysis is routinely done to establish electrical current values in the wire bonds to determine wire size requirements. For typical signal type currents, 1 mil diameter wire is used. For higher current capability, 1-½ mil or 2 mil diameter wires are used, and in some cases multiple parallel wires have been used.

The hybrid control package will be covered and hermetically sealed by normal processes, even though it will be contained in the hermetically sealed solid state controller case. This is to give adequate protection for internal handling through screening and environmental test procedures, as well as handling during final assembly in the end product. It is also necessary in view of the propose fluid filling of the end item device.

The normal Teledyne high reliability screening procedure will be used on a 100% basis for all the hybrid packages for this program. These screening procedures are listed in detail in Table 1.

TABLE 1. Screening Procedures for Hybrid Control Circuits

	TEST	SCREENING CRITERIA
1.	Incoming dice visual inspection	Criteria based on MIL-STD-883 method 2010 test Condition A.
2.	Post-die attach visual inspection	
3.	Pre-cover visual inspection	
4.	Stabilization bake	MIL-STD-883 method 1008 test Condition C (150 C) 72 hrs.
5.	Temperature cycling	MIL-STD-883 method 1010 test Condition C (-65°C) and +150°C) 22 cycles.
6.	Mechanical shock	MIL-STD-883 method 2002 test Condition B (1500G, ½ ms) 5 impacts Y axis.
7.	Hermeticity a) Gross	MIL-STD-883 method 1014 test Condition C, step 1.
	b) Fine	MIL-STD-883 method 1014 test Condition A except packages are helium filled at seal.
8.	Burn-in	MIL-STD-883 method 1015 test Condition B 160 hrs. @ 125°C junction temperature.
9.	Electrical test	Per hybrid specification.
	a) DC parameters at 25°C and at max. and min. rated operational temperature.	
	b) AC parameters at 25°C and at max. and min. operational temperature.	
	c) Final Functional test at 25°C.	
10.	External visual	MIL-STD-883 method 2009.

TECHNIQUES

The packaging utilizing hybrid-microelectronics and in accordance with MIL-P-81653 concepts is shown in Fig. 20. In this case, the basic assembly would consist of the copper heat sink base, power chip, hybrid control circuit package and miscellaneous components such as the optical isolators (which are themselves hybrid circuits). The hybrid control circuit with its copper heat sink strip is mounted to copper support members which are brazed to the copper heat sink base. It is proposed to use slots in these members as shown in the drawing, to engage the copper strip of the hybrid package and solder this joint to minimize thermal drops. Any diaphram effects in this mechanical mounting system would be minimized by fluid filling.

A deck is provided above the hybrid circuit to provide a mounting board for the optical isolators. These are very low power generating components and the increased distance from the heat sink has no adverse thermal effects.

The method of fluid filling electrical devices must contend with the temperature coefficient of expansion of the fluid, which should be minimized. One common method is to fill the device and seal it off at the maximum operating temperature or slightly over. In this case, about 125°C. Then at all future operating conditions, there will be less than atmospheric pressure within the device, and the differential to atmosphere can never exceed 15 psi under any conditions. If the unit were sealed cold, the interior pressure would be higher than atmospheric at elevated temperature, and there is no limit to the pressure differential that could build up.

The hermetic seal of the package cover seam would be done prior to fluid filling and it is proposed to use either electron beam welding or laser welding. The final seal would be accomplished with a pinch-off tube.

An alternate approach to packaging is shown in Fig. 21, with two significant modifications. First, the terminations are brought out on a surface 90 from the mounting (heat sink) surface. This affords several benefits:

a. Increases heat sink area.
b. Facilitates implementation of an Integrated Wiring Termination System (IWTS).
c. Improves ease of replacement.

Secondly, it is proposed to use mounting flanges in lieu of mounting studs to further maximize heat sinking.

Referring to Fig. 21, an L-shaped structure is proposed to provide rigidity and mechanical strength between the heat sink plane and the lead/terminal plane. The power switching devices are again mounted on the heat sink as discussed previously. The hybrid package is mounted to the heat sink by the same structure proposed for the 1 inch cube package, and the transformer deck is the same. This package calls for wire exit leads. To maintain hermeticity and still provide leads, it is proposed to use a hermetically sealed header to bring the leads through the package wall. The external wires would be soldered to the header pins and potted for general protection in that area.

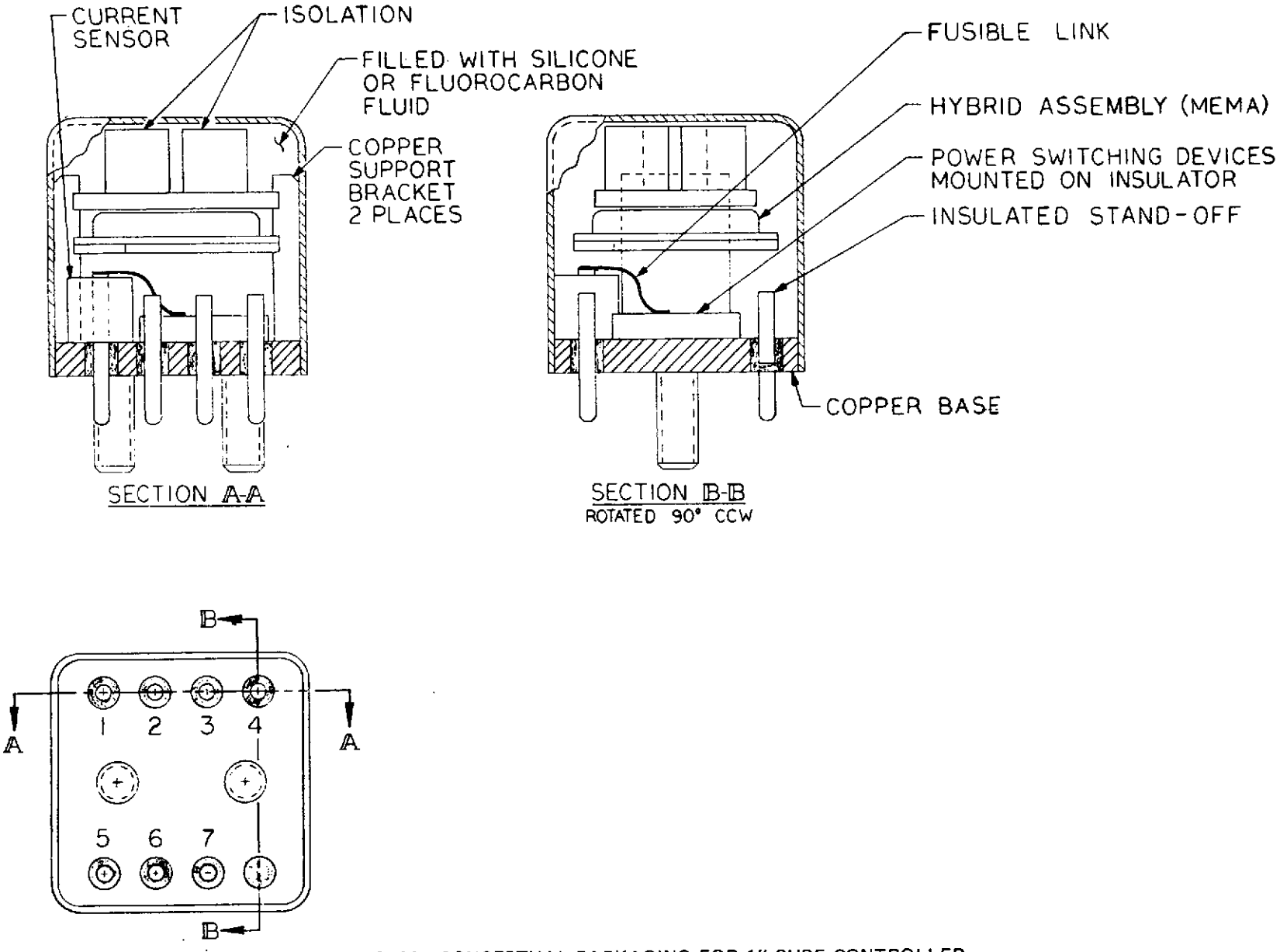


FIG. 20. CONCEPTUAL PACKAGING FOR 1" CUBE CONTROLLER WITH MIL-P-81653 MOUNTING CONCEPT

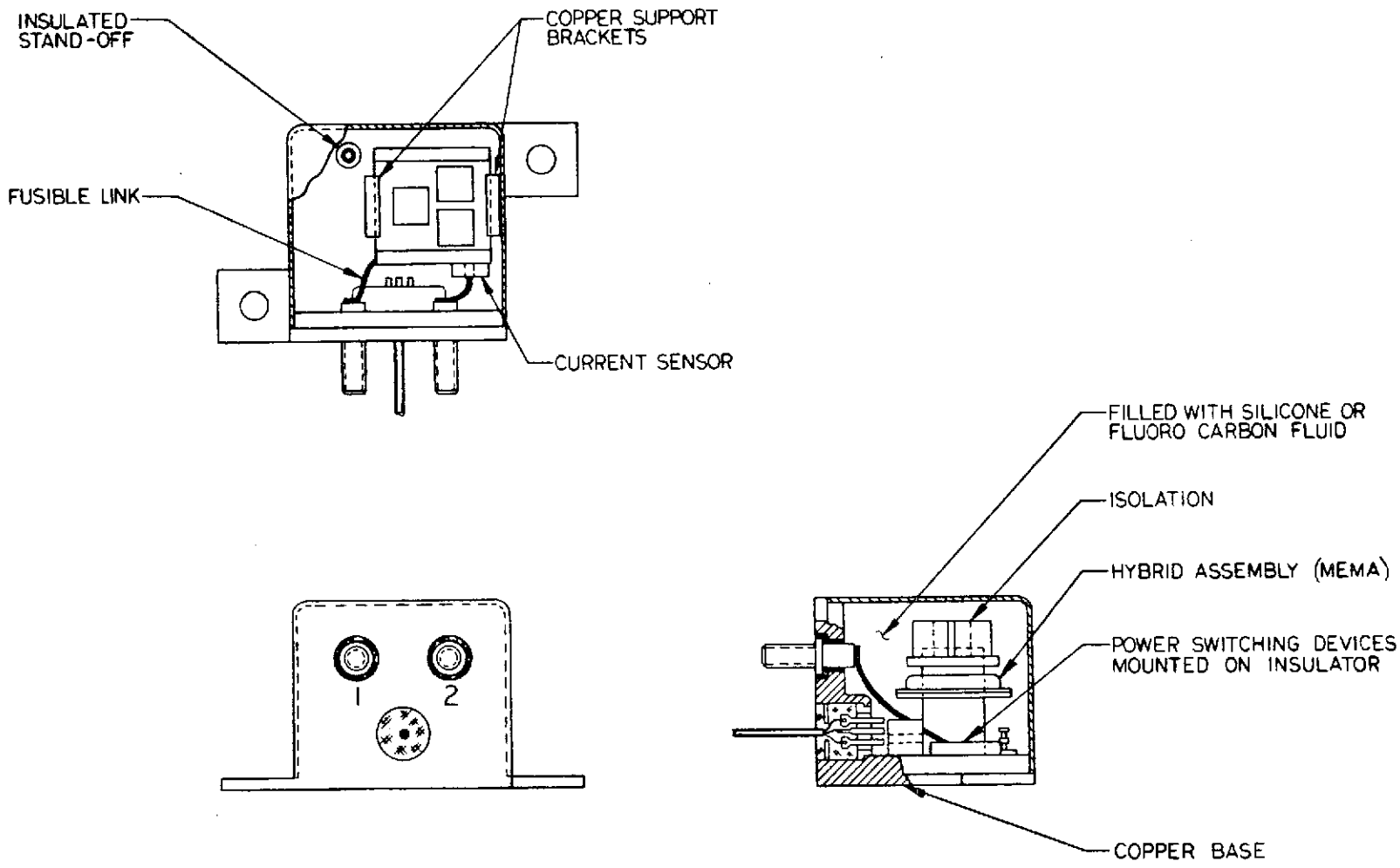


FIG. 21. CONCEPTUAL PACKAGING FOR 1" CUBE CONTROLLER
WITH ALTERNATE MOUNTING CONCEPT

RELIABILITY

A preliminary reliability prediction analysis has been conducted to determine the failure rate of DC Solid State Power Controllers using hybrid-microelectronics for flight hardware. The predictions are based on the service and environmental conditions of the specifications.

The approaches and assumptions used consisted of a functional analysis of the design. It indicated that the functional blocks in each design assume a totally serial relationship. This results in a conservative estimate of the circuit capability. The basic failure rates of each chip or die comprising the hybrid-microelectronic control package was calculated at the maximum hybrid package case temperature of +125°C, which is +5°C over the specified 120°C maximum case temperature of the controller. Thermal analysis of the design shows that the use of beryllia substrate and the method of mounting the HYBRID internally insures a low order of thermal resistivity. For prediction purposes, the junction temperature of integrated circuits and semiconductor dice was assured to be at HYBRID case temperature plus 10°C, or 135°C. This is in accord with recommendations of the RADC Reliability Handbook, Volume II. Failure rates for capacitor and resistor elements was based on using +125°C as the component ambient temperature. MIL-HDBK-217A was used as the source of failure rates except as otherwise noted in the discussion below. The use of silicone or fluidcarbon oil as a filler within the controller housing, facilitates heat sinking and provides a dampening effect on other environments such as shock and vibration. Therefore, an environmental K factor of 1.0 was applied to all calculated failure rates.

The failure rate for the hybrid-microelectronic control package can be estimated by analysing its constituent elements. The I.C. failure rate used for this prediction was based on life test data published by Fairchild Semiconductor* for devices which have received 100% burn-in screening prior to usage. That figure is .030 failure per 10^6 hours (+135°C junction temperature) and is applicable to packaged devices.

In order to predict the failure rate of the hybrid-microelectronic control assembly it is necessary to estimate the intrinsic failure rate of "bare" dice by removing the failures of the packaged device which cannot be attributed to the "bare" die. The approach then is to eliminate the effects due to leads, base, package, etc., leaving the failure rate due to dice alone. I.C.'s used in Teledyne HYBRIDS are subjected to extensive pre-use screening and testing as follows:

100% AC Testing
100% DC Testing
100% Thermal Testing
100% Optical Inspection (at dice level and again at MEMA precover)

* Microcircuits Reliability Report - Fairchild Semiconductors, May 6, 1969; 83.8 million part hours (all devices).

RELIABILITY (Continued)

When the intrinsic die failure rates are estimated as outlined, and the effects due to extensive screening and inspection are taken into account, a dice failure rate of .020 failures per 10^6 hours results.

A similar rationale is applicable to other types of dice. Failure rates from MIL-HDBK-217 for Minutemen quality parts were used to represent intrinsic die failure rates. These rates were normalized for operation at +125°C (capacitors, resistors) and at +135°C junction temperature for semiconductors in accordance with factors of MIL-HDBK-217. Table 2 shows the failure rate for 1 Amp and 5 Amp DC Controllers.

TABLE 2. 1 Amp and 5 Amp DC Controller

FAILURE RATE ESTIMATE

(Failures per 10^6 hours)

QTY.	COMPONENT		FR SOURCE	FR
4	Integrated Circuits (I.C.'s)	@ .020	1	.080
18	Resistors, film	@ .007	2	.126
8	Capacitors, ceramic	@ .038	2	.304
6	Diodes, general purpose	@ .005	2	.030
6	Transistors	@ .010	2	.060
3	Diode - Zener	@ .102	2	.306
1	Power Transistor	@2.000	2	2.000
2	Transformers	@ .200	2	.400
100	Lead Bonds	@ .00007	3	.007
	Substrate, Frame & Cover		4	.004
24	External Leads	@ .00005	5	.001
		Total Failure Rate		3.318

Failure Rate Sources:

1. See discussion above.
2. Normalized MIL-HDBK-217A, Minutemen level failure rates.
3. Ultrasonic lead bond estimate based on Teledyne and industry data.
4. Best engineering estimate.
5. Welded termination estimate based on Teledyne and industry data.

TABLE 3. SPECIFICATIONS - Teledyne 1 Amp and 5 Amp Solid State Power Controllers

REQUIREMENTS	1 AMP DC CONTROLLER Teledyne P/N 673-10004	5 AMP DC CONTROLLER Teledyne P/N 673-10001
Mechanical & Dimensional Characteristics		
Configuration	See Fig. 15	See Fig. 15
Dimension	See Fig. 15	See Fig. 15
Enclosure	Hermetic Seal	Hermetic Seal
Weight	3.0 ounces maximum	3.0 ounces maximum
Mounting Torque	15 in. lbs.	15 in. lbs.
Thermal Characteristics		
Thermal Resistance Case-to-Sink	0.5 C/watt with specified mounting torque	0.5 C/watt with specified mounting torque
Heat Sink Temperature (Design Consideration)	+118°C maximum	+118°C maximum
Electrical Characteristics	-54°to +120°C case temperature (unless otherwise specified)	-54°to +120°C case temperature (unless otherwise specified)
General		
Terminal Arrangement	SPST (normally open)	SPST (normally open)
Insulation Resistance	100 megohm minimum	100 megohm minimum
Dielectric Withstanding Voltage	1000 vAC (RMS)	1000 vAC (RMS)
Isolation		
Between control and trip terminals shorted and output terminals shorted	1000 vAC (RMS)	1000 vAC (RMS)
Life (operating cycles)	10^6 minimum	10^6 minimum
Radio Interface	MIL-STD-461	MIL-STD-461
Power Dissipation (maximum @ 25°C ambient)		
"ON"-rated load	1.5 watt, maximum	4.5 watt maximum
"OFF"	.150 watt, maximum	.164 watt, maximum

TABLE 3. SPECIFICATIONS - Teledyne 1 Amp and 5 Amp Solid State Power Controllers (cont.)

REQUIREMENTS	1 AMP DC CONTROLLER Teledyne P/N 673-10004	5 AMP DC CONTROLLER Teledyne P/N 673-10001
Power Circuit		
Supply Voltage	30 vDC, maximum	30 vDC, maximum
Limits - Curves 1 & 6 MIL-STD-704A	15 vDC, minimum	15 vDC, minimum
Current (rated)	1 Ampere	5 Amperes
Voltage Drop	.5 volts DC, maximum	.5 volts DC, maximum
Leakage Current	100μ Amps, maximum	500μ Amps, maximum
Current Limiting	Applicable	Applicable
DC ripple	5% rated load (peak to peak), maximum	5% rated load (peak to peak), maximum
Fail Safe (I^2t)	1200	1200
Transients		
Operating Voltage	Applicable	Applicable
Spike Overvoltage	Applicable	Applicable
Response		
Turn-On Time	1.0 mSec, maximum	1.0 mSec, maximum
Rise Time	.1 mSec, minimum .5 mSec, maximum	.1 mSec, minimum .5 mSec, maximum
Turn-Off Time	6.0 mSec, maximum	6.0 mSec, maximum
Fall Time	.5 mSec, minimum 5.0 mSec, maximum	.5 mSec, minimum 5.0 mSec, maximum
Trip Free	Applicable	Applicable
Trip-Out Time		
Non-repetitive Reset	Applicable (30 seconds minimum between resets)	Applicable (30 seconds minimum between resets)
Repetitive Reset	Applicable	Applicable
Trip Indication		
Not Tripped	Current sink, 0 to 50 mA	Current sink, 0 to 50 mA
Tripped	Open circuit, 0 to 32 vDC	Open circuit, 0 to 32 vDC
Control Circuit		
Supply Voltage		
Maximum	32 vDC	32 vDC
Rated	28 vDC	28 vDC
Minimum	20 vDC	20 vDC

TABLE 3. SPECIFICATIONS - Teledyne 1 Amp and 5 Amp Solid State Power Controllers (cont.)

REQUIREMENTS	1 AMP DC CONTROLLER Teledyne P/N 673-10004	5 AMP DC CONTROLLER Teledyne P/N 673-10001
Control Circuit (cont.)		
Turn-On Voltage	24 vDC, minimum	24 vDC, minimum
Rate of Change	.5 vDC/mSec, minimum	.5 vDC/mSec, minimum
Turn-Off Voltage	5.0 vDC, maximum	5.0 vDC, maximum
Rate of Change	.5 vDC/mSec, minimum	.5 vDC/mSec, minimum
Input Current	20 mA, maximum	25 mA, maximum
Input Transients	Applicable	Applicable
Noise Immunity	Applicable	Applicable
Reset	By removing and re-applying DC control voltage	By removing and re-applying DC control voltage
Time to Reset (removal)	5 mSec, minimum 80 mSec, maximum	5 mSec, minimum 80 mSec, maximum
Environmental Characteristics		
Case Temperature		
Operating	-54°C to +120°C	-54°C to +120°C
Storage	-65°C to +150°C	-65°C to +150°C
Shock		
Mechanical	40 G's for 11.0 +1.0 mSec	40 G's for 11.0 +1.0 mSec
Temperature	-54°C to +120°C ambient	-54°C to +120°C ambient
Vibration		
Sinusoidal (operating)		
G Level	15 G's, maximum	15 G's, maximum
Frequency Range	5 to 2000 Hz	5 to 2000 Hz
Random (operating)		
Power Spectral Density	0.2 G^2/Hz, maximum	0.2 G^2/Hz, maximum
Frequency Range	20 to 2000 Hz	20 to 2000 Hz
Acceleration	100 G's	100 G's
Salt Fog	Applicable	Applicable
Humidity	Applicable	Applicable
Temperature-Altitude		
Operating Ambient		
Temperature	-54°C to +120°C	-54°C to +120°C
Altitude	Sea Level to 100 K ft.	Sea Level to 100 K ft.
Non-Operating Ambient	-65°C to + 150°C	-65°C to +150°C
Altitude	0.65 to 15.4 psia	0.65 to 15.4 psia
Explosive Decompression	Not Applicable	Not Applicable

TEST RESULTS

Teledyne 1 Amp DC Solid State Power Controller
P/N 673-10004

Pin Identification

Pin No.	Function
1	Control Voltage (+)
2	Signal Common
3	Trip Indicator
4	Power In (+)
5	Power Out (-)
6	No Connection
7	Test Point (Emitter)
8	Test Point (Base)

Terminal Arrangement - SPST (Normally Open)

TEST	REQUIREMENT	RESULTS
Insulation Resistance	100 megohms, min.	>100 megohms
Dielectric Withstanding Voltage	1000 vAC (RMS), min.	>1000 vAC (RMS)
Isolation	1000 vAC (RMS), min.	>1000 vAC (RMS)
Power Dissipation		
"ON" (rated load)	1.5 watts, max.	1.0 watt
"OFF"	.150 watt, max.	.003 watt
Voltage Drop		
Serial No. 1	.5 volts, max. @ 1 Amp	150 millivolts
Serial No. 3	.5 volts, max. @ 1 Amp	250 millivolts
Overshoot		<25%
Response		
Serial No. 1		
Turn ON Time	1.0 mSec, max.	2.8 mSec
Rise Time	.1 mSec, min.; .5 mSec, max.	.7 mSec
Turn OFF Time	6.0 mSec, max.	1.0 mSec
Fall Time	.5 mSec, min.;5.0 mSec, max.	.5 mSec
Serial No. 2		
Turn ON Time	1.0 mSec, max.	2.5 mSec
Rise Time	.1 mSec, min.; .5 mSec, max.	.5 mSec
Turn OFF Time	6.0 mSec, max.	1.0 mSec
Fall Time	.5 mSec, min.;5.0 mSec, max.	.5 mSec

TEST RESULTS (cont.)

Teledyne 1 Amp Solid State Power Controller
P/N 673-10004

TEST	REQUIREMENT	RESULTS
Leakage Current	100 μAmps, max.	<100 μAmps
Time to Rest (removal)	5.0 mSec, min.; 80 mSec, max.	80 mSec
Trip Indication		
Not Tripped	Current Sink, 0 to 50 mA	0 to 50 mA
Tripped	Open Circuit, 0 to 32 vAC	0 to 32 vDC
Turn ON Voltage	24 vDC, min.	<24 vDC
Turn OFF Voltage	5 vDC, max.	<5 vDC
Control Voltage		
Rate of Change	.5 vDC/μSec, min.	>.5 vDC/μSec
Control Current	20 mA, max.	12 mA @ 24 vDC 13 mA @ 28 vDC 15 mA @ 32 vDC

			Serial #1	Serial #2
Current Limiting				
Trip Current		@ 25°C	1.4 Amp	1.4 Amp
		@-55°C	1.5 Amp	1.5 Amp
		@ 90°C	1.3 Amp	1.3 Amp
Time to Trip @ 300% Load		@ 25°C	4.0 Sec	4.0 Sec
		@-55°C	5.0 Sec	5.0 Sec
		@ 90°C	3.0 Sec	3.0 Sec
Time to Trip				
30 vDC Supply Voltage	100%	Output Current	No Trip	No Trip
30 vDC " "	150%	" "	4.0 Sec	4.0 Sec
30 vDC " "	500%	" "	4.0 Sec	4.0 Sec
40 vDC " "	150%	" "	4.0 Sec	4.0 Sec
60 vDC " "	150%	" "	4.0 Sec	4.0 Sec
80 vDC " "	150%	" "	.02 Sec	.02 Sec
40 vDC " "	500%	" "	4.0 Sec	4.0 Sec
60 vDC " "	500%	" "	.02 Sec	.02 Sec
80 vDC " "	500%	" "	.02 Sec	.02 Sec

TEST RESULTS (cont.)

Teledyne 1 Amp Solid State Power Controller
P/N 673-10004

Temperature Tests at -55°C and +90°C
Note. Units did not operate satisfactorily above 100°C because of improper transformer core. This can be readily corrected in future units.

Insulation Resistance	All Units Tested Satisfactorily
Dielectric Withstanding Voltage	" " " "
Isolation	" " " "
Power Dissipation	" " " "
Rated Current and Voltage	" " " "
Voltage Drop of Rated Current	" " " "

Control Input Transients
A single pulse of plus and minus 100 volts peak amplitude and 100 μSec duration, repeated 10 times at 3 second intervals. All units tested satisfactorily.

A train of 10 pulses of plus and minus 100 volts peak amplitude and 100 μSec duration each, repeated 10 times at 3 second intervals. All units tested satisfactorily.

Above tests repeated between trip indicator terminal and ground (DC return) terminal. All units tested satisfactorily.

Test Circuit
The test circuit for DC controllers is shown in Fig. 22.

TEST RESULTS

Teledyne 5 Amp DC Solid State Power Controller
P/N 673-10001

Pin Identification

Pin No.	Function
1	Control Voltage (+)
2	Signal Common
3	Trip Indicator
4	Power In (+)
5	Power Out (-)
6	No Connection
7	Test Point (Emitter)
8	Test Point (Base)

Terminal Arrangement - SPST (Normally Open)

TEST	REQUIREMENT	RESULT
Insulation Resistance	100 megohms, min.	>100 megohms
Dielectric Withstanding Voltage	1000 vAC (RMS), min.	>1000 vAC (RMS)
Isolation	1000 vAC (RMS), min.	>1000 vAC (RMS)
Power Dissipation		
"ON" (rated load)	4.5 watts, max.	3.5 watts
"OFF"	.164 watt, max.	.015 watt
Voltage Drop		
Serial No. 4	.5 volts, max.	350 mV @ 5 Amps
Serial No. 5	.5 volts, max.	350 mV @ 5 Amps
Overshoot		<25%
Response		
Serial No. 4		
Turn ON Time	1.0 mSec, max.	1.8 mSec
Rise Time	.1 mSec, min.; .5 mSec, max.	.5 mSec
Turn OFF Time	6.0 mSec, max.	1.3 mSec
Fall Time	.5 mSec, min.;5.0 mSec, max.	1.6 mSec
Serial No. 5		
Turn ON Time	1.0 mSec, max.	1.6 mSec
Rise Time	.1 mSec min. ; .5 mSec, max.	.35 mSec
Turn OFF Time	6.0 mSec, max.	1.4 mSec
Fall Time	.5 mSec, min.;5.0 mSec, max.	1.5 mSec

TEST RESULTS (cont.)

Teledyne 5 Amp Solid State Power Controller
P/N 673-10001

TEST	REQUIREMENT	RESULT
Leakage Current	500 μAmps, max.	<500 μAmps
Time to Reset (removal)	5.0 mSec, min; 80 mSec, max.	80 mSec
Trip Indication		
Not Tripped	Current Sink, 0 to 50 mA	0 to 50 mA
Tripped	Open Circuit, 0 to 32 vDC	0 to 32 vDC
Turn ON Voltage	24 vDC, min.	<24 vDC
Turn OFF Voltage	5 vDC, max.	> 5 vDC
Control Voltage		
Rate of Change	.5 vDC/μSec, min.	>.5 vDC/μSec
Control Current	25 mA, max.	19 mA @ 24 vDC 20 mA @ 28 vDC 21 mA @ 32 vDC

			Serial #4	Serial #5
Current Limiting				
Trip Current		@ 25°C	5.9 Amps	6.1 Amps
		@ 90°C	5.2 Amps	6.0 Amps
		@-55°C	5.8 Amps	6.3 Amps
Time to Trip @ 300% Load		@ 25°C	2.5 Sec	2.0 Sec
		@ 90°C	2.0 Sec	1.8 Sec
		@-55°C	3.0 Sec	2.2 Sec
Time to Trip				
30 vDC Supply Voltage	100% Output Current		No Trip	No Trip
30 vDC " "	150% " "		2.2 Sec	2.0 Sec
30 vDC " "	500% " "		2.5 Sec	2.0 Sec
" "	150% " "		2.5 Sec	2.0 Sec
" "	150% " "		2.5 Sec	2.0 Sec
" "	150% " "		.02 Sec	.02 Sec
" "	500% " "		2.5 Sec	2.0 Sec
" "	500% " "		.02 Sec	.02 Sec
" "	500% " "		.02 Sec	.02 Sec

TEST RESULTS (cont.)

Teledyne 5 Amp DC Solid State Power Controller
P/N 673-10001

Temperature Tests at -55°C and +90°C

Note. Units did not operate satisfactorily above 100°C because of improper transformer care. This can be readily corrected in future units.

Insulation Resistance	All units tested satisfactorily
Dielectric Withstanding Voltage	" " " "
Isolation	" " " "
Power Dissipation	" " " "
Rated Current and Voltage	" " " "
Voltage Drop at Rated Current	" " " "

Control Input Transients

A single pulse of plus and minus 100 volt peak amplitude and 100 μSec duration, repeated 10 times at 3 second intervals. All units tested satisfactorily.

A train of 10 pulses of plus and minus 100 volt peak amplitude and 100 μSec duration each, repeated 10 times at 3 second intervals. All units tested satisfactorily.

Above tests repeated between trip indicator terminal and ground (DC return) terminal. All units tested satisfactorily.

Test Circuit

The test circuit for DC controllers is shown in Fig.22.

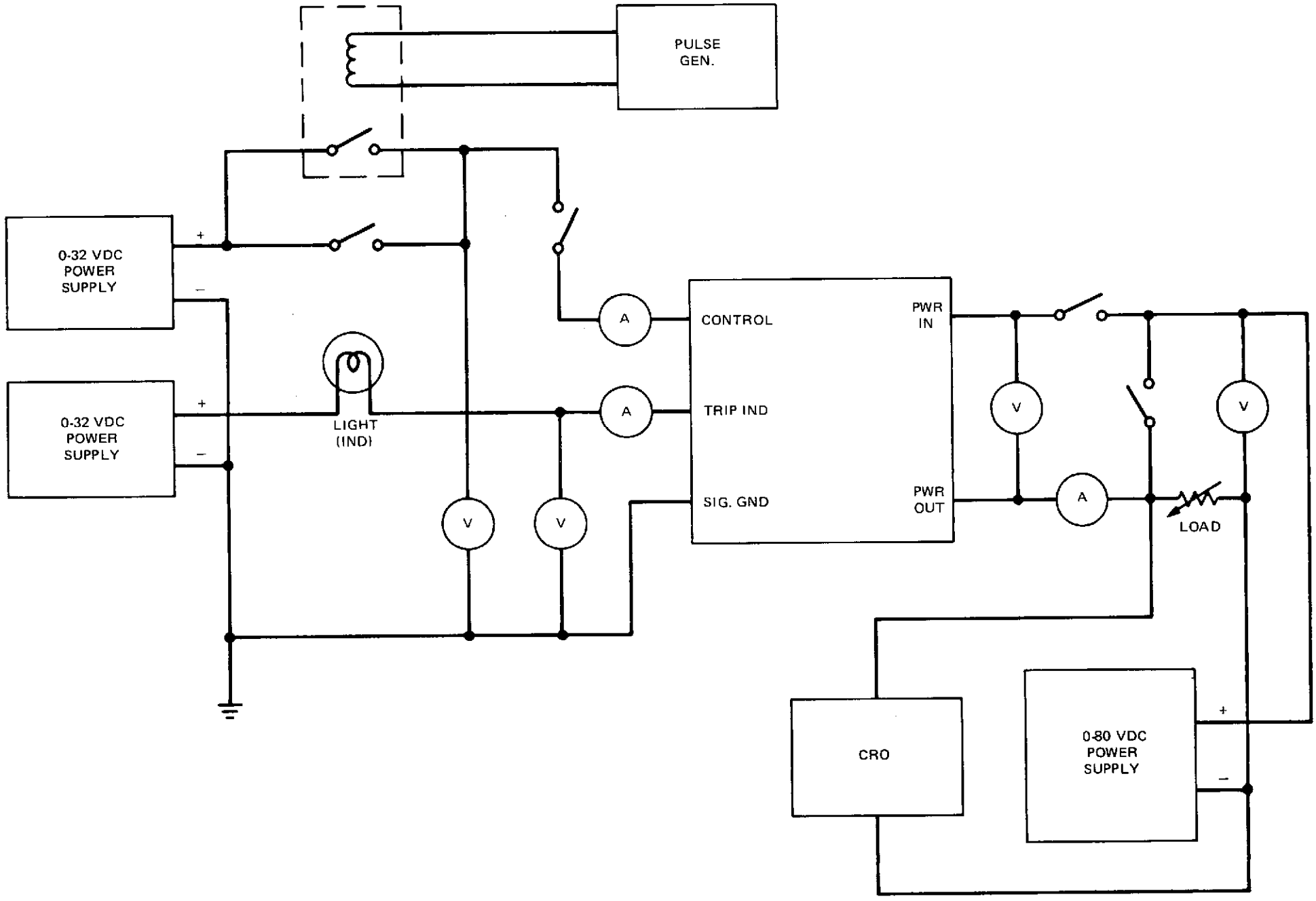


FIG. 22. TEST CIRCUIT FOR DC CONTROLLERS

AC SOLLID STATE POWER CONTROLLERS

ZERO AXIS SWITCHING

It is desirable in solid state switching of AC voltages to have the controller turn ON at zero voltage and turn OFF at zero current to minimize the effects of EMI. By proper gating of the solid state switching element (Triac or inverse parallel Silicon Controlled Rectifier), this is readily accomplished. Continuous switching ON and OFF can be at each half cycle or at each full cycle.

In the switching of AC inductive loads, particularly transformers, care must be taken to avoid a DC component being developed in switching. A core may be saturated to such an extent that this is possible. Full cycle switching minimizes the problem. Full cycle gating is more complex than half cycle gating as memory has to be established in the circuitry. The scope of the contract was such that hybrid-microelectronic packaging was not feasible. Consequently, it was not possible to package the additional circuitry required for full cycle switching. A circuit has been developed (Pat. Pending) which incorporates a CMOS logic gate in conjunction with an existing circuit to form full cycle control. When quantities warrant hybrid-microelectronic assembly, full cycle control can be included in optimum packaging. Half cycle zero voltage switching was used in the prototype units utilizing a unique circuit developed by Teledyne and covered by patent #3,648,075. This circuit will be discussed in detail later in the report.

POWER OUTPUT TERMINATION

MIL-P-81653 specifies a 3 terminal power output configuration, as indicated in Fig. 23. The zero voltage switching circuitry developed by Teledyne permits a two wire output configuration, as shown in Fig. 24. The arguments for or against the two or three wire system are identical for AC controllers as those for the already-discussed DC controllers. The main disadvantage of the two wire system is that status indication requires slightly more circuitry. The two wire system was employed in the prototype AC controllers.

POWER CHIP SELECTION

Three silicon devices are available for AC voltage switching, namely Transistors, Silicon Controlled Rectifiers and Triacs. Transistors are seldom used as they must be connected within a full wave bridge for AC operation, resulting in two diode voltage drops plus the voltage drop of the transistor itself. They also do not possess the current surge capabilities of Silicon Controlled Rectifiers or Triacs. Current limiting would be possible with a Transistor switching element where it is not practical with either the Silicon Controlled Rectifier or Triac switching element.

Silicon Controlled Rectifiers used in inverse parallel configuration are widely used in AC voltage switching. They are available with high current ratings, high voltage ratings and possess high current surge capabilities. Care must be used in gating for transformer loads. It is particularly important to ensure that two SCR's are fired exactly at 180° relative to each other.

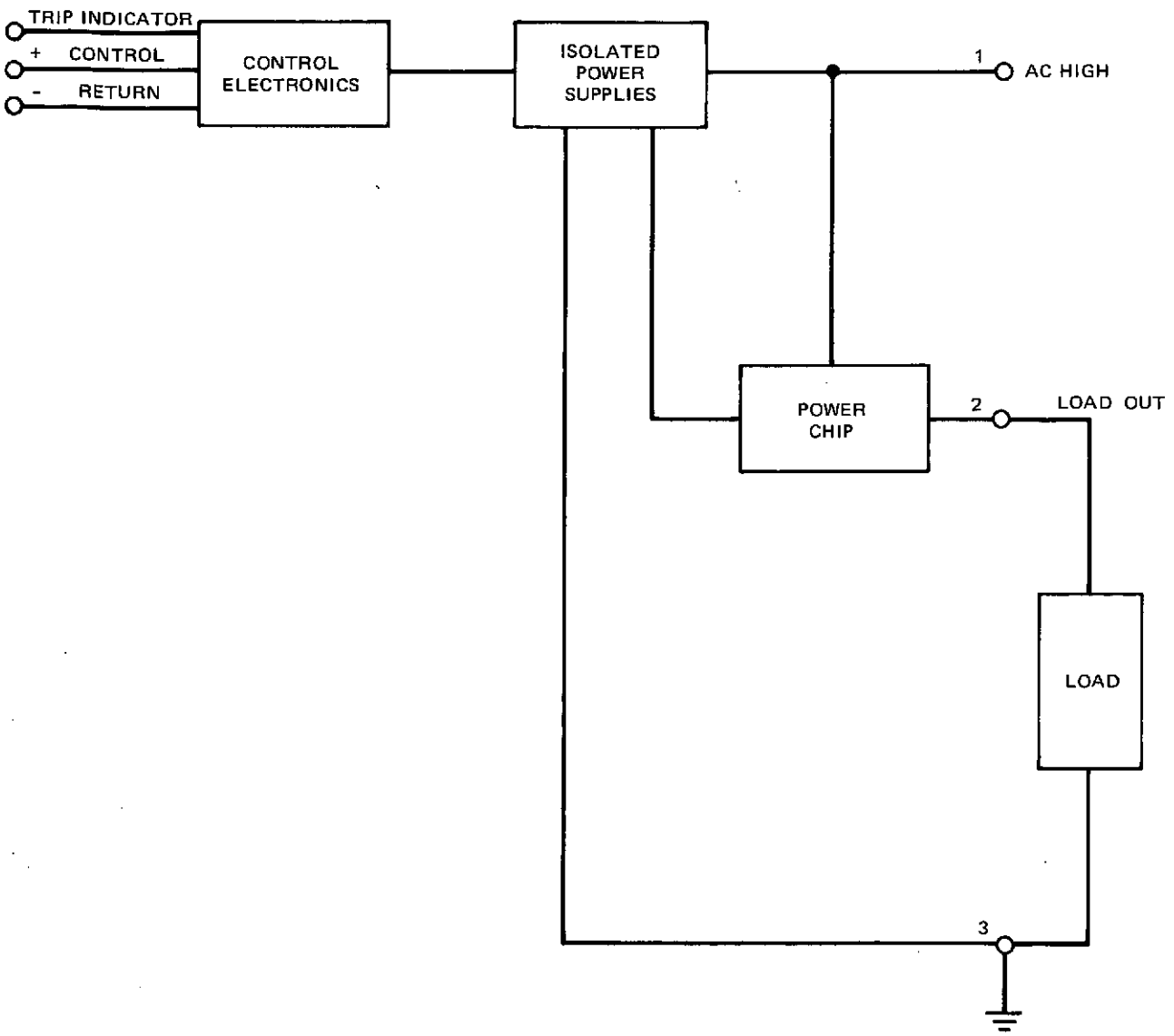


FIG. 23. MIL-P-81653 3-TERMINAL OUTPUT AC CONTROLLER

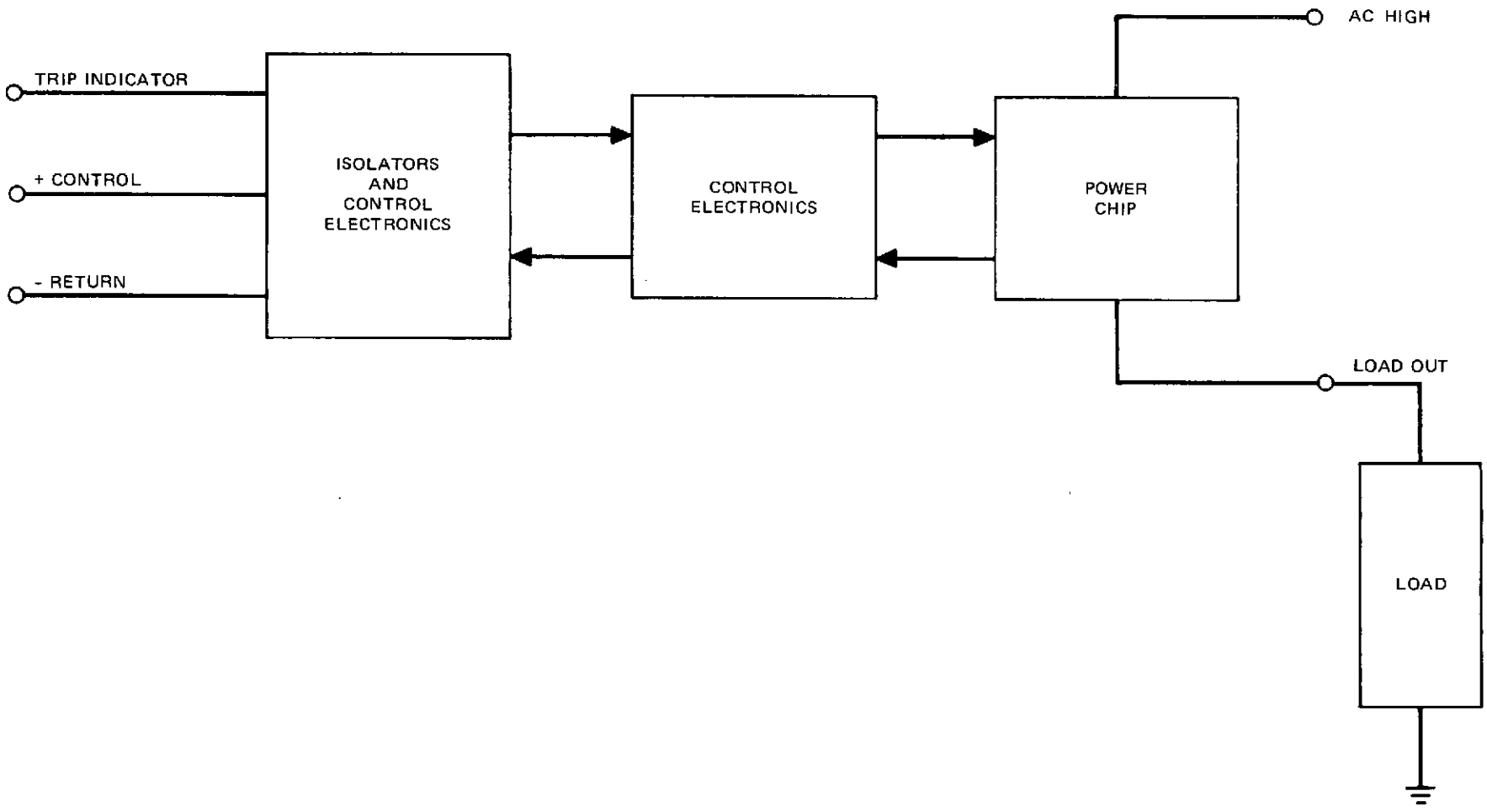


FIG. 24. 2-TERMINAL OUTPUT AC CONTROLLER

POWER CHIP SELECTION (cont.)

If this is not accomplished, the positive and negative current loops will differ in magnitude and a resultant DC will flow through the low impedance of the primary of the transformer.

Triacs (silicon bi-directional thyristors) possess most of the same features as Silicon Controlled Rectifiers. The distinct advantage is that only a single component is required for the switching element, and reduced component count is a major objective in the development of the controller. The single gate assists in minimizing DC offset problems. It is not completely eliminated because of inherent small differences that exist within the Triac itself when conducting in one direction and then in the opposite direction. Less componentry is required for zero axis switching with the Triac. The required rupture capacity of the specification can be satisfied with a Triac. For higher rated AC controllers, and where very high rupture capacities are specified, the inverse parallel SCR's should be considered. Selected Triac chips from the 2N5443 family were used for the prototype AC controllers. These chips have a 40 Amp continuous duty rating and a 400 Ampere surge capability for 1 cycle of a 400 Hz voltage line. A further consideration in selection of this particular chip was its center firing gate and glass passivation.

POWER DISSIPATION

Since current limiting is not practical in solid state switching of AC voltages, power dissipation requirements are not as critical as those for DC controllers. The main consideration on power dissipation is through the period when overcurrent is detected and trip-out takes place. The AC power controllers trip-out within one half cycle in the event of a short-circuit. The surge capacity of the chip is more meaningful than power dissipation in short-circuit conditions. The one half cycle trip-out does not allow sufficient time for appreciable heat dissipation. As a result, chip mounting similar to that shown in Fig. 6 was used in the prototype AC controllers.

ISOLATION

Isolation between the load circuit and the control circuit is performed by opto-couplers for the control, short-circuit protection and waveform distortion functions. Transformer coupling is used for the trip-out function. Referring to the circuit schematic, Fig. 27, the control function in the absence of overload, short-circuit and waveform distortion results in both of the inputs of NOR gate U4A to be at ground potential with output of U4A high, which is coupled to inputs of U4C with a resulting low output, allowing light emitter diode of U5 to conduct. This is with a positive 28V control voltage applied. With the emitter diode of U5 conducting, the SCR portion of U5 is also conducting. At low voltages of the AC power line, Q3 is biased OFF. This allows the DC voltage developed by BR1 to be passed by the SCR of U5 to the gate of Triac Q4, turning it ON. As the DC voltage increases, Q3 is forwarded to biased ON by voltage divider formed by R13 and R11, shorting the gate of the SCR of U5 to ground and turning it OFF. This is the principle of zero voltage gating covered by Teledyne patent #3.648,075. The isolation circuits of the other functions will be discussed later.

SHORT-CIRCUIT PROTECTION

Short-circuit protection is obtained by developing a voltage across R17, full wave rectifying it to DC by means of BR2 and causing a light emitter diode of U2 to conduct. This forward biases the transistor of U2 putting a logic 1 voltage to input of NOR gate U4A. As a result, the output of U4A and inputs of U4C go low. The output of U4C goes high and the Triac is turned off instantly, in a half cycle or less. Problems were encountered in testing where at a combination of overload current and temperatures above 90°C the controller would not trip-out. By either reducing the temperature to 85°C or reducing the frequency, trip-out was successful. This failure was completely due to the characteristics of the Triac used at 400 Hz. This problem can be corrected by selecting a Triac with more favorable 400 Hz characteristics.

CONTROL VOLTAGE SELECTION

The rationale for control voltage selection is the same for AC controllers as that previously discussed for DC controllers.

TRIP INDICATION

Trip-out time as a function of overload should be within the limits indicated in Fig. 25. Trip-out is obtained by sensing a current by transformer T1 and feeding its corresponding voltage pulses to operational amplifier U1. This forward biases Q1 and through the timing and shaping circuit consisting of R1, R3, CR2, R2 and C2, the input of NOR gate U4A is brought to logic level 1. This results in the output of U4C going high and turning off the controller.

Trip indication is obtained by the successive gating of U4A, U4B, U4D and eventual biasing of Q2. The logic is such that in a non-tripped condition, Q2 is conducting, and in a tripped condition, Q2 is cut-off. The logic may be reversed by connecting the base of Q2 to the output of U4B. A voltage indication rather than current sink indication may be accomplished by connecting the collector of Q2 through a resistor to the 28 volt control supply. The collector output of Q2 is transient protected by R9 and CR4. The trip-out is latched by positive feedback to the output of U4B through CR3 to one of the inputs of U4A.

STATUS INDICATION

The general rationale for status indication is the same for AC controllers as that previously discussed for DC controllers. Status indication was not provided in the prototype AC controllers as the scope of the contract did not warrant the use of hybrid-microelectronics, and it was impossible to add this feature in the packaging desired. Status indication could be provided in the desired packaging using hybrid-microelectronic packaging concepts.

A status indication circuit was developed and is shown in simplified form in Fig. 26. Current is sensed by toroid transformer T1 (same transformer core and primary used in trip-indicating circuit). It is transformer coupled to operational amplifier A1, forward biasing Q1 ON and gating G1 high. G1 output goes low, biasing OFF Q2. Current sinking logic could be reversed as described

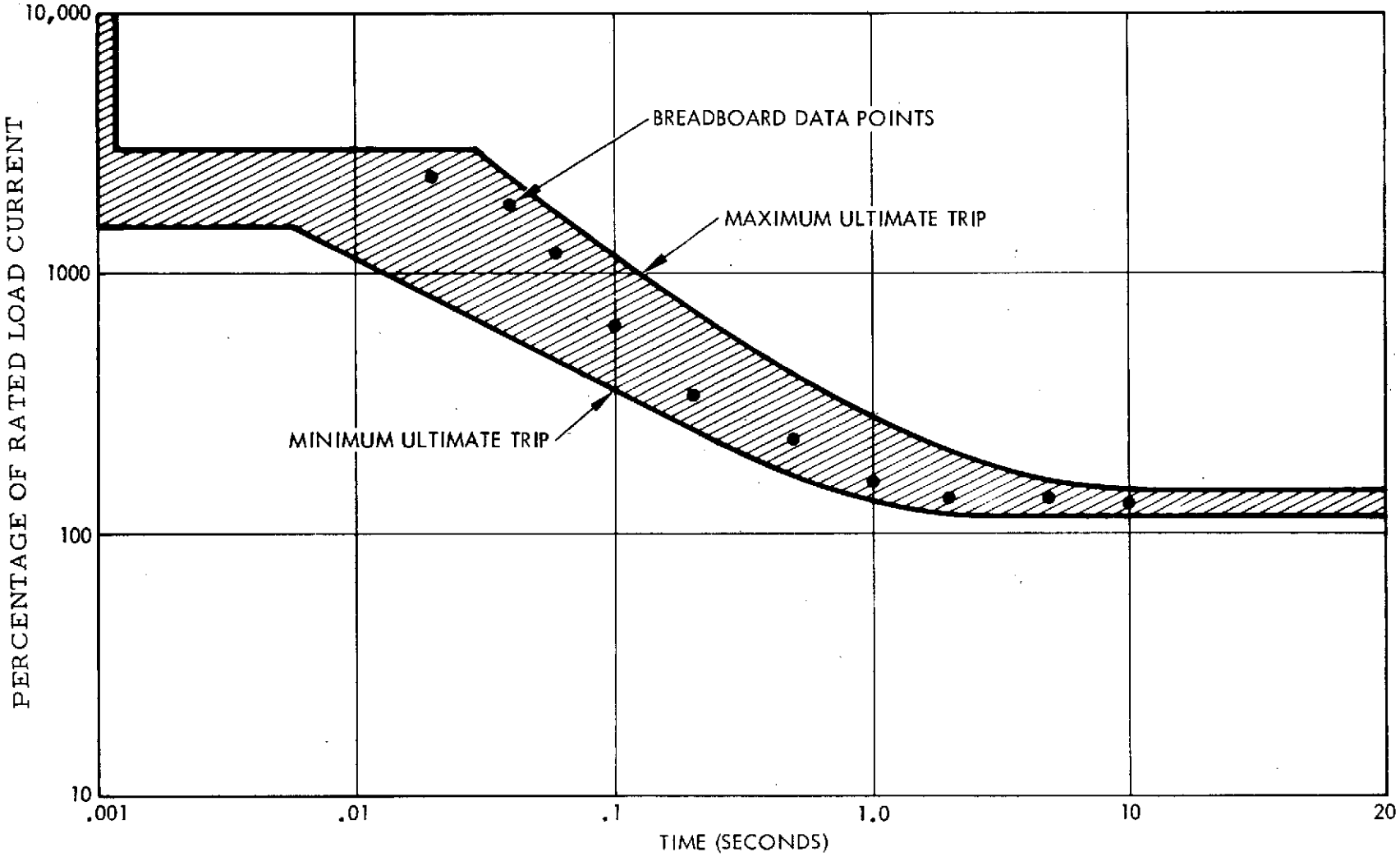


FIG. 25. MIL-P-81653 AC POWER CONTROLLER TRIP CHARACTERISTICS

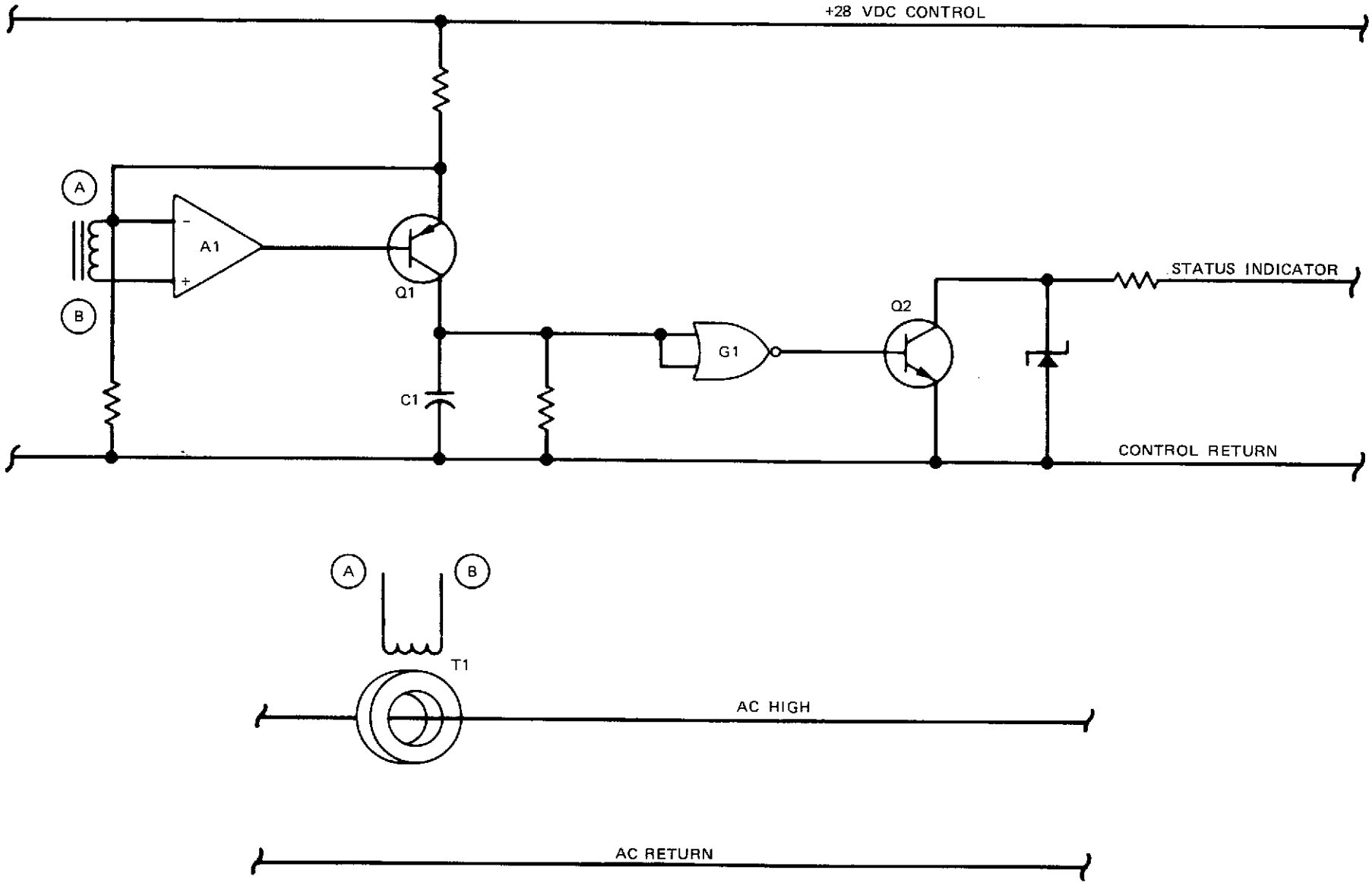


FIG. 26. AC CONTROLLER STATUS INDICATOR
SIMPLIFIED SCHEMATIC

in trip-out circuit. Also, a voltage level signal could be furnished. An analog signal with the output of A1 a function of current, could also be furnished.

WAVEFORM DISTORTION

If the core of an inductor becomes sufficiently saturated to cause a DC offset or half waving load current conditions, it is sensed by the voltage drop across R12 of the schematic, Fig. 27. This causes light emitter diode of opto-isolator U3 to conduct and forward bias ON the transistor of U3, gating U4A high, which through U4C and U5 turns power circuit OFF instantly in less than a half cycle.

RESET

Reset of the AC controller is accomplished by removing and re-applying the control voltage as previously described for DC controllers. Control voltage should be removed a minimum of 100 mSec before re-applying. The controller is latched in trip-out condition under overload, short-circuit and waveform distortion fault conditions.

TRANSIENT VOLTAGE PROTECTION

The power output circuit is protected by the breakdown voltage rating of Q4, the power Triac. Further protection is offered by the filter consisting of R16 and C5. This filter increases the effective circuit dv/dt to over 200V/μSec. This R-C network does contribute to higher leakage current. The network appears as a capacitive reactance in excess of 30K at 400 Hz. Since a low power factor exists between this current and applied voltage, almost no power dissipation occurs either in load or controller output.

The control input circuit is transient protected by R7, CR1 and C1. C1 also serves to set the 5 mSec time-to-reset. The trip indicator circuit is protected by R9 and CR4.

FUSING (Fail Safe)

The fusing requirements for the AC controller are met in the same manner as previously discussed for the DC controller.

FOUL-UP PROTECTION

The AC power controller is not as susceptable to damage by improper wiring as is the case for the DC controller. A diode which was omitted in the prototype AC controllers is shown in the schematic, Fig. 27. This offers protection against improper wiring of the control circuit.

AC POWER CONTROLLER CIRCUIT SCHEMATIC

The AC power controller circuit schematic is shown in Fig. 27. This is the circuit of the 1 Amp AC power controller delivered to NASA Manned Space-

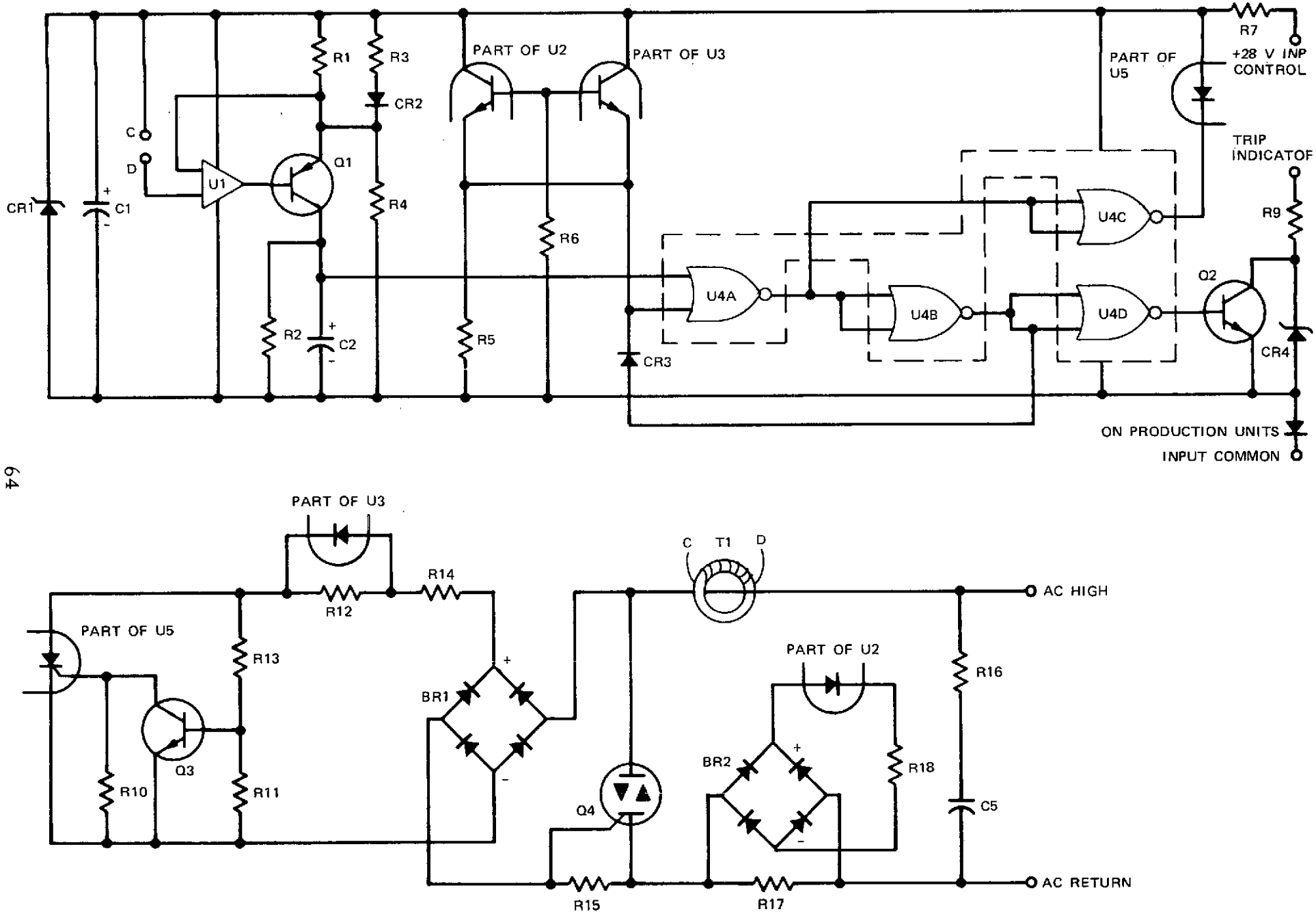


FIG. 27. AC POWER CONTROLLER CIRCUIT SCHEMATIC

craft Center/Houston ; Teledyne P/N 673-10005. The block diagram illustrating the functions is shown in Fig. 28.

PACKAGING

The 1 Amp AC power controller was packaged as shown in Fig. 29. An exploded view of the assembly is shown in Fig. 30. and the bottom and top circuit board assemblies are shown in Figs. 31 and 32.

The 1 Amp AC power controller using hybrid-microelectronic assembly concepts could be packaged as shown in Figs. 19, 20 and 21, where conceptual packaging for the DC controller was illustrated and discussed.

RELIABILITY

The rationale in arriving at predicted reliability is the same for the AC controller as for the previously discussed DC controller. The failure rate is shown in Table 4.

TABLE 4. AC POWER CONTROLLER FAILURE RATE ESTIMATE
(failures per 10^6 Hours)

QTY	COMPONENT		FR SOURCE	FR
2	Integrated Circuits	@ .020	1	.040
16	Resistors, Film	@ .007	2	.112
3	Capacitors	@ .038	2	.114
3	Diodes, Gen. Purpose	@ .005	2	.015
3	Transistors	@ .010	2	.030
1	Triac	@1.3	6	1.300
3	Optical Couplers	@ .20	6	.600
2	Rectifier Bridges	@ .02	2	.040
100	Lead Bonds	@ .00007	3	.007
24	External Leads	@ .00005	5	.0012
2	Diodes, Zener	@ .102	2	.204
1	Transformer	@ .200	2	.200
	Substrate, Frame and Cover		4	.004
		Total Estimated Failure Rate		2.667

Failure Rate Sources

1. See discussion above (Reliability, DC Controllers).
2. Normalized MIL-HDBK-217A Minuteman level failure rates.
3. Ultrasonic lead bond estimate based on Teledyne and industry data.
4. Best engineering estimate.
5. Welded termination estimate based on Teledyne and industry data.

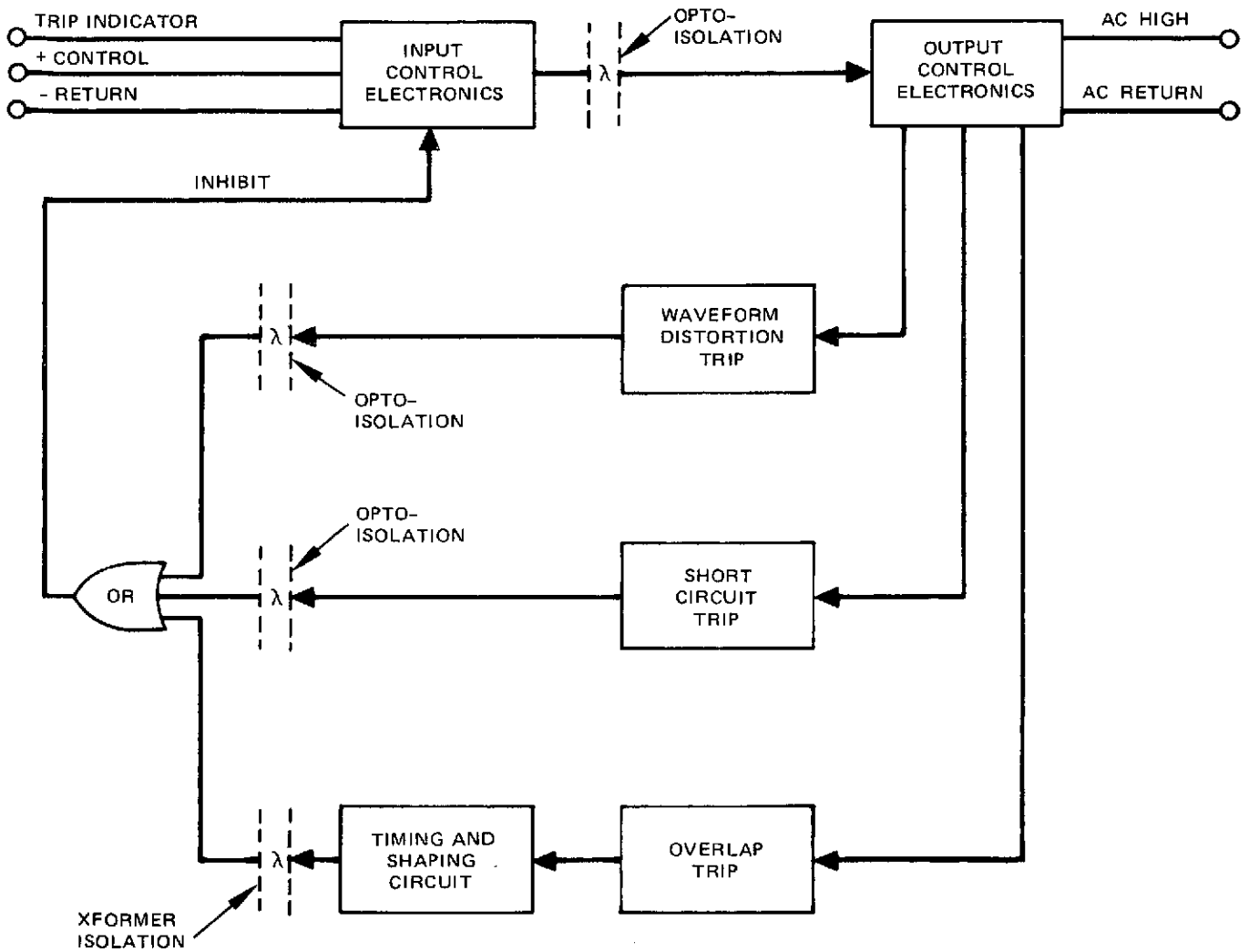
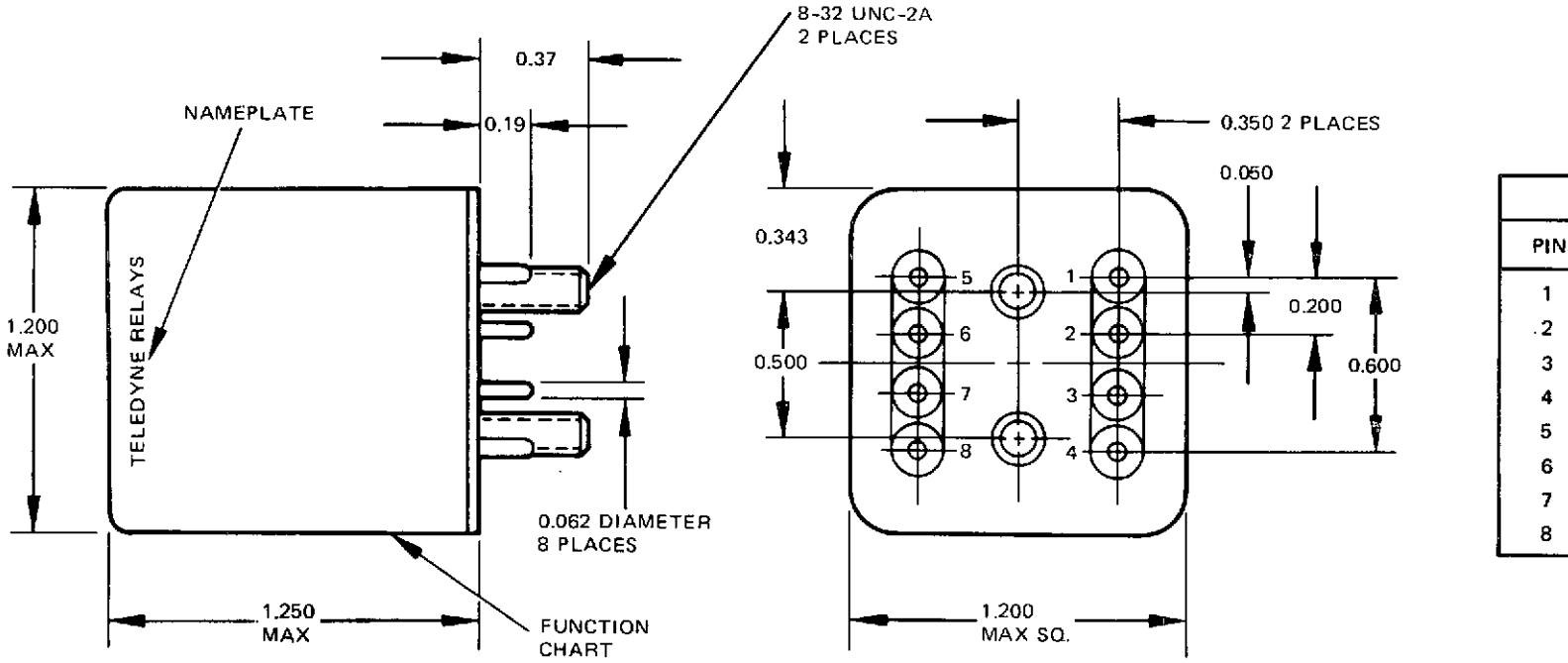
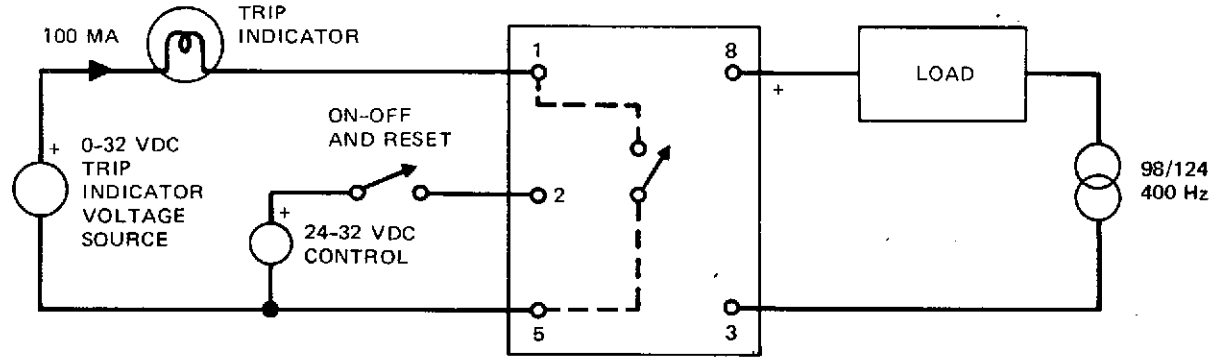


FIG. 28. FUNCTIONAL DIAGRAM AC POWER CONTROLLER

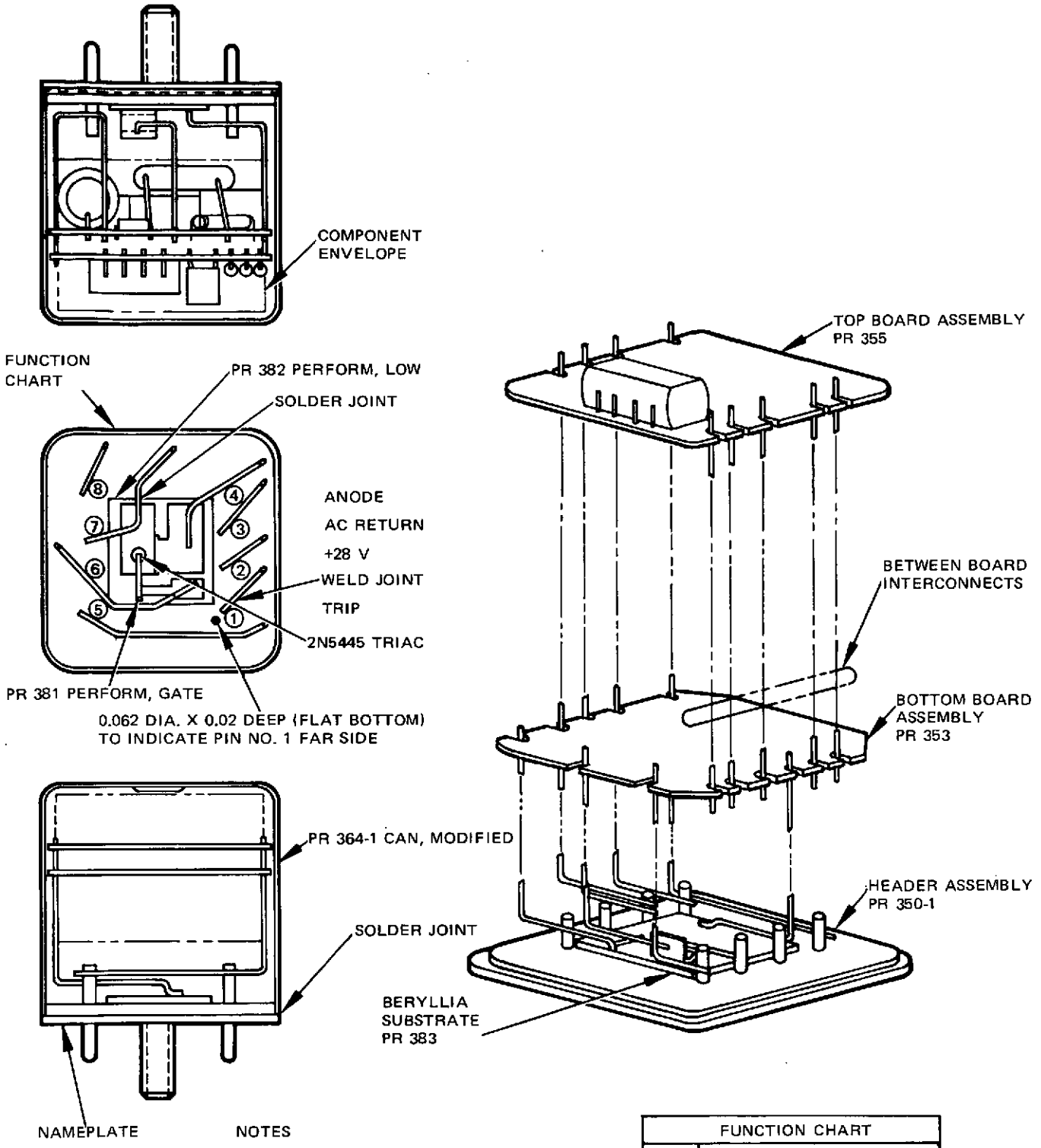


FUNCTION CHART	
PIN	DESCRIPTION
1	TRIP IND.
2	INPUT +28 VDC
3	AC RETURN
4	TEST POINT (A)
5	DC RETURN
6	TEST POINT (G)
7	TEST POINT (K)
8	AC HI



P/N 673–10005 1 AMP

FIG. 29. OUTLINE DWG 1 AMP AC POWER CONTROLLER



NOTES

1. FOR SCHEMATIC, SEE DRAWING PR 357
2. FOR OUTLINE DIM. DRAWING, SEE PR 366

FUNCTION CHART	
PIN	DESCRIPTION
1	TRIP IND
2	INPUT +28 VDC
3	AC RETURN
4	TEST POINT (A)
5	DC RETURN
6	TEST POINT (G)
7	TEST POINT (K)
8	A C HI

FIG. 30. ASSEMBLY LAYOUT LAMP AC POWER CONTROLLER

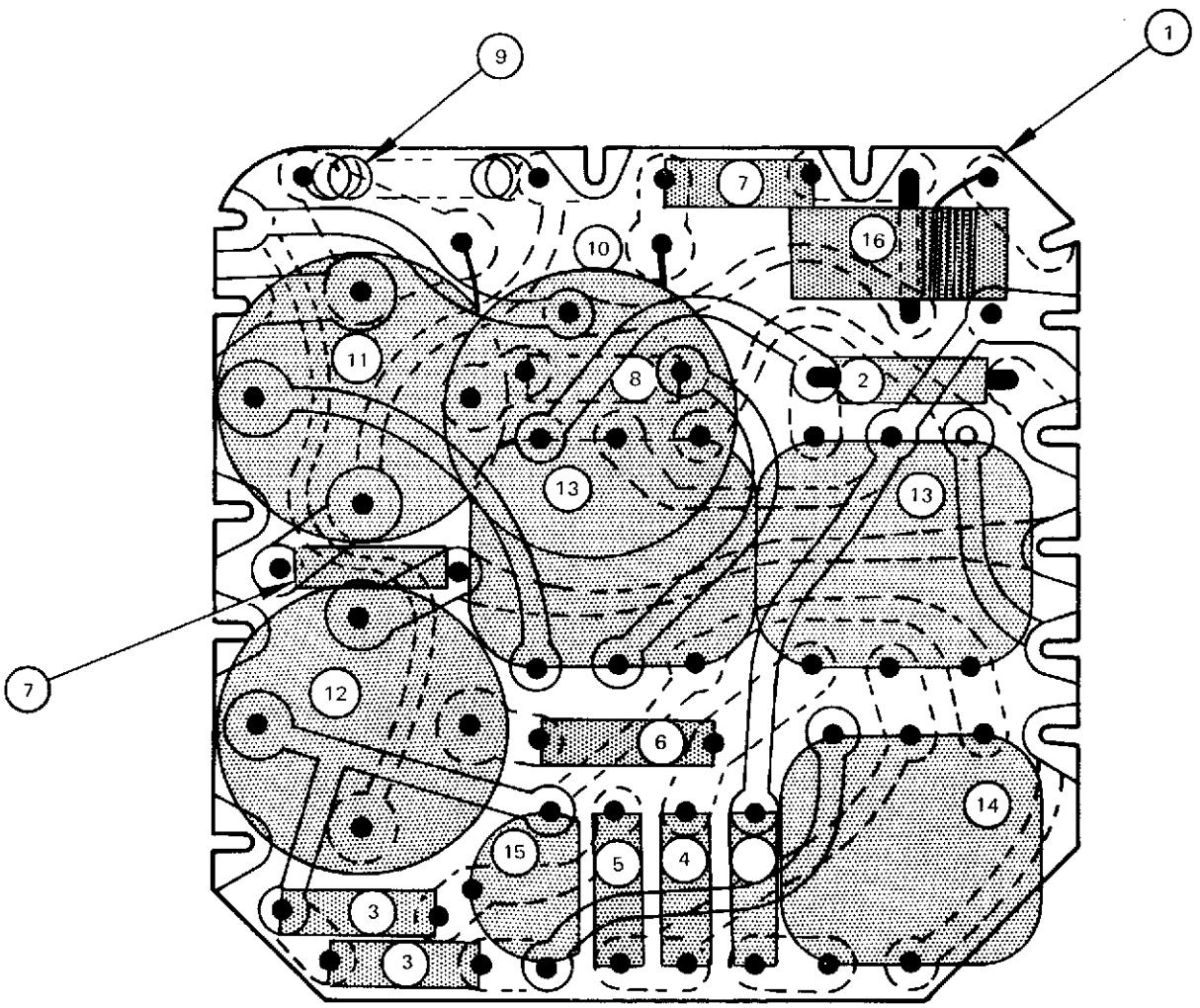


FIG. 31. CIRCUIT BOARD ASSEMBLY – BOTTOM 1 AMP AC POWER CONTROLLER

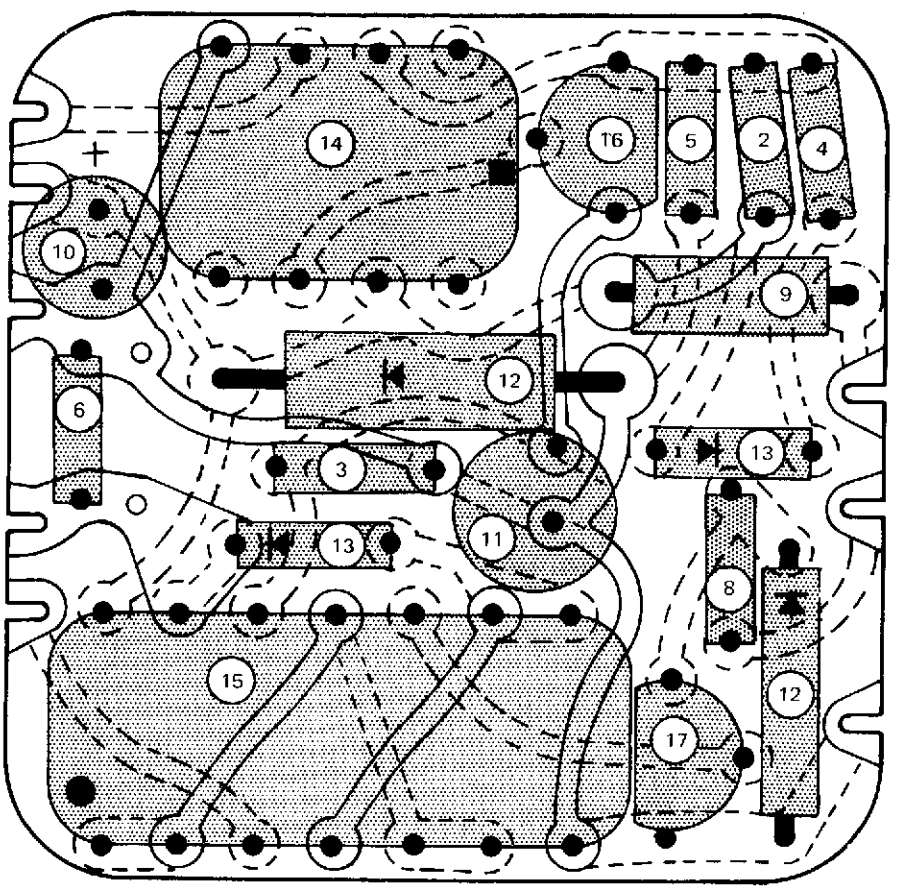


FIG. 32. CIRCUIT BOARD ASSEMBLY – TOP 1 AMP AC POWER CONTROLLER

TABLE 5. SPECIFICATIONS - 1 Amp AC Solid State Power Controller
Teledyne P/N 673-10005

REQUIREMENTS	TELEDYNE P/N 673-10005
Mechanical and Dimensional Characteristics	
Configuration	See Fig. 29
Dimensions	See Fig. 29
Enclosure	Hermetic Seal
Weight	3.0 ounces max.
Mounting Torque	15 in. lbs.
Thermal Characteristics	
Thermal Resistance Case-to-Sink	0.5°C/W with specified mounting torque
Heat Sink Temperature (Design Consideration)	118°C, maximum
Electrical Characteristics	-54°C to +120°C case temperature unless otherwise specified
General	
Terminal Arrangement	SPST (Normally Open)
Insulation Resistance	100 megohms
Dielectric Withstanding Voltage	1000 vAC (RMS)
Isolation	
Between control and trip terminals shorted and output terminals shorted	1000 vAC (RMS)
Life (operating cycles)	10^6 minimum
Radio Interference	MIL-STD-461
Leakage Current	4 + j13 maximum *
Power Dissipation (maximum @ 25°C ambient)	
"ON" at rated load	1.75 watt maximum
"OFF"	.311 watt maximum

* j13 mA leakage is due to dV/dT suppression network which appears as a capacitive reactance in excess of 30K @ 400 Hz.
Since a low power factor exists between this current and applied voltage, almost no power dissipation occurs either in load or controller output.

TABLE 5. SPECIFICATIONS - 1 Amp AC Solid State Power Controller (cont.)
Teledyne P/N 673-10005

REQUIREMENTS	TELEDYNE P/N 673-10005
POWER CIRCUIT	
Supply Voltage	124 vAC (RMS) maximum
Limits 1 & 6 of Curve 1 MIL-STD-704A	98 vAC (RMS) minimum
Current (Rated)	1.0 Amperes
Frequency (Rated)	400 Hz ±5%
Voltage Drop	1.5 vAC (RMS) maximum
Rupture Capacity	400 Amperes Peak
Waveform Distortion	1.5 vAC (RMS) or 6V Peak
Fail-Safe	I^2t = 1200 A^2 seconds
Transients	
Operating Voltage	180 vAC (RMS)
Response	
Turn-ON Time (from application of control)	2.5 mSec maximum
Turn-OFF Time (from removal of control)	2.5 mSec maximum
Trip-Free	Applicable
Trip-Out Time	Applicable
Non-repetitive Reset	Applicable
Repetitive Reset	Applicable
Trip Indication	
Tripped	Switch closed, .025 mA maximum leakage
Not-Tripped	Current Sink, 0 to 100 mA
Zero Voltage Turn-ON	Applicable - half cycle control
Zero Voltage Turn-OFF	Applicable - half cycle control
CONTROL CIRCUIT	
Supply Voltage	
Maximum	32 vDC
Rated	28 vDC
Turn ON Voltage	20 vDC minimum
Rate of Change	.5 V/μSec minimum
Turn OFF Voltage	5 vDC maximum
Rate of Change	.5 V/μSec minimum
Input Resistance	2.2 K ohms

TABLE 5. SPECIFICATIONS - 1 Amp AC Solid State Power Controller (cont.)
Teledyne P/N 673-10005

REQUIREMENTS	TELEDYNE P/N 673-10005
CONTROL CIRCUIT (cont.)	
Input Transients	Applicable
Noise Immunity	Applicable
Reset	By removing and re-applying DC control voltage
Time to Reset (removal)	5 mSec minimum 100 mSec maximum
ENVIRONMENTAL CHARACTERISTICS	
Case Temperature	
Operating	-54°C to +120°C
Storage	-65°C to +150°C
Shock	
Mechanical	40 G's for 11 mSec
Temperature	-54°C to +120°C Ambient
Vibration	
Sinusoidal (operating)	
G level	15 G maximum
Frequency Range	5 to 2000 Hz
Acceleration	100 G's
Salt Fog	Applicable
Humidity	Applicable
Temperature Altitude	Applicable
Operating Ambient Temperature	-54°C to +120°C
Altitude	Sea level to 100 K ft.
Non-Operating Ambient	-54°C to +120°C
Operating Ambient	-54°C to +120°C
Altitude	.65 to 15.4 psia
Explosive Decompression	Not Applicable

TEST RESULTS - 1 Amp AC Solid State Power Controller
Teledyne P/N 673-10005

PIN IDENTIFICATION

PIN NO.	FUNCTION
1	Trip Indicator
2	Control Input +28 vDC
3	Power Out , AC Return
4	Test Point , A
5	Control Input Return
6	Test Point , G
7	Test Point , K
8	Power In , AC High

TEST	REQUIREMENT MIL-P-81653	RESULTS
GENERAL (all units unless noted)		
Terminal Arrangement	SPST-Normally Open	100 megohms
Insulation Resistance	100 megohms	100 megohms
Dielectric Withstanding Voltage to Case	1000 vAC (RMS)	1500 vAC (RMS)
Isolation Between control and trip terminals shorted and output terminals shorted	1000 vAC (RMS)	1500 vAC (RMS)
Radio Interference	Applicable	MIL-STD-461 Class 1D
Leakage current	6 mA maximum	All units below 2 mA
Power Dissipation		
ON	1.75 watts maximum	1.65 watts
OFF	.310 watt maximum	.300 watt
POWER CIRCUIT (all units unless noted)		
Supply Voltage	124 vAC (RMS) max.	All units OK
	98 vAC (RMS) min.	All units OK
Current		
Rated	1 Ampere	All units OK
Minimum	100 mA	All units OK

TEST RESULTS - 1 Amp AC Solid State Power Controller (cont.)
Teledyne P/N 673-10005

TEST	REQUIREMENT MIL-P-81653	RESULTS
POWER CIRCUIT (cont.)		
Frequency	400 Hz ±5%	All Units OK
Voltage Drop		
No load to Rated	1.5 vAC (RMS) max.	All Units <1.4 vAC (RMS)
Fail Safe	Applicable	Not Tested
Response		
Turn ON Time	1 cycle max.	½ cycle max.
Turn OFF Time	1 cycle max.	½ cycle max.
Trip-Out Time		
Non-repetitive reset	2 sec. max.	<2 sec. all units
Trip Indication		
Current Sink Method		
Tripped	Not Specified	Open Contact 0-32 vDC
Not Tripped	Not Specified	Current Sink 0-100 mA
CONTROL CIRCUIT (all units unless specified)		
Supply Voltage	3.5 to 8.0 vDC	20 to 32 vDC
Turn ON Voltage	3.5 vDC min.	20 vDC min.
Rate of Change	.5 vDC/μSec min.	>.5 vDC/μSec
Turn OFF Voltage	2.5 vDC max.	5 vDC max.
Rate of Change	.5 vDC/μSec min.	>.5 vDC/μSec.
Time to Reset	5 mSec min., 20 mSec max.	5 mSec min., 100 mSec max.

CONTROL INPUT TRANSIENTS (all units unless noted)
A single pulse of plus and minus 100 volt peak amplitude and 100μSec duration repeated 10 times at 3 second intervals. All units tested satisfactorily.
A train of 10 pulses of plus and minus 100 volt peak amplitude and 100μSec duration each, repeated 10 times at 3 second intervals. All units tested satisfactorily.
Repeated above tests between trip terminal and control input return terminal. All units tested satisfactorily.

TEST RESULTS: 1 Amp AC Solid State Power Controller (cont.)
Teledyne P/N 673-10005

TEMPERATURE TESTS (all units unless noted)

The following tests were made at -55°C and +120°C (unless otherwise noted)

- Insulation Resistance
- Dielectric Withstanding Voltage
- Isolation
- Leakage Current
- Rated Current and Voltage (-55°C and +125°C)
- Voltage Drop (-55°C and +125°C)
- Control Circuit (-55°C and +125°C)
- Reset Circuit (-55°C and +125°C)

On the above tests, all units tested satisfactorily.

Trip-Out under overload (-55°C to +85°C)

Note: The Triac chip that was used failed to turn off when an overload @ 125°C was applied. The controller operated satisfactorily to +85°C under all overload conditions. This situation can be corrected by using a power Triac chip of different characteristics.

TRIPOUT TIME CHARACTERISTICS

Tripout time versus percentage of overload are shown in Figs. 33, 34, 35 and 36 for 3 prototype AC controllers.

Note: Where units failed to fall within the trip-out time versus overload, this situation can be corrected by putting more effort on the timing and shaping circuit controlling trip-out.

TEST CIRCUITS FOR AC POWER CONTROLLERS

The test circuits for AC power controllers are shown in Fig. 37 and Fig. 38.

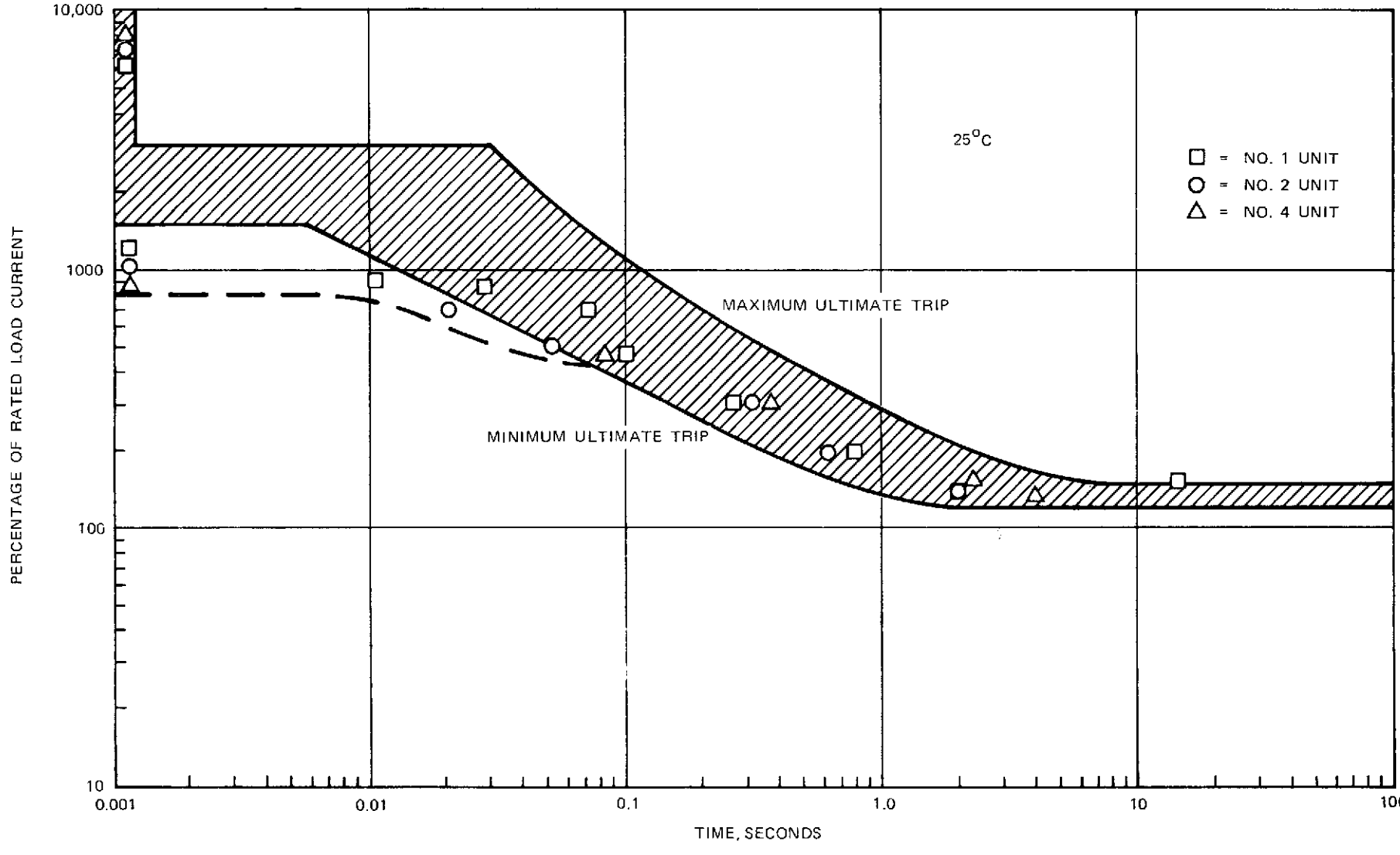


FIG. 33. TRIP CHARACTERISTICS 1 AMP AC POWER CONTROLLER +25°C

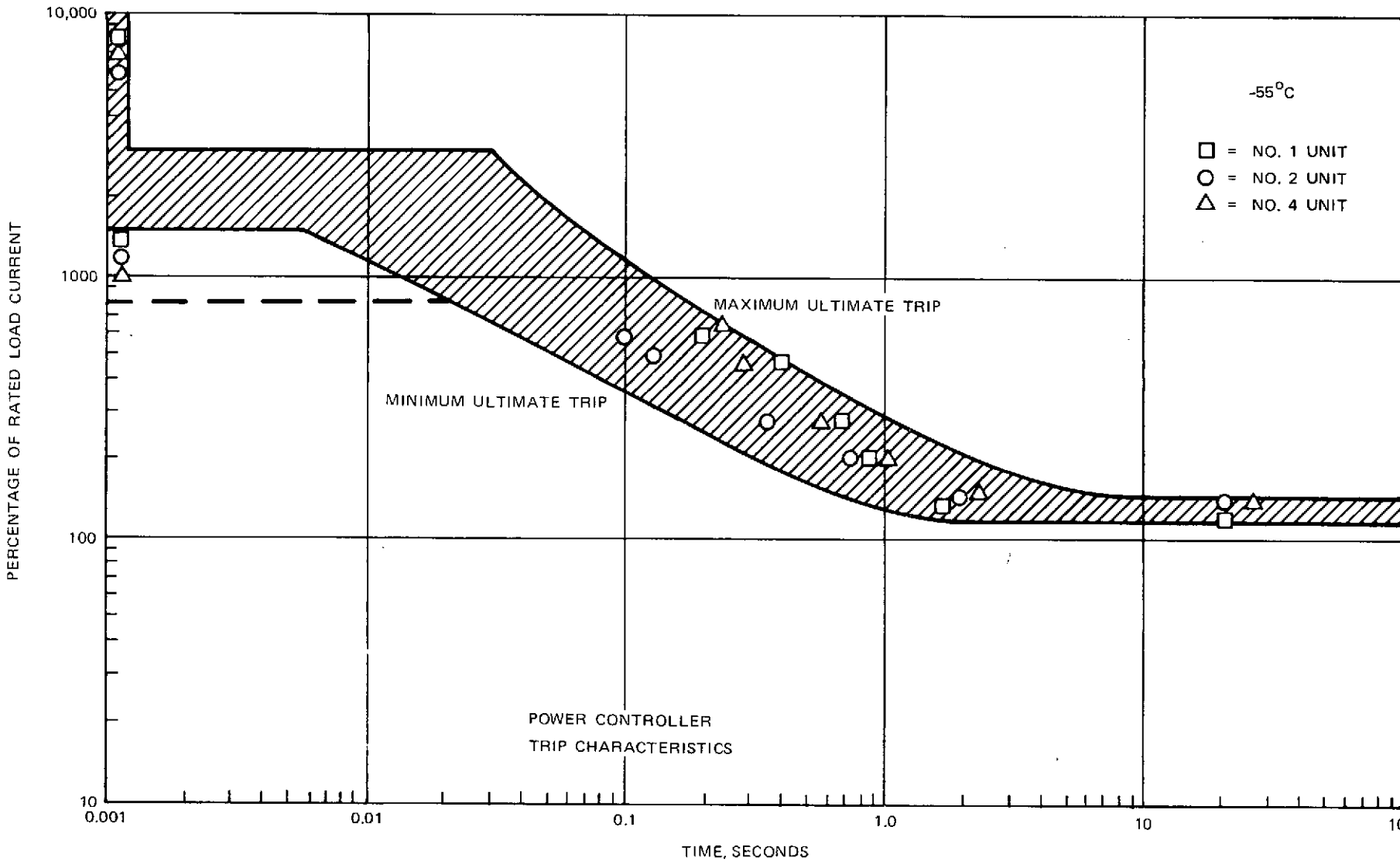


FIG. 34. TRIP CHARACTERISTICS 1 AMP AC
POWER CONTROLLER -55°C

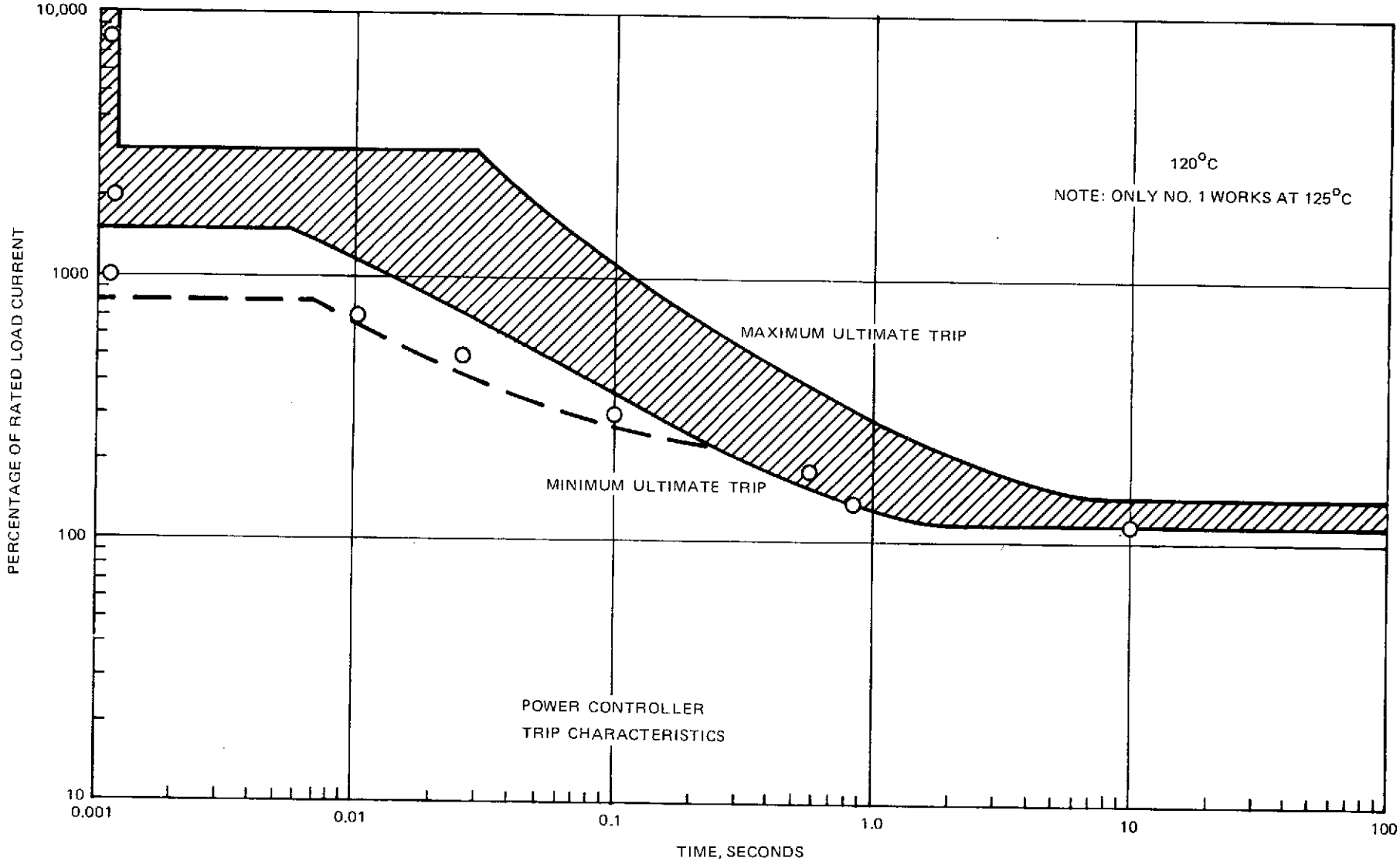


FIG. 35. TRIP CHARACTERISTICS 1 AMP AC
POWER CONTROLLER +120°C

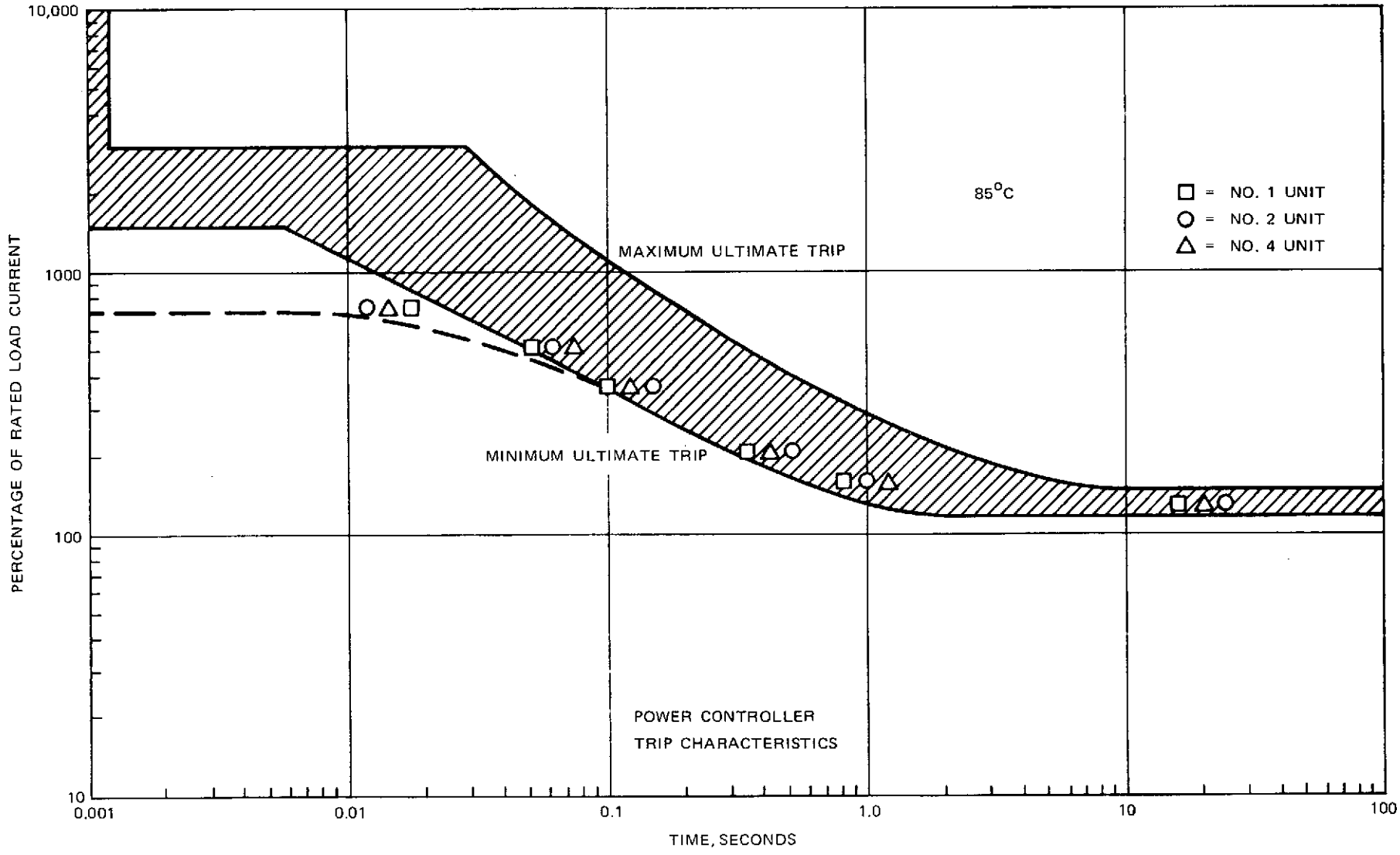


FIG. 36. TRIP CHARACTERISTICS 1 AMP AC
POWER CONTROLLER +85°C

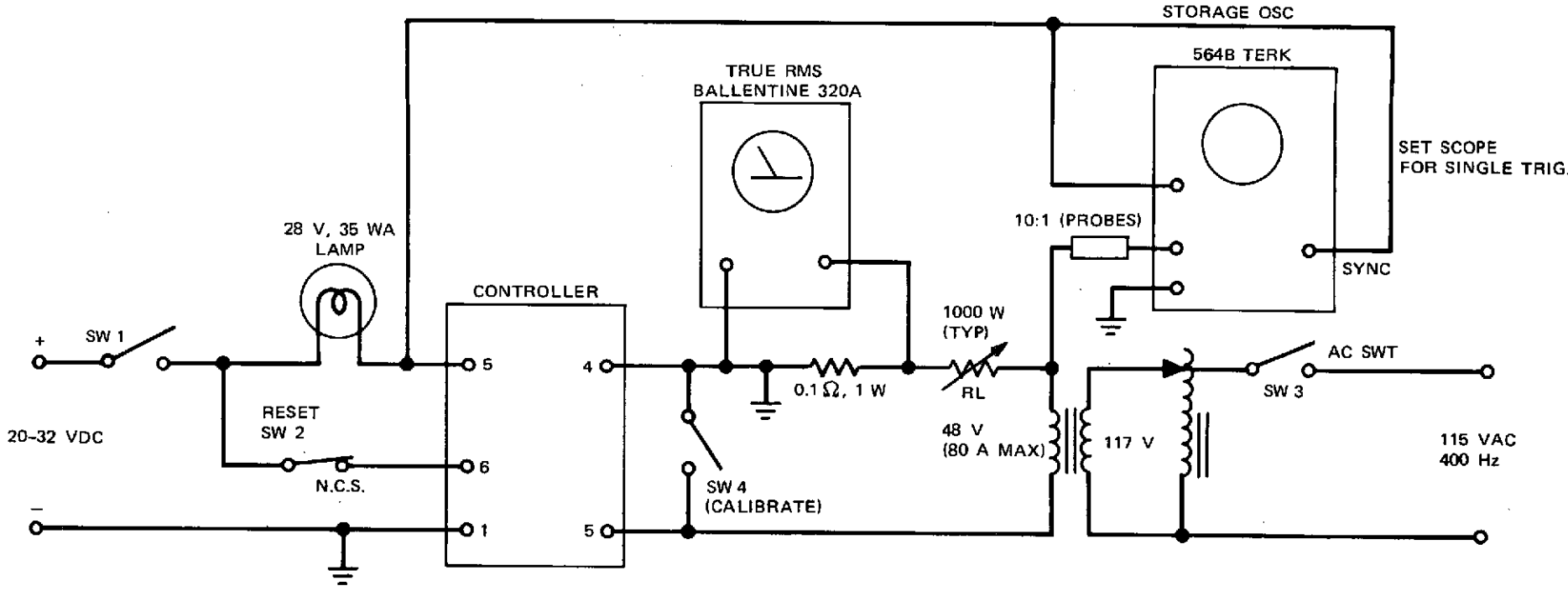


FIG. 37. TEST CIRCUIT FOR TRIP-OUT TIME vs OVERLOAD

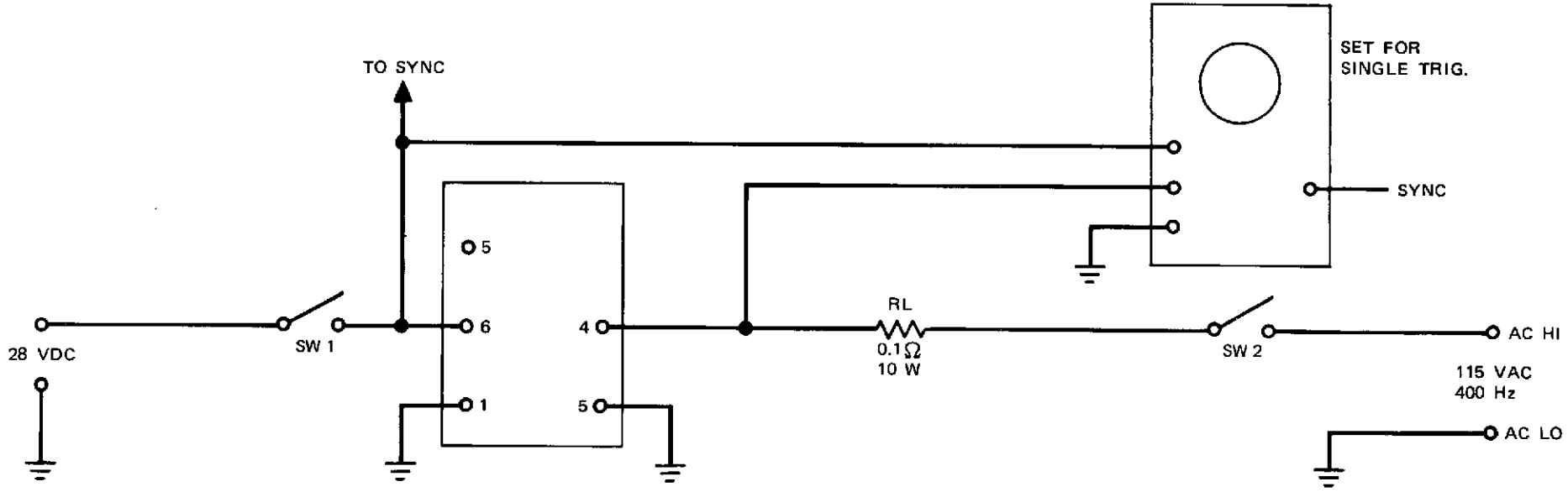


FIG. 38. TEST CIRCUIT FOR SHORT CIRCUIT