NASA CR- 13288 T

Optimal Space Communications Techniques

Status Report

January 22, 1973 – July 21, 1973

National Aeronautics and Space Administration

Goddard Space Flight Center

under

NASA Grant NGR 33-013-077

COMMUNICATIONS SYSTEMS LABORATORY

DEPARTMENT OF ELECTRICAL ENGINEERING

THE CITY COLLEGE OF
THE CITY UNIVERSITY of NEW YORK

Donald L. Schilling

Professor of Electrical Engineering

Principle Investigator

Optimal Space Communication Techniques

Status Report

January 22, 1975 - July 21, 1975

Prepared for

National Aeronautics and Space Administration

Goddard Space Flight Center

under

NASA Grant NGR 33-016-077

Principal Investigator

Donald L. Schilling

Professor of Electrical Engineering

COMMUNICATIONS SYSTEMS LABORATORY

DEPARTMENT OF ELECTRICAL ENGINEERING

AN ALL DIGITAL PHASE-LOCKED LOOP FOR FM DEMODULATION

by

JOHN GRECO

Optimal Space Communications Techniques

Status Report

January 22, 1973 – July 21, 1973

Prepared for

National Aeronautics and Space Administration

Goddard Space Flight Center

under

NASA Grant NGR 33-013-077

Principal Investigator

Donald L. Schilling

Professor of Electrical Engineering

COMMUNICATIONS SYSTEMS LABORATORY

DEPARTMENT OF ELECTRICAL ENGINEERING

TABLE OF CONTENTS

Introduction

This status report summarizes one aspect of the research sponsored by the National Aeronautics and Space Administration under NASA Grant NGR 33-013-077 for the period 22 January 1973 through 21 July 1973.

Part I of this report is the culmination of our study of the Digital PLL FM Demodulator. Here we show that the 2nd order PLL Demodulator yields a lower threshold than the 1st or 3rd order loops. Although the study was performed using proportional plus integral filters, it is felt that changes in the filter pole-zero pattern will produce only second-order effects and not alter our main conclusion.

Part II describes a new area of PLL investigation.

Particpating in this program were:

Drs. I. Paz and D. L. Schilling

and Doctoral Students:

Messrs: J. F. Greco, M. Steckman and D. Ucci

AN ALL DIGITAL PHASE-LOCKED LOOP FOR FM DEMODULATION

by

JOHN GRECO

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

With the recent trend toward digital processing of signals and the advances in digital circuit technology, various digital designs of phase-locked loops have emerged. At recent conferences [1], [2] entire technical sessions have been devoted exclusively to digital phase-locked loops.

The development of digital phase locked-loops has proceeded similarly to the analog phase-locked loop development in that two basic problems have been considered: tracking a carrier signal (or synchronizing bit streams) and demodulating FM signals. Typical problems associated with carrier tracking are the mean time to gain lock, steady-state phase error probability density, mean time to lose lock, and the location of threshold. Analyses concerning FM demodulation concern the loop performance based of signal-to noise calculations and the location of threshold with a modulated input.

One method used to track a carrier involves varying the sampling time [3] in an attempt to lock on to the zero crossings. Another method [4] uses in-phase sampling and quadrature-phase sampling in order to determine phase error. In addition, these sampling rates are variable. Other techniques [5], [6], which are not completely digital, require mid-phase and in-phase integrations, followed by a multiplication in order to obtain phase error information.

One of the earliest schemes for constructing a digital phase-locked loop for FM demodulation [7] employed a voltage controlled oscillator (VCO) using shift registers and a gate which detects when a certain number of pulses are counted. The phase error signal is obtained using an exclusive-or gate whose inputs are the VCO output and a hard-limited version of the input. The input to such a digital phase-locked loop does not consist of a sampled signal, but rather the hard limited form of the FM signal, which provides information about its zero crossings. Other

1

digital techniques [8], [9], [10] use uniform samples of the FM signal but require a voltage controlled oscillator and multiplier for phase detection. The performance of these systems was obtained by computer simulation. It is also possible to use a variable sampling frequency [11] to demodulate FM.

It is interesting to note the digital phase-locked loop progress being made abroad. In Japan, hybrid systems have been studied [12], [13] in which the sampling process occurs after the phase detector, and the digital signal converted back into analog form to drive a voltage-controlled oscillator. Such phase-locked loops with sampled-data control were the forerunners to the all digital phase-locked loops currently being investigated.

The digital phase-locked loop presented in this thesis operates as a (nonlinear) digital filter: the input is the uniform sample sequence of the FM signal and the output is the sample sequence of the demodulated message. All operations within the loop are digital: gating, storing in registers, shifting, adding binary words, and the VCO algorithm. Further-more, the system is designed so that it operates on the input sequence in real-time, requiring all the digital operations to be performed within the sampling period. This feature enables the digital phase-locked loop to be constructed and tested using actual modulation, instead of a computer simulation. Since the digital phase-locked loop is designed using stan-dard logic operations, it can be constructed using LSI, with its advantages of low cost and high reliability.

The structure of the digital phase-locked loop presented in this thesis is similar to that of an analog phase-locked loop: the phase error between input and VCO is generated by taking the product of these two signals, and this error signal is processed by a digital filter. Two dis-tinguishing features of this digital phase-locked loop are the real-time and synchronous operation. The restriction of real-time operation places limitations on the number and type of digital calculations allowable, as

2

well as placing an upper limit on the sampling frequency, as all computations must be performed with one sampling period. As a result, it is necessary to sample the IF FM signal at a frequency below the IF frequency; the permissible sampling frequencies for this sub-sampling process are examined in Ch. 2. A second consequence of real-time operation is the preclusion of digital multipliers, as digital multiplication requires excessive computation time. Hence all gains appearing in the digital phase-locked loop are powers of 1/2, which are realized by shifting a binary word. However, we must still construct a phase detector without using a binary multiplication.

The solution to the phase detector problem is to use a voltage controlled oscillator whose wave form is a square wave, having the values ±1. Then the binary multiplication of the input by the VCO signal reduces to a logic operation: the bits of the input word are exclusive-or gated by the VCO output. Since the VCO output is required only at the sampling times, an actual oscillator (or counter) is not present in the system; instead, an algorithm is developed which determines the correct VCO output at the sampling time given all the previous VCO inputs. This algorithm is realized as a logic operation which requires negligible computation time.

Although using a square wave VCO makes real-time operation possible, the square wave introduces undesirable harmonics into the digital phase-locked loop. It is impossible to have all of these harmonics fall outside the loop bandwidth because of the frequency aliasing produced by sampling. In order that these harmonics have a minimum effect on the loop operation, a design condition is derived. The harmonic contribution to the output is also calculated.

The digital phase-locked loop internal arithmetic is performed with a finite number of bits and therefore quantization noise is present. An examination of the quantization noise at the error signal leads to a second design equation for the loop.

The original motivation for designing a digital phase-locked loop

3

was to obtain threshold extension over a discriminator. Computer
analyses of analog phase-locked loops [14] predicted up to seven
dB threshold extension with a third order loop. In order to obtain an
indication of the digital phase-locked loop performance near threshold,
a deterministic model for an input noise spike is introduced to the loop
equation, which is solved on a general-purpose digital computer, and
the result examined to see whether or not the digital phase-locked loop
follows the input spike. Although this method cannot predict the abso-
lute location of threshold, it does give a relative performance measure
between the first, second, and third order digital phase-locked loops.

The digital phase-locked loops were constructed using DTL and
TTL logic cards and tested with sinusoidal and constant modulation.
It is found that the first order loop threshold is identical to that of a
discriminator, the second order loop provides threshold extension over
the first order loop, and, most importantly, the third order loop does not
provide any threshold extension beyond the second order loop and it can
degrade the performance. This important result is found to be caused by
the third order loop losing lock temporarily in response to an input noise
spike.

In addition to the experimental determi   of threshold, the effect
of the number of bits used and the resulting truncation on the threshold
is determined experimentally. It is found that if the sampled input signal
is coded into a three-bit binary word, threshold is five dB worse than for
coding into a ten-bit binary word. The result of truncating to ten bits all
binary words in the loop is to lose one dB in threshold.

CHAPTER 2

THE ALL DIGITAL PHASE-LOCKED LOOP

In this chapter, the structure of the digital phase-locked loop is developed, with particular attention to the real-time operation of the system. The restriction that the unit operate in real-time places limitations on the sampling frequency and on the number and type of calculations performed by the loop. As a result, a computationally simple algor' m is developed to represent a square wave voltage-controlled oscillator; but although the algorithm is simple, the square wave introduces harmonics into the loop. A condition which minimizes the harmonic contribution is developed, and it serves as a design equation. A second disign equation involving quantization noise is introduced concerning the maximum phase error allowable in the digital phase-locked loop.

2.1 Digital Phase-locked Loop Structure

The block diagram of the all digital phase-locked loop (DPLL) is shown in Fig. 2.1-1. The received noisy FM signal is band-pass filtered, yielding $x(t)$, sampled, and converted to a binary word, x_k. From this point on, all signals in the DPLL appear as binary words. The DPLL error signal, e_k, is the product of the input x_k and the digital voltage controlled oscillator (VCO) output w_k. Digital filtering of this error signal yields the loop output, y_k, which in turn determines the new VCO output, w_{k+1}. The particular digital filters considered are a proportional path, proportional plus integral paths, and proportional plus integral plus double integral paths, yielding first, second, and third order DPLL's respectively. The DPLL output is converted to a staircase signal by a digital-to analog (D/A) converter and low pass filtered to produce the analog output, $y(t)$.

The digital phase-locked loop is designed to operate as a real-time computer, requiring all calculations to be performed in one sampling period. This requirement places restrictions on the number and type of arithmetic operations possible, and on the sampling frequency.
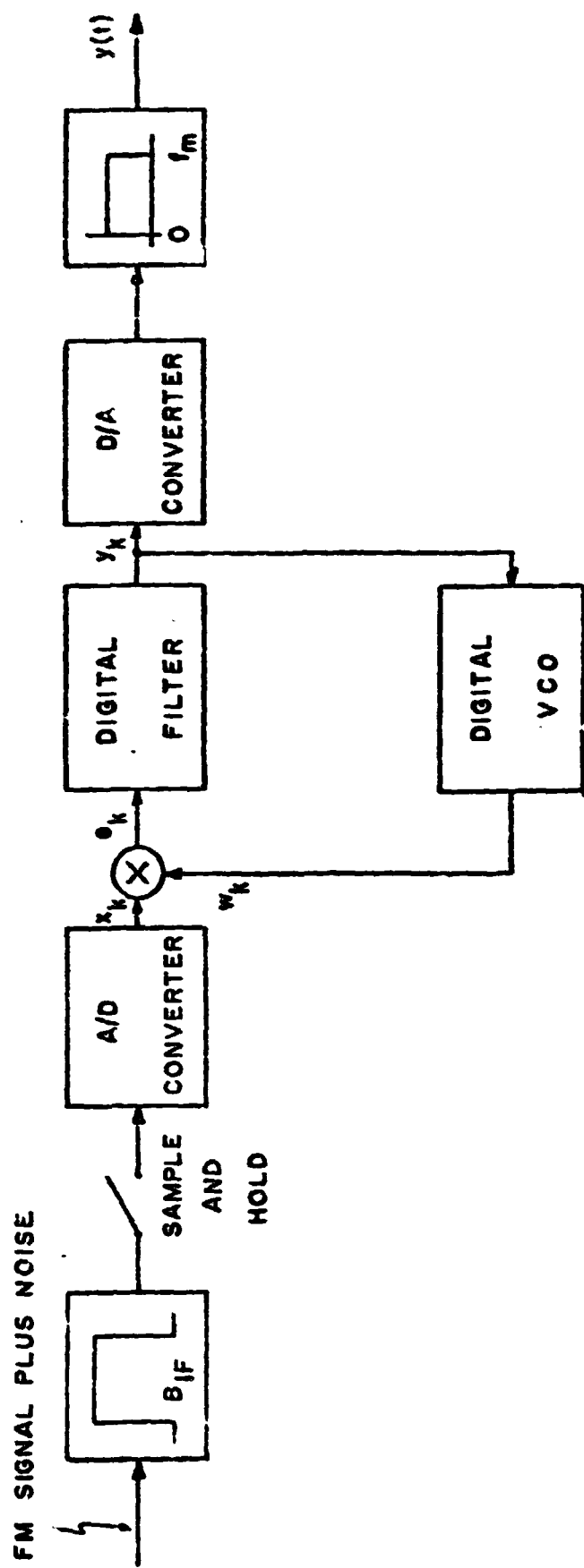
5

Fig. 2.1-1. The all digital phase-locked loop.

2.2 Determination of Sampling Frequency

The digital phase-locked loops were constructed using DTL and TTL logic, having speeds of 1 MHz and 10 MHz respectively. Allowing for ten logic operations per computation interval (which is equal to the sampling period), the sampling frequency must be less than $1/(10 \cdot 1 \mu sec) = 100$ KHz. Therefore it is impossible to sample the bandpass signal $x(t)$ (Fig. 2.1-1) at the Nyquist rate or greater.

It is, however, possible to sample the bandpass signal below the Nyquist rate without losing any information. Let $x(t)$ occupy a bandwidth B Hz centered about f_O Hz, as shown in Fig. 2.2-1a. Then it can be shown [14] that an allowable sampling rate is:

$$f_s \geq 2B \tag{2.2-1a}$$

$$n f_s = f_O \pm B/2 \tag{2.2-1b}$$

There are other possible smapling frequencies. To obtain them, first consider $x(t)$ sampled at twice the highest frequency component: $f_s = 2(f_O + B/2)$. The sampled spectrum appears in Fig. 2.2-1b. If the sampling frequency is reduced slightly, spectral overlap occurs. But if we continue reducing f_s, we reach the situation of Fig. 2.2-1c, where $f_s = 2(f_O - B/2)$ and no overlap is present. It is possible now to reduce f_s until the arrangement of Fig. 2.2-1d appears, where $f_s = f_O + B/2$. Hence, f_s can fall anywhere within the interval

$$[(f_O + B/2), 2(f_O - B/2)]$$

Further reduction of f_s yields overlap, until we reach the situation of Fig 2.2-1e; here $f_s = f_O - B/2$. We can continue to reduce f_s until Fig. 2.2-1f results with $f_s = 2(f_O + B/2)/3$. Therefore, the sampling frequency may fall anywhere in the interval

$$[2(f_O + B/2)/3, (f_O - B/2)]$$

Continuing this process, the next allowable sampling frequency is $f_s = 2(f_O - B/2)/3$ shown in Fig. 2.2-1g, and f_s may be reduced until $f_s = 2(f_O + B/2)/4$ as in Fig 2.2-1h, yielding the interval
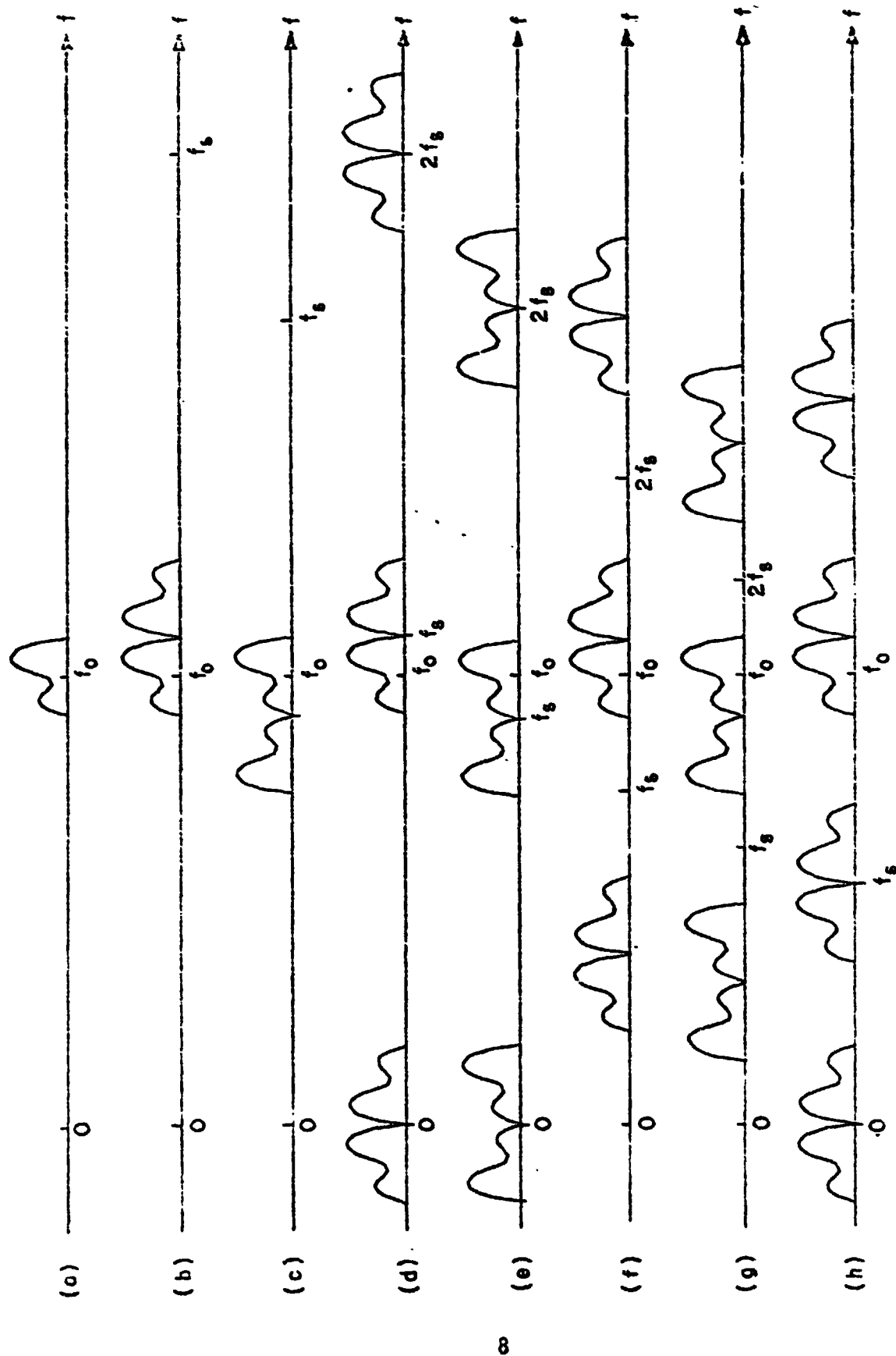
Fig. 2.2-1. Spectra of the bandpass signal and sampled bandpass signal for various sampling frequencies, f_s.

8

$$[2(f_o + B/2)/4, \ 2(f_o - B/2)/3 \ ]$$

The generalization of this procedure is that the sampling frequency must fall in the interval

$$\left[\ \frac{2}{k+1}(f_o + B/2), \ \frac{2}{k}(f_o - B/2) \right] , \tag{2.2-2}$$

with k an integer, for no spectral overlap to occur. Of course, we must also have $f_s \geq 2B$. Notice that the values of f_s specified by Eq. (2.2-1b) are included in the endpoints of the intervals of Eq. (2.2-2).

Summarizing the above, if $x(t)$ is a bandpass signal occupying a bandwidth B Hz centered about f_o Hz, then $x(t)$ is specified completely by its sample values at instants $t = k/f_s$ where

$$f_s \geq 2B \tag{2.2-3a}$$

$$f_s \ \epsilon \left[\frac{2}{1}(f_o + B/2), \ \infty \right) \ \cup$$

$$\left[\frac{2}{2}(f_o + B/2), \ \frac{2}{1}(f_o - B/2) \right] \ \cup$$

$$\left[\frac{2}{3}(f_o + B/2), \ \frac{2}{2}(f_o - B/2) \right] \ \cup$$

$$\vdots$$

$$\left[\frac{2}{n+1}(f_o + B/2), \ \frac{2}{n}(f_o - B/2) \right] \ \cup$$

$$\vdots$$

$$\tag{2.2-3b}$$

The important conclusion is that it is possible to sample $x(t)$ at a rate slower than the carrier frequency f_o.

For ease in implementation, we shall sample according to

$$f_s = 2Bm \tag{2.2-4a}$$

$$n.f_s = f_o - B/2 \tag{2.2-4b}$$

where m and n are positive integers; together, these imply

$$f_o/f_s = n + 1/4m \tag{2.2-5}$$

9

Using $m = 1$ in Eqs. (2.2-4) leads to an interesting interpretation. Writing the bandpass signal $x(t)$ as

$$x(t) = a(t) \cos 2\pi f_0 t + b(t) \sin 2\pi f_0 t \qquad (2.2-6)$$

where $a(t)$ and $b(t)$ are bandlimited to $B/2$ Hz, the sample values are, using Eq. (2.2-5)

$$x(kT_s) = a(kT_s) \cos k\pi/2 + b(kT_s) \sin k\pi/2 \qquad (2.2-7)$$

Note that if k is an even integer, $k = 2p$,

$$x(2pT_s) = (-1)^p a(2pT_s) + 0 \qquad (2.2-8)$$

and if k is an odd integer, $k = 2p + 1$,

$$x[(2p + 1)T_s] = 0 + (-1)^p b[(2p + 1)T_s] \qquad (2.2-9)$$

Hence the even numbered samples provide information for reconstructing $a(t)$, since the Nyquist rate for $a(t)$ is $2(B/2) = f_s/2$, while the odd numbered samples provide information for reconstructing $b(t)$. Having determined $a(t)$ and $b(t)$, $x(t)$ is determined via Eq. (2.2-6).

2.3 The Digital Voltage Controlled Oscillator

A voltage controlled oscillator (VCO) is an oscillator whose frequency deviation from its nominal frequency is proportional to the input:

$$w(t) = g\left(2\pi f_0 t + G_{VCO} \int_{-\infty}^{t} y(\tau) \, d\tau\right) \qquad (2.3-1)$$

where
$\quad y(t) = $ VCO input
$\quad w(t) = $ VCO output
$\quad f_0 = $ VCO nominal frequency
$\quad g(\cdot) = $ VCO waveform, with $g(x + 2\pi) = g(x)$
$\quad G_{VCO} = $ VCO gain, in (rad/sec)/volt.

In the digital phase-locked loop we are interested solely in the VCO output at the sampling instants since only these values are required for the computations. The VCO output at the sampling instant $t = kT_s$

10

is, using Eq. (2.2-5)

$$w(kT_s) \equiv w_k = g(k\pi/2m + G_{VCO} \int_{-\infty}^{kT_s} y(\tau)\,d\tau) \quad (2.3\text{-}2)$$

Since we have $y(kT_s) \equiv y_k$ available, as opposed to $y(t)$, the integration is performed digitally as a summation:

$$w_k = g(k\pi/2m + G_{VCO} \sum_{p=-\infty}^{k-1} y_p) \quad (2.3\text{-}3)$$

Note that the summation extends only up to $p = k-1$; this is a consequence of the causality of the digital filter. Defining the VCO phase by

$$\hat{\phi} = G_{VCO} \sum_{p=-\infty}^{k-1} y_p \quad (2.3\text{-}4)$$

we obtain the recursive relation

$$\hat{\phi}_k - \hat{\phi}_{k-1} = G_{VCO} y_{k-1} \quad (2.3\text{-}5)$$

and the VCO output is

$$w_k = g(k\pi/2m + \hat{\phi}_k) \quad (2.3\text{-}6)$$

Fig. 2.3-1 illustrates the computations required to generate the VCO output. The VCO input y_k (identical to the DPLL output) is scaled by G_{VCO} and digitally integrated (or accumulated), forming the VCO phase $\hat{\phi}_k$, which is then added to the carrier term, $k\pi/2m$. And then the VCO waveform $g(\cdot)$ must be evaluated.

We can avoid the need for calculating the carrier term $k\pi/2m$ by recognizing that

$$k\pi/2m + \hat{\phi}_0 + \sum_{p=0}^{k-1} G_{VCO} y_k$$

$$= \hat{\phi}_0 + \sum_{p=0}^{k-1} (\pi/2m + G_{VCO} y_k) \quad (2.3\text{-}7)$$

That is, the carrier term may be obtained by integrating the constant $k\pi/2m$. Hence, we may modify Fig. 2.3-1 to Fig. 2.3-2, which is computationally simpler, as now only a constant term is added at each calculation.
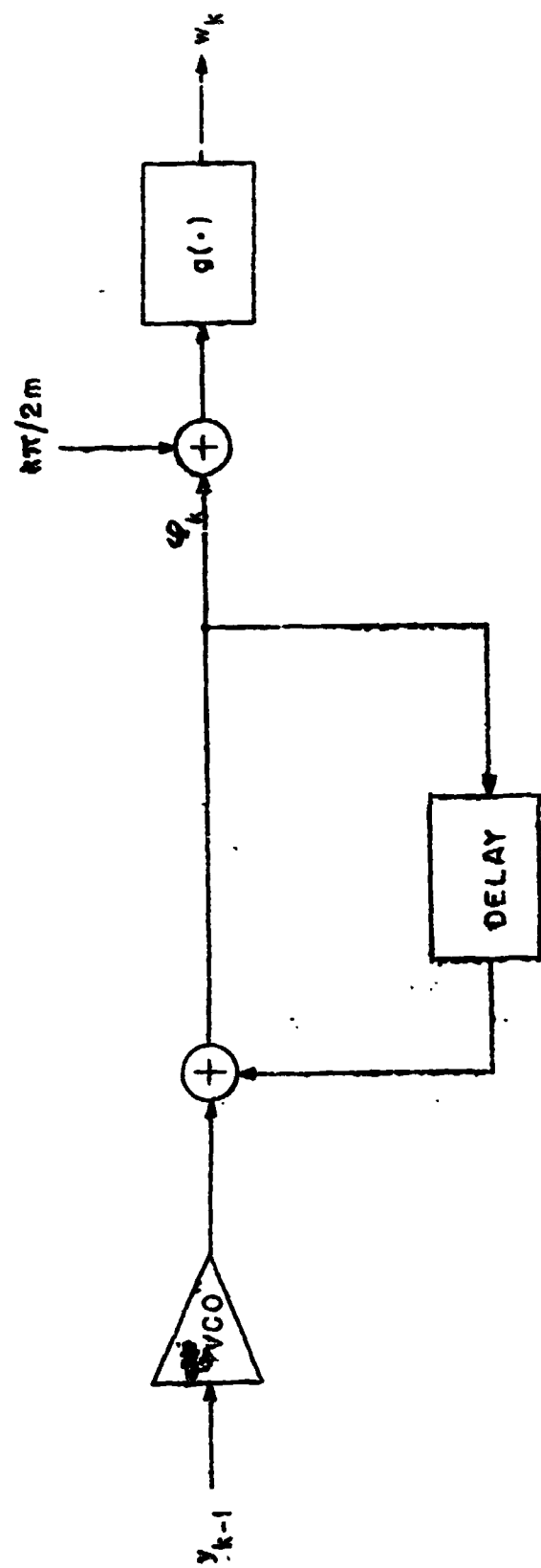
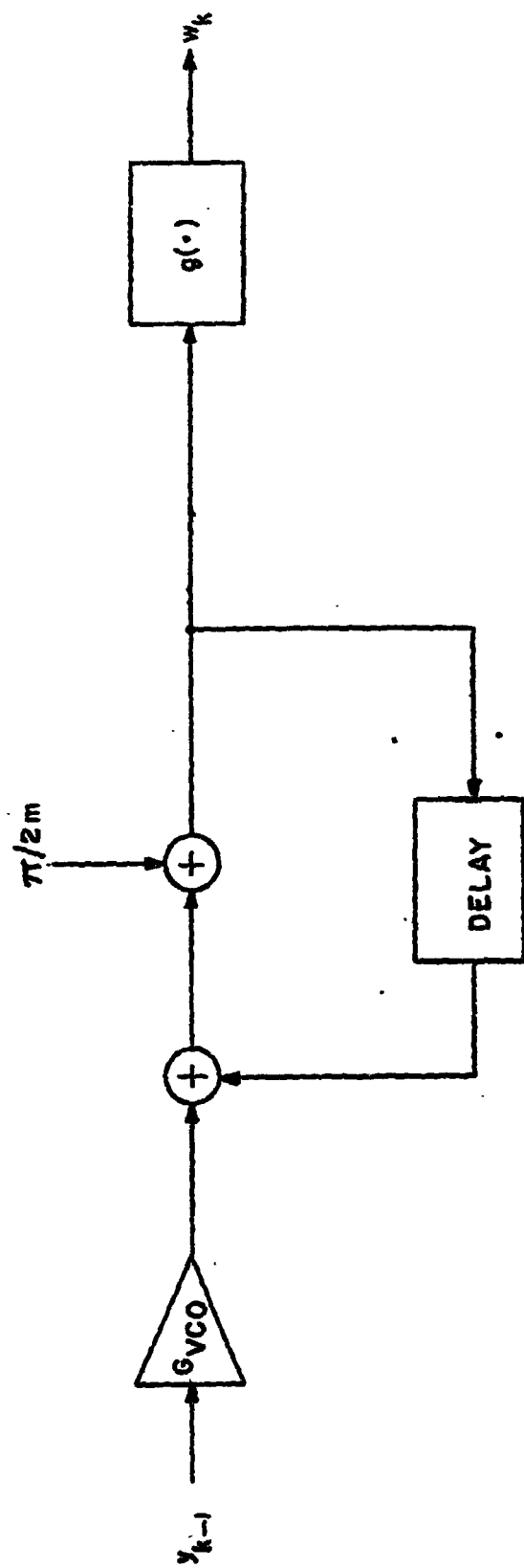Fig. 2.3-1. The digital voltage controlled oscillator.

Fig. 2.3-2. The digital VCO, with the carrier term obtained by integration of the constant term, $\pi/2m$.

The next task is to choose the VCO waveform, $g(\cdot)$. Two factors are important here: the complexity of the $g(\cdot)$ computation and the multiplication of the VCO output and the DPLL input.

The function computation must be sufficiently brief as it must be performed within the computation interval. This can be accomplished using a read only memory (ROM). The function argument is used to _address the ROM which is preprogrammed with the function values. A typical access time is 22 nsec using TTL.

The function values determine the complexity of the digital multiplication required. For, if the VCO output can assume any value (i.e., any of the discrete quantized values), as is the case for $g(x) = \sin x$, then the digital multiplier must be able to multiply two arbitrary binary numbers, an operation which more computation time than is available. One solution to this problem is to utilize a ROM: the binary words to be multiplied are used ￫ address the ROM, by concatenating the two words, for example, and the ROM stores the product at this address. This scheme, however, is made impractical by the memory capacity required. For example, if we are working with 10-bit arithmetic, there are $2^{10} \cdot 2^{10} > 10^6$ possible products to compute, and hence the ROM must store one million 10-bit words.

A solution to the multiplication problem is to choose the VCO waveform $g(\cdot)$ to be a square wave, having only values ± 1:

$$g(x) = Sq(x) \equiv \begin{cases} +1, & 0 \leq x \leq \pi \\ -1, & \pi \leq x \leq 2\pi \end{cases}$$

$$g(x) = g(x + 2\pi) \tag{2.3-8}$$

Hence the binary multiplication is reduced to a simple logic operation: if $g(x) = +1$, pass the input with no change; if $g(x) = -1$, form the "one's complement" (or whatever negative arithmetic is used) of the input. This operation is accomplished using exclusive-or gates and sufficient computation time is available.

14

To complete the digital VCO design, we must specify how $g(\cdot)$ is computed.

2.4 Digital VCO Algorithm

Having decided that the VCO outputs are limited to ± 1, we must now determine which of the two is correct, given the VCO argument, $k\pi/2m + \hat{\phi}_k$. That is, we must determine whether the VCO argument falls in the interval $[0, \pi)$ or $[\pi, 2\pi)$. Moreover, the intervals are considered modulo 2π to account for the periodicity of $g(\cdot)$. But the binary numbers group themselves naturally as a result of the pattern of ones and zeros. For example, if we look at a list of the binary numbers from 0 to 7, shown in Table 2.4-1, and focus attention on the second digit, we immediately see that this digit partitions the orginal numbers into groups of two. Furthermore, we can arbitrarily say that the first group represents the $[0, \pi)$ interval, the next group represents the $[\pi, 2\pi)$ interval, the next group represents the $[2\pi, 3\pi)$ interval, and so on. In fact, if the list of binary numbers is continued above 7, the same identification can be made using the second bit, since this bit always exhibits a periodic pattern. Furthermore, if we consider negative numbers using offset binary, the same identification can be made, as is seen in Table 2.4-2. There is an ambiguity at zero since there are two binary representations of zero and hence the VCO output depends on how the value zero is approached. But this difficulty is minor, as the VCO argument will rarely be exactly zero.

Therefore, the VCO output is determined by one bit of the binary word representing the VCO argument: if this bit is a 0, the VCO output is $+1$; if this bit is a 1, the VCO output is -1. Also, to allow for the periodicity in $Sq(\cdot)$, the adder used to integrate the VCO input is allowed to overflow. The particular bit used to determine the VCO output fixes the VCO gain. Above we used the 2's place digit—hence the interval $[0, 2^1)$ corresponds to the interval $[0, \pi)$, producing the gain

15

Binary Numbers, 0 to 7	2's Place Digit
1 1 1	1
1 1 0	1
1 0 1	0
1 0 0	0
0 1 1	1
0 1 0	1
0 0 1	0
0 0 0	L

Table 2.4- 1. The binary numbers and their two's place digit

Decimal No.	Offset Binary No.	2's Place Digit
+ 7	1 1 1 1	1
6	1 1 1 0	1
5	1 1 0 1	0
4	1 1 0 0	0
3	1 0 1 1	1
2	1 0 1 0	1
1	1 0 0 1	0
0	1 0 0 0	0
	0 1 1 1	1
- 1	0 1 1 0	1
- 2	0 1 0 1	C
- 3	0 1 0 0	0
- 4	0 0 1 1	1
- 5	0 0 1 0	i
- 6	0 0 0 1	0
- 7	0 0 0 0	0

Table 2.4-2. The offset binary numbers and their two's place digit.

$\pi/2^1$ (rad/sec)/binary number. If the quantization step size is S volts, the VCO gain is $\pi/2^1$ S (rad/sec)/volt. In general, using the 2^n place digit produces the gain $\pi/S\ 2^n$ (rad/sec)/volt.

Note that this gain is implicitly introduced by the $\eta(\cdot)$ calculation and so the VCO gain is not accurately presented in Fig. 2.3-2. Fig. 2.4-1 corrects the situation, where both an explicit gain, g_1, as well as the implicit gain g_2 are shown. The VCO gain includes both:

$$G_{VCO} = g_1 \cdot g_2$$

Note that we must now add the constant $\pi/2m$ with the implicit gain removed; hence we add the term $(\pi/2m)/g_2$. Also note that the output is labeled B_n, the 2^n bit of the integrator binary word. The VCO output w_k is determined from B_n via

$$w_k = \begin{cases} +1, & B_n = 0 \\ -1, & B_n = 1 \end{cases}$$

If m is a power of 2, the term $(\pi/2m)/g_2$ is simply represented. For example, if the VCO output is determined by the 2^4 bit (n = 4) then

$$\pi/g_2 = 10000$$

and

$$\pi/2g_2 = 01000$$

$$\pi/4g_2 = 00100$$

$$\pi/8g_2 = 00010$$

$$\pi/16g_2 = 00001.$$

Of course, it is also possible to obtain values which are combinations of the above, such as

$$\pi/(8/5)g_2 = \pi/2g_2 + \pi/8g_2 = 01010.$$

Finally, in constructing the DPLL the VCO output $w_k = \pm 1$ is never actually generated. Instead, the B_n bit is used directly to process the
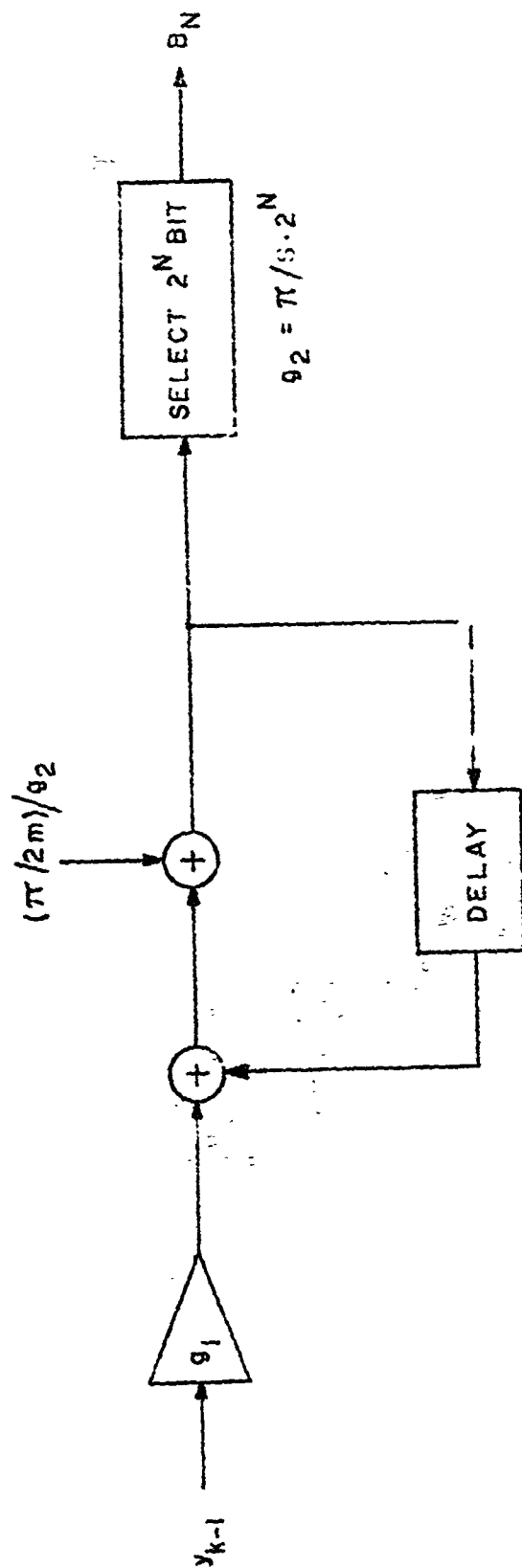
17

Fig. 2.4-1. The digital VCO, showing the explicit gain, g_1, and the implicit gain, g_2.

y_{k-1}

g_1

$(\pi/2m)/g_2$

DELAY

SELECT 2^N BIT

$g_2 = \pi/s \cdot 2^N$

B_N

input binary. For if either one's complement or offset binary arithmetic is employed, then negating a binary word is equivalent to complementing it. Hence the B_n bit can gate each bit of the put through an exclusive-or gate, as shown in Fig. 2.4-2. If $B_n = 0$, gate output is identical to the input (a multiplication by $+1$) while $B_n = 1$, the gate output is the complement of the input (a multiplication by -1). Hence the multiplier output is indeed $w_k \cdot x_k$. Of course, if two's complement arithmetic were employed, the exclusive-or gating operation must be modified.

Summarizing, we see that one bit of the VCO argument serves to determine the VCO output, and the particular bit used determines the implicit VCO gain. The product of DPLL input and VCO output is realized as an exclusive-or gating operation, requiring negligible computation time.

2.5 Design Considerations--Maximum Error Signal

In order for the DPLL to demodulate without distortion, the error signal, e_k in Fig. 2.1-1, must be an accurate measure of the phase error between the input and VCO. The product of input signal and VCO output yields the term $\sin(\varphi_k - \hat{\varphi}_k)$, and therefore the difference $\varphi_k - \hat{\varphi}_k$ must be kept much less than $\pi/2$ to have $e_k \approx \varphi_k - \hat{\varphi}_k$; the smaller this phase error, the better is the approximation. However, e_k is represented by a binary word having a fixed number of bits, and decreasing its range of values deteriorates the signal-to-quantization noise ratio. Hence a trade-off exists between the accuracy or the approximation $\sin(\varphi_k - \hat{\varphi}_k) \approx \varphi_k - \hat{\varphi}_k$ and the signal-to-quantization noise ratio.

Let the system A/D converter code analog signals amplitude limited to V volts into B-bit binary numbers, producing a quantization step size S:

$$S = 2V/2^B \tag{2.5-1}$$

Let the phase difference $\varphi_k - \hat{\varphi}_k$ range over 2 M of these levels:
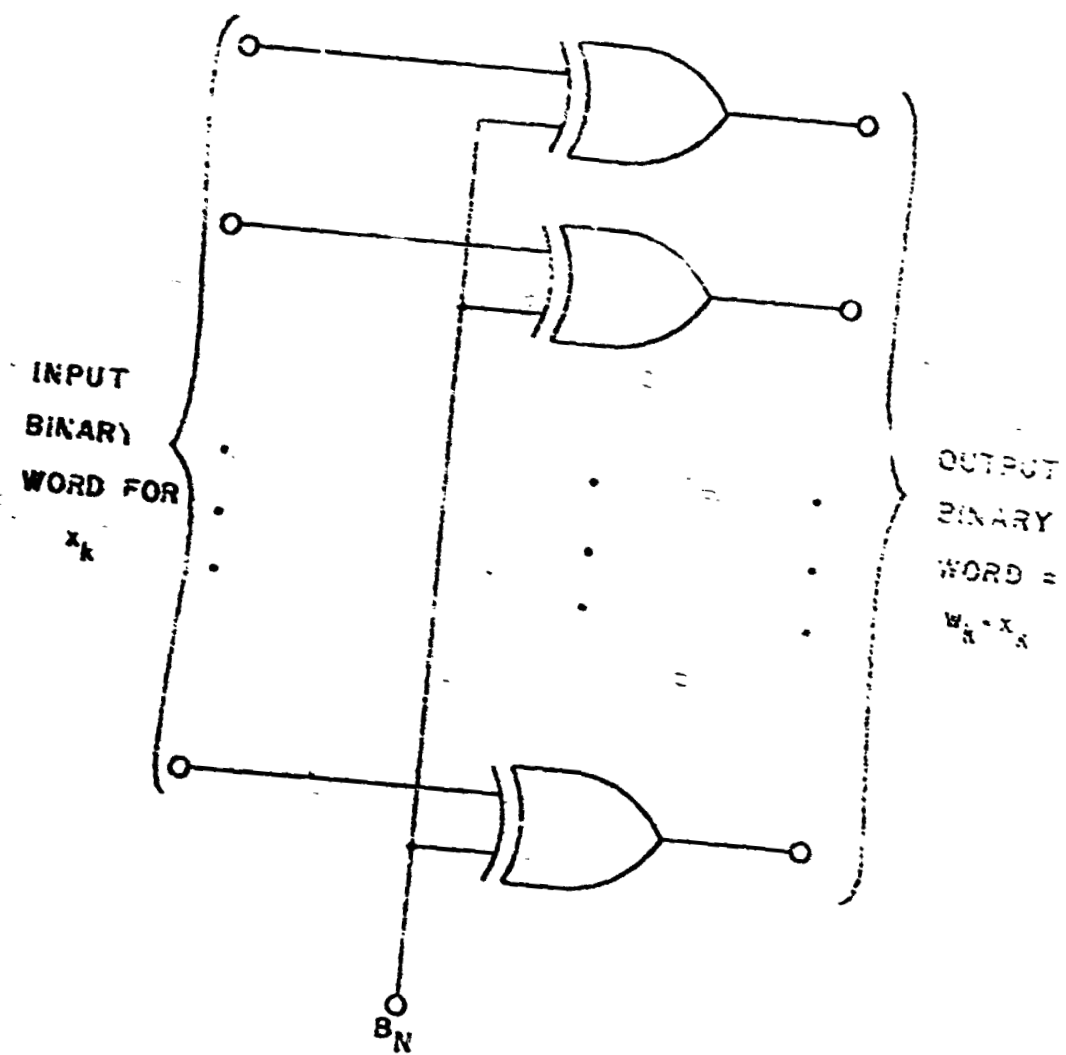
$$| \varphi_k - \hat{\varphi}_k | \leq MS \tag{2.5-2}$$

19

Fig. 2.4-2. The exclusive-or gating of the in... signal, x_k, to produce the product $w_k \cdot x_k$.

Then assuming $\varphi_k - \hat{\vartheta}_k$ is uniformly distributed over its range, the quantization noise is

$$N_q = S^2 / 12 \tag{2.5-3}$$

and the signal power is

$$E[(\varphi_k - \hat{\vartheta}_k)^2] = \frac{1}{2M+1} \sum_{n=-M}^{M} (nS)^2 = \frac{M(M+1)(2M+1)S^2}{3} \tag{2.5-4}$$

The signal-to-quantization noise ratio is then

$$S/N_q = 4M(M+1) \tag{2.5-5}$$

As a result of the approximation $\sin(\varphi_k - \hat{\vartheta}_k) \approx \varphi_k - \hat{\vartheta}_k$, the harmonic noise introduced is

$$N_d = E\left\{ [(\varphi_k - \hat{\vartheta}_k) - \sin(\varphi_k - \hat{\vartheta}_k)]^2 \right\}$$

$$= \frac{1}{2M+1} \sum_{n=-M}^{M} (nS - \sin nS)^2 \tag{2.5-6}$$

and the signal-to-harmonic noise is

$$\frac{S}{N_d} = \frac{M(M+1)(2M+1)S^2}{3 \sum\limits_{n=-M}^{M} (nS - \sin nS)^2} \tag{2.5-7}$$

Eqs. (2.5-5) and (2.5-7) are plotted in Figs. 2.5-1 and 2.5-2 as a function of the maximum phase difference, MS, for the case of an A/D converter which accepts ±5 volts maximum and uses 10 and 12 bits respectively. As expected, the signal-to-quantization noise ratio improves when the signal range increases, while the signal-to-harmonic noise ratio deteriorates for increasing signal range. The digital phase-locked loops are designed so that these two ratios are equal. From Figs. 2.5-1 and 2.5-2 the maximum allowable phase errors are:

Fig. 2.5-1. Signal-to-quantization noise and signal-to-harmonic noise as a function of the maximum phase difference for a ten-bit λ/D converter.
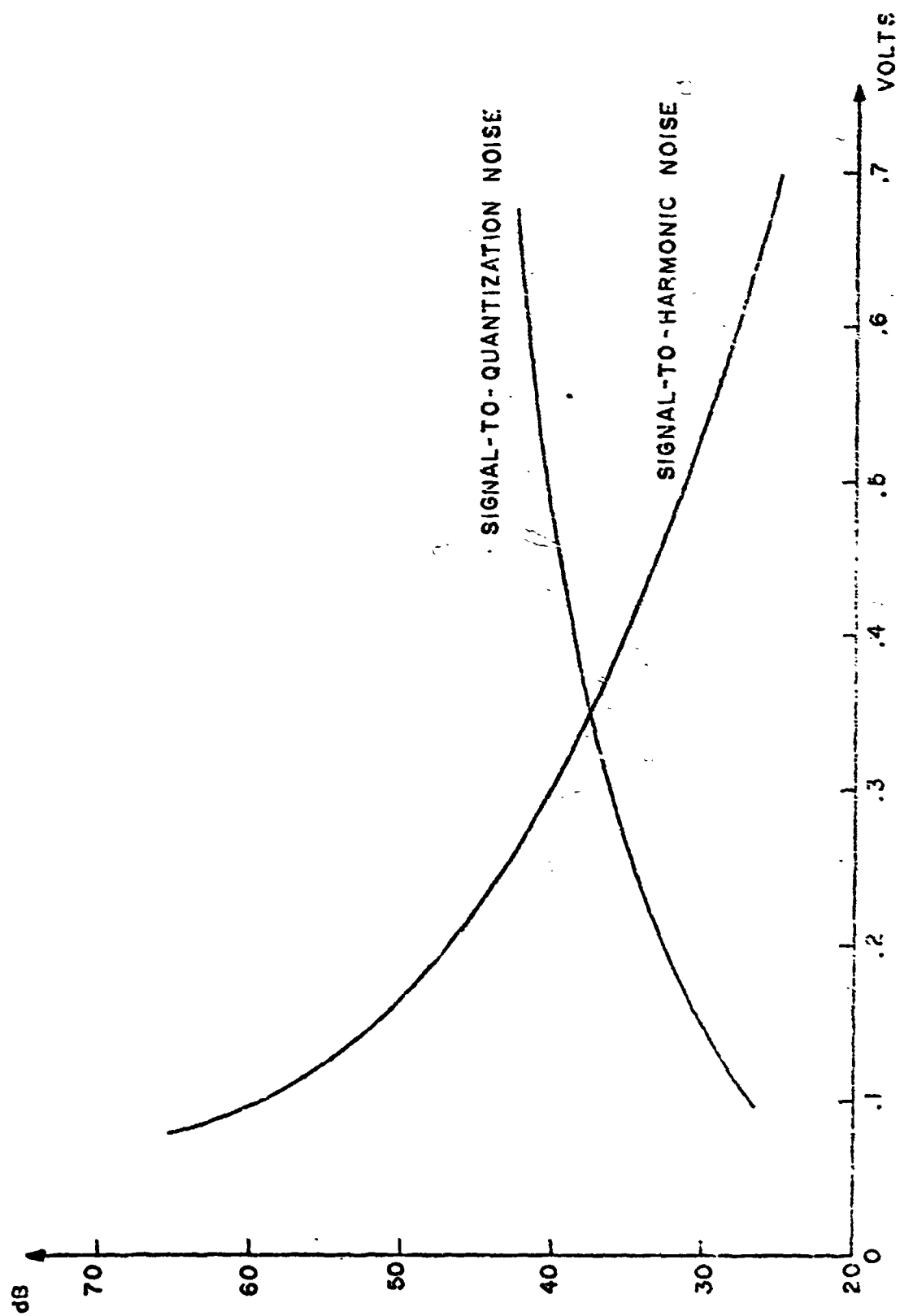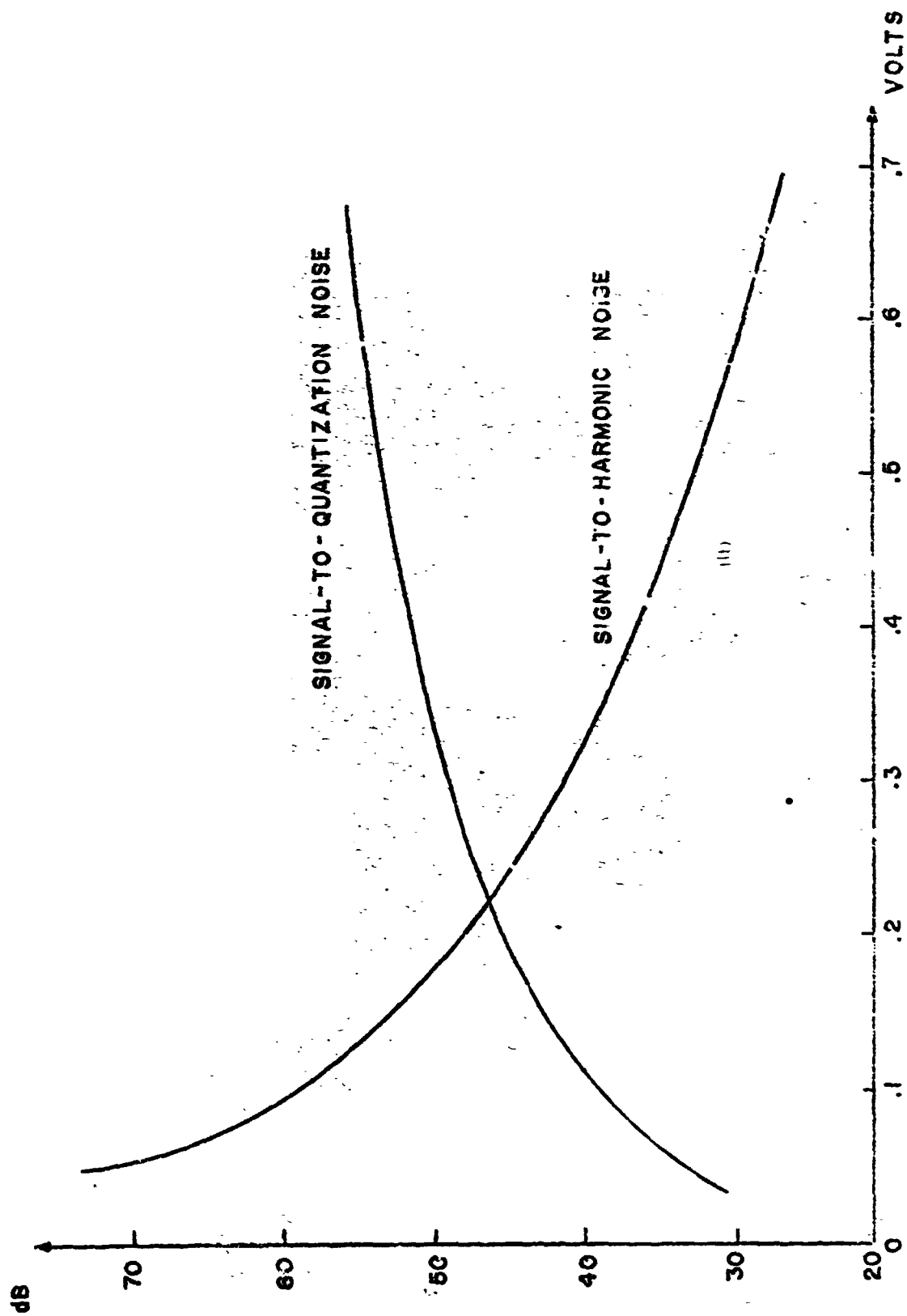
Fig. 2.5-2. Signal-to-quantization noise and signal-to-harmonic noise as a function of the maximum phase difference for a 12-bit A/D converter.

N. mber of Bits	Maximum Phase Error
10	0.35
12	0.23

Table 2.5-1

The maximum allowable phase error places a restriction on the loop gains as will be seen in the following chapter.

2.6 Design Considerations--VCO Harmonics

Although the square wave function of Eq. (2.3-8) adopted for the VCO leads to a simple computational algorithm, it has the disadvantage of introducing harmonics into the DPLL. For the function $Sq(x)$ has the Fourier series

$$Sq(x) = \frac{4}{\pi}\left[\sin x + \frac{1}{3}\sin 3x + \frac{1}{5}\sin 5x + \cdots + \frac{1}{2n+1}\sin(2n+1)x+\cdots \right] \quad (2.6-1)$$

and the product $-2\cos[2\pi f_o t + \varphi(t)]Sq[2\pi f_o t + \hat{\varphi}(t)]$ generates harmonics at $f = 0, 2f_o, 4f_o, 6f_o, \ldots, 2pf_o, \ldots$. Now in an analog phase-locked loop, these harmonics would be sufficiently attenuated by the loop filter and the VCO integration. However, in the digital phase locked loop, the sampling process shifts these frequencies, and eventually a harmonic will be folded (aliased) into the loop bandwidth. Since $f_o = (n + 1/4m)f_s$, the frequency f_o gets aliased to $f_s/4m$, and therefore the multiplier output contains harmonics at

$$0, f_s/2m, 2f_s/2m, \ldots, pf_s/2m, \ldots \text{ Hz.}$$

But the frequency f_s is equivalent to zero frequency and so the $2m^{th}$ harmonic is aliased to d.c., falling within the loop bandwidth. The products

$$\left[-2\cos(k\pi/2m + \varphi_k)\right]\frac{4}{\pi(4m-1)}\sin\left[k(4m-1)\pi/2m + (4m-1)\hat{\varphi}_k\right] \quad (2.6-)$$

and

$$\left[-2\cos\left(k\pi/2m + \varphi_k\right)\right]\frac{4}{\pi(4m+1)}\sin\left[k(4m+1)\pi/2m + (4m+1)\hat{\varphi}_k\right] \quad (2.6-2b)$$

generate this $2m^{th}$ harmonic which is

$$\frac{4}{\pi}\left\{\frac{1}{4m-1}\sin\left[(4m-1)\hat{\varphi}_k + \varphi_k\right] + \frac{1}{4m+1}\sin\left[(4m+1)\hat{\varphi}_k - \varphi_k\right]\right\} \quad (2.6-3)$$

If the loop is following the input modulation, then $\hat{\varphi}_k \approx \varphi_k$ and the amplitude of this $2m^{th}$ harmonic is approximately

$$\frac{4}{\pi}\left[\frac{1}{4m-1} + \frac{1}{4m+1}\right] = \frac{32m}{\pi(16\,m^2 - 1)} \quad .$$

The above analysis indicates that m should be made large in order that the aliased harmonic have small amplitude and not interfere with the loops tracking ability. However, the multiplier output first harmonic is at $f = f_s/2m$, and increasing m causes this harmonic to fall within the DPLL bandwidth. As the amplitude of the first harmonic is approximately $4(1 + 1/3)/\pi = 16/3\pi$, it is the first harmonic that poses the greater threat of loop malfunction than the $2m^{th}$ harmonic. If the input modulation produces a frequency deviation Δf Hz, then this first harmonic has a frequency deviation of approximately (assuming $\hat{\varphi}_k \approx \varphi_k$) $2\Delta f$ Hz. Requiring that this first harmonic fall outside the loop bandwidth, B_L, we have

$$(f_s/2m) - 2\Delta f \geq B_L \quad (2.6-4)$$

Eq. (2.6-4) and Table 2.5-1 form the basis of design of the first order phase-locked loop, Chapter 3. Consideration of the DPLL's response to input spikes then allows design of the second and third order DPLL's, in Chapters 4 and 5.

2.7 Linearized Model of the DPLL

While the use of a square wave VCO simplifies the DPLL implementation, it introduces a severe nonlinearity into the DPLL difference equation, making it impossible to solve exactly except in a limited number of

special cases (the first order DPLL equation is solved in Ch. 3 when the input carrier is unmodulated). We therefore introduce a linearized model, developed on the basis of the design conditions of Sections 2.5 and 2.6.

The product of input carrier and square wave VCO generates harmonics at 0, $f_s/2m$, $2f_s/2m$, ..., $pf_s/2m$, ... Hz, with p an integer. Of these harmonics, only the d.c. term contains information about the phase error between input and VCO, and ideally, this shou!' be the only term present. Eq. (2.6-4) stipulated that the additional harmonics fall outside the DPLL bandwidth. As previously observed, the sampling process folds the $2m^{th}$ harmonic to d.c.; also, this $2m^{th}$ harmonic has an amplitude of approximately $8m/(16m^2-1)$ (relative to the d.c. term). Hence, to obtain a linearized model we may neglect all the harmonics except the first, so that

$$e_k \approx \frac{4}{\pi} \sin(\varphi_k - \hat{\varphi}_k) \qquad (2.7\text{-}1)$$

Furthermore, the phase difference $(\varphi_k - \hat{\varphi}_k)$ is restricted according to Table 2.6-1, and we therefore can further approximate:

$$e_k \approx \frac{4}{\pi} (\varphi_k - \hat{\varphi}_k) \qquad (2.7\text{-}2)$$

Using Eq. (2.7-2), the linearized model of the DPLL appears in Fig. 2.7-1. Note that the input to the linearized model is the input phase, φ_k.

The suppressing of the harmonics is supported by the square wave nature of the VCO: if the VCO argument lies anywhere in the $[0, \pi)$ interval, the VCO output is a $+1$. Therefore, although the true VCO phase is perturbed from that in the linearized model, the VCO output sequence may still be identical.

2.8 Hardware Considerations

The digital phase-locked loops designed were constructed using commercially available DTL and TTL logic cards. As previously mentioned, all computations are performed within one sampling period, which is chosen to be 20 μsec to accomodate the logic speed. All computations are performed in parallel form.
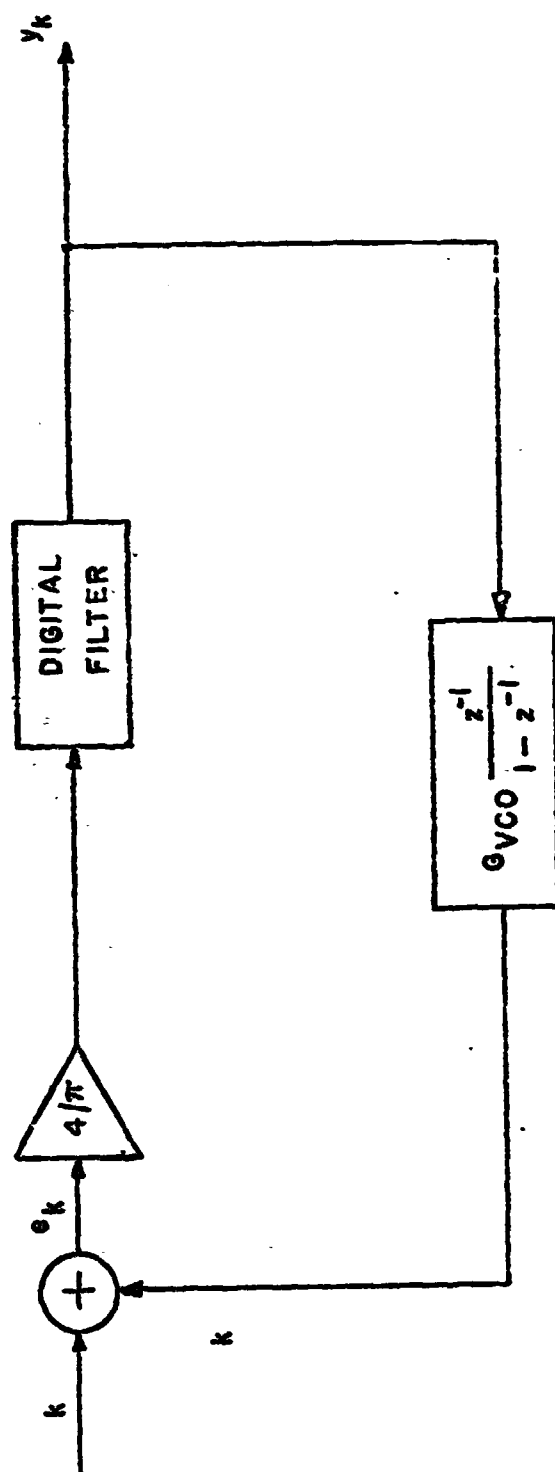
Fig. 2.7-1. The linearized model of the all digital phase-locked loop.

The A/D converter employed generates words in offset binary form: the most significant bit is the sign bit which is a 1 for positive voltages; negative voltages are represented by the complement of the corresponding positive voltage word. There are two representations of zero volts: $+0 = 100...0$; $-0 = 011...1$. Table 2.8-1 illustrates the offset binary words obtained when the input voltage is between -7 and $+7$ volts; for simplicity only 4 bits are used. The A/D converter used in the DPLL converts voltages between -5 and $+5$ volts into 10-bit offset binary words.

2.8.1 Multiplication by $1/2^N$

To avoid a binary multiplication (which is excessive in computation time) all gains appearing in the DPLL are chosen to be powers of $1/2$. As a result, the multiplication operation becomes a shifting operation, shifting the binary word once for each factor of $1/2$. However, care must be taken in performing this shifting operation: The sign bit must NOT be shifted, and the bits which become vacant must be filled with the complement of the sign bit. For example,

$$\frac{1}{4}(+4) = \frac{1}{4}(1100) = 1001.00$$

and

$$\frac{1}{4}(-4) = \frac{1}{4}(0011) = 0110.11$$

(If the answer is allotted only four bits, then the two bits to the right of the binary point are dropped. We shall see later that in the DPLL's designed here these bits are not dropped from the answer.)

2.8.2 Addition Algorithm

In order to correctly add two offset binary words, an algorithm is required. Let the two N-bit words to be added be denoted by $A = a_1 a_2 ... a_N$ and $B = b_1 b_2 ... b_N$, with a_1 and b_1 the sign bit. The algorithm consists of the following steps:

28

Voltage Levels (volts)	Offset Binary Word
+ 7	1111
6	1110
5	1101
4	1100
3	1011
2	1010
1	1001
0	{ 1000 / 0111
- 1	0110
- 2	0101
- 3	0100
- 4	0011
- 5	0010
- 6	0001
- 7	0000

Table 2.8-1. Illustrating offset binary coding.

1. Form the ordinary binary sum $A + B = c_0 c_1 c_2 \cdots c_N$, where c_0 = the sign bit carry.

2. Use the carry <u>into</u> the sign bit as an end-around carry, resulting in the new sum $d_0 d_1 d_2 \cdots d_N$.

3. The answer in offset binary is obtained by deleting the digit d_1:

$$A + B = d_0 d_2 d_3 \cdots d_N.$$

Several examples will elucidate the algorithm:

Example 2.8-1

$$+3 = 1011$$
$$+2 = 1010$$

Step 1.

$$0 \swarrow \text{carry into sign bit}$$
$$1011$$
$$\underline{1010}$$
$$10101$$

Step 2.

$$10101$$
$$\underline{0}$$
$$10101$$

Step 3. Answer = $1101 = +5$

Example 2.8-2

$$+3 = 1011$$
$$-2 = 0101$$

Step 1.

$$1 \swarrow \text{carry into sign bit}$$
$$1011$$
$$\underline{0101}$$
$$10000$$

Step 2.

$$10000$$
$$\underline{1}$$
$$10001$$

Step 3. Answer = $1001 = +1$

2.8.3 Arithmetic Saturation

If two numbers whose sum exceeds the voltage range are added using the above algorithm, an erroneous result occurs, referred to as <u>overflow</u>. For example, $+4 + 6 = 1100 + 1110 = 1011$ (using the algorithm) but $1011 = +3$.

30

In linear digital filters it is possible for overflow to generate limit cycles, which can be eliminated by having the addition process saturate[16]. The DPLL is a nonlinear digital filter, and to prevent the possibility of limit cycles, the arithmetic is modified to include positive and negative saturation when the sum exceeds the allowable limit.

First, we must detect when overflow occurs, and whether it is positive or negative. Note that overflow can never occur when adding numbers of opposite sign. When two positive numbers are added, the sign bit carry is 1; if in addition, overflow occurs, the carry into the sign bit is also a 1. Hence positive overflow occurs when both of these carries are 1. Adding two negative numbers always produces a 0 sign bit carry, and overflow produces a 0 carry into the sign bit; hence negative overflow occurs when both these carries are 0. These two conditions are easily detected using nand gates, as shown in Fig. 2.8-1.

Having determined an overflow situation, we may generate the most positive or most negative number, whichever is required. The adder plus saturation processing is shown in Fig. 2.8-2, where the adder is followed by a storage register and a bank of nand gates. The inverted output of the storage register is used; hence $R =$ the complement of whatever is stored. The negative overflow signal is inverted and used to reset the register; the positive overflow signal gates every bit through a nand gate.

When no overflow occurs, $N = P = 1$, and the register is not reset. The register stores C and its output is $\overline{C}$; each bit is complemented by the nand gates producing $Y = \overline{\overline{C}} = C$.

When positive overflow occurs, $P = 0$ ($N = 1$) and the nand gate output is $Y = 1111$, the maximum positive voltage, regardless of the register output.

When negative overflow occurs, $N = 0$, $P = 1$ and the register is reset to zero, producing $R = 1111$. The nand gates invert this producing $Y = 0000$, the most negative voltage.

SIGN BIT CARRY

CARRY INTO SIGN BIT

P (POSITIVE OVERFLOW)

N (NEGATIVE OVERFLOW)
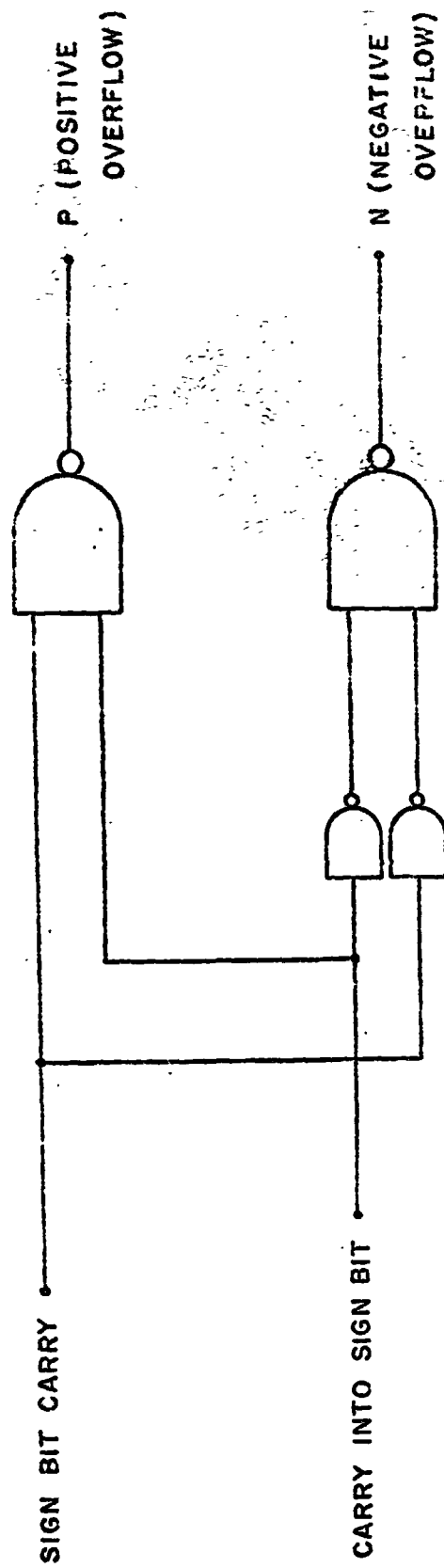
POSITIVE OVERFLOW OCCURS IFF P = 0

NEGATIVE OVERFLOW OCCURS IFF N = 0

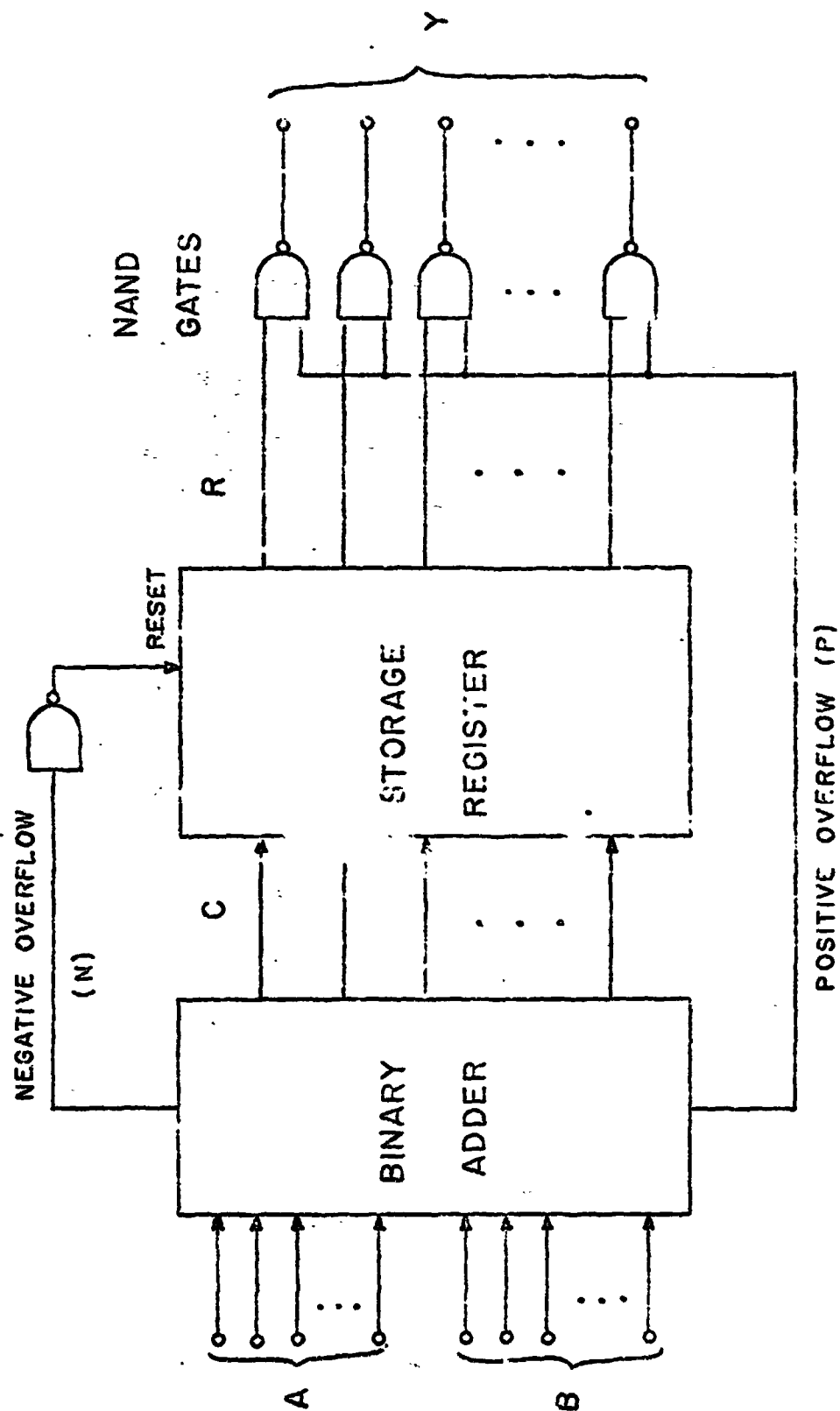Fig. 2.8-1. The required logic for detecting positive and negative overflow.

Fig. 2.8-2. The binary addition hardware including the saturation processing.

2.8.4 VCO Overflow

The VCO algorithm was developed in Sec. 2.4 where it was concluded that the VCO integrator must be allowed to overflow in order to realize the periodicity of the square wave function, Sq(·). This means that if, for example, we are working with ±7 volts maximum, the addition must be performed on a modulo 8 basis.

Let us examine the addition algorithm of Sec 2.8.2 by adding +5 and +4. The result should be

$$+5 +4 = +1 \bmod 8 \tag{2.8-1}$$

The addition algorithm, without saturation of course, yields

```
·        1 ──────┐
+5  =  1 1 0 1   │
+4  =  1 1 0 0·  │
       ───────   │
       1 1 0 0 1  │
       ─────── ╷ ─┘
           ──  ┴
       1 1 0 1 0
```

$$+5 +4 = 1 1 0 1 0 = +2$$

Note that the answer is too large. In fact, the addition algorithm will always generate a larger result because the overflow (the carry into the sign bit) is the end around carry. Hence to achieve the correct overflow sum, we must prevent the end around carry operation.

Next, consider the sum −5 −4, whose sum is

$$-5 -4 = -1 \bmod 8$$

The addition algorithm yields

```
         0 ──────┐
-5  =  0 0 1 0   │
-4  =  0 0 1 1   │
       ───────   │
       0 0 1 0 1  │
           ─── 0 ◄┘
       ───────
       0 0 1 0 1
```

$$-5 -4 = 0 1 0 1 = -2$$

Here, the difficulty is that the end around carry is a zero, when it should be

33

a one. This will always be the case for negative overflow because the
operation $-A-B$ is really the sum $(1111-A)+(1111-B)$
$=11110-A-B$, and for negative overflow the end around carry is zero,
so that our result is different from the correct result, $11111-A-B$.

Therefore, to obtain a correct result for the VCO integration (addition),
it is necessary to make two modifications in the existing addition process.
First, the saturation hardware must be eliminated. Second, the end around
carry must be complemented whenever overflow is detected. The end around
carry modification may be simplified by noting that under normal loop opera-
tion the VCO integrator will never overflow negatively, since the positive
number $\pi/2m$ is added at each computation. Hence, the end around carry
may be set to zero for all VCO computations.

CHAPTER 3

THE F.. ST ORDER DIGITAL PHASE-LOCKED LOOP

3.1 The First Order DPLL Equation

The first order digital phase-locked loop is shown in Fig. 3.1-1. Referring to this figure, let the sampled FM signal plus noise be denoted by x_k:

$$x_k = -2\cos(2\pi f_0 k T_s + \omega_k) + n_k \qquad (3.1-1)$$

where

f_0 = carrier frequency

T_s = sampling period

ω_k = input phase

n_k = IF noise

The reason for choosing the signal amplitude of 2 volts is seen below. Incorporating Eq. (2.2-5), we have

$$x_k = -2\cos(k\pi/2m + \omega_k) + n_k \qquad (3.1-2)$$

The error signal e_k is the product of the input and VCO output, w_k:

$$e_k = x_k \cdot w_k \qquad (3.1-3)$$

The DPLL output, y_k, is simply proportional to the error for a first order loop:

$$y_k = g \cdot e_k \qquad (3.1-4)$$

where g = forward loop gain. The VCO phase $\hat{\omega}_k$ is then

$$\hat{\omega}_k = \hat{\omega}_{k-1} + G_{VCO} y_{k-1} \qquad (3.1-5)$$

where G_{VCO} = VCO gain, which includes both any explicit scaling of the loop output, as well as the implicit gain introduced by the Sq($\cdot$) algorithm, as explained in Ch. 2. Finally, the VCO output is

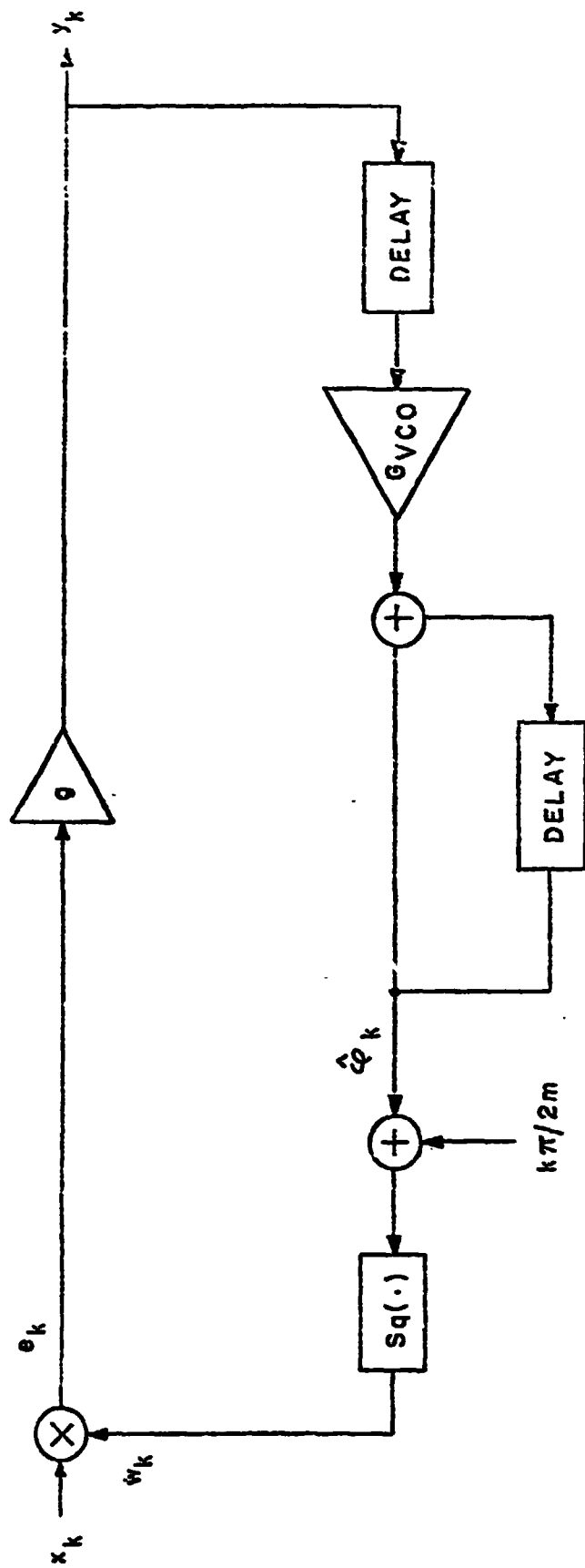$$w_k = Sq(k\pi/2m + \hat{\omega}_k) \qquad (3.1-6)$$

Fig. 3.1-1. Block diagram of the first order digital phase-locked loop.

Combining Eqs. (3.1-2) through (3.1-6), we obtain the equation for the VCO phase $\hat{\varphi}_k$:

$$\hat{\varphi}_{k+1} = \hat{\varphi}_k - 2G \cos(k\pi/2m + \hat{\varphi}_k) Sq(k\pi/2m + \hat{\varphi}_k)$$
$$+ G n_k Sq(k\pi/2m + \hat{\varphi}_k) \qquad (3.1-7)$$

where $G = G_{VCO} \cdot g =$ loop gain. To bring this equation into a clearer form, expand the $Sq(\cdot)$ function using a Fourier series

$$Sq(x) = \frac{4}{\pi} \sum_{p=0}^{\infty} \frac{1}{2p+1} \sin(2p+1)x \qquad (3.1-8)$$

and expand the product of the fundamental component and the input FM signal. Then

$$-2G \cos(k\pi/2m + \varphi_k) Sq(k\pi/2m + \hat{\varphi}_k) = \frac{4}{\pi} G \sin(\varphi_k - \hat{\varphi}_k)$$
$$+ \frac{4}{\pi} G \sin(k\pi/2m + \varphi_k + \hat{\varphi}_k)$$

$$-2G \cos(k\pi/2m + \varphi_k) \frac{4}{\pi} \sum_{p=1}^{\infty} \frac{1}{2p+1} \sin(2p+1)(k\pi/2m + \hat{\varphi}_k)$$

$$= \frac{4}{\pi} G \sin(\varphi_k - \hat{\varphi}_k) + \frac{4}{\pi} G h_k(\varphi_k, \hat{\varphi}_k) \qquad (3.1-9)$$

The first term is a measure of the discrepancy between the input and VCO phases while h_k is the contribution from the harmonics generated by the square wave VCO. The DPLL equation is thus

$$\hat{\varphi}_{k+1} - \hat{\varphi}_k + \frac{4}{\pi} G \sin(\hat{\varphi}_k - \varphi_k) = G n_k Sq(k\pi/2m + \hat{\varphi}_k)$$
$$+ \frac{4}{\pi} G h_k(\varphi_k, \hat{\varphi}_k) \qquad (3.1-10)$$

The left side of this equation is the digitized version of a first order analog loop, where the derivative is replaced by a difference:

$$\frac{d\hat{\varphi}(t)}{dt} + G_{analog} \sin[\hat{\varphi}(t) - \varphi(t)]$$
$$\approx (\hat{\varphi}_{k+1} - \hat{\varphi}_k)/T_s + G_{analog} \sin(\hat{\varphi}_k - \varphi_k) \qquad (3.1-11)$$

37

Note that the corresponding analog loop gain is

$$G_{analog} = \frac{4}{\pi} f_s G \qquad (3.1-12)$$

The factor $4/\pi$ represents the Fourier coefficient of the square wave fundamental while the factor f_s enters because computations in the digital loop are performed every sampling period, T_s.

The first order DPLL equation, Eq. (3.1-10), is a first order, non-linear difference equation, whose solution is obtained under special input conditions in Secs. 3.3 and 3.4.

3.2 Stability Condition or the Loop Gain

A first order analog loop possesses stable VCO states (phases) for any positive loop gain when the input carrier is unmodulated ($\omega_k \equiv 0$) and no noise is present ($n_k \equiv 0$). For any initial VCO phase, the VCO phase eventually settles to zero (modulo 2π); the larger the loop gain, the smaller the transient time required. The digital loop has different restrictions.

First, consider the case where the added harmonics h_k are not included, yielding the equation

$$\hat{\phi}_{k+1} = \hat{\phi}_k - \frac{4}{\pi} G \sin \hat{\phi}_k \qquad (3.2-1)$$

In order that $\hat{\phi}_k \longrightarrow 0$ for any initial value $\hat{\phi}_o$, we must have $(4/\pi)G < 2$, as demonstrated in App. 1. Larger loop gains require smaller transient times (where transient time is defined, for example, as the time required for the VCO phase to be within 0.1 radian).

Now if the harmonics are included, the gain restriction changes, as it is no longer possible to have $\hat{\phi}_k \longrightarrow 0$ in the steady state. For example, assume that $\hat{\phi}_k \equiv 0$; then

$$\hat{\phi}_{k+1} - \hat{\phi}_k = G e_k = -2G (\cos k\pi/2m)(Sq\, k\pi/2m) \qquad (3.2-2)$$

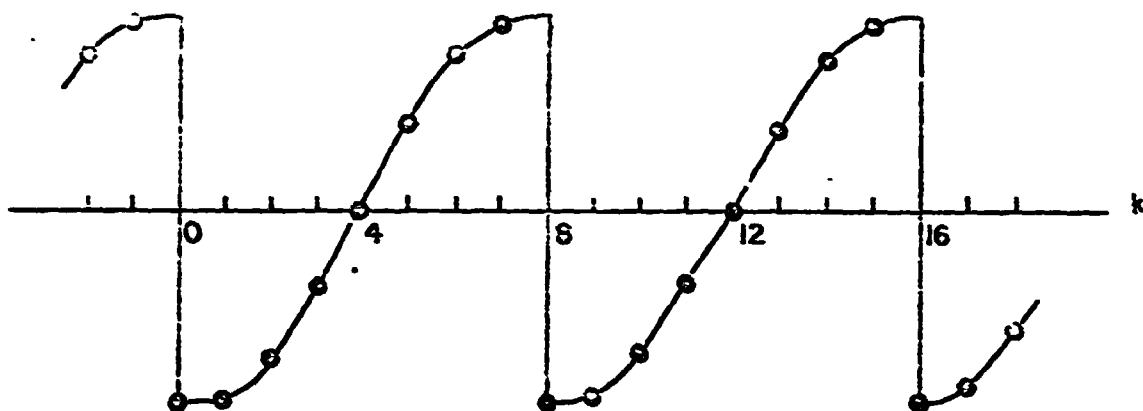which is shown in Fig. 3.2-1 for the case $m = 4$, and when this integrated

Fig. 3.2-1. The assumed DPLL error signal e_k when both input and VCO phase are identically zero.
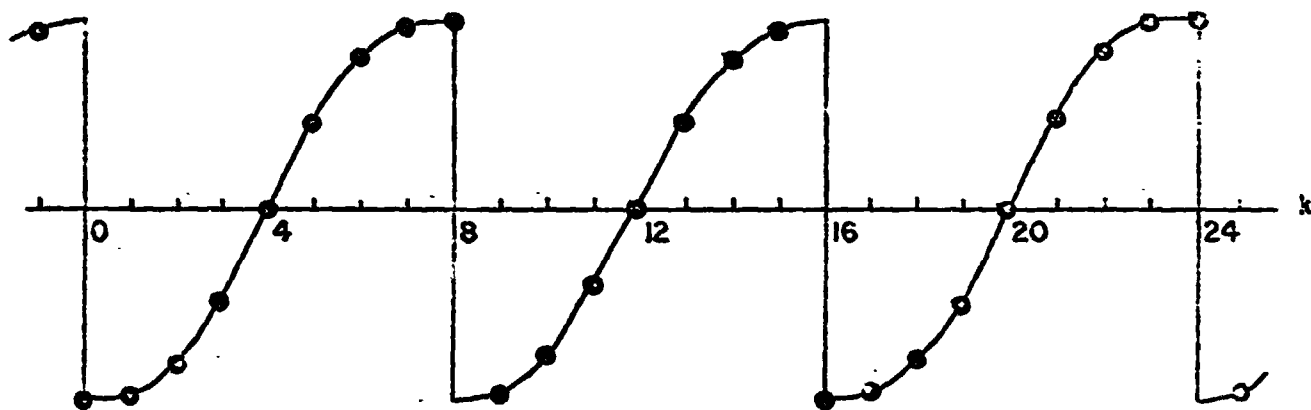

Fig. 3.2-2. The steady state error signal generated when the input carrier is unmodulated.

to form $\hat{\phi}_k$, the result is not identically zero, as originally assumed. Therefore, more care must be taken in calculating the VCO phase.

Assume that at $k = 0$, the VCO phase is zero: $\hat{\phi}_0 = 0$. Then

$$e_0 = -2 \cos 0 \cdot \pi/2m \; Sq(0 \cdot \pi/2m + 0) = -2 \cdot 1 = -2$$

and

$$\phi_1 = \phi_0 + Ge_0 = 0 - 2G$$

Now the VCO output w_1 should be $+1$:

$$w_1 = Sq(1 \cdot \pi/2m + \hat{\phi}_1) = Sq(\pi/2m - 2G) = +1$$

Therefore

$$\pi/2m - 2G \geq 0$$

and

$$G \leq \pi/4m \qquad\qquad (3.2\text{-}3)$$

We shall see that this (in addition to the obvious requirement $G > 0$) is precisely the gain restriction for stability. Then

$$e_1 = (-2 \cos \cdot/2m) \cdot (+1)$$

and

$$\hat{\phi}_2 = 0 - 2G - 2G \cos \pi/2m$$

implying

$$w_2 = Sq(2\pi/2m - 2G - 2G \cos \pi/2m) = +1$$

since

$$2\pi/2m > 2\pi/2m - 2G - 2G \cos \pi/2m = (\pi/2m - 2G) + (\pi/2m - 2G \cos \pi/2m) > 0$$

In fact, it follows that for $0 \leq k \leq 2m$, the VCO output is $+1$, since

$$\hat{\phi}_k = \hat{\phi}_0 + G \sum_{p=0}^{k-1} -2 \cos p\pi/2m$$

and

$$0 \leq k\pi/2m + \hat{\phi}_k < \pi \qquad \text{for } 0 \leq k \leq 2m$$

40

At $k = 2m + 1$, the VCO phase is

$$\hat{\varphi}_{2m+1} = \hat{\varphi}_o + G \sum_{p=0}^{2m} -2G \cos p\pi/2m = 0 + 0 = 0$$

and hence the VCO output is -1:

$$w_{2m+1} = Sq((2m+1)\pi/2m + 0) = -1$$

Similarly, the VCO output remains at -1 for $2m+1 \leq k \leq 4m-1$. Finally, at $k = 4m$, the VCO phase is

$$\hat{\varphi}_{4m} = \hat{\varphi}_o + G \sum_{p=0}^{2m} -2\cos p\pi/2m + G \sum_{p=2m+1}^{4m-1} (-1)(-2\cos p\pi/2m) = 0$$

and the sequence repeats. The resulting steady state output is shown in Fig.3.2-2 for the case $m = 4$; it is an eight-point sequence followed by a seven-point sequence, etc. Note that this signal has a zero average value, while the sequence of Fig 3.2-1 does not.

The gain restriction, Eq. (3.1-4) has another interpretation: it prevents the VCO output from executing two consecutive sign changes; i.e., it prevents VCO jitter. To illustrate this, note that the VCO argument always increases:

$$\Delta(k\pi/2m + \varphi_k) = \pi/2m + \Delta \varphi_k = \pi/2m + G e_k > \pi/2m - 2G \geq 0$$

Therefore, if the VCO argument crosses from a -1 to a $+1$ interval, it must remain in the $+1$ interval at least for the next sample. In fact, the most the argument can increase is $\pi/2m + \pi/2m = \pi/m$, and hence the VCO output remains $+1$ for at least m samples.
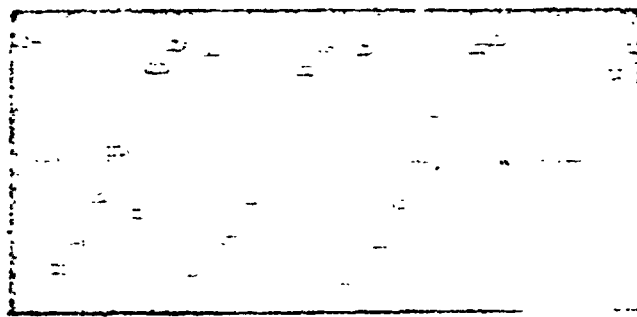
Fig. 3.2-3 shows photographs of the D/A output the first order DPLL for different loop gains. The DPLL has unit forward loop gain ($g = 1$) and an explicit VCO gain of $1/16$; the implicit VCO gain was varied, producing different loop gains. The A/D converter codes a ± 5
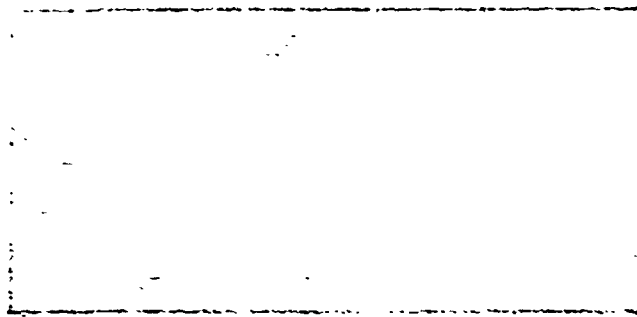
(a) $G = \pi/20$
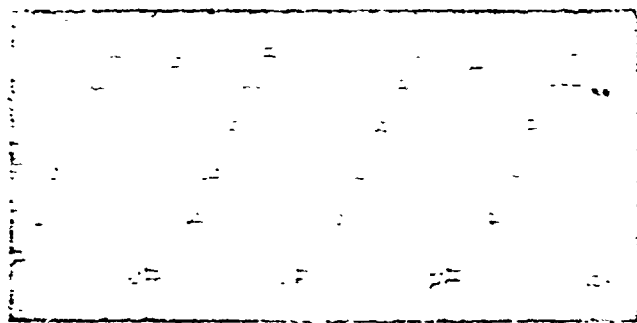
(b) $G = \pi/10$

(c) $G = \pi/5$

Fig. 3.2-3. D/A outputs of a first order DPLL having loop gain G and an unmodulated input carrier.

42

volt input signal into 10-bit binary words; the sampling frequency is 50 KHz and m = 4.

Fig. 3.2-3a shows the error signal when the VCO output is chosen using the third most significant bit of the VCO argument. Since this bit carries the value $5/4 = 1.25$ volts, the implicit VCO gain is $\pi/1.25$ and the loop gain is

$$G = (1/16)(\pi/1.25) = \pi/20$$

Note that this gain is less than the critical gain, $\pi/4m = \pi/16$, and so the DPLL should generate the sequence of Fig 3.2-2. Indeed, examining Fig 3.2-3a we see exactly the anticipated sequence: nine levels, followed by seven levels, followed by nine levels, etc. The spikes seen on the left side of some of the levels is a flaw in the D/A converter, not in the DPLL.

Next, in Fig 3.2-3b, the VCO output is chosen using the fourth most significant bit, yielding an implicit gain of $\pi/0.625$ and a loop gain

$$G = \pi/10$$

which is greater than the critical gain and therefore should result in an unstable DPLL. Fig. 3.2-3b bears this out: after two negative levels, the VCO output changes sign, producing a positive level, and changes sign once again, generating a negative level. This is precisely the consecutive VCO sign changes referred to above. Such a DPLL does not generate the desired steady state sequence and is classified as unstable.

Finally, the loop gain is again doubled by using the fifth most significant bit for the VCO output; $G = \pi/5$. Fig 3.2-3c shows that now there are two occasions where the VCO output changes twice consecutively; the third and eighth levels are inverted and the VCO corrects itself on the fourth and ninth levels.

One final point concerning the steady state. Originally it was assumed that the initial VCO phase, $\hat{\phi}_o$, was zero, which led to the steady state error sequence. But $\hat{\phi}_o$ does not necessarily have to be zero to generate this sequence. In order that the initial VCO output be $+1$, we require

$$0 \leq \varphi_0 \leq \pi$$

To assure that the VCO generates 2 m successive +1 outputs, we examine its argument at $k = 2m$; if this argument is less than π, then all VCO outputs for $0 \leq k \leq 2m$ are indeed +1, since the VCO argument always increases. Hence we require

$$2m\pi/2m \div \hat{\varphi}_{2m} < \pi$$

But

$$\hat{\varphi}_{2m} = \hat{\varphi}_0 + G \sum_{p=0}^{2m-1} -2\cos p\pi/2m = \hat{\varphi}_0 - 2G$$

and therefore

$$\hat{\varphi}_0 < 2G$$

Therefore, if

$$0 \leq \hat{\varphi}_0 \leq 2G \qquad\qquad (3.2-4)$$

we are in the steady state.

3.3 Transient Response to an Unmodulated Carrie:

An analog phase-locked loop having positive loop gain will drive any initial VCO phase to zero (modulo 2π) in response to an unmodulated carrier input. Initial VCO phases of $\pm\pi$ (modulo 2π) place the loop at an unstable equilibrium point and theoretically the loop should remain there indefinitely. However, in practice, it is impossible to remain preciesly at this point and once perturbed from it, however slightly, the loop migrates to a stable equilibrium point. Theoretically it requires infinite time for the VCO phase to reach zero; in practice, of course, this transient time is finite.

The VCO phase of the digital phase-locked loop described by Eq. (3.2-1) (i.e., where the error signal harmonics are suppressed) is also driven to zero for any initial VCO phase, provided the gain restriction $0 < 4G/\pi < 2$ is met. Theoretically, infinite time is required for the VCO phase to reach zero, except for certain isolated initial VCO phases, for which a finite time

is required. This is pursued further in App. 1.

When the square wave VCO harmonics are included yielding Eq. (3.1-7) the DPLL reaches the steady state output sequence for any initial VCO phase (including π modulo 2π). Furthermore, the transient time is always finite, depending on the loop gain and the initial VCO phase.

We have previously seen that if $0 \leq \hat{\phi}_o < 2G$ there is no transient-- the steady state sequence begins immediately. If $\hat{\phi}_o > 2G$ the VCO output changes sign before $k = 2m+1$, which reduces the VCO phase in an effort to reach the steady state. More precisely, if

$$2G \leq \phi_o < 2G + 2G \cos \pi/2m + \pi/2m \qquad (3.3\text{-}1)$$

then the VCO output w_k is

$$w_k = \begin{cases} +1, & 0 \leq k \leq 2m+1 \\ -1, & k = 2m \end{cases} \qquad (3.3\text{-}2)$$

This result is proved in App. 2. The VCO phase at $k = 2m$ is

$$\hat{\phi}_{2m} = \hat{\phi}_o + G \sum_{p=0}^{2m-1} w_p \cdot (-2 \cos p\pi/2m)$$

$$= \hat{\phi}_o + G \sum_{p=0}^{2m-1} (+1)(-2 \cos p\pi/2m)$$

$$= \hat{\phi}_o - 2G \qquad (3.3\text{-}3)$$

That is, the VCO phase is reduced by $2G$. Therefore, if in addition to Eq. (3.3-1) we have $\hat{\phi}_o < 4G$, then $\hat{\phi}_{2m} < 2G$, and steady state is reached after $2m$ iterations. If $4G \leq \hat{\phi}_o < 6G$, then $2G \leq \hat{\phi}_{2m} < 4G$ and $0 \leq \hat{\phi}_{4m} < 2G$, and steady state is reached after $4m$ iterations. Continuing in this manner, the region in the $\hat{\phi}_o - G$ plane specified by 3.3-1) is partitioned into smaller regions; each region has a finite transient time associated with it. Fig. 3.3-1 illustrates these regions for $m = 4$.

If

$$2G + 2G \cos \pi/2m + \pi/2m \leq \hat{\phi}_o < 2G + 2G \cos \pi/2m + 2G \cos 2\pi/2m + 2\pi/2m \qquad (3.3\text{-}4)$$
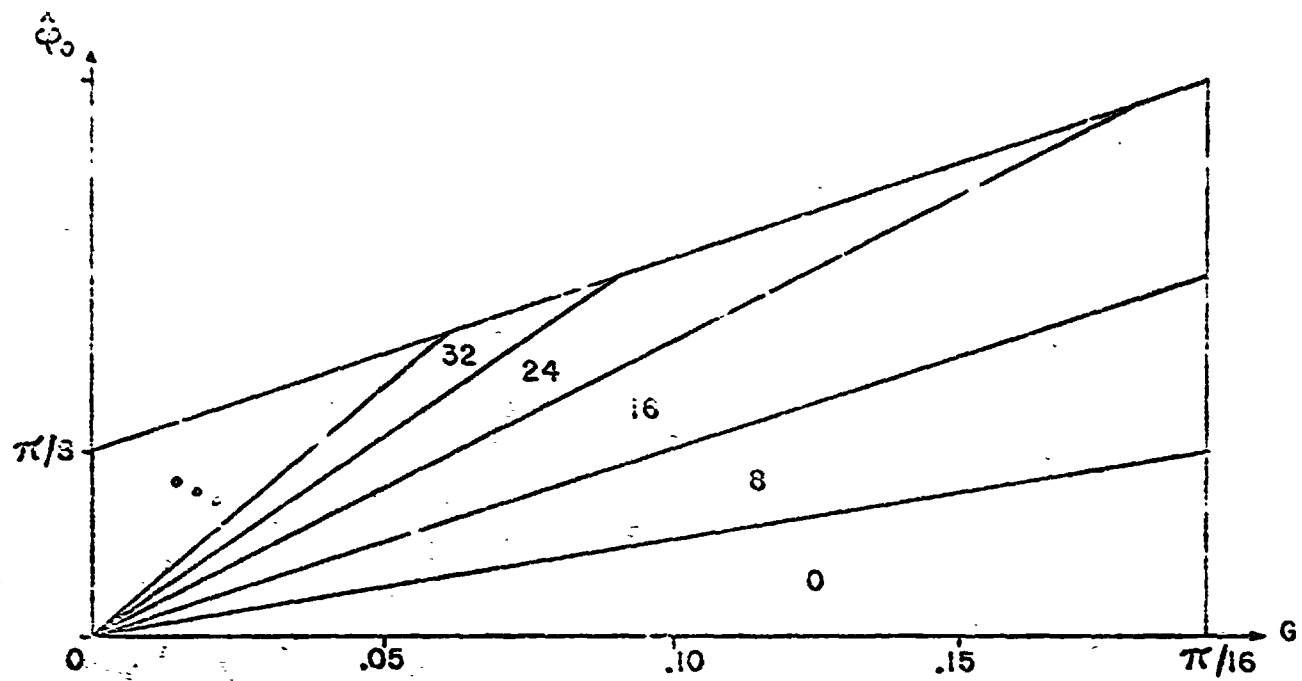
45

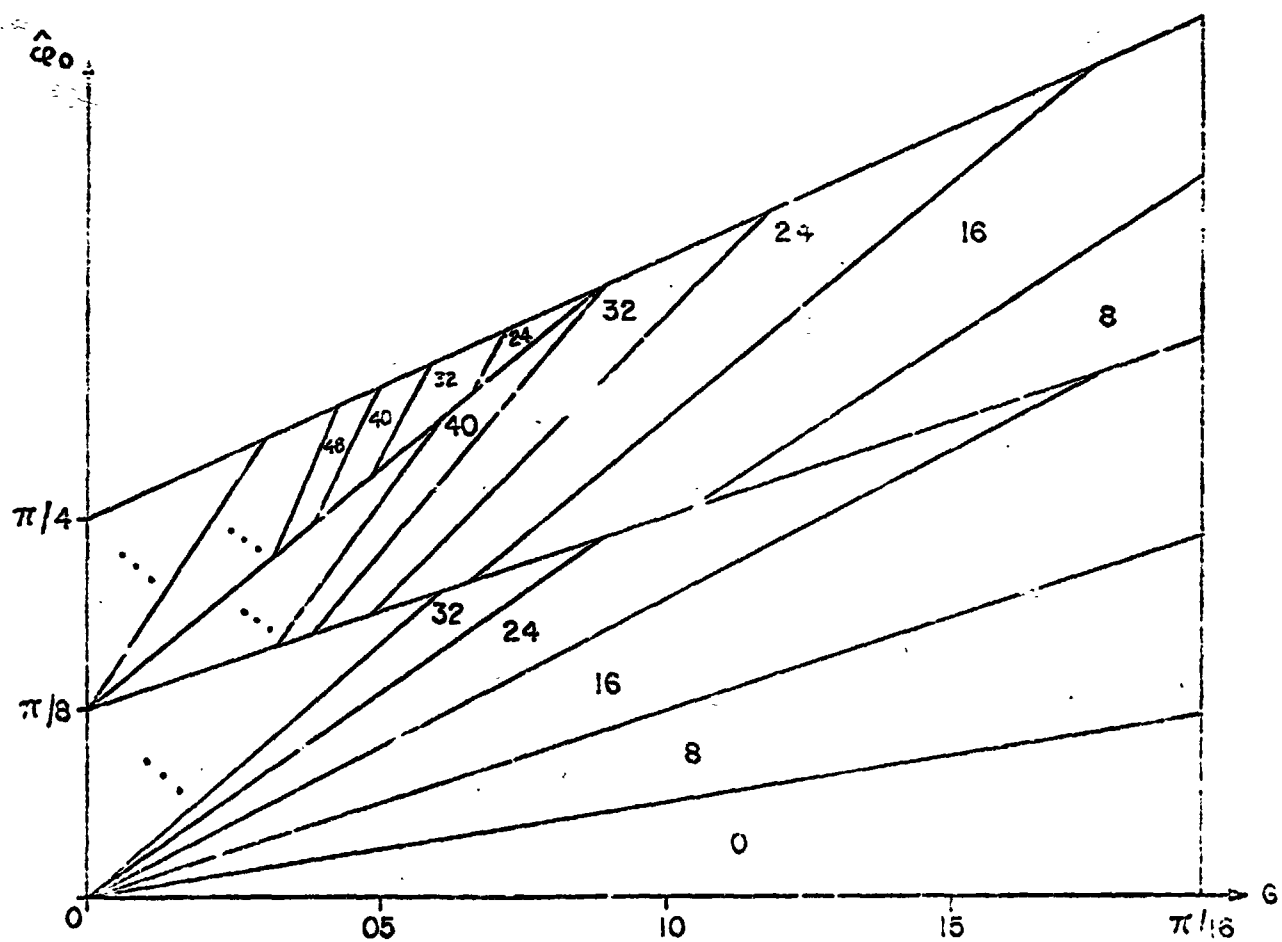Fig. 3.3-1. The partitioning of the region of Eq. (3.3-1).

Fig. 3.3-2. The regions of Fig. 3.3-1 plus the shifted regions, with their associated transient times.

46

then

$$w_k = \begin{cases} +1, & 0 \leq k \leq 2m - 2 \\ -1, & 2m - 1 \leq k \leq 2m \end{cases} \qquad (3.3-5)$$

(App. 2); i.e., the VCO output changes sign at $k = 2m - 1$. The VCO phase at $k = 2m$ is

$$\hat{\varphi}_{2m} = \hat{\varphi}_o + G \sum_{p=0}^{2m-2} (+1)(-2\cos p\pi/2m) + G(-1)(-2\cos(2m-1)\pi/2m)$$

$$= \hat{\varphi}_o - 2G - 4G\cos\pi/2m \qquad (3.3-6)$$

Note than Eqs. (3.3-4) and (3.3-6) imply that

$$-2G\cos\pi/2m + \pi/2m \leq \hat{\varphi}_{2m}$$

and since $2G < \pi/2m$ (the stability condition).

$$0 < \hat{\varphi}_{2m}$$

so that we must fall into a region already considered. In fact, we can partition the region of Eq. (3.3-4) by shifting the previously established regions upward by the amount $2G + 4G\cos\pi/2m$, and then shifting the newly created regions until the entire region of Eq. (3.3-4) is partitioned.

The transient time associated with a shifted region is simply $2m$ greater than the transient time associated with the original region. The original and shifted regions are illustrated in Fig. 3.3-2.

Generalizing, if

$$\sum_{p=0}^{n-1} 2G\cos p\pi/2m + (r-1)\pi/2m \leq \hat{\varphi}_o < \sum_{p=0}^{r} 2G\cos p\pi/2m + r\pi/2m \qquad (3.3-7)$$

then

$$w_k = \begin{cases} +1, & 0 \leq k \leq 2m - r \\ -1, & 2m - r < k \leq 2m \end{cases} \qquad (3.3-8)$$

where $0 \leq r \leq 2m$ (App. 2). The VCO phase at $k = 2m$ is

$$\hat{\varphi}_{2m} = \hat{\varphi}_0 + G \sum_{p=0}^{2m-r} (+1)(-2\cos p\pi/2m)$$

$$+ G \sum_{p=2m-r+1}^{2m-1} (-1)(-2\cos p\pi/2m)$$

$$= \hat{\varphi}_0 - 2G - 4G \sum_{p=1}^{r-1} \cos p\pi/2m \tag{3.3-9}$$

Again,

$$0 < \hat{\varphi}_{2m} < \hat{\varphi}_0 \tag{3.3-10}$$

(App. 2) and therefore the transient requires a finite number of iterations. The duration of the transient for a given $\hat{\varphi}_0$ and G is determined by building upon the regions of Fig. 3.3-2 until the entire rectangular region $0 < G < \pi/4m$, $0 \leq \hat{\varphi}_0 \leq \pi$ is partitioned. For $m = 4$, the result of such a construction is illustrated in Fig. 3.3-3.

Next, we consider $-\pi \leq \hat{\varphi}_0 < 0$. This will complete the analysis of the transient response since the DPLL responds identically to $\hat{\varphi}_0$ as it does to $\hat{\varphi}_0 + 2\pi n$, with n an integer. When $\hat{\varphi}_0$ is negative, the VCO output is initially -1, which in turn produces a positive output which increases the initially negative VCO phase. However, unlike the case for positive $\hat{\varphi}_0$, it is possible to fall into the steady state before $2m$ iterations. Before beginning the transient analysis, we list the VCO phase in the steady state sequence. This list appears in Table 3.3-1. Recognizing that the steady state sequence may begin at $k = 0$ or $k = 2m$, the steady state VCO phases intervals become the union of the intervals for $\hat{\varphi}_n$ and $\hat{\varphi}_{n+2m}$, listed in Table 3.3-2. Hence, if at any time during the transient the VCO phase falls into the interval given in Table 3.3-2, then the steady state sequence is generated.

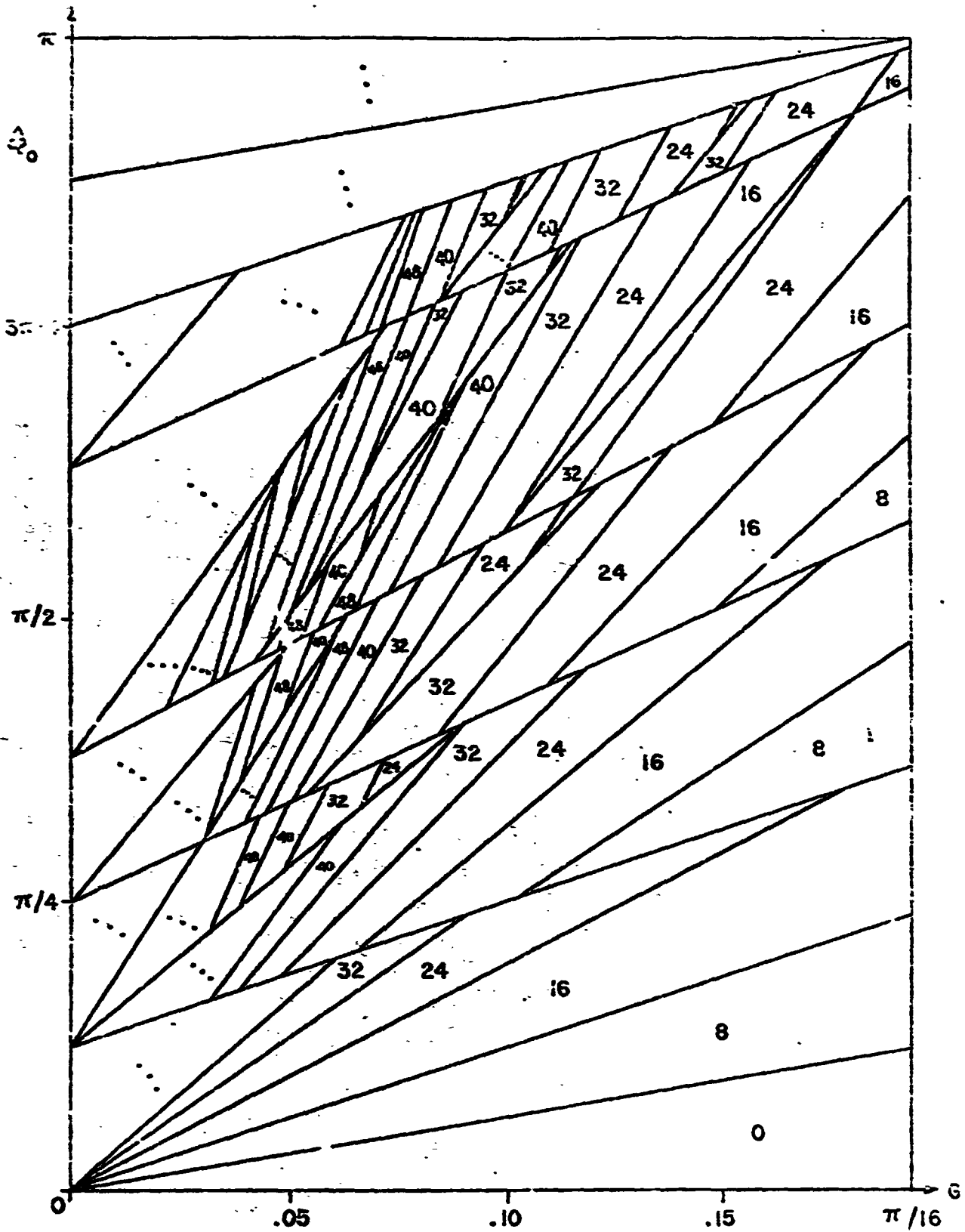If

$$-2G - \pi/2m \leq \varphi_0 < 0 \tag{3.3-11}$$

then

Fig. 3.3-3. Transient time (normalized to the sampling period) as a function of loop gain and positive initial VCO phase for the first order DPLL.

$$0 \le \hat{\varphi}_0 < 2G$$

$$-2G \le \hat{\varphi}_1 < 0$$

$$\vdots$$

$$-2G \sum_{p=0}^{n-1} \cos p\pi/2m \le \hat{\varphi}_n < 2G - 2G \sum_{p=0}^{n-1} \cos p\pi/2m$$

$$\vdots$$

$$-2G \le \hat{\varphi}_{2m} \le 0$$

$$0 \le \hat{\varphi}_{2m+1} < 2G$$

$$-2G \cos \pi/2m \le \hat{\varphi}_{2m+2} < 2G - 2G \cos \pi/2m$$

$$\vdots$$

$$-2G \sum_{p=1}^{n-1} \cos p\pi/2m \le \hat{\varphi}_{2m+n} < 2G - 2G \sum_{p=1}^{n-1} \cos p\pi/2m$$

$$\vdots$$

$$0 \le \hat{\varphi}_{4m} < 2G$$

Table 3.3-1 The VCO phase in the steady state DPLL output sequence.

50

$$-2G \leq \hat{\varphi}_0 < 2G$$

$$-2G \leq \hat{\varphi}_1 < 2G$$

$$\cdot$$
$$\cdot$$
$$\cdot$$

$$-2G \sum_{p=0}^{n-1} \cos p\pi/2m \leq \hat{\varphi}_n < 2G - 2G \sum_{p=1}^{n-1} \cos p\pi/2m$$

$$\cdot$$
$$\cdot$$
$$\cdot$$

$$-2G \leq \hat{\varphi}_{2m} < 2G$$

Table 3.3-2. The intervals that result from taking the union of the $\hat{\varphi}_n$ interval and the $\hat{\varphi}_{n+2m}$ interval of Table 3.3-1.

51

$$w_k = \begin{cases} -1, & k = 0 \\ +1, & 1 \leq k \leq 2m \end{cases} \qquad (3.3\text{-}12)$$

(proved in App. 2). That is, the first VCO output is -1, causing the VCO phase to increase, and the VCO to generate a $+1$ output at the next sample time. Also,

$$\hat{\phi}_{2m} = \hat{\phi}_o + (-1)(-2\cos 0 \, \pi/2m) + G \sum_{p=1}^{2m-1} (+1)(-2\cos p\pi/2m)$$

$$= \hat{\phi}_o + 2G \qquad (3.3\text{-}13)$$

and therefore

$$-2G < -\pi/2m \leq \hat{\phi}_{2m} < 2G$$

and so we have certainly reached steady state after $2m$ iterations. However, we actually reach steady state sooner; for if $-2G \leq \hat{\phi}_o < 0$, Table 3.3-2 tells us that we are in the steady state. Furthermore, since

$$\hat{\phi}_1 = \hat{\phi}_o + G(-1)(-2\cos 0\pi/2m) = \hat{\phi}_o + 2G$$

we reach the steady state after one iteration when

$$-4G \leq \hat{\phi}_o < -2G$$

Continuing, if $-6G \leq \hat{\phi}_o < -4G$, the after $2m$ iterations,

$$-4G \leq \hat{\phi}_{2m} < -2G$$

and hence the total transient requires $2m+1$ iterations. If $-8G \leq \hat{\phi}_o < -6G$, the transient requires $2m + 2m + 1 = 4m + 1$ iterations. Extending these results, the region of Eq. (3.3-11) is partitioned as shown in Fig. 3.3-4, where each region is labeled with the associated transient time and $m = 4$.

If

$$-2\pi/2m - 2G - 2G\cos\pi/2m \leq \hat{\phi}_o < -2G - \pi/2m \qquad (3.3\text{-}14)$$

Fig. 3.3-4. The partitions of the region of Eq. (3.3-11).

Fig. 3.3-5. The regions of Fig. 3.3-4 shifted down and their associated transient times.

then

$$w_k = \begin{cases} -1, & 0 \leq k \leq 1 \\ +1, & 2 \leq k \leq 2m \end{cases} \tag{3.3-15}$$

(App. 2). Here the first two VCO outputs are -1 before the VCO output changes sign. The VCO phase at $k = 2m$ is

$$\hat{\phi}_{2m} = \hat{\phi}_o + G \sum_{p=0}^{1} (-1)(-2\cos p\pi/2m) + G \sum_{p=2}^{2m-1} (+1)(-2\cos p\pi/2m)$$

$$= \hat{\phi}_o + 2G + 4G\cos\pi/2m \tag{3.3-16}$$

and combining this result with Eq. (3.3-14) we obtain

$$\hat{\phi}_o \leq \hat{\phi}_{2m} < 2G \tag{3.3-17}$$

so that steady state is indeed reached. Here it is possible to fall into the steady state sequence at $k = 2$; from Table 3.3-2, this happens when

$$-2G - 2G\cos\pi/2m \leq \hat{\phi}_2 < 2G - 2G\cos\pi/2m \tag{3.3-18}$$

Since $\hat{\phi}_2 = \hat{\phi}_o + 2G + 2G\cos\pi/2m$, Eq (3.3-18) becomes

$$-4G - 4G\cos\pi/2m \leq \hat{\phi}_o < -4G\cos\pi/2m \tag{3.3-19}$$

The intersection of the regions of Eqs. (3.3-14) and (3.3-19) yields a region which requires two iterations to reach steady state. The remaining portion of the region of Eq. (3.3-14) is partitioned by shifting the regions of Fig. 3.3-4 down by $2G + 4G\cos\pi/2m$, as specified by Eq. (3.3-16); the result is illustrated in Fig. 3.3-5, again for the case $m = 4$.

The generalization of the above is that for

$$-\left[(r+1)\pi/2m + \sum_{p=0}^{r} 2G\cos p\pi/2m\right] \leq \hat{\phi}_o < -\left[r\pi/2m + \sum_{p=0}^{r-1} 2G\cos p\pi/2m\right] \tag{3.3-20}$$

and $\phi_o \geq -\pi$, the VCO output is

54

$$w_k = \begin{cases} -1, & 0 \leq k \leq r \\ +1, & r+1 \leq k \leq 2m \end{cases} \qquad (3.3\text{-}21)$$

where $0 \leq r \leq 2m-1$ (App. 2). The VCO phase at $k = 2m$ is

$$\phi_{2m} = \phi_o + G \sum_{p=0}^{r} (-1)(-2\cos p\pi/2m)$$

$$+ G \sum_{p=r+1}^{2m-1} (+1)(-2\cos p\pi/2m)$$

$$= \hat{\phi}_o + 2G + 4G \sum_{p=1}^{r} \cos p\pi/2m \qquad (3.3\text{-}22)$$

and

$$\varphi_o < \hat{\phi}_{2m} < 2G \qquad (3.3\text{-}23)$$

(App. 2) so that the steady state is approached without an overshoot into the $\hat{\phi} > 2G$ region. Steady state is reached at $k = r+1$ if, by Table 3.3-2,

$$-2G \sum_{p=0}^{r} \cos p\pi/2m \leq \phi_{r+1} < 2G - 2G \sum_{p=1}^{r} \cos p\pi/2m \qquad (3.3\text{-}24)$$

Since

$$\hat{\phi}_{r+1} = \hat{\phi}_o + G \sum_{p=0}^{r} (-1)(-2\cos p\pi/2m) \qquad (3.3\text{-}25)$$

Eq. (3.3-24) can be expressed in terms of $\hat{\phi}_o$:

$$-4G \sum_{p=0}^{r} \cos p\pi/2m \leq \phi_o < 4G - 4G \sum_{p=0}^{r} \cos p\pi/2m \qquad (3.3\text{-}26)$$

Note that it is impossible to fall into the steady state at $k = r+1$ if $r > m$, since the regions of Eqs. (3.3-26) and (3.3-20) do not overlap:

$$- 4G \sum_{p=0}^{r} \cos p\pi/2m \; > \; - \left[r\pi/2m + \sum_{p=0}^{r-1} 2G \cos p\pi/2m \right] \quad \text{for } r > m$$

We may now proceed to construct regions in the $\hat{\phi}_o$ - G plane and label the required transient time. We start by confining attention to a region specified by Eq. (3.3-20) for a particular value of r; let us call this region R. The first step is to see if it is possible to fall into the steady state sequence after r iterations; i.e., we find the intersection of the regions of Eq. (3.3-20) and R. (As noted previously, this intersection is null if r > m.) This region requires r transient iterations. For any other point in R, the VCO phase satisfies Eq. (3.3-22); i.e., after 2m samples, it increases by the amount

$$\Delta = 2G + 4G \sum_{p=1}^{r} \cos p\pi/2m.$$

Hence, we translate the previously constructed regions upward by this amount, consider only their intersection with R, and observe that the transient time for the translated region is 2m greater than that for the original region. After this construction, there will still be a portion of R which is not partitioned. To partition this remaining region, we translate the newly constructed regions downward by the amount Δ, and continue this process until R is completely partitioned. The result of this process is illustrated in Fig. 3.3-6 where the entire region $-\pi \leq \hat{\phi}_o < 0$, $0 < G < \pi/4m$ is partitioned, for m = 4. Coupling this figure with Fig. 3.3-3 yields the complete transient behavior of the first order DPLL, since the loop responds identically to $\hat{\phi}_o + 2\pi$ as it does to $\hat{\phi}_o$.

One interesting feature of the digital phase-locked loop is that it does not possess an unstable equilibrium point (or, more precisely, sequence), as do both the analog loop and digital loop without VCO harmonics. For assume that the VCO is 180° out of phase with the input carrier. Then the VCO phase, which is initially π radians, becomes at k = 8:
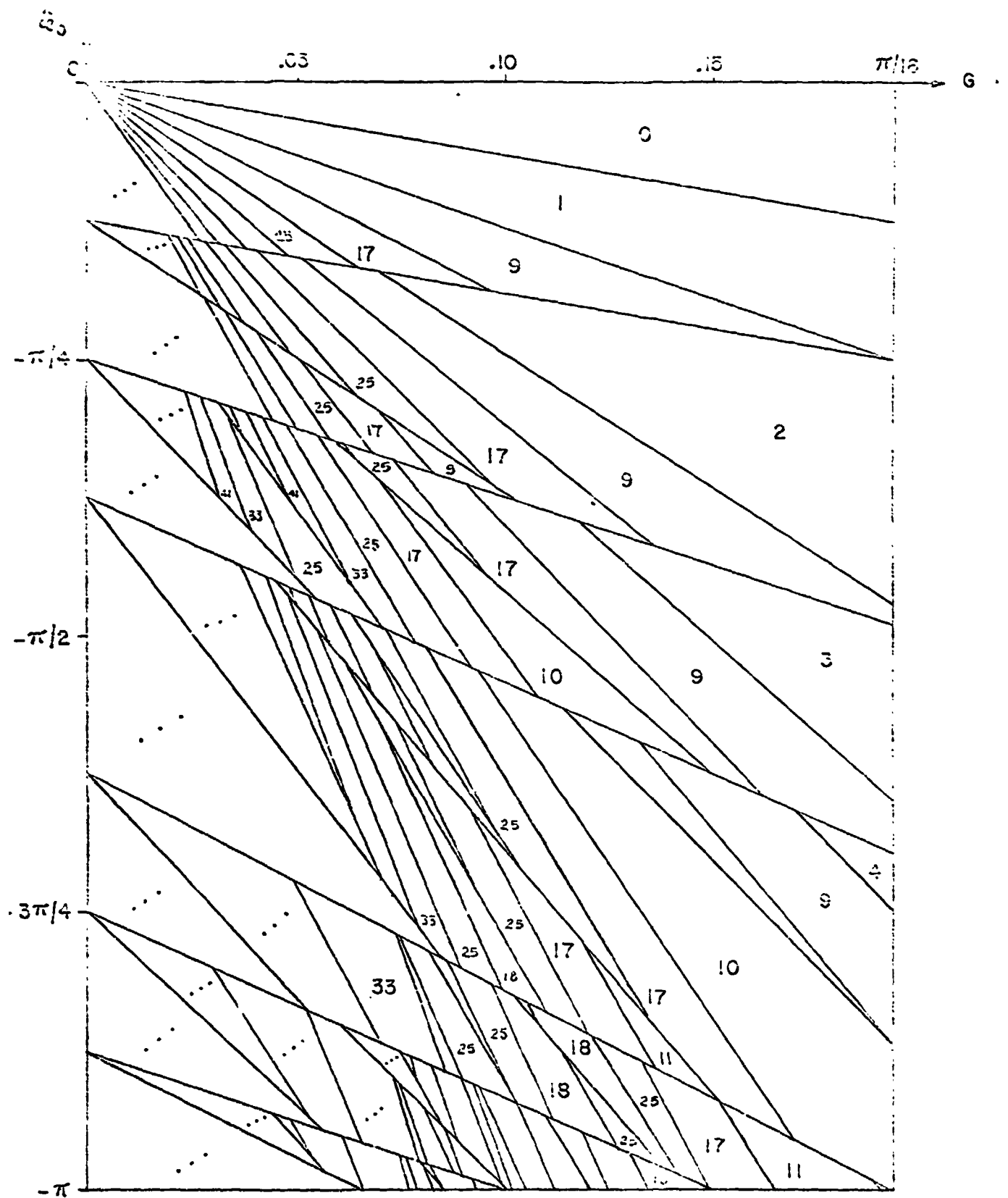
Fig. 3.3-6. Transient time (normalized to the sampling period) as a function of loop gain and negative initial VCO phase for the first order DPLL.

$$\hat{\phi}_8 = \hat{\phi}_o + G \sum_{p=0}^{7} (-1)(-2 \cos p\pi/8)$$

$$= -\pi + 2G$$

and the VCO output is

$$w_8 = Sq(8\pi/8 + \hat{\phi}_8) = Sq(2G) = +1$$

Hence the error signal at $k = 8$ is

$$y_8 = (-2 \cos 8\pi/8)(+1) = +2$$

as opposed to the -2 originally assumed, and

$$\phi_9 = -\pi + 2G + 2G = -\pi + 4G.$$

We see that it is impossible to keep the VCO phase at $-\pi$ after eight iterations, but instead this phase increases and the DPLL approaches the stable equilibrium sequence of Fig. 3.2-1.

A second feature of the DPLL is the variation of the transient time as a function of the loop gain, G, for some fixed initial VCO phase. Of course, we expect the transient time to decrease as the loop gain increases, as larger loop gains correspond to "faster" loops. This indeed is the situation for an analog loop but it is not precisely correct for the digital loop, with or without harmonics.

For the analog loop (where the sum terms are neglected) described by

$$\frac{d\hat{\phi}}{dt} = -G \sin \hat{\phi} \qquad (3.3-29)$$

we have

$$-\frac{1}{G} \int_{\hat{\phi}_o}^{0} \frac{d\hat{\phi}}{\sin \hat{\phi}} = \int_{0}^{T} dT$$

Since the left side diverges, we consider the time T for the initial VCO phase to reach 0.01 radian (an arbitrary figure). Then

58

$$T = \frac{1}{G} \int_{0.01}^{\hat{\Phi}_o} \frac{dx}{\sin x} = \frac{K}{G}$$

and the transient time is inversely proportional to the loop gain.

The digital loop with the VCO harmonics suppressed it described by Eq. (3.2-1), repeated here for convenience:

$$\hat{\Phi}_{k+1} = \hat{\Phi}_k - (4/\pi) G \sin \varphi_k \qquad (3\ 3\text{-}30)$$

Here, $0 < (4/\pi)G < 2$ for stability (Sec. 5.2). The number of iterations required for $|\hat{\Phi}_k| \leq 0.01$ is obtained as a function of loop gain, G, using a simple computer program, and the results are displayed in Fig. 5.3-7 for $\hat{\Phi}_o = \pi/2$ and $\hat{\Phi}_o = -3\pi/8$. The transient times are computed at discrete values of loop gain and so the graph is a set of discrete points. Notice that the inverse relationship between gain and transient time holds only for $G < 0.8$, but not for larger loop gains. From App. 2, we know that for $0 < (4/\pi)G < 1$ the VCO phase goes to zero monotonically but that for $1 < (4/\pi)G < 2$ it oscillates about zero, its magnitude approaching zero. Notice that although the difference equation Eq. (3.3-2) is a discrete version of the differential equation, Eq. (3.3-29), the former exhibits two distinct transient behaviors, while the latter exhibits only one. When G is small, the difference equation is a good approximation to the differential equation, and indeed both equations exhibit similar monotonic transient responses. However, if G becomes larger ($(4/\pi)G > 1$, to be exact), the approximation gets poorer. The difference equation is still stable but now exhibits an oscillatory transient, and the computed results show that the transient increases as the loop gain increases. This is expected as larger loop gain causes a greater overshoot of the origin by $\hat{\Phi}_k$ and hence more iterations are required to achieve $|\hat{\Phi}_k| \leq 0.01$.

For the digital loop, with VCO harmonics included, the transient times are obtained from Figs. 3.3-3 and 3.3-6 by simply following a horizontal line at $\hat{\Phi}_o$ through the various regions. The results are displayed in Fig. 3.3-8 for $\hat{\Phi}_o = \pi/2$ and $\hat{\Phi}_o = -3\pi/8$, and we see that the curve is roughly an
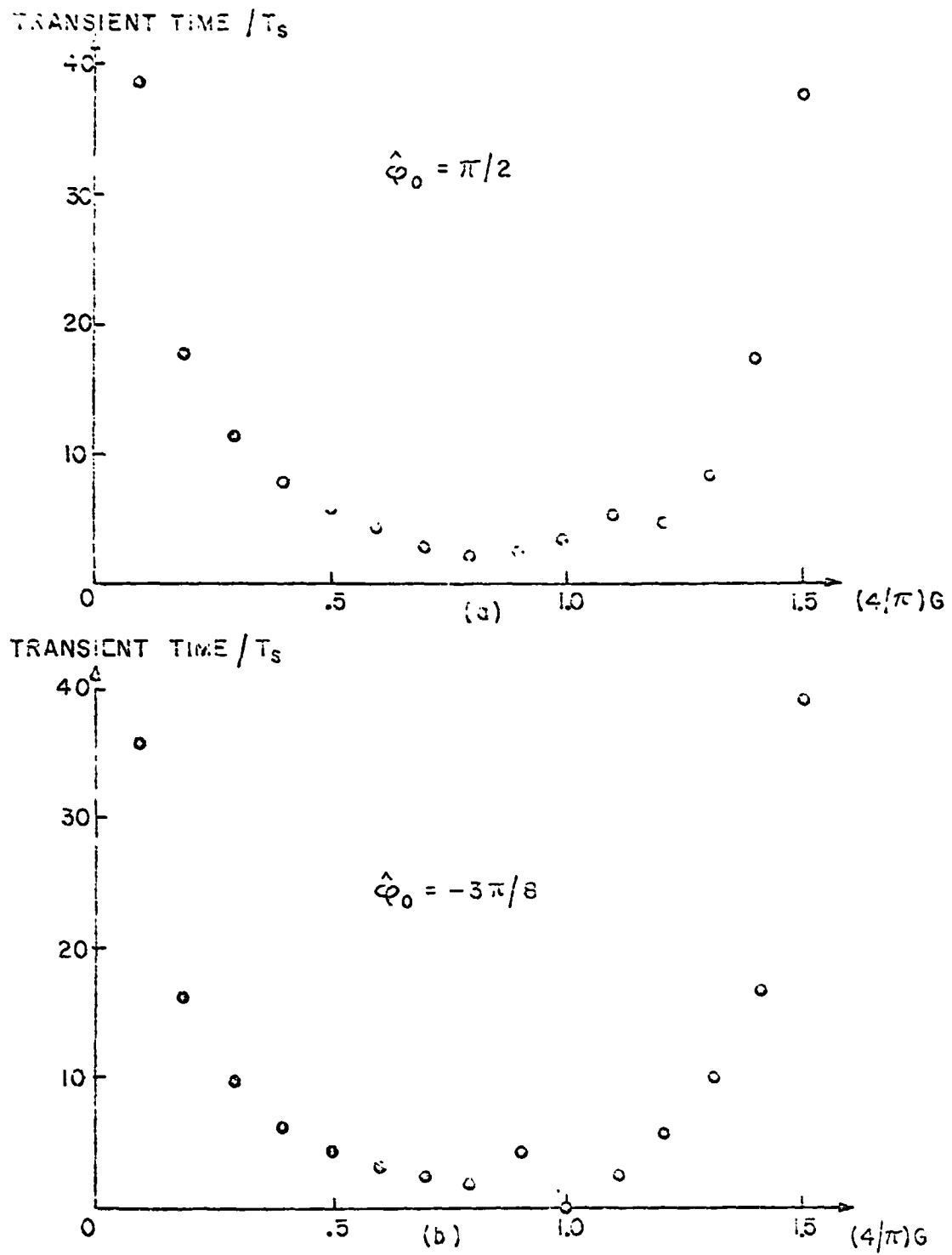
59

Fig. 3.3-7. Transient time as a function of loop gain for a first order DPLL without harmonics.
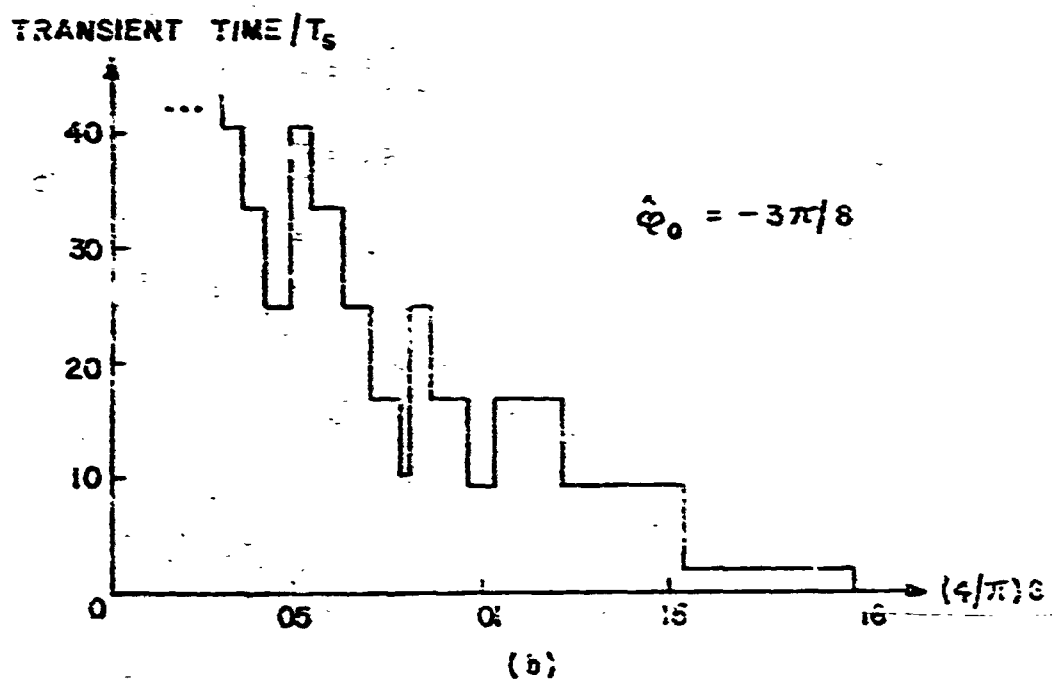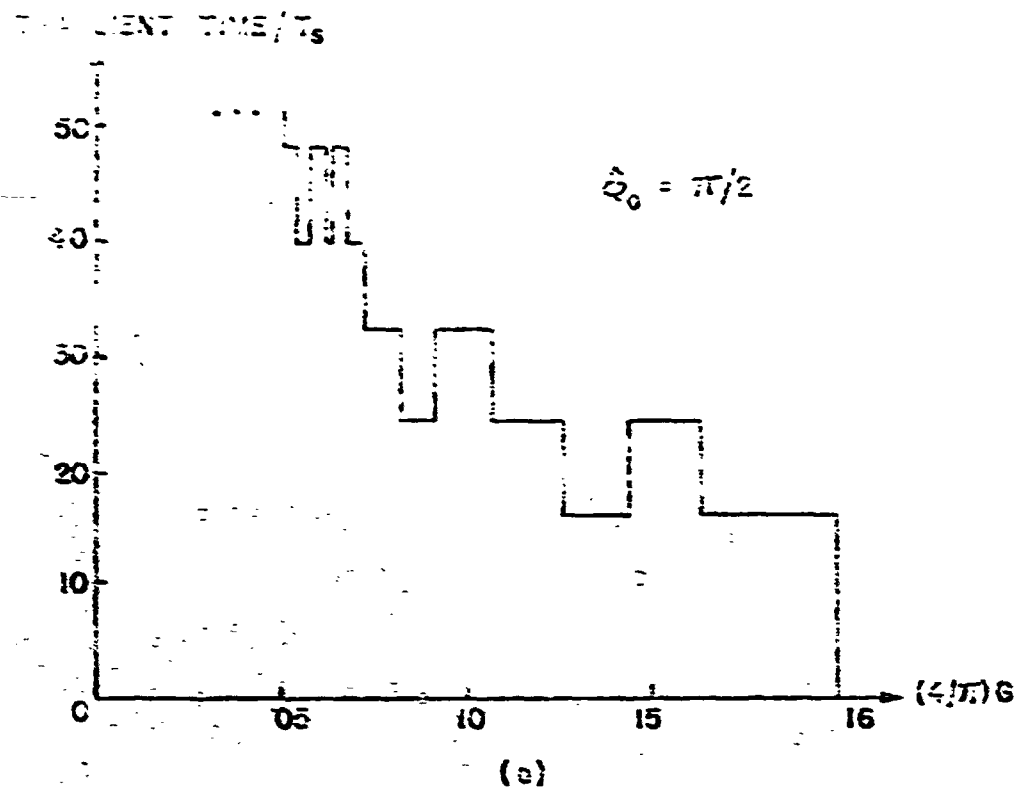
60

Fig. 3.3-8. Transient time as a function of loop gain for a first order DPLL with harmonics included.

inverse relationship except for certain intervals of gain where the loop falls into a "faster" region.

3.4 Response to a Frequency Offset

If the input carrier frequency is deviated by Δf Hz, a phase error develops between the input and VCO, generating a phase error which has a nonzero average value. Such a phase error sequence is illustrated in Fig. 3.4-1. The average value is just the correct amount to deviate the VCO frequency by Δf Hz so that the loop is in equilibrium, tracking the deviation with a phase lag error.

This thesis deals with the FM demodulation capabilities of a digital phase-locked loop as opposed to the tracking capabilities. Therefore, we examine the steady state behavior of the DPLL, not the transient response. Indeed, a complete solution of Eq. (2.1-7) is extremely difficult, even for the case of no noise and an input frequency offset.

With the DPLL in the steady state we can calculate the phase error developed as a function of input frequency deviation, and use the result to obtain the maximum trackable offset as a function of the loop gain.

The input to the DPLL is

$$x_k = -2\cos(k\pi/2m + k\,2\pi\Delta f/f_s) \qquad (3.4\text{-}1)$$

where Δf = frequency offset in Hz. The VCO is running at the same frequency but with a phase error and the VCO output can be written as

$$w_k = Sq\left[(k - E)(\pi/2m + 2\pi\Delta f/f_s)\right] \qquad (3.4\text{-}2)$$

Let the deviated frequency correspond to $2N$ samples:

$$N = \left[\pi/(\pi/2m + 2\pi\Delta f/f_s)\right] \qquad (3.4\text{-}3)$$

where the square brackets denote "integer part". The equation that determines E as a function of Δf states that over N samples the VCO phase shall increase by the amount $N\,2\pi\Delta f/f_s$:

Fig. 3.4-1. Typical phase error sequence when the input frequency is deviated from the carrier frequency.
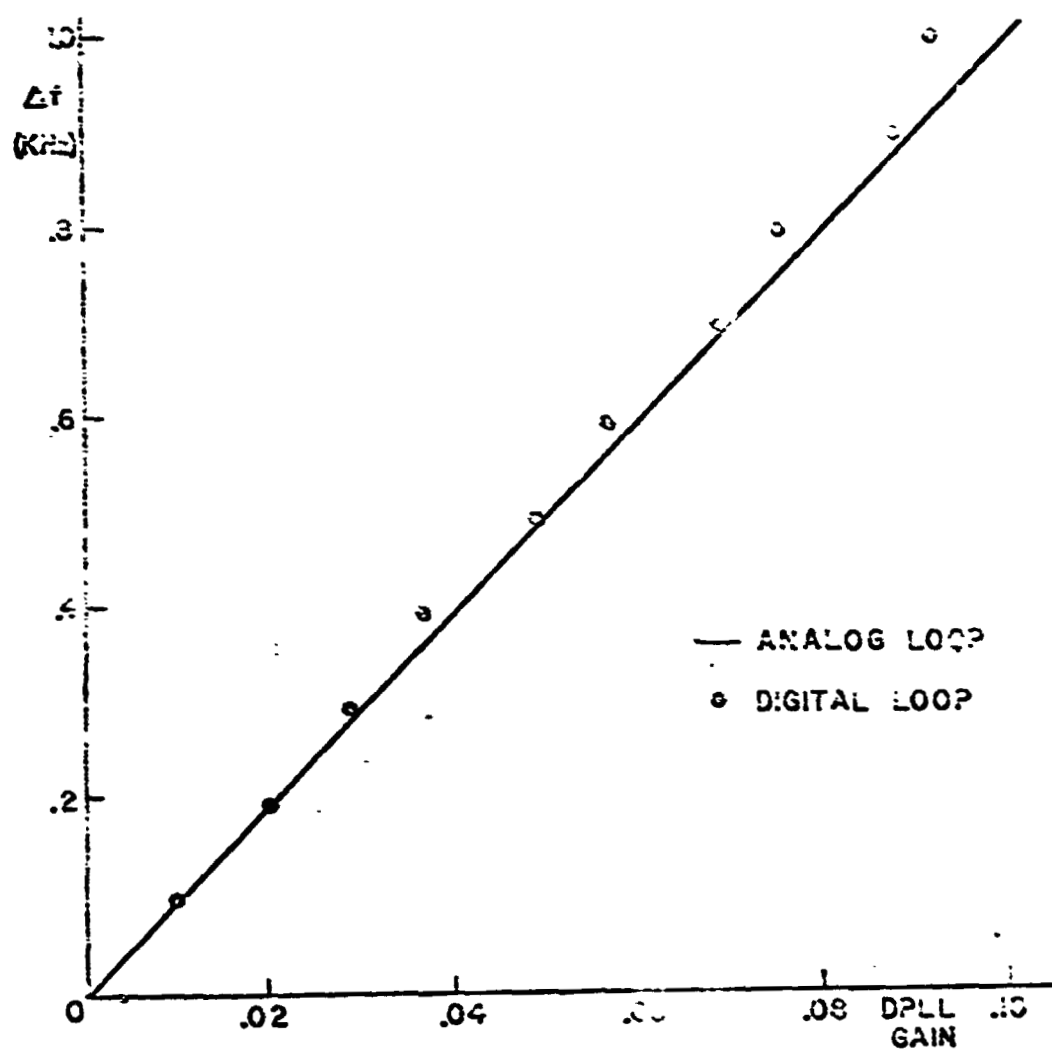

Fig. 3.4-2. Maximum trackable frequency deviation as a function of loop gain for both analog and digital phase-locked loops.

$$\sum_{p=E}^{E+N-1} (+1)\left[-2\cos p\left(\pi/2m + 2\pi\Delta f/f_s\right)\right] = N\, 2\pi\Delta f/f_s \qquad (3.4\text{-}4)$$

Performing the summation and using the approximation

$$N\left(\pi/2m + 2\pi\Delta f/f_s\right) \approx \pi$$

we obtain

$$E = \frac{1}{2} + \frac{1}{\left(\dfrac{\pi}{2m} + \dfrac{2\pi\Delta f}{f_s}\right)} \sin^{-1}\left\{ \frac{\dfrac{N\,2\pi\Delta f}{f_s}\ \sin\dfrac{1}{2}\left[\dfrac{\pi}{2m} + \dfrac{2\pi\Delta f}{f_s}\right]}{2G} \right\} \qquad (3.4\text{-}5)$$

The maximum offset trackable occurs when the argument of the inverse sine is unity:

$$2G = (N\, 2\pi\,\Delta f/f_s)\,\sin(\pi/2m + 2\pi\,\Delta f/f_s)/2 \qquad (3.4\text{-}6)$$

Note that if $(\pi/2m + 2\pi\Delta f/f_s)/2 \ll \pi/2$, then Eq. (3.4-6) becomes

$$2\pi\Delta f \approx (4/\pi)\, G\, f_s \qquad (3.4\text{-}7)$$

which is the corresponding result for a first order analog loop where, as observed in Sec 3.1,

$$G_{analog} = (4/\pi)\, G\, f_s . \qquad (3.4\text{-}8)$$

In Fig. 3.4-2, the maximum trac___e offset, Δf, is plotted against the loop gain, G, for both the digital and analog phase-locked loops, for the case $m = 4$, and as anticipated by Eq. (3.4-7), the two curves agree closely.

3.5 Design Values for the First Order DPLL

The first order DPLL utilizes a 10-bit A/D converter, and therefore the error signal is a 10-bit word. From Table 2.5-1, the restriction on the phase error signal, e_k, is

$$|e_k|_{max} \leq 0.35 \qquad (3.5\text{-}1)$$

64

The restriction that the first VCO harmonic fall outside the DPLL bandwidth, B_L, is given by Eq. (2.6-4), and repeated here:

$$f_s/2m - 2\Delta f \geq B_L \qquad (3.5-2)$$

where

$$f_s = \text{sampling frequency}$$

$$\Delta f = \text{maximum frequency deviation}$$

All of the digital phase-locked loops were constructed using TTL and DTL logic, having speeds of 1 MHz and 10 MHz respectively and to allow a sufficient computation interval for third order loop calculations, the sampling frequency is chosen to be 50 KHz.

The digital filter in the first order DPLL is simply a proportional path of gain g_1 producing the linearized model of Fig. 3.5-1. If the input carrier is deviated in frequency by Δf Hz, the input phase is

$$\varphi_k = 2\pi \Delta f k T_s \qquad (3.5-3)$$

and the error signal, e_k, appearing in the linearized model of Fig 2.7-1 is

$$e_k = \frac{4}{\pi} \frac{2\pi\Delta f/f_s}{(4/\pi) g_1 G_{VCO}} = \frac{2\pi\Delta f}{Gf_s} \qquad (3.5-4)$$

where G = loop gain = $g_1 \cdot G_{VCO}$. Imposing the restriction of Eq. (3.5-1) yields

$$\frac{2\pi\Delta f}{Gf_s} \leq 0.35 \qquad (3.5-5)$$

The input phase-output voltage transfer function of the linearized model is

$$\frac{Y(z)}{\Phi(z)} = \frac{(4/\pi) g_1 (1 - z^{-1})}{1 - [1 - (4/\pi)g_1 G_{VCO}] z^{-1}} \qquad (3.5-6)$$

and taking the difference $(1-z^{-1})\Phi(z)$ as the input frequency yields the

input frequency-output voltage transfer function:

$$\frac{Y(z)}{(1 - z^{-1})\hat{\theta}(z)} = \frac{(4/\pi)\, g_1}{1 - [1 - (4/\pi)G]\, z^{-1}} \tag{3.5-7}$$

If $(4/\pi) \ll 1$, the bandwidth, B_L, of this transfer characteristic is given by (App. 3)

$$B_L \approx (2/\pi^2)\, f_s \cdot G \qquad Hz \tag{3.5-8}$$

Using Eqs. (3.5-8) and (3.5-5) in Eq. (3.5-2), we obtain the design equation

$$m \leq f_s / 11.28\, \Delta f \tag{3.5-9}$$

The sampling frequency is chosen to be 50 KHz which allows a sufficient computation interval (20 μ sec) for the DTL and TTL logic employed. Then, for $\Delta f = 600$ Hz, Eq. (3.5-9) yields

$$m \leq 7.4 \tag{3.5-10}$$

The VCO algorithm is simplified when m is a power of two; hence we choose $m = 4$. Eqs. (3.5-5) and (3.5-8) yield

$$G \geq 0.216$$
$$B_L \approx 2.16\ \text{KHz} \tag{3.5-11}$$

The realizable loop gains are of the form

$$G = \pi/5 \cdot 2^N, \qquad N = \text{integer} \tag{3.5-12}$$

and using $N = 1$ yields $G = 0.314$, satisfying Eq. (3.5-11). However, the maximum allowable loop gain from stability considerations is $\pi/2m = \pi/8 = 0.394$, and this proves to be too close to 0.314, so we shall use

$$G = \pi/5 \cdot 2^2 = 0.157 \tag{3.5-13}$$

As the condition $(4/\pi)\, G \ll 1$ is not satisfied, the bandwidth approximation of Eq. (3.5-8) is conservative; the actual bandwidth is

$$B_L = 1800 \ Hz,$$

which still satisfies Eq. (3.5-2).

The fact that our maximum frequency deviation is rather small ($\Delta f = 500$ Hz) stems directly from the limitions of the logic speed. Had faster logic been available, then Δf could have been increased by the same factor as the logic speed increases. For example, using ECL, the sampling frequency could be increased by a factor of 10 and hence Δf could be ten times larger without changing the value of m.

Summarizing, the design values for the first order DPLL are:

$$G = 0.157 = \pi / 5 \cdot 2^2$$
$$\Delta f = 600 \ Hz$$
$$f_s = 50 \ KHz$$
$$m = 4$$

For an additional illustration of the design procedure, consider a voice channel requiring

$$f_m = 3500 \ Hz$$
$$\beta = 3$$
$$\Delta f = 10.5 \ KHz$$

If the A/D converter employs ten bits, we require

$$m \leq f_s / 11.28 \ \Delta f = 8.45 \cdot 10^{-6} \ f_s \qquad (3.5-14)$$

Using $f_s = 500$ KHz allows us to choose $m = 4$; the required arithmetic computations can be performed in one sampling period if ECL logic is utilized. The bandwidth restriction is

$$B_L < f_s / 2m - 2 \ \Delta f = 36 \ KHz$$

and loop gain restriction is $G \geq 0.3$. The choice for the loop gain is $G = \pi/5 \cdot 2 = 0.314$ resulting in $B_L = 36$ KHz.

3.6   Hardware Implementation

The block diagram of the first order DPLL is shown in Fig. 3.6-1.
Following the sample-and-hold and analog-to-digital conversion, we
have a ten-bit binary word, x_k. The bank of exclusive-or gates performs
the multiplication of x_k and the VCO output, $w_k = Sq(k\pi/2m + \hat{\varphi}_k)$,
and the result is stored in the output register, whose contents are conver-
ted back to analog form and filtered. The output is also scaled and inte-
grated to generate the VCO argument, $(k+1)\pi/2m + \hat{\varphi}_{k+1}$, which is stored
in the VCO register and used to multiply the next input, x_{k+1}.

To obtain the gain $G = \pi/5 \cdot 2^2$, a factor of $1/16 = 1/2^4$ is used for
the explicit VCO gain, leaving $\pi/(5/2^2)$ as the implicit VCO gain. This
implicit is realized by using the third most significant bit of the VCO
register to feed the exclusive-or gates (multiplier), as this bit corresponds
to $5/2^2$ volts. Notice that the foward loop contains unity gain; this is
because the D/A converter uses only ten bits and scaling in the foward
loop would mean a loss of bits in the output. Also, the unity gain insures
that a maximum number of the D/A's ten bits are used, so that the signal-
to-quantization noise ratio is a maximum.

In order to avoid introducing truncation error, the VCO register and
adder use 14 bits. In this way, all bits are retained after the scaling by
1/16. The constant $(\pi/8)/(\pi/1.25) = 1.25/8$ has the 14-bit binary
representation given by

$$1.25/8 = 1\,0\,0\,0\,0\,1\,0\,0\,0\,0.0\,0\,0\,0$$

This follows from the fact that the sign bit represents 5 volts.

To understand the sequence of events in the first order DPLL, consider
the timing diagram illustrated in Fig. 3.6-2. The computation interval
(itentical to the sampling period) of 20 μsec is divided into five addition
intervals as shown. The last two are for the VCO computation; the remain-
ing three, labelled AT1, AT2, AT3 are not used in the first order DPLL--
they are reserved for the second and third order DPLL computations. Al-
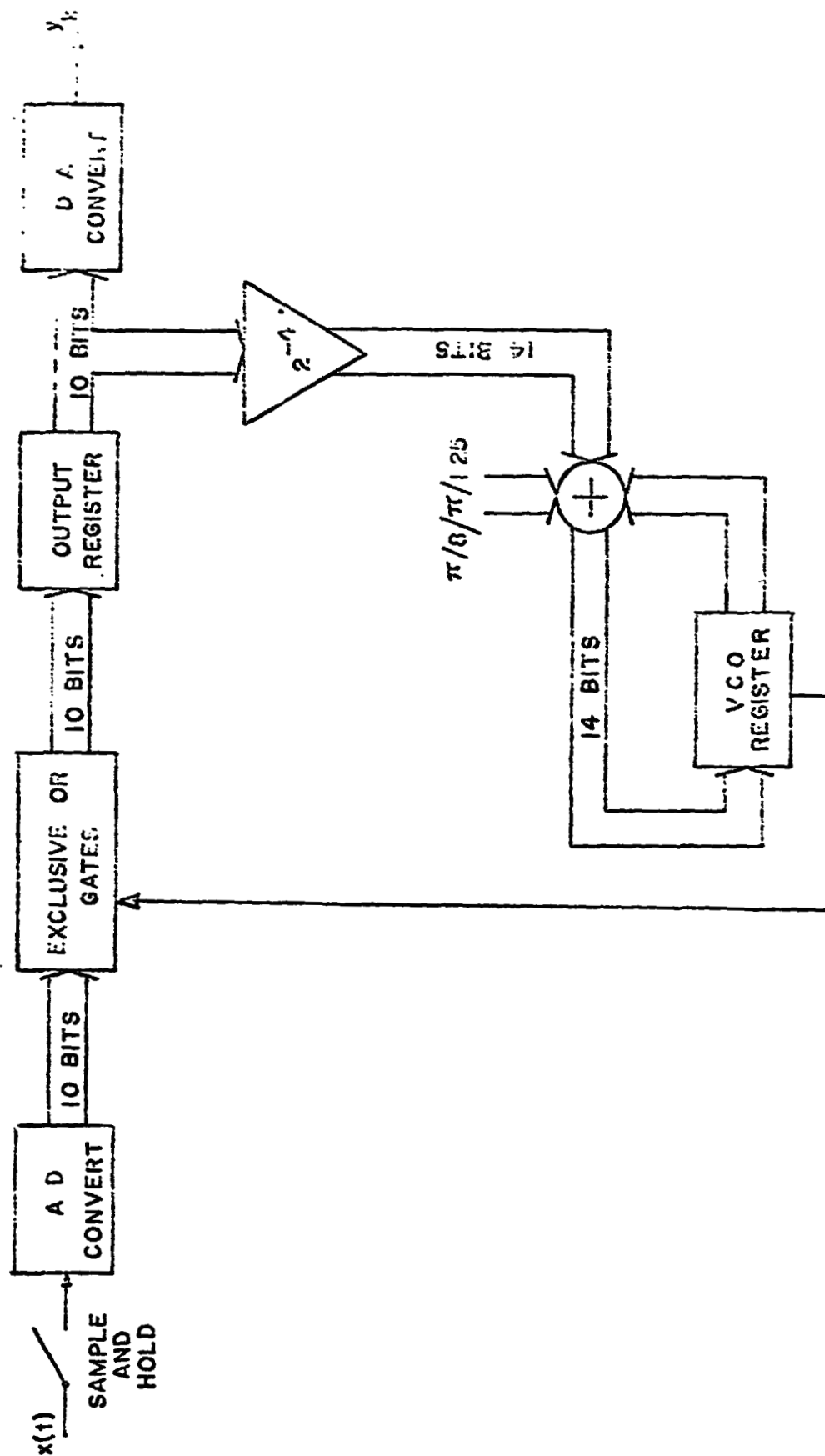though Fig. 3.6-1 explicitly shows a three-input adder, only a two-input

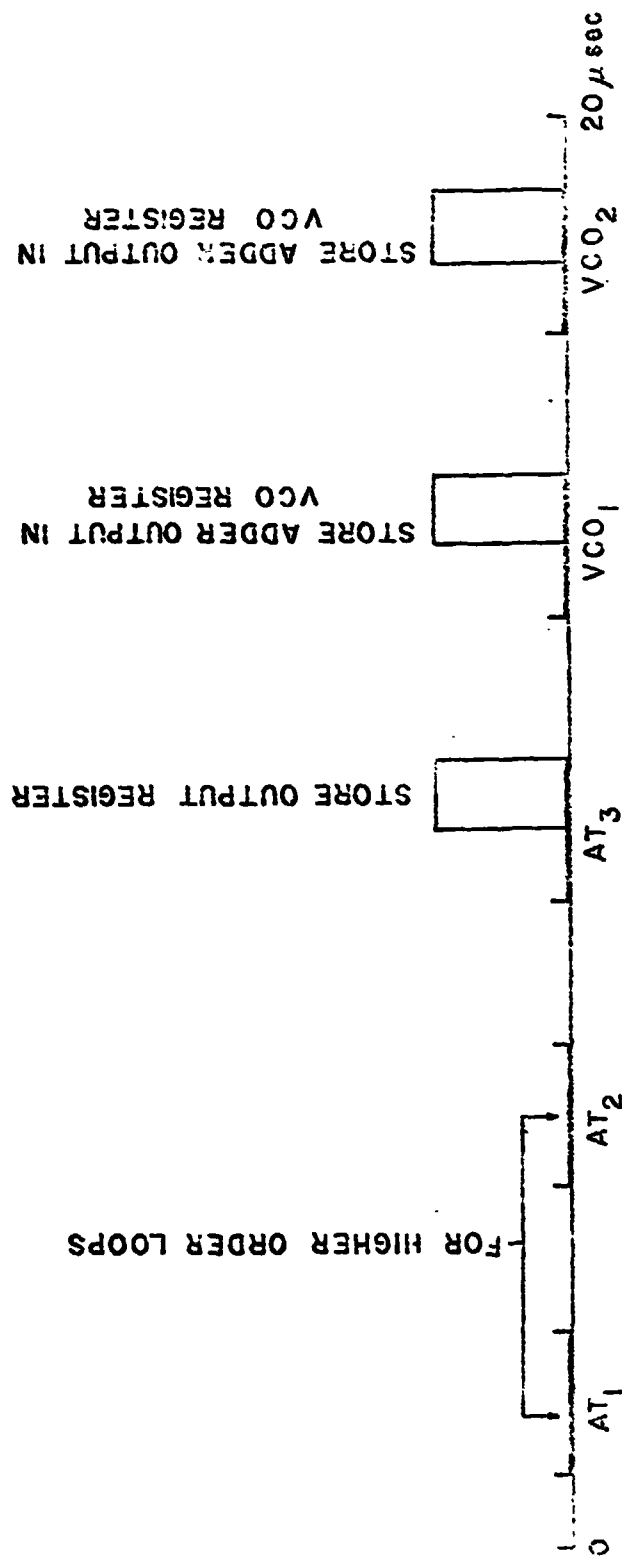68

Fig. 3.6-1. Schematic diagram of the first order DPLL.

Fig. 3.6-2. Timing diagram for the first order DPLL.

adder is employed and we use this two-input adder twice, requiring the two VCO addition intervals shown in the timing diagram.

We start at $t = 0$ with the input binary word x_k (the A/D converter requires 10 μsec for conversion; hence $x(t)$ was sampled at $t = 10$ μsec of the previous computation interval). As soon as x_k is generated, it is passed through the exclusive-or gates; that is, x_k is multiplied by $w_k = Sq(k\pi/2m + \hat{\phi}_k)$. At $t = 10$ μsec, a command is given to store this product, y_k, in the output register. At $t = 13$ μsec, y_k is taken from the output register and sent to two channels: the output and the feedback paths. In the feedback path, $(1/16)y_k$ is added to the VCO register contents, denoted by VCO_k, and this temporary result is stored in the VCO register. During the next VCO computation interval, the contents of the VCO register are added to the constant $(\pi/8)/(\pi/1.25)$ and the result stored again in the VCO register. The VCO register now contains the new value of the VCO argument, VCO_{k+1}, where

$$VCO_{k+1} = (\pi/8)/(\pi/1.25) + y_k/16 + VCO_k$$

This value is used to generate the VCO output by having the third most significant bit of the VCO register feed the exclusive-or gates. At $t = 20$ μsec, the new input, x_{k+1}, is available and the computation cycle begins again.

3.7 Output Noise

In this section we compute the output thermal, quantization, and harmonic noise of the digital phase-locked loop. At large input signal-to-noise ratios, the DPLL is able to follow the input modulation with a small phase error; hence the linearized model of Sec. 2.8 is used in the calculation. This first order linearized model is shown in Fig. 3.7-1. The quantization noise which arises from the finite number of voltage levels available is present regardless of any thermal noise, and is responsible for the maximum attainable output signal-to-noise ratio. As the quanti-
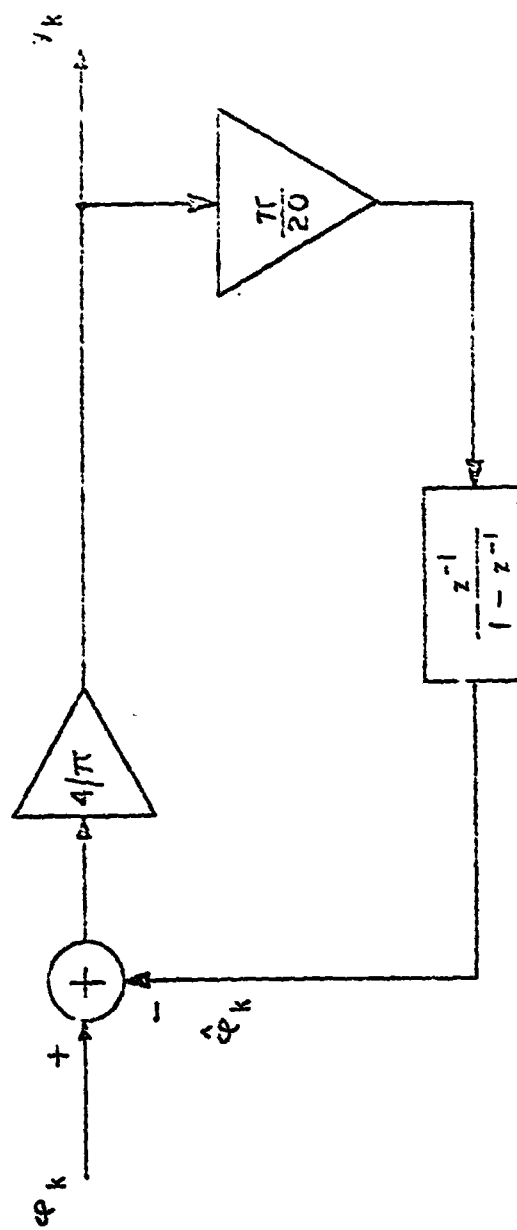
Fig. 3.7-1. Linearized model of the first order DPLL.

zation noise is present when the phase error is small, the output quantization noise is calculated using the linearized model.

At low input signal-to-noise ratios, the input noise spikes begin to appear and the phase error no longer remains small, invalidating use of the linearized model. To gain some insight into the DPLL performance with input noise spikes, a deterministic model of a noise spike is introduced, the DPLL nonlinear difference equation is solved via computer, and the result (VCO phase solution) is examined to see whether or not the DPLL follows the input spike.

3.7.1 Output Thermal Noise

Let the input FM signal be corru ted by additive white, Gaussian noise having a two-sided power spectral density $\eta/2$. Then the bandpass filtered signal plus noise is expressed as

$$x(t) = n_1(t)\cos 2\pi f_0 t - n_2(t)\sin 2\pi f_0 t + A\cos\left[2\pi f_0 t + \varphi(t)\right] \qquad (3.7\text{-}1)$$

where $n_1(t)$ and $n_2(t)$ are white, Gaussian noises, bandlimited to B_{IF}, the IF bandwidth, and having two sided power spectral density η. Also, f_0 is the carrier frequency. When the input signal-to-noise ratio $(S_i/N_i = \eta B_{IF}/2A^2)$ is large, Eq. (3.7-1) is approximately given by

$$x(t) \approx 2A\cos\left[2\pi f_0 t + \varphi(t) + n_2(t)/2A\right] \qquad (3.7\text{-}2)$$

That is, the thermal noise introduces a phase contribution $n(t) = n_2(t)/2A$, having two-sided power spectral density

$$G_n = \eta/4A^2 \qquad (3.7\text{-}3)$$

The linearized first order DPLL transfer function is

$$H(z) = \frac{Y(z)}{\Phi(z)} = \frac{z-1}{z+G-1} \qquad (3.7\text{-}4)$$

and the output noise power is

$$N_o = \int_{-f_m}^{f_m} G_n(f)\; |H(e^{j2\pi f/f_s})|^2\, df \qquad (3.7\text{-}4)$$

73

where f_m is the cut-off frequency of the output low pass filter. Now $f_m \ll f_s$ and so for $|f| \le f_m$ we have

$$|H(e^{j2\pi f/f_s})| \approx 2\pi f/Gf_s \qquad (3.7\text{-}6)$$

yielding

$$N_o \approx (2\pi/Gf_s)^2 \, \eta \, f_m^3 / 6A^2 \qquad (3.7\text{-}7)$$

The input signal power is $S_i = 2A^2$; the output signal-to-noise ratio is

$$\frac{S_o}{N_o} = \frac{S_o}{(2\pi/Gf_s)^2 \, \eta f_m^3 / 6A^2} \qquad (3.7\text{-}8)$$

If the modulating signal is a constant, producing a fixed frequency deviation Δf Hz from the carrier, the input phase is

$$\varphi_k = 2\pi\Delta f\, k/f_s \qquad (3.7\text{-}9)$$

The linearized model tracks this frequency deviation with a phase error:

$$\hat{\phi}_k = \varphi_k - 2\pi\Delta f/(4/\pi)f_s G \qquad (3.7\text{-}10)$$

and the output is a constant:

$$y_k = 2\pi\Delta f/f_s G \qquad (3.7\text{-}11)$$

Hence the output signal power is $S_o = (2\pi\Delta f/f_s G)^2$ and

$$\frac{S_o}{N_o} = 3\beta^2 \frac{S_i}{\eta f_m} \qquad (3.7\text{-}12)$$

as expected.

If the modulation is sinusoidal the input phase is

$$\varphi_k = \beta \sin 2\pi f_m k/f_s \qquad (3.7\text{-}13)$$

with β = modulation index, f_m = modulating frequency, and, of course,

74

$\Delta f = 2 f_m$. Then the linearized loop output is also sinusoidal with amplitude given by

$$ y_{max} = \beta \, |\Xi(e^{j2\pi f_m/f_s})| \approx 2\pi \beta f_m / G f_s \tag{3.7-14} $$

The output signal power is $S_o = (y_{max})^2/2$, and, as expected,

$$ \frac{S_o}{N_o} = \frac{3}{2} \beta^2 \frac{S_i}{N_i} \tag{3.7-15} $$

The results of Eqs. (3.7-12) and (3.7-15) are of course identical to results for an ordinary discriminator, as the DPLL transfer function is identical to a differentiator transfer function; that is, above threshold, the digital phase-locked loop performance is identical to a discriminator.

3.8 Quantization Noise

As we have a finite number of bits available, we have a finite number of voltage levels representable be these bits. Hence, the sampled input signal is quantized to these levels and an error is committed, producing a noise component at the output. This quantization noise component is present even with no input thermal noise, and limits the maximum attainable output signal-to-noise ratio.

At each sampling instant, when the A/D converter acts on an input voltage level, the binary word obtained represents the voltage level rounded off to the nearest available level. Thus the error committed lies between $-S/2$ and $+S/2$, where S is the quantization step size. Assuming that the true level is uniformly distributed over its range, the error is uniformly distributed over the range $(-S/2, S/2)$, and has a variance

$$ \sigma^2 = S^2/12 \tag{3.7-16} $$

Now, the quantization errors from sample to sample are independent. This follows from the fact that between samples the input signal varies over many quantization levels. In fact, the sampling frequency is below the carrier frequency and so, between samples, the input varies over at

least one cycle, which means a variation over all the quantization
levels. Since the errors are independent, the power spectral density
of the quantization noise is white [17]:

$$G_{n_q} = S^2 / 12 f_s \qquad (3.7\text{-}17)$$

where f_s is the sampling frequency. The output quantization noise, N_q^q,
is therefore

$$N_q = \int_{-f_m}^{f_m} G_{n_q} |E(e^{j2\pi f/f_s})|^2 df = (2\pi/G)^2 (f_m/f_s)^3/18 \qquad (3.7\text{-}18)$$

3.7.3 Spike Response

The thermal output noise results obtained above are valid only at
large input signal-to-noise ratios, for which the input noise approxima-
tion of Eq. (3.7-2) and the linearization of the DFLL are valid. When the
input signal-to-noise ratio deteriorates, both of these assumptions are
invalid and the input signal is corrupted by noise spikes. A noise spike
appears when the signal plus noise phasor rotates completely around the
origin causing the input phase to increase by 2π radians. The input fre-
quency consequently contains a sharp pulse, having the area 2π. Figure
3.7-2 illustrates the input phase and instantaneous frequency when a spike
appears.

The spike duration, T_{spike}, depends upon the IF bandwidth, B_{IF}. To
obtain this relationship, consider the modulation deviating the carrier to
the high end of the IF bandwidth. Then all the noise components are at a
lower frequency than the carrier and the tendency is for the signal plus
noise phase angle to rotate clockwise. If at some instant of time all the
noise power is concentrated at the lowest IF frequency, then the noise
phasor is rotating at $-B_{IF}$ Hz with respect to the signal phasor, and the
time required for one complete revolution is

$$T_{spike} = 1/B_{IF} \qquad (3.7\text{-}19)$$

INPUT PHASE

2π
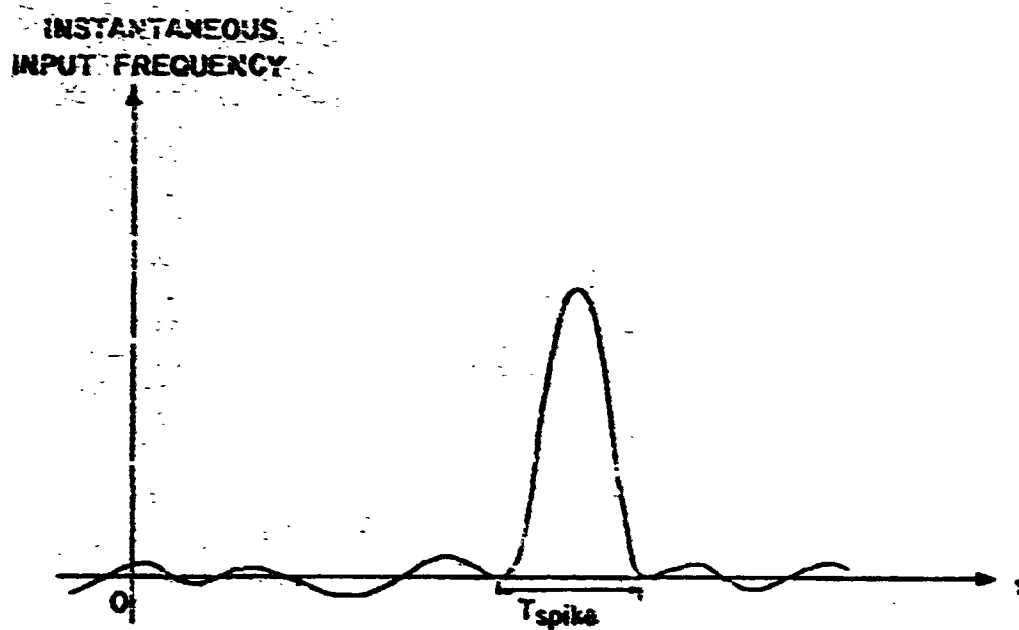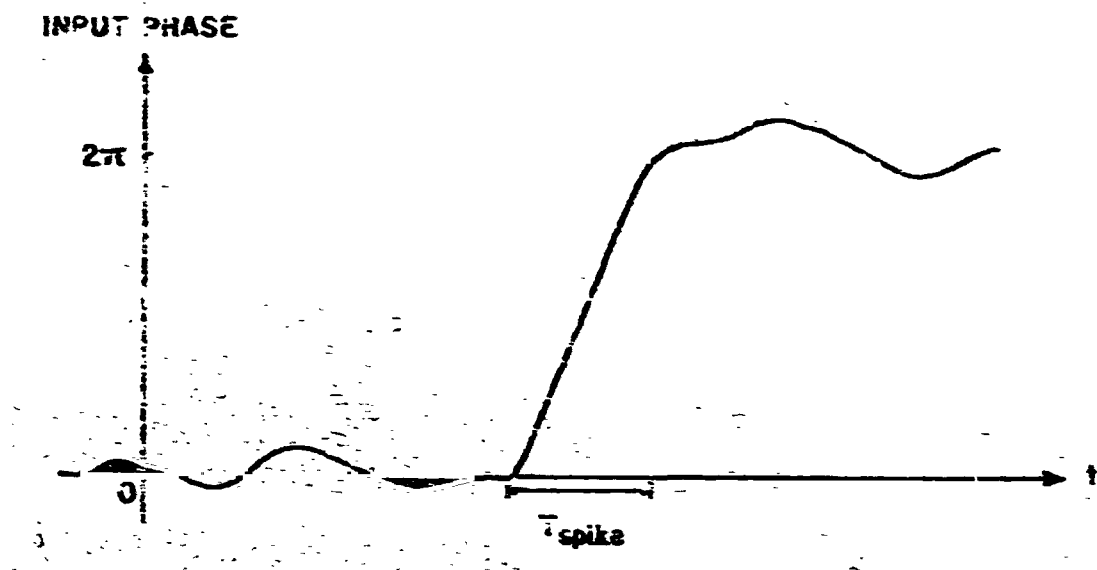
0

T_spike

INSTANTANEOUS
INPUT FREQUENCY

0

T_spike

Fig. 3.7-2. The input phase and instantaneous frequency when a noise spike appears.

This, of course, represents the fastest possible spike.

A differentiating discriminator demodulates the input phase change producing a spike, or, as it is sometimes referred to, a "click", in the output. It is the appearance of clicks that degrades the output signal and causes the output signal-to-noise ratio to fall off sharply. A phase-locked loop possesses the ability to convert an input spike into a doublet (the derivative of a spike) by virtue of its periodic phase detector characteristic. The power spectral density of the doublet is f^2 times the power spectral density of the spike and hence the doublet contributes significantly less power to the baseband signal than does the spike.

To see how a phase-locked loop converts a spike into a doublet, let us examine the phase detector characteristic. The characteristic arises from the product of input signal $[-2\cos(\omega_0 t + \varphi)]$ and VCO square wave fundamental $[(4/\pi)\sin(\omega_0 t + \hat{\varphi})]$ and is given by

$$e_k = (4/\pi)\sin(\varphi_k - \hat{\varphi}_k) \qquad (3.7-20)$$

Eq. (3.7-20) is plotted in Fig. 3.7-3. When the phase-locked loop is demodulating the input, we are operating in the vicinity of $e_k = 0$. (Our design equation based on quantization noise and harmonic distortion requires $|e_k| < 0.35$ for a two-bit A/D converter.) When a noise spike appears, the input phase φ_k rapidly increases by 2π, producing a large phase error. Depending on the loop gain (and the nature of the spike), the VCO phase $\hat{\varphi}_k$ may either increase by 2π or remain in the neighborhood of zero. In the former case, the DPLL follows the spike and the output, which is proportional to the derivative of the VCO phase will contain a spike. In the latter case, the VCO phase may initially increase (in an attempt to follow the spike) but returns to its initial value; a typical plot of $\hat{\varphi}_k$ might appear as in Fig. 3.7-4 . Notice that $\hat{\varphi}_k$ contains a spike. The output, being proportional to the derivative of the VCO phase, contains a doublet, as shown in Fig. 3.7-4. Notice, that in order to convert a spike into a doublet, the DPLL must "slip a cycle", which is to say that the input phase and VCO phase differ by 2π. This, of course, has no
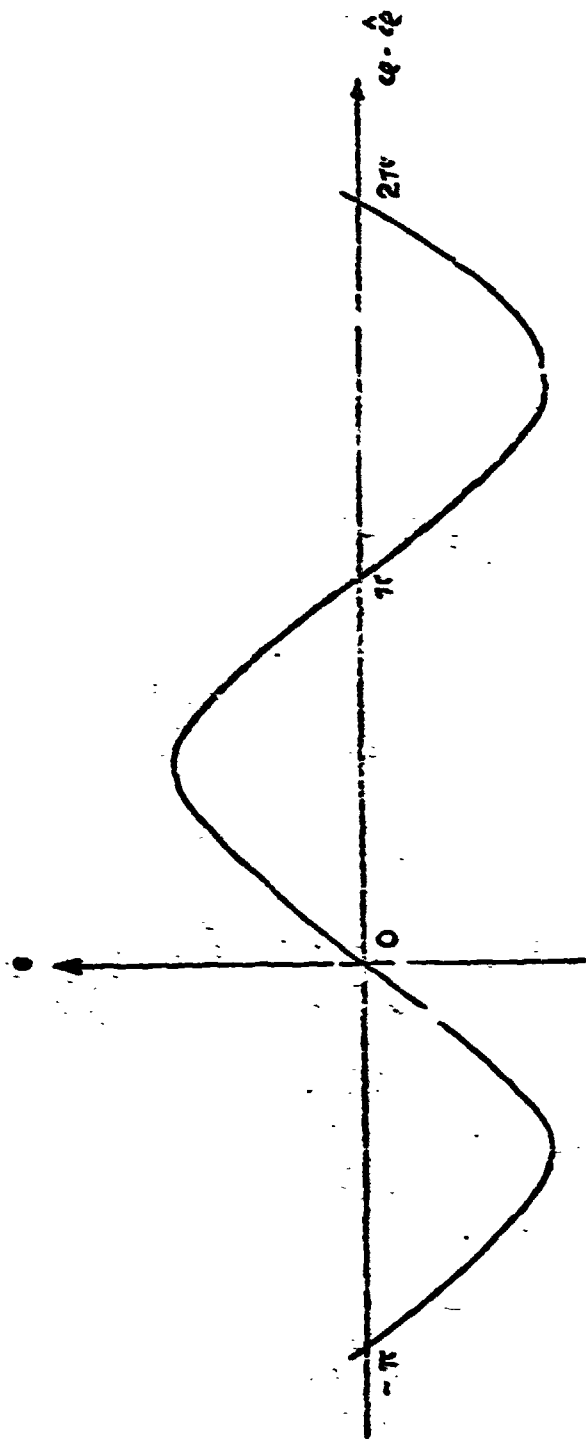
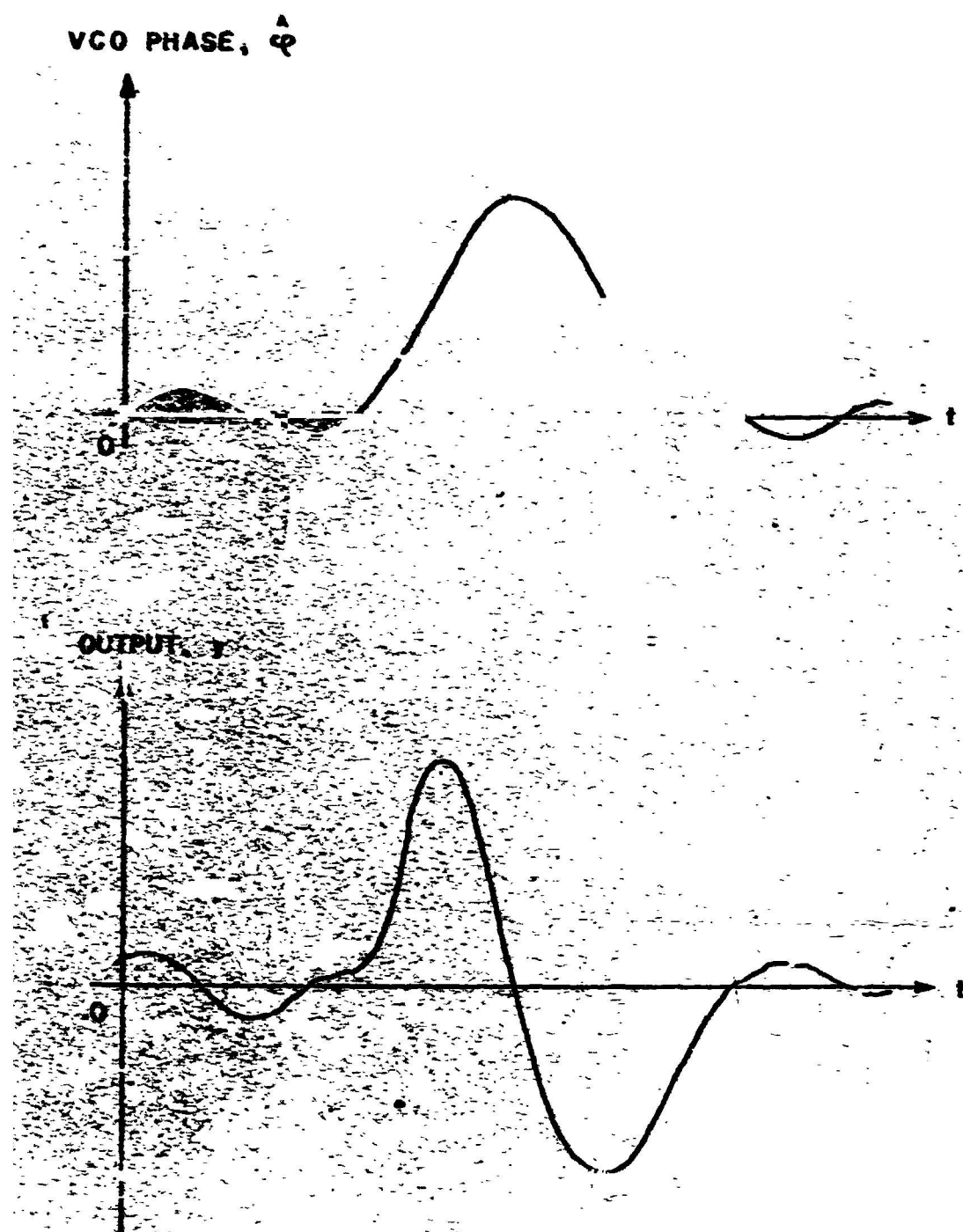Fig. 3.7-3. The phase detector characteristic of a phase-locked loop.

VCO PHASE, $\overset{\wedge}{\varphi}$

OUTPUT, y

Fig. 3.7-4. The VCO phase, $\overset{\wedge}{\varphi}$, and DPLL output, y, when the DPLL converts an input noise spike into a doublet.

effect upon the loop operation as the phase detector characteristic is periodic, with period 2π.

We therefore would like to determine how the first order DPLL responds to input noise spikes. To this end we introduce a deterministic model for the input phase during a spike: φ_k shall increase from 0 to 2π in T_{spike} seconds in a sinusoidal manner:

$$\varphi_{spike}(t) = \pi(1 - \cos \pi t/T_{spike}), \quad 0 \leq t \leq T_{spike} \quad (3.7-21)$$

illustrated in Fig. 3.7-5a. In addition, we let the input carrier amplitude decrease, also in a sinusoidal manner:

$$A_{spike}(t) = (A+\epsilon)/2 + [(A-\epsilon)/2]\cos 2\pi t/T_{spike} \quad (3.7-22)$$

for $0 \leq t \leq T_{spike}$, where ϵ is the minimum amplitude. This amplitude variation is illustrated in Fig. 3.7-5b. Hence, when a spike occurs, the expression for the input is

$$x_k = -A_{spike}(kT_s)\cos[k\pi/2m + \varphi_k + \varphi_{spike}(kT_s)] \quad (3.7-23)$$

A spike is most likely to occur when the modulation deviates the carrier to one extreme of the IF bandwidth, as all the noise components have a larger (or smaller) frequency than the deviated carrier. We shall consider sinusoidal modulation:

$$\varphi_k = \beta \sin 2\pi k f_m/f_s \quad (3.7-23)$$

where
$$f_m = \text{modulating frequency}$$
$$\beta = \text{modulation index}$$

The instantaneous frequency is a maximum $(\beta f_m = \Delta f)$ at $k = 0$; therefore we introduce a negative spike at $k = 0$. In accordance with the first order design values, we choose $\Delta f = 600$ Hz and consider $f_m = 200$ Hz, $\beta = 3$. Then
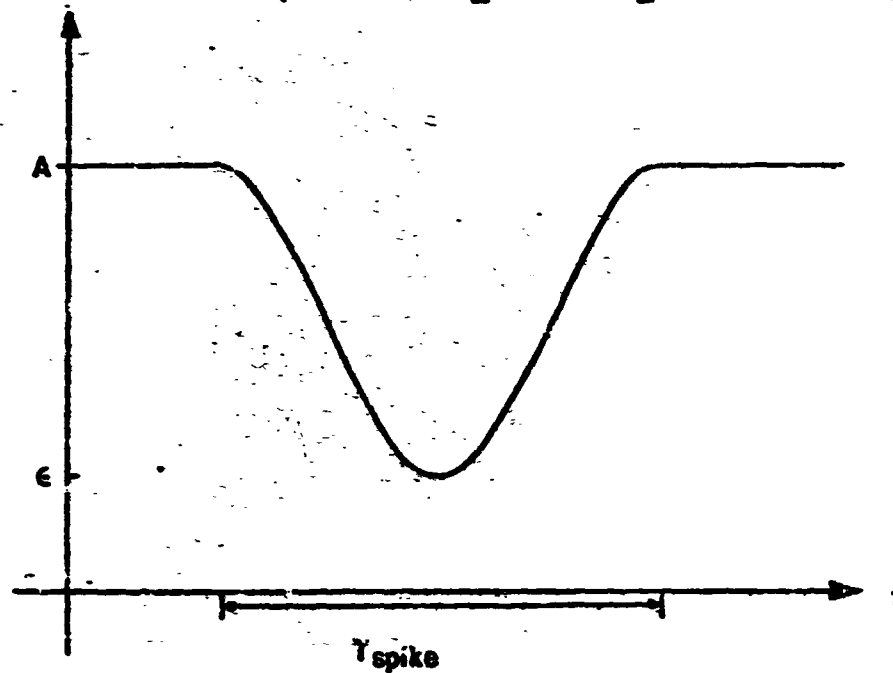
$$B_{IF} = 2(3 + 1)200 = 1600 \text{ Hz} \quad (3.7-24)$$

$$\varphi_{spike}(t) = (1 - \cos \pi t / T_{spike})$$

2π

T_{spike}

t
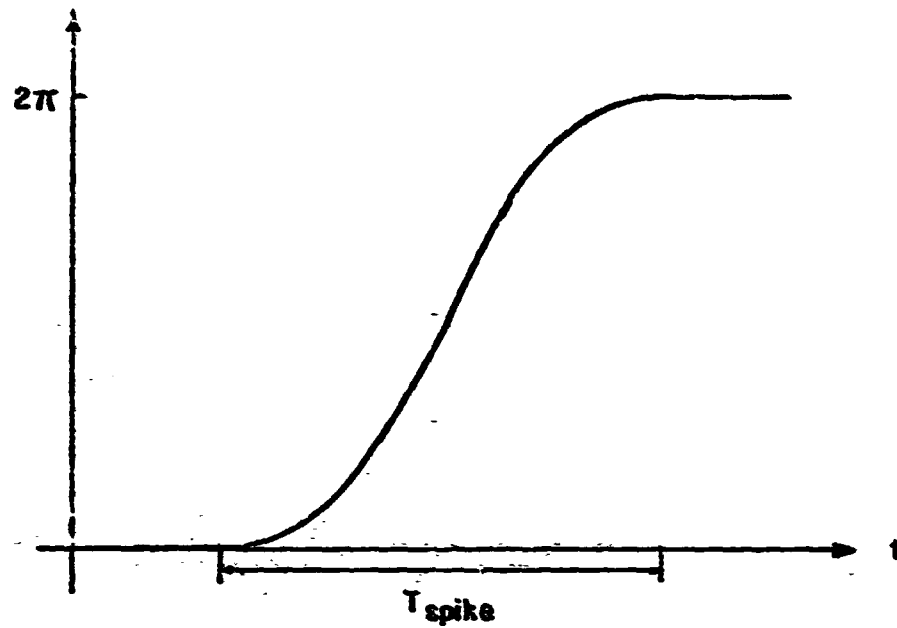
(a)

INPUT AMPLITUDE, $A_{spike}(t) = \dfrac{A+\epsilon}{2} + \dfrac{A-\epsilon}{2} \cos 2\pi t / T_{spike}$

A

ϵ

T_{spike}

t

(b)

Fig. 3.7-5. The deterministic spike model: (a) phase variation; (b) amplitude variation.

and

$$T_{spike} \approx 1/1600 = 0.625 \text{ ms} . \qquad (3.7\text{-}25)$$

In terms of the sampling period $(T_s = 20 \mu\text{sec})$ this is

$$T_{spike} \approx .625 \text{ ms} /20 \mu\text{sec} = 31 \text{ samples} \qquad (3.7\text{-}26)$$

The input phase plus the negative spike is illustrated in Fig 3.7-6 for the above parameters.

Before we examine the DPLL response to the spike, we first examine the DPLL response to the sinusoidal modulation alone so that we have a basis for comparison. Fig. 3.7-7 is the VCO phase, $\hat{\varphi}_k$, obtained by a computer solution of the DPLL difference equation:

$$\hat{\varphi}_{k+1} = \hat{\varphi}_k - (\pi/10)\cos(k\pi/8 + \varphi_k)\, \text{Sq}\,(k\pi/8 + \hat{\varphi}_k) \qquad (3.7\text{-}27)$$

with

$$\varphi_k = 3 \sin 2\pi\, 200\, k / 50,000$$

The solution is generated by starting at $k = -250$ with $\hat{\varphi}_{-250} = 0$, and is printed out beginning at $t = 0$, so that the transient time is one complete cycle of the modulation. The distortion present is attributable to two facts: first, the teleprinter can space only an integral number of spaces; second, we are looking at the unfiltered solution to Eq. (3.7-27) which contains the harmonics generated by the square wave VCO. Despite this distortion, it is clear that the DPLL is following the sinusoidal modulation.

The sinusoidal modulation plus noise spike is now introduced to the DPLL, and the solution for $\hat{\varphi}_k$ is found and plotted using the program of Fig. 3.7-8. The programming language is FOCAL [18] and the program was run on a PDP-8 minicomputer. Computer variables correspond to equation variables according to Table 3.7-1. The program is rather straightfoward: lines 2.05 to 2.15 compute the error signal with or without the spike (the proper case being determined by line 2.05), line 2.20 updates the VCO
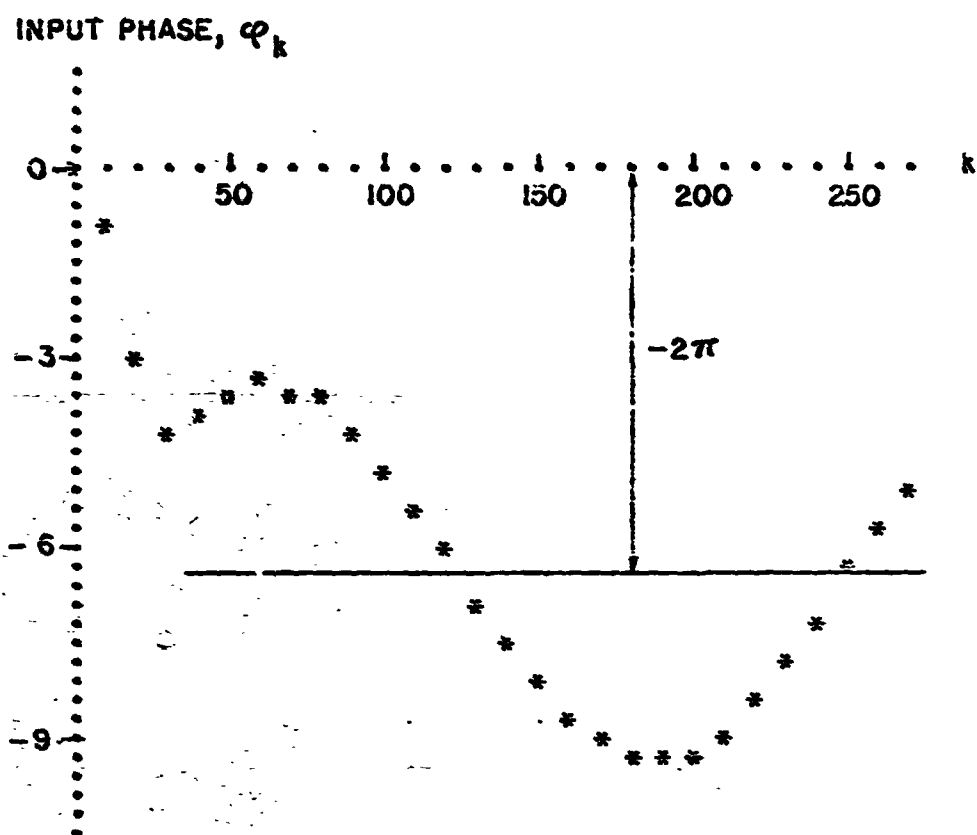
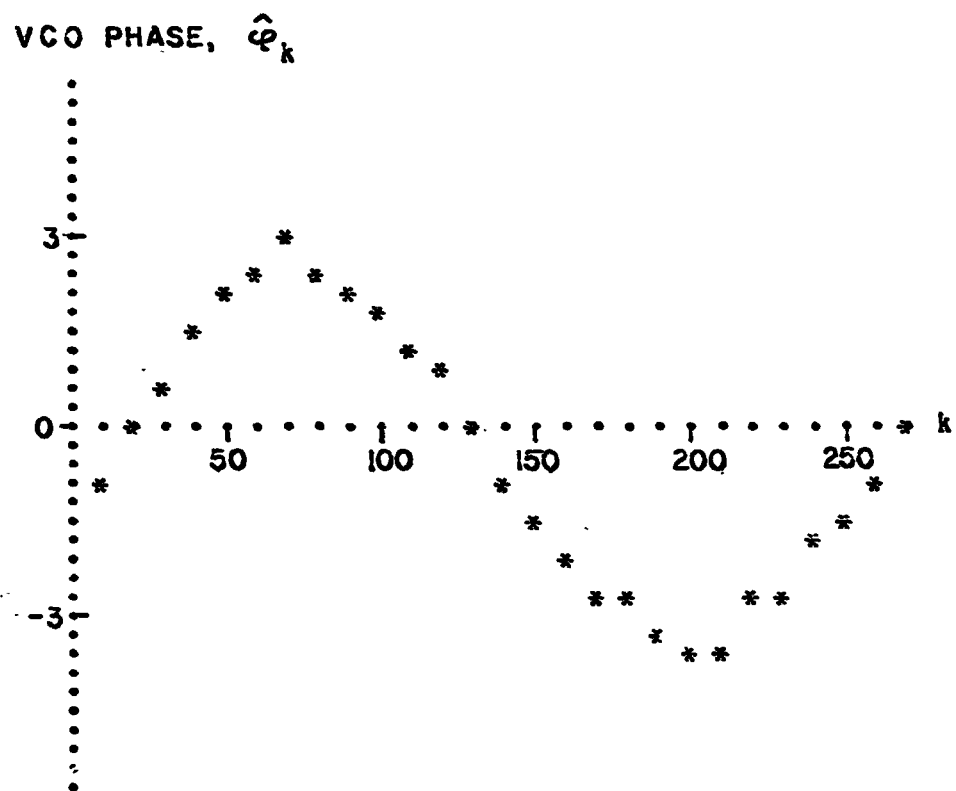Fig. 3.7-6. The input sinusoidal phase plus a 32-sample spike.

VCO PHASE, $\hat{\varphi}_k$

Fig. 3.7-7. First order DPLL respor to sinusoidal modulation.

```
C-FOCAL,1969

01.05 A T,F
01.10 S W=3.14159;S G=W/5*2+2;S PK=0
01.15 F K=-250,1,270;DO 2
01.20 QUIT
       .

02.05 S H=3*FSIN(2*W*200*K/50000);I (K*<T-K>)2.15
02.10 S EK=<2+F>/2+<2-F>*FCOS(2*W*K/T)/2
02.11 S PK=-EK*FCOS(K*W/8+H-W*(1-FCOS<W*K/T>))
02.12 S EK=EK*FSGN(FSIN<K*W/8+PK>);GOTO 2.2
02.15 S EK=-2*FCOS(K*W/8+H)*FSGN[FSIN<K*W/8+PK>]
02.20 S PK=PK+G*EK
02.25 I (K 2.9,2.3,2.35
02.30 F X=0,1,60;T "."
02.31 T #
02.35 I (K/10-FITR(K/10))2.9,2.4,2.9
02.40 F X=0,1,FITR(40+<10/3>*PK);T " "
02.45 T "*",#;F X=0,1,40;T " "
02.50 T ".",!
02.90 C
*
```

Fig. 3.7-8. FOCAL program for solving the first order DPLL equation
with sinusoidal modulation plus an input noise spike.

Program Variable	Equation Variable
T	Spike duration, T_{spike}
E	Minimum carrier amplitude, ϵ
W	π
G	Loop gain, G
H	Input phase, φ_k
EK	Error signal, e_k
P.	VCO phase, $\hat{\varphi}_k$

Table 3.7-1. Correspondence between the variables appearing in the computer program of Fig. 3.7-8 and the DPLL equation variables.

phase, and lines 2.30 through 2.90 are the plotting subroutine for plotting every tenth computed value.

First, a spike having no amplitude variation ($\epsilon = A = 2$) is introduced. The result, shown in Fig. 3.7-9 clearly shows that the DPLL follows the input spike, and therefore the DPLL output contains a spike. If the input amplitude is allowed to drop, the DPLL still follows the spike, as illustrated in Fig. 3.7-10 where $\epsilon = 0.5$. Decreasing ϵ further, the DPLL suppresses the spike, as evidenced by Fig. 3.7-10 where $\epsilon = 0.2$. In general, we expect that as ϵ decreases, it becomes easier for the DPLL to suppress the input spike, because the gain of the DPLL depends on the carrier amplitude. Furthermore, a loop with a small gain cannot respond quickly to the rapidly changing input phase when a spike is present. Notice also that when the spike appears, the input amplitude (and therefore the loop gain) drops precisely when the phase is changing most rapidly. Hence, in decreasing ϵ, we reach a point where the loop becomes sluggish enough and cannot follow the spike.

If a wider spike (larger T_{spike}) is introduced we expect the DPLL to follow it, as this slower spike will be within the dynamic capability of the loop. For example, let us introduce a 40-sample spike having $\epsilon = 0.2$. Although the DPLL did not follow the corresponding 22-sample spike, Fig. 3.7-12 shows that widening the spike allows the DPLL to follow it: in a sense, the DPLL has more time to follow the phase change, even though its gain may drop.

In conclusion, then, the analysis using the above noise spike model shows that we should not expect any threshold improvement by the first order DPLL over the conventional discriminator. It is for the second and third order DPLL's where we have more degrees of freedom available (i.e., additional loop gains to adjust) that we expect to obtain threshold improvement.
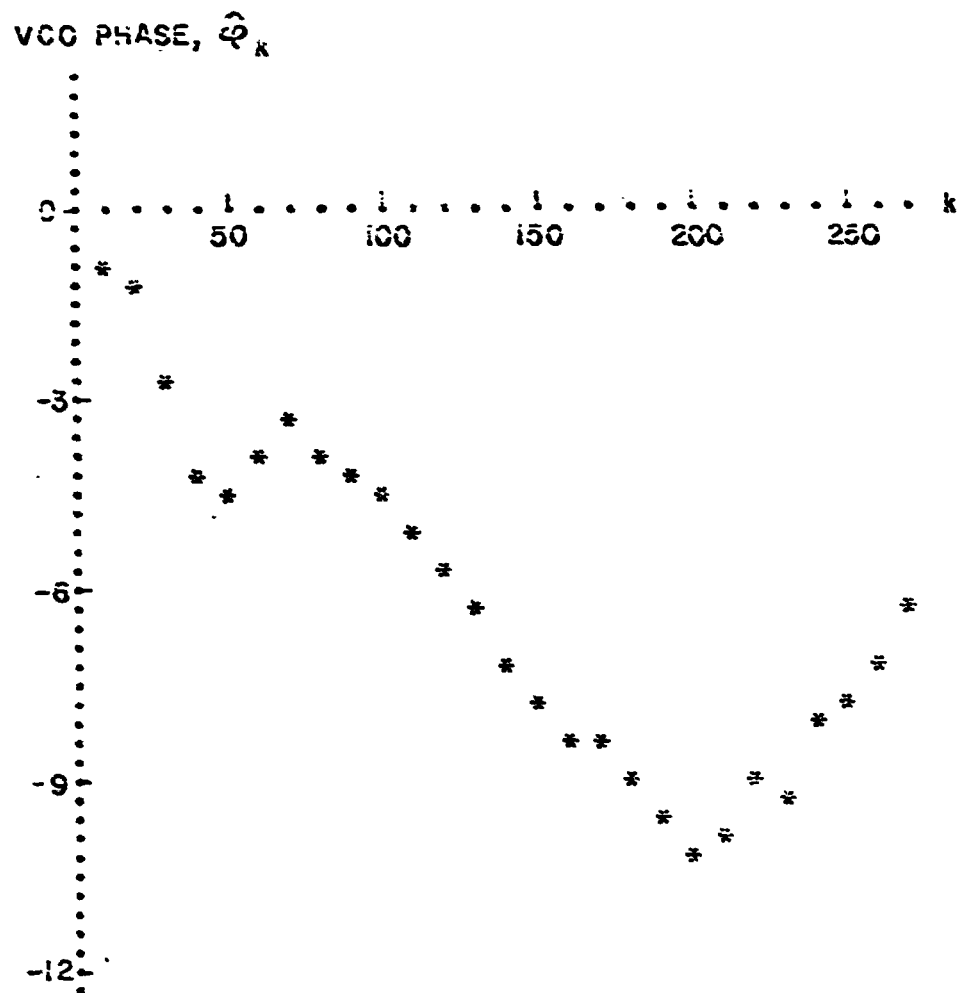
Fig. 3.7-9. First order DPLL response to sinusoidal modulation plus. a 32-sample, constant amplitude spike.
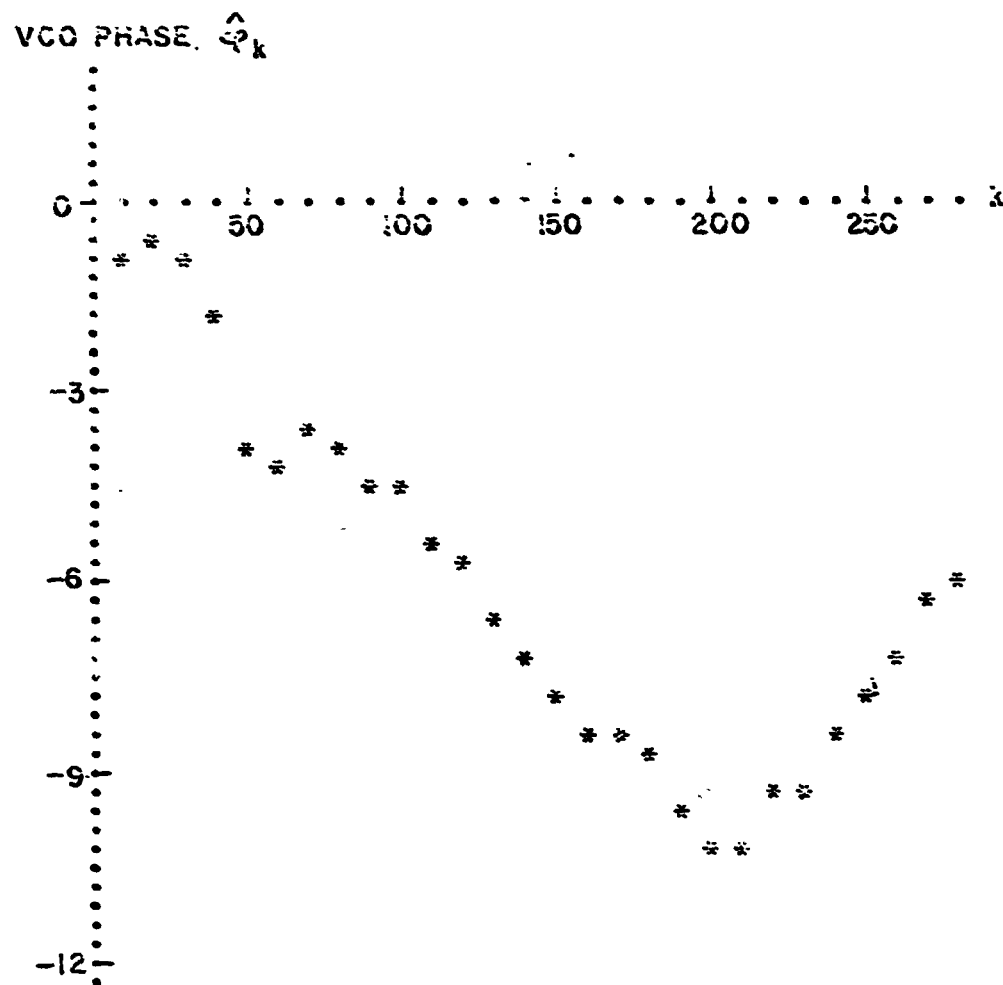
89

Fig. 3 ΄ - ΄0. First order DPLL response to sinusoidal modulation plus a 32-sample, 0.5 minimum amplitude spike.
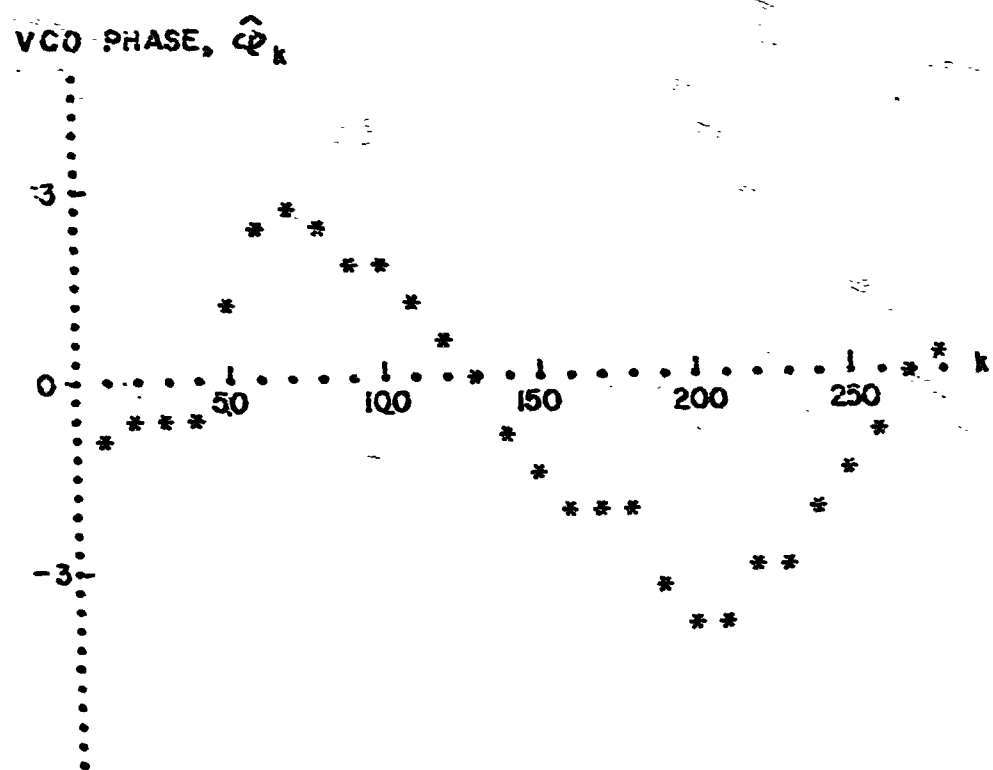
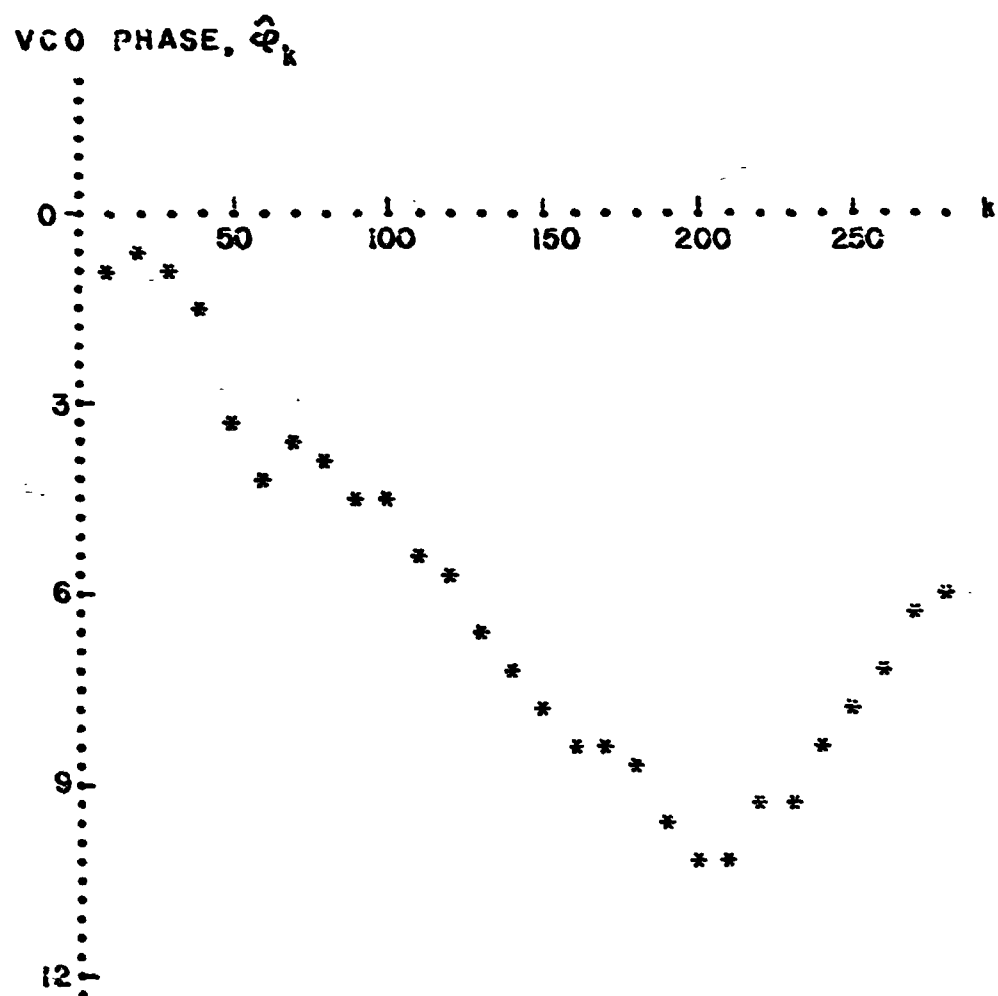Fig. 3.7-11. First order DPLL response to sinusoidal modulation plus a 32-sample, 0.2 minimum amplitude spike.

Fig. 3.7-12. First order DPLL response to sinusoidal modulation plus
a 40-sample, 0.2 minimum amplitude spike.

5.2.4 Harmonic Noise

Besides the thermal and quantization noise, another noise contribution, generated by the VCO square wave harmonics, appears at the output of the DPLL. Recall that the sampling frequency is related to the carrier via

$$(n + 1/4m)f_s = f_0$$

where
$$f_s = \text{sampling frequency}$$
$$f_0 = \text{carrier frequency}$$
$$n, m = \text{integers}$$

Therefore, the carrier frequency is shifted to the frequency $f_s/4m$. The VCO square wave contains odd harmonics, which are shifted to the frequencies

$$f_s/4m, \ 3f_s/4m, \ 5f_s/4m, \ldots, \ (2p+1)f_s/4m, \ldots$$

with p an integer. The phase error signal which is the product of input and VCO signals contains the sum and difference frequencies, located at

$$0, \ f_s/2m, \ 2f_s/2m, \ 3f_s/2m, \ldots, \ qf_s/2m, \ldots$$

with q an integer. Only the term at 0 Hz contains any useful information, namely a quantity proportional to the phase difference between input and VCO. The design equation developed in Sec. 2.6 guaranteed that the next term, at $f_s/2m$ Hz, falls outside the DPLL bandwidth. However, since the sampling frequency is equivalent to zero frequency, the term with $q = 2m$ is the first to fall into the DPLL bandwidth, and contributes to the output noise. This term does not affect the VCO operation (as argued when developing the linearized model in Sec. 2.7) but does contribute output noise which we label harmonic distortion.

To calculate the harmonic distortion, we must go back to the VCO and find the harmonic terms which generate the distortion. There are two such

harmonics, the $(4m-1)^{st}$ and the $(4m+1)^{st}$; the sum of the $(4m-1)^{st}$ harmonic and the carrier frequency is a distortion term, while the difference of the $(4m+1)^{st}$ harmonic and carrier is also a distortion term. These harmonics appear explicitly in the square wave Fourier series as

$$Sq(x) = \frac{4}{\pi}\left[\sin x + \cdots + \frac{1}{4m-1}\sin(4m-1)x + \frac{1}{4m+1}\sin(4m+1)x + \cdots\right]$$

$$(3.7-28)$$

and we have

$$-2\cos(k\pi/2m + \varphi_k)\, Sq(k\pi/2m + \hat{\varphi}_k)$$

$$= \frac{4}{\pi}\sin(\varphi_k - \hat{\varphi}_k) + \cdots$$

$$-\frac{4}{\pi}\frac{1}{4m-1}\sin[(4m-1)\hat{\varphi}_k + \varphi_k]$$

$$-\frac{4}{\pi}\frac{1}{4m+1}\sin[(4m+1)\hat{\varphi}_k - \varphi_k] + \cdots \qquad (3.7-29)$$

Hence the distortion terms are

$$D = \frac{4}{\pi}\frac{1}{4m-1}\sin[(4m-1)\hat{\varphi}_k + \varphi_k]$$

$$+ \frac{4}{\pi}\frac{1}{4m+1}\sin[(4m+1)\hat{\varphi}_k - \varphi_k] \qquad (3.7-30)$$

The exact amount of distortion observed at the DPLL output (the output of the low pass filter) depends on the modulation (φ_k). We consider the case of constant modulation (a frequency deviation from the carrier) and sinusoidal modulation.

If the input signal is deviated from the carrier by Δf Hz, then the input phase φ_k is given by

$$\varphi_k = k\, 2\pi\Delta f/f_s \qquad (3.7-31)$$

Using the linearized model of Fig. 3.7-1, we conclude that the first order DPLL tracks this deviation with a lag in phase:

$$\hat{\phi}_k = \phi_k - 2\pi \Delta f / (4/\pi) f_s G \qquad (3.7-32)$$

with G, the loop gain. Hence this distortion terms are

$$D = \frac{4}{\pi} \frac{1}{4m-1} \sin\left[k\, 2\pi 4m\, \Delta f/f_s - (4m-1)\, 2\pi\, \Delta f/(4/\pi) f_s G\right]$$

$$+ \frac{4}{\pi} \frac{1}{4m+1} \sin\left[k\, 2\pi 4m\, \Delta f/f_s - (4m+1)\, 2\pi\, \Delta f/(4/\pi) f_s G\right] \qquad (3.7-33)$$

We observe that when the input is a frequency deviation, Δf Hz, the harmonic distortion is at the frequency $4m\,\Delta f$ Hz. Its amplitude is bounded by

$$|D| \le \frac{4}{\pi} \frac{8m}{16m^2 - 1} \qquad (3.7-34)$$

and its power is bounded by

$$N_D \le 20\log \frac{1}{\sqrt{2}} \frac{4}{\pi} \frac{8m}{16m^2 - 1} \qquad dB \qquad (3.7-35)$$

Now the noise in Eq. (3.8-35) will not necessarily be found at the low pass filter output since the frequency $4m\,\Delta f$ Hz may fall outside the filter passband. The filter is set to the maximum modulating frequency, $f_m = (\Delta f)_{max}/\beta$, and therefore Eq. (3.7-35) does not apply if

$$\Delta f > f_m/4m \qquad (3.7-36)$$

For example, if we are working with $f_m = 200$ Hz, $(\Delta f)_{max} = 600$ Hz, and $m = 4$, then only frequency deviations less than $200/16 = 12.5$ Hz contribute harmonic distortion as per Eq. (3.7-35). This is not to say that frequency deviations greater than 12.5 Hz contribute no distortion at all; they do contribute but not as a result of the $4m \pm 1$ VCO harmonics. If we tabulate the harmonics generated by the multiplier, eventually we find one that folds down into the f_m baseband, and since the VCO harmonic amplitudes decrease as $1/n$, the noise contribution will certainly be within the bound of Eq. (3.7-35).

Next, consider sinusoidal modulation with modulating frequency f_m

and modulation index β:

$$\varphi_k = \beta \sin k \, 2\pi f_m/f_s \quad . \tag{3.7-37}$$

According to the linearized loop the VCO phase is sinusoidal:

$$\varphi_k = A \sin(k \, 2\pi f_m/f_s + \alpha) \tag{3.7-38}$$

where

$$A e^{j\alpha} = \beta \left. \frac{4G/\pi}{1 - (1 - 4G/\pi)z^{-1}} \right|_{z = e^{j \, 2\pi f_m/f_s}} \tag{3.7-39}$$

The harmonic distortion terms are

$$D = \frac{4}{\pi} \frac{1}{4m-1} \sin[(4m-1)A \sin(k \, 2\pi f_m/f_s + \alpha) + \beta \sin k \, 2\pi f_m/f_s]$$

$$+ \frac{4}{\pi} \frac{1}{4m+1} \sin[(4m+1)A \sin(k \, 2\pi f_m/f_s + \alpha) + \beta \sin k \, 2\pi f_m/f_s] \tag{3.7-40}$$

Now $f_m \ll f_s$ so that in Eq. (3.7-39), $z \approx 1$ and $A \approx \beta$, $\alpha \approx 0$ and the distortion is approximately given by

$$D \approx \frac{4}{\pi} \frac{8m}{16m^2 - 1} \sin(4m\beta \sin k \, 2\pi f_m/f_s) \tag{3.7-41}$$

It follows that the harmonic distortion contains odd harmonics of the modulating tone. The amplitude of the fundamental frequency (f_m) is negligible in comparison to the signal amplitude. The $(2n+1)^{st}$ harmonic distortion is

$$D_{2n+1} \approx \frac{4}{\pi} \frac{8m}{16m^2 - 1} \, 2J_{2n+1}(4m\beta) \sin k \, 2\pi(2n+1) f_m/f_s \tag{3.7-42}$$

where J_p is a Bessel function of order p, and the corresponding noise is

$$N_{D_{2n+1}} \approx 20 \log \frac{1}{\sqrt{2}} \frac{4}{\pi} \frac{8m}{16m^2 - 1} \, 2J_{2m+1}(4m\beta) \quad \text{dB} \tag{3.7-43}$$

Again, we must be careful and remember that only those harmonic frequencies passed by the output filter will contribute to the output distortion.

Eq. (3.7-43) may be bounded by realizing that $4m\beta$ is large and using

asymptotic expression for the Bessel function:

$$J_n(x) \sim \frac{2}{\pi x} \cos(x - n\pi/2 - \pi/4) \qquad (3.7-44)$$

Hence $|J_n(x)| \leq \sqrt{2/\pi x}$ and

$$N_{D_{2n+1}} < 20 \log \frac{1}{\sqrt{2}} \frac{4}{\pi} \frac{8m}{16m^2-1} \frac{2}{\sqrt{\pi 2m\beta}} \qquad (3.7-45)$$

3.8 Experimental Results

The first order DPLL was tested and signal-to-noise curves obtained for sinusoidal and constant offset modulation for modulation indices of 3 and 10. The parameters used were:

$$\begin{aligned}
\text{sampling frequency, } f_s &= 50 \text{ KHz} \\
\text{loop gain,} \qquad .G &= \pi/20 \\
\text{frequency deviation, } \Delta f &= 600 \text{ Hz} \\
\text{carrier frequency, } \qquad f_o &= 55.125 \text{ KHz} \qquad (3.8-1)
\end{aligned}$$

The test facility is shown in Fig 3.8-1. The carrier amplitude is kept at 2 volts peak (input signal power = 3 dB). For constant modulation (a frequency deviation from the carrier) the distortion analyzer is not required and the output noise is measured at the filter output. (The Ballantine meter used does not respond to d.c.; hence its reading does not include the signal power.)

3.8.1 Generation of the IF Noise

In order to generate the IF noise, a special technique was employed. Ordinarily, one could "rectangular" band-pass filter a white noise source; however, it was difficult to build such a bandpass filter when $B_{IF} = 1600$ Hz (for $\beta = 3$) or $B_{IF} = 1320$ Hz (for $\beta = 10$) and $f_o = 53.125$ KHz, requiring $Q \sim 30$. The technique used explicitly generated the noise according to its bandpass representation

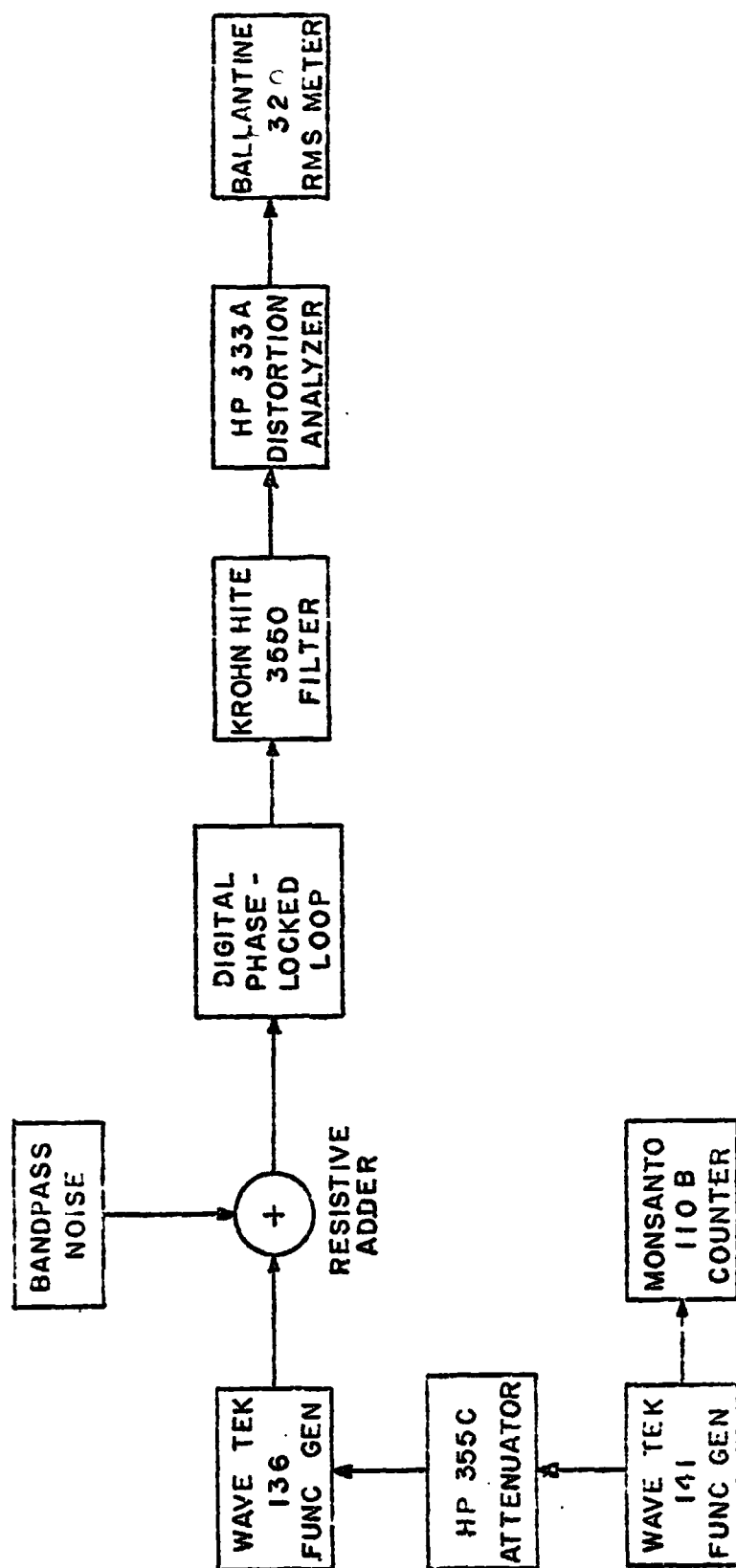$$n(t) = n_1(t) \cos 2\pi f_o t + n_2(t) \sin 2\pi f_o t \qquad (3.8-2)$$

Fig. 3.8-1. Test facility for obtaining signal-to-noise performance curves of the DPLL.

where $n_1(t)$ and $n_2(t)$ are independent white noise sources bandlimited to $B_D/2$ Hz and having equal power spectral densities. A block diagram illustrating the equipment used appears in Fig 3.8-2. A General Radio Gaussian white noise source is filtered using a four-pole filter to get $n_1(t)$; $n_2(t)$ is obtained similarly. Both $n_1(t)$ and $n_2(t)$ are then mu᠎ ᠎lied by carrier terms and the two products added using a resistive adder. The $90°$ phase shift between the two oscillators is guaranteed by synchronize᠎᠎ tion: the sync out signal of the Wave Tek 132 is precisely $90°$ out of phase with its output signal. When measurements were taken on the DPLL, the multiplier outputs were adjusted for equal power output.

3.8.2 Results for Constant Modulation

For the case of constant offset modulation the carrier is detuned by $\Delta f = 600$ Hz to 53.725 KHz. The output signal is constant and using the linearized model,

$$y_k = 2\pi\Delta f/f_s G = 0.48 \text{ volts}$$

which corresponds to the output signal power

$$S_o = 10 \log y_k^2 = -6.4 \text{ dB}$$

The output quantization noise is calculated from Eq. (3.7-18) and the results are:

$$\beta = 3, \quad N_q = -92.4 \quad \text{dB} \tag{3.8-3a}$$

$$\beta = 10, \quad N_q = -107.6 \quad \text{dB} \tag{3.8-3b}$$

The reason for these extremely low figures lies in the fact that we are using a 50 KHz sampling frequency on a signal bandlimited to 200 Hz (for $\beta = 3$). As a result of the mammoth oversampling, the quantization noise is undetectable. The question one wants to ask, then, is can the sampling frequency be reduced? In fact, reducing f_s provides more computation time. The answer lies in the design equation, Eq. (3.5-9), obtained
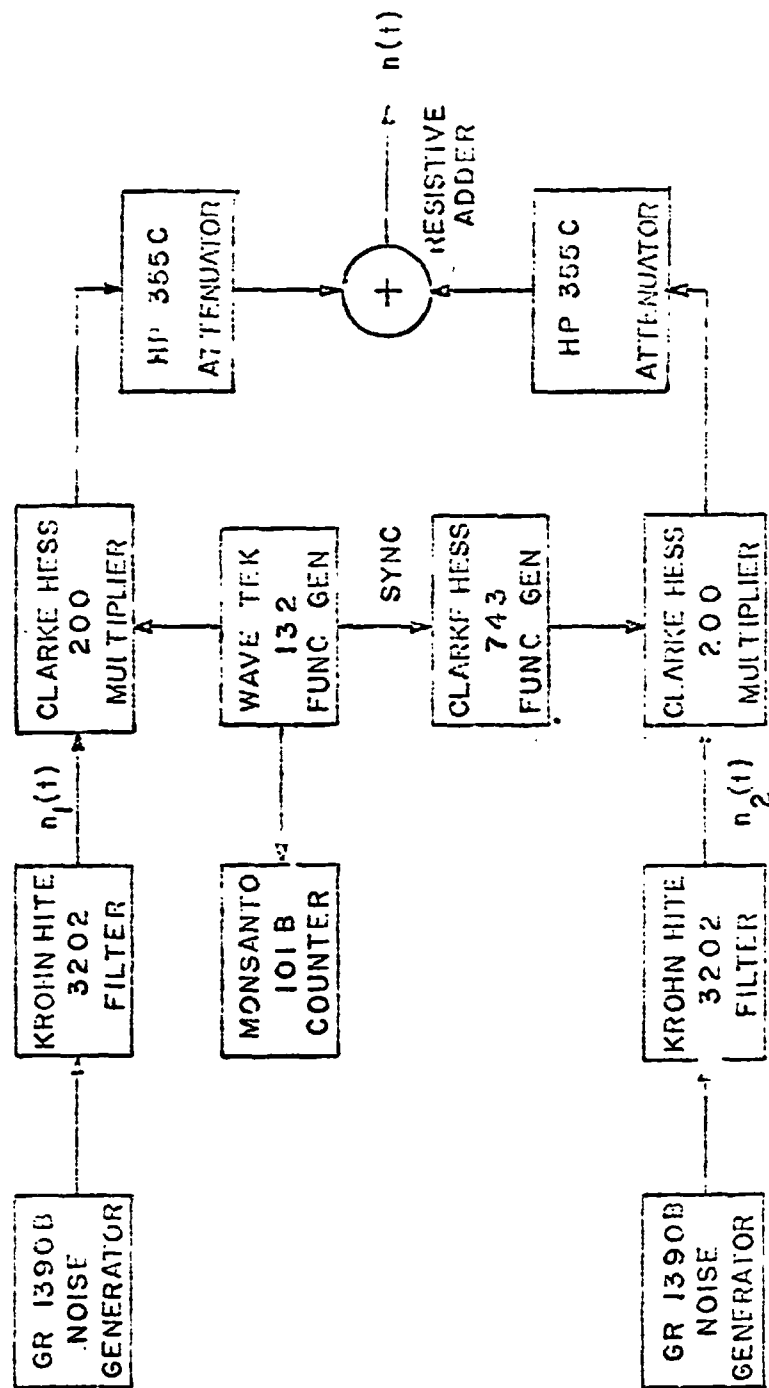
Fig. 3.8-2. Generation of the noise.

from considering the VCO harmonics:

$$m \leq f_s / 11.28 \, \Delta f \qquad (3.5\text{-}9)$$

One must pay a price for reducing f_s: either Δf or m must be reduced. Now with f_s = 50 KHz we are using Δf = 600 Hz and m = 4. Certainly we cannot reduce Δf significantly and reducing m results in distortion contributed by the VCO harmonics. So we use f_s = 50 KHz and conclude that the output signal-to-noise ratio will certainly not be limited by the quantization noise.

Figs. 3.8-3 and 3.8-4 are the experimentally obtained results for constant modulation with β = 3 and β = 10 respectively. The thermal noise curve $S_o/N_o = 3\beta^2 S_i / \eta f_m$ is superimposed in each case.

The first observation is that both curves level off as anticipated. For β = 3 the horizontal portion of the curve corresponds to N_o = -46.5 dB while for β = 10 we have N_o = -61.5 dB. As mentioned above, this is not due to quantization; it is due to the phase jitter between the carrier oscillator and the DPLL clock. This jitter was observed on the sampled carrier, whose sampled values are theoretically given by $x_k = -2 \cos k\pi/3$, a periodic sequence. The actual sequence obtained is not periodic as the phase jitter results in the sampled sequence $x_k = -2 \cos (k\pi/8 + \epsilon_k)$, with ϵ_k representing the jitter.

Using the measured output noise, we may calculate the oscillator jitter. Let the phase jitter sequence, ϵ_k, have a variance σ_ϵ^2, independent of k, and let the phase jitter be independent from sample to sample. Then assuming the D/A sequence "looks like" impulses to the output low pass filter, the power spectral density of the phase jitter is constant and given by

$$G_\epsilon = \sigma_\epsilon^2 / f_s$$

with f_s the sampling frequency. The linearized DPLL has the transfer function
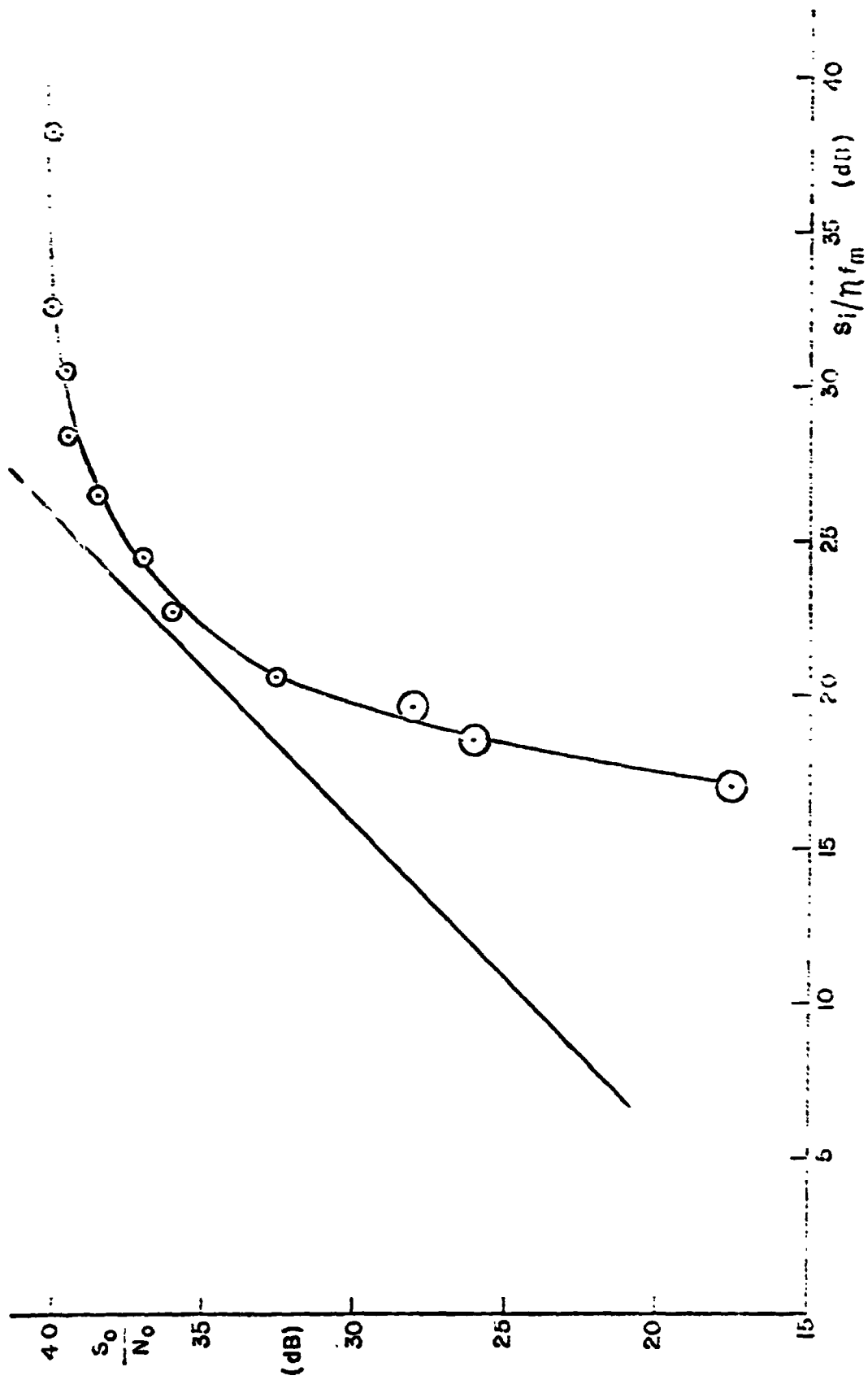
$$H(f) \approx 2\pi f / f_s G$$

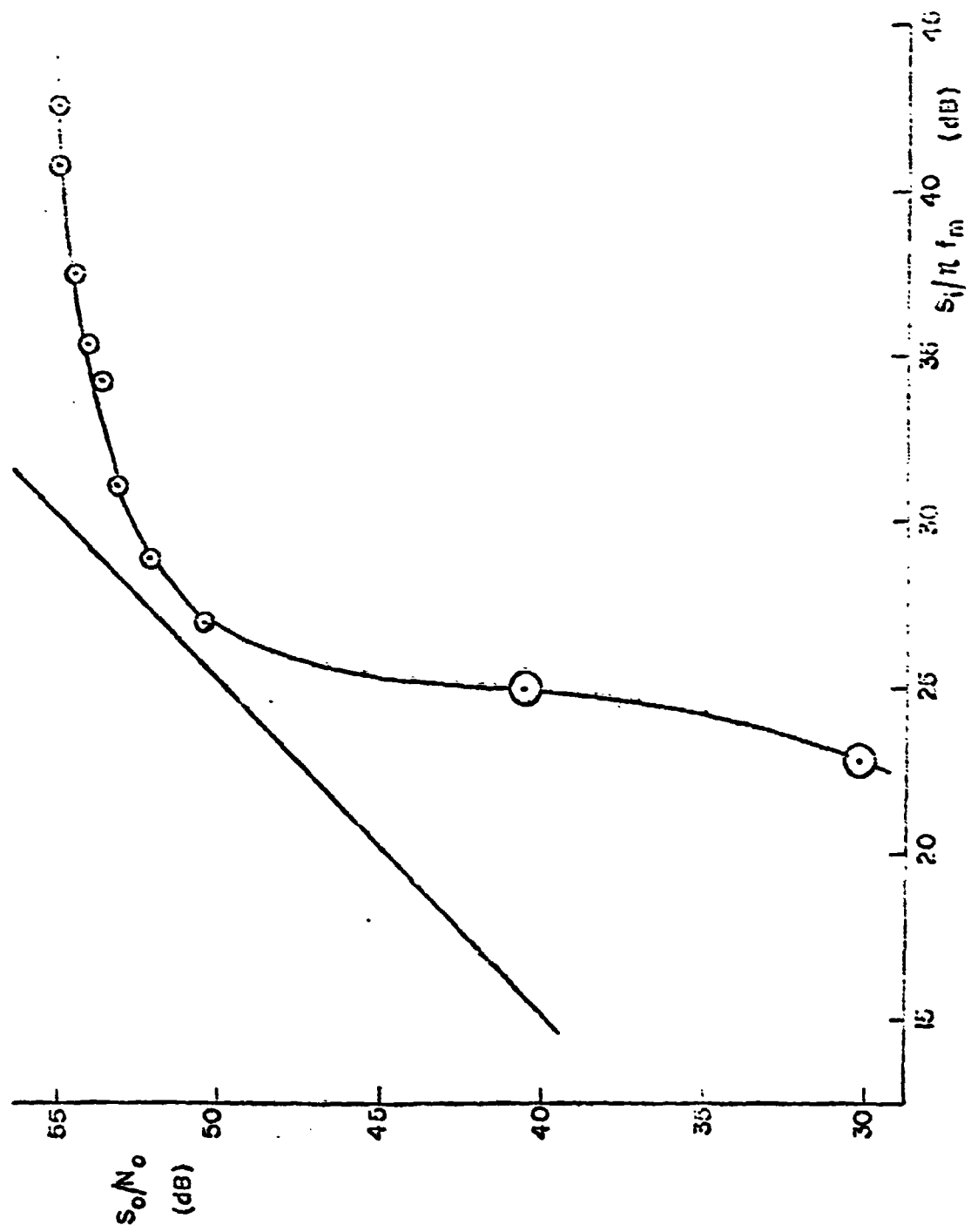Fig. 3.8-3. First order DPLL performance with constant offset modulation and $\beta = 3$.

Fig. 3.8-4. First order DPLL performance with constant offset modulation and $\beta = 10$.

where the approximation is valid for $|f| \ll f_m$. The output phase jitter noise is

$$X_j = \int_{-f_m}^{f_m} (2\pi f/f_s G)^2 (\sigma_\varepsilon^2/f_s) df = \frac{2}{3} \sigma_\varepsilon^2 \left(\frac{2\pi}{G}\right)^2 \left(\frac{f_m}{f_s}\right)^3$$

Using the measured value, $X_j = -46.5$ dB we find $\sigma_\varepsilon^2 = 0.34$ radian. This value is not caused simply by the phase jitter between the carrier oscillator and sampling clock, but also represents any input signal distortion from a true sinusoid.

In the laboratory the carrier oscillator was synchronized with the sampling frequency in an attempt to reduce the DPLL output noise. The synchronization procedure required dividing the sampling frequency by 16 via a counter, and extracting the seventeenth harmonic of the resulting square wave, thus insuring that $f_o = (1 + 1/16)f_s$. The effect of synchronization was a reduction in the output noise of 5 dB, which corresponds to a phase jitter variance of 0.11 radian. As mentioned above, even if it were possible to perfectly synchronize the carrier and sampling frequencies, any distortion in the sinusoidal nature of the carrier signal introduces an effective phase jitter, as the sampled values are in error from their theoretical values.

The synchronization hardware must be removed when the DPLL is tested with modulation, as it is impossible to both synchronize the carrier and modulate it simultaneously. In practice, the carrier frequency is derived using a narrow band, tracking phase-locked loop, and the sampling frequency derived from it.

The spectrum of the output jitter was determined experimentally by measuring the output power as a function of the low pass filter cutoff frequency. The result was that the output spectrum is parabolic which implies a white input spectrum, as the DPLL differentiates the input phase.

The second feature of the experimentally obtained curves is the location of threshold. For $\beta = 3$, threshold occurs when $S_i/\eta f_m = 21$ dB; for

$\beta = 10$, threshold is at 27 dB.

3.8.3 Results for Sinusoidal Modulation

The first order DPLL was tested with sinusoidal modulation $(\theta_k = \beta \sin k 2\pi f_m/f_s)$ with $\Delta f = 600$ Hz using $\beta = 3$ and $\beta = 10$, resulting in $f_m = 200$ Hz and 60 Hz respectively. The output signal is sinusoidal with amplitude A and phase α caluclated from the DPLL transfer function:

$$Ae^{j\alpha} = \beta \left. \frac{4/\pi}{1 + \frac{4}{\pi} G \frac{z^{-1}}{1 - z^{-1}}} \right| \quad z = e^{j 2\pi f_m/f_s} \tag{3.8-4}$$

For both $f_m = 200$ Hz and $f_m = 60$ Hz, we have

$$e^{j 2\pi f_m/f_s} \approx 1$$

and Eq. (3.8-4) yields

$$A \approx 2\pi \Delta f/f_s G = 0.48 \text{ volts} \tag{3.8-5}$$

The output signal power is

$$S_o = 10 \log A^2/2 \approx -9.4 \text{ dB} \tag{3.8-6}$$

which is 3 dB below the signal power for constant offset modulation. This is, of course, expected as with constant offset modulation the carrier is always deviated by Δf, while with sinusoidal modulation the carrier deviation is varying from $+ \Delta f$ to $- \Delta f$.

In the experimental setup the output low pass filter is set to f_m Hz. Hence the noise measured at the output does not include the third harmonic distortion generated by the VCO harmonics. Also, this output filter attenuates the signal power an additional 3 dB so that the experimentally obtained signal power is $-9.4 - 3 = -12.4$ dB. Hence we expect the signal-to-noise curves to level off 6 dB below the corresponding curves for constant offset modulation, as the phase jitter noise is the same for both types of

modulation.

The experimental results are shown in Figs. 3.8-5 and 3.8-6 for $\beta = 3$ and $\beta = 10$ respectively. The curves level off at about 34 dB and 48 dB respectively, which are 6 dB and 7 dB below the corresponding curves for constant offset modulation, in good agreement with the anticipated 6 dB drop.

The values of $S_i/\eta f_m$ at which threshold occurs are 18 dB for $\beta = 3$ and 21 dB for $\beta = 10$. Threshold for $\beta = 3$ agrees closely with that of a discriminator [19] as expected from the computer results with simulated spikes. Also notice that with sinusoidal modulation, threshold occurs at a lower $S_i/\eta f_m$ value than with constant offset modulation. This is expected as the constant modulation keeps the carrier deviated to its maximum value where it is most susceptible to spikes. Sinusoidal modulation deviates the carrier to its maximum only momentarily, resulting in fewer input spikes at the same carrier-to-noise ratio. Hence we have fewer output spikes with sinusoidal modulation and threshold is improved.

3.8.4 Results Using a Three-Bit A/D Converter

The extremely small value for the calculated quantization noise prompts us to ask how the quantization step size affects the DPLL performance. We anticipate that the level portion of the signal-to-noise curve will remain unchanged, as the phase jitter noise due to the incoming signal will dominate the quantization noise. If the rest of the curve also remains unchanged, then we can greatly simplify the hardware required by reducing the number of registers, gates, adders, etc, needed.

However, decreasing the number of bits deteriorates the phase error signal. We are working with a maximum error signal of 0.48 volts; assuming this signal is uniformly distributed, the error signal power is -17.2 dB. Using ten bits, the step size is $10/2^{10} \approx 10$ mv. and the quantization noise is -50.8 dB. Changing to three bits brings the quantization noise up to -8.8 dB, and the phase error signal is now lost in the quantization
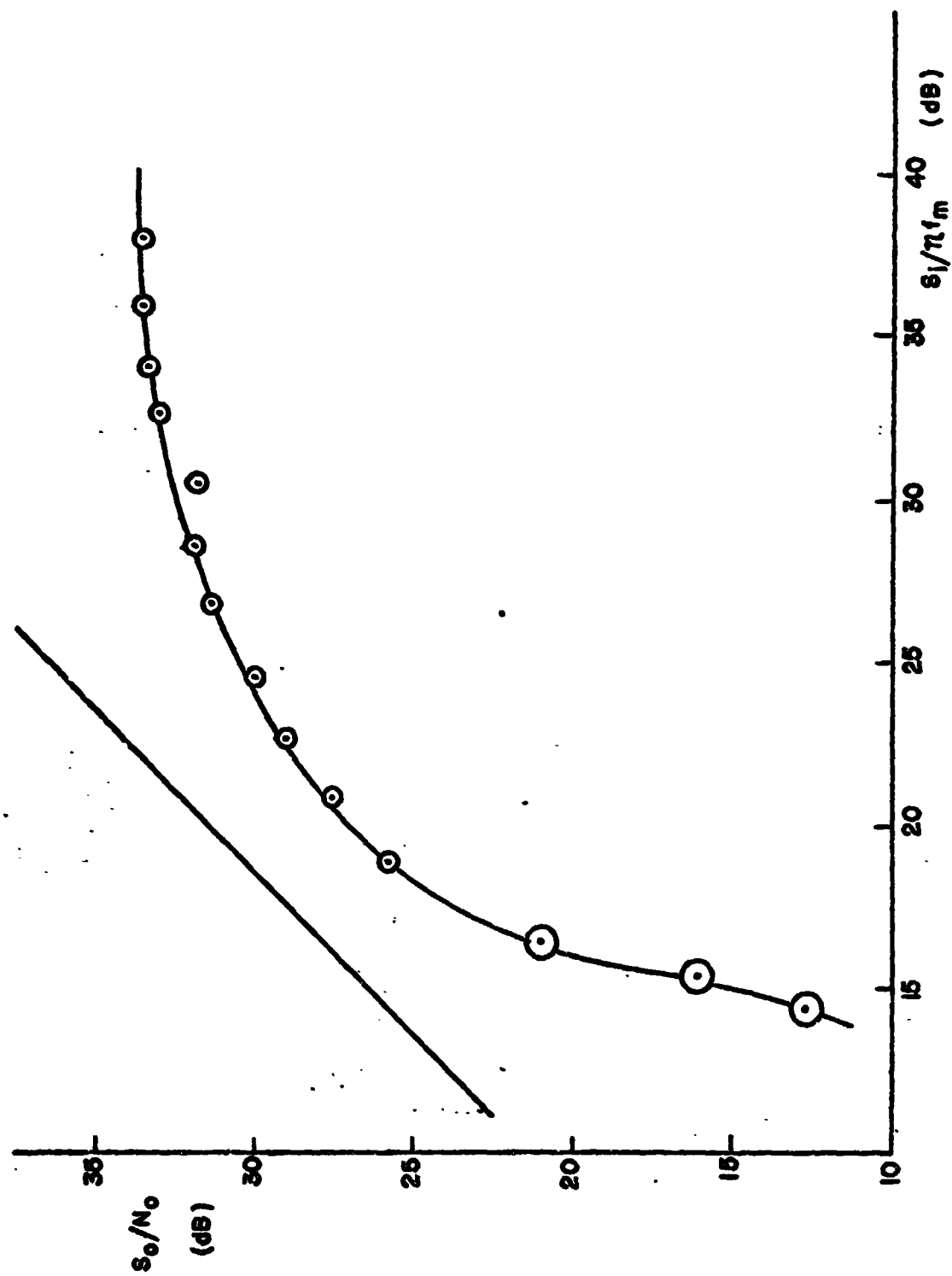
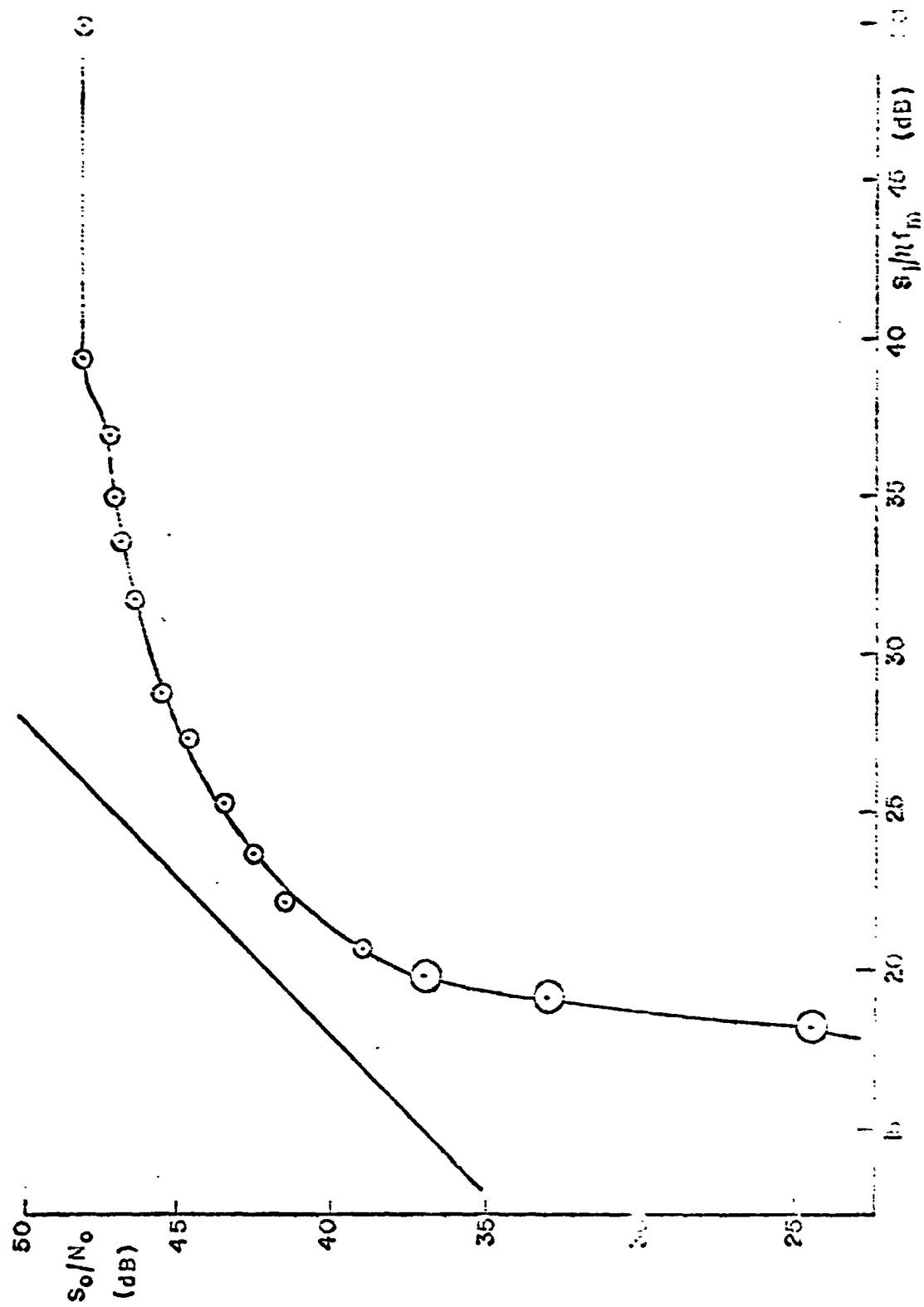Fig. 3.8-5. First order DPLL performance with sinusoidal modulation and $\beta = 3$.

Fig. 3.6-6. First order DPLL performance with sinusoidal modulation and $\beta = 10$.

noise.

The effect of the number of bits employed was determined exper-
imentally. The desired number of bits were taken from the A/D output
and the unused bits tied to the complement of the sign bit. Fig. 3.8-7
illustrates the DPLL performance using only three bits at the A/D con-
verter. (this is the smallest number we could use, as two bits would
provide only levels of ±2.5 v. and 0 v. Our carrier amplitude is 2 v.
and hence all sampled values would be truncated to 0 v. This repre-
sents a practical, not a theoretical problem.) The step size is now
$S = 10/2^3 = 1.25$ v. and the calculated output quantization noise is in-
creased by the factor $(2^7)^2 = 41$ dB to -51.4 dB. The quantization
noise plus the -47 dB jitter noise gives a total output noise of -45.8 dB;
the measured noise is -44.8 dB.

More important than the leveling off noise is the effect of the use of
fewer bits on the threshold performance. With 3-bit operation, threshold
occurs at 24 dB. which is 5 dB above the value for 10-bit operation.
Furthermore, this value is worse than that for a discriminator, indicating
that spikes appear at the output when no spikes are present at the input.
Observe from Fig. 3.8-7 that threshold occurs almost immediately as we
enter the thermal noise region--almost no 45° slope region exists. We
conclude that the large quantization noise in the phase error signal plus
the input thermal noise sufficiently perturb the phase error so as to cause
the DPLL to occasionally lose lock. The transient required to regain lock
produces a spike in the output, even though no spike was present at the
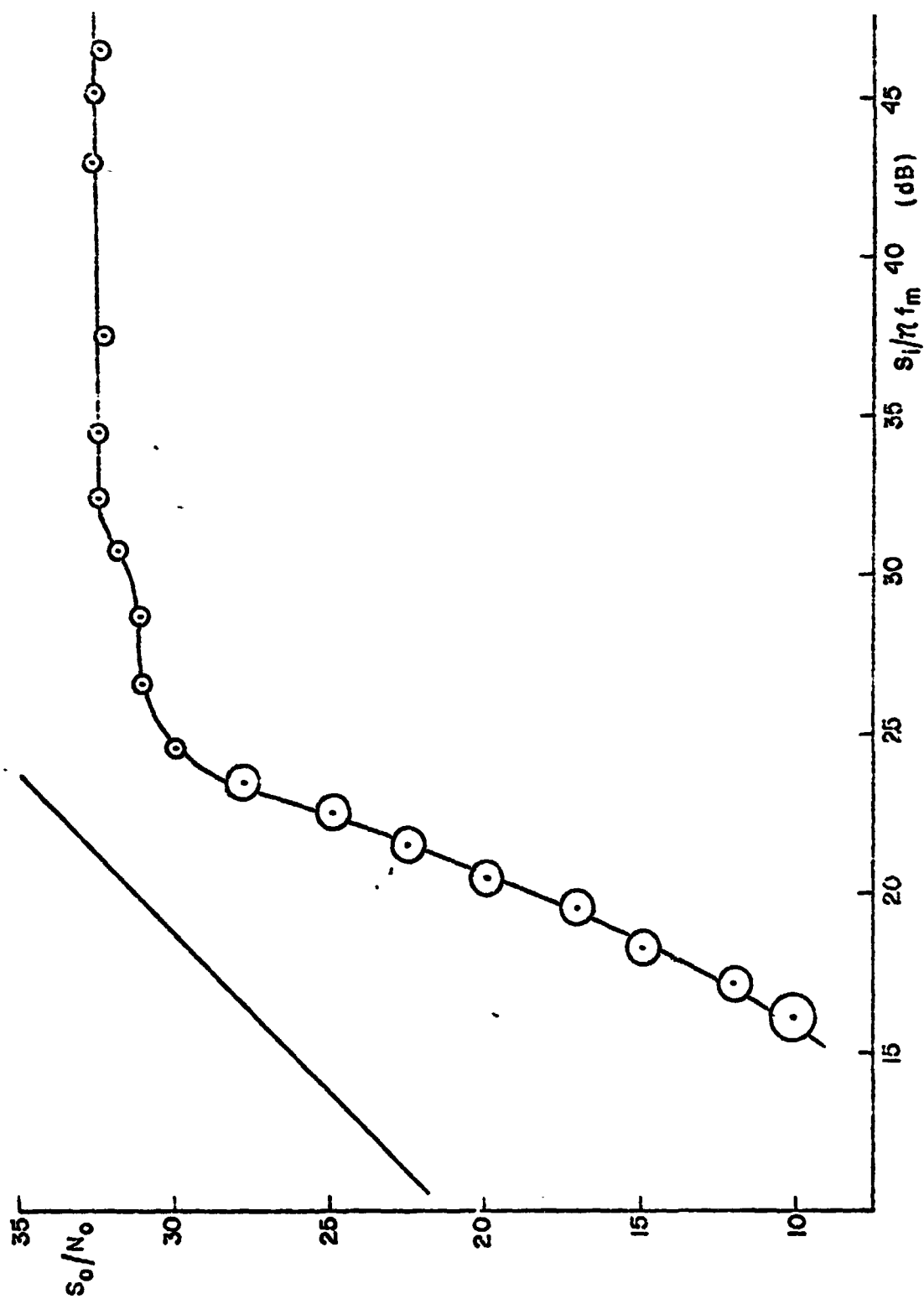input.

Fig. 3.8.7. First order DPLL performance with sinusoidal modulation, $\beta = 3$, and a three-bit A/D converter.

CHAPTER 4

THE SECOND ORDER DIGITAL PHASE-LOCKED LOOP

When an integration path is added to the foward loop filter of
the first order DPLL, a second order DPLL results. The additional in-
tegral path gives us an additional degree of freedom (the integral path
gain) so that we have more flexibility in designing the second order
DPLL to meet the design equations of Ch. 3 as well as to produce a
better spike response than the first order DPLL.

This chapter deals with the properties of a second order DPLL,
including the design procedure for determing the loop gains, the hard-
ware implementation, and the theoretical and experimental results.

4.1 Second Order DPLL Structure and Equation

The block diagram of the second order DPLL appears in Fig. 4.1-1.
The only difference between this and the first order DPLL is the integral
path present in the forward loop filter. This integrator is realized in a
way identical to the VCO integrator design (in fact, the second order
DPLL was implemented by time-sharing one integrator for both the VCO
and forward loop filter; the details are presented in Sec. 4.4); the pro-
portional plus integral filter is shown in Fig. 4.1-2. Representing the
Z-transforms of e_k and y_k by $E(z)$ and $Y(z)$ respectively, the transfer
function of this filter is

$$\frac{Y(z)}{E(z)} = g_1 + g_2 \frac{1}{1 - z^{-1}} \tag{4.1-1}$$

and the corresponding difference equation is

$$y_k = y_{k-1} + (g_1 + g_2)e_k - g_1 e_{k-1} \tag{4.1-2}$$

As with the first order DPLL, we have

$$e_k = (x_k + n_k) \, Sq(k\pi/2m + \phi_k) \tag{4.1-3a}$$
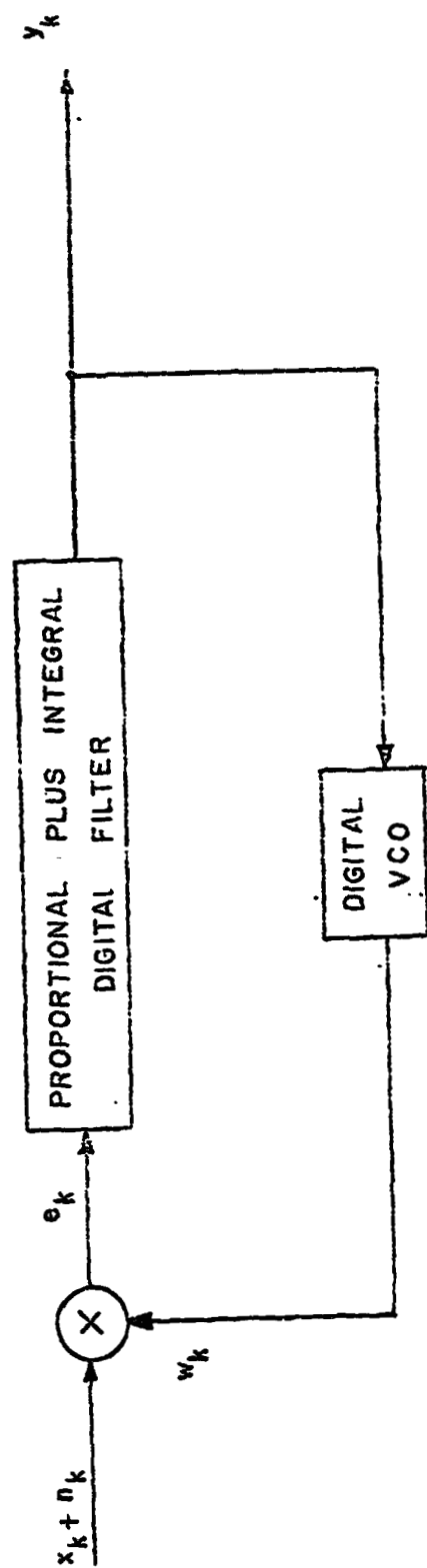
$$x_k = -2\cos(k\pi/2m + \varphi_k) \tag{4.1-3b}$$

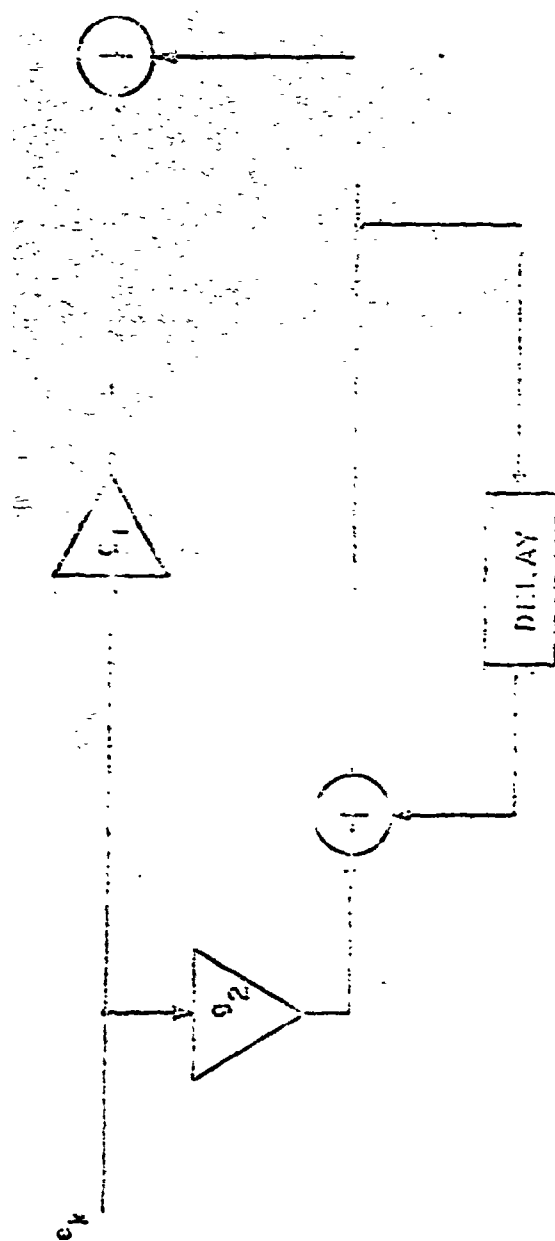Fig. 4.1-1. Block diagram of the second order digital phase-locked loop.

Fig. 6.1.1.2: The proportional plus integral digital filter; the proportional gain is c_1, the integral gain is c_2.

$$\hat{\phi}_{k+1} = \hat{\phi}_k + G_{VCO} y_k \qquad (4.1-3c)$$

where

$\cdot e_k$ = error signal

n_k = input IF noise

ϕ_k = input phase

$\hat{\phi}_k$ = VCO phase

G_{VCO} = VCO gain

Combining Eqs. (4.1-2) and (4.1-3) yields the equa   for the second order DPLL:

$$\hat{\phi}_{k+1} = 2\hat{\phi}_k - \hat{\phi}_{k-1}$$

$$- (G_1 + G_2) 2 \cos(k\pi/2m + \phi_k) \, Sq(k\pi/2m + \hat{\phi}_k)$$

$$+ 2G_1 \cos[(k-1)\pi/2m + \phi_{k-1}] \, Sq[(k-1)\pi/2m + \hat{\phi}_{k-1}]$$

$$+ (G_1 + G_2) n_k \, Sq(k\pi/2m + \hat{\phi}_k)$$

$$- G_2 n_k \, Sq[(k-1)\pi/2m + \hat{\phi}_{k-1}] \qquad (4.1-4)$$

where G_1 = proportional loop gain and G_2 = integral loop gain. As expected, this is a second order, nonlinear difference equation in $\hat{\phi}$, the VCO phase.

4.2 Stability Condition on the Linearized Model

When the phase difference between the input and VCO is small ($<< \pi/2$), the phase error is given by

$$e_k \approx (4/\pi)(\phi_k - \hat{\phi}_k) \qquad (4.2-1)$$

and the linearized model of Fig. 4.2-1 may be used. We shall use this model to find the restriction on the loop gains, G_1 and G_2, for stability.
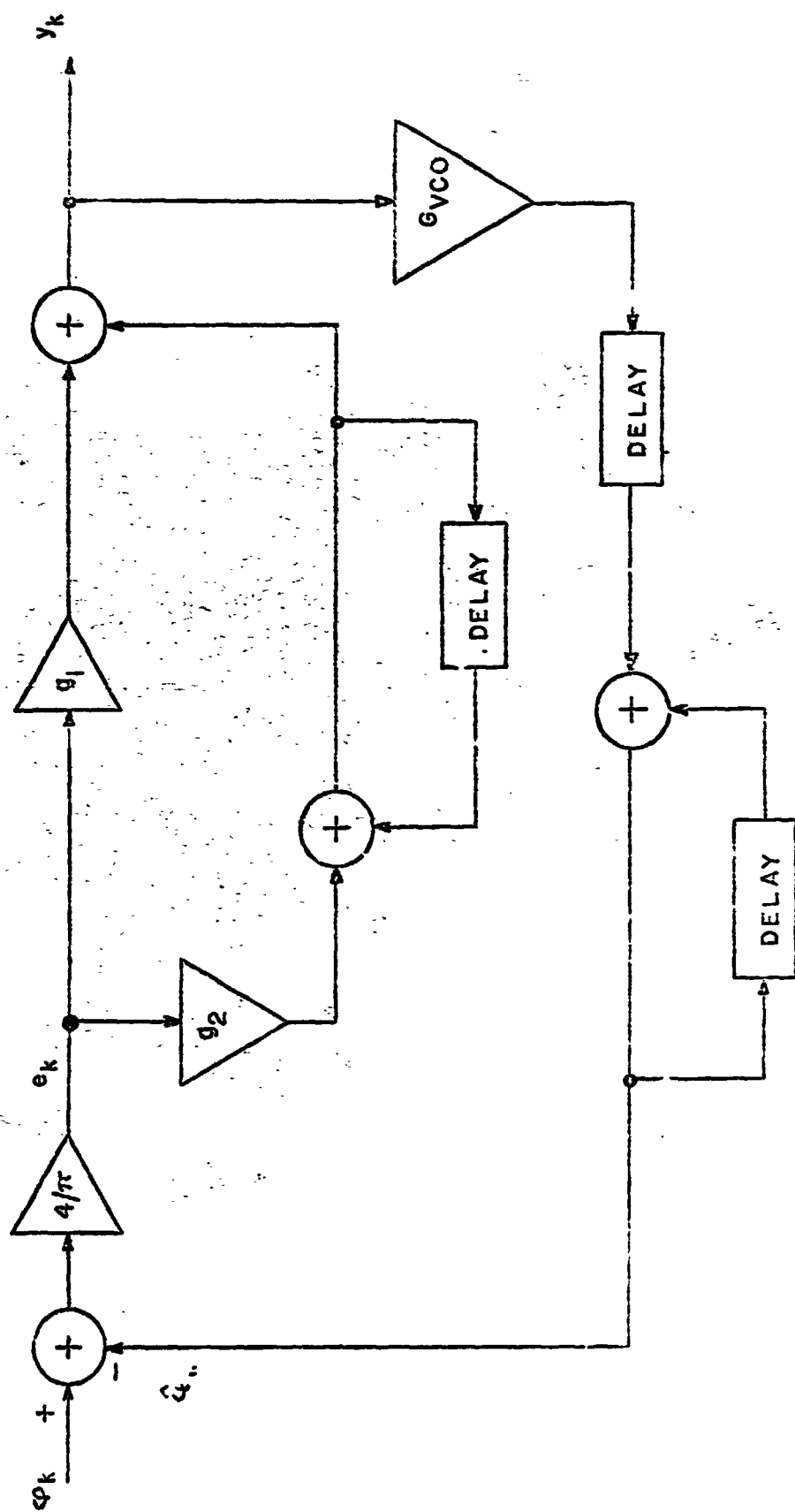
114

Fig. 4.?-1. Linearized model of the second order DPLL.

The characteristic equation for the linearized model is

$$1 + \frac{4}{\pi}\left[g_1 + g_2 \frac{1}{1-z^{-1}} \right] G_{VCO} \frac{z^{-1}}{1+z^{-1}} = 0 \qquad (4.2-2)$$

which simplifies to

$$z^2 + z\left[(4/\pi)(G_1 + G_2) - 2 \right] + \left[1 - (4/\pi)G_1 \right] = 0 \qquad (4.2-3)$$

with $G_1 = g_1 \cdot G_{VCO}$ = proportional loop gain

$\quad\quad G_2 = g_2 \cdot G_{VCO}$ = integral loop gain.

The DPLL is stable if and only if all of the roots of Eq. (4.2-3) lie inside the unit circle, $|z| < 1$. The bilinear transformation

$$z = (s+1)/(s-1) \qquad (4.2-4)$$

maps the interior of the unit z-plane circle onto the left-half of the s-plane, enabling the application of the Routh-Hurwitz test on the resulting polynomial in s. Using Eq. (4.2-4) in Eq. (4.2-3) secures

$$(4/\pi)G_2 s^2 + (4/\pi)G_1 s + \left[4 - (4/\pi)(2G_1 + G_2) \right] = 0 \qquad (4.2-5)$$

for which the Routh-Hurwitz test gives the restrictions for stability:

$$(4/\pi) G_2 > 0 \qquad (4.2-6a)$$

$$(4/\pi) G_1 > 0 \qquad (4.2-6b)$$

$$4 - (4/\pi)(2G_1 + G_2) > 0 \qquad (4.2-6c)$$

The first two conditions are obvious and the third is satisfied when we use gains of the form $\pi / 5 \cdot 2^N$, with N a positive integer. Therefore when the phase error is small, the second order DPLL is stable regardless of how much scaling is introduced. Of course, using this linear model, we cannot conclude anything concerning the DPLL response to arbitrary initial conditions (initial integrator value, initial VCO phase), as this acquisition problem involves operating initially with large phase

error.

4.3 Design of Second Order Loop Gains

To enable comparison to the first order DPLL, we shall design
the second order DPLL to demodulate a maximum frequency offset of
500 Hz and use $m = 4$. The two design equations developed in
Sec. 2.5 and Sec. 2.6 become

$$(e_k)_{max} \leq 0.35 \tag{4.3-1}$$

$$f_s/8 - 1200 > B_L \tag{4.3-2}$$

where

e_k = phase error signal

B_L = linearized second order DPLL bandwidth

f_s = sampling frequency = 50 KHz.

As the second order DPLL tracks frequency deviations with zero
phase error, we consider sinusoidal modulation in connection with the
condition of Eq. (4.3-1). Let the modulation be at the frequency f_m Hz
with modulation index β, so that

$$\varphi_k = \beta \sin k \, 2\pi f_m/f_s \tag{4.3-3}$$

The error signal, e_k, is then sinusoidal with amplitude A and phase α
given by

$$Ae^{j\alpha} = \beta \left. \frac{(4/\pi)(z-1)^2}{z^2 + z[(4/\pi)(G_1 + G_2) - 2] + [1 - (4/\pi)G_1]} \right|_{z = e^{j2\pi f_m/f_s}} \tag{4.3-4}$$

As $f_m \ll f_s$, we have the approximation $z \approx 1$ in the denominator and
$|z - 1| = 2\sin \pi f_m/f_s \approx 2\pi f_m/f_s$ in the numerator, yielding

$$A \approx (2\pi f_m/f_s)^2 \beta/G_2 \tag{4.3-5}$$

Hence, condition Eq (4.3-1) is a restriction on the integral loop gain:

$$G_2 \geq \beta(2\pi f_m/f_s)^2/0.35 \qquad (4.3-6)$$

Using $f_m = 200$ Hz, $\beta = 3$, $f_s = 50$ KHz, we have

$$G_2 \geq 0.0054 \qquad (4.3-7)$$

We choose

$$G_2 = \pi/5 \cdot 2^6 \doteq 0.0098 \qquad (4.3-8)$$

We cannot satisfy Eq. (4.3-2) as easily because one cannot find a simple expression, not even an approximate expression, for the DPLL bandwidth, B_L, in terms of the loop gains G_1 and G_2. Therefore we calculate the magnitude of the DPLL transfer function

$$H(f) = \frac{z(4/\pi)(G_1+G_2) - (4/\pi)G_1}{z^2 + z[(4/\pi)(G_1+G_2)-2] + [1-(4/\pi)G_1]}\Bigg|_{z = e^{j2\pi f_m/f_s}}$$

$$(4.3-9)$$

as a function of f and determine the bandwidth graphically. In Eq. (4.3-9), G_2 is fixed by Eq. (4.3-8) and G_1 takes on the discrete values $\pi/5 \cdot 2^N$ with N an integer. The restriction of Eq. (4.3-2) is equivalent to $B_L < 4.05$ KHz and if we require a factor of two in the inequality, we find the possible values of N are $N \geq 3$.

• The field of second order DPLL candidates is narrowed by considering the response to the simulated noise spike introduced in Sec. 3.7. As before we superimpose the spike on sinusoidal modulation, solve the DPLL difference equation, Eq. (4.1-1), and examine the solution to determine whether or not the DPLL follows the spike.

The computer program which achieves this is shown in Fig. 4.3-1, with Table 4.3-1 identifying the variables. This program is essentially

118

```
C-FOCAL, 1969

01.05 A N,T,E
01.10 S W=3.14159;S G1=E/5*2:N;S G2=W/5*2:7;S PK=0;S IK=0
01.15 F K=-250,1,270;DO 2
01.20 QUIT


02.05 S H=3*FSIN(2*W*200*K/50000);I (K*<T-K>)2.15
02.10 S EK=<2+E>/2+<2-E>*FCOS(2*W*K/T)/2
02.11 S EK=-EK*FCOS(K*W/3+H-W*(1-FCOS<W*K/T>))
02.12 S EK=EK*FSGN(FSIN<K*W/3+PK>);GOTO 2.2
02.15 S EK=-2*FCOS(K*W/3+H)*FSGN(FSIN<K*W/3+PK>)
02.20 S IK=IK+G2*EK;S PK=PK+G1*EK+IK
02.25 I (K)2.9,2.3,2.35
02.30 F X=0,1,63;T "."
02.31 T #
02.35 I (K/10-FITR(K/10))2.9,2.4,2.9
02.40 F X=0,1,FITR(40+<10/3>*PK);T " "
02.45 T "*",#;F X=0,1,40;T " "
02.50 T ".",!
02.90 C
*
```

Fig. 4.3-1. FOCAL program to solve the second order DPLL equation for the case of sinusoidal modulation plus a spike.

Computer Variable	Equation Variable
T	spike duration, T_{spike}
E	minimum spike amplitude
G1	proportional loop gain, G_1
G2	integral loop gain, G_2
H	input phase, φ_k
EX	phase error signal, e_k
IK	integrator value
PK	VCO phase, ϑ_k

Table 4.3-1. The correspondence between the variables appearing in the program of Fig. 4.3-1 and the DPLL equations.

the same as that for the first order DPLL, except for line 2.20 which integrates the scaled error signal (G2 EK), and includes this value (IK) in updating the VCO phase (PK).

The computer results obtained for $3 \leq N \leq 8$ are not very impressive. In all cases, when a constant amplitude, 32-sample duration spike is introduced, the DPLL loses lock and does not immediately regain lock. Fig. 4.3-2 is the VCO phase for the case $N = 4$ and spike duration 0.54 msec. It is clear that the DPLL has lost lock in response to the spike, and even if lock is finally regained, the output noise generated during the transient period severely deteriorates the DPLL output, making it worse than the first order DPLL. Hence it is impossible to find a second order DPLL which meets the phase error requirement and responds satisfactorily to input noise spikes.

To continue the search for a second order DPLL requires changing the integral loop gain and therefore changing the maximum phase error signal. The phase error condition was based upon having equal quantization noise and harmonic distortion at the phase detector. We have already seen that the quantization noise (and hence the error signal harmonic distortion) is not significant compared to the phase jitter, and so we shall decrease the integral path by a factor of 2 (to the next available gain) and thereby double the phase error.

Using $G_2 = \pi/5 \cdot 2^7$, the bandwidth requirement is satisfied for $N \geq 3$. For $N = 3$, the second DPLL follows a 32-sample constant amplitude spike as shown in Fig. 4.3-3 and therefore we expect this second order DPLL to have an identical threshold to the first order DPLL.

Setting $N = 4$ and introducing a 32-sample, constant amplitude spike, we obtain the response of Fig. 4.3-4, in which the DPLL does not follow the input spike. Widening the input spike to 40-samples yields the response of Fig. 4.3-5 where the VCO phase initially follows the spike but recovers and suppresses the spike. Further widening of the input
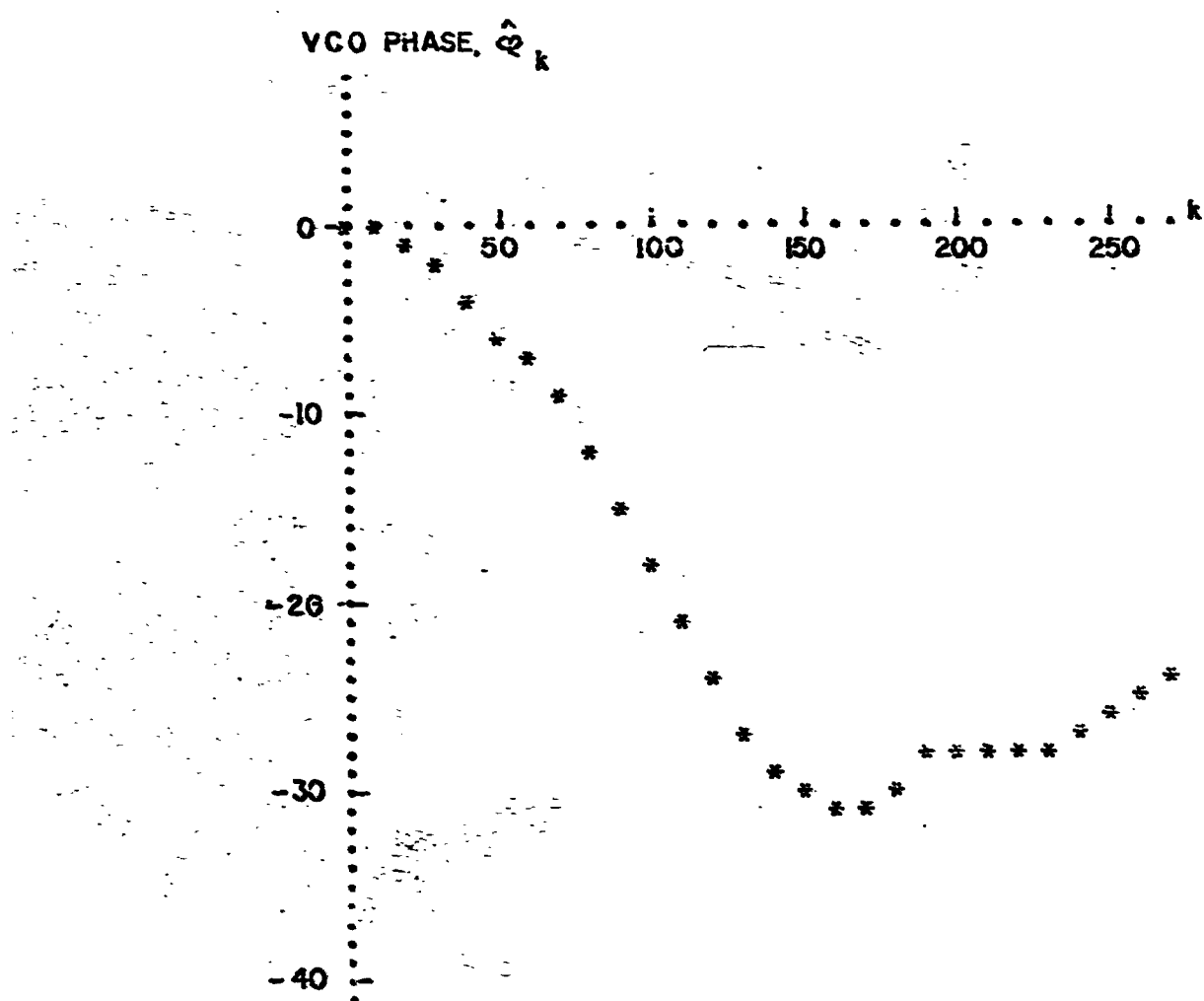
Fig 4.3-2. Second order DPLL response to sinusoidal modulation plus
a 32-sample, constant amplitude spike with N = 4.
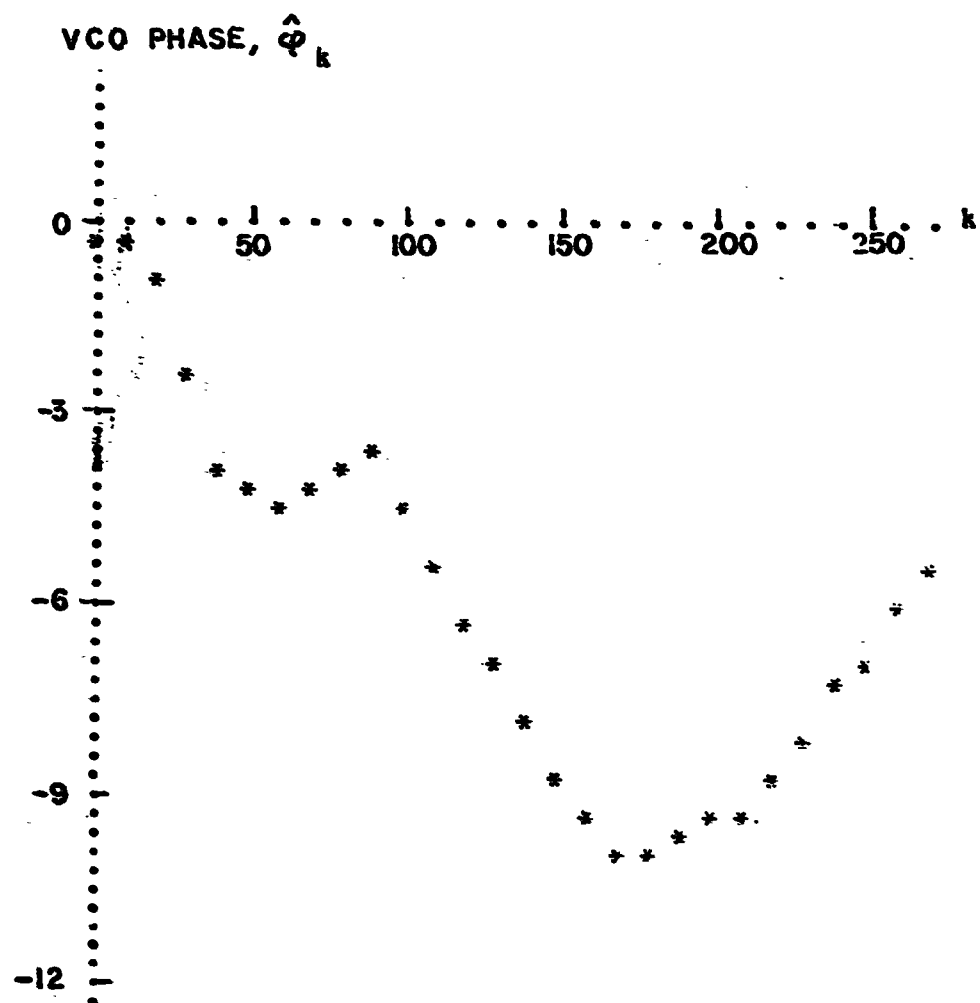
Fig. 4.3-3. Second order DPLL response to sinusoidal modulation plus a 32-sample, constant amplitude spike with N = 3.
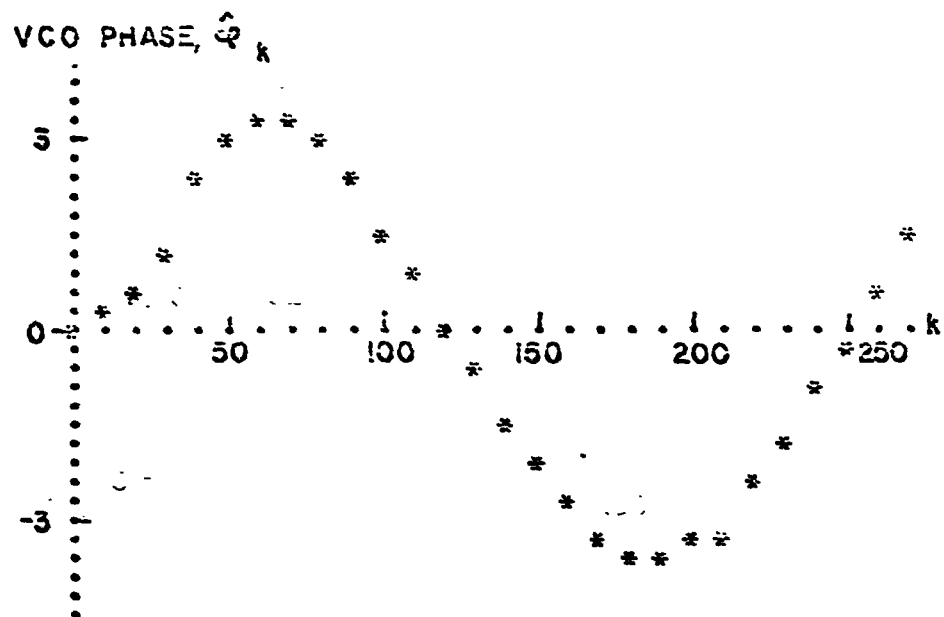
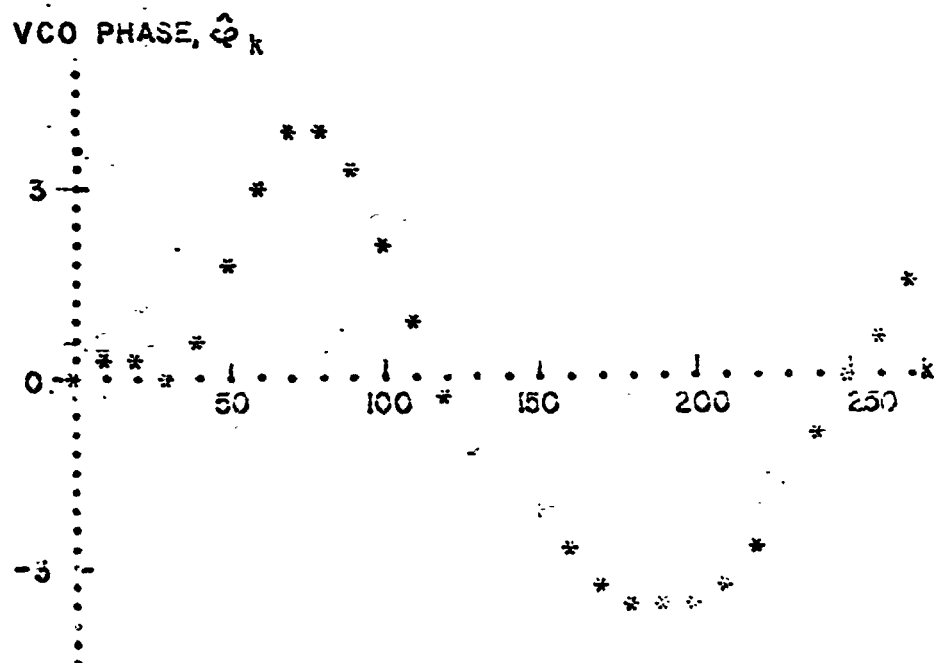Fig. 4.3-4. Second order DPLL response to sinusoidal modulation plus a 32-sample, constant amplitude spike.

Fig. ..3-5. Second order DPL response to sinusoidal ... plus a 40-sample, constant amplitude spike.

spike to 49-samples results in the DPLL reproducing the spike, as illustrated in Fig 4.3-6. If the minimum spike samplitude is dropped to 1 volt, the DPLL no longer follows the 49-sample spike; Fig. 4.3-7 illustrates this. Keeping the minimum amplitude at 1 volt, the spike duration must be increased to 70-samples before the DPLL tracks the spike.

For $N = 5$, the DPLL follows a 46-sample, constant amplitude spike, and follows a 68-sample, 1 volt minimum amplitude spike.

For $N = 6$, we find that the DPLL tracks a 40-sample, constant amplitude spike. If the minimum spike amplitude is reduced to 1 volt, and the spike duration increased to 60 samples, then the DPLL loses lock as a result of the input spike. The response is shown in Fig. 4.4-8, where we see it takes two cycles of modulation for the DPLL to regain lock.

Thus the choice for the proportional path gain is between $N = 4$ and $N = 5$. In order to eliminate one value we consider the spike model superimposed on constant modulation, which results in a 600 Hz frequency deviation from the carrier. The computer program is modified so that $H \equiv \varphi_k = 2\pi k\, 600/50000$.

For $N = 4$ the DPLL responses to various constant amplitude spikes are illustrated in Fig. 4.3-9. In (a) and (b) the spike duration is 40 and 43 samples respectively and in both cases the DPLL does not follow the spike. a 44-sample spike is introduced and the response; (c), shows that the DPLL now follows this spike. When the spike is again widened to 46 samples, the VCO phase develops an error of 4π radians (Fig. 4.3-9d) instead of the expected 2π radians. This occurs because of the DPLL's underdamped transient response, which is observed in Fig. 4.3-9c as an undershoot of the steady state input phase. In Fig. 4.3-9d, this undershoot becomes sufficient to bring the phase error beyond the unstable equilibrium point at $\varphi_k - \hat{\varphi}_k = 3\pi$, and so steady state is reached at $\varphi_k - \hat{\varphi}_k = 4\pi$. Hence the DPLL follows the 46-sample spike, and generates
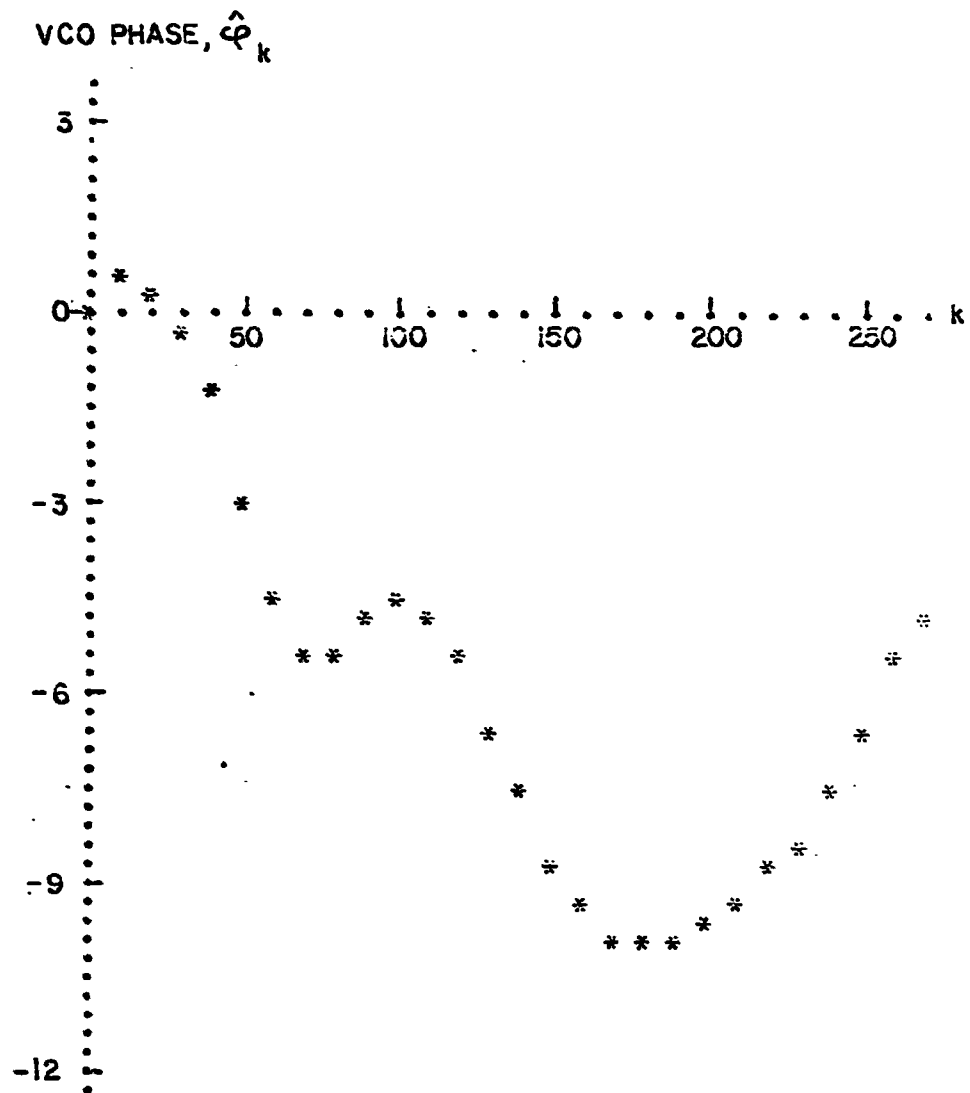
Fig. 4.3-6. Second order DPLL response to sinusoidal modulation plus a 49-sample, constant amplitude spike.
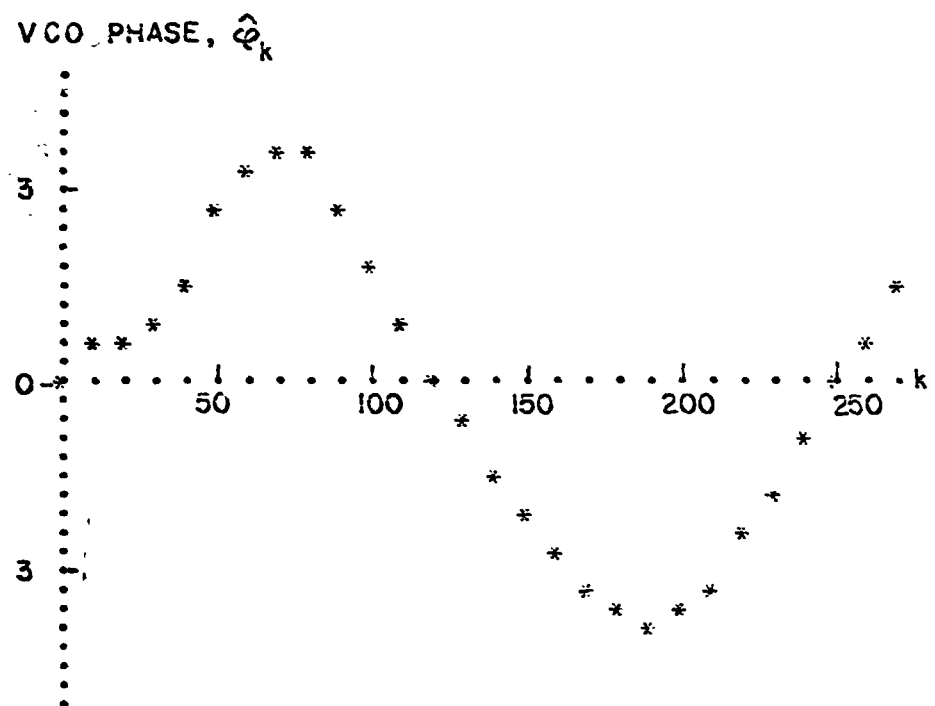
126

Fig.4.3-7. Second order DPLL response to sinusoidal modulation plus a 49-sample, one volt minimum amplitude spike.
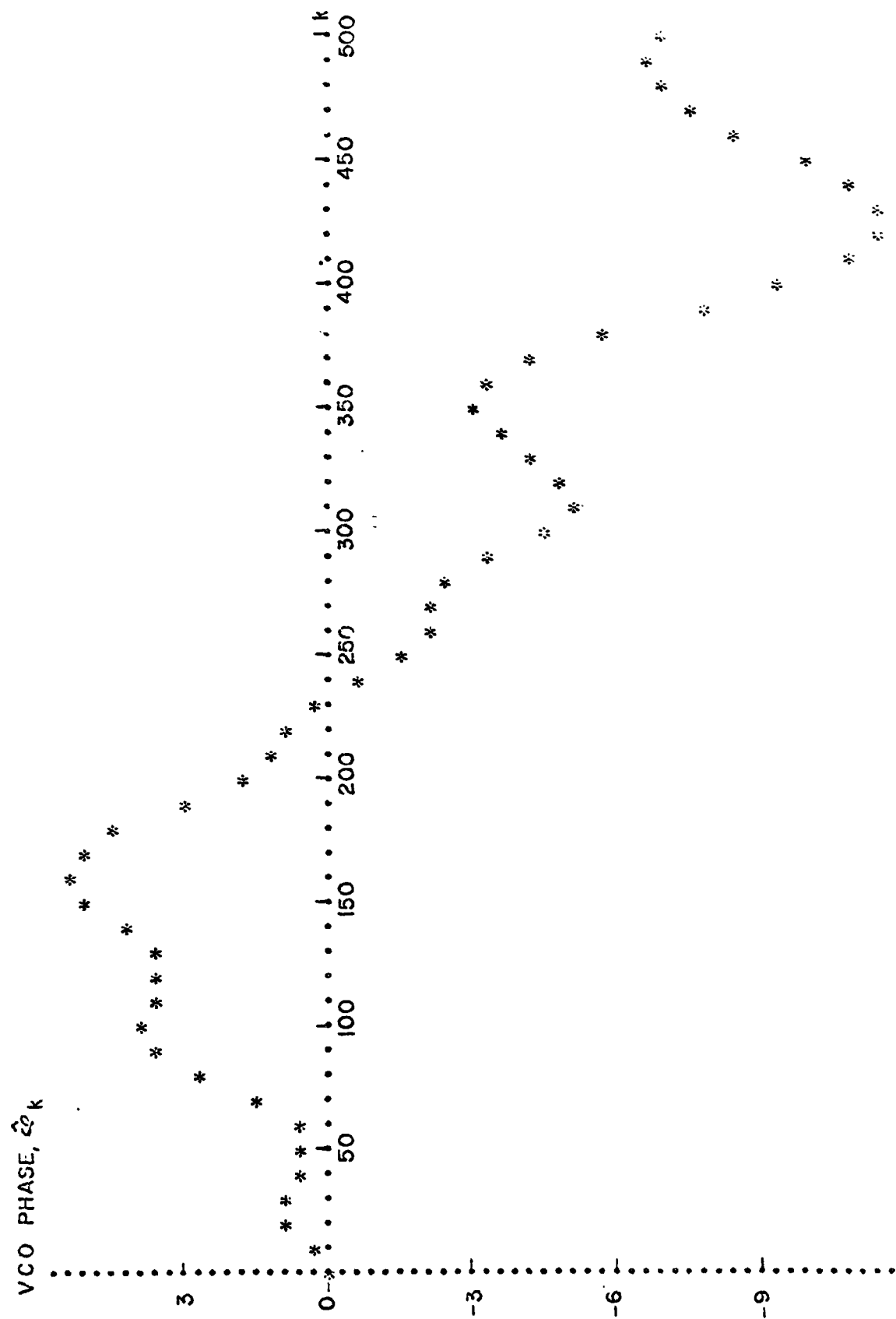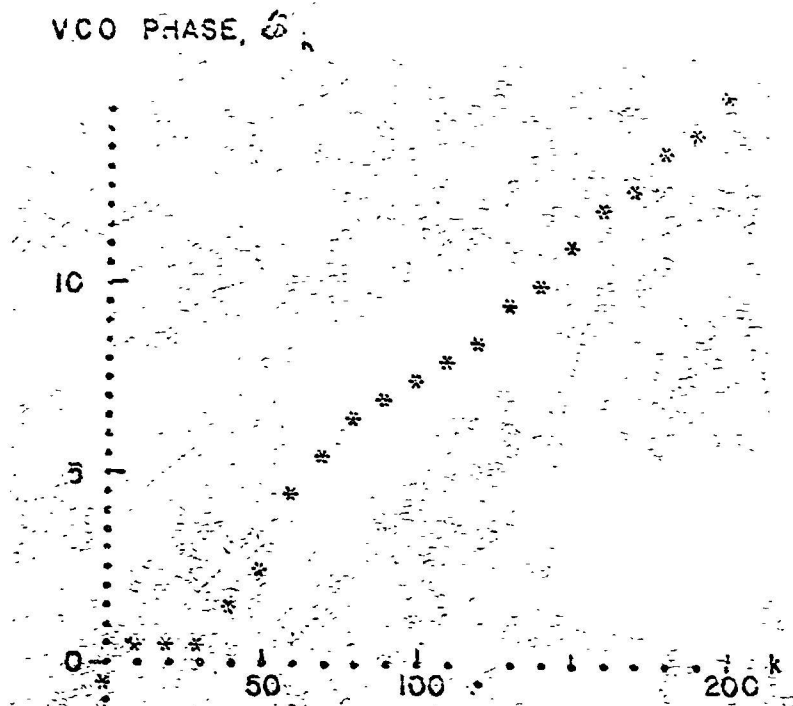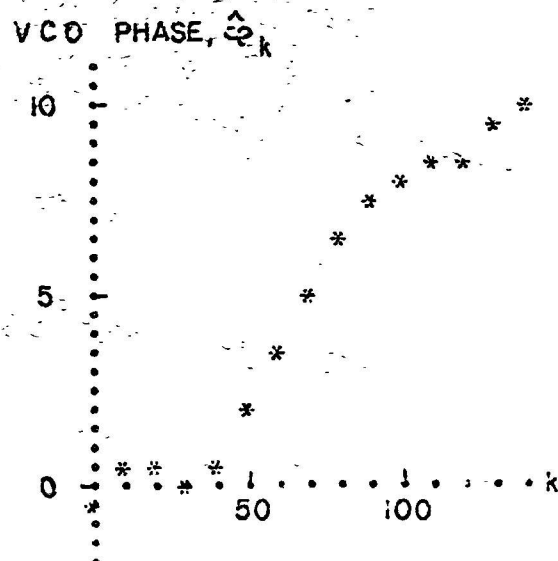
127

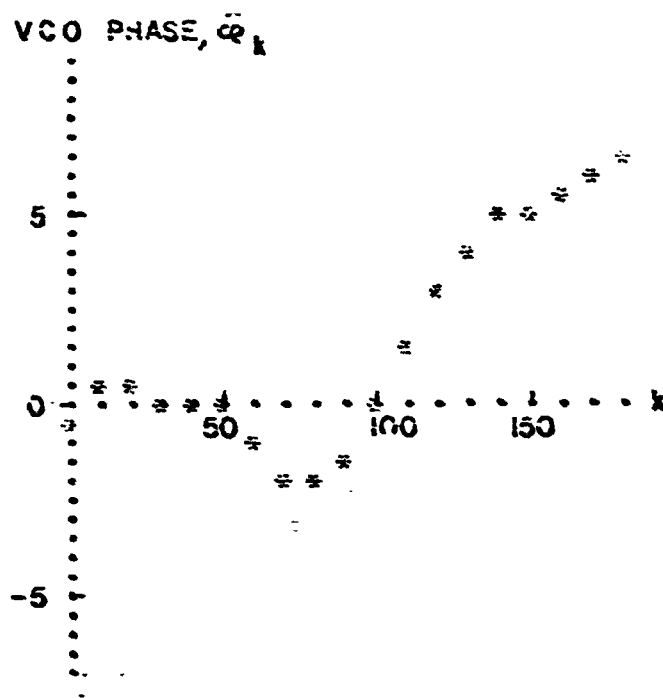Fig. 4.3-8. Second order DPLL response to sinusoidal modulation plus a 60-sample, one volt minimum amplitude spike.
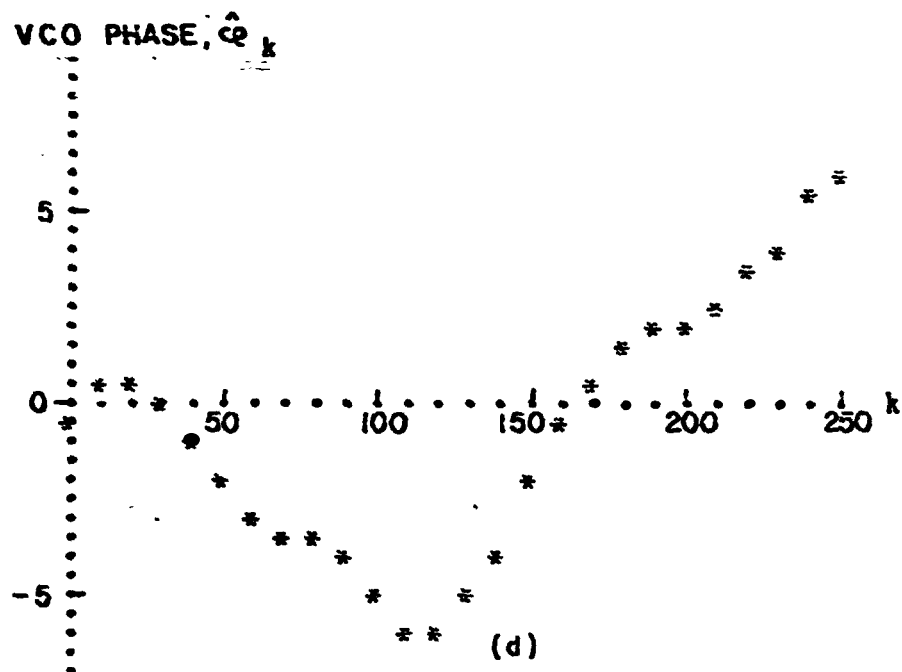
128

VCO PHASE, $\hat{\phi}_k$

(a)

VCO PHASE, $\hat{\phi}_k$

(b)

Fig. 4.3-9a,b. Second order DFLL response to constant offset modulation plus a spike of duration (a) 40 samples, (b) 3 samples.

Fig. 4.3-9c,d. Second order DPLL response to constant offset modulation plus a spike of duration (c) 44 samples, (d) 46 samples.

an output spike having an area of 4π. It is possible for the undershoot to generate a 6π phase error, as illustrated in Fig. 4.3-9e, where the input spike lasts 60 samples. Here the DPLL output contains a 6π-area spike in responst to the input 2π-area spike.

Next consider $N = 5$; the spike responses appear in Fig. 4.3-10. In (a), we see that the DPLL deos not follow a 32-sample spike. This remains the case until the spike duration is 38-samples, at which point the DPLL follows the spike, shown in (b). Increasing the spike duration to 39 samples, the DPLL develops a 4π radian error, again because of the underdamped response, as shown in (c). Note however that this DPLL with $N = 5$ is more underdamped than the DPLL with $N = 4$, as here, a 39-sample spike generates a 4π-area spike, whereas previously ($N = 4$) a 2π-area spike was generated. This underdamped behavior causes trouble when a 45-sample spike is introduced; Fig. 4.3-10d shows that the VCO slips several cycles in an attempt to relock to the input, and hence generates a large output spike. Notice that in Fig. 4.3-9d the VCO has not yet regained lock and the output spike generated will have an area of at least 8π.

The fact that the DPLL having $N = 5$ is more underdamped than that with $N = 4$ is further borne out by examining the linearized DPLL transfer function. The two curves are shown in Fig. 4.3-11 where we immediately notice the larger resonant peak for $N = 5$. Of course, when the phase error is large, the linearized model does not apply, but when the DPLL is close to its equilibrium value, we can expect a larger overshoot from the $N = 5$ loop than for $N = 4$.

Therefore our choice for the second order DPLL gains is

$$G_1 = \pi/5 \cdot 2^4 \qquad\qquad (4.3-10a)$$

$$G_2 = \pi/5 \cdot 2^7 \qquad\qquad (4.3-10b)$$

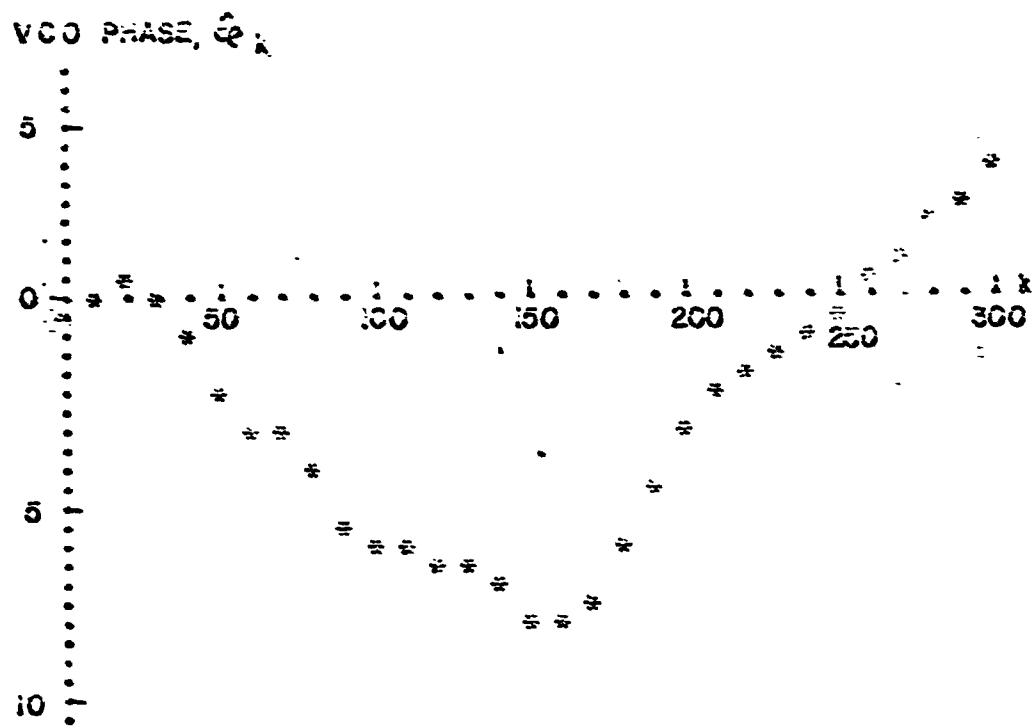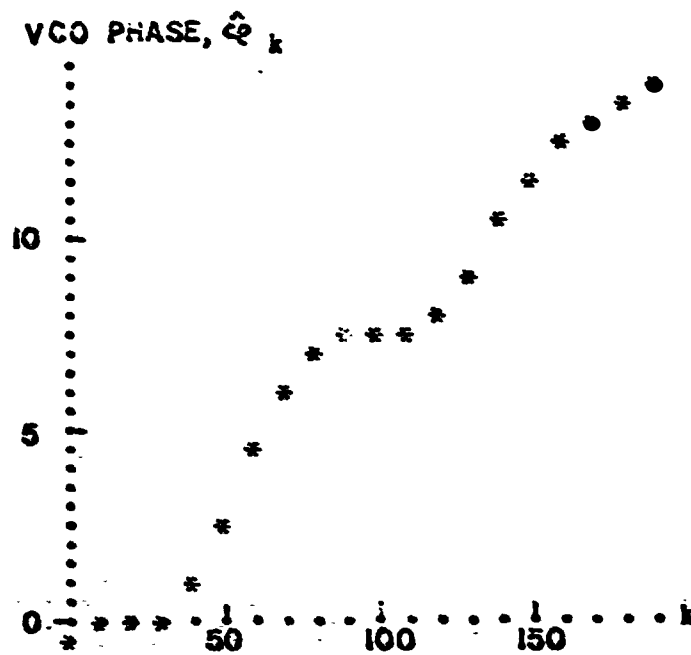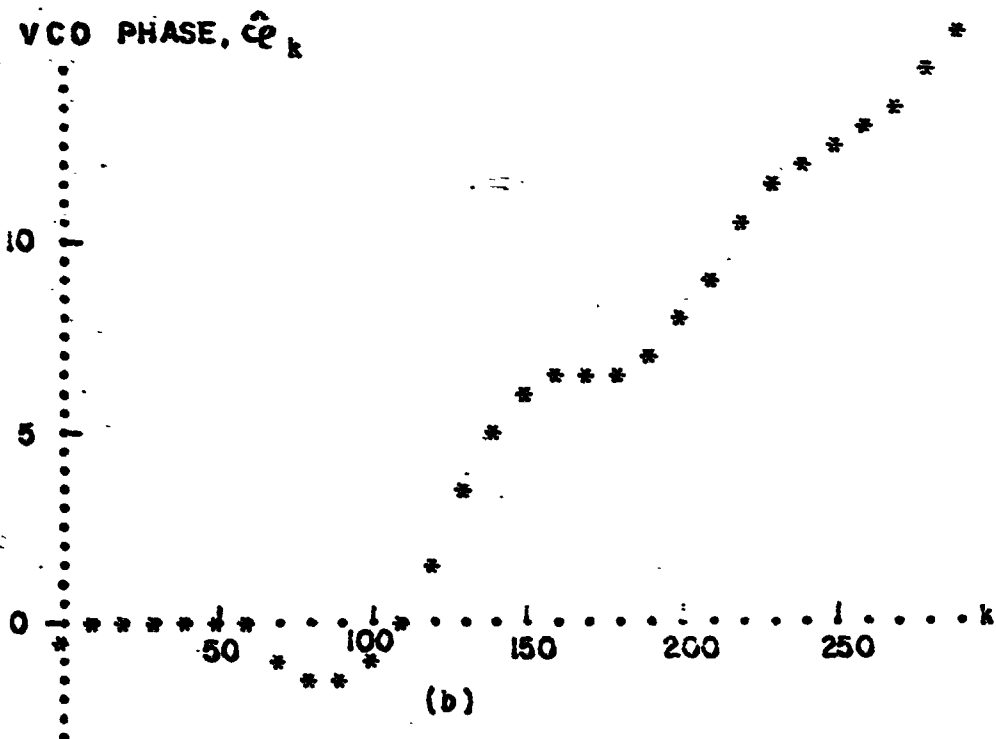**Fig. 4.3-9e.** Second order DPLL response to constant offset modulation plus a 60-sample spike.

Fig. 4.3-10a,b. Second order DPLL response to constant offset modulation plus a spike of duration (a) 32 samples, (b) 38 samples.
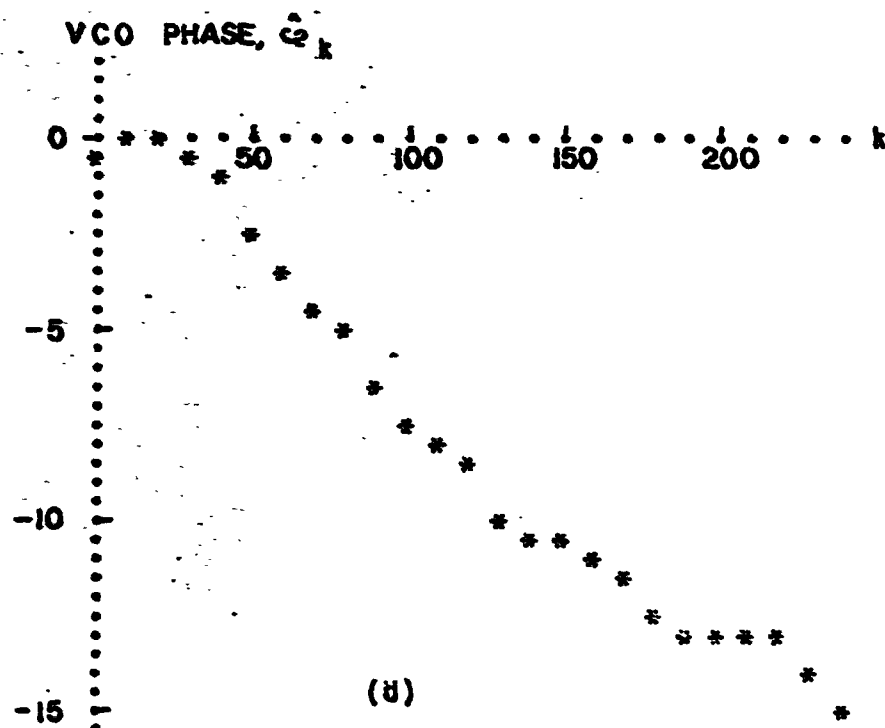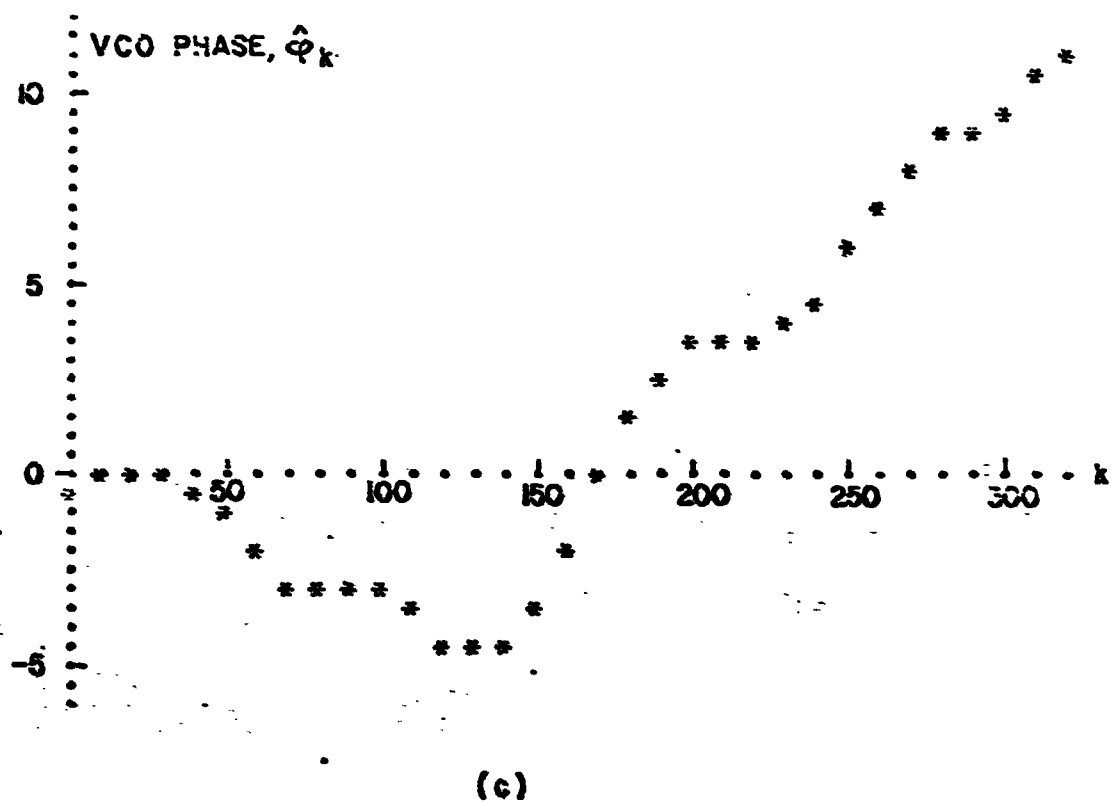
133

Fig. 4.3-10c,d. Second order DPLL response to constant offset modulation plus a spike of duration (c) 39 samples, (d) 45 samples.
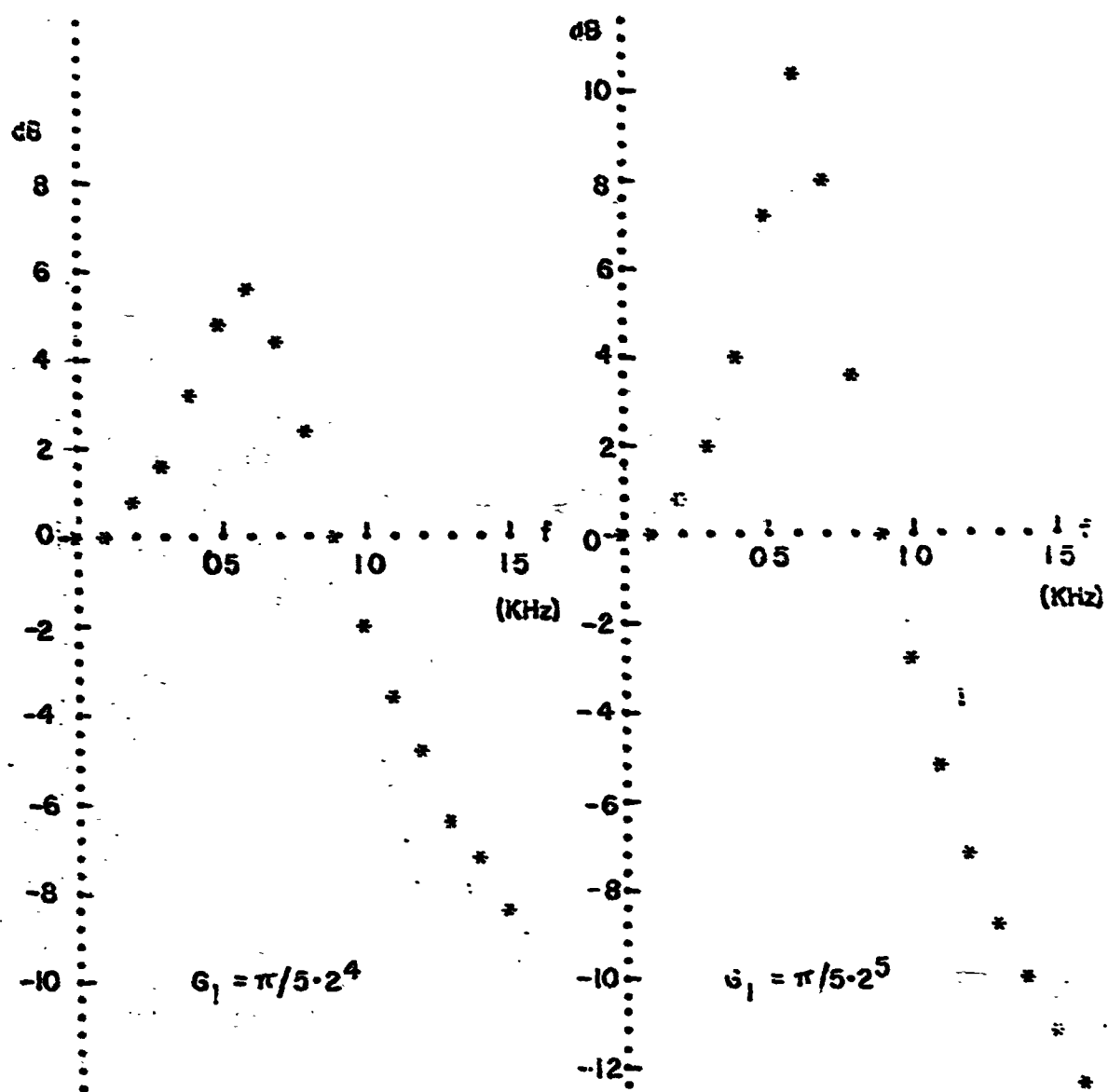
Fig. 4.3-11. Linearized second order DPLL transfer functions.

135

4.4 Hardware Implementation

The block diagram of the second order DPLL is shown in Fig. 4.4-1. The proportional loop gain $G_1 = \pi/5 \cdot 2^4$ is obtained using unity gain in the forward path, a $1/2^5$ scaling for the explicit VCO gain, and an implicit VCO gain of $\pi/(5/2)$, obtained by using the second most significant bit of the VCO register for the VCO output. This is the maximum implicit VCO gain available, as the most significant bit (the sign bit) is always 1 as a result of adding the VCO carrier term $(\pi/2m)$. The constant offset representing $\pi/8$ is the binary word $1000100...0$.

In order to obtain the integral path gain $G_2 = \pi/5 \cdot 2^7$, we must add a scaling of $1/2^3$ to the forward loop integral path. We choose to place this scaling before the integration in order to minimize the probability of overflowing the integrator. In order to avoid truncation of three bits, the foward loop integrator (adder and register) consists of 13 bits. Hence the output adder, A_2 in Fig. 4.4-1, is also a 13-bit adder.

The D/A converter at the output has a 10-bit capacity and so a truncation error is introduced. The output is fed back to the VCO through a $1/2^5$ scaling and to avoid truncation, the VCO operates using 18 bits.

As previously mentioned, the foward loop integrator and VCO integrator are time-shared, which is to say that adders A_1, A_2, and A_4 represent the same piece of hardware. Although the foward loop integrator register contains only 13 bits, it is easily converted to an 18-bit word by adding five additional bits whose values are the complement of the sign bit.

The schematic diagram of the second order DPLL and the associated timing diagram appear in Fig. 4.4-2. There are two adders with the additional saturation logic and three registers: an output register, a forward loop integral (FLI) register, and the VCO register. The transfer gates provide a buffer during the integration process and also provide flexibility in the timing. To understand the operation, refer to the schematic and timing diagram. The sequence of events is:
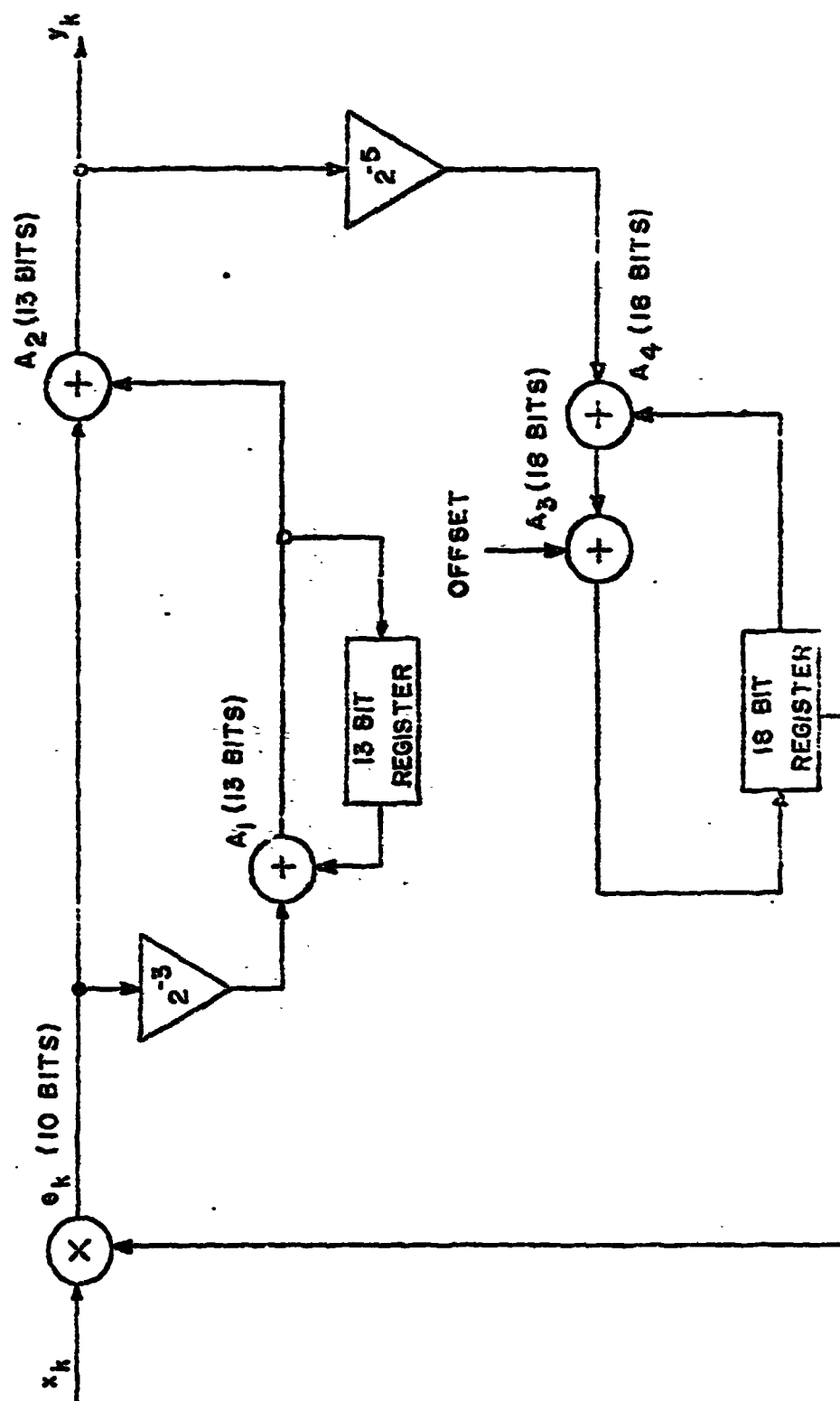
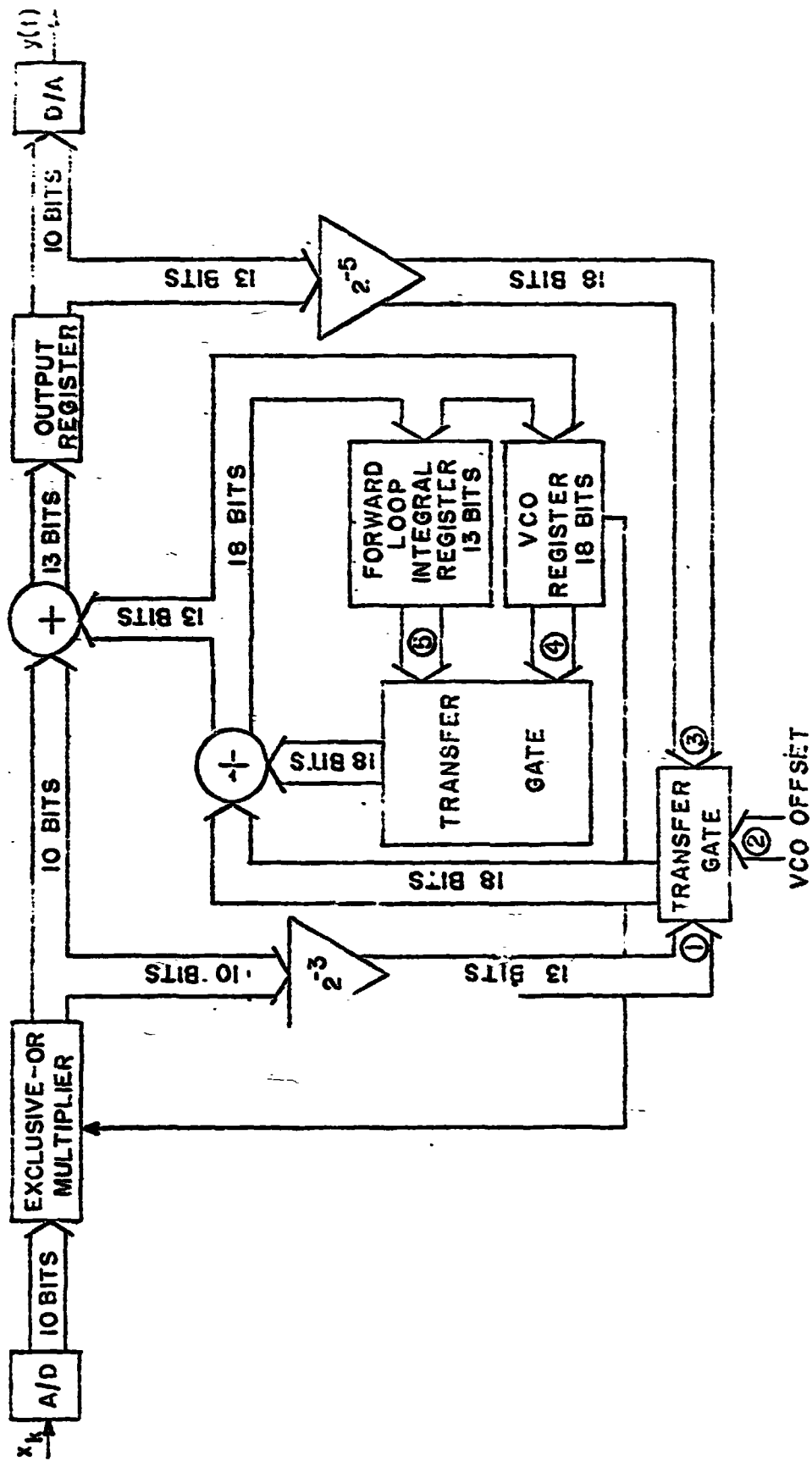Fig. 4.4-1. Block diagram of the second order DPLL.

137

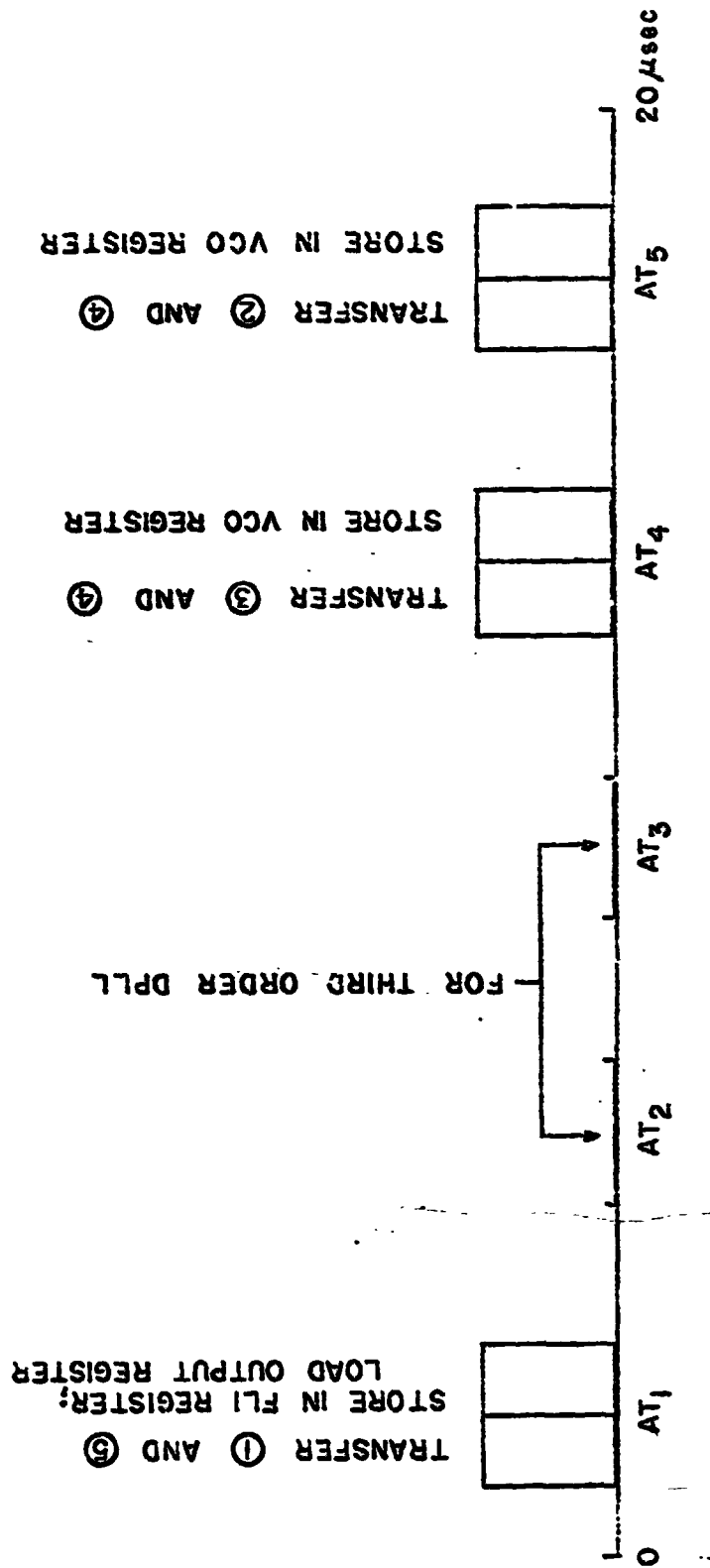Fig. 4.4-2a. Schematic of the second order DPLL.

138

Fig. 4.4.2b. Second order DPLL timing diagram.

Forward Loop Integration (performed during AT 1): The scaled error signal (signal ①) and FLI register (signal ⑤) are added and the result is stored in the FLI register.

Output Addition (AT 1): The error signal and its integral are added and stored in the output register. The D/A conversion also takes place at this time.

VCO Integration (AT 4 and AT 5): First, the scaled output (signal ③) is added to the VCO register (signal ④) and the result stored in the VCO register. This occurs during AT 4. Next, the VCO offset (signal ②) is added to the VCO register (signal ④) and the result is stored in the VCO register.

The second bit of the VCO register is then used to multiply (exclusive-or gate) the next input (x_{k+1}), generating e_{k+1}, and the sequence begins again.

4.5 Output Noise

As with the first order DPLL, the second order DPLL output contains quantization, thermal, and harmonic noise. In addition, a truncation noise is introduced as the D/A converter uses only ten of the thirteen output signal bits.

4.5.1 Quantization Noise

The input signal is quantized using B bits and a quantization step size S, introducing white quantization noise having power spectral density $G_{N_q}(f)$ given by

$$G_{N_q}(f) = S^2 T_s /12$$

where T_s is the sampling period. The linearized second order DPLL transfer function is

140

$$\Xi(z) = \frac{Y(z)}{\hat{\theta}(z)} = \frac{[(\frac{4}{\pi}g_1 + \frac{4}{\pi}g_2)z - \frac{4}{\pi}g_1] \, [z-1]}{z^2 - z(\frac{4}{\pi}g_1 G_{VCO} + \frac{4}{\pi}g_2 G_{VCO} - 2) + (1 - \frac{4}{\pi}g_1 G_{VCO})}$$

$$(4.5-1)$$

where g_1, g_2, and G_{VCO} are identified in Fig. 4.2-1. For $z = \exp(j2\pi f/f_s)$ and $f \ll f_m$ = maximum modulating frequency, we have $z \approx 1$ as $f_m \ll f_s$, and Eq. (4.5-1) becomes approximately

$$|H(z)| = \left|\frac{Y(z)}{\hat{\theta}(z)}\right|_{z=e^{j2\pi f/f_s}} \approx 2\pi f / G_{VCO} f_s \qquad (4.5-2)$$

That is to say, the linearized DPLL transfer function is approximately that of a differentiator. The output quantization noise is

$$N_q = \int_{-f_m}^{f_m} |H|^2 \, G_{N_q}(f) \, df = (2\pi S/G_{VCO})^2 (f_m/f_s)^3 / 18 \qquad (4.5-3)$$

4.5.2 Thermal Noise

Since a second order DPLL behaves approximately as a differentiator, the output signal-to-noise ratio at high input signal-to-noise ratios is given by the results of Sec. 3.8.1:

$$S_o/N_o = 3\beta^2 S_i/N_i \qquad \text{for constant modulation} \qquad (4.5-4a)$$

$$S_o/N_o = \frac{3}{2}\beta^2 S_i/N_i \qquad \text{for sinusoidal modulation} \qquad (4.5-4b)$$

Again, these results are identical to those for an ideal differentiating discriminator.

4.5.3 Truncation Noise

The effect of truncating the number of bits used is essentially the same as quantizing; however, in truncating, we quantize a finite number of levels into a subset of these levels. The expression for the quantiza-

tion noise assumes the error is uniformly distributed. This is not
strictly true for truncation, as the discrete values give rise to discrete
errors.

Let the D/A converter operate using N bits and have a step size
S volts. Assume the binary word available has $M + N$ bits, and the
last M bits are lost in the D/A conversion process. Then the error com-
mitted in truncation is 0, $\pm S/2^M$, $\pm 2S/2^M$, . . . , $\pm (2^M - 1)S/2^M$ volts.
Furthermore, zero error is made in 2^N of the 2^{N+M} possible numbers;
nonzero errors are each made in 2^{N-1} numbers. The error probability
density function is thus a set of impulses, the impulse at the origin hav-
ing area $1/2^M$, while the impulses at $\pm p S/2^M$, $1 \leq p \leq 2^M - 1$, having
area $1/2^{M+1}$. The variance of this distribution is

$$\sigma_T^2 = \sum_{p=-2^M+1}^{2^M-1} (pS/2^M)^2/2^{M+1} = \frac{S^2}{3}(1-2^{-M})(1-2^{-M-1}) \quad (4.5-5)$$

Note that if M is large, this reduces to the result for an error uniformly
distributed over the interval $[-S, +S]$.

Assuming the truncation error is endependent from sample-to-sample
and that the D/A staircase looks like a sequence of impulses to the out-
put low pass filter, the power spectral density of the truncation noise is
constant [17]:

$$G_{N_T} = \sigma_T^2 T_s = \frac{S^2}{3f_s}(1-2^{-M})(1-2^{-M-1}) \quad (4.5-6)$$

with T_s the sampling period. Hence the truncation noise appearing at
the output is

$$N_T = \frac{2}{3}S^2(f_m/f_s)(1-2^{-M})(1-2^{-M-1}) \quad (4.5-7)$$

where f_m is the output filter cutoff frequency.

Harmonic Noise

The harmonic noise generated by the square wave VCO is calculated in a similar manner as for the first order DPLL. Two changes that must made are:

1. The VCO phase is now calculated using the second order DPLL linear model.

2. The harmonics generated at the error signal are filtered by the proportional plus integral filter in the forward path.

As developed in Sec 3.8.4, the distortion terms are

$$D = \frac{4}{\pi} \frac{1}{4m-1} \sin[(4m-1)\hat{\theta}_k + \varphi_k]$$

$$+ \frac{4}{\pi} \frac{1}{4m+1} \sin[(4m+1)\hat{\theta}_k - \varphi_k] \qquad (4.5-8)$$

For the case of constant modulation, the input is deviated from the carrier frequency by Δf Hz and

$$\varphi_k = k\, 2\pi \Delta f / f_s \qquad (4.5-9)$$

In the second order DPLL linearized model, the VCO follows this input with zero phase error, $\hat{\varphi}_k = \varphi_k$, and the distortion terms become:

$$D = \frac{4}{\pi} \frac{8m}{16m^2 - 1} \sin k\, 2\pi 4m \Delta f / f_s \qquad (4.5-10)$$

As with the first order DPLL, the harmonic distortion occurs at the frequency $4m\, \Delta f$ Hz. The proportional plus integral filter has the transfer function

$$T(f) = g_1 + g_2 \frac{1}{1-z^{-1}} \Bigg|_{z=e^{j2\pi f/f_s}} \qquad (4.5-11)$$

If the harmonic frequency ($4m\, \Delta f$) falls within the output low pass filter cutoff (f_m), then the filter transfer function is approximately

143

$$\left.\frac{Y(z)}{\Theta(z)}\right|_{z=e^{j2\pi 4m\,\Delta f/f_s}} \approx g_2 f_s / 2\pi 4m\,\Delta f \qquad (4.5\text{-}12)$$

by virtue of the fact that $4m\,\Delta f/f_s < f_m/f_s \ll 1$. Hence at the output the harmonic distortion amplitude is

$$|D| = \frac{4}{16m^2 - 1}\,\frac{g_2 f_s}{\pi^2 m\,\Delta f} \qquad (4.5\text{-}13)$$

and the output power is

$$N_D = 20\log\frac{4g_2 f_s}{\sqrt{2}\,(16m^2 - 1)\,\pi^2 m\,\Delta f} \qquad dB \qquad (4.5\text{-}14)$$

When the carrier is sinusoidally modulated at f_m Hz with modulation index β, we have

$$\varphi_k = \beta\sin k\,2\pi f_m/f_s \qquad (4.5\text{-}15)$$

Using the linear model, the VCO phase is sinusoidal with amplitude A and phase α where

$$Ae^{j\alpha} = \beta\left.\frac{z(\frac{4}{\pi}G_1 + \frac{4}{\pi}G_2) - \frac{4}{\pi}G_1}{z^2 + z(\frac{4}{\pi}G_1 + \frac{4}{\pi}G_2 - 2) + (1 - \frac{4}{\pi}G_1)}\right|_{z=e^{j2\pi f_m/f_s}}$$

$$(4.5\text{-}16)$$

and since again we have $z \approx 1$, the amplitude and phase are approximately $A \approx \beta$, $\alpha \approx 0$. Hence, as with the first order DPLL, the distortion is

$$D = \frac{4}{\pi}\,\frac{8m}{16m^2 - 1}\,\sin(4m\beta\sin k\,2\pi f_m/f_s) \qquad (4.5\text{-}17)$$

and it contains odd harmonics of the modulating frequency. The amplitude of the $(2n+1)^{st}$ harmonic at the output is

144

$$\left| D_{2n+1} \right| = \frac{4}{\pi} \frac{8m}{16m^2 - 1} 2J_{2n+1}(4m\beta) \frac{g_2 f_s}{2\pi(2n+1)f_m} \qquad (4.5-18)$$

and the output noise is

$$N_{D_{2n+1}} = 20 \log \left| D_{2n+1} \right| / \sqrt{2} \qquad dB \qquad (4.5-19)$$

As mentioned in Sec. 3.8.4, only those harmonics below the low pass filter cutoff frequency will contribute noise according to Eq. (4.5-19).

4.6 Expreimental Results

The second order DPLL was tested using the following parameters:

sampling frequency, f_s	= 50 KHz
proportional loop gain, G_1	= $\pi/5 \cdot 2^4$
integral loop gain, G_2	= $\pi/5 \cdot 2^7$
carrier frequency, f_o	= 53.125 KHz
modulation index, β	= 3, 10
carrier amplitude	= 2 volts

The test facility was identical to the setup used to test the first order DPLL, Fig. 3.9-1, including the generation of the IF noise.

4.6.1 Results for Constant Modulation

With the carrier deviated by $\Delta f = 600$ Hz, the DPLL output is constant:

$$y_k = 2\pi \Delta f / G_{VCO} f_s \quad :: \quad 1.92 \quad \text{volts} \qquad (4.6-1)$$

which corresponds to an output signal power

$$S_o = 20 \log y_k = 5.7 \quad dB \qquad (4.6-2)$$

The output quantization noise computed from Eq. (4.5-3) is

$$\beta = 3, \quad N_q = -80.4 \quad dB \qquad (4.6-3a)$$
$$\beta = 10, \quad N_q = -95.6 \quad dB \qquad (4.6-3b)$$

145

The truncation of three bits by the D/A converter contributes, according to Eq. (4.5-7)

$$\beta = 3, \quad N_T = -66.6 \quad dB \qquad (4.6-4a)$$

$$\beta = 10, \quad N_T = -71.8 \quad dB \qquad (4.6-4b)$$

With no thermal noise added to the carrier, the output noise measured is

$$\beta = 3, \quad N_o = -35.0 \quad dB \qquad (4.6-5a)$$

$$\beta = 10, \quad N_o = -50.3 \quad dB \qquad (4.6-5b)$$

As was the case with the first order DPLL, the output noise which dominates the quantization and truncation noise, is caused by the phase jitter between the carrier oscillator and sampling frequency clock. Notice that this output noise has a parabolic spectrum, as narrowing the output filter from $f_m = 200$ to $f_m = 60$ Hz results in a 14.3 dB drop in noise power; the theoretical drop is $(60/200)^3 = -15.3$ dB.

The signal-to-noise curves for $\beta = 3$ and $\beta = 10$ appear in Figs. 4.6-1 and 4.6-2 respectively. Both curves level off at values close to the corresponding first order DPLL curves. The curves then approach the thermal noise asymptotic curves and then fall off sharply as threshold appears. The input signal-to-noise values at which threshold occurs are

$$\beta = 3, \quad S_i/\eta f_m = 17 \quad dB \qquad (4.6-6a)$$

$$\beta = 10, \quad S_i/\eta f_m = 22 \quad dB \qquad (4.6-6b)$$

This is a substantial improvement over the first order DPLL performance; the threshold extension is 4 dB for $\beta = 3$ and 5 dB for $\beta = 10$.

Computer simulations and experimental measurements for a second order analog phase-locked loop [14] have produced the results displayed in Table 4.6-1, where the digital phase-locked loop results are included for comparison. Notice that both analog and digital phase-locked loops have comparable performances for $\beta = 3$.
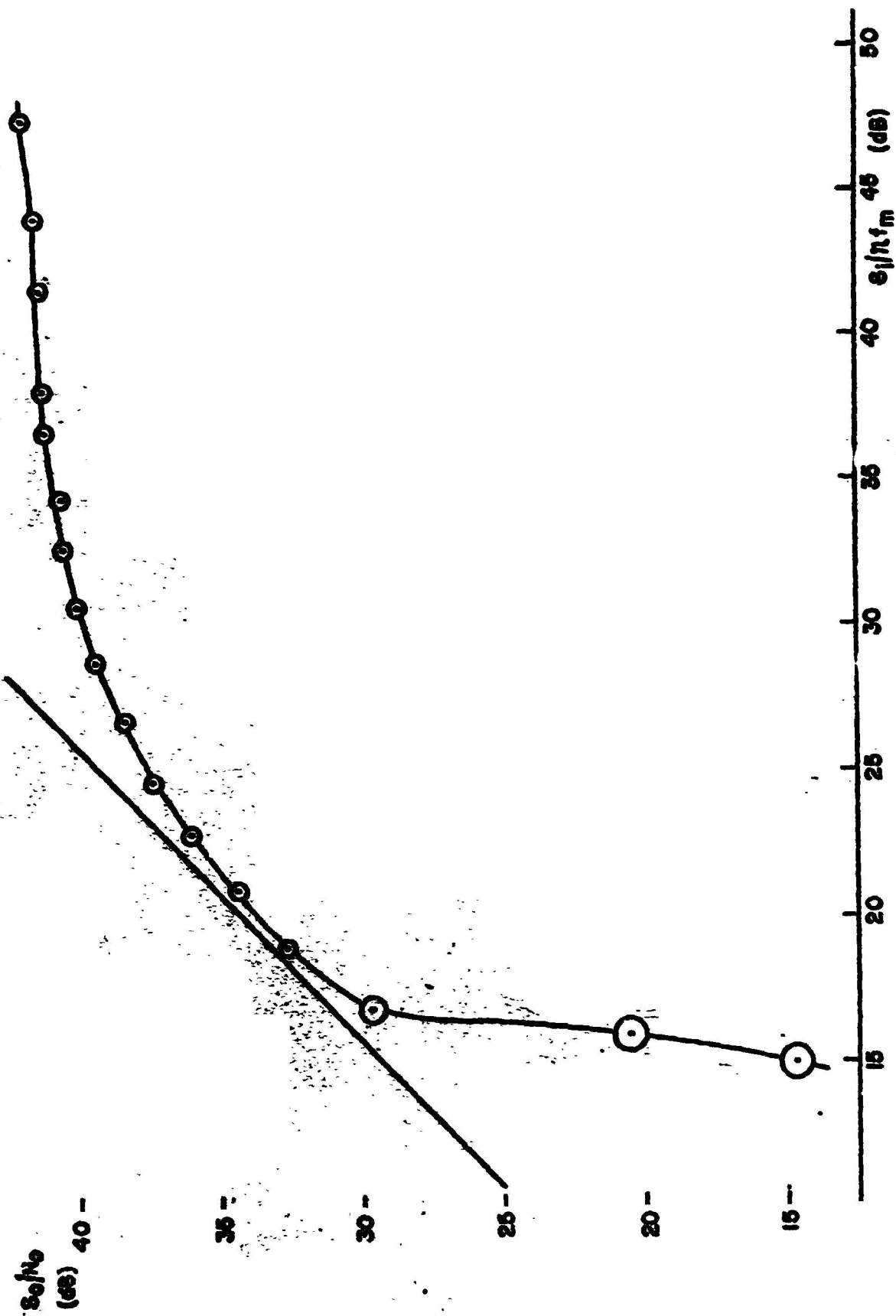
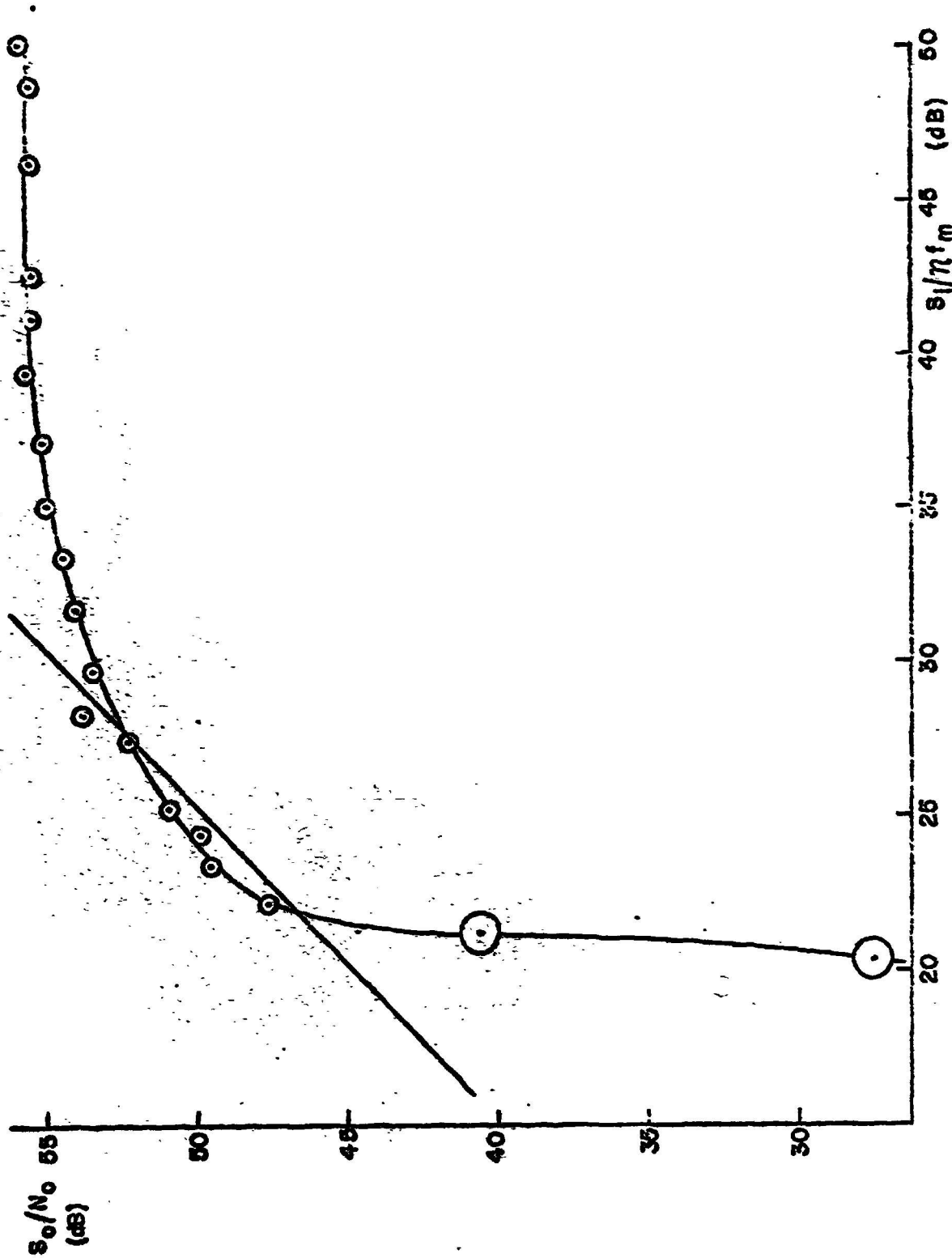Fig.4.8-1. Second order DPLL performance with constant offset modulation and $\beta = 3$.

147

Fig. 4.8-2. Second order DPLL performance with constant offset modulation, $\beta = 10$.

Modulation Index	Threshold ($S_i/\eta f_m$, dB)		
	Analog PLL		Digital PLL
	Theoretical	Experimental	Experimental
3	16.5	16.5	17
12	21.2	21.6	22 ($\beta = 10$)

Table 4.6-1. Comparison of analog and digital phase-locked loop performance.

4.6.2 Results for Sinusoidal Modulation

The second order DPLL was tested with sinusoidal modulation with $\Delta f = 600$ Hz and modulating frequencies of 200 and 60 Hz ($\beta = 3$ and $\beta = 10$ respectively). Using the linear model, the output signal amplitude, A, is

$$A = \beta \frac{(z-1)[(\frac{4}{\pi}g_1 + \frac{4}{\pi}g_2)z - \frac{4}{\pi}]}{z^2 + (\frac{4}{\pi}G_1 + \frac{4}{\pi}G_2 - 2) + (1-\frac{4}{\pi}G_1)} \Bigg|_{z=e^{j2\pi f_m/f_s}} \tag{4.6-7}$$

and the output signal power is

$$S_o = 20 \log A/\sqrt{2} \qquad \text{dB} \tag{4.6-8}$$

The calculated values are

$$\beta = 3, \quad S_o = 3.54 \quad \text{dB} \tag{4.6-9a}$$

$$\beta = 10, \quad S_o = 2.63 \quad \text{dB} \tag{4.6-9b}$$

The calculated values of quantization and truncation are identical to those for constant modulation calculated previously. As the output low pass filter is set at the modulating frequency, we do not include the third harmonic distortion. With no thermal noise added at the input, the measured output noise is

$$\beta = 3, \quad N_o = -35.9 \quad \text{dB} \tag{4.6-10a}$$

$$\beta = 10, \quad N_o = -50.2 \quad \text{dB} \tag{4.6-10b}$$

This noise is attributable to the phase jitter between the carrier frequency and the sampling frequency and is identical to that measured with constant modulation.

The experimentally obtained signal-to-noise curves for sinusoidal modulation appear in Figs. 4.6-3 and 4.6-4. Threshold occurs at the following input signal-to-noise ratios:
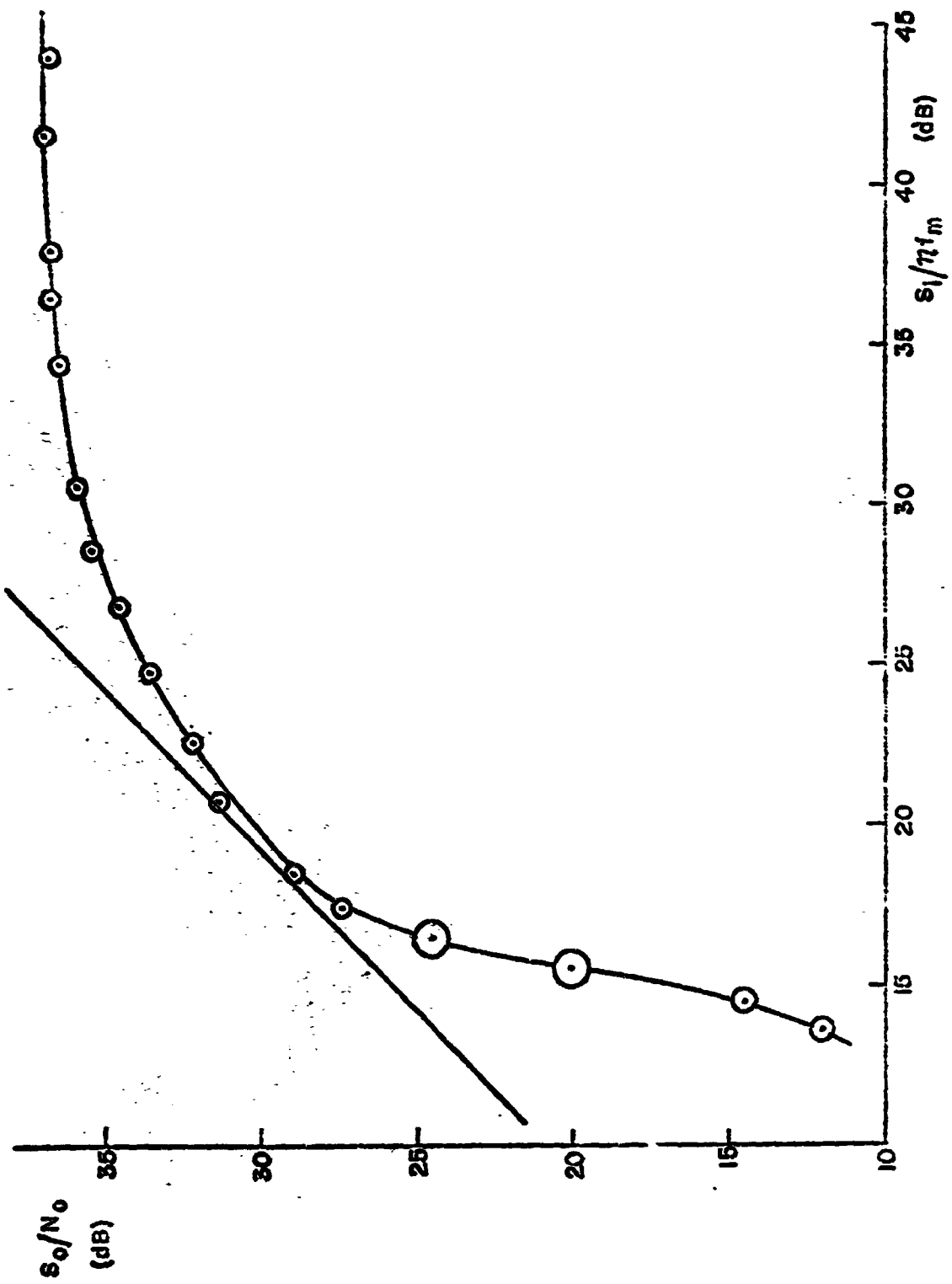
Fig. 4.6-3. Second order DPLL performance with sinusoidal modulation and $\beta = 3$.
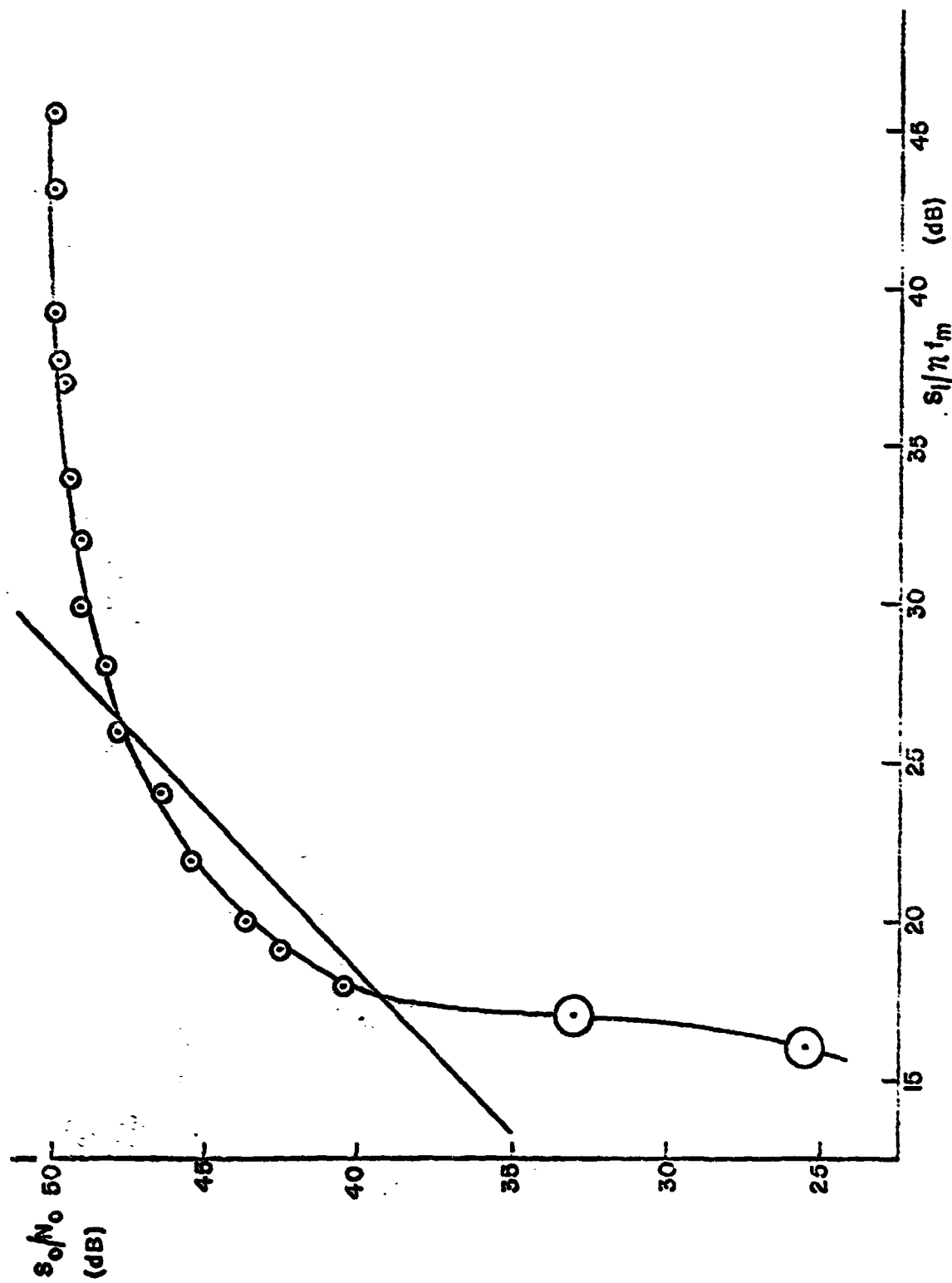
Fig. 4.6-4. Second order DPLL performance with sinusoidal modulation and $\beta = 10$.

$$\beta = 3, \quad S_i/\eta \, f_m = 17 \text{ dB} \qquad\qquad (4.6\text{-}11a)$$

$$\beta = 10, \quad S_i/\eta \, f_m = 18 \text{ dB} \qquad\qquad (4.6\text{-}11b)$$

which represent improvements of 1 dB and 3 dB respectively over the first order DPLL.

4.6.3 Effect of the Number of Bits

The second order DPLL was modified so that only three of the ten bits from the A/D converter were used. As with the first order DPLL, this serves to increase the quantization noise by 42 dB, but the total output quantization noise is still negligible in comparison to the phase jitter noise. However, the phase error signal becomes lost in the increased quantization noise, and we expect a deterioration of threshold.

Fig. 4.6-5 is the experimental results for the second order DPLL using three A/D converter bits, with sinsoidal modulation and $\beta = 3$. Notice that threshold occurs at an input signal-to-noise ratio of 22 dB, which is 5 dB above the threshold obtained using a ten-bit A/D converter. This degradation is very close to that obtained for the first order DPLL.

4.6.4 Effect of Truncation Within the DPLL

As previously mentioned, a truncation of three bits is introduced at the D/A converter, as it can only accept ten bits. We no determine the effect on the DPLL performance of using ten-bit arithmetic throughout the DPLL. This means that after scaling, we truncate the result to ten bits, introducing truncation noise as shown in Fig. 4.6-6.

The noise source N_{T_1} corresponds to a truncation of three bits, while N_{T_2} represents a five-bit truncation. From Eq. (4.5-6), the power spectral densities of these noise sources are

$$G_{N_{T_1}} = 5.5 \cdot 10^{-10} \text{ watts/Hz}$$

$$G_{N_{T_2}} = 6.4 \cdot 10^{-10} \text{ watts/Hz} \qquad\qquad (4.6\text{-}12)$$
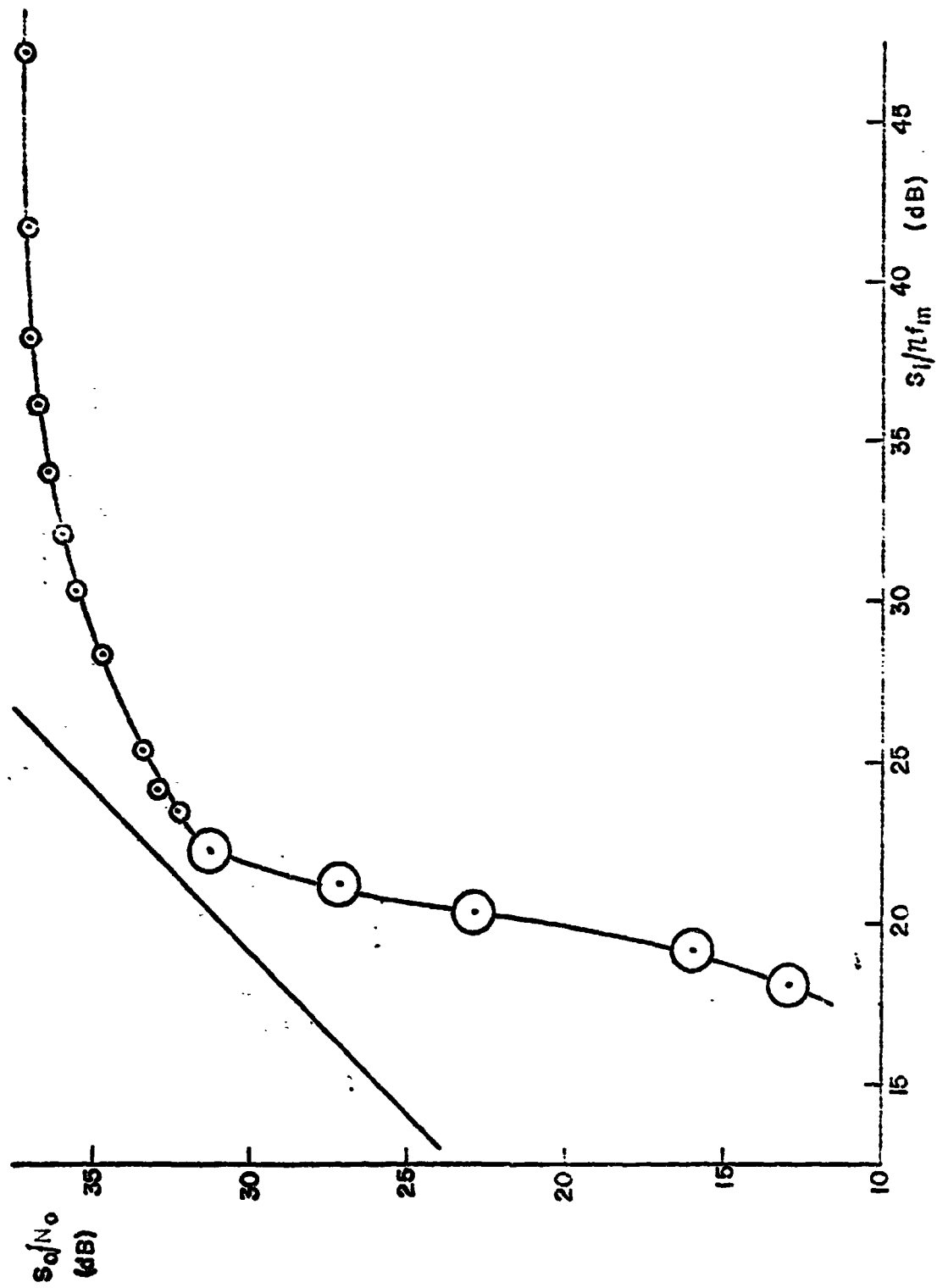
Fig. 4.6.5. Second order DPLL performance with sinusoidal modulation, $\beta = 3$, and a three-bit A/D converter.
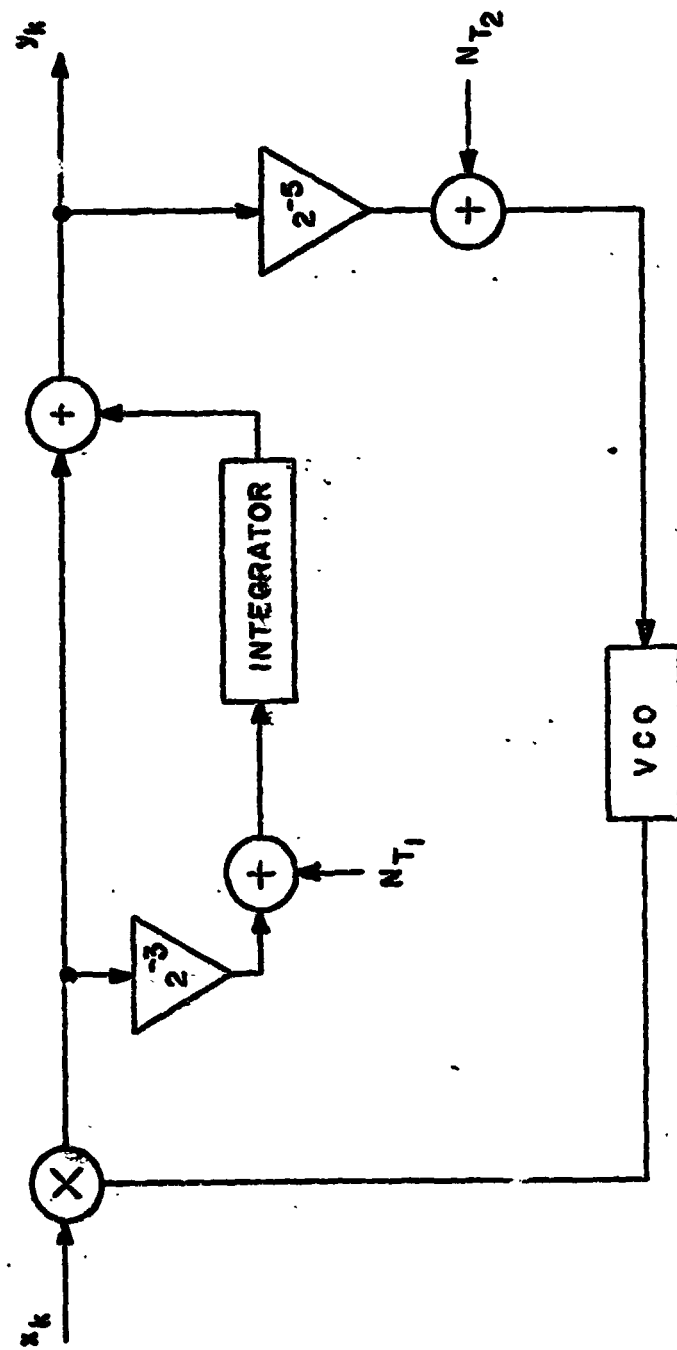
Fig. 4.6-6. Second order DPLL with truncation noise sources added for ten-bit operation.

Using the linearized DPLL model, the transfer functions relating N_{T_1} and N_{T_2} to the output are respectively

$$H_1(f) = \left. \frac{z-1}{z^2 + z\left(\frac{4}{5\cdot 2^4} + \frac{4}{5\cdot 2^7} - 2\right) + \left(1 - \frac{4}{5\cdot 2^4}\right)} \right|_{z=e^{j2\pi f/f_s}}$$

$$H_2(f) = \left. \frac{z\left(\frac{4}{5/2} + \frac{4}{5\,2^2}\right) - \frac{4}{5/2}}{z^2 + z\left(\frac{4}{5\cdot 2^4} + \frac{4}{5\cdot 2^7} - 2\right) + \left(1 - \frac{4}{5\cdot 2^4}\right)} \right|_{z=e^{j2\pi f/f_s}}$$

$$(4.6\text{-}13)$$

Assuming that these noise sources are independent, the output noise is

$$N_T = \int_{-f_m}^{f_m} \left(|H_1|^2 G_{N_{T_1}} + |H_2|^2 G_{N_{T_2}}\right) df \qquad (4.6\text{-}14)$$

Now since $f_m \ll f_s$, we have the approximation for $|f| < f_m$:

$$H_1(f) \approx \frac{2\pi f/f_s}{4/(5\cdot 2^7)}$$

$$H_2(f) \approx 2^5 \qquad (4.6\text{-}15)$$

and the output truncation noise is $N_T = -35.9$ dB. This is precisely the amount of phase jitter noise measured at the output and therefore the output noise should increase to -32.9 dB when ten-bit arithmetic is used.

The above analysis does not provide any information about the ten-bit arithmetic on threshold. This result was obtained experimentally; the signal-to-noise curve is displayed in Fig. 4.6-7. First we observe that the curve levels off at 34 dB, which is the anticipated 3 dB below the
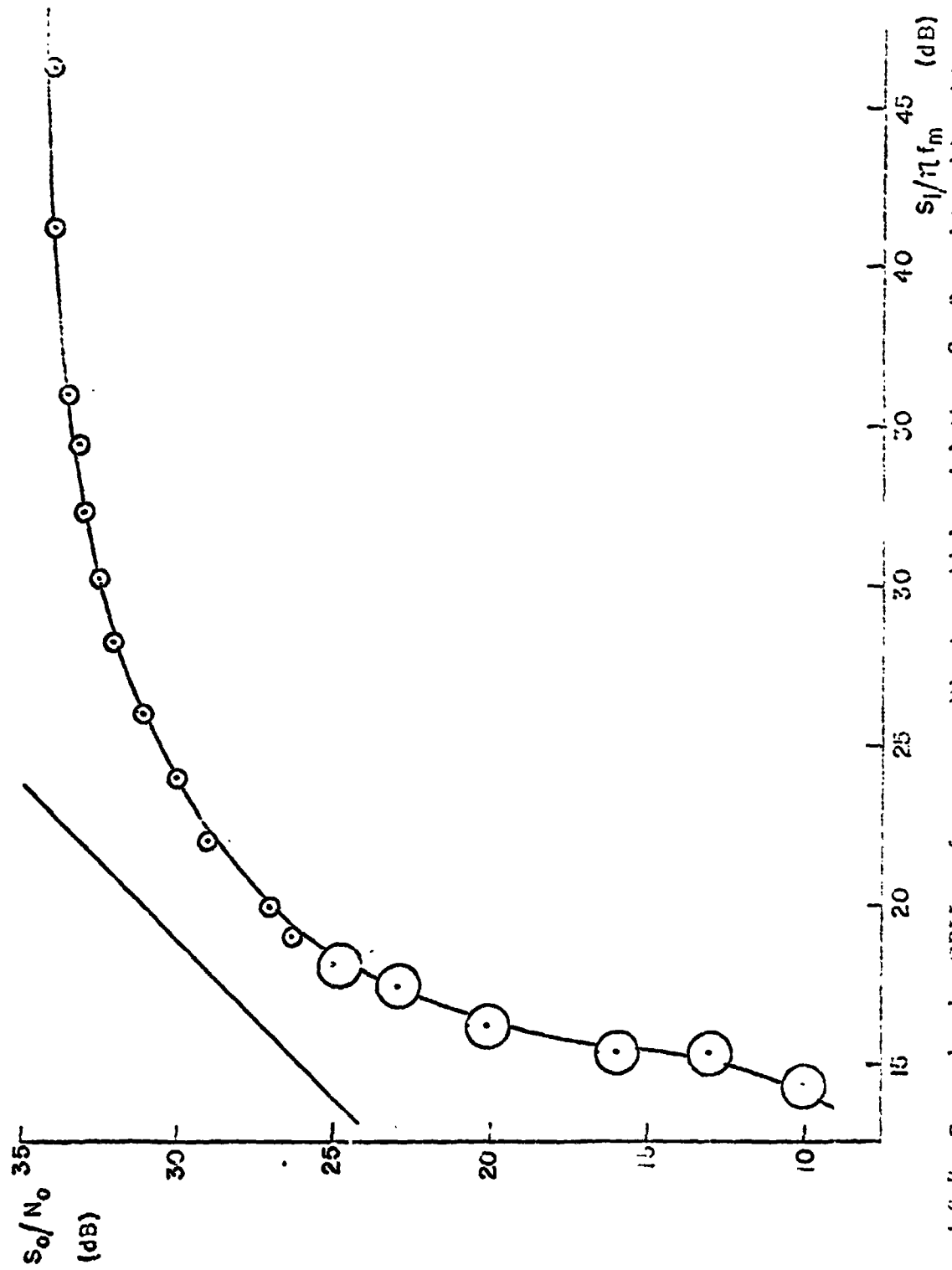
Fig. 4.6.7. Second order DPLL performance with sinusoidal modulation, $\beta = 3$, and ten-bit arithmetic.

curve where no internal truncation is performed. Secondly, we notice that threshold occurs at an input signal-to-noise ratio of 18 dB, which is 1 dB above the original value.

CHAPTER 5

THE THIRD ORDER DIGITAL PHASE-LOCKED LOOP

.1 Third Order DPLL Structure and Equation

The third order DPLL is obtained by adding a double integral path to the forward loop filter of the second order DPLL, resulting in the structure of Fig. 5.1-1. Note that the double integral path is realized by the addition of a single integrator following the existing integrator of the second order DPLL. The gain is labeled g_3/g_2, making the double integral path gain $(g_3/g_2)\, g_2 = g_3$.

Denoting the new integrator output by b_k, and the previous integrator output by a_k, we have the equations

$$b_k = b_{k-1} + (g_3/g_2)a_k \tag{5.1-1a}$$

$$a_k = a_{k-1} + g_2 e_k \tag{5.1-1b}$$

$$y_k = a_k + b_k + g_1 e_k \tag{5.1-1c}$$

which combine to yield the difference equation of the proportional plus integral plus double integral digital filter:

$$y_k = 2y_{k-1} - y_{k-2} + (g_1 + g_2 + g_3)e_k$$
$$- (2g_1 + g_2)e_{k-1}$$
$$+ g_1 e_{k-2} \tag{5.1-2}$$

In addition, we have for the VCO

$$\hat{\phi}_{k+1} = \hat{\phi}_k + G_{VCO} y_k \tag{5.1-3}$$

and the phase error

$$e_k = x_k \, Sq(k\pi/2m + \hat{\phi}_k) \tag{5.1-4}$$

Combining Eqs. (5.1-2), (5.1-3), and (5.1-4) yields the difference equation of the third order digital phase-locked loop:
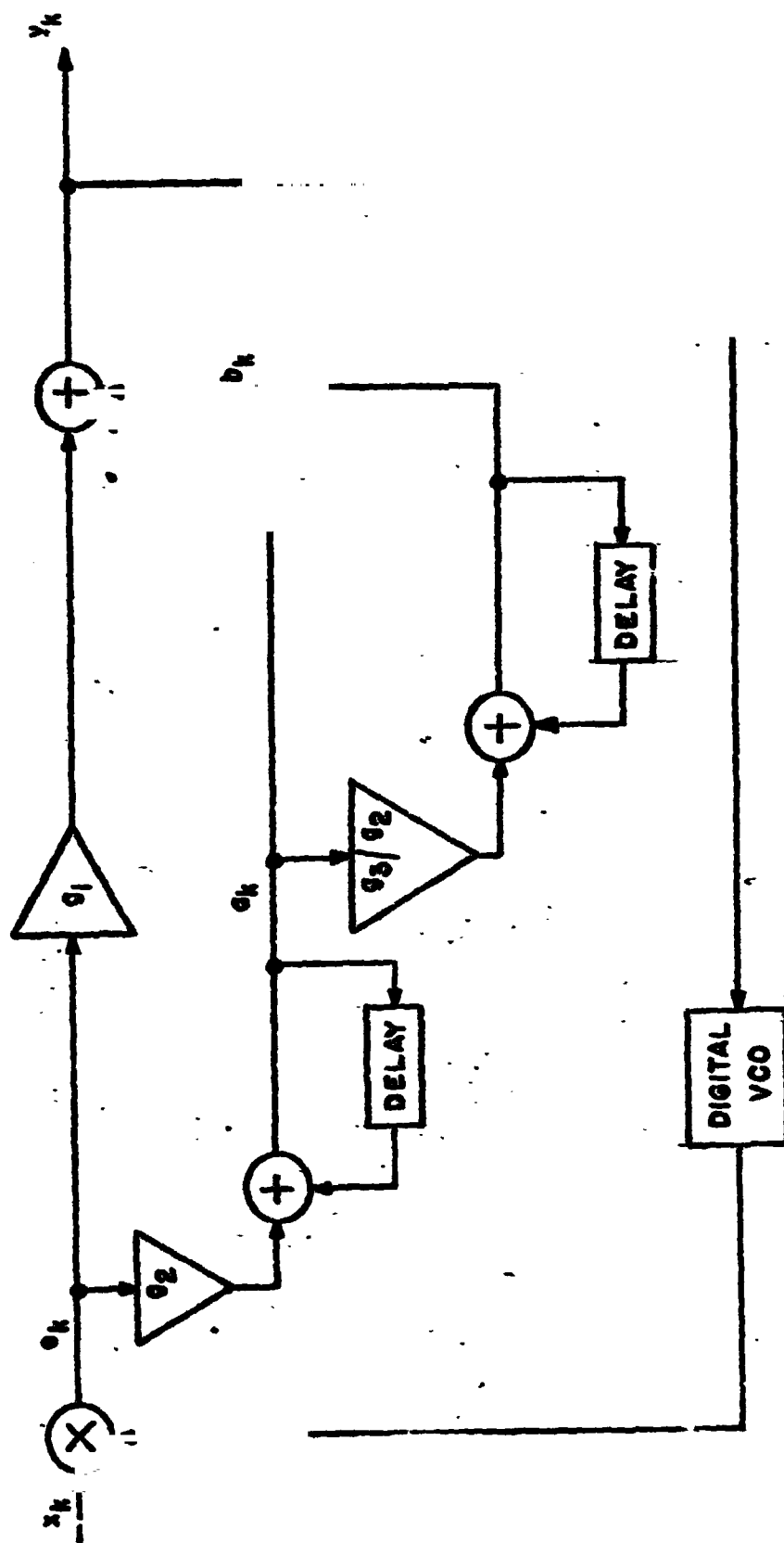
159

Fig. 5.1-1. Structure of the third order DPLL.

$$\hat{\theta}_{k+1} = 3\hat{\theta}_k - 3\hat{\theta}_{k-1} + \hat{\theta}_{k-2}$$

$$+ (G_1 + G_2 + G_3)x_k \, \text{Sq}\,(k\pi/2m + \hat{\theta}_k)$$

$$- (2G_1 + G_2)x_{k-1} \, \text{Sq}\,[(k-1)\pi/2m + \hat{\theta}_{k-1}]$$

$$+ G_1 x_{k-2} \, \text{Sq}\,[(k-2)\pi/2m + \hat{\theta}_{k-2}] \qquad\qquad (5.1\text{-}5)$$

where

$$G_1 = g_1 \cdot G_{VCO} = \text{proportional loop gain}$$

$$G_2 = g_2 \cdot G_{VCO} = \text{integral loop gain}$$

$$G_3 = g_3 \cdot G_{VCO} = \text{double integral loop gain}$$

and

$$x_k = -2\cos(k\pi/2m + \theta_k) + n_k \qquad\qquad (5.1\text{-}6)$$

where

$$\theta_k = \text{input phase}$$

$$n_k = \text{IF noise.}$$

The third order DPLL equation is a third order, nonlinear difference equation in the VCO phase, $\hat{\theta}_k$.

5.2 Stability Condition on the Linearized Model

When the VCO is closely tracking the input pha: ae phase error is approximately

$$e_k = -2\cos(k\pi/2m + \theta_k)\,\text{Sq}\,(k\pi/2m + \hat{\theta}_k)$$

$$\approx (4/\pi)(\theta_k - \hat{\theta}_k) + \text{harmonic terms} \qquad\qquad (5.2\text{-}1)$$

Neglecting the harmonic terms produces the linearized model of the third order DPLL, shown in Fig. 5.2-1. We shall find the restriction on the loop gains for stability.

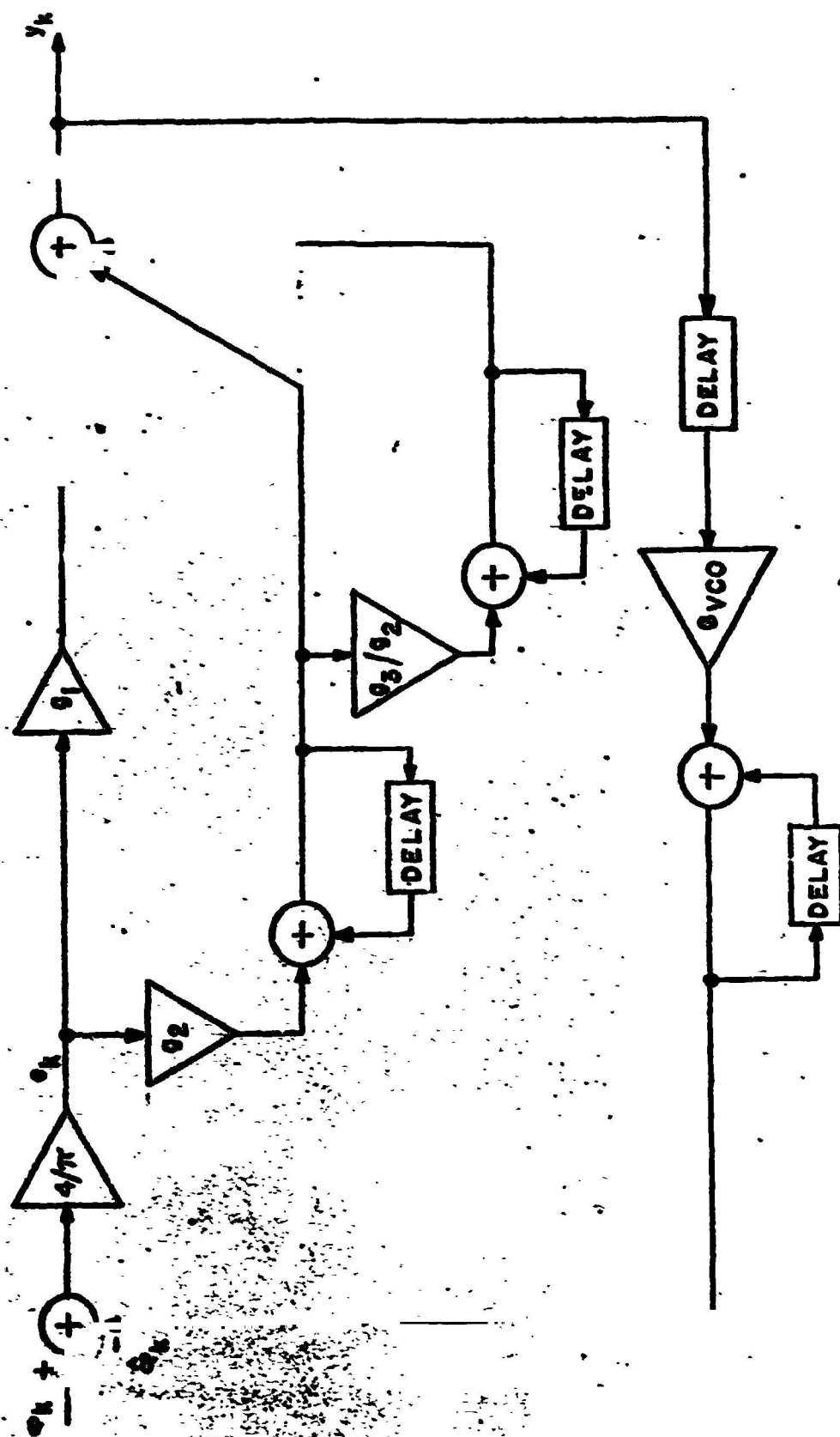The characteristic equation of the linearized model is

Fig. 5.2-1. The linearized model of the third order DPLL.

$$1 + \frac{4}{\pi}\left[G_1 + \frac{G_2}{1-z^{-1}} + \frac{G_3}{(1-z^{-1})^2}\right]\frac{z^{-1}}{1-z^{-1}} = 0 \qquad (5.2\text{-}2)$$

or, equivalently,

$$z^3 + (\frac{4}{\pi}G_1 + \frac{4}{\pi}G_2 + \frac{4}{\pi}G_3 - 3)z^2 + (3 - 2\frac{4}{\pi}G_1 - \frac{4}{\pi}G_2)z$$

$$+ (\frac{4}{\pi}G_1 - 1) = 0 \qquad (5.2\text{-}3)$$

Stability of the linearized model is guaranteed if all the characteristic roots lie inside the unit circle in the z-plane. We make the transformation

$$z = \frac{s+1}{s-1} \qquad (5.2\text{-}4)$$

which maps the interior of the unit circle in the z-plane onto the left half s-plane. The resulting polynomial in s,

$$\frac{4}{\pi}G_3 s^3 + (2\frac{4}{\pi}G_2 + \frac{4}{\pi}G_3)s^2 + (4\frac{4}{\pi}G_1 - \frac{4}{\pi}G_3)s$$

$$+ (8 - 4\frac{4}{\pi}G_1 - 2\frac{4}{\pi}G_2 - \frac{4}{\pi}G_3) = 0 \qquad (5.2\text{-}5)$$

is subjected to a Routh-Hurwitz test which generates the four restrictions:

$$\frac{4}{\pi}G_3 > 0 \qquad (5.2\text{-}6a)$$

$$2\frac{4}{\pi}G_2 + G_3 > 0 \qquad (5.2\text{-}6b)$$

$$8 - 4\frac{4}{\pi}G_1 - 2\frac{4}{\pi}G_2 - \frac{4}{\pi}G_3 > 0 \qquad (5.2\text{-}6c)$$

$$(2\frac{4}{\pi}G_2 + \frac{4}{\pi}G_3)(4\frac{4}{\pi}G_1 - \frac{4}{\pi}G_3) > \frac{4}{\pi}G_3(8 - 4\frac{4}{\pi}G_1 - 2\frac{4}{\pi}G_2 - \frac{4}{\pi}G_3)$$

$$(5.2\text{-}6d)$$

Now from the hardware considerations and the VCO algorithm, the gains are restricted to the form $\pi/5\cdot2^N$, with N a positive integer. Hence all the loop gains are positive and less than unity so that conditions (a), (b), and (c) are satisfied. Condition (d) simplifies to

$$\frac{4}{\pi}G_1\left(\frac{4}{\pi}G_2 + \frac{4}{\pi}G_3\right) \;>\; \frac{4}{\pi}G_3 \qquad\qquad (5.2\text{-}7)$$

and letting

$$G_1 = \pi/5\cdot 2^N$$

$$G_2 = \pi/5\cdot 2^M$$

$$G_3 = \pi/5\cdot 2^L$$

we have the stability condition

$$\frac{1}{2^N}\left[\frac{1}{2^M} + \frac{1}{2^L}\right] \;>\; \frac{5}{4}\cdot\frac{1}{2^L} \qquad\qquad (5.2\text{-}8)$$

5.3 Design of the Third Order DPLL Gains

In designing the third order DPLL we shall use the same sampling frequency, carrier frequency, and modulation as was used with the first and second DPLL's:

sampling frequency, f_s = 50 KHz

carrier frequency, f_0 = $(n + 1/8)$50 KHz

maximum frequency deviation, Δf = 600 Hz

The general design equations were developed in Secs. 2.5 and 2.6 and are repeated here:

$$|e_k| \;\le\; 0.35 \qquad\qquad (5.3\text{-}1)$$

$$f_s/2m - 2\,\Delta f \;\ge\; B_L \qquad\qquad (5.3\text{-}2)$$

where B_L is the bandwidth of the linearized model.

As with the second order DPLL, we consider sinusoidal modulation in imposing the phase error restriction of Eq. (5.3-1). Let the input phase be

$$\varphi_k = \beta\sin k\,2\pi f_m/f_s \qquad\qquad (5.3\text{-}3)$$

where f_m is the modulating frequency. Then the phase error appearing in the linearized model of Fig. 5.2-1 is sinusoidal with amplitude A and phase angle α, where

$$Ae^{j\alpha} = \beta \left. \frac{\frac{4}{\pi}(z-1)^3}{z^3 + z^2\left[\frac{4}{\pi}(G_1+G_2+G_3) - 3\right] + z\left[3 - \frac{4}{\pi}(2G_1+G_2)\right] + (\frac{4}{\pi}G_1-1)} \right|_{z=e^{j2\pi f_m/f_s}}$$

(5.3-4)

Since $f_m << f_s$, we obtain the approximate result

$$Ae^{j\alpha} \cdot \approx \beta(2\pi f_m/f_s)^3 /G_3$$

(5.3-5)

Combining this result with the design condition of Eq. (5.3-1) yields

$$G_3 \geq \beta(2\pi f_m/f_s)^3 /0.35$$

(5.3-6)

Using $\beta = 3$, $f_m = 200$ Hz, and $f_s = 50$ KHz, we have

$$G_3 \geq 1.2 \cdot 10^{-4}$$

(5.3-7)

We shall initially select

$$G_3 = 1.54 \cdot 10^{-4} = \pi/5 \cdot 2^{12}$$

(5.3-8)

As was the case with the second order DPLL, we cannot obtain an expression for the linearized model bandwidth, B_L, in terms of the loop gains. Hence we search the G_1-G_2 plane for those third order DPLL;s which satisfy Eq. (5.3-2), which is

$$B_L < 5.05 \text{ KHz}$$

(5.3-9)

The region of the G_1-G_2 plane that must be searched is restricted by the discrete values of the gains and the stability condition. Having chosen G_3, the stability condition becomes

$$\frac{1}{2^N}\left[\frac{1}{2^M} + \frac{1}{2^{12}}\right] > \frac{5}{4} \cdot \frac{1}{2^{12}}$$

(5.3-10)

165

which is approximately given by

$$N + M < 11 . \tag{5.3-11}$$

(Eq. (5.3-11) is a sufficient condition for Eq.(5.3-10); we note that $N = 1$, $M = 11$ also satisfies Eq. (5.3-10).) A search of this restricted region eliminates the values $M = 1$, 2 as they violate Eq. (5.3-9).

In order to select one third order DPLL from the set of candidates satisfying the design equations, we introduce the spike model and observe the various DPLL responses. The third order nonlinear DPLL difference equation is solved using the FOCAL program appearing in Fig. 5.3-1; Table · 5.3-1 identifies the computer variables with the equation variables. This program is essentially the same as that used in conjunction with the second order DPLL, the only difference being line 2.20, in which the error signal, EK, is integrated to give AK, which in turn is integrated to give BK. Then the VCO phase, PK, is updated using the proportional signal, $G1 * EK$, the integral signal, AK, and the double integral signal, BK. The computations allow a transient time equal to one cycle of modulation (250 computations); also, the initial conditions (VCO phase, and both integrator values) are zero.

The computer results show that all of the third order DPLL candidates lose lock in response to a constant amplitude, 32-sample spike. While we have shown that for small phase errors these loops are stable, an input spike increases the phase error and the behavior predicted by the linear model is no longer valid. It turns out that with $G_3 = \pi/5 \cdot 2^{12}$, the third order DPLL cannot regain lock after a large disturbance.

In an attempt to find a stable third order DPLL, the effect of the double integration was reduced by changing G_3 to $\pi/5 \cdot 2^{13}$. The result again was that any combination of G_1 and G_2 yielded a DPLL that lost lock in response to an input spike.

Further reduction in G_3 to $\pi/5 \cdot 2^{14}$ produces several DPLL's which are stable in response to a constant amplitude, 32-sample duration input spike. These candidates were first subjected to constant amplitude, variable duration spikes to compare their performance with the second order DPLL. Only one, with $N = 3$, $M = 8$, showed improvement in that the input

C-FOCAL, 1969

```
01.10  A  L,M,N,T,E
01.20  S  W=3.14159; S  G1=W/5*2+N; S  G2=W/5*2+M; S  G3=W/5*2+L
01.30  S  PK=0; S  AK=0; S  BK=0
01.40  F  K=-250,1,600; DO  2
01.50  QUIT

02.05  S  H=3*FSIN(2*W*200*K/50000); I  (K*<T-K>)2.15
02.10  S  EK=<2+E>/2+<2-E>*FCOS(2*W*K/T)/2
02.11  S  EK=EK*FSIN(K*W/8+H-W*(1-FCOS<W*K/T>))
02.12  S  EK=EK*FSGN(FCOS<K*W/8+PK>); GOTO  2.2
02.15  S  EK=2*FSIN(K*W/8+H)*FSGN(FCOS<K*W/8+PK>]
02.20  S  AK=AK+G2*EK; S  BK=BK+CK*G3/G2; S  PK=PK+G1*EK+BK+AK
02.25  I  (K)2.9,2.3,2.35
02.30  T  !!!; F  X=0,1,60; T  "."
02.31  T  #
02.35  I  (K/10-FITR(K/10))2.9,2.4,2.9
02.40  F  X=0,1,FITR(40+<10/3>*PK); T  "  "
02.45  T  "*",#; F  X=0,1,40; T  "  "
02.50  T  ".",!
02.90  C
*
```

Fig. 5.3-1. FOCAL program to solve the third order DPLL equation for sinusoidal modulation plus a spike.

Program Variable	Equation Variable
PK	VCO phase, $\hat{\varphi}_k$
AK	Integrator value, a_k
BK.	Second integrator value, b_k
EK	Error signal, e_k
G1	Proportional loop gain, G_1
G2	Integral loop gain, G_2
G3	Double integral loop gain, G_3

Table 5.3-1. The correspondence between the variables appearing in the program of Fig. 5.3-1 and the third order DPLL equation.

168

spike duration could be increased to 67 samples before the DPLL began following the spike. (The second order DPLL began following spikes having a 49-sample duration.) Fig. 5.3-2 is the VCO phase in response to a 68-sample duration, constant amplitude spike, and it is clear that the DPLL follows the spike. If the spike amplitude is permitted to drop to 1 volt, the DPLL does not follow this spike as displayed in Fig. 5.3-3.

When the spike duration is increased to 70 samples, the VCO phase responds in an altogether different fashion. Fig. 5.3-4 is the VCO phase for a 0.5 volt and 0.2 volt minimum spike amplitude. Notice that now the DPLL neither follows the spike nor supresses it; instead, positive spikes are generated. In (a), the DPLL relocks to the sinusoidal modulation with a $+2\pi$ phase error and in the process generates a $+2\pi$-area spike. Note that this spike lasts 110 samples (the input spike lasts 70 samples). In (b), the DPLL relocks with a 4π phase error, generating a 4π-area spike lasting 150 samples. What we observe here is that the DPLL loses lock as a result of both the phase error being increased and the carrier amplitude being decreased by the input spike. In the process of regaining lock, positive spikes are generated, and these spikes have a larger duration and area than the input spike.

An attempt to further decrease G_3 brings no improvement. While the momentary loss of lock phenomenon is not present, the effect of the double integral path is so small so that the third order DPLL behaves essentially as the second order loop. For example, with L = 15, M = 7, - 4 $\ni$ input spike duration can be widened to 47 samples before the `` . μlows it; the second order DPLL with identical proportional loop gain and integral loop gain follows a 49-sample spike. Other gain combinations yield poorer performance than the second order DPLL.

Therefore, we conclude that although a third order DPLL has the ability to suppress more input spikes than a second order DPLL, the third order DPLL also has the tendency to lose lock in response to wide input spikes. While the DPLL regains lock, in doing so it generates spikes whose area may be greater than the area of the input spike.
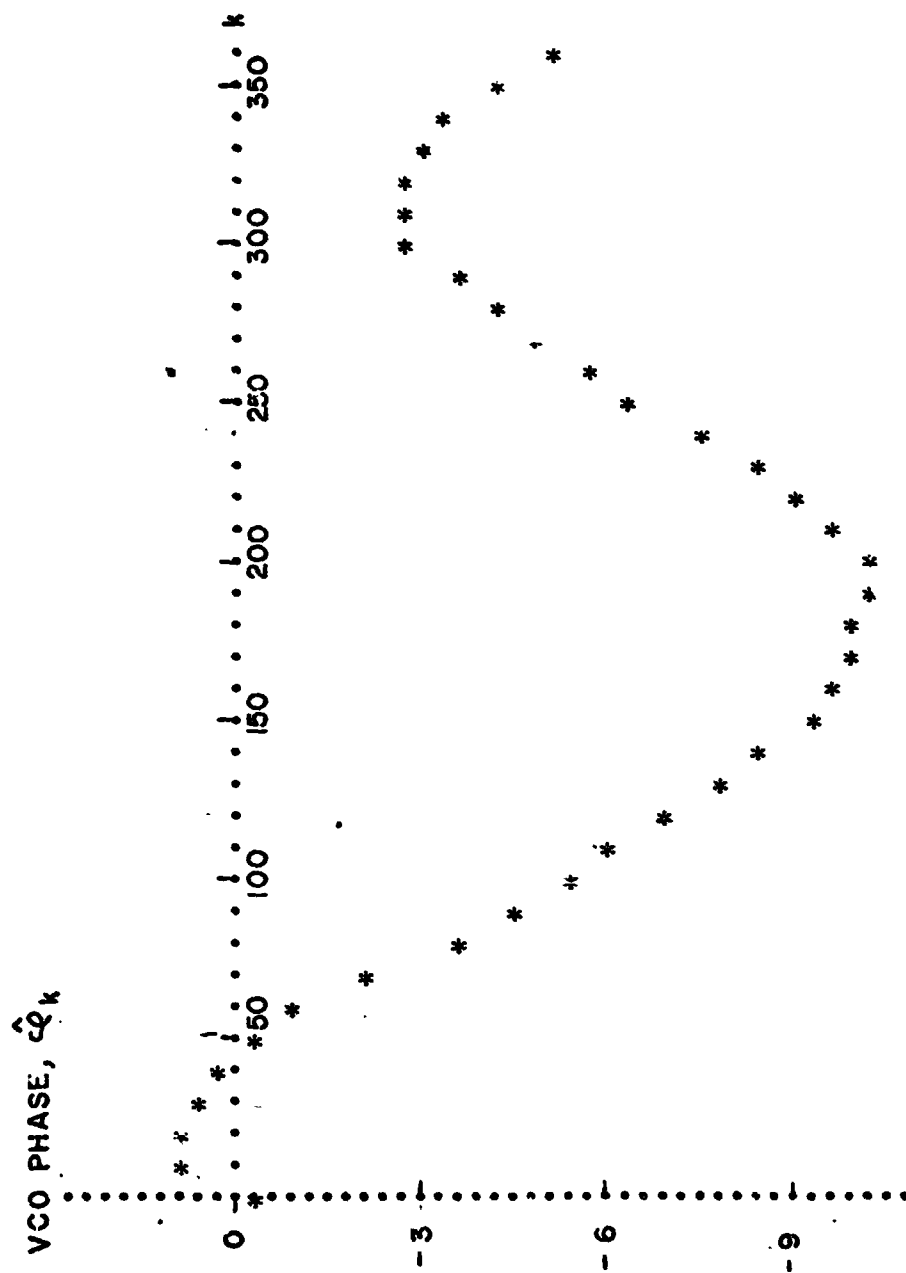
Fig. 5.3-2. Third order DPLL response to sinusoidal modulation plus a 68-sample, constant amplitude spike.
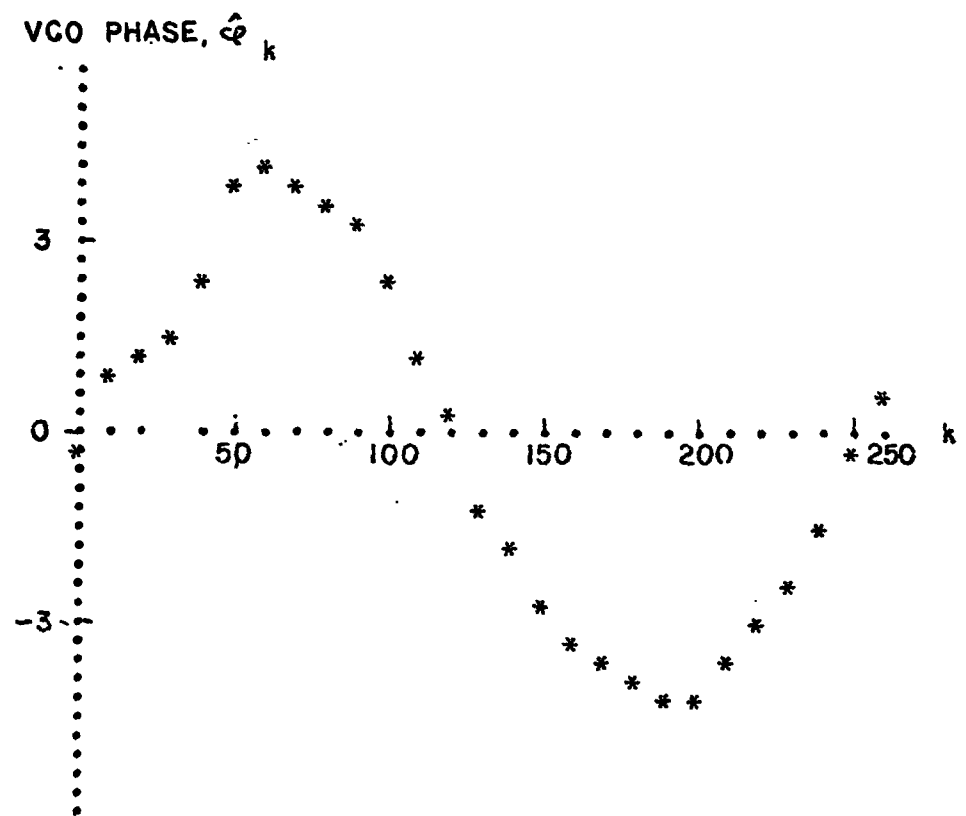
170

Fig. 5.3-3. Third order DPLL resp   ^ t sinusoidal modulation plus a
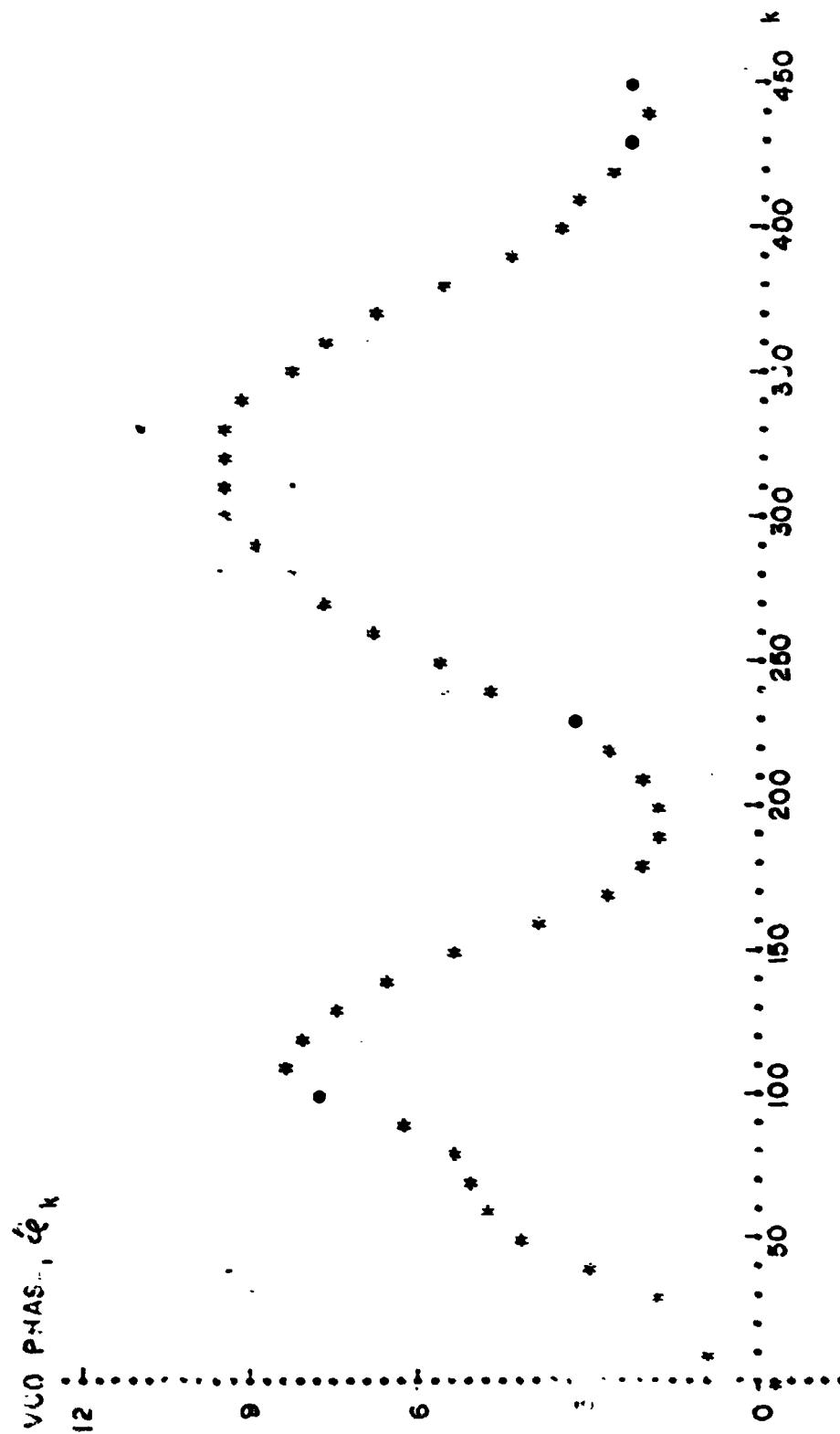68-sample, 1 volt minimum amplitude spike.

Fig. 5.8-4a. Third order DPLL response to sinusoidal modulation plus a 70-sample, 0.5 volt minimum amplitude spike.
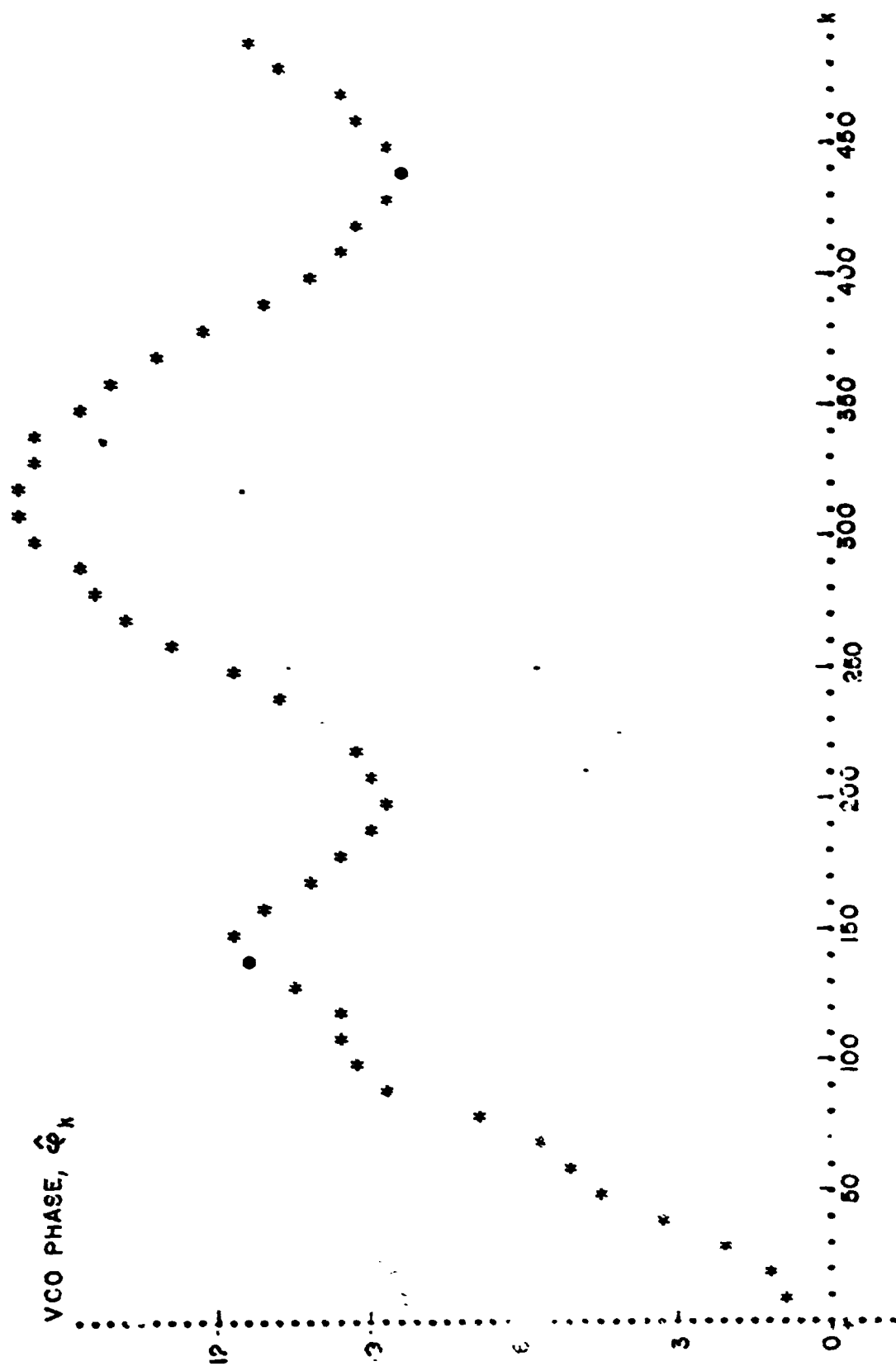
172

Fig. 5.3-4b. Third order DPLL response to sinusoidal modulation plus a 70-sample, 0.2 volt minimum amplitude splice.

173

5.4 Hardware Implementation

In order to experimentally verify the predictions obtained via computer, a third order DPLL having gains

$$G_1 = \pi/5 \cdot 2^3$$
$$G_2 = \pi/5 \cdot 2^8$$
$$G_3 = \pi/5 \cdot 2^{14}$$

was constructed.

The block diagram illustrating the gain locations and values appears in Fig. 5.4-1, where we observe that scaling is performed prior to integration in order to prevent saturation from occuring in the adders. In order to avoid truncation, the registers and associated adders have increased capacity to handle the original ten bits plus the bits introduced by sacling. Notice, in fact, that had only ten bits been used throughout, the DPLL would be identical to a second order DPLL as the double integral term is scaled (shifted) by 11 bits, and would not contribute anything to the output. The VCO output which feeds the exclusive-or multiplier is the third most significant bit introducing the implicit VCO gain of $\pi/(5/2^2)$.

Although five adders are shown in Fig. 5.4-1, only two actually appear in the implemented DPLL. One is the output adder A_5, which employs 21 bits. The other adder performs the functions of A_1, A_2, A_3, and A_4 on a time-shared basis and employs 26 bits to accommodate the VCO computations. The time-shared operation may be understood by referring to Fig. 5.4-2, in which a schematic diagram and timing diagram appear. The sequence of events is as follows:

AT$_1$ (First-integration): The scaled error signal (signal ①) is added to the contents of the forward loop integrator (FLI) register (signal ⑤) and the result is stored in the FLI register, thus integrating the scaled error signal.

AT$_2$ (Second integration): The FLI register contents are scaled (signal ⑦) and added to the second forward loop integrator
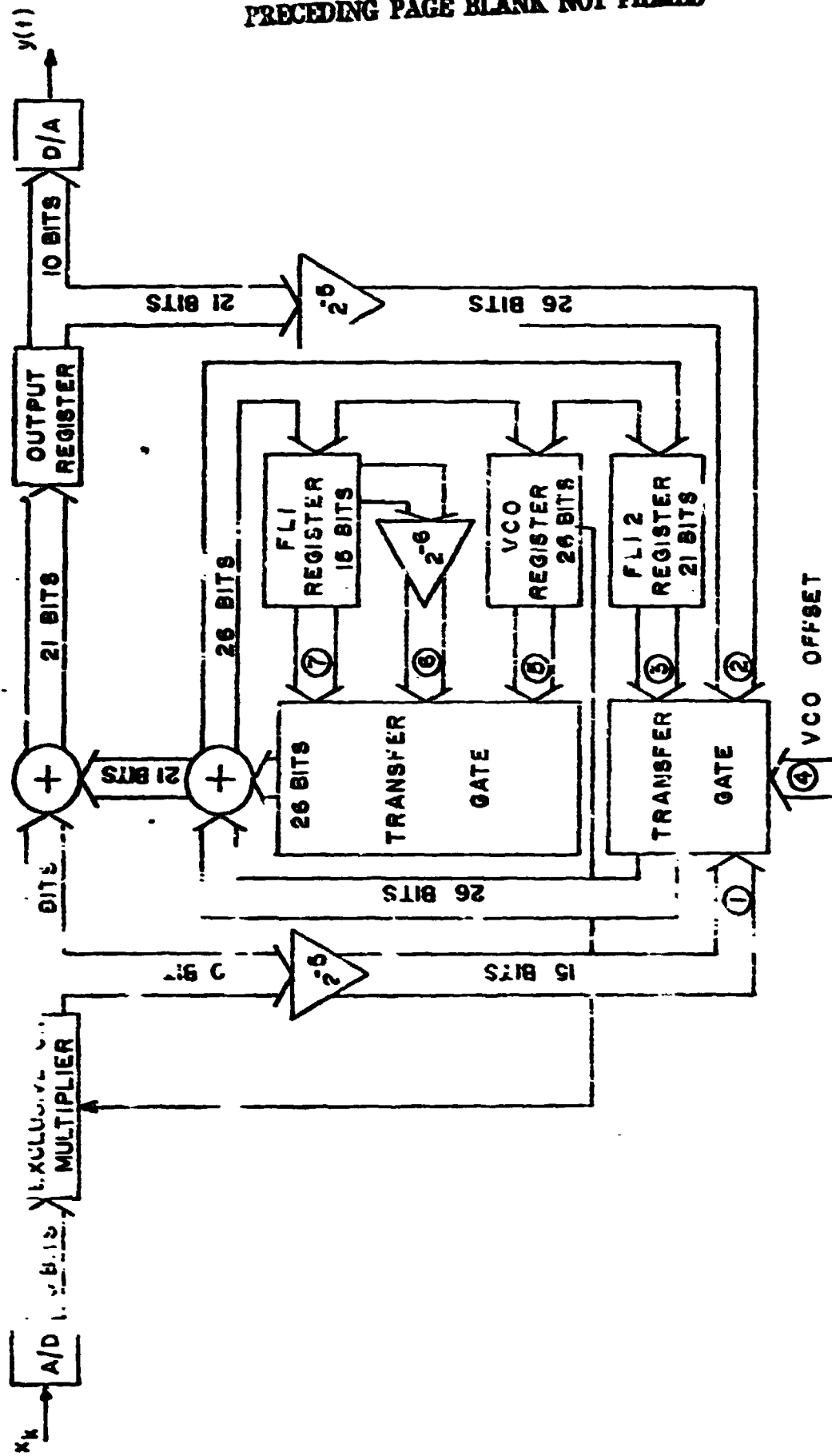
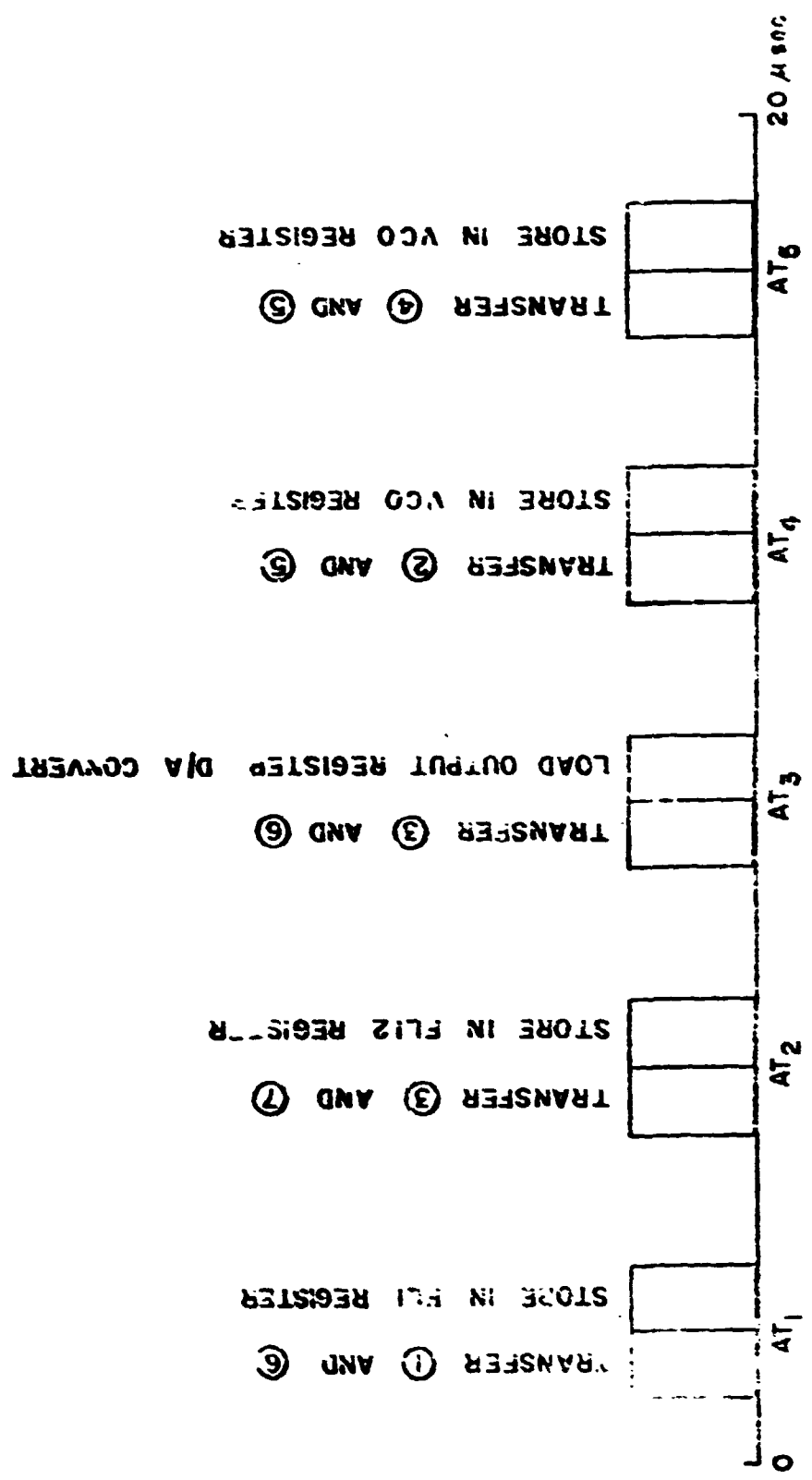Fig. 5.4-2a. Schematic diagram of the third order DPLL.

Fig. 5.4-2b. Timing diagram for the third order DPLL.

(FLI 2) register contents (signal ③) and the result is stored in the FLI 2 register, thus integrating the integrator value, or double integrating the error signal.

AT_3 (Sum of both integrations): The FLI register contents (signal ⑥) · are added to the FLI 2 register contents (signal ③) obtaining the sum of integral plus double integral of the error signal. The result is **not** stored anywhere; however, the output register receives a command to store the output of the 21-bit adder, which at this time is the sum of the error signal plus the integral plus the double integral of the error signal. Also, the D/A converter is made operative, generating the output y_k in analog form.

AT_4 (VCO computation): The scaled output (signal ②) is added to the contents of the VCO register (signal ⑤) and this temporary sum is stored in the VCO register.

AT_5 (VCO computation): The VCO offset ($\pi/2m = \pi/8$) (signal ④) is added to the contents of the VCO register (signal ⑤) and the sum is stored in the VCO register, completing the VCO phase computation. The third bit of the VCO register is used to exclusive-or gate the A/D output, generating the next error signal, e_{k+1}, and the cycle begins again.

The time-shared operation makes it a simple matter to change from third order to second order operation. All we need do is to move the "load output register command pulse" to the second half of AT_2. Then the output register contains the sum of only the proportional plus integral signals, and the DPLL operates as the second order system.

5.5 Output Noise

As with the second order DPLL, the third order DPLL output contains quantization, thermal, truncation, and harmonic noise. However, the harmonic noise is now obtained by filtering the multiplier output through a proportional plus integral plus double integral filter. Also, the D/A converter truncates eleven bits from the 21-bit output register.

5.5.1 Quantization Noise

As a result of converting the sampled input signal to a B-bit binary word, quantization noise is introduced. If the voltages representable by the B-bit words are spaced by S volts, and the quantization error is assumed to be independent from sample to sample, the quantization noise has a power spectral density given by

$$G_{N_q} = S^2 / 12\, T_s \qquad (5.5-1)$$

where T_s is the sampling period.

The linearized DPLL model, Fig. 5.2-1) has the transfer function

$$H(z) = Y(z)/\phi(z) =$$

$$\frac{\frac{4}{\pi}\left[(g_1+g_2+g_3)z^2 - (2g_1+g_2)z+g_1\right]\left[z-1\right]}{z^3 +\left[\frac{4}{\pi}(G_1+G_2+G_3)-3\right]z^2 +\left[3-\frac{4}{\pi}(2G_1+G_2)\right]z +(\frac{4}{\pi}G_1 - 1)} \qquad (5.5-2)$$

For $z = e^{j2\pi f/f_s}$ and $f << f_s$, this transfer function approximates to

$$H(e^{j2\pi f/f_s}) \sim 2\pi f/G_{VCO}\, f_s \qquad (5.5-3)$$

which is the transfer function of a differentiator. The output quantization noise is therefore

$$N_q = \int_{-f_m}^{f_m} |H|^2 G_{N_q}\, df = (2\pi S/G_{VCO})^2 (f_m/f_s)^3/18 \qquad (5.5-4)$$

as was obtained for the second order DPLL.

5.5.2 Thermal Noise

Since the third order DPLL behaves approximately as a differentiator, the output signal-to-noise ratio at high input signal-to-noise ratios is given by the results of Sec. 3.8-1, which are identical to those of an ideal

179

differentiating discriminator:

$$\frac{S_o}{N_o} = 3\beta^2 \frac{S_i}{\eta f_m} \qquad \text{for constant modulation} \qquad (5.5\text{-}5a)$$

$$\frac{S_o}{N_o} = \frac{3}{2}\beta^2 \frac{S_i}{\eta f_m} \qquad \text{for sinusoidal modulation} \qquad (5.5\text{-}5b)$$

5.5-3 Truncation Noise

The result derived in Sec. 4.5-3 for the output truncation noise applies also to the third order DPLL:

$$N_T = \frac{2}{3} S^2 (f_m/f_s)(1 - 2^{-M})(1 - 2^{-M-1}) \qquad (5.5\text{-}6)$$

where **M** is the number of bits truncated.

5.5-4 Harmonic Noise

In the third order DPLL, the harmonics generated at the phase detector are filtered by a proportional plus integral plus double integral digital filter having the transfer function $T(z)$:

$$T(z) = g_1 + g_2 \frac{1}{1 - z^{-1}} + g_3 \frac{1}{(1 - z^{-1})^2} \qquad (5.5\text{-}7)$$

For $z = \exp(j2\pi f/f_s)$ with $f \ll f_s$, the transfer function becomes approximately

$$T(z) \approx g_3 / (2\pi f/f_s)^2 \qquad (5.5\text{-}8)$$

When constant modulation is introduced, the carrier frequency is deviated by Δf Hz and the third order DPLL track ... frequency deviation with zero phase lag:

$$\hat{\omega}_k = \omega_k = 2\pi \Delta f/f_s \qquad (5.5\text{-}9)$$

The harmonic distortion terms are identical to those in the second order

DPLL:

$$D = \frac{4}{\pi} \frac{8m}{16m^2 - 1} \sin k \, 2\pi \, 4m \, \Delta f / f_s \tag{5.5-10}$$

and the filtered output amplitude is

$$|D| = \frac{4}{\pi} \cdot \frac{8m}{16m^2 - 1} \cdot \frac{g_3}{(2\pi 4m \, \Delta f / f_s)^2} \tag{5.5-11}$$

producing the output noise

$$N_D = 20 \log \frac{4}{\sqrt{2} \, \pi} \cdot \frac{8m}{16m^2 - 1} \cdot \frac{g_3}{(2\pi 4m \, \Delta f / f_s)^2} \quad \text{dB} \tag{5.5-12}$$

When the carrier is sinusoidally modulated at f_m Hz with a modulation index β, the input phase is

$$\varphi_k = \beta \sin k \, 2\pi f_m / f_s \tag{5.5-13}$$

At this frequency, the transfer function from input phase to VCO phase in the linearized model is approximately $1\angle 0$, and therefore,

$$\hat{\varphi}_k \approx \varphi_k \tag{5.5-14}$$

Hence the harmonic distortion terms are identical to those of the second order DPLL and contains odd harmonics of the modulating frequency. The $(2n+1)^{st}$ harmonic appears in the output with amplitude

$$|D_{2n+1}| = \frac{4}{\pi} \cdot \frac{8m}{16m^2 - 1} \, 2J_{2n+1}(4m\beta) \frac{g_3}{[2\pi(2n+1)f_m / f_s]^2} \tag{5.5-15}$$

and contributes noise in the amount

$$N_{D_{2n+1}} = 20 \log |D_{2n+1}| / \sqrt{2} \quad \text{dB} \tag{5.5-12}$$

This noise component will appear in the output only if the frequency $(2n+1)f_m$ is below the output low pass filter cutoff frequency.

181

5.6 Experimental Results

The third order DPLL was tested using the loop gains

proportional loop gain, $G_1 = \pi/5 \cdot 2^3$

integral loop gain, $G_2 = \pi/5 \cdot 2^8$

double integral loop gain, $G_3 = \pi/5 \cdot 2^{14}$

The computer results of Sec. 5.3 show that this set of gains yields a stable DPLL which momentarily loses lock in response to input noise spikes.

The parameters used in the signal-to-noise measurements are:

sampling frequency, $f_s = 50$ KHz

carrier frequency, $f_o = 53.125$ KHz

modulating frequency, $f_s = 200$ Hz

modulation index, $\beta = 3$

Fig. 5.6-1 is the third order DPLL performance curve for sinusoidal modulation. We observe that threshold occurs at an input signal-to-noise ratio of 24 dB, which is 6 dB worse than the first order DPLL. The reason for this poor performance is found by examining the DPLL output, where one observes spikes extending over a full cycle of modulation. Such spikes are not simply reproductions of the input spikes but rather are the result of the DPLL losing lock. When the input noise is increased the output spike durations increase as the DPLL is thrown farther out of lock and requires a longer transient to regain lock.

The above statements are clearly illustrated in Fig. 5.6-2 where there appear photographs of the third order DPLL output when the input signal-to-noise ratio is 13 dB. In (a) we obs ordinary noise spikes appearing in the sinusoidal output signal. In (b) the oscilloscope sweep speed has been reduced to observe many of the output and we observe that the DPLL loses lock of the sinusoidal modulation and requires about six cycles of modulation to relock. Note that in addition, we observe the ordinary noise spikes occasionally appearing in the output. Finally, in
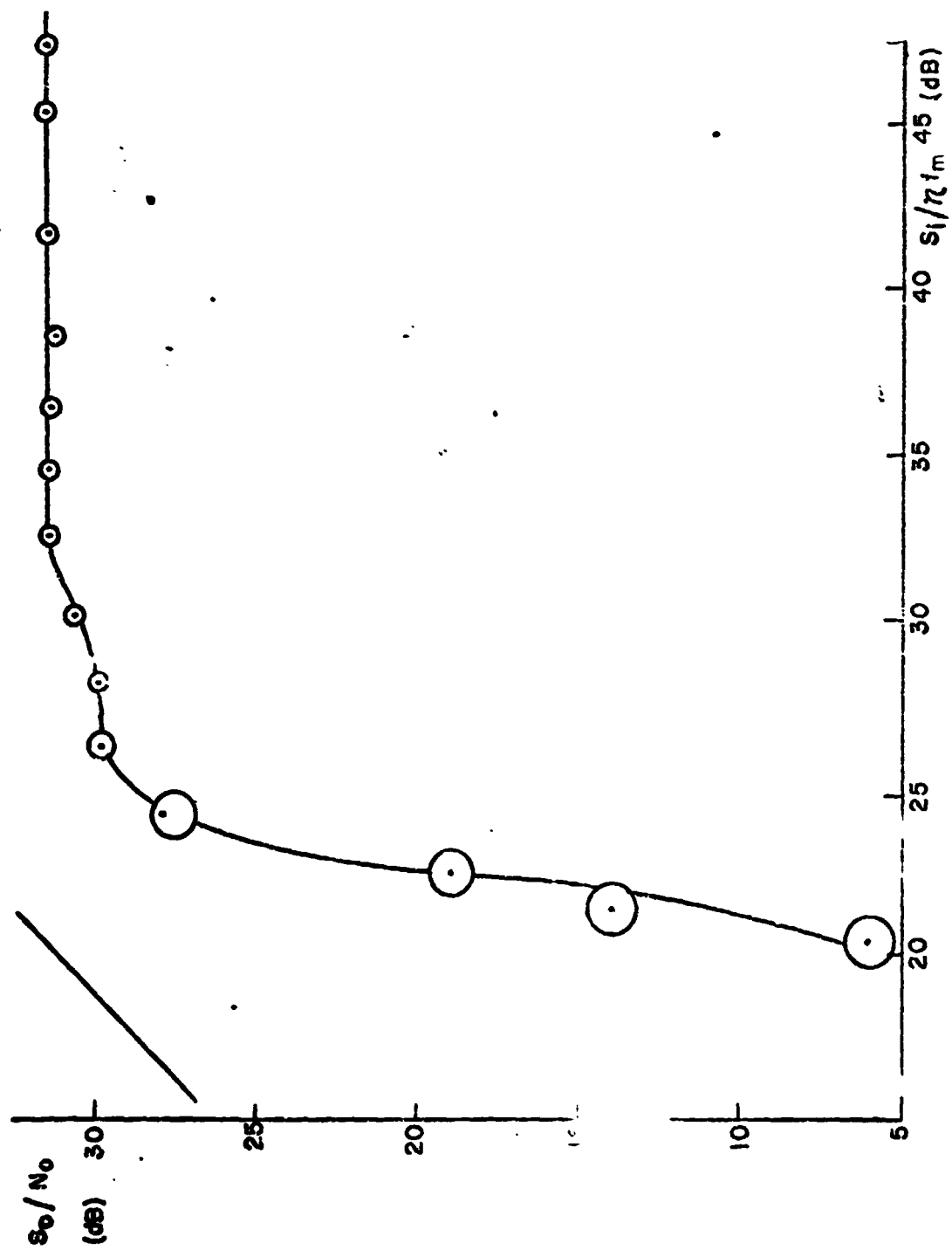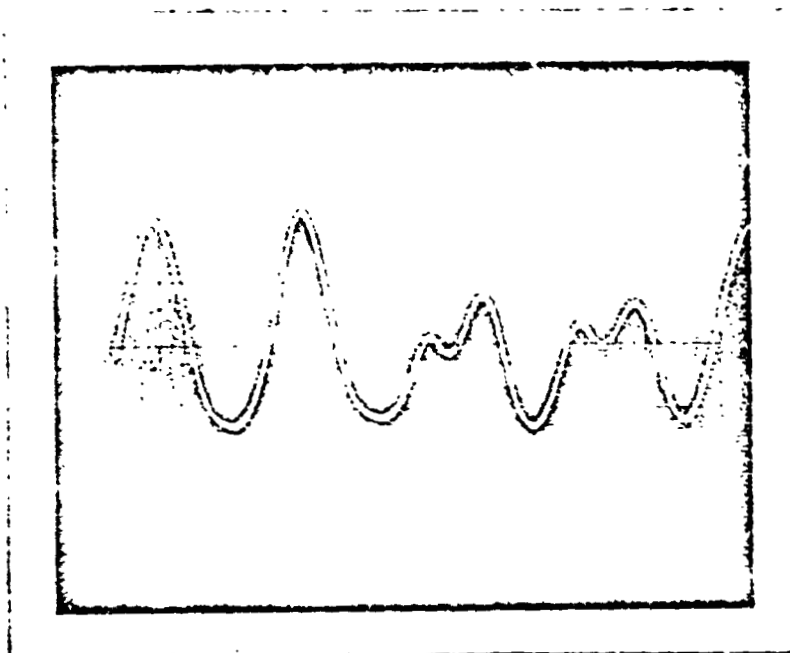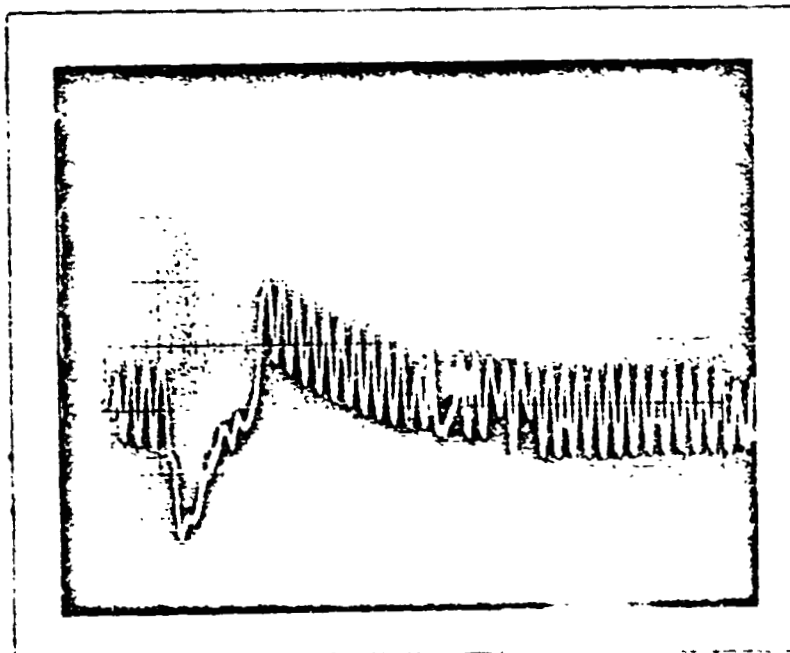
Fig. 5.6-1. Third order DPLL performance with sinusoidal modulation and $\beta = 3$.
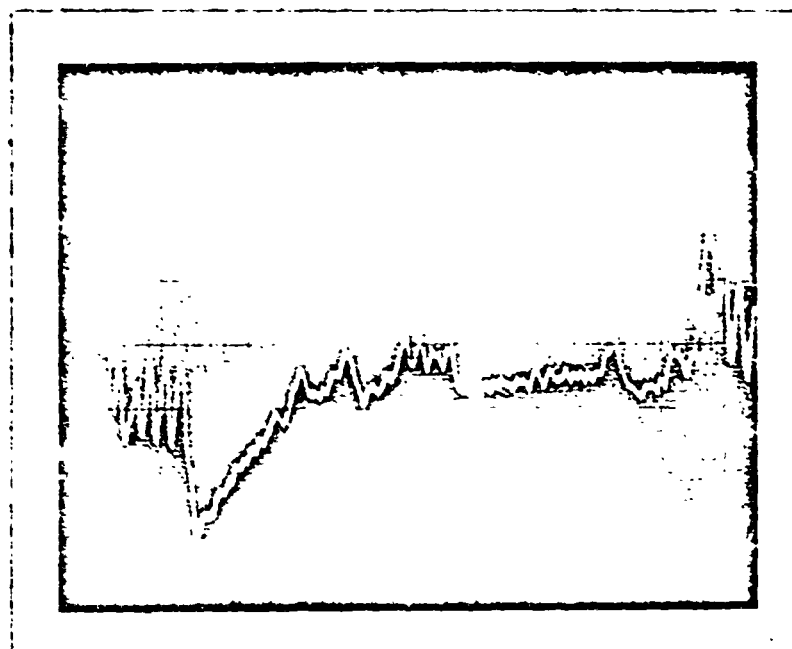
(a)

(b)

Fig. 5.6-2. Third order DPLL output with 300 Hz sinusoidal modulation and an input signal-to-noise ratio of 13 dB. In (a), observe input noise spikes being reproduced at the output while in (b), observe the loss of lock.

(c)

Fig 5.6-2c. Illustrating third order DP; L losing lock to the sinusoidal modulation.

(c), a more severe loss of lock is di. piayed, with the DPLL requiring about 34 cycles of modulation to regain lock. It is precisely this loss of lock which contributes significantly to the output noise and is respon-sible for the degradation in performance of the third order DPLL.

The third order DPLL performance with constant offst .odulation appears in Fig. 5.6-3, where we observe that threshold occurs at an input signal-to-noise ratio of 17 dB, which is identical to threshold for the second order DPLL. However the third order DPLL occe ionally loses lock and this accounts for the steeper slope below thr ol. than for the sec-ond order DPLL which retains lock even after an input spike Note for example that at $S_i/\eta f_m = 15$ dB, we have $S_o/N_o = 19$ dB for the second order DPLL and $S_o/N_o = 15$ dB for the third order D. L.

A computer simulation [14] for a third order analog phase-locked loop predicts $S_i/\eta f_m = 15.8$ dB at threshold; experimental results yielded [14] $S_i/\eta f_m = 16.3$, which is only a 0.2 dB improvement over the sec-ond order analog phase-locked loop. Notice that the same phenomenon occurs with the digital phase-locked loops; the third order DPLL provides no threshold improvement over the second order DPLL.

A photograph of an output spike appears in Fig. 5.5-4, for which the input signal frequency is deviated 600 Hz above the carrier frequency and the input isgnal-to-noise ratio is 14 dB. The spike is negative, as are all the spikes, since the input signal frequency is deviated to its positive ex-teme. We may calculate the theoretical area of the output spike and com-pare it to the experimentally obtained value.

When the DPLL follows an input noise spike, the VCO phase increases by 2π radians. The DPLL output, y_k, is related to the VCO phase, $\hat{\phi}_k$, via

$$\hat{\phi}_{k+1} - \hat{\phi}_k = (1/2^3)\, y_k \qquad (5.6-1)$$

and assuming a spike occurs during the interval $k = 1$ to $k = K$, the summa-tion of the output values is
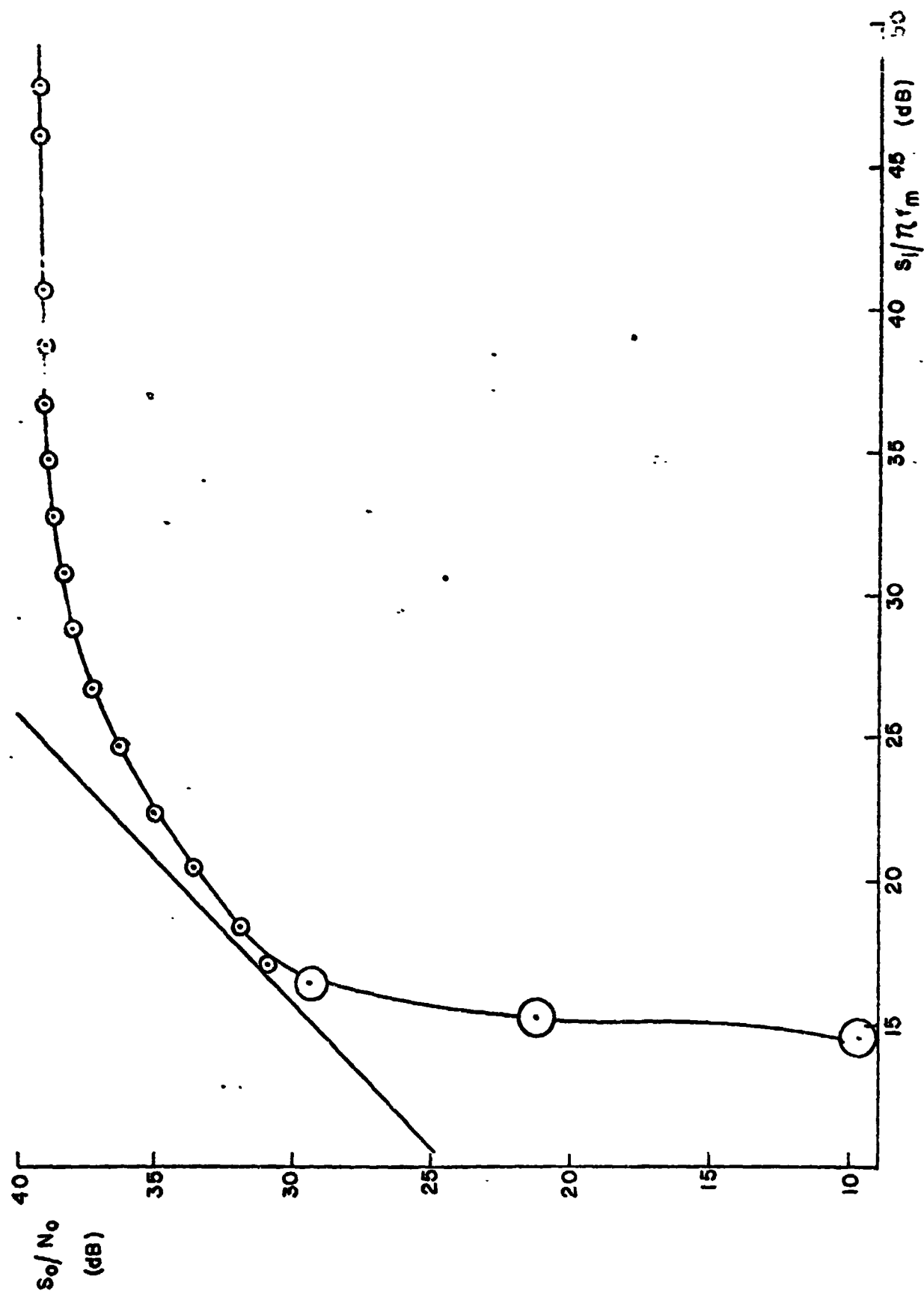
Fig. 5.6-3. Third order DPLL performance with constant offset modulation and $\beta = 3$.
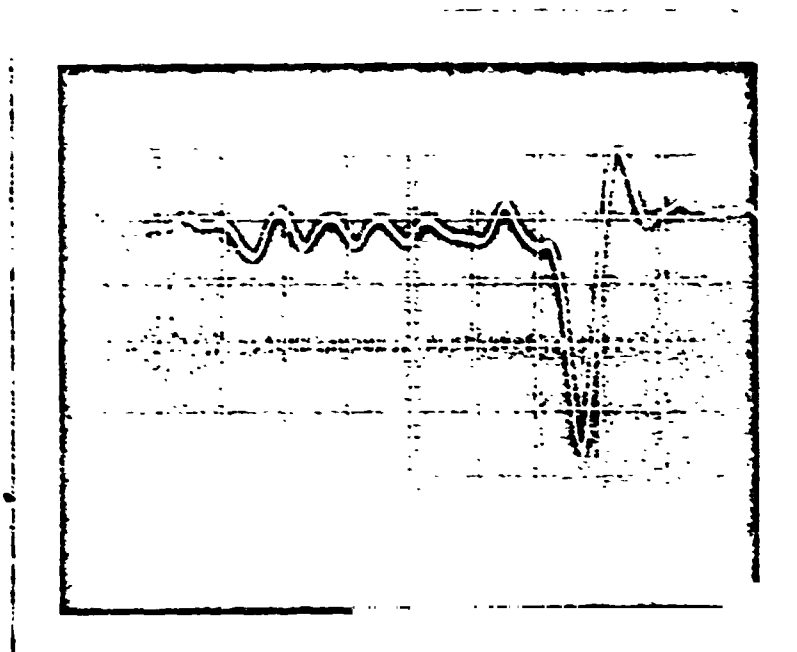
Fig. 5.6-4. A thermal noise spike appearing in the third order DPLL output when the carrier frequency is deviated by 600 Hz and $S_i / \eta f_m = 14$ dB.
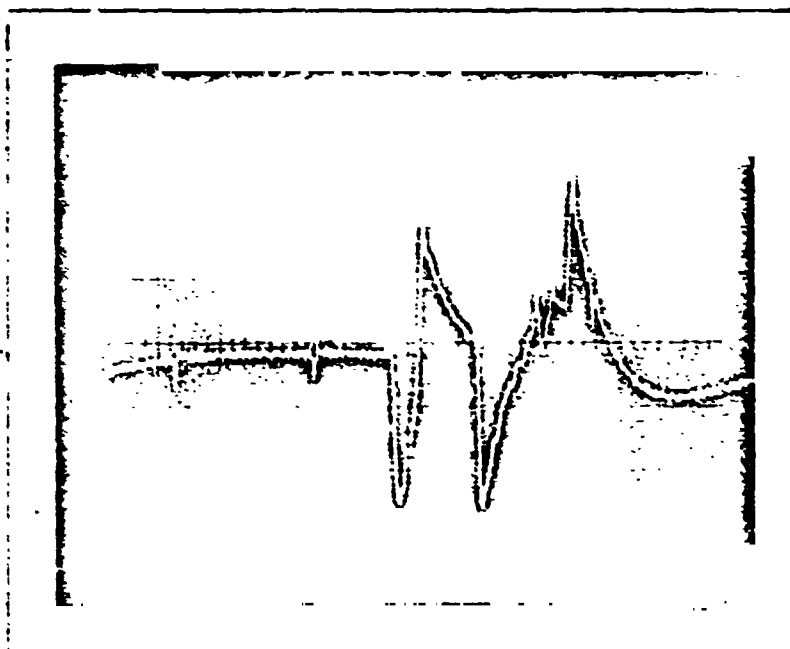

Fig. 5.6-5. Illustrating the third order DPLL loss of lock in response to an input spike.

$$\sum_{k=1}^{K} y_k = (40/\pi)(\dot{\phi}_{K+1} - \dot{\phi}_1) = \ldots = 80 \text{ volts} \tag{5.6-2}$$

As each y_k represents the output voltage over the entire sampling period, $T_s = 20 \mu$ sec., the area under the output spike is

$$T_s \sum_{k=1}^{K} y_k = 1.6 \text{ mv-sec} \tag{5.6-3}$$

Approximating the spike of Fig. 5.6-4 by a triangle, the beneath it is approximately

$$\text{Area} = \frac{1}{2} (0.8 \text{ cm})(3.6 \text{ cm})(0.2 \text{ v/cm})(5 \text{ msec/cm}) = 1.44 \text{ mv-sec.} \tag{5.6-4}$$

in good agreement with the theoretical value.

The DPLL loss of lock is illustrated in Fig. 5.6-5 in which the oscilloscope sweep is slowed to 50 msec/cm. To put this picture into proper perspective, recognize that the two small spikes to the left of the large ones are thermal noise spikes similar to that of Fig. 5.6-4. The relative sizes of these spikes clearly demonstrates that the DPLL loss of lock contributes significantly to the output noise.

CHAPTER 6

CONCLUSIONS

In this concluding chapter, a summary is presented of what has been accomplished by this thesis, and how it compares with other phase-locked loop analyses and experiments; in addition, a discussion is given concerning what problems have not yet been solved.

The all digital phase-locked loop featured in this dissertation was originated by J. Gardnick, D. L. Schilling, and this author. It is completely digital in nature; i.e., beyond the A/D converter, all signals in the DPLL are binary words. Within the DPLL, there is no conversion back to an analog signal for the purpose of tuning a voltage controlled oscillator. In fact, there is no oscillator or counter within the DPLL; instead there is an algorithm to determine the value an oscillator would have at the sampling instant. In this way, we generate the oscillator output only at the time that its value is needed for other computations.

Another feature of the DPLL presented here is its synchronous, real-time operation. The sampling frequency is constant and all the required arithmetic and logic operations are performed within one sampling period, generating an output sequence whcih is converted to analog form and filtered. An equation (developed in Sec. 2.2) relating the sampling frequency to the carrier frequency must be satisfied to guarantee proper DPLL operation. The synchronous operation enables a time-shared operation of one DPLL to demodulate several FM signals simultaneously.

To obtain the real-time operation of the DPLL the VCO is designed so that its output has two possible values, corresponding to a square wave oscillator. This eliminates the need for a binary multiplication at the phase detector as a multiplication by ±1 is accomplished using ex-

clusive-or gating. While the use of a square wave VCO simplifies the DPLL hardware, it greatly complicates the analysis of the non-linear, DPLL difference equation. A unique feature of this equation is that its solution does not converge to zero in response to a carrier input but approaches a periodic sequence having an average value of zero. This behavior results directly from the absence of any filtering immediately after the phase detector multiplier.

The transient response to an unmodulated carrier could be obtained only for the first order DPLL and for the case of no input thermal noise. The time to gain lock as a function of initial VCO phase and loop gain cannot be expressed in closed form but is presented graphically. When an integrator is added to the forward path (yielding the second order DPLL), not even a graphical solution could be developed. (Compare to [21] where a stability analysis could be performed only for a first order system.) As a result, no information about the acquisition performance of the second and third order DPLL's was obtained. No attempt was made to pursue such an investigation.

The purpose of this work was to design, develop, and analyze a digital phase-locked loop for FM demodulation and threshold extension. To obtain information about the DPLL performance at low input signal-to-noise ratios, a model of an input noise spike was introduced, and the DPLL equation was solved using a digital computer. This procedure could not predict where threshold occurs, but could only provide a comparison between first, second, and third order DPLL's and a differentiating discriminator. Despite this limitation, the spike model was successful in finding a second order DPLL which yielded a five dB threshold extension beyond that of a first order DPLL. This improvement is obtained for constant offset modulation with a modulating index of 10. Furthermore, the spike model predicted the momentary loss of lock of the third order DPLL in response to an input spike, and it was this loss of lock that deteriorated the third order DPLL performance, producing no

threshold extension beyond the second order DPLL for constant offset modulation and threshold deterioration for sinusoidal modulation. This is an extremely important "negative result". In the past, investigators have discussed the threshold extension of higher order loops. Here, we have shown that threshold extension does not occur.

The experimental results obtained show that the second order DPLL provides as much threshold extension as does an analog phase-locked loop [14]. Furthermore, it is demonstrated that no additional extension is obtained by a third order DPLL, as was previously demonstrated experimentally with analog phase-locked loops [14].

The experimental results also show the effect of the number of bits used on the threshold signal-to-noise ratio. It is found that in reducing the number of bits in the A/D converter from 10 to 3, threshold is deteriorated by 5 dB. In addition, if 10-bit arithmetic is used throughout the DPLL (thus introducing truncation error), threshold suffers a deterioration of 1 dB.

The fact that maximum threshold extension occurs for constant offset modulation suggests that further research be conducted in applying the DPLL for demodulating M-ary FSK signals. In this respect, the transient behavior of the DPLL must be investigated when the input frequency deviation abruptly changes. Also, the DPLL acquisition perfor- in the presence of noise must be examined.

FIRST ORDER DPLL TRANSIENT RESPONSE--

HARMONICS NOT INCLUDED

Here we consider the transient response to an unmodulated carrier by the first order digital phase-locked loop in which the square wave VCO harmonics are suppressed. The equation describing the system is Eq. (3.2-1), repeated here:

$$\hat{\phi}_{k+1} = \hat{\phi}_k - (4G/\pi) \sin \hat{\phi}_k \qquad (A1-1)$$

If $0 < 4G/\pi < 2$ then any initial $\hat{\phi}_0$ except π (mod $\pm$ to 2π) generates a sequence whose limit is zero (modulo 2π). In general, the sequence has infinite length; however, for certain isloated values of $\hat{\phi}_0$ (which depends on the loop gain G), the sequence has finite length (i.e., the transient lasts a finite time).

Theorem A-1. The sequence generated by Eq. (A1-1) converges to zero (modulo 2π) if $0 < 4G/\pi < 2$ and $\hat{\phi}_0 \neq \pi$ (modulo 2π).

Proof: Observe that because of the $\sin \hat{\phi}_k$ term, the sequence is unchanged by a $2\pi n$, n an integer, shift; hence we consider $-\pi < \phi_0 < \pi$ only.

First restrict the gain G so that

$$0 < 4G/\pi < 1$$

Then the sequence is monotonic decreasing and bounded from below if $0 \leq \hat{\phi}_0 < \pi$, while the sequence is monotonic increasing and bounded from above if $-\pi < \hat{\phi}_0 < 0$. Hence the sequence converges and it is clear from Eq. (A1-1) that the limit is zero.

Next, consider

$$1 \leq 4G/\pi < 2$$

Then the curves $(4G/\pi) \sin \hat{\phi}$ and $\hat{\phi}$ intersect at $\hat{\phi} = \pm \hat{\phi}_1$ in the interval $(-\pi, \pi)$, as shown in Fig A1-1. Note that if $\hat{\phi}_0 = \hat{\phi}_1$, then $\hat{\phi}_1 = 0$ and
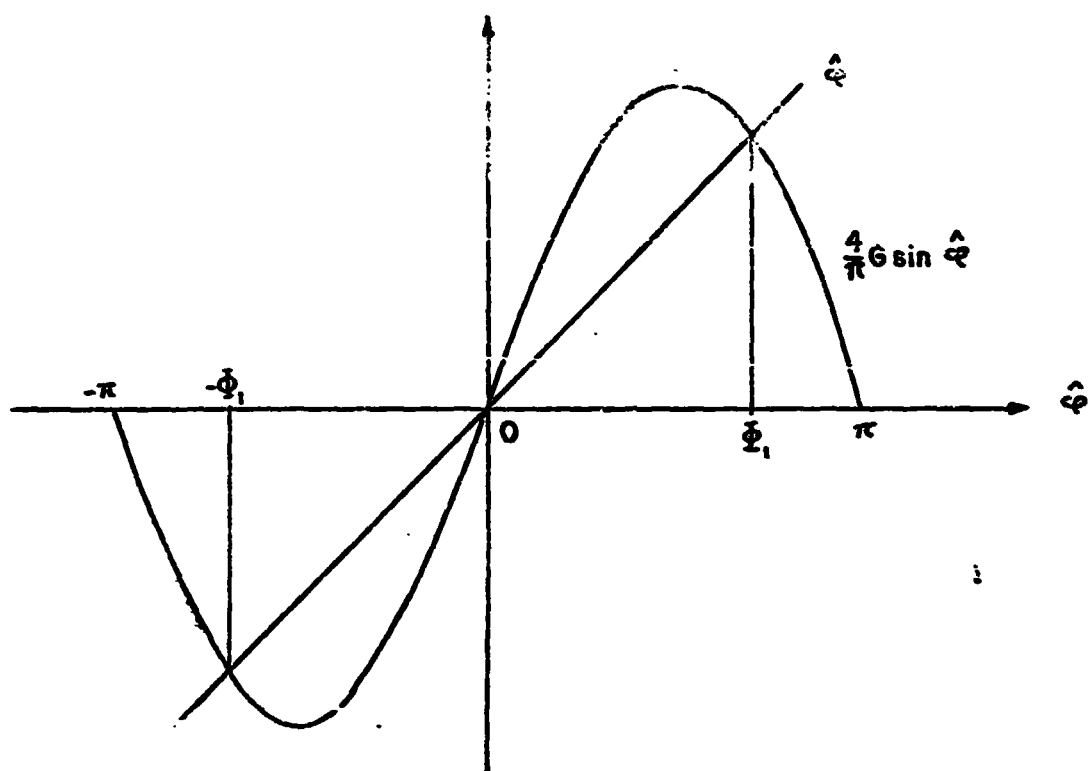
Fig. A1-1. The determination of Φ_1.

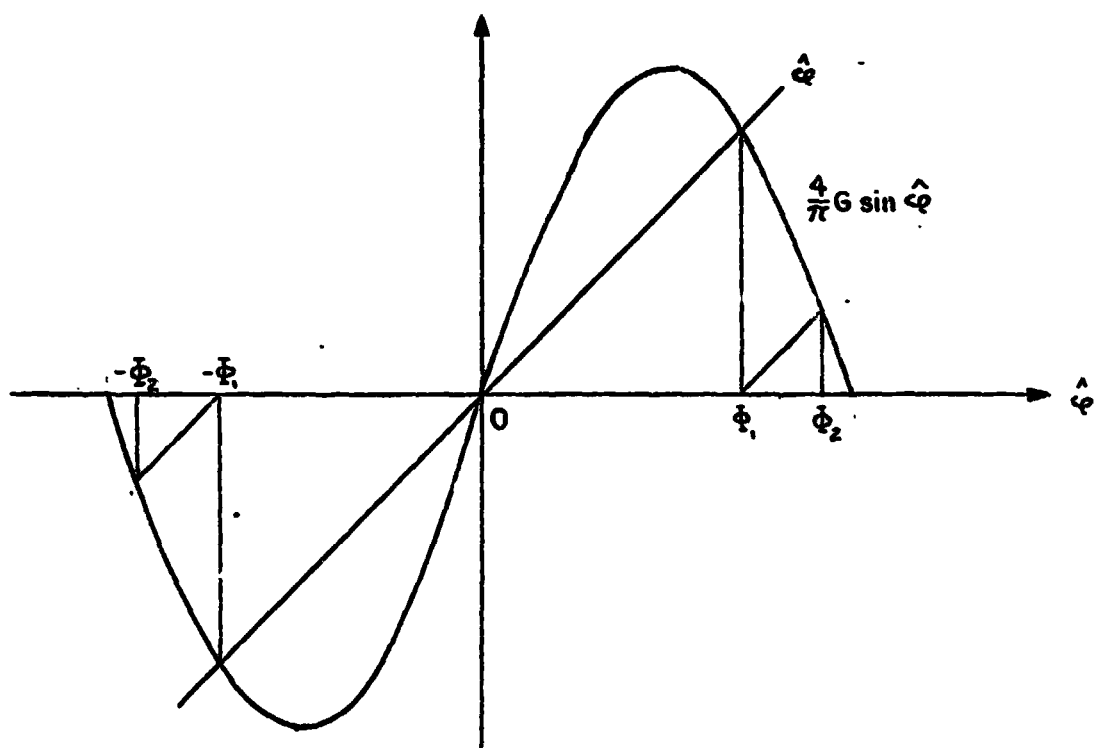Fig. A1-2. The determination of Φ_2.

194

$\hat{\varphi}_k = 0$ for $k \geq 2$; we reach the steady state after one iteration. If $|\hat{\varphi}_0| < \Phi_1$, the sequence alternates in sign but decreases in magnitude:

$$|\hat{\varphi}_{k+1}| < |\hat{\varphi}_k|$$

For when $0 < \hat{\varphi}_0 < \Phi_1$, we have $\hat{\varphi}_1 = \hat{\varphi}_0 - (4G/\pi) \sin \hat{\varphi}_0 < 0$ and $-\hat{\varphi}_1 < \hat{\varphi}_0$ since $(\sin \hat{\varphi}_0)/\hat{\varphi}_0 < 2/(4G/\pi)$ as $(4G/\pi) < 2$. A similar argument holds when $-\Phi_1 < \hat{\varphi}_0 < 0$. Hence the sequence $|\hat{\varphi}_k|$ converges and from Eq. (A1-1), $|\hat{\varphi}_k| \longrightarrow 0$. Therefore, $\hat{\varphi}_k \longrightarrow 0$.

If $\Phi_1 < |\hat{\varphi}_0| < \pi$, there are two regions to consider:

$$\Phi_1 < |\hat{\varphi}_0| < \Phi_2$$
$$\Phi_2 < |\hat{\varphi}_0| < \pi$$

where Φ_2 is the VCO phase required to generate Φ_1 at the next iteration:

$$\Phi_1 = \Phi_2 - (4G/\pi) \sin \Phi_2$$

The value Φ_2 is shown geometrically in Fig. A1-2. Note that if $\hat{\varphi}_0 = \pm \Phi_2$, then $\hat{\varphi}_1 = \pm \Phi_1$, and $\hat{\varphi}_k = 0$ for $k \geq 2$; i.e., the transient requires two iterations.

When $\Phi_1 < |\hat{\varphi}_0| < \Phi_2$, we have $0 < |\hat{\varphi}_1| < \Phi_1$, since the curve $\sin \varphi$ is between the two straight lines, φ and $\varphi - \Phi_1$ (see Fig. A1-2). Hence $\hat{\varphi}_k \longrightarrow 0$.

For $|\hat{\varphi}_0| > \Phi_2$, we again partition this interval at $\pm \Phi_3$ where

$$\Phi_2 = \Phi_3 - (4G/\pi) \sin \Phi_3$$

Now $\hat{\varphi}_0 = \pm \Phi_3$ generates the sequence $\hat{\varphi}_1 = \pm \Phi_2$, $\hat{\varphi}_2 = \pm \Phi_1$, $\hat{\varphi}_k = 0$, for $k \geq 3$ and the transient consists of three iterations. If $\Phi_2 < |\hat{\varphi}_0| < \Phi_3$, then $\Phi_1 < |\hat{\varphi}_1| < \Phi_2$, and $\hat{\varphi}_k \longrightarrow 0$.

This partitioning process is continued indefinitely yielding the points $\Phi_1, \Phi_2, \ldots, \Phi_n, \ldots$ given by

$$\Phi_1 = (4G/\pi) \sin \Phi_1$$

$$\dot{\phi}_k = \dot{\phi}_{k+1} - (4G/\pi) \sin \dot{\phi}_{k+1} \qquad k \geq 2$$

If $\phi_0 = \dot{\phi}_r$, then the transient is finite, requiring n iterations, while if $\phi_0 \neq \dot{\phi}_n$, the transient requires an infinite number of iterations.

FIRST ORDER DPLL TRANSIENT RESPONSE--

HARMONICS INCLUDED

In this appendix we prove the assertions made in Sec 3.3 about the first order DPLL transient where the VCO waveform is a square wave.

Theorem A2-1. If $0 < 2G < \pi/2m$ and

$$\sum_{p=0}^{n-1} 2G \cos p\pi/2m + (r-1)\pi/2m \leq \hat{\phi}_o < \sum_{p=0}^{r} 2G \cos p\pi/2m + r\pi/2m \qquad (A2-1)$$

then

$$w_k = Sq(k\pi/2m + \hat{\phi}_k) = \begin{cases} +1, \ 0 \leq k \leq 2m-r \\ -1, \ 2m-r < k \leq 2m \end{cases} \qquad (A2-2)$$

where $0 \leq r \leq 2m$.

Proof: We must show that

$$0 \leq k\pi/2m + \hat{\phi}_k < \pi \quad \text{for} \quad 0 \leq k \leq 2m-r$$

$$\pi \leq k\pi/2m + \hat{\phi}_k < 2\pi \quad \text{for} \quad 2m-r < k \leq 2m \qquad (A2-3)$$

These conditions may be simplified by observing that the VCO argument, $k\pi/2m + \hat{\phi}_k$, is an increasing function of k. This is true because $\Delta\hat{\phi}_k = Ge_k \geq -2G > -\pi/2m$. Hence the conditions of Eq. (A2-3) reduce to four conditions:

(i) $\quad 0 \leq \hat{\phi}_o$

(ii) $\quad (2m-r)\pi/2m + \hat{\phi}_{2m-r} < \pi \qquad (0 \leq r \leq 2m)$

(iii) $\quad \pi \leq (2m-r+1)\pi/2m + \hat{\phi}_{2m-r+1} \qquad (0 \leq r \leq 2m)$

(iv) $\quad 2m\pi/2m + \hat{\phi}_{2m} < 2\pi$

Proof of these four inequalities is straightforward.

(1) From the hypothesis,

$$\hat{\phi}_0 \ge \sum_{p=0}^{r-1} 2G \cos p\pi/2m + (r-1)\pi/2m = \sum_{p=0}^{r-1} (2G \cos p\pi/2m + \pi/2m) > 0$$

(ii) From the VCO operation,

$$\phi_{2m-r} = \phi_0 + G \sum_{p=0}^{2m-r-1} (+1)(-2G \cos p\pi/2m)$$

$$< \sum_{p=0}^{r} 2G \cos p\pi/2m + r\pi/2m - \sum_{p=0}^{2m-r-1} 2G \cos p\pi/2m \ .$$

But

$$\sum_{p=0}^{2m-r-1} \cos p\pi/2m = - \sum_{p=2m-r}^{2m} \cos p\pi/2m$$

since

$$\sum_{p=0}^{2m} \cos p\pi/2m = 0 \ .$$

Also,

$$\sum_{p=2m-r}^{2m} \cos p\pi/2m = - \sum_{p=0}^{r} \cos p\pi/2m \ .$$

Therefore,

$$\sum_{p=0}^{r} \cos p\pi/2m - \sum_{p=0}^{2m-r-1} \cos p\pi/2m = 0$$

and

$$\hat{\phi}_{2m-r} < r\pi/2m \le \pi.$$

(iii) We have

$$\hat{\phi}_{2m-r+1} = \hat{\phi}_0 + G \sum_{p=0}^{2m-r} (+1)(-2 \cos p\pi/2m)$$

$$\ge \sum_{p=0}^{r-1} 2G \cos p\pi/2m + (r-1)\pi/2m - \sum_{p=0}^{2m-r} 2G \cos p\pi/2m$$

But, as in (ii),

$$\sum_{p=0}^{r-1} \cos p\pi/2m \; - \; \sum_{p=0}^{2m-r} \cos p\pi/2m \; = \; 0$$

and $\hat{\phi} \geq (r-1)\pi/2m$, which is identical to (iii).

(iv) We have, using Eq. (A2-4),

$$\hat{\phi}_{2m} = \hat{\phi}_o + G \sum_{p=0}^{2m-r+1} (+1)(-2\cos p\pi/2m) + G \sum_{p=2m-r}^{2m-1} (-1)(-2\cos p\pi/2m)$$

$$< r\pi/2m + \sum_{p=0}^{r} 2G\cos p\pi/2m - \sum_{p=0}^{2m-r+1} 2G\cos p\pi/2m + \sum_{p=2m-r}^{2m-1} 2G\cos p\pi/2m$$

$$= r\pi/2m + \sum_{p=2m-r}^{2m-1} 2G\cos p\pi/2m \; < \; r\pi/2m + \sum_{p=2m-r}^{2m-1} \pi/2m$$

$$= r\pi/2m + r\pi/2m \leq 2\pi,$$

proving (iv) and the theorem.

<u>Theorem A2-2</u>. With the hypotheses of Th. A2-1, $0 < \hat{\phi}_{2m} < \phi_o$.

<u>Proof:</u> We have

$$\hat{\phi}_m = \hat{\phi}_o + G \sum_{p=0}^{2m-r} (+1)(-2\cos p\pi/2m) + G \sum_{p=2m-r+1}^{2m-1} (-1)(-2\cos p\pi/2m)$$

$$= \hat{\phi}_o - 2G - 4G \sum_{p=1}^{r-1} \cos p\pi/2m$$

Since $\displaystyle\sum_{p=1}^{r-1} \cos p\pi/2m > 0$, we have immediately $\hat{\phi}_{2m} < \hat{\phi}_o$.

Using Eq. (A2-1),

$$\hat{\phi}_{2m} \geq \sum_{p=0}^{r-1} 2G \cos p\pi/2m + (r-1)\pi/2m - 2G - 4G \sum_{p=1}^{r-1} \cos p\pi/2m$$

$$= \sum_{p=1}^{r-1} [\pi/2m - 2G \cos p\pi/2m] > 0,$$

since $2G < \pi/2m$.

Theorem A2-3. If $0 \leq 2G < \pi/2m$ and

$$-(r+1)\pi/2m - \sum_{p=0}^{r} 2G \cos p\pi/2m \leq \phi_o < -r\pi/2m - \sum_{p=0}^{r-1} 2G \cos p\pi/2m \quad (A2-6)$$

and $\phi_o \geq -\pi$, then

$$w_k = \begin{cases} -1, & 0 \leq k \leq r \\ +1, & r+1 \leq k \leq 2m \end{cases} \quad (A2-7)$$

where $0 \leq r \leq 2m-1$.

Proof: As in Th. A2-1, we need only prove the following:

(i) $-\pi \leq \hat{\phi}_o$

(ii) $r\pi/2m + \hat{\phi}_r < 0$

"ii) $0 \leq (r+1)\pi/2m + \hat{\phi}_{r+1}$

(iv) $2m\pi/2m + \hat{\phi}_{2m} < \pi$.

The proofs are straightforward:

(i) is part of the hypotheses.

(ii) $\hat{\phi}_r = \phi_o + G \sum_{p=0}^{r-1} (-1)(-2\cos p\pi/2m) < -r\pi/2m$, directly from Eq. (A2-6).

(iii) $\hat{\phi}_{r+1} = \hat{\phi}_o + G \sum_{p=0}^{r} (-1)(-2\cos p\pi/2m) \geq -(r+1)\pi/2m$, directly from Eq. (A2-6).

200

(iv) $\hat{\phi}_{2m} = \hat{\phi}_0 + G \sum_{p=0}^{r} (-1)(-2\cos p\pi/2m) + \sum_{p=r+1}^{2m-1} (+1)(-2\cos p\pi/2m)$

$$< -r\pi/2m - 2G \sum_{p=0}^{r-1} \cos p\pi/2m + 2G \sum_{p=0}^{r} \cos p\pi/2m - 2G \sum_{p=r+1}^{2m-1} \cos p\pi/2m$$

by Eq. (A2-6). Now

$$-2G \sum_{p=0}^{r-1} \cos p\pi/2m + 2G \sum_{p=0}^{r} \cos p\pi/2m = 2G\cos r\pi/2m$$

and

$$-\sum_{p=r+1}^{2m-1} \cos p\pi/2m = \sum_{p=1}^{r} \cos p\pi/2m$$

Therefore,

$$\hat{\phi}_{2m} < -r\pi/2m + 2G\cos r\pi/2m + 2G \sum_{p=1}^{r} \cos p\pi/2m$$

$$= \sum_{p=1}^{r} [-\pi/2m + 2G\cos p\pi/2m] + 2G\cos r\pi/2m$$

Now, since $2G < \pi/2m$, the summation term is negative, so that

$$\hat{\phi}_{2m} < 2G\cos r\pi/2m \le \pi/2m$$

proving (iv) and the theorem.

<u>Theorem A2-4.</u> With the hypotheses of Th. A2-3, $\hat{\phi}_0 < \hat{\phi}_{2m} < 2G$.

<u>Proof:</u>

$$\hat{\phi}_{2m} = \hat{\phi}_0 + G \sum_{p=0}^{r} (-1)(-2\cos p\pi/2m) + G \sum_{p=r+1}^{2m-1} (+1)(-2\cos p\pi/2m)$$

$$= \hat{\phi}_0 + 2G + 4G \sum_{p=1}^{r} \cos p\pi/2m$$

201

Since $\sum\limits_{p=1}^{r} \cos p\pi/2m > 0$, we have immediately $\hat{\varphi}_{2m} > \hat{\varphi}_o$.

Using Eq. (A2-6),

$$\hat{\varphi}_{2m} < -r\pi/2m - \sum_{p=0}^{r-1} 2G \cos p\pi/2m + 2G + 4G \sum_{p=1}^{r} \cos p\pi/2m$$

$$= \sum_{p=1}^{r} [-\pi/2m + 2G \cos p\pi/2m] + 2G \cos r\pi/2m$$

$$< 2G \cos r\pi/2m \leq 2G.$$

APPENDIX 3

FIRST ORDER DPLL BANDWIDTH

In this appendix, we calculate the bandwidth of the linearized first order DPLL, having transfer function

$$T(z) = \frac{4\pi g_1}{1 - (1 - 4G/\pi)z^{-1}} \tag{A3-1}$$

To obtain the frequency characteristec, we set

$$z = e^{j2\pi f/f_s} \tag{A3-2}$$

where f_s is the sampling frequency. The bandwidth, B_L, is the frequency for which

$$|T(e^{j2\pi B_L/f_s})| = |T(1)|/\sqrt{2} \tag{A3-3}$$

or, equivalently,

$$|1 - (1 - 4G/\pi)e^{-j2\pi B_L/f_s}|^2 = 2(4G/\pi)^2 \tag{A3-4}$$

Now,

$$|1 - (1 - 4G/\pi)e^{-j2\pi B_L/f_s}|^2$$

$$= 4(1 - 8G/\pi)\sin^2 \pi B_L/f_s + (4G/\pi)^2 \tag{A3-5}$$

and if $8G/\pi \ll 1$, then $\pi B_L/f_s \ll \pi/2$ and

$$4(1 - 8G/\pi)\sin^2 \pi B_L/f_s + (4G/\pi)^2 \approx (2\pi B_L/f_s)^2 + (4G/\pi)^2 \tag{A3-6}$$

and we obtain from Eq. (A3-4)

$$B_L \approx (2/\pi^2) f_s G \tag{A3-7}$$

The above result has a graphical interpretation. The quantity

$$d = |1 - (1 - 4G/\pi)e^{-j\theta}| = |e^{j\theta} - (1 - 4G/\pi)|$$

is the distance between $z = 1 - 4G/\pi$ and $z = e^{j\theta}$ as shown in Fig. A3-1. We are looking for θ such that $d = \sqrt{2}(4G/\pi)$. Now if $4G/\pi << 1$, then near $z = 1$, the unit circle and a vertical line passing through $z = 1$ are approximately identical, as illustrated in Fig. A3-2. Hence to find θ, we may construct an isosceles right triangle as shown, and the arc subtended by θ is approximately $4G/\pi$ radians. Since $\theta = 2\pi$ corresponds to $f = f_s$, the bandwidth is

$$B_L \approx (f_s/2\pi)(4G/\pi) = (2/\pi^2)f_s G,$$

as before.

Note that using the vertical line in lieu of the unit circle results in a bandwidth which is smaller than the exact value. This is clear from Fig. A3-2.
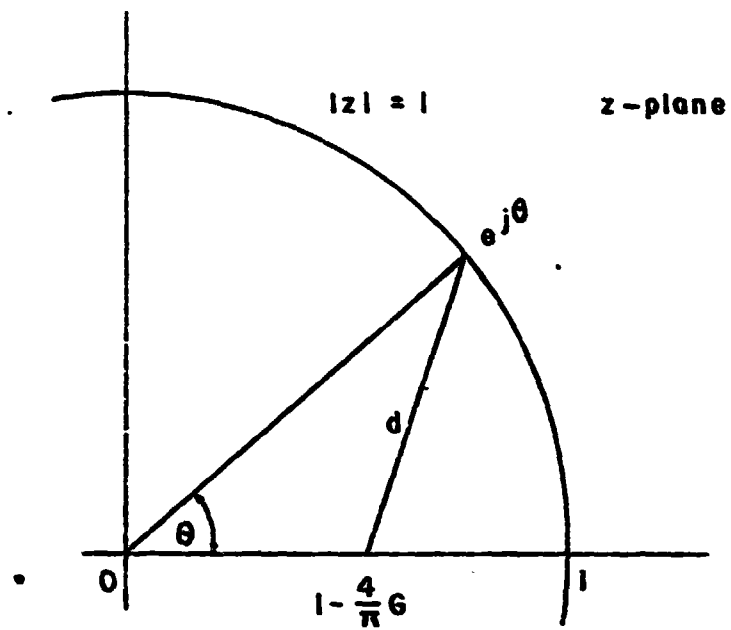
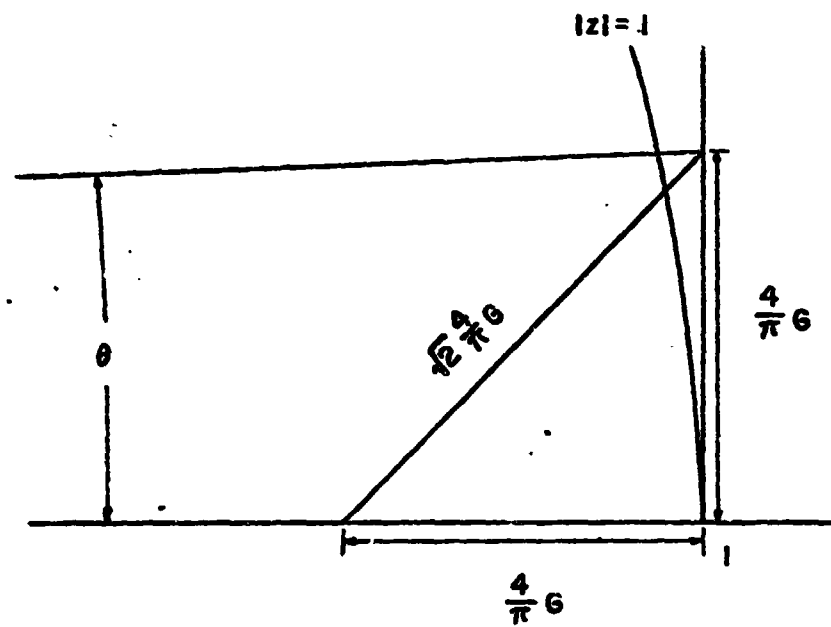Fig. A3-1. Illustrating the quantity $d = |e^{j\theta} - (1 - 4G/\pi)|$.

Fig. A3-2. The situation in the neighborhood of $z = 1$ when $4G/\pi << 1$.

REFERENCES

1. IEEE International Conf. on Communications, Session 14, "Digital Phase Locked Loops", Phila., Pa., June, 19-21, 1972.

2. International Telemetering Conf., Session V, "Digital Phase Locked Loops", Los Angeles, Ca., Oct. 10-12, 1972.

3. J. K. Holmes, "Digital Command System Second-Order Sub-Carrier Tracking Loop Performance", presented at ICC, Phila., Pa., June 19-21, 1972.

4. F. D. Natali, "All Digital, Coherent Demodulator Techniques", presented at ICC, Phila., Pa., June 19-21, 1972.

5. W. J. Hurd and O. T. Andersen, "Digital Transition Tracking Symbol Synchronizer for Low SNR Coded Systems", IEEE Trans. Comm. Tech., Vol. Com-18, No. 2, April 1970, pp. 141-147.

6. J. R. Cessna and D. M. Levy, "Phase Noise and Transient Times for a Binary Quantized Digital Phase-Locked Loop in White Gaussian Noise", IEEE Trans. Comm. Tech., Vol. Com-20, No. 2, April, 1972, pp. 94-104.

7. G. Pasternack and R. L. Whalin, "Analysis and Synthesis of a Digital Phase Locked Loop for FM Demodulation", Bell Syst. Tech. J., Vol. 47, Dec., 1968, pp. 2207-2239.

8. C. N. Kelly and S. C. Gupta, "The Digital Phase-Locked Loop as a Near-Optimum FM Demodulator", IEEE Trans. Comm. Tech., Vol. Com-20, No. 3, June, 1972, pp. 406-411.

9. C. N. Kelly and S. C. Gupta, "Discrete-Time Demodulation of Continous-Time Signals", IEEE Trans. on Info. Theory, Vol. IT-18, No. 4, July, 1972, pp. 488-493.

10. D. R. Polk and S. C. Gupta, "Quasi-Optimum Digital Phase-Locked Loops", IEEE Trans. on Comm. Tech., Vol. Com-21, Jan., 1973, pp. 75-82.

11. C. S. Gill and S. C. Gupta, "First Order Discrete Phase-Locked Loop with Applications to Demodulation of Angle-Modulated Carrier", _IEEE Trans. Comm. Tech._, Vol. Com-20, No. 3, June, 1972, pp. 454-462.

12. T. Muratani, M. Okawa, A. Ogawa, "Analysis of Phase-Locked Loop with Sampled-Data Control", _Electronics and Comm. in Japan_, Vol. 54-B, No. 12, Dec., 1971, pp. 52-59.

13. K. Moriyama and K. Yamaguchi, "A Digital Automatic Phase-Control Method Using Electronic Circuit", _Electronics and Comm. in Japan_, Vol. 55-C, No. 2, Feb., 1972, pp. 68-76.

14. P. W. Osborne and D. L. Schilling, "Threshold Analysis of Phase-Locked Loop Demodulators Using Most Likely Noise", _IEEE Trans. on Comm. Tech._, Vol. Com-19, No. 1, Feb., 1971, pp. 31-41.

15. H. Taub and D. L. Schilling, _Principles of Communication Systems_, Mc Graw Hill Book Co., 1971, pp. 161,162.

16. P. M. Ebert, J. E. Mazo, M. G. Taylor, "Overflow Oscillations in Digital Filters", _Bell Syst. Tech. J._, Vol. 48, No. 9, Nov., 1969, pp. 2999-3020.

17. Taub and Schilling, op. cit., p. 263.

18. The Software Writing Group, _Programming Languages_, PDP-8 Handbook Series, 1970, Ch. 11.

19. Taub and Schilling, op. cit., p. 356.

20. R. W. Chang, J. E. Mazo, J. Salz, "Stability Analysis of a Digital Rate-Locked Loop", _IEEE Trans. on Comm._, Vol. Com-20, No. 6, Dec., 1972, pp. 1136-1139.

II. A New Area of Investigation

The Phase Lock:d Loop employs a linear loop filter to process the phase detected signal before correcting the frequency of the voltage controlled oscillator.

We feel that the output of the phase detector can be processed nonlinearly thereby obtaining a "better" estimate of the phase of the incoming signals. Nonlinear processors are in general diffi- cult to construct and may even require the use of a digital computer. Schilling and Ucci have determined a relatively simple nonlinear processor.

Schilling and Ucci are currently analyzing the response of a PLL which uses an adaptive delta modulator as a nonlinear processor. The delta modulator can be used to obtain an accurate estimate of the phase and is easily integrated, thereby resulting in an efficient low volume, low cost device.

A detailed discussion of this device will b. presented in the final report.