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16. Abstract

A power processor breadboard for the JPL 20CM Ion Engine was designed fabricated and tested to determine compliance with the electrical specification. The power processor breadboard used the Silicon-Controlled Rectifier (SCR) series resonant inverter as the basic power stage to process all the power to the ion engine.

The breadboard power processor was integrated with the JPL 20cm ion engine and complete testing was performed. The integration tests were performed without any silicon-controlled rectifier failure. This demonstrated the ruggedness of the series resonant inverter in protecting the switching elements during arcing in the ion engine.

A new method of fault clearing the ion engine and returning back to normal operation without elaborate sequencing and timing control logic was evolved. In this new method, the main vaporizer was turned off and the discharge current limit was reduced when an overload existed on the screen/accelerator supply. After the high voltage returned to normal, both the main vaporizer and the discharge were returned to normal.

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FORWARD

This work is based on the series inverter and control system (ASDTIC) development work performed by Dr. F. C. Schwarz while at NASA Electronic Research Center and NASA Lewis Research Center. This program is a continuation of the technical work performed under Contract NAS12-2183 and reported in NASA CR-120928, "Development of a Multikilowatt Ion Thruster Power Processor."

The electrical design and fabrication was performed by Leonard Inouye and Shig Miyabe. The power component design, development and testing was performed by Morris Chester. The ion engine operation was performed by Bob Kemp and Ed Ashwell.

We would like to thank Jack Shank of NASA Lewis for his support during the design phase and especially during the ion engine power processor integration phase, JPL Electric Propulsion Group for the loan of the 20CM Hollow Cathode Ion Engine, and Mr. E. V. Pawlik of JPL for technical support in running the 20CM Ion Engine.

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1.0 SUMMARY

The series resonant inverter design was modified to be applicable to the requirements for a 20cm ion engine power processor.

This configuration of the silicon-controlled rectifier series resonant inverter was developed in which the excessive series resonant capacitor energy was circulated through the load and returned to the source. The maximum frequency of operation was 20kHz.

High power component development work was performed on the series resonant capacitor, the series resonant inductor, the power transformer and the silicon-controlled rectifier to reduce weight and to improve efficiency.

High threshold digital logic and linear analog integrated circuits were incorporated into the design to reduce the effective part count and to obtain high noise immunity during arcing of the ion engine.

The two-loop control system was also incorporated in all critical regulators to maintain high regulation accuracy and good transient response.

The following is a summary of the 20cm ion engine power processor breadboard characteristics:

o	Input:	200Vdc to 400Vdc
o	Output:	10 outputs per requirements of Appendix A
o	Output Power:	2.7KW maximum
o	Commands:	5 on/off plus two analog signals per requirements of Appendix A
o	Telemetry:	14 channels
o	Size:	76cm (30 in.) x 91cm (36 in.) x 15cm (6 in.) high
o	Weight of Breadboard:	25.6 kilograms (56.6 lbs.)

o	Weight of Components:	9.0 kilograms (20 lbs.).
o	Efficiency:	86.8 to 85.4% at full power. 83.8 to 82% at half power.
o	Total Part Count:	2661 including circuit redundancy.
o	Total In-Line Components for Reliability Analysis:	1030.

The above characteristics are not the final values for a flight power processor but are given to present the development status. Efficiency can be improved by the development of improved silicon-controlled rectifiers. Weight can be reduced by mechanical design and packaging of the components to reduce the ratio of total weight to component weight. The in-line components for reliability analysis can be reduced by 230 by the use of redundant circuit design in the command and protection system.

The breadboard was completely checked out with a resistive load bank to simulate the range of ion engine static loading and fault characteristics.

The power processor breadboard and JPL 20cm ion engine were integrated and tested at TRW Systems.

The test facility includes a vertically mounted five-foot (diameter) x ten-foot (length) vacuum chamber, laboratory power supplies, complete monitoring of all voltage and currents drawn by the ion engine, and a junction panel to facilitate transfer between laboratory supplies and the ion engine power processor.

Startup, steady-state and arcing operation were performed on the ion engine and the power processor breadboard. During integration testing, the only problems occurred during arcing. When a short developed in the ion engine, the screen supply output filter capacitor

voltage was instantaneously developed across the cabling between the ion engine and the power processor. The output ground terminal in the power processor was now elevated to a very high voltage and caused insulation failures between the other grounds in the power processor.

There was no failure of any kind of the power silicon-controlled rectifier during these tests, thereby demonstrating the ruggedness of the SCR series resonant inverter stage during all modes of operation.

Current noise variations on all input and output power lines were monitored to determine if interaction occurred between power source, power processor and ion engine. Conducted electromagnetic interference measurements were also monitored. Because of the low di/dt characteristics of the sinewave currents generated by the series resonant inverter, MIL-STD 461, Notice 3 specification was met except at some high frequencies. Additional high frequency filtering and packaging would reduce the high frequency components.

During ion engine/power processor integration testing, a new method of ion engine fault clearing was demonstrated. When an overload appears on the beam/accelerator supply, the main vaporizer is turned off and the arc current level is reduced to 4 amps. This lowers the plasma density, the short can be cleared and the high voltage is returned to normal. After normal high voltage is obtained, both the arc and main vaporizer return to normal operation. Because the power processor can operate continuously into a short circuit, this method helps clear a shorted engine without an elaborate sequencing system to protect the power processor when operating during a short and overload recovery.

2.0 INTRODUCTION

During the past few years, NASA, TRW and other government contractors have performed studies on solar powered electrical spacecraft. The results of these studies indicate that the development of a lightweight SCR series resonant power processor could greatly enhance spacecraft performance and reliability. Thus, the NASA Lewis "Development and Improvement of Ion Engine Power Processor" program is recognized as an important link in the development of a truly flightworthy electrically propelled spacecraft of the future.

High power silicon-controlled rectifiers (SCR's) or thyristors have been used in high voltage and high power equipment for industrial applications for many years. The design objectives in industry were primarily low cost and low maintenance whereas the design requirements of low weight and high efficiency for space equipment are usually not a factor in ground applications.

In space applications, the primary design requirements are high reliability and low weight. Power processor inefficiency results in spacecraft weight penalties due to increased power source capacity and heat rejection capability required to supply the additional power processor losses.

Future high power spacecrafts will be using high voltage distribution to minimize the cable weight and losses and will have high power loads such as electric propulsion, direct broadcast communications and other high power type loads or experiments.

The "Development and Improvement of Ion Engine Power Processor" program's primary objective is to develop and apply the SCR Series Resonant Inverter circuit to rugged, high input voltage electric propulsion power processing equipment. The SCR power processing technology utilizes the SCR series resonant circuit for inverting the input power from a solar array and an analog signal to discrete time interval converter (ASDTIC) as the low level amplifier and control stage for regulated current and voltage outputs. These basic circuits, which were initially developed at NASA ERC and were applied by TRW to the design of a power processing system capable of meeting the load requirements for a 2.5KW Kaufman Thruster.

Basic development was performed at TRW under contract NAS12-2183, "Multikilowatt Ion Thruster Power Processor" for NASA ERC during the period from 1 July 1969 to 30 January 1970, and from 1 July 1970 to 30 October 1970 (11 months total period). During this period, a breadboard model was developed to establish baseline performance characteristics of such a system. The unit, capable of operation over an input voltage range of 200 to 400 volts, had an efficiency of 90%, a component mass of 14.58kg, and a part count of 3240. Preliminary integration testing of the beam, accelerator, and arc modules of this power processor, with a 20cm ion engine, demonstrated the exceptional ruggedness of the SCR series resonant circuit concept during thruster arcing and startup. Results of this program were reported in NASA CR 120928, "Development of a Multikilowatt Ion Thruster Power Processor."

The period of performance of the present program was from 1 June 1971 to 1 March 1972, under contract NAS3-14383, and from 15 May 1972 to 15 October 1972, under contract NAS3-14383, Amendment 1, for a total period of 14 months.

During the first period, the following tasks were performed for the development and improvement of the SCR power processing technology:

- Weight and part count were reduced to 9kg and 1030 parts by operation of the SCR series resonant inverter at 20kHz and by use of high threshold logic integrated circuits.
- A reliability study of the complete ion engine power processor was performed and incorporation of majority voting redundance (2 out of 3) for all output regulation control circuits improved the reliability to 0.925 for 10,000 hours. (No redundancy was incorporated in the command and protection system because of its possible change after ion engine tests.)
- The design, fabrication, and testing of a complete power processor system for the JPL 20cm ion engine included all component, circuit, and redundancy improvements obtained from the preceding tasks.

During the second period, the power processor breadboard was integrated with a 20cm ion engine and the following critical operation performance was demonstrated:

- Controlled Engine Startup
- Stability of the Engine Control Loops
- Simplified Ion Engine Fault Clearing
- Safe, continuous operation of the power processor with overloads and engine arcing
- Protection of input power bus from overloads.

3.0 20CM ION ENGINE POWER PROCESSOR BREADBOARD

The 20cm Ion Engine Power Processor Breadboard was designed to operate the JPL 20cm hollow cathode mercury ion engine. The detail requirement specification is included in Appendix A, 20cm Ion Thruster Power Processor Specification.

A power processor system block diagram was selected to maximize the total efficiency and to provide maximum flexibility to changes in power requirements, changes in control loops, and changes in command and sequencing for reliable operation of the 20cm ion engine.

A detailed electrical design was performed and a complete power processor breadboard was fabricated. Testing was performed with a simulated resistive load to demonstrate compliance with the power processor specification over the load range and overload conditions.

A summary of the test data is presented.

An analysis of the power processor design is also presented in order to indicate where penalties exist and where improvements can have the greatest leverage.

3.1 System Block Diagram

Figure 3-1 represents the block diagram mechanization of the electrical requirements of the ion thruster power processor. It can be divided into three basic areas.

- o The power circuit
- o The command and protection circuit
- o The output regulator circuitry

The mechanization of the system is influenced by the following items:

- o Engine control functions during startup, during normal operation and during overload
- o Use of the SCR series resonant inverter power stage
- o Maximize efficiency
- o Maintaining all control electronics at ground potential
- o System grounding philosophy

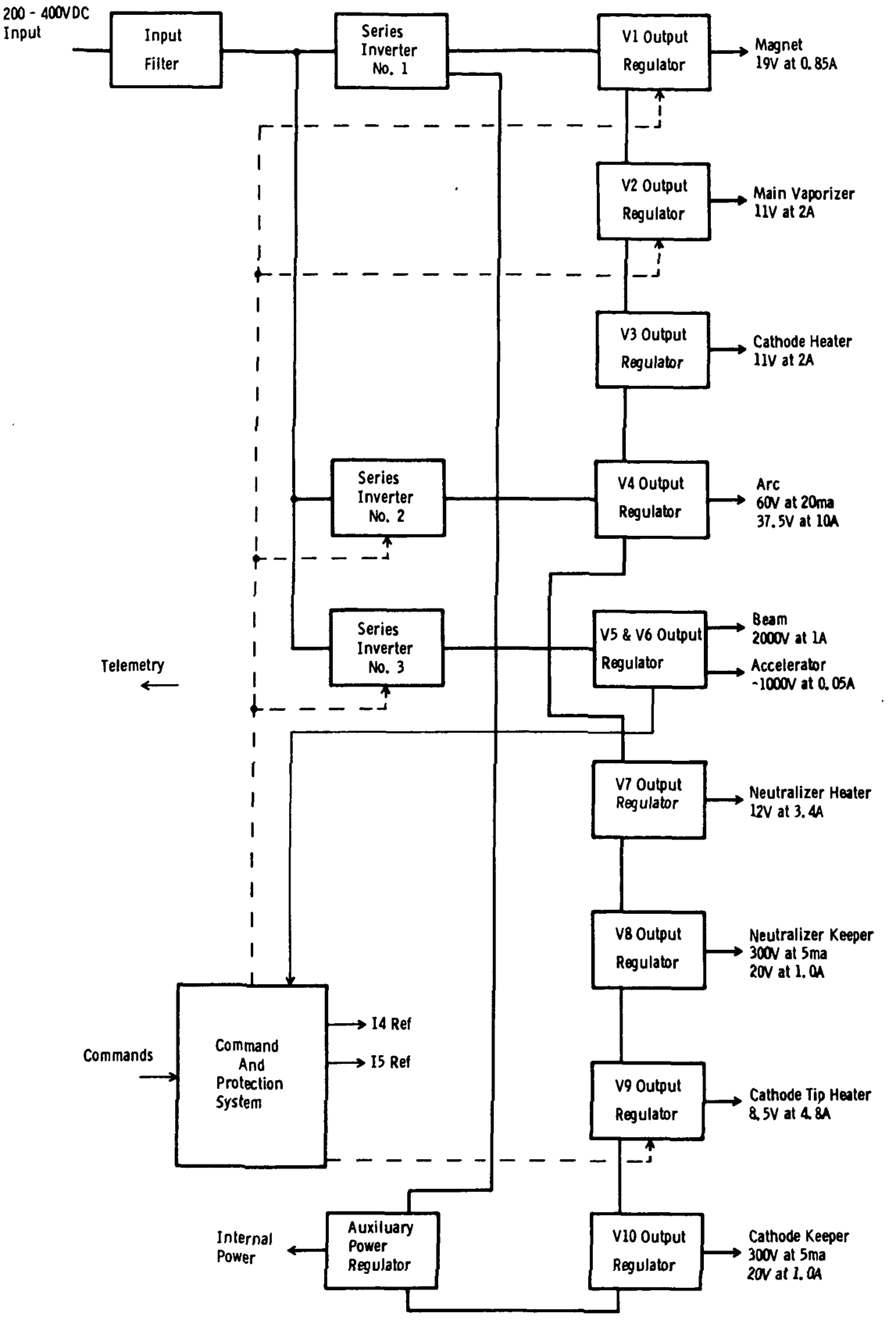


Figure 3-1. Ion Thruster Power Processor Block Diagram

The heavy darkened lines show the flow of the 200V to 400Vdc solar array power through a common input filter into three SCR series inverters.

The input filter design consists of a two-stage LC network for filtering the high ac current drawn by the inverters to 1% RMS of the maximum input average dc current. The filter design is such that the filter Q is under 1.4 without causing any loss in filter efficiency. A common input filter is used to reduce the total filter weight of the power processor. It is expected that there will be some minor cross-coupling between the three inverters because of the common input filter, however, the regulator action of the three inverters will keep this modulation from appearing in the output loads and the input filter will attenuate the cross-coupling signal to less than 1%.

Series inverter No. 1 is the multiple output inverter. It provides a constant current source to all its loads which are connected in series and runs at a constant frequency. This inverter supplies the following transformers which can supply current directly to the outputs or can be shorted resulting in zero power being delivered to the outputs.

- o PS1 Magnet supply
- o PS2 Vaporizer supply
- o PS3 Cathode heater supply
- o PS4B Arc booster supply
- o PS7 Neutralizer heater supply
- o PS8 Neutralizer keeper supply
- o PS9 Cathode tip heater supply
- o PS10 Cathode keeper discharge supply
- o Internal auxiliary supply

The total power rating of the inverter is about 200W.

SCR series inverter No. 2 powers only the PS4 output (the arc supply) and has a power rating of about 400W. Its operating frequency varies proportional to the output power.

SCR series inverter No. 3 supplies the PS5 and PS6 outputs (beam and accelerator) and has a power rating of about 2200W. Its operating frequency also varies proportional to the output power.

Detail block diagram of each section are included in Appendix B and illustrate the following characteristics:

- o Control loops and measurement techniques
- o Power and command interface
- o Output protection against high voltage arc-over

3.2 Electrical Design

A brief summary of the electrical design is presented for the three series inverters included in Figure 3-1, Ion Thruster Power Processor Block Diagram.

Appendix C in Section 6.0 discusses the development and energy control concepts for the Series Resonant Inverter.

Appendix D in Section 6.0 discusses the power component development performed for the series resonant inverter to reduce weight and losses.

Section 3.5, Design Analysis gives a summary of the weight efficiency part count and reliability for the electrical design.

3.2.1 Series Resonant Inverter No. 3 (Beam/Accelerator Supply)

In the following sections, the power stage design inverter control logic and the regulator control system are discussed. Performance evaluation of the series resonant inverter is also presented.

3.2.1.1 Power Stage

The schematic of the V5, V6 series inverter power stage is shown in Figure 3-2. The inverter consists of the main SCR-s, (SCR1, 2), auxiliary SCR's (SCR3, 4), the series resonant inductors (L1, L2, L3, L4, L5), the series resonant capacitors (C1, C2), the suppression networks for the main and auxiliary SCR's, the output transformer (T), the output rectifiers and the filter capacitors.

Circuit operation is as follows:

- o With C1 and C2 charged as shown, auxiliary SCR (SCR4) is turned on to circulate energy in C2 into transformer T and energy in C1 back to the source.
- o When the voltage on C1 reaches 450V, SCR1 is turned on causing an oscillatory current to flow through the series combination of L1, L5, T and C2.
- o As the current passes through zero, SCR1 is turned off and C2 is charged to a voltage higher than the supply voltage.

- o Auxiliary SCR (SCR3) is next turned on, to circulate energy in C1 into transformer T and energy in C2 back to the source.

- o When the voltage on C2 reaches 450V, SCR2 is turned on causing current to flow through L2, L5, T and C1. The turning off of SCR2 completes one full cycle.

The current flowing through transformer T when the SCR's are conducting develops a voltage which is rectified, filtered and delivered to the load. Regulation is achieved by sensing the 2000V output and then controlling the repetion rate of the SCR's.

3.2.1.2 SCR Series Inverter Control Logic

In this section, the requirements for the SCR series inverter control logic will be identified and the mechanization of the control system using digital circuit functions will also be presented. A brief discussion of the type and definition of the circuit function will also be included, and the precautions used in the application will be reviewed.

Power conditioning equipment is increasingly incorporating more digital control functions in the regulating system and in control logic. Recognizing and anticipating the future growth of this trend, TRW has conducted in-house study for the identification of the best available digital IC's for power-processor control applications particularly in terms of noise immunity, since this is the key to the reliable operation of digital iC's. The criteria for evaluating candidate IC's are:

- o All low-level signals are dc with no ac or capacitive coupling of the digital signals. This is to ensure that ac noise does not generate a false signal.

- o All time delays are mechanized using passive parts instead of regenerative one shots to minimize noise susceptibility. All other regenerative circuits are reviewed to ensure high noise immunity.

- o The input impedance of all control circuits are maintained low to have high noise immunity yet without causing excessive efficiency reductions.

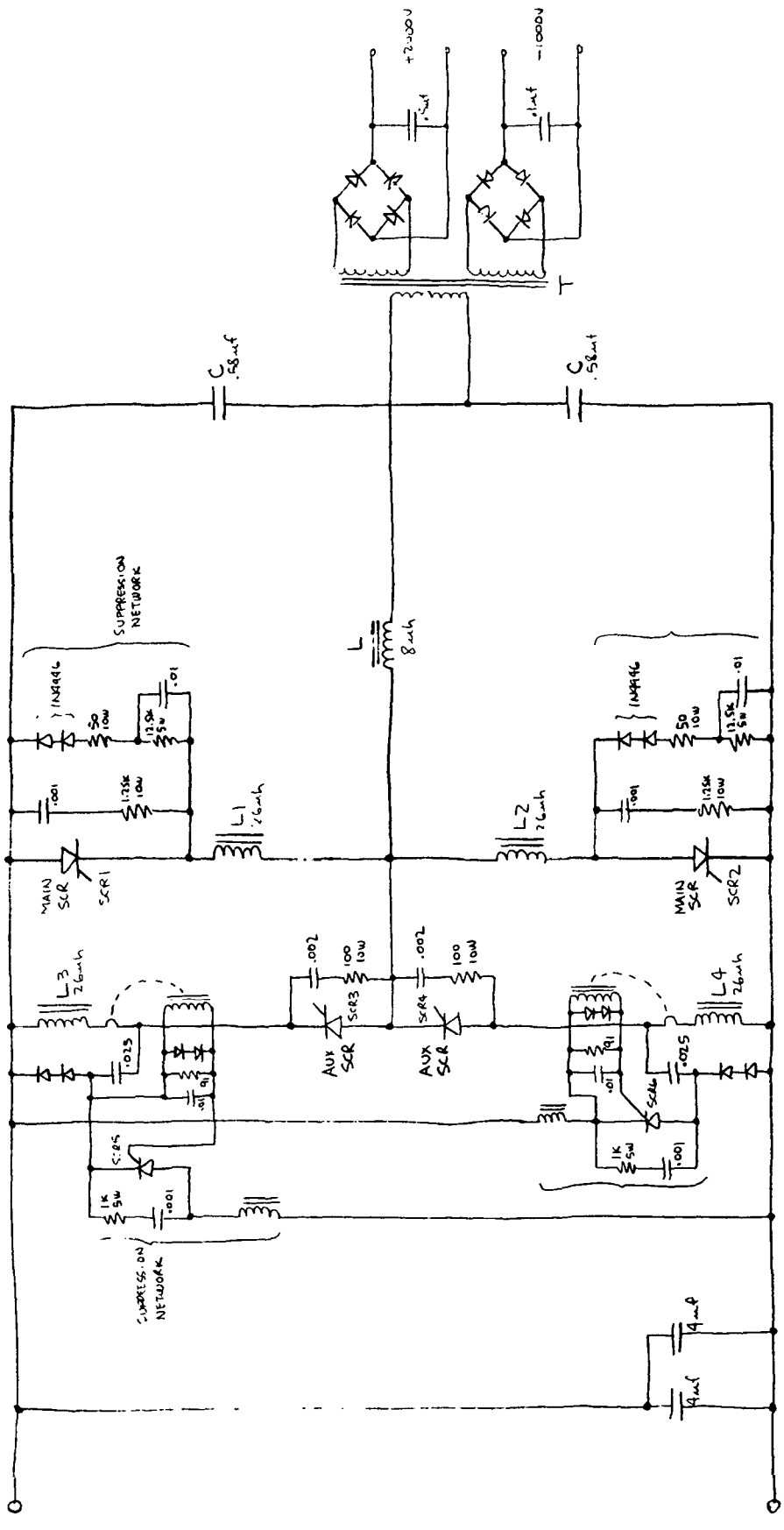
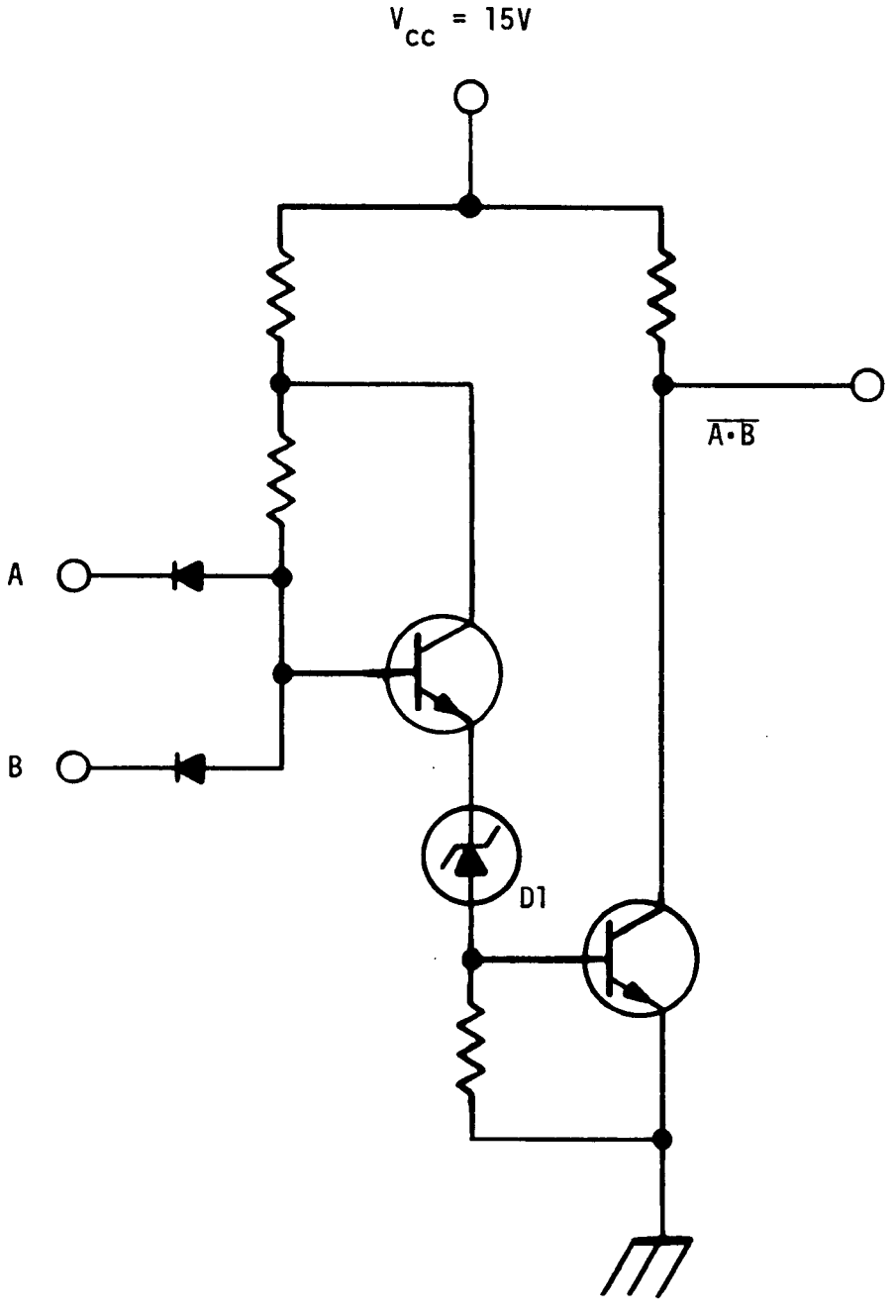
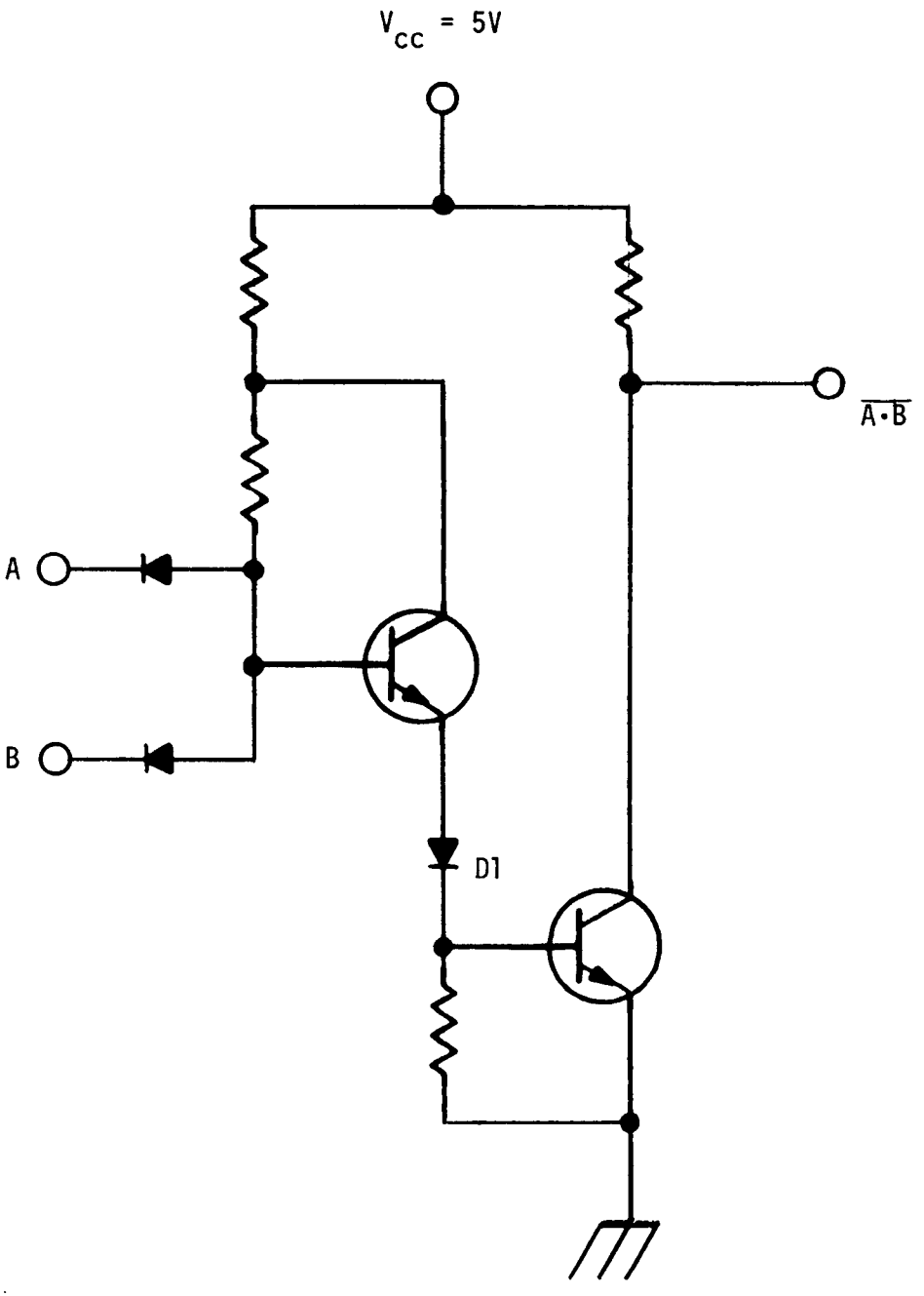


Figure 3-2. V5, V6 Inverter Power Stage



(a) HTL



(b) DTL

FIGURE 3.3 LOGIC GATE SCHEMATIC

The integrated circuit family most suitable for this application is Motorola High Threshold Logic, Figure 3-3(a). The High Threshold Logic (HTL) family of integrated circuits has a higher degree of inherent electrical noise immunity than other standard forms of IC logic families. The basic HTL logic gate is similar to the Diode Transistor Logic (DTL) gate circuit, Figure 3-3 (b). A considerable higher input threshold characteristic is exhibited by the HTL devices by using a reversed-biased base-emitter junction operating in the zener mode as compared to a forward-biased diode junction for the corresponding D1 element in the DTL gate. A typical 7.5V input signal is required to turn-on the HTL output inverting transistor as compared to a 1.5V signal necessary for DTL, thus giving an increased noise margin of 6V. The propagation delay of HTL is in the order of 110ns. Consequently, it is a relatively slow logic family, a property which aids in rejecting noise.

In summary, the HTL devices may be characterized as an IC family with a high degree of inherent noise immunity, a high input threshold, and a large logic swing. These characteristics make the line very attractive for use where electrical noise rejection is an important consideration, as well as for applications where interfacing with various discrete components is required.

In applying digital control logic to the power conditioning control system, it is necessary to determine the required functions and define their operations. The basic digital functions are identified and defined in Table 3-1.

The SCR series inverter has the following requirements for the control logic:

- Limiting of the series capacitor voltage
- Detection of the end of a power half cycle
- Starting procedure
- Regulation requirement
- Sequencing of SCR's for different half cycles.

TABLE 3-1

DIGITAL FUNCTIONS

TYPE	DEFINITIONS
NOR Gate	If a logical-1 input is present on any input terminal, the output is a logical-0.
NAND Gate	If a logical-1 input is present on all input terminals the output terminal is a logical-0. If any input is alogical-0, the output is a logical-1.
R-S Flip-Flop	Two NAND gates are cross connected in a positive feedback mode to maintain memory data. A momentary logical-0 forces the respective NAND gate to a logical-1 and the other NAND gate to a logical-0.
Pulse Stretcher	The pulse stretcher gives an output logical-1 output pulsewidth equal to the sum of the input logical-1 input pulse and a time interval determined by an external timing capacitor.
Exclusive-OR Gate	A logical-1 output signal is obtained, if one of the input signals is a logical-1 and the other input is a logical-0.

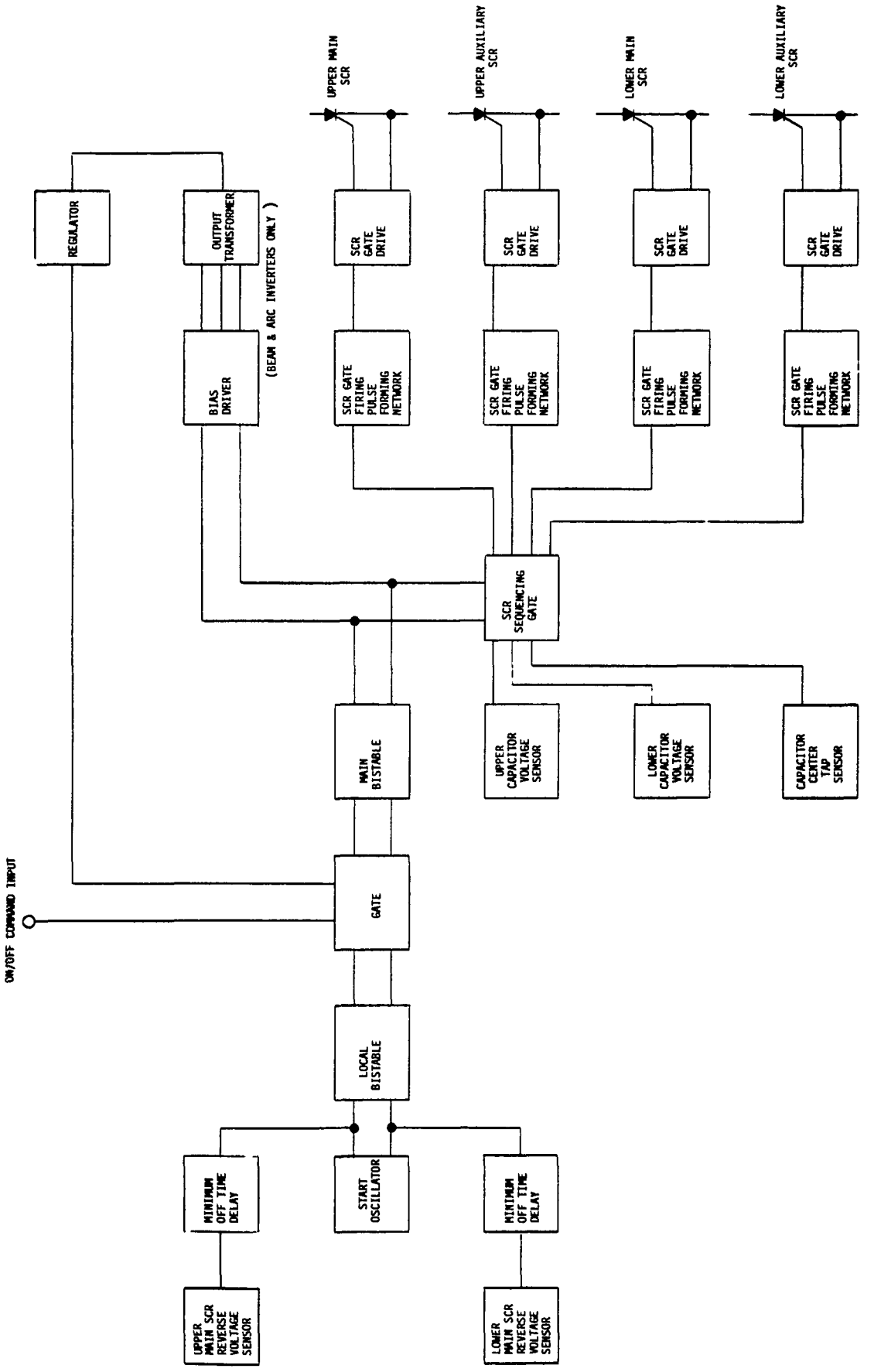


Figure 3-4. SCR Series Inverter Control Block Diagram

A capacitor voltage sensor continuously monitors the voltages on the series resonant inverter capacitors and programs the firing of the main line power SCR's in such a manner that the voltage ratings of the components in the circuit are never exceeded.

The next protection function is to determine when the current in the main power SCR has gone to zero so that the next power half cycle can be initiated. This function is mechanized by sensing that a reverse voltage condition has existed on the power SCR for at least the minimum off time to guarantee that the power SCR is off.

Now that the normal running protection functions have been identified, it is necessary to provide the correct starting procedure. When the system is initially activated, reverse voltage condition does not exist on either of the two main line power SCR's. To start the series resonant inverter, a low frequency oscillator becomes active and causes the control logic to switch and cause current flow in the power SCR. Once the system is running normal, the low frequency oscillator becomes disables.

The output regulator control signal must be able to override the control logic and stop power flow to the output filter circuitry.

The control function to be mechanized is the normal sequencing of the power SCR's from one half cycle to the other half cycle.

Figure 3-4 shows the series inverter control system block diagram.

Figure 3-5 illustrates the control logic diagram to program the firing of the main power SCR's and the auxiliary SCR's. The control system uses standard digital IC functions including pulse stretchers, R-S flip flops, Nand gates and voltage sense amplifiers. The high threshold logic digital circuits are used because of their high noise immunity (about 6 volts) and therefore they are immune to high EMI noise generated by the switching noise of high current circuits.

The control system contains five basic functions:

(1) SCR Sequencing
(2) Main Command Control
(3) Start Circuit
(4) Determination of Termination of Current Flow in Main SCR
(5) ON/OFF Control of Logic System

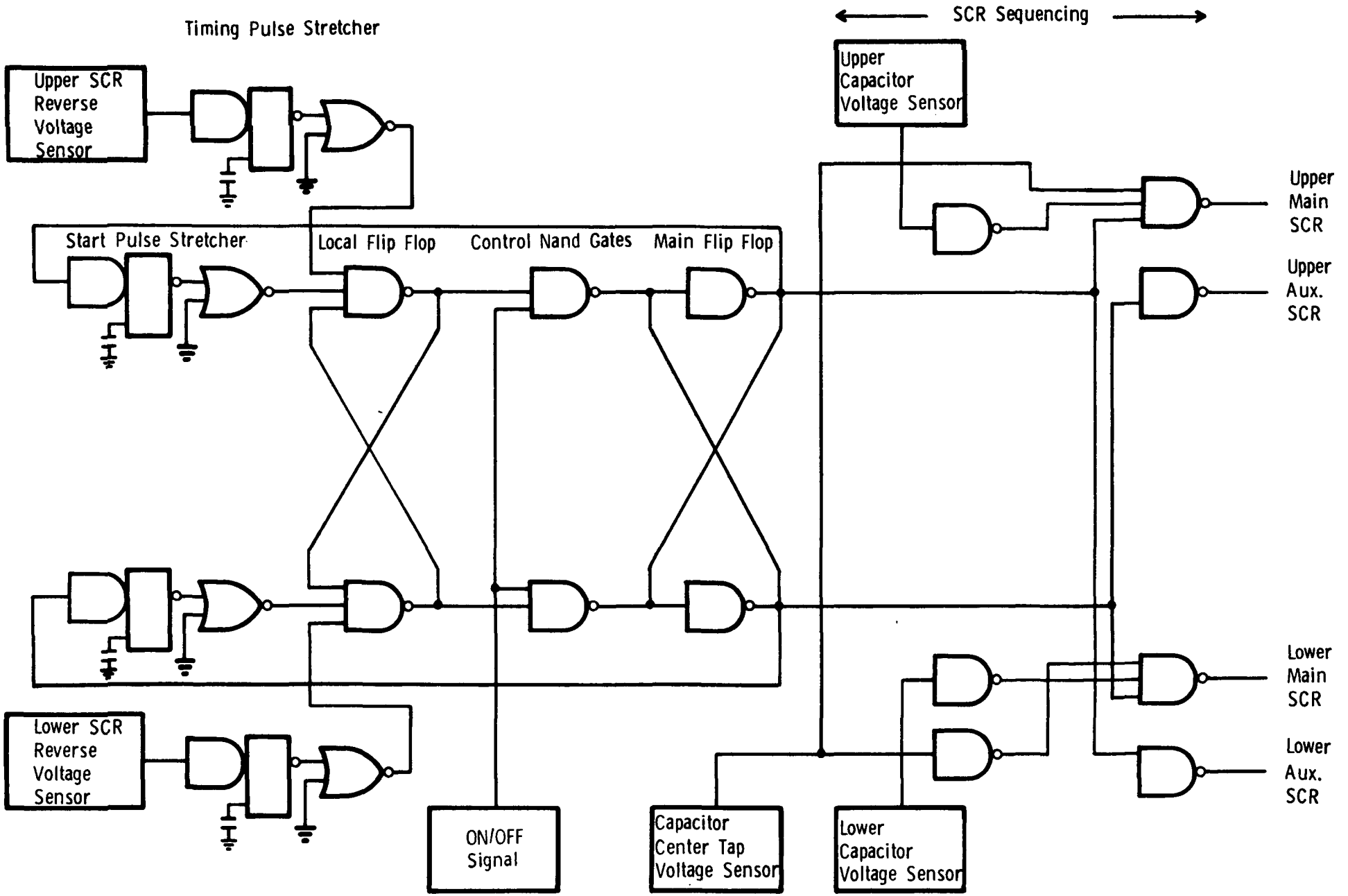


Figure 3-5 SCR INVERTER CONTROL LOGIC BLOCK DIAGRAM

Three voltage sensors combine with the associated Nand gates and steer the firing or sequencing of the main and auxiliary SCR's. The capacitor polarity voltage sensor determines which set of SCR's (lower auxiliary SCR and upper main SCR or upper auxiliary SCR and lower main SCR) can be fired. The capacitor positive and negative voltage sensor determine the capacitor voltage that is necessary to fire the main SCR's in order to maintain constant current flow through the main SCR and resonant inductor. The main flip flop provides the "0" and "1" logic to fire the alternate power half cycles and is the main command function.

Two start pulse stretchers receive signals from the main flip flop and provide a low frequency oscillation to transfer the local flip flop and the main flip flop, and generate the initial turn-on pulse for the series inverter to start series inverter oscillation.

Once the power system oscillates, the current in the main power SCR goes to zero and a reverse voltage appears across the mainline SCR. The SCR reverse voltage sensor detects this reverse voltage condition and after a fixed time period determined by the timing pulse stretcher, the voltage sensor causes the local flip flop to transfer which causes the main flip flop to transfer and starts a new power cycle for the SCR series inverters.

The ON/OFF signal controls the control Nand gates and inhibits the transfer of the local flip flop signal to the main flip flop. This signal could be an ON-OFF siwtch control, a regulator circuit output signal or an undervoltage/overvoltage bus voltage sensor to terminate operation of the SCR series inverter.

Digital integrated circuits have also been used for the pulse forming networks to generate SCR firing signals.

Figures 3-6 and 3-7 show the detail schematics of the SCR series inverter control logic. Starting with Figure 3-6, U1 and U9 are the voltage comparators which sense reverse voltage on the main SCR's. U2 is a pulse stretcher which provides the minimum off time before another half cycle can commence. U4 is the start oscillator, U5 is the local bistable, U6 is a NAND gate which couples the regulator signal into the control logic, U7 is the main bistable which commands the SCR firing, and U8 is a buffer stage to drive the bias driver circuit. U12 and U13 provide the ON/OFF command interface. In Figure 3-7,

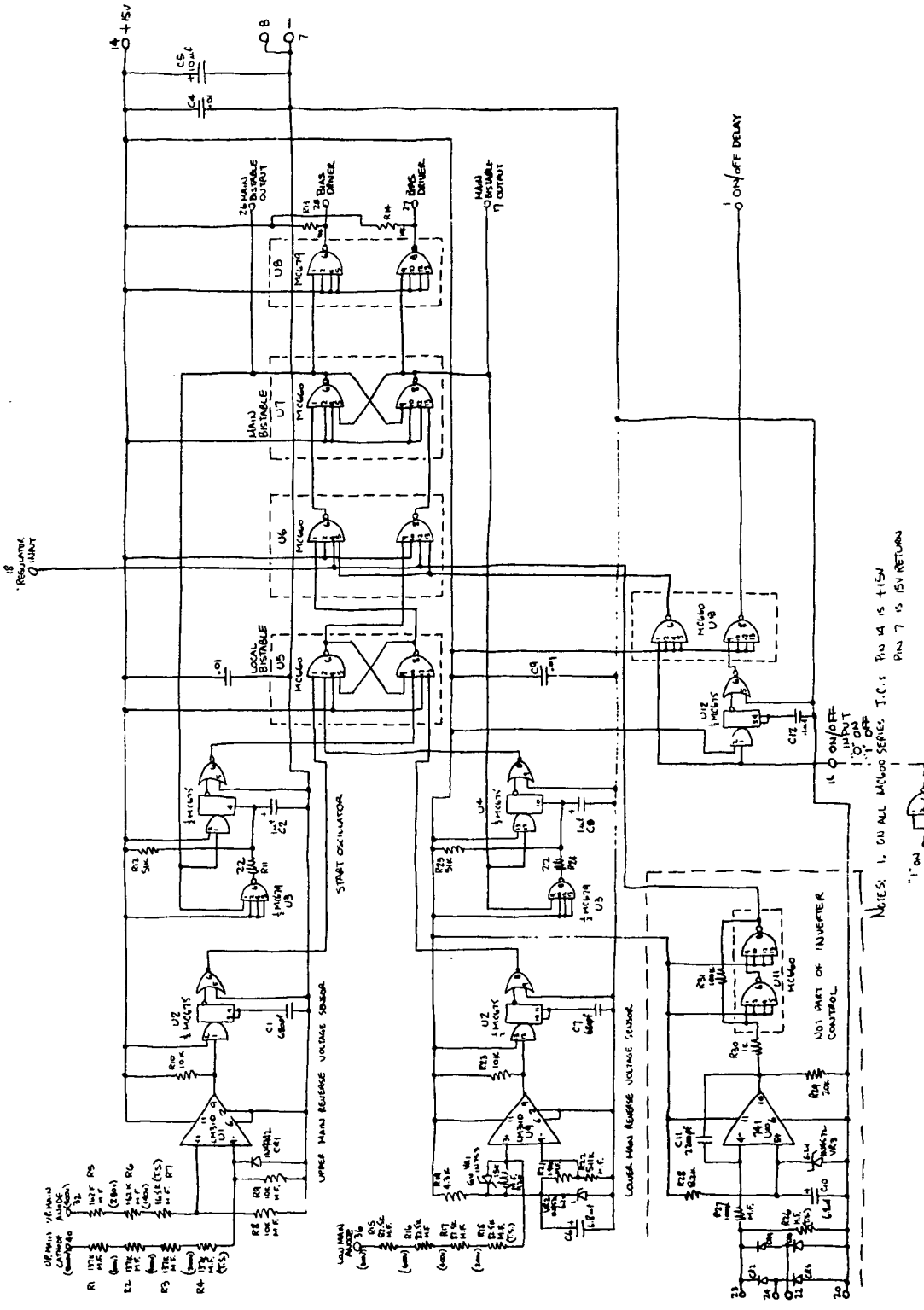
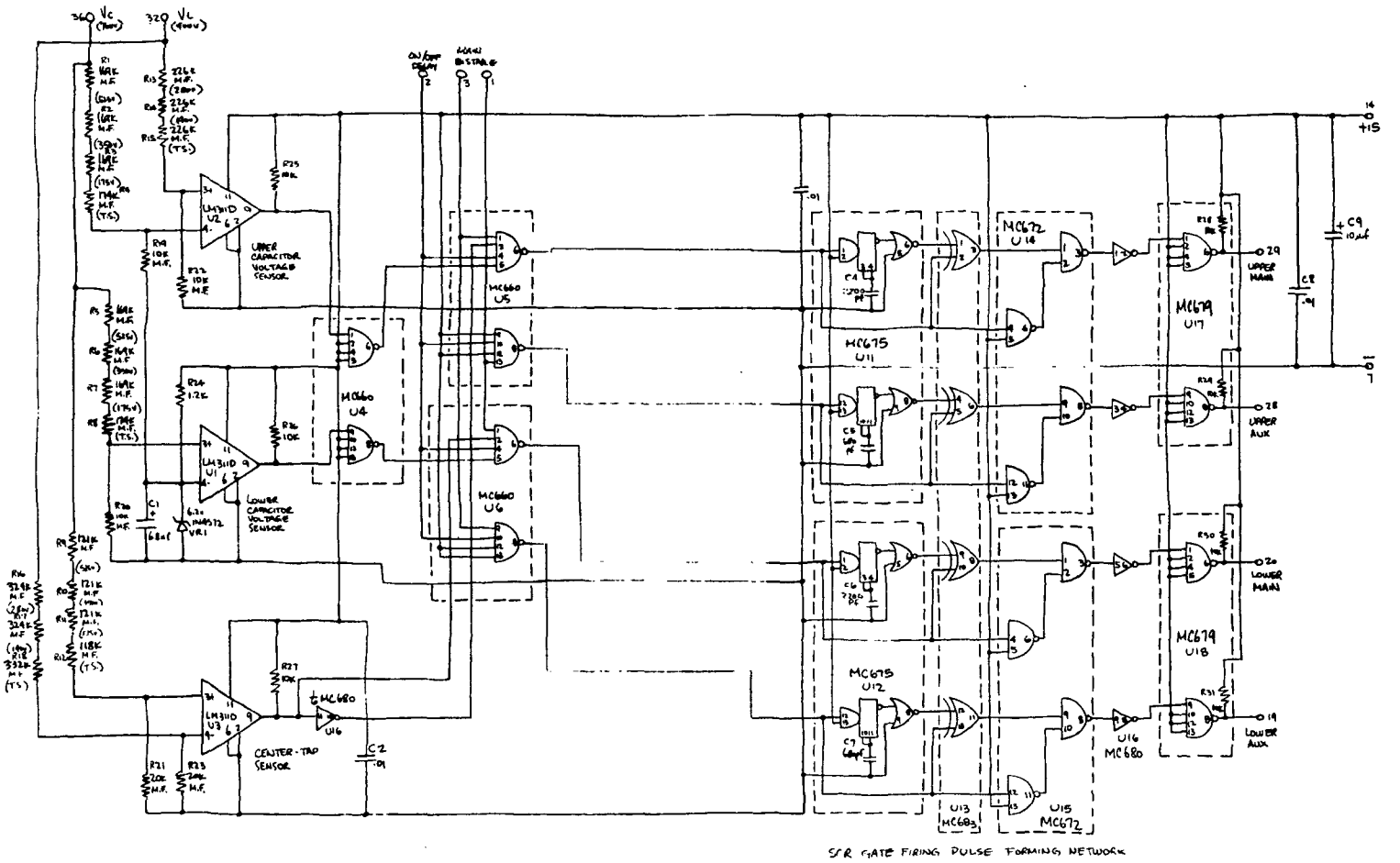


Figure 3-6 SCR Series Inverter Control Logic A



NOTES: 1. ON ALL MC600 SERIES I.C.'s PIN 14 IS +15V
PIN 7 IS 15V RETURN

Figure 3-7. SCR Series Inverter Control Logic B

U1, U2 and U3 are the voltage comparators which sense the capacitor voltages. U5 and U6 are NAND gates which determine which SCR is to be fired. U11, U12, U13, U14, U15, U16, U17 & U18 form the SCR gate firing pulse forming network.

3.2.1.3 Two Loop Control System (ASDTIC)

The application of the two loop control technique for the output regulators is a principle factor in the Power Supply meeting the stringent specifications. The block diagram of this control technique is shown in Figure 3-8. The power circuits which are part of the control loop include:

- Power switches
- Power input/output isolation
- Power transformation and rectification
- Output filter network

The control circuits include:

- DC output sensing
- Filter-network energy level sensing
- Integrating amplifier
- Threshold detector
- Control signal input/output isolation
- Pulse generator
- Power drive interface circuit

The above list identifies all functional requirements for the two loop control system. The input/output power and control signal isolation is not required unless the power switching is done on the primary side and output sensing is performed on an isolated secondary output.

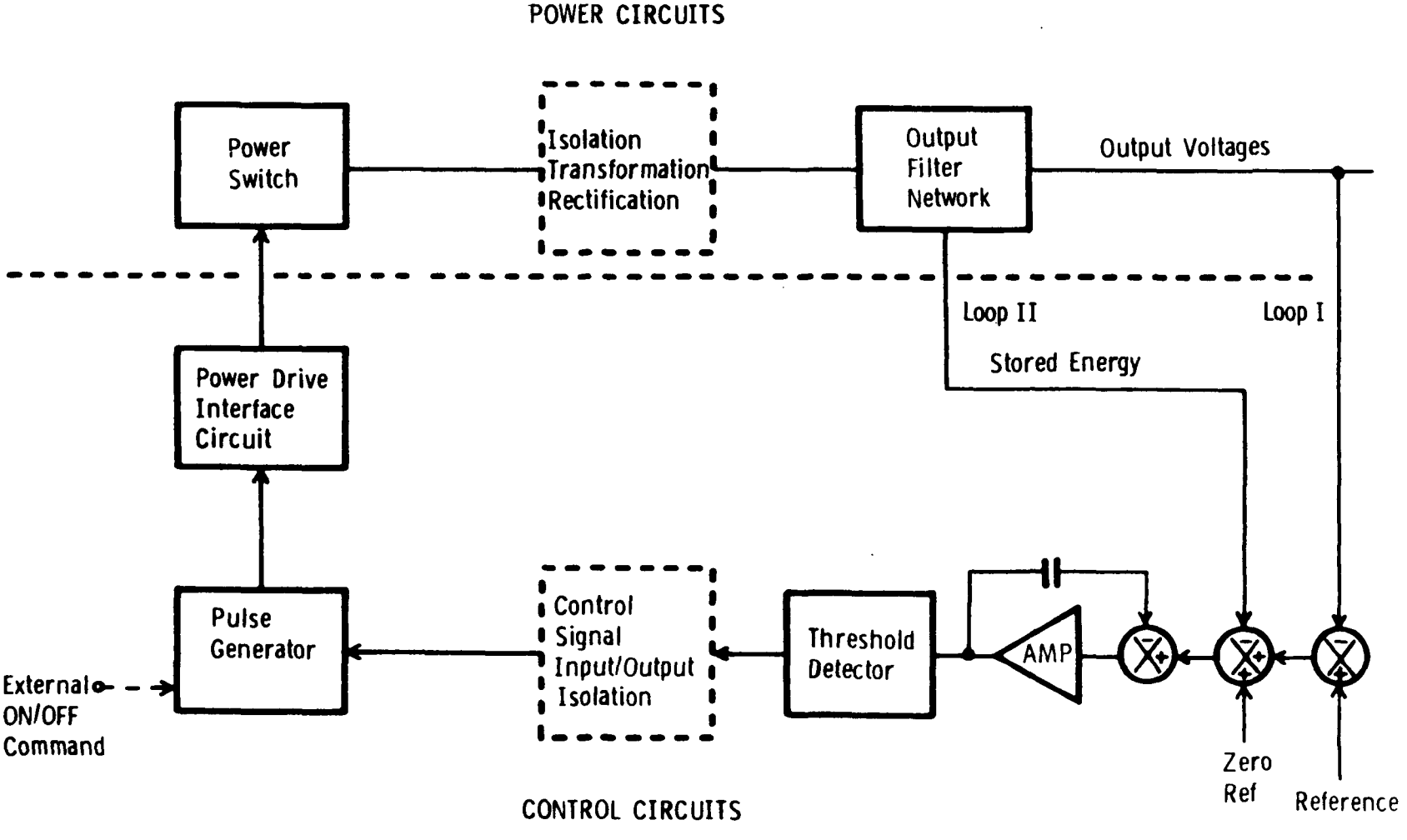


Figure 3-8 ASDTIC TWO-LOOP CONTROL SYSTEM

The ASDTIC system employs two control loops to achieve simultaneously high dc gain and regulator stability. In addition to the conventional dc control loop, loop I of Figure 3-8, there is an ac loop sensing the transient energy storage in the output filter network. The ac information is continuously integrated by the operational amplifier, and is superimposed on the dc error to effect control of the duty cycle of the power switch through a threshold detector and a pulse generator with its attendant power circuit interface circuits.

The ac energy loop which secures zero net energy per cycle is capable of making correction in the power switch duty cycle without having to wait for the relative slow response of the dc loop. The system can therefore be regarded as an adaptive control system, where the regulator action is effective on a per-cycle basis dependent upon any change in energy stored in the output filter network.

Figure 3-9 illustrates a typical Bode plot for an output regulator using ASDTIC control. It shows the gain vs. frequency characteristic for the dc loop and the ac loop. The corner frequency f_1 is due to the time constant of the integrating amplifier, while f_2 is due to the output filter network and the output resistive load. If there were no ac loop, for frequencies higher than f_2, the gain vs. frequency would follow the -40db/decade relationship or greater depending on the characteristics of the output filter network. The ac loop, on the other hand, only has a -20db/decade slope due to the integrator, which intersects the dc loop characteristics at f_3.

The composite open-loop gain-frequency characteristic is therefore represented by the dotted lines in Figure 3-9. Notice at the crossover frequency f_c, a -20db/decade slope is achieved for good phase margin. Consequently, high dc gain, large phase margin, and insensitivity of f_c to the time constant of the output filter and load, are simultaneously achieved.

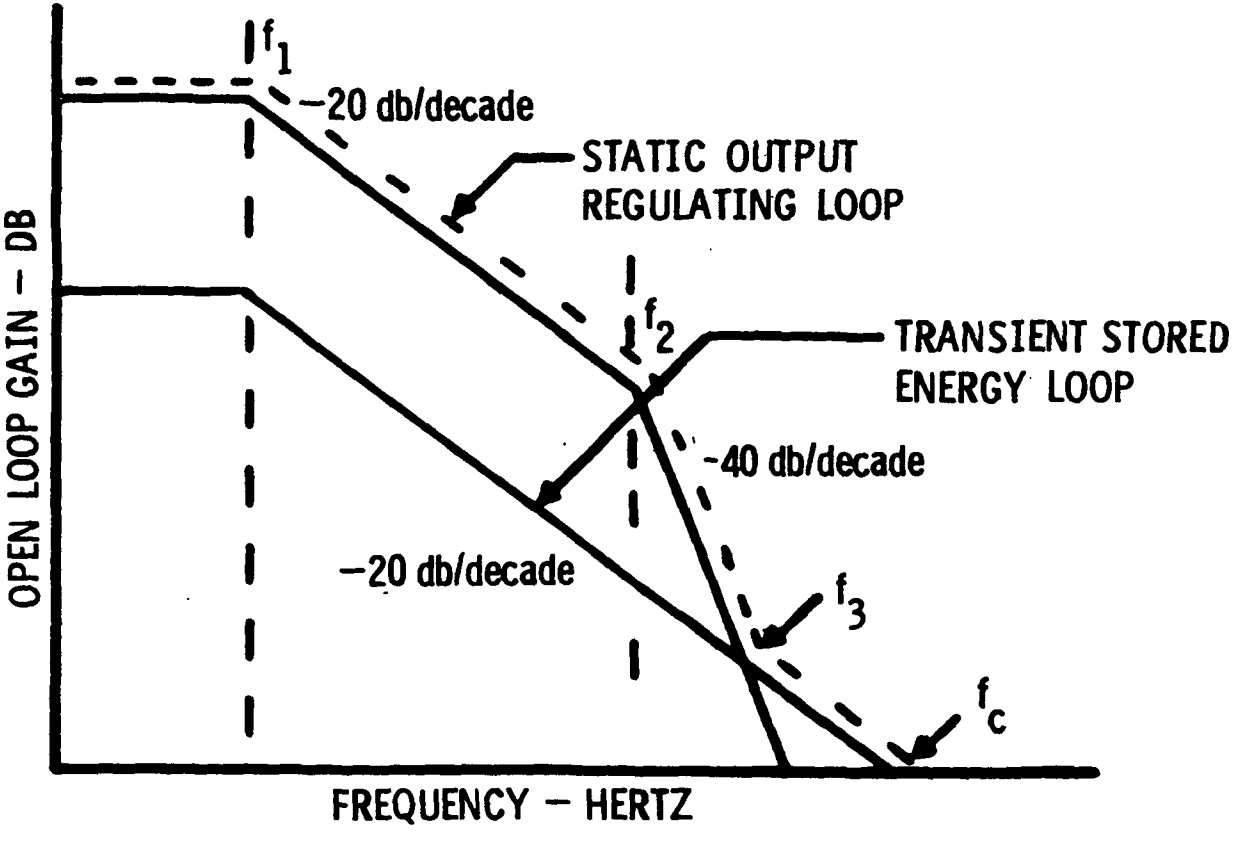


Figure 3-9 BODE PLOT OF ASDTIC CONTROL SYSTEM

The advantages in using ASDTIC in series-inverter operations are derived primarily from the implementation of two-loop control:

- o High dc gain and high ac gain at low frequencies are obtained from the two loops, which provide precision output regulation and active filtering of the line disturbances.
- o Despite the high DC gain, the AC loop maintains regulator stability with a good phase margin. The stable operation is time-invariant as it is insensitive to line, load and circuit parameter changes.
- o Because of the high gain and the adaptive-control property of the ASDTIC AC loop, good dynamic performances can be obtained with respect to line and load changes.
- o The ASDTIC control system has been microminiaturized for size, weight, and part-count reduction.

The V4, V5 and V6 regulator control schematic is shown in Figure 3-10. The DC output is sensed and fed to the ASDTIC integrator U1; also the AC signal from the output capacitor is fed to U1. U2 is the ASDTIC threshold detector. The coupling transformer provides isolation between the output ground system and the series inverter ground system. U3 is the output buffer stage and the signal from U3 goes to the NAND gate between the local bistable and main bistable of the series inverter control logic to provide the regulating function.

U4 and U5 are additional integrators which provide regulating signals from other outputs. (i.e., the beam inverter has the V5 and V6 output from the same transformer. The main regulating loop is the V5 voltage, a supplementary loop is I6 current limit which is fed to U4 integrator input.)

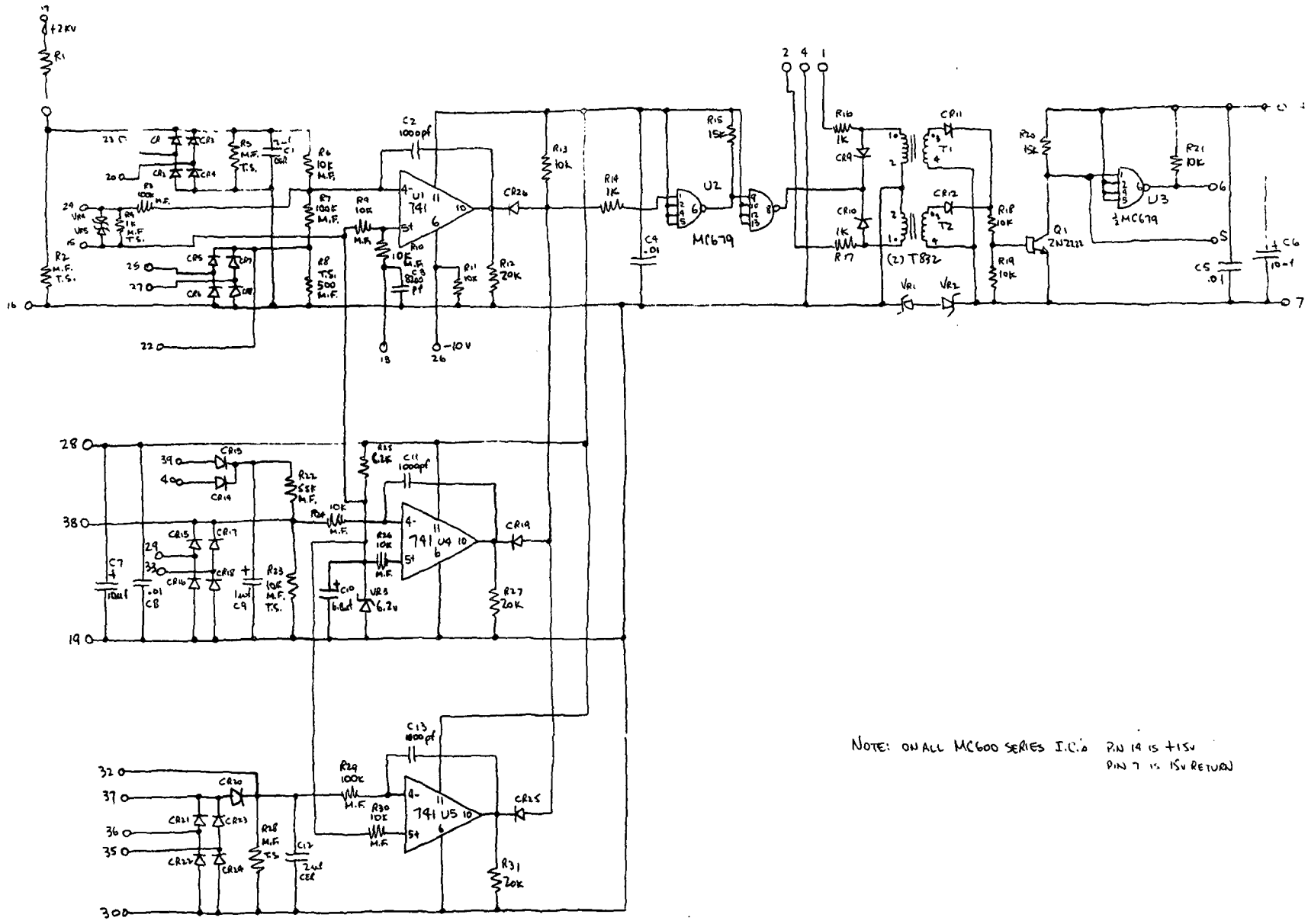


Figure 3-10 V4, V5, V6 Regulator

3.2.1.4 Performance Data

The following paragraphs document the breadboard test data obtained from the ion engine power processor beam supply shown in Figure 3-2. Circuit waveform photographs are presented to show the voltage excursions are within the limits of component ratings for all operating conditions of low line or high line with either normal load or output shorts.

The beam supply uses the ASDTIC principle for its regulating loop. The beam supply output voltage is tablulated below as a function of input line voltage and output current. The beam breadboard output voltage variation was ±0.5V or ±0.025%. The specification requirement is ±1%.

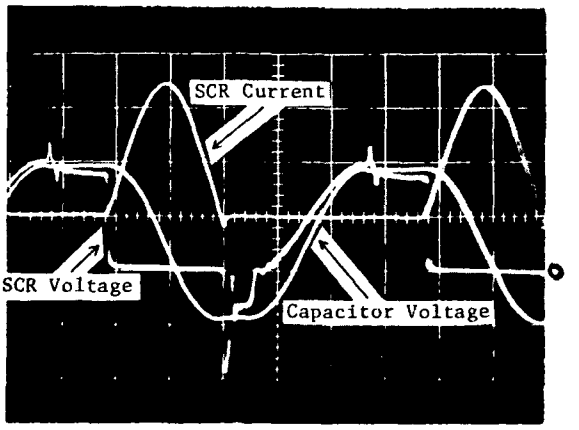
Beam Supply Output Voltage-Volts

V_{IN}	Iout mA				
	950	750	550	350	150
200	2011	2011	2011	2011	2011
250	2011	2011	2011	2011	2011
300	2011	2011	2011	2011	2011
350	2012	2012	2011	2011	2011
400	2012	2011	2011	2011	2011

The beam supply circuit waveform photographs are shown in Figures 3-11 through 3-15. Capacitor voltage is shown on each photograph as a reference.

Figure 3-11 shows waveforms of the mainline SCR voltage and current and the capacitor voltage for an input dc voltage range of 200V to 400V and normal output conditons. Sinewave currents flow through the SCR and the amplitude is held constant as the input is varied from 200 to 400 volts. The capacitor voltage shown controls the firing of the mainline SCR's such that the capacitor and SCR peak voltages are under control and within the limits of component ratings.

The SCR voltage shows a high peak reverse voltage up to about 400V during turn-off because of the energy left in the inductor due to SCR reverse turn-off current. The peak transient of about 80V that occurs 30ms later in the 200V input photograph is due to the other mainline SCR turning off. The SCR reverse turn off current is a parameter that must be reduced to obtain control of transients and reduce power loss in the SCR suppression networks since at present the SCR suppression networks are designed to absorb this transient.



MAINLINE SCR
VOLTAGE
CURRENT

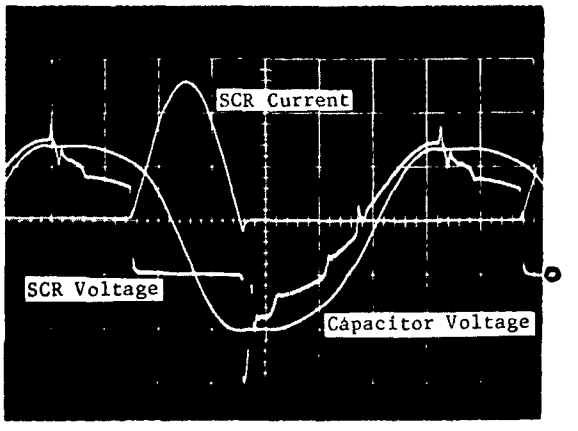
V = 200V/div

I = 20A/div

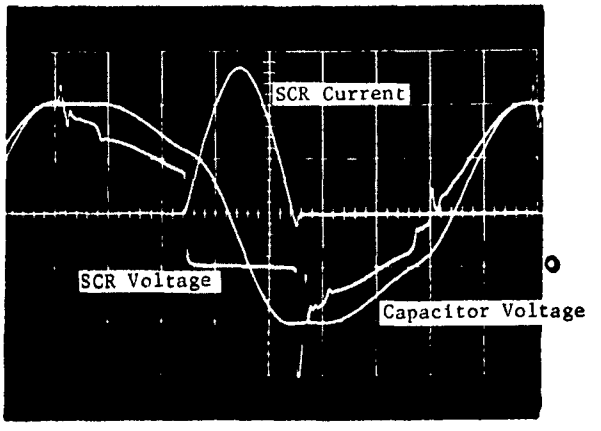
T = 10μsec/div

FULL LOAD

V_{in} = 200V



V_{in} = 300V



V_{in} = 400V

CAPACITOR VOLTAGE

V = 200V/div

Figure 3-11 Mainline SCR Voltage and Current, Capacitor Voltage Waveform - Normal Output

Figure 3-12 shows waveforms of the mainline SCR voltage and current and the capacitor voltage for a shorted output condition. The peak SCR current remained constant as the output was shorted. The capacitor and SCR peak voltages increased by the amount equal to the normal transformer voltage of 90V and are under control and within component limitations.

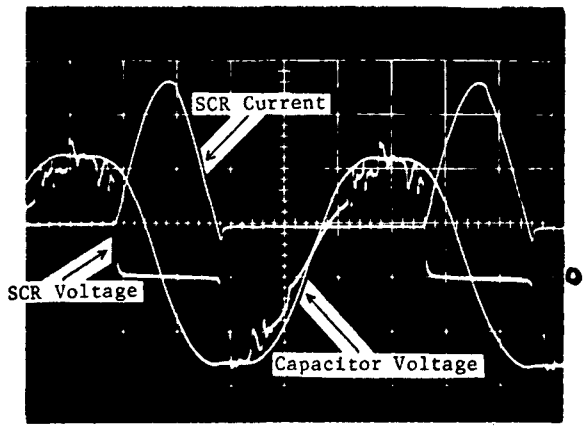
Figure 3-13 shows waveform of the auxiliary SCR voltage and current and the capacitor voltage for a normal output condition. The auxiliary SCR transfers the excess energy stored in the series capacitor to the load or to the source. With low input voltage, the excess energy is small therefore the auxiliary SCR conducts very little current. As the input voltage is increased, the excess energy increases and consequently the auxiliary SCR conducts more current in order to stabilize the system.

Figure 3-14 shows waveforms of the auxiliary SCR voltage and current and the capacitor voltage for a shorted output condition. With no power being delivered to the load, the excess energy in the system is large and therefore the auxiliary SCR transfers a larger amount of current in order to keep the system under control.

Figure 3-15 shows waveforms of the transformer voltage and current and the capacitor voltage. The power transformer current is not a pure sine-wave since it is the sum of the auxiliary and mainline SCR currents yielding a complex waveform.

Figure 3-16 shows a plot of the beam supply efficiency versus line voltage for two load conditions. The reduced efficiency at an input voltage of 250V is a result of an increase in the peak current in the system.

The reduced efficiency for the beam supply at an input voltage range of 210 to 280V is a result of an increase in the peak current which is caused by an unbalance in the system due to lower efficiency of the power SCR's. The arc supply does not exhibit this condition because the overall power level is lower, the percentage unbalance is less, and the SCR efficiency is higher. The major loss contributor in the beam supply is the SCR's which are very sensitive to current. (SCR losses; Beam 5.8%; Arc 1.76%.) The losses associated with the SCR's in the beam supply with increase in peak current are significant and appear as efficiency losses.

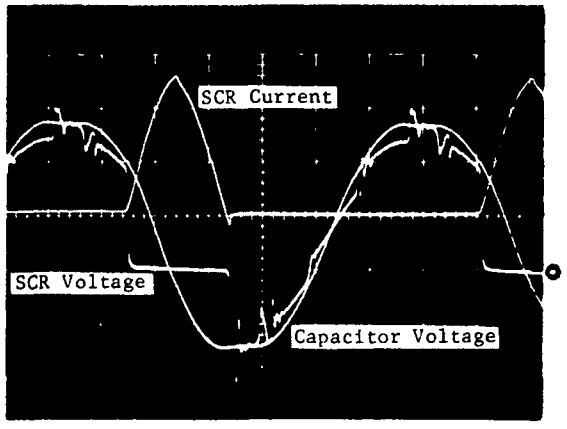


MAIN LINE SCR
VOLTAGE
CURRENT

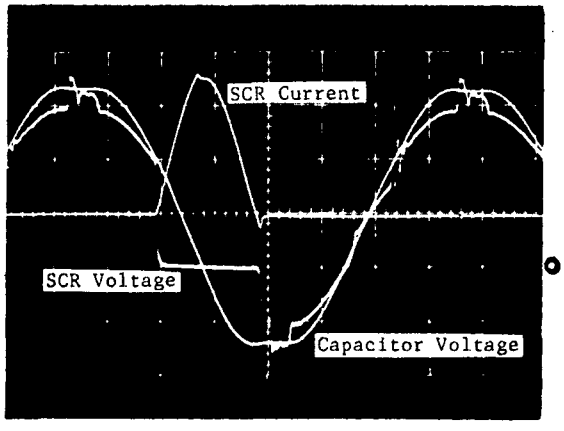
V = 200V/div
I = 20A/div
T = 10usec/div

SHORT CIRCUIT

V_{in} = 200V



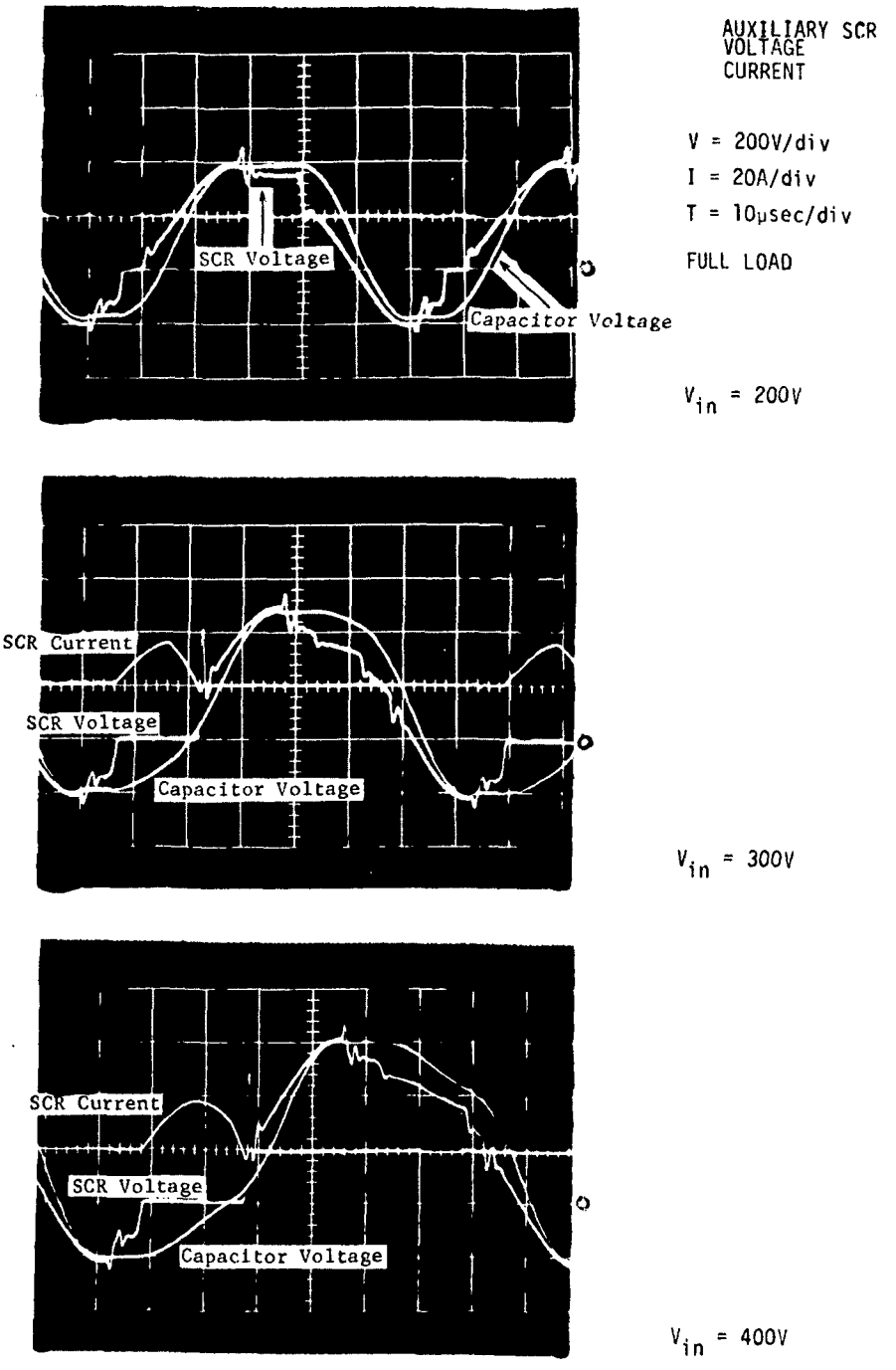
V_{in} = 300V



V_{in} = 400V

CAPACITOR VOLTAGE
V = 200V/div

Figure 3-12. Mainline SCR Voltage and Current, Capacitor Voltage Waveforms - Output Shorted



AUXILIARY SCR
VOLTAGE
CURRENT

V = 200V/div
I = 20A/div
T = 10μsec/div

FULL LOAD

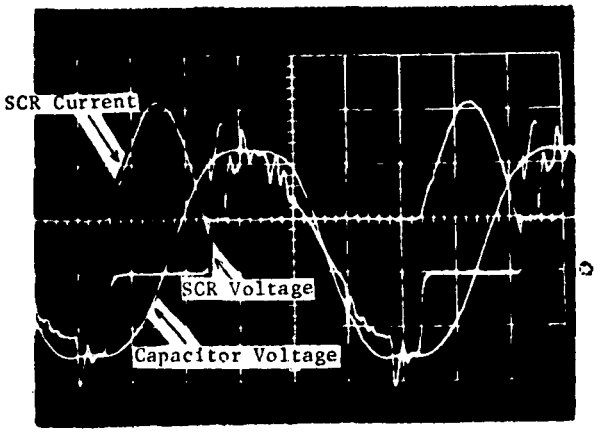
V_{in} = 200V

V_{in} = 300V

V_{in} = 400V

CAPACITOR VOLTAGE
V = 200V/div

FIGURE 3-13 Auxiliary SCR Voltage and Current
Capacitor Voltage
Normal Output

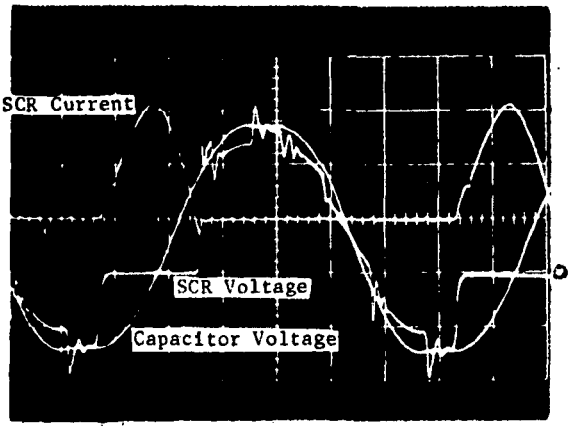


AUXILIARY SCR
VOLTAGE
CURRENT

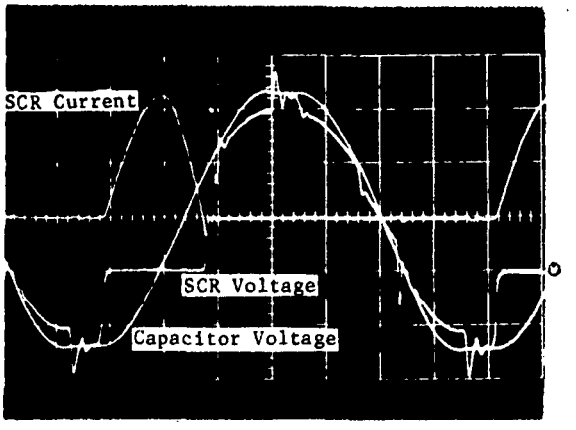
V = 200V/div
I = 20A/div
T = 10μsec/div

SHORT CIRCUIT

V_{in} = 200V



V_{in} = 300V



V_{in} = 400V

CAPACITOR VOLTAGE
V = 200V/div

Figure 3-14 Auxiliary SCR Voltage and Current Capacitor Voltage Output Shorted

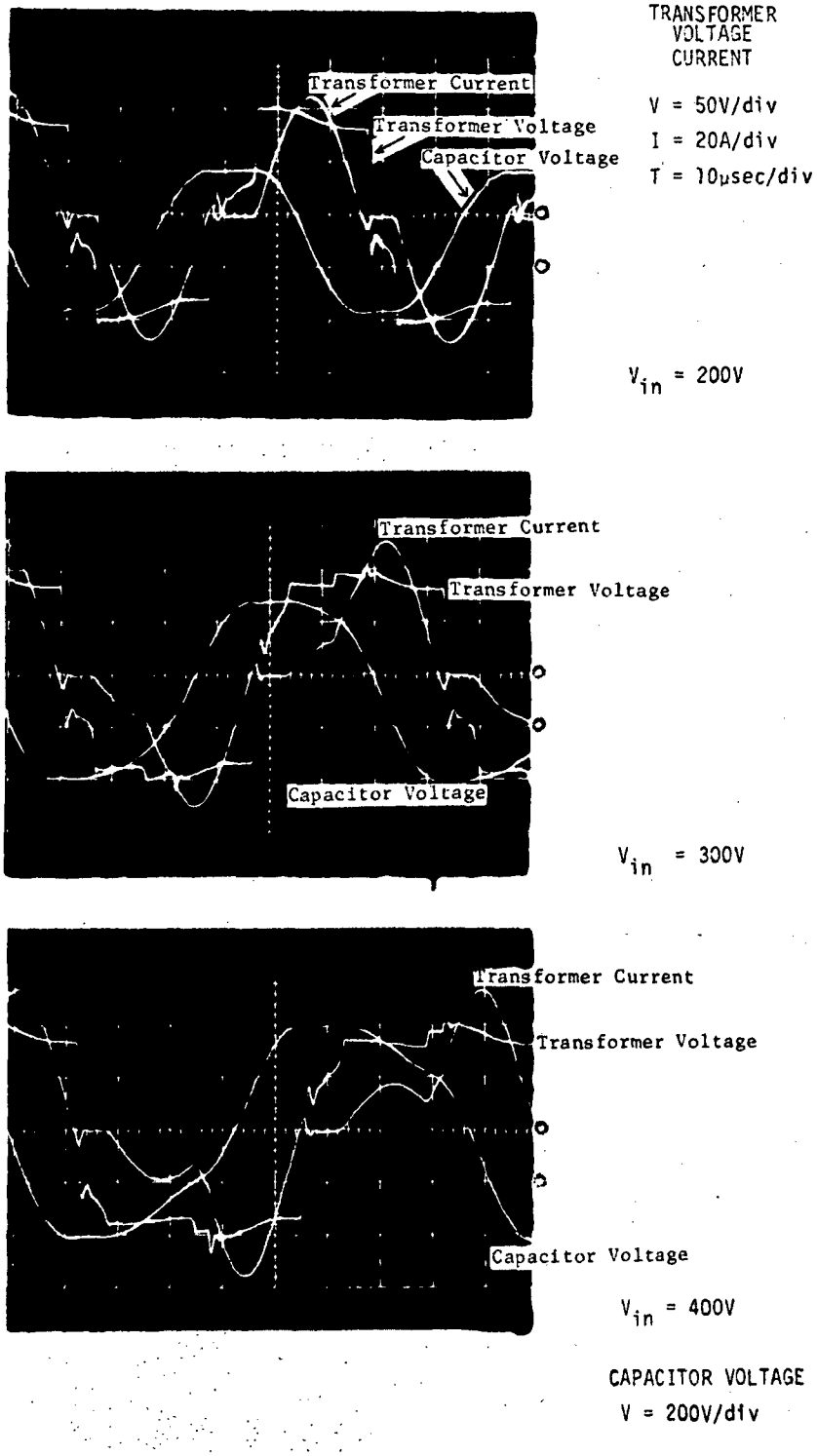


**Figure 3-15 Transformer Voltage & Current
Capacitor Voltage
Normal Output**

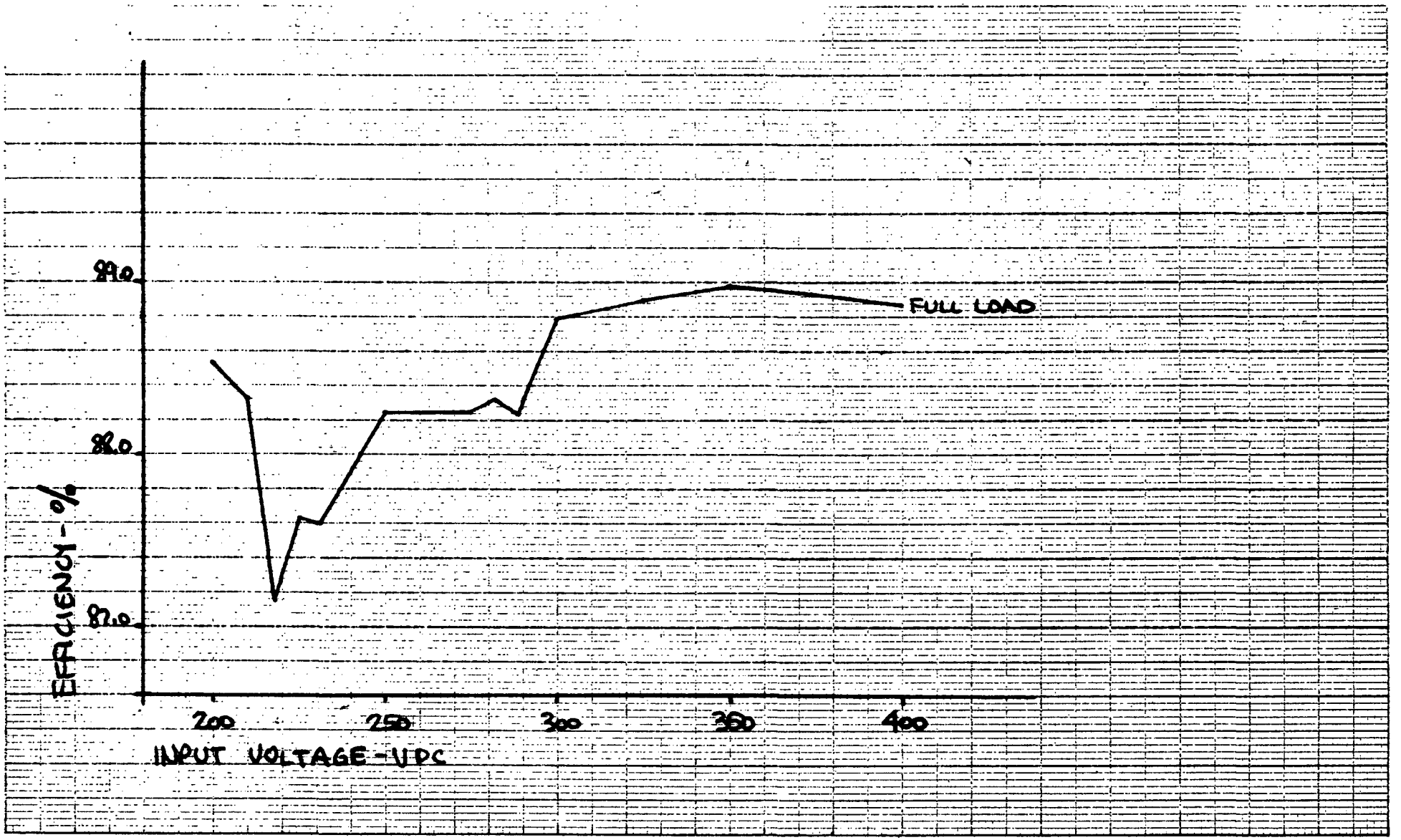


Figure 3-16 Beam Supply Efficiency

Figure 3-17 shows the RMS input ripple current as a function of input voltage for the beam supply. This variation in input current ripple is also effected by the changes in the peak-to-peak current variation in the power stage. The specification limit is 1% RMS of the maximum input dc current which is about 0.125A RMS.

The main advantage of the series resonant inverter is that it is a current source and does not reflect a high peak surge back to the power source. Figure 3-18 and 3-19 show the input current during turn on and turn off.

Figure 3-20 shows the input current during a short across the output. The current variation is due to contact bounce in shorting mechanism. Figure 3-21 shows the input current when a short is removed. The ac variations in the input current is due to momentary arcing between the shorting contacts when they are pulled apart. Figure 3-22 and 3-23 show the input current when the system is started into a no load condition

During all these transient conditions, no large current surge was drawn from the dc power bus that could cause collapse of the current limited solar array source. No extra current regulator circuitry was added to the system to provide this protection feature which is inherent in the series resonant inverter design.

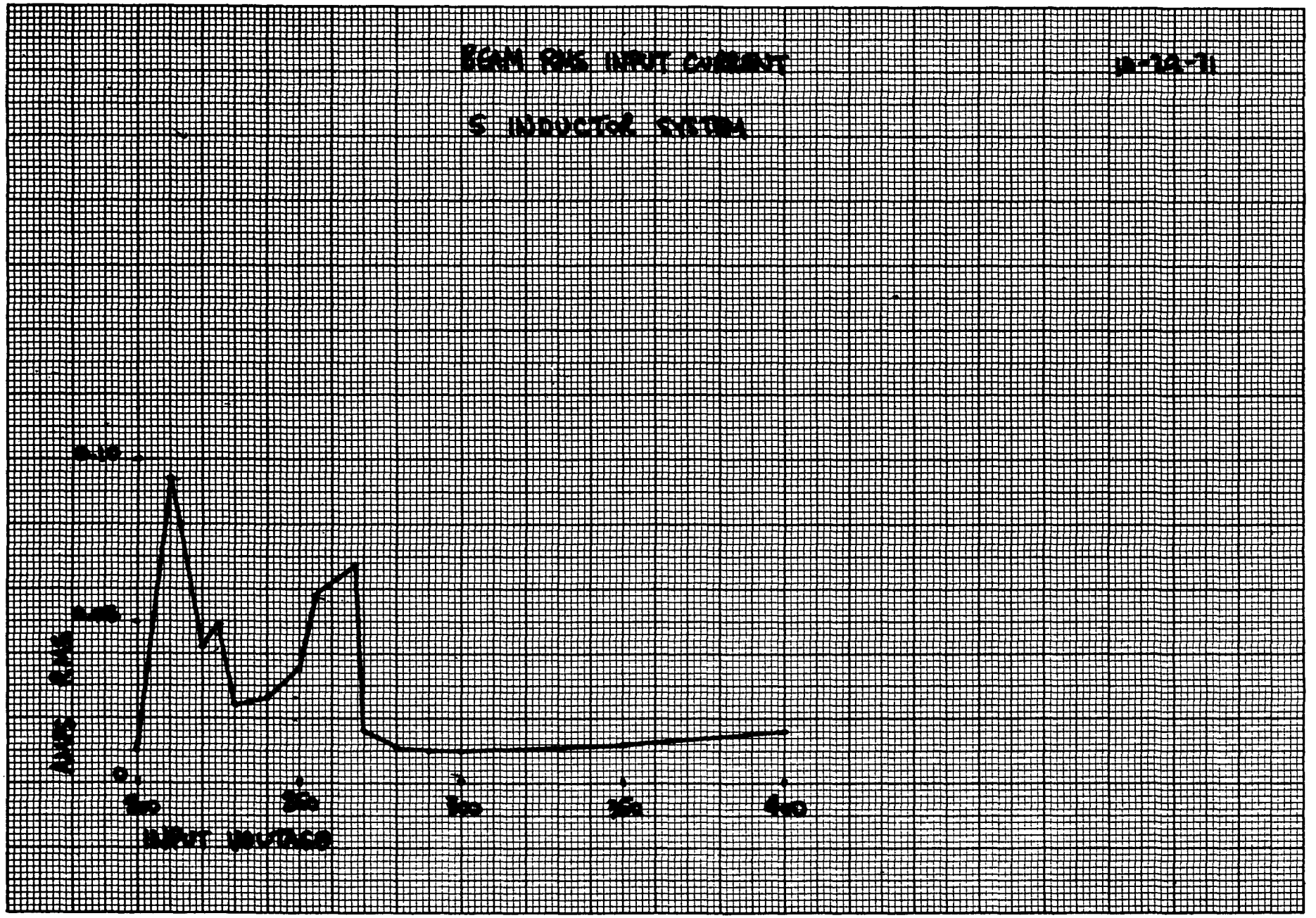
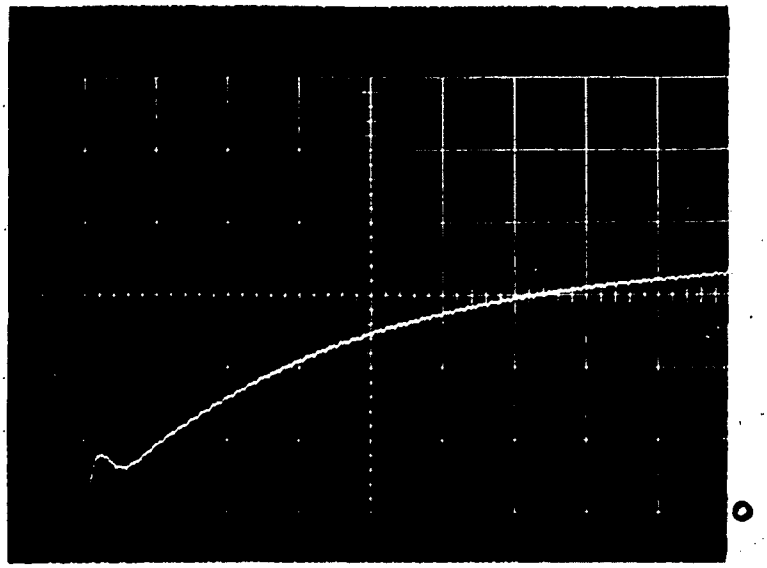


Figure 3-17



Input Current

I = 2 Amp/div

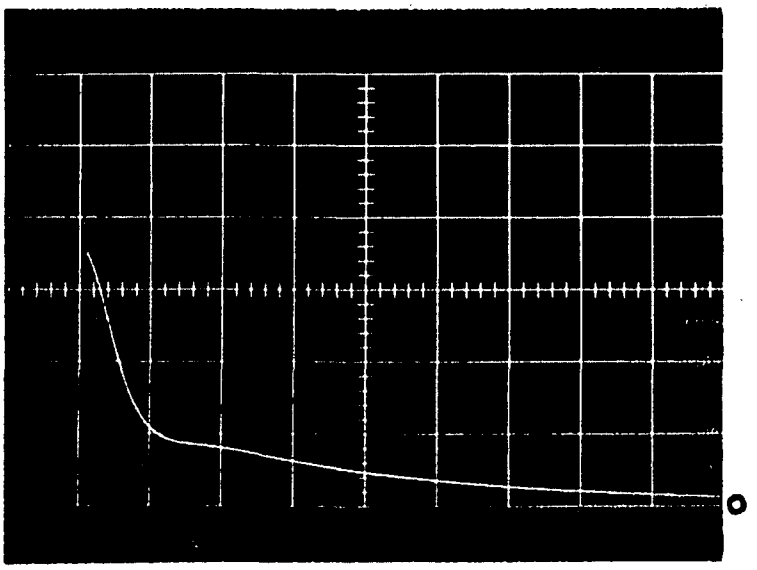
T = 500 μs/div

Turn"ON"

Vin = 300v

Iin = 7.3 Amp
(Full Load)

Figure 3-18



Input Current

I = 2 Amp/div

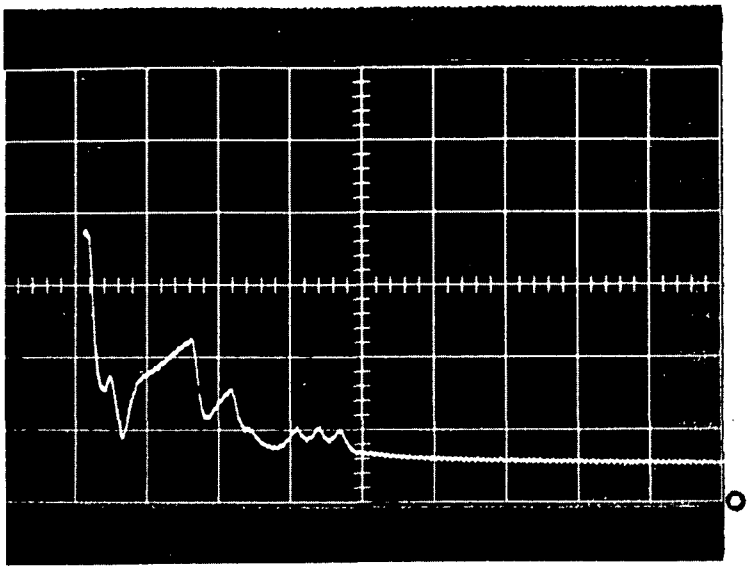
T = 200 μs/div

Turn "OFF"

Vin = 300v

Iin = 7.3 Amp
(Full Load)

Figure 3-19



Input Current

I = 2 Amp/div

T = 1 ms/div

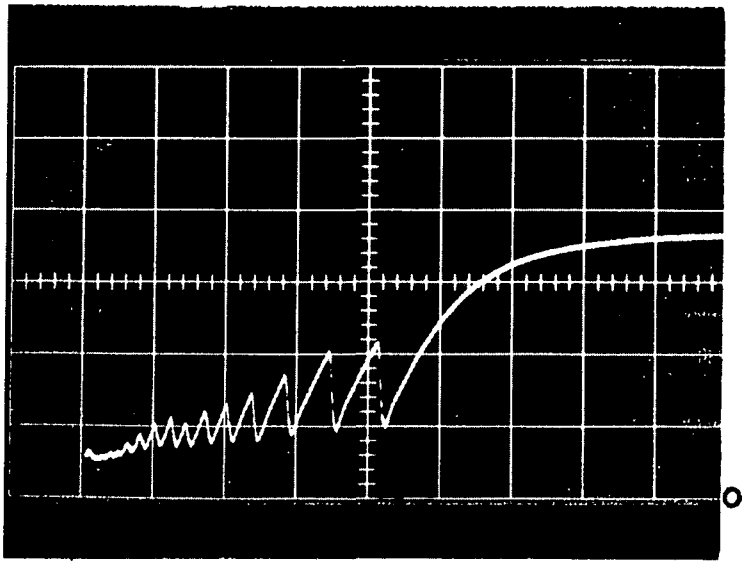
Short "ON"

Vin = 300v

Iin = 7.3 Amp.

(Full Load)

Figure 3-20



Input Current

I = 2 Amp/div

T = 2 ms/div

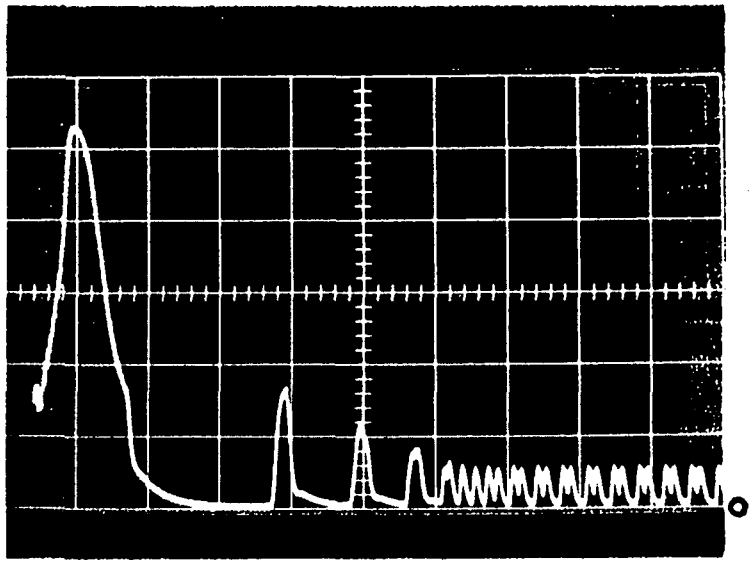
Short "OFF"

Vin = 300v

Iin = 7.3 Amp

(Full Load)

Figure 3-21



Input Current

I = 2 Amp/div

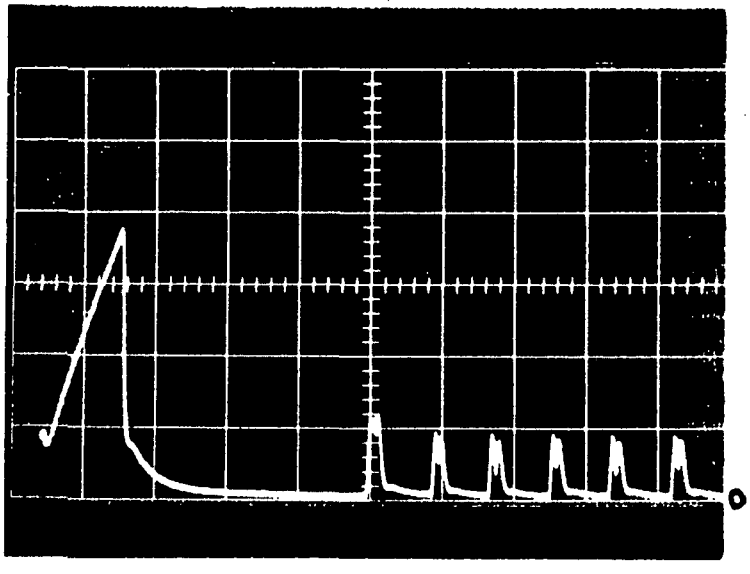
T = 2 ms/div

Turn "ON"

Vin = 200v

Iin = 580 ma
(51 ma Load)

Figure 3-22



Input Current

I = 2 Amp/div

T = 2 ms/div

Turn "ON"

Vin = 336v

Iin = 270 ma
(51 ma Load)

Figure 3-23

3.2.3 Series Inverter No. 1 Multiple Output Inverter

The multiple output inverter uses the same series resonating power stage as the V4 inverter. The output stage shown in dashed lines in Figure 3-24 is replaced by the output stage shown in Figure 3-26. The L and C values for the multiple inverter are as follows:

$$L1, L2, L3, L4 = 260\mu H$$
$$L5 = 80\mu H$$
$$C1, C2 = .085\mu F$$

The sinusoidal current I flowing through the series connected output transformer string shown in Figure 3-26 is a constant frequency, constant amplitude current. The turns ratio of the series connected transformers determine the power sharing of the series string. Regulation of each output is achieved by phase firing of the shunt transistor which shunts the transformer secondary current thus regulating the output.

3.2.4 Series Inverter No. 2 (Arc Supply)

The schematic of the V4 series inverter power stage is shown in Figure 3-24. The operation of the inverter is similar to the V5, V6 inverter discussed in Section 3.2.1.

The arc supply also uses the ASDTIC principle for its regulating loop. The arc supply output current variation is $\pm$4mA or $\pm$.05%. The results are tabulated below. The specification requirement is $\pm$0.1%. The magnetic current sensors contribute most of the regulation error.

Arc Supply Output Current - AMPS

Vin	Vout Volts			
	30	20	10	0
200	7.603	7.605	7.606	7.611
250	7.607	7.606	7.607	7.610
300	7.606	7.606	7.608	7.609
350	7.606	7.606	7.608	7.609
400	7.606	7.606	7.608	7.609

Figure 3-25 shows a plot of the arc supply efficiency versus line voltage.

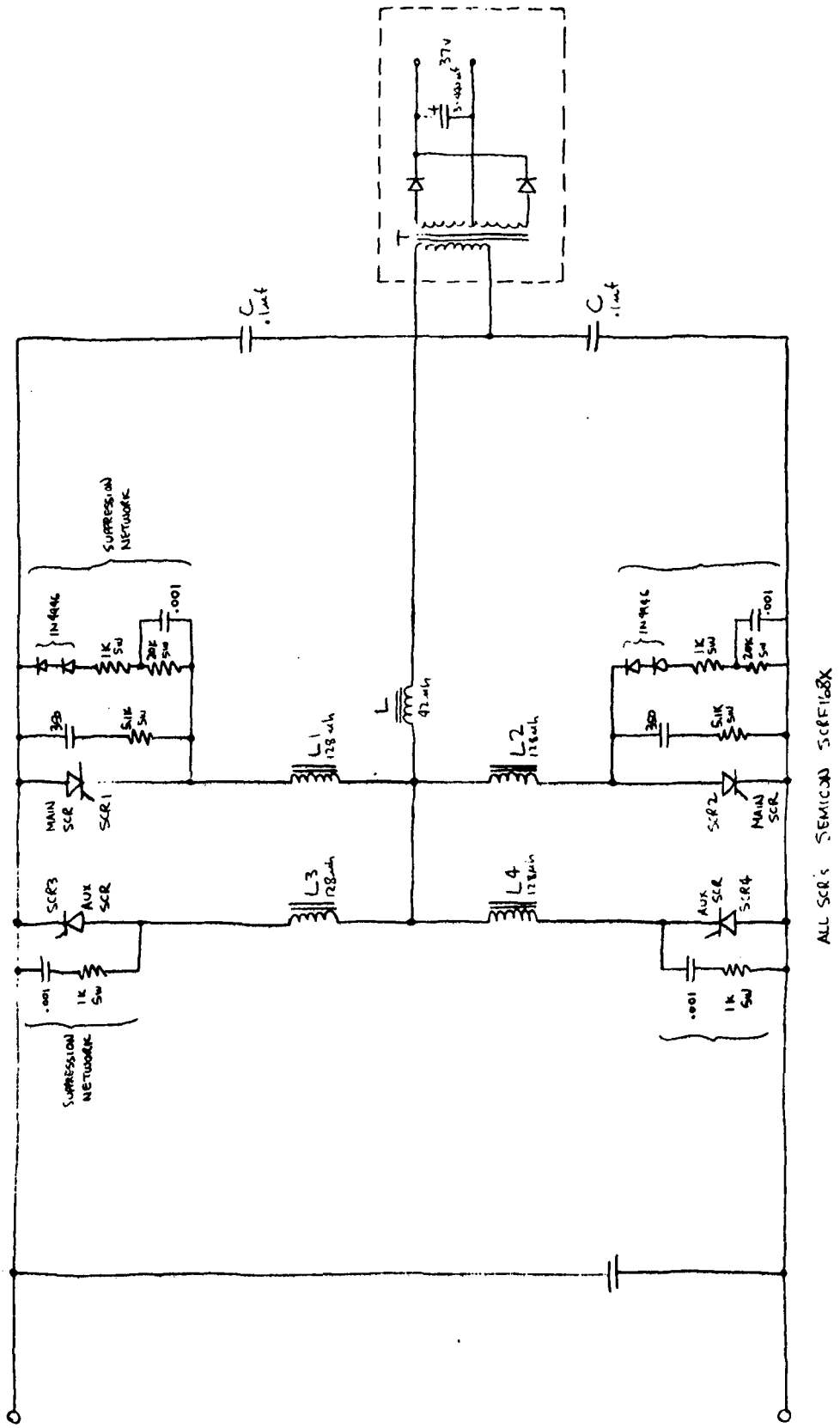


Figure 3-24. Arc and Multiple Inverter Power Stage

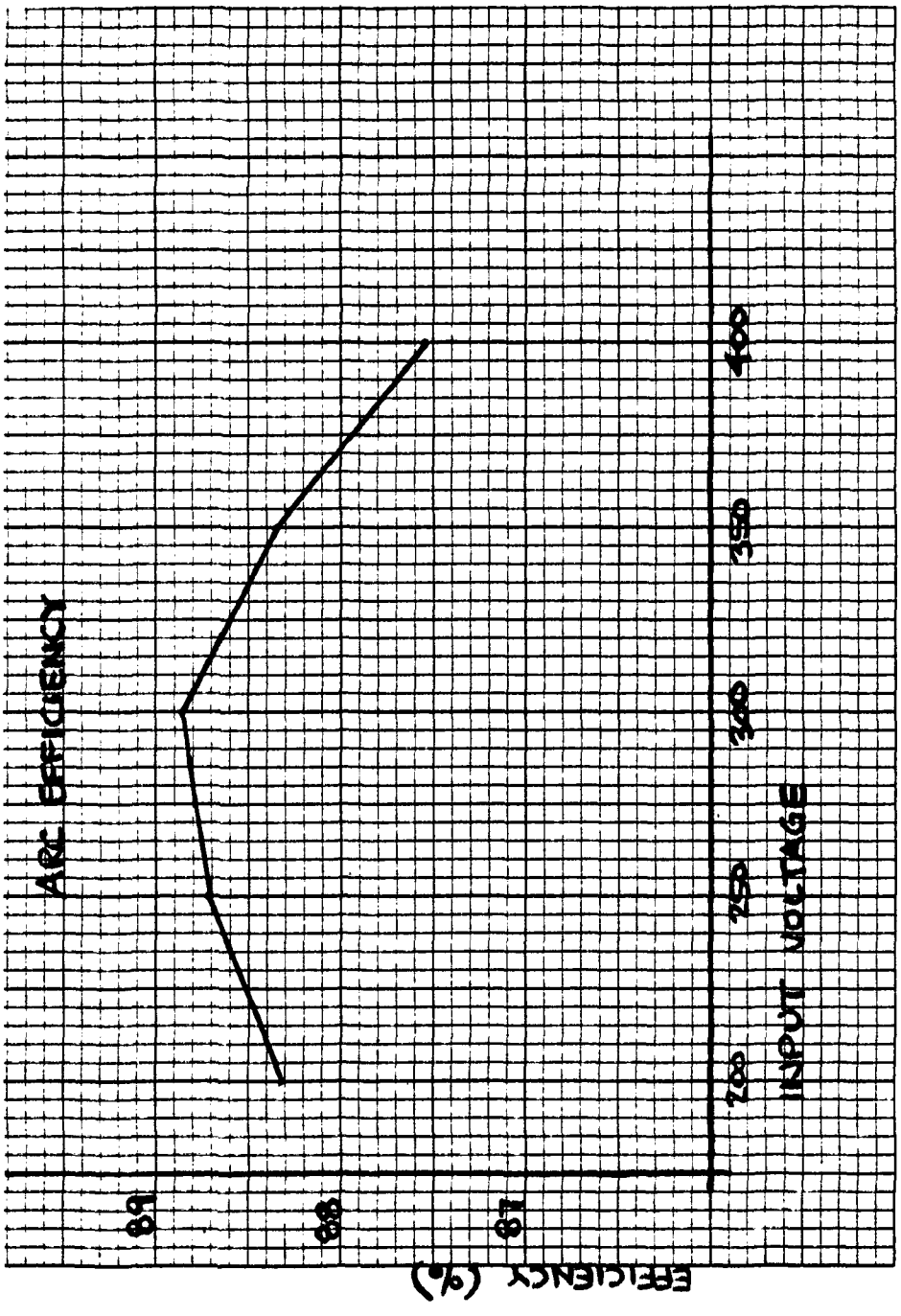


Figure 3-25. Arc Supply Efficiency

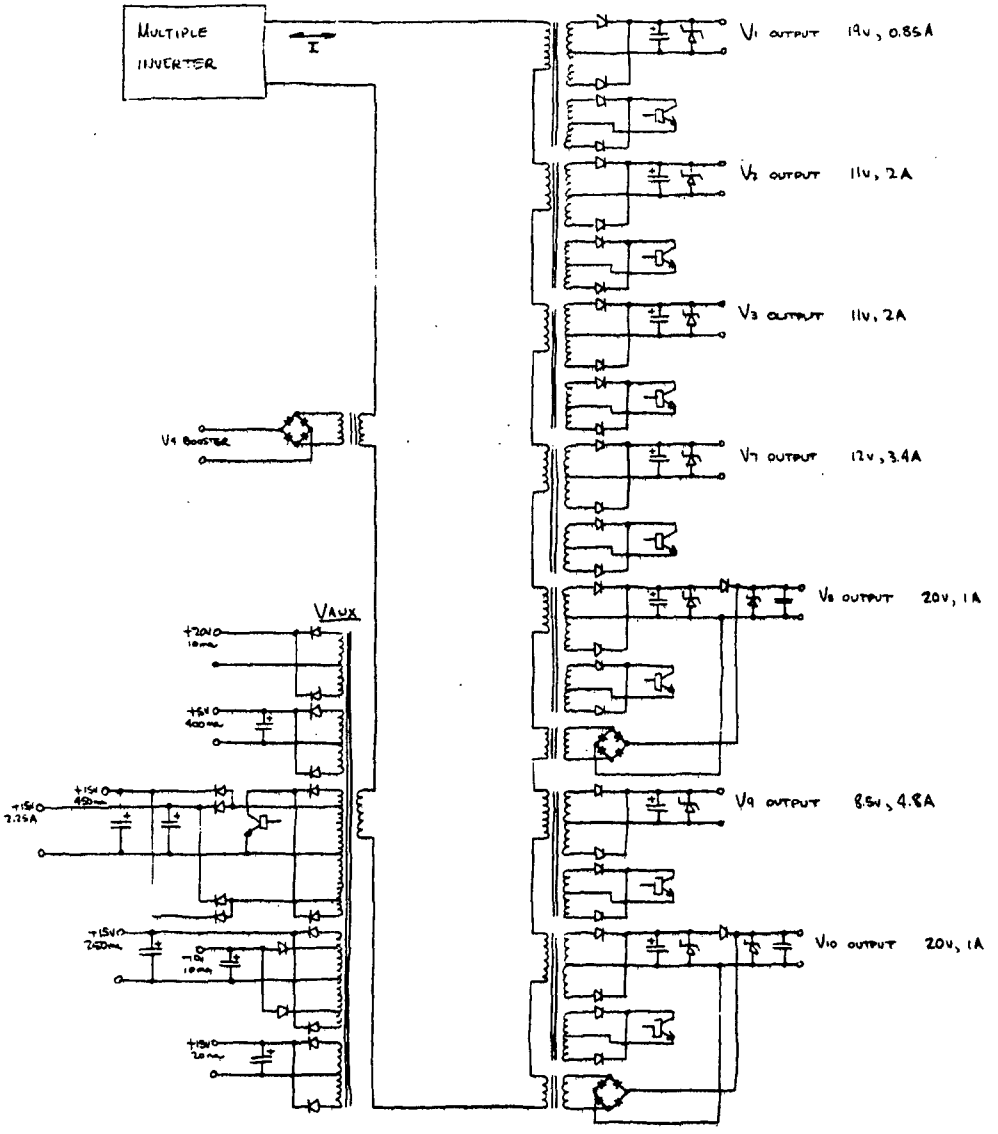


Figure 3-26. Multiple Output Inverter Block Diagram

Figure 3-27 illustrates the output regulator for the low power outputs (V2) with U1 providing the voltage regulation function. U2 provides the current regulation function. U5 provides the closed loop function between the I5 current and the I2 current. U3 is the ASDTIC threshold detector and U4 is the output buffer stage which provides drive to the shunt transistor (2N2880) through a stage of current amplification.

3.3 Mechanical Design

Figure 3-28 shows the total fabricated breadboard. Its overall envelope dimensions are 76cm (30 in) x 91cm (36 in) x 15cm (6 in) high. The unit is designed to operate at room ambient. The baseplate was not designed to adequately distribute the heat in the power SCR's to the baseplate for operation in thermal vacuum.

The breadboard was layed out to optimize the power flow from input to output and to separate the high voltage circuitry from the low voltage circuitry. Optimum grouping of components was determined so that noise coupling from the high power circuitry to the control circuitry would be minimized and the interwiring between functions simplified.

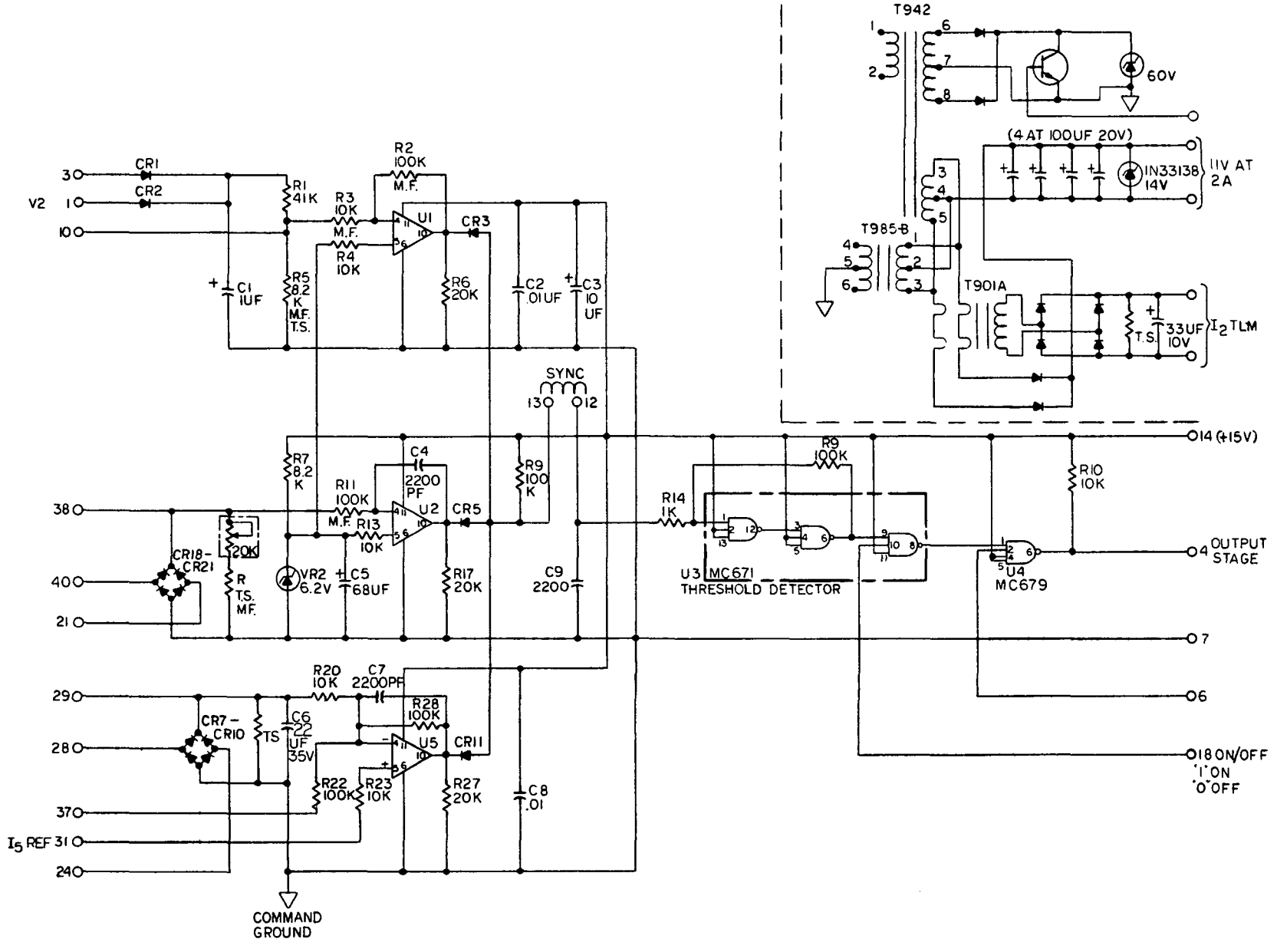


Figure 3-27. Multiple Output Regulator, V2

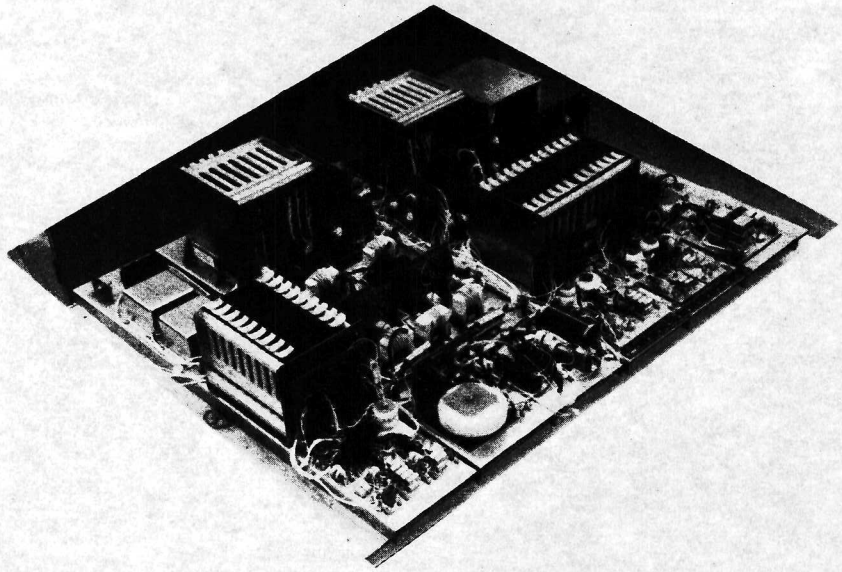


Figure 3-28 20CM Ion Thruster Power Processor Breadboard

The unit consists of six 6" x 30" - 60 mil aluminum channels which were bolted together after component assembly had been completed. Two 1 inch aluminum angles were bolted along each 36 in. edge for increased structural rigidity.

Figure 3-29 illustrates the basic layout of the breadboard with the functions identified. All of the outputs from the power processor are on the right side of the power processor with high voltage outputs separated from the outputs operating at ground potential (V2, V7, V8).

The input power comes into the input filter area and into the beam supply inverter. Therefore most of the power for the power processor has a short cable run from the input filter. All of the output regulators have majority voting redundancy (2 out of 3) and a separate control card is used for each non-redundant channel.

The inverter control logic for the arc, multiple, and beam power inverter is located on the left side of the power processor. The beam and arc redundant regulators and the command and protection system are also located in the same area.

The total weight of the unit is 25.6KG (56.6 lbs) with a component weight of 9.0KG (20 lbs)., Section 3.5.1 will identify the component weight for each function of the power processor. In the construction of the control cards both cost and ease of removal were the governing design requirements.

Four multiple use PC cards were designed to facilitate construction of the power processor controls and regulators. These designs were made for the worst case in each application and sections were used as appropriate for a particular regulator or control.

These control cards include:

(1) Inverter logic flip flop
(2) Inverter logic SCR sequencing
(3) V4 and V5 output regulator
(4) Multiple output regulators

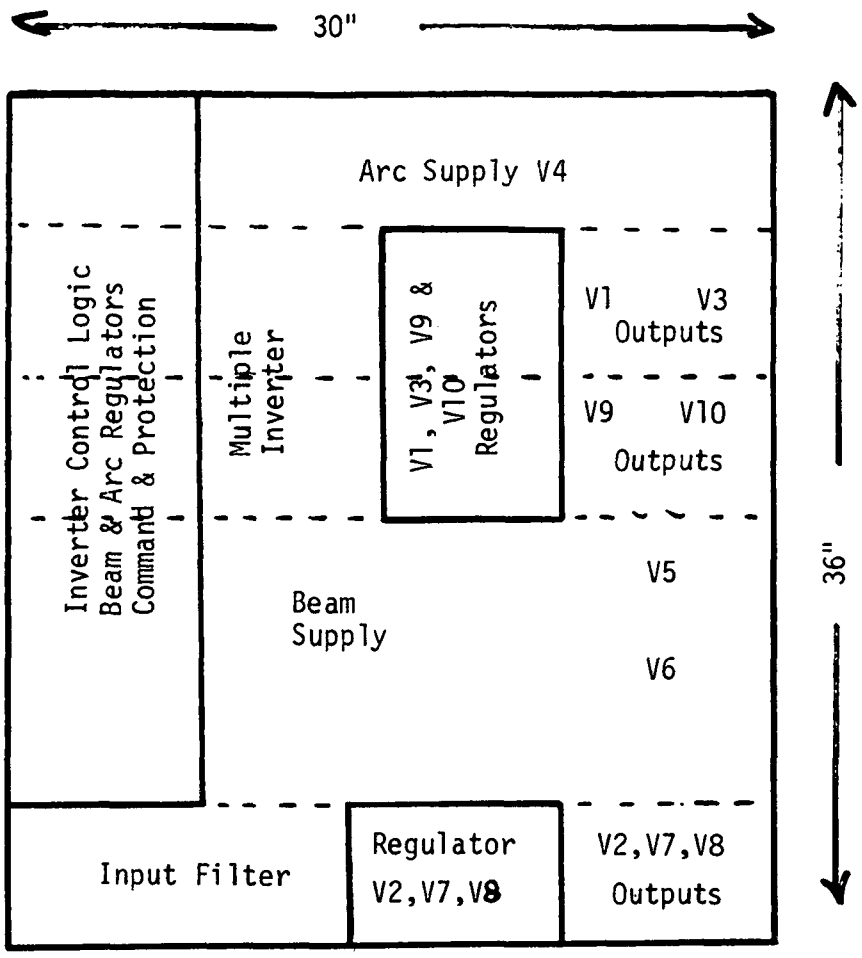


FIGURE 3-29. BREADBOARD LAYOUT

Figure 3-30 illustrates these different card designs. Each card has a 41 pin Elco connector. This is a rugged connector so that the reliability of the card connection would be high with repeated insertion and removal from the mating connector during development testing.

Both the connectors, the excessive card area, and rigid card mounting fixture penalized the weight of the power processor breadboard design.

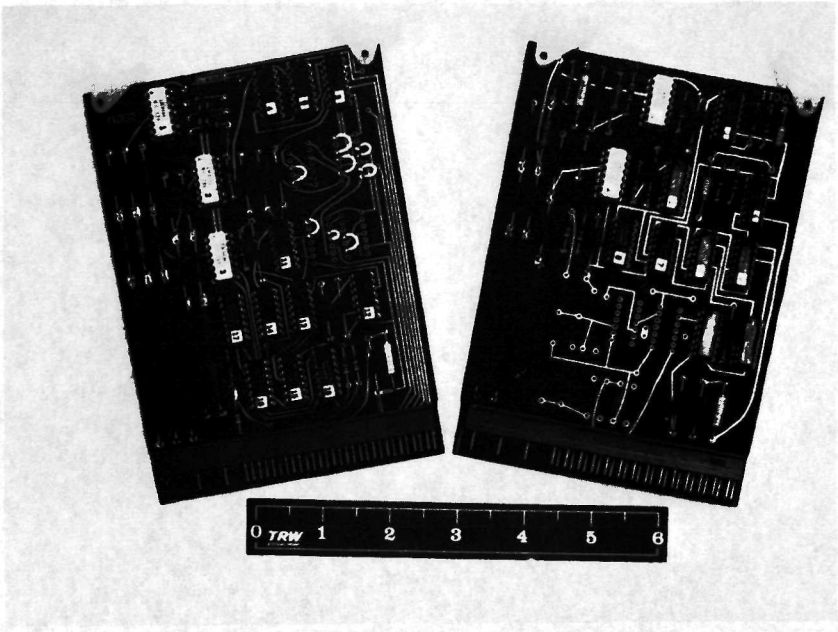
Figure 3-31 shows the cards for the command and protection system. Hard wiring is used on these cards because there was no commonality between cards.

3.4 20CM Power Processor Test Results

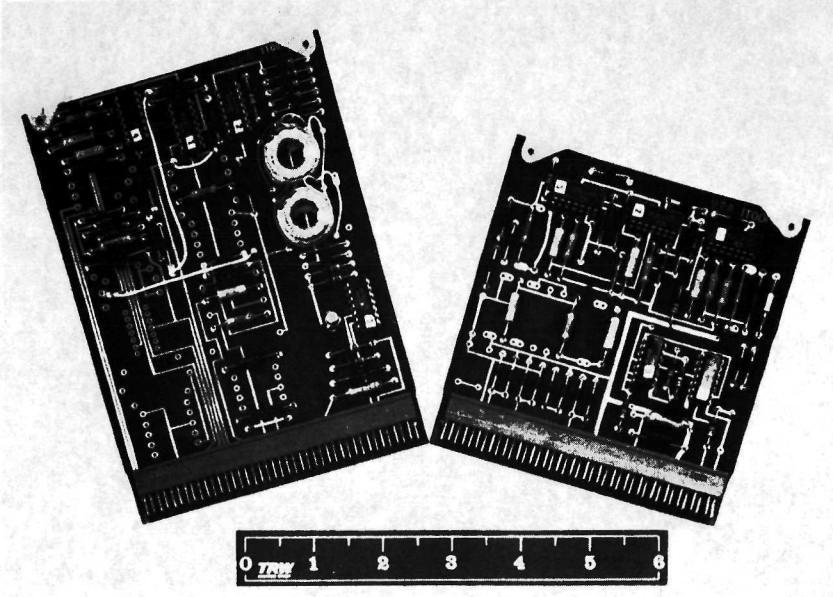
Tests were performed to check out regulation, efficiency, command, telemetry and output fault protection. During the output fault protection tests, three transformers, V4 booster, V1 power and V10 power, failed with a short between the secondary and shield. At the time of the testing, the failure was blamed on a poor electrostatic shield connection. It was later discovered during ion engine/power processor integration tests that the beam supply output was overshooting to over 3kV during shorting tests and was causing the component failure.

Tables 3-II, -III and -IV presents the input and output data over the input line range of +200V to +400Vdc when operating at full output power. Tables 3-V, -VI and -VII present the data when operating at half output power. Efficiency ranged from 86.7 to 85.4% at full power and 83.8 to 82.1% at half power. The V5 regulation is $\pm$ 1.5V out of 2kV (< 0.1%) and the I4 regulation is $\pm$ 12mA out of 9A (< 0.15%). This superior performance is obtained by using the ASDTIC control system which is described in Section 3.2.1.3.

Figure 3-32 illustrates the input current ripple as a function of input supply voltage. The specification limit is 150mA RMS (1% RMS of the maximum input current). At low input voltages this magnitude is exceeded.



a) Inverter Control Logic



b) Regulator Controls

FIGURE 3-30 PHOTOS OF CONTROL CARDS

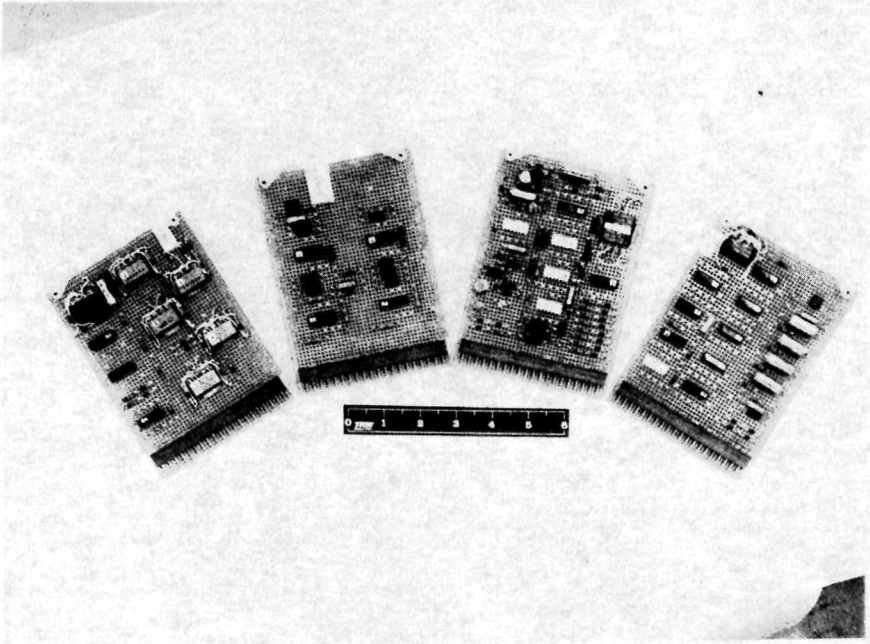


FIGURE 3-31 PHOTO OF COMMAND & PROTECTION CONTROL CARDS

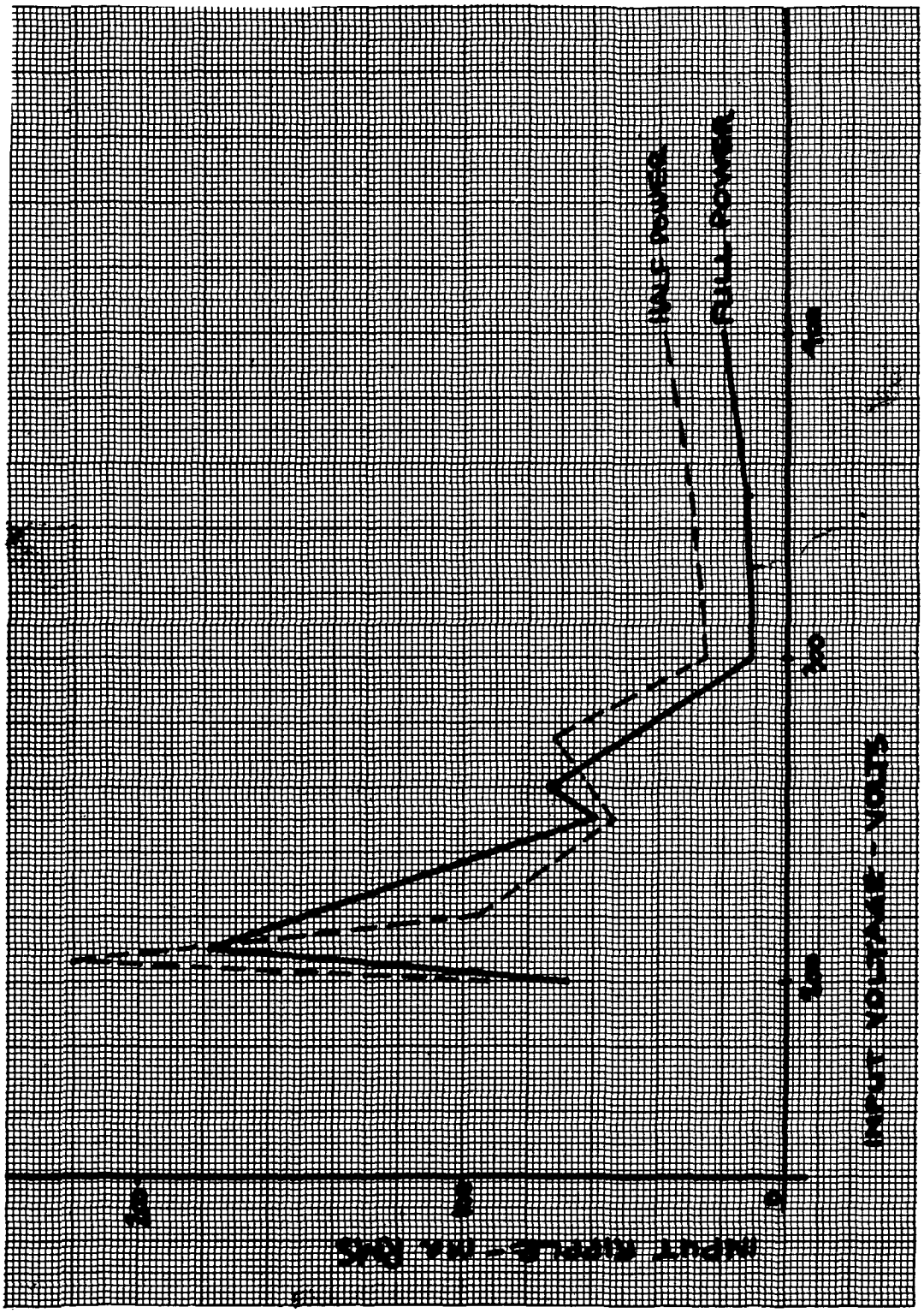


FIGURE 3-32. INPUT RIPPLE

TABLE 3-II. 20CM POWER PROCESSOR ELECTRICAL PERFORMANCE

FUNCTION	VOLTAGE	CURRENT	VOLTAGE RIPPLE P-P	CURRENT RIPPLE P-P	POWER
V_{IN}	201.2	13.492			2714.59
V_2	11.10	1.99	0.90 v	100 ma	22.09
V_7	11.55	3.20	0.95	150	36.96
V_8	20.67	1.015	1.40	45	20.98
V_1	17.61	0.85	3.00	65	14.97
V_3	10.44	1.98	1.00	120	20.67
V_9	7.44	4.76	1.20	360	35.41
V_{10}	18.67	0.955	1.10	45	17.83
V_4	34.60	8.895	2.10	200	307.77
V_5	2019	0.9192	0.38	—	1855.86
				TOTAL OUTPUT POWER	2332.54
				EFFICIENCY	85.93%

TABLE 3-III. 20CM POWER PROCESSOR ELECTRICAL PERFORMANCE

FUNCTION	VOLTAGE	CURRENT	VOLTAGE RIPPLE P-P	CURRENT RIPPLE P-P	POWER
V_{IN}	303.4	8.927			2707.54
V_2	10.94	1.97	0.75v	85 ma	21.55
V_7	12.17	3.38	0.70	115	41.13
V_8	20.44	1.005	0.80	50	20.54
V_1	17.56	0.85	0.85	70	14.93
V_3	10.45	1.98	0.65	95	20.69
V_9	7.504	4.82	0.95	300	36.17
V_{10}	18.86	0.965	0.85	35	18.20
V_4	35.10	9.00	1.45	85	315.90
V_5	2019	0.9215	0.37	—	1860.51
				TOTAL OUTPUT POWER	2349.62
				EFFICIENCY	86.78%

TABLE 3-IV. 20CM POWER PROCESSOR ELECTRICAL PERFORMANCE

FUNCTION	VOLTAGE	CURRENT	VOLTAGE RIPPLE P-P	CURRENT RIPPLE P-P	POWER
V_{IN}	394.8	6.863			2709.51
V_2	10.53	1.89	0.60 v	85 ma	19.90
V_7	12.14	3.36	0.60	125	10.79
V_8	19.95	0.98	1.30	60	19.55
V_1	17.56	0.85	1.00	65	14.93
V_3	10.47	1.985	0.70	100	20.78
V_9	7.53	4.82	0.80	320	36.28
V_{10}	18.80	0.965	0.80	70	18.14
V_4	35.10	9.02	1.40	90	316.60
V_5	2019	0.9193	0.39	—	1856.07
				TOTAL OUTPUT POWER	2313.04
				EFFICIENCY	85.37%

TABLE 3-V. 20CM POWER PROCESSOR ELECTRICAL PERFORMANCE

FUNCTION	VOLTAGE	CURRENT	VOLTAGE AT 20mA	POWER
V_{IN} •	201	7.431		1493.63
V_2	12.23	1.07		13.55
V_7	11.60	1.55		20.31
V_8	23.0	0.545	230	12.04
V_1	18.73	0.365		7.78
V_3	10.70	0.95		11.26
V_9	7.85	2.26		19.52
V_{10}	21.9	0.495	302	11.10
V_4	30.4	5.00	56.4	157.00
V_5	2022	0.487		982.20
			TOTAL OUTPUT POWER	1229.76
			EFFICIENCY	82.08%

TABLE 3-VI. 20CM POWER PROCESSOR ELECTRICAL PERFORMANCE

FUNCTION	VOLTAGE	CURRENT	VOLTAGE AT 20mA	POWER
V_{IN}	300	4.893		1467.90
V_2	12.43	1.09		13.55
V_7	12.31	1.65		20.31
V_8	22.5	0.535	227	12.41
V_1	20.0	0.389		7.78
V_3	11.26	1.00		11.26
V_9	8.20	2.38		19.52
V_{10}	22.2	0.50	297	11.10
V_4	30.4	5.00	56.4	152.00
V_5	2021	0.486		982.00
			TOTAL OUTPUT POWER	1229.76
			EFFICIENCY	83.78%

TABLE 3-VII. 20CM POWER PROCESSOR ELECTRICAL PERFORMANCE

FUNCTION	VOLTAGE	CURRENT	VOLTAGE AT 20mA	POWER
V_{IN}	395	3.790		1495.87
V_2	12.43	1.09		13.55
V_7	12.48	1.66		20.72
V_8	22.5	0.53	228	11.93
V_1	20.7	0.402		8.32
V_3	11.49	1.02		11.72
V_9	8.35	2.43		20.29
V_{10}	22.2	0.50	304	11.10
V_4	30.3	5.00		151.50
V_5	2021	0.487		984.23
			TOTAL OUTPUT POWER	1233.36
			EFFICIENCY	82.45%

More detailed measurements versus frequency and interference studies with the solar array power source must be performed to identify power processor specification requirement and the detail design of the power processor input filter and control electronics.

3.5 Design Analysis

An analysis was performed on the 20cm ion engine power processor breadboard to establish its characteristics such as:

- o Weight
- o Efficiency
- o Part count
- o Reliability

This analysis does not represent the actual values that would be obtained for a flight type design, but are given to indicate the present state of the art and areas where improvements can be obtained.

3.5.1 Weight Analysis

Table 3-VIII lists the different major component weight for each function in the 20cm power processor. The circuit redundancy is also included in weight analysis. Of the beam supply component weight of 3167 gms only 518 gms are in the control electronics.

When comparing the total weight of the beam supply and input filter, the input filter is about 1/2 of the total beam inverter weight. The weight density of the beam inverter-input filter is 4.95KG per 2KW or 2.5KG/KW (5.5 lb/KW) for the components.

The weight-loss factor for the beam supply and input filter is 4.95KG x .259KW = 1.28KG·KW.

TABLE 3- IX Summary of Breadboard Component Weights

ITEM	WEIGHT (gms)	PERCENTAGE OF TOTAL WEIGHT
Beam Supply	3167	35
Arc Supply	1414	16
Multiple Supply	2064	23
Command & Protection	545	6
Input Filter	1787	20
TOTAL	8977	100

Table 3-IX summarizes the weight of the 20cm power processor functions. It also shows the relative percentages of weight for each function. The beam supply (2KW) accounts for 35% of the total weight while the multiple output supply (200W) account for 23% of the total weight. All the multiple outputs contain a large number of low power components which account for the weight penalty.

The input filter also accounts for a large percentage of the total weight. Improving the filter capacitor will reduce this weight penalty.

3.5.2 Efficiency Analysis

Table 3-X lists the estimated losses in all the functions of the power processor. The major loss is in the beam power SCR's. Other major contributors are the power inductors and SCR suppression network to control the dv/dt. If reduction could be made in the SCR forward conduction loss and in the SCR reverse current flow, about 3% improvement in overall efficiency could be obtained.

The efficiency of the multiple output inverter is low due to the large number of low output voltages and their output rectification losses.

TABLE 3-XI EFFICIENCY ANALYSIS SUMMARY OF 20CM POWER PROCESSOR BREADBOARD

	POWER OUTPUT	LOSSES
Input Filter		10W
Beam Supply	2000W	249W
Arc Supply	300W	40W
Multiple Supply	159W	40W
Control Electronics		40W
TOTAL	2459W	379W
	Input Power	2838W
	Efficiency	87%

Table 3-XI summarizes the losses in all the functions of the power processor. All the control electronics are listed as one item including the SCR control logic circuits, all output regulators and the command & protection system.

TABLE 3-VIII. Weight Analysis of Power Processor Functions

TABLE 6-VII WEIGHT ANALYSIS OF POWER PROCESSOR FUNCTIONS

FUNCTION	ITEM	WEIGHT GMS
Beam Supply	1. Inverter Power Stage	
	Capacitor - Series	122
	Inductors - Series	1000
	Capacitors - Input	100
	SCR's	468
	Suppression Newtork	56
	2. SCR Firing Circuit	62
	3. Inverter Control Logic	106
	4. Output Power Circuits	
	Transformer - Output	662
	Output Rectifiers	46
	Output Capacitors	160
	Bias Driver	35
	5. Regulator Controls	
	Regulator Controls (Majority Voting)	292
	Miscellaneous Transformers	58
	Subtotal	3167
Input Filter	Inductor - First Stage	658
	Inductor - Second Stage	265
	Capacitors - First Stage	873
	Subtotal	1787

FUNCTION	ITEM	WEIGHT GMS
Arc Supply	1. Inverter Power Stage	
	Capacitor Series	50
	Inductors - Series	328
	Capacitor - Input	50
	SCR's	72
	Suppression Network	28
	2. SCR Firing Circuit	62
	3. Inverter Control Logic	106
	4. Output Power Circuits	
	Transformer - Output	212
	Output Rectifiers	12
	Output Capacitors	124
	Output Zener	20
	Bias	35
	5. Regulator Controls	
	Regulator Control (Majority Voting)	257
	Miscellaneous Transformers	58
	Subtotal	1414

FUNCTION	ITEM	WEIGHT GMS
Multiple Output Inverter	1. Inverter Power Stage	
	Capacitor - Series	50
	Inductors - Series	180
	Capacitor - Input	50
	SCR's	72
	Suppression Network	28
	2. SCR Firing Circuit	62
	3. Inverter Control Logic	106
	4. Output Power Circuits V1, V2, V3, V7, V8, V9, V10	590
	5. Output Regulators (Majority Voting)	700
	6. Auxiliary Output Power Circuit	84
	7. Auxiliary Output Regulator Sync	142
	Subtotal	2064
Command & Protection System	Command & Protection	350
	Start Circuit	70
	Storage Capacitor	125
	Subtotal	545

TABLE 3-X. Efficiency Analysis of 20CM Power Processor Breadboard

FUNCTION	ITEM	LOSS WATTS	PERCENT OF FUNCTION
Beam Supply	SCR	130	5.8
	Transformer	27	1.20
	Inductors	33	1.44
	Capacitors - Series	12	.53
	Output Diodes	12	.53
	Input Filter	11	.45
	Suppression	24	1.07
	Total Loss	249	
	Output Power Input Power	2000 2249	
	Efficiency = $\frac{2000}{2249} \times 100$		89
Arc Supply	SCR	6	1.76
	Transformer	3	.88
	Inductors	14	4.12
	Capacitors - Series	1	.29
	Output Diodes	10	2.94
	Suppression	4	1.18
	Output Capacitor	2	.59
	Total Loss	40	
	Output Power Input Power	300 340	
	Efficiency = $\frac{300}{340} \times 100$		88.3
Input Filter		10	

FUNCTION	OUTPUT SUPPLY	OUTPUT VOLTAGE	OUTPUT POWER	OUTPUT DIODE	POWER LOSS TRANSFORMER	OUTPUT CAPACITOR
Multiple Output Inverter	V1	19V	16	0.7	0.7	0.2
	V2	10V	20	1.6	0.9	0.4
	V3	17V	17	0.8	0.6	0.2
	V7	12V	45.6	3.0	1.5	0.8
	V8	22V	11	0.4	0.6	0.2
	V9	12V	36	2.4	1.1	0.6
	V10	22V	13.2	0.5	0.6	0.2
	V_{Aux}	15V	40	1.1	1.1	0.7
Total			198.8	10.5	7.5	3.3
Total Output Circuitry Loss						21.3W
Shorting Transistor Losses						3.6W
Inverter						
Capacitor - Series						1W
SCR						4W
Inductors						8W
Suppression						2W
Total Losses						39.9W
Output Power						198.8W
Input Power						238.7
Efficiency = $\frac{198.8}{238.7} \times 100$						83.0%

TABLE 3-XII. Part Count Analysis of Power Processor

FUNCTION	ITEM	NO.
Input Filter	Inductors	2
	Capacitors	2
	Resistors	2
	Subtotal	6
Beam Supply	1. Inverter Power Stage	
	Capacitor - Series	2
	Inductor - Series	5
	Capacitors - Input	2
	SCR's	4
	Suppression Network	32
	2. SCR Firing Circuit	60
	3. Inverter Control Logic	121
	4. Output Power Circuits	
	Transformer - Output	1
	Output Rectifiers	2
	Output Capacitors	2
	Bias Driver	18
	5. Regulator Controls	
	Regulator Controls (47x3)	141
	Majority Voting Gate	17
	Misc. Transformers	3
	Subtotal	410

FUNCTION	ITEM	NO.
Arc Supply	1. Inverter Power Stage	
	Capacitor - Series	2
	Inductors - Series	5
	Capacitor - Input	1
	SCR's	4
	Suppression Network	18
	2. SCR Firing Circuit	60
	3. Inverter Control Logic	121
	4. Output Power Circuits	
	Transformer - Output	1
	Output Rectifiers	1
	Output Capacitors	2
	Output Zener	1
	Bias Driver	18
	5. Regulator Controls	
	Regulator Control (60x3)	180
	Majority Voting Gate	17
	Misc. Transformers	3
	Subtotal	434

FUNCTION	ITEM	NO.
Multiple Output Inverter	1. Inverter Power Stage	
	Capacitor - Series	2
	Inductors - Series	5
	Capacitor - Input	1
	SCR's	4
	Suppression Network	18
	2. SCR Firing Network	60
	3. Inverter Control Logic	121
	4. Output Power Circuits V1, V2, V3, V7, V8, V9, V10	60
	5. Output Regulators (318x3)	954
	Majority Gates	119
	6. Auxiliary Output Power Circuit	17
	7. Auxiliary Output Regulator and Sync (62x3)	186
	Majority Gates	17
	Subtotal	1581
Command & Protection System	Control Cards	183
	Start Circuitry	47
	Subtotal	230

3.5.3 Part Count Analysis

TABLE XII lists the detail analysis of the part count for the basic function of the 20cm power processor breadboard. Redundancy is noted in the different areas and increases the total part count.

TABLE XIII. Part Count Summary of Power Processor

ITEM	TOTAL NO. OF PARTS	IN-LINE FAILURE PARTS
Input Filter	6	6
Beam Supply	410	252
Arc Supply	434	237
Multiple Supply	1581	305
Command & Protection	230	230
TOTAL	2661	1030

TABLE XIII summarizes the part count for the different function. The number of in-line components that can contribute to failure and have no redundancy are also tabulated.

The total part count is 2661 components but only 1030 can contribute to the power processor failure. The command & protection system does not have any redundancy and its in-line failure components could be greatly reduced.

3.5.4 Reliability Analysis

Figure 3-33 shows the redundancy block diagram for the Engineering Model breadboard design that was evolved after performing preliminary electrical circuit design discussed in Appendix E, reliability assessment. Each functional block has a preferred redundancy code marked in it such as:

N - Nonredundant
M - Majority Voting
Q - Quad Components

All power circuits are marked (N) - nonredundant - in order to maintain high efficiency without any weight penalty. All output power supply regulators use majority voting type of redundancy. The command and protection system are nonredundant because of the design changes that were necessary during ion engine power processor integration testing. The redundant configuration design can easily interface with the total power system. The auxiliary power supply regulator will also be in the majority voting configuration.

The failure rate data used for the reliability analysis in Appendix E was very conservative due to the lack of reliability and life data necessary to substantiate the new high power, high voltage components failure rate.

Table 3-XIV shows the failure rate for each power processor function using the failure rate in Table E-III. The command and protection system has a failure rate of 2119. This number can be reduced by the use of redundancy in the regulator and some circuit modifications both to eliminate parts with high failures and to further reduce part count.

The reliability for the power processor using an experience factor 0.5 is 0.925 using the conservative failure rates shown in Table E-III.

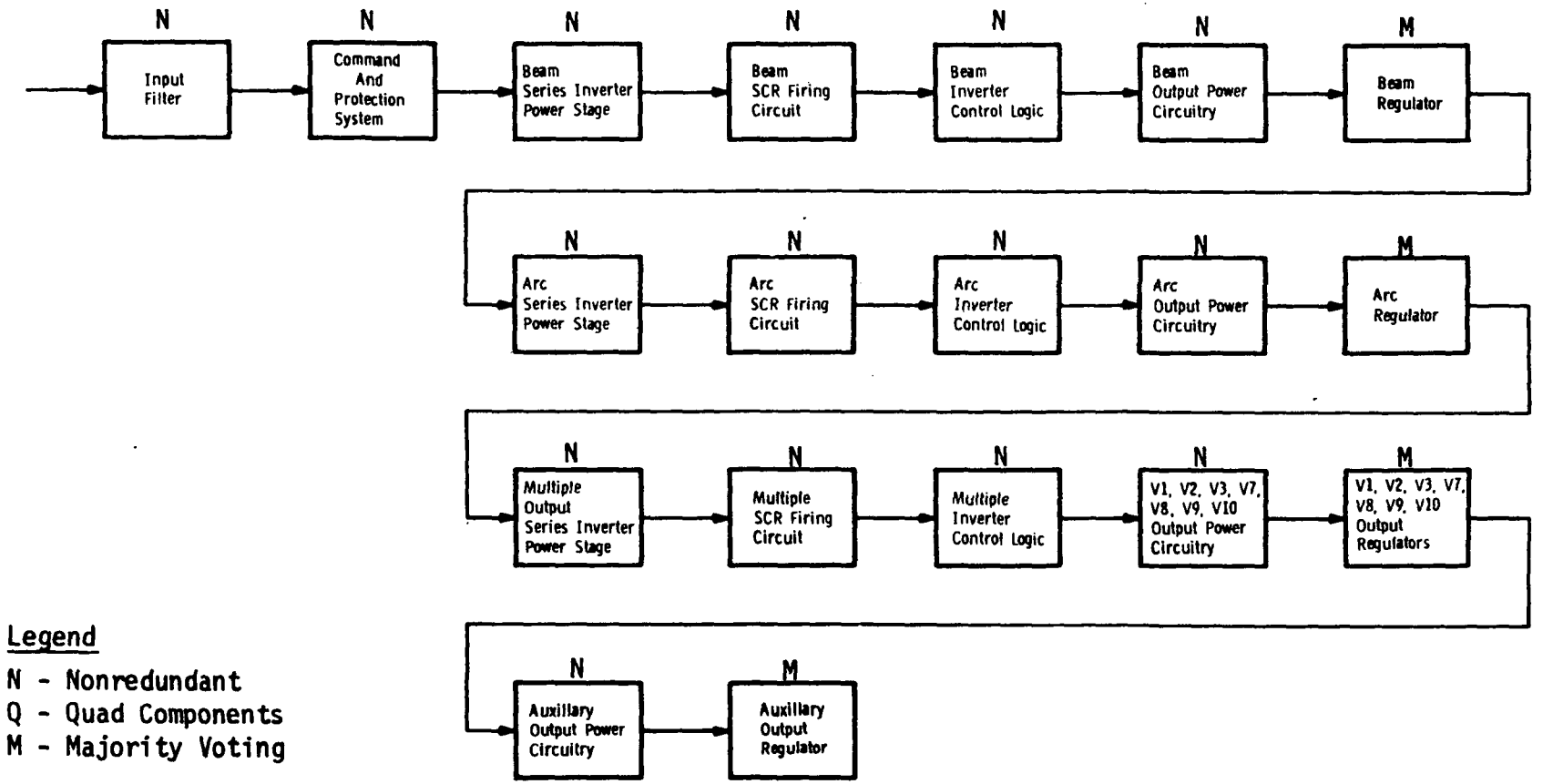


FIGURE 3-33

POWER PROCESSOR REDUNDANCY CONFIGURATION

TABLE 3-XIV 20CM THRUSTER POWER PROCESSOR BREADBOARD MODEL RELIABILITY PREDICTION

POWER PROCESSOR FUNCTION	FAILURE RATE USING TABLE 12-III	
Input Filter	180.0	
Command & Protection System	2119.4	
Beam Inverter Power Stage	1658.1	
Beam Inverter Firing Circuit	322.8	
Beam Inverter Control Logic	1011.8	
Beam Output Power Stage	869.2	
Beam Regulator (majority Voting)	61.8	
Sub-total of Beam Supply		3921
Arc Inverter Power Stage	996.5	
Arc Inverter Firing Circuit	322.8	
Arc Inverter Control Logic	1011.8	
Arc Output Power Stage	754.8	
Arc Regulator (Majority Voting)	80.3	
Sub-total of Arc Supply		3163
Multiple Output Inverter Power Supply	996.5	
Multiple Inverter Firing Circuit	322.8	
Multiple Output Inverter Control Logic	1011.8	
Multiple Output Power Supply Power Stage	3142.2	
Multiple Output Power Supply Regulators (Majority Voting)	390.3	
Auxiliary Power Supply Power Stage	714.0	
Auxiliary Power Supply Regulator (Majority Voting)	24.6	
Sub-total of Multiple Output Supply		6599
Total Failure Rate	15991.2	
Reliability with Experience Factor of 0.5	.925	

The multiple output inverter has over 40% of the total power processor failure rate while the beam supply has less than 25% of the total failure rate. This higher rate in the multiple output inverter is caused by the large number of control functions required, and the large number of parallel output filter capacitors necessary to filter the AC currents, and the output fault protection zener diodes. The command and protection system only account for 13% of the total failure rate.

4.0 20CM ION ENGINE/POWER PROCESSOR INTEGRATION

The 20cm hollow cathode ion engine was installed in the test facilities and operated with laboratory power supplies. Then the power processor was integrated with the ion engine at the test facility. After minor problem areas were identified and resolved, the ion engine was operated with the power processor for over 100 hours with at least 25 cold engine startups. The following functional operation was demonstrated:

1. Startup of Neutralizer Keeper
2. Neutralizer Keeper Voltage Regulation
3. Startup of Cathode Keeper
4. Startup of Anode
5. Anode Voltage - Cathode Vaporizer Control Loop
6. Application of High Voltage to Accelerator and Screen
7. Beam Current Regulation from 0.25 to 1.0A
8. Recovery from Internal Engine Shorts
9. Shutdown of Ion Engine

4.1 Ion Engine Test Facility

The ion engine test facility includes a vacuum tank in which to operate the ion engine, power supplies, engine instrumentation and the associate controls for the facility.

Thruster performance tests were performed in the vertical ion engine test facility shown in Figure 4-1. This chamber (5 ft. diam. x 10 ft. long) has been specifically instrumented for performing life and performance testing on complete ion engine propulsion systems at power levels ranging from 5 to 5,000 watts. The engine is mounted at the top of the chamber and exhausted vertically downward. Provisions can be made to use either a frozen mercury target or a titanium collector and to operate the collector and shrouds at ground potential or floating at the beam exhaust potential.

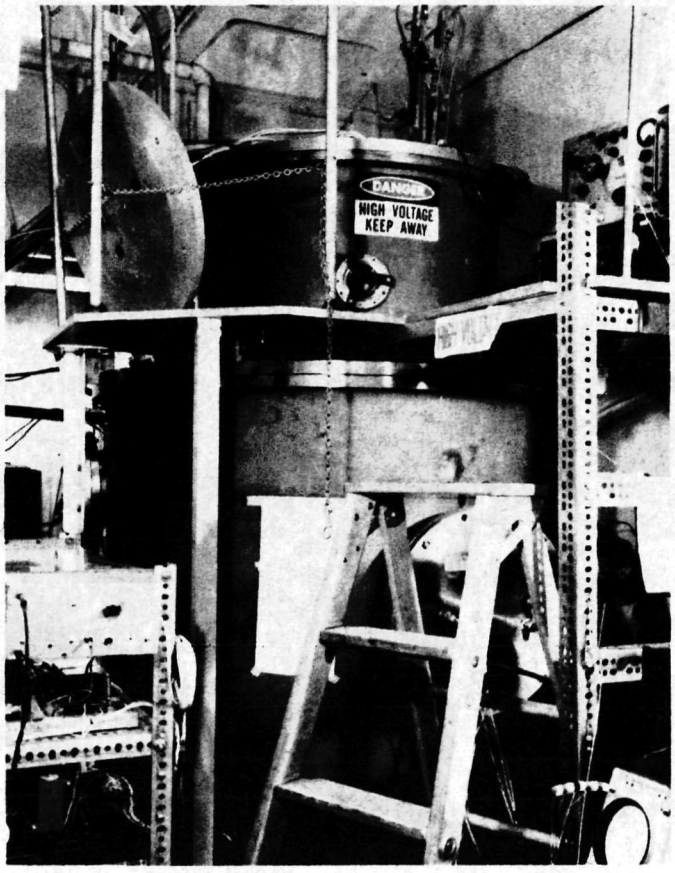


Figure 4-1 Ion Engine Test Tank

Laboratory research and testing of ion engines require that the ion beam produced terminate on a collector. The impinging ions sputter away collector material and release occluded and dissolved gases. A high purity material of low sputtering yield is therefore desired, both from the standpoint of collector durability and minimizing foreign material returning to the thruster. Copper and aluminum are the conventional materials for ion beam collectors. The frozen mercury collector concept, originally developed at TRW Systems, is gaining in popularity for use during long-term mercury bombardment engine life tests.

Titanium is a novel alternative. It may be obtained in high purity form, and it has a sputtering yield substantially lower than copper and slightly lower than aluminum: approximately 2 atoms/ion for 3 Kev H_g^+. Its principal advantage, however, is that the atoms sputtered from the collector and onto other vacuum chamber surfaces actively absorb (or getter) virtually every species of residual chamber gas. Titanium gettering of CO and H_2 is particularly attractive, since these gases are not cryopumped at LN_2 temperature. The additional pumping action afforded by sputtered titanium reduces chamber pressure during thruster operation which is a very desirable condition in many thruster tests and experiments.

A vacuum-jacketed line brings LN_2 from a bulk storage tank. A separate pipe provides water-free GN_2 from the same tank for purging the 4 x 10 tank and its associated cold LN_2 lines.

The LN_2 may be routed through the tubing of all interior shrouds. In order to maintain adequate vacuum conditions, it is necessary to control the temperature of the shroud within a few degrees so that the material, once trapped, will not be desorbed during positive temperature excursions. For this purpose thermocouple sensing temperature controllers are used to operate the solenoid valves. The particular instrument chosen uses a copper-constantan thermocouple and is of the time-proportioning type with automatic offset control.

Best control of tank pressure is attained when the entire shroud is at the temperature of boiling liquid nitrogen; that is, it is desirable for the discharge from the outlet tube to be always on the verge of spitting liquid. This condition has been achieved, despite changing heat loads and moderate changes in quality of the incoming coolant, by locating the thermocouples on the outlet tubes near their respective shrouds.

Figure 4-2 shows the ion engine test facility console. It includes seven different functional areas.

(1) Top, panel meters for all currents and voltages to the ion engine.

(2) Center section-left side panel, ac power control, vacuum tank controls, facility monitoring and emergency shutdown if failure occurs in the facility equipment or input power.

(3) Center section, center panel, low voltage supply operating at ground potential and low voltage instrumentation.

(4) Center section, right side panel, all power supplies floating at screen or beam potential and high voltage instrumentation. This equipment is shielded by a plexiglas front panel for personnel safety.

(5) Bottom section, left side, accelerator power supply.

(6) Bottom section, extreme right side, beam power supply.

(7) Extreme left side, strip recorder to monitor engine functions.

Figure 4-3 is the interlock logic diagram for the test facility.

Figure 4-4 shows the thermocouples logic block diagram in the test facility for determining performance and for obtaining closed loop operation of the engine control loops through the respective laboratory power supply.

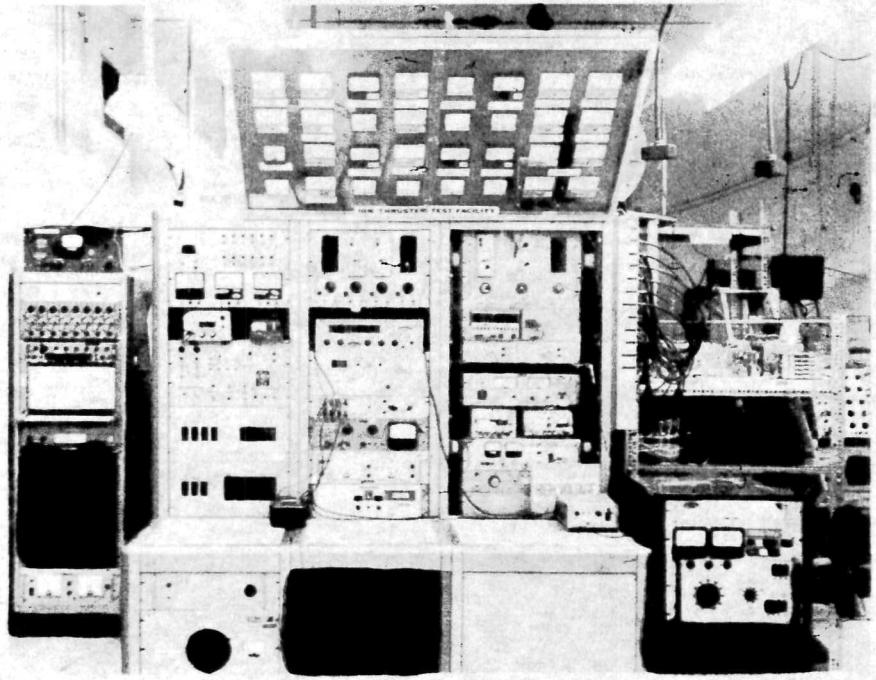


Figure 4-2 Ion Engine Test Facility Console

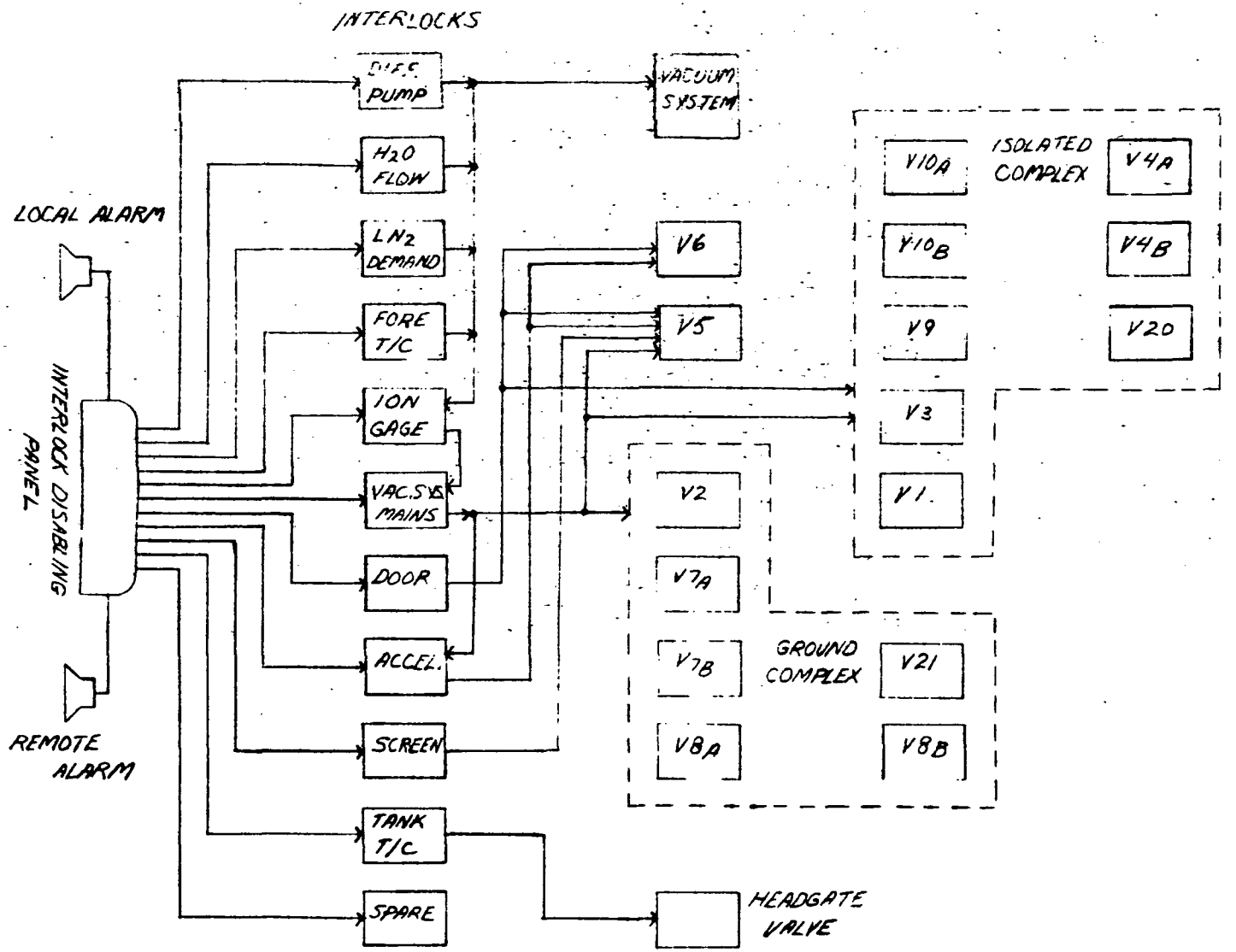


Figure 4-3. Interlock Logic Flow

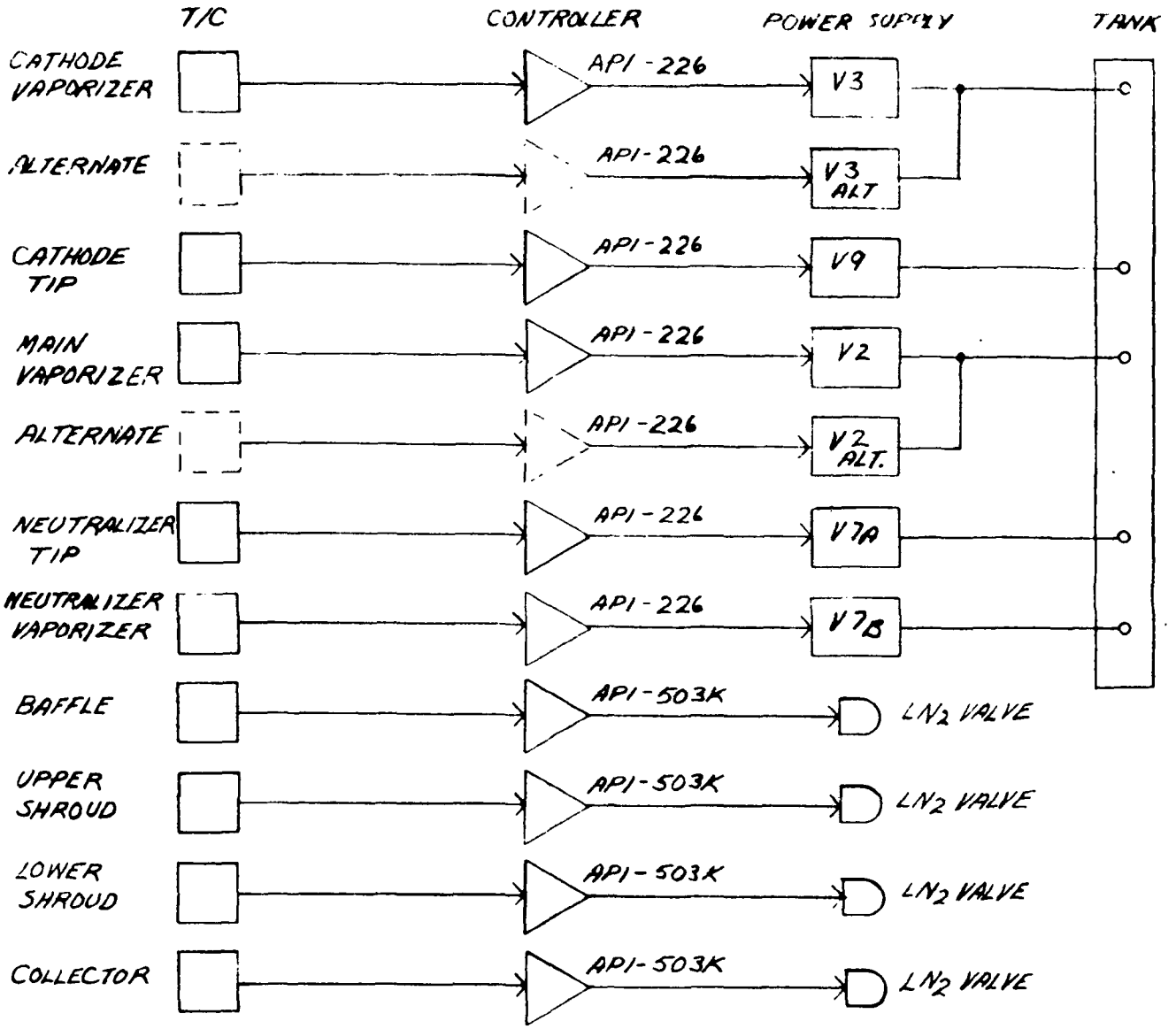


Figure 4-4. Thermocouple Control Logic Flow

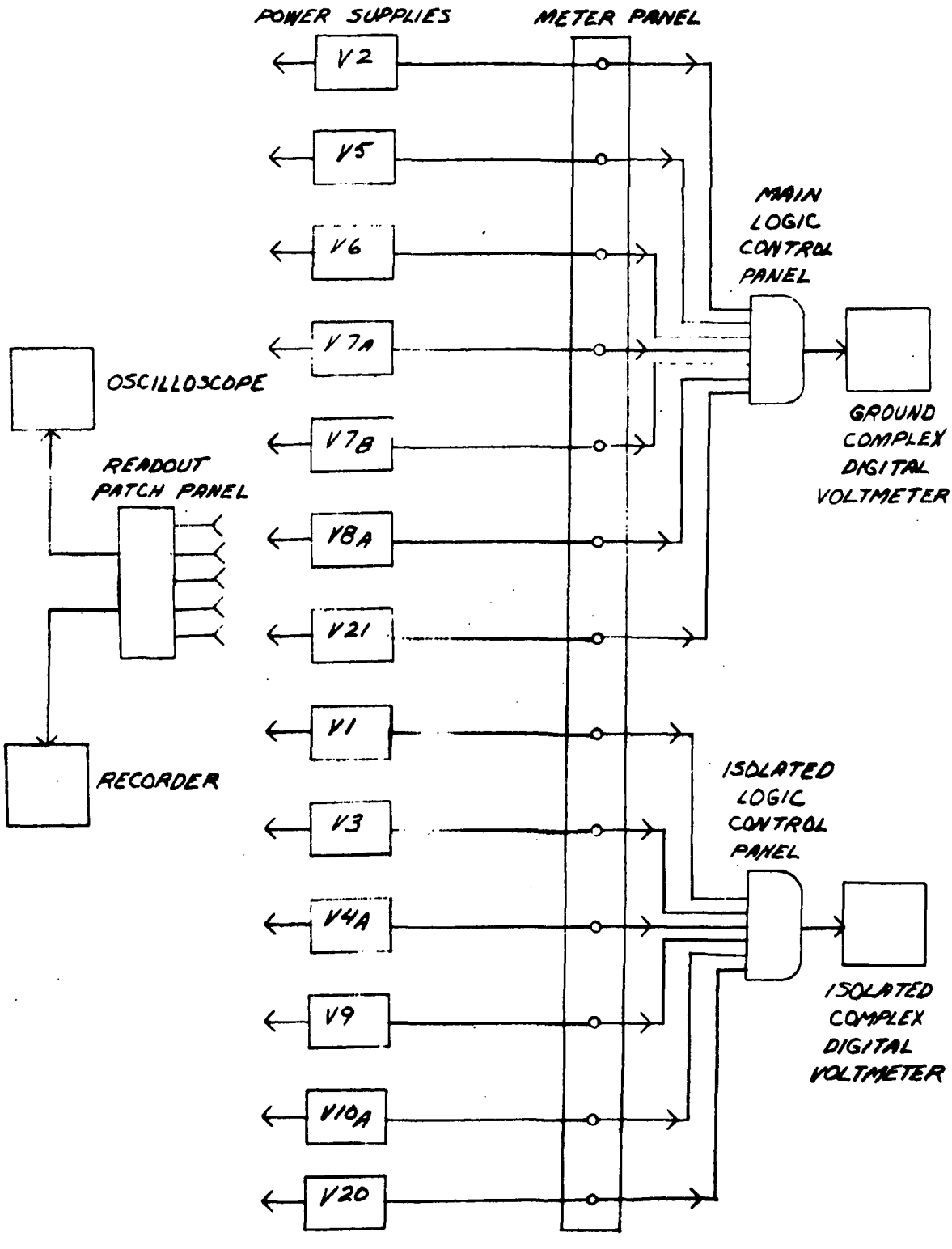


Figure 4-5. Readout Logic Flow

Figure 4-5 is the ion engine instrumentation block diagram for the test facility.

Figure 4-6 is the ion engine wiring diagram for the test facility.

Figure 4-7 is the wiring diagram of the laboratory power supply, the current measurements for the DVM, and the current test loops to monitor noise on the respective leads to the ion engine.

Figure 4-8 is the test facility junction box used to transfer the ion engine power from the laboratory power supplies to the power processor breadboard.

Unique features of this facility of interest to the program are:

- Precision current, voltage, and temperature measurements can be made at either ground or floating high voltage. These measurements are made with high accuracy digital voltmeters that are connected to each of the key thruster outputs of interest through a master logic panel. There are two digital voltmeters; one capable of measurement at input voltages from 0 to 4KV relative to ground potential, and the second meter capable of half percent accuracy measurement at input voltages ranging from 0 to 500V relative to the thruster floating potential. High precision current shunts are available for accurate current readings.

- Continuous monitoring for voltage and current to 1% accuracy is accomplished by a master meter panel.

- Monitoring of transient thruster outputs is possible through connection of oscilloscope and high speed recorders to the thruster output.

- Current and/or voltage regulated supplies are available.

- The system is instrumented for automatic operation. In the event of a failure, a local alarm is initiated and a special logic network relays a signal to central plant security where 24-hour surveillance is maintained for all of TRW. Failure modes may be initiated by the following faults:

    1. Loss of Power
    2. High Vacuum Chamber Pressure
    3. Overcurrent and Beam Power Supply
    4. Excessive Demand on Liquid Nitrogen Reservoir
    5. High Diffusion Pump Temperature
    6. Open Relay Rack Doors
    7. Accelerator Overcurrent.

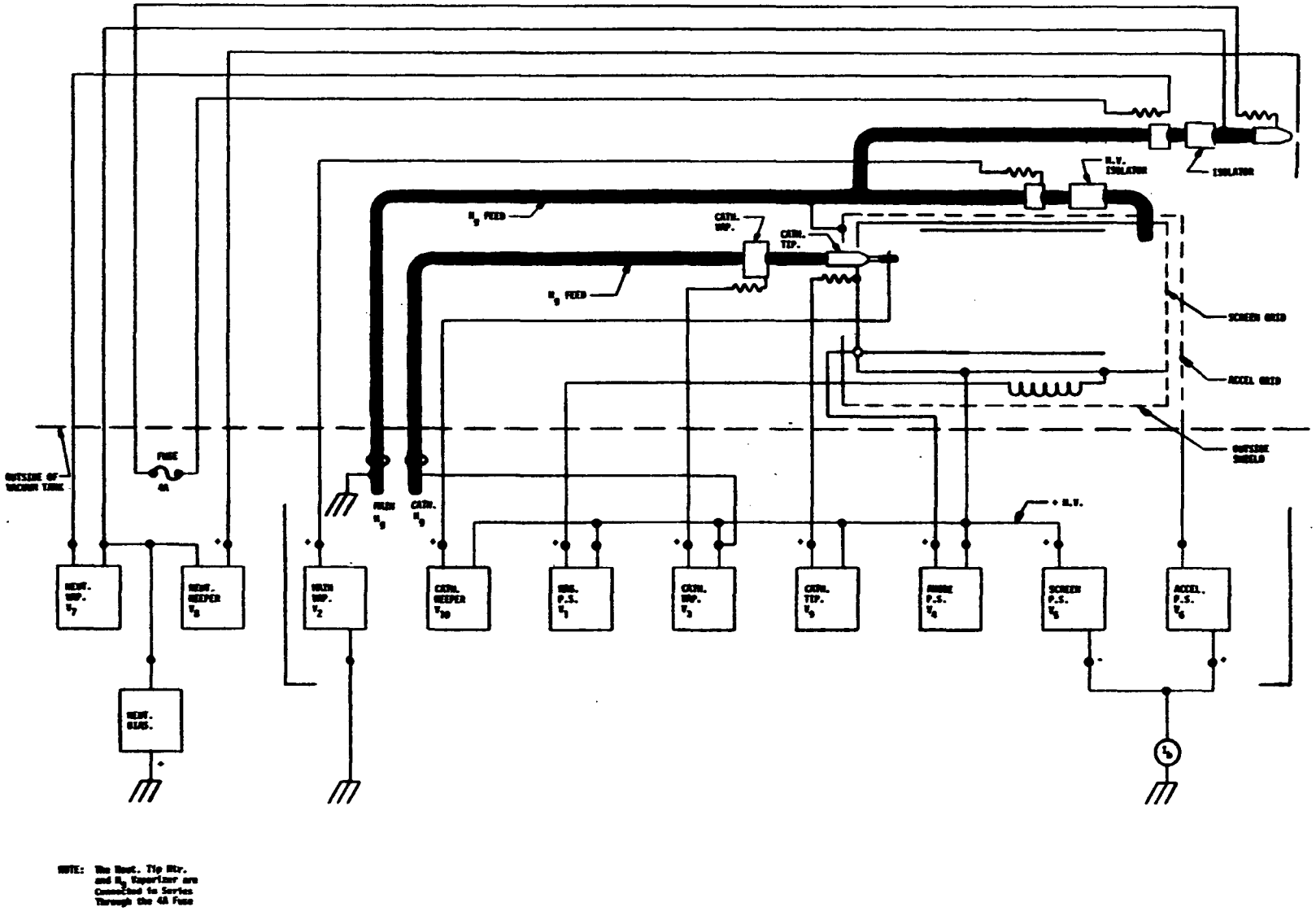


Figure 4-6. Ion Engine Wiring Diagram

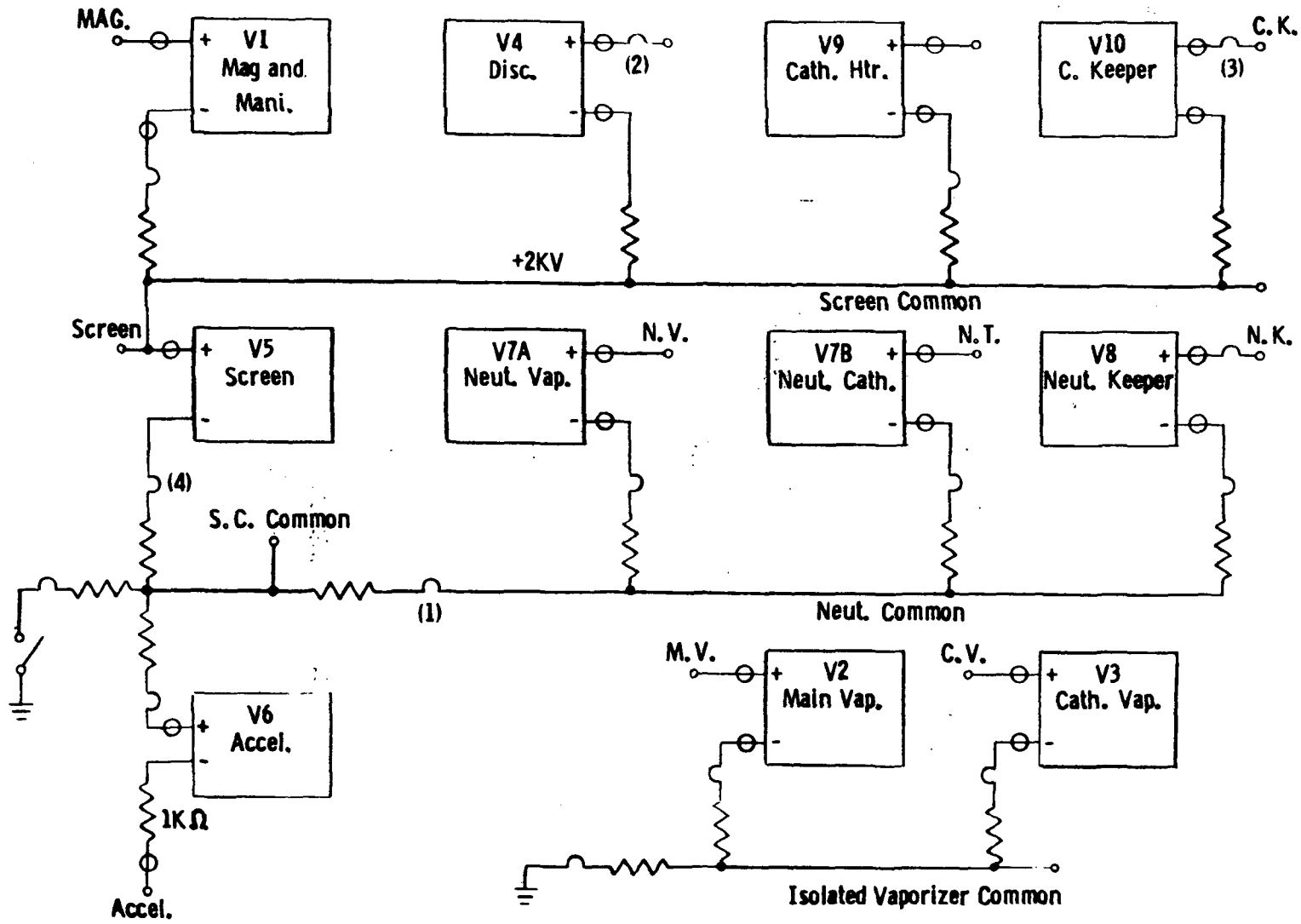


FIGURE 4-7 LABORATORY POWER SUPPLIES AND INSTRUMENTATION BLOCK DIAGRAM

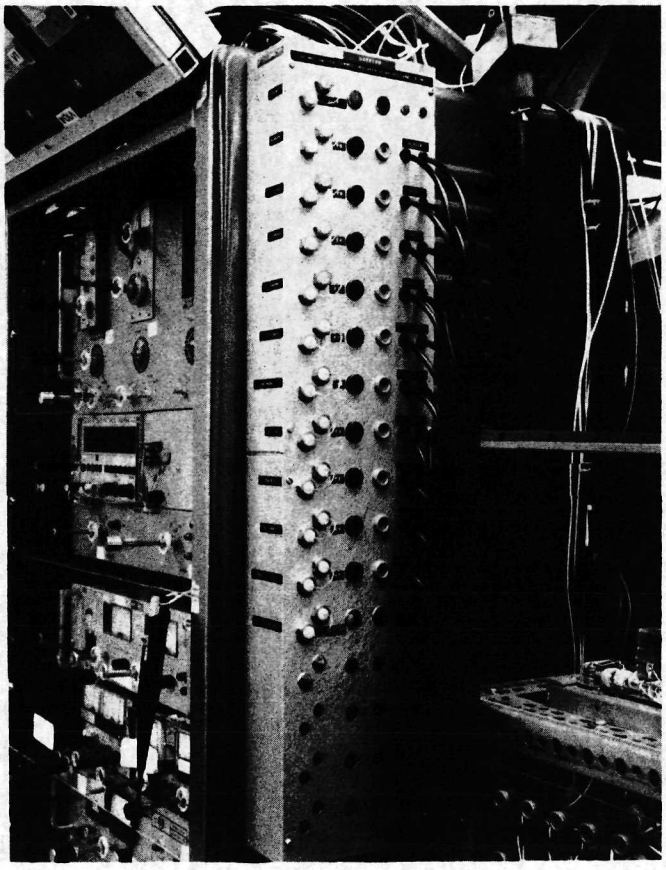


Figure 4-8. Test Facility Junction Box

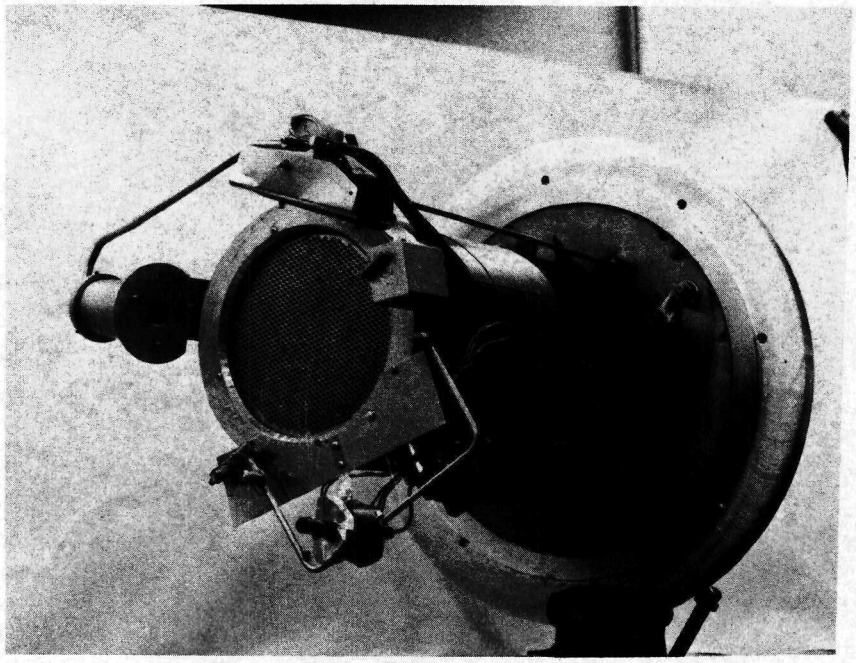


Figure 4-9. 20 CM Hollow Cathode Ion Engine

4.2 Power Processor Test Fixture

In order to facilitate the testing of the power processor, a special test fixture, shown in Figure 4-10, was fabricated to provide safety for the test personnel, to position the power processor in the engine test facility and to monitor the performance of the power processor.

The test fixture is covered by plexiglas on all sides and top to provide high voltage isolation and prevent material from falling on the equipment.

The power processor is located in the top section of the test fixture. Access holes provide capability to switch the individual output supplies off manually and to adjust the different engine output current and voltage references. Output power connectors are located on the left side.

The bottom section of the test fixture includes all the output and input power instrumentation. The DVM on the left side monitors all potentials floating at the screen supply output and the DVM on the right monitors all potentials referenced to ground.

Power processor instrumentation schematics are shown in Figures 4-11 and 4-12. Figure 4-11 shows instrumentation for all outputs floating at the screen potential. Figure 4-12 shows instrumentation for all outputs referenced to ground. Zener diodes are placed across the output current measuring shunts to limit high voltage transients appearing across the shunts.

4.3 Ion Engine Integration Test Results

The JPL 20cm hollow cathode ion engine was operated initially with the test facility power supplies. During engine arcing, some of the power supplies floating at beam potential failed. The output zener diode clamping system used in the power processor design and discussed in Appendix B, Power Processor Block Diagram, was incorporated across all the laboratory power supplies in the engine test facility.

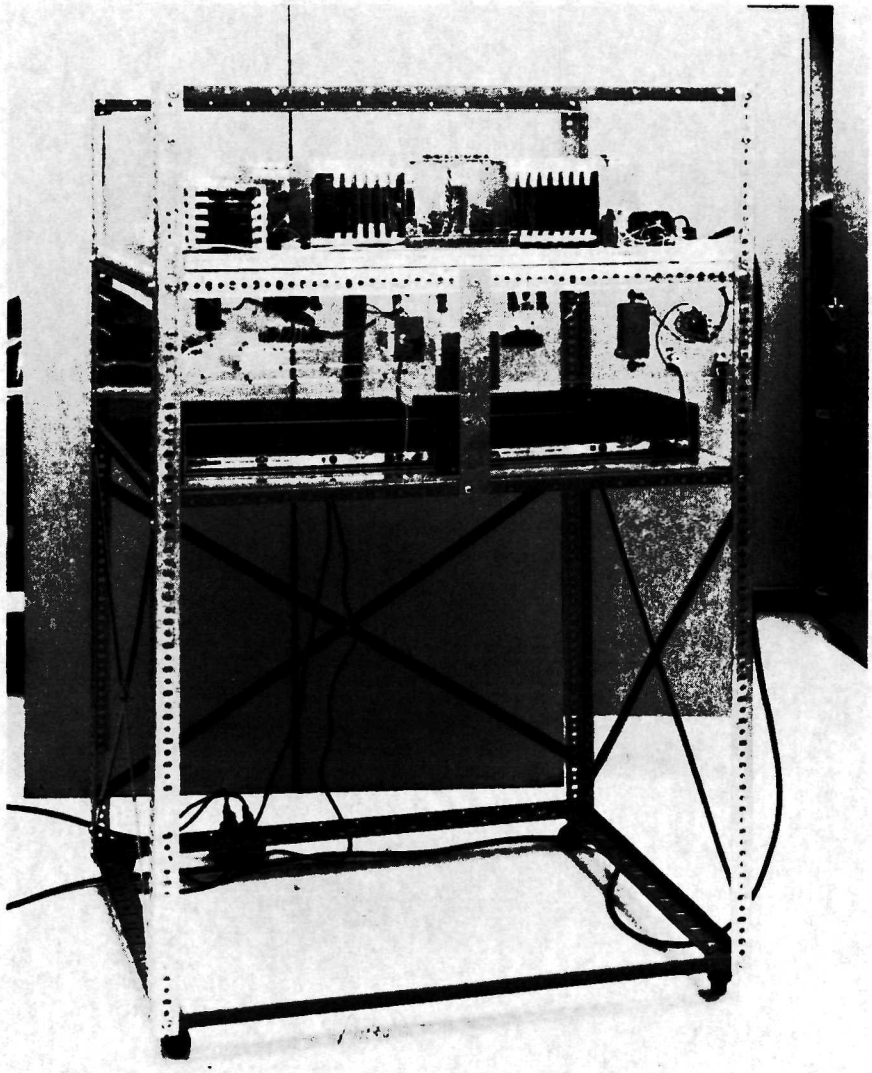


Figure 4-10. Power Processor Test Fixture

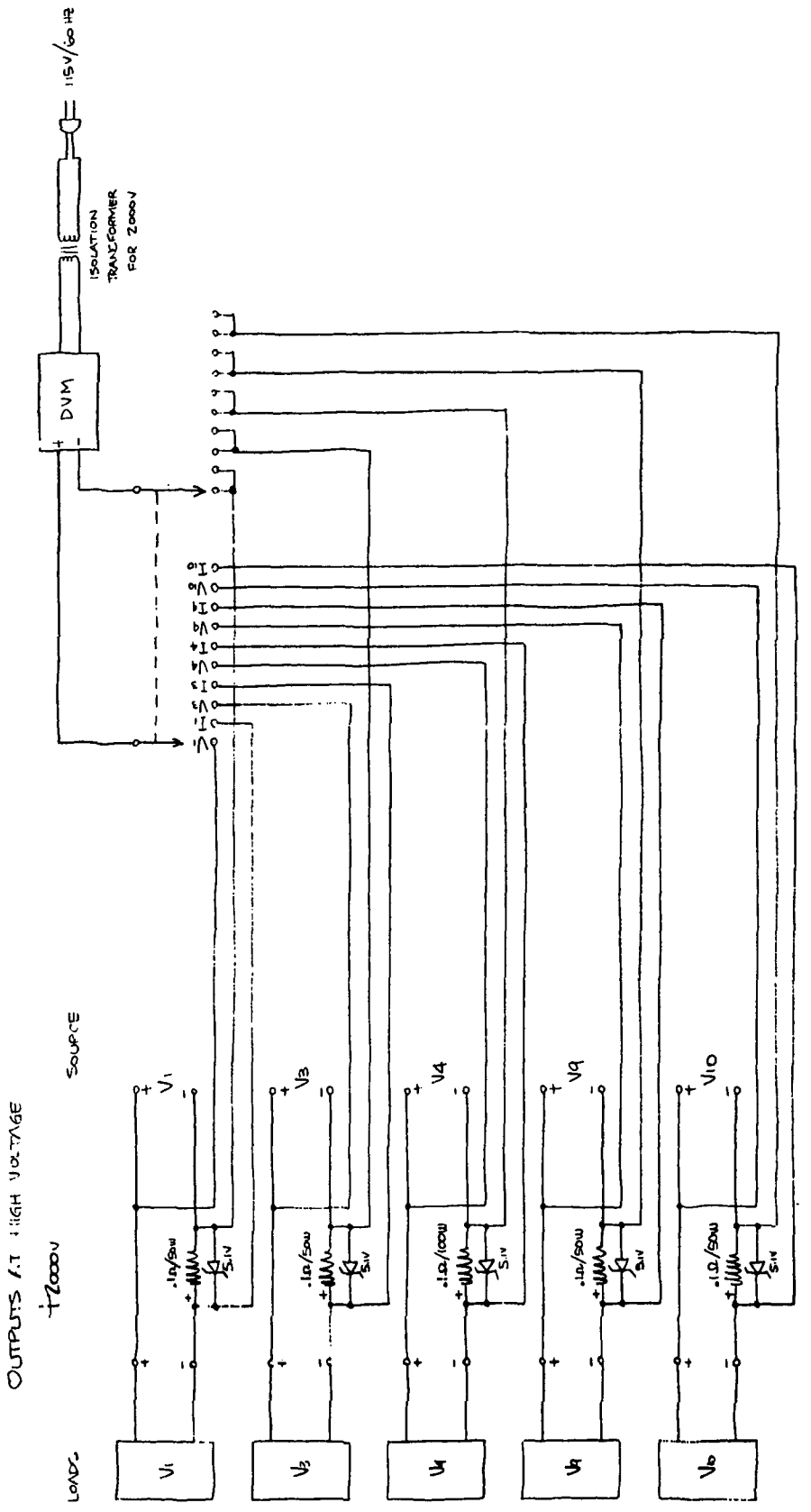


Figure 4-11. Power Processor Instrumentation Schematic High Voltage Reference

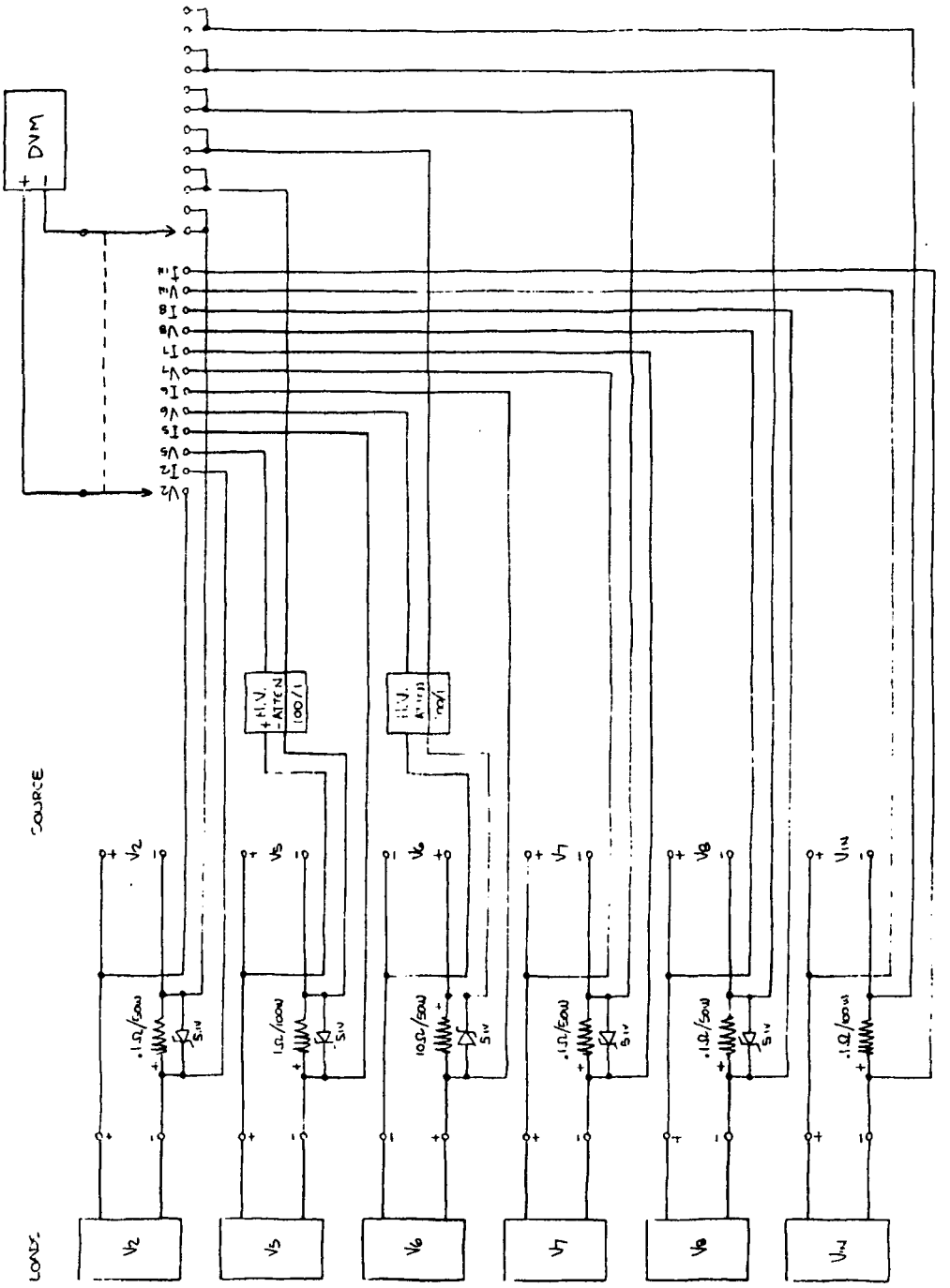


Figure 4-12. Power Processor Instrumentation Schematic Ground Voltage Reference

During the overall testing with the ion engine, the following engine malfunctions were noted:

(1) Open neutralizer vaporizer heater - replaced heater.

(2) High leakage resistance across cathode vaporizer isolator (isolator removed). Thermal runaway of controller.

(3) High leakage resistance across main vaporizer isolator (isolator cleaned three times). Thermal runaway of beam current.

(4) Holes in cathode baffle plate and mercury vapor in the back of the engine caused hard starting of engine and arcing in the vacuum tank (replaced plate).

(5) Open cathode vaporizer (replaced vaporizer).

The engine received from JPL is a labroatory breadboard type engine with many hours of operation and therefore its reliability is low. In addition, it is not thermally designed for space flight and therefore requires about 1 hour operation before stable ion engine performance is obtained, during which time many overload or internal arcs occur.

During integration testing with the ion engine, the following problem areas were identified and resolved in the power processor and instrumentation:

- During the startup mode of the ion engine the output voltage for the beam and accelerator overshot to approximately +3KV and -1.5KV for the respective outputs when an arc occurred. This excessive voltage caused transformer breakdown in the un-potted high voltage magnetics.

To correct this condition, all failed high voltage magnetics were reviewed and magnetics with insufficient insulation were redesigned with increased dielectric. All high voltage magnetics were potted.

An RC lead network was added to the beam regulator to improve the starting transient response when operating into a no load condition.

A 100 picofarad capacitor was added to the beam regulator control logic input to bypass noise coupling due to the high ac current flowing in the power lines. This prevents false turn-on of the inverter.

- During shorting or arcing of the ion engine, low voltage magnetics and control electronics failed. During these transient conditions, high dc voltage would appear in the negative return line on the screen supply across the current monitoring shunts used for monitoring power processor performance with the ion engine. The high voltage would cause the output control electronics ground return line to be elevated above input power and command power grounds. This causes failure due to insufficient voltage insulation between the different isolated control power supplies.

- To prevent high transient voltages from appearing across the shunts, power zeners were added across the shunts to limit voltage buildup. Power resistors were added to the screen and accelerator output lines to the engine to limit the peak value of output capacitor current discharge during overloads to 200 amperes.

  The combination of the last two items limited the peak voltage transient between grounds to 200V, mainly due to L di/dt effect on the cabling. In addition, increased insulation was placed on the different low level magnetics to provide ground isolation.

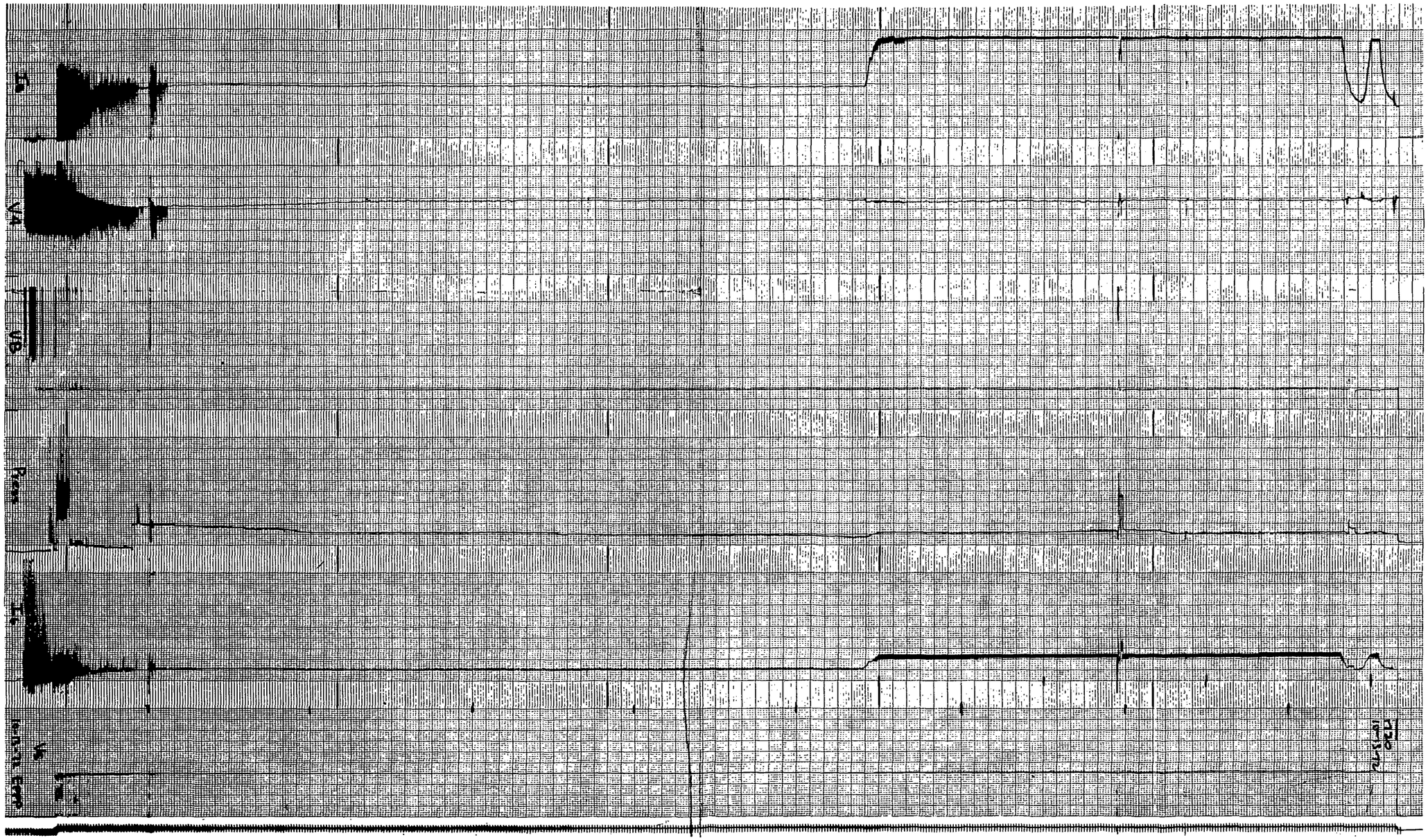


Figure 4-13. Ion Engine Performance Data

- The regulator transistor on V9 and V2 output had failed. Due to electronic failures that occurred previously, the output regulators were not synchronized and would turn off when high collector current was present. This causes high voltage transients due to leakage inductance of the output transformer to appear across the collector to emitter junction. This high voltage transient would cause the transistor to fail due to secondary breakdown.

  After the synchronizing circuit was repaired and power zener diodes were added across the collector-emitter of the transistor, high transient voltages were eliminated and no further failures occurred.

Figure 4-13 illustrates a strip recording of the ion engine. It shows the following engine functions:

- Beam Current (1 amp full scale)
- Discharge Voltage (50 volts full scale)
- Neutralizer Keeper Voltage (50 volts full scale)
- Tank Pressure
- Accelerator Current (50mA full scale)
- Beam Voltage (5KV full scale)

The trace shows the initial startup of the neutralizer. Once the neutralizer becomes active, the discharge V4, the cathode vaporizer V3, and main vaporizer V2 are turned on. The system is allowed to operate for a period of time until the discharge current has stabilized. The high voltage V5, along with V6, is then turned on. The engine continues to arc over until the V4 discharge voltage becomes stable and starts regulating and the beam current is regulated at the commanded valve. After approximately three hours of operation at 0.5 amperes beam current, the beam current reference is increased to 1.0 ampere level. After about 1-1/2 hours of operation at 1 ampere, arcs occurred in the engine and the automatic fault

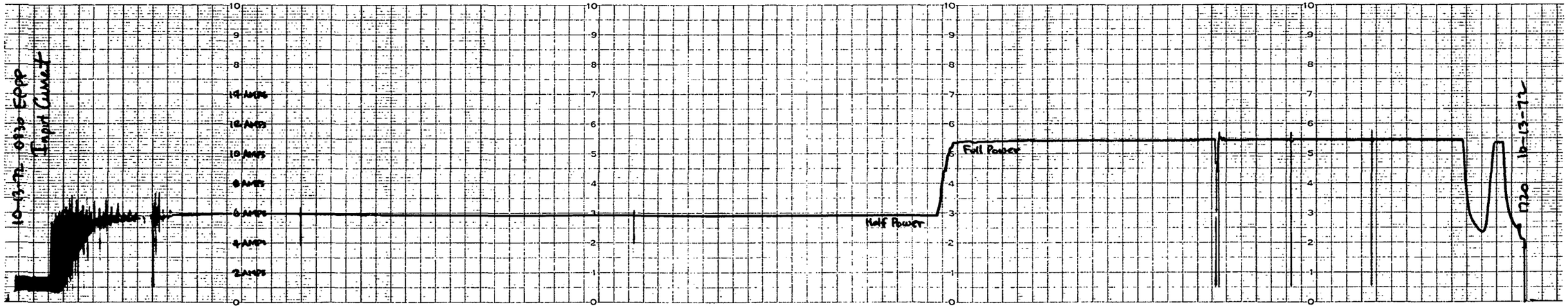


Figure 4-14. Power Processor Input Current for Same Run Shown in Figure 4-13

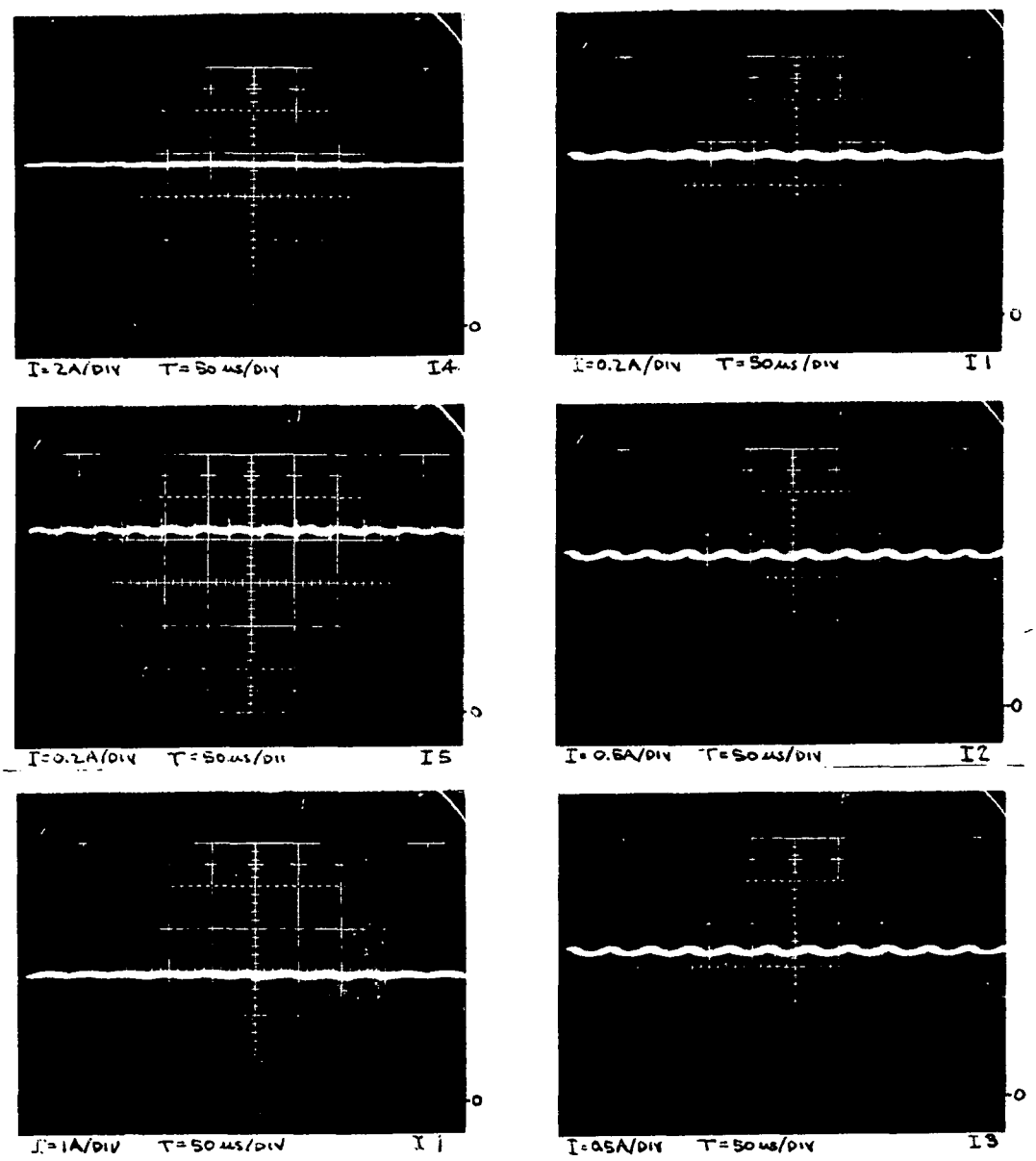
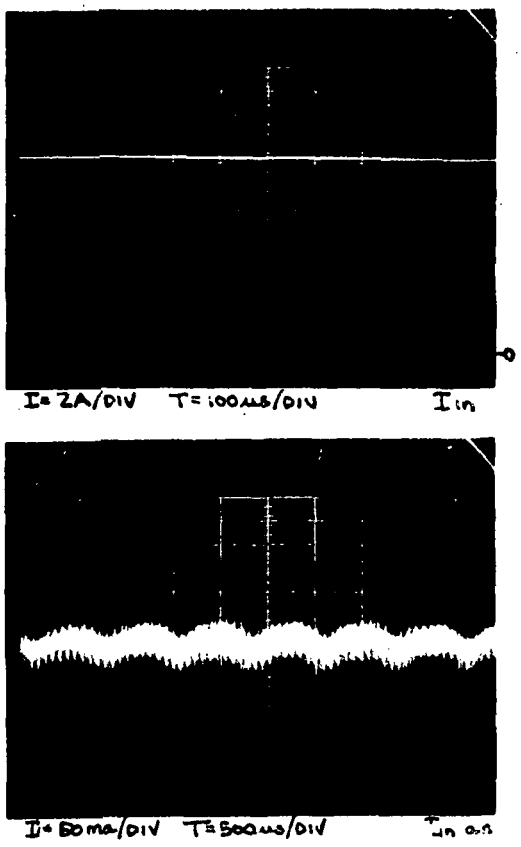


Figure 4-15. Ripple on Power Processor Input and Output Lines with Resistive Load

EPPP Breadboard

Input Currents into loadbank



Output Currents into Loadbank

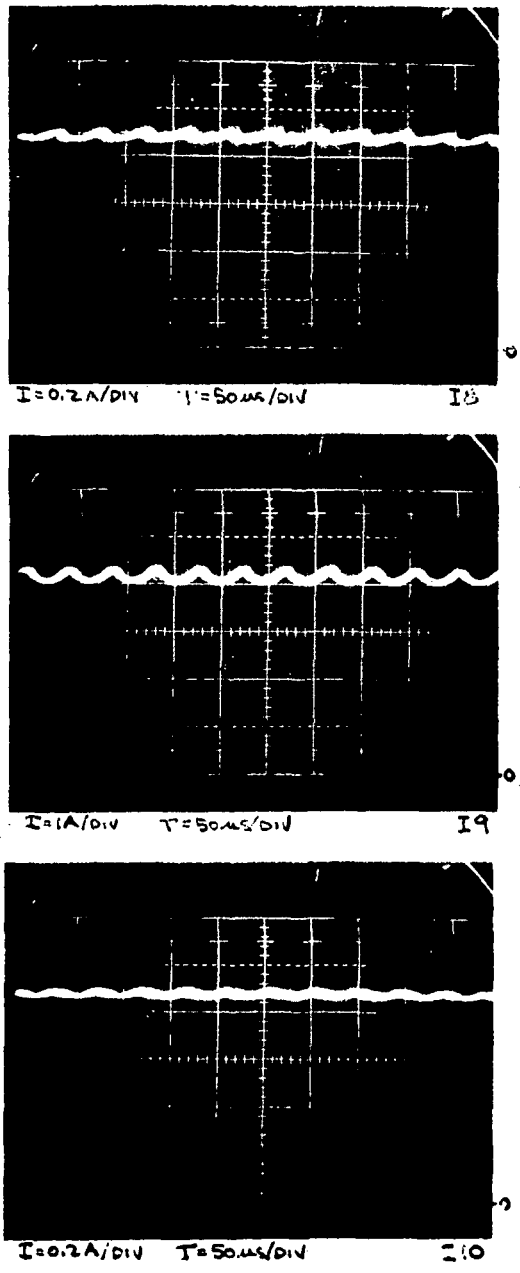


Figure 4-15. Ripple on Power Processor Input and Output Lines with Resistive Load (Continued)

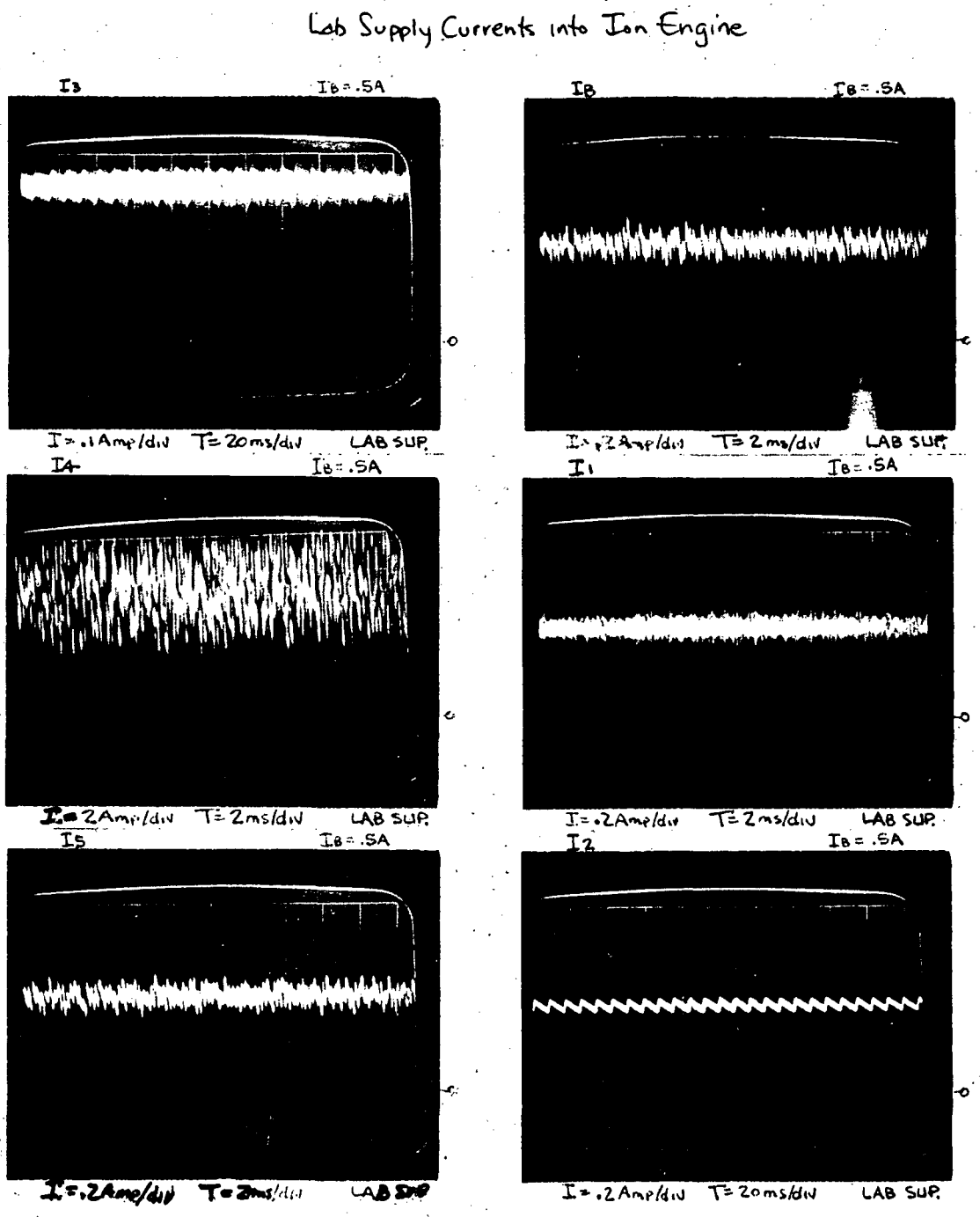


Figure 4-16. Ripple on Power Lines (Ion Engine - Laboratory Power Supplies)

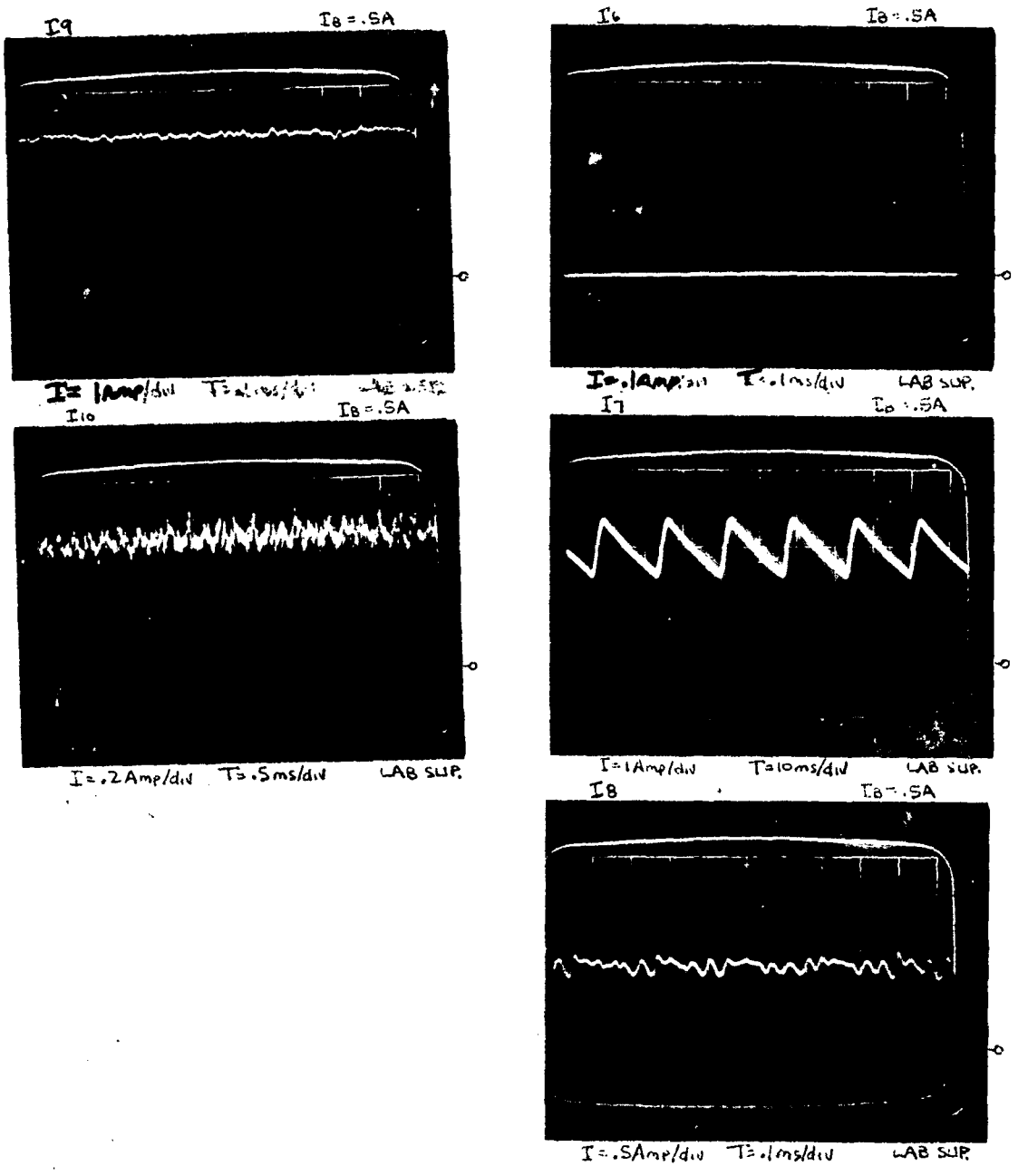


Figure 416. Ripple on Power Lines (Ion Engine - Laboratory, Power Supplies), Continued

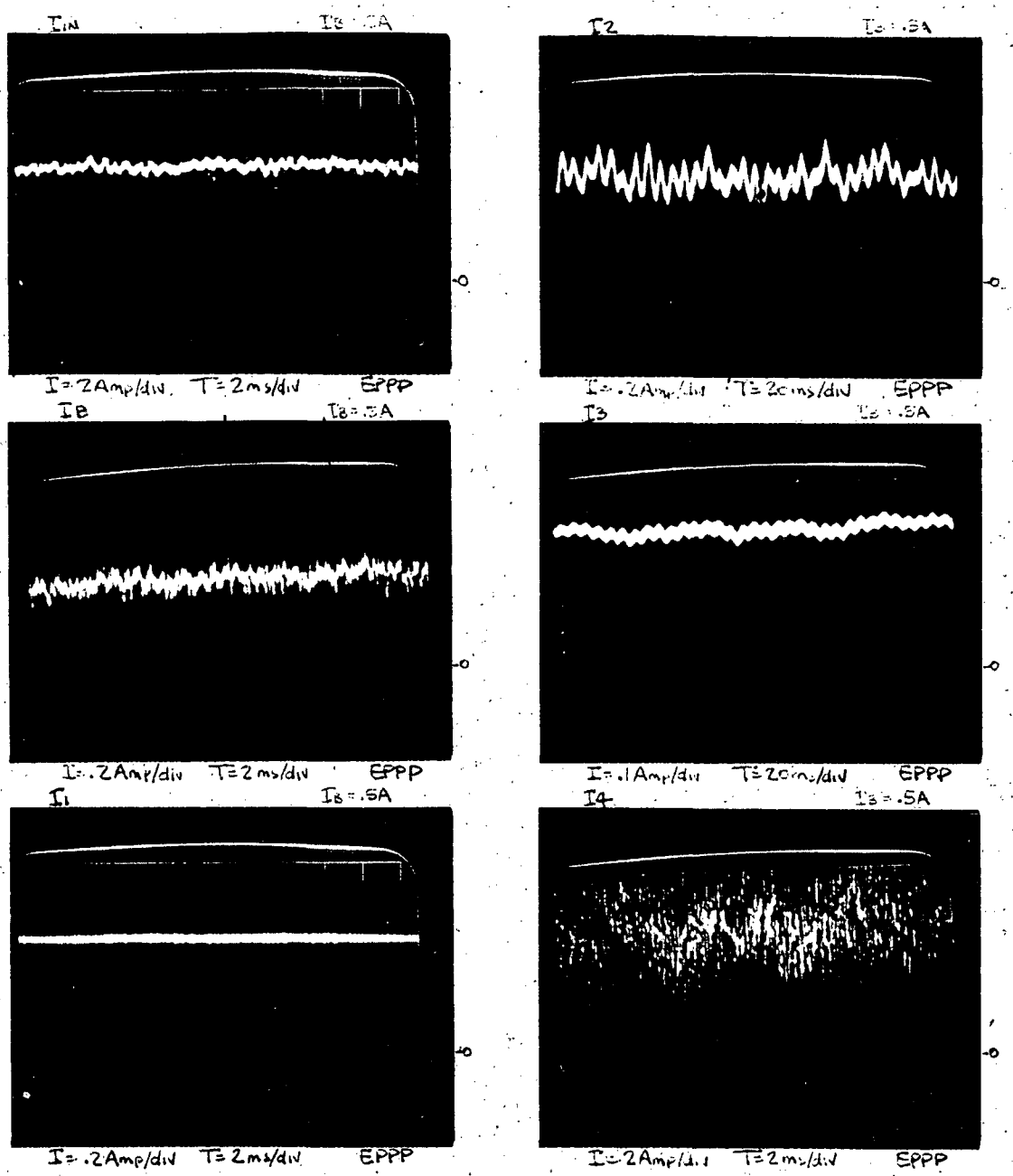


Figure 4-17. Ripple on Power Lines (Ion Engine - Power Processor Operations)

clearing system cleared the arcs and returned the engine back to normal operation. At the end of the trace, the beam current reference was varied to show the response time and stability of the beam current/main vaporizer control loop.

Figure 4-14 illustrates the input current for the power processor during the same ion engine run illustrated in Figure 4-13. At the start of the run current was drawn for the neutralizer vaporizer and keeper during start. Once the discharge was turned on, the input current varied due to overload on the discharge supply. Then the beam current is turned on and both the dc magnitude and magnitude of the ac variation increased. Once stable operation was obtained, the input current remained constant except for occasional dips, when overloads occurred in the engine. The slight current overshoot that occurs during overloads is due to recharging of the output filter on the beam supply. Note that there is no large inrush of current to the power processor that could cause collapse of the solar array bus during any mode of the ion engine operation.

The high frequency noise on the power processor and ion engine was also investigated to identify any problem areas. Figure 4-15 shows the output ripple on the input and output lines for the power processor when operating into a resistive load bank.

Figure 4-16 illustrates the noise on the power lines to the ion engine when operating from the test facility power supplies.

Figure 4-17 illustrates the power processor input and output currents when operating the ion engine. All the data has not been completely reviewed in detail. The only general comments are:

1) The ion engine load increases the current ripple delivered by the power processor.
2) The power processor input current ripple is also increased by the ion engine load.

Both broadband and narrow band conduction electromagnetic interference data were taken on all the input and output power lines for the power processor operating with the resistive load bank and with the ion engine.

Figures 4-18 through 4-22 show the narrow band data for the following lines:

$+V_{IN}$	Figure 4-18	V8 Output	Figure 4-21
V4 Output	" 4-19	V10 Output	" 4-22
V5 Output	" 4-20		

Both with the ion engine and load bank, no major difference was observed between the two loading conditions. The output lines exceeded the high frequency MIL-STD-461A Notice 1 limits.

Figures 4-23 through 4-27 show the broadband data for the two different loading conditions. All lines are above the MIL-STD-461A Notice 1 data. In addition, the V4 and V10 lines exhibited peaks at 450KHz.

It is expected that with mechanical packaging and high frequency filters, the power lines can be brought into specification.

The ion engine may require some additional filtering at the engine assembly itself so that the overall combination will be within specification. Additional study is required to determine the acceptable EMI levels and optimum filtering requirements for the power processor and ion engine.

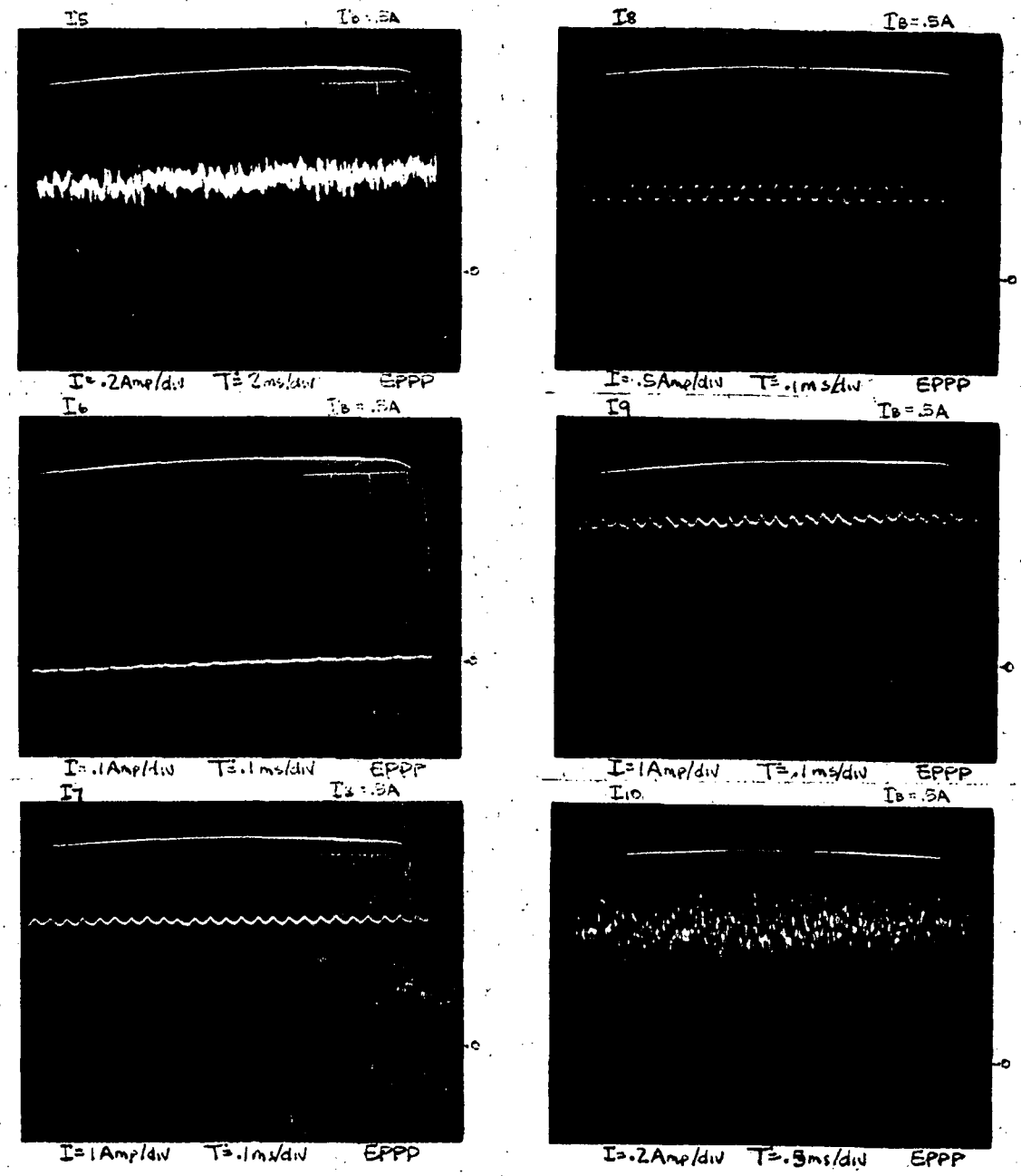


Figure 4-17. Ripple on Power Lines (Ion Engine + Power Processor Operations), Continued

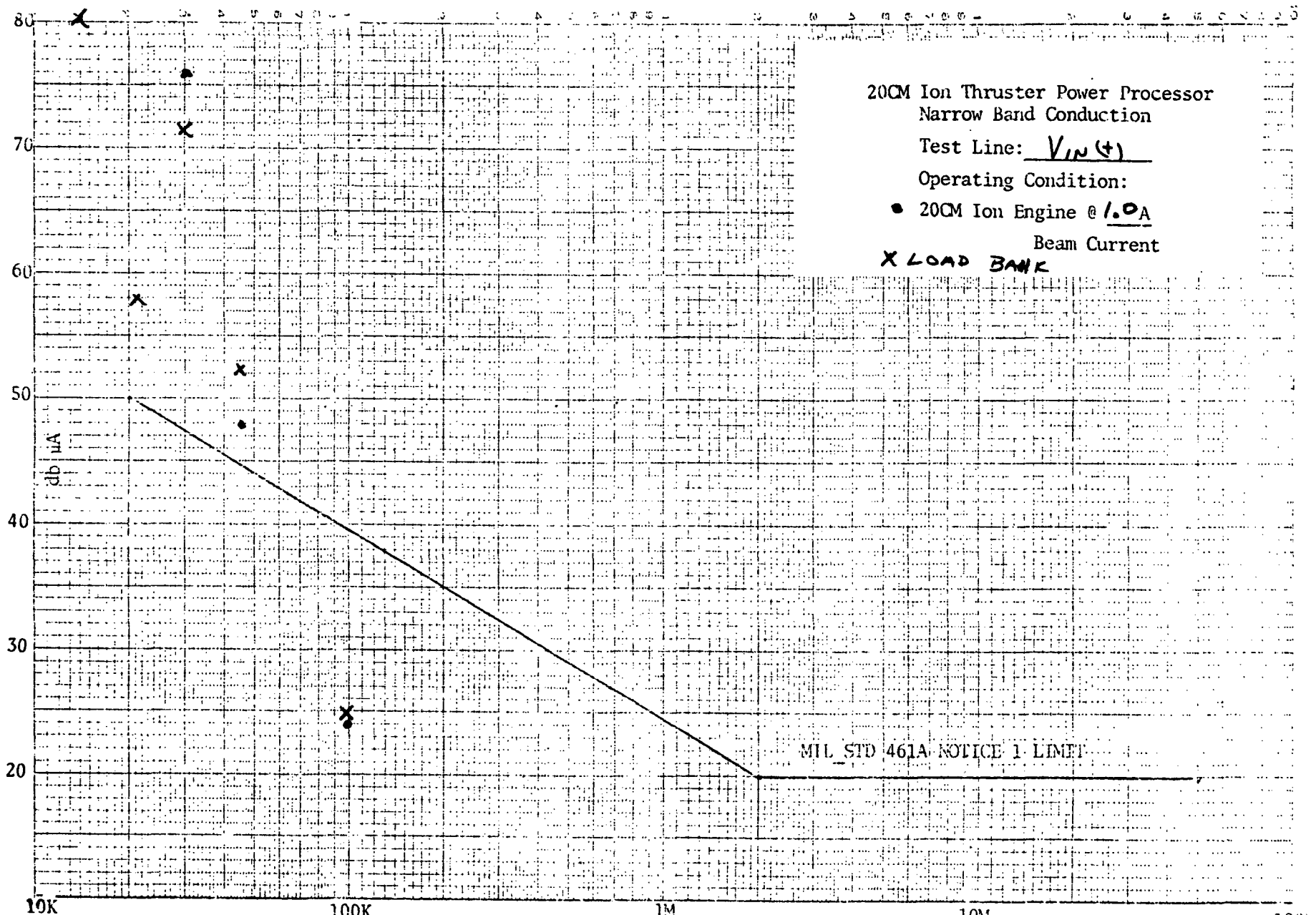

20CM Ion Thruster Power Processor
Narrow Band Conduction
Test Line: V_{IN} (+)
Operating Condition:
• 20CM Ion Engine @ 1.0A
Beam Current
X LOAD BANK
MIL STD 461A NOTICE 1 LIMIT
80
70
60
50
40
30
20
db µA
10K
100K
1M
10M
100M
FREQUENCY (HERTZ)

FIGURE 4-18

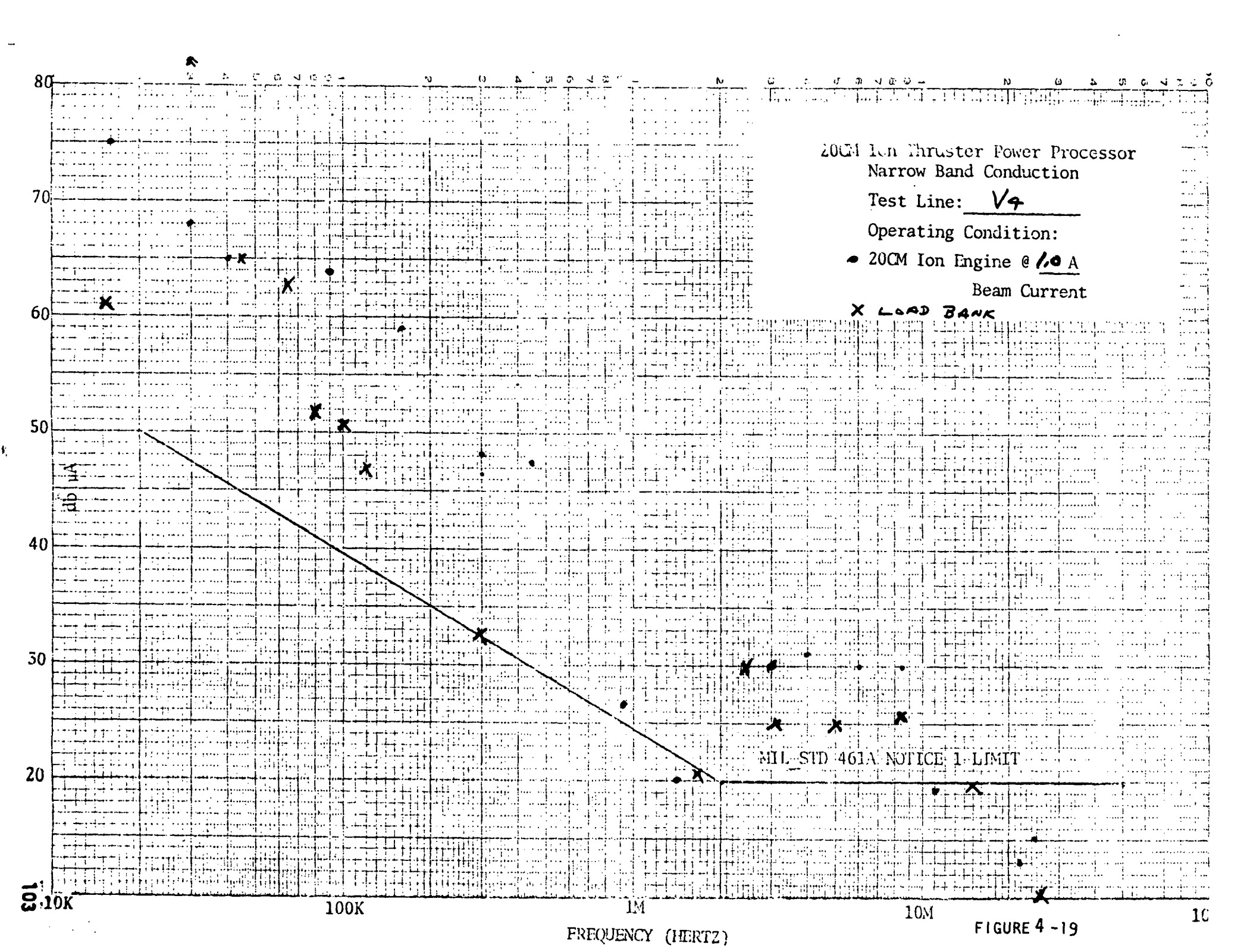

20CM Ion Thruster Power Processor
Narrow Band Conduction
Test Line: V4
Operating Condition:
• 20CM Ion Engine @ 1.0 A
Beam Current
X LOAD BANK
MIL STD 461A NOTICE 1 LIMIT
80
70
60
50
40
30
20
10
dB µA
10K
100K
1M
10M
FREQUENCY (HERTZ)

FIGURE 4-19

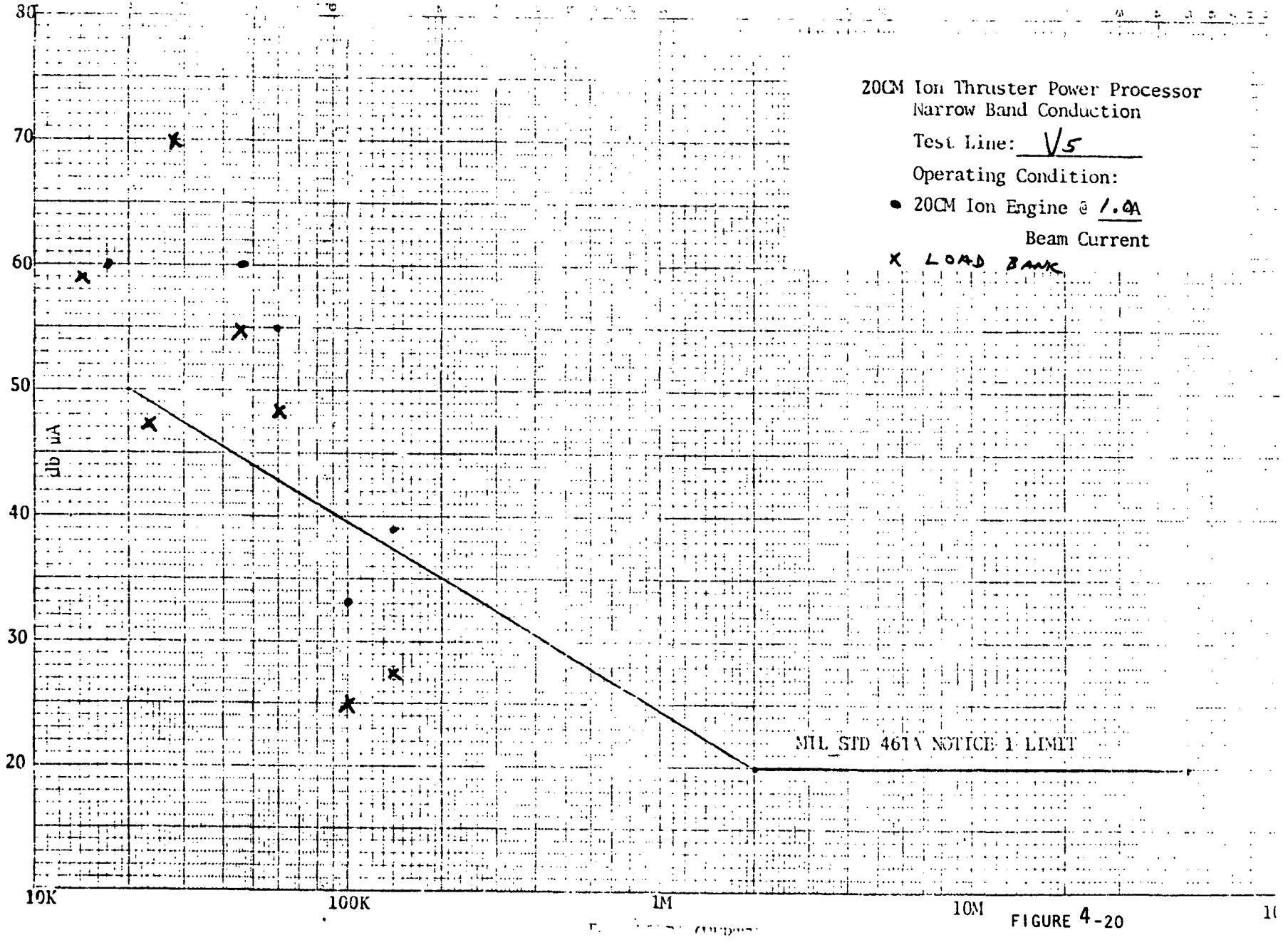

20CM Ion Thruster Power Processor
Narrow Band Conduction
Test Line: V5
Operating Condition:
• 20CM Ion Engine @ 1.0A
Beam Current
X LOAD BANK
MIL STD 461A NOTICE 1 LIMIT
dB µA
80
70
60
50
40
30
20
10K
100K
1M
10M

FIGURE 4-20

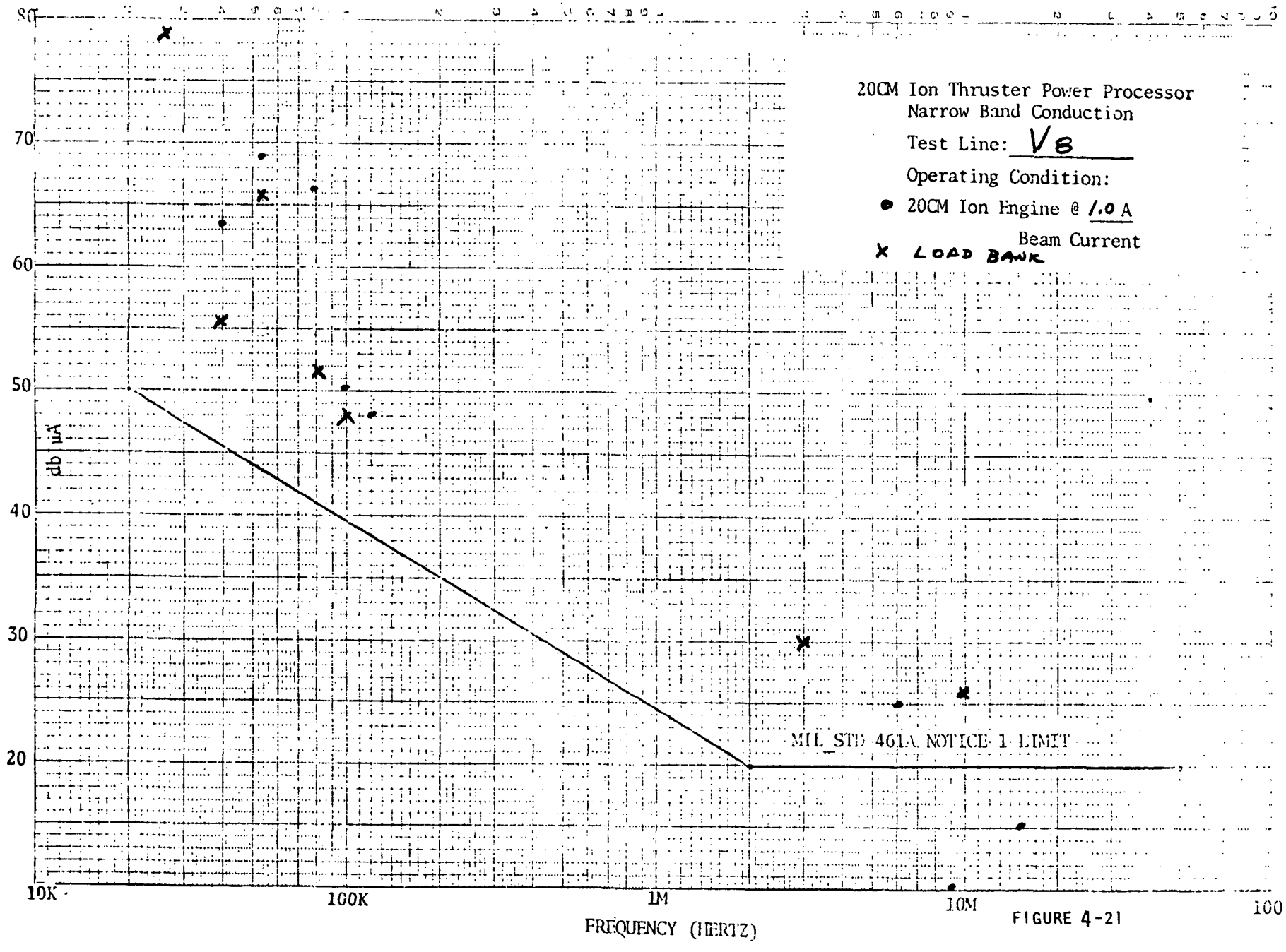

20CM Ion Thruster Power Processor
Narrow Band Conduction
Test Line: V8
Operating Condition:
● 20CM Ion Engine @ 1.0 A Beam Current
× LOAD BANK
MIL STD 461A NOTICE 1 LIMIT
dB µA
80
70
60
50
40
30
20
10K
100K
1M
10M
100
FREQUENCY (HERTZ)

FIGURE 4-21

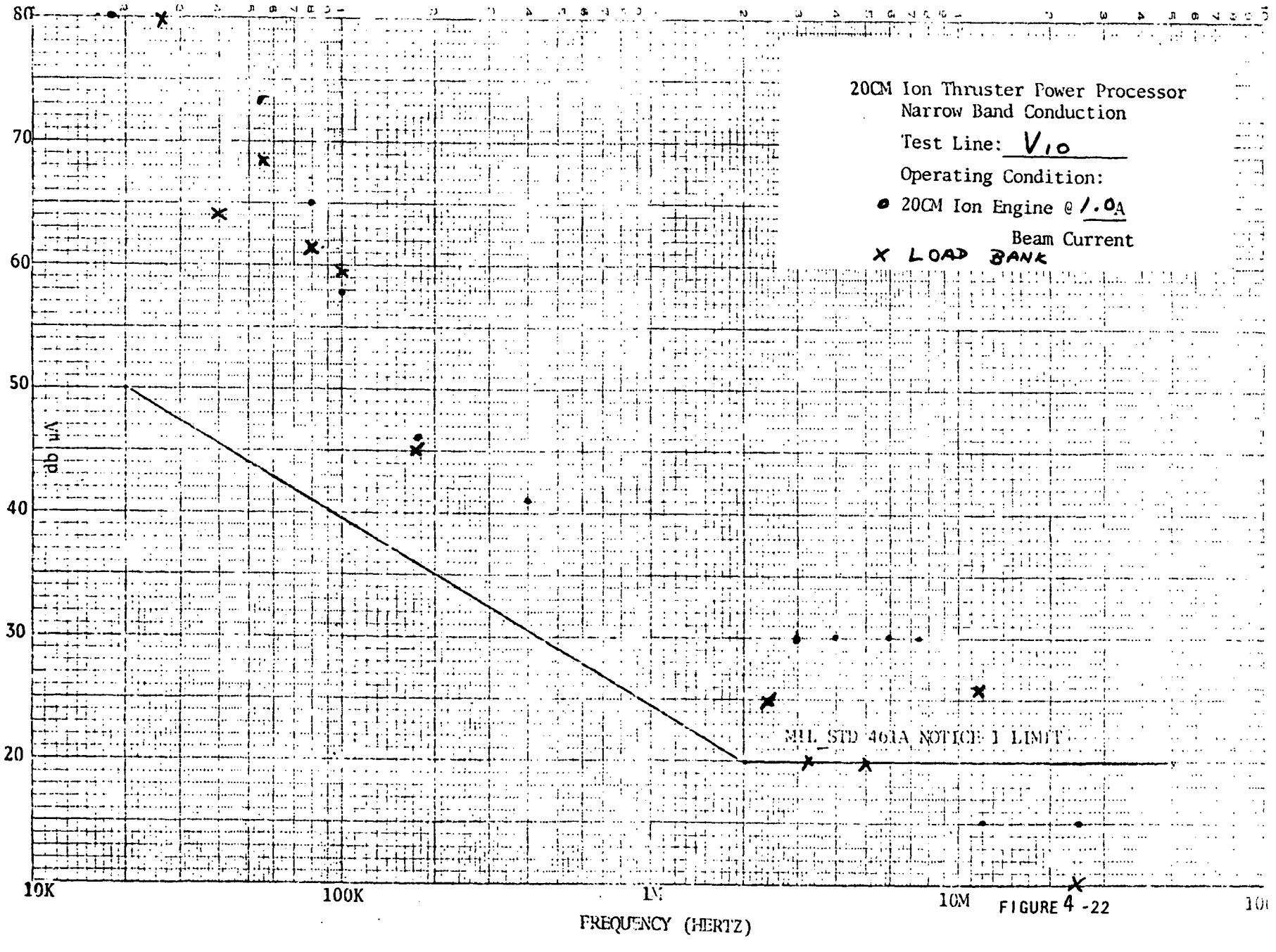

20CM Ion Thruster Power Processor
Narrow Band Conduction
Test Line: V10
Operating Condition:
● 20CM Ion Engine @ 1.0A
Beam Current
X LOAD BANK
MIL STD 461A NOTICE 1 LIMIT
80
70
60
50
40
30
20
dB μV
10K
100K
1M
10M
FREQUENCY (HERTZ)

FIGURE 4 -22

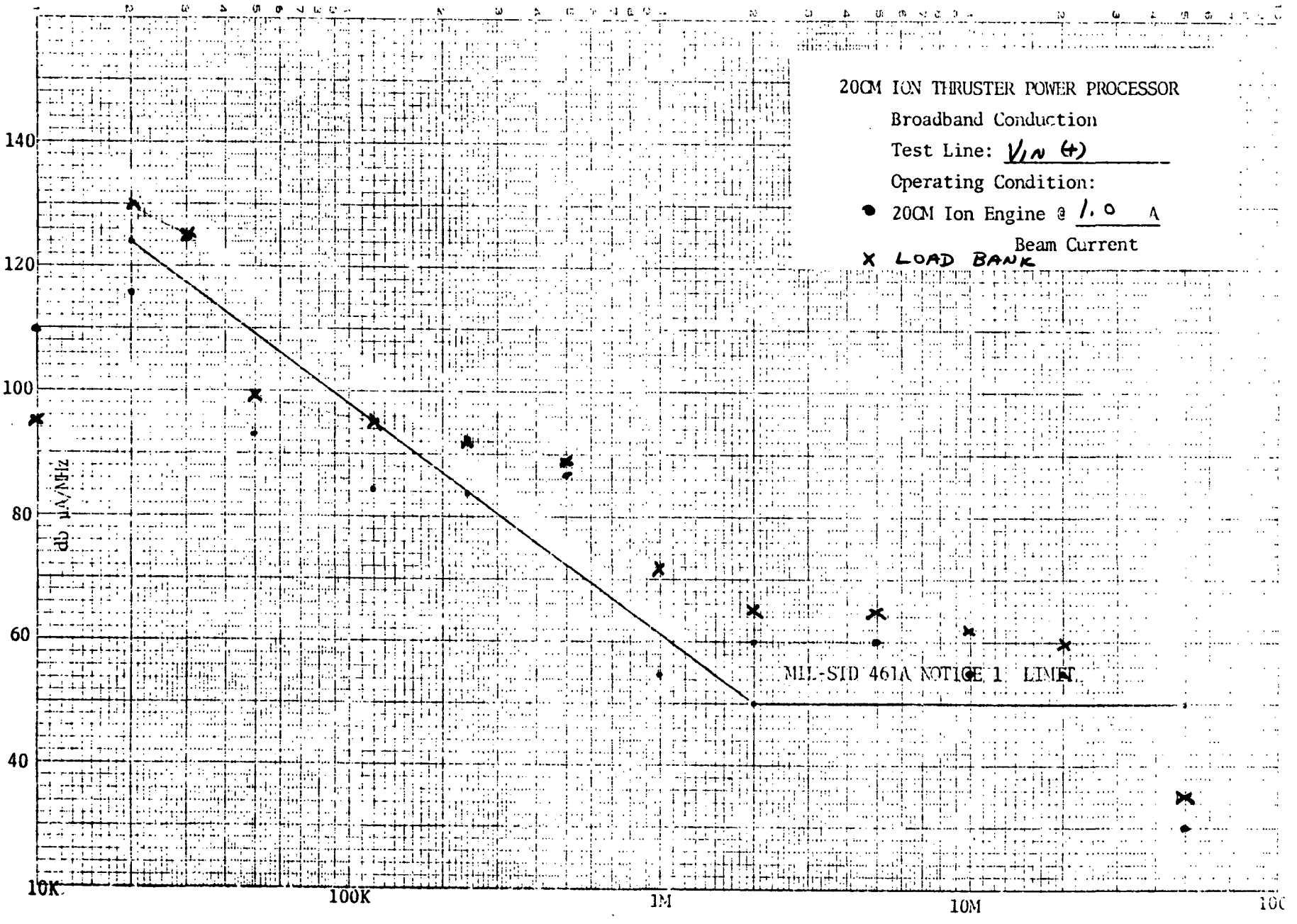

20CM ION THRUSTER POWER PROCESSOR
Broadband Conduction
Test Line: VIN (+)
Operating Condition:
20CM Ion Engine @ 1.0 A
Beam Current
X LOAD BANK
MIL-STD 461A NOTICE 1 LIMIT
140
120
100
80
60
40
dB µA/MHz
10K
100K
1M
10M
100
FREQUENCY (HERTZ)

FIGURE 4-23

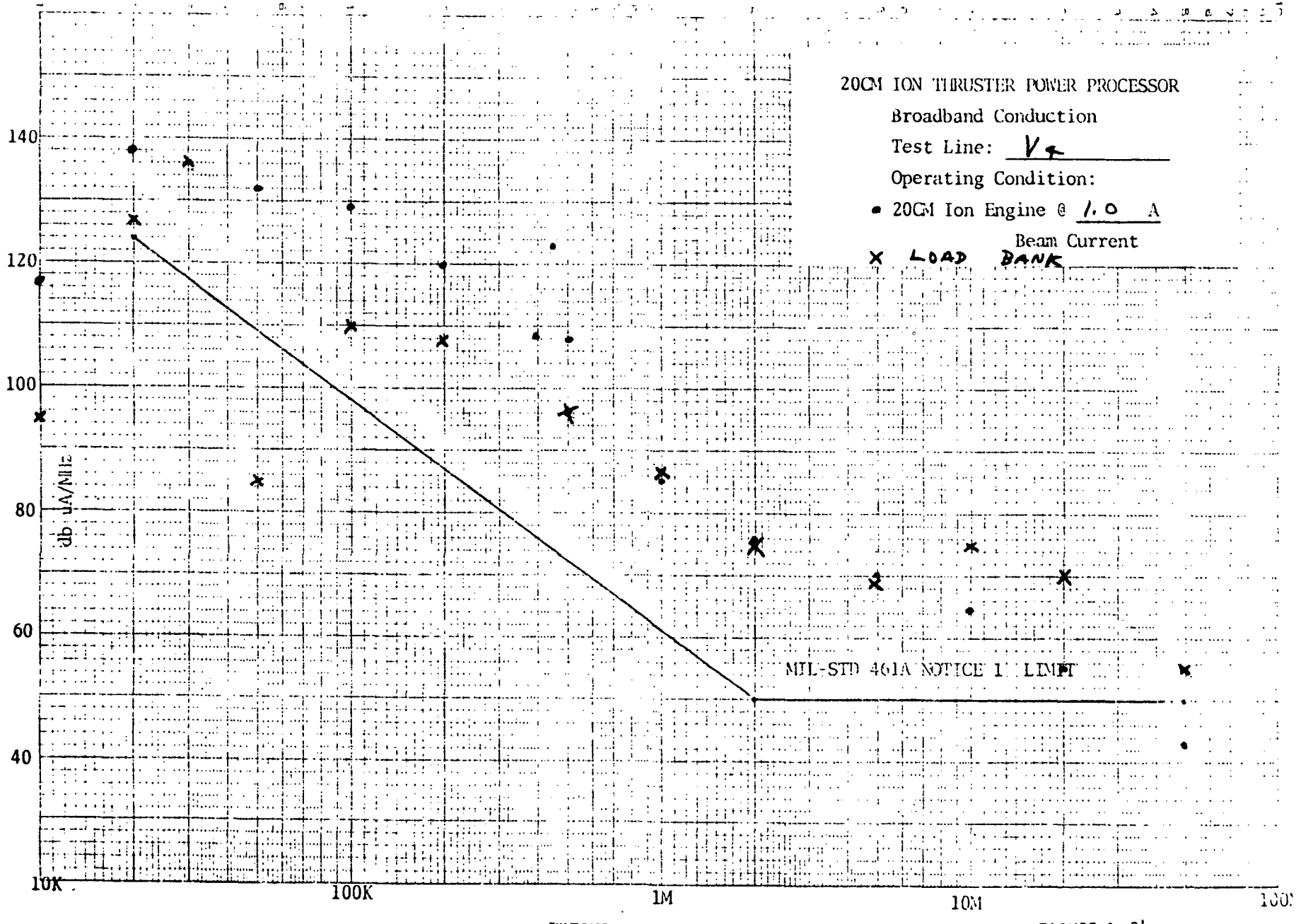

20CM ION THRUSTER POWER PROCESSOR
Broadband Conduction
Test Line: V+
Operating Condition:
• 20CM Ion Engine @ 1.0 A
Beam Current
X LOAD BANK
MIL-STD 461A NOTICE 1 LIMIT
db uA/MHz
140
120
100
80
60
40
10K
100K
1M
10M
FREQUENCY (HERTZ)

FIGURE 4-24

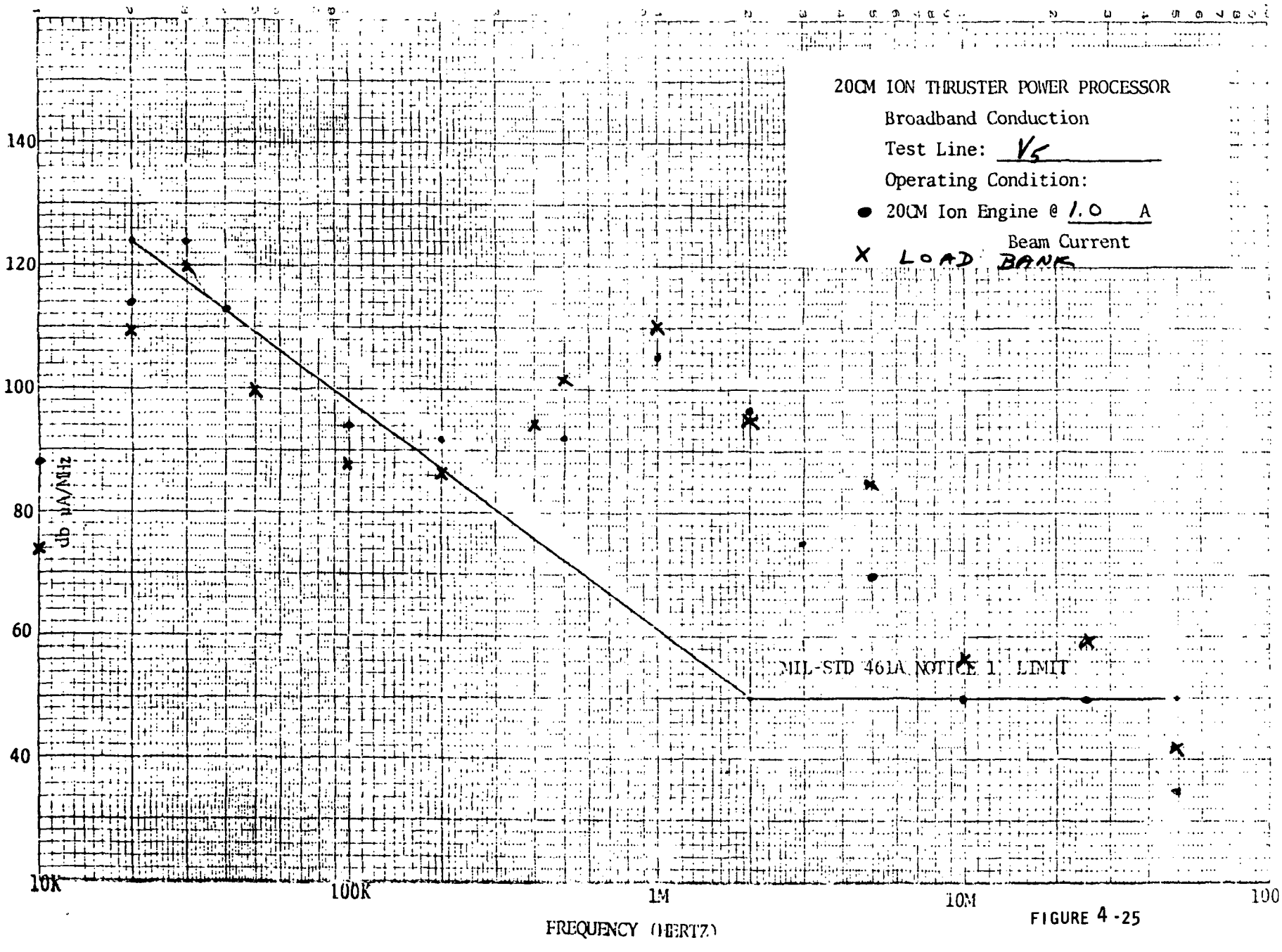

20CM ION THRUSTER POWER PROCESSOR
Broadband Conduction
Test Line: V5
Operating Condition:
● 20CM Ion Engine @ 1.0 A
Beam Current
X LOAD BANK
MIL-STD 461A NOTICE 1 LIMIT
140
120
100
80
60
40
db μV/MHz
10K
100K
1M
10M
100
FREQUENCY (HERTZ)

FIGURE 4-25

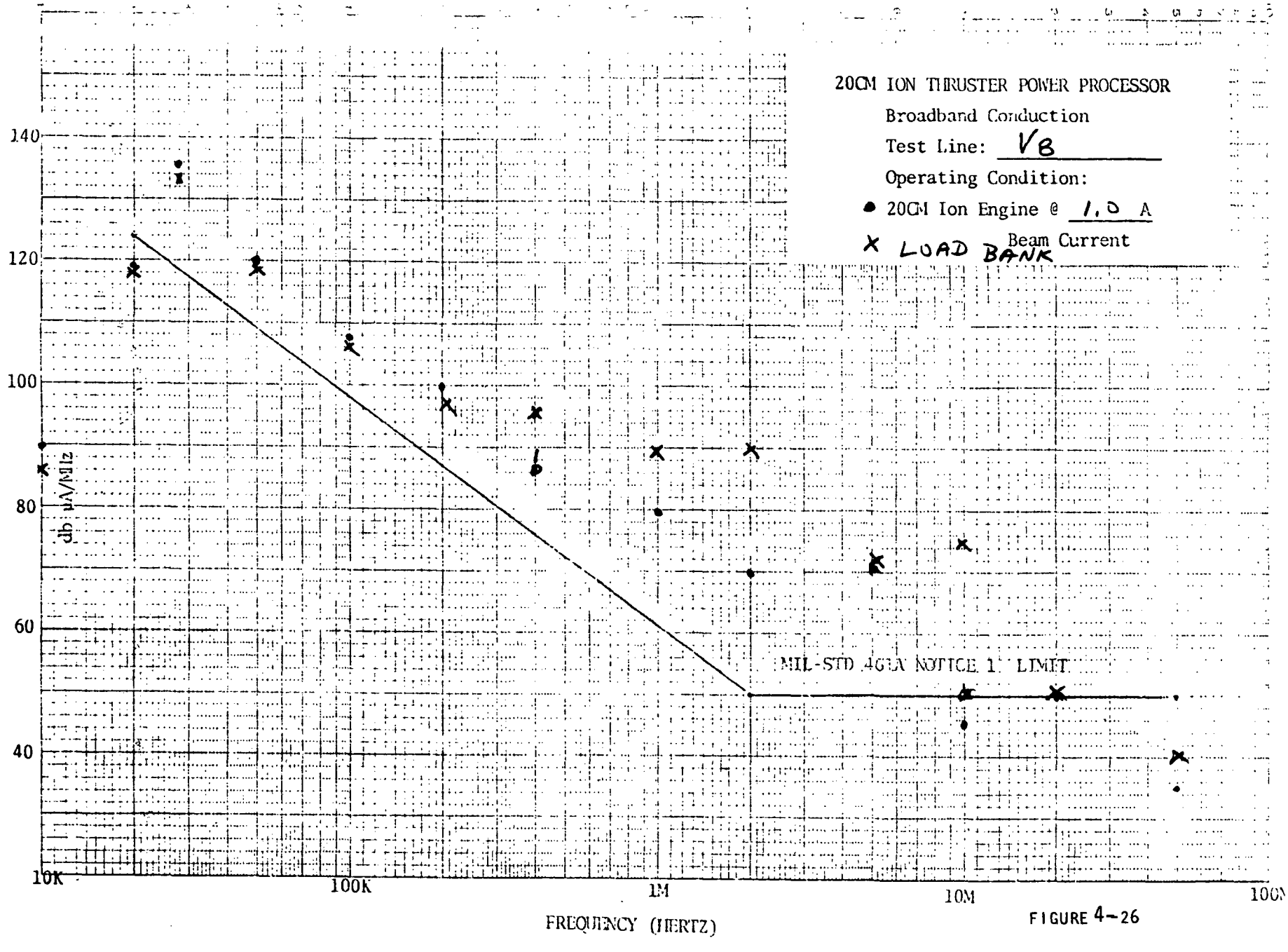

20CM ION THRUSTER POWER PROCESSOR
Broadband Conduction
Test Line: V8
Operating Condition:
● 20CM Ion Engine @ 1.0 A Beam Current
X LOAD BANK
MIL-STD 461A NOTICE 1 LIMIT
140
120
100
80
60
40
dBμV/MHz
10K
100K
1M
10M
100M
FREQUENCY (HERTZ)

FIGURE 4-26

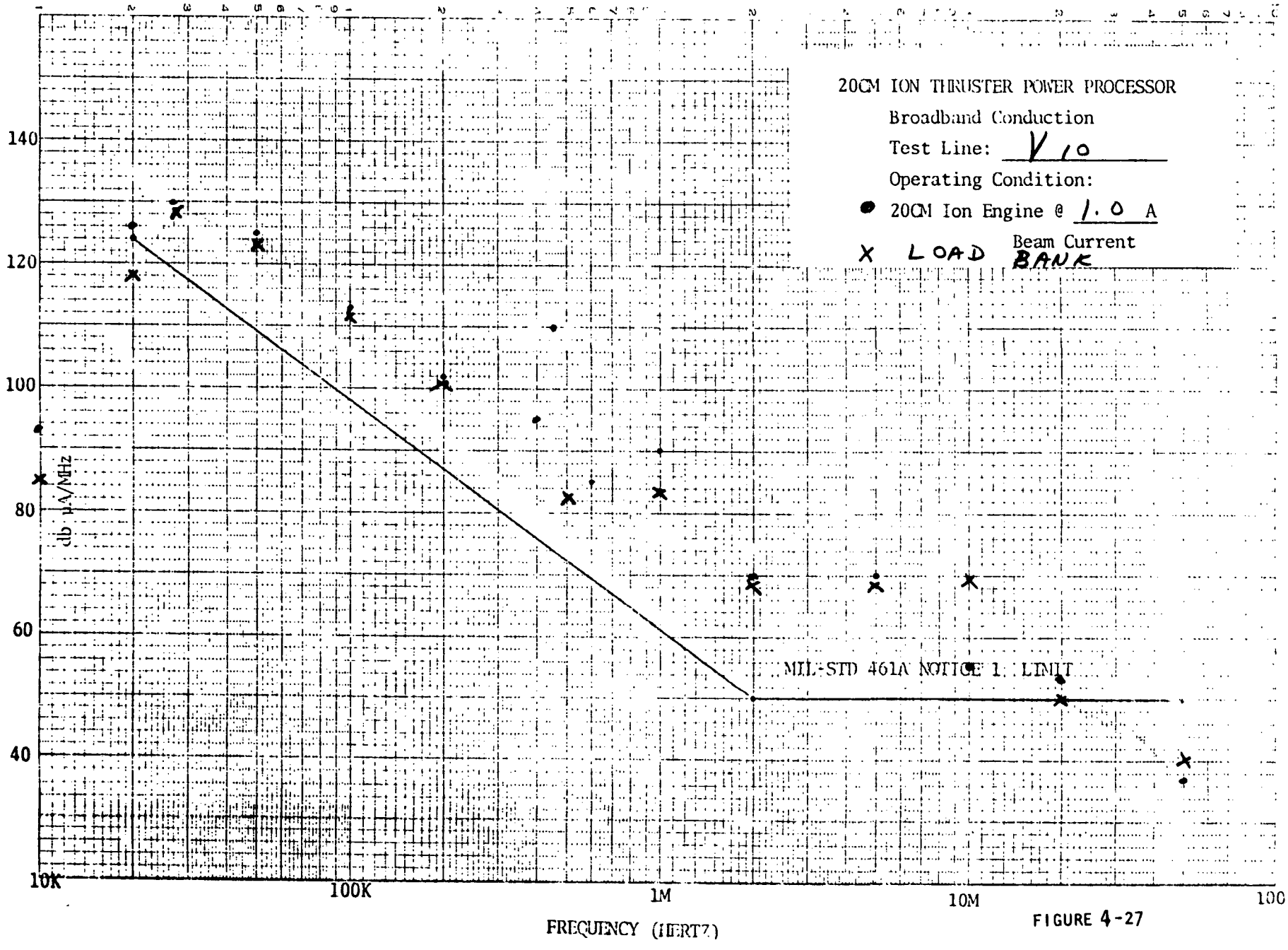

20CM ION THRUSTER POWER PROCESSOR
Broadband Conduction
Test Line: V 10
Operating Condition:
● 20CM Ion Engine @ 1.0 A Beam Current
X LOAD BANK
MIL-STD 461A NOTICE 1 LIMIT
db µA/MHz
140
120
100
80
60
40
10K
100K
1M
10M
100
FREQUENCY (HERTZ)

FIGURE 4-27

5.0 CONCLUSIONS

Many significant technical objectives were accomplished during the program to advance the state-of-the-art in power conditioning power circuit and control circuit design, in power and control components and in the design and development of an ion thruster power processor. Significant advances were also accomplished in the integration testing of a 20cm ion thruster and power processor and in the determination of the interface requirements between the solar array source, power processor, ion engine and spacecraft.

Testing demonstrated that the SCR Series Resonant Inverter is very adaptable to the requirements of a power processor unit for an ion thruster.

The most important attributes demonstrated by the SCR Series Resonant Inverter are (1) ruggedness, (2) clearance of shorts within the ion thruster, (3) adaptability to input voltages as high as 400Vdc, (4) simplicity of design due to power handling capability, and (5) potential compliance with EMI requirements.

SCR Series Resonant Inverter

A new SCR series resonant inverter was developed where the peak instantaneous current level in the power semiconductor is under control both during startup, steady state, and transient or fault modes of operation. Also a system was evolved to control the energy level in the LC resonant tank, thus limiting the voltage levels across the power semiconductors. In this inverter design, the turn-on and turn-off switching losses are greatly reduced because switching occurs at zero current, the reliability of the SCR's is increased, and the internally generated electromagnetic interference is reduced because the rate of change of current is controlled by the LC resonant tank.

High Voltage, High Power & High Frequency Operation

Operation at input voltages between 200 to 400Vdc has been demonstrated. The high input voltage places many new requirements on semiconductors and filter capacitors. Fast turn off, high voltage silicon-controlled rectifiers were used as the power semiconductor instead of transistors.

With the use of high voltage, high current silicon-controlled rectifiers, a single power stage can handle all the power requirements for the screen supply. Because of power limitation of transistors, many modular power stages are necessary to obtain the total power rating.

Microelectronic Circuits

In order to reduce the part count of the power processing design, both linear and digital integrated circuits were applied to all lower level circuitry. All signals were DC coupled, all time delays were passive instead of regenerative one-shot or monostable. All input impedances were maintained low in order to obtain high noise immunity from the high switching currents in the power processor power stages and from the high transients generated by the ion engine during its startup, steady-state and fault modes of operation. High threshold logic (HTL) operating at +15V supply was implemented for the digital circuitry. The 6V noise margin of the HTL logic provided more reliable operation for the power processor. In some special cases where long cabling was used between functions, noise levels were high and caused some out-of-tolerance operation on the engine. In future designs, low impedance line drivers will be used to transfer the digital signals over long distances between functions in the power processor.

Design, Fab. & Test 20CM Power Processor

A complete power processor breadboard shown in Figure 5-1, was developed to meet the electrical requirements of the JPL 20cm hollow cathode ion engine. It has a maximum power rating of 2.7kW and an overall efficiency of 86%. It contains 10 separate regulated outputs to control the different ion engine elements. The power processor operates directly off the 200 to 400Vdc input bus and requires no additional external low voltage power for its operation. It has all the necessary command and telemetry channels to simulate operation with an electric propulsion spacecraft and to identify interface requirements.

The power system was designed to maximize the overall efficiency. All control circuitry is at ground potential even for the outputs floating at +2kV screen supply. The power system is also designed

with separate ground returns for output power, input power, commands and telemetry so that, during fault transients of the ion engine, current loops are not generated in the power processor control electronics resulting in either component faulures or false operating conditions.

The breadboard measures 30 x 36 inches and weighs 56 lbs. (20 lbs. for components). It includes majority voting (2 out of 3) redundancy in all output regulators and has an overall reliability number of 0.925.

Because of the possible change and experimentation to be performed during the ion engine/power processor integration testing, redundancy was not incorporated in the command and protection system of the power processor.

Ion Engine/Power Processor Integration Tests

The power processor was integrated with a 20cm JPL ion engine. After solving instrumentation, grounding and noise coupling problem areas, reliable performance was demonstrated:

- Startup of neutralizer and cathode keepers
- Startup of discharge
- Turn on of high voltage
- Regulation for neutralizer keeper voltage
- Regulation of discharge voltage
- Regulation of beam current
- Two-step fault clearing system of first reducing discharge current and main vaporizer and secondly turning off beam and accelerator voltage if fault remains.
- Turn-on procedure
- Turn-off procedure

The ion engine operation was demonstrated during startup, steady-state operation for 0.25 to 1.0A beam current, fault clearing and turn-off modes. In addition, the input current variation from the power processor and electromagnetic interference levels on all input power, commands, telemetry and output power lines were measured.

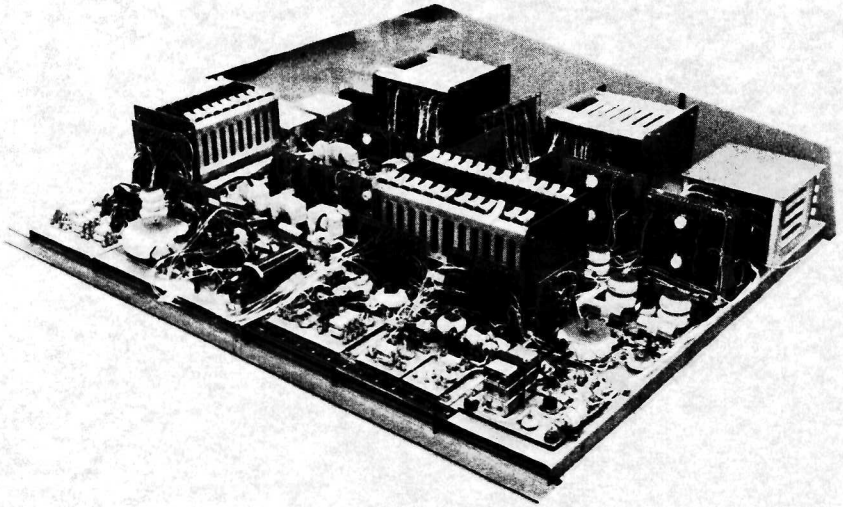


Figure 5-1. 20cm Power Processor Breadboard

6.0 APPENDICES

The following appendices are included:

Appendix A - 20CM Ion Thruster Power Processor Specification and Recommended Changes to Specification

Appendix B - Detail Block Diagram of 20CM Ion Thruster Power Processor

Appendix C - Series Resonant Power Stage Development

Appendix D - Component Development and Testing

Appendix E - Reliability Analysis

APPENDIX A

A. 20CM ION THRUSTER POWER PROCESSOR SPECIFICATION

The original specification at the beginning of contract NAS3-14383 (1 June 1971) were modified by JPL during a meeting held at TRW Systems in November 1971. These changes will be identified by enclosing them in brackets [ ].

During the process of performing the 20cm ion engine/power processor integration testing, additional specification requirement changes were identified and are discussed in Section A.2.

A.1 20CM Engine Power Processor Requirements (Appendix A of RFP)

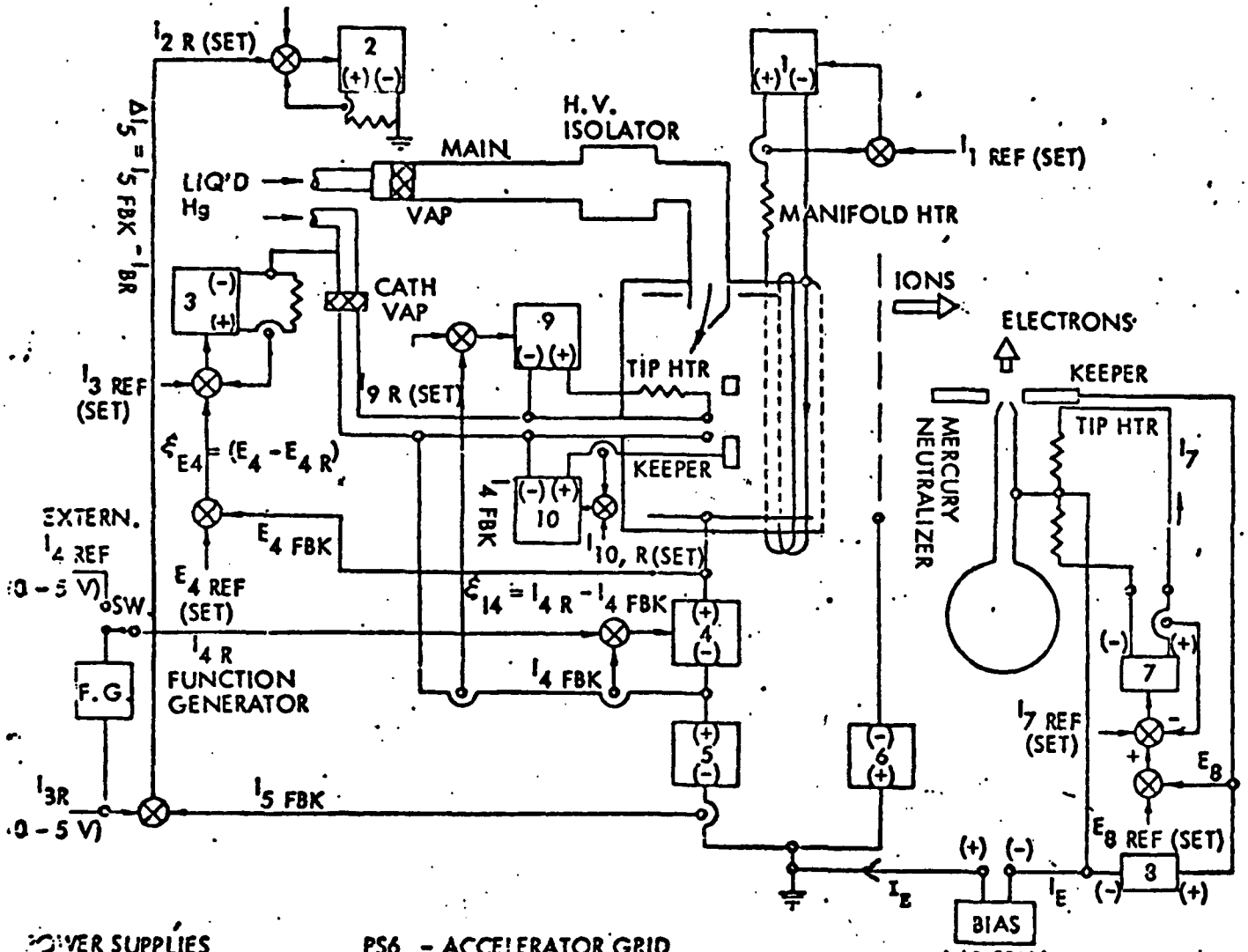
A.1.1 Electrical Requirements

A.1.1.1 Input

The power conditioner shall be compatible with a spacecraft solar cell array power source and provide stable operation of the JPL ion thruster. For design purposes 300V input is considered the nominal voltage, and the normal input voltage variation for which the power conditioner shall satisfy the output requirements specified, shall be 200 to 400V. The power conditioner shall remain operating below 200V (with out-of-tolerance outputs permissible) but will automatically shut off at or below 180V. The power conditioner shall not start below 200V input.

The solar cell array is an inherent unidirectional power source and is current limited. The power conditioner shall not supply reverse current to the input power source. Any network of filtering necessary to assure compatibility with the solar cell array power source shall be part of the power conditioner. The current ripple generated by the P.C. on the input line shall not exceed 1% RMS.

In order to avoid transient overloading of the solar panel, the peak power demand shall, under no condition, exceed 1.1 times maximum steady-state operational power.



POWER SUPPLIES
PS1 - MAGNET, MFLD HTR
PS2 - VAPORIZER MAIN
PS3 - VAPORIZER CATH
PS4 - ARC
PS5 - SCREEN (BEAM)
PS6 - ACCELERATOR GRID
PS7 - NEUTRALIZER HEATER
PS8 - NEUTRALIZER KEEPER
PS9 - CATHODE TIP HEATER
PS10 - CATHODE KEEPER
PS11 - BIAS LAB SUPPLY

FIGURE A-1 20CM THRUSTER HOLLOW CATHODE CONTROL LOOPS

TABLE A-I POWER REQUIREMENTS - HOLLOW CATHODE - 30CM THRUSTER

GROUP	SUPPLY NO.	SUPPLY NAME	TYPE	MAXIMUM RATING			NOMINAL RATING					RANGE OF CONTROL	
				E	I	P	E	I	P	Regulation	Peak Ripple		
				V	A	W	V	A	W				
I	1	Magnet Manifold	DC	19	0.85	16	13	0.6	8	0.1(I)	5	0.5-0.85 preset by I_{1REF}	Constant current
	7	Neutral Heater	DC	12	3.4	40	5.2	1.5	8	Loop (2)	-	0.3 - 3.4	Set I_{7REF} within 2.8 - 3.4A
	8	Neutral Keeper	DC	300V 20	5 mA 1.0	20	10	0.5	5	Loop or 5.0 (I)	2	(2)	Set E_8 Ref within 10-20V
	9	Cathode Tip Heater	DC	8.5	4.8	40	7.5	4	29	5.0 (I)	-	0-3	
	10	Cathode Keeper	DC	300V 20	5 mA 1.0	20	10	0.5	5	(5)	2	0.3 - 0.6 Set I_{10REF}	Constant current
II	2	Vaporizer Main	DC	11	2	22	5.5	1.1	6	Loop or 5.0 (I)	-	0.5 - 1.5 for a 1.6A setting	Set I_{2REF} within 1.6 - 2.0A
	3	Cathode Vaporizer	DC	11	2	22	5.5	1.1	6	Loop or 5.0 (I)	-	0.5 - 1.9 for a 2.0A setting	Set I_{3REF} within 1.6 - 2.0A
	4	ARC	DC	60V 37.5	N.L. 9+1	375	37	8 + 1	333	0.1 (I)	2	0.5 - 1.0 2-10	I_{4R} sets 2-9A limit
	5	BEAM	DC	2200(1)	1.05	2100	2kv	1.0	2kw	1.0 (E)	5	0.5 - 1.0	
	6	Accel.	DC	1100(1)	0.05	50	1kv	0.01	10	(2)	5	-	

NOTES: (1) No load voltage; max permissible. (2) See text.

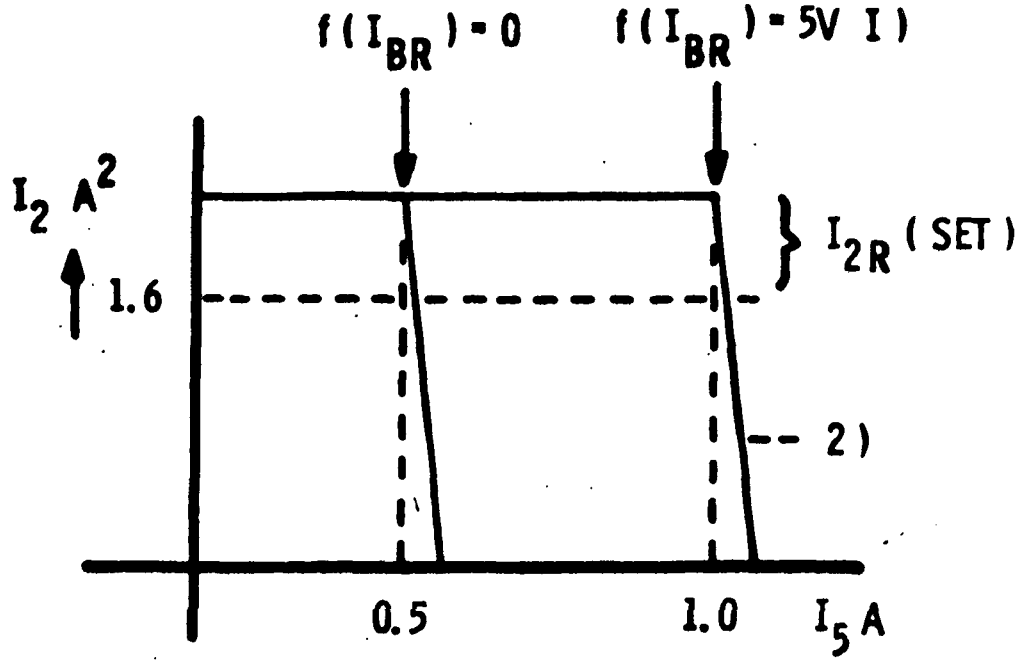
TABLE A -II

TELEMETRY DATA

SUPPLY #	NAME	TELEMETRY			
		0 - 5V Range		High Accuracy Part of TM Range	
		Current	Voltage	Current	Voltage
1	Magnet	0.3 - 0.9 A	---	0.50 - 0.75 A	---
2	Vapor. Main	0 - 2 A	---	---	---
3	Vapor. Cath.	0 - 2 A	---	---	---
4	Arc	0 - 9 A(1)	30 - 40 V(2)	2 - 9 A(1)	34 - 36 V(2)
5	Beam	0 - 1 A	1700 - 2100	0.5 - 1 A	1950 - 2050
6	Accel.	0 - 20 mA	---	---	---
7	Neutr. Htr.	0 - 4 A	---	---	---
8	Neutr. Keeper	0 - 0.8 A	0 - 30	---	---
9	Cath. Tip Htr.	0 - 5 A	---	---	---
10	Cath. Keeper	0 - 0.8 A	0 - 30	---	---

NOTES: (1) MUST MEASURE TRUE ARC CURRENT.

(2) VOLTAGE AT THE THRUSTER END.



1) Point at which I_2 Drops Rapidly is Controlled by I_{BR} . at $I_5 < I_{BR}$: I_2 = CONST

2) Slope $\Delta I_2/\Delta I_5$ = 400 $\left[\frac{A}{A}\right]$ APPROXIMATELY.

FIG. A-2 CHARACTERISTICS OF SCREEN-VAPORIZER SERVO LOOP

A.1.1.2 Outputs

The power conditioner electrical output requirements are a function of the JPL ion thruster input requirements and its operating characteristics. Figure A-1 shows a block diagram of the ion engine and power conditioning system.

The following subparagraphs present the detailed power conditioner output requirements. Electrical outputs are defined in Table A-I and Table A-II.

A.1.1.2.1 Electromagnet and Manifold Heater Supply No. 1

The supply shall be capable of providing the requirements listed in Table A-I and Table A-II.

The No. 1 supply provides power to the electromagnet and manifold which are connected in series. The resistance of the electromagnet is expected to be as follows:

(a) Cold Resistance: $R_{25°C} = 4.5\Omega$

(b) Hot Resistance: $R_{200°C} = 8.0\Omega$

22 AWG Copper Wire is being used.

The inductance of the electromagnet is 7mH.

The power requirement of the manifold heater is 8 watts at 0.60A. The manifold heater utilizes 80Ni-20Cr wire with a negligible temperature coefficient. The resistance value of the heater is 14Ω and remains practically constant throughout the operating temperature range. The supply shall be designed to provide a maximum of 16W or 19V at 0.85A for continuous operation. The supply shall be capable of supplying a load floating at 2000V above ground.

A.1.1.2.2 Main Vaporizer Supply No. 2

Output requirements for supply No. 2 are given in Table A-I and Table A-I and Table A-II. The load resistance is 5Ω (dc) and 7-1/2Ω (ac) remains practically constant throughout the full range of operating temperature. Supply No. 2 will be current limited and will operate at the spacecraft ground potential.

The power supply shall be current limited and shall be self-protected against overloads.

Supply No. 2 shall operate closed loop with the beam power supply No. 5 as shown in Figure A-2.

The feedback signal in this loop shall be derived by sensing I_5 current. The error in sensing I_5 feedback shall not exceed 0.5% of actual value.

An externally supplied reference signal, I_{BRef} will be compared to the feedback current I_5. Proportional control shall be used; the positive error signal ΔI_5 will control the input of the No. 2 supply. The range of control of I_2, per Table A-I, shall be 0.5 to 2.0. The $\Delta I_2/\Delta I_5$ shall be 100.

A.1.1.2.3 Cathode Vaporizer Supply No. 3

The supply shall be capable of providing the requirements specified in Table A-I and Table A-II.

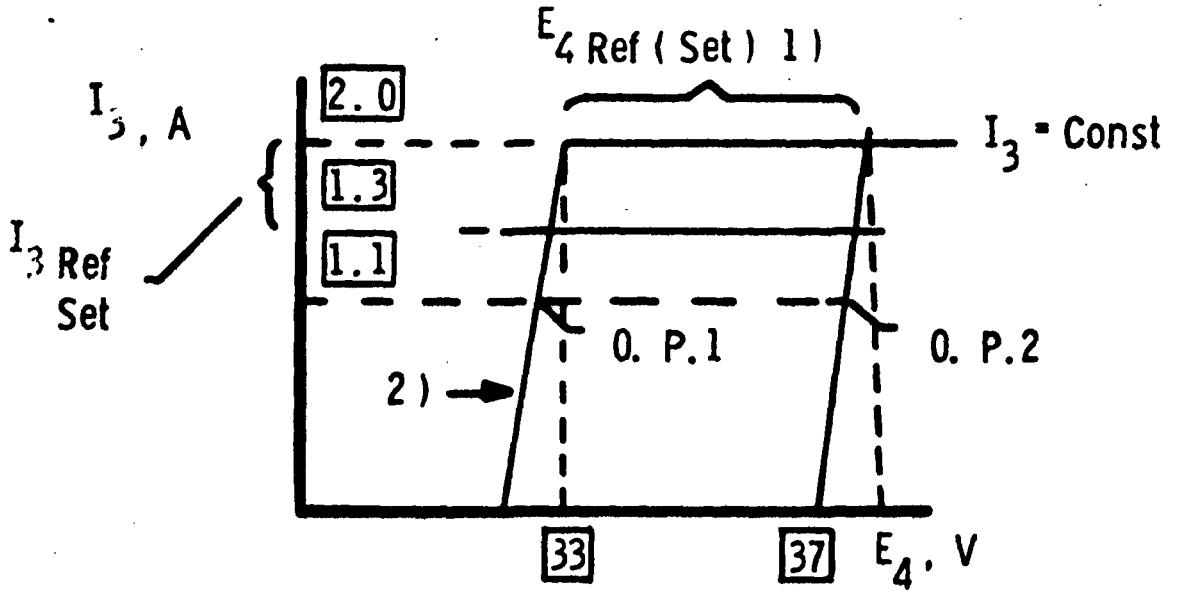
The load resistance is 5 ±0.2Ω (dc) and remains practically constant throughout the full range of operating temperature. PS-3 will be current limited; it will operate at 2KV above-ground potential, or at ground potential and shall be self-protected against overloads.

Supply No. 3 shall operate in closed loop with the arc power supply No. 4 (paragraph A.1.1.2.4.).

This loop is the major loop. Another, minor current loop is provided that maintains the output current constant and is equal to the preset reference value I_{3Ref}. The I_{3Ref} covers the range of 1.6 to 2.0A (Figure A-3).

Initially, after the thruster is ignited, the major servo loop is open (i.e., $E_4 > E_{4Ref}$) and the supply No. 3 operates at the constant current mode (Figure A-3).

The major servo loop closes when E_4 drops below E_{4Ref} because the arc current I_4 has reached the level of reference I_{4Ref} (Figure A-4) and PS-4 has started to operate in the current limited region.



1) Point at which I_3 rapidly drops is preset by E_{4Ref}, at $E_4 > E_{4Ref}$ I_3 = CONST

2) Slope $\Delta I_3/\Delta E_4$ to be approximately 0.8 $\left[A/V\right]$

FIG. A-3 CHARACTERISTICS OF ARC CATHODE SERVO LOOP

This loop is self-compensating which means that lowering of E_4 causes a reduction of I_3 and a reduction of Hg vapor within the arc, resulting in a rise of E_4.

The E_{4Ref} shall be adjustable from 32V to 35V.

A.1.1.2.4 Arc Supply No. 4

Supply No. 4 shall be capable of providing the requirements specified in Table A-I and Table A-II.

The supply shall be capable of supplying a load floating at 2000V above ground.

The specified value of E_4 shall be provided at the output terminals of the power conditioner.

In view of the fact that the arc power supply carries the sum of the arc and beam currents, the "true" arc current shall be derived from the sensor placed in the negative arc return line, as per Figure A-1.

The arc supply requires two modes of operation: (a) startup, and (b) normal closed loop operation. These are discussed separately. The E-I characteristic is shown in Figure A-4.

(a) Startup: For startup, in order to initiate a discharge within the thruster ionization chamber, a minimum of 60Vdc open circuit with a short circuit capability of at least 20mA shall be provided.

(b) Normal Operation: Once a discharge has been initiated, an uninterrupted voltage transition to the lower level of operation is required.

The open loop E-I characteristic of the supply is shown in Figure A-4a. The exact shape of the characteristic shall be at the discretion of the designer, providing that the output voltage at the thruster terminals at 10A in all cases is not lower than 37.5V and minimum 60V at no-load.

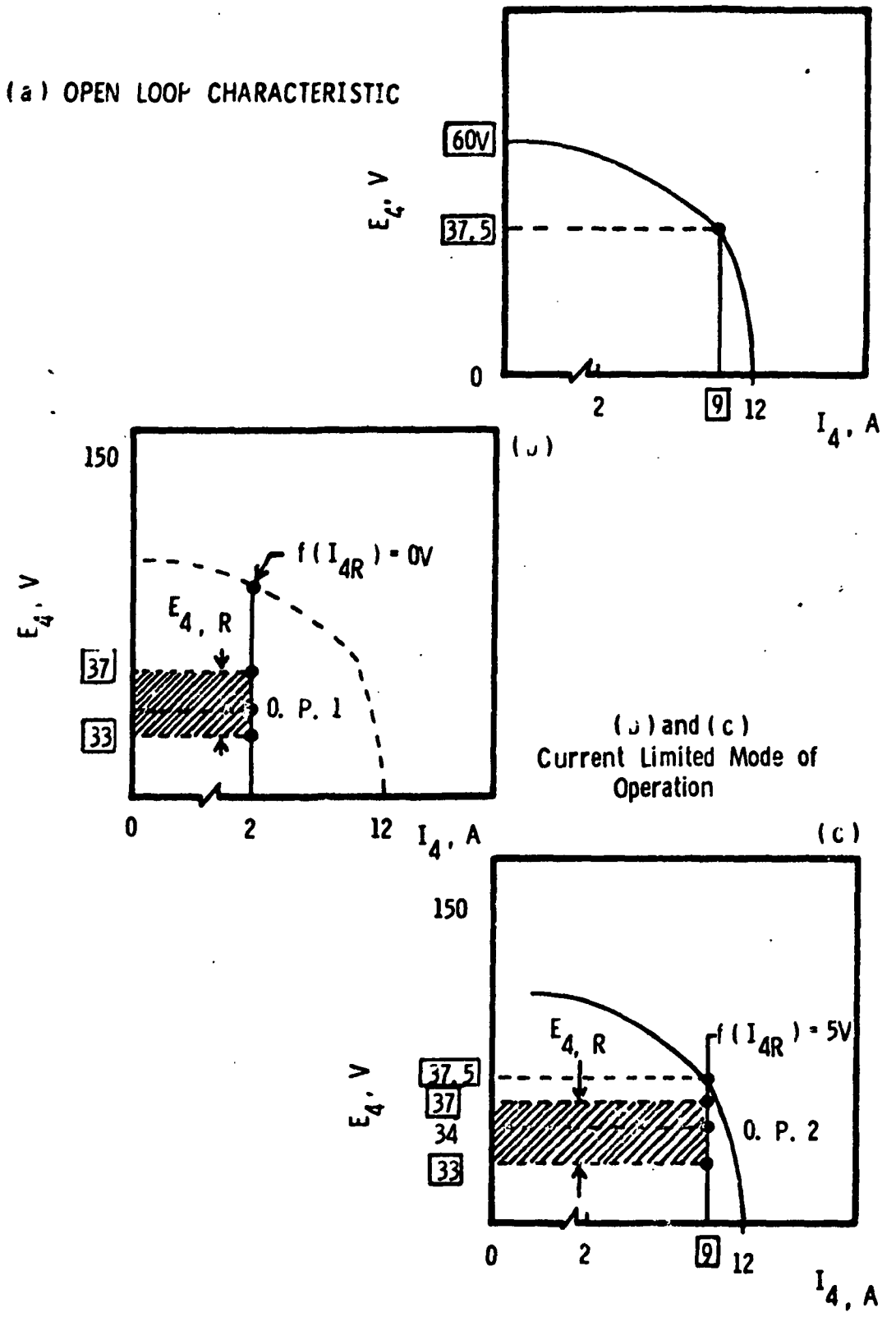


FIG. A-4 E-I CHARACTERISTICS OF THE ARC POWER SUPPLY NO. 4

The operating point will settle at a voltage level defined by E_{4R}. For example, in Figure A-4b E_{4R} = 33V, and in Figure A-4c E_{4R} = 34V. The range of E_{4R} setting shall be [33-37V,] as further described in Figure A-3. The slope of the current limit shall be approximately $\Delta E_4/\Delta I_4$ = [100[V/A].] Arc supply No. 4 shall operate in closed loop with the cathode vaporizer supply No. 3. This major loop shall force PS-4 to operate in the current limited mode at the voltage level determined by E_{4Ref}. This reference shall be presettable to [33 to 37V.] For further details see paragraph A.1.1.2.3.

A.1.1.2.5 Beam Power Supply No. 5

The supply shall be capable of providing the requirements specified in Table A-I and Table A-II.

A minor servo loop shall keep the output voltage constant within 1.0% for line voltage and load current variations specified.

Supply No. 5 will operate closed loop with the vaporizer supply No. 2 as described in paragraph A.1.1.2.2. (Also see Figure A-5.)

The current sensor of I_{5FBk} (see Figure A-1) shall be compensated, as not to measure the accelerator current that circulates through PS-5.

A.1.1.2.6 Accelerator Supply No. 6

The supply shall be capable of providing the requirements specified in Tables A-I and A-II.

A minor servo loop shall keep the sum of the output voltage E_4 + E_5 + E_6 constant within 0.1% for line voltage of 200 to 400V over load current variations as follows: I_4 = 2 -10A, I_5 = 0.5 -1.0A, I_6 = 5 -10mA.

A.1.1.2.7 Neutralizer Cathode-Vaporizer Supply No. 7

The supply shall be capable of providing the requirements listed in Table A-I and Table A-II. The current limit shall be internally adjustable within [2.8 to 3.2A] range. Supply shall be capable of supplying a load floating at [200V] below the ground.

The output of the No. 7 supply shall be controllable by a voltage feedback signal from the output of the No. 8 supply. This signal will be compared to a voltage regerence (E_{8Ref}) and the error signal generated will be used to control the output current. E_{8Ref} shall be internally adjustable to allow presetting E_8 anywhere within the range of 10 to 20V.

In addition, another feedback loop which permits operating supply No. 7 at constant current will be provided. The I_7 current feedback will be compared to a current reference (I_{7Ref}) and the error signal will keep I_7 at a constant preselected value. The range I_{7Ref} will be internally adjustable to preset I_7 within 3.0A and 3.8A. The two loops will be designed so that the voltage loop will have priority over the current loop.

The control characteristics shall be such that the constant output current I_7 will be maintained until E_8 drops below E_{8Ref}; below this value of E_8, the current I_7 will be reduced proportionally; this will be accomplished by means of an error signal ($E_{8Ref} - E_8$) (See Figure A-6).

Slope $\Delta I_7/\Delta E_8$ (Figure A-5) shall be approximately .8A/V.

A.1.1.2.8 Neutralizer Keeper Supply No. 8

The supply shall be capable of providing the requirements specified in Table A-I and Table A-II. An output isolation of 200V shall be provided for bias operation. The neutralizer keeper supply requires two modes of operation: (a) initiating a discharge, and (b) normal operation.

(a) Initiating a Discharge - For startup and initiating a discharge in the neutralizer, a minimum of 300Vdc at 5mA with a short circuit capability of 20mA shall be provided. Once a discharge has been initiated, an uninterrupted voltage transition to the normal operating level shall be provided.

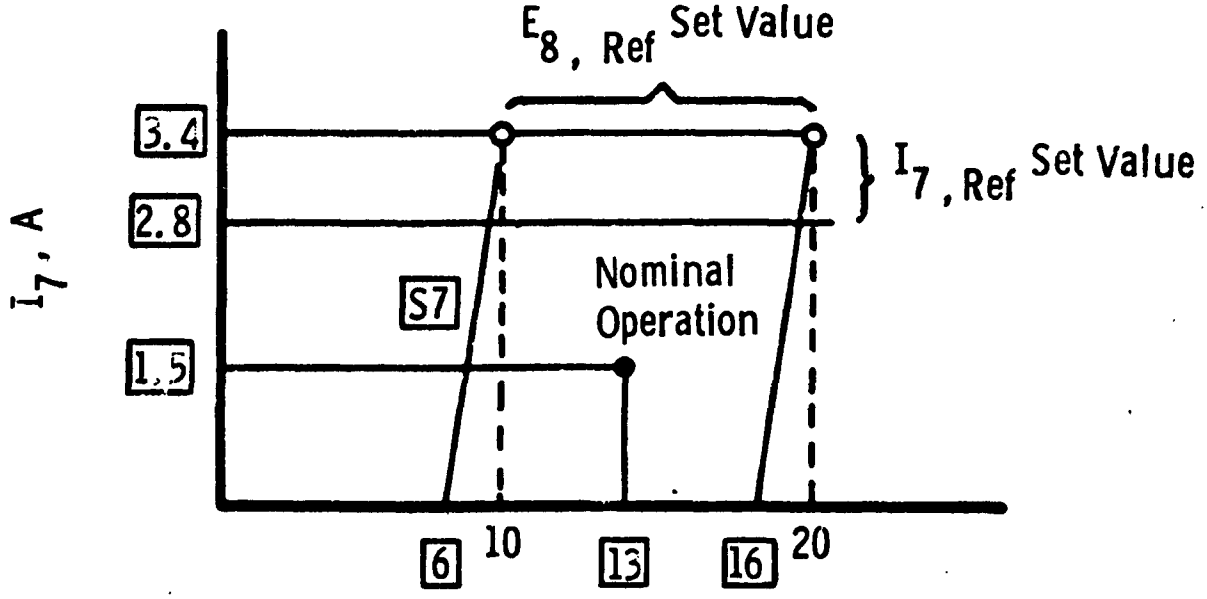


FIG. A-5 SERVO LOOP CHARACTERISTICS OF NEUTRALIZER SYSTEM

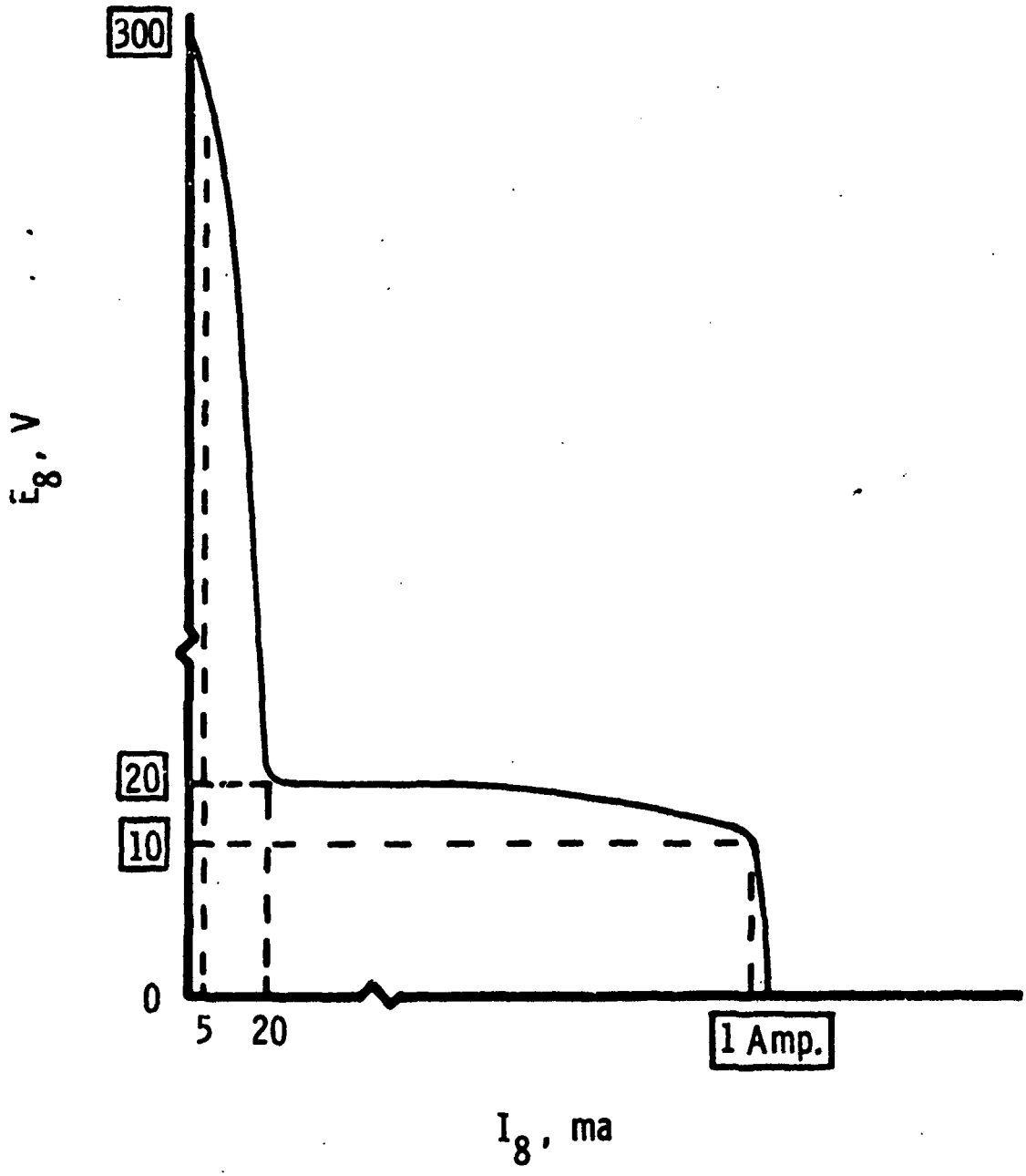


FIG. A-6 NEUTRALIZER KEEPER SUPPLY, NO. 8 AND CATHODE KEEPER SUPPLY, NO. 10

(b) Normal Operation - The normal operation of the neutralizer keeper supply requires 20V at maximum current with current limit adjustable between 0.5A (See Figure A-6) to 0.6A. The exact shape of the characteristic below 0.5A shall be at the discretion of the designer. The operating point lies in the vicinity of 1.0A in the constant current region.

This supply operates in a closed loop with supply No. 7, as described in paragraph A.1.1.2.7.

A.1.1.2.9 Cathode Tip Heater Supply No. 9

The supply shall be capable of providing the requirements specified in Table A-I and Table A-II.

The load resistance is 1.75 ±0.1Ω (dc) hot and 0.2Ω (dc) cold. Tungsten wire is used for this heating element.

The power supply shall be current limited and be self-protected against overloads. It does not need to be of a regulated type.

PS-9 shall be turned on by the ON-1 COMMAND (para. A.1.1.4.2). A 5V/5mA signal from the controller or an auxiliary source as provided by JPL shall be capable of turning the PS-9 off.

A.1.1.2.10 Cathode Keeper Supply No. 10

The supply shall be capable of providing the requirements specified in Table A-I and Table A-II. Requirements are provisional and may change. Supply requires two modes of operation: (a) initiating a discharge and (b) normal operation; requirements for (a) are identical with these defined for PS-8; requirements for (b) differ. In the low voltage region, supply will operate at the constant current, as preset by the I_{10Ref}.

The output of this supply is floating 2KV above the ground.

A.1.1.3 Overload Response

It is necessary that each individual supply shall be protected against excessive current.

It shall be the design objective that all the supplies shall be short circuit proof and shall not be overloaded even by a permanent short. Each supply should be capable of operating with any such load without causing any component to exceed the temperature allowed by reliability assessment of the component.

In addition, supplies 5 and 6 shall be equipped with an overcurrent detector that initiates a temporary shutdown in case of a sustained arc between grids. The shutdown shall occur only if the overcurrent condition persists for a period longer than approximately 100ms.

A.1.1.4 Startup and Shutdown

A.1.1.4.1 Commands

The power conditioner will be activated from an external source by means of commands for operating relays. Each command shall have:

(a) Amplitude of 20 to 31Vdc.
(b) Duration of 20ms or more.
(c) Current capability of 100mA.

All command lines will be power conditioner ground potential.

A.1.1.4.3 Startup Procedure

(a) Reset latching relays by OFF 2-CMD.
(b) Turn on PS 1, 4, 8, 9, 10 by ON-1 CMD.
(c) After a time delay, as defined by the operator, turn on PS 2, 3, 7 by ON-2 CMD.
(d) After a time delay, as defined by the operator, turn on PS 5 and 6 by ON-3 CMD.
(e) The power conditioner shall then be ready to respond to $I_{B,Ref}$ signal.

A.1.1.4.4 Shutdown Procedure

Two OFF commands are available:

(a) OFF-1 CMD - turns off vaporizer supply No. 2 only.
(b) OFF-2 CMD - turns off all power supplies.

The OFF-1 command shall not be nullified by arcing tripping and the recovery of the system. The capability shall be provided to restart the power conditioner and nullify the OFF-1 command by sending the ON-2 command only.

Two types of shutdowns may occur:

Regular Shutdown - The OFF commands will be generated by the controller to terminate operation of a well running engine, which is to be used again. Procedure is aimed at eliminating any possible contamination of surfaces by condensation of mercury. First, by "OFF 1" Relay CMD the Vaporizer Supply No. 2 is turned off. Rate of delivery of mercury decays. Wait until beam current decays below 1/3 of the preset reference value and then send the OFF 2 CMD.

Emergency Shutdown - "OFF 2" Relay CMD will be given, "OFF 1" CMD will not be used.

A.1.1.4.5 Recovery from Arcing

Some of the arcs that occur within the thruster or between the thruster and the facility ground will not extinguish and must be interrupted artificially. The mechanization of PC shutdown and restart shall be as follows: Shutdown of the thruster shall be initiated by one of the overcurrent trips as defined in Para. A.1.1.3. Such a signal shall shutdown supplies Nos. 1, 2, 5, 6. After a delay, that can be readjusted, power supplies Nos. 5 and 6 will be turned on. The magnet power supply No. 1 is also turned on, and magnet current linearly increases to the full value within three seconds (Para. A.1.1.3). The main vaporizer power supply No. 2 is turned on after a preset delay (Para. A.1.1.3).

Should the arcing and restart occur, after "OFF 1" was applied, restarting sequence will not nullify such command.

A.1.1.5 Analog Control of the Spacecraft

A.1.1.5.1 The analog signal required to command the spacecraft will be supplied in the form of I_{BRef} from a source with maximum impedance of 1KΩ; maximum current drain from this source will be less than 40μA. The value of this reference signal shall be continuously varied from 0Vdc (I_5 = 0.5A) to +5Vdc (I_5 = 1.0A). Figure A-7 shows the steady-state transfer characteristics of the system. The command line shall be at P.C. ground.

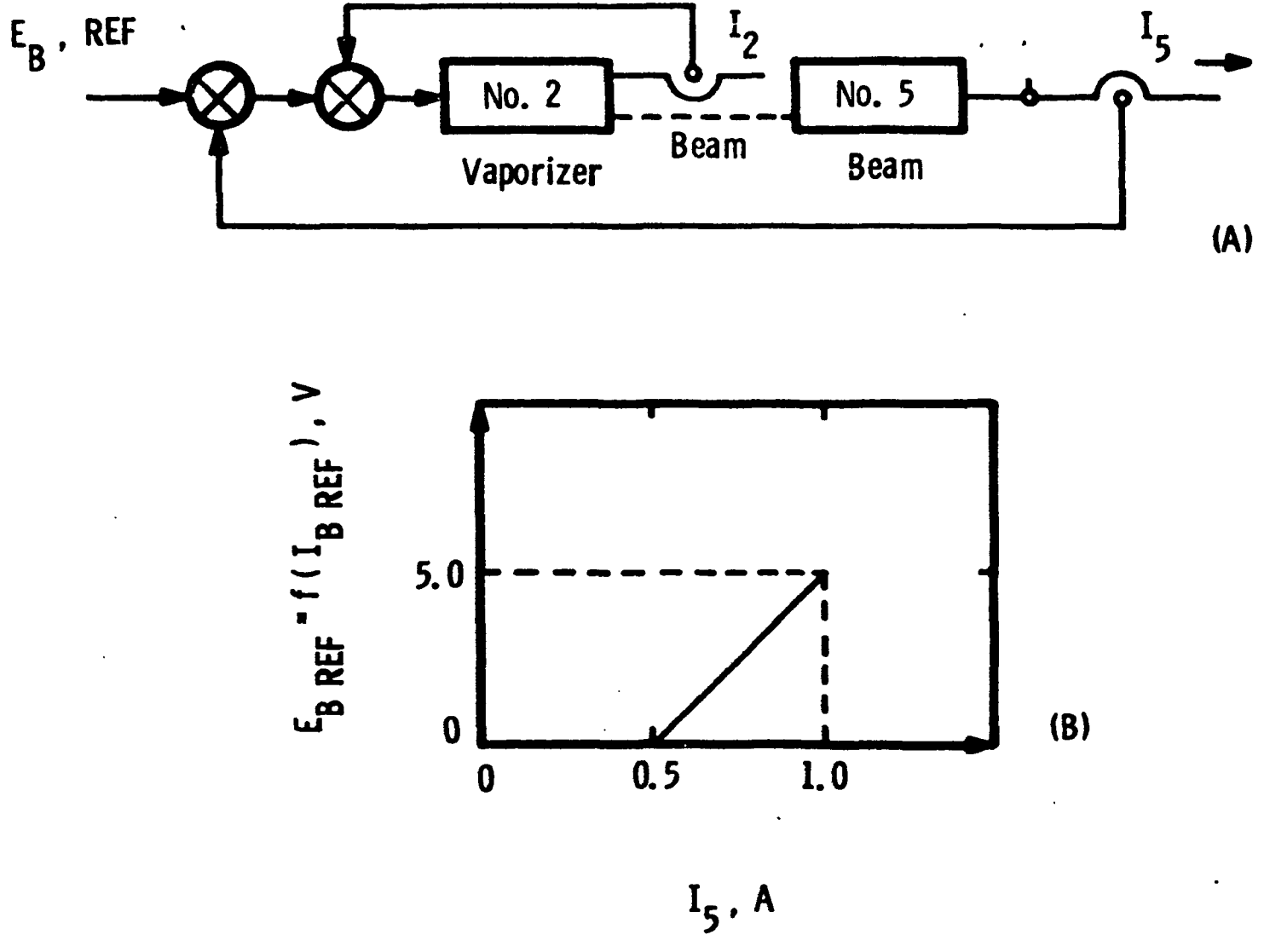


FIG. A-7. VAPORIZER/BEAM SUPPLIES CLOSED LOOP RELATIONSHIPS

A.1.1.5.2 I_{4Ref} signal will be supplied from a source similar to that described in Para. A.1.1.5.1 above. The value of this reference signal shall be continuously varied from 0Vdc (I_4 = 2A) to +5Vdc (I_4 = 9A).

A.1.1.6 Telemetry Outputs

A.1.1.6.1 Amplitude

The power conditioner shall provide telemetry signals which shall continuously and linearly represent a given parameter from -0.5Vdc to 5.5Vdc, where zero volts and 5Vdc correspond to zero and 100% points, respectively.

Telemetry signals shall not, under any condition, exceed the range -2V to 7Vdc. Noise and ripple shall not exceed ±1% RMS.

A.1.1.6.2 Source Impedance Loading

The source impedance shall be 10KΩ or less.

The power conditioner shall not be inhibited from proper operation by telemetry loads (such as a short circuit) or by externally-induced telemetry-line noise or EMI.

A.1.1.6.3 Accuracy

Calibration accuracy of ±2% of full scale setting plus an addition ±2% of the read value will be provided, with a maximum design drift of 1% over 10,000 hours of operation for all 0 to 5V telemetry signals, except as noted below.

Telemetry signals I_1, I_4, I_5, E_4, E_5 and E_6 must be of high accuracy. Over the temperature range 15°C to 75°C, these signals shall have a calibration accuracy equal to or better than one-half percent of actual value plus one-half percent of full scale for ranges specified in Table A-II.

A.1.1.6.4 Grounding

The grounds for output power, chassis, commands, and telemetry shall be separated to allow for common connection at a remote point

on the payload without the creation of ground loops. Power conditioner ground will be firmly connected to the tank ground.

A.1.1.7 Miscellaneous

A.1.1.7.1 Maximum voltage between the grids shall be less than 5KV for no-load to full load on the screen supply, and for 1mA to full load on the accelerator supply.

A.1.1.7.2 Rise time of voltages E_5 and E_6 should be as fast as feasible.

A.1.1.7.3 Toggle switches will be provided in order to modify the mechanization of the automatic recovery from an arcing (see Para. A.1.1.5) and to allow the substitution of automatic turn-on or turn-off of any of the power supplies Nos. 1, 2, and 4 with a manual one.

A.1.1.7.4 The rectifiers of the accelerator supply No. 6 will be capable of carrying the full screen current while the arcing between grids persists.

A.1.1.7.5 Because of an extremely high noise environment, great care in selection of various logic devices shall be applied. Wherever possible high threshold logic shall be used. Slow gates shall be given preference, but if not available, slowdown networks in all critical digital lines shall be added.

A.1.1.7.6 The temperature range to be covered is 0°F to 160°F on the baseplate of the P.C. chassis.

A.1.1.7.7 Temperature drift within the current sensors will not exceed $\pm$0.5% of the actual value for temperature stable region of operation. The regulation bandwidth as specified in Table 4-I will be increased accordingly.

A1.1.8 Design Criteria and Considerations

Consideration shall be given to the requirements of the over-all system at each step of the design and fabrication of the power conditioner. The Contractor should consider the following criteria, in the priority listed, in making the trade-offs required during design, manufacture, and test.

The criteria in sequence of importance are: Efficiency, reliability, and weight.

A.2 Recommended Changes to 20CM Engine Power Processor Requirements

Changes are recommended for the control of the input current to the power processors, for the outputs for the turn-on sequences, recycle procedure and for the analog control of the power processor.

A.2.1 Input

Delete last sentence of Section A.1.1.1, "In order to avoid transient overloading of the solar panel, the peak power demand shall under no condition, exceed 1.1 times maximum steady state operational power."

Add the following section to paragraph A.1.1.1, "The input ripple current reflected back to the power source shall meet the proposed narrowband - Conducted Interference limits of MIL-STD/461 Notice 3 as a minimum when operating under all conditions during startup steady-state or fault clearing and over full throttling range."

Because of the high impedance characteristics of the solar array, load dynamic changes of ion engine/power processor, will cause ac modulation of the solar array dc voltage. The input magnitude over the frequency range of 10Hz to 100kHz shall be 20V peak to peak. The input filter and power conditioning shall be compatible with this ac modulation of the input power bus and not cause out of tolerance operation, premature shutdown or component overstress.

The power processor/ion engine will be throttled so that the solar array is operating near its maximum power point. An input current limit signal will also be generated as an external command signal to the power processor so that maximum input current will always be below the maximum power point current of the solar array. During output overload or recharging of the output filter capacitor, power can be delivered at a maximum rate determined by the power stage design. Therefore an active input current limit loop must be implemented into the power conditioner design.

A.2.2 Output

Add the following paragraph at the end of Section A.1.1.2: "All outputs shall be capable of operation between no load, full load, overload or short condition without any component damage or overstress during both the transient and steady-state operation."

A.2.3 Cathode Vaporizer

The original cathode vaporizer failed open during ion engine/power processor integration testing. A new cathode vaporizer was received from JPL, that had different impedance characteristics but still requiring the same power level.

Change Table A-I Power Requirements

Supply 3 Cathode Vaporizer

Maximum Rating:

E	11V	to	18.7V
I	2A	to	1.18A

Change load resistance value from 5 ohms to 16 ohms in Section A.1.1.2.3 Cathode Vaporizer Supply No. 3.

A.2.4 Startup Procedures

Because of the integration experience of 20CM ion engine/power processor a more flexible turn-on command should be implemented. The following is the recommended changes for paragraph A.1.1.4.3. The PC shall be commanded on using the following sequence and nomenclature:

(1) On-1 Commands. Neutralizer turns on - PS7 - Neutralizer Heater, and PS8 - Neutralizer Keeper on.

(2) On-2 Commands Cathode - On - PS9 - Cathode Tip Heater, PS10 - Cathode Keeper and PS1 - Magnet Turn-on.

(3) On-3 Commands Anode - On - PS3 Cathode Vaporizer and PS4 Discharge Turn-on.

(4) On-4 High Voltage - On - PS6 Accelerator and PS5 Screen - Turn-on.

(5) On-5 Main Vaporizer - On - PS2 Main Vaporizer - Turn-on.

The time intervals between command and sequencing of commands will be determined by thruster characteristics and will be established external to the PC. Commands can be sent in any order and therefore command interlocks must not be included in the PC control system design.

A.2.5 Recovery from Arcing

Tests performed during the 20CM ion engine/power processor integration has shown another possible recycle procedure that would allow clearing without a complete shutdown of the beam/accelerator high voltage outputs.

Change paragraph A.1.1.4.5 Recovery from Arcing to as follows:

"Some of the arcs that occur within the thruster or between the thruster and the facility ground will not extinguish and must be interrupted artificially. The mechanization of PC shutdown and restart shall be as follows. Shutdown of the thruster shall be initiated by one of the overcurrent sensors on PS6 - Accelerator or PS5 Screen. After sensing an overload condition PS4 - Discharge Current Reference will be reduced to a preset current level in the range of 3 to 4A and PS2 Main Vaporizer will be turned off. If the overload clears, return PS4 Discharge Current Reference and PS2 Main Vaporizer back to normal level after 2 seconds. But if the overload lasts for a longer period (approximately 0.5 sec adjustable), turn-off PS6 Accelerator & PS5 Screen. After 0.5 sec (adjustable) turn PS6 and PS5 back on and after 2 sec. return PS4 Discharge Current Reference and PS2 Main Vaporizer back to normal, if overload is cleared."

The Anode voltage PS4 and Cathode Vaporizer PS3 control loop shall not be disabled during the overload condition.

Should the arcing and restart occur after "OFF-1" command was applied, the restarting sequence shall not nullify the command and restart PS2 Main Vaporizer.

A.2.6 Analog Control of Input Current to Power Processor

Add new Section A.1.1.5.3 as follows: "In order to control the peak current drawn by the power processor when operation with a degraded solar array and to eliminate collapse of the solar array bus and interaction with other loads, an analog signal is required to set the input current. I_{in} reference shall be derived from an external source with a maximum impedance of 1kΩ. Maximum current drain from this source

shall be less than 50μA. The value of this reference normally will be continuously varied from +1V (3A) to +5V (15A). The PC shall not respond to a reference signal greater than 5.1V.

A.2.7 Telemetry Channels

Table A-II Telemetry Data should be modified to include the 0-60V range for the discharge and the 0-300V range for the cathode and neutralizer keepers during startup.

In addition, the ion engine should have temperature sensors located on the vaporizers in order to evaluate performance of the ion engine. Changes in the operating temperature can identify vaporizer degradation and failure. The following temperature measurements should be maintained as a minimum:

Main Vaporizer
Cathode Vaporizer
Neutralizer Vaporizer

Additional temperature monitoring channels should be located in the power processor to determine baseplate temperature.

APPENDIX B

B. DETAIL BLOCK DIAGRAM OF 20CM ION THRUSTER POWER PROCESSOR

The detail block diagram for the ion thruster power processor shown in Figure 3-1 is again shown as Figure B-1.

Block diagrams are included for each power processor output and internal auxiliary power.

The command and protection system block diagrams are also described.

The power processor grounding philosophy is also discussed.

B.1 Output

All the active control loops are shown in simple block diagram form in Figure B-1, in order to show the power and command interfaces. Detailed block diagrams are given in the following sections for all the regulating loops. The ASDTIC control system is applied wherever possible to improve both regulation accuracy and regulator feedback control loop stability.

B.1.1 PS1, Magnet Supply

Figure B-2 shows the detail block diagram for the V1 supply. Constant frequency of 20KHz from the multiple output inverter excites the primary of the current transformer T_1. The main output N2 of T_1 has 2000V insulation between primary and secondary and an electrostatic shield. The primary current in N1 is transferred to winding N2 from which it flows to the output filter capacitor Co. To control the output current and voltage characteristics, shorting

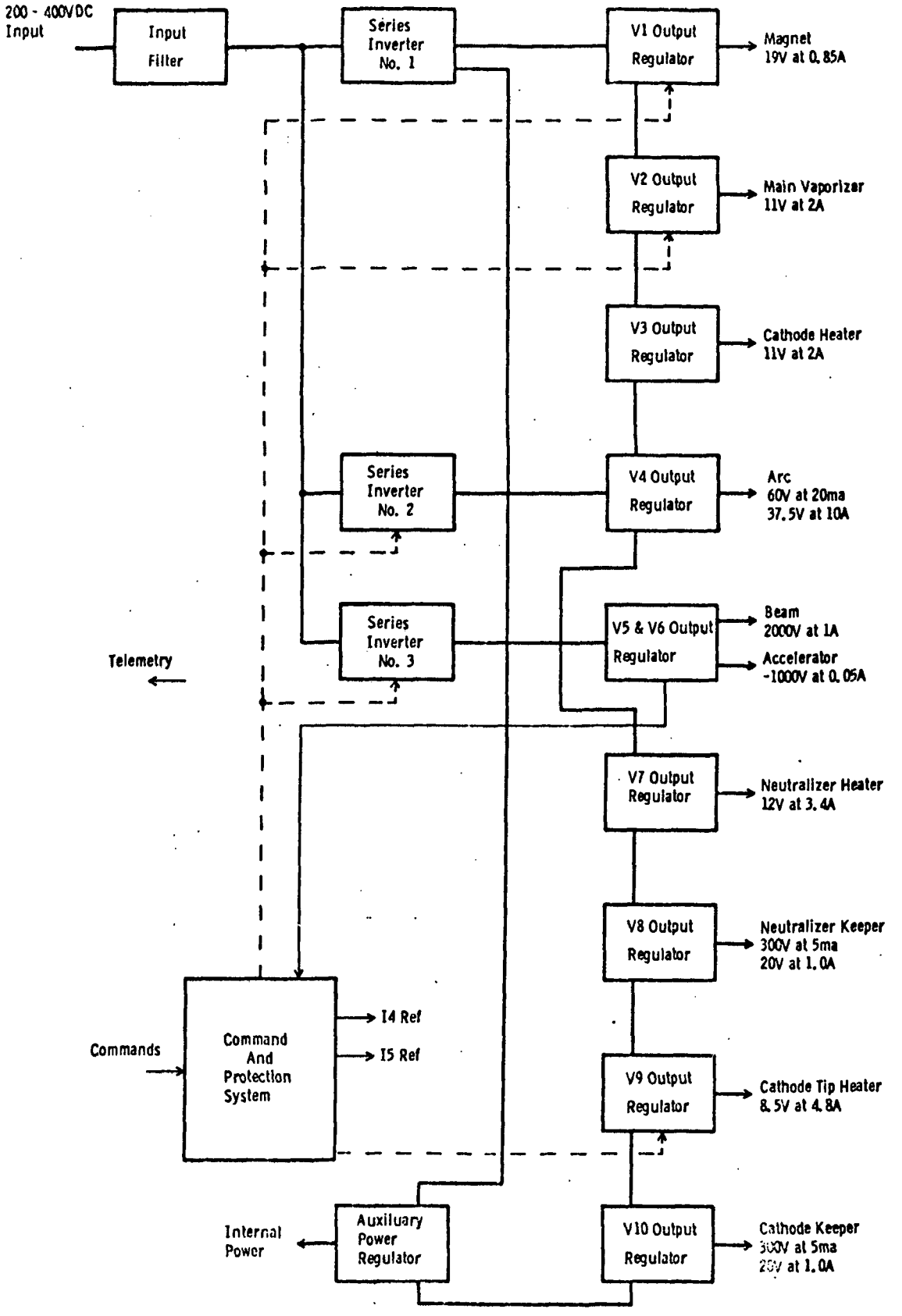


Figure B-1. Ion Thruster Power Processor Block Diagram

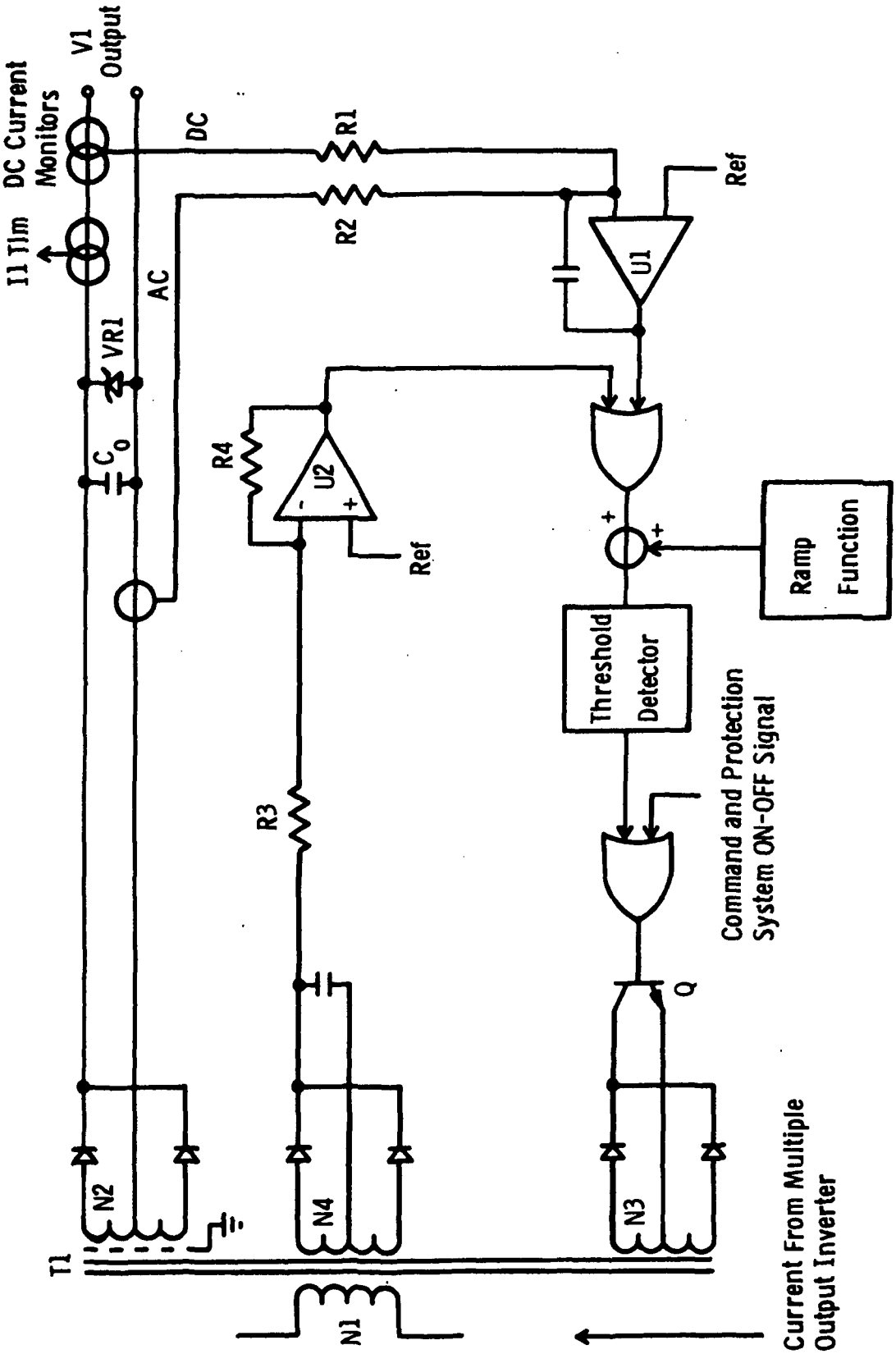


FIGURE B-2. V1 - MAGNET POWER SUPPLY BLOCK DIAGRAM

transistor Q is turned-on which places a short across winding N3 and all the secondary current flows to winding N3 and zero power is absorbed from the multiple output series resonant inverter since the reflected primary voltage is zero,except to satisfy magnetic and shorting transistor losses.

There are two regulating loops, a voltage control loop and a current control loop. The voltage loop V2 controls the maximum value of the output and commands the shorting transistor Q. The gain of the voltage loop is controlled by the ratio of R4 to R3. The current regulating loop utilizes the ASDTIC (analog signal to discrete time interval converter) principle to perform the system regulation. The ramp function is added to the output of the operational amplifier to obtain regulator stability when operating in a constant frequency system.

The primary current is converted to a dc voltage signal via the primary current transformer and integrated by the operational amplifier U1. To correct for output regulation error, a dc current transformer measures the actual output current and modifies the output of the integrating operational amplifier to meet $\pm$ 0.1% accuracy. This system allows high dc gain to be used in the amplifiers while maintaining stable regulator loop characteristics.

The command and protection system can turn the power supply off through the output OR gate.

To limit the output at no load operation a power zener diode VR1 conducts and clamps the maximum output voltage. The V1 output floats at +2kV (screen supply) and can arc over to ground. The output zener diode can pass the high transient current during a high voltage arc and protects the power transformer, output rectifiers or output filter capacitors from failure due to high voltage.

Note that all the control electronics are isolated from the V1 output by means of magnetic isolation for the output current monitors and output voltage monitors and can operate safely at ground potential.

B.1.2 PS2, Main Vaporizer Supply

Figure B-3 details the control system for the main vaporizer (PS2) power supply. This supply has three regulating loops.

- o V2 voltage limiting by means of operational amplifier U2
- o I2 current limiting by means of operational amplifier U1
- o I5 current control by means of operational amplifier U3

The first two loops are for maximum current and voltage limiting. The third loop controls the ion engine beam current flow by varying the power applied to the main vaporizer. The beam control loop gain is adjusted by changing the ratio of R5 to R4.

Power from the multiple output inverter provides the constant current source for the primary. Output voltage and current control is provided by the shorting transistor Q across winding N3. The V2 output is referenced to ion engine ground. The control electronic is again isolated and can operate at command ground which is common to the I5 reference signal ground return.

Because the V2 output is referenced to ion engine ground, the +2kV output can arc over to the V2 output and cause excessive output voltage. Output zener diode VR1 bypasses this discharge directly to ground and protects the output power components.

B.1.3 PS3, Cathode Vaporizer Supply

Figure B-4 is the block diagram for the cathode vaporizer (PS3) power supply. Transformer T2 provides 2000V insulation. The supply has three control loops.

- o V3 voltage limiting by means of operational amplifierU2
- o I3 current limiting by means of operational amplifier U1
- o V4 voltage regulator by means of operational amplifier U3

The first two loops control the maximum voltage and current output. The third loop controls the discharge voltage of the ion engine arc source by means of the cathode vaporizer output power. The gain of the V4/I3 control loop is adjusted by the R5/R4 ratio.

All control electronics can operate at ground potential.

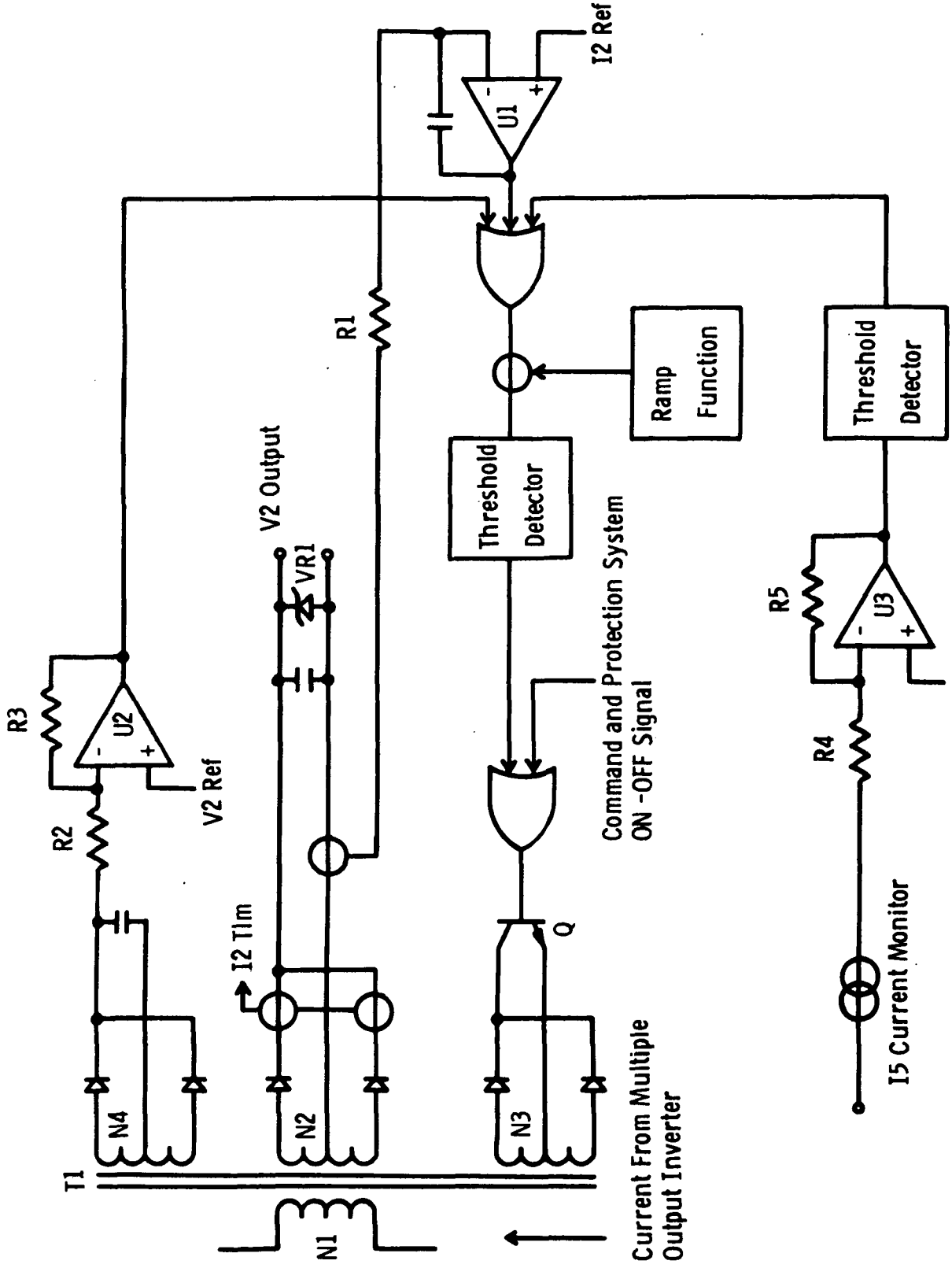


FIGURE B-3. V2 - Main Vaporizer Power Supply Block Diagram

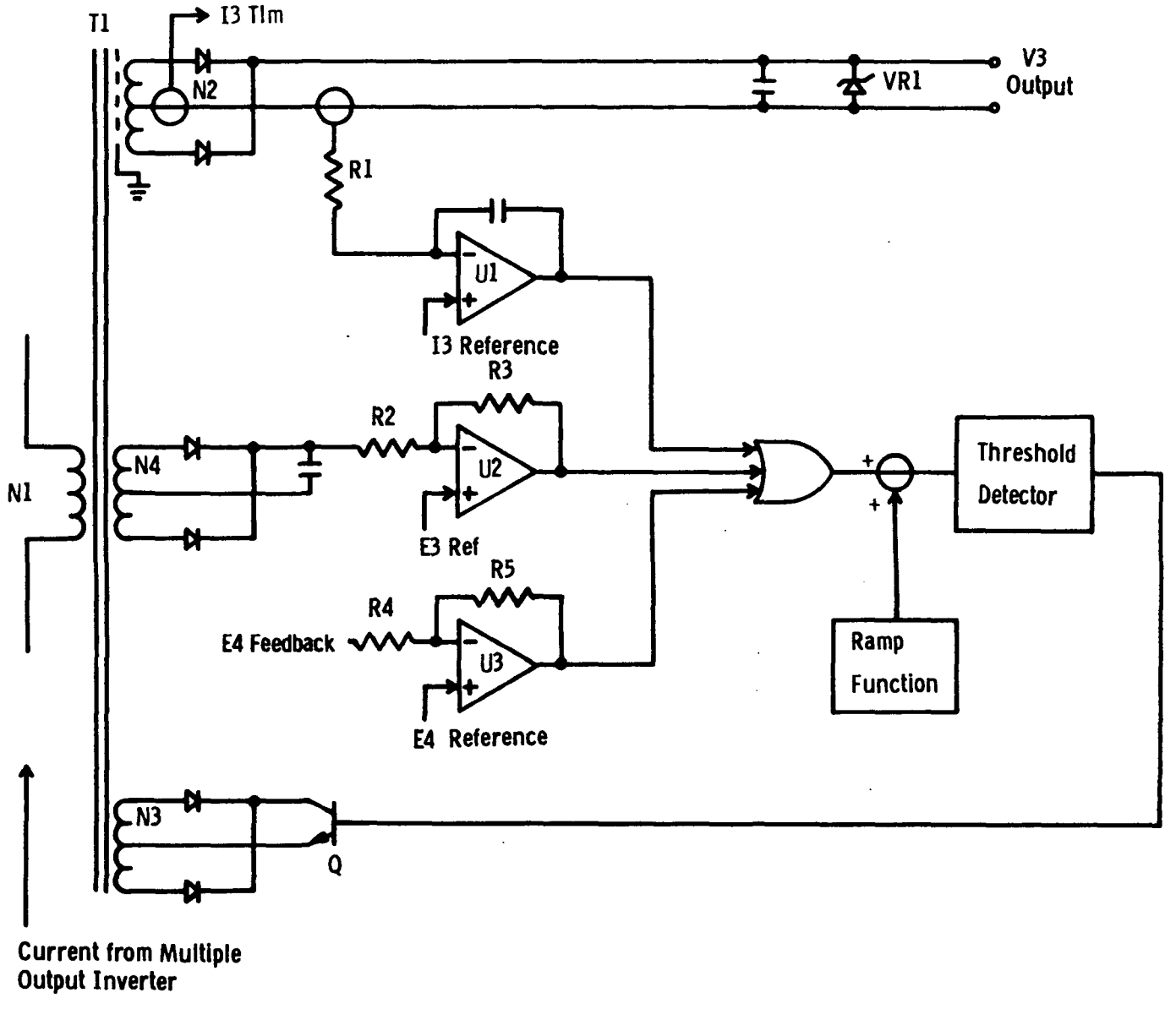


FIGURE B-4. V3 - Cathode Vaporizer Power Supply Block Diagram

Output zener diode VR1 limits the maximum no load output voltage and protects the output circuitry from overstress during arc over of the beam supply.

B.1.4 PS4, Arc Supply

Figure B-5 is the block diagram for the arc supply. The main power is obtained from series inverter No. 2 through transformer T_1.

The output winding N2 floats at +2kV beam supply output and must have the +2kV insulation between the output winding N2 and the remainder of the transformer windings. Winding N2 provides 37.5V at 10A maximum capability. Both output voltage and current is controlled by the operating frequency of series inverter No. 2.

Transformer T2 supplies the high voltage (at low current) required to ignite the arc supply. The constant current source from the multiple output inverter provides the primary energy to transformer T2. The secondary turns N2 is selected to provide 20 mA of secondary current. The output voltage is limited to 60V by the output zener diode VR1. The output zener diode limits the output overstress during beam supply arc over to ground.

The V4 discharge or arc supply has two feedback loops.

- o Output voltage limiting by means of operational amplifier U2
- o Output current regulation by means of operational amplifier U1

The first loop limits the maximum output voltage across transformer T1. The external command reference current I4 controls the operating point of the arc supply during steady-state operation. The current regulating loop incorporates the ASDTIC amplifiers for control where the secondary ac current signal is fed into operational amplifier U1, through gain adjusting resistor R2 and the dc output current signal from a two core series connected magnetic amplifier. The dc loop provides the high static accuracy and the ac loop provides regulator stability characteristic and eliminates the time constant in the magnetic current sensing amplifier.

The output of either operational amplifier operates the threshold detector depending on the mode of operation, i.e., voltage or current regulation. The signal goes through an output/input ground isolation in order to isolate the input power ground of the series inverter No. 2 control electronics and the command ground which is common to the I4 reference and the regulator control

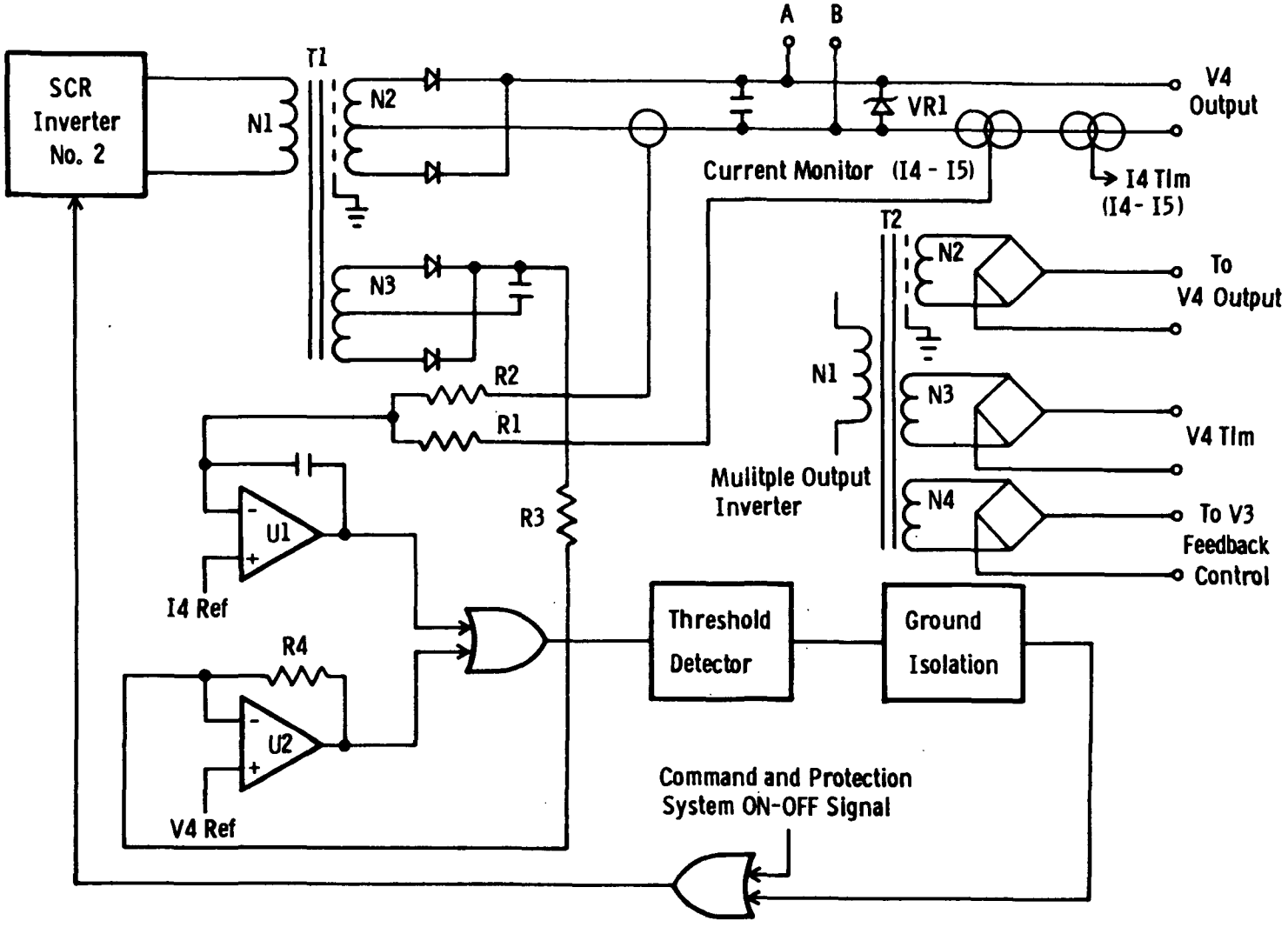


FIGURE B-5. V4 - ARC POWER SUPPLY BLOCK DIAGRAM

electronics. Here again the V4 output is floating at +2kV and all the control electronics are referenced to ground and isolation is provided by the current sensors and isolated winding N3 on Transformer T_1.

Transformer T_2 not only contains the 60V booster output, but also the V4 telemetry signal and the feedback control signal to V4/I3 engine control loop for the V3 output.

B.1.5 PS5 and PS6, Beam and Accelerator Supplies

Figure B-6 is the block diagram for V5 and V6 power supplies. Both high voltage outputs are combined into a single power stage in order to reduce overall part count. Power transformer T1 supplies +2kV at winding N2 and -1kV at winding N3. Winding N4 is used to provide output voltage indication for telemetry and provides the necessary ground isolation for the telemetry system. Output limiting resistors RL1 and RL2 control the peak current that can flow from the output filter capacitors C1 and C2. The limiting resistors not only limit the peak discharge current but also control the transient voltage that can appear on the cabling to the engine and the separation of the output ground from the engine ground during the transients.

Series inverter No. 3 supplies the total output power for this supply. Two regulating loops are included.

- o V5 and V6 output regulation by means of operational amplifier U1
- o I6 overload control by means of operational amplifier U2

The voltage regulating loop incorporates the ASDTIC control system to maintain output regulation accuracy and regulator stability. The dc loop senses the stored energy in the output capacitor C1 by means of a current transformer. The output signal from operational amplifier U1 controls the threshold detector, the input/output ground isolation circuit, and the control logic for SCR series inverter No. 3. The input/output ground isolation separate the output ground return from the input power ground return for the SCR series inverter control logic.

The I6 overload control comes into action during shorts on the V6 output and protects the winding N3 from damage since it is designed to pass only 50mA instead of 1A which is the total capability of the series resonant inverter No. 3.

No overload control loop is mechanized for the V5 output since it is inherent in the design of the series inverter control system at slightly higher than one ampere.

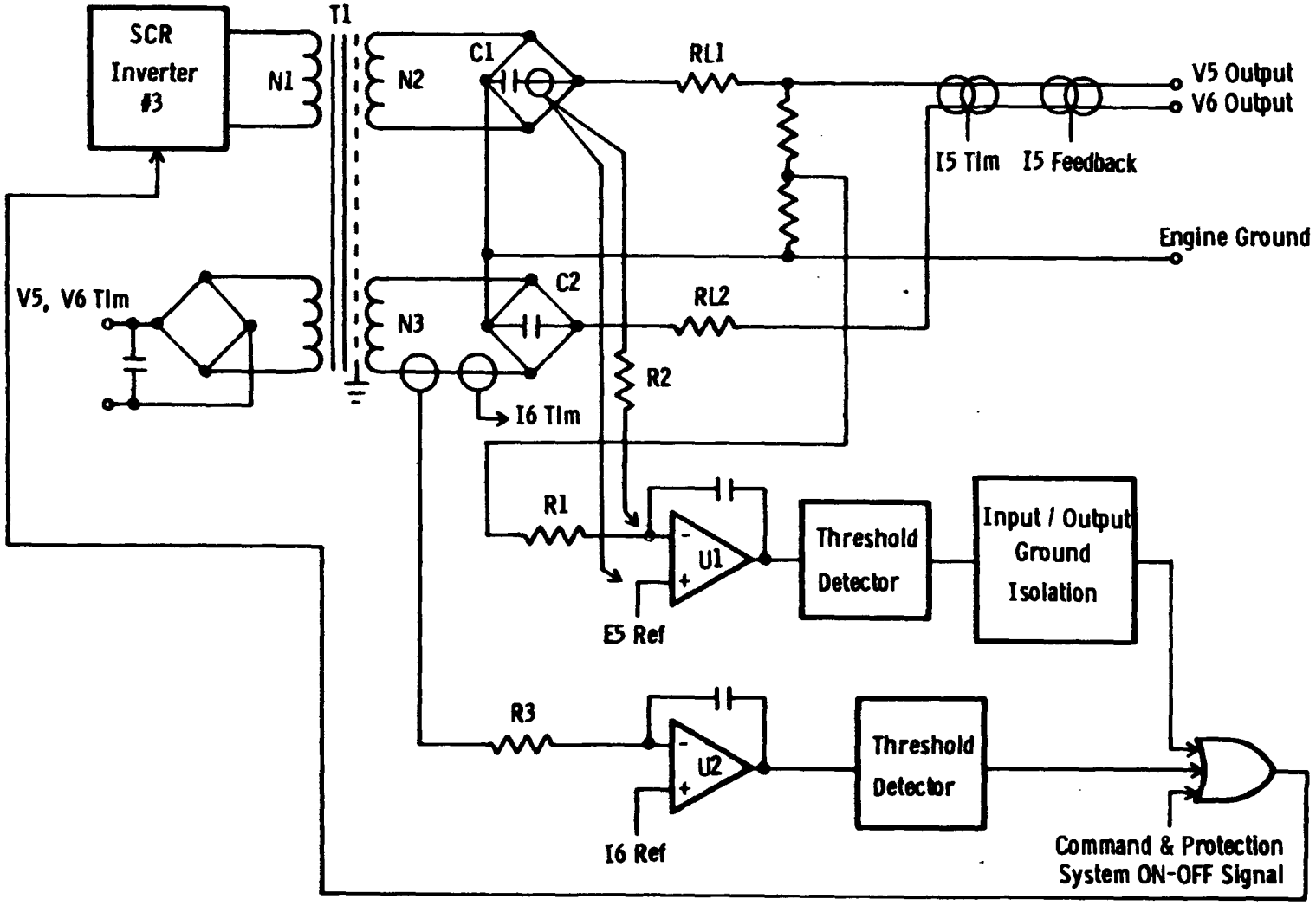


FIGURE B-6. V5 AND V6 - BEAM AND ACCELERATOR POWER SUPPLY BLOCK DIAGRAM

B.1.6 PS7, Neutralizer Heater Supply

Figure B-7 is the block diagram for the neutralizer heater supply. Constant high frequency ac current from the multiple output inverter passes through winding N1 of transformer T_1. Current transformer T_1 passes energy into winding N2 and supplies energy into the V7 output rectifier-filter circuit. To regulate the output voltage or current, winding N3 is shorted by transistor Q and zero energy is absorbed from the multiple output inverter power stage.

The control system has three separate regulating loops

- o I7 output current regulation by means of operational amplifier U1
- o V7 output voltage limiting by means of operational amplifier U2
- o V8 output voltage control by means of operational amplifier U3

The first two loops limit the maximum output voltage and current of the supply. The V8 voltage regulation loop controls the performance of the neutralizer keeper output voltage to maintain stable neutralizer operation. The gain of the engine control loop is adjusted by the R5/R4 resistor rather than by the operational amplifier U3. The ramp function generator is added to the operational amplifier outputs and provides stability for the V7 control loop.

All the electronics are isolated from the V7 output power circuitry and can allow the V7 output to float to ±200Vdc with respect to output ground, while the controls are referenced to input power ground.

Output zener diode protects the output power circuitry during arc over from the beam supply output.

B.1.7 PS8, Neutralizer Keeper Supply

Figure B-8 is the block diagram for the neutralizer keeper supply. Constant ac current from the multiple output inverter power stage feeds the primary winding on T_1, the main power transformer and T_2, the 300 booster transformer. Output energy flows into winding N2 on transformer T1 and is rectified and filtered by the output filter capacitor C1. Power regulation is performed by the shorting transistor Q across winding N3 on transformer T1.

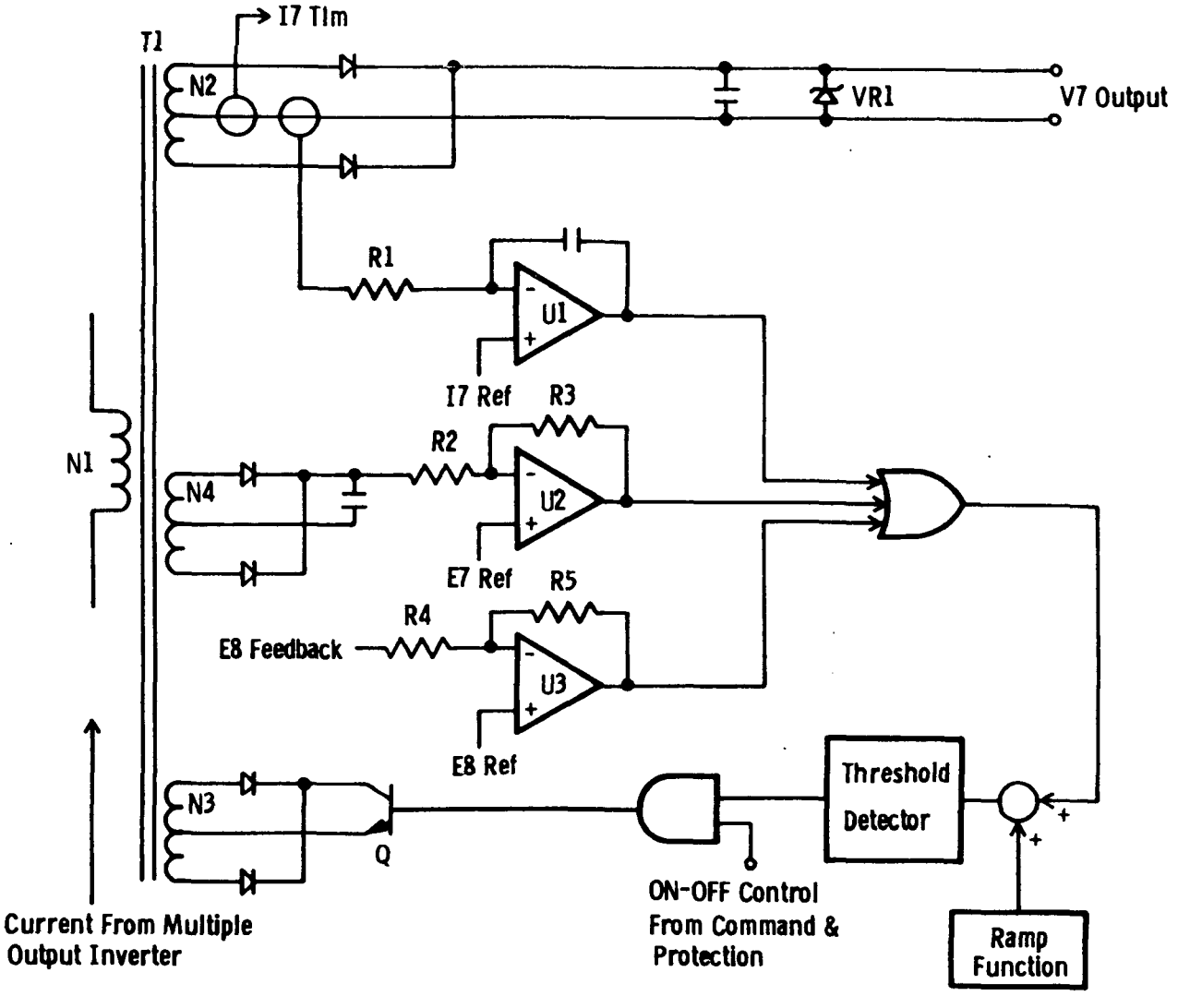


FIGURE B-7. V7 - NEUTRALIZER HEATER POWER SUPPLY BLOCK DIAGRAM

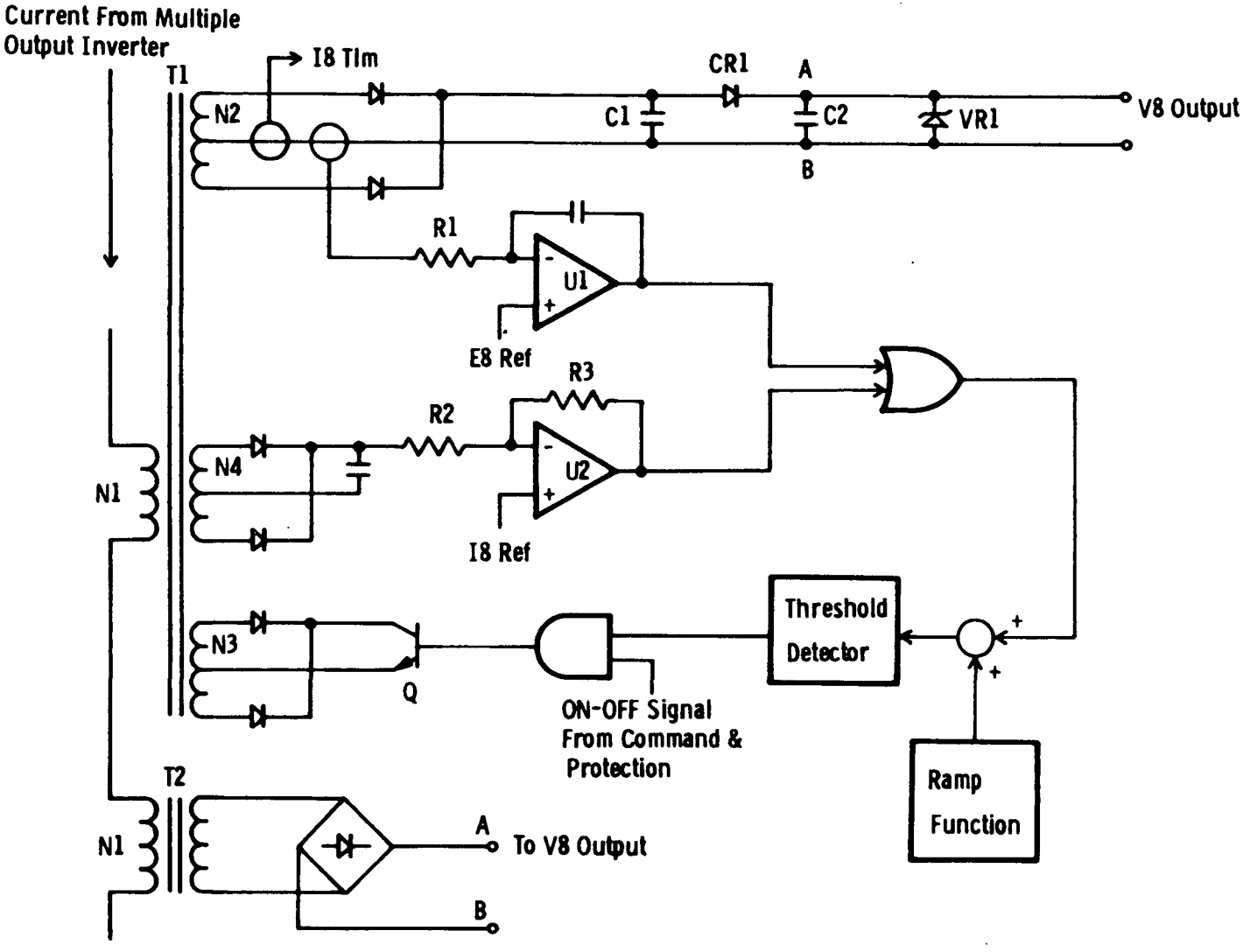


FIGURE B-8. V8 - NEUTRALIZER KEEPER POWER SUPPLY BLOCK DIAGRAM

During startup, the keeper load impedance is very high and transformer T2 supplies 20 mA average current to the output capacitor C2. The output voltage across C2 builds up until the output zener VR1 starts conducting and limits the output voltage at 300Vdc. Diode CR1 isolates the high voltage from appearing on the 20V output capacitor C1. During turn-on of the keeper supply, the output voltage makes a smooth transfer from high voltage (300V) to the low voltage high current (20 to 10Vdc). The output filtering only includes capacitance and therefore a oscillation is not set up between the negative impedance of the keeper discharge and a typical LC filter used for output filtering.

The problem with this design is that when the high voltage (+2kV at 1A) arcs over to the neutralizer keeper output and to ground, the full one amp flows in the zener diode and causes about 300W dissipation. Alternate fault protection systems must be developed for this circuit.

The control system has two feedback loops

- Output current regulation by means of operational amplifier U1
- Output voltage limiting by means of operational amplifier U2

The output of the operational amplifier and ramp function controls the shorting transistor Q to provide the necessary output control characteristics.

The control electronics are isolated from the output power and therefore allows the output to float $\pm$ 200V with respect to engine ground.

B.1.8 PS9, Cathode Tip Heater Supply

Figure B-9 is the block diagram for the cathode tip heater supply. Its design is very similar to the neutralizer vaporizer supply PS7, described in Section B.1.6, except that the V9 output must float at +2kV beam potential and that the voltage control loop for the keeper potential is eliminated.

All electronics are at ground potential since voltage isolation is provided by the magnetic voltage and current sensing.

The power transformer T_1 has a shield winding between the high voltage output and the rest of the transformer.

B.1.9 PS10, Cathode Keeper Supply

Figure B-10 is the block diagram for the cathode keeper supply. Its design is very similar to the neutralizer keeper supply V8 described in Section B.1.7, except that the V10 output must float at +2kV beam potential. The output zener diode VR1 must only pass the beam discharge current on the zener diode in the forward condition and 20mA zener diode when clamping the output at 300Vdc.

All electronics are at ground potential since voltage isolation is provided by the magnetic voltage and current sensing.

Both transformers T_1 and T_2 have shields between the high voltage winding and the rest of the transformer.

B.1.10 Internal Auxiliary Supply

Figure B-11 is the block diagram for the internal auxiliary power supply. Constant current from the multiple output series inverter passes through the primary winding N1 and feeds all the secondary load. The power transformer provides all steady state power and separates all the different ground returns for the different loads. The load includes:

1) +15V at output engine ground return
2) +15V multiple inverter logic, +15V, +5V, at input power return
3) +20V,+15V and -10V at command ground return

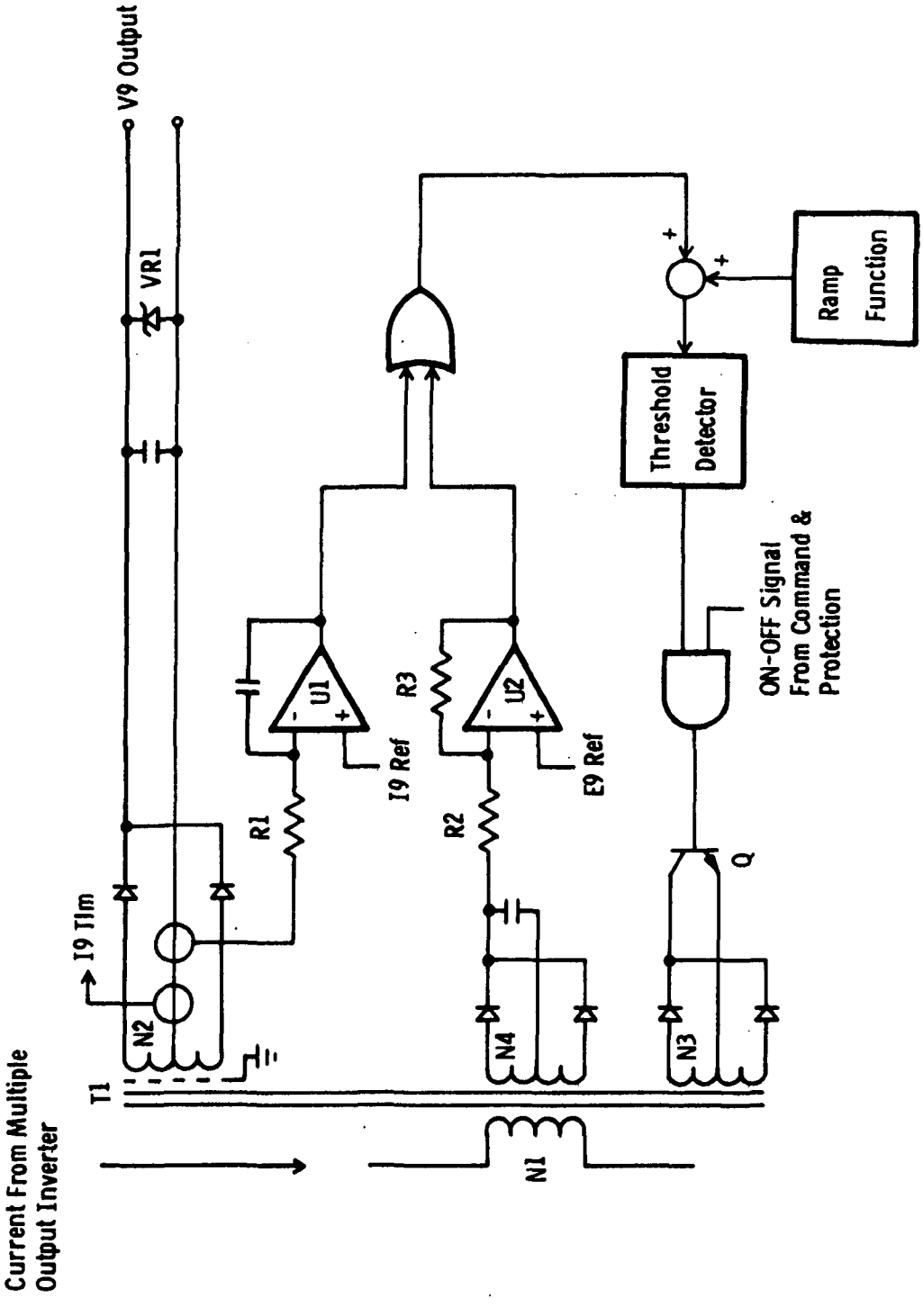


FIGURE B-9. V9 - CATHODE TIP HEATER POWER SUPPLY BLOCK DIAGRAM

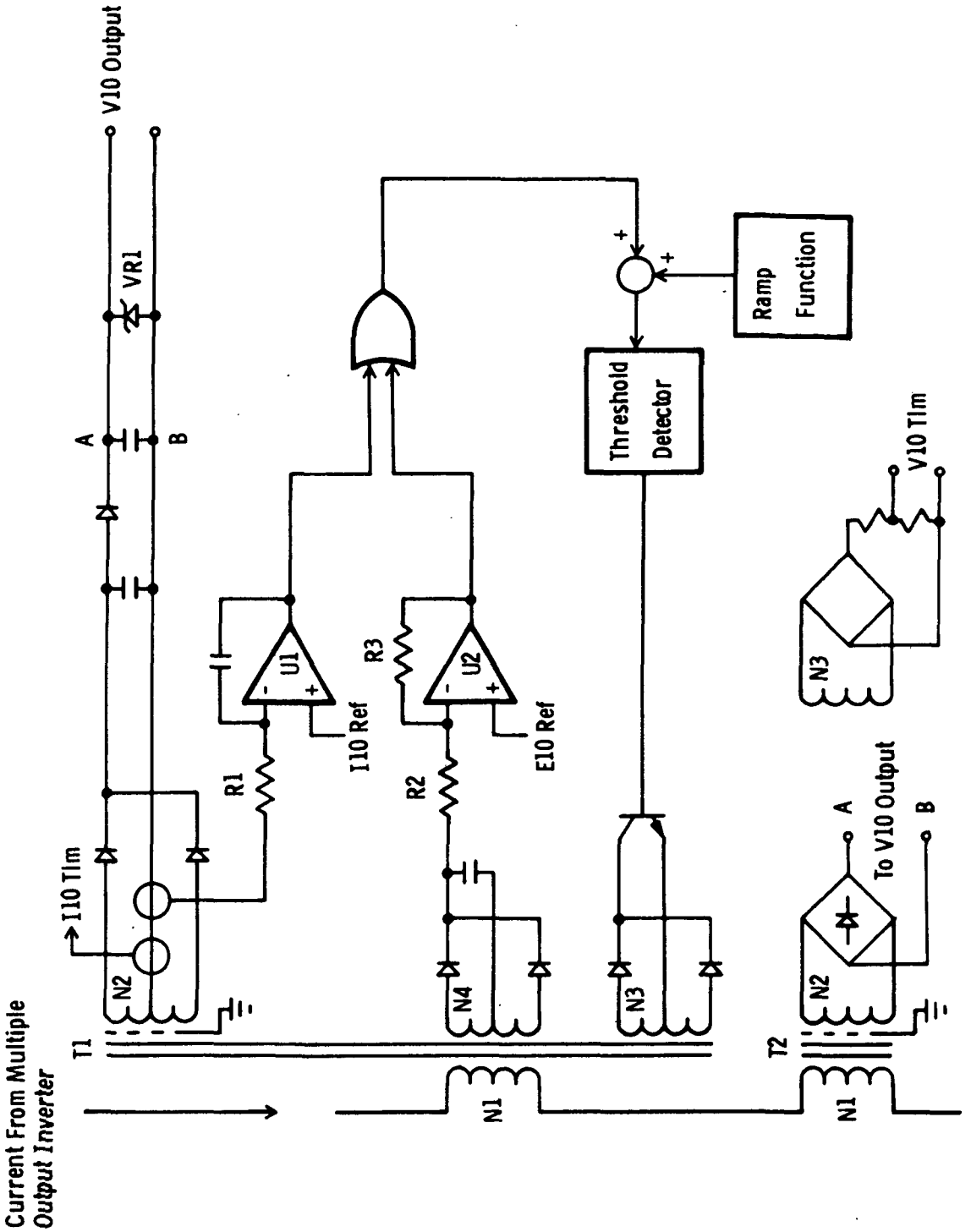


FIGURE B-10. V10 - CATHODE KEEPER POWER SUPPLY BLOCK DIAGRAM

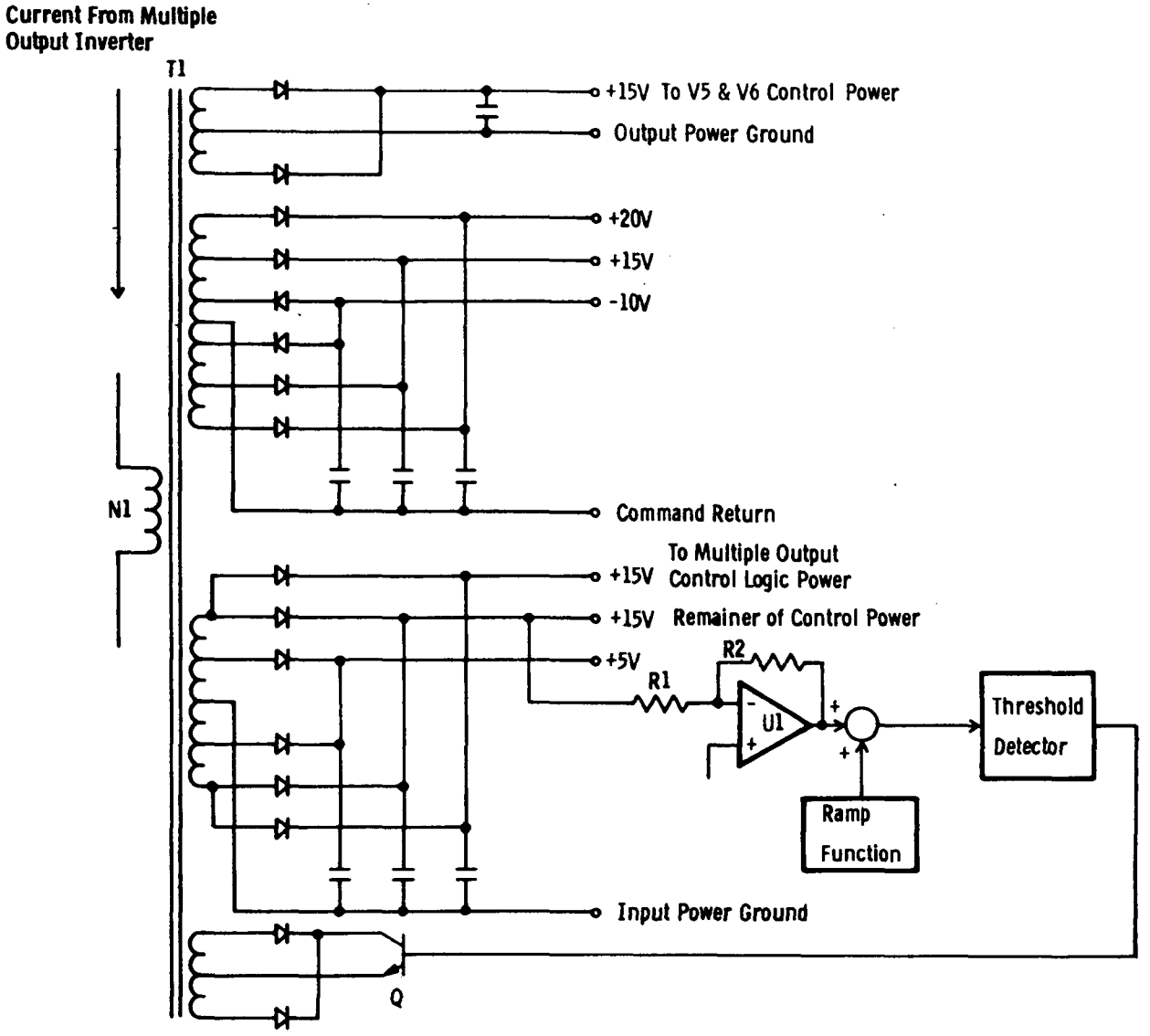


FIGURE B-11. INTERNAL AUXILIARY POWER SUPPLY BLOCK DIAGRAM

This transformer must provide adequate insulation between windings so that under transient overload conditions in the engine, separation of the grounds does not cause failure of the transformer insulation.

The regulation of the voltage is performed by the shorting transistor Q across winding N2.

Figure B-12 shows the voltage and ground returns for the different output regulators. Note all inverter control logic operates on +15V and input power ground.

Also shown on the diagram is the relative operating potentials of the different outputs to the ion engine.

B.2 Command and Protection Circuitry

The command and protection system logic block diagram has been completed, and Figures B-13 through B-15 show the detailed mechanization. Figure B-13 shows the interface between the input commands and the different circuits in the power processor.

The on-command is a signal to the start SCR in the startup circuitry shown in Figure B-13 and sets the On-1 R-S flip-flop and releases the off clamp for the multiple inverter SCR control logic and V1, V4, V8, V9 and V10 output regulators.

On-2 command turns on V3, V7 and V2 output regulators.

On-3 command turns on the V5 & V6 power supply.

The Off-1 command turns off the V2 supply main vaporizer.

Either Off-2 or input bus under voltage or overvoltage turns off the total power conditioner.

The analog signals I4 ref. and I_{Beam} ref. are level shifted from the 0-5V input to signalscompatible with the output regulators and impedance matched to provide the correct loading of the command system by the two operational amplifiers U1 and U2.

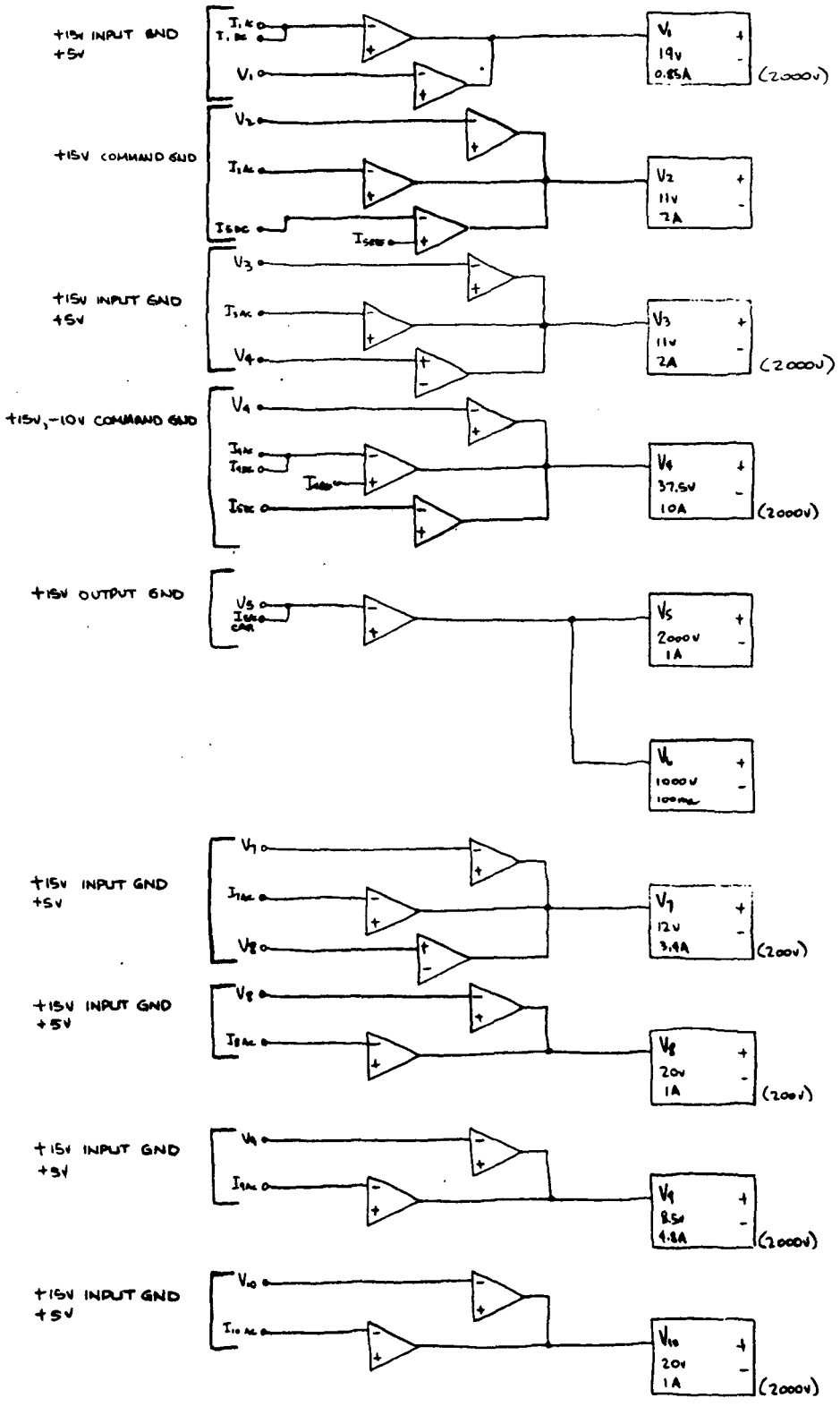


FIGURE B-12. SUPPLY VOLTAGE & OUTPUT GROUND BLOCK DIAGRAM

Figure B-14 illustrates the block diagram for the startup and emergency shutdown of the power processor.

The On-1 signal turns on SCR1 and current flows through the high impedance current limiting resistor and charges up the energy storage capacitor. When the capacitor voltage reaches about 24V, the voltage sensor turns on the series regulator and allows the 15Vdc to be applied to multiple SCR inverter control logic and the total system becomes operational because the auxiliary power supply supplied by the multiple output inverter is now operational. After a fixed time, a timer turns on SCR2 and commutates SCR1 off and current flow through the limit resistor stops.

If the voltage sensor senses less than 18V on the energy storage capacitor before the timer activates, the series regulator is turned off and the energy storage capacitor is allowed to recharge back up and a restart is attempted again at 25Vdc.

During initial start only the multiple inverter SCR control logic obtains power in order to conserve the energy stored in the energy storage capacitors.

If an external 28V supply was available from the spacecraft, this start-up system to obtain power from the 200 to 400Vdc input bus could be eliminated.

The 15V bus common to the input power ground is sensed and if below tolerance the following functions are turned off:

V1. V2, V3, V7, V8, V9, V10, Beam and Arc inverters.

The 200 to 400Vdc input bus is monitored and if an out of tolerance condition exists all three power inverters are turned off, instantaneously, to protect the power circuit from overstress and a command is sent to turn the total power processor off by means of Off-2 command in the command system.

Figure B-15 shows the fault clearing system block diagram for the power processor.

An overload on the beam or accelerator current sensor turns off the V2 main vaporizer and changes the I4 current reference for 2 sec. If the overload clears the current sensor signal disappears and V2 and I4

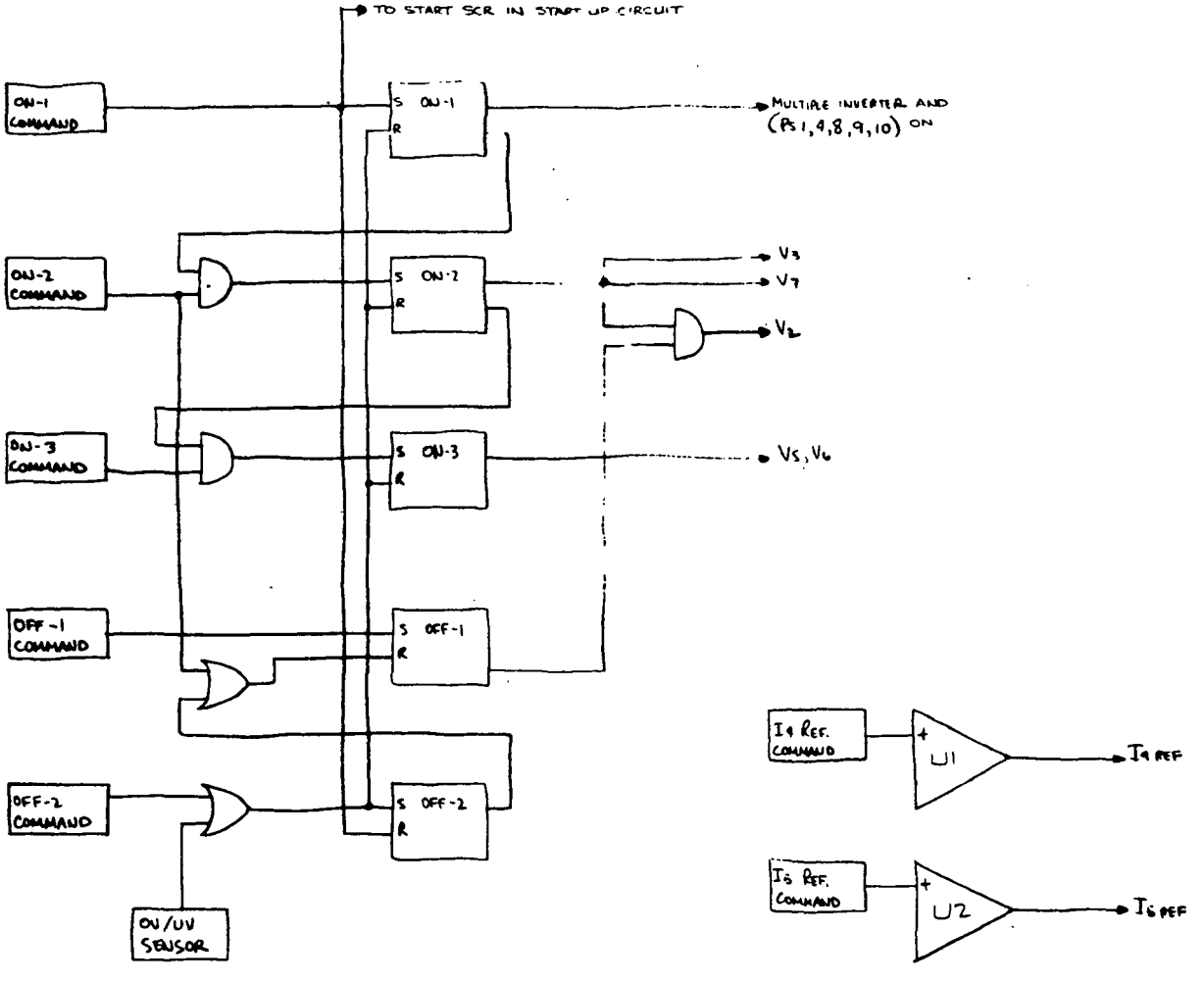


FIGURE B-13. COMMAND SYSTEM BLOCK DIAGRAM

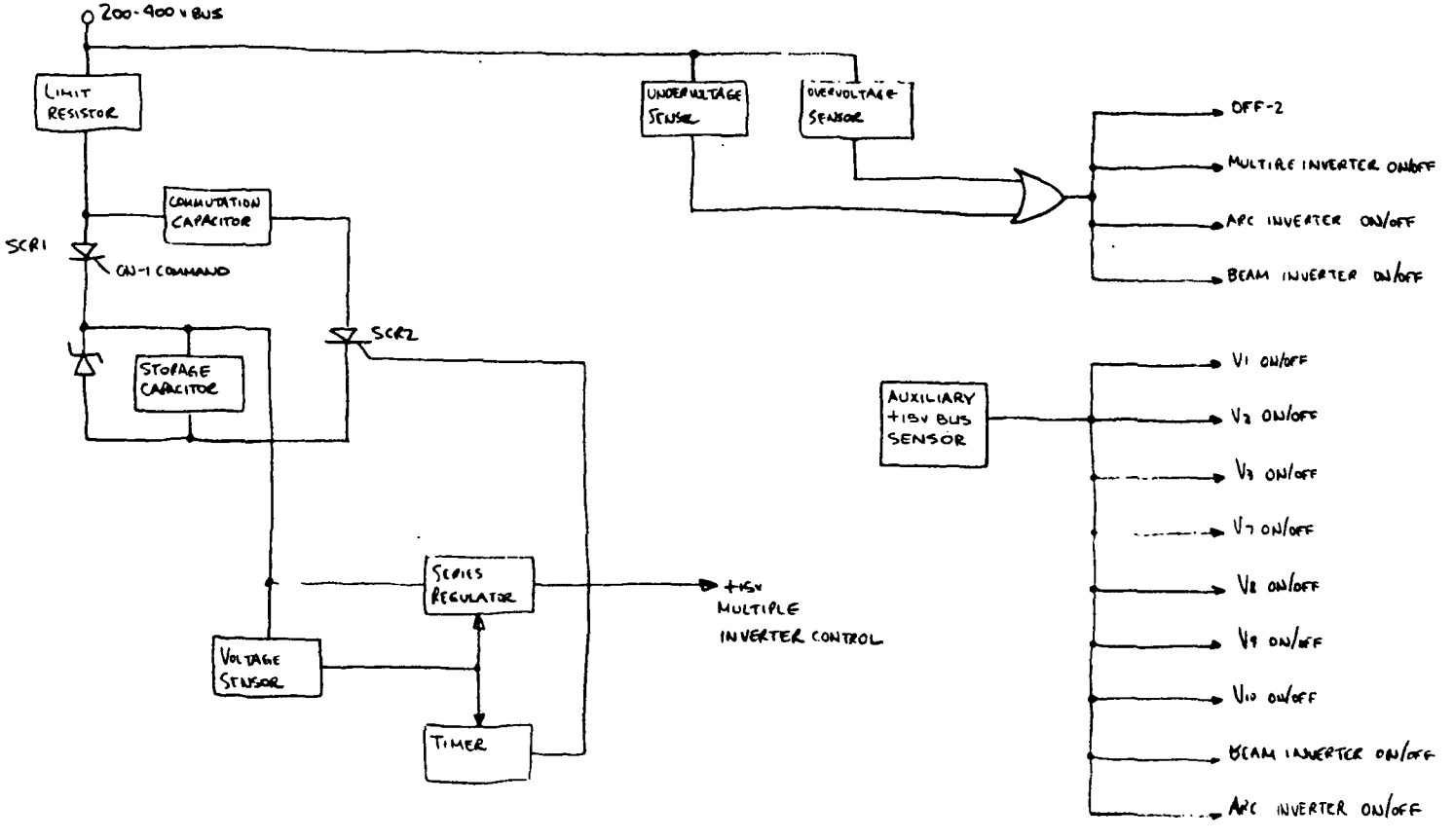


FIGURE B-14. STARTUP CIRCUIT/INPUT VOLTAGE PROTECTION BLOCK DIAGRAM

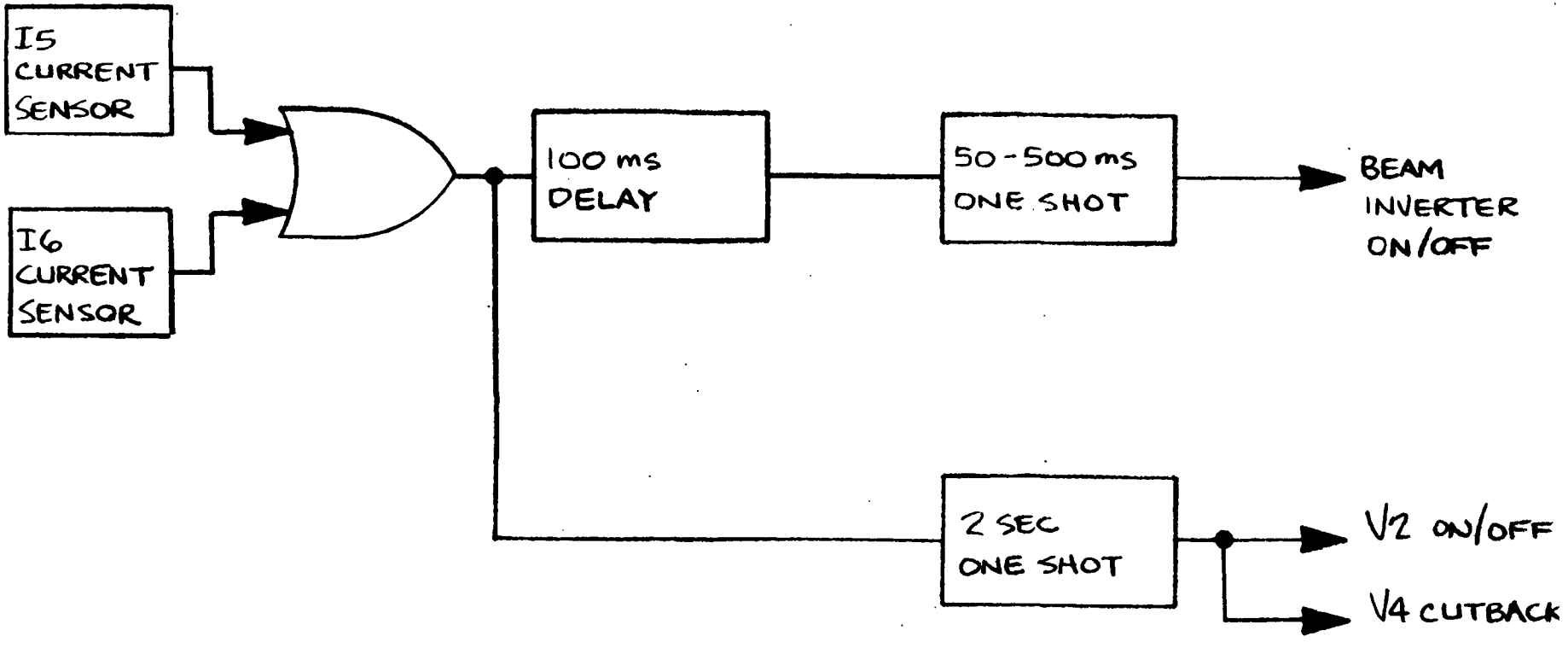


FIGURE B-15 PROTECTION SYSTEM BLOCK DIAGRAM

return back to normal after 2 sec.

If the overload lasts over 100ms the beam inverter (V5 & V6 outputs) is turned off, and after 50 to 500ms, the inverter is allowed to return back to normal operation.

B.3 System Grounding Philosophy

Figure B-16 details the grounding philosophy for the ion engine power processor. Four separate internal grounds are included in the power processor:

- o Input Power Ground (Solar Array)
- o Output Power Ground (Ion Engine)
- o Command Ground
- o Telemetry

Each ground can be connected together externally to the power processor at the power system common ground. By separating the ground returns in the power processor, ground loops cannot occur in the power processor during steady state or overload conditions of the ion engine. When overloads occur in the engine, peak currents up to 200A can be drawn from the output filter capacitor in supply V5. If this large current pulse was allowed to flow in the power processor control circuit ground returns, low level control electronics could fail or cause fault signals to be generated.

The command and telemetry circuitry ground returns are also isolated so that each subsystem can be grounded at their own outputs instead of having multiple grounding.

Both high power 2.7kW and high voltage +2kV can induce transients in the grounding system that have not been observed in the lower power spacecraft power conditioning equipment. Therefore, it is extremely important to provide this ground isolation in order to have a reliable power processor operation.

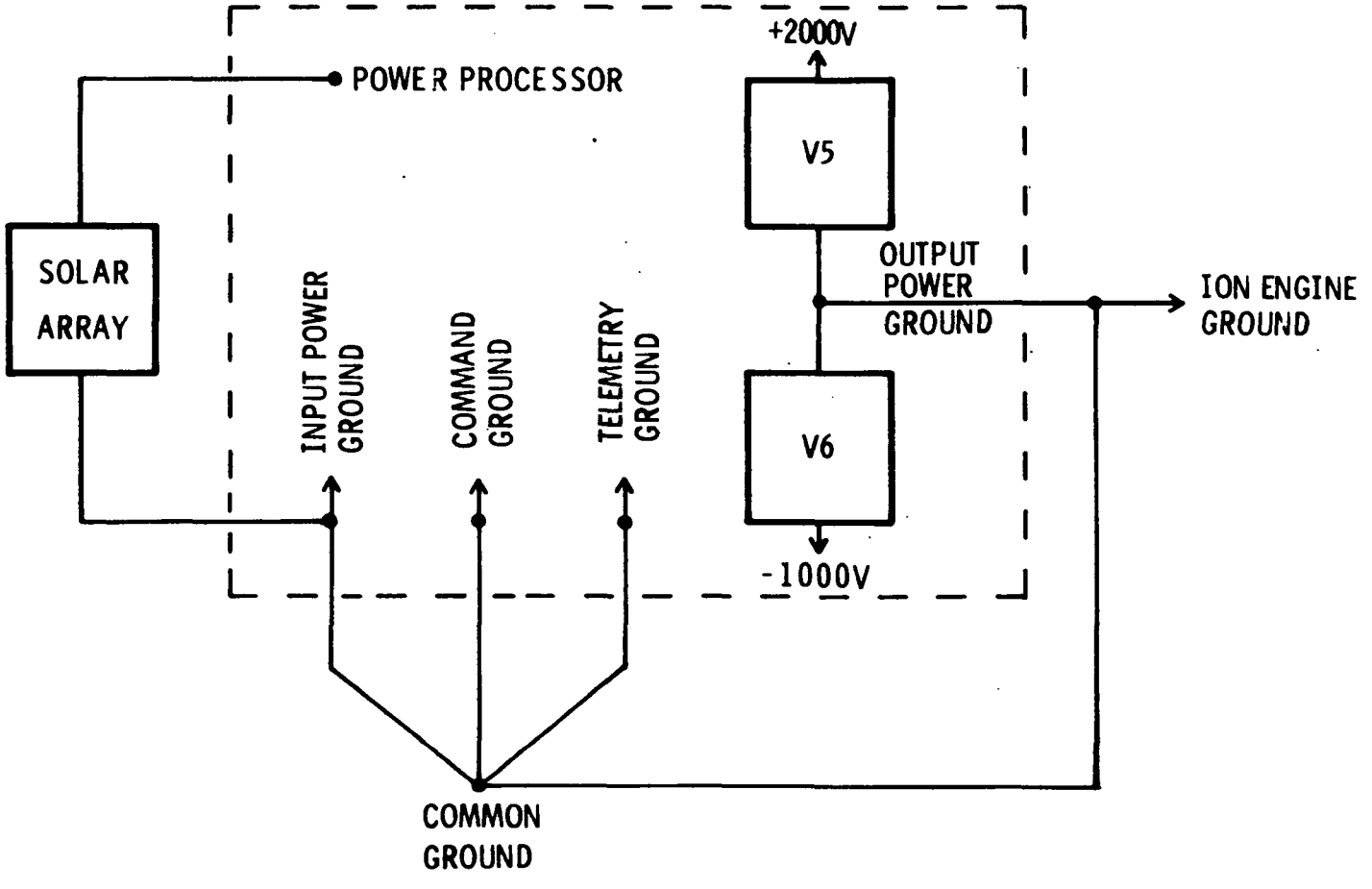


FIGURE B-16. POWER PROCESSOR GROUNDING SYSTEM

C. SCR SERIES INVERTER POWER STAGE DEVELOPMENT

In this section, the theory of operation, methods of energy control, and the configuration of the SCR series inverter stage for the 200-400Vdc bus will be discussed. The advantages of the SCR series resonant inverter will also be identified. Problem areas will also be discussed.

C.1 Basic SCR Series Inverter Operation

A dc to dc converter-regulator using an SCR series inverter as its intermediate inversion stage is shown in Figure C-1. It consists of two SCR's, SCR1 and SCR2, two identical inductors each with an inductance L, two identical capacitors each with a capacitance C, and output transformer T, a diode bridge, and a current-averaging capacitor filter C1. When an SCR is turned on, an oscillatory current flows through the series combination of L, T and C. The sinusoidal current flow, occuring at a frequency determined by the L-C components, is zero when an SCR is initially turned on, builds up to a maximum determined by the circuit design, and then returns to zero. As the current passes through zero, the capacitor is charged to a voltage higher than the supply voltage and the inductor voltage drops to zero. The sum of the capacitor voltage and transformer voltage appears as a reverse voltage on the conducting SCR during its recovery to a blocking state. Consequently, separate forced commutation circuit components are not required.

The sinewave current insures SCR operation below the maximum di/dt rating and minimizes the voltage-current product during the initial switching interval to mitigate the disadvantage of slow SCR switching. The current amplitude is changed by the turns ratio of transformer T before it is rectified and filtered by capacitor C1, which provides a low ripple direct-voltage output.

By neglecting the small resistive component inherent in L, T, C, and the source, the current flowing through the inductor and transformer, upon closure of SCR1, is given by:

$$i = \frac{V_{M1} - V_T}{\sqrt{L/2C}} \operatorname{Sin} \frac{t}{\sqrt{2LC}} \qquad (1)$$

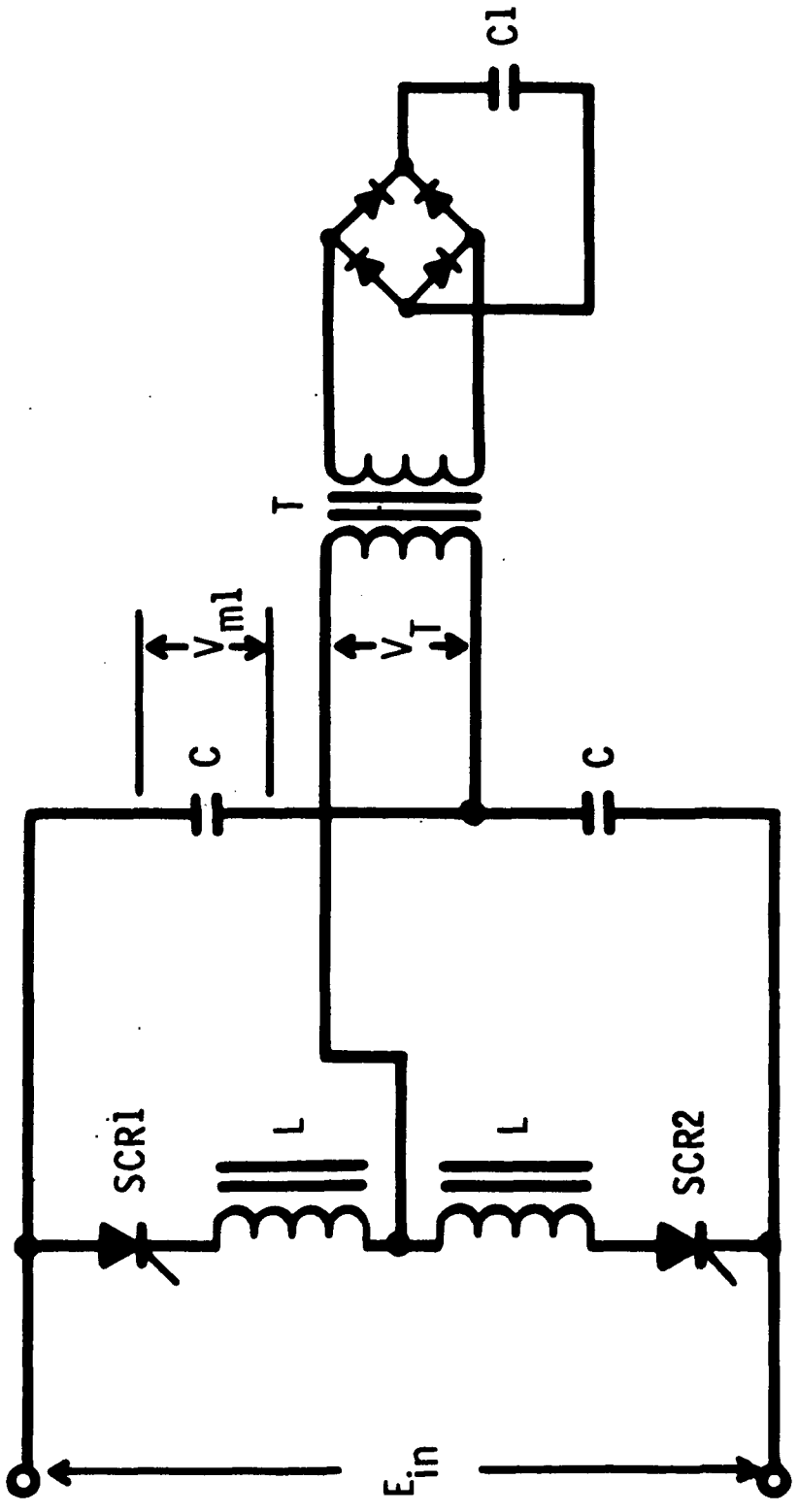


Figure C-1. Basic DC to DC Converter Using Series Inverter for Intermediate Inversion

where V_{M1} is the voltage across the upper C at time t=0 when SCR1 is turned on, V_T is the amplitude of the squarewave voltage across the transformer primary. The latter voltage is clamped at a value established by the low-ripple voltage across the output capacitor C1.

A functional subtlety regarding voltage V_{M1}, the series capacitor voltage, can be illustrated by the extreme case of an output short circuit. At V_T=0, there can be no output power. However, each sinusoidal current pulse represents a certain increment of energy derived from the power source. Since the energy not consumed by the load must be stored in the series capacitor C, voltage V_{M1} across C can build up quickly. Clearly, in order to avoid excessive voltage buildup across C, a means must be implemented to dissipate, or to return to the source, all energy not consumed by the load.

The above energy buildup phenomenon is now analyzed to gain more insight into the series-inverter operation. Let V_{01} be the initial voltage across the upper C at the beginning of the first half-cycle of conduction through SCR1. It can be shown that, during this first half-cycle, the voltage across the upper C is

$$(V_c)_1 = V_T + (V_{01} - V_T) \cos \frac{t}{\sqrt{2LC}} \qquad (2)$$

After half-cycle of conduction by SCR1, it is turned off. Following a controlled time interval, SCR2 is turned on. During this second half-cycle, voltage across the upper C can be shown to be:

$$(V_c)_2 = E_{in} - V_T - (E_{in} - V_T - V_{02}) \cos \frac{t}{\sqrt{2LC}} \qquad (3)$$

where V_{02} is the initial voltage across the upper C at the beginning of the second half-cycle (or, the end of the first half-cycle).

Starting with V_{01} and using equations (2) and (3) alternately, with their respective proper initial voltages, the voltage V_c at the end of the nth cycle can be shown to be:

$$(V_c)_n = 2n\, E_{in} - 4nV_1 + V_{01} \qquad (4)$$

or

$$\frac{d(V_c)_n}{dn} = 2(E_{in}-2V_T) \qquad (5)$$

Equation (5) indicates that:

(1) For $E_{in} < 2V_T$, $(V_c)_n$ would decrease with n, i.e., voltage across C cannot buildup. In steady-state inverter operation, $E_{in} < 2V_T$ is thus impossible.

(2) For $E_{in} = 2V_T$, $(V_c)_n$ would be identical for each n, i.e., steady-state operation can result. While this is true academically, it is nevertheless not recommended due to its imminent proximity with case (1).

(3) For $E_{in} > 2V_T$, $(V_c)_n$ would increase with n, i.e., voltage across C will buildup indefinitely until limited by dissipative inverter elements. The rate of increase is maximum at $V_T = 0$, as is evident from (5).

It can be concluded, from the above three cases that, for a series inverter to operate reliably, the following two conditions must be met: (a) V_T must be designed to be less than one-half of the minimum nominal input voltage E_{in}, and (b) a means must be implemented to limit the energy buildup in C.

C.2 Methods to Limit Energy Buildup in C

There are two basic methods for limiting the capacitor buildup:

(a) Transfer of the stored energy in the inductor to the load or to the source at a point during the half-cycle when a particular capacitor voltage level has been reached.

(b) Transfer of the excess energy stored in the capacitor to the load or to the source between the end of a half-cycle power pulse and the start of the following pulse.

1. Method (a) was used during the development phase of the Multikilowatt Ion Thruster Power Processor under Contract NAS12-2183. Figure C-2 shows the basic power circuit schematic. SCR1 and SCR2 are the main line SCR's. When a main SCR is conducting, a sinewave current is passed until the respective series-resonant capacitor (upper or lower

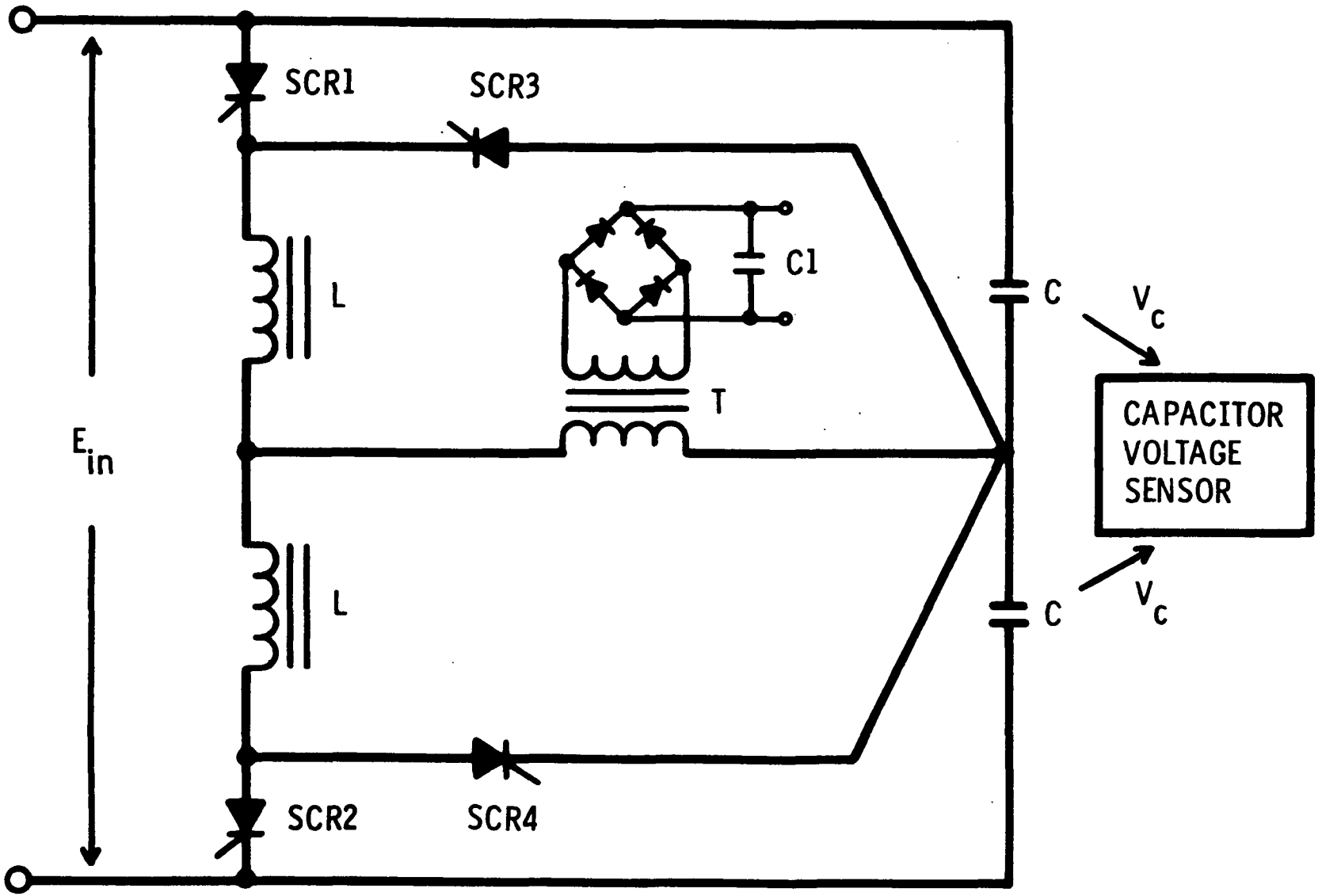


Figure C-2. SCR Series Resonant Inverter with Excessive Inductor Energy Returned to Load

C) reaches a predetermined value. The capacitor voltage sensor then fires the respective auxiliary SCR (SCR3 or SCR4), which terminates the current flow into the series capacitor and allows the inductor energy to transfer into the power transformer T. With the firing of SCR3, SCR1 is turned off as a result of a reverse bias voltage derived from the lower C. Current decays linearly to zero in L and T. SCR3 then turns off, completing one switching event.

2. Method (b) was used in the development of the 28V, 100A Army Power Supply Contract DAA B07-70-C-0245, where excess capacitor energy is transferred back to the source. Here, a simple "spill-over" network consisting of L2, D1, and D2 in Figure C-3 is added to the basic inverter. Current flow in L2 starts as soon as capacitor voltage rises higher than the bus voltage E_{in}. Energy is thus processed by L2 and the two C's and is returned to the source. Meanwhile, the capacitor voltage continues its sinusoidal rise until it passes its peak and returns to a value equal to E_{in}, when the current in L2 is at its peak value. At this time, SCR1 has been turned off completely, providing that the resonant frequency of $1/2\pi \sqrt{2L_2C}$ is less than that of $1/2\pi \sqrt{2L_1C}$. The subsequent flyback of current in L2 continues to drive the capacitor voltage until current in L2 vanishes. Detail analysis of this circuit will show that the amplitude of the current pulse is proportional to the source voltage E_{in}, and that the current in each power-circuit element is sinusoidal.

3. In addition to the two aforedescribed approaches, which have been successfully demonstrated through their respective contract fulfillment, TRW Systems has been developing additional alternatives of capacitor energy control under Contract NAS3-14383. Figure C-4 illustrates a mechanization of method (b), where excess capacitor energy is transferred to both the load and the source. Again, sinewave currents are passed in both main (SCR1, 2) and auxiliary SCR's (SCR3, 4). At the start of a switching event, the capacitor voltage sensor determines the energy level in a series capacitor. If this level is too high the appropriate auxiliary SCR is fired. Assuming the polarity shown on the two resonant capacitors, SCR4 is turned on, which circulates energy in the lower capacitor into transformer T and energy in the upper capacitor back to the source. When the voltage on the upper capacitor reaches the set value, SCR1

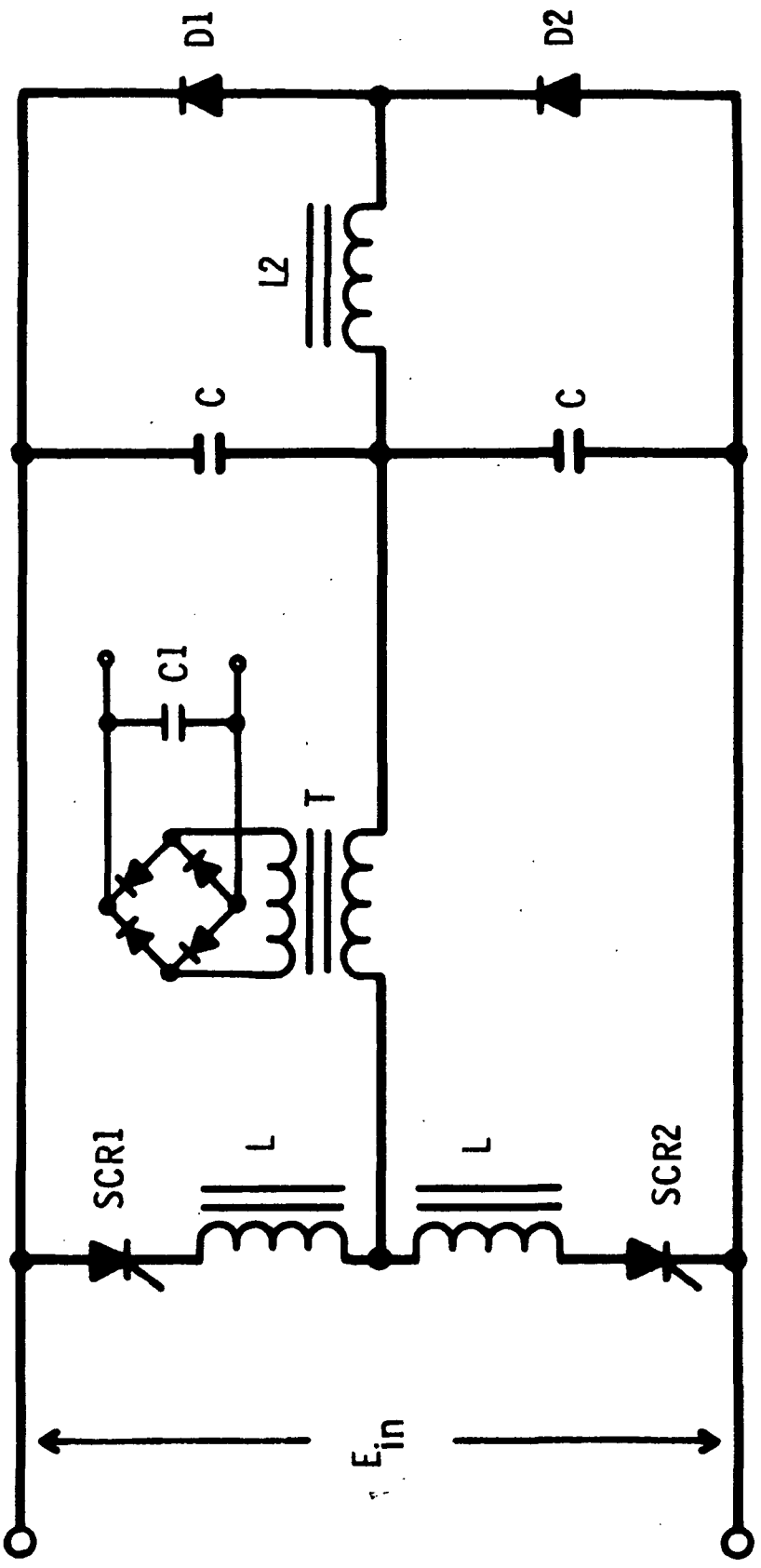


Figure C-3. SCR Series Resonant Inverter with Excessive Capacitor Energy Transferred to the Source

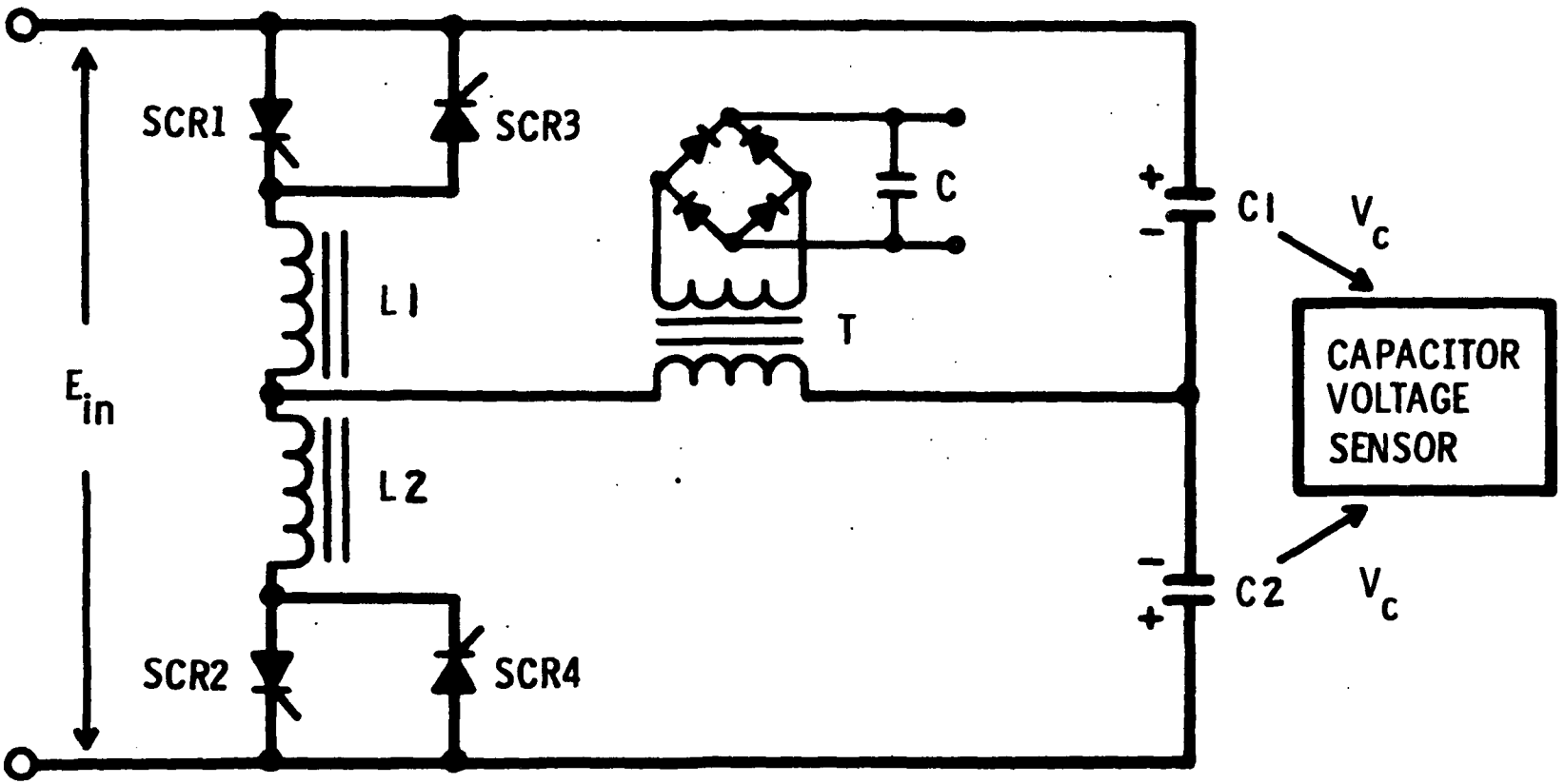


Figure C-4. SCR Series Resonant Inverter with Excessive Capacitor Energy Transfer to the Source and Load

is turned on. By controlling the firing of the main line SCR's, the peak current in the inductors and main line SCR's and the capacitor voltages are maintained under control.

C.3 System Used in Power Processor

The basic series inverter configuration used in the power processor is shown in Figure C-4. The evolution of the basic series inverter circuit to the final configuration will be discussed.

The series inverter configuration shown in Figure C-4 with the back to back parallel connection of the SCR's allows a high forward dv/dt to be applied to the non-conducting SCR when the conducting SCR turns off. The sum of the capacitor voltage and transformer voltage appears as a reverse voltage on the conducting SCR during its recovery to a blocking state. To further aggravate the condition, the reverse recovery current in the SCR turning off generates a large voltage across the inductor and that voltage added to the capacitor voltage and transformer voltage appears across the SCR's. Since the SCR's are connected back to back, forward voltage is applied to one and reverse voltage to the other.

Figure C-5 shows the next generation configuration of the series inverter. A third inductor was added to isolate the auxiliary SCR's from the main SCR's. With this configuration, the high forward dv/dt condition on the main SCR's were eliminated. The auxiliary SCR's, however, still experienced the dv/dt problem. The reverse recovery current in the auxiliary SCR turning off generates voltage across L3 which appears as a forward voltage across the other auxiliary SCR.

Figure C-6 shows the four inductor configuration of the series inverter. With inductors in series with all the SCR's, adequate isolation is achieved. The SCR's no longer are subjected to high forward dv/dt at any time.

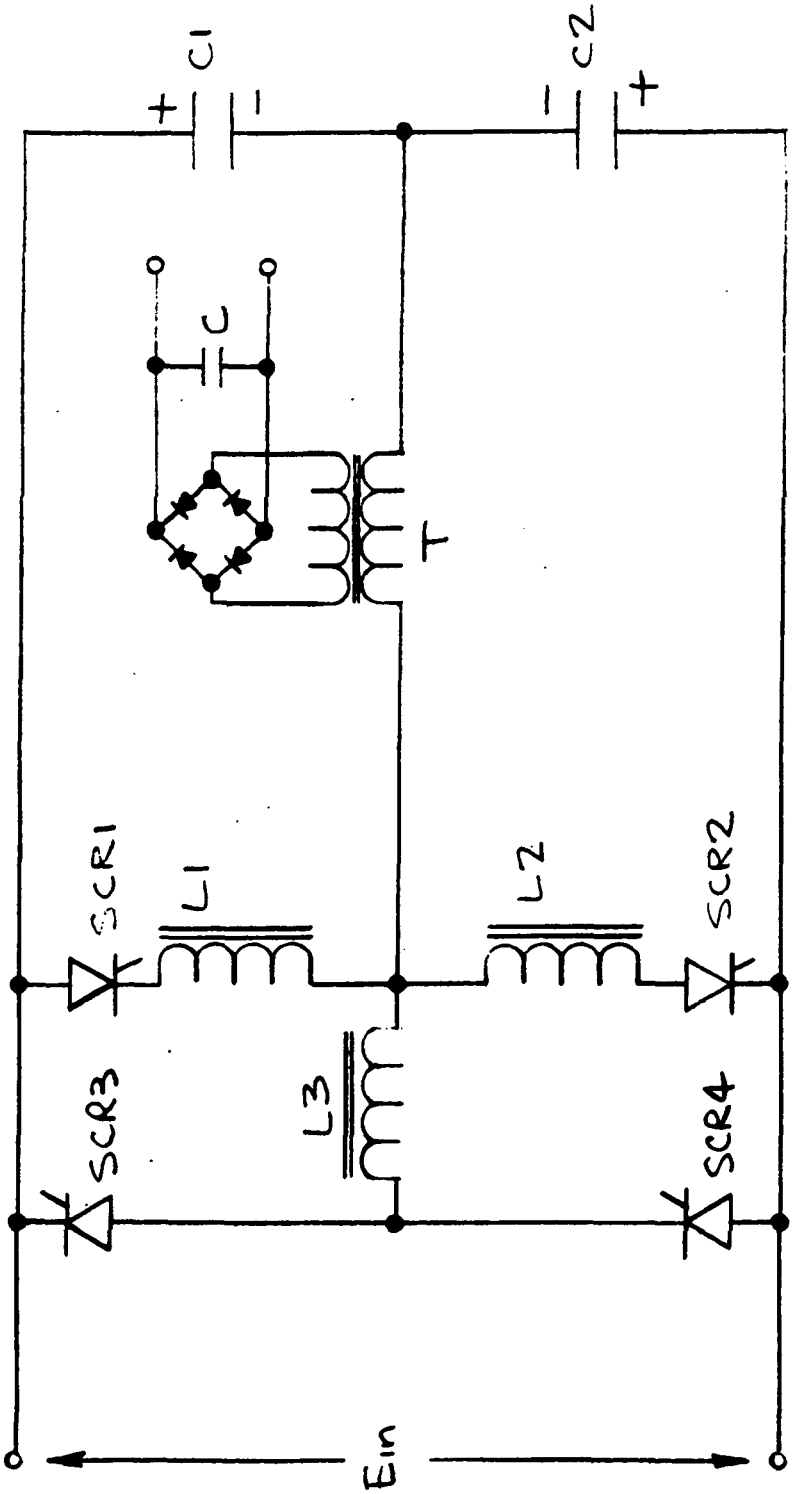


FIGURE C-5 SCR SERIES RESONANT INVERTER
3 INDUCTOR SYSTEM

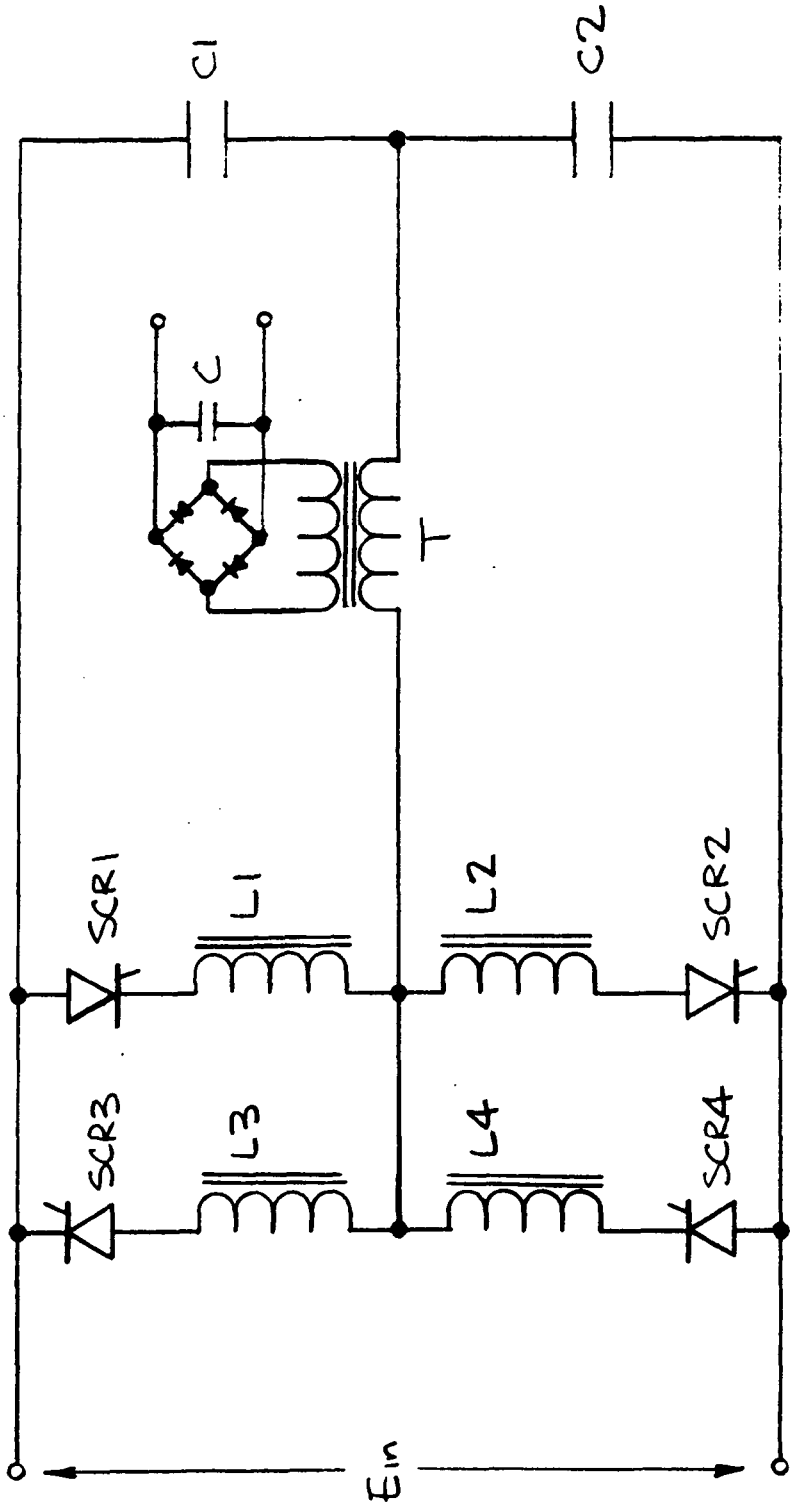


FIGURE C-6 SCR SERIES RESONANT INVERTER
4 INDUCTOR SYSTEM

Figure C-7 shows the final configuration of the series inverter. A fifth inductor was added in series with the output transformer. The fifth inductor was added to obtain better current balance between alternate half cycles under short circuit operation when the voltage across the tranformer is zero.

C.4 Problem Areas in Design

The main problem area in the series inverter design is the inability of the system to balance the currents in alternate half cycles or multiples of half cycles resulting in the generation of subharmonic oscillations.

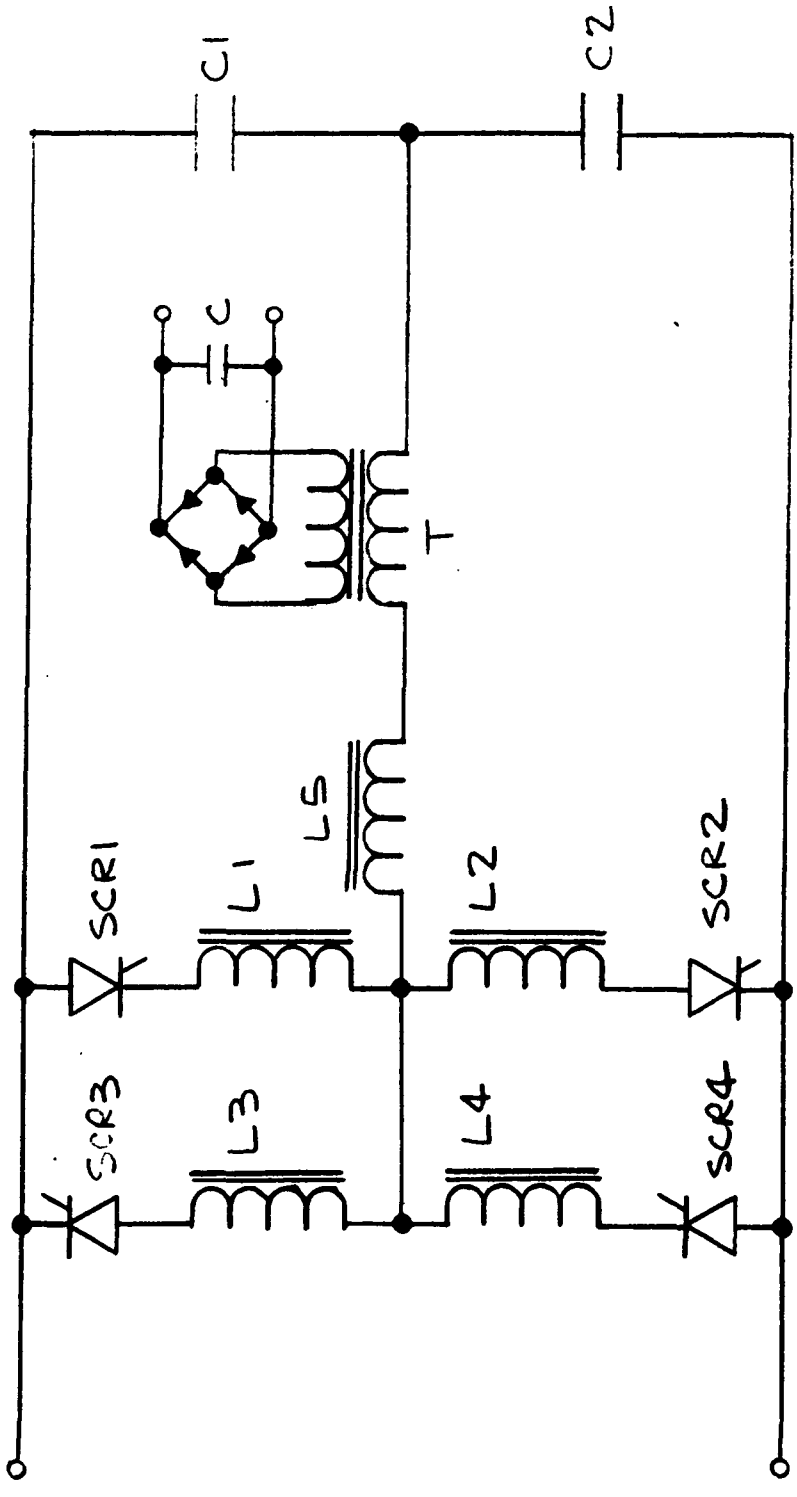


FIGURE C-7 SCR SERIES RESONANT INVERTER
5 INDUCTOR SYSTEM

APPENDIX D

D. COMPONENT DEVELOPMENT AND TESTING

A major amount of effort was spent on the power components for the 20cm Power Processor. The high power (2kW), high input voltage (400V) and high output voltage (2kV) components have not been used in previous flight space programs.

These power components greatly influence the electrical design in the following manner:

- To operate within the component rating
- Power processor efficiency due to component internal losses, both steady-state and switching
- Power processor weight to the component weight
- Insulation and thermal requirements
- Operating frequency
- Power processor reliability due to the limited component failure rate information

In order to obtain the desired system efficiency, the main series resonant circuit components such as transformers, reactors, capacitors, silicon controlled rectifiers, connecting hookup wire, terminations and input and output filtering must be as efficienct as the practical state of the art permits. To this end the component designs have been measured to determine losses and analyzed to account for losses. In the case of the magnetics certain basic experiments have been performed to understand the loss mechanism and to obtain quantitative data for design purposes. High audio frequency or ultrasonic frequency loss measurements are difficult to perform at high power AC levels because of the difficulty in obtaining the desired accuracies. The usual problems of ac loss measurements were circumvented by the simple expediency of using a low loss switching system to convert ordinary dc power into the desired ac and measuring the dc power input, thereby eliminating the subtle time and phase measurements needed for ac power determinations. This basic circuit shown in Figure D-22 to measure reactor and capacitor losses was modified to measure transformer copper losses and core losses. Two other test circuits were developed and breadboarded to obtain SCR performance data to exact usage conditions. Detailed comments on the component level are discussed below and while the comments are pertinent to all inverters, the beam, the arc, and the multiple, they relate specifically to the beam design unless otherwise noted.

D.1 Silicon Controlled Rectifiers (Thyristors)

The silicon controlled rectifier (SCR) generates the major efficiency penality in the power processor and therefore complicates the thermal and mechanical design due to the point source of heat and limited component operating temperature (125°C). It also has a high failure rate history due to the poor design application of the component in most power processing equipment. In fact during the process of testing for the SCR characteristics, the device may be subjected to conditions that can cause component damage or failure, like breakover due to reapplied forward dv/dt. Studies should be performed to identify the correct component testing, application design limits and failure modes.

D.1.1 Requirements

The SCR is used in three different series inverters with different power ratings. Its basic requirements are listed in Table D-1. These values represent the new requirements for the 30CM ion thruster power processor design and are slightly higher than in the 20CM power processor design. The major requirements for the SCR are:

(1) Forward and reverse blocking voltage
(2) Forward conduction drop
(3) Gate firing and blocking requirement
(4) Turn-off time
(5) Reapplied forward dv/dt
(6) Reverse peak current and stored charge.

The optimized requirements listed in Table D-1 result in conflicts for the SCR design. For instance, for a higher blocking voltage the blocking junction must be thicker, and therefore, the forward voltage drop is greater, the reverse recovery time is longer, and the stored charge is greater.

TRW Systems has worked with a number of SCR vendors and the devices that come closest to meeting the specification at this time are the Semicon SCRF168X for the low power requirements and the Westinghouse Electric T5070870A4AA for the high power requirements.

Table D-1

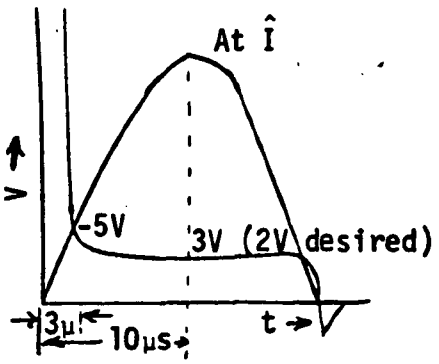
Application

- o SCR 20 kHz Series Inverters
- o Three different application power levels

Application Requirements

- o 1000V, 7μsec recovery devices at T_{case} = 90°C, T_{jn} = 100°C (Whichever more severe)
- o Efficiency in operation is of prime importance

Device Requirements

Symbol	SCR Characteristic	Requirements	Conditions
V_{DRM}	Repetative Peak off State Voltage	1000V	25°C Static DC Test 5mA limit
V_{RRM}	Repetative Peak Reverse Voltage	1000V	25°C Static DC Test 5mA limit
t_q	Turn off time	7μs	T_{jn} = 100°C dv/dt reapplied = 200V/μs
V_{FM}	Forward drop and dynamic turn on		At $\hat{I}$ 25°C

I_{pk}	Peak Current of 20μs Sine pulse	14.8A	21.4A	77A	T_{jn} = 100°C
I_o	(Max) Average Current	3.8A	5.5A	20A	T_{Case} = 90°C
I_{RMS}	(Max) RMS Current	6.6A	9.5A	34A	Whichever is Greater
Q_R	Recovered Charge, Max.	.25μcoul	1μcoul	2.0μcoul	

($\frac{dI}{dt}$=2.5A/μs $\frac{dI}{dt}$=3.5A/μs $\frac{dI}{dt}$=12A/μs)

Symbol	SCR Characteristic	Requirements	Conditions
dV/dt	Reapplied Critical Rate of Forward Voltage Rise	200V/μs	T_{jn} = 100°C
dV/dt	Static Critical Rate of Forward Voltage Rise t > 2tq	400V/μs	T_{jn} = 100°C
dI/dt	Critical Rate of Rise of On State Current	100A/μs	T_{jn} = 100°C
V_{GT}	Gate Voltage	1A pulse ≈ .3μs rise, 10μs long	
I_{GT}	Gate Current	From 15V source	ADVISE IF NOT SUITABLE
I_H	Holding Current	Generally not critical	ADVISE SUITABLE VALUES
I_L	Latching Current		

D.1.2 SCR Test Circuits

Test circuits had to be designed and built in order to evaluate SCR parameters. These included both static and dynamic type testers.

a. Static Breakdown Tests

Figures D-1 and D-2 illustrate the SCR test circuits used to evaluate the forward and reverse blocking characteristics of the power SCR's.

In Figure D-1, the high voltage DC power supply is connected in series with a current limiting resistor and the test SCR. The power supply voltage is increased until forward breakdown occurs.

In Figure D-2, the high voltage DC power supply is connected in series with a power resistor and a current meter. In this test, the reverse leakage current of the SCR is monitored.

b. Dynamic Tester

Figure D-3 illustrates the SCR test circuit developed by TRW Systems to subject the SCR to operating conditions closely simulating the Series Resonant Inverter Operation. This tester is a further development of the tester developed under contract NAS12-2183.

In this circuit, the test SCR is connected in series with capacitor C and power inductor L1, and sine current pass through the inductor, capacitor, and test SCR. Under this condition, the forward dynamic voltage characteristic and the reverse turn-off current can be monitored. By changing the resonant elements L and C the current pulse period and current magntiude can be varied over a wide range.

The pulse firing circuits for the SCR's used in this tester use high threshold logic to generate a squarewave firing pulse to the SCR's gate circuit. The output transistor stage driving the pulse transformer has an emitter resistor to control the gate current accurately for wide variation in gate impedances. In this circuit configuration, the digital logic generates the currect pulsewidth and the current drive source generates the correct rise time and current amplitude to the SCR Gate.

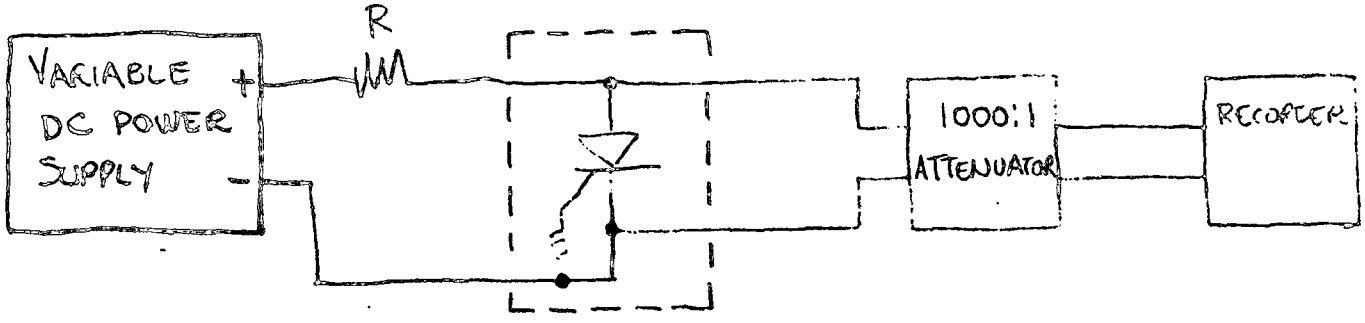


Figure D-1. Test Setup for Forward Breakover Voltage Measurement

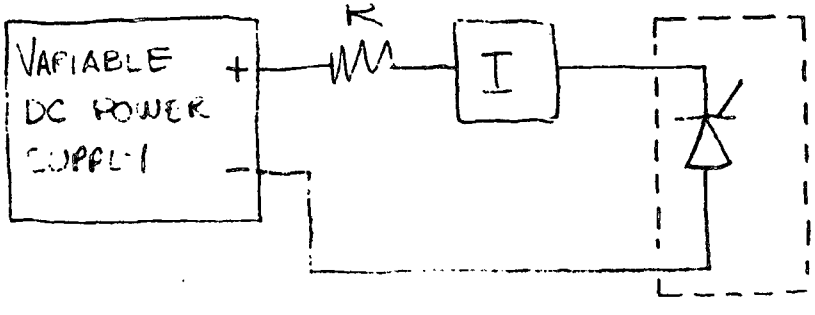


Figure D.-2. Test Setup for Reverse Leakage Current Measurement

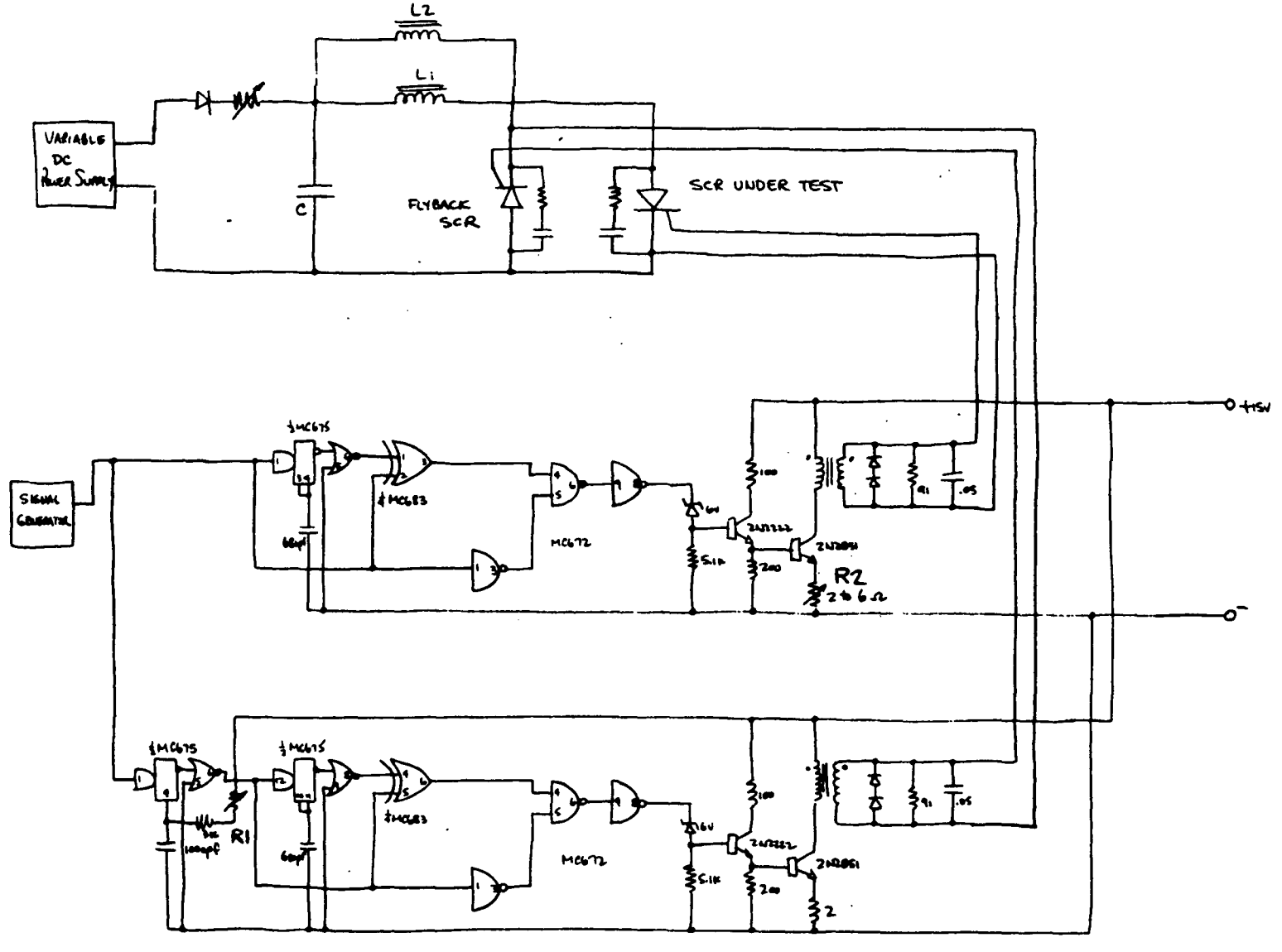


Figure D-3

SCR TESTER.

10-27-71

The flyback SCR is fired through inductor L2 and returns the energy of C to its original condition. By controlling the firing of the flyback SCR by R1, the turn-off time of the test SCR can be evaluated. By varying the value of L2, the forward dv/dt rating of the test SCR can also be tested.

Figure D-4 is the basic test circuit received from Westinghouse to test SCR turn-off time and forward dv/dt characteristics. This tester is used to check the manufacturer's component ratings. Figure D-5 is the digital logic circuitry to generate the SCR firing pulse width and the sequencing of the different power SCR's.

D.1.3 SCR Test Data

a. Static Characteristics

Figure D-6 and D-7 show the forward static characteristics for two different units of the Westinghouse High Frequency SCR Part No. 5070870A4AA, as a function of SCR temperature using the test circuit shown in Figure D-1. These units have a voltage rating greater than 1000V at operating temperatures of +125°C which is greater than the manufacturers rating of 800V.

Figure D-8, -9 and -10 show the SCR's leakage as a function of temperature and reverse voltage for a sample set of units using the test circuit shown in Figure D-2. The unit's reverse voltage characteristic was also determined at +125°C.

b. Dynamic Characteristics - Westinghouse Type 507

In order to evaluate the devices for compliance to the requirements at 125°C and at room temperatures several testers were developed. The circuits of these testers are shown in Figures D-3, -4 and -5. Figure D-11 show a typical SCR voltage and current relationship as a function of time using test circuit in Figure D-3. The saturated SCR voltage drop cannot be monitored accurately in this waveform. The saturated drop is extremely important in that it is the predominate efficiency loss. The L_1 C parameters are varied in such a fashion (large C, small L_1) that high peak current with the correct pulse period can be obtained with low input DC supply voltage.

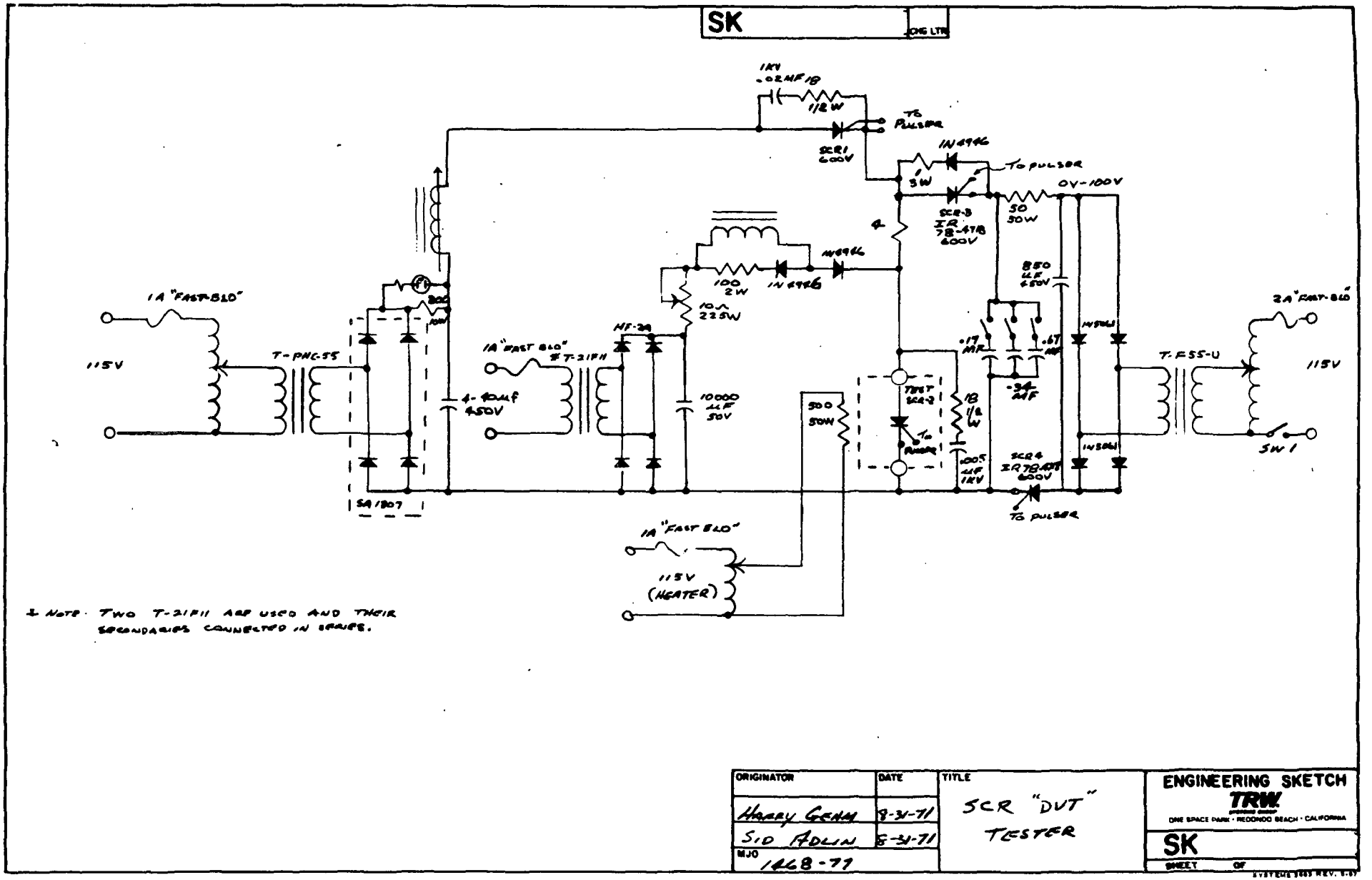

SK
1KV .02MF 1B
1/2 W
TO PULSER
SCR1 600V
IN4996
1 5W
TO PULSER
0V-100V
50 50W
SCR-3 IR 78-47B 600V
4
IN4996
100 2W
IN4996
10Ω 225W
850 UF 450V
.17 MF
.67 MF
.34 MF
INSULI
INSULI
INSULI
1A "FAST-BLO"
115V
T-PNC-55
SA1807
4-40MF 450V
1A "FAST BLO"
T-21P11
HF-24
10000 UF 50V
500 50W
TEST SCR-2
TO PULSER
18 1/2 W
1005 UF 1KV
SCR4 IR 78-47B 600V
TO PULSER
T-F55-U
2A "FAST-BLO"
115V
SW 1
1A "FAST BLO"
115V (HEATER)
1 NOTE: TWO T-21P11 ARE USED AND THEIR SECONDARIES CONNECTED IN SERIES.
ORIGINATOR
HARRY GENN
SID ADLIN
DATE
8-31-71
8-31-71
MJO 1468-77
TITLE
SCR "DUT" TESTER
ENGINEERING SKETCH
TRW
ONE SPACE PARK · REDONDO BEACH · CALIFORNIA
SK
SHEET OF

Figure D -4

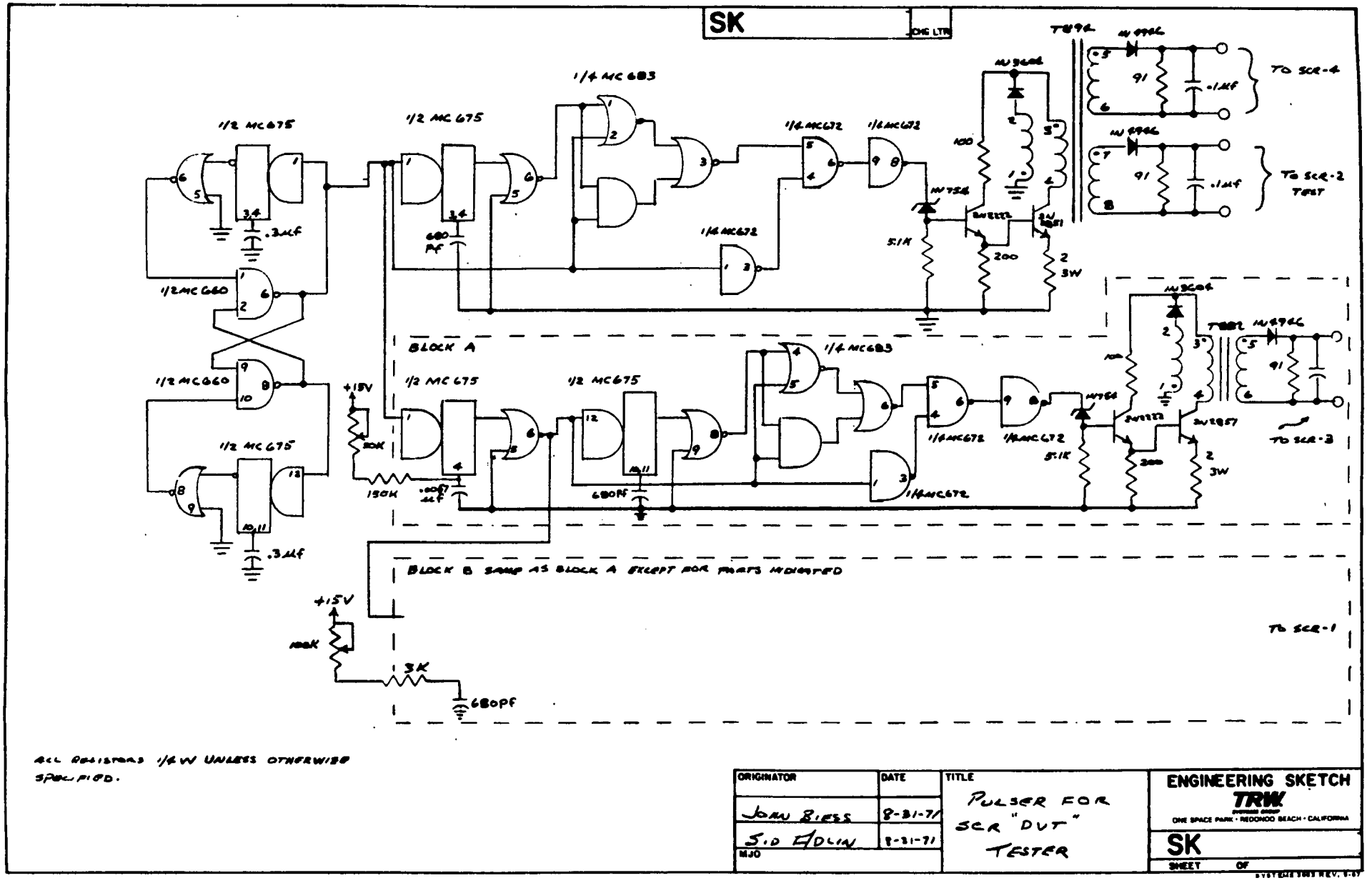

SK
1/2 MC675
1/2 MC660
1/4 MC683
1/4 MC672
.3μf
680 pf
BLOCK A
BLOCK B SAME AS BLOCK A EXCEPT FOR PARTS INDICATED
+15V
+18V
20K
150K
.005 μf
680pf
3K
5.1K
200
2 3W
100
91
.1μf
TO SCR-4
TO SCR-2
TEST
TO SCR-3
TO SCR-1
ALL RESISTORS 1/4W UNLESS OTHERWISE SPECIFIED.
ORIGINATOR
JOHN BIESS
S.D EDLIN
MJO
DATE
8-31-71
8-31-71
TITLE
PULSER FOR SCR "DUT" TESTER
ENGINEERING SKETCH
TRW
ONE SPACE PARK · REDONDO BEACH · CALIFORNIA
SK
SHEET OF

Figure D-5

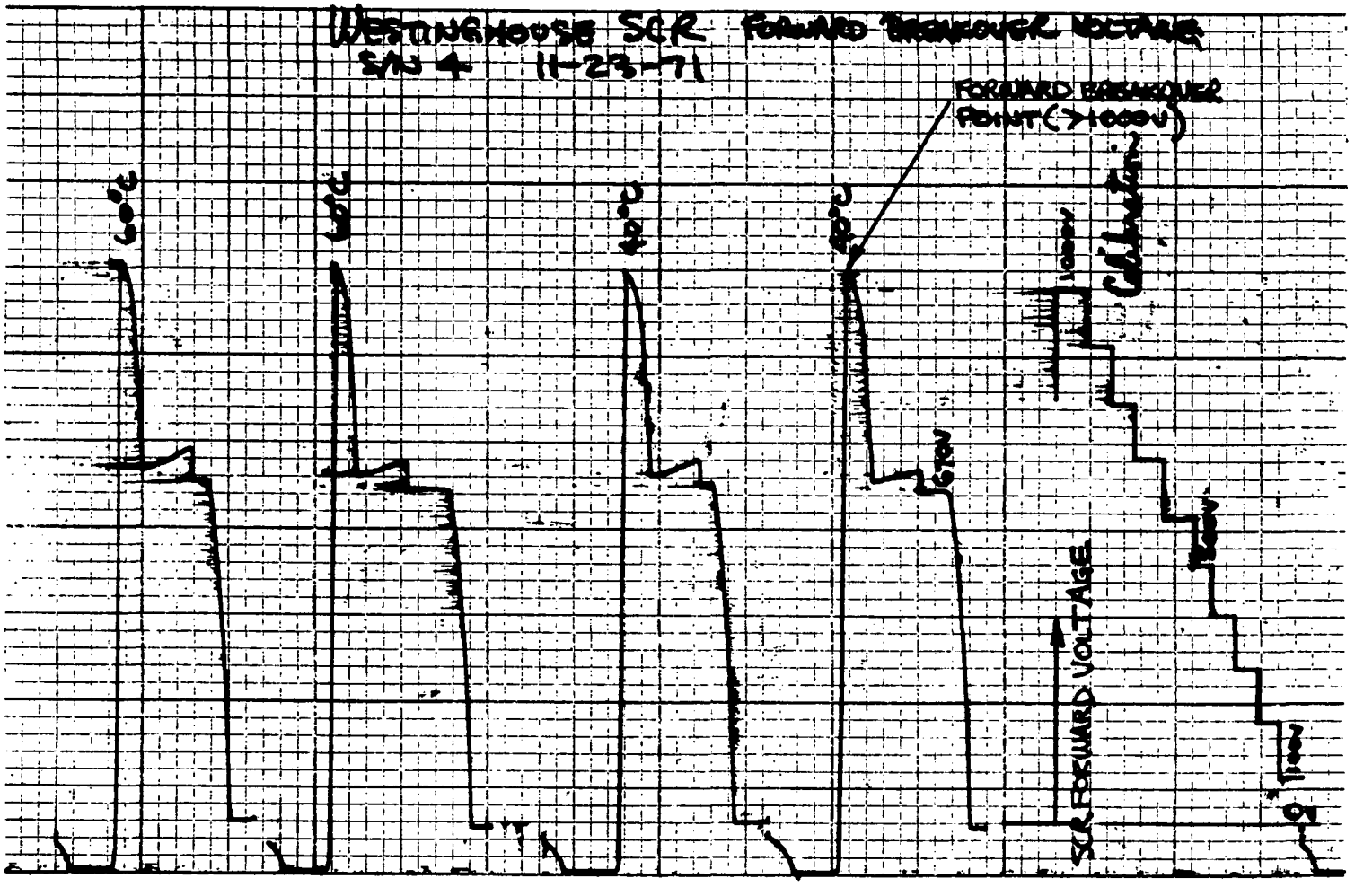


Figure D-6. SCR Forward Breakover Voltage vs Temperature

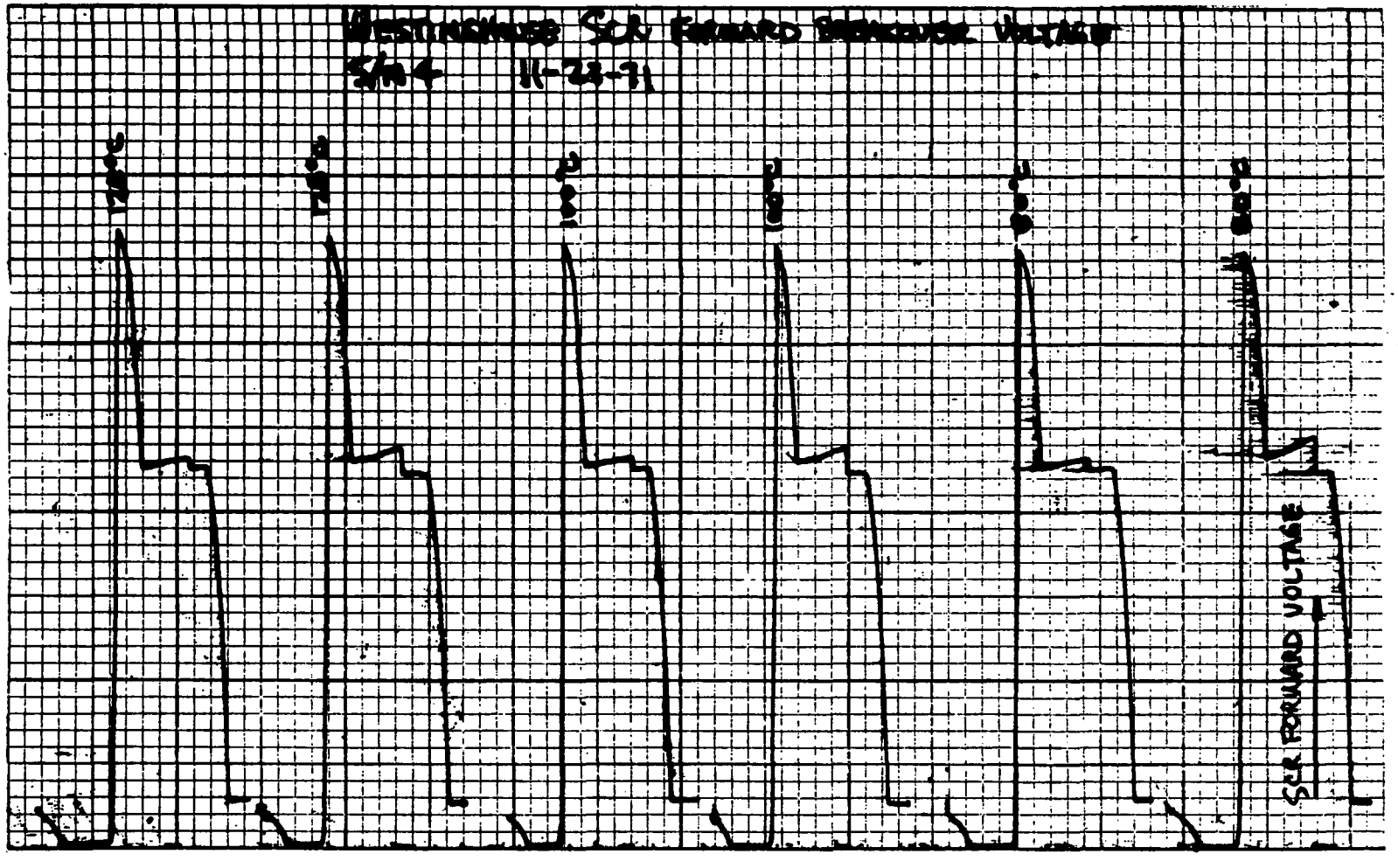


Figure D-6. SCR Forward Breakover Voltage vs Temperature

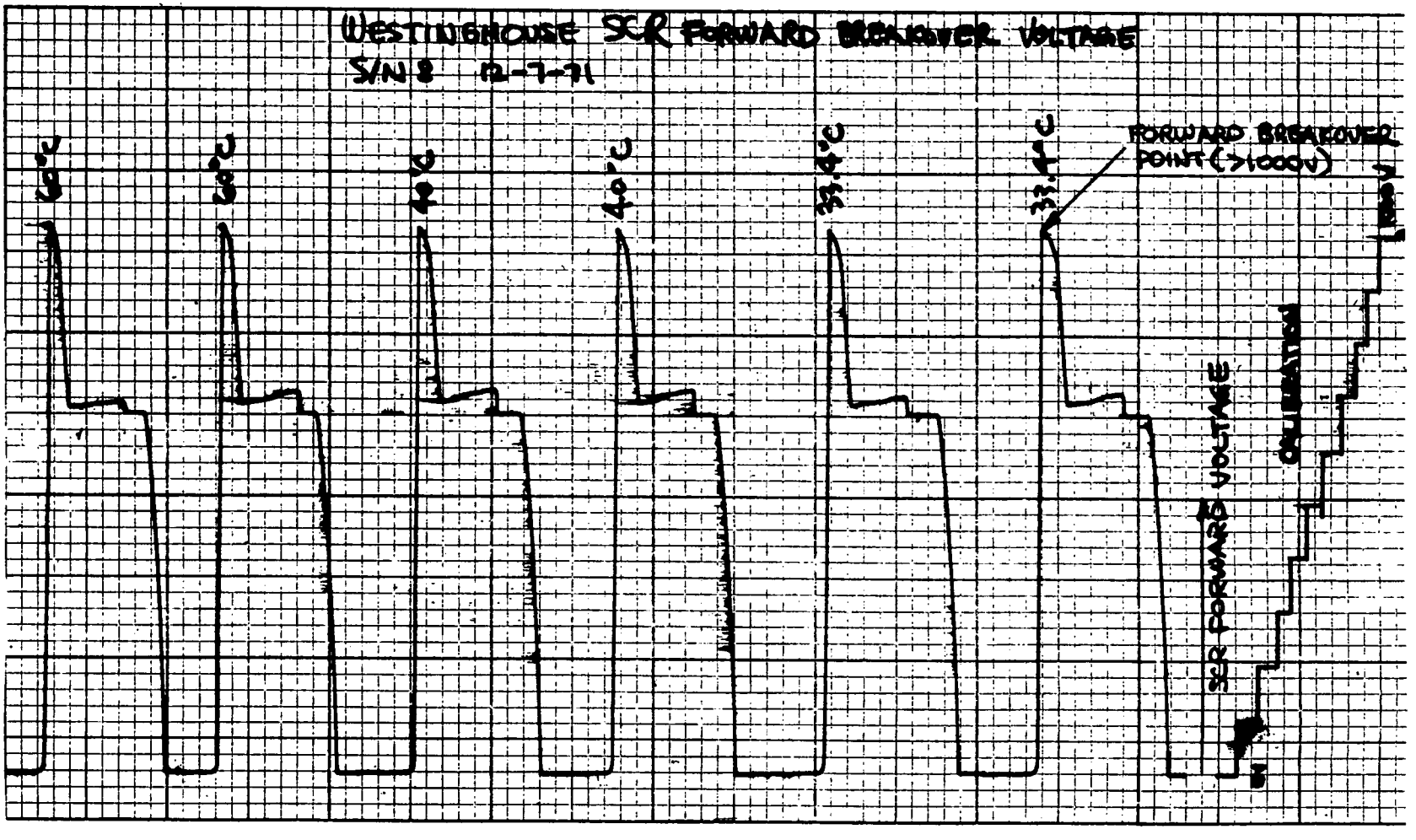


Figure D-7a. SCR Forward Breakover Voltage vs Temperature

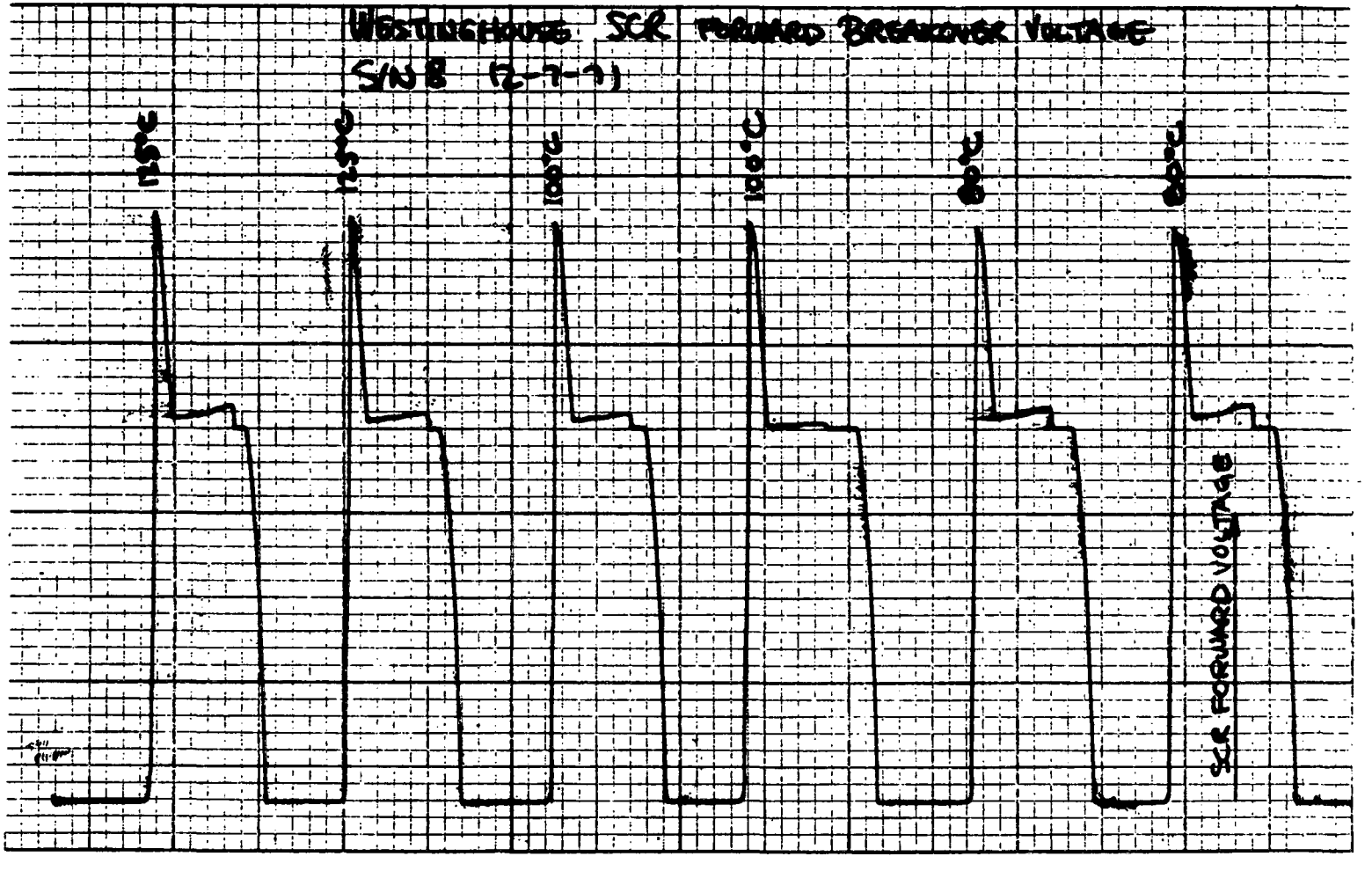


Figure D-7b. SCR Forward Breakover Voltage vs Temperature

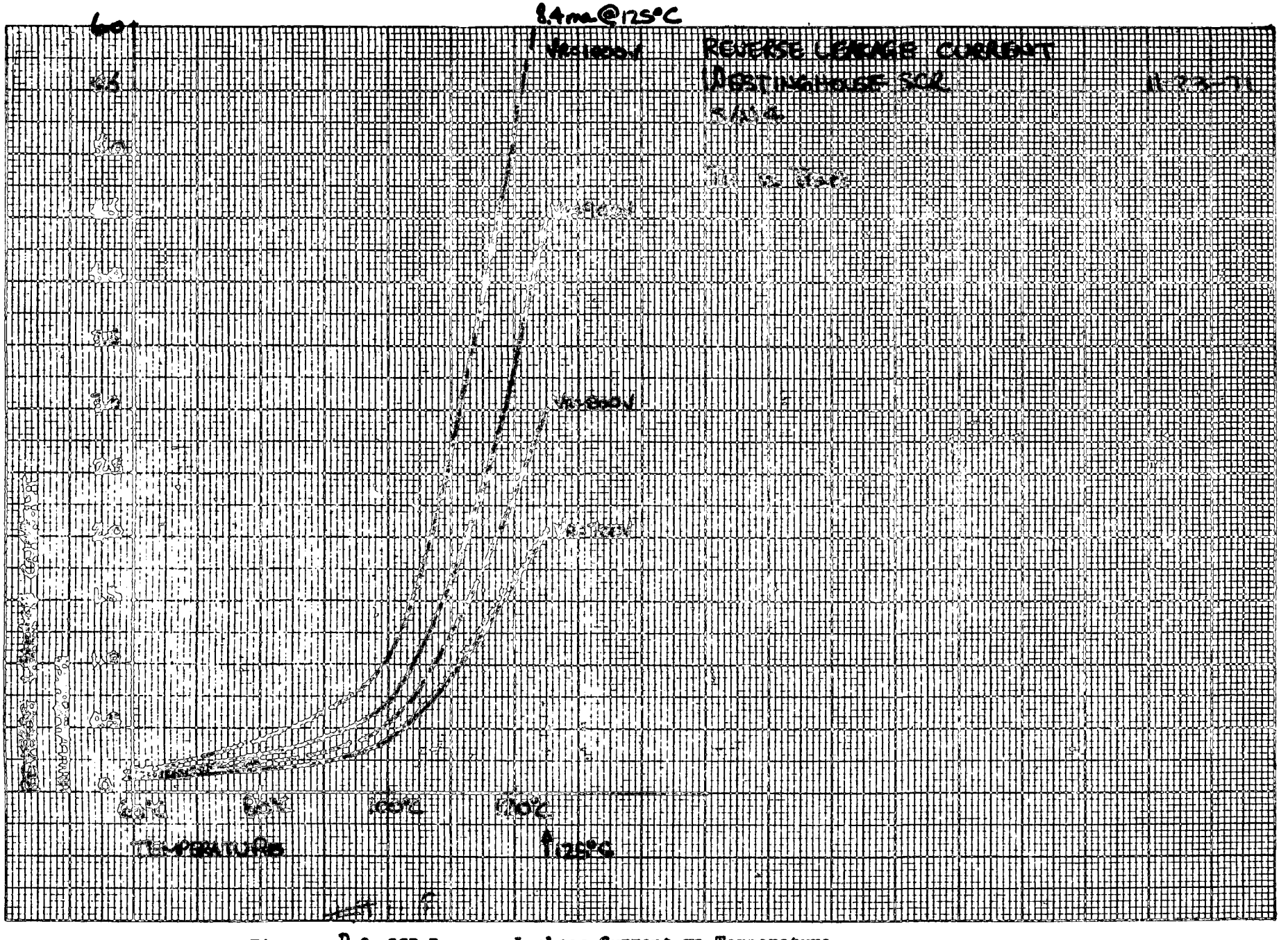


Figure D-8. SCR Reverse Leakage Current vs Temperature

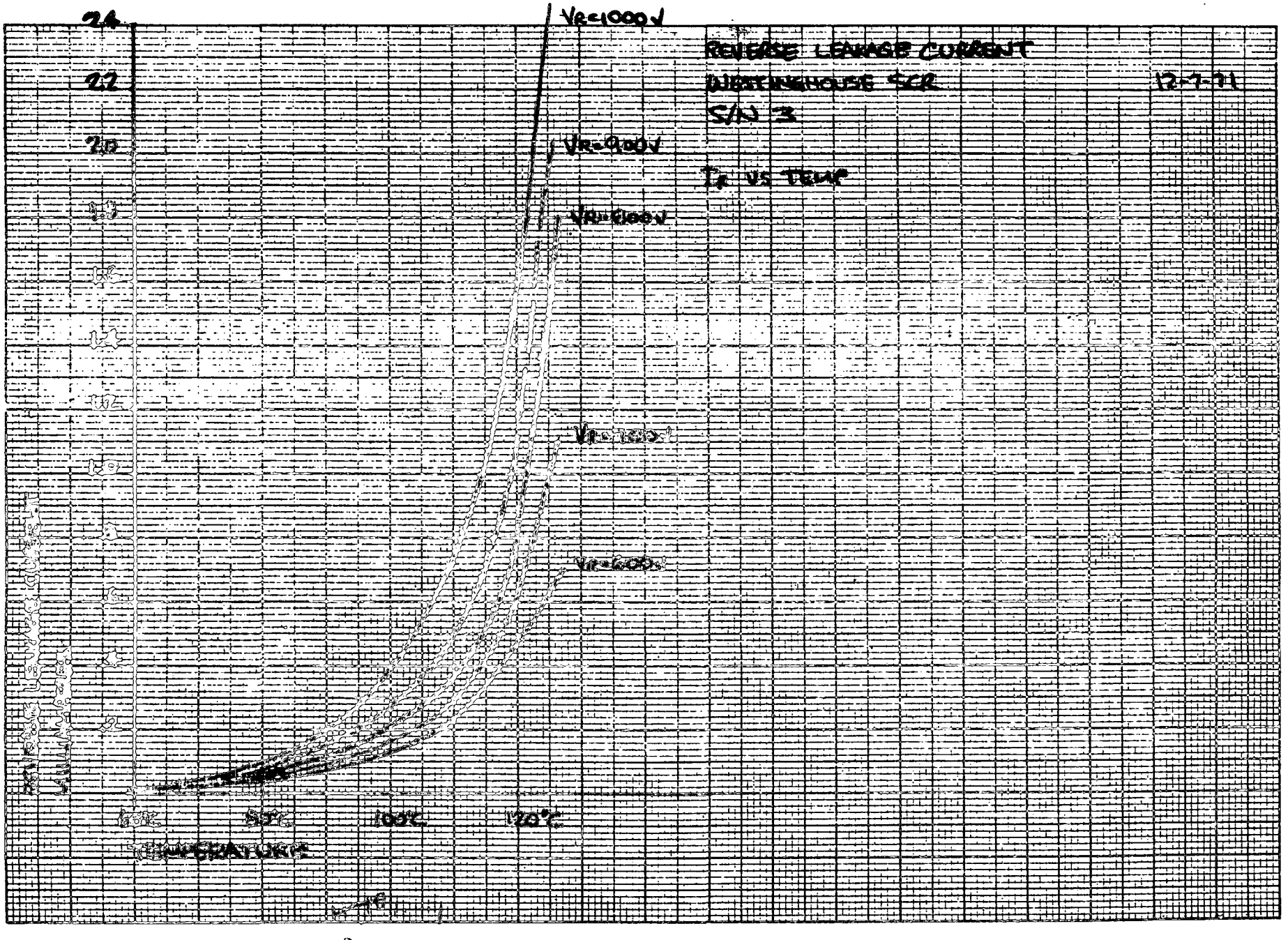


Figure D-9. SCR Reverse Leakage Current vs Temperature

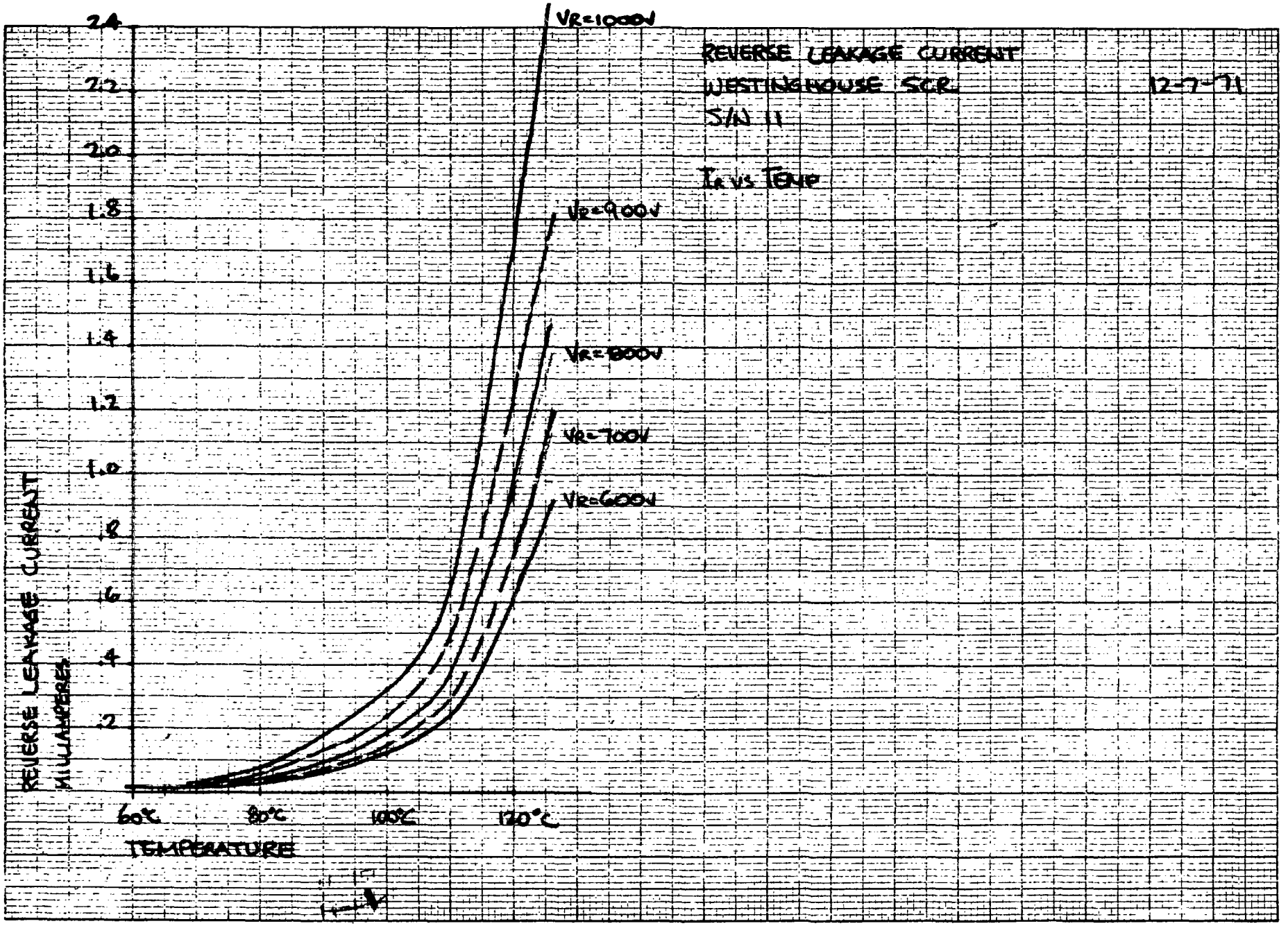
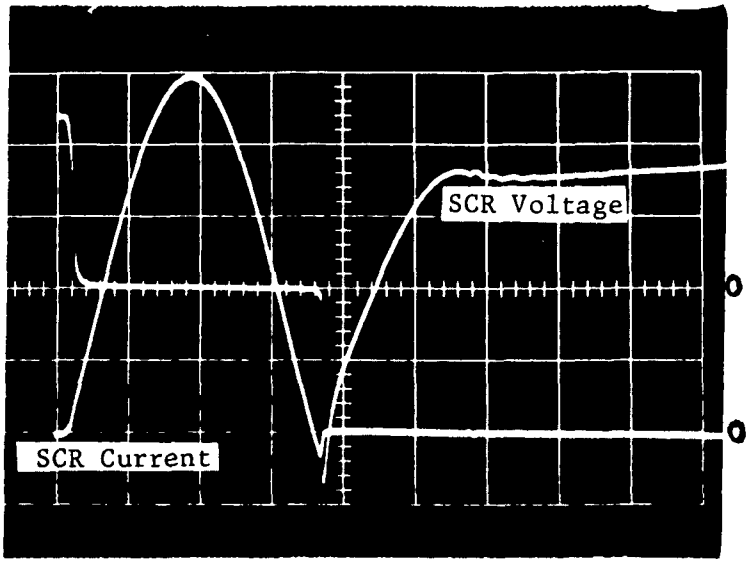


Figure D-10. SCR Reverse Leakage Current vs Temperature



V=100v/div

I=10amps/div

T=5usec/div

Figure D-11 Test SCR Voltage and Current

When checking for turn-off time and reapplied forward dv/dt, the L_1,C parameters are varied in the opposite fashion (small C and large L_1) and the supply voltage is increased to obtain the correct voltage conditions on the SCR. The value of L_2 is also adjusted to obtain the correct value of reapplied forward dv/dt.

Dynamic turn-on and forward drop characteristics are shown in Figure D-12 for the Westinghouse High Frequency SCR Part No. T5070870A4AA. Figure D-12A and B shows the change in saturated drop as a function of pulse period. Figure D-12D shows the reverse current turn off which is an expansion of Figure D-12C current.

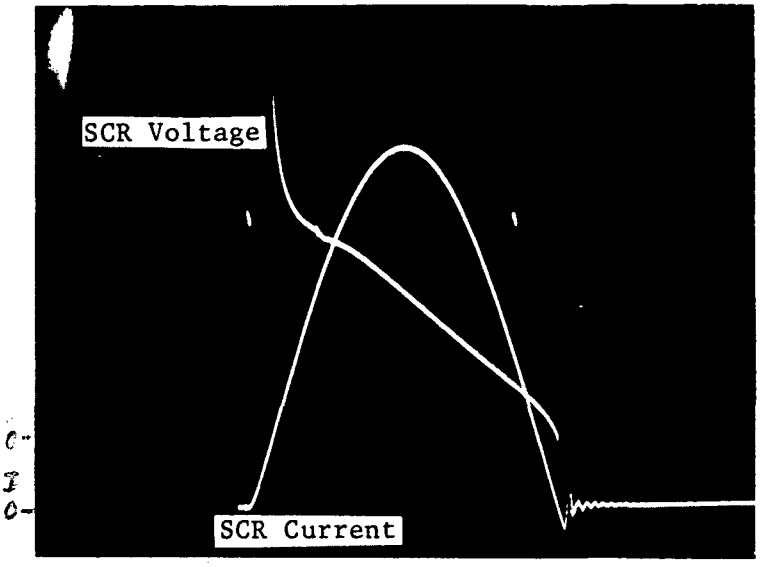
The reverse current flow during turn-off is a very important element in that this current level is flowing in the series resonant inductors when the SCR finally turned off. This inductive energy must be then dissipated in the SCR surpression networks in order to reduce voltage transients in the system and this contributes to the losses in power processor efficiency.

This reverse current also changes at a fast rate (di/dt) and can contribute to increased electromagnetic interference for the total power processor.

Figure D-13 illustrates the changes in the Westinghouse High Frequency SCR turn-off time as a function of case temperature, using the test circuit shown in Figure D-3. The reapplied forward dv/dt was 100V per microsecond. The components maximum operating temperature in the ion thruster power processor is being designed to be less than 100°C. Serial No. 8 (See Figure D-13) would not be used for the application because of the limited design margin. Component screening is necessary to obtain best static, turn-on and turn-off characteristics.

Figures D-14A, B & C show the SCR dynamic characteristics for 10, 20 and 30kHz series inverter operation. Figure D-15 is a plot of the instantaneous power loss for the 20kHz operation, shown in Figure D-14B. The reverse current flow during turn-off causes a peak power loss. The average value of the power loss for 10, 20 and 30kHz operation is plotted in Figure D-16. At lower frequency operation both the average saturated loss and switching loss is lower because the SCR has more time to turn on before the peak current level is reached and because there

20usec

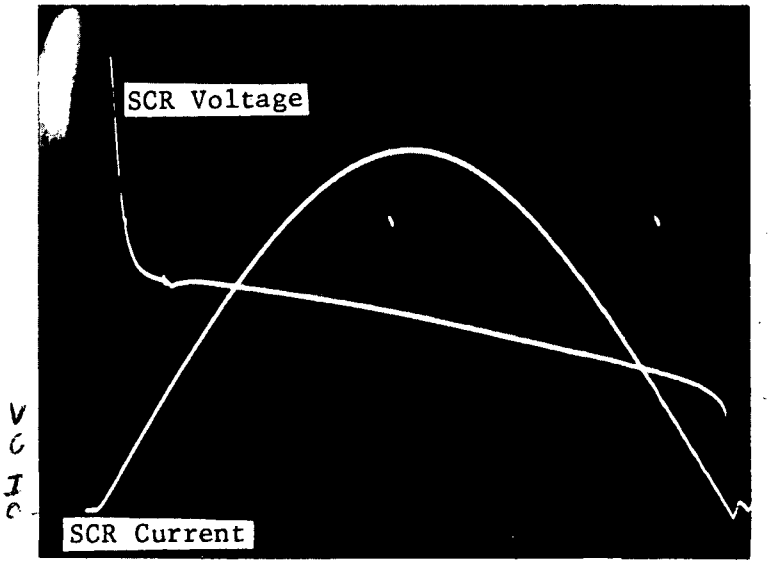


T5070870A4AA

V= 2v/cm
I= 10A/cm
Time=5usec/cm

Figure D-12A

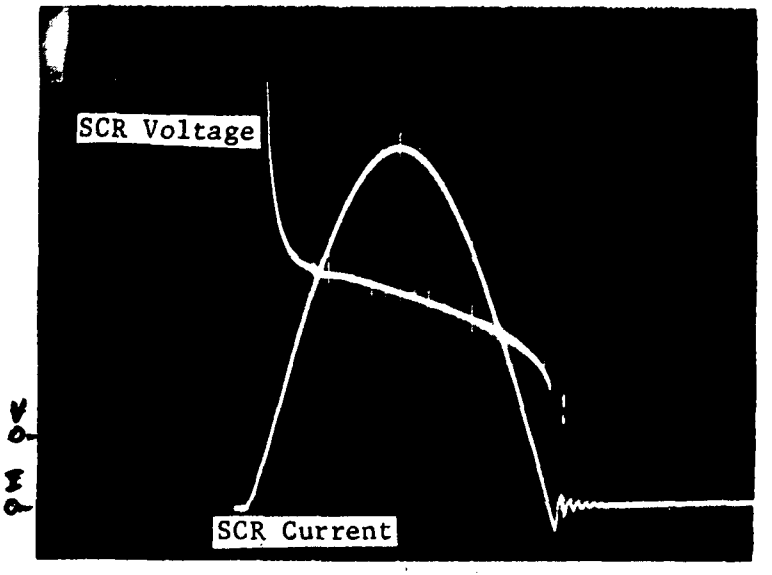
40usec



T5070870A4AA

V= 2v/cm
I= 10A/cm
Time=5usec/cm

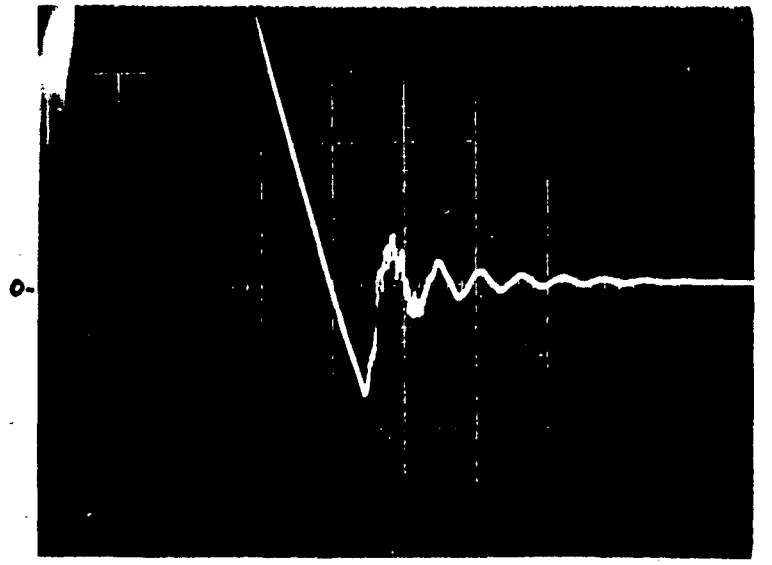
Figure D-12B



V=2v/cm
I=10A/cm
time=5usec/cm

Figure D-12C

Reverse Recovery Current



Peak Current=50A
SCR I =2A/cm
Time=1usec/cm

Figure D-12D

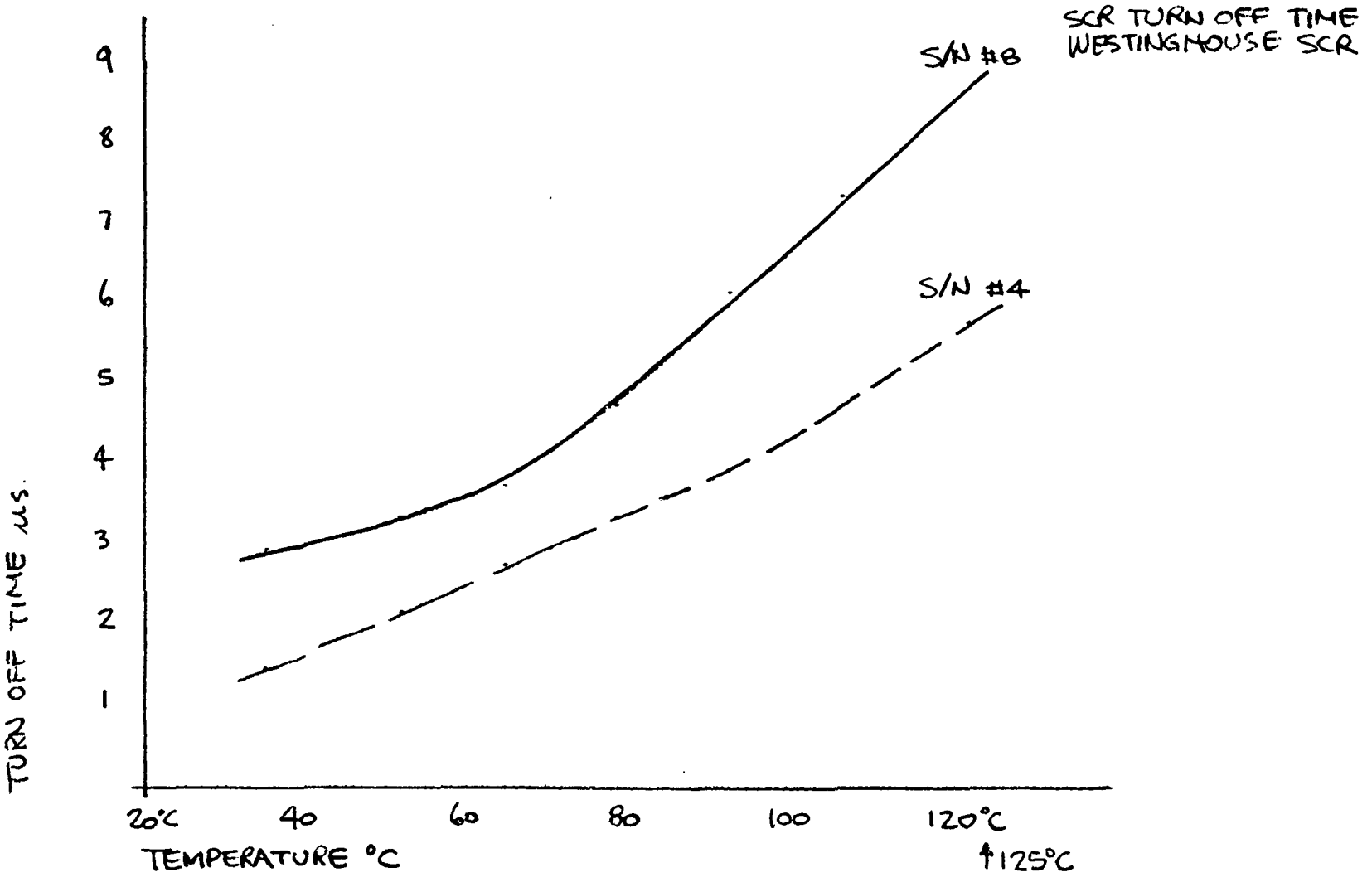
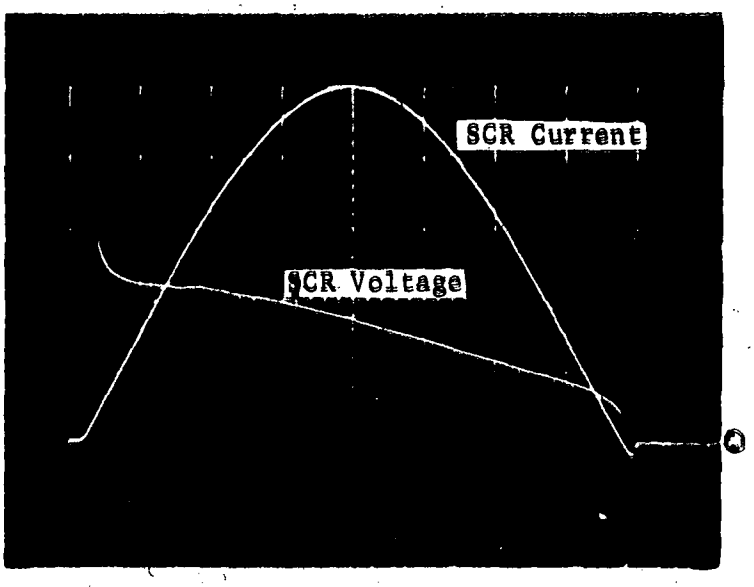


Figure D-13. SCR Turn-Off Time vs Temperature

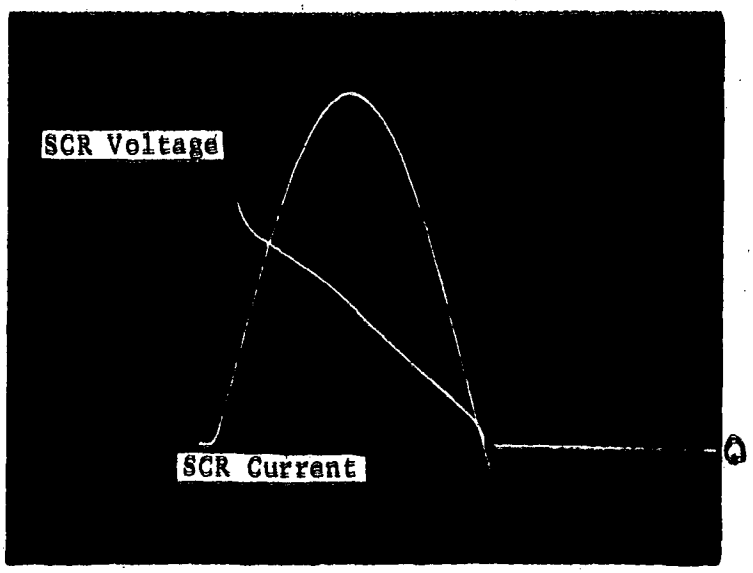


V=2v/div

I=10amps/div

T=5usec/div

Figure D-14A. SCR Forward Voltage-Current; 10KHZ Operation



V=2v/div

I=10amps/div

T=5usec/div

Figure D-14B. SCR Forward Voltage-Current; 20KHZ Operation

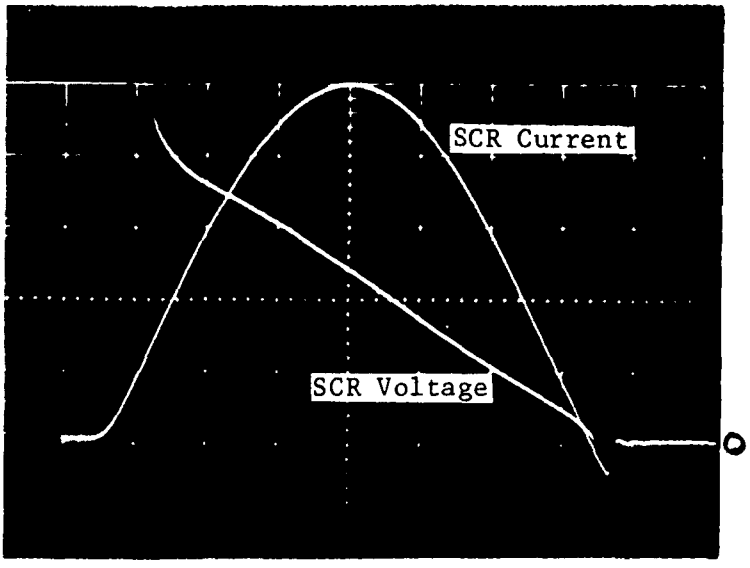


Figure D-14C. SCR Forward Voltage-Current; 30KHZ Operation

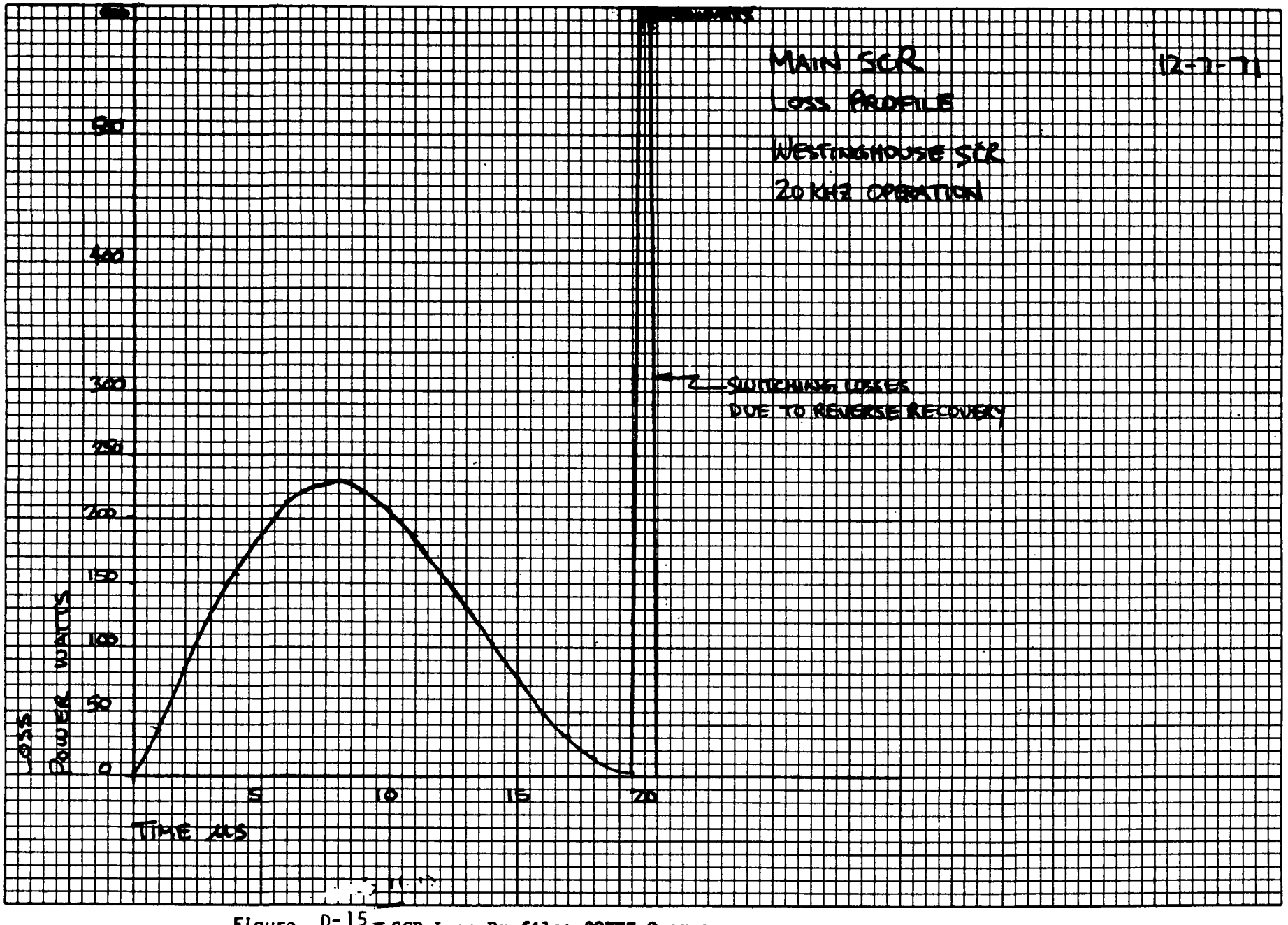


Figure D-15 – SCR Loss Profile; 20KHZ Operation

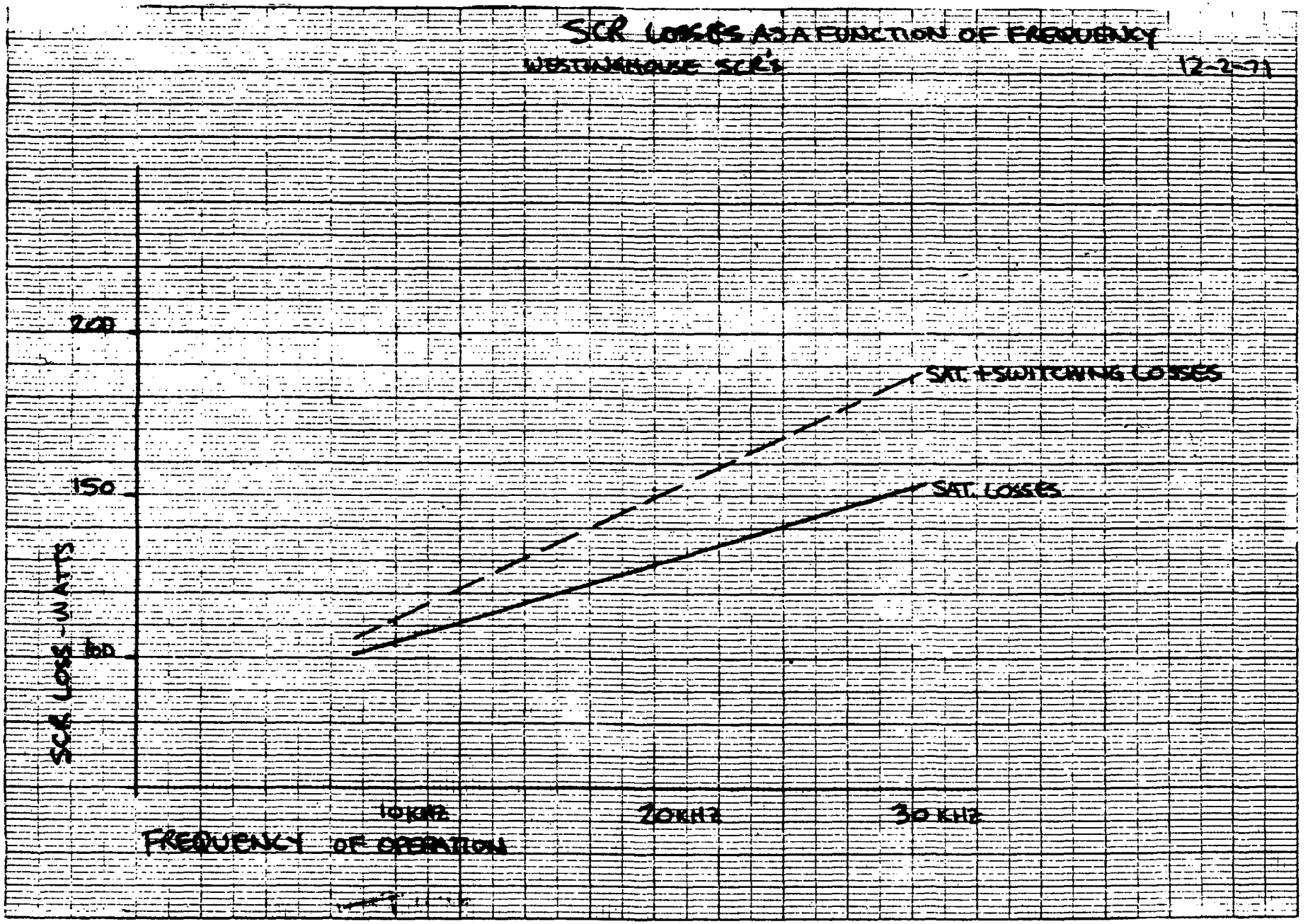


Figure D-16. SCR Losses as a Function of Frequency

is less stored charge for the SCR during turn-off.

c) Dynamic - Semicon

Figure D-17A through G shows the dynamic characteristics for the Semicon SCR Part No. SCRF168X, using Figure D-3 as the test circuit. The unit was tested with different forward current and time periods to evaluate its characteristics for operation as a power SCR for the beam supply. Figure D-17E and G shows the reverse turn-off current as a function of temperature. The unit has lower saturated drop and reverse stored charge but the voltage rating is 800V peak when tested with rectified 60 cycle voltage source. The unit lacks adequate design margin for component derating.

d) Dynamic - GE XC399 Interdigitated Gate

Twelve units of GE XC399 interdigitated gate SCRs were borrowed from Mr. Robert McKechnie of U. S. Army, Fort Belvoir, Va., for component evaluation.

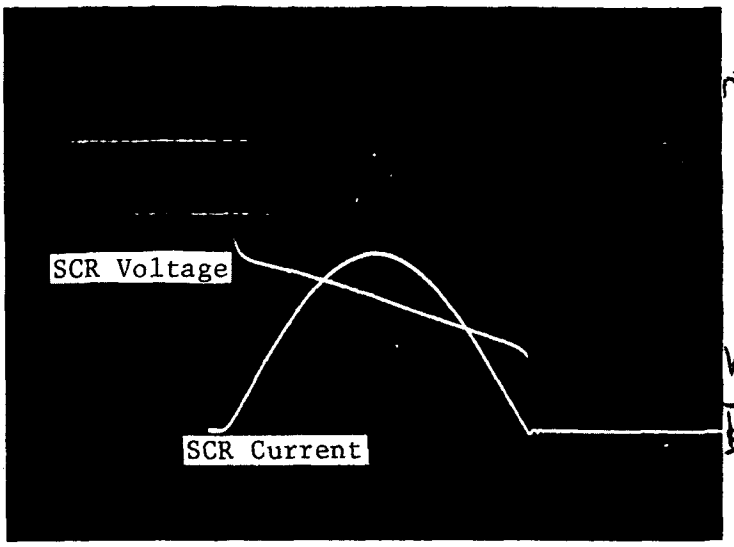
Figure D-18 shows the forward conduction drop as a function of pulse period and peak current amplitude using the test circuit shown in Figure D3. The units had high forward drop during the initial turn-on of the SCR and the forward conduction drop was over 4V at the peak of the sinewave current.

The peak reverse current was about 12A. Because of the high forward drop and high reverse current, further component evaluation was terminated. The units also had a turn off time of 25μs which would not allow high frequency operation of the SCRs.

e) Gate Assisted SCR

The 12 Gate Assisted Westinghouse SCR's (600V) developed under contract NAS12-2198 which were received from NASA Lewis Research Center under contract NAS3-14383 were also tested using the test circuit shown in Figure D-3. Figure D-19A, B & C shows the typical SCR current, saturated voltage and input gate current. These units require a high gate current for a long period in order to turn on. The gate drive circuit in Figure D-3 had to be modified in order to get these high gate current levels.

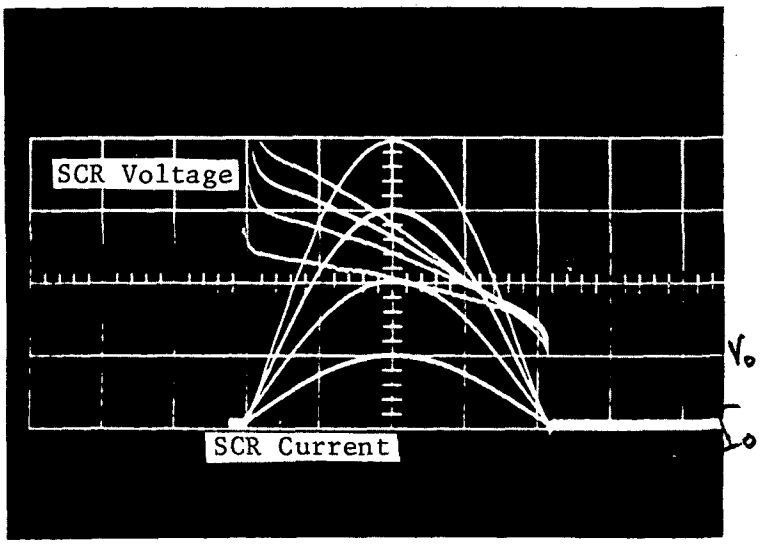
SEMICON
SCRF168X



V=5v/cm
I=20A/cm
T=5usec/cm

20usec

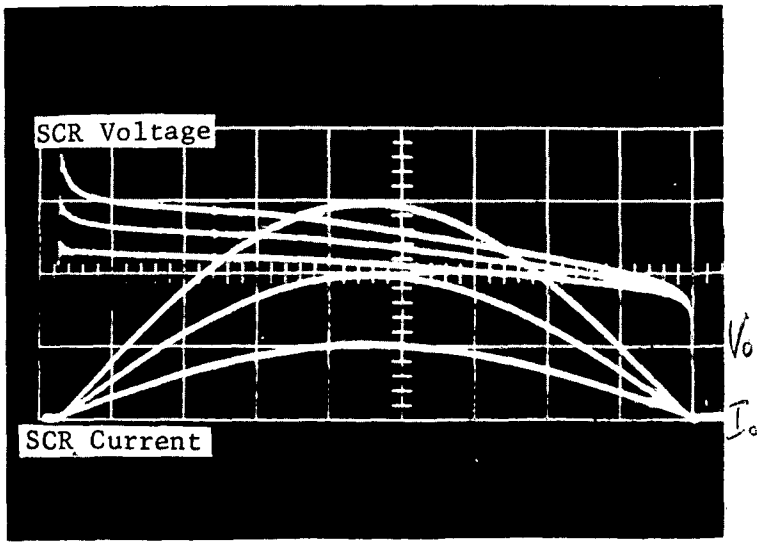
Figure D-17A



V=2v/cm
I=10A/cm
T=5usec/cm

20usec

Figure D-17B



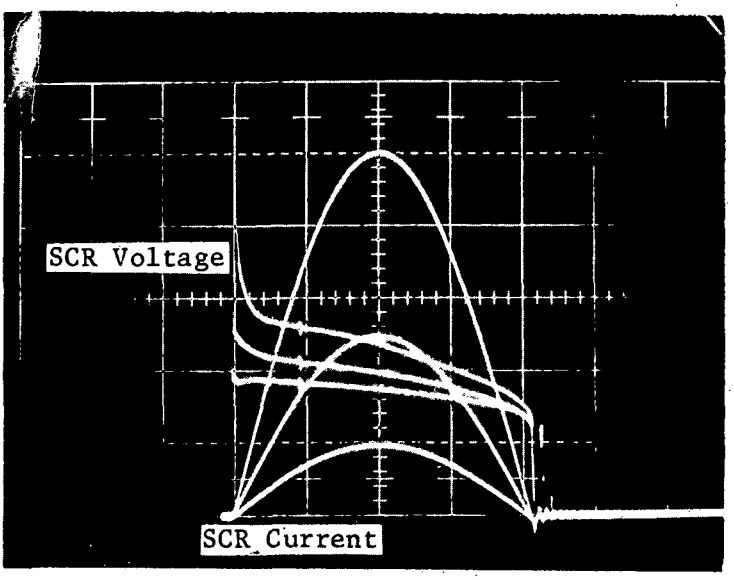
V=2v/cm
I=10A/cm
T=5usec/cm

40usec

Figure D-17C

Semicon SCRF168X

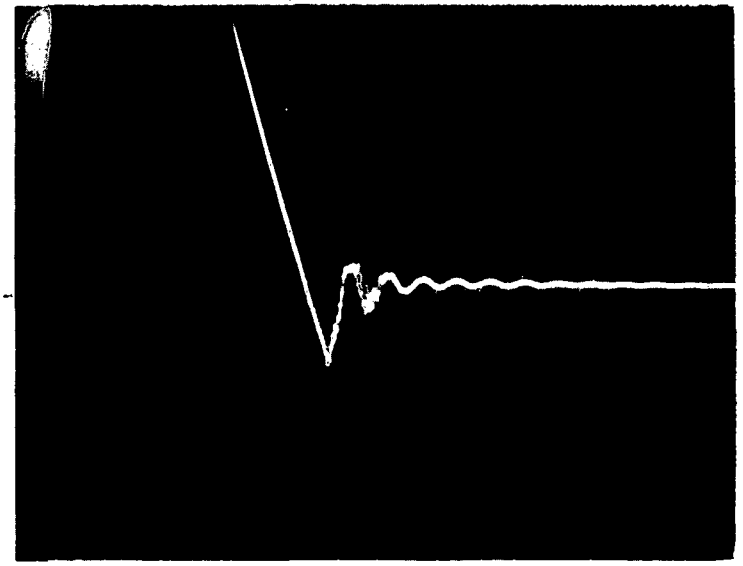
Temperature=125C



V=2v/cm
I=10A/cm
T=5usec/cm

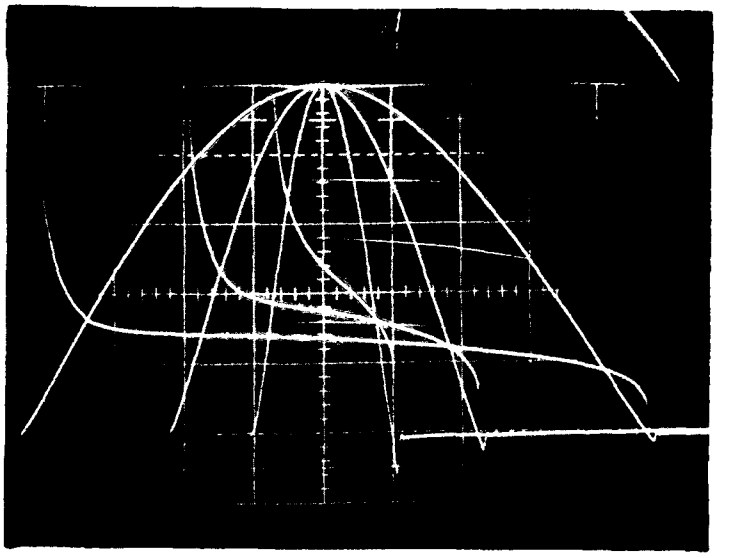
Figure D-17F

Reverse Recovery Current



Peak Current=50A
SCR Current=2A/cm
Time=1usec/cm

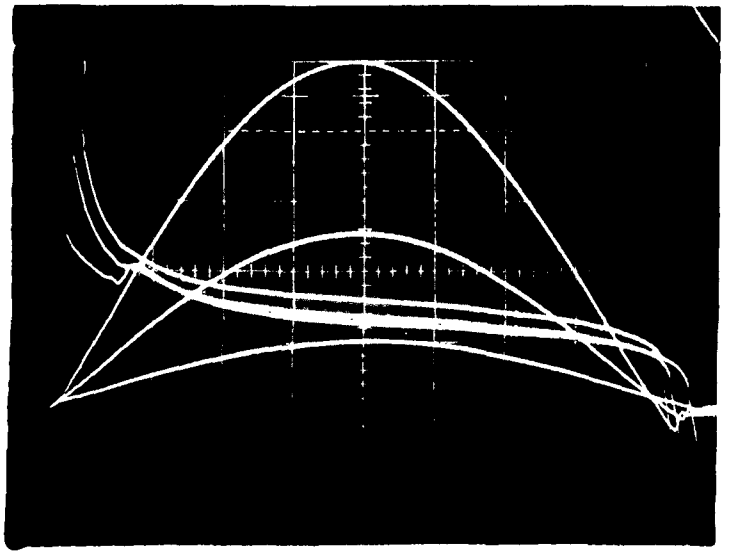
Figure D-17G



I = 20A/div

V = 2 V/div

T = 10μs/div



I = 20A/div

V = 2 V/div

T = 5μs/div

Figure D-18. GE XC 399
Interdigitated Gate SCR Forward
Dynamic Characteristics

Figure D-19A shows the minimum value of gate current which the SCR would turn on, the sinewave current is distorted but most important is that the unit has high saturated drop for over 10μs. Figures D-19B & C show the improvement as the gate current is increased up to 12A.

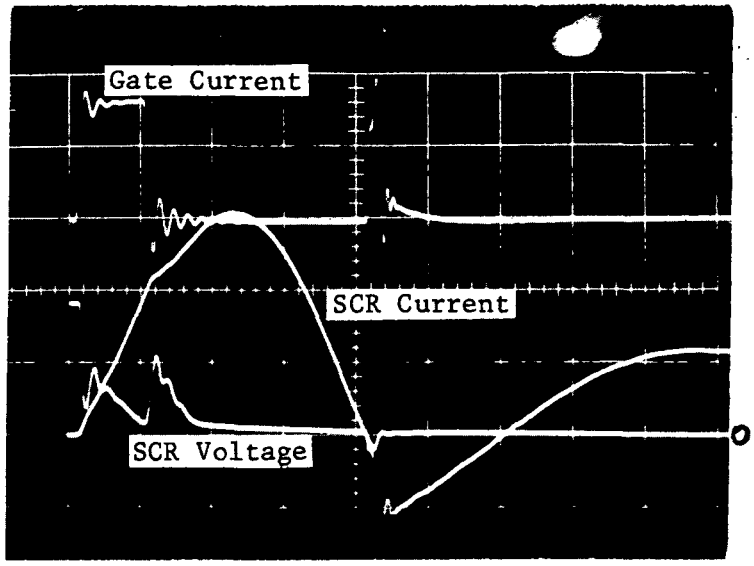
Because of the high forward drop and low blocking voltage (600V), additional testing of the unit was terminated about 1 August 1971.

Four new gated assisted turn-off SCR's (1000V) developed by Westinghouse under Contract NAS3-14394 were received, 1 August 1972. These units were tested and Figure D-20 illustrates the dynamic turn-on and Figure D-21 illustrates the reverse turn-off current.

The units had forward drops of about 2.5V.

Additional evaluation of the Gate Assisted SCR's was performed. All of the monthly progress reports for contract NAS3-14394 "High Voltage and Current Gate Assisted Turn-off Thyristor Development" were reviewed. Telephone conservations were held with Dr. Pittman and Jerry Brewster of Westinghouse about the SCR's, test circuits and component failure mode.

Test circuits were fabricated for thyristor evaluation. In the process of testing for component parameters such as turn on time, forward conduction drop, reverse recovery current, turn-off time and reapplied forward dv/dt, two of the four 1,000V units and one of the 600V gate assisted units were destroyed during the testing for turn-off time and reapplied forward dv/dt characteristics. Turn-on of the gate assisted SCR's by means of a premature application of reapplied forward dv/dt, causes a destructive failure of the components. The thyristors have very fast turn-on and a low forward conduction drop of about 2.5V (a major improvement in the losses) but have high reverse current during turn-off and require a complex gate firing circuit.



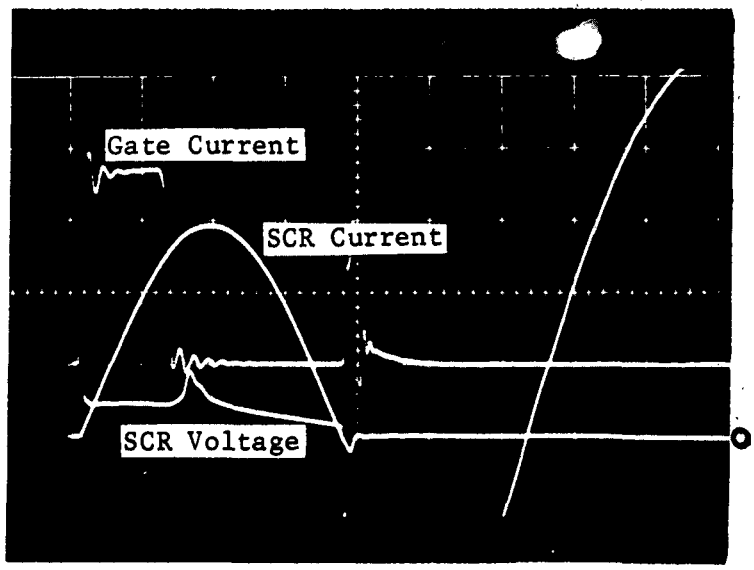
I_{gate}=2amps/div

I=20amps/div

V=50v/div

T=5usec/div

Figure D-19A. Westinghouse GATTS SCR
I_{gate}=3.25amps



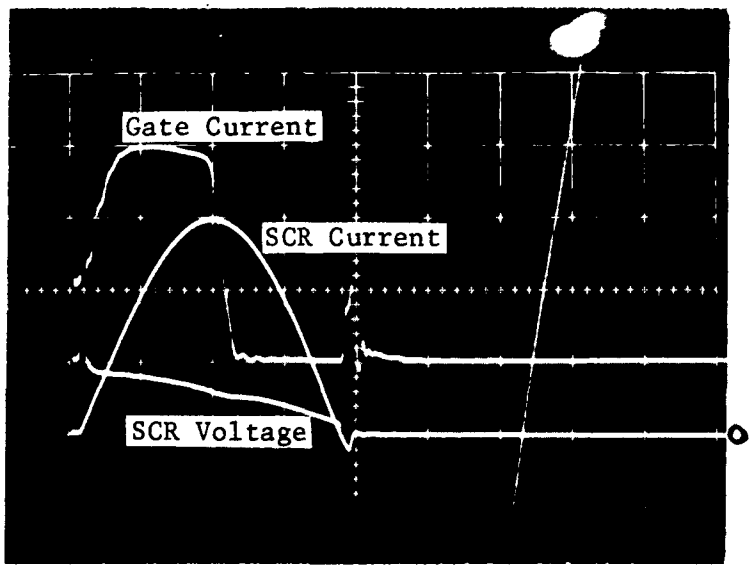
I_{gate}=2amps/div

I=20amps/div

V=10v/div

T=5usec/div

Figure D-19B. Westinghouse GATTS SCR
I_{gate}=5.40amps



I_{gate}=4amps/div

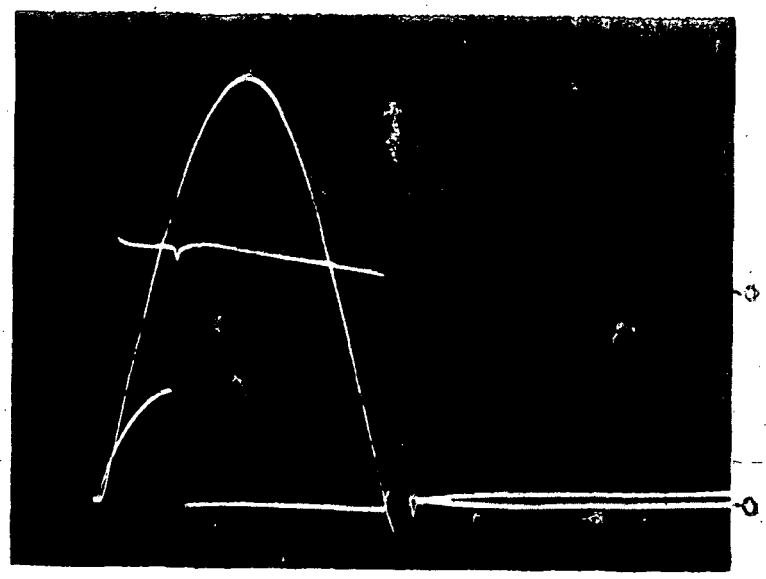
I=20amps/div

V=5v/div

T=5usec/div

Figure D-19C. Westinghouse GATTS SCR
I_{gate}=12amps

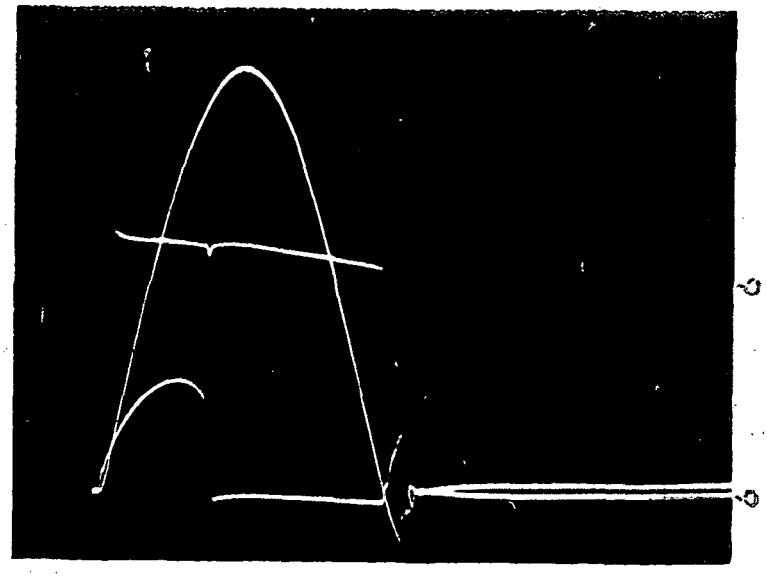
Westinghouse Accelerated-Gate SCR



T=5usec/cm

V=5v/cm

I=10A/cm



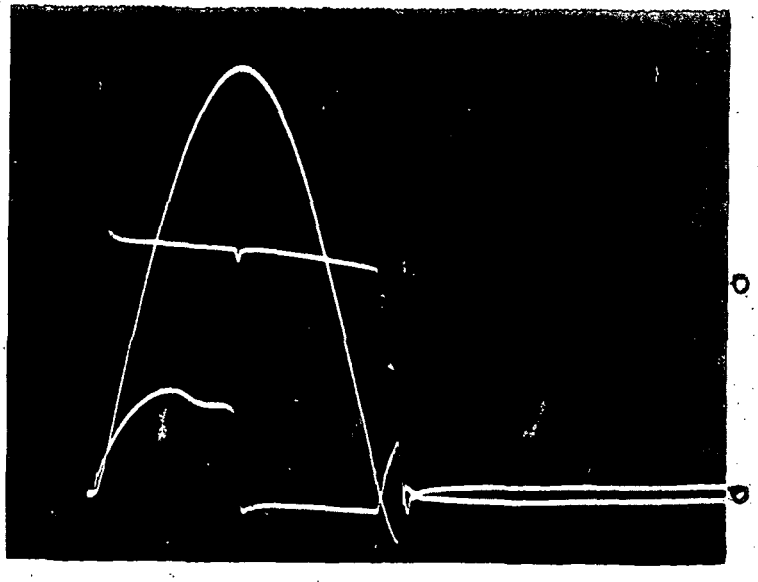
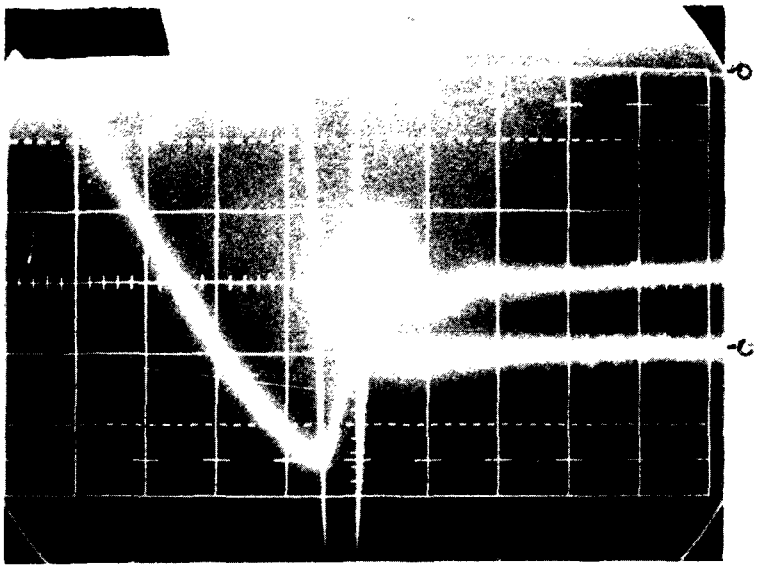


Figure D-20

Westinghouse Accelerated-Gate SCR



V=20v/cm
I=5a/cm
T=1usec/cm

Reverse Recovery Current
I_f=60amp peak half sine for 2o usec

Figure D-21

The gate firing circuit requires the following preliminary functions for reliable operation:

(1) 15A 3μs turn-on pulse

(2) Anode current sensing circuit to determine zero current flow to initiate turn-off pulse

(3) 15A 3μs turn-off pulse

(4) Negative 10V, 10Ω source as gate back bias.

The mechanization of these functions at present causes a high part count, since all of these functions must be generated for each of four SCR's used in the SCR series resonant inverter.

Because of the funding limits and schedule requirements for contract NAS3-14383, work on the high voltage and current gate assisted turn-off thyristor was terminated. It is recommended that NASA Lewis perform more component evaluation, gate control circuit design and application work on the gate assisted turn-off SCR's.

D.2 Magnetics

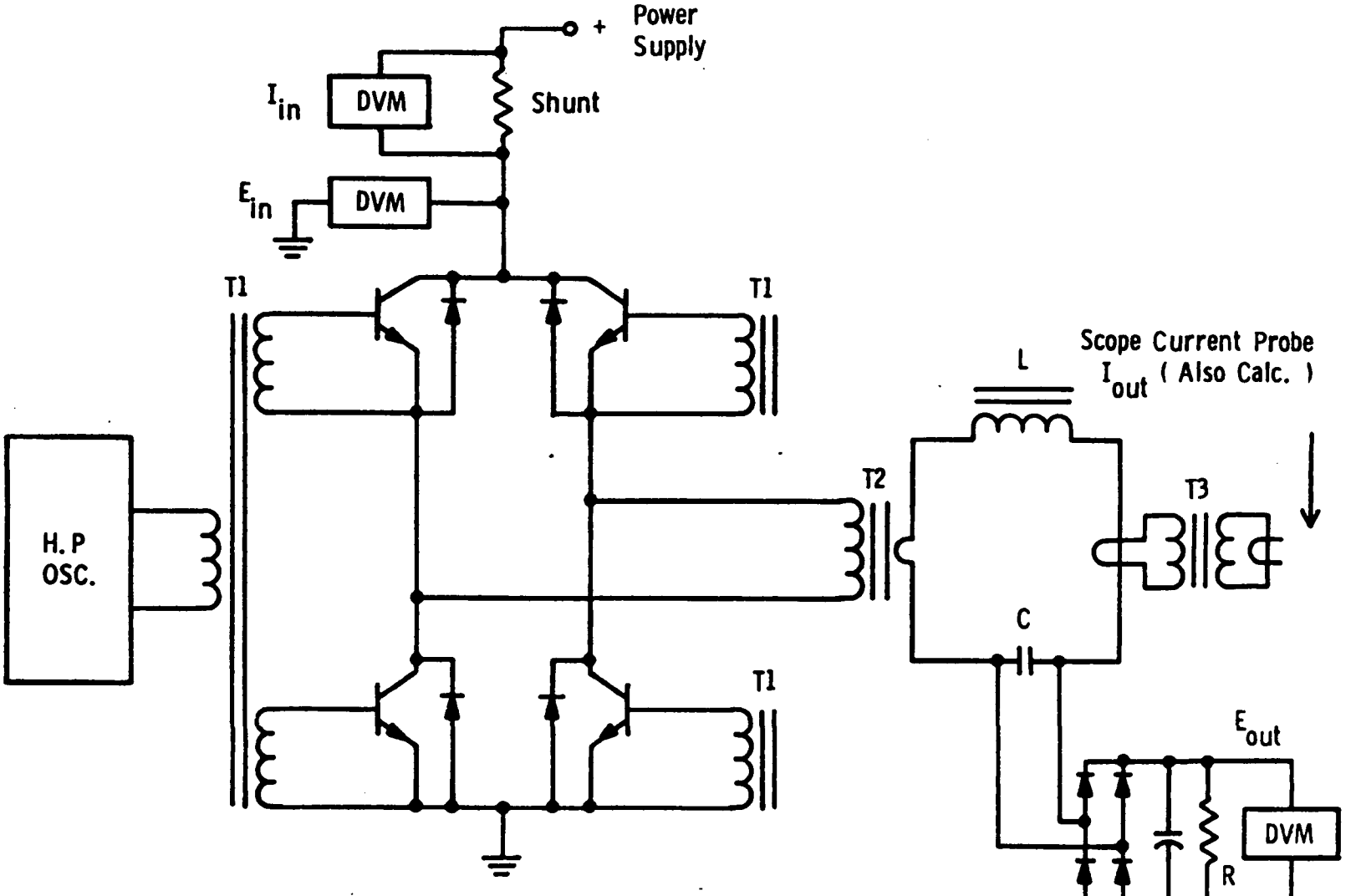
D.2.1 Basic Test Circuit

Figure D-22 illustrate the test circuit used to measure power component losses. A dc power supply provides the power to a bridge inverter configuration which provides square wave ac power to the output power transformer T2.

The drive on transformer T1 is adjusted so that there is a slight dead time between the two half cycles and thereby reducing transistor losses due to transistor storage time.

The output winding of T2 has a low number of turns (1 to 5 max). This output winding excites the LC tank . The input oscillator frequency is adjusted to match the resonance characteristic of the LC resonant tank.

Transformer T3 is a current stepdown transformer with a turns ratio of 1 to 10. The output current of T3 can be used to monitor the circuit operation with a scope. Current levels up to 100A peak in the LC tank can be easily monitored.



Loss Measurements Circuit

Figure D-22

The diode bridge network across the resonant capacitor monitors the peak to peak voltage on the component. In this manner, the digital voltmeter can accurately monitor the circuit voltage and test conditions on different components can be reproduced for relative comparison of characteristics.

The input power is determined by measuring the input dc voltage and dc current. Losses in the bridge inverter transistor and power transformer T2 can be subtracted to determine the actual power loss in the LC tank.

D.2.2 Transformers

Both design and experimental work was performed on the evaluation of core material operating at high frequency and high flux density, on the design and application of high current large gauge wire, on the winding procedures, on the design of the electrostatic shield, and on component impregnation to increase its thermal capability. Mathematic optimization analysis was also performed to determine optimum transformer design to produce a minimum total weight of the transformer or inductors and the weight of the power source to compensate for the component losses.

Checks of the actual component designs showed good corelation between the calculated and the built components.

A summary of the program results are:

1. Use Litzendraht wire #33 strand or smaller for all windings and shield in frequency range of 10 to 25kHz, to reduce eddy current losses in the wire when operating in high frequency high flux level field.

2. Maximize winding coupling. All windings must be single pass near 360° with all starts and stops approximately at the same place in order to reduce leakage inductance between windings.

3. Any winding which cannot fit in a single layer must be progressively wound (sometimes known as bank wound) so as to minimize turn-to-turn capacity effects, and the high frequency circulating currents internal to the transformer.

4. For maximum current sharing, any high current winding or low current winding which is in a leakage flux field, must have all Litzendraht strands sufficiently twisted to attempt as a goal that each strand be placed in the exact or equivalent flux field and each carry its own share of the total current, thereby reducing winding losses.

5. Where a shield is required that is in a high flux field (such as the beam transformer) it must be designed from #33 wire or smaller to reduce the eddy current losses in the shield.

6. The transformer must be designed with MN60 or MN100 Ferrite assuming a 2200 gauss maximum flux density in order to reduce the transformer core loss.

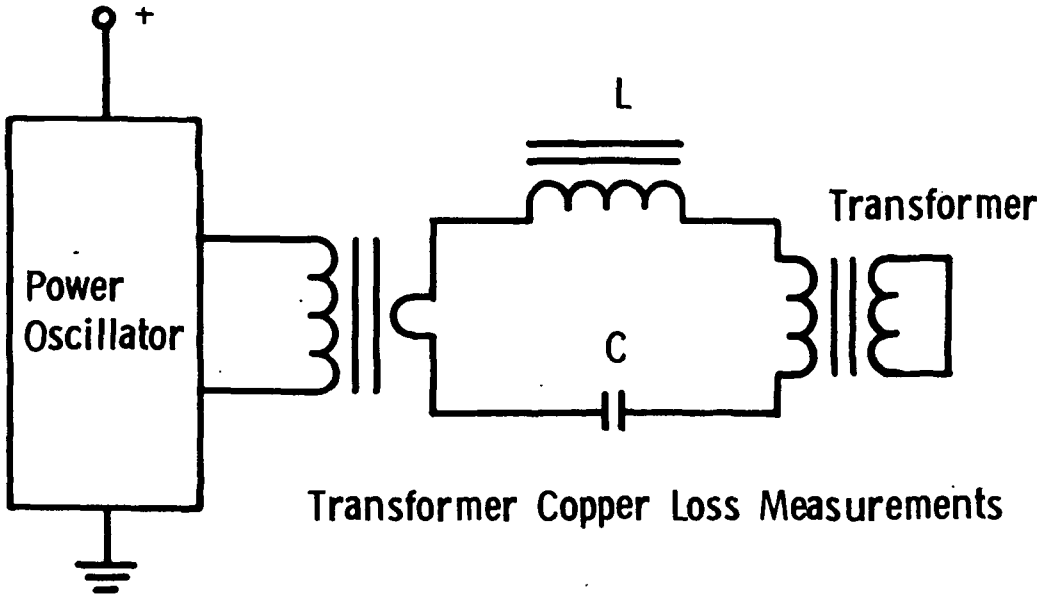
The design intent is to reach the optimum efficiency weight figure as theoretically determined by the magnetic equations developed to achieve minimum total weight of transformer and source.

Figure D-23 shows the circuit connections that are made to Figure D-22 in order to measure the test power transformer I^2R losses.

Figure D-24 shows the circuit connections that are made to measure the test power transformer core loss.

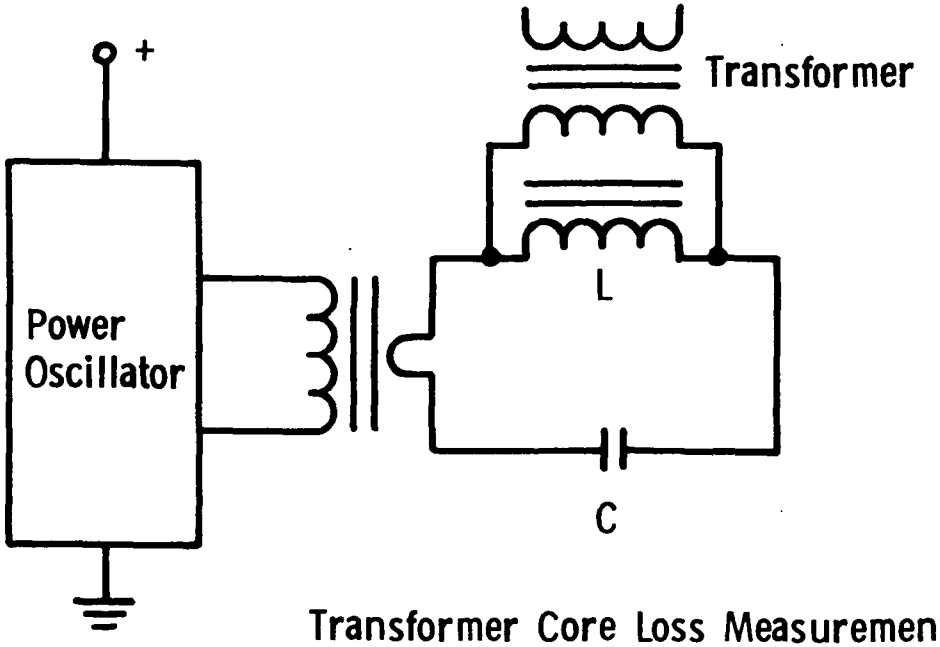
Data from the core loss tests are plotted in Figure D-25. Watts per pound versus flux density at 25kHz are shown for MN100 and MN60 ferrite material from Ceramic Magnetics, Fairfield, N.J. It was found to be the lowest loss ferrite core material.

Now that the magnetic had the lowest losses compatible with the weight requirements, would they work in the series resonant inverter design. The low power magnetics used in the multiple output inverter worked well since the inverter is always running at its maximum operating frequency. But the beam (V5) and arc (V4) transformers did not perform correctly at low output power when the off time between power pulses became large. The flux level would reset during the off time so that during the next power pulse the power transformer would saturate, power could not be delivered to load and another power pulse would be required. This caused the system to operate at a random frequency and caused input filtering problems. To correct this flux fall back a bias winding was added to the transformer to balance the circuit operation, but the power loss in exciting the core was excessive.



Transformer Copper Loss Measurements

Figure D -23



Transformer Core Loss Measurements

Figure D-24

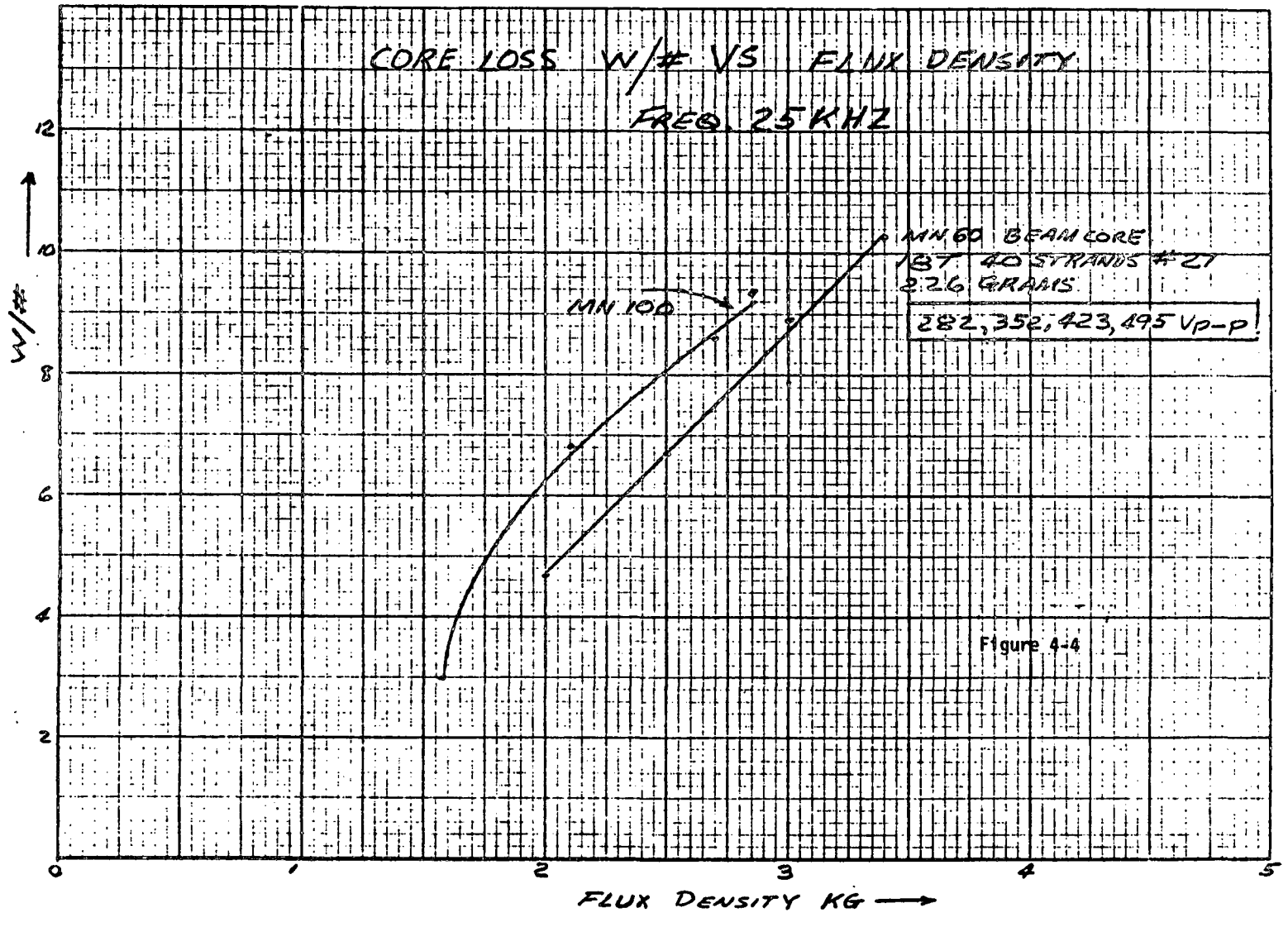


Figure D-25

The transformer was redesigned using one mil supermalloy. Core loss data showed that the aluminum core boxes on the cores caused extra losses. Therefore, tape wound cores were bought with plastic boxes. The bias winding is still required for balanced circuit operation when operating at reduced output power but the power loss in the drive circuit is minimal.

Some of the design characteristic of the high voltage beam transformer to reduce its weight and maintain high reliability will be presented.

The high voltage design aspects of the beam transformer are listed below in the form of a checklist to ensure that all design and construction details are consistent with a high voltage application.

The following items are to be reviewed:

1. Excessive dielectric stress
2. Creepage breakdown paths
3. Cleavage breakdown paths
4. Breakdown due to outgassing
5. Corona breakdown
6. Breakdown due to dielectric voltage pileup.

Wire

1. Establish electrical stress design rating and basis.
2. Design calculations for worst case wire stress.
3. Circuit stress usage including transients of startup shutdown, allowed load transients.
4. Worst case test stress.
5. Ratio of stress rating to maximum stress applied.
6. Temperature rating versus usage and derating for lifetime.
7. Thermal shock rating versus usage.
8. Minimum wire size (if less than #38 shop procedures and practices to prevent wire damage).

Leads

Start & Finish leads

Winding Extension

- o Anchoring
- o Breakout
- o Insulation crossover
- o Insulation tubing
- o Tubing material
- o Tubing bondability
- o Tubing sensitivity to corona

Winding Lead Attachment

- o Anchoring
- o Breakout
- o Soldering, tabs and sharp points
- o Soldering mechanical-electrical protection (pads, other)
- o Stripping (winding and lead attachment)
- o Lead attachment material
- o Lead attachment voltage rating versus worst case usage
- o Lead attachment material bondability
- o Lead attachment material corona sensitivity
- o Can air be trapped in lead attachment
- o Does lead attachment have to be flexible and if so can impregnation cause lead breakage.

Turn to Turn

1. Establish electrical stress design rating and basis.
2. Design calculations of worst case turn to turn stress.
3. Circuit verification of design worst case usage analysis.
4. Worst case test stress.
5. Ratio of stress rating to maximum stress applied

6. Bank winding (design intent and manufacturing control)
   - 6.1 Bank winding definition (design def.; mfg. def).
   - 6.2 Bank winding shop documented procedural instructions.
   - 6.3 Bank winding shop practice.
   - 6.4 Maximum turns separation by design for instruction "bank wind" must include allowance for throwbacks, stray turns, falloff turns.
7. Is there any unnecessary tape to destroy or impair design intent?

Barrier Insulation

1. Established electrical stress design rating and basis.
2. Design calculations of worst case analysis.
3. Worst case test stress.
4. Ratio of stress rating to maximum stress applied.
5. Examine rating in terms of bonding, encapsulation integrity, creepage, cleavage, corona and dielectric voltage pileup.

Winding to Winding (especially for toroid wound magnetics)

1. Established interwinding insulation stress rating and basis.
2. Design calculations of worst case interwinding stress.
3. Circuit usage analysis (starting and turn-off transients, circuit faults and opens).
4. Worst case test stress.
5. Ratio of stress rating to maximum stress applied.
6. Documented shop procedure for uniformity control.
7. Documented definition of "in and out" taping.
8. Documented definition and procedure of overlap including fractional overlap or ID or OD instructions.
9. Definition and shop procedure of peripheral wrap.
10. Definition and shop procedure of peripheral wrap foldover.
11. Examine rating in terms of bonding, encapsulation integrity, creepage, corona, dielectric voltage pile-up, and end winding integrity.

Layer to Layer Insulation

1. Examine items 1 through 5 and 11 of winding to winding for stick wind or hand wind layer type coils with particular emphasis on creepage and cleavage control.

Encapsulation and Impregnation

1. Dielectric strength design rating.
2. Control of thick sections
3. Reinforcement to prevent cracking
4. Design considerations of temperature and thermal shock
5. Procedural control of impregnation integrity

Termination

1. Terminal mechanical strength
2. Control of sharp corners and edges of terminals after soldering
3. Mechanical and electrical pads to insulate against inside sharp terminal protrusions
4. Potting performance around sharp edges of terminals. (Will it crack due to thermal shocks initiated by sharp mechanical gradients?)
5. Breakdown terminal to terminal or over other paths

Mounting

1. Does mounting include conductor material?
2. If so, is there adequate insulation for breakdown and creepage?
3. Will thermal shock break bond between transformer and mounting

Figure D-26 shows a complete V5 beam output transformer which has been impregnated by a special process where there is a minimum of external potting compound. The potting increased the total weight by only 11%.

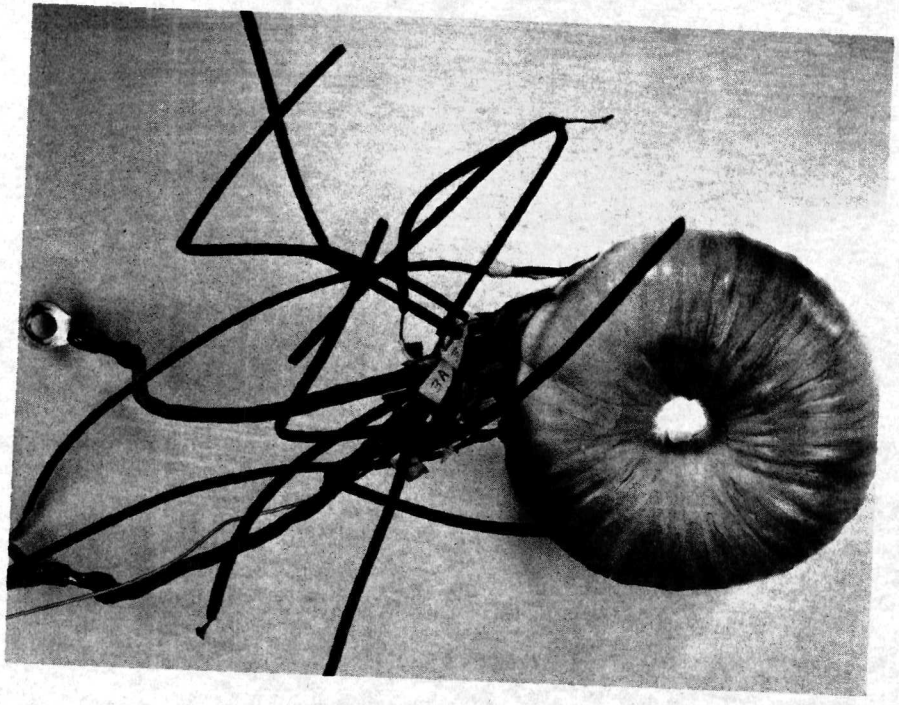


Figure D-26 Beam Power Transformer 717 gms, 10cm diam x 4cm high

D.2.3 Reactor

The powdered molybdenum permalloy reactor designs for the inverter LC resonant tank were measured in the series resonant power tester shown in Figure D-22, and when analyzed, was found to have higher losses than could be accounted for by core loss curve data and wire loss data which included factors for skin effect and proximity effect.

In order to identify the discrepancy between the calculated and measured values a number of simple and basic experiments were performed.

A ferrite core design was fabricated using some ferrite "U" cores which were available. This reactor design embodied all the known or suspected techniques to reduce losses. The input power required to maintain and circulate a specific voltage and current in the series resonant L & C was measured. Using this ferrite L and a polystyrene C the circuit was now carefully monitored to determine relative losses. The first basic experiment was inserting some turns of wire with a constant total cross-section into the air gap vicinity and taking data on observed additional losses as a function of:

a) number of turns
b) size of litz strands
c) homemade litz versus high quality manufactured litz
d) soldered or unsoldered wire ends
e) untwisted and very well twisted strands
f) distance of turns from gap
g) limited frequency range
h) thin copper sheet
i) aluminum plate
j) distance of aluminum plate from air gap

In addition to these experiments data was also taken on:

Reactor designs

a) powdered cores
b) ferrite open gap cores ("U" core)
c) ferrite closed gap core (cup core)

and repeated elsewhere

Capacitor losses

Transformer losses

Core losses

SCR losses

Wire losses

The results of these tests are the following set of design principles and preferences which apply for high "Q" inductors in the range of 10-25kHz.

Principles -

1. Litzendraht wire of size #33 stranding (or smaller) must be used.
2. The wire must not be in the gap flux field.
3. The Litz must be well twisted or litzendrant to allow each strand to be in an equivalent field even if the field is non-uniform.
4. Minimize turns to turn capacity effects by progressive winding if single layer design is not practical.

Preferences -

1. The open gap reactor must be mounted so that the gap does not come less than 3/4" away from thick section conductors.
2. A gapped ferrite core design is preferable to a molybdenum powdered iron core design to maintain low losses but the presence of high flux field in the spacecraft due to gap may force the use of powdered molybdenum toroidal cores for this application.

The design intent is to reach the optimum efficiency as theoretically determined by the magnetic equations developed to achieve a minimum total weight of inductors and sources.

D.2.4 Cabling Losses

A 25kHz power circuit measurement was made to determine the loss of a 10-foot length of Litzendraht 312 strands of #33. This was compared to the calculated I^2R loss of the wire using the dc resistance measured value. The measurement was made with the circuit diagram shown in Figure D-27, which is a modification of the test circuit shown in Figure D-22.

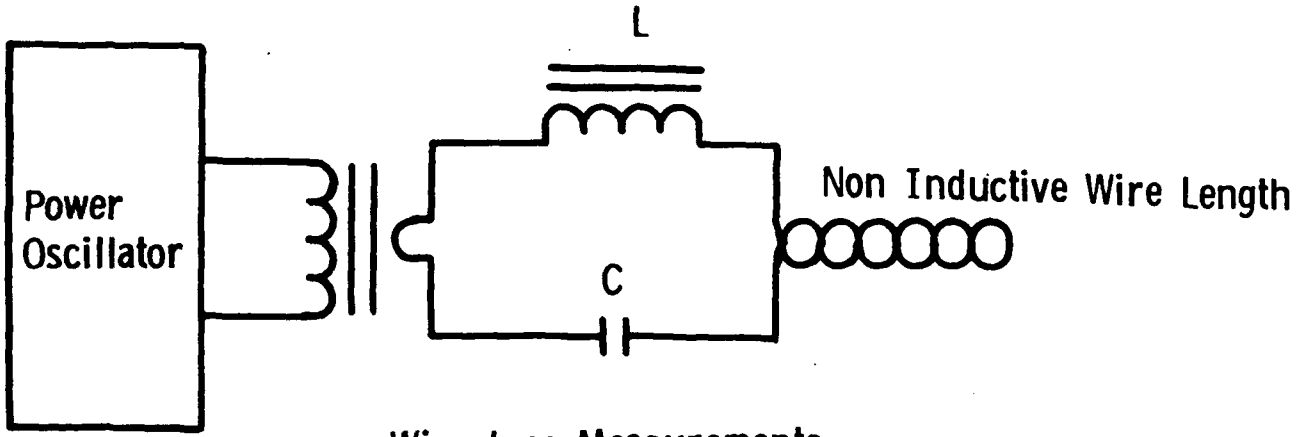
This test was repeated for a 10-foot length of #10 stranded wire. In both cases, the leads were measured on a wood work bench. Both loss measurements were repeated to determine if there was a change when the wire was taped to an aluminum chassis fabricated for the breadboard. The results are tabulated in Table D-II. From the results of the test, Litzendraht wire is recommended for the power connections.

Wire Sample 10 Foot	Power Loss	Calc. Loss	Difference	Additional Loss due to Metal Chassis
312/33	17.4W	16W	1.4W	2.7W
#10 Stranded	31.1W	14.4W	16.7W	2.8W

Table D-II. Losses in 10-Foot Wire Sample 39A RMS 25kHz

D.3 Capacitors

Extensive capacitor testing was performed to determine the capacitor dielectric construction that would operate reliably and efficiently at the higher operating frequencies and high peak currents for the series resonant inverter. The same resonant tank test shown in Figure D-22 was used to determine losses. The series resonant capacitor does not present a technology problem at this time, both high current and low loss characteristics are obtained without any weight penalty. Foil polypropylene capacitors are recommended for this application.



Wire Loss Measurements

Figure D-27

The high voltage output filter is not causing any penalty. Both low weight and reliable operation has been demonstrated. Metalized polypropylene is used. No failures have occurred but repeated discharge of the capacitor into an engine arc can degrade the internal lead connection and cause increased losses.

The low voltage output filters use conventional tantalum capacitors.

Because of the 400V input and high ac current for the input filter capacitor, tantalum capacitors can not be used for the design.

D.3.1 Series Resonant

The following is a list of capacitor types that were evaluated for the series resonant capacitor:

Teflon	- Foil
Polystyrene	- Foil
Teflon	- Metallized
Polypropylene	- Foil
Polysulfone	- Foil
Polycarbonate	- Foil

Polypropylene foil is the type that is presently being used in the design. Some comments of other capacitor dielectrics are approximate because the list includes several promising candidates in addition to the polypropylene dielectric.

A teflon foil capacitor would appear to have an order of magnitude lower loss than the polypropylene, but it has two disadvantages which require investigation if it is to replace the polypropylene. Teflon has the characteristic that it will sublime in the presence of corona leading to early catastrophic failure. This potential problem can be controlled by a well designed and manufactured unit hermetically sealed, completely impregnated, and wetted in a suitable low loss fluid. The second teflon characteristic problem is that it is an extremely high cost material which is difficult to process into a thin pinhole-free dielectric film. Because it is so expensive, its use is limited to low quantity units which almost precludes the high reliability attendant with quantity production by many

vendors. The first problem can be controlled by a suitable corona test which is recommended for any capacitor in this application. Unfortunately, the corona test is not a standard test, and most vendors are not set up to perform it. The second problem can be overcome by favorable results of statistical sample testing. It is recommended that further investigation be made to obtain teflon capacitors for this application. This investigation is to be made concurrent with the polypropylene procurement, and replacement, if possible, to be made on a form and fit one-for-one basis.

Polystyrene dielectric is limited to 85°C with derating and is full rated to 65°C. This temperature limit is inconsistent with this program requirement because the radiating heat sink would have to grow in size and weight to accommodate this lower operating temperature.

Polysulfone is an especially interesting material because it has a higher dielectric strength than polypropylene. Its full rated temperature is as good and may be better, but at the present time, it does not enjoy the vendor acceptance or experience that polypropylene has because it is a newer material.

Polycarbonate dielectric exhibits some 5 times the loss of other acceptable materials. Its interest lies in filtering applications where the ac ripple current losses will not impact on efficiency. It is currently more promising than polysulfone for these applications only because it is a more popular material used by many vendors and is covered by MIL Spec up to 400V (MIL-C-39022).

A series of loss measurements was made determining the comparative input power required to excite the series resonant circuit to a specific level of circulating VA. The test circuit shown in Figure D-22 was used to determine capacitor losses. The same value of capacitance of the different dielectrics was used in the tests in order to improve accuracy of data. The absolute loss of one of the capacitors was established by a measurement of its temperature rise and its surface area. Table D-III compares the input power difference at 25kHz with a capacitor swing of 700V peak-to-peak. While the position in the table of the different dielectrics is reliable, the loss values are offered only as a guide.

Table D-III. Capacitor Loss Characteristics

Capacitor Dielectric	Watts Loss at 700V p-p 25kHz	% Dissipation in Resonant Circuit
Teflon-Foil	0.4	0.004
Polystyrene-Foil	2.4	0.024
Teflon-Metallized	4.8	0.047
Polypropylene-Foil	5.2	0.051
Polysulfone-Foil	5.2	0.051
Polycarbonate-Foil	28.0	0.28

These measurements were made on capacitors manufactured by Components Research Corporation of Santa Monica, California. The low losses listed above are possible because of the low resistance terminations found on these capacitors. We found this manufacturer to be competent, helpful, and cooperative beyond the usual vendor-user relationship.

It is interesting to note the performance of the metallized teflon capacitor versus the foil teflon capacitor. At a 39A rms level, there was an additional loss of 4.4 watts due to the extra resistance of the metallized conductor thickness of 1 to 2 millionths of an inch compared to the foil thickness of 170 to 250 millionths of an inch, some 2 orders of magnitude different. This corresponds to less than three milliohms resistance and substantiates the decision to use metallized dielectric construction for low ac applications.

The present dielectric and conductor choice is polyprop lene-foil which was chosen because it is full rated to 125°C; it is a low-loss capacitor; it is an established dielectric film made by more than one manufacturer in large quantities; it is processed into capacitors by several reliable vendors; and it is consistent with the program low-weight requirements.

Figure D-28 shows the series resonant capacitor used in the beam supply. It is a hermetic sealed unit.

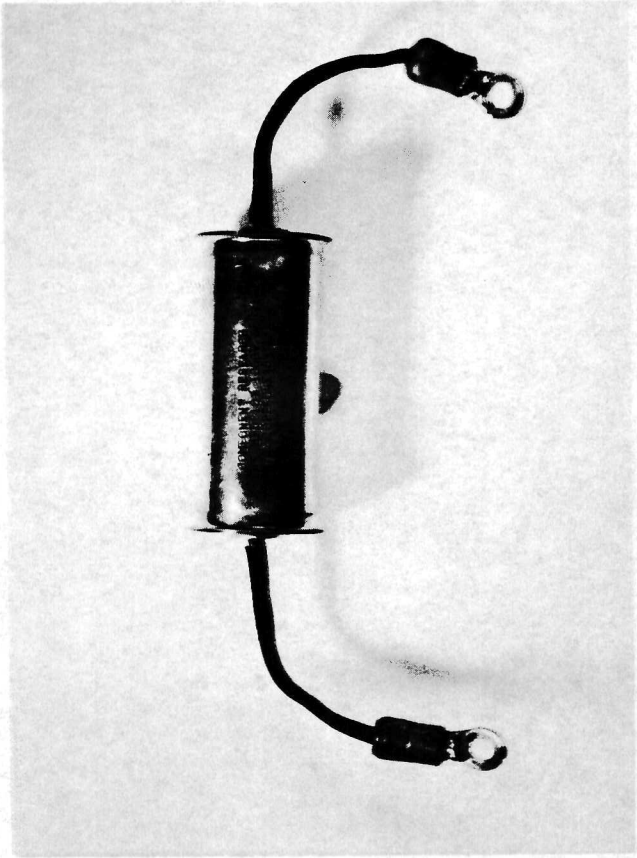


Figure D -28

Series Resonant Capacitor (Beam Supply)

0.5μFd @ 100V
61 gms, 2.5cm diam x 6.2 cm

Figure D -29

Beam Supply High Voltage Output Capacitors

0.5μFd @ 2400V
150 gms, 3.9 cm diam x 8.8 cm

A resonant circuit power loss measurement indicated a threefold increase in power loss for the oil-filled sealed polypropolene capacitor when compared to the dry encased capacitor. The loss was traced to the ferromagnetic bands of the compression hermetic seal which were generating eddy current losses because they were coupled to the single turn of capacitor lead generating some 9 watts of eddy current losses at 25kHz when 39A rms was flowing through the single turn. This seal is to be changed by the manufacturer to a metallized ceramic seal. While investigating the source of this loss, the capacitors were temperature cycled from -55°C to +65°C for ten cycles and measured before and after the cycles. There was no measured change in capacitance, internal resistance, dissipation constant, or loss measurement.

D.3.2 High Voltage Output Filter Capacitors

Studies on the component requirements, the type of dielectric and manufactures have been performed for the beam output filter capacitors. The unit must filter the high frequency ac current from the beam output power transformer to less than 5% peak ripple voltage. The 0.5μFd, 2400V capacitor shown in Figure D-29 meets the output filtering requirement. The unit used metallized polypropylene dielectric and is manufactured by Plastic Capacitor, which has experience in the high voltage capacitor field.

A rating that is not covered is the discharge rate of the capacitor. During the ion engine/power processor integration testing, a large number of overloads were presented to the power supply and its output filter. These overloads caused a large discharge current from the capacitor. The output current limiting resistor in the power processor limit the value to 200A peak. Can the capacitor have long life when subjected to this type of operation? The high current flow in the connection between the foils can dissipate a high peak energy and cause internal opens. Note that there has not been any failures of the component, but this is a new requirement that must be satisfied in the component application in order to ensure power processor reliability.

D.3.3 Low Voltage Output Filter Capacitors

Tantalum foil and slug capacitors are used on all low voltage output filters. The main design requirement is to ensure it has the correct ac current rating to filter ac current from the respective series resonant inverter. In the high output current supplies, many parallel units were used which degrade the reliability because of the increased part count.

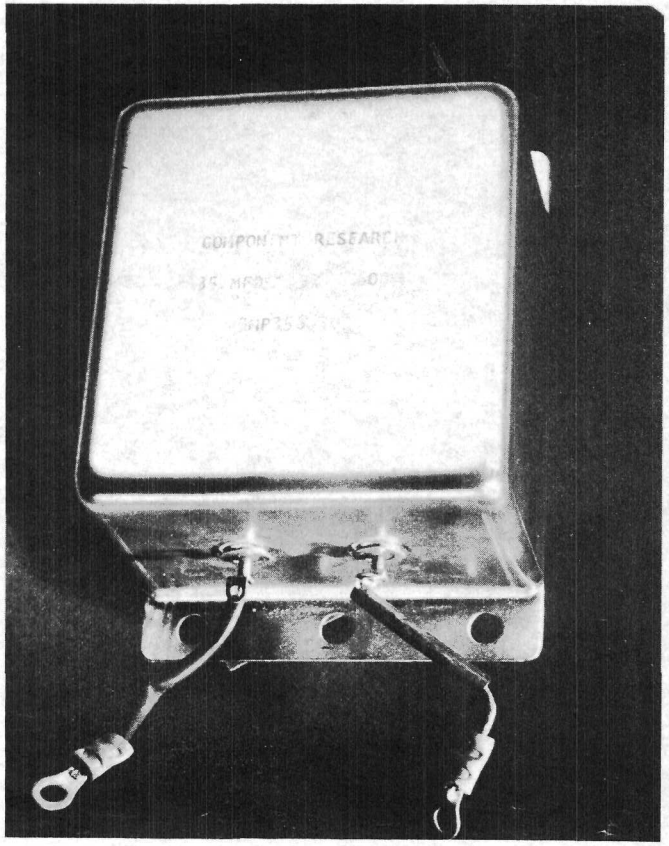
D.3.4 Input Filter Capacitors

Because of the 400V maximum input to the power processor standard tantalum capacitors cannot be used because of 450V maximum rating which does not allow any component derating.

The input filter of the power processor used a two stage filter design to attenuate the ac current drawn by the power inverter and to control the expected ac modulation of the solar array power bus by the different power processor and equipment loads.

The present filter design uses 70μFd for the first stage and 16μFd for the second stage. Four 4μFd foil polycarbonate capacitors are used for the second stage, one each is mounted at the input terminals for the arc and multiple inverter and 2 units are mounted at the input to the beam inverter. These units supply the high ac current drawn by the respective inverters.

The second stage filter inductor reduces the current magnitude to the first stage filter capacitors and therefore their ac requirement is greatly reduced. Figure D-30a shows a 35μFd 600V polycarbonate foil type capacitor, first used for the filter capacitor. The total weight for two units is 874 grams. The component has excessive ac current capability and therefore, a capacitor redesign was performed. Figure D-30b shows a 25μFd, 600V metallized polycarbonate capacitor, developed by Component Research. The total weight of 3 units of the first stage filter capacitor is 531 grams, a net savings of 343 grams.



(a) Polycarbonate-foil
35μFd @ 600V
437 gm, 8.5 cm x 8 cm x 5.3cm

(b) Polycarbonate-metallized
25μFd @ 600V
177 gms, 5.1 cm diam x 8.5 cm

Figure D-30 Input Filter Capacitors

E. RELIABILITY ASSESSMENT

The power processor reliability can be greatly influenced by the power system mechanization which determines total part count, by the control of the component stress and derating, by the component application, by component manufacture control and by the method of system or internal redundancy implementation.

TRW Systems has been designing and developing power processing equipment for long life and high reliability space programs. Many design techniques have been developed to improve power conditioning reliability. In the following sections, general redundancy techniques, component failure and system configuration will be discussed and the reliability vs weight tradeoff data will also be presented for the ion engine power processor.

E.1 Methods of Reliability Improvement

Several conventional techniques are available to the power conditioner designer in maximizing the reliability of a power supply. These are:

a) The selection of circuits of inherently high reliability

b) The derating of parts with respect to thermal, electrical, and mechanical stresses

c) The selection and screening of parts

d) The implementation of redundancy in the system design

With proper parts application and screening, and with adequate derating with respect to thermal, mechanical, and electrical stresses, the possibility of a failure should be virtually eliminated with the exception of potential wearout failure modes. It was not the purpose of this study to investigate the realism of part failure rates when correct derating and proper parts application policies are followed. Whether attributable to undetected manufacturing defects or incorrectly calculated stress levels, the fact remains that failures in space applications have occurred.

Four basic approaches to implementing redundancy were considered for each type of unit: parallel, standby, quad, and majority voting. Each method has its own weight and efficiency penalty and interaction between systems.

The reliability equations and basic configuration for each are described in the following paragraphs:

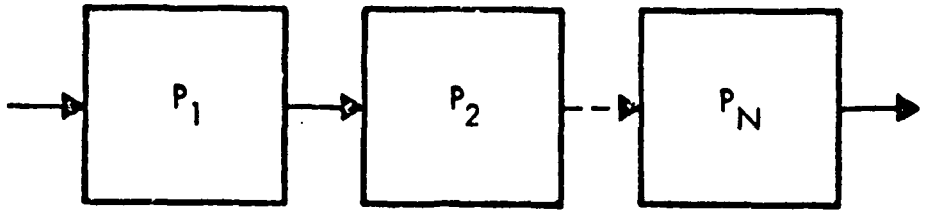


Figure E-1. Basic System Reliability Model

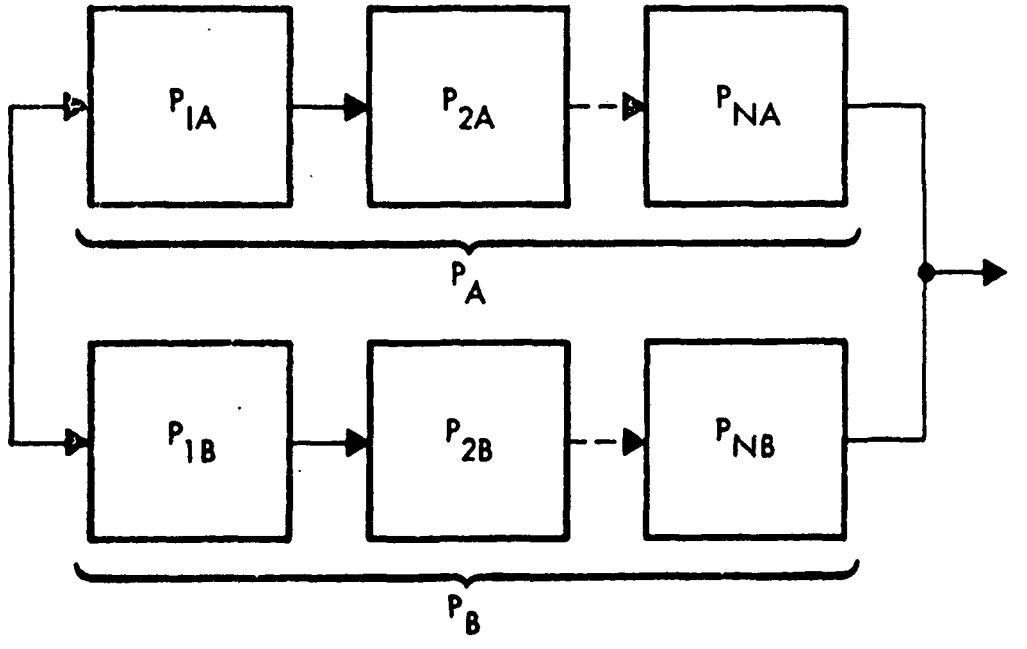


Figure E-2. Parallel Redundant System Reliability Model

a) Non-Redundant

Since each part of a nonredundant unit has its own failure rate, the general equation for the probability of survival is:

$$P_S = e^{-\lambda t}$$

where

P_S = probability of survival or reliability

λ = the summation of the failure rates for all parts

t = total operating time required.

Figure E-1 shows a basic system configuration of "N" elements in series. The equation for the probability of survival of the system is

$$P_S = P_1 \times P_2 \times - - - - \times P_n$$

where

$P_1 \rightarrow P_n$ are the reliabilities of each element.

b) Parallel Operating

Figure E-2 shows a parallel redundant system comprised of two groups of 1 through "N" series elements. Each of the two parallel groups is completely independent and either one can perform the required function.

The probability of survival is:

$$P_S = 1 - [(1-P_A)\ (1-P_B)]$$

where

P_A and P_B are the survival probabilities of the independent strings

Parallel operating channels have limited usage because there are some failure mode conditions which they cannot correct. For example, one of the two parallel channels could fail in a manner which causes their common output voltage to go above limits. But with higher power conditioning equipment, the parallel operating channels is becoming a standard method to improve the reliability with only minimal penalty in total weight. Work is progressing

slowly on the necessary sensing and fault clearing equipment for each module.

Another design problem area is the load sharing between modules and the influence on output ripple if one module is supplying all the output load.

c) Standby

In the standby redundant configuration of Figure E-3, there are two parallel channels, but only one is operating at any time. This configuration requires additional circuitry to sense a failure in the operating channel and a switching element to transfer to the standby elements in case of a primary element failure.

The equation for probability of survival is:

$$P_S = 1 - [(1-P_1P_{SW})(1-P_2P_{SW})]$$

where

P_1 and P_2 are the reliabilities of the independent channels, and

P_{SW} = the reliability of the failure sensing and switching elements

Standby redundancy is generally used for power circuits in low power units since it does not cause a significant loss in efficiency and there is only a minor weight penalty to the total power system. But in high power units, the standby redundancy techniques cause a large weight penalty for the redundant change and the input and output switchgear is not qualified for flight and is also heavy.

If a failure occurs in a power circuit; the failed power circuit is switched out and the standby circuit is energized to control the output power. This approach will produce an output transient during the switching interval. The failure-sensing circuits monitor the output voltage and generate the transfer signal if the output voltage is not within tolerance. A sufficient time delay is designed into the circuitry so that erroneous transfer is not allowed during start-up or load-switching transients.

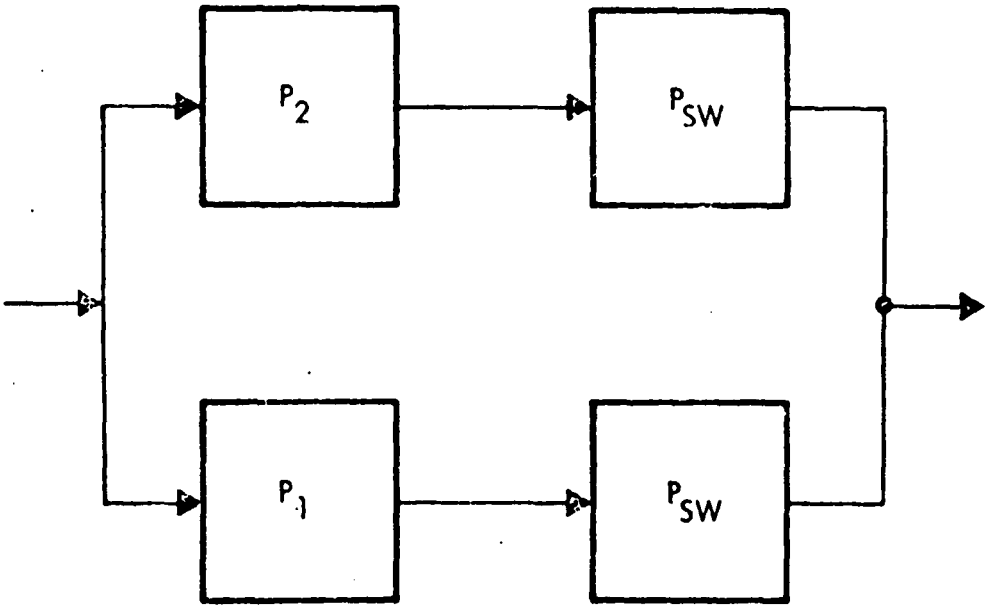


Figure E-3. Standby Redundant System Reliability Model

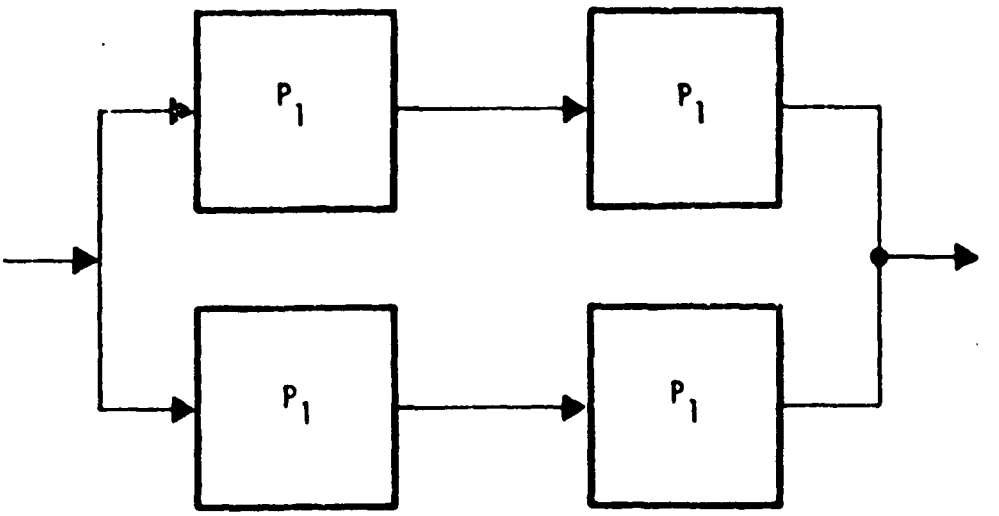


Figure E-4. Quad Redundant System Reliability Model

Standby redundancy cannot be used for all of these circuits because of the extreme difficulty in sensing a failure or out-of-tolerance condition on the propogation of failure to other components.

d) Quad

Quad redundancy is normally implemented at the part level and is illustrated in Figure E-4. Either string can perform the required function. The reliability of this configuration is:

$$P_S = 1 - (1-P_1^2)^2$$

where

P_1 = the reliability of a single part

The quad configuration is normally not used for series power handling circuits because of its poor efficiency. There are areas where the reliability must be improved and that takes these attendent weight and efficiency penalties.

The selected methods of implementing part redundancy are shown in Figure E-5.

The redundant transformer, Figure E-5a, consists of two series transformers with parallel primary and secondary windings which are interconnected. The parallel windings protect against open-circuit failures and the series transformers are used to protect against turn-to-turn shorts in one winding. The disadvantages of this approach are that each winding must be capable of full load current rating and also full input voltage rating. Each transformer is twice as large as a simple nonredundant transformer and the total VA rating of the magnetics is four times normal. The same technique is used for a choke but the effect of an inductance change to 50% of normal, should a winding develop a turn-to-turn short, must be considered in the design.

Figure E-5b shows a transistor and its redundant equivalent which is composed of two parallel strings of two transistors in series. If one series transistor develops a short, the remaining good transistor maintains normal operations. The diode in the base

circuit of the upper transistor protects against a collector to base short which could otherwise produce uncontrolled base current to the other transistors. The base resistors are needed to protect the current-driving signal source if a transistor base-to-emitter short develops and to cause current sharing among the four transistors.

The disadvantages of this configuration are that the normal current gain is reduced to one-half when used as a linear amplifier, and all four transistors must have the same power rating as the single nonredundant transistor. The system must be designed to accommodate wide variations in gain, both for normal and failure modes.

Figure E-5c shows the nonredundant and the redundant capacitor configurations. The redundant capacitor has two parallel strings of two series capacitors. Resistors are placed in parallel with the capacitors to cause equal division of voltage. This is particularly important for tantalum capacitors where a normal unbalance in leakage current can cause unequal division of voltage. This unbalance in voltage may produce voltage reversal on the capacitors during discharge and a resultant failure.

The disadvantages of this configuration are its increased size and weight and the fact that capacitance can vary from 0.5C to 1.5C. If not considered in the design, this variation can produce excessive ripple or regulator instability.

The normal failure mode of resistors is to drift, open or develop a partial short, and not a complete end-to-end short. The redundant resistor Figure E-5d is two resistors in parallel. The problem of the redundant resistor is its resistance variation under failure mode conditions.

The redundant diode configuration, Figure E-5e, contains two parallel strings of two diodes in series. The problem of the redundant diode is its increased power loss and change in output voltage when one diode shorts. The zener or reference diode cannot be implemented in this manner and still maintain the voltage accuracy required. Whenever a voltage must be sensed and compared

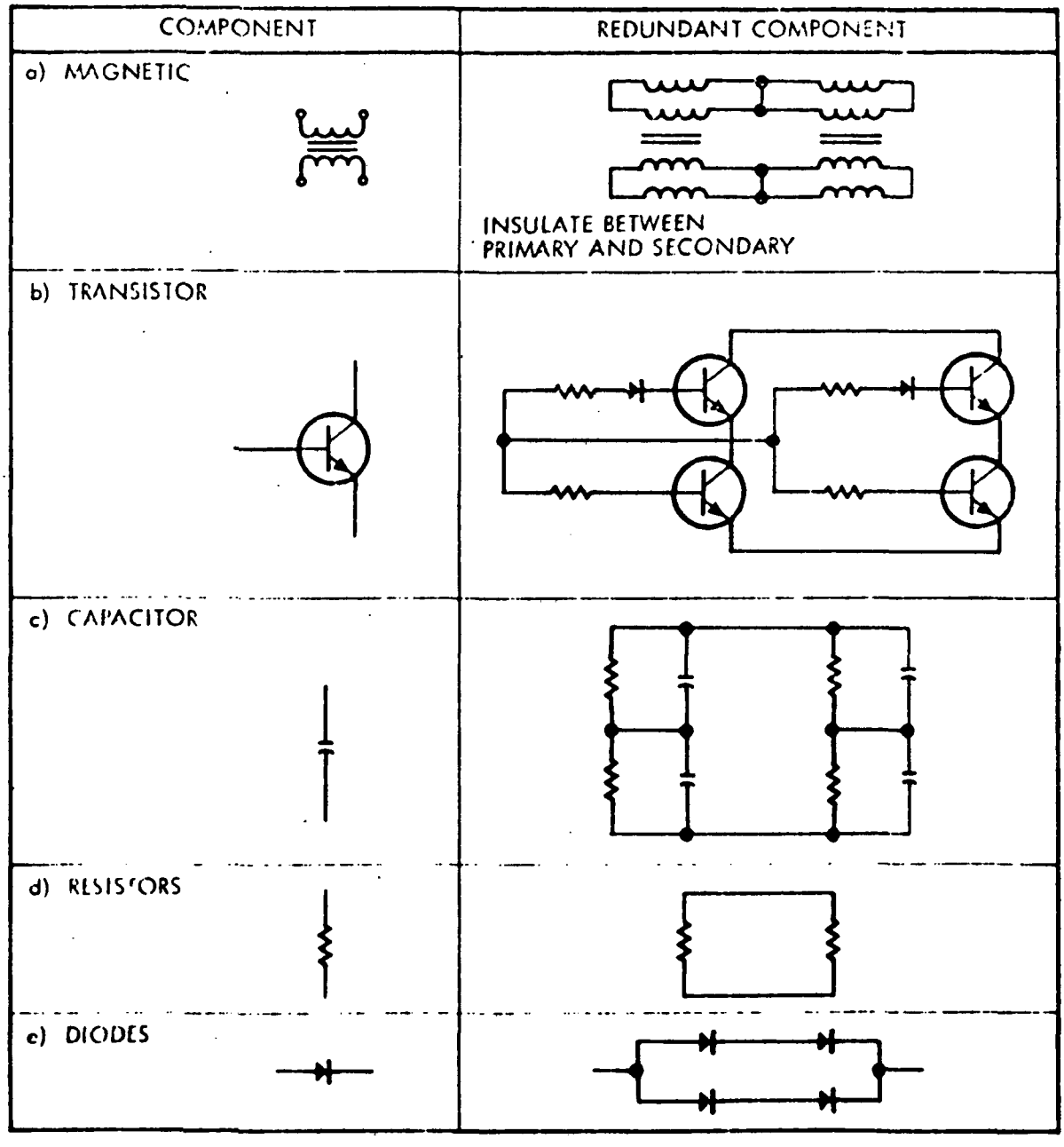


Figure E-5. Methods of Implementing Part Redundancy

to a reference in a redundant design, the majority voting circuit must be used to maintain a close regulation tolerance (± percent). A precision voltage divider also cannot be obtained by the quad redundant approach.

Relays for command and protection control are used in a circuit level majority voting redundant configuration.

e) Majority Voting

Figure E-6 shows a block diagram of a majority voting configuration. Two out of the three elements must be operative in order to perform the required function. The probability of survival is:

$$P_S = 1 - [(1-P_1P_2)(1-P_2P_3)(1-P_1P_3)]$$

where

P_1, P_2, and P_3 are the reliabilities of each element

In most cases $P_1 = P_2 = P_3$, therefore

$$P_S = 1 - (1-P_1^2)^3$$

Majority voting redundancy is generally applied to low-level signals, and logic circuitry.

The regulator amplifier design uses the majority voting configuration for the voltage sensing and error amplifying stages. Figure E-7 shows that the nonredundant configuration of the voltage sensing and error amplifier is composed of a voltage divider that reduces the magnitude of the sensed voltage to a level comparable to the reference, a precision voltage reference, a summing point, and an error amplifier stage. The redundant majority voting block diagram is illustrated in Figure E-8. It has three nonredundant parallel circuits plus three AND gates and an OR gate. Each AND gate receives two amplified signals, and if they are correct, the output signal is obtained. Both digital and analog signals can be controlled in this fashion except that with analog signals gain variations will appear depending on how many channels are operating within their linear range.

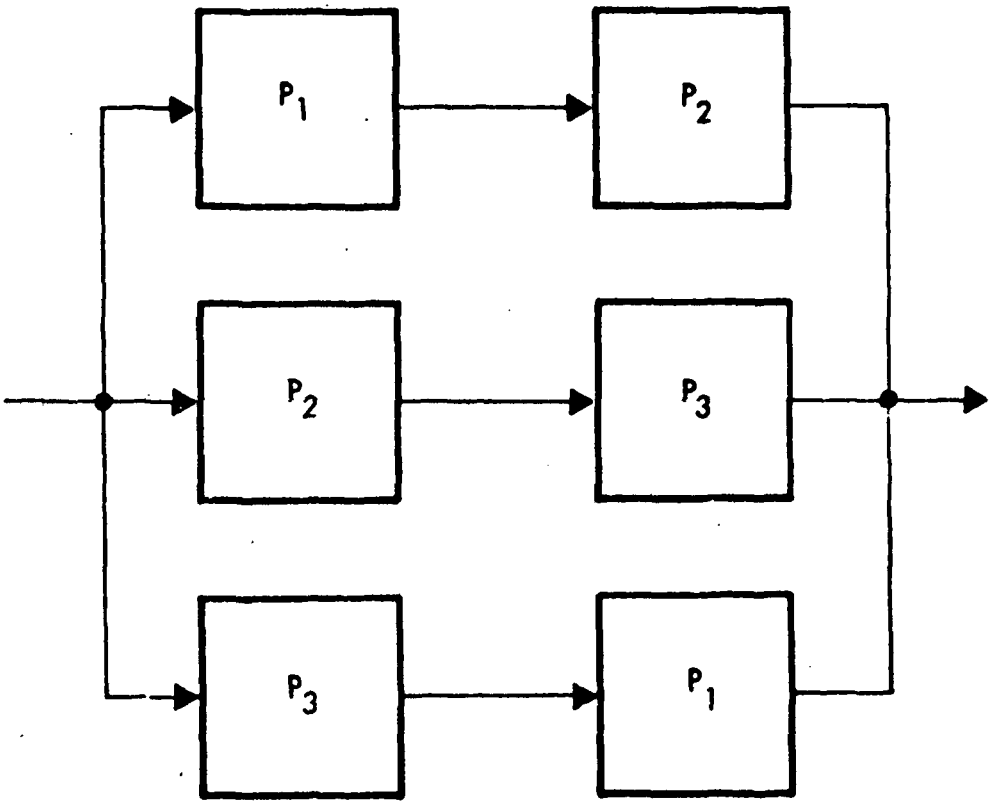


Figure E-6. Majority Voting System Reliability Model

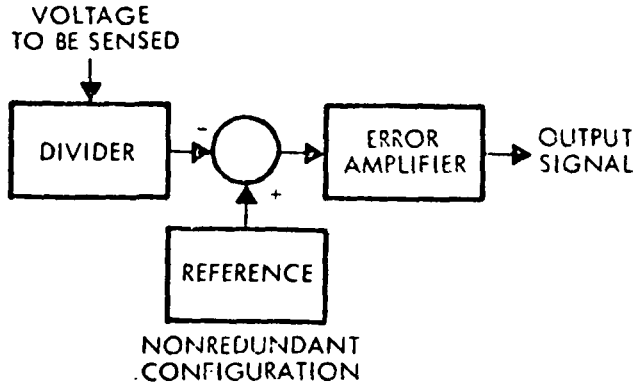


Figure E-7. Nonredundant Voltage Sensing and Error Amplifier Block Diagram

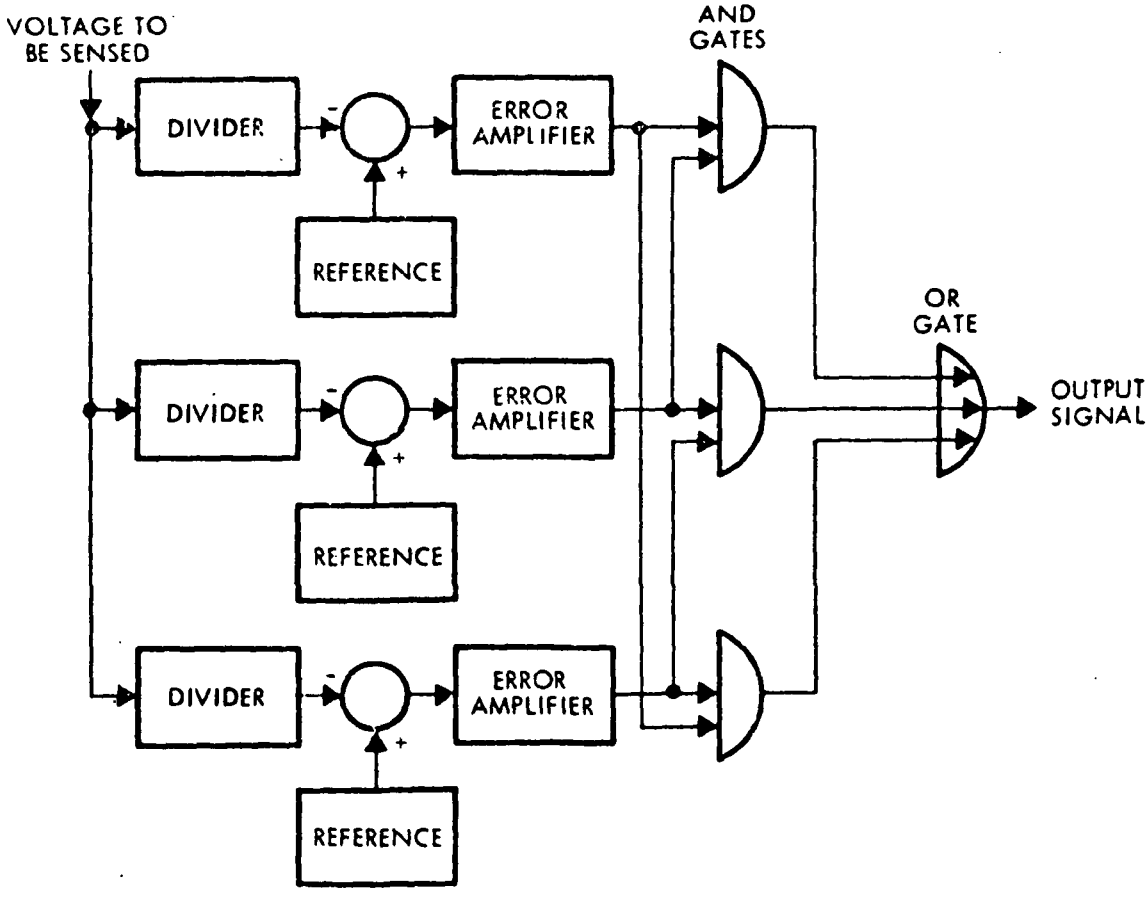


Figure E-8. Majority Voting Redundant Configuration of Voltage Sensing and Error Amplifier

E,2 Component Failure Rates

Reliability predictions are made at various stages of the system design process to provide maximum confidence of meeting the required system reliability, also for use in establishing reliability requirements for design specifications and in support of tradeoff studies and other evaluations made during the course of design. The validity of such reliability predictions depends heavily upon the use of meaningful failure rate data and resulting piece part failure rate estimates.

In applying a component, it must have adequate derating for each basic design parameter shown in Table E-1 both while operating at steady state or during transients such as startup and output overload. Failure rate data is based on correct component application. Failure rates for most electronic parts may be assumed constant as a function of time as long as the mission duration does not exceed the wearout life of the part, and adequate screening is employed to eliminate potential early failures; thus for such items, a single failure rate value provides the needed characterization of probable failure incidence. Wearout times are greatly in excess of any mission duration typically encountered by equipment of TRW design.

The failure probability and hence failure rate which an item will exhibit in a given application clearly depends upon the severity of the stresses, tolerances, etc., found in the application as compared with the design capability built into the device. Two factors frequently accounted for in adjusting failure rates for varying application conditions are:

(i) Temperature, either ambient or some critical temperature level internal to the device; and

(ii) some principal or critical stress parameter, the nature of which will vary depending upon the part. For electronic parts this stress is often voltage, current, or some allied characteristic central to the design of the part. The degree of stress is typically compared to device capability by expressing the actual stress as a percentage of the stress level for which the part is rated, i.e., 25% of rated stress.

TABLE E-1 SIGNIFICANT PART PARAMETERS

1. CAPACITORS

- DC Voltage
- AC Voltage
- Transient Voltage
- AC Current
- Temperature (thermal stress)
- Inverse Voltage (Electrolytic Only)
- Frequency

2. RESISTORS

- Continuous Power
- Transient Power
- Transient Duration
- Maximum Voltage
- Insulation Resistance
- Steady-State Temperature (thermal stress)
- Transient Temperature (thermal stress)

3. DIODES

- Forward Current
- Continuous Power
- Reverse Voltage
- Transient Power
- Transient Duration
- Steady-State Junction Temperature (thermal stress)
- Transient Junction Temperature (thermal stress)

4. TRANSISTORS

- Continuous Power
- Transient Power
- Transient Duration
- DC Collector Current
- AC Collector Current
- DC Base Current
- AC Base Current
- VCB
- VCE
- VEB
- Steady-state Junction Temperature (thermal stress)
- Transient Junction Temperature (thermal stress)
- VEBO
- V_{CEX}
- VCBO

5. SILICON-CONTROLLED RECTIFIERS (SCR)

- Repetitive Peak Reverse Voltage
- Transient Peak Reverse Voltage
- RMS Reverse Voltage
- Continuous Reverse DC Voltage
- Peak Forward Blocking Voltage
- Average Forward Current
- RMS Forward Current
- Peak Fault (surge) Current
- I squared load
- Gate Power Dissipation
- Steady-State Worst-Case Temperature (thermal stress)
- Transient Worst-Case Temperature (thermal stress)

6. TRANSFORMERS

- Primary voltage
- Primary Current
- Secondary Voltage
- Secondary Current
- Maximum Frequency
- Minimum Frequency
- Maximum Transient Primary Voltage
- Maximum Transient Secondary Voltage
- Insulation Resistance
- Hot Spot Temperature
- Maximum DC Primary Voltage

7. INDUCTORS

- Current (AC)
- Current (DC)
- Voltages
- Transient Voltages
- Insulation Resistance
- Minimum Frequency
- Maximum Frequency
- Hot Spot Temperarure
- Dielectric Strength

The ideal failure rate estimate would be based upon a large amount of statistically significant data collected in an application closely approximating the contemplated mission in stress and temperature levels. For at least one application, TRW has a source which fulfills many of these requirements. The 28 TRW space vehicles launched to date represent an extensive source of failure rate data for satellite mission (Reference 1 - Table E-II). The design philosophy employed in these equipments also renders these data valid as being representative of the nominal (30°C, 25% of rated stress level) conditions for which failure rates in this practice are specified. For many items, however, TRW space vehicles' orbiting history does not provide an adequate basis for failure rate estimation due to the small number of hours and/or number of failures which have been accumulated to date. In order to ensure the development of a representative list of failure rates, several other sources (References 2, 3, 4, 5, 6, 7, 8 and 9, Table E-II, have been consulted and a comparison of the respective estimates made.

The list of recommended failure rates presented in Table E -III represents an assimilation of such data sources. The principal source upon which each recommended value is based is shown for each entry. Finally the TRW Electronics Component Handbook has served as an overall source of qualitative and comparative data to ensure that a reasonable ordering of relative failure rate estimates exists among the several part types involved. Such relativism is particularly important when tradeoffs involving the use of several candidate part types are being considered.

This experience has been used as the most realistic basis for determining the failure rates of the generic part types. The selected failure rates represent a major assumption in the analysis of power system reliability.

Table E-IV lists the possible failure modes and relative percentages. In many cases component drift will not cause a power processor failure. In order to do a realistic reliability analysis, a failure mode and effects analysis must be performed.

TABLE E-11. REFERENCE FOR RELIABILITY DATA

1. 71-2286.1-019, 99900-7454-RO-00, "Orbital Reliability of TRW Spacecraft," by R. C. Billups and E. H. Barnett; February 1971

2. Failure Rate Data Handbook (FARADA), Bureau of Naval Weapons, U. S. Naval Ordance Laboratory, Corona, California.

3. NASA CR-84628, PRCR-948, "Study of Reliability Data from In-Flight Spacecraft," by E. E. Bean and C. E. Bloomquist; March 1967.

4. RADC TR-67-108, "RADC Reliability Notebook, Volume II," by D.M.Ryerson, S.L.Webster, and F.G.Albright; September 1967.

5. TRW Electronic Components Handbook (ECH).

6. 70-APS-118, "SSAPS Subtask B (Preliminary Design) Component Failure Rates," by R. A. Paulson; 24 November 1970.

7. 7423.4-052/70, "Failure Rate Determination for MOS-LSI Chips," by A. G. Linowiecki; 3 March 1970.

8. 7423.4-497, "Failure Rates of MOSFET IC's, J.E.deCastro; dated 19 October 1967.

9. 71.7534-5, "Gyro Reliability," by John Nicklas, 10 May 1971 (Confidential)

TABLE E-III

COMPONENT FAILURE RATES

Components	Failure Rate per 10^9 Hours
Capacitors:	
Ceramic	3
Ceramic 1000V	30
Polycarbonate	30
Polypropeline	30
Tantalum	20
Tantalum - Solid	14.4
Diodes:	
Signal	1.4
Power	36
Zener	14.4
Zener-Power	115
High Voltage	82
Integrated Circuits:	
Digital	25
Linear	50.4
Magnetics:	
Inductors	1
Inductors - AC Voltage	7.7
Transformer Signal	1.3
Transformer - Med Power	10.8
Transformer - High Power	35
Transformer - High Power & High Voltage	65
Relays:	
Magnetic Latch (Less than 10,000 cycles)	5
Non-Latch (Less than 10,000 cycles)	60
Resistors:	
Carbon Composition	1
Metal Film	1.4
Power Wire Wound	18
Potentiometer	1.4
High Voltage	18
SCR:	
Low Power	100
High Power	125
Transistors:	
Signal	3.6
Medium Power	7.2

TABLE E-IV PART FAILURE MODES

Part Type	Shorts (%)	Opens (%)	Drift (%)	Drift Causes
Capacitors (fixed)				
Ceramic	44	44	12	ΔC, power factor,
Paper - plastic/plastic	17	25	58	insulation resistance, dielectric strength,
Tantalum foil	10	20	70	mechanical
Solid Tantalum	70	14	16	
Glass/mica	50	30	20	
Resistors				
Carbon film	--	60	40	ΔR, intermittent,
Carbon composition	--	50	50	insulation resistance,
Wirewound	5	35	60	dielectric strength
Variable (Wirewound/composition)	7	23	70	
Inductive Devices				
Coil	3	5	92	ΔL, ΔQ, ΔR, Δ rise time,
Transformer (< 0.5W)	25	10	65	insulation resistance, intermittent,
(.5 - 10W)	--	89	11	dielectric strength
(10 - 1000W)	15	10	75	
Diodes				
Silicon (Alloy and diffused)	40	30	30	ΔI_R, Δr, ΔV_Z (zeners),
Germanium (Alloy and diffused)	6	78	16	mechanical
Zener (Silicon)	15	5	80	
SCR	10	--	90	
Transistors				
Silicon (< 1W)	10	30	60	hfe, I_{EBO}, V_{CE}, V_{CB},
(1 - 10W)	50	35	15	mechanical, noise, intermittent
(> 10W)	60	35	5	
Germanium (≤ 1W)	60	25	15	

E.3 Power Processor System Configurations

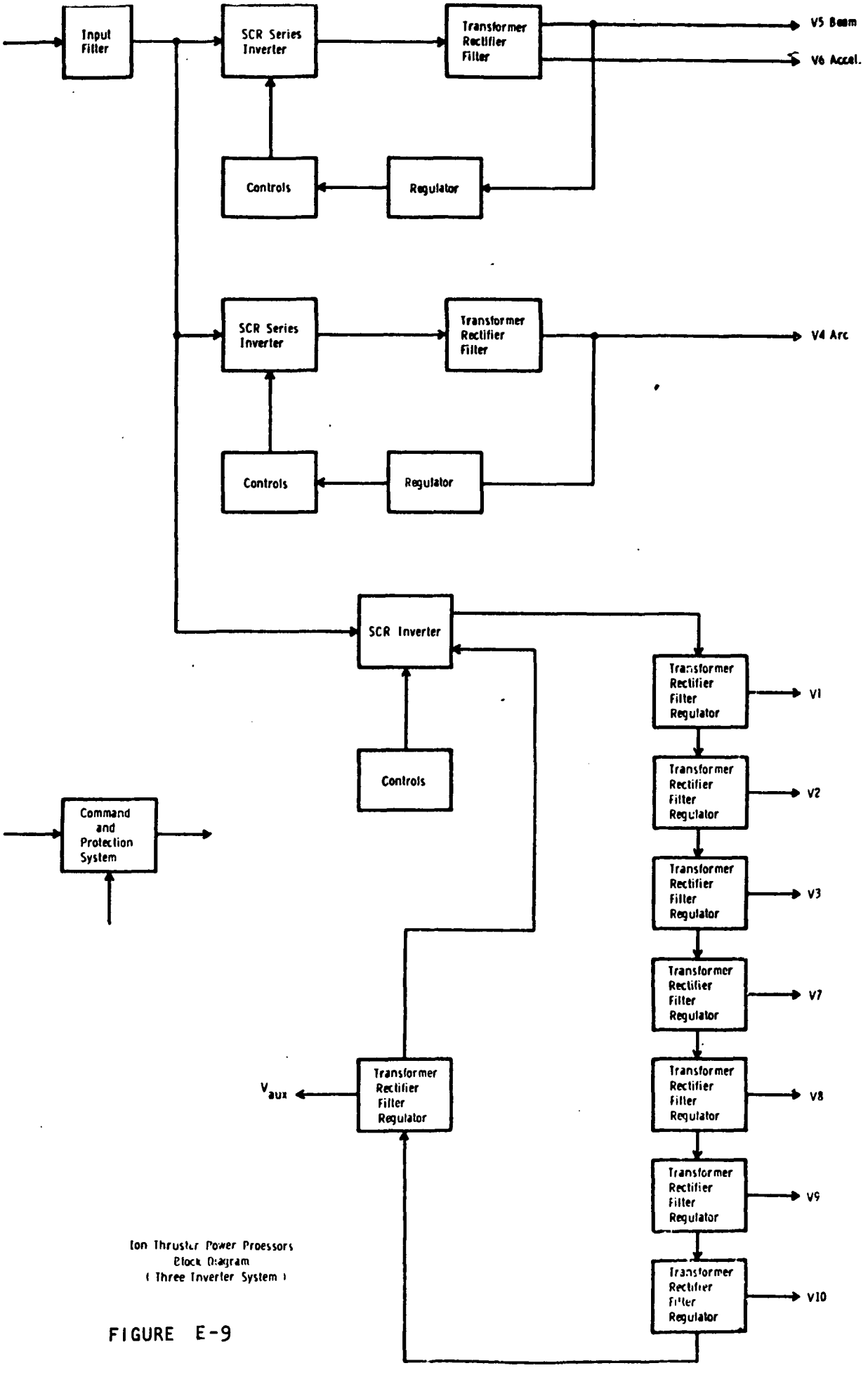
Because of the complex nature of the ion thruster power processor, it can be mechanized in many configurations. Each configuration has both advantages and disadvantages when trading off weight, efficiency, part count, and reliability.

The power system can be mechanized in three basic configurations, single, two or three SCR series inverters to processor the input 200-400Vdc bus to meet the ten different output requirements (V_1 through V_{10}).

Figure E-9 illustrates the block diagram that was mechanized under contract NAS12-2183 and NAS3-1438. It contains three SCR series inverters, one inverter for the beam and accel supplies (V_5 and V_6) at a power level of 2000 watts, a second inverter for the arc supply V_4 and a third unit, multiple output inverter which contained the remaining seven outputs for the ion engine and an auxiliary power supply for the internal control circuits. The command and protection system processes all the input commands to control the turn on and turn off sequence and engine protection during arcs for the ion engine. This system provides the maximum efficiency over wide load variations and maximum flexibility to changes in the sequencing and control of output voltages to the ion engine. A detailed discussion of the block diagram is contained in Section 3.

In performing the reliability study of the power processor, alternate power system configurations were identified. The main goal of the alternate configurations was to improve the non-redundant configuration by minimizing the number of power components whose reliability is difficult to improve without great penalty in efficiency and weight.

Figure E.-10 illustrates the block diagram of the power processor system using a single high power inverter to supply all the outputs of the ion engine. Each output has its own output power transformer, rectifier, filter and output regulator circuit. The inverter runs at its maximum frequency at all times and provides a constant ac current to all the load transformers. The method of regulation of output power is to short the power transformer and terminate any additional power flow to the load. The same command protection system processes the commands and protects the engine during overload conditions.



Ion Thruster Power Processors
Block Diagram
(Three Inverter System)

FIGURE E-9

Figure E-11 illustrates the mechanization using two series inverters. One inverter supplies the beam and accel supplies (V5 and V6) and the second inverter contains the remainder of the outputs in a single multiple output inverter design.

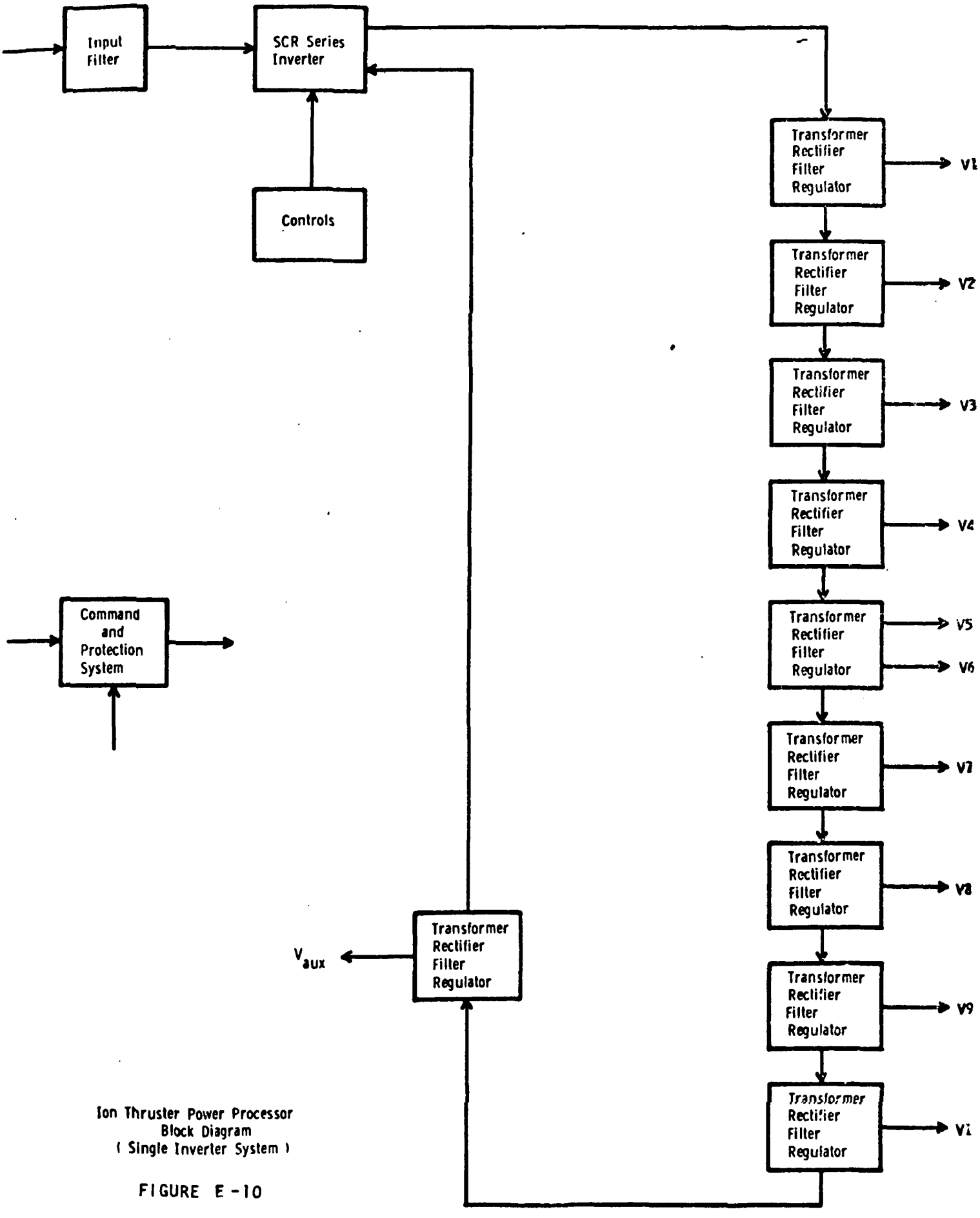
Figure E-12 shows the estimated efficiency of the three configurations as a function of output power. All three systems obtain approximately the same efficiency at full power with the single inverter slightly more efficient since it has only one SCR control logic circuit and no bias driver power requirements for transformer excitation to balance the current waveforms. The single and two inverter system have more losses at the lower output power levels in that the multiple inverters are operating at a high current level to satisfy the maximum power output. These losses in the inverter remain almost constant with large changes in output power level.

Figure E-12 also shows the packaged weight estimate for the three power processor configurations. Actually, spacecraft system studies must be performed to identify the optimum configurations. Preliminary studies indicate that the efficiency should be maximized over a wide range of output power level because of the throttling requirement for the electric propulsion engines in order to operate the solar array at the maximum power point. More complete studies are needed to tradeoff power processor weight, efficiency and reliability for the different power processor configurations, spacecraft applications and ion engine throttling range.

Figure E-13 illustrates the reliability block diagram of the baseline power processor design using three SCR series inverters to provide the output power requirements. The system is divided up into this grouping to aid in the redundancy improvement study that will be discussed later. Each block of Figure E-9 falls into one of the three basic categories of control circuits, intermediate power circuits, and power circuits.

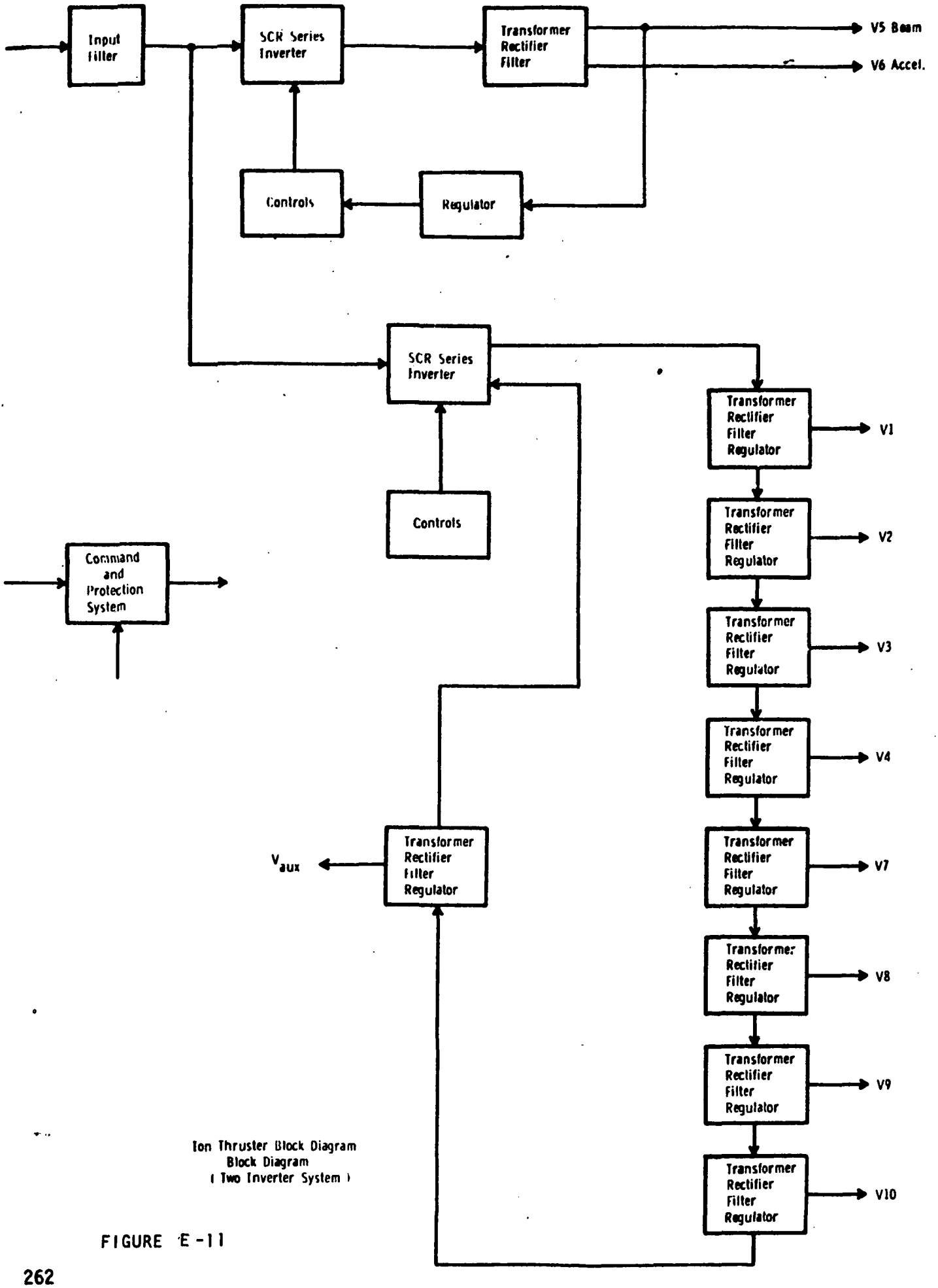
The control circuits include the following items:

1. Command and Protection System
2. Beam Inverter Control Logic
3. Beam Regulator
4. Arc Inverter Control Logic
5. Arc Regulator
6. Multiple Inverter Control Logic
7. V1, V2, V3, V7, V8, V9, V10 Output Regulators
8. Auxiliary Output Regulator



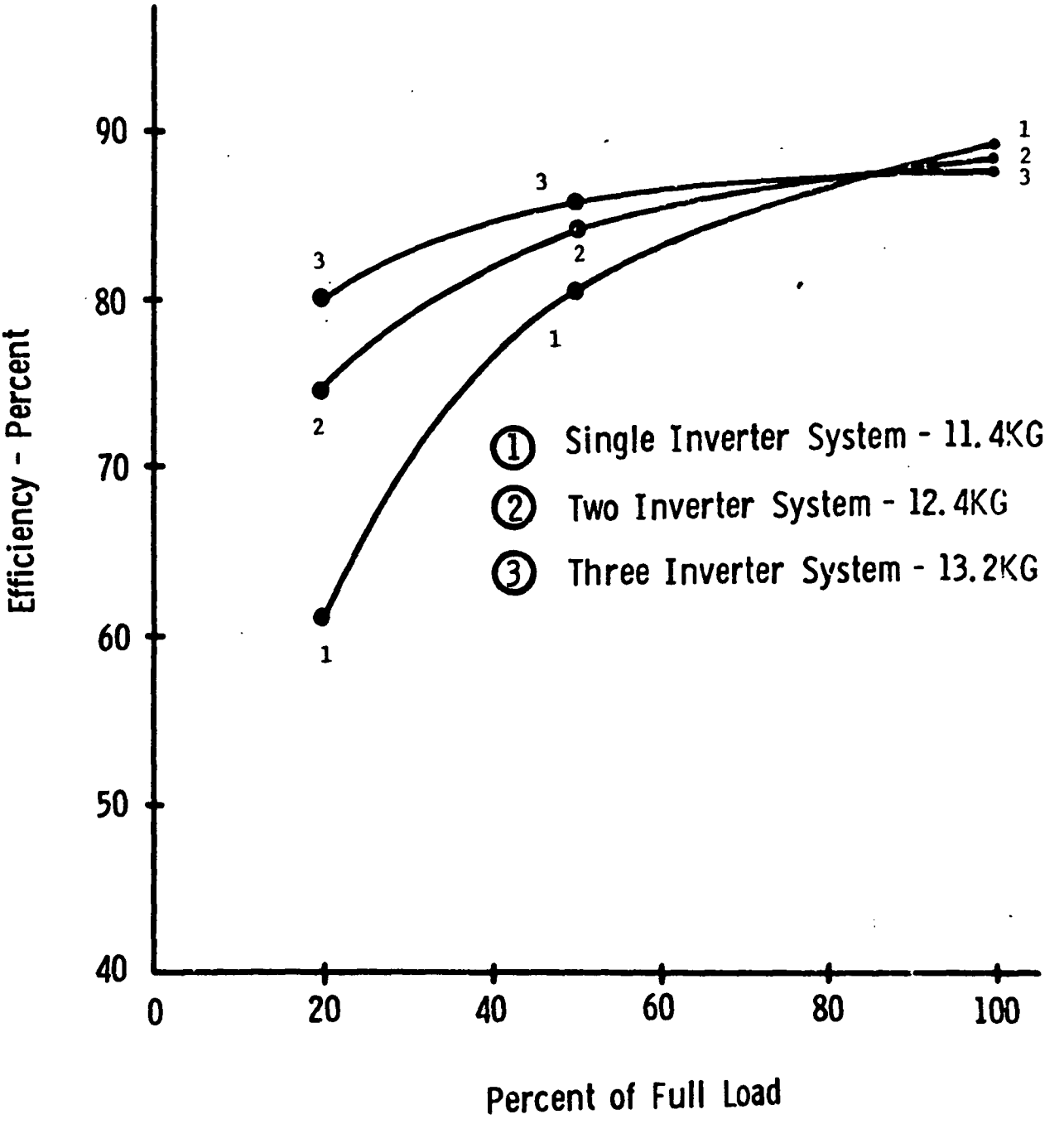
Ion Thruster Power Processor
Block Diagram
(Single Inverter System)

FIGURE E-10



Ion Thruster Block Diagram
Block Diagram
(Two Inverter System)

FIGURE E-11



System Operating Efficiency As
A Function Of Operating Power Level

FIGURE E-12

The intermediate power circuits include:

1. Beam SCR firing circuit
2. Arc SCR firing circuit
3. Multiple SCR firing circuit

The power circuits include:

1. Input filter
2. Beam inverter power stage
3. Beam output power circuitry
4. Arc inverter power stage
5. Arc output power circuitry
6. Multiple output series inverter power stage
7. V1, V2, V3, V7, V8, V9, V10 output power circuitry

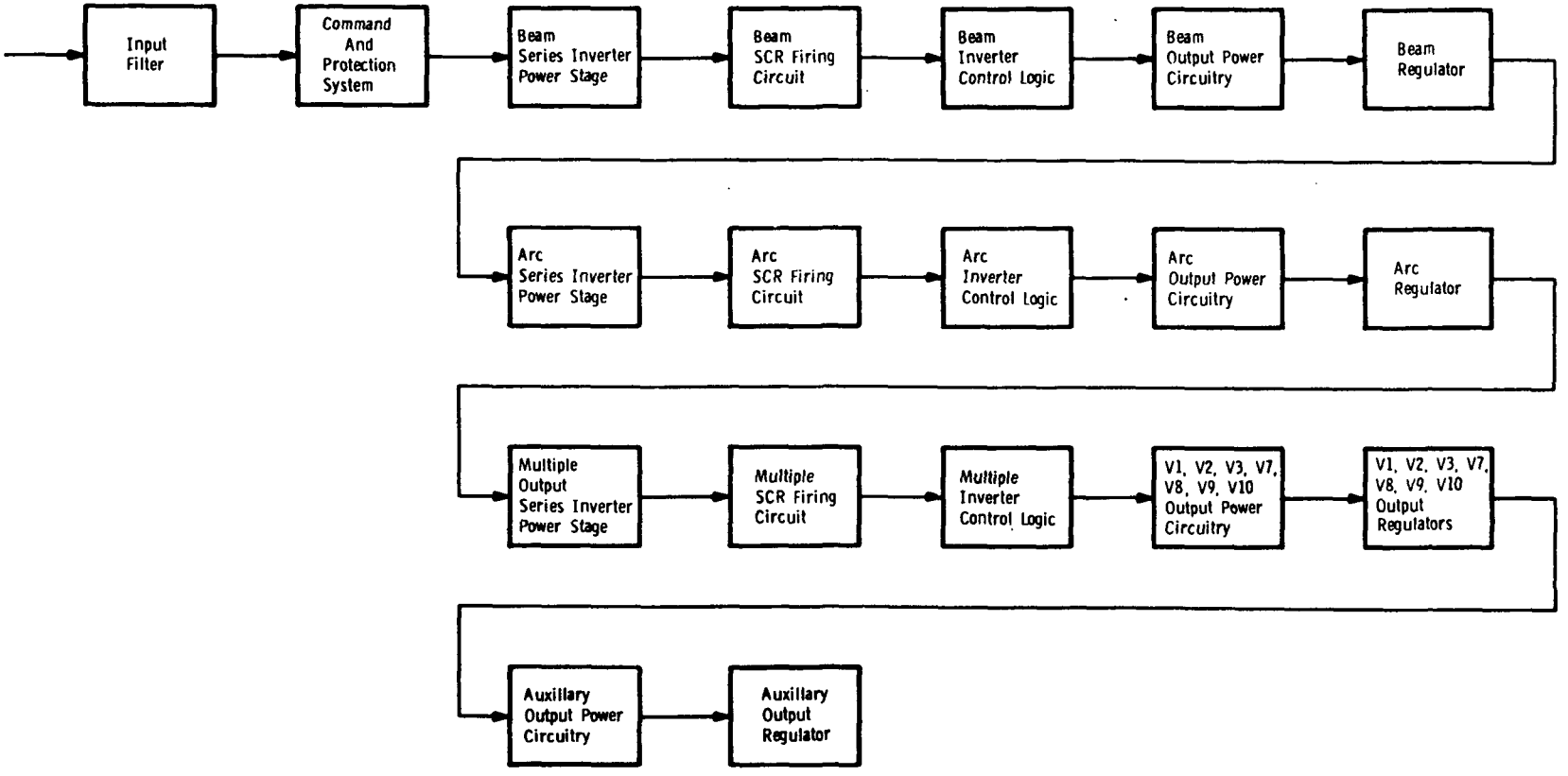
Failure rates were accumulated for each function and the total reliability determined.

The single inverter power processor configuration, as shown in Figure E-10, was selected as an alternate approach in order to determine relative reliability improvement between the two different power system approaches. A reliability block diagram similar to Figure E-13 was generated.

E.4 Reliability Tradeoff Study

Specific methods of implementing redundancy in the units of the various systems have been reviewed for the system optimization analyses. The investigations included consideration of the failure modes of each type of unit, the effects of unit failures on system operation and the effects of implementing redundancy on unit weight and performance.

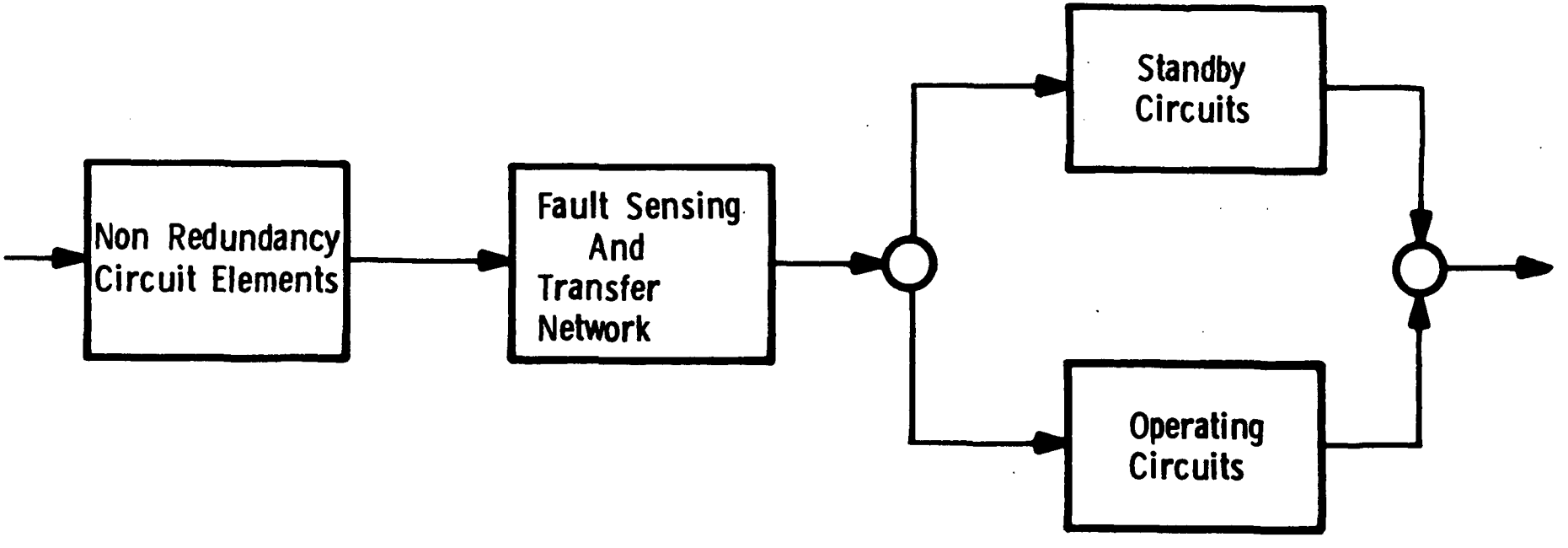
Figures E-14 and E-15 show the simplified block diagrams for the two basic approaches of standby redundancy and majority voting redundancy. In Figure E-14 an extra function block has been added to sense failure of the operating circuits and cause a transfer to the redundant non-operating channel. This technique has the advantage of lower overall part count and lower losses but has a disadvantage, that time delay of up to 5 to 10ms could exist where there would be no power or loss of control circuit (over-voltage condition).



Baseline Reliability Block Diagram

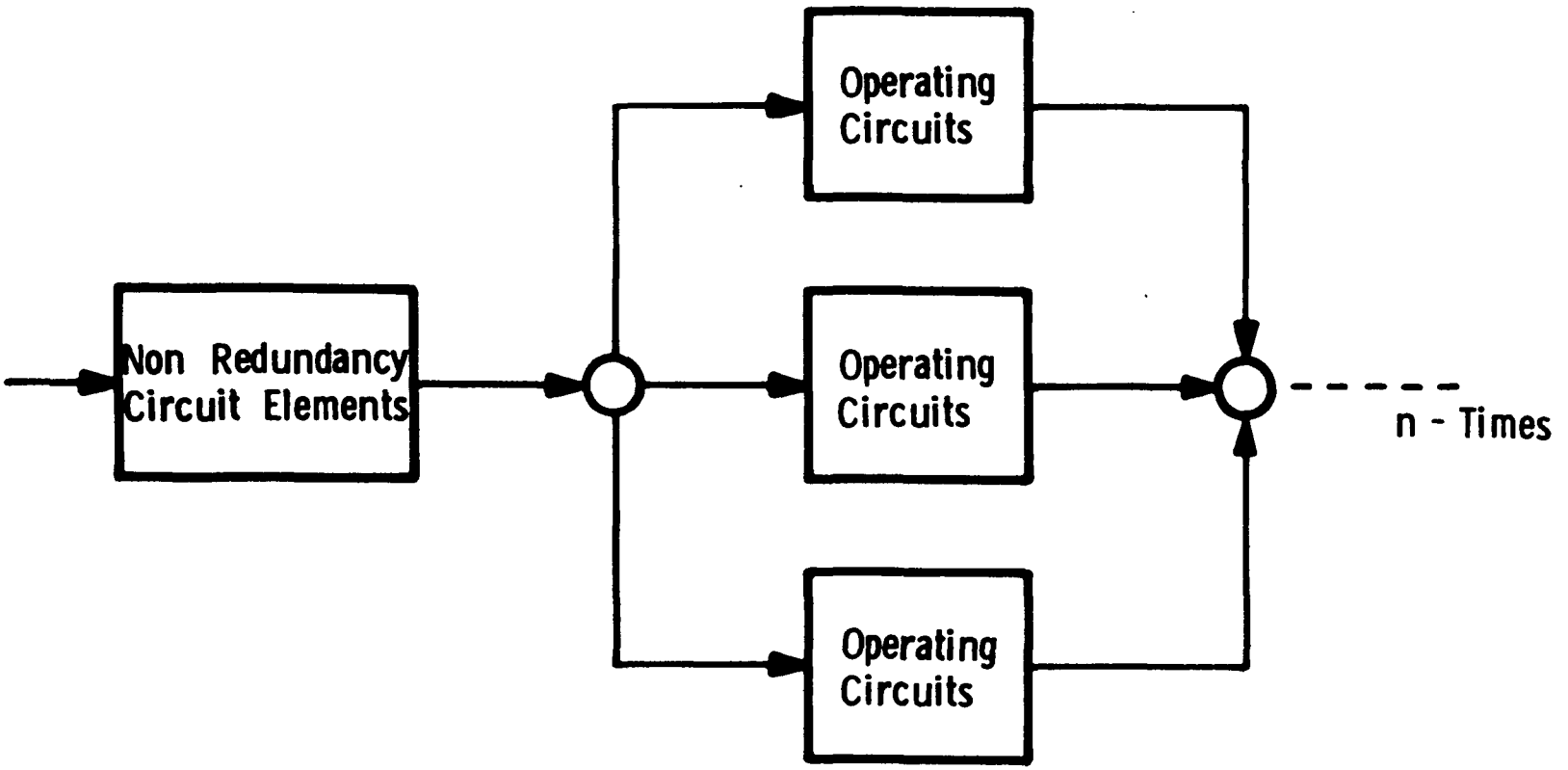
(Non Redundant 3 Inverter System)

FIGURE E-13



Standby Redundancy Block Diagram

FIGURE E-14



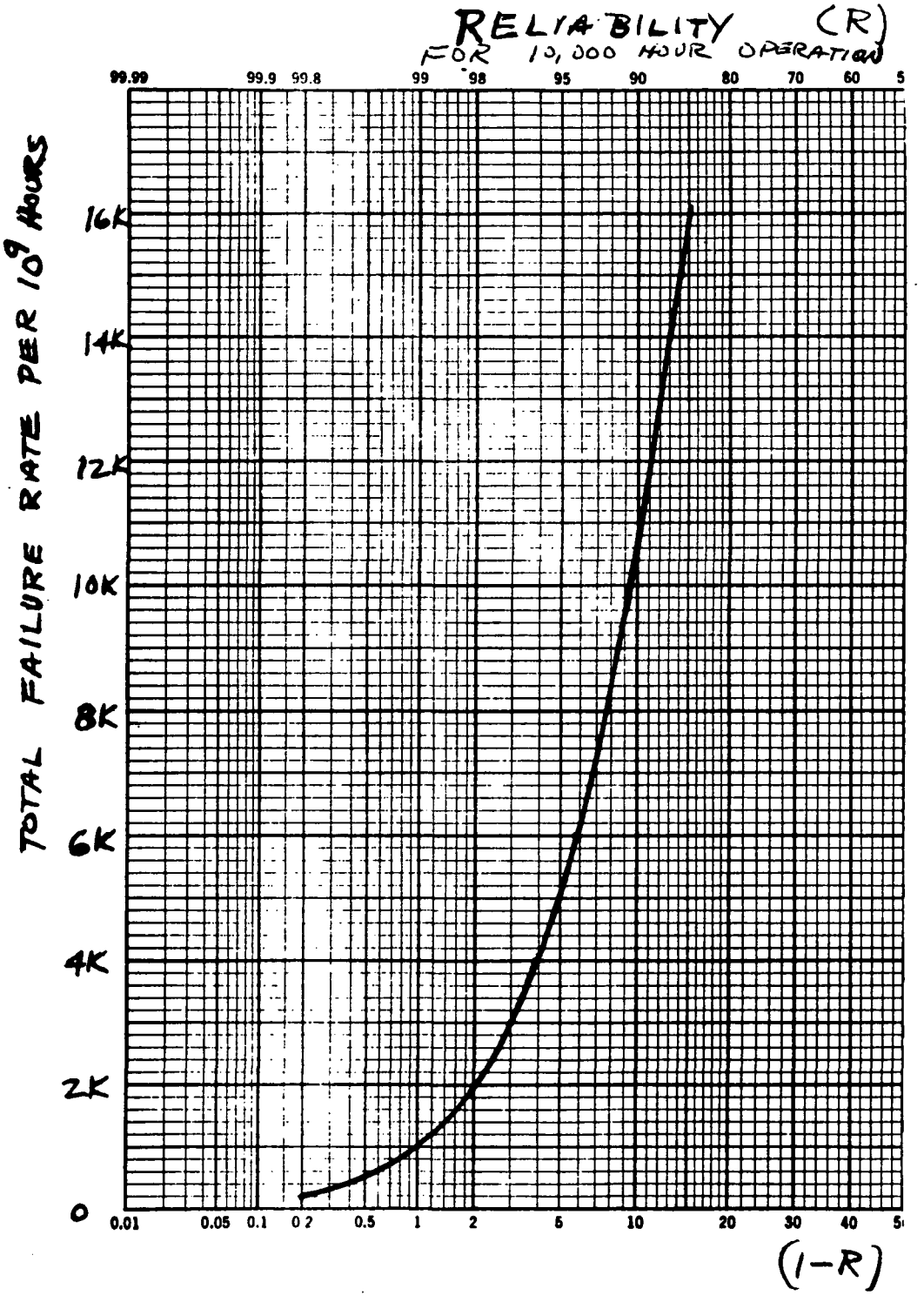
Majority Voting Block Diagram

FIGURE E-15

TABLE E-V

SUMMARY OF REDUNDANCY CONFIGURATIONS FOR THREE INVERTER SYSTEM

ITEM	-FR (Failure per 10^{-9} hours)	+ΔWt for Components Grams	+Δ Loss Watts	+Δ Wt for losses Grams	+Δ Wt Total Grams	$\frac{\Delta \text{ wt}}{\Delta \text{ FR}}$
Inverter Control Logic (MV)	962	385	8			
For Three Inverters	2886	1155	24	720	1875	.65
Beam Regulator (MV)	244	390	1.2	36	426	1.75
Arc Regulator (MV)	229	345	1.2	36	381	1.65
Multiple Output Regulators (MV) V_1 V_2 V_3, V_7, V_8, V_9, V_{10}	1890	930	5.6	170	1100	.58
SCR Firing Circuit (quad)	262	450	0.5			
For Three Inverters	786	1350	1.5	45	1395	1.03
Auxiliary Power Circuit (MV)	484	305	2.5	75	380	1.25
and Output Regulator (MV)	524	518	2.0	60	578	1.11
TOTAL	7043	4993	38.0	1140	6133	0.87



FAILURE RATE VS. RELIABILITY

FIGURE E-16

Figure E-15 is the majority voting configuration where instantaneous response to failure is obtained with a disadvantage of higher overall part count and higher losses for the other two operating channels.

Table E-III lists the different components used in the power processor design and its failure rate used in performing the reliability analysis.

Table E-V was generated to determine selected areas of redundancy that could be incorporated without any great penalty in weight or efficiency. From this table, majority voting redundancy for the beam, arc and multiple output was selected in that it provides the least amount of power loss. These areas of redundancy will be incorporated in the 20CM Engineering Model Breadboard Design and the total reliability will be updated.

The reliability goal for the power processor is 0.96 for 10,000 hours operation. Figure E-16 shows the failure rate as a function of reliability for 10,000 hours. To reach 0.96, the failure rate must be reduced to 4,000 failures per 10^9 hours or a mean time between failure of 250,000 hours. To reduce the failure rate of the power processor, it is necessary first to simplify the circuitry and then apply the redundancy techniques that will improve the reliability without a great penalty in weight or efficiency.

Figure E-17 shows the weight vs. reliability for the different redundancy configurations for the baseline or three inverter approach. These configurations include the following:

Code 30	No Redundancy
Code 31	Standby Controls
Code 32	Standby Multiple Outputs Power Circuitry and Regulators
Code 33	Three Beam Supplies - 2 Required for Full Power
Code 34	Standby Controls and Multiple Output Power Circuitry
Code 35	Standby Controls and Three Beam Supplies

Code 36	Standby Multiple Outputs and Three Beam Supplies
Code 37	Standby Controls, Multiple Output and Three Beam Supplies
Code 38	Majority Voting Controls

The losses for each configuration have been estimated and converted to additional solar array and spacecraft weight for the input power and thermal heat transfer. The conversion factor is 0.03 kilograms per watt of power processor loss. The goal is to obtain the lowest overall weight with the highest reliability. Figure E-18 shows the total weight (unit weight plus source weight for losses) for the different redundant configuration. In analyzing the results of Figure E-18, configurations 34 and 38 can provide a reliability of 0.94 with a weight penalty of about 6 kilograms.

The alternate system configuration, using a single SCR series inverter for the power processor, was also analyzed. The redundancy configurations included were:

Code 10	No Redundancy
Code 11	Standby Control Circuit
Code 12	Majority Voting Control Circuits
Code 13	Standby Multiple Output Power & Control Circuit
Code 14	Standby Control and Multiple Output Power Circuits
Code 15	Majority Voting Control Circuits & Standby Multiple Output Power Circuits

Figure E-19 shows the unit weight for the different configurations. Figure E-20 shows the effect of the unit weight and source weight for the internal power losses. Configurations 12 and 14 show a system capable of 0.95 reliability with a weight penalty of 6 kilograms.

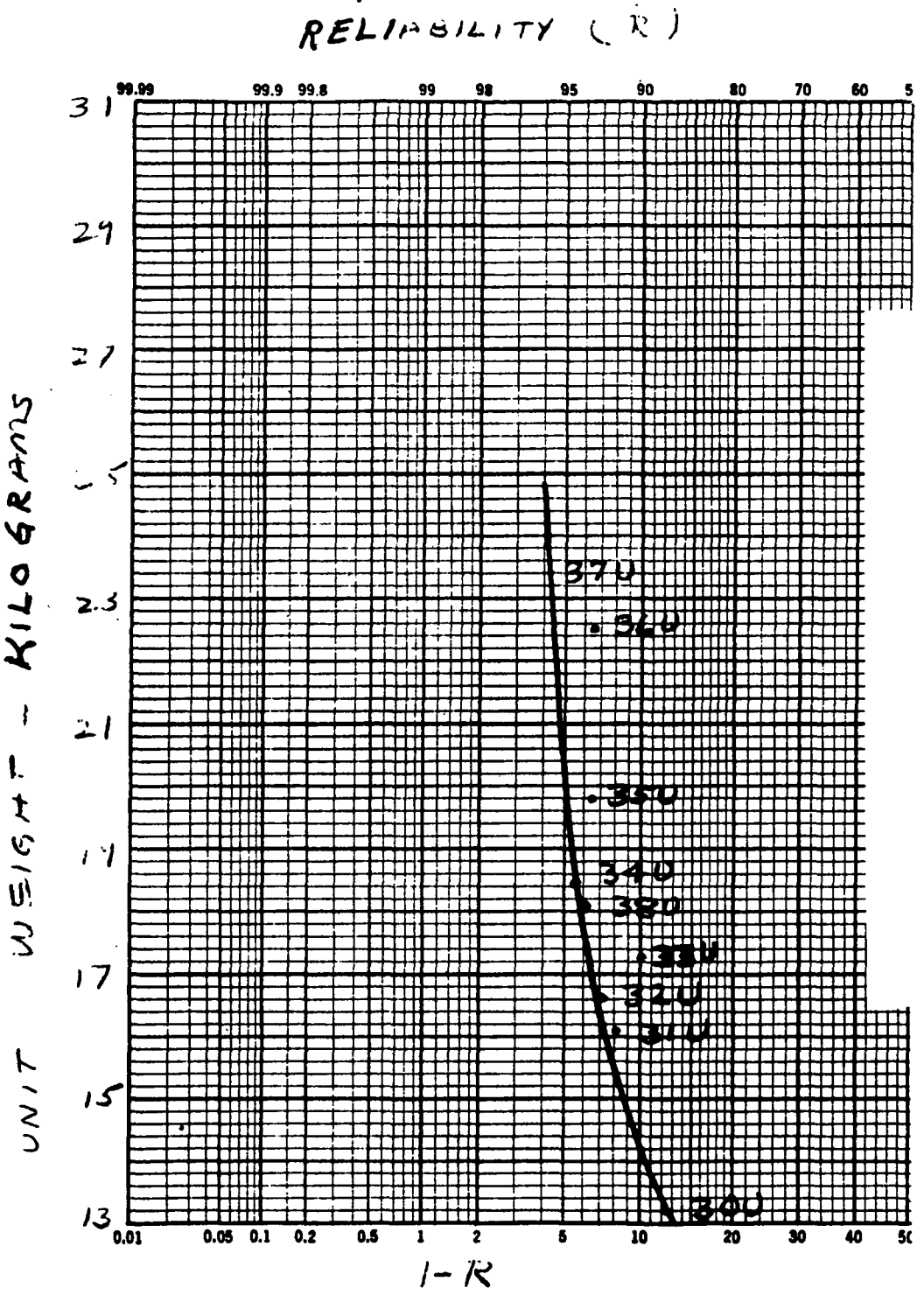


FIGURE E-17

BASELINE RELIABILITY CONFIGURATION VS. UNIT WEIGHT

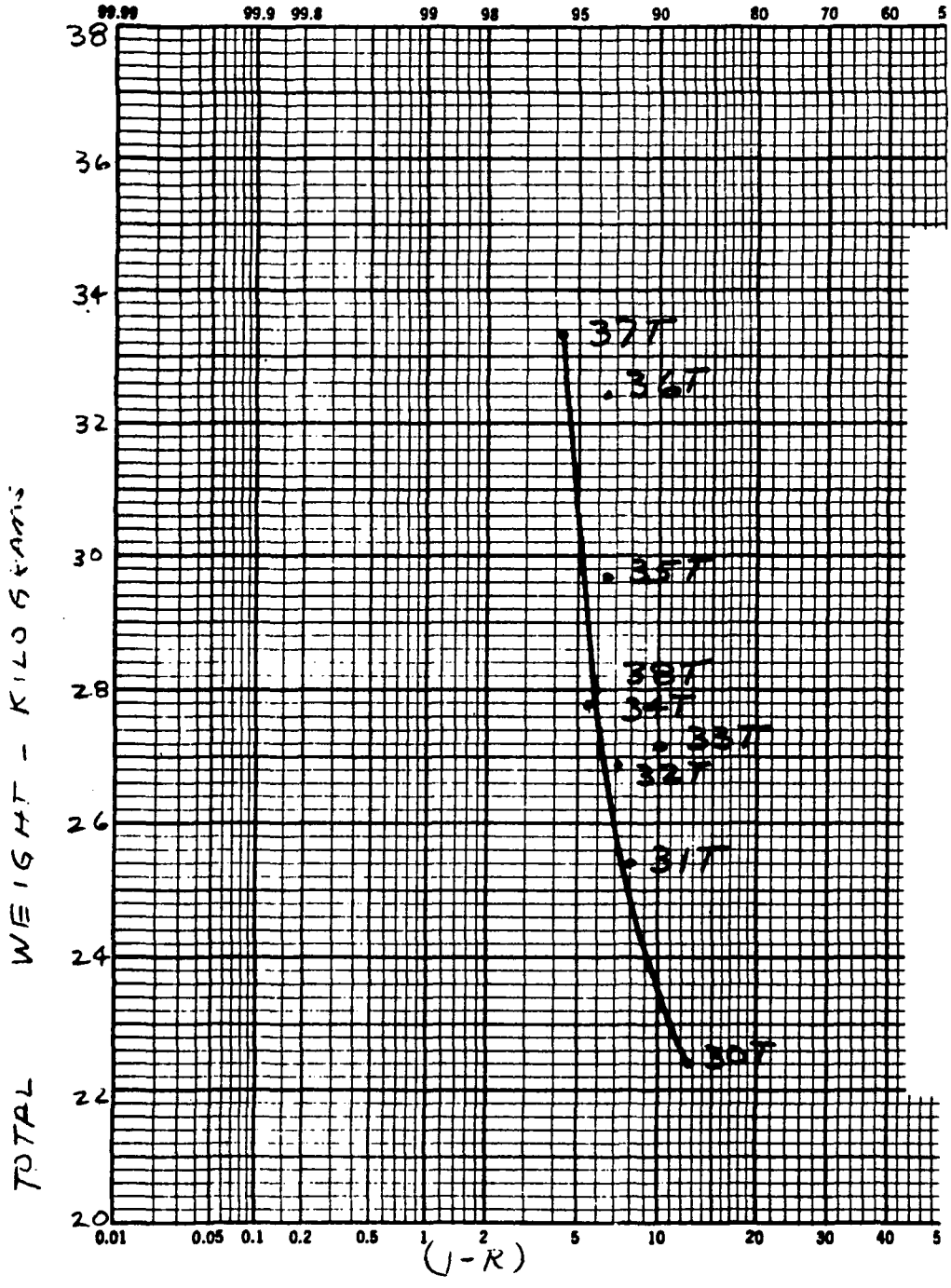


FIGURE E-18

BASELINE RELIABILITY CONFIGURATION VS. TOTAL WEIGHT
(UNIT & SOURCE WEIGHT FOR LOSSES)

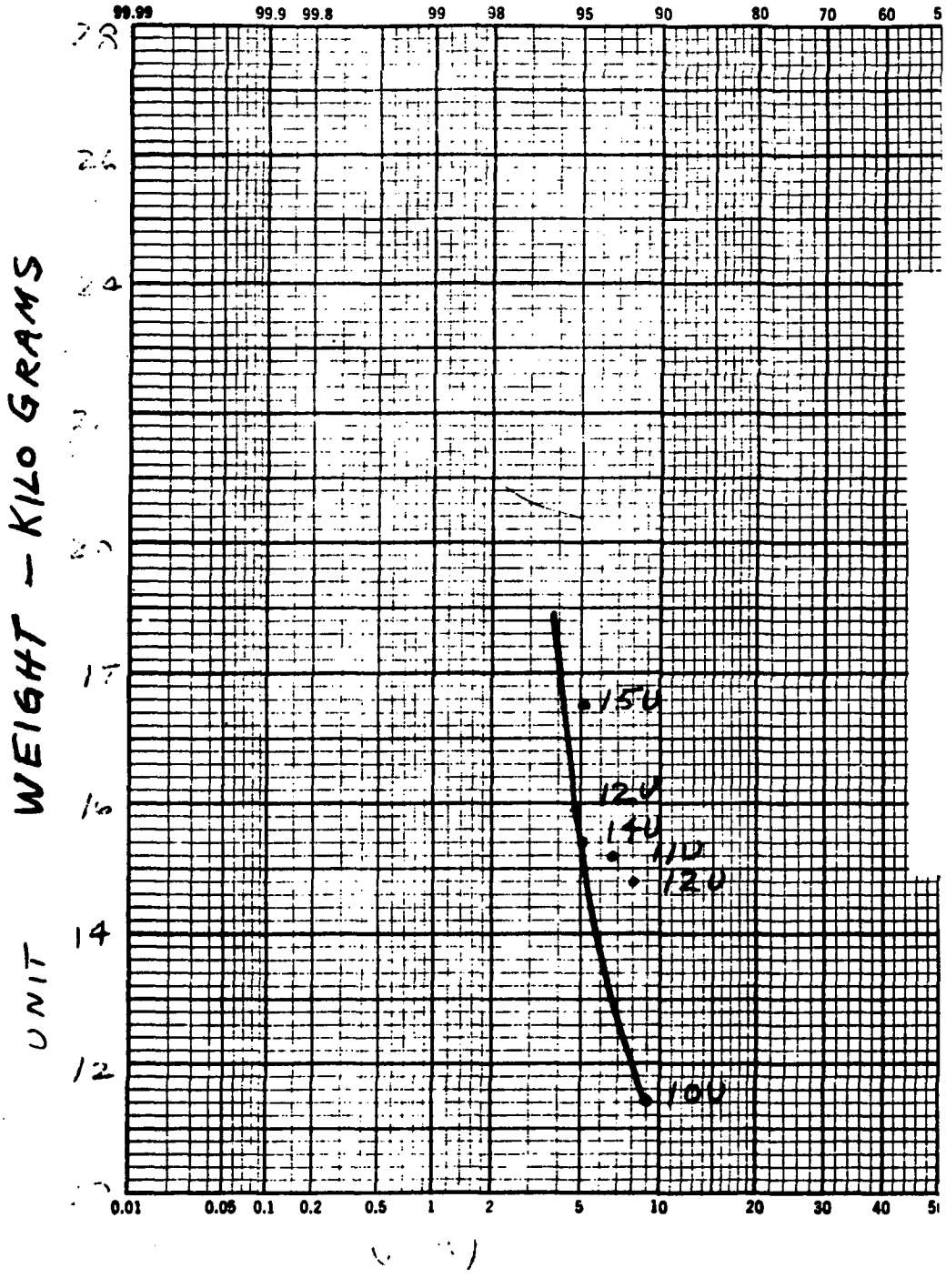


FIGURE E-19

ALTERNATE SYSTEM RELIABILITY CONFIGURATIONS
VS. UNIT WEIGHT

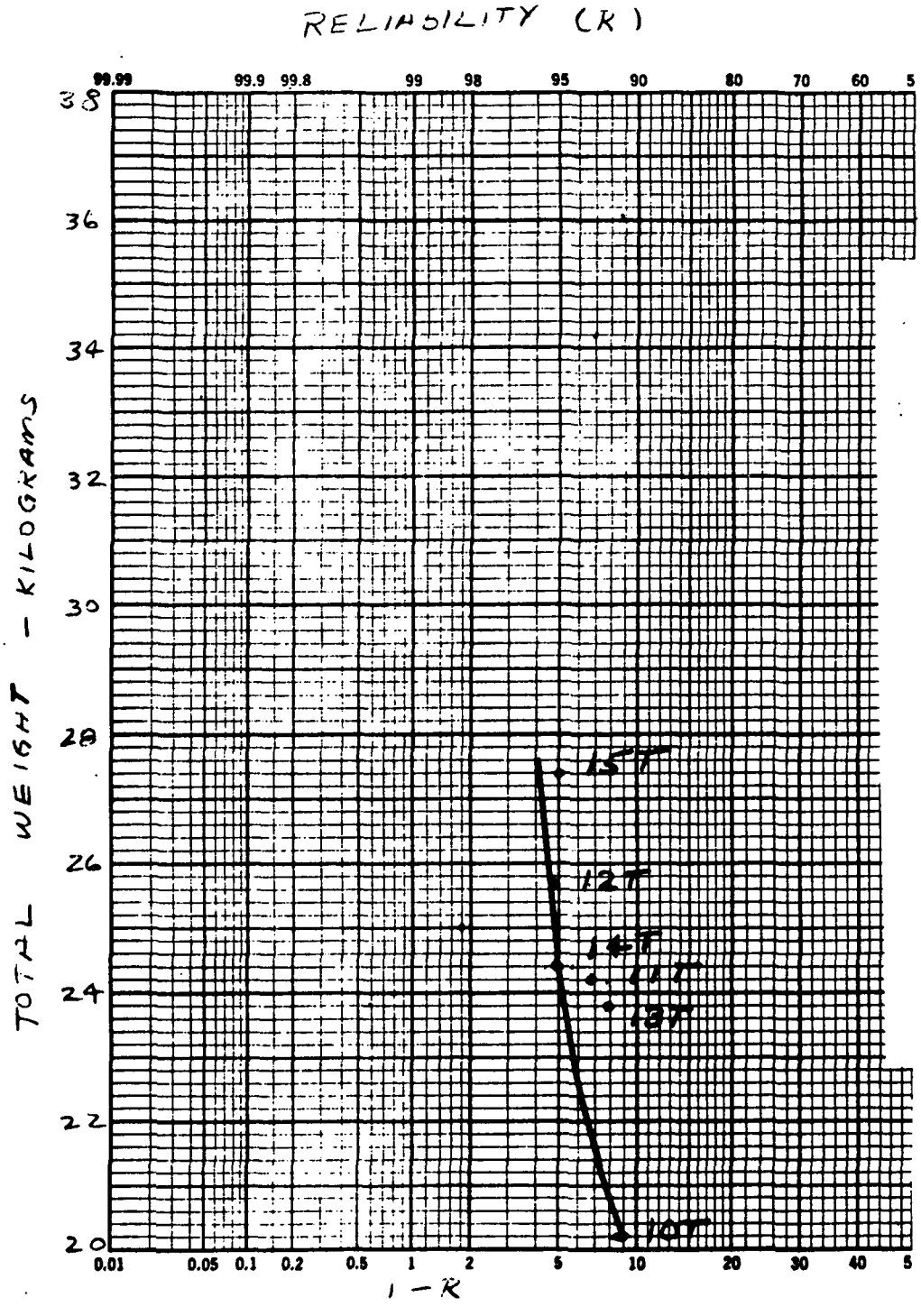


FIGURE E-20

ALTERNATE SYSTEM RELIABILITY CONFIGURATIONS VS. TOTAL WEIGHT
(UNIT WEIGHT & SOURCE WEIGHT FOR LOSSES)