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ASDTIC CONTROL AND STANDARDIZED INTERFACE CIRCUITS APPLIED TO BUCK, PARALLEL AND BUCK-BOOST DC TO DC POWER CONVERTERS

by A. D. Schoenfeld and Y. Yu

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Prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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16. Abstract

Versatile standardized pulse modulation nondissipatively regulated control and control signal processing circuits were applied to three most commonly used dc to dc power converter configurations: the series switching buck-regulator, the pulse modulated parallel inverter, and the buck-boost converter.

The unique control concept and the commonality of control functions for all switching regulators have resulted in improved static and dynamic performance and control circuit standardization.

New power-circuit technology was also applied to enhance reliability and to achieve optimum weight and efficiency.

Three demonstration models for each of the three types of dc to dc converters were built, tested, and delivered to NASA/LeRC.

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FOREWORD

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1. SUMMARY

The application of versatile pulse modulation control and control signal processing circuits to the three most commonly used nondissipatively regulated dc to dc converter power circuit configurations: the series switching buck regulator, the pulsewidth modulated parallel inverter, and the buck-boost converter, is discussed in detail.

The Analog Signal to Discrete Time Interval Converter (ASDTIC), conceived originally within NASA, was utilized as the Standardized Analog Control Signal Processor (ACSP) of the three dc to dc converter regulators. The application has resulted in uniformly superior static and dynamic performance for all three types of dc to dc converters.

Commonality of control signal functions for all switching regulators, made possible by the ASDTIC and the newly developed Digital Control Signal Processor (DCSP) circuits, has resulted in control-circuit standardization of the three dc to dc converters.

New power-circuit technology, including component stress control and recovery of power transistor switching loss, was applied to improve reliability and to optimize weight and efficiency.

Three demonstration models for each of the three types of dc to dc converters were built, tested, and delivered to NASA LeRC. The static and dynamic performance of the demonstration models, as well as the power component stress control philosophy implemented in their design, has greatly advanced the state-of-the-art in the design of dc to dc converters.

2. INTRODUCTION

A nondissipatively-regulated dc to dc converter generally achieves efficient voltage transformation and regulation through cyclic operation of its power switch in alternate conduction and nonconduction states. Consequently, the converter control system must be able to converter analog signals derived from the converter output and the control reference, through an A-to-D process, into discrete time intervals in controlling the on-off duty cycle of the power switch. The modulated pulse train derived from the cyclic operation of the power switch is then converted back, through a D-to-A process, to analog form at the converter output by a low-pass filter. Converter output regulation can be achieved through modulation of the power switch on-time (T_n) and/or off-time (T_f).

A pulse modulation for voltage or current regulation of dc to dc converters can be implemented through numerable control circuits proposed and in use today. Generally speaking, they can be categorized into two types of feedback control mechanization: (1) single-loop feedback control and (2) multiple loop feedback control.

The electrical performance of a dc to dc converter depends, to a large extent, on the quality of its control system. Unfortunately, most single-loop approaches suffer from many inherent limitations:

- Due to the presence of a second-order LC filter for output ripple reduction, the utilization of a high gain and wider band width amplifier necessary for good static regulation, high audio-susceptibility reduction, and fast dynamic response is usually accompanied by an increasing risk of dynamic instability induced by line or load changes and variations in component characteristics due to component tolerances, environmental effects, and aging.
- The long time constant associated with the low-pass filter delays the rate of power-switch-modulation adjustment responding to a dynamic line and/or load disturbance, thus compromising the converter dynamic response.
- Due to the many transport delays including the power transistor storage time, additional loop gain is needed to reduce the error, which again leads to an increasing risk of instability.

The stringent demands of space and military programs have served to promote considerable research effort toward the development of an electronic control system capable of mitigating these limitations. One such system was conceived and disclosed through a NASA Internal Research Program.[1,2] The system utilizes a multiple-loop control mechanization. The controlling element is basically an Analog-Signal-to-Discrete-Time-Interval-Converter (ASDTIC), which was subsequently reduced to a microminiaturized thin film hybrid module.[3,4] Since then, the ASDTIC module has been employed in different types of nondissipative regulator applications, with the static regulation and dynamic performances approaching those generally exhibited only by dissipative regulators.

The basic objectives of this program were to develop and demonstrate the application of ASDTIC to the three most commonly used dc to dc converter power circuit configurations and to develop the associated control signal processing circuits. The successful performance of this program did lead to the following achievements:

- Verify and demonstrate the application of the ASDTIC control system to three distinct and functionally different types of dc to dc converter power circuit configurations:

  Buck-Boost Converter
  Series Switching Buck-Regulator
  Pulse Modulated Parallel-Inverter

- Design and development of interface circuitry between the ASDTIC control element and the power circuits of the respective dc to dc converters. These control signal processing circuits should exhibit commonality among different converters to further standardization.

- Accomplishment of superior performance characteristics including superb static and dynamic output characteristics and input current inrush limiting (for the prevention of the collapse of current limited primary power sources).

- Construction, testing, and delivery of one breadboard and two brassboard demonstration models for each of the three types of dc to dc converters.

In accordance with the contract, the program proceeded sequentially through the following phases:

Task 1: Technical Plan
Task 2: Converter Development and Design
Task 3: Converter Fabrication and Test

A Technical Plan summarizing results of Task 1,[5] was used to guide the efforts of Task 2. A report,[6] prepared at the conclusion of Task 2 served as a construction plan for the three regulator converters. One breadboard and two brassboard demonstration models of each converter type were subsequently built and tested to establish their compliance with the technical specifications. The demonstration models were delivered to NASA/LeRC.

This report presents the pertinent information generated in the course of the three tasks performed over a period of one year starting in September 1971.

The presentation starts with a general switching-regulator converter control block diagram presented in Section 3, from which ASDTIC concept is evolved. Using ASDTIC as the standardized Analog Control Signal Processor, a qualitative discussion of ASDTIC then follows in Section 4, which highlights its salient features. To complete the control-circuit standardization, a Digital Control Signal Processor (DCSP) is described in Section 5. The design guidelines for the power and control circuits of the three aforementioned dc to dc converters are presented in Section 6. The three converter block diagrams, featuring the commonality of functional blocks, are given in Section 7, followed by circuit descriptions in Section 8. The construction of the demonstration models of the three types of dc to dc converters is discussed in Section 9. The static and transient performance data are included in Sections 10 and 11, respectively. Recommendation for future tasks is presented in Section 12, and the report ends with conclusions in Section 13.

To anyone working with nondissipatively regulated dc to dc converters, certain design intricacies inevitably make themselves felt throughout the converter design and development stage. While by no means intended as a

final solution to an optimum converter design, the work described herein nevertheless represents a step forward in an effort to bring into sharp focus the converter system design philosophy as well as its functional standardization. Specifically, the effort resulted in the following key achievements:

(1) The control system implementation through standardized control and interface circuits including both standardized analog and digital-control signal processors. These circuits can be applied to all types of switching regulators using either transistors or SCR's as power switches.

(2) The successful application of the standardized control system to the three most commonly used dc to dc converters: (A) the energy-storage buck-boost converter, (B) the series-switching buck regulator, and (C) the pulse-modulated parallel-inverter converter. The static regulation and dynamic performance of each converter were demonstrated to approach the high levels generally exhibited only by dissipative regulators.

(3) Active power-component stress control under all conceivable transient operations was facilitated by a peak-current sensor and the standardized digital control signal processor, thus enhancing the reliable operation of each converter.

(4) Optimum weight-efficiency was made possible by: (A) energy-recovery networks to minimize the switching losses in the power switch, (B) an active magnetics-saturation sensor to eliminate saturation current in the parallel-inverter transformer, (C) a set of well-conceived power magnetics design equations, and (D) a proportional power switch base current drive.

3. SWITCHING REGULATOR CONTROL PHILOSOPHY

As stated in Section 2, the analog signal at the output of a switching-regulator, after comparison with a reference, must be transformed into a digital signal to control the on-off duty cycle of the power switch. The controlled digital pulse train at the power switch output is averaged by an energy storage element, and the analog control signal is derived from the regulated dc output of the dc to dc converter.

The objective of this section is twofold. One is to present a general switching-regulator control system block diagram, from which the various conventional single-loop control methods are categorized, and their relative drawbacks reviewed. The second is to provide a brief history of two-loop control, from which the specific control system used in this program is evolved.

3.1 General Switching-Regulator Control System Block Diagram

Generally speaking, the A-to-D-to-A process is accomplished, as shown in the block diagram of Figure 1, where a series switching converter is used for illustration purpose.

Starting with a signal at the converter output, i.e., point A of Figure 1 and tracing clockwise, the signal is processed by an Analog Control Signal Processor (ACSP) composed of a reference, an error amplifier, and a ramp function generator. After comparing the sensed signal to the reference, the error is amplified by a properly-compensated amplifier, which results in a signal at point B. The amplified output is then either: (1) combined with, or (2) transformed into, a ramp function. The ramp can be a flux ramp via a magnetic device, or it can be a voltage ramp obtained, for example, by charging a capacitor. When the instantaneous ramp voltage reaches a threshold level, it causes the threshold detector output, point C of Figure 1, to change state. This change of state, in turn, actuates a Digital Control Signal Processor (DCSP) to control the turn-on or the turn-off of the power switch Q. Voltage pulses with an amplitude

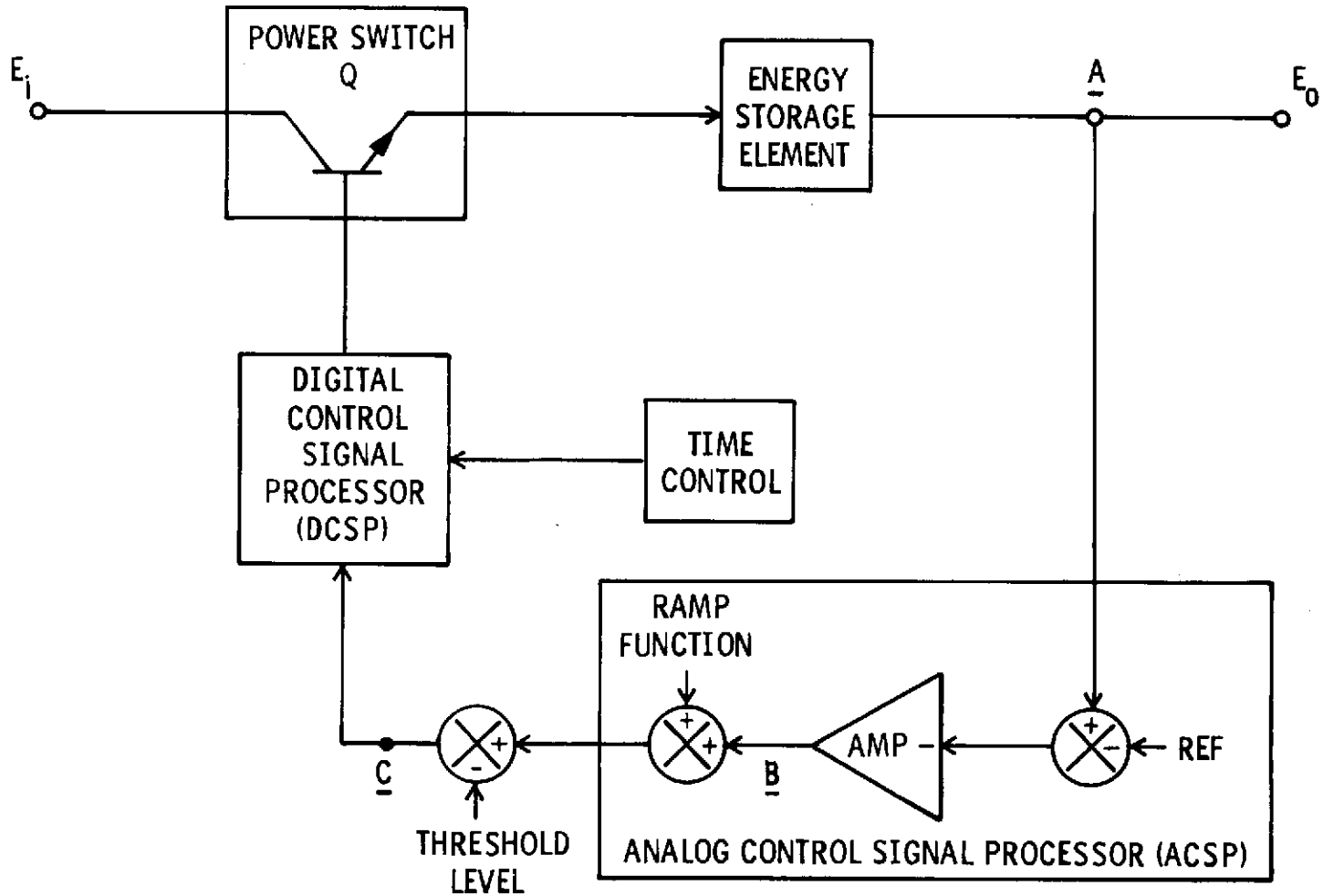

Figure 1. A Generalized Converter Control Circuit Block Diagram

corresponding to the input voltages E_i are averaged by the energy storage element, thus closing the loop at its starting point, i.e., point A. This general control concept can be implemented through numerous circuits. The variations are primarily due to the different means through which the ramp function and the threshold level are mechanized.

Notice the necessity of a ramp function intersecting a threshold level, for without it the transformation from the analog error at point B to a digital pulse train at point C and at the power switch output is impossible to initiate. Notice, also, the significance of the DCSP. Depending on how it is mechanized, the duty-cycle of the power switch can be controlled by the following combinations of on-time T_n and off-time T_f: (1) constant T_n, variable T_f, (2) constant T_f, variable T_n, (3) constant $(T_n + T_f)$, variable T_n and T_f, and (4) variable $(T_n + T_f)$, variable T_n and T_f.

3.2 Category of Single-Loop Control Methods and Their Inherent Limitations

Generally speaking, the intersection of the ramp and the threshold level in classical, single feedback loop control is achieved through either one of the three following implementations:

(1) The ramp (or, the threshold level) at the ACSP output, generated from the amplified error, intersects a fixed threshold level (or, a fixed ramp) to actuate the DCSP. [7, 8, 9, 10, 11, 12]

(2) The ramp or the threshold level is generated as an exclusive function of converter input voltage E_i. When the ramp is line dependent, the threshold level is fixed. Likewise, a line dependent threshold level is complemented by a fixed ramp. The composite analog error and the ramp are compared to the threshold level to actuate the DCSP. [13, 14]

(3) The ramp is simply the ac ripple of the converter output voltage, E_o. The error amplifier is essentially unity gain and there are two threshold levels corresponding to the peak and valley of the output ripple. The two threshold levels are combined with the DCSP to form a bistable hysteretic trigger. [15, 16, 17, 18]

Converters of category (1) derive the ramp or the threshold level from the output error exclusively. This method suffers from the following inherent limitations:

- Due to the presence of a second-order LC energy storage element for output ripple reduction, the utilization of a higher gain and wider bandwidth ACSP amplifier necessary for good static regulation, high audio-susceptibility reduction, and fast dynamic response is usually accompanied by an increasing risk of dynamic instability. The instability can be induced by line or load changes and variations in component characteristics due to component rating tolerances, environmental effects, and aging.
- The long time constant associated with the low-pass output filter delays the rate of power-switch-modulation adjustment responding to a dynamic line and/or load disturbance, thus compromising the converter dynamic response.
- Due to the many transport delays including the power transistor storage time for all converters and power transistor on time T_n for certain types of converters, converter instability becomes imminent when a high gain, large bandwidth control is attempted.

Consequently, the performance for converters of category (1) are inevitably compromised by the stability criterion. These inherent limitations are partially alleviated in converters of category (2). The static and dynamic regulation against line change is improved, in an open-loop fashion, by the line dependent ramp or threshold-level generation. However, static line regulation and converter stability are still degraded by transport delays, and the dynamic performance against load changes is again hampered by the output energy storage element.

Converters of category (3) represent a classical application involving a second-order system with hysteresis. Generally, their dynamic performances are superior to those of categories (1) and (2). The output ripple itself is used as the ramp between two hysteretic levels, within which the dynamics against line and load distrubances are bounded. The simplicity and unconditional stability of the nonlinear control has lent itself to extensive

modeling and analysis [15,17,19,20]. Its known functional subtleties include: (A) the heavy dependence of converter performance on the amount of equivalent series resistance (ESR) in the output filter capacitor, (B) the dc output voltage is a function of the transistor storage time and the output ripple waveform; its average value within the boundary of two hysteretic levels is not precisely controlled, (3) although its operating frequency range can be made small [21], it is still unable to engage in a constant frequency operation, which may be mandatory for applications involving frequency synchronization, and (4) thus far, the control has been applied only to the buck type switching regulators and their equivalent [21].

Up to this juncture, the common denominator of the three control categories discussed above is the utilization of a single feedback loop.

3.3 History of Two-Loop Control

Confronted with such inherent limitations of the single feedback-loop switching regulator, multi feedback-loop regulation-control concepts were advanced. As early as 1964, patents [22,23] were filed in which a second feedback signal was applied to effectively reduce the hysteresis width of the bistable trigger, thus allowing a higher frequency of operation than otherwise feasible. A converter where both dc and ac information were included in its feedback loop by sensing the voltage in front of the filter inductor was reported [24], which resulted in stable operation of the converter over a relatively large change in output-filter capacitance.

Another two-loop regulation control concept was developed in which the ramp is generated by reproducing the current in the output filter inductor [25]. The ramp is then summed with the output of the error amplifier and is used in a closed loop fashion to control the on-off of the power switch through a bistable hysteretic trigger. Basically, this system closely resembles converters of category (3) in principle. The ramp generated from the inductor current is identical in waveform to the ripple across the output filter capacitor having a sufficient ESR. The converter, therefore, possesses the performance advantages of control category (3). However, by using the inductor current to replace the capacitor voltage as the ramp function, the converter operation no longer depends heavily on the capacitor ESR. Furthermore, the use of the additional feedback permits

the design of a high-gain dc loop for precision output voltage regulation. The technique also provides inherent current limiting. However, due to its two-state modulation, it is limited to performing duty cycle control at a constant off time, T_f.

Still another regulation control concept employing an additional feedback loop was conceived within a NASA Internal Research Program [1, 2]. Here the ramp function is generated by integrating the rectangular ac voltage at the power switch output. A modified version of this concept derives the ramp function by integrating the ac voltage across the filter inductor. The additional ac loop is responsible for improvements in static and dynamic converter performances. In conjunction with a fixed threshold level and the DCSP, the triangular integrator output is used as the ramp function to accomplish power switch duty-cycle control. This concept uses an Analog to Discrete Time Interval Converter (ASDTIC) for the ACSP and threshold detector functional blocks of Figure 1 [3, 4, 26]. The control is flexible, as it can be accomplished through either a constant T_n, a constant T_f, a constant $(T_n + T_f)$, a line dependent T_n, or a two-state modulation.

4. STANDARDIZED ANALOG CONTROL SIGNAL PROCESSOR (ACSP)

As described in Section 3, the modified ASDTIC derives the necessary ramp function by integrating the voltage across the filter inductor. In this section, the original implementation of the control concept is first described, which then leads to the modified version used in the present program. The inherent merits of ASDTIC are discussed with regard to its dynamic capability and stability, thus laying the foundation for a qualitative understanding of the high performance exhibited by the ASDTIC-controlled dc to dc converter-regulator.

4.1 Original ASDTIC Implementation.

The ASDTIC control concept, originally conceived within NASA,[2] can be represented in Figure 2, where a series-switching converter is utilized for illustration. The filter inductor L_o is shown to have a dc resistance. R_{dc}. Voltages e_i and e_o at either end of the inductor are divided down by a factor K_d, and compared with reference E_R. Thus, the integrator input voltage contains error signals e_{dc} and e_{ac}, where $e_{dc} = K_d e_o - E_R$, and $e_{ac} = K_d e_i - E_R$. The integrator is, in reality, a high gain dc amplifier with capacitor feedback. Consequently, e_{dc} is extremely small and $/e_{ac}/ >> e_{dc}$ holds, leaving the integrator input voltage, x, as that shown in Figure 2. The triangular integrator ac output, serving as the ramp function, is superimposed on the amplified dc error to intersect a threshold level, E_T. The intersection actuates the DCSP to perform the proper control of the power switch.

This implementation was tested and found to yield excellent regulation against input-voltage variation. However, its performance against load change was hampered by resistance R_{dc} in the inductor winding. Qualitatively, the detrimental effect of R_{dc} to load regulation is understandable. Voltages e_i and e_o differ by a voltage drop across R_{dc}, yet both voltages are compared with the same reference E_R to establish the dc error. The inner loop sensing e_i is, therefore, interferring with the proper function of the outer loop sensing e_o, which prevents a precision regulation for e_o. In the worst-case limit, when only the inner loop exists, the load regulation against a load-current change ΔI_o is $R_{dc}\Delta I_o$.

4.2 ASDTIC Concept Used to Implement a Standardized ACSP.

The modified ASDTIC concept was used in this program for the regulation control of three different types of dc to dc converters. The commonality facilitated the use and demonstrated the practicality of the standardized Analog Control Signal Processor (ACSP).

The modified ASDTIC concept is represented in Figure 3. The error-processing component of the standardized ACSP is a high-gain error amplifier with a capacitor feedback, i.e., an integrator. Two input signals are applied to the integrator-amplifier through two feedback control loops. The first loop senses the dc output voltage e_o of the converter, divides it by a factor $K_d \leqq 1$, and compares $K_d e_o$ to the amplifier reference E_R. The difference $e_{dc} = K_d e_o - E_R$ becomes the dc error input. In conjunction with a threshold-detector level E_T, the dc output level of the integrator-amplifier is determined by e_{dc}. The second loop senses the ac component of $(e_i - e_o)$ across the filter inductor L_o, transforms it by a factor $n \gtreqless 1$, and feeds $e_{ac} = n\ (e_i - e_o)$ differentially to the integrator-amplifier. The rectangular ac voltage e_{ac}, along with the much smaller dc error e_{dc}, are integrated. The integrator triangular output, serving as the ramp function, is superimposed on the amplified dc error to intersect the threshold-level E_T. The threshold detector actuates the Digital Control Signal Processor (DCSP) to control the duty cycle of power switch Q.

Notice that, unlike Figure 2 in which the inner loop sensing e_i handles both dc and ac information, the second loop of Figure 3 processes only the ac information for the purpose of ramp generation. It, therefore, no longer interferes with the dc regulating function of the first loop sensing e_o. Experimentally, the modified ASDTIC of Figure 3 exhibited an order of magnitude improvement over that of Figure 2 insofar as the load regulation was concerned. As for the regulation against line change, the two systems offer essentially identical performances. Consequently, the system of Figure 3 was utilized in the present program. An additional feature not to be overlooked in the system concept of Figure 3 is its universal adaptability to all switching regulators. For as long as there exists within the regulator an inherent ac waveform suitable for ramp-function generation, the standardized ACSP can be conveniently applied to sense a dc voltage signal at any point in the converter.

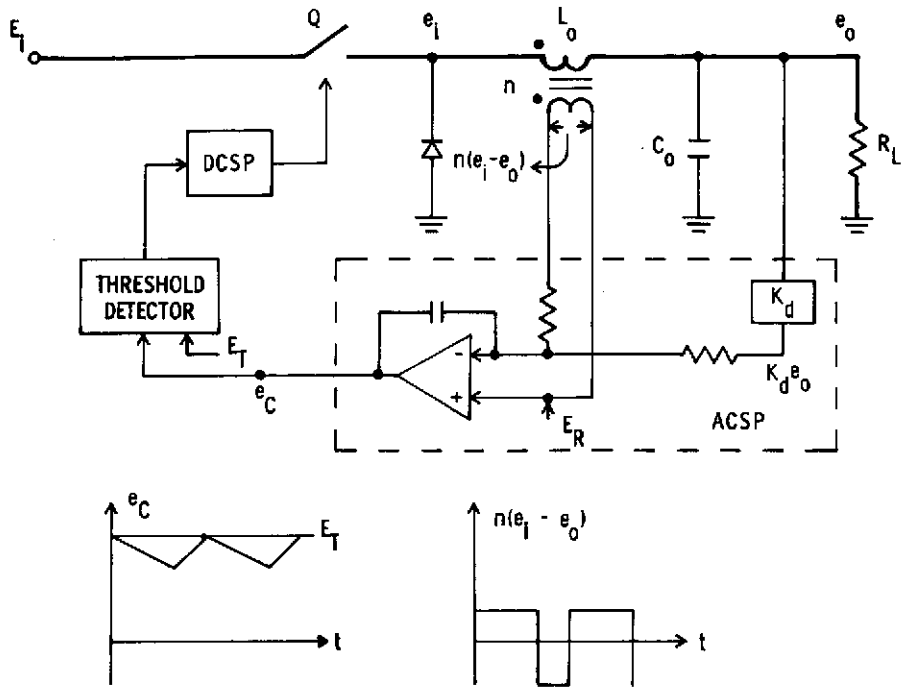

Figure 2. Original ASDTIC Implementation

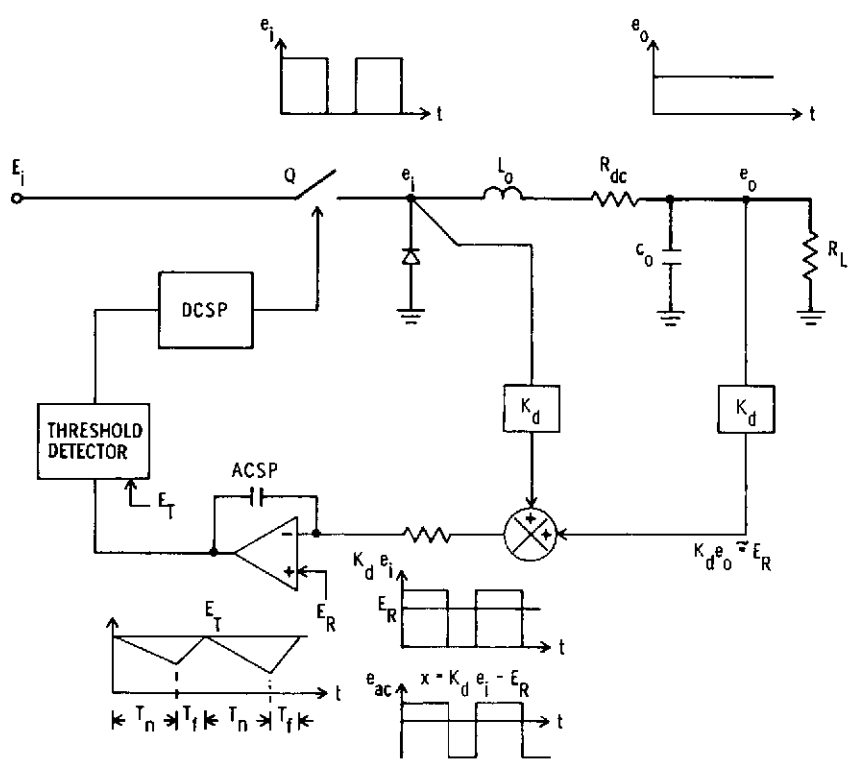

Figure 3. Modified ASDTIC Implementation

4.3 Inherent Merits of the Standardized ACSP

As stated previously, the long time constant of the output energy-storage elements and the various transport lags often make it impossible to achieve simultaneously fast transient response, stability, and precision regulation for a dc to dc converter employing a single-loop control.

In this regard, the two-loop standardized ACSP using the ASDTIC regulation control concept offers the following merits:

(1) Owing to the additional ac loop, the rate of change of the regulator duty cycle in responding to line disturbances is not limited by the relatively slow dc loop.

The fast reaction can be verified by considering Figure 4(A), in which the converter output voltage is regulated at $e_o = E_o$, and sudden changes in input voltage are indicated to occur at t_1, t_2, and t_3. For clarification, the following conditions are assumed: (A) The DCSP is programmed for a constant "T_n" operation. Each time an increasing ramp intersects the threshold level, it initiates the conduction of the power switch for a fixed time interval T_n, and the output voltage is regulated by controlling T_f. (B) The time constant of the output filter is much longer than a switching period $(T_n + T_f)$, thus maintaining an essentially constant E_o within a switching period independent of any step change in e_i. (C) All components are ideal and lossless. Under these assumptions, the integrator and inductor voltages for Figure 4(A) are shown in Figure 4(B) and Figure 4(C), where T_n is constant as assumed. During T_n, the voltage across the inductor is $e_i - e_o$, where e_i is the step waveform of Figure 4(A) and $e_o = E_o$ is the regulated output voltage. The slope of the integrator ramp during T_n is thus proportional to $e_i - e_o$, while during T_f the slope is constant determined by E_o.

Between $t = 0$ and $t = t_1$, when $e_i = 2E_o$, the steady-state operation results in equal T_n and T_f, giving a duty cycle $T_n/(T_n + T_f) = 0.5$. When e_i is suddenly increased from $2E_o$ to $4E_o$ at t_1, which for clarity was made to coincide with the start of a new T_n, the steeper ramp slope proporational to $3E_o$ during T_n now causes the ramp amplitude to be three times larger at the

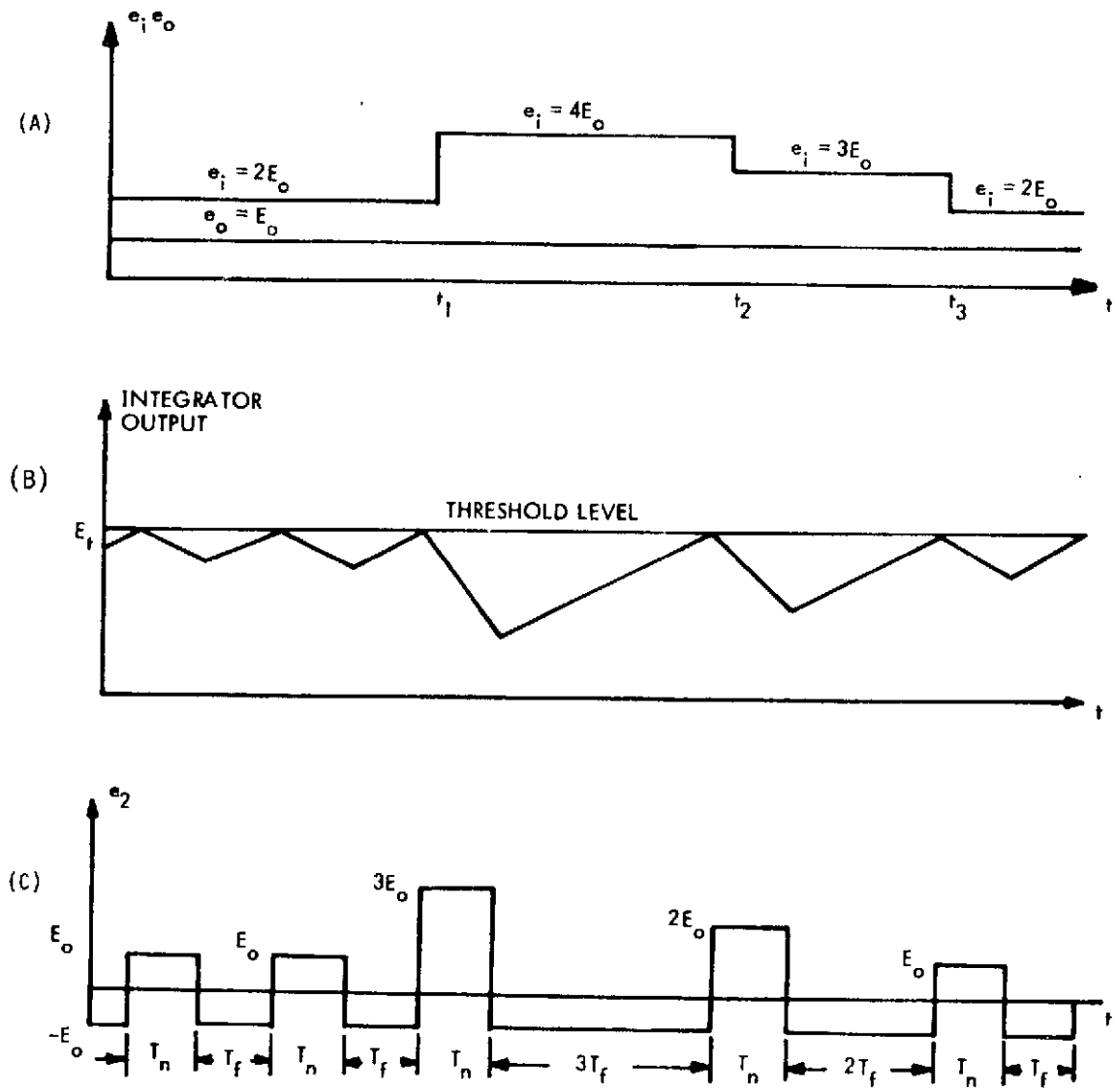

Figure 4. Adaptive Duty-Cycle Control Waveform

end of T_n. It therefore takes a time interval of $3T_f$ before the positive ramp can intersect the threshold again to start the next T_n, giving a new duty cycle of 0.25. Since the required steady-state duty cycle is e_o/e_i for this converter, the duty cycle becomes 0.5 and 0.25 when $e_i = 2e_o$ and $e_i = 4e_o$, respectively.

The correct duty cycle is adaptively achieved on an instantaneous basis without being delayed by the time constant of the output filter. Similarly, the auto-compensation effect for step input changes at t_2 and t_3 can be easily verified.

(2) <u>The regulator stability is immune to control component parameter Changes.</u>

The small-signal open-loop frequency response of this standardized ACSP is given in Appendix A. The analytical results show that the converter stability is not effected by changes in the output-filter configuration, the output loading, the error amplifier gain, the threshold level, the integrator time constant, and all other critical control parameters. The immunity reduces significantly the effort normally required in performing the worst-cast stability analysis. Such an analysis would be time consuming, as all parameter changes due to initial tolerances, temperature variation, and aging must be considered collectively. The immunity also provides a highly desirable feature for specific applications such as nuclear-hardening electronics, in which critical component parameters are known to undergo drastic changes.

(3) <u>High gain, wide bandwidth, and precision regulation against line and load changes.</u>

Analysis has also shown that the two-loop standardized ACSP can achieve high gain and stable operation concurrently. The open-loop dc gain is essentially that of the ACSP operational error amplifier, which is in the order of 100 db. The ac loop can be designed to eliminate the roll-off effect of the output filter, thus significantly increasing the bandwidth of the converter operating at a given switching frequency. These combined features are responsible for the good line and load regulation exhibited by the converters controlled by the standardized ACSP.

(4) Elimination of the detrimental effects of transport lags and other functional subtleties.

Since the auto-compensation between T_n and T_f is achieved by sensing the inductor voltage, in which the power-switch storage time is treated as part of on-time, T_n, the effect of the storage time on the output regulation and line rejection is minimized.

More important, the functional subtlety of certain converter types such as the buck-boost converter and the boost converter has made them most vulnerable to limitations of the single-loop control. The outputs of each of these converters are decoupled from the control-signal path during power-transistor on time T_n. The consequences are: (1) As far as its feedback control loop sensing the output error is concerned, the entire on-time interval T_n is equivalent to a transport lag, and (2) A low-frequency characterization of these converters has revealed a novel "positive-zero" term [27] in the frequency response of these converters. The two factors significantly limit the bandwidth of these converters when controlled by a single-loop sensing only the output error.

(5) Capability of controlling all switching regulators operated in different duty-cycle control modes.

The standardized ACSP is applicable to all switching regulators capable of providing an ac waveform for ramp generation. The ramp at the output of the standardized ACSP can be used in conjunction with a single threshold level or a bistable hysteresis level so that the DCSP can be configured to achieve duty-cycle control using either a constant T_n, a constant T_f, a variable T_n and T_f with $(T_n + T_f)$ constant, or a variable T_n and T_f with $(T_n + T_f)$ also variable.

The aforementioned advantages have been verified by the performance of the three different types of dc to dc converter demonstration models using the standardized ACSP.

The application of the standardized ACSP was complemented by a standardized Digital Control Signal Processor (DCSP), which is discussed in the next section.

5. STANDARDIZED DIGITAL CONTROL SIGNAL PROCESSOR (DCSP)

Presented in this section is a novel DCSP which, in conjunction with the standardized ACSP described in Section 4, could form a universal control circuit for all dc to dc converters.

The implementation of the standardized DCSP is shown in Figure 5. It is composed of two pulse stretchers, three NAND gates, and two R-S flip-flops. Each pulse stretcher gives an output pulsewidth equal to the sum of the input pulsewidth and a stretched time interval determined by external RC time constants. The digital outputs from flip-flop #2 are fed back directly as inputs to the respective pulse stretcher. The output at point Q is used to control the on-off times of the power switch through a driver whose output is proportional to the current in the power switch.

The DCSP receives the following signals:

(1) Converter Input Voltage Applied to R92. The converter voltage, E_i, along with R92, C92, and the internal-threshold level of pulse stretcher (2), determines the on-time interval T_n for the power switch.

(2) Regulated Voltage Applied to R91. This voltage, along with R91, C91, and the threshold level inside pulse stretcher (1), determines the minimum off-time T_m during transient operations.

(3) ACSP and Current Regulator Signals. By applying these regulator signals from the respective threshold detectors to NAND (1), digital signals in series with NAND (2) are not affected. Consequently, on time T_n, is not altered by the regulator function. The regulating signals applied to NAND (1) therefore serve only to inhibit the turn-on of the power switch by extending the off-time interval beyond the programmed minimum off time, T_m, to achieve the required duty-cycle control.

(4) ON-OFF Command Applied to NAND (3). A logical-0 applied to NAND (3) causes its output to be logical-1; this condition corresponds to the off condition for the power switch. A logical-1 applied to NAND (3) allows the DCSP to start the converter at a free-running frequency $1/(T_n + T_m)$ until the output regulation level is reached.

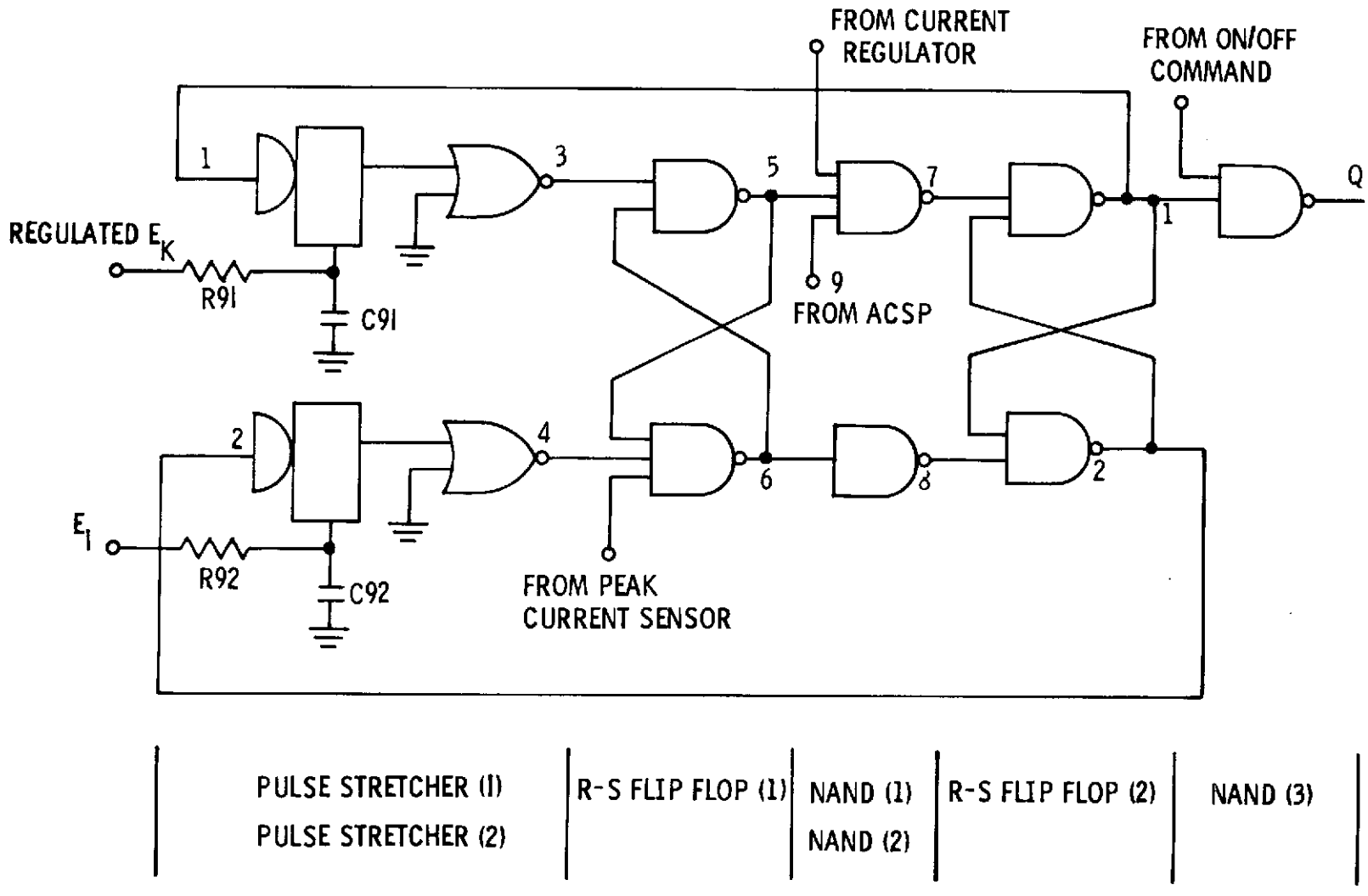

Figure 5. Standardized Digital Control Signal Processor (DCSP)

(5) Peak-Current Sensor Signal Applied to NAND (2). To limit the peak transient current in the power transistor switch requires that it be turned off before the normal T_n is timed out. The early termination of T_n is accomplished by a logical-0 input to R-S flip-flop #1 before the pulse-stretcher (2) output changes state. The signal is obtained from the peak-current sensor.

The new standardized DCSP was developed with a total of only seven parts including three IC's, two capacitors, and two resistors. Furthermore, it is readily adaptable to different methods of duty-cycle control. The DCSP shown here, with converter input voltage E_i applied to R92, is configured for a converter duty-cycle control based on a constant E_iT_n, i.e., a line-dependent variable on time T_n and a variable off time T_f. However, if an externally-generated constant voltage independent of varying E_i were applied to R92, the DCSP would then produce a constant T_n and a variable T_f. If the feedback signals to the pulse stretchers were not from the outputs of the R-S flip-flop (2), but were from the flip-flop (1), then both T_n and T_f would vary, yet the sum of T_n and T_f would be kept constant, resulting in constant-frequency operation. An external clock (with a frequency higher than the free-running frequency of the DCSP) applied to flip-flop (1) would result in synchronization of the converter switching frequency with the clock frequency. From these descriptions, the following advantages offered by this standardized DCSP become evident: (1) circuit simplicity, (2) performance of multiple functions and ease of interfacing including control, command, protection and orderly converter startup, (3) flexibility of adapting to various switching regulators, and (4) versatility of the circuit to perform duty-cycle control at either constant T_n, constant T_f, constant $T_n + T_f$, or a line-dependent T_n.

6. ASDTIC-CONTROLLED POWER CONVERTER DESIGN GUIDELINES

The objectives of this program were to demonstrate the application of the standardized Analog Control Signal Processor (ACSP) to three most used dc to dc converter configurations, and to develop a Digital Control Signal Processor (DCSP) which, in conjunction with the ACSP, would be used as a universal control circuit for the regulation and control of any dc to dc converter.

In the process of the design and development of the demonstration models for the three types of dc to dc converters, new power circuit technology was applied to improve reliability and to optimize weight and efficiency.

To achieve these objectives, certain guidelines were established. The design guidelines used in this program and their rationale are discussed below.

6.1 Power Circuit Design Guidelines

(1) High Reliability through Component Stress Control. One of the most lagging aspects of power processing technology at present is that of reliability. By this is meant the failure to consistently achieve in operational equipment the reliability that one might anticipate from consideration of the reliability of the components themselves. The reliability of the power converters can be greatly enhanced by controlling the power component stresses during steady state and, more important, during dynamic operations such as step line and/or load changes, sudden output short circuit, and converter starting. The power switch is the single most vulnerable and important power component, whose operation also determines the stress level of essentially all other power components. For this reason, a peak current sensor, which turns off the switch as soon as the switch current exceeds a certain limit, and an energy-recovery network, which minimizes the stresses and the switching loss in the power switch, shall be implemented for each converter [28].

(2) Optimum Weight Efficiency Tradeoff. Aside from reliability, weight and efficiency are the two other major concerns in the designing of power converters. To achieve a balance between weight and efficiency, the following guidelines were adopted:

(A) Converters processing large line and load variations should be designed to pass a trapezoidal power-switch current at heavy load, and a triangular current at light load. In other words, the power inductor should be designed to exhibit a critical inductance at an intermediate load.

(B) The power magnetics contribute to a majority of the total converter weight as well as significant portions of the total converter loss. Their design must be guided by a set of carefully derived design equations. See Appendix B.

(C) To maintain high efficiency at light load, the utilization of a proportional base-collector current drive is necessary.

(D) The aforementioned energy-recovery networks should be used to prevent the overlap of high voltage and high current associated with the power switch during its switching intervals, thus improving the efficiency and eliminating the possibility of secondary breakdown.

(E) High current spikes resulting from saturation of power magnetics of the pulse modulated parallel-inverter should be eliminated through active means. See Appendix C.

(3) Source EMI Control without High Resonant Peaking. Due to the audio-frequency line disturbance (i.e., 2.8V rms), the resonant peaking of the input filter must be controlled to prevent (A) the regulation limits of the power processors from being exceeded due to low voltage resonant valleys, and (B) the filter and the converter components from being over-stressed due to peak resonance. The filter must be designed with a large damping factor, yet without a significant efficiency penalty. The two-stage input filter which represents such a design shall be used. The optimum filter design shall be enhanced by an essentially constant switching frequency independent of input line voltage at full-load operation. See Appendix D for detailed filter design.

(4) Fool-proof Design. The converter must be designed to protect itself against a polarity reversal of the input line and a shorted or open converter output.

6.2 Control Circuit Design Guidelines

(1) Commonality of Regulation Control-Signal Functions. Adoption of the standardized ACSP to all three converters shall lead to the commonality in performing the basic analog to digital control-signal functions.

(2) Commonality of Control Circuits. In addition to the ASDTIC control elements in the voltage and current regulators, commonality should be achieved for all the interface and peripheral circuits. The realization of this design goal shall be achieved by the design of a novel Digital Control Signal Processor (DCSP).adaptable to all converters. The DCSP shall accommodate all control signal requirements including (A) interface with the digital signals from ASDTIC control elements, (B) provisions for duty-cycle control with either a constant on time, a constant off time, a line-dependent variable on time, or a constant frequency, (C) processing of the peak current protection of the power switch, (D) response to on/off command and enforcing an orderly converter starting, and (E) synchronization to an external clock frequency, if needed.

(3) Application of Digital Control Logic. The very nature of pulse modulation control in switching regulators has paced the present trend of increasingly incorporating more digital functions in regulator and control circuits. Realizing that noise immunity is the key to reliable digital IC application in switching regulators, the High Threshold Logic (HTL) family of IC's shall be used in the design of the DCSP. It has a high input threshold, a large logic swing, and a relatively long propagation delay (100 nanoseconds). These characteristics make the HTL most attractive for use where electrical noise rejection is an important consideration, as well as for applications where interfacing with various discrete components is required.

In addition, the following two guidelines were imposed on the digital control circuits: (A) all low-level control signals shall be dc coupled, with no ac or capacitive coupling for digital pulses; thus minimizing noise-generated false triggering, and (B) controlled time intervals wherever possible whall be mechanized using passive parts instead of regenerative one-shots to minimize noise susceptibility.

(4) Meeting Ripple Requirement during Dynamic Operations. To accommodate critical instrumentation and equipment loads aboard the spacecraft, it is desirable to limit the converter output voltage excursion to within the ripple specification limits during dynamic input line voltage and load changes This design goal of containing the converter transient response within the limits of the ripple specification shall be achieved through the integrated design of the power and control circuits.

6.3 Brassboard Converter Package Design Guidelines

(1) Division of Power and Control Circuit Modules. The power and control circuits shall be separated to facilitate the demonstration of control circuit commonality among different converters. Furthermore, this separation shall isolate from the low-level control-circuit boards interference-prone power components and leads carrying high switching currents.

(2) Division of Control Circuit Board into Submodules. To further standardization and to enhance maintainability, interchangeability, and functional block identification, the control circuit shall be divided into submodules of control and protection functions.

(3) Separation of High Voltage (HV) and Low Voltage (LV) Circuits. The circuit design should enable a simple division between HV and LV circuits to aid in the packaging of components. Sufficient separation of HV and LV circuits must be established to ensure reliable converter operation. To ensure personnel safety, HV components and terminals shall be totally enclosed.

(4) Provision of Test Points for Control Signal Tracing. Since one of the program objectives is to introduce to design engineers the ASDTIC control system concept, selected points which permit observation of control signal flow shall be made available through a test connector. The test points shall be protected against external shorts.

7. CONVERTER SPECIFICATIONS AND BLOCK DIAGRAMS

The program provided for the demonstration of standardized control on three types of dc to dc converters. The three most commonly used dc to dc converter configurations, shown in Figure 6, were selected for demonstrating the applicability of the ASDTIC control and of the newly developed interface and peripheral circuits: (1) the buck-boost converter, (2) the series switching buck-regulator, and (3) the pulse modulated parallel-inverter.

The buck-boost converter is usually used for low part count, high efficiency applications. This circuit can achieve voltage transformation with one power switch, and by duty cycle control of the same power switch, output regulation control is also achieved. The buck-boost converter has added advantages in high output voltage applications, as the number of secondary turns in the step-up magnetics can be reduced through the use of power switch on to off time ratios greater than one.

The series switching buck-regulator is the highest efficiency, lowest part count, lightest dc to dc converter. It is used where there are no input to output isolation requirements and where the single output voltage is lower than the lowest input voltage. It is also used as a pre-regulator to square wave parallel inverters where efficiency is less critical or for converter applications having multiple output voltages with wide load variations.

The pulse modulated parallel inverter is used for high efficiency multiple output applications. Power inversion and regulation is accomplished in the same power stage as in the switching-buck regulator, however, there are two power switches required, operating alternatively to effect voltage transformation. On the other hand, the separate LC filters in each output provide a degree of load isolation.

7.1 Converter Specifications

The equipment specifications for the three dc to dc converters are summarized in Table 1. Test data showing compliance by the deliverable converter units with these requirements are provided in Section 10.

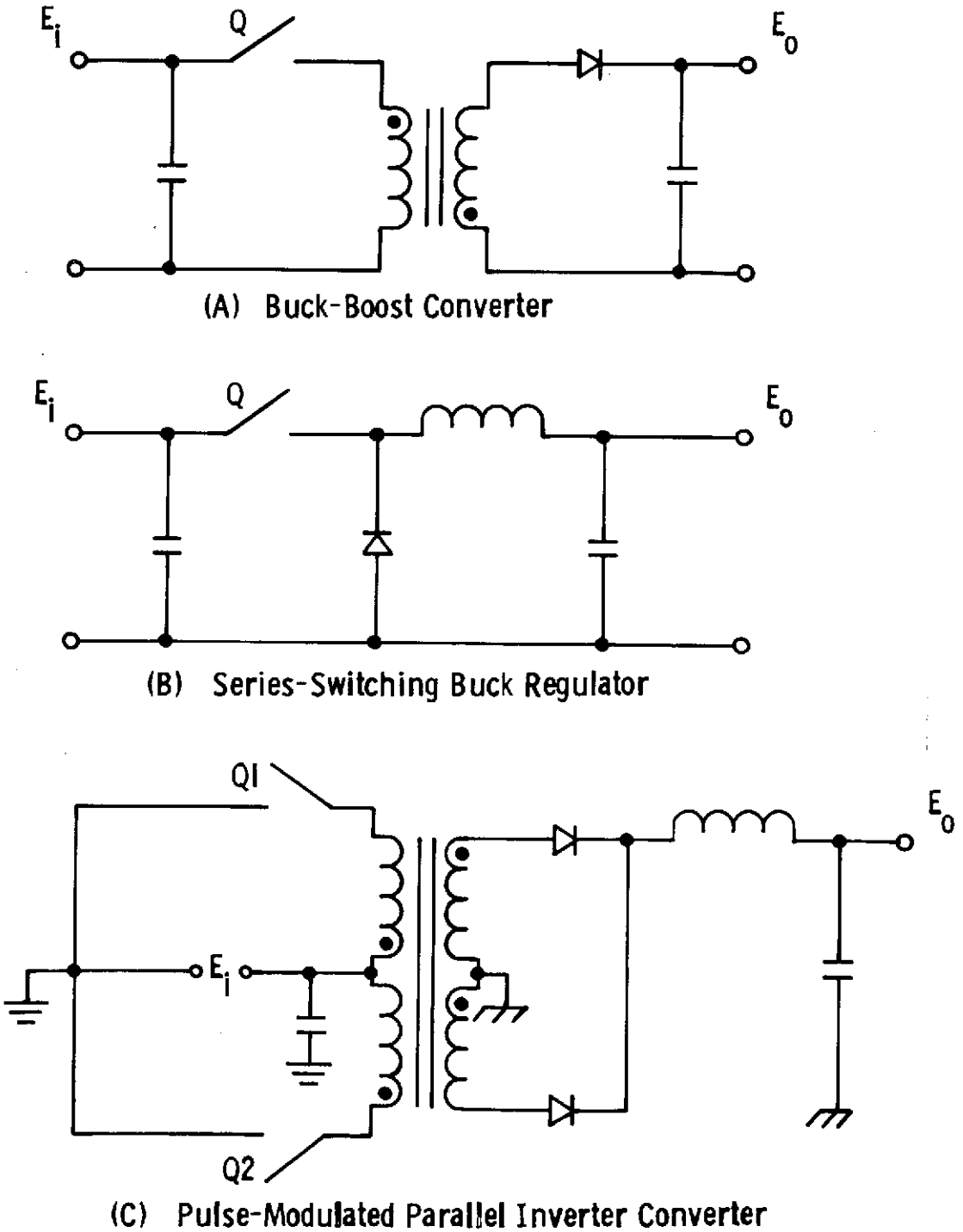

Figure 6. Power Configurations of the Three Demonstration Converter Models

Table 1. SUMMARY OF DC TO DC CONVERTER SPECIFICATIONS

PERFORMANCE PARAMETERS	BUCK BOOST CONVERTER	SERIES SWITCHING BUCK-REGULATOR	PULSE MODULATED PARALLEL-INVERTER	REQUIREMENT OBJECTIVE
Audio Susceptibility Test	2.8V RMS	2.8V RMS	2.8V RMS	Demonstrate ASDTIC line rejection
Source Current Ripple	MIL-STD-461 (N3)	MIL-STD-461 (N3)	MIL-STD-461 (N3)	Typical Space Requirement
Reverse Input Protection	yes	yes	yes	Fool-proof
Temperature Range	-25°C to 85°C	-25°C to 85°C	-25°C to 85°C	Abnormal space environment
Input Voltage Range	20 to 40V	24 to 40V	24 to 40V	Demonstrate wide input voltage range
Output Power Rating	42W	40W	60W	Typical equipment converter
Full-Load Efficiency	90%	92%	85%	Efficient Power Circuit Design
Input/Output Isolation	10 Meg-ohm	none	10 Meg-ohm	Isolation Feature
Package Weight	1.0Kg	0.75Kg	2.5Kg	Brassboard packaging larger and heavier than flight equipment to facilitate control-circuit demonstration.
Current Regulator Adjustment Regulation	10% to 100% FL ±5%	10% to 100% FL ±5%	none	Single loop current regulator for overload protection.
Output Load Voltage	28V	20V	1000V, ±15V, +5V	Demonstrate buck-boost buck, and multiple outputs
Output Voltage Regulator	±0.2%	±0.2%	(Sense → ±0.2%, ±5%, ±8% 1KV)	Precision Voltage Regulator for a single high voltage
			(Sense → ±2%, ±3%, ±6% dø/dt)	Good overall regulation for multiple outputs
Output Load Current	0.15A to 1.5A	0.2A to 2A	1000V → 0.03A to 0.04A, ±15V → 0.25A to 0.5A, +5V → 0.5A to 1A	Large load variation
P-P Output Voltage Ripple	1%	1%	0.5%, 1%, 1%	Typical for space applications

7.2 Converter Block Diagram

Utilizing the guidelines presented in Section 6, a common block diagram, shown in Figure 7, was conceived for all three converters shown in Figure 6. The broad lines represent the flow of power from input to output, proceeding from left to right. The division between the power circuitry and the control circuitry is also shown.

Before entering the description of each functional block, the following clarifications of Figure 7 are made: (1) Since the parallel inverter employs two power switches Q1 and Q2 rather than a single switch Q as each of the other two converters, dual sets of peak-current sensors, energy-recovery networks, and proportional current drives are required, (2) The blocks enclosed by dotted lines are applicable only partially to the three converters as required, (3) While only a single output is shown in Figure 7, the pulse modulated parallel inverter actually supplies four output-load voltages listed in Table 1, and (4) A dØ/dt sensor sensing the rate of flux change in the inverter transformer is incorporated in the parallel inverter as an alternate means of load voltage control in addition to sensing and regulating the 1KV output, thus achieving no precise regulation for any specific output, but a better across-the-board regulation for all four outputs. With these points clarified, the commonality of all three converters, based on an identical functional block diagram, becomes evident.

Detailed functions performed by converter power and control blocks are presented in Tables 2 and 3, respectively. The design of these functions was guided by the groundrules prescribed in Section 6. In this program, one breadboard and two brassboards were designed, fabricated, and tested for each of the three aforementioned converters.

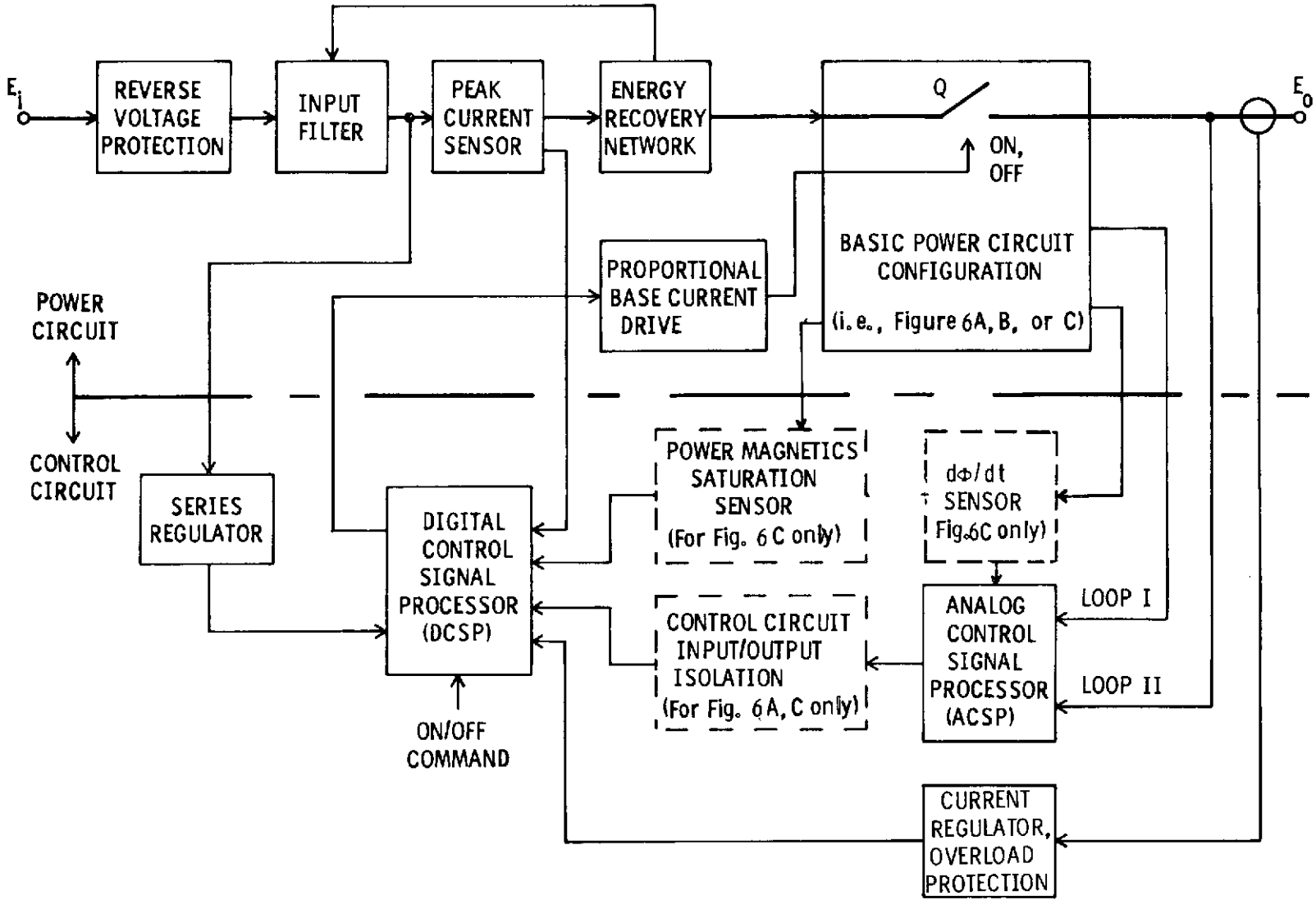

Figure 7. A Common Block Diagram For All Three Converters

Table 2. SUMMARY OF POWER-CIRCUIT FUNCTIONS

POWER CIRCUIT FUNCTIONAL BLOCKS	DESCRIPTION OF POWER CIRCUIT FUNCTIONS
REVERSE INPUT PROTECTION	PROTECTION AGAINST INADVERTENT APPLICATION OF A REVERSED POLARITY INPUT TO THE CONVERTER.
INPUT FILTER	TO ATTENUATE THE ALTERNATING CURRENT COMPONENT GENERATED BY THE CONVERTER SWITCHING SO THAT THE CURRENT REFLECTED BACK INTO THE SOURCE SHALL MEET THE DESIGN GOAL, AND TO PREVENT THE SOURCE-VOLTAGE TRANSIENTS FROM ADVERSELY AFFECTING THE CONVERTER OPERATION.
PEAK CURRENT SENSOR	OVER THE NORMAL STEADY-STATE OPERATION, THE PEAK CURRENT SENSOR REMAINS INEFFECTIVE. HOWEVER, IT DETECTS ANY TRANSIENT POWER-SWITCH CURRENT GREATER THAN A PRE-SET VALUE, AND PROVIDES AN INPUT TO THE DCSP TO EFFECT AN IMMEDIATE TURN-OFF OF THE POWER SWITCH. FOLLOWING A CONTROLLED OFF TIME, THE POWER SWITCH IS TURNED ON AGAIN. IF THE CAUSE FOR THE EXCESSIVE PEAK CURRENT IS NO LONGER PRESENT, THE PEAK-CURRENT SENSOR WILL AGAIN BECOME INEFFECTIVE. SINCE THE CURRENT IN OTHER POWER COMPONENTS IS INTIMATELY RELATED TO THE INSTANTANEOUS LEVEL OF THE POWER-SWITCH CURRENT, THE PEAK-CURRENT SENSOR ESSENTIALLY CONTROLS THE ELECTRICAL STRESSES OF ALL POWER COMPONENTS DURING ANY LINE, LOAD, AND CIRCUIT TRANSIENT INCLUDING CONVERTER STARTING AND SUDDEN OUTPUT FAULT. EXISTING CONVERTERS OFTEN FORSAKE THIS FUNCTIONAL BLOCK, AND RELY ON GENEROUS CURRENT DERATING OF THE POWER SWITCH AND OTHER ASSOCIATED POWER COMPONENTS TO MAINTAIN RELIABLE CONVERTER OPERATION. SUCH A PRACTICE NOT ONLY PLACES THE CONVERTER AT THE MERCY OF UNCONTROLLED TRANSIENT CURRENTS, BUT IT WILL BECOME INEVITABLY IMPRACTICAL IN VIEW OF THE FORTHCOMING HIGHER POWER RATING OF FUTURE CONVERTERS.
ENERGY RECOVERY NETWORK	IT REDUCES THE SWITCHING LOSS IN THE POWER TRANSISTOR SWITCH. BY PROCESSING THIS OTHERWISE LOST ENERGY AND FEEDING IT BACK TO THE INPUT FILTER, CONTROL OF TRANSISTOR PEAK-POWER DISSIPATION AND IMPROVEMENT OF CONVERTER EFFICIENCY ARE SIMULTANEOUSLY ACHIEVED.
PROPORTIONAL BASE CURRENT DRIVE	IN ACCORDANCE WITH THE SIGNAL OBTAINED FROM THE DCSP, IT PROVIDES A PROPORTIONAL BASE-COLLECTOR CURRENT DRIVE FOR THE POWER TRANSISTOR SWITCH. ADVANTAGES OFFERED BY THE CURRENT DRIVE INCLUDE (1) OPTIMUM BASE LOSS WITH WIDE LINE AND LOAD VARIATIONS, (2) SHORT TRANSISTOR STORAGE TIME AT LIGHT LOAD, AND (3) IMPROVED RELIABILITY
BASIC POWER CIRCUIT CONFIGURATION	POWER MODULATION/VOLTAGE TRANSFORMATION (SINGLE OR MULTIPLE OUTPUT FILTERING, POWER-CIRCUIT INPUT/OUTPUT ISOLATION FOR BUCK-BOOST AND PARALLEL-INVERTER CONVERTERS).

Table 3. SUMMARY OF CONTROL-CIRCUIT FUNCTIONS

CONTROL-CIRCUIT FUNCTIONAL BLOCKS	DESCRIPTION OF CONTROL CIRCUIT FUNCTION
ANALOG CONTROL SIGNAL PROCESSOR (ACSP)	IT UTILIZES TWO-LOOP SENSING, DESCRIBED IN SECTION 3. LOOP I SENSES THE AC VOLTAGE ACROSS THE ENERGY-STORAGE INDUCTOR. LOOP II SENSES THE CONVERTER DC OUTPUT VOLTAGE. WORKING IN UNISON WITH A THRESHOLD DETECTOR, THE ACSP PROVIDES A DIGITAL OUTPUT SIGNAL TO EFFECT POWER-SWITCH DUTY CYCLE CONTROL FOR PRECISION REGULATION OF THE CONVERTER OUTPUT VOLTAGE.
CONTROL CIRCUIT INPUT/ OUTPUT ISOLATION	BY NECESSITY, THE ACSP, THROUGH THE VOLTAGE DIVIDER AND INTEGRATING ERROR AMPLIFIER, IS OHMICALLY COUPLED TO THE CONVERTER OUTPUT. THE DCSP PROCESSING THE ACSP DIGITAL OUTPUT, HOWEVER, MUST BE COUPLED TO THE CONVERTER INPUT SO AS TO REMAIN OPERATIONAL EVEN WHEN THE CONVERTER OUTPUT IS SHORT CIRCUITED. IT IS FOR THIS REASON THAT THE CONTROL CIRCUIT INPUT/OUTPUT ISOLATION BLOCK IS NEEDED BETWEEN THE ACSP AND THE DCSP FOR THE BUCK-BOOST AND THE PARALLEL-INVERTER CONVERTER, WHERE THE INPUT AND OUTPUT POWER CIRCUITS ARE ALSO ISOLATED.
DIGITAL CONTROL SIGNAL PROCESSOR (DCSP)	THE DCSP IS THE NERVE CENTER OF THE CONTROL SYSTEM,,AS IT MUST PROCESS ALL INCOMING SIGNALS AND TRANSMIT THE CORRECT OUTPUT SIGNAL TO OPERATE THE POWER SWITCH. THE SIGNALS IT RECEIVES ARE FROM (1) THE ACSP AND THE CURRENT REGULATORS, (2) PEAK-CURRENT SENSOR, (3) ON/OFF COMMAND, AND (4)EXTERNAL FREQUENCY SYNCHRONIZATION, IF NEEDED. IN THE CONTROL CIRCUIT MECHANIZATION, THE DCSP ALSO DETERMINES (1) THE CONDUCTION TIME OF THE POWER SWITCH AS A FUNCTION OF THE CONVERTER INPUT VOLTAGE, AND (2) A MINIMUM NONCONDUCTION OR OFF TIME FOLLOWING TERMINATION OF EACH CONDUCTION INTERVAL WHEN THE PEAK-CURRENT SENSOR IS EFFECTIVE. THE ACSP OR CURRENT REGULATOR ONLY OVERRIDES THE MINIMUM OFF TIME, AND LENGTHENS THE OFF TIME TO THE LEVEL REQUIRED FOR REGULATION.
SERIES REGULATOR	DURING THE CONVERTER STARTUP AND THE CURRENT-REGULATING OR OVERLOAD MODE, THE SERIES REGULATOR RECEIVES THE CONVERTER INPUT AND PROVIDES A REGULATED DC VOLTAGE FOR THE DCSP, THE CURRENT REGULATOR, THE PROPORTIONAL BASE CURRENT DRIVE, THE PEAK CURRENT SENSOR, AND THE INPUT HALF OF THE INPUT/OUTPUT ISOLATION. HOWEVER, DURING THE NORMAL OPERATION WHEN THE RATED VOLTAGE IS MAINTAINED AT THE CONVERTER OUTPUT, THE SERIES REGULATOR IS CONTROLLED TO OPERATE IN ITS "OFF" STATE BY THE APPLICATION AT ITS OUTPUT TERMINALS A VOLTAGE HIGHER THAN ITS REFERENCE LEVEL. SUCH AN APPLIED VOLTAGE IS READILY OBTAINED THROUGH A RECTIFIER-FILTER IN CONJUNCTION WITH A WINDING ON THE POWER MAGNETICS OF EACH CONVERTER. BY SO DOING, THE POWER REQUIRED BY THE VARIOUS CONTROL SYSTEM BLOCKS DURING NORMAL CONVERTER OPERATIONS IS DERIVED FROM THE SWITCHING CONVERTER RATHER THAN THE SERIES REGULATOR, THUS SIGNIFICANTLY IMPROVING CONVERTER EFFICIENCY.
CURRENT REGULATOR	ITS FUNCTIONS ARE: (1) TO PROVIDE AN ADJUSTABLE REGULATED CURRENT AS REQUIRED, AND (2) TO ENHANCE THE PROTECTION AGAINST OVERCURRENT, WHICH MAY BE CAUSED, FOR EXAMPLE, BY A SUSTAINED SHORT CIRCUIT AT THE CONVERTER OUTPUT.
POWER MAGNETICS SATURATION SENSOR	THE SPECIAL POWER TRANSFORMER CONFIGURATION USED IN THE PARALLEL-INVERTER CONVERTER EMPLOYS TWO UNCUT SATURABLE CORES. BY LETTING ONE CORE SATURATE BEFORE THE OTHER, AN ADVANCE SIGNAL IS GENERATED WITH A CONTROLLED LEAD TIME FOR INITIATING THE TURN-OFF OF THE CONDUCTING TRANSISTOR. THROUGH SUCH A MECHANIZATION, THE IMPENDING CORE SATURATION IS ANTICIPATED, AND THE POWER SWITCH IS TURNED OFF SUFFICIENTLY IN ADVANCE TO ELIMINATE THE NORMALLY-HIGH SATURATION CURRENT.

8. POWER AND CONTROL CIRCUIT DESCRIPTIONS

In section 7.2 a common functional block diagram was illustrated for all three demonstration-model dc to dc converters. In this section, circuit design and operation of each functional block will be described. The converter schematics corresponding to the three power configurations of Figure 6 are given in Figures 8, 9, and 10. Descriptions are presented for all power circuits and control circuits in terms of these schematic diagrams.

8.1 Converter Schematics

The dividing lines in Figures 8, 9, and 10, similar to the division shown in the aforementioned block diagram, illustrate the division of components in the breadboard and brassboard models between power circuit assemblies and control circuit modules.

The pertinent electrical parameters of power- and control-circuit parts in each functional block for all three converters are identified in Appendix E.

8.2 Power-Circuit Description

Basic Power Stage Configurations

The basic power-stage configurations for the three converters are described in Tables 4, 5, and 6 and Figures 11, 12, and 13. The presentation includes operations, waveforms, design equations and criteria used in designing the basic power stages.

Other Power Circuit Blocks

To facilitate a smooth flow of concise technical information in the main text of this report, the very detailed circuit descriptions and design criteria of power circuits associated with all three converters are being reserved in its separate entirety. Readers who are particularly interested in specific design and operation details of the converter power circuits are hereby referred to Appendix F.

8.3 Control-Circuit Description

Similarly, circuit descriptions and design criteria of control-circuit functional blocks for all three converters are presented in Appendix G.

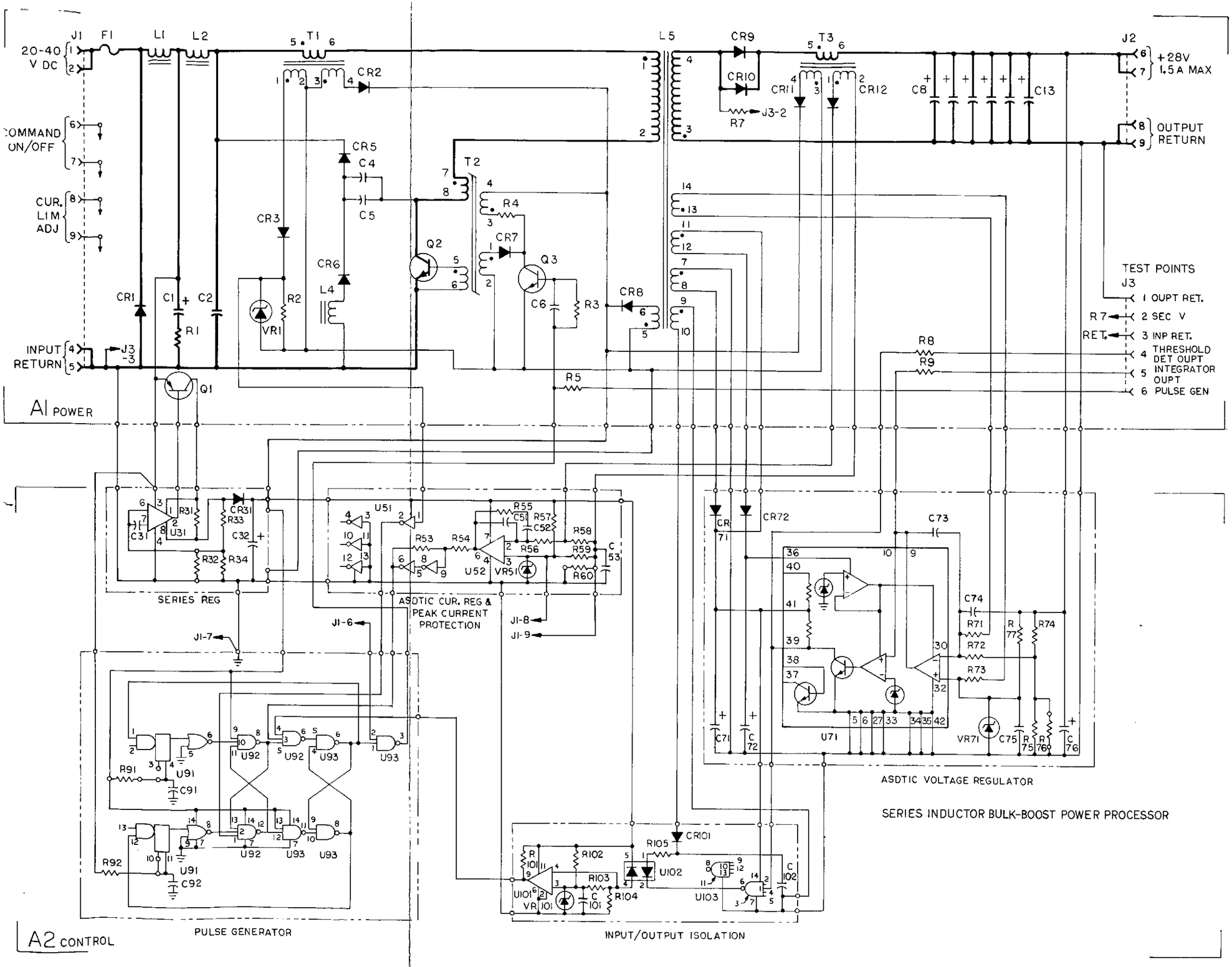

Figure 8. Schematic Diagram of the Buck-Boost Converter

FOLDOUT FRAME

FOLDOUT FRAME

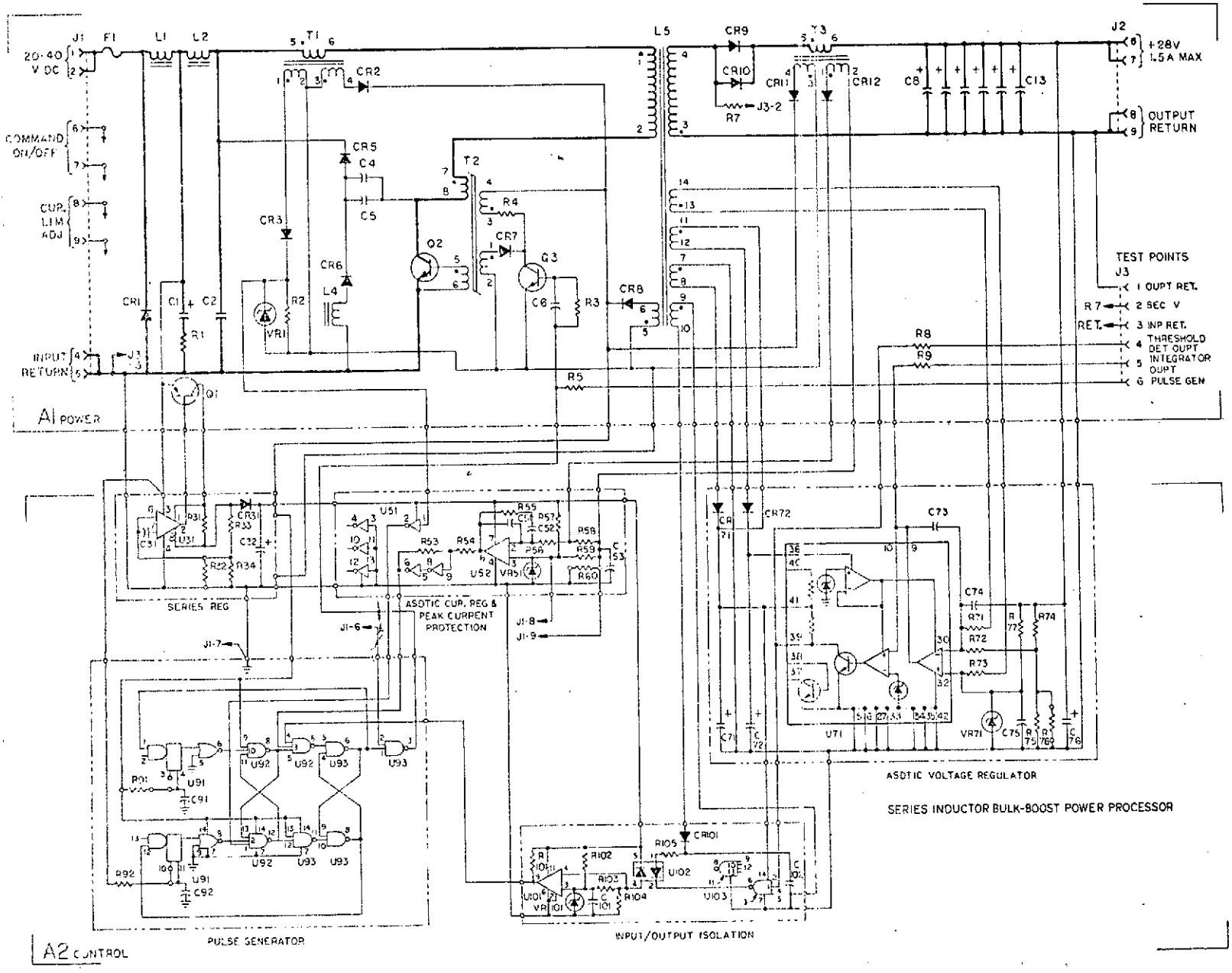

Figure 8. Schematic Diagram of the Buck-Boost Converter

ME

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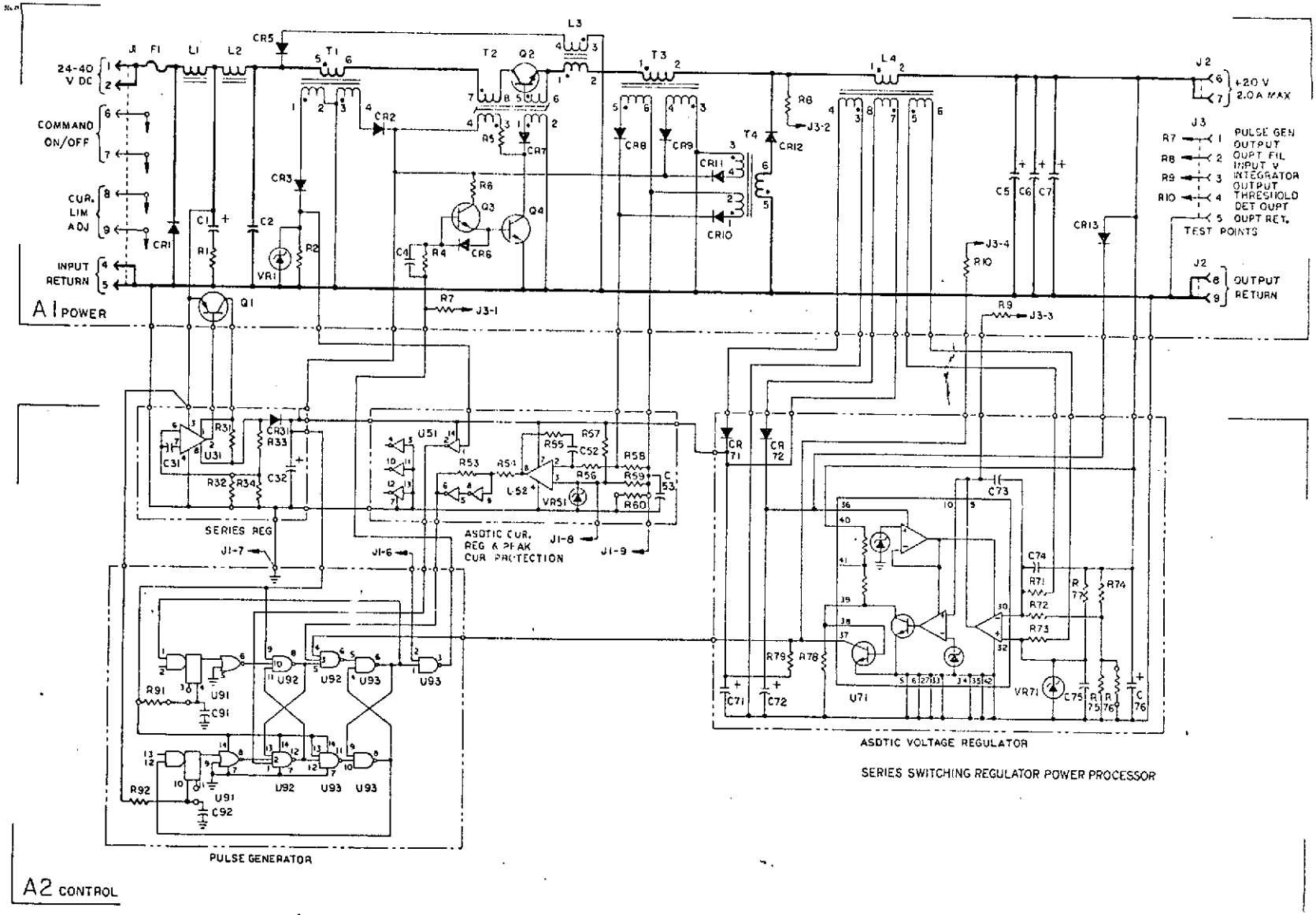

Figure 9. Schematic Diagram of the Series Switching Buck Regulator

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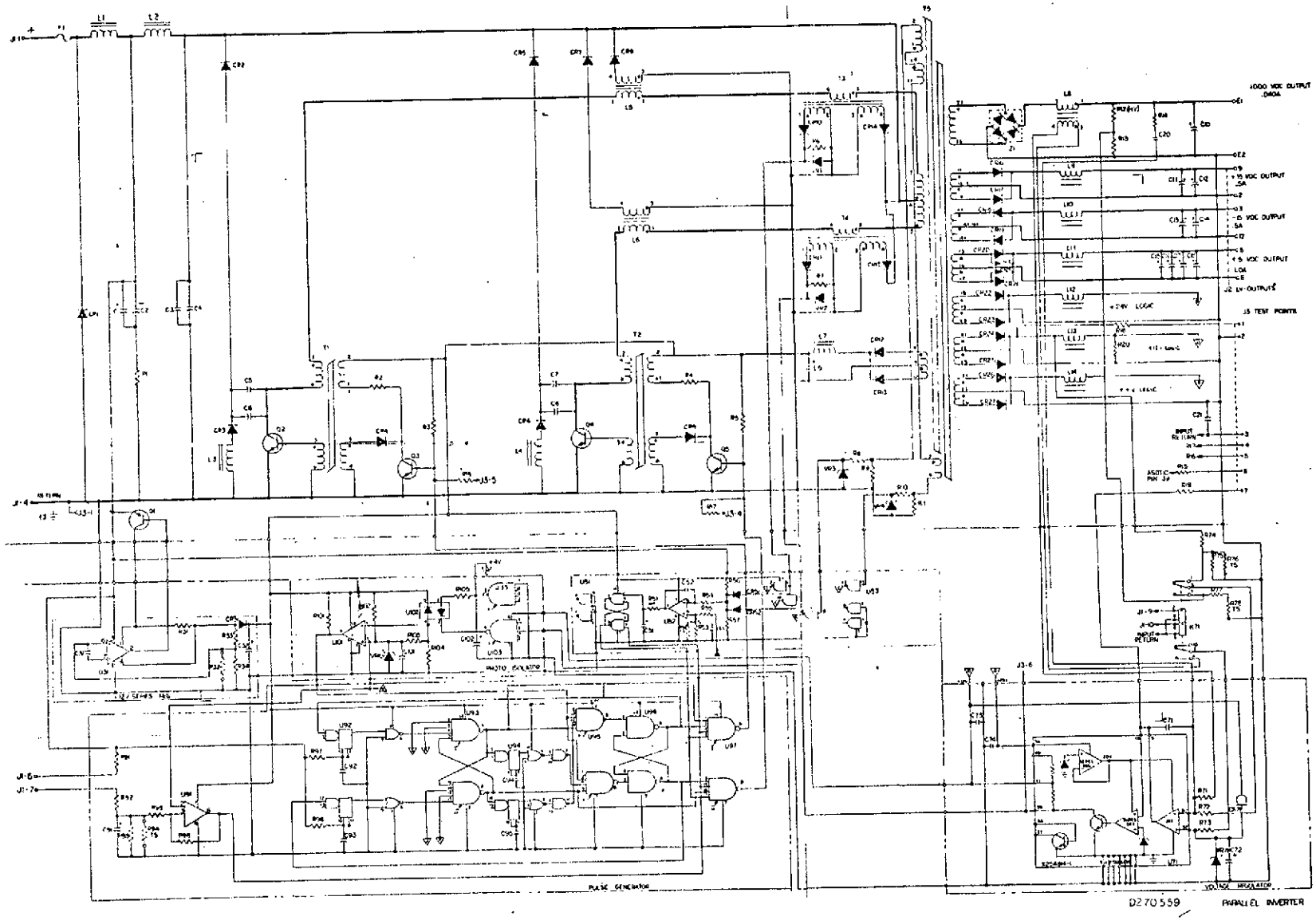


Figure 10. Schematic Diagram of the Pulse Modulated Parallel-Inverter Converter

36

NOT REPRODUCIBLE

Table 4. BASIC BUCK BOOST CONFIGURATION

(1) CIRCUIT AND WAVEFORMS

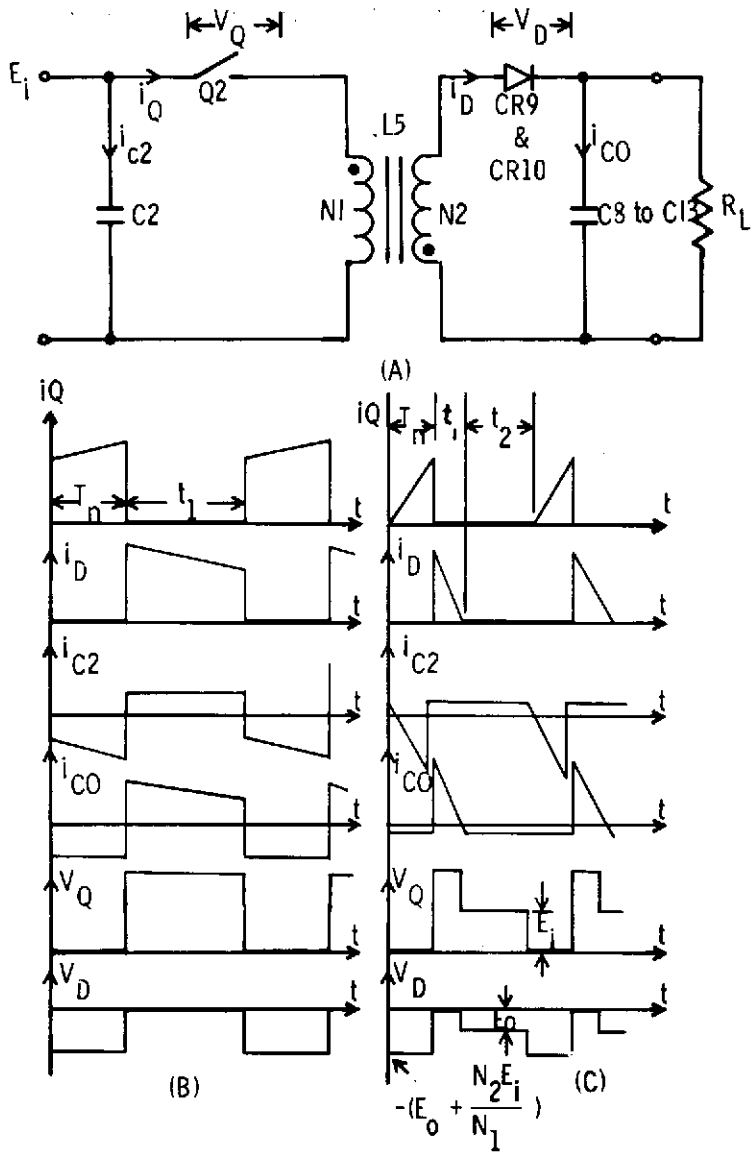


Figure 11. Buck Boost Converter Configuration and Waveform.

In Figure 11(A), the energy-storage inductor utilizes a core which has a fairly linear flux vs MMF characteristic. Energy is derived from the power source (in this case through the input filter), and stored inductively in the inductor during on-time interval T_n when power transistor Q2 is conducting. When it is turned off, a current flow through the inductor secondaries must occur, since the MMF of the core cannot change instantaneously. Thus the energy previously stored in the primary inductance during T_n is delivered from the secondary winding during the off half cycle, T_f, as output energy. Through fast recovery diodes CR9 and CR10, the energy is received by the load and filter capacitors C8 through C13. Notice that the energy is delivered to the output in the form of a series of unidirectional current pulses, allowing the output filter to be merely capacitors.

Depending on the line and load conditions, the operating waveforms for a given design can have either a non-zero MMF in the inductor at heavy load, or a zero MMF during a portion of the power switch off time in each cycle at light load.

These two conditions are shown in Figures 11(B) and (C).

Table 4. BASIC BUCK BOOST CONVERTER CONFIGURATION (CONT'D)

(2) DESIGN CRITERIA

Based on relationships for volt-second balance on the inductor and energy balance for the converter, time intervals t_1 and t_2 are derived in terms of T_n, input E_i, output E_o, and load resistance R_L, where

$$t_1 = \frac{E_i T_n}{E_o} \frac{N_2}{N_1}$$

$$t_2 = \frac{eE_i^2 R_L T_n - 2L_p E_o (E_o + \frac{N_2 E_i}{N_1})}{2L_p E_o^2} T_n$$

Here, e is the efficiency, and L_p is the primary inductance of the converter. Notice that a critical $R = R_k$ exists, below which t_2 becomes negative, i.e., physically unrealizable. This resistance value can be predicted by letting t_2 be zero, and solving for R_L, where

$$R_L = R_k = \frac{2L_p E_o (\frac{E_o}{E_i} + \frac{N_2}{N_1})}{eE_i T_n}$$

The period of T for each steady-state cycle is:

$$T = T_n + t_1 = T_n \left(1 + \frac{E_i N_2}{E_o N_1}\right), \quad R_L \leq R_k$$

$$T = T_n + t_1 + t_2 = \frac{eR_L (E_i T_n)^2}{2L_p E_o^2} = \frac{e(E_i T_n)^2}{2L_p P_o} \quad R_k < R_L$$

where $P_o = E_o^2/R_L$ is the converter output power.

In this design, $T \cong 40\mu s$ for $R_L \leq R_k$.

Tradeoff studies were undertaken to identify the optimum power circuit design. The study results indicated that, with the specified line and load ranges, the design giving a zero t_2 at heavy load and a non-zero t_2 at light load, would provide the highest efficiency and minimum weight. To carry out this design philosophy, the threshold between zero and non-zero t_2 is set to occur at a converter input voltage of 20V and an output corresponding to one-third of the full load.

With an input voltage variation between 20V to 40V and a regulated output voltage at 28V, a unity turns ratio for N1 and N2 becomes attractive for two reasons: (1) Such a turns ratio will cause a duty cycle that does not approach zero or unity, thus relieving the switching characteristic requirements of semiconductors and leaving ample time to reset various magnetics; (2) Such a turns ratio facilitates the use of bifilar windings for N1 and N2. With N2/N1 = 1, E_o = 28V, e = 0.9, E_1 = 20V, $E_i T_n = 560 \times 10^{-6}$ vs, and R_k = 60 ohms (i.e., about one-third of full load), inductance L_p is calculated to be 220μH.

Using the same notation, the peak flux density in the core, B_p, is

$$B_p = \frac{P_o}{eE_i} \frac{L_p}{N_1 A} \left(1 + \frac{N_2 E_i}{N_1 E_o}\right) + \frac{E_i T_n}{2N_1 A}, \quad A = \text{core area}$$

Equations prescribing a minimum weight inductor design are given in Appendix B, which are also applicable for inductor design of other converters.

To reduce the core loss, a ferrite toroid with cut gaps along its diameter was selected to achieve the desired permeability. The converter efficiency improvement as a result of changing to the ferrite core was calculated to be about one percent.

For a given inductor and a specified $E_i T_n$, the steady-state power rating of the transistor and the diode are readily determined from the worst-case voltage and current over the range of line and load variations. Other selection criteria include the current gains, the conduction voltage drop, the switching characteristic and its effect on control circuit noise susceptibility, the storage time, and the secondary breakdown susceptibility.

From a weight viewpoint only, a C-L-C filter is more attractive than a capacitor filter. However, the capacitor filter is superior with respect to its power loss and its output impedance, and is selected for the design. AC capacitors with negligible ESR's, such as the polycarbonate type, were considered but not chosen, due to their excessive size and weight. Six tantalum-foil capacitors in parallel, with 100μF each, are then chosen to meet the 1% peak-to-peak output ripple requirement at the cold environment (-25°C) when the ESR of the capacitor is the highest.

Table 5. BASIC SERIES SWITCHING BUCK REGULATOR CONFIGURATION

(1) CIRCUIT AND WAVEFORMS

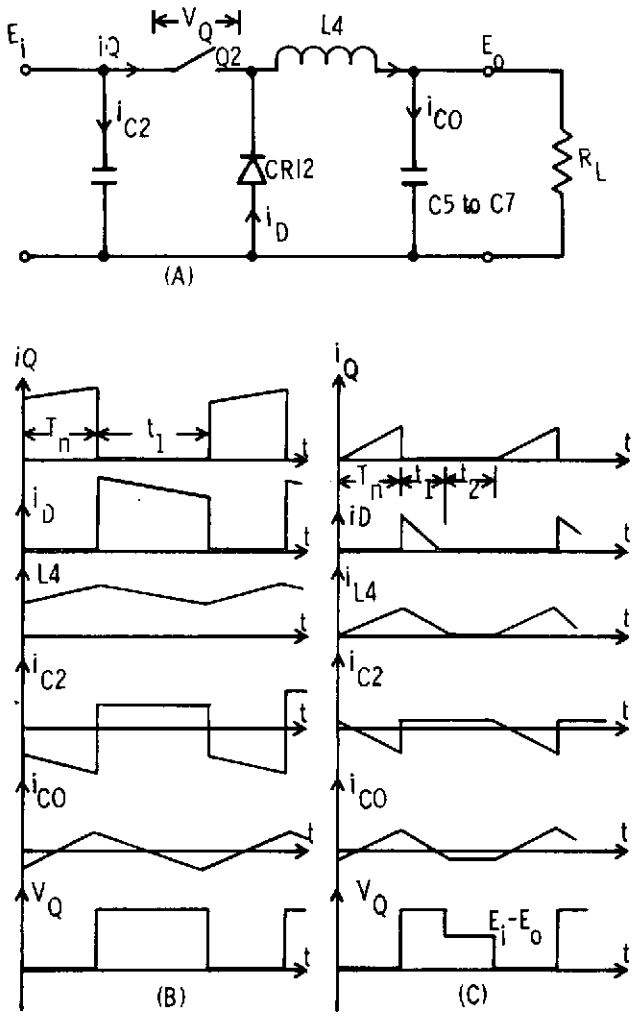


Figure 12 Series Switching Regulator Configuration and Waveform

In Figure 12(A), transistor Q2 is controlled by the ASDTIC module to turn on and off cyclically for respective time intervals T_n and T_f. During T_n, CR12 is reverse biased, and voltage E_i is applied to the output filter. During T_f, CR12 conducts to maintain the MMF continuity in L4, and an essentially zero voltage is applied to the filter. After averaging by the filter, a dc output voltage E_o is obtained.

Table 5. BASIC SERIES SWITCHING BUCK REGULATOR CONFIGURATION (CONT'D)

(2) DESIGN CRITERIA

In the subject converter, the control circuit is implemented in such a way that time interval T_n is inversely proportional to input voltage E_i, or,

$$T_n = \frac{\text{Constant}}{E_i}$$

Based on relationships for volt-second balance on the inductor and energy balance for the converter, time intervals t_1 and t_2 are derived in terms of T_n, E_i, E_o, and R_L, where

$$t_1 = \frac{E_i - E_o}{E_o} T_n$$

$$t_2 = \frac{dR_L E_i^2 (E_i - E_o) T_n - 2L\, E_i E_o^2}{2L\, E_o^3}\, T_n$$

Here, e is the efficiency, and L is the filter inductance. Notice that a critical $R_L = R_k$ esists, below which t_2 becomes negative, i.e., physically unrelizable. This resistance value can be predicted by letting t_2 be zero, and solving for R_L, where

$$R_L = R_k = \frac{2LE_o^2}{eE_i T_n (E_i - E_o)}$$

From equations representing T_n, t_1, and t_2, the period T of a steady-state cycle is

$$T = T_n + t_1 = \frac{E_i T_n}{E_o}, \quad R_L \leq R_k$$

$$T = T_n + t_1 + t_2 = \frac{e\left(\frac{E_i}{E_o} - 1\right)(E_i T_n)^2}{2LP_o}, \quad R_k < R$$

where $P_o = E_o^2/R_L$ is the converter output power. In this design,

$$T \cong 30\ \mu s \text{ for } R_L < R_k$$

Similar to the buck-boost converter, the approach for $t_2 = 0$ at heavy load and $t_2 > 0$ at light load yields optimum efficiency and weight. The threshold between zero and non-zero t_2 is designed to occur at an input of 32V and an output corresponding to one-third of the full load. With E_o = 20V, e = 0.92, E = 32V, $E_i T_n = 600 \times 10^{-6}$ VS, and R_k = 30 ohms, inductance L is calculated to be approximately 250 μH.

The peak-flux density in the core is:

$$B_P = \frac{LP_o}{NAE_o} + \frac{(E_i - E_o)T_n}{2NA}$$

where N is the number of turns on the inductor, and A is the cross sectional area of the core. Using the magnetics design equations presented in Appendix B, the optimum permeability is determined to be 125 gauss/oersted. Preliminary weight and efficiency estimate shows that the required efficiency of 92% can be achieved without special ferrite core design. Consequently, a molypermalloy powder core is used for the inductor.

The selection criteria for Q2 and CR12 are similar to those presented for the buck-boost converter.

Three tantalum foil capacitors, each a 100μF, are used to meet the 1% ripple requirement at -25°C when the ESR of each capacitor is the highest.

Table 6. BASIC PARALLEL-INVERTER CONVERTER CONFIGURATION

(1) CIRCUIT AND WAVEFORM

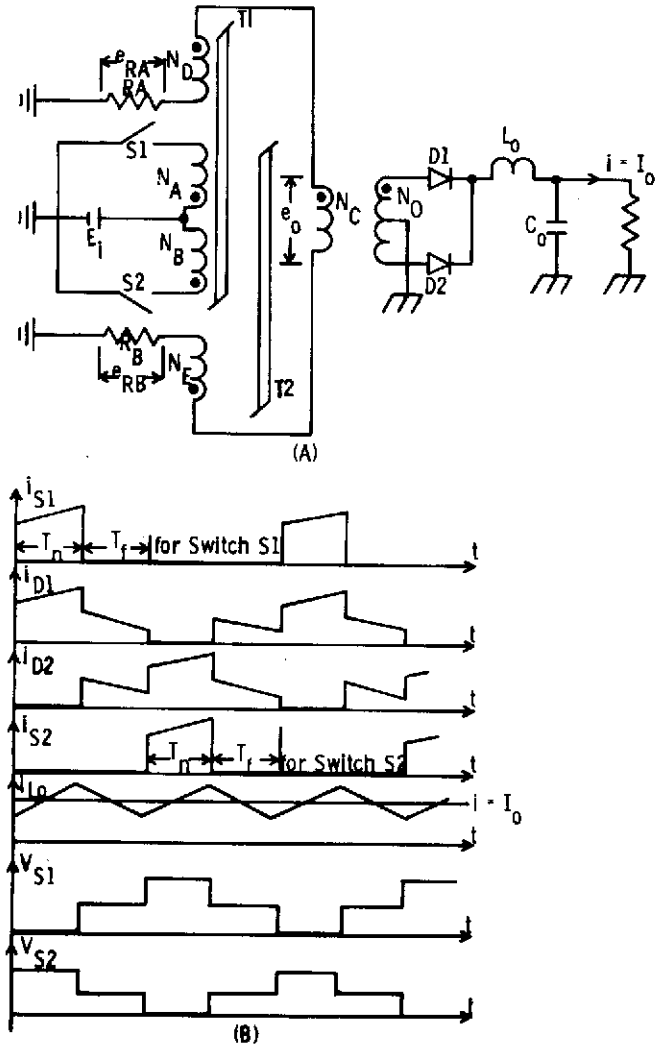


Figure 13. Parallel-Inverter Converter Configuration and Waveform

In pulsewidth modulation (PWM) converter shown in Figure 13, each of the two switches, S1 or S2, is controlled to turn on and off cyclically; conduction of both S1 and S2 are mutually-exclusive events. The L_oC_o filter of each output receives an input voltage corresponding to $(N_o/N_A)E_i$ during T_n, and receives an essentially zero voltage during T_f. This voltage pulse train is averaged by the output filter to yield the required output voltage.

The utility of high-power parallel inverter has been hampered by high-stress conditions caused by the saturation of the power transformer. Saturation is either necessary to turn off the conducting switch, [29] or it is inevitable due to asymmetry between the two inverter halves. The asymmetry cyclically impresses a differential volt-second increment to the core, resulting in its ultimate saturation at one end of its BH loop. Even when a saturation sensor is used, the inability of the transistor switch to turn off immediately after detection of saturation by the sensor (due to signal delay and the transistor storage time) generally results in a very high saturation current before the eventual interruption. This high current causes heavy electrical stresses on transistor switches, which results in lower converter efficiency and reliability. Such losses establish an urgent need for a method to anticipate the impending core saturation. The anticipation initiates the turn-off of the power switch sufficiently in advance of saturation, so that by the time the switch is opened, appreciable saturation current is yet to materialize.

A published two-core transformer configuration [30] seemed applicable for fulfilling such a need. The design was originally intended for a free-running parallel-inverter. Extending the same technique to a PWM parallel-inverter converter was investigated and experimentally demonstrated by first designing and operating a low power, low voltage PWM parallel inverter using the two-core configuration. Successful completion of this task led to the high power, high voltage design meeting all the requirements for the various loads specified in this contract.

The transformer configuration employs two identical, uncut saturable cores. By letting one core saturate before the other, an advance signal is generated with a controlled lead time for initiating the turn-off of the conducting transistor. Through such a mechanism, a complete prevention of saturation-current spike is achieved.

Table 6. BASIC PARALLEL-INVERTER CONVERTER CONFIGURATION (CONT'D)

(2) DESIGN CRITERIA

The transformer contains two identical cores T1 and T2, push-pull primary windings N_A and N_B, control winding N_C, and two flux-sensing windings N_D and N_E. Windings N_A, N_B, and N_C are common to both cores, while winding N_D is on T1 only, and N_E is on T2 only. The circuit loop contains N_C, N_D, and N_E is closed by resistors R_A and R_B. Generally, $N_A = N_B$, $N_D = N_E$, and $R_A = R_B$.

To analyze the steady-state performance of the two-core transformer, let both core flux start ascending from their respective negative-saturation flux levels. The five equations governing the circuit operation, based on S1 conducting, are

$$N_D \frac{d\phi_1}{dt} = e_D$$

$$N_E \frac{d\phi_2}{dt} = e_E$$

$$N_A \left(\frac{d\phi_1}{dt} + \frac{d\phi_2}{dt} \right) = E_i$$

$$N_C \left(\frac{d\phi_1}{dt} + \frac{d\phi_2}{dt} \right) = e_c$$

$$-e_{RB} + e_E + e_C - e_D + e_{RA} = 0$$

The last equation above can be simplified by neglecting e_{RA} and e_{RB}, which holds during normal converter operation when T1 and T2 are not saturated. By so doing, solutions for $d\phi_1/dt$ and $d\phi_2/dt$ can be derived as:

$$\frac{d\phi_1}{dt} = \left(\frac{E_i}{N_A} \right) \left(\frac{N_E + N_C}{N_D + N_E} \right)$$

$$\frac{d\phi_2}{dt} = \left(\frac{E_i}{N_A} \right) \left(\frac{N_E - N_C}{N_D + N_E} \right)$$

The above two equations identify the faster $d\phi_1/dt$ in relation to $d\phi_2/dt$. The positive saturation flux level of core T1 is thus reached first, with T2 still unsaturated. During the time interval when $d\phi_1/dt = 0$ and $d\phi_2/dt > 0$, a large voltage is impressed across e_{RA} and e_{RB}. Assuming $R_A = R_B$, and with $d\phi_1/dt = 0$, one has:

$$e_{RA} = e_{RB} = \frac{E_i}{2N_A} (N_Q + N_C)$$

Notice that a voltage of this amplitude exists whenever core T1 is saturated and core T2 is not. The voltage becomes an excellent anticipation signal for the pending saturation of T2. The proper design, therefore, is to utilize the leading edge of this voltage signal to initiate the turn-off of Switch S1. Taking into consideration the signal transport delay and the storage-time delay of S1, this design ensures that core T2 will not saturate within these delay intervals, thereby eliminating any saturation current associated with the two-core transformer. A detailed transformer design and discussion is presented in Appendix C.

The inductor in each output is designed to have an MMF greater than zero during steady-state operation. The output inductance L_o is therefore determined by the following constraint:

$$L_o > \frac{E_o (T_f)_{max}}{2 I_{o\,min}}$$

where E_o and I_o are the dc voltage and current associated with the respective output. Using this equation, L_o for the 1kV, the +15V, the -15V, and the +5V output are designed to be 0.7H, 1.25mH, 1.25mH, and 0.53mH, respectively.

The peak flux density in the core inductor is

$$B_P = \frac{L_o P_o}{NAE_o} + \frac{E_o T_f}{2NA}$$

where N is the number of turns on the inductor, A is the cross-sectional area of the inductor core, and P_o is the output power. It is clear that the maximum B_P occurs at the maximum load and the maximum line voltage when T_f is the longest.

A high voltage 15PD114K capacitor, made by Component Research, is used for C10 across the 1kV output. This capacitor provides the least weight, and is experimentally confirmed to meet the specified ripple requirement.

The solid tantalum capacitors used in the other outputs are selected to meet the specified output ripple requirements at the cold environment when the ESR's of the capacitors are the highest. Their voltage ratings are selected to be much higher than the respective output voltage specified. Thus, in case of an inadvertent open load on any output, the abnormally high open load voltage due to peak charging of the capacitor will not cause them to fail.

9. CONVERTER FABRICATION

One breadboard and two brassboard demonstration models were fabricated for each of the three converter types. The deliverable breadboards were built with the objective of achieving easy accessibility to all components. The brassboards were packaged similar to flight equipment brassboards with the understanding that they were not required to undergo any vibration or other environmental tests except for temperature testing. The following paragraphs describe the features and design characteristics of the brassboard prototypes:

9.1 General Mechanical Design Features

The following general design features were incorporated:

- Each converter has an aluminum sheet metal baseplate to which all power items are attached.
- Removable cover completely encloses the converter. No parts are mounted on the cover.
- The power circuit and the control circuit of each converter are separated into different subassemblies. The division facilitates the demonstration of the universal control circuits, exhibits modular capability, and isolates the control circuits from leads carrying high current at the power switching frequencies.

Specific features of power-circuit fabrication include:

- The power circuitry is mounted directly onto the baseplate, thus, providing a good heat sink.
- Power components were placed to follow the circuit flow from input to output.
- Careful consideration was given to provide short leads that conduct high-frequency current, and to separate them from those leads carrying critical control circuit signals, thus, minimizing electromagnetic interaction.

Specific features of control-circuit fabrication include:

- Modularization concepts were used in the layout of the control-circuit boards. The series regulator, the standardized DCSP, the input/output isolation, the ASDTIC voltage regulator, and the current regulator, are located on separate printed circuit boards. These modules are mounted on an epoxy glass base and are interconnected by jumper wires. The modular construction aids in (1) the identification of each functional block, (2) the maintainability of the control circuitry, and (3) the multiple use of parts common to all three units. The whole control board is secured on four standoffs that mount to the baseplate.
- Test points showing critical control signal flow are brought out through a connector. Each test point is protected by a series resistor. These resistors are designated as R5 to R9 in the buck-boost converter, as R7 to R10 in the series switching buck-regulator, and as R15 to R18 in the pulse modulated parallel-inverter converter.
- A copper ground plane is provided on the printed circuit board of the voltage regulator to assist heat dissipation from the micro-miniaturized ASDTIC control module.

9.2 Converter Outline, Interface, and Weight

TABLE 7. SUMMARY OF CONVERTER SIZE, INTERFACE, AND WEIGHT

Converters (Output Power)	Overall size $(mm)^3$	Interface Connectors	Converter Weight (gram)	Specified Maximum Converter Weight (grams)
Buck-boost converter (output power 42W)	170.2x177.8x45.7	Three Cannon D, one for input power, one for output power, one for test points.	862.3 without cover, or 20.5 g/watt 976.6 with cover, or 23.2 g/watt	1000
Series-switching buck regulator (output power 40W)	170.2x152.4x45.7	Same as above	682.5 without cover, or 17.1 g/watt 784.5 with cover, or 19.6 g/watt	750
Pulse-modulated parallel-inverter converter (output power 60W; four output voltages, of which one is high voltage).	152.4x127.0x193.0	Three Cannon D, one for input power, one for low-voltage output, one for test points. The high-voltage output is supplied from a high-voltage connector, which can be totally concealed during converter operation for personnel safety.	1629 without cover, or 27.1 g/watt 1868 with cover, or 31.1 g/watt	2500

9.3 Converter Assembly and Subassembly

9.3.1 Buck-Boost Converter

The various subassemblies of the mechanical structure are clearly visible in Figure 14, in which the brassboard converter is shown with the cover removed. Power components are mounted directly onto the baseplate. Also, the control board secured on four standoffs are mounted to the baseplate. The interconnection between the power board and the control board is provided by a jumper wire cable. The control board can be detached from the baseplate and folded out for easy inspection.

Starting from the upper right corner of the printed-circuit control board and tracing clockwise, the control-circuit modules are (1) the Digital Control Signal Processor - DCSP, (2) the series regulator, (3) the ASDTIC current regulator, (4) the ASDTIC voltage regulator using the micro-miniaturized ASDTIC control module, and (5) the input/output isolation.

9.3.2 Series Switching Buck Regulator Converter

The mechanical-structure assembly, shown in Figure 15, is similar to that of the buck-boost converter, with one notable exception. The "input/output isolation" subassembly is absent, as there is no such requirement for the series-switching buck-regulator converter.

9.3.3 Parallel-Inverter Converter

This converter has a different mechanical structure from the other two converters, due to the multiple outputs and the separation and isolation required for the high voltage power circuits. The configuration is shown in Figure 16, with the cover removed.

An aluminum sheet metal baseplate provides the mounting surface for the mechanical structure and electronic subassemblies. Internally, there are two aluminum sheet metal trays for mounting the electronic components. The components in the input filter circuit are mounted on one of the end plates along with the input connector, shown on the left side of Figure 16. The low voltage circuit and the control board are mounted on opposite sides of the middle sheet metal tray. The sheet metal tray on the right is the mounting surface for the high voltage circuitry on one side and the inverter section

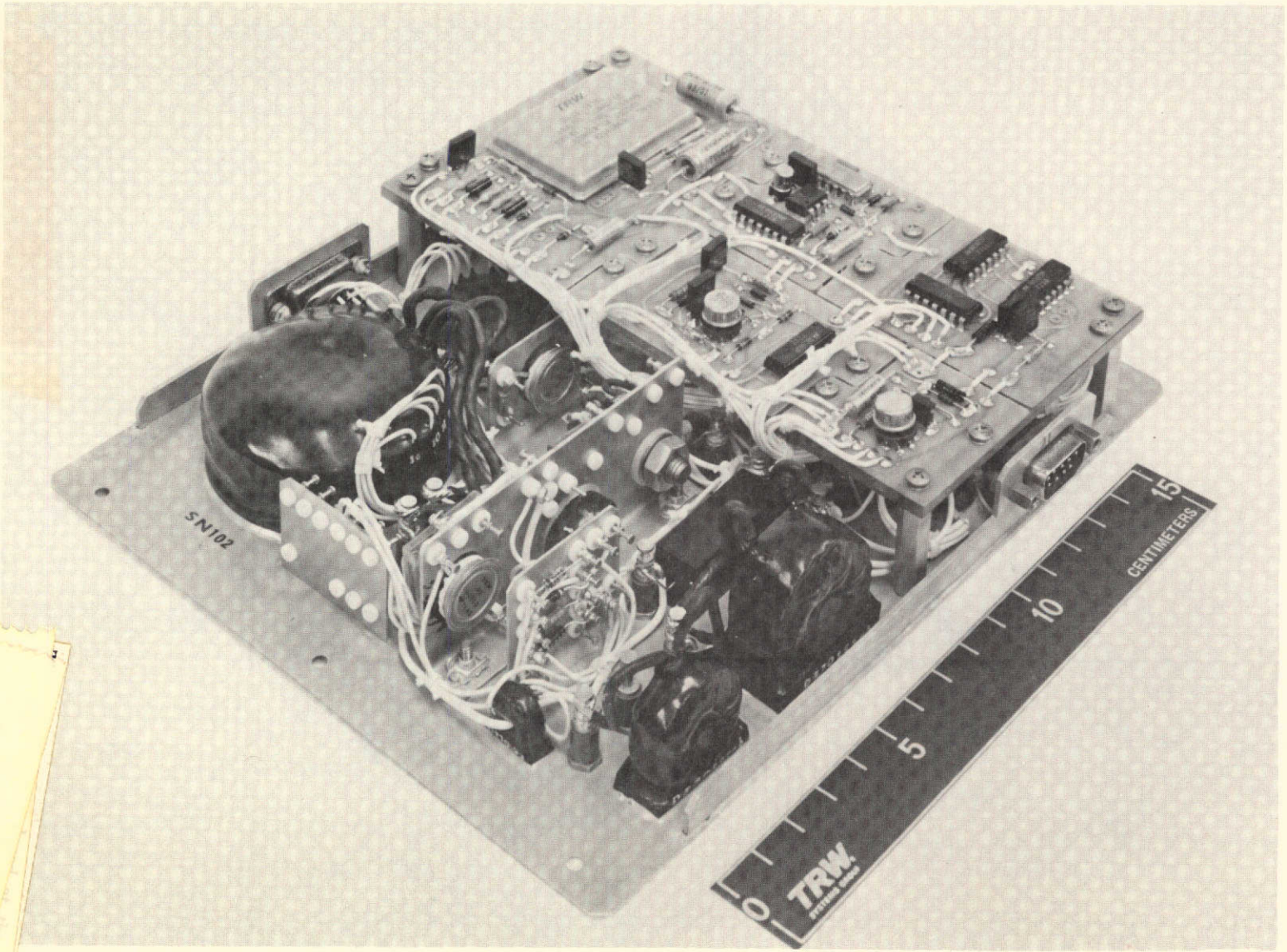


Figure 14. Buck-Boost Converter Barassboard Configuration

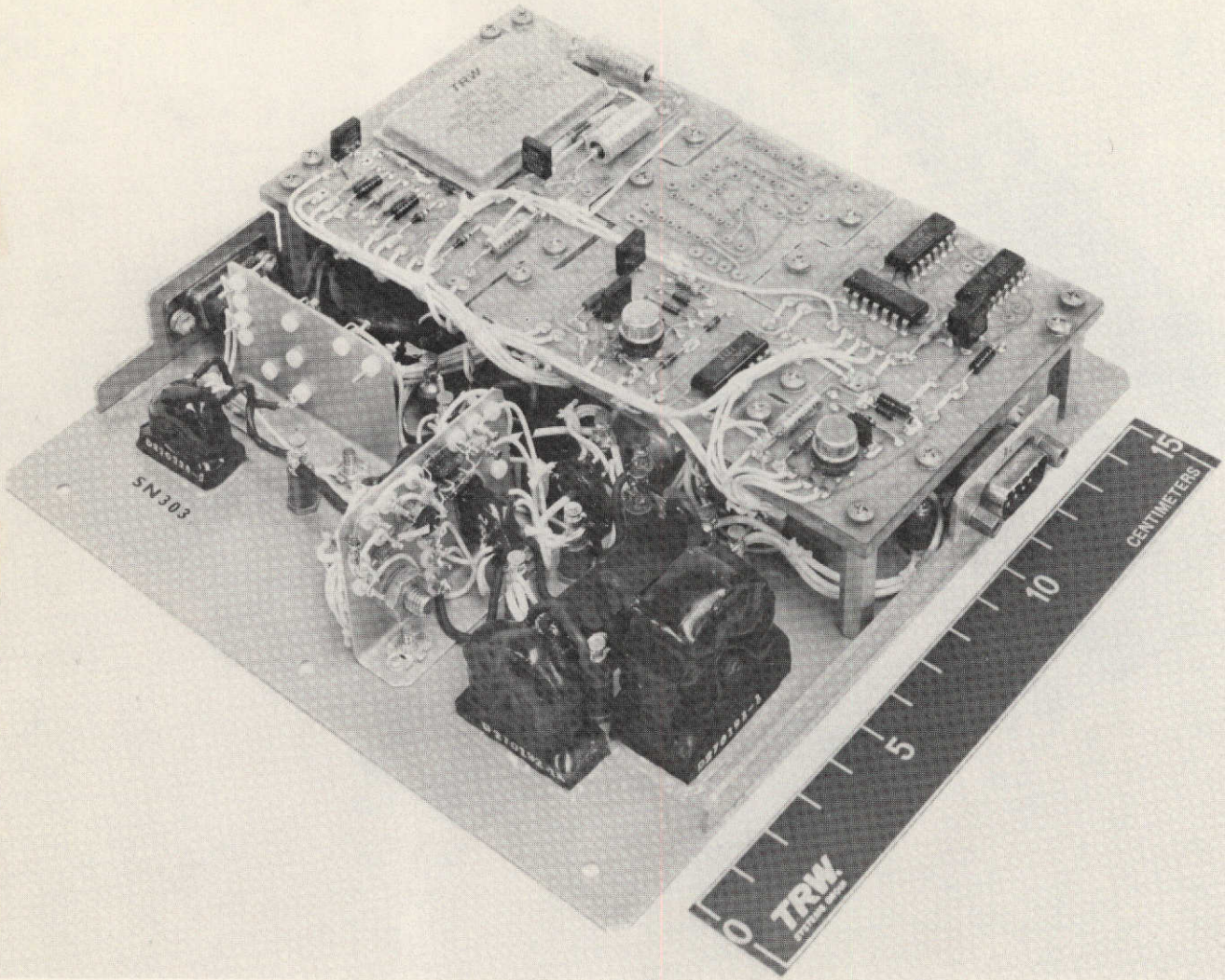


Figure 15. Series Switching Regulator Brassboard Configuration

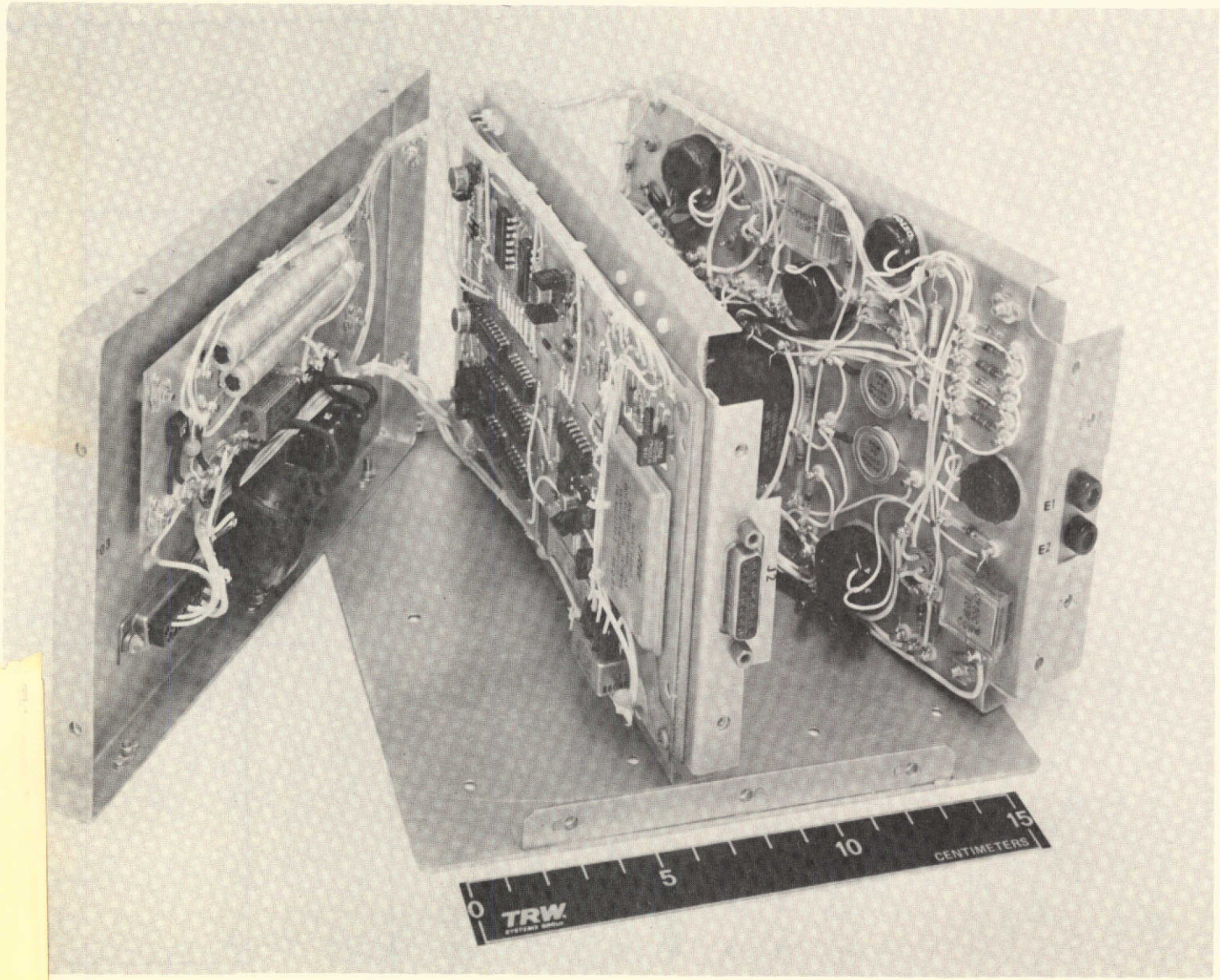


Figure 16. Parallel-Inverter Converter Brassboard Configuration

on the other side. These aluminum trays provide (1) adequate structural support for these components, (2) low thermal resistance path for conducting heat away from the power components, and (3) adequate separation between input components, the high voltage circuitry and the control circuit. Insulated terminals are mounted on the heat sink for attachment and wiring of the power circuit components. High voltage components are carefully separated and insulated to avoid voltage breakdown.

The control board is similar in concept and construction as the control board for the other two converters; it is slightly larger in size. The same considerations were given to the placement of components and separation of critical leads as were done for the other two converters.

9.4 Test Points

To exhibit the critical signal flow of the ASDTIC control system, suitable test points are provided for each converter. Observed waveforms from these test points include:

- Inductor voltage E_L, which is the ac signal input to the integrator
- Integrator output voltage E_I
- Threshold detector output voltage E_D
- Digital control signal processor (DCSP) output voltage E_P

The test points are brought out to a connector, each through a series resistance for isolation purpose. Using the buck-boost converter as an example, the test points are marked in the simplified control-system block diagram shown in Figure 17.

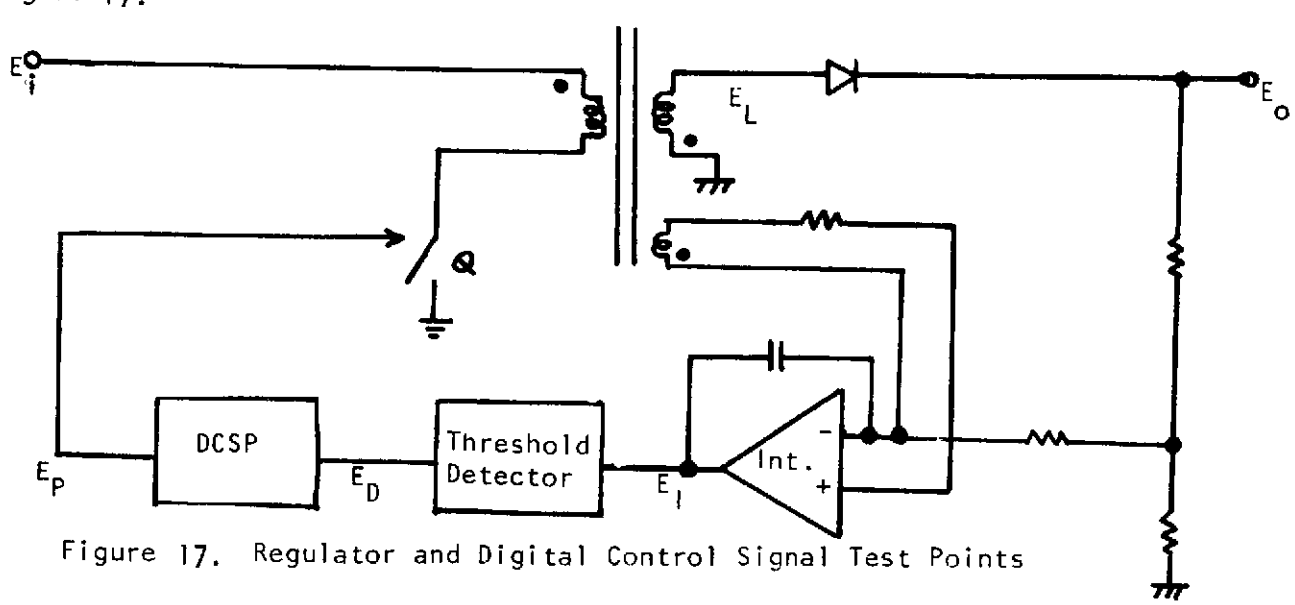


Figure 17. Regulator and Digital Control Signal Test Points

10. CONVERTER STEADY-STATE PERFORMANCE

Typical steady-state performance data taken on the three types of converter brassboards over the line, load, and temperature ranges are summarized in Tables 8, 9, and 10. These tables demonstrate that the converter capabilities either meet or exceed the specification requirements. Unless otherwise specified, all test data were taken based on the following specified input voltage, output load, and temperature ranges:

Converter	Input Range (V)	Load Range (W)	Temp Range (°C)
Buck-boost converter	20 to 40	4.2 to 42 (28V)	-25 to 85
Pulse modulated parallel-inverter converter	24 to 40	30 to 40 (1kV) 3.75 to 7.5 (15V) 3.75 to 7.5 (-15V) 2.5 to 5 (+5V)	-25 to 85
Series switching buck-regulator converter	24 to 40	4.0 to 40 (28V)	-25 to 85

Table 8. STEADY-STATE PERFORMANCE DATA FOR BUCK-BOOST CONVERTER

Temp. (°C)	E_i (V)	(I_{in})DC (A)	(ΔI_{in})p-p ripple (mA)	I_o (A)	E_o (V)	(ΔE_o)p-p ripple (mV)	Switching Freq. (kHz)	Maximum Output Current Deviation from Regulator Setting (mA)
+25	20	2.291	12	1.473	28.029	210	27.8	5.5
		0.293	12	0.150	28.028	65	16.1	2.5
	30	1.517	14	1.473	28.029	165	27.8	--
		0.197	25	0.150	28.028	65	10.6	--
	40	1.137	7	1.473	28.029	160	27.8	3.5
		0.149	23	0.150	28.029	75	8.8	2.0
+85	20	2.336	20	1.472	28.022	210	25.6	16.5
		0.295	20	0.150	28.022	70	12.5	5.0
	30	1.534	18	1.472	28.022	180	25.6	--
		0.198	35	0.150	28.022	90	8.7	--
	40	1.151	13	1.472	28.022	170	25.6	8.0
		0.151	40	0.150	28.022	90	7.3	3.5
-25	20	2.284	10	1.471	28.030	240	30.0	5
		0.296	20	0.150	28.029	60	16.6	4
	30	1.513	8	1.471	28.029	200	30.0	--
		0.199	25	0.150	28.029	75	12.5	--
	40	1.139	5	1.471	28.029	190	30.0	3.5
		0.151	35	0.150	28.029	80	10.0	5

Table 9. STEADY-STATE PERFORMANCE DATA FOR SERIES-SWITCHING BUCK REGULATOR

Temp (ic)	E_i (V)	(I_{in}) DC (A)	(ΔI_{in}) Peak Ripple (mA)	I_0 (A)	E_0 (V)	(ΔE_0) P-P Ripple (mV)	Switching Frequency (kHz)	Maximum Output-Current Deviation from Regulator Setting
+25	24	1.758	3.0	1.987	20.021	30	33	1
		0.202	2.0	0.199	20.022	25	31	3
	32	1.341	6.0	1.987	20.021	60	31	--
		0.161	6.0	0.199	20.022	70	19	--
	40	1.079	6.5	1.988	20.021	80	31	1.5
		0.132	13.0	0.199	20.022	100	14	3
+85	24	1.769	2.0	1.987	20.014	30	32	3
		0.204	1.0	0.199	20.015	25	32	4.5
	32	1.349	6.0	1.987	20.014	60	30	--
		0.164	6.0	0.199	20.015	75	17	--
	40	1.094	7.0	1.987	20.014	80	30	1.5
		0.135	6.5	0.199	20.014	100	13	4.5
-25	24	1.748	3.0	1.986	20.017	40	33	2
		0.200	1.0	0.201	20.017	30	28	3.5
	32	1.331	5.0	1.986	20.017	65	33	--
		0.160	3.0	0.201	20.017	80	22	--
	40	1.076	5.0	1.986	20.017	90	34	2
		0.133	8.0	0.201	20.017	110	16	5

Table 10(A). STEADY STATE PERFORMANCE DATA FOR PULSE MODULATED PARALLEL-INVERTER CONVERTER (REGULATING 1KV)

Temp. (°C)	E_{in} (V)	(I_{in}) DC (A)	I_{out}				E_{out}				(ΔE_{out}) p-p				Ripple Frequency (kHz)
			1 kV (mA)	+15V (mA)	-15V (mA)	+5V (mA)	1 kV (V)	+15V (V)	-15V (V)	+5V (V)	1 kV (mV)	+15V (mV)	-15V (mV)	+5V (mV)	
25	24	2.998	41.60	511	504	1028	1000.58	15.281	15.270	5.286	700	50	50	30	22.8
		2.046	31.70	256	253	530	1000.26	15.291	15.280	5.342	900	50	50	25	22.4
	32	2.295	41.60	511	506	1034	1000.58	15.366	15.360	5.322	1200	70	70	40	21.2
		1.576	31.70	259	255	525	1000.26	15.455	15.447	5.401	1050	70	70	40	24.4
	40	1.828	41.60	511	508	1029	1000.57	15.276	15.262	5.293	1500	70	70	40	23.8
		1.260	31.70	254	251	526	1000.29	15.194	15.185	5.306	1500	70	70	40	23.8
85	24	3.035	41.60	518	506	1039	1001.11	15.367	15.352	5.353	800	50	50	20	21.6
		2.069	31.80	258	253	538	1001.07	15.374	15.362	5.424	750	50	50	20	23.6
	32	2.319	41.60	515	510	1050	1001.12	15.490	15.481	5.412	1200	65	65	30	22.8
		1.605	31.80	261	258	547	1001.08	15.591	15.571	5.513	1250	65	65	30	24.0
	40	1.871	41.60	516	508	1045	1001.09	15.428	15.413	5.591	1700	75	75	40	22.2
		1.287	31.80	257	254	541	1001.10	15.420	15.416	5.456	1600	75	75	40	22.4
-25	24	2.960	41.50	507	500	1005	999.43	15.158	15.148	5.196	800	50	50	20	23.8
		1.982	30.60	254	251	520	999.59	15.165	15.154	5.256	800	50	50	30	23.6
	32	2.259	41.50	508	500	1008	999.43	15.193	15.186	5.217	1300	70	80	35	23.2
		1.524	30.60	256	251	523	999.58	15.255	15.247	5.291	1300	70	80	35	23.2
	40	1.823	41.50	508	501	1010	999.42	15.200	15.186	5.227	1600	80	80	45	24.8
		1.247	30.60	254	250	520	999.56	15.146	15.134	5.252	1600	80	80	40	24.6

TABLE 10(B). STEADY-STATE PERFORMANCE DATA FOR PULSE MODULATED PARALLEL-INVERTER CONVERTER (REGULATING dØ/dt)

E_i (V)	Temp (°C)	E_o		
		1kV (V)	±15 (V)	+5 (V)
24 to 40V	25°C	989.59 to 1005.13	15.198 to 15.310	5.266 to 5.356
	85°C	977.20 to 989.37	14.993 to 15.202	5.258 to 5.371
	-25°C	998.96 to 1013.75	15.234 to 15.342	5.241 to 5.331

Remarks:

(1) ±15V have identical output voltage

(2) No current data are taken, for efficiency should be identical to the case where 1kV is regulated.

(3) The output-voltage variation represents the worst-case data under the conditions of:

(a) Max. load on all outputs

(b) Min. load on all outputs

10.1 Output Voltage Regulation

The output-voltage regulation data for all three converters are presented, respectively, in Tables 8, 9 and 10.

The regulation at minimum load, of the buck-boost converter and the series switching buck-regulator converter, was measured at open-load and at the specified 10% of full load. While the open-load test data is not shown in Tables 8 and 9, it was recorded in the test report. Insignificant changes were noted when the minimum load is decreased from 10% of full load to open circuit.

The regulation performance data for all three converters over the specified line, load, and temperature changes are summarized in Table 11.

Table 11. SUMMARY OF OUTPUT-VOLTAGE REGULATION

Converters	Outputs (V)	Requirements (%)		Measurements (%)	
Buck-boost	28	±0.2		*± 0.014	
Buck-regulator	20	±0.2		*± 0.020	
		1kV Regulated	dØ/dt Regulated	1kV Regulated	dØ/dt Regulated
Pulse Modulated Parallel-Inverter	1000	±0.2	±2	±0.085	±1.83
	+15	±5	±3	±1.48	±1.11
	-15	±5	±3	±1.47	±1.13
	+5	±8	±6	±3.16	±1.38

* Including no load.

10.2 Efficiency

Converter efficiencies for nominal full-load operation at room temperature are summarized in Table 12.

Table 12. SUMMARY OF CONVERTER EFFICIENCY AT FULL LOAD AND ROOM TEMPERATURE

Converters	Input Voltage (V)	Measurement (%)	Requirement (%)
Buck-Boost	20	90.1	
	30	90.7	90
	40	90.8	
Series Switching Buck-Regulator	24	94.3	
	32	92.7	92
	40	92.2	
Pulse Modulated Parallel-Inverter	24	87.6	
	32	85.3	85
	40	85.6	

10.3 Output Current Regulation

The current-regulator performance of the buck-boost converter and the series-switching buck-regulator converter during overload and short circuit is shown in Tables 8 and 9 as Deviation from Regulator Setting; the regulator setting being adjustable from 10% to 100% of full load. In the case of the parallel-inverter converter, the overload protection causes the converter to turn off when a severe overload or a short curcuit occurs.

The current regulator and limiter performances for all three converters are summarized in Table 13.

Table 13. SUMMARY OF OUTPUT-CURRENT REGULATION

Converters	Outputs (A)	Requirements (%)	Measurement (%)
Buck-Boost	1.5A Max	±5 of full load	±1.23
	0.15A Min	±5 of full load	±0.40
Pulse Modulated Parallel-Inverter	Four outputs	None	Converter turn-off when any of the four outputs is overloaded or short-circuited.
Series Switching Buck-Regulator	2.0A Max	±5	±0.150
	0.2A Min	±5	±0.25

10.4 Output Voltage Ripple

The worst peak-to-peak switching-frequency ripple for each converter is summarized in Table 14.

Table 14. SUMMARY OF OUTPUT-VOLTAGE RIPPLE

Converters	Output (V)	Maximum Ripple Allowed (mV)	Maximum Ripple Measured (mV)	Conditions of Maximum Ripple
Buck-Boost	28V	280	240	Low line, heavy load, and low temperature
Pulse Modulated Parallel-Inverter	1kV	5000	1800	High line, light load, low temperature
	+15V	150	80	
	-15V	150	80	
	+ 5V	50	45	
Series-Switching Buck-Regulator	20V	200	110	High line, light load, low temperature

10.5 Source Current Ripple

The design goal for the conducted interference was MIL-STD-461A (Notice 3).

Over the specified line, load, and temperature range, the switching frequency variation for each converter was:

Buck-Boost:	7.3kHz to 30.0kHz
Series-Switching Buck-Regulator:	12.8kHz to 33.0kHz
Pulse Modulated Parallel-Inverter:	21.6kHz to 24.8kHz

Within these frequency ranges, all data points for the measured source-current ripple were within the limit specified by the design goal.

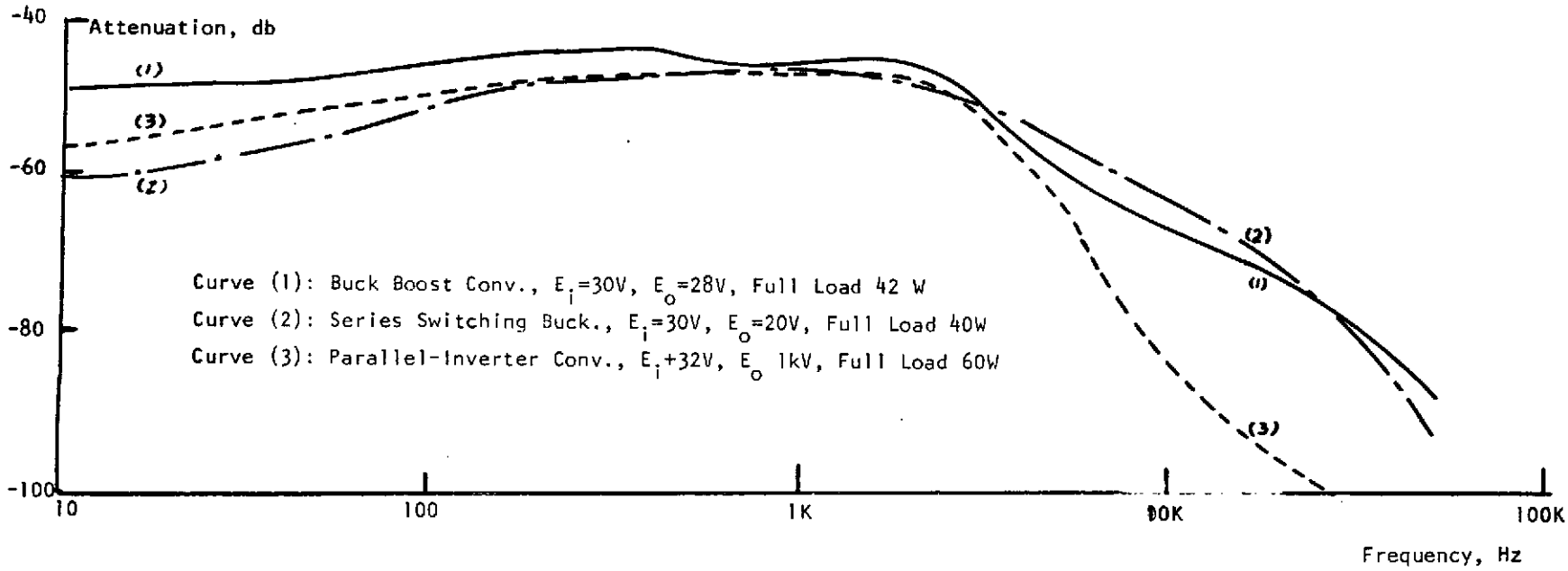
10.6 Audio Susceptibility

A 2.8V rms sinusoidal voltage was superimposed on the nominal DC input to test the converter's capability in rejecting the line disturbance. For each converter, the mean of the specified input voltage was selected as the DC input. The measured line rejection in "db" are shown in Fig.18, for all three converters. The data include both heavy and light load operations at room temperature. Here, the "db" is defined as

$$db = 20 \log_{10} \frac{\dfrac{\text{audio output ac voltage}}{\text{output dc voltage}}}{\dfrac{\text{audio input ac voltage}}{\text{input dc voltage}}}$$

For the buck-boost converter, the significantly different rejection as a function of load is due to the different MMF status in the energy-storage inductor. In heavy-load operations, a trapezoidal current in the inductor windings during on-time T_n and off time T_f never let the inductor MMF to vanish.

The average value of the trapezoidal inductor current must decrease (increase) as the line input is increased (decreased), requiring the inductor to adjust its average stored energy continuously during the audio test. In contrast, a triangular inductor current in light-load operations has a time interval of zero MMF within each steady-state cycle. This time interval makes it possible for the inductor to achieve equilibrium between its energy storage and energy discharge (i.e., a zero net incremental energy) within one cycle of converter switching despite the much slower input-voltage variation at the audio frequency. In the case of a trapezoidal current where such an interval is non-existant, the inductor energy balance can only be achieved through a cyclic migration of the minor BH loop, which can



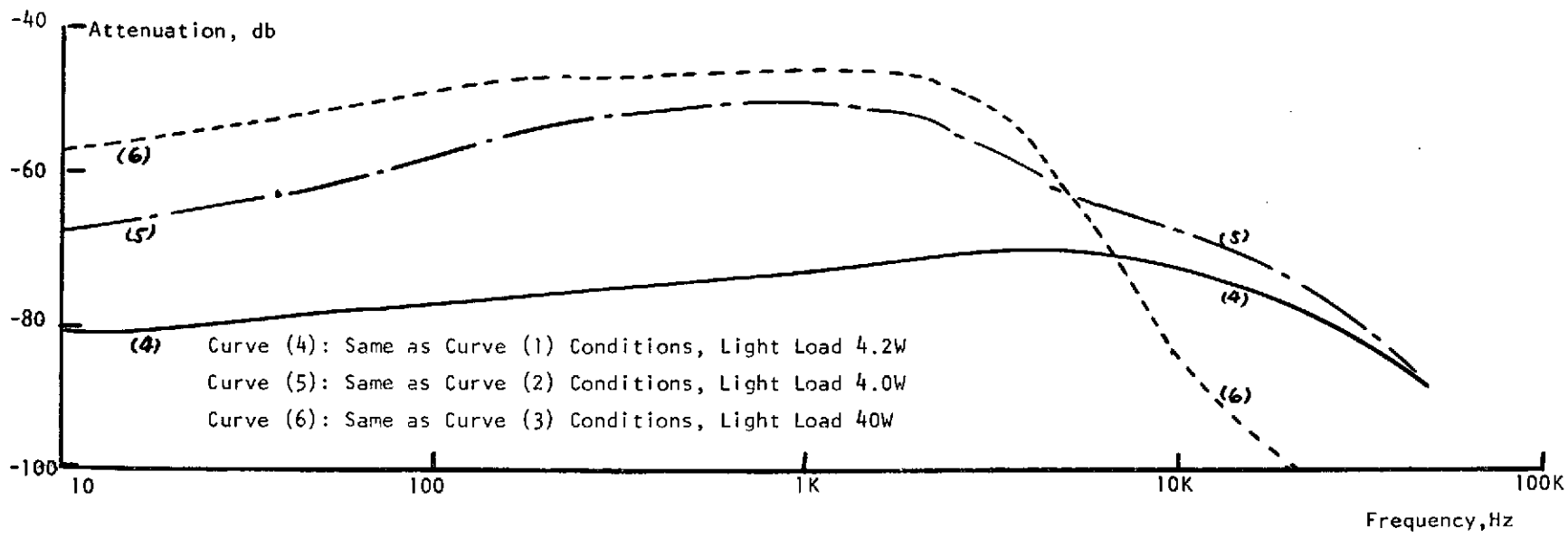


Figure 18. Measured Audio-Susceptibility Performance

proceed only at a limited rate dictated by the output filter and other compensation networks used in the control system.

For the series switching buck-regulator converter and the pulse modulated parallel-inverter converter, the rejection performances demonstrate little differences with respect to the loading, and are generally superior to the buck-boost converter at full load (i.e., trapezoidal inductor current). This is easily explained by the fact that for either of these two converters, the average of the trapezoidal current is also the output load current. Inasmuch as the load resistance is kept constant during the audio test, and that the output voltage remains closely regulated, the average of the trapezoidal current is essentially unchanged. Consequently, little is required for the inductor to establish an energy equilibrium during the audio test.

It is for these reasons that rejection performances of the series-switching buck-regulator converter and the pulse modulated parallel converter are better than that of the buck-boost converter with each converter operating under trapezoidal inductor current. Furthermore, the difference between line-rejection at full load and at light load (i.e., trapezoidal vs. triangular inductor current) is relatively insignificant for the series-switching buck-regulator converter and the pulse modulated parallel-inverter converter as compared to the buck-boost converter.

The converter output was monitored throughout the audio-susceptibility test. The corresponding audio signal at the converter output, plus its regular switching-frequency ripple, was within the respective peak ripple specification for each converter.

10.7 Output Impedence

In the interest of defining regulation performance with dynamic loads, the output impedance was measured for the buck-boost converter and the series-switching buck-regulator, each providing a single regulated output. The measured data are plotted in Figure 19. Notice the absence of any sharp peak in the impedance curve, which signifies a well-damped transient following either a step or a sinusoidal load change.

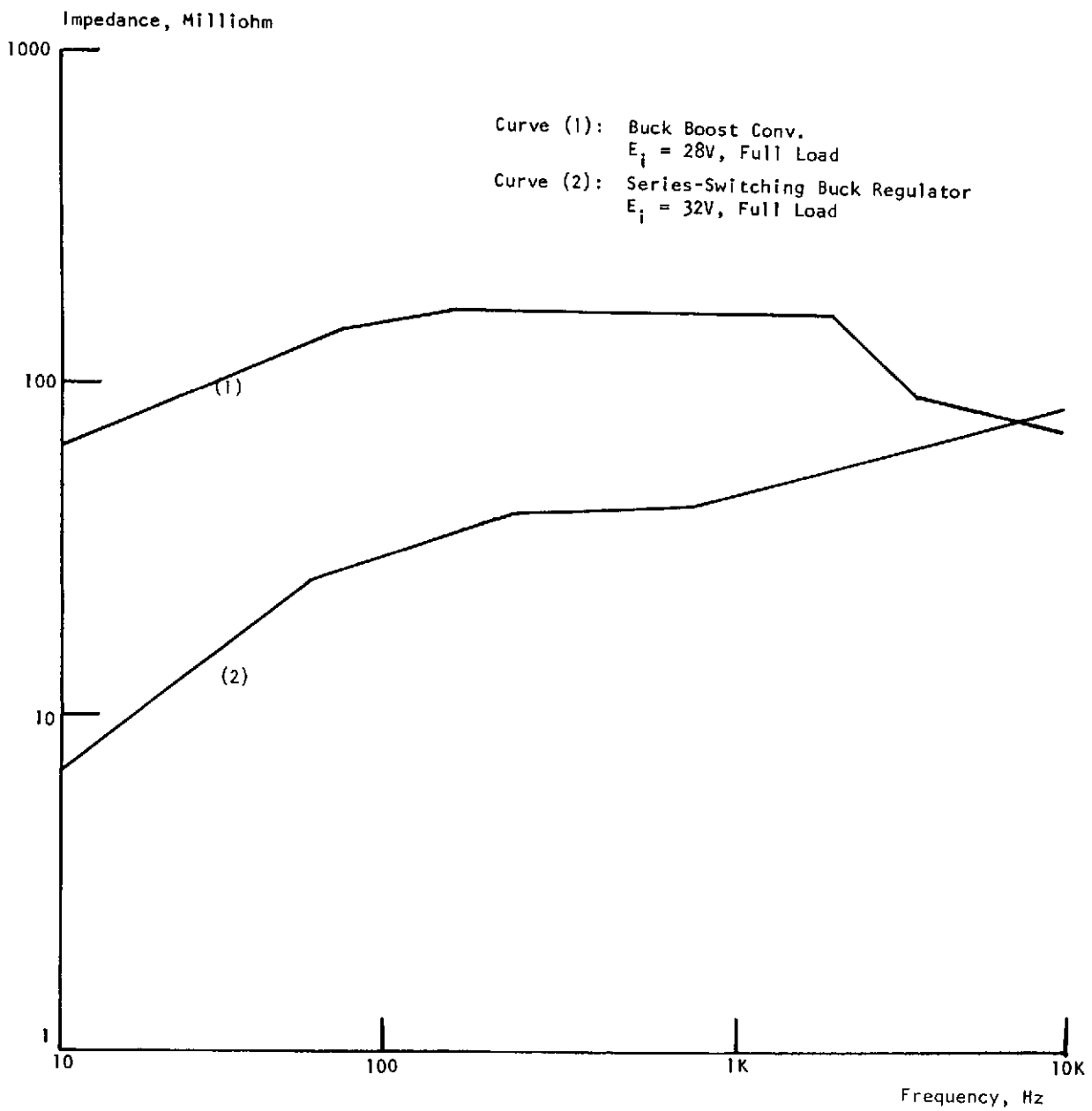


Figure 19. Measured Output Impedance

10.8 Input/Output Isolation

The dc isolation impedance is measured (1) between the input ground and the output ground for the buck-boost converter, (2) between the input ground and each output ground for the pulse modulated parallel-inverter converter and (3) among the four output grounds of the parallel-inverter converter. In each case, the isolation impedance is found to be an order of magnitude higher than the specified 10 mega ohms.

10.9 Summary of Comparison Between Performance and Requirements

A summary of requirements compared with capabilities for each converter is provided in Tables 15(A) and 15 (B). These data show that the converter performances meet or exceed all specification requirements. Certain aspects of the steady-state performances were analyzed to substantiate the measurement data. The analyses were documented in the Brassboard Construction Plan [6].

10.10 Discussion of Results

10.10.1 Output Voltage Regulation

The excellent output-voltage regulation presented in Section 10.2 is due to the high dc gain (in the order of 100db) analyzed in Appendix A. The output-voltage variation was caused primarily by temperature change, which affected the reference zener voltage and the voltage-divider resistors. Better temperature-stabilized networks for these components have been developed [3].

10.10.2 Efficiency

The efficiency goal was met by (1) carefully optimizing the loss in each functional block and (2) using the energy-recovery network. A breakdown of converter losses was calculated for each converter in the Brassboard Construction Plan [6]; measurements verify these calculations.

10.10.3 Output Current Regulation

Good regulation presented in Section 10.4 is again due to the high dc gain analyzed in Appendix A. The current variation was primarily due to the error produced in the current-sensing magnetics.

Table 15(A) REQUIREMENTS VERSUS CAPABILITIES OF PROTOTYPE CONVERTERS

Performances	Buck-Boost Converter		Parallel-Inverter Converter		Switching Buck-Regulator	
	Requirement	Capability	Requirement	Capability	Requirement	Capability
Input Voltage Range	20 to 40V	20 to 40V	24 to 40V	24 to 40V	24 to 40V	24 to 40V
Audio Susceptibility	2.8V rms	Output within ripple spec.	2.8V rms	Output within ripple spec.	2.8V rms	Output within ripple spec.
Source Current Ripple	MIL-STD-461 Notice 3, As a design goal	MIL-STD-461 Notice 3 Met	MIL-STD-461 Notice 3, As a design goal	MIL-STD-461 Notice 3 Met	MIL-STD-461 Notice 3, As a design goal	MIL-STD-461 Notice 3 Met
Reverse Input Protection	Yes	Yes	Yes	Yes	Yes	Yes
Isolation	Yes	Yes	Yes	Yes	No	No
Power Transformer Saturation	--	No Saturation	No Saturation	No Saturation	--	No Saturation
Temperature Range	-25 to 85°C	-25 to 85°C	-25 to 85°C	-25 to 85°C	-25 to 85°C	-25 to 85°C
Voltage Regulation	±0.2%	±0.015%	See Table 15(B)	See Table 15(B)	±0.2%	±0.02%
Efficiency	90%	90.7%	85%	85.3%	92%	92.7%
P-P Output-Voltage Ripple	1%	0.85%	See Table 15(B)	See Table 15(B)	1%	0.55%
Current Regulation	±5%	±1.23%	None	O.L. Protection Provided	±5%	±0.25%
Brassboard Weight	1kg	0.862kg	0.75kg	0.683kg	2kg	1.629kg
Load Range	0.15 to 1.5A	Open to 1.5A	See Table 15(B)	See Table 15(B)	0.2 to 2A	Open to 2A

Table 15(B) REQUIREMENTS VERSUS CAPABILITIES OF PULSE MODULATED PARALLEL-INVERTER CONVERTER

Outputs (Volt)	Peak-Peak Ripple(%)		* Load Range (mA)		Regulation (%)			
					Sensing 1kV		Sensing dØ/dt	
	Requirement	Capability	Requirement	Capability	Requirement	Capability	Requirement	Capability
1000	0.5	0.18	30 to 40	30 to 40	± 0.2	± 0.085	± 2	± 1.83
+15	1	0.6	250 to 500	250 to 500	± 5	± 1.48	± 3	± 1.11
-15	1	0.6	250 to 500	250 to 500	± 5	± 1.47	± 3	± 1.13
+ 5	1	0.9	500 to 1000	500 to 1000	± 8	± 3.16	± 6	± 1.38

* All loads can be opened without causing any component failure.

10.10.4 Output Voltage Ripple

The specified output-voltage ripple was met by properly-designed power and control circuits. Analysis substantiating the design was presented in reference [6].

10.10.5 Source Current Ripple

The two-stage filter used in this program allows the source-current ripple to be met without appreciable efficiency loss. Computer programs confirming the satisfactory filter attenuation performance were given in reference [6]. See Appendix D for design detail.

10.10.6 Audio-Susceptibility

As presented in Appendix A, the high loop gain provides good audio-susceptibility performance from dc to beyond the resonance frequency of the output filter. At higher frequencies, the audio input is attenuated by the passive filter.

10.10.7 Output Impedance

Low output impedance is made possible by the high gain and large bandwidth of the ASDTIC control, as well as the output-filter design with low characteristic impedance $[(L_o/C_o)^{1/2}]$.

10.10.8 Input/Output Isolation

For the buck-boost converter and the parallel-inverter converter, the impedance between the input and the output is essentially the isilation impedance of the optical coupler. This impedance is at least an order of magnitude higher than the ten megohms specified.

11. CONVERTER TRANSIENT PERFORMANCE

The transient response of a converter is important with regard to the following power system performances:

(1) During severe line and load transients, the electrical stresses on all power-handling components of the converter must be controlled to within their safe operating limits. If this control is not established, the converter reliability assessment based on the statistical failure rate of individual components is of limited real value.

(2) Spacecraft instrumentation and equipment loads often require a power quality which stays within a given specification during not only steady-state, but also during transient line and load conditions.

(3) During a severe transient such as converter startup by command, the converter should not demand a current higher than the capability of the current-limited primary source. This is necessary in order to avoid a system shutdown due to a collapse of the source voltage.

In relation to these desirable characteristics, oscillograms of waveforms were taken on all three converters under conceivable large-signal line and load changes. The waveforms included the output voltage, the power-switching current, and the source current. The following types of transients were investigated:

- Converter startup by command, with output at full load
- Converter startup by command, with output shorted
- Converter startup by step application of input voltage
- Sudden converter output short
- Recovery from an output short
- Step change between the specified minimum and maximum operating input voltage
- Step change between the specified minimum and maximum load.

These oscillograms are shown in Figures 20 to 26, from which the following transient performances can be established:

(1) The stress level of the power switch (and of all power components) during any line and load transients was limited to within 200% of the nominal steady-state value. The control was made possible through the design of the previously-described peak-current sensor and Digital Control Signal Processor - DCSP.

(2) The design goal of meeting the steady-state 1% ripple specification during transient was met for most dynamic operations. Furthermore, all transients were critically damped, indicating good dynamic stability. During starting, there was no output-voltage overshoot.

(3) The source current was always under control during large dynamic changes of line and load including sudden output short circuit. The control was enabled by the joint function of the peak-current sensor, the DCSP, and the ASDTIC current regulator.

There are three traces in each oscillogram. From top to bottom, they are the source current, the output voltage, and the power-switch current, respectively.

Many interesting observations can be made on the oscillograms from Figures 20 to 26. A complete identification on the nature of each wave-waveform in its minute detail is not the primary objective here. However, the following points of importance are noted for the respective figures:

<u>Figure 20: Transients During Converter Command On</u>

- There is no output-voltage overshoot during turn-on.
- Initially, the peak-current sensor is limiting the power-switch current. The current regulator becomes active subsequently, which then controls the source current until voltage regulation is reached at the converter output.

Figure 21. Transients During Converter Command On With Output Shorted

- The zero output voltage reflects the short circuit at the converter output.
- For the parallel-inverter converter, the 1kV output is shorted. The time rate of 0.1 ms/Division does not show the automatic turn-off of the converter follwoing 20 milliseconds of switching. The turn-off is caused by the overload protection circuit described in page 121.

Figure 22. Transients During Converter Turn-On By a Step Input Voltage

- The large initial source current is the charging current of the input filter.
- Had there not been the damping resistor R1 shown in the filter on page 105, the inrush current into the input-filter capacitors would be significantly higher.

Figure 23. Transients During Sudden Converter Short Circuit

- The turn-off of the parallel inverter 20 milliseconds into the occurrence of the short circuit is evident.
- Of particular significance is the utility of the buck-boost converter in handling a load where frequent short circuits are expected. It can be seen from the top oscillogram that the source current never exceeds its maximum steady-state value, which is 2.3 Amperes for a 20-Volt input voltage.
- The source current for the parallel-inverter converter also shows excellent performance. This is due to the joint effort of the peak current sensor and the DCSP, which effects a much shorter on time and a lower frequency operation when the output is shorted. As a result, the average source current actually decreases slightly subsequent to the short-circuit event.

Figure 24. Transients During Removal of an Output Short

- The oscillograms bear resemblance to Figure 20. The only difference is the absence of any initial high peak current in either the power switch or the source when the short circuit is removed and the converter output voltage starts to build up. This is caused by the current regulator, which is already in effect due to the short circuit prior to the recovery. This was not the case during the converter "command on" in Figure 20, in which the current regulator is effective only after the initial peak-current transient has subsided.

Figure 25. Transients During Step Input Voltage Change

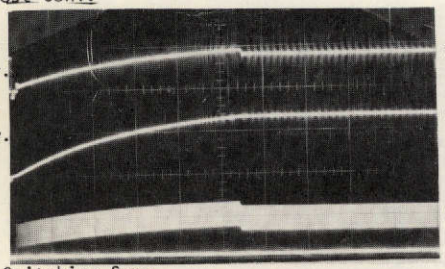
- The output-voltage excursion for the three converters are, from the top, 140 mV, 60 mV, and 4000 mV, respectively. Corresponding to the regulated output voltage of 28V, 20V, and 1000V, the excursions are within the 1%, 1%, and 0.5% ripple specification of the three converters.
- No disorderly current can be observed during the input-voltage transition.

Figure 26. Transients During Step Load Change

- For the first two oscillograms, the transition of power-switch current between triangular waveform at light load to trapezoidal waveform at heavy load is evident.
- The absence of any prolonged oscillation is in good agreement with the prediction derived from the output-impedance measurement shown in page 62.

(A) Buck Boost Conv.

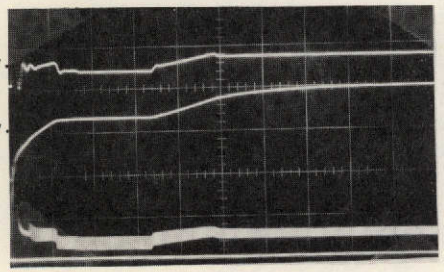
2A/Div.
20V/Div.
4A/Div.
5ms/Div.



Source Current
Output Voltage
Collector Current

(B) Series Switching Conv.

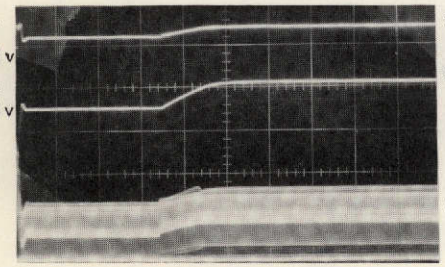
2A/Div.
10V/Div.
4A/Div.
4ms/Div.



Source Current
Output Voltage
Collector Current

(C) Parallel Inverter Conv.

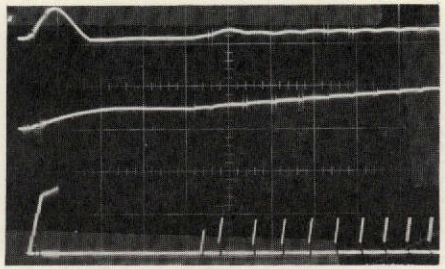
5A/Div.
500V/Div
4A/Div.
10ms/Div



Source Current
Output Voltage
Collector Current

(D) Buck Boost Conv.

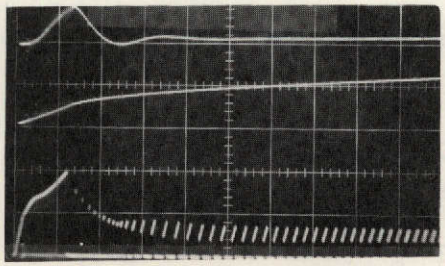
2A/Div.
5V/Div.
4A/Div.
0.2ms/Div.



Source Current
Output Voltage
Collector Current

(E) Series Switching Conv.

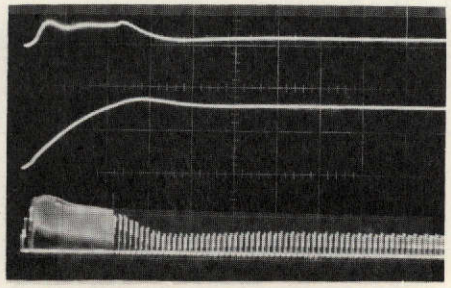
5A/Div.
10V/Div.
4A/Div.
0.2ms/Div.



Source Current
Output Voltage
Collector Current

(F) Parallel-Inverter Conv.

5A/Div.
500V/Div.
10A/Div.
0.5ms/Div.



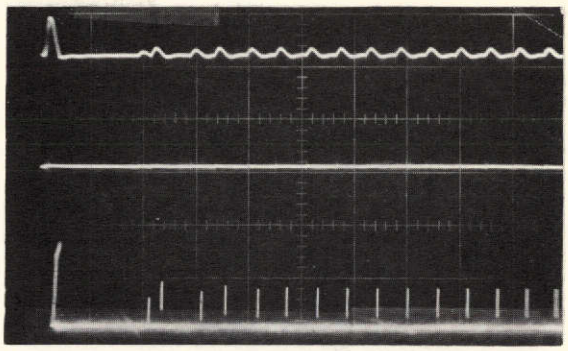
Source Current
Output Voltage
Collector Current

CONVERTER OUTPUT: FULL LOAD

Figure 20. Transients During Converter Command On. Figures (D),(E), and (F) Are Expanded Views of Figures (A),(B), and (C), Respectively.

(A) Buck Boost Conv.

2A/Div.
5V/Div.
4A/Div.
1ms/Div.



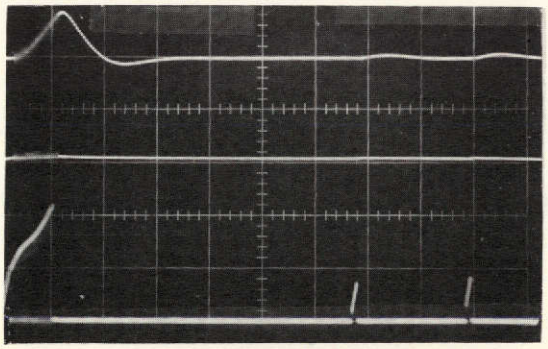
Source Current

Output Voltage

Collector Current

(B) Series Switching Conv

5A/Div.
10V/Div.
4A/Div.
0.5ms/Div.



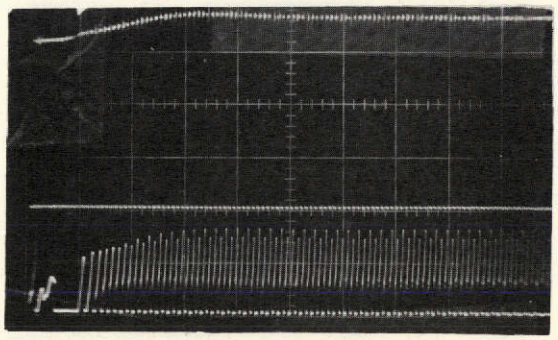
Source Current

Output Voltage

Collector Current

(C) Parallel-Inverter Conv.

5A/Div.
500V/Div.
10A/Div.
0.1ms/Div.



Source Current

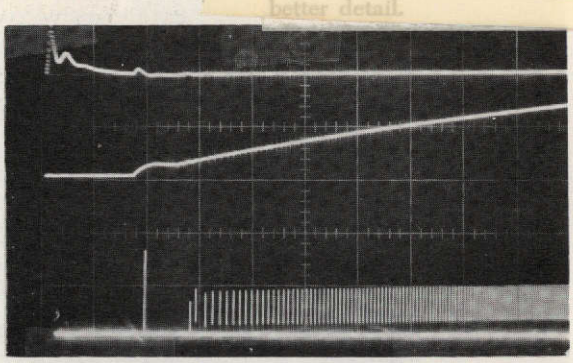
Output Voltage

Collector Current

Figure 21. Transients During Converter Command On, with the Output Load Short Circuited

(A) Buck Boost Conv.

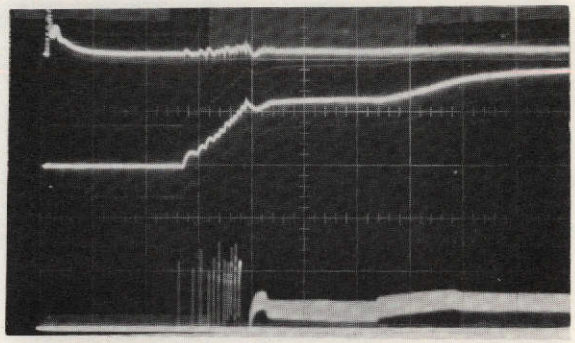
10A/Div.
10V/Div.
4A/Div.
1ms/Div.



Source Current
Output Voltage
Collector Current

(B) Series Switch Conv.

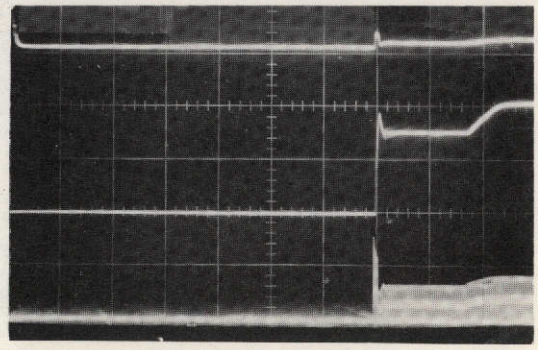
10A/Div.
10V/Div.
4A/Div.
2ms/Div.



Source Current
Output Voltage
Collector Current

(C) Parallel-Inverter Conv.

10A/Div.
500V/Div.
10A/Div.
20ms/Div.

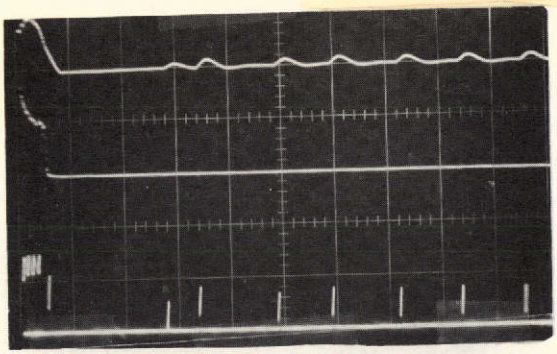


Source Current
Output Voltage
Collector Current

Figure 22. Transients During Converter Turn-on by a Step Application of Input Voltage from 0 to 40V with Output at Full Load

(A) Buck Boost Conv.

2A/Div.
10V/Div.
4A/Div.
0.5ms/Div.



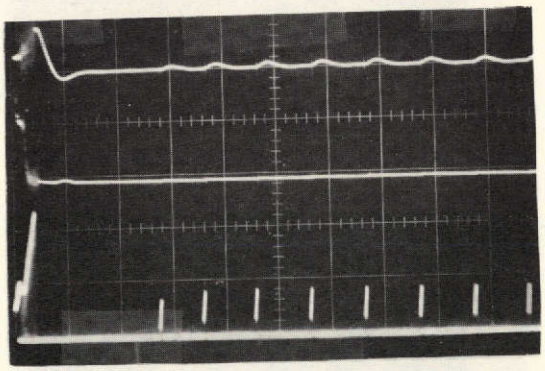
Source Current

Output Voltage

Collector Current

(B) Series Switching Conv.

5A/Div.
10V/Div.
4A/Div.
0.2ms/Div.



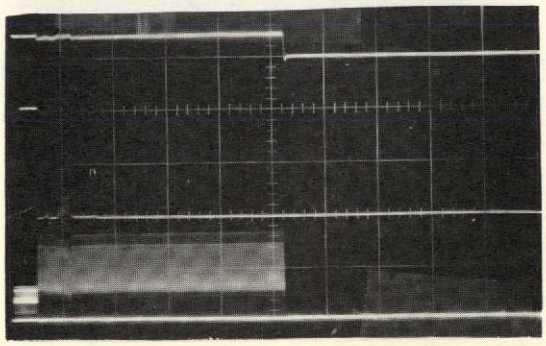
Source Current

Output Voltage

Collector Current

(C) Parallel-Inverter Conv.

5A/Div.
500V/Div.
10A/Div.
5ms/Div.



Source Current

Output Voltage

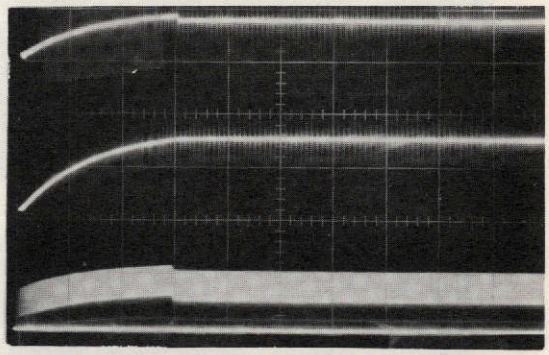
Collector Current

The sudden interruption of collector current in the parallel-inverter converter is caused by the overload turn-off protection circuit.

Figure 23. Transients During Sudden Converter Output Short Circuit

(A) Buck Boost Conv.

2A/Div.
20V/Div.
4A/Div.
10ms/Div.



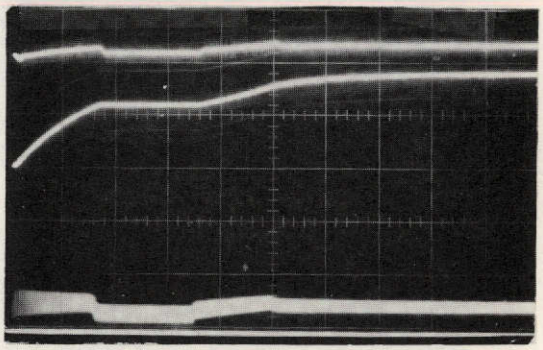
Source Current

Output Voltage

Collector Current

(B) Series Switching Conv.

5A/Div.
10V/Div.
4A/Div.
2ms/Div.



Source Current
Output Voltage

Collector Current

(C) Parallel Inverter Conv.

Due to the fact that subsequent to an output short circuit the overload trip designed for this converter will turn off the converter completely, no recovery from a shorted load can be observed.

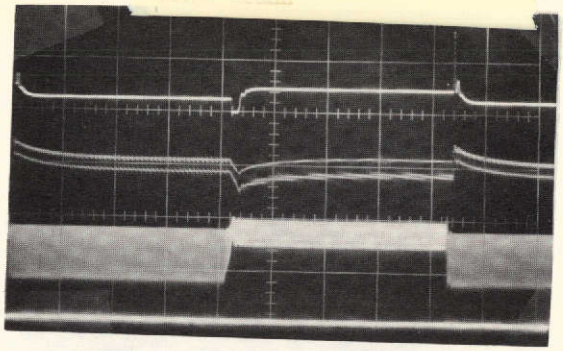
Figure 24. Transients During Recovery from the Removal of an Output Short

(A) Buck Boost Conv.

5A/Div.
.5V/Div.
2A/Div.
5ms/Div.

E_i = Between 20V and 40V

P_o = Full Load, 42W



Source Current

Output Voltage

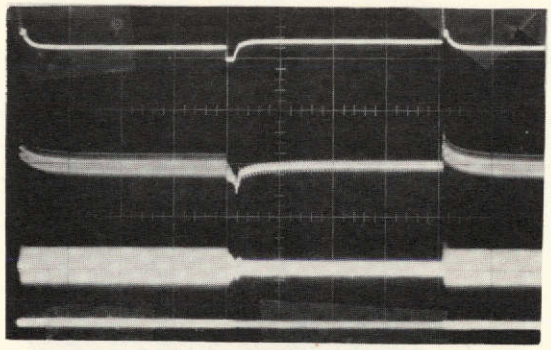
Collector Current

(B) Series Switching Conv.

5A/Div.
0.1V/Div.
2A/Div.
5ms/Div.

E_i = Between 24V and 40V

P_o = Full Load, 40W



Source Current

Output Voltage

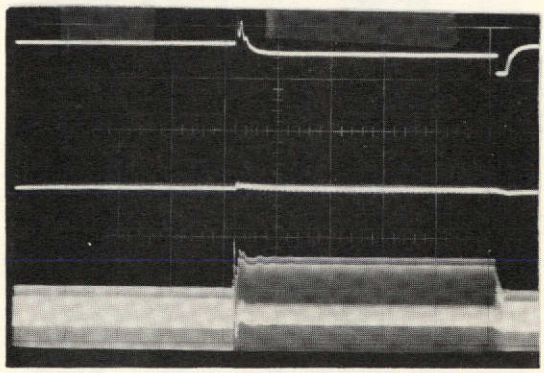
Collector Current

(C) Parallel-Inverter Conv.

5A/Div.
50V/Div.
4A/Div.
5ms/Div.

E_i = Between 24V and 40V

P_o = Full Load, 60W



Source Current

Output Voltage

Collector Current

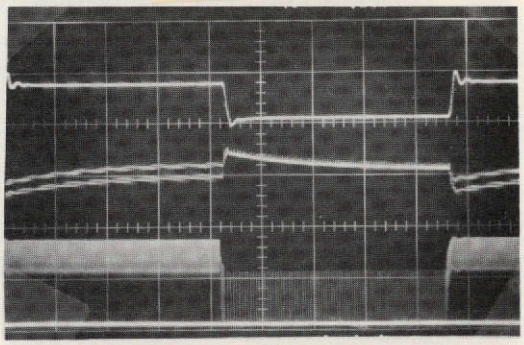
Figure 25. Transients During Step Input Voltage Change

(A) Buck Boost Conv.

2A/Div.
.5V/Div.
2A/Div
2ms/Div.

E_i = 32V

I_o = Between 0.15A and 1.5A



Source Current

Output Voltage

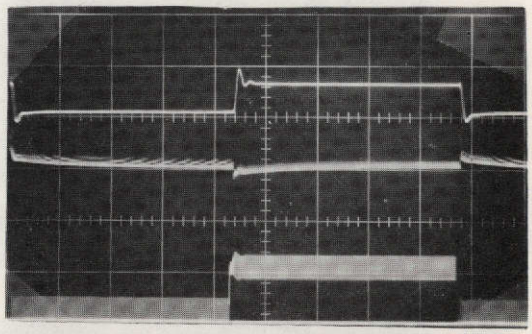
Collector Current

(B) Series Switching Conv.

2A/Div.
.5V/Div.
2A/Div.
2ms/Div.

E_i = 32V

I_o = Between 0.2A and 2A



Source Current

Output Voltage

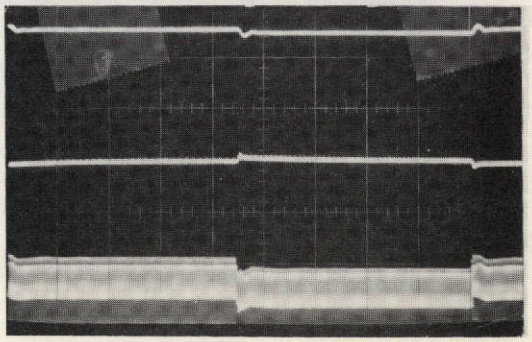
Collector Current

(C) Parallel-Inverter Conv.

5A/Div.
50V/Div.
4A/Div.
2ms/Div.

E_i = 32V

I_o = Between 30mA and 40mA for the 1000V output



Source Current

Output Voltage

Collector Current

Figure 26. Transients During Step Load Change

12. RECOMMENDATIONS FOR FUTURE WORK

Future work needed on the ASDTIC control system can be categorized into two areas: (1) Application, and (2) Analysis.

12.1 Application

(1) Fabrication of Integrated and Microminiaturized Control Circuits

The present ASDTIC program has demonstrated: (A) the versatility of the ASDTIC control concept and (B) the commonality of control-circuit modules among different types of converters. These accomplishments have greatly facilitated the future integration of the entire control circuit into either a single control module or several control modules using microminiaturization techniques. Such an integration would enhance the standardization and cost reduction of power processing equipment.

(2) Application of ASDTIC for High Power Converters Containing Multiple Power Modules.

The need for higher converter power rating in space applications has been growing, and will exceed the capability of the available high-frequency switching transistors. Consequently, it is expected that future converters involving high power (multi-kilowatt or higher) will utilize series and parallel multiple power modules. The application of ASDTIC, so far, has been limited to the control of a signal power module. The extension of ASDTIC control to multiple power modules is needed in order to enhance the technical readiness and the standardization of future high-power processing equipment.

(3) ASDTIC Applications Other than Power Processing

By the very nature of the analog signal to digital time interval conversion, ASDTIC could be utilized in all applications where the on/off ratio of a switch is controlled as a means to achieve a desired performance. The motor speed control, in which the motor acts as a higher-order filter, is but an example of possible ASDTIC applications.

12.2 Analysis

Power processing for space applications has, from necessity, been a rapidly evolving technology. The effort associated with nondissipative-converter analyses has been unable to keep pace with the degree of sophistication already achieved in the circuit development. However, with the capability of ASDTIC control now established, and with many applications anticipated in the future, it is desirable to pursue at this time, an analytical program to achieve a comprehensive quantitative understanding of ASDTIC control for different power converters using a variety of duty-cycle modulation techniques. The analysis should include small and large-signal stability performance, audio-susceptibility rejection, output impedance, static and dynamic regulation, and the interaction between the negative impedance of the regulator and the input filter to the converter. Specifically, the analytical results from this program would provide the following utilities:

(1) To lend theoretical support to the existing high-performance dc to dc converter ASDTIC control system development.

(2) To identify the optimum control system and duty cycle control mode for the most commonly used dc to dc converter and other critical power processing equipment.

13. CONCLUSIONS

The Analog Signal to Discrete Time Interval Converter (ASDTIC), conceived originally within NASA, and reduced subsequently into miniaturized hybrid form, was utilized successfully as the controlling element for the three most commonly used dc to dc converter/switching regulators: the series-switching buck-regulator converter, the buck-boost converter, and the pulse-modulated parallel-inverter converter. The design was guided by the objectives of promoting performance and reliability improvements, and to achieve control circuit standardization.

To achieve these objectives, a systematic design of both power and control electronics was performed, which has led to major achievements in power-circuit reliability and technology improvement, control-circuit standardization, and superior converter performances. [32]

13.1 Power Circuit Technology Improvement

Power circuit technology improvements include the following features:

(1) Peak-current limiting was provided for each converter to gain control of all power component stresses during steady-state and dynamic operations, thus enhancing greatly the reliability of each converter. Furthermore, the interaction between the converter and the primary power source is brought under control.

(2) Energy-recovery networks were used to prevent the simultaneous occurrence of high voltage and high current in the power transistors and to recover the energy stored in the transformer leakage inductance, thus eliminating transistor secondary breakdown and reducing switching losses.

(3) Optimum weight and efficiency were achieved through (A) the design of magnetic components based on a set of minimum weight equations, (B) elimination, through active means, of high current spikes due to saturation of the parallel-inverter converter power transformer, and (C) the use of a proportional current drive, energy recovery network, and a two-stage input filter.

13.2 Control Circuit Standardization

The control circuit standardization includes:

(1) Adoption of the ASDTIC microminiaturized control module to the three dc to dc converters led to uniformly outstanding static and dynamic regulation as well as control loop stability.

(2) Commonality was also attained in the control loop interface circuits of the three converters. This was achieved through a novel Digital Control Signal Processor (DCSP) design, adaptable to all dc to dc converters.
Utilizing a total of only seven parts, the DCSP processes all control requirements including (A) interface with ASDTIC voltage and current regulators, (B) provision of duty-cycle control with either a constant on-time, a constant off-time, a line-dependent variable on-time, or a constant frequency, (C) processing of the peak current protection for the power switch, (D) response to on/off command and enforcing an orderly converter startup, and (E) synchronization to an external clock frequency, if needed.

(3) To facilitate standardization, control circuit submodules were divided in accordance with their respective control and protection functions to enhance maintainability, interchangeability, and subsystem circuit block identification.

13.3 Performances

One breadboard and two brassboard demonstration models were fabricated and tested for each converter. All specified steady-state efficiency, ripple, and regulation requirements were either met or exceeded. Outstanding were precision voltage regulation (within the vicinity of $\pm 0.02\%$ over a two-to-one input line change, open to full load output change, and a temperature range of -25°C to + 85°C). The good transient performances as reflected in the oscillograms presented in this report are excellent. The power switch current, the source current, and the output voltage are controlled under all dynamic operations. In fact, the 1% peak voltage ripple

includes not only that of the steady-state, but also the voltage excursion during these non-concurrent dynamic conditions: (1) converter starting, either switch-on or command-on, (2) resuming regulation following the removal of an output short circuit, (3) a step change between minimum and maximum input voltage, (4) a step change between 10% and 100% full load, and (5) a 2.8V rms superimposed on the converter dc input voltage during the audio-susceptibility test.

In summary, the ASDTIC microminiaturized control module and control system were demonstrated to be applicable for controlling the three most commonly used dc to dc converters, with superior static and dynamic performance. New technology was developed and applied to improve reliability and to achieve optimum converter weight and efficiency. Commonality of signal functions for all converters, enabled by the ASDTIC control module and the new Digital Control Signal Processor design, facilitates the standardization of future high-performance dc to dc converter regulation, control, and protection circuits.

APPENDIX A

SMALL SIGNAL ASDTIC OPEN LOOP FREQUENCY RESPONSE

A1. Frequency Response

The ASDTIC two-loop control performs the regulating function through discrete pulses generated by the nonlinearity of pulse width modulation. A precise small-signal analysis encompassing the entire A-to-D-to-A process from dc to switching frequency of the converter would require extensive analytical modeling and simulation technique. Such an effort was, unfortunately, beyond the scope of this application-oriented development program; it was identified as a future task in section 12 of this report.

In an attempt to gain at least some qualitative insight into the ASDTIC control system, an analysis based on a low-frequency linear model was carried out for a series-switching regulator to access the control system's frequency response. The control circuit diagram is shown in Figure 27. Using the symbols designated in this figure, the open-loop frequency response can be shown to be:

$$G(s) = \alpha(s)\,\beta(s)\,\gamma(s) \tag{A1}$$

$$\alpha(s) = \frac{1}{1 + \frac{sR_L}{R_L + R_{dc}}\left[\left(R_{dc} + R_c + \frac{R_{dc}R_c}{R_L}\right)C_o + \frac{L_o}{R_L}\right] + s^2 L_o C_o\left(\frac{R_L + R_c}{R_L + R_{dc}}\right)}, \quad \begin{matrix} R_L >> R_c \\ R_L >> R_{dc} \end{matrix} \tag{A2}$$

$$\beta(s) \cong \frac{\dfrac{gKR_4R_L K_u}{(R_3 + R_4)(R_L + R_{dc})}}{1 + s\dfrac{KC_2R_3R_4}{R_3 + R_4}} \tag{A3}$$

$$\gamma(s) = 1 + s\left(\frac{L_o N R_3}{gR_L R_4} + \frac{R_3 C}{g} + R_c C_o\right) + s^2 L_o C_o \frac{NR_3}{gR_4}\left(1 + \frac{R_4 C R_c}{L_o N}\right) \tag{A4}$$

Here, $\alpha(s)$ is the frequency response of the output filter, B(s) is the integrator-amplifier characteristic, with its time constant denoted in the denominator, and $\gamma(s)$ represents the stabilizing effect provided by loop I in conjunction with loop II.

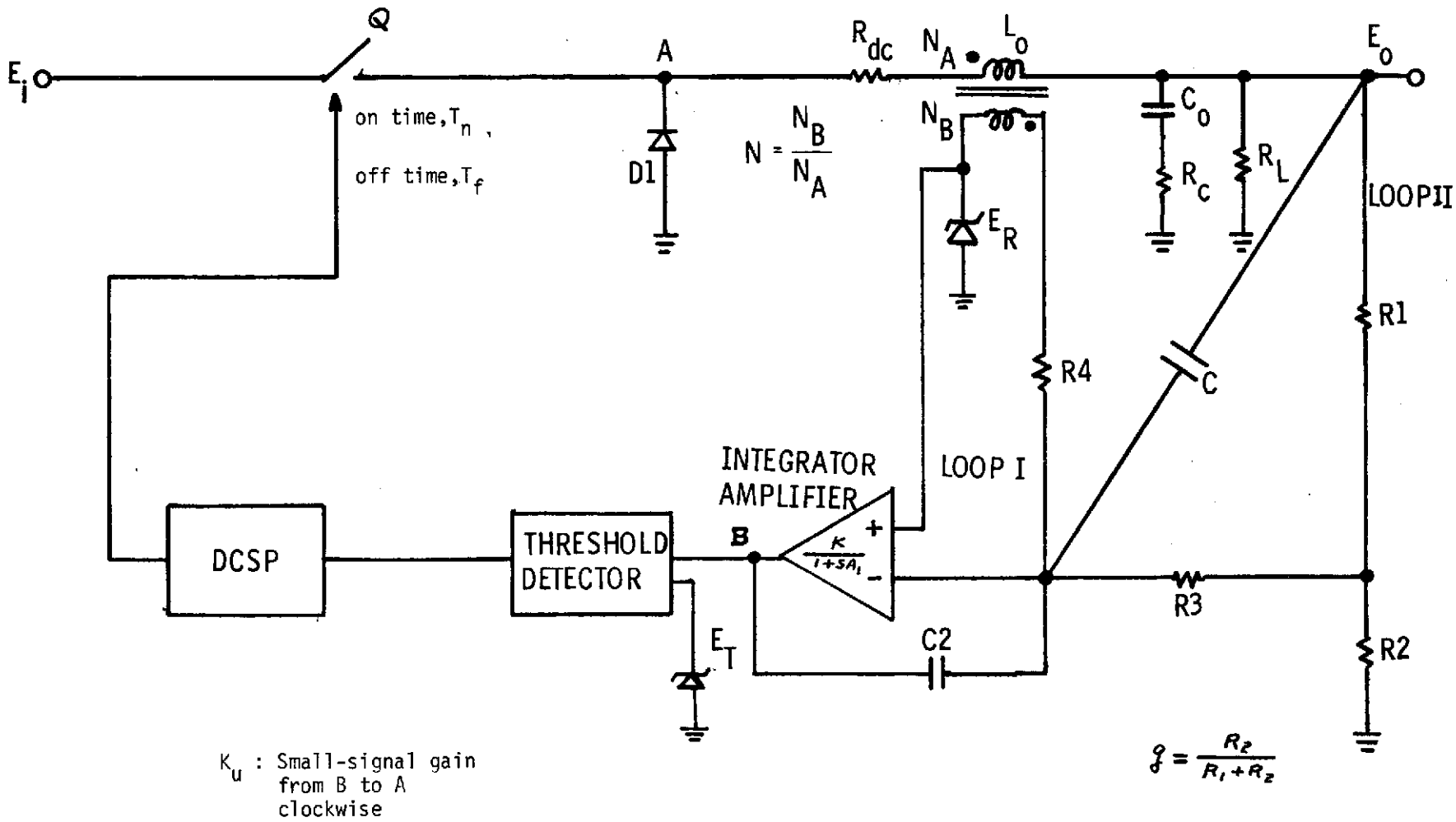


Figure 27. Block Diagram of ASDTIC-Controlled Series-Switching Buck Regulator

This response is sketched in Figure 28.

The five points designated as point "a" to "e" are related to equations (A1) to (A4) as the following:

(A) The amplitude of point "a" is determined by the numerator of equation (A3), the dc gain.

(B) The frequency at point "b" is determined by the denominator of equation (A3), the corner frequency at the integrator amplifier. Between "b" and "c" the gain decreases at -6db/octave.

(C) Point "c" represnets the L_oC_o filter resonance shown in the denominator of equation (A2). Between "c" and "d" the gain decreases at -18db/octave if the damping term (i.e., the "S" term) in the denominator of $\alpha(S)$ is small.

(D) The frequency at point "d" is determined by the S^2 term in equation (A4). Between "d" and "e", the gain decreases at -6db/octave.

(E) Point "e" represents the unity-gain point with a -6db/octave slope.

A2. Discussion of Analytical Results

Several important observations can be made as the following:

(A) The immunity of stability to filter components L_oC_o:
The effect of L_oC_o on the frequency response is reflected by points "c" and "d", based on the S^2 term in the denominator of equation (A2) and in equation (A4). Any change in L_o or C_o tends to move these two points of Figure 28 in the same direction (e.g., points c' and d', thus compensating each other and leaving point "e" unchanged. The stability is, therefore, not affected.

(B) High Gain, Large Bandwidth, and Precision Regulation
The dc gain is represented by the product involving the numerator of equation (A3). Since the open-loop dc gain of the operational amplifier, K, generally exceeds 100db, the converter dc loop gain is extremely high. Furthermore, the second order filter effect is eliminated by the $\gamma(s)$ term of eq. (A4) for frequencies higher than point "d". The extension of the -6db/octave slope from "d" to "e" greatly increases the bandwidth of the converter.

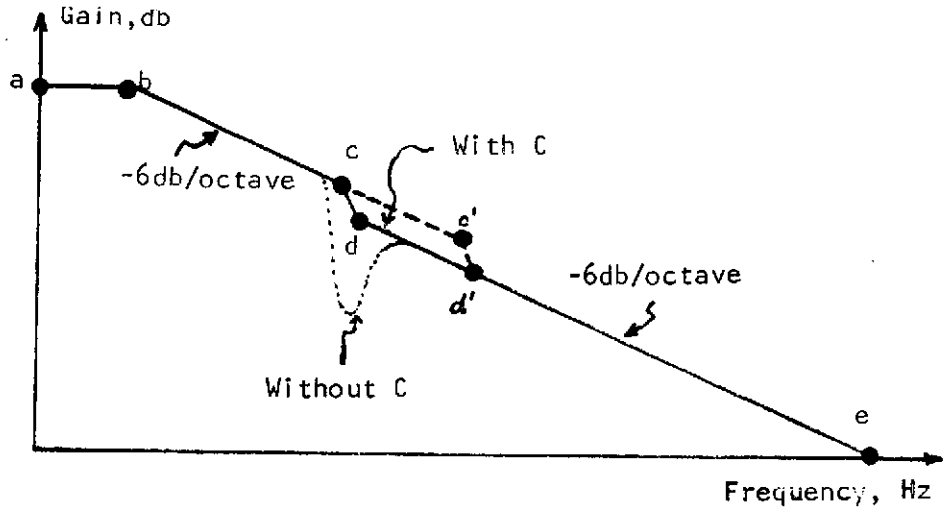


Figure 28. Open-Loop Frequency Response of the ASDTIC Control

(C) Stability of the Two-Loop Control System

From the numerator of equation (A3) the increasing dc gain as a function of R_4 (for a given R_3) becomes evident, which results in better static regulation performance. However, the (R_4/R_3) ratio in the s^2 term of equation (A4) suggests a migration of point "d" toward a higher frequency when (R_4/R_3) is increased, thus creating an extended frequency band between point "c" and "d", within which the roll-off rate is at -18db/octave. The fast roll-off results in a poorer phase margin. Ideally, the (R_4/R_3) ratio should be designed with points "c" and "d" to coincide so as to mitigate this undesirable situation. The -6db/octave slope between "c" and "e" thus maintains converter stability.

(D) The Necessity for Capacitor C in Figure 27

The negative peaking at the frequency corresponding to point "d" increases drastically with a reduction in C. The peaking amplitude is determined by the damping term (i.e., the "s" term) in equation (A4). The addition of capacitor C in Fig.27 serves to increase the damping of $\gamma(s)$. Without C, the deterimental effects associated with the peaking would include: (A) prolonged ringing at a frequency corresponding to "d" subsequent to sudden line and/or load changes, and (B) degraded audio-susceptibility performance within a frequency band centered around point "d". This frequency, F_n, can be expressed as the following:

$$F_n = \frac{1}{2\pi\sqrt{L_o C_o}} \left[\frac{\gamma R_4 R_L}{N R_3 (R_L + R_c)} \right]^{\frac{1}{2}} \qquad (A5)$$

APPENDIX B

MINIMUM-WEIGHT TOROID-CORE INDUCTOR DESIGN EQUATIONS

B1. Introduction

The design of a toroid inductor is normally achieved rather routinely. Based on information concerning the inductance L needed, the peak curent I_p through it, and the saturation flux density B_s of the core material, the designer starts with a core having area A, mean length z, window area A_w, and permeability μ. The number of turns N needed to make inductancd L is then calculated.

At this point two comparisons are made: (1) $\mu N I_p/z = \mu H_p$ is compared to B_s to see if the magnetic capability is fully utilized, and (2) N is multiplied by A_c (i.e., A_c being the sectional area of copper per each turn of conductor as required to handle the winding current with peak value I_p) to see if the window area A_w is sufficient to accomodate the windings, from which the relative value of A_w with respect to $NA_c/F_w = A_x$, where F_w is the estimated winding factor, is determined. Six possibilities would emerge from these comparisons, namely;

(A) $\mu H_p > B_s$, $A_x > A_w$, (B) $\mu H_p > B_s$, $A_x < A_w$, (C) $\mu H_p < B_s$, $A_x > A_w$,
(D) $\mu H_p < B_s$, $A_x \approx A_w$, (E) $\mu H_p \approx B_s$, $A_x < A_w$, and (F) $\mu H_p \approx B_s$, and $A_x \approx A_w$.

Cases (A), (B), and (C) point to either core saturation or inability to accomodate all windings within the given window area, indicating the need for a larger core. Case (D) represents a surplus in the magnetic capability of the core; a higher -μ and smaller core may be in order. As for case (E), the fact that the window is left unfilled is synonymous to the need for a lower - μ and smaller core for space utilization. Only case (F) represents an inductor design utilizing fully the electromagnetic capability provided by the core-winding combination.

It is highly unlikely, ever for an experienced designer, to choose the right core so that case (F) is achieved in the first try. More often that not, many passes will be taken before case (F) can be arrived

at. Furthermore, there normally exists a number of designs, all of which can satisfy conditions specified in case (F). However, only one of them would provide the lightest combined core and wire copper weight. The minimum inductor weight equations will result in different inductor designs for different conductor sizes selected.

The objective of this discussion is to determine, for a given L, B_s, and A_c, what particular set of A, N. z, and μ will give the combination of least iron and copper weight.

B2. Nomenculatures and Assumptions

The following symbols are used in this appendix:

- A: core sectional area in $meter^2$
- A_c: copper-conductor area per turn in $meter^2$
- A_w: window area of toroid core in $meter^2$
- B_s: saturation flux density of the core material in $weber/m^2$
- D_c: specific gravity of the copper conductor in kg/m^3
- D_i: specific gravity of the magnetic core in kg/m^3
- F_w: winding factor
- F_c: the ratio of mean length per turn of copper conductor to the circumference of the core section, i.e., the pitch factor
- I_p: peak current in ampere in the inductor winding
- L: inductance in Henry's
- N: number of turns
- μ: permeability of the core material in MKS unit, and
- z: mean length of the circular magnetic path in meters.

While the method presented herein is applicable to any core section configuration, a square toroid core section is assumed for convenience. Thus, for a core cross-sectional area A, the circumference of the core section is $4\sqrt{A}$ The mean length per turn of copper conductor is, therefore, $4F_c\sqrt{A}$.

B3. Problem Formulation

Using the aforementioned symbols, two basic equations can be written as:

$$\frac{\mu N^2 A}{z} = L \qquad (B1)$$

and

$$\frac{\mu N I_p}{z} = B_s \qquad (B2)$$

Combining these two equations gives

$$NA - \frac{L I_p}{B_s} = 0 \qquad (B3)$$

The window area is

$$A_w = \pi r^2 = \pi \left(\frac{z}{2\pi} - \frac{\sqrt{A}}{2} \right)^2$$

Where r is the inside radius of the core. Multipling A_w by the winding factor, F_w, gives the total copper area. Assuming that the window is filled, then $NA_c/F_w = A_w$ gives

$$\frac{N A_c}{\pi F_w} = \left(\frac{z}{2\pi} - \frac{\sqrt{A}}{2} \right)^2$$

or,

$$\sqrt{\frac{A_c}{\pi F_w}} \cdot \sqrt{N} - \frac{z}{2\pi} + \frac{\sqrt{A}}{2} = 0 \qquad (B4)$$

As noted before, the mean length per turn of the copper conductor is $4F_c\sqrt{A}$. The total copper and iron weight, W_t, is, thus;

$$W_t = 4 F_c A_c D_c N \sqrt{A} + D_i A z \qquad (B5)$$

The mathematical problem of minimizing inductor weight is now defined as the following: Find the values for A, N, and z to cause a minimum W_t in eq. (B5), using eqs. (B3) and (B4) as constraints. Also find μ from eq. (B2) for this particular set of A, N, and z.

B4. Analytical Solutions Using Lagrange Multipliers

A necessary condition for f (x, y, z) to have a minimum when x, y, z, are subjected to the constraints of

$$p(x,y,z) = 0 \quad \text{and} \quad q(x,y,z) = 0$$

may be found by adding to these two equations the conditions that the function

$$h(x,y,z) = f(x,y,z) - \alpha p(x,y,z) - \beta q(x,y,z)$$

has a minimum, where α and β are as Lagrange Multipliers. Specifically, in addition to p (x, y, z) = o and q (x, y, z) = o, one has the following three more equations:

$$\frac{\partial h}{\partial x} = 0 \quad , \quad \frac{\partial h}{\partial y} = 0 \quad , \quad \frac{\partial h}{\partial z} = 0$$

These five equations can be used to solve the five unknowns x, y, z, α and β.

Relating the foregoing discussion to the present problem, f (x, y, z) corresponds to eq. (B5), p (x, y, z) and q (x, y, z) are equivalent to eqs. (B3) and (B4), thus;

$$f(x,y,z) = 4F_c D_c A_c x y^2 + D_i x^2 z \, , \quad y = \sqrt{N} \, , \quad x = \sqrt{A}$$

$$p(x,y,z) = x^2 y^2 - \frac{L I_p}{B_s} = 0 \qquad \text{(B6)}$$

$$q(x,y,z) = \sqrt{A_c / \pi F_w} \cdot y - \frac{z}{2\pi} + \frac{x}{2} = 0 \qquad \text{(B7)}$$

Therefore,

$$h(x,y,z) = 8F_c D_c A_c x y^2 + D_i x^2 z - \alpha\left(x^2 y^2 - \frac{L I_p}{B_s}\right) - \beta\left(\sqrt{\frac{A_c}{\pi F_w}}\, y - \frac{z}{2\pi} + \frac{x}{2}\right)$$

$$\frac{\partial h}{\partial x} = 8F_c A_c D_c y^2 + 2D_i z x - 2\alpha x y^2 - \frac{\beta}{2} = 0 \qquad \text{(B8)}$$

$$\frac{\partial h}{\partial y} = 16 F_c A_c D_c x y - 2\alpha x^2 y - \beta\sqrt{\frac{A_c}{\pi F_w}} = 0 \qquad \text{(B9)}$$

$$\frac{\partial h}{\partial z} = D_i x^2 + \frac{\beta}{2\pi} = 0 \qquad \text{(B10)}$$

Solving (B6) to (B10) for the non-trivial solutions, one obtains:

$$A = \frac{1}{3}\left(\frac{L I_p A_c}{B_s \pi F_w}\right)^{\frac{1}{2}} S \qquad (B11)$$

$$N = 3\left(\frac{L I_p \pi F_w}{A_c B_s}\right)^{\frac{1}{2}} S^{-1} \qquad (B12)$$

$$z = 2\sqrt{3}\,\pi\left(\frac{L I_p A_c}{B_s \pi F_w}\right)^{\frac{1}{4}}\left(S^{-\frac{1}{2}} + \frac{S^{\frac{1}{2}}}{6}\right) \qquad (B13)$$

$$\mu = \frac{2\pi}{\sqrt{3}}\left(\frac{B_s}{I_p}\right)^{\frac{5}{4}}\left(\frac{A_c}{\pi F_w}\right)^{\frac{3}{4}} L^{-\frac{1}{4}} S\left(S^{-\frac{1}{2}} - \frac{S^{\frac{1}{2}}}{6}\right) \qquad (B14)$$

$$S = \left(1 + \frac{12 F_c F_w D_c}{D_i}\right)^{\frac{1}{2}} - 1$$

Equations (B11) to (B14) illustrate the particular set of A, N, z, and μ that will produce the minimum combined copper and iron weight for an inductor with inductance L, peak winding current I_p, winding cross-sectional area A_c, saturation flux density B_s, winding factor F_w, pitch factor F_c, specific gravities D_c for copper and D_i for the core. Here, A and z are in meters, and μ in Weber/Amp-turn-meter. To convert μ into Gauss/oersted, eq. (B14) would have to be divided by $4\pi \times 10^{-7}$.

As one would expect from a problem of this complex nature, the equations obtained are not as simple as we like them to be. However, they are certainly not incompatible with actual slide-rule evaluations. Furthermore, the equations are readily adaptable for computer processing. In reality, of course, it is rather unlikely that a commercially available core would exist to match precisely those characteristics defined in eqs. (B11) to (B14), and that the mismatch would probably be most prominent for permeability μ, where a few discrete ones can be chosen commercially. Nevertheless, these equations do provide a guideline in designing an optimum weight inductor. The selective process is accomplished without time-consuming iterations, yet it results in the minimum combined iron and copper weight for the required inductor.

B5. Minimum Inductor Weight

Using eqs. (B5), (B11), (B12), and (B13), the minimum W_t in kilograms can be shown to be

$$(W_t)_{min} = \frac{2\pi D_c}{\sqrt{3}} \left(\frac{L I_p A_c}{B_s \pi F_w} \right)^{\frac{3}{4}} S^{-\frac{1}{2}} \left[6 F_c F_w + \frac{D_i}{D_c} \left(S + \frac{S^2}{6} \right) \right] \qquad (B15)$$

B6. Numerical Simplification of Equations (B11) to (B15).

To enhance the utility of equations (B11) to (B15), simplifications can be made to combine the numerical constants within each equation. In the example below, the following constants are assumed for the molypermalloy-powder-core inductor:

$$F_w = 0.4,\ F_c = 2,\ D_c = 8.9 \text{kg/m}^3,\ D_i = 7.8 \text{kg/m}^3,$$

$$B_s = 0.4 \ \text{w/m}^2.$$

Using these constants, the A, N, Z, μ, and W_T presented in equations (B11) to (B15) become functions of L, I_p, and A_c only. The corresponding simplified equations are:

$$A = 2.6 \times 10^{-4} (L I_p A_c)^{\frac{1}{2}} \qquad (B16)$$

$$N = 96 (L I_p / A_c)^{\frac{1}{2}} \qquad (B17)$$

$$z = 0.174 (L I_p A_c)^{\frac{1}{4}} \qquad (B18)$$

$$\mu = 7.2 (I_p)^{-\frac{5}{4}} (L)^{\frac{-1}{4}} (A_c)^{\frac{3}{4}} \qquad (B19)$$

$$(W_t)_{min} = 9.1 \times 10^{-4} (L I_p A_c)^{\frac{3}{4}} \qquad (B20)$$

Here, L is in microhenry, I_p in Ampere, A_c in circular mil, A in square centimeters, N in turns, z in centimeters, μ in Gauss/oersted, and (W_t) in grams.

Thus, with a given L, l_p, and A_c, these equations define completely the optimum permeability as well as the core configuration to achieve a minimum inductor weight. Furthermore, notice the ease of estimating this minimum possible inductor weight, through equation (B20), without the need of actually designing the inductor itself.

B7. Conclusion

Equations specifying the core dimension, the permeability, and the number of turns, are derived to facilitate a toroid inductor design with minimum weight. Without any iteration process, these equations prescribe an inductor with a specified inductance, where the window of the toroid is essentially filled, and the magnetic capability of the core is fully utilized without causing saturation. Furthermore, the inductor weight can be estimated without actually designing the inductor.

APPENDIX C

PARALLEL INVERTER TWO-CORE TRANSFORMER DESIGN

C 1. Design Equations

The basic circuit equations have been identified in Table 8, page 42, which led to the conclusion of earlier saturation of core T1 due to the larger $d\phi/dt$ in T1 as compared to that in T2.

Let the total conduction time of a power switch S1 be T_n, part of which is T_d, where T_d is the sum of the delay including signal transport and transistor storage time, then the difference $\Delta\phi$ in flux level between T1 and T2 when T1 saturates is

$$\Delta\phi = \int_0^{T_n - T_d} \left(\frac{d\phi_1}{dt} - \frac{d\phi_2}{dt}\right) dt = \frac{E_i}{N_A} \cdot \frac{N_E - N_D + 2N_c}{N_D + N_E} \cdot (T_n - T_d)$$

by designing $N_D = N_E$,

$$\Delta\phi = \frac{E_i}{N_A} \frac{N_c}{N_E} (T_n - T_d)$$

Since the $d\phi/dt$ following the saturation of T1 is

$$\frac{d\phi}{dt} = \frac{E_i}{N_A}$$

the time it takes for T2 to saturate successively to T1 is $(N_C/N_E)(T_n - T_d)$. Consequently, if one designs

$$T_d \leqq (N_c/N_E)(T_n - T_d)$$

core T2 would never saturate. The proper design, therefore, is

$$\frac{N_c}{N_E} \geqq \frac{(T_d)_{max}}{(T_n)_{min} - (T_d)_{max}}$$

where $(T_d)_{max}$ is the longest delay expected. The denominator of the above equation is merely $\Phi_1/(d\phi_1/dt)$ where Φ_1 is the flux capacity of T1. However,

$d\phi_1/dt$ was obtained in the report (see Section 8., page 42). Substitution of $d\phi_1/dt$ into the last equation gives:

$$N_C \geqq \frac{(T_d)_{max}}{\Phi_1} \frac{N_E E_i}{N_A} \frac{N_E + N_C}{N_D + N_E}$$

realizing $N_D = N_E$ and rearranging,

$$N_C \geqq \frac{E_i N_D (T_d)_{max}}{2 N_A \Phi_1 - E_i (T_d)_{max}}$$

The foregoing discussion on the half cycle applies when S1 of Figure 13 is the conducting switch. However, the equations used are general, and are independent of whether S1 or S2 is conducting. This means that, so long as both T1 and T2 start approximately at the positive saturation flux level at the beginning of the next half cycle, core T1 would again reach the negative saturation level earlier than core T2. In other words, T1 is the saturating transformer during either half of an operating cycle, and T2 is the core limiting the saturation current. The equations derived are applicable during both half cycles.

C2. Numerical Design

In the actual transformer design, two identical cores are used, each a 52115-1D by Magnetics, Inc. The saturation knee starts pronouncely at 0.8 Weber/meter^2, giving each core a flux-density capacity of 1.6 Weber/meter^2. With an area of 0.151 cm^2 for each core, core T1, thus, has a flux capacity of 24.2×10^{-6} Weber. Using $E_i = 24V$, $N_A = 16$, $N_D = N_E = 35$, and $N_C = 5$, it can be calculated that $d\phi_1/dt = 0.83$. The time required to drive T1 from its negative to its positive saturation is, therefore, about 24.2/0.83 = 29 μs. Given 3 or 4 μs for various delays and another 7 or 8 μs for the shortest T_{off} during normal operation, a 25 kHZ operation is achieved at the minimum input voltage.

With $E_i = 40V$, $N_A = 16$, $N_E = 32$, $\Phi_1 = 24.2 \times 10^{-6}$ Weber, and $(T_d)_{max} = 3 \times 10^{-6}$ sec, the last equation identifies that $N_C \geqq 5.5$ should be used. In actual design, $N_C = 5$ rather than $N_C = 6$ is used as it generated less loss. The selection is supported by experimental observation, which shows that no saturation current is observed in the converter breadboard throughout the line, load, and temperature range. It is noted that such a performance is

achieved without overdesign of the transformer flux capability, as both cores are used very close to their full extent. A decrease of N_C from 5 to 4 definitely produces saturation current at high temperature, high input, and full load.

C3. Other Discussions

The following points concerning the two-core transformer should be noted:

- To a first degree of approximation, the conduction time of the transistor is inversely proportional to the input voltage with this transformer configuration is being used.

- The transformer core will determine the operating T_n; any on-time interval set by the pulse stretcher of the the DCSP will have to be longer than the operating T_n in order not to interfere with the intended operation of the two-core transformer.

- While the transformer is free from any saturation current at the end of a conduction half cycle, its function does not include the suppression of charging current into the transformer winding capacitance at the start of a conduction half cycle. This charging effect is more pronounced for high-voltage converters such as the subject converter, which includes 1kV as one of its output voltages.

- Depending on the initial flux level for the two cores, transformer saturation may occur at the end of the first half cycle of converter operation following the converter turn-on. However, the saturation current is still limited by the peak current sensor discussed in the report.

APPENDIX D

A TWO-STAGE INPUT FILTER WITH NONDISSIPATIVELY-CONTROLLED DAMPING

D1. Introduction

In space applications where switching regulators are frequently employed, an input filter is normally required between the regulator and the power source. The filter serves two functions: 1) to prevent the alternating current component generated by the regulator switching from being reflected back into the power source having high source impedance, and 2) to isolate line-voltage transients in the source so as not to degrade the performances of the switching regulators downstream. Consequently, the filter is required to provide not only high attenuation at the switching frequency of the regulator, but also sufficient damping against any line disturbance so that output peaking is properly controlled at the resonant frequency. In conjunction with the ever-present requirements of small filter size, weight, and loss, a satisfactory filter design becomes rather difficult to achieve without trading one or more performance characteristics for the others.

For example, a conventional LC filter can be highly efficient due to a low damping factor, yet resonant peaking is very high. During severe line transients, such as a step change of the source voltage (including the sudden connection of the source voltage to an initially relaxed filter), the peak transient output voltage across capacitor C may reach a dangerously high level. The damping factor of the filter can be easily increased by introducing resistance R to bring the resonant peaking under control. However, since most of the pulse current drawn by the switching regulator must now encounter R, the efficiency of the filter is greatly reduced.

Described in the following is a two-stage filter capable of providing low loss, high attenuation, and a controlled resonant peaking. The filter

is particularly useful for regulated converters having such stringent efficiency, attenuation, and peaking requirements that conventional single-stage filter systems would simply become either inapplicable or impractical with respect to size and weight.

The two-stage input filter power circuit was presented in page 46 of this report. The following descriptions include component selection guidelines, transfer-function analysis, and design procedures.

D2. Component Selections

The following guidelines can be observed in selecting filter components:

(1) Since C2 supplies the majority of the pulse current required by the switching regulator, the use of low-dissipation capacitors is desirable. Various types of capacitors are likely candidates including mylar, polycarbonate, and polysulfane.

(2) Inductor L2 supplies a minor portion of the alternating current. The use of molypermalloy power-core material for small core loss is, thus desirable.

(3) Capacitor C1 handles very small alternating current during steady-state operation. Foil, solid, and wet-slug tantalum capacitors are suitable for C1.

(4) During steady-state operation when the switching frequency is much greater than the filter resonant frequency, the resistor R1 encounters negligible current. Practically any type of resistor can be used for R1. However, the resistor should have a peak power capability to handle the current inrush due to a step change in the source voltage E_i such as when E_i is sudenly applied to an initially relaxed filter.

(5) Inductor L1 passes essentially a direct current corresponding to that required by the switching regulator. Eddy-current and hysteresis losses are thus of negligible concern. However, design experience indicates that when a higher saturation flux core material such as gapped silicon steel is used for size and weight savings, the small ad handled by L1 seemed to incur enough core loss to place an equivalent resistance across L1. At the switching frequency of the converter, the resistance may be of such a low value as to cause a degradation of filter attenuation capability from its designed performance level.

D3. Filter Transfer Function

By solving two loop equations for the two-stage filter, its transfer function G(s) can be derived as

$$G(s) = \frac{e_o}{e_i} = \frac{1 + sC_1R_1}{\left[\frac{C_2}{C_1}(1+sC_1R_1) + (1+s^2L_2C_2)\right](1+sC_1R_1+s^2L_1C_1) - \frac{C_2}{C_1}(1+sC_1R_1)^2}$$

Three frequencies of particular interest are: (1) the first-stage filter resonant frequency f_1, (2) the second-stage resonant frequency f_2, and (3) the regulator switching frequency F.

(1) At f_1 where $S^2 L_1 C_1 = -1$, the magnitude of G(S), or peaking at f_1, can be derived to be:

$$P_1 = \left|G(j2\pi f_1)\right| = \frac{1 + D^2}{\left(\frac{C_2}{C_1}\right)^2 + D^2\left[1 - \left(\frac{f_1}{f_2}\right)^2 - \frac{C_2}{C_1}\right]^2} \qquad (D1)$$

Here, D is the damping factor of the first stage, i.e.,

$$R_1 = D\sqrt{\frac{L_1}{C_1}} \qquad (D2)$$

(2) At f_2 where $S^2 L_2 C_2 = -1$, the second peak of G(S) can be derived to be:

$$P_2 = \left|G(j2\pi f_2)\right| = \frac{L_2}{L_1} \qquad (D3)$$

The resonance of the high-Q second stage is, thus, effectively clamped to a value corresponding to L_2/L_1 by the presence of the first stage. Since $L_2/L_1 < 1$ is normally observed, peaking beyond 0-db is, therefore, impossible.

(3) At F, where $F \gg f_1$ and $F \gg f_2$, it can be shown that the value of /G(s)/ becomes

$$P_F = \left|G(j2\pi F)\right| = \frac{1}{\left(\frac{f_1}{f_2}\right)^2\left(\frac{F}{f_1}\right)^3\left(\frac{1}{D}\right) - \frac{C_2}{C_1}\left(\frac{F}{f_1}\right)^2}$$

Solving for approximate (F/f_1),

$$\frac{F}{f_1} \cong \frac{1}{\left(\frac{f_1}{f_2}\right)^{2/3}\left(\frac{1}{D}\right)^{1/3} P_F^{1/3}} + \frac{\frac{C_2}{C_1}}{3\left(\frac{f_1}{f_2}\right)^2\left(\frac{1}{D}\right)} \qquad (D4)$$

D4. Design Procedure

The following general observations to aid in the design of a two-stage filter can be make:

- o The factor L_2/L_1 should be less than unity to avoid the second-stage peaking defined in eq. (D3). In typical designs, L_2/L_1 = 0.25 to 0.5 is common.
- o In conjunction with $(f_1/f_2)^2 = L_2\ C_2/L_1\ C_1$, the factor C_2/C_1 should be sufficiently small to permit a positive real solution for D in eq. (D1). Solving for D^2,

$$D^2 = \frac{1 - P_1^2 (C_2/C_1)^2}{P_1^2\left[1 - (C_2/C_1)(1 + \frac{L_2}{L_1})\right]^2 - 1} \qquad (D5)$$

For example, let P_1^2 = (i.e., P = $\sqrt{2}$ for a + 3db peaking), and L_2/L_1 = 0.25. It is then necessary that

$$\left[1 - \frac{C_2}{C_1}(1 + 0.25)\right]^2 > 0.5, \qquad \left(\frac{C_2}{C_1}\right)^2 < 0.5$$

in order for D^2 of eq. (D5) to be positive. Thus,

$$\frac{C_2}{C_1} < 0.225$$

In actual design, C_2/C_1 less than 0.225 should be used to achieve a reasonable value of D that is not exceedingly large. Typically, C_2/C_1 ranges between 0.05 to 0.1.

Using these design equations, the following step by step design procedures can be explained:

1) Calculate the maximum rms current in C2 based on given line and load conditions including overload requirements of the switching regulator.

2) Based on this rms current, choose the capacitors for C2. With the capacitance of C2 selected, a check is make to ensure that the maximum steady-state ripple voltage across C2 is not excessively large. If the calculated result proves otherwise, C2 should be increased accordingly.

3) The ratio of L_2/L_1 and C_2/C_1 can be chosen to achieve a given attenuation at a specified frequency for as long as they are consistent with the afore-described general observations. Some recommended ratios are given here as functions of attenuation, A_T.

$20 \log_{10} A_T$ (i.e., db)	-40	-60	-80	-100
L_2/L_1	1/3	1/4	1/4	1/4
C_2/C_1	1/10	1/15	1/15	1/20
$(f_1/f_2)^2$	1/30	1/60	1/60	1/80

4) With C_2/C_1 and L_2/L_1 chosen, eq. (D5) can be used to calculate the damping factor D in order to limit the resonant peaking to the specified P_1, i.e., the magnitude of the first peak of G(S).

5) In conjunction with a given set of A and F, eq. (D4) is applied to calculate f_1.

6) Determine L_1 from

$$L_1 = \frac{1}{(2\pi f_1)^2 C_1}$$

7) From eq. (D2) and the selected L_2/L_1 ratio, calculate R_1 and L_2.

D5. Effect of Regulator Negative Impedance on Input Filter Performance

The effect of regulator negative impedance on the input-filter performance was discussed in the literature. [31] The discussion was limited to the possible van del Pol type of oscillation when an improperly design filter is matched to the regulator.

Another effect of regulator negative impedance is to degrade the audio-susceptibility performance. The input filter for the parallel-inverter converter is used as an example for illustration.

A voltage of 1V rms is applied to the filter input terminal. The filter output supplies a resistor; the negative resistance representing R is simply $-E_i^2/P_i$, where E_i is the converter input voltage, and P_i is the converter input power [31]. For the parallel-inverter converter, $(E_i)_{min} = 24V$ and $(P_i)_{max} \cong 70W$, giving $R \cong -8.2$ ohms.

With $L_1 = 381\ \mu H$, $L_2 = 127\ \mu H$, $C_1 = 200\ \mu F$, $C_2 = 20\ \mu F$, and $R_1 = 3$ ohms, the audio performance of the filter was calculated by a computer, first using $R = \infty$ and then using $R = -8.2$ ohms. Analytical results are sketched in Figure 29 in which the impact of the regulator negative resistance on the filter audio performance is evident.

The additional peaking due to the presence of the negative regulator resistance was not treated in the analysis of Section D3, as the added component would make the transfer function too complicated to gain any analytical insight. Nevertheless, the equations derived and the design procedure generated still serve as a convenient design tool to meet a required source-current ripple specification. However, the actual filter resonant peaking as a result of the negative-resistance load will be higher than those predicted in equations (D1) and (D3). Using the afore-described filter as an example, the audio-susceptibility data with and without the negative resistance, as calculated by a computer, is presented in Figure 29.

Two additional subtleties involving filter-regulator combinations are noted:

(1) It is, in reality, a negative "impedance" rather than a negative "resistance" that the converter reflects. Over the audio frequency spectrum, the "impedance" may closely resemble a "resistance" only at low frequencies when the open loop gain of the regulator is high.

(2) If the Bode plot of the regulator loop reaches unity gain before the filter resonance-peak frequency, then there is no negative impedance at the filter resonant frequency. Under this circumstance, the resonant peaking of the filter supplying the regulator would be approximately the same as predicted in Eq. (D1).

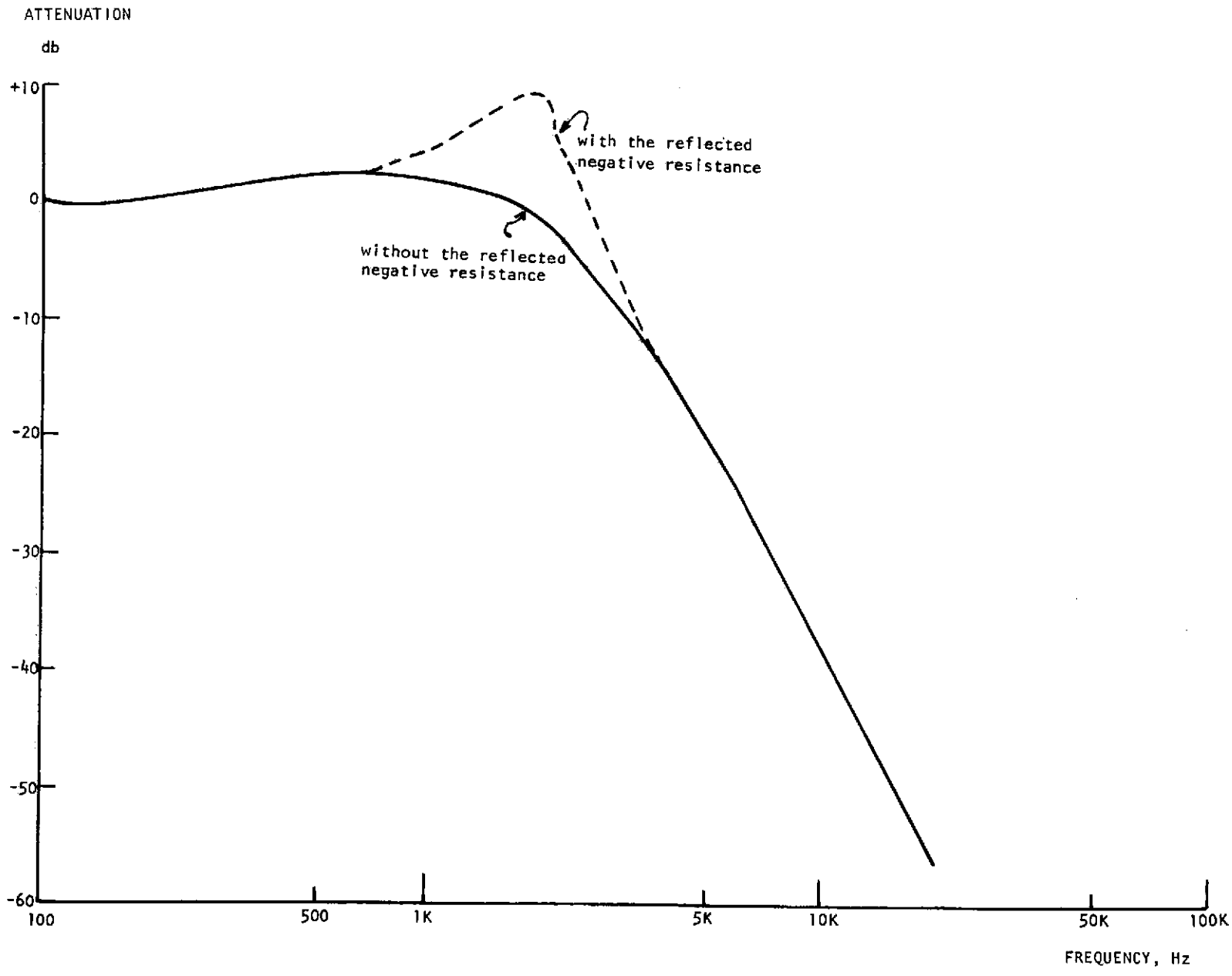


Figure 29. Input-Filter Frequency Response With and Without the Reflected Negative Resistance From the Converter-Regulator

Table 16. POWER CIRCUIT COMPONENTS AND PARAMETERS

POWER CIRCUIT BLOCKS	BUCK-BOOST CONVERTER	SERIES SWITCHING CONVERTER	PARALLEL-INVERTER CONVERTER
Reverse Input Protection	F1 : 5A fuse CR1 : IN5627	Same	Same
Input Filter	L1 : L744, 381μH L2 : L710A, 127μH R1 : 3Ω, 5W C1 : 100μF, 75V C2 : 10μF, 50V	Same as Buck-Boost Converter	L1 : L744, 381μH L3 : L710A, 127μH R1 : 3Ω, 5W C1,C2 : 100μF, 75V each C3,C4 : 10μF, 50V each
Peak-Current Sensor	T1 : L688B VR1 : JAN IN759A CR2 : IN3604 CR3 : JAN IN4942 R2 : 221Ω, 1W R10 : TS (Test Selected)	T1 : L688B VR1 : JAN IN759A CR2 : IN3604 CR3 : JAN IN4942 R2 : 422Ω, 1W R10 : TS	T3,T4 : L688A VR1, 2 : IN759A CR15,15 : IN3604 R6,R7 : 140Ω, 1W U53 : MC680P
Energy Recovery Network	L4 : L697 CR5 : IN9050D CR6 : JAN IN6942 C4,C5 : 0.01μF, 300V, Glass	L3 : L746 CR5 : JAN IN4942	L3,L4 : L697 L5,L6 : L706 CR7,8 : PD9050E CR2-6 : JAN IN4942 CR5-8 : 0.01μF, 300V, Glass
Proportional Current Drive	T2 : T980A Q3 : JAN 2N2222A CR7 : IN3604 R3 : 10K, 1/8W R4 : 2K, 2W	T2 : T980C Q3,Q4 : JAN 2N2222A CR6,7 : IN 3604 R4 : 10K, 2W R5,R6 : 1K, 1W C4 : 1000pF, 200V	T1,T2 : T983C CR4,9 : IN3604 Q3,Q5 : 2N2851 R2,R4 : 2K, 2W R3,R5 : 1K, 1W
Basic Power Circuit Configuration	L5 : L966C, 220μH Q2 : PT9310, TRW CR8 : JAN IN4942 CR9,10 : PD9050D C8-C13 : 100μF, 50V, each	L4 : L704A, 250μH Q2 : 2N5660 CR12 : PD9050D C5-C7 : 100μF, 50V, each	L7 : L753 L8 : L761A,700mH L9,10 : L712A, 1.25mH L11 : L713A, 0.53mH T5 : T992D Q2,Q4 : PT9310 Z1 : 652-827, Unitrode CR12,13 : JAN IN4942 CR16-19 : PD9050D CR20,21,28,29: PD9050A C9 : 25uF, 20V C10 : 0.11μF, 1.5kV C11-14 : 22μF, 50V, each C15,16 : 100μF, 20V, each

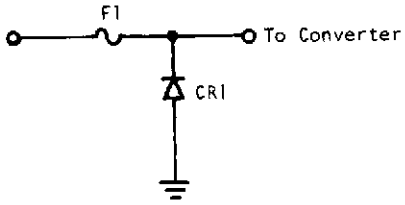
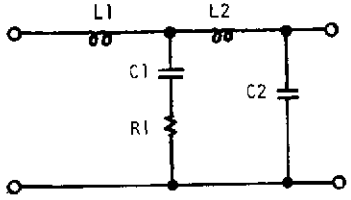
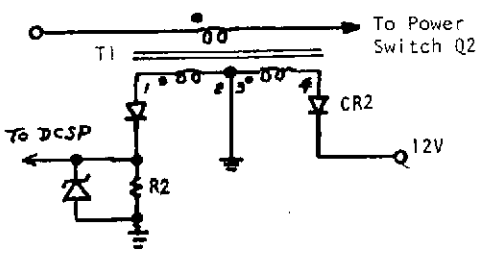
APPENDIX E2

Table 17. CONTROL CIRCUIT COMPONENTS AND PARAMETERS

Control-Circuit Blocks	Buck-Boost Converter		Series Switching Converter		Parallel-Inverter Converter	
ASDTIC Voltage Regulator	R71,R73 : 39.2K, 1/10W R72 : 10K, 1/10W R74 : 43.2K, 1/10W R75 : 16.2K, 1/20W R76 : TS, 1/20W R77 : 21.5K, 1/10W CR71,72 : JAN IN4942	C71 : 10μF, 20V C72,76 : 15μF, 50V C73 : 2200pF, 200V C74 : 0.039μF,100V C75 : 1μF, 50V U71 : X254814,TRW VR71 : PT4-2273	R71,73 : 51.1K, 1/10W R72 : 10K, 1/10W R74 : 28.7K, 1/10W R75 : 16.2K, 1/20W R76 : TS, 1/20W R77 : 14.7K, 1/10W R78 : 4.02K, 1/10W R79 : 15K, 1/8W	C71 : 10μF, 20V C72,76 : 15μF, 50V C73 : 2200pF, 200V C74 : 0.022μF, 100V C75 : 1μF, 50V VR71 : PT4-2273 CR13,71, 72 : JAN IN4942 U71 : X254814,TRW	R12 : 10M, 1W R13 : 120K, 1/4W R14 : 100K, 1/2W R71,73 : 46.4K, 1/10W R72 : 10K, 1/10W R74 : 5.49K, 1/10W R75 : 8.06K, 1/10W R76 : TS, 1/10W R77 : 120K, 1/4W R78 : TS, 1/10W	C71 : 2200pF, 200V C72 : 6.8μF, 35V C73 : 0.022μF,100V C74 : 0.047μF,200V C20 : 250pF, 1.5kV U71 : X254814,TRW CR22-25 : JAN IN4942 L12,13 : L 754 VR71 : PT4-2273 CR71 : IN 5297
ASDTIC Current Regulator	R53 : 200K, 1/8W R54 : 1K, 1/8W R55 : 25.5K, 1/20W R56 : 23.7K, 1/20W R57 : 2K, 1/20W R58 : 4.32Ω, 1W R59 : 511Ω, 1/20W R60 : TS, 1/20W	C51 : 47pF, 200V C52 : 1500pF, 200V C53 : 0.1μF, 100V VR51 : PT4-2273 T3 : T965A CR8,11, 12 : JAN IN4942 U51 : MC680P U52 : RA2909	R53 : 200K, 1/8W R54 : 1K, 1/8W R55 : 100K, 1/10W R56 : 22.1K, 1/20W R57 : 2K, 1/20W R58 : 1Ω, 1W R59 : 432Ω, 1/20W R60 : TS, 1/20W	C52 : 1500pF, 200V C53 : 0.1μF, 100V VR51 : PT4-2273 T3 : T967B T4 : T966A CR8-11 : JAN IN4942 U51 : MC680P U52 : μA 741	None	
Input/Output Isolation	R101 : 1K, 1W R102 : 4.75K, 1/20W R103 : 1.33K, 1/20W R104 : 240K, 1/8W R105 : 56.2Ω, 1W CR101 : JAN IN4942	C101 : 0.01μF, 200V C102 : 33μF, 10V VR101 : FCT 1122 U101 : LM3110 U102 : MCD2 U103 : MC679P	None		R102 : 16.5K, 1/20W C102 : 2.2μF, 20V CR101 : None CR26,27: JAN IN4942 L14 : L755 All other components same as the buck-boost converter.	
Digital Control Signal Processor (DCSP)	R91 : TS, 1/10W R92 : 68.1K, 1/10W C91 : 1500pF, 200V	U91 : MC675P U91 : MC670P U93 : MC672P	R92 : 56.2K, 1/10W C91 : 330pF, 200V C92 : 3300pF, 200V All others same as the buck-boost converter		R97,98 : 15K, 1/10W C92,93 : 0.022μF, 100V C94,95 : 820pF, 200V	U92,94 : MC675P U93,95 : MC660P U96 : MC672P U97 : MC679P
Series Regulator	R31 : 4.32Ω, 1W R32 : TS, 1/20W R33 : 84.5K, 1/20W R34 : 20K, 1/20W Q1 : 2N4900	C31 : 47pF, 200V C32 : 15μF, 20V CR31 : JAN IN4942 U31 : LM205H	Same		Same	
Overload Protection, Undervoltage Protection, Power Magnetics Saturation Sensor	None		None		R51 : 10K, 1/8 R52 : TS, 1/20W R53 : 61.9K, 1/10W R54 : 11K, 1/20W R55 : 47.5K, 1/20W R56 : 39.2K, 1/20W R57 : 2K, 1/20W R91 : 9.09K, 1/20W R92 : 7.5K, 1/20W R93 : 8.66K, 1/20W R94 : TS, 1/20W R95 : 1K, 1/20W R96 : 75K, 1/20W	C51 : 6.8μF, 35V C52 : 1500pF, 200V C53 : 0.1μF, 100V C91 : 33μF, 20V U51 : MC680P U52 : RA2909 U53 : MC680P U91 : μA741 R8,10 : 10K, 1/8W R9,11 : 560Ω, 1/4W VR3,4 : IN965B CR51,52: IN3604

APPENDIX F

DESIGN CRITERIA AND DESCRIPTION OF POWER CIRCUIT FUNCTIONAL BLOCKS

SKETCH OF POWER CIRCUIT BLOCKS	CIRCUIT DESCRIPTION	DESIGN CRITERIA
REVERSE INPUT PROTECTION 	The protection is accomplished by isolating the input source and the converter through the opening of fuse F1 when a negative voltage is inadvertently applied to the converter.	(A) F1 shall not blow during slow converter startup. (B) F1 shall blow before CR1 in case of a reversed input. (C) F1 shall not blow during a step converter start. The majority of the inrush current during converter startup is the charging current to C1 and C2, when L1 and L2 saturate. This current is maximum when the input step voltage is the highest. With the application of a 40V step input, and with nonlinear saturable inductors, a computer program was used to solve for inrush current. Comparing the analytical result to the blow-time curve of the fuse led to the conclusion the fuse will not blow in this worst case.
INPUT FILTER 	The first filter stage with L1-C1-R1 controls the resonant peak of the filter responding to the specified 2.8V rms audio-frequency input voltage. The second stage L2-C2 supplies most of the pulse current required by the buck boost power configuration at switching frequency. The ac component of the pulse current can be attenuated by the combined action of both filter stages to meet the prescribed conducted interference level. Using a high-quality polycarbonate capacitor for C2 results in very little power loss. With C2 providing essentially all the ac component of the pulse current, negligible current flows in C1 and R1 during steady-state operations. Control of resonant peaking is, thus, achieved without degrading the converter efficiency.	(A) Meet MIL-STD-461A (N3) Conducted interference. (B) Sufficient damping for limited resonance peaking. (C) No oscillation when coupled to a regulated converter (i.e., a negative impedance). Design procedures, supported by a computer program, are shown in Appendix F.
PEAK CURRENT SENSOR 	Instantaneous current in Q2 is sensed by current transformer T1, and is reproduced as voltage V_{R2} across R2. During the off time of Q2, reset of core T1 is accomplished through winding 3-4, diode CR2, and a separately generated reset voltage (12V). Voltage V_{R2} is coupled to the DCSP. Any V_{R2} that exceeds a threshold level immediately initiates the turn-off of Q2. Exactly how long the transistor remains in the OFF state subsequent to shutoff by the peak current sensor depends on the minimum	The sensor will not interfere with the normal steady-state operation when there is no excessive peak current. Therefore, with threshold voltage level E_T, the design should be: $$(V_{R2})_{max} = \frac{N_{56}\, R_2\, (I_P)_{max}}{N_{12}} < E_T$$ where $(I_P)_{max}$ is the maximum peak current expected during normal steady-state operations.

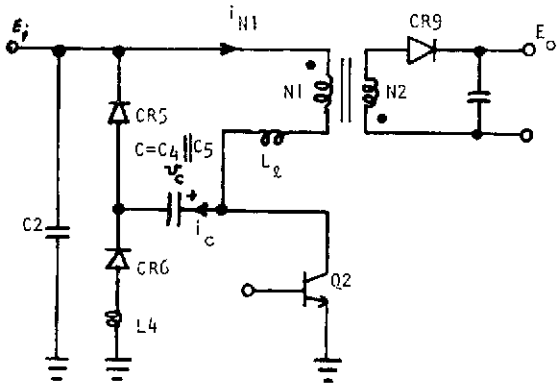
APPENDIX F

DESIGN CRITERIA AND DESCRIPTION OF POWER CIRCUIT FUNCTIONAL BLOCKS (CONT'D)

POWER CIRCUIT BLOCKS | CIRCUIT DESCRIPTION | DESIGN CRITERIA

off time, Tm, programmed into the Digital Control Signal Processor.
Two such sensors are required for the parallel inverter converter, one for each power transistor switch.

ENERGY RECOVERY NETWORK



(1) For Buck-Boost Converter

The function of this network is to absorb the forceful release of energy stored in the leakage inductance of the power inductor after power transistor Q2 is switched from the On state to the Off state. By trapping this energy and returning it to the input filter, higher efficiency and more reliable operation due to less electrical stress on the power transistor are simultaneously achieved.

When Q2 is suddenly turned off, a forceful release of the energy stored in the leakage inductance L_ℓ finds C, CR5, and N1 as a circulating path. Since L_ℓ is always made small through careful inductor design, the resonant frequency determined by L_ℓ and C is very high; the pulse current reaches an amplitude approximately equal to i_{N1} instantly before the end of T_n. As a result of this current, voltage V_c is quickly changed to a reversed voltage which overshoots $[(N_1/N_2)E_o+V_{CR9}]$. When this happens, a path consisting L4, CR6, C, L_ℓ, N1, and C2 forms a complete circuit. This path allows V_c to be clamped at a voltage corresponding to $[(N_1/N_2)E_o+V_{CR9}]$. When Q2 is subsequently turned on, a resonant path provided by C, Q2, L4 and CR6 causes V_c to decay sinusoidally. When the decaying V_c reaches $-(E_i+V_{CR5})$, it is clamped to this voltage, causing a step decrease of i_c to zero. Current i_{L4} now decays linearly at a rate determined by $(E_i+V_{CR5}+V_{CR6})/L4$, and is received as a charging current by capacitor C2.

(A) The proper design of the network should start with an accurate measurement of the leakage inductance L_ℓ. Knowing the peak current I_p in L_ℓ, the energy stored in L_ℓ becomes $L_\ell I_p^2/2$. Since the voltage V_c changes from approximately $[(N_1/N_2)E_o+V_{CR9}]$ to $-(E_i+V_{CR5})$, capacitor C can be estimated by equating $L_\ell I_p^2/2$ to $CV^2/2$, or,

$$L_\ell I_p^2 \cong C\left\{[(N_1/N_2)E_o+V_{CR9}]^2 + [E_i+V_{CR5}]^2\right\}$$

Inductance L4 is then designed in accordance with

$$\pi\sqrt{L_4C} \leq T_n .$$

The trapped energy is then allowed to return fully to the source.

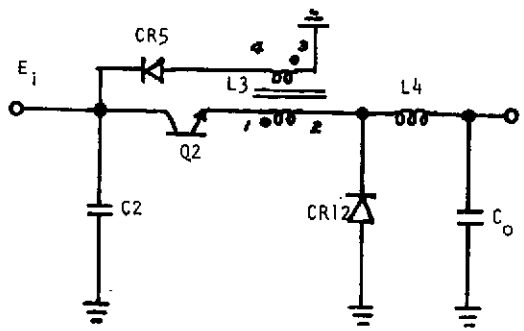
(B) Due to the high frequency current (in the order of meghertz) associated with C, a high quality ac capacitor such as the glass type or the polycarbonate type is needed in order to realize the intended efficiency improvement.

(C) The result of energy recovery can be best demonstrated by oscillograms of Fig. 30 showing the turn-off characteristic of Q2 with and without the network. As high current and high voltage associated with the turn-off of Q2 are made mutually exclusive in Fig. 30(A), the significant efficiency and reliability improvements provided by the energy-recovery network, thus, become evident.

DESIGN CRITERIA AND DESCRIPTION OF POWER CIRCUIT FUNCTIONAL BLOCKS (CONT'D)

POWER CIRCUIT BLOCKS

ENERGY RECOVERY NETWORK(CONT'D)



CIRCUIT DESCRIPTION

(2) For Series-Switching Regulator Converter

The network function is to prevent uncontrolled transient dissipation in Q2 during the turn-on switching interval.

It is noted that conductions of Q2 and CR12 are, ideally, mutually exclusive. However, due to the generally shorter turn-on time of Q2 as compared to the turn-off time of CR12, a short overlapping interval does exist, during which both Q2 and CR12 conducts. If there were no energy-recovery network, a short-circuit path is formed by C2, Q2, and CR12. With C2 being charged to essentially the input voltage E_i, the current during this overlapping interval is limited only by the small circuit stray impedances. As a result, high current at supply voltage is associated with switch Q2. Needless to say, this current is detrimental to the converter efficiency and reliability.

To mitigate this undesirable circuit condition, L3 is designed to absorb all the voltage through winding N_{12} until CR12 is completely turned off. Rate of current rise in Q2 during this interval is limited to $E_i/L3$. This rate is designed such that the transistor current will reach quiescent value only after the diode regains its full blocking capability, thus, eliminating any uncontrolled transistor current. Energy stored in L_3 through winding N_{12} during T_n is returned to C2 through N_{34} and CR5 during T_f.

DESIGN CRITERIA

(A) The proper design of L3 should start with a worst-case estimate of the longest turn-off switching time of CR12. Let this recovery time be T_R, the design equation for the primary inductance L3 would be:

$$L3 \doteq \frac{E_i T_R}{\{I_o - [(E_i - E_o)T_n/2L_4]\}}$$

where I_o is the dc output current, and L_4 is the filter inductance of the power filter.

(B) Following the turn-off of power transistor Q2, the time it takes to return the stored energy in L3 back to the input - filter capacitor C2 is $(N_{34}/N_{12})T_R$. The upper constraint on (N_{34}/N_{12}) is therefore $(N_{34}T_R/N_{12}) < T_m$, where T_m is the minimum off time programmed into the DCSP. If this inequality is not observed, cyclic increase in the flux level will occur in L3, causing an ultimate saturation of L3 and a consequent loss of a controlled switching characteristic during the turn-on of Q2.

(C) The lower boundary in designing N_{34}/N_{12} is established by the power loss associated with the recovery network itself. The form factor of the current in N_{34} decreases as N_{34}/N_{12} is reduced.

(D) During the previously described overlapping conduction interval for CR12, the voltage across CR5 is

$$V_{CR5} = (1 + \frac{N_{34}}{N_{12}})E_i.$$

This voltage must be considered in selecting CR5.

APPENDIX F

DESIGN CRITERIA AND DESCRIPTION OF POWER CIRCUIT FUNCTIONAL BLOCKS (CONT'D)

POWER CIRCUIT BLOCKS	CIRCUIT DESCRIPTION	DESIGN CRITERIA
ENERGY-RECOVERY NETWORK (CONT'D)	An attendent advantage of the energy-recovery network is to minimize the high-frequency voltage spike at the converter output. This spike voltage is normally associated with the high current during the previously described overlapping interval had there been no energy-recovery network. Through the utilization of L3 and CR5, a high di/dt energy source no longer exists. Without the presence of this energy source, the output-voltage switching spike is virtually eliminated.	(E) The result of energy recovery can be best demonstrated by oscillograms of Figure 31 showing the turn-on characteristic of Q2 with and without the network. As high current and high voltage associated with the turn-on of Q2 are made mutually exclusive in Figure 31(A), the significant efficiency and reliability improvements provided by the energy-recovery network, thus, become evident.
	(3) For the Parallel-Inverter Converter	
FIGURES FOR THE TWO PREVIOUS CONVERTERS ARE APPLICABLE HERE	Discussions for the series switching regulator and the buck-boost converter are applicable here. The turn-on energy recovery network discussed in the series switching regulator is particularly important, without which the winding capacitance reflected from the high-voltage secondary winding into the primary will cause a very high charging current. The network eliminates any sharp current spike when the transistor is turned on.	All discussions advanced for the buck-boost converter and the series-switching converter are applicable.
PROPORTIONAL CURRENT DRIVE SEE SKETCH ON PAGE 110	The proportional base-collector current drive offers three advantages. (1) Higher efficiency at light load, (2) less storage time at light load, and (3) more base current for any transient over-current in the collector, thus enhancing reliability by maintaining the transistor in saturation.	(A) The turns ratio of N_{56}/N_{78} is chosen to enforce saturation of Q2 during conduction. The criterion is $\frac{N_{56}}{N_{78}} \leq (h_{FE})_{min}$ for Q2
	The description starts with the signal applied to the base of Q3 through R3 in parallel with C6. The signal is derived from the Digital Control Signal Processor to be discussed later. It is a digital signal with either a logical zero or a logical one forcing function.	(B) The number of turns on N_{34} is designed to reset core T2 within the minimum off time of Q2, i.e. $N_{34} \leq \frac{12\ T_{off} N_{56}}{(V_{BE})_{Q2}\ T_m}$

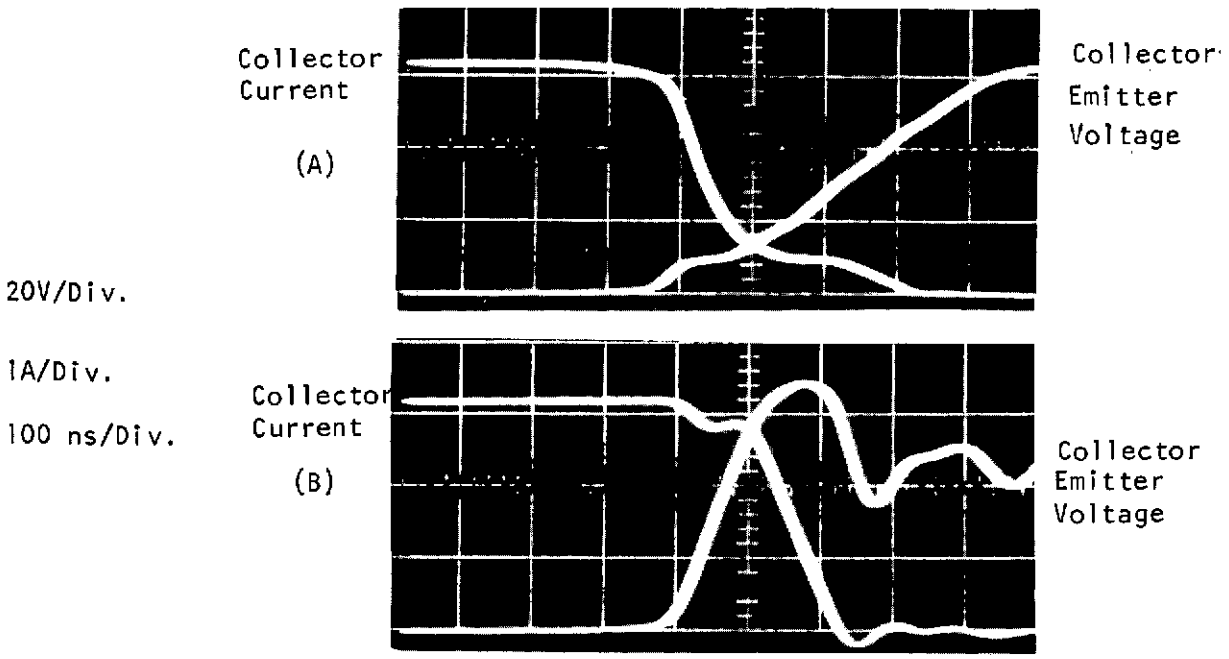


Figure 30. Buck-Boost Converter Power Transistor Switching Pattern with and without the Energy Recovery Network (During Turn-off)

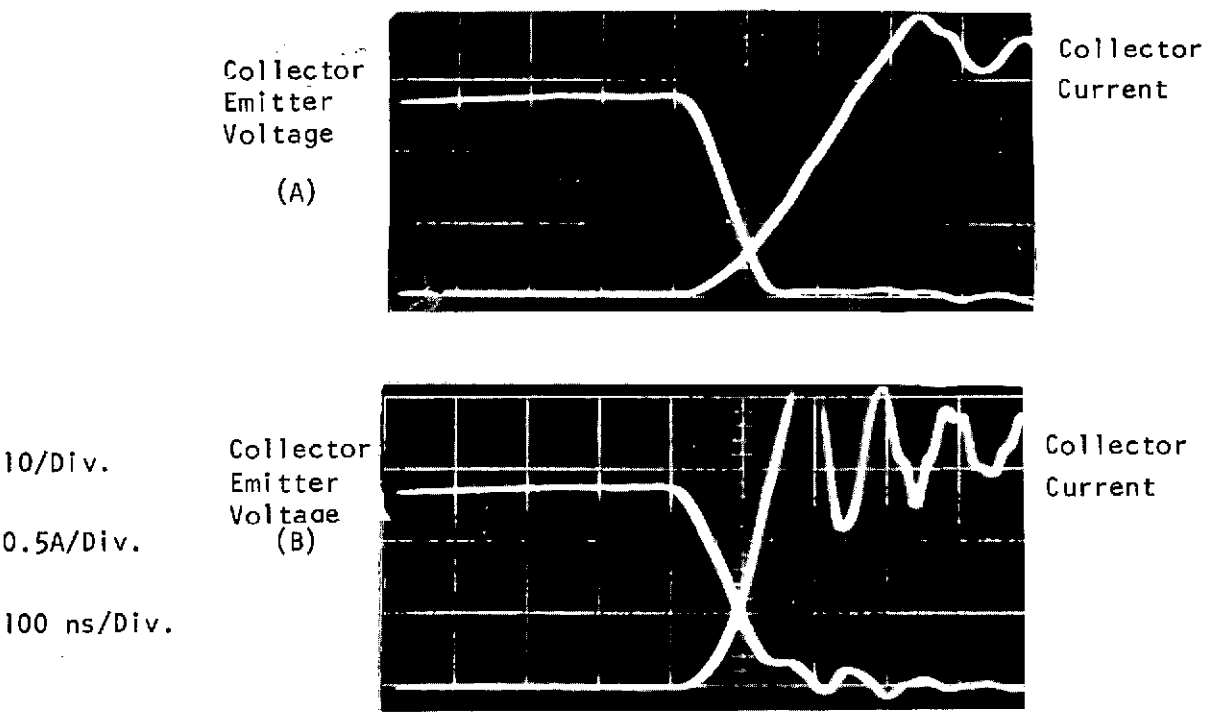


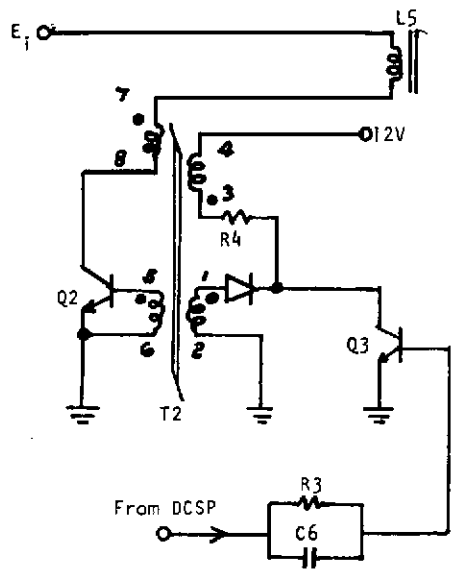
Figure 31. Series Switching Buck Regulator Power Transistor Switching Pattern with and without the Energy Recovery Network (During Turn-on)

APPENDIX F

DESIGN CRITERIA AND DESCRIPTION OF POWER CIRCUIT FUNCTIONAL BLOCKS (CONT'D)

POWER CIRCUIT BLOCKS

PROPORTIONAL-CURRENT DRIVE (CONT'D)



CIRCUIT DESCRIPTION

Let one steady-state cycle start when Q3 has just been turned on by a logical one signal. The voltage across N_{34}, which is essentially the separately-generated 12V, drives the flux level in core T2 toward, say, negative saturation. The undotted end of each winding becomes positive. No base current is supplied to Q2, and Q2 is held cut off. When the flux level reaches the negative saturation, current in N_{34} is limited by R4, which keeps T2 in saturation and stores a small amount of energy in the post-saturation inductance associated with winding N_{34}. After a time interval T_f as determined by the Digital Control Signal Processor, the logical-1 signal suddenly becomes a logical-0, causing Q3 to turn off. The stored energy is now transferred to N_{56}, causing base current to flow in Q2 and initiating the conduction. Subsequently, current flows into the dotted end of N_{78}, the voltages at the dotted ends of all windings become positive, and the flux level in T2 ascends from negative saturation. Thus Q2 is held on, no current flows in N_{12} or N_{34} so long as Q3 remains off, and N_{78} and N_{56} act as current transformer windings such that i_{N56} is proportional to i_{N78}.

The circuit is designed so that at the end of the logical-0 time interval, the ascending flux level has yet to reach positive saturation, i.e., T2 operates on a minor B-H loop.

DESIGN CRITERIA

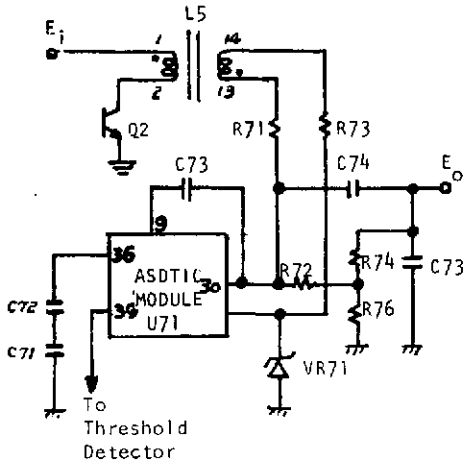
Here, $(V_{BE})_{Q2}$ is the base-emitter forward drop across Q2, the 12V is the externally-generated reset voltage across N_{34}, and T_m has been designated before as the minimum off time set by the DCSP during transient operations when the converter output voltage is below the regulated value.

APPENDIX G1

DESIGN CRITERIA AND DESCRIPTION OF ASDTIC VOLTAGE REGULATOR

CONTROL CIRCUIT BLOCKS

ASDTIC VOLTAGE REGULATOR



CIRCUIT DESCRIPTION

(1) For the Buck-Boost Converter

The central component of the regulator is U71, the microminiaturized ASDTIC control module, manufactured by TRW's Microelectronics Center [3]. In this report, only its application is described.

The module receives a bias voltage of 24V at its pin 36, the 24V being the series outputs of C71 and C72. A series regulator internal to the module provides a 20V output to bias the internal threshold detector and the internal integrator amplifier (with an external feedback capacitor C73 across pin 9 to pin 30). The signals integrated by the integrator are derived from two separate sensing loops.

Loop I sensing the dc converter output voltage is coupled to the inverting integrator terminal through R72, and is compared to reference voltage VR71. The ac voltage across winding N_{13-14} on L5 is sensed by Loop II and is fed differentially to the integrator input terminal through R71 and R73. During T_n of power transistor Q2, the integrator output-voltage ramps downward. Conversely, an increasing ramp voltage is produced during T_f. The triangular integrator output voltage thus obtained is superimposed on the amplified dc error (resulted from Loop I sensing) to effect the regulator control in conjunction with the internal threshold detector.

As soon as the increasing ramp reaches the threshold level, a logical-0 signal is obtained from the threshold-detector output at Pin 39 of the ASDTIC control module. The logical-0 signal is used to initiate a time interval controlled by the standardized DCSP (to be discussed later); the interval corresponds to T_n of power transistor Q2. The turn-on of Q2 reverses the polarity of voltage across N_{13-14}, initiating a negative ramp that lasts for an interval T_n. At the end of T_n, the turn-off of Q2 reverses the voltage across N_{13-14}, returning to an increasing ramp. The instant when the ascending voltage reaches the threshold level marks the beginning of the next T_n, thus the steady-state cycle repeats itself. In summary, for a given T_n determined by the DCSP, the regulation is controlled by adjusting T_f.

DESIGN CRITERIA

(A) Since the voltage across N_{13-14} during T_n is the converter input E_i modified by the turns ratio N_{13-14}/N_{1-2}, and the integrator time constant is $(R_{71}+R_{73})\,C_{73}$, the ramp excursion ΔV_r at the integrator output becomes

$$\Delta V_r = \frac{E_i T_n}{(R_{71}+R_{73})C_{73}} \cdot \frac{N_{13-14}}{N_{1-2}}$$

Since the linear range of the integrator amplifier is about 5V, voltage ΔV_r should be kept to below this value to maintain linear operation. Generally, the design of ΔV_r can range from 1 to 3V.

(B) The design of resistances R_{72} and $(R_{71} + R_{73})$ determines the respective loop gain of the two loops. Its effects were discussed in detail in Appendix A.

(C) Due to the high dc gain of the integrator amplifier, the output regulation is essentially limited only by the sensing resistors and the zener reference. Resistors of the same type should be used for R_{74} to R_{76}, and the zener used has a temperature coefficient of 0.0005%/°C.

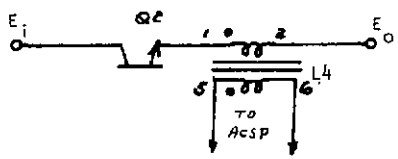
(D) Capacitor C74 connected between the converter output and the inverting input terminal of the integrator is very important. This capacitor, while not included in the original ASDTIC concept, is nevertheless indispensible in realizing the intended utility of the ASDTIC. The theoretical background and the critical functions of C74 are presented in Appendix A. Since this capacitor couples the converter output-voltage ripple into the ASDTIC integrator through pin 30 of the ASDTIC module, the integration output voltage may be distorted from its ideal triangular waveform.

APPENDIX G1

DESIGN CRITERIA AND DESCRIPTION OF ASDTIC VOLTAGE REGULATOR (CONT'D)

CONTROL CIRCUIT BLOCKS

ASDTIC VOLTAGE REGULATOR(CONT'D)



SENSING 1KV: AC SIGNAL FROM 1 KV INDUCTOR (SEE FIGURE 10, PAGE 36)

SENSING dØ/dt: AC SIGNAL FROM THE TWO-CORE TRANSFORMER (SEE FIGURE 10, PAGE 36)

CIRCUIT DESCRIPTION

(2) For the Series Switching Regulator Converter

Referring to the sketch on the previous page, the difference is that the sensed ac voltage is now obtained from a winding on the output inductor L4. Furthermore, instead of using a logical-0 signal at pin 39, a logical-1 signal at pin 37 is used to actuate the DCSP. The dual signal capability is provided by the internal binary at the threshold-detector output of the micro-ASDTIC module.

The change is required for the series switching regulator due to the elimination of the input/output isolation block, which acts as an inverting gate from a digital signal viewpoint.

(3) For the Parallel-Inverter Converter

Two regulating methods are applied:

(A) Regulating one of the multiple outputs to maintain precision regulation for the selected output. Naturally, the regulation of the other outputs does not attain the same precision level as the output from which the control signal is sensed.

(B) Regulating the rate of flux change in the two-core transformer to maintain good overall regulation on all multiple outputs.

Since a major portion of the output power is with the 1KV output, it was chosen for closed-loop regulation to demonstrate method (A). The output is sensed by a divider R12-R13. Due to the high voltage across it, the divider is physically placed in the converter power module across the HV output even though it clearly serves a control function. The rest of the regulator description is identical to the buck-boost converter.

To demonstrate method (B), the rate of change of flux in the transformer is sensed by a low voltage winding $N_{21-22-23}$. The winding voltage is rectified, fed through R_{72} into the integrator, and compared with the same reference, VR71, of the dc loop. The instantaneous difference between the pulse train and the reference becomes the ac signal integrated by the integrator. Consequently, both the dc and the ac loops use the same low voltage signal passing through the same R_{72}. The rest of the voltage-regulator description is identical to method (A).

DESIGN CRITERIA

Since the voltage across N_{56} of L4 during T_n is the voltage difference $(E_i - E_o)$ modified by the turns ratio N_{56}/N_{12}, and the integrator time constant is $(R_{71} + R_{73})\,C_{73}$, the ramp excursion ΔV_r at the integrator output becomes:

$$\Delta V_r = \frac{(E_i - E_o)T_n}{(R_{71}+R_{73})C_{73}} \cdot \frac{N_{56}}{N_{12}} .$$

Regulation by method (A) and method (B) is interchangeable. The interchangeability is provided by a two-pole double-throw magnetic-latching relay.

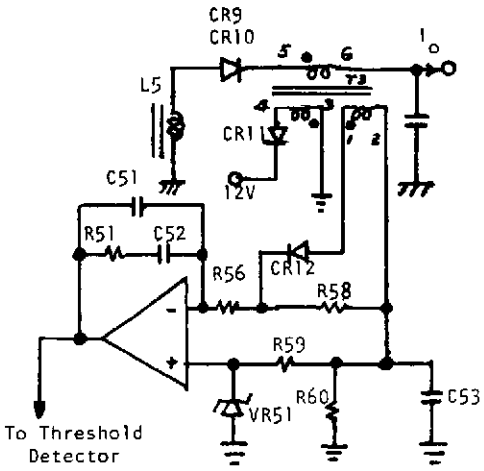
Regardless of the regulating method used, the ramp voltage at the integrator output has a positive slope during T_f, and a negative slope during T_n. As explained in Appendix C, on time is prescribed by the two-core transformer for a given converter input voltage. Regulation is achieved by controlling T_f. When the positive-ramp voltage at the integrator output exceeds the reference level of the threshold detector, a logical-0 signal is obtained from the detector output through pin 39 of the ASDTIC module. This signal is processed by the input/output isolation and the DCSP which, in turn, controls the duty cycle of the power switch.

APPENDIX G2

DESIGN CRITERIA AND DESCRIPTION OF ASDTIC CURRENT REGULATOR

CONTROL CIRCUIT BLOCKS

CURRENT REGULATOR



CIRCUIT DESCRIPTION

(1) For the Buck-Boost Converter

The current regulator performs two functions: (1) regulate the steady-state output current to any adjustable level, and (2) work in conjunction with the peak current sensor to limit electrical stresses on power-handling components.

The most convenient way of applying ASDTIC to the current regulator is to utilize the current signal in the secondary winding of the energy storage inductor. This current waveform contains both dc and ac components . The dc component corresponds to the average output current to be regulated, and the ac component can be integrated by the integrator. The integrator output contains an ac ripple superimposed on a dc amplified error.

Current transformer T3 senses the instantaneous current in the secondary winding of the power inductor. This current waveform is reproduced as voltage pulses across R58. Winding N_{34} and diode CR11, connected across a fixed 12V voltage, ensure the proper reset for core T3. The reset occurs during T_n when no current flows in the secondary of the power inductor.

The voltage across R58 is compared with a reference composed of VR51, voltage divider R59-R60, and noise-suppression capacitor C53, and the error is fed differentially to the integrator through R56. An external resistor is placed across R59 through a connector, and is used to adjust the regulated current level. When this external resistor is opened, voltage V_{R58} is compared with the highest reference voltage across R59, and the regulated output current likewise the highest. Resistance R60 is therefore designed so that this highest current is limited to approximately 110% of the full load current. As the external resistance across R59 is reduced, so is the regulated output current which can be adjusted to any value between 10% to 100% of full load current.

DESIGN CRITERIA

(A) The maximum integrator ramp voltage is

$$(\Delta V)_{max} = \frac{(T_f)_{max}(N_{12}/N_{56})(I_o R_{58})}{R_{56} C_{52}}$$

where $(T_f)_{max}$ is the longest off time associated with the current-regulator operation, which occurs at a regulated current that is 10% of the full-load current under the combined condition of a short-circuited output load and a 40V input voltage.

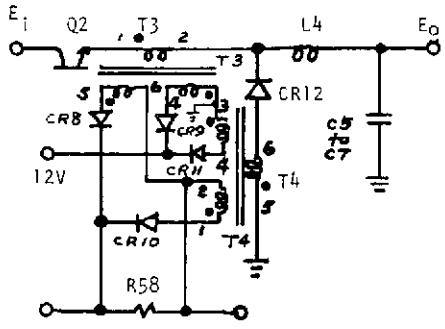
N_{56} and N_{12} are windings on T3, and I_o is the 100% full load current. The resulting $(\Delta V)_{max}$ must remain within the linear range of the integrator.

(B) Resistors R59 and R60 are selected so that, without any external adjustment across R59 the current regulator will limit the output to 1.1 I_F, where I_F is the rated full-load current. Since the current would appear across R_{58} as an average voltage 1.1 I_F R_{58} (N_{12}/N_{56}), resistances R_{59} and R_{60} must divide the zener reference VR51 such that

$$\frac{(VR51)(R_{59})}{R_{59} + R_{60}} = 1.1\ I_F\ R_{58}(N_{12}/N_{56})$$

APPENDIX G2

DESIGN CRITERIA AND DESCRIPTION OF ASDTIC CURRENT REGULATOR (CONT'D)

CONTROL CIRCUIT BLOCKS	CIRCUIT DESCRIPTION	DESIGN CRITERIA
ASDTIC CURRENT REGULATOR (CONT'D) REFER TO SKETCH ON PAGE 113	The integrator's negative feedback network contains C52, R55, and C51. Capacitor C51 has an extremely small capacitance and is used to roll-off the gain at very high frequencies. The value for R_{51} in series with the feedback capacitor C52 provides the lead-lag compensation. The composite integrator output is compared with a threshold detector. The threshold-detector logical-0 output goes to the DCSP to inhibit the turn-on of power switch Q2. Output current regulation is therefore achieved by controlling T_f, with T_n still being the same as that for the voltage-regulating mode.	
	(2) For the Series Switching Regulator Converter	
	Unlike the buck-boost converter where the converter output current is the average of the output-diode current over the full cycle, the output of the series-switching regulator is the full-cycle average of the inductor current, which includes the power-transistor current in Q2 during T_n and the power-diode current in CR12 during T_f. Consequently, sensing of both currents is needed. Current transformers T3 and T4 sense the instantaneous current in Q2 and CR12, respectively. The current-transformer windings for each are N_{12} and N_{56}. The currents sensed are summed (through CR8 and CR10) and converted into a voltage across R58. Winding N_{34} of each transformer is a reset winding, which receives a 12V reset voltage through CR9 for T3 and CR11 for T4. The rest of the circuit description is identical to that presented for the buck-boost converter.	(A) and (B) are identical to those in the buck-boost converter. (C) An additional design constraint is that the current-sensing turns ratio for T3 and T4 must be identical to reflect the continuous MMF in filter inductor L4 during the transition from T_n to T_f and back to T_n. In the subject converter, a turns ratio of ten is used for both T3 and T4.

APPENDIX G3

DESIGN CRITERIA AND DESCRIPTION OF INPUT/OUTPUT ISOLATION AND SERIES REGULATOR

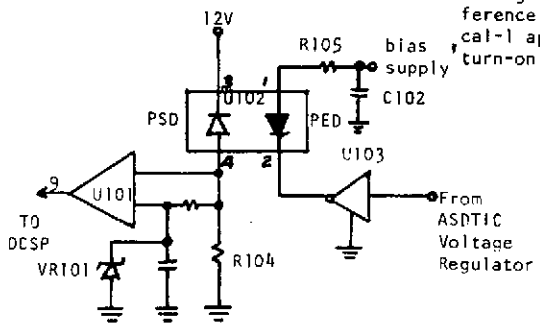
CONTROL CIRCUIT BLOCKS

CIRCUIT DESCRIPTION

DESIGN CRITERIA

INPUT/OUTPUT ISOLATION

(FOR BUCK-BOOST AND PARALLEL-INVERTER CONVERTER ONLY)



The central component for input/output isolation is U102. It consists of a photoemissive diode (PED) integrated into a single entity for the transfer of a light signal with high impedance between the two diodes. PSD is designed to operate in the reverse direction. With no current applied to the PED across terminals 1 and 2, the only current flowing in the PSD is the negligible dark leakage current.

When a logical-1 signal is applied to NAND gate U103, the internal transistor is turned on, and the PED begins to conduct. The conduction of PED causes the reverse current to increase in PSD, resulting in a voltage across R104. When this voltage exceeds reference VR101 of the voltage comparator U101, a logical-1 appears at Pin 9 of U101, which initiates the turn-on of the power transistor Q2 through the DCSP

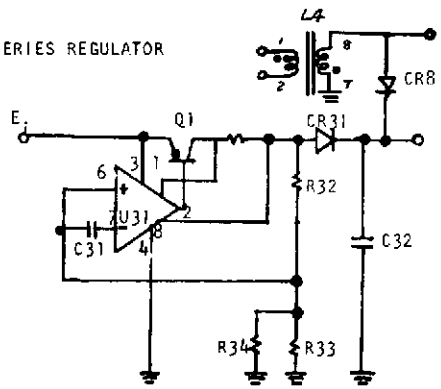
(A) The design guideline of utilizing no ac coupling (to minimize noise-generated false signal) has restricted the use of magnetic pulse transformers for isolation. The dc magnetic coupling requires an auxiliary ac source, therefore, the optical coupling is more attractive from the viewpoints of parts count and power loss, and was chosen for the converter design.

(B) The critical point in optical-isolation design is resistor R105. To start with, the PED of U102 is being driven from an open-collector NAND gate. Since the minimum specified dc transfer ratio between PED and PSD is 0.001 at 85°C, the current in the PED should be 10^3 times that in the PSD. Since the PSD current has to reach (VR101/R104) ≈ 30μA before the voltage comparator can be effected, the current needed in PED is 30mA. Resistor R105 should be set so that

$$R_{105} \leq \frac{V_{C102} - V_{12} - V_{CE(SAT)}}{30 \times 10^{-3}}$$

where V_{C102}, V_{12}, and $V_{CE(SAT)}$ are the voltage across C102, the conducting PED, and the conducting transistor inside of U103.

SERIES REGULATOR



The series regulator (SR) is needed to provide the bias supply for the control logic and for the magnetics resetting. The central component is an IC linear amplifier U31. Pass transistor Q1 is used to boost the regulator's power capability. Resistors R32, R33 and R34 sense the output voltage, divide it down, and compare with a reference internal to U31. Compensating capacitor C31 provides the local feedback. The SR output feeds diode CR31 and C32. Diode CR31 protects U31 from being damaged by the discharging current of C32 when the converter input voltage applied to pin 3 of U31 is suddenly reduced to zero. In addition to shaping the frequency characteristic of the SR, capacitor C32 also handles various input and output pulse current.

(A) In this SR configuration, the linear amplifier U31 must have a voltage capability higher than 40V in order to handle the maximum input voltage to the converter. Therefore, LM205 is used for U31, which has a 50V voltage rating.

(B) During normal operation, when a regulated converter output voltage is maintained, the voltage across C32 as a result of charging current through CR8 is slightly higher than the internal reference of U31, causing Q1 to be biased off. However, during abnormal operations including (a) converter startup before the output voltage reaches its regulated value, (b) when the current regulator is active and the converter output voltage is below its regulation level, and (c) any transient that causes the converter output voltage to dip below its regulated level, conduction of Q1 is immediately resumed to restore active operation of the SR. Thus, in this way, no efficiency degradation is caused by the SR during normal steady-state converter operations.

APPENDIX G4

DESIGN CRITERIA AND DESCRIPTION OF DIGITAL CONTROL SIGNAL PROCESSOR (DCSP)

CONTROL CIRCUIT BLOCKS

DIGITAL CONTROL SIGNAL PROCESSOR

SEE FIGURE 5 ON PAGE 20

CIRCUIT DESCRIPTION

(1) For Buck-Boost and Series-Switching Converters

Pulse stretchers (1) and (2) are contained in a single monolithic IC, MC 675; the MC numbers are Motorola designations. It gives an output pulse-width equal to the sum of the input pulse width and a stretched time interval determined by external circuit components ($R_{91}C_{91}$ and $R_{92}C_{92}$). The R-S flip-flop (1) and NAND (1) are contained in a single triple-input NAND gate, MC 670. The NAND (2), (3), and R-S flip-flop (2) use a single quad 2-input NAND, MC 672. The digital outputs from R-S flip-flop (2) are fed back directly as the inputs to the respective pulse stretcher. The output from NAND (3) is used to drive the base of Q3 in the power-switch proportional-current-drive circuit. When Q3 is turned on, power transistor Q2 is turned off.

Consequently, a logical-0 output from NAND (3) turns Q2 on, and a logical-1 output from NAND (3) turns Q2 off.

Voltage signals applied to the DCSP include the following:

(A) The Converter Input Voltage Applied to R92. The converter voltage E_i, along with R_{92}, C_{92}, and internal threshold level of pulse stretcher (2), determines the on-time interval T_n for power transistor Q2.

(B) A regulated 12V Applied to R91. This voltage, along with R91, C91, and the threshold level inside pulse stretcher (1), determines the minimum off-time T_m of Q2 during transient operations.

(C) Regulated 12V Supply. It is used to bias all DCSP gates.

(D) ABDTIC Voltage and Current Regulator Signals. By applying these regulator signals to NAND (1), digital signals in series with NAND (2) are not affected. Consequently, T_n, discussed in item (A), is not altered by the regulator function. The regulating signals applied to NAND (1), therefore, serve only to inhibit the turn-on of Q2 by extending the off-time interval beyond the programmed T_m to achieve the required duty-cycle control.

DESIGN CRITERIA

(A) Following consideration of converter stability criterion and the desire for optimum size and weight, it was decided that:
(a) the DCSP should provide an essentially constant switching frequency at full-load operation independent of the converter input voltage to facilitate an optimum filter design and (b) at light load, the frequency should be allowed to decrease to avoid instability and excessive switching loss.

(B) For the buck-boost converter, this is done by charging C92 from two resistors. One is R92 connected to converter input E_i; the other is a 20K resistor within the pulse stretcher internally connected through pin 11 of the MC 675 to a regulated logic bias voltage $E_k \equiv$ 12V. Using the method of superposition, voltage V_c across an initially-uncharged C_{92} is:

$$V_c = \frac{E_i R_{92} + e_k R_{in}}{R_{92} + R_{in}} \left(1 - \exp\left[\frac{t}{C\, r_{92}}\right]\right)$$

where r_{92} is the parallel resistance of R_{92} and R_{in}.

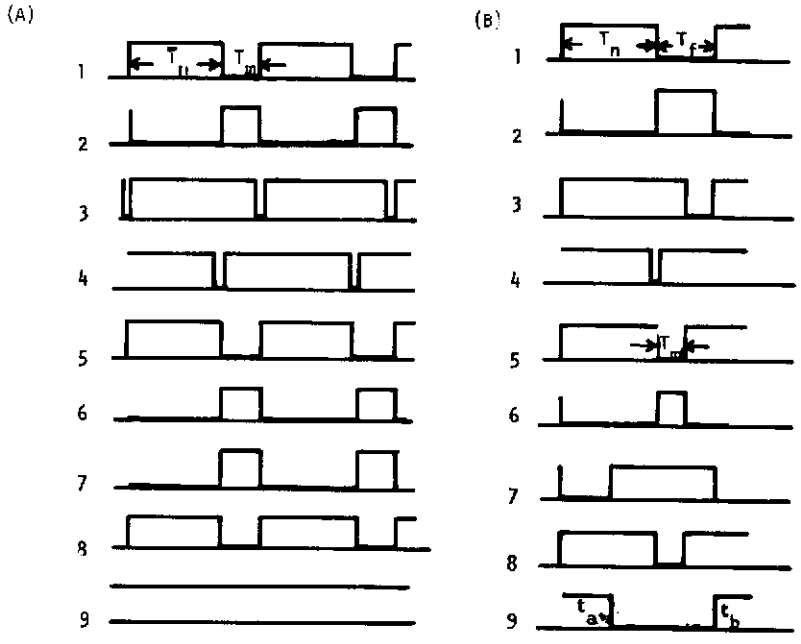
Let E_T be the internal threshold of a pulse stretcher and recognizing that $E_T < E_K << E_i$, one has:

$$T_n \cong \frac{E_T C_{92} R_{92}}{E_i + E_k \frac{R_{92}}{R_{in}}}$$

Since $(T_n + T_f)$ is equal to $\left(1 + \frac{E_i N_2}{E_o N_1}\right) T_n$, where E_o is regulated output voltage, and $N_2/N_1 = 1$ is the designed energy-storage inductor turns ratio, the period of one cycle becomes:

DESIGN CRITERIA AND DESCRIPTION OF DCSP (CONT'D)

CONTROL CIRCUIT BLOCKS	CIRCUIT DESCRIPTION	DESIGN CRITERIA
DIGITAL CONTROL SIGNAL PROCESSOR (CONT'D) REFER TO FIGURE 5 ON PAGE 20	The transmission of digital signals around the loop are explained by waveforms at the key points identified as points 1 through 9. To start with, it is assumed the control signal 9 is always a logical-1, which is equivalent to no regulator action. When signal 2 goes to logical-0, pulse stretcher output 4 starts to time out T_n. When signal 1 goes to logical-0, pulse stretcher signal 3 starts to time out T_m. Signals 3 and 4 cause both flip-flops to change states when the signals go to a logical-0 state, and the converter will be free-running at a frequency determined by $1/[T_n + T_m]$. The next group of waveforms shows the operation with regulator signal 9 as the controlling function. At time t_a, signal 9 goes logical-0, forcing singal 7 to go logical-1. Pulse stretcher signal 4 times out T_n normally. Signal 3 also times out T_m and changes the state of signals 5 and 6. However, because 9 is maintaining 7 high at logical-1, the change in 5 is not registered in 7. Thus off-time T_f continues beyond T_m until T_b, when 9 becomes logical-1. Thus, the output signal 1 is made to provide a logner off time because of the regulator action.	$$T_n + T_f = \left(\frac{E_i + E_o}{E_o}\right)\left(\frac{E_T C_{92} R_{92}}{E_i + E_K \frac{R_{92}}{R_{in}}}\right)$$ If E_o is related to E_k as follows: $$E_k \frac{E_{92}}{R_{in}} = E_o,$$ the total interval $(T_n + T_f)$ will be independent of E_i, and is equal to $(E_T C_{92} R_{92}/E_o)$. These equations were followed Experimentally, the frequency varies from 25.6kHz to 27.5 kHz over the converter input-voltage range from 20V to 40V at full load. (C) For the series-switching buck regulator, a DCSP design using constant $E_i T_n$ leads directly to an essentially constant operating frequency independent of line variation. The frequency can easily be expressed as $(E_o/E_i T_n)$, and is calculated to be 33kHz.



Transmission of Digital Signals

(A) With No Regulator Control

(B) With Regulator Control

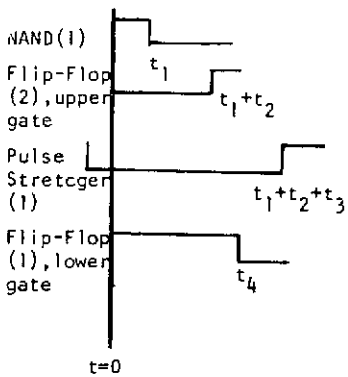
APPENDIX G4

DESIGN CRITERIA AND DESCRIPTION OF DCSP (CONT'D)

CONTROL CIRCUIT BLOCKS

DIGITAL CONTROL SIGNAL PROCESSOR (CONT'D)

SEE FIGURE 5 ON PAGE 20



t_T = minimum switching times for two gates and the pulse strectcher
= $t_1+t_2+t_3$ = 150 nanoseconds

t_4 = maximum switching time for one gate = 100 nanoseconds

CIRCUIT DESCRIPTION

(E) The ON-OFF command applied to NAND(3). A logical-0 applied to NAND(3) causes its output to be logical-1; this condition corresponds to the off condition for Q2. A logical-1 applied to NAND(3) allows the free-running DCSP to start the converter.

(F) The Peak-Current Sensor Singal to Flip-Flop (1). To limit the peak transient current in Q2 requires that Q2 be turned off before the normal T_n is timed out. The early termination of T_n is accomplished by a logical-0 input to Flip-Flop (1) before signal 4 of the pulse stretcher changes state. The signal is obtained from the peak-current sensor through an inverting gate.

Performing all these functions, with excellent noise immunity, the innovative DCSP was developed with a total of only seven parts including three IC's, two capacitors, and two resistors. Furthermore, the DCSP is readily adaptable to different methods of duty-cycle control. The DCSP shown here, with converter input voltage E_i applied to R92, is configured for a converter duty-cycle control based on a constant E_iT_n, i.e., a line-dependent variable on time T_n and a variable off time T_f. However, if an externally-generated constant voltage independent of varying E_i were applied to R92, the DCSP would then produce a constant T_n and a variable T_f. If the feedback signals to the pulse stretchers were not from the outputs of the R-S flip-flop (2), but were from flip-flop (1), then both T_n and T_f would be kept constant, resulting in a constant-frequency operation. An external clock (ap- plied to flip-flop(1) would result in the synchronization of converter switching the clock frequency.

DESIGN CRITERIA

(D) In order not to interfere with the normal regulator function, the minimum off-time interval, T_m, programmed into the DCSP must be shorter than the shortest T_f demanded by the regulator. The time constant $R_{91}C_{91}$ is thus designed so that

$$T_m \cong \frac{R_{91}C_{91}E_T}{E_k} < \text{shortest} \quad (T_f)$$

where E_k is the regulated bias supply, and E_T is the threshold level of the pulse stretcher.

(E) Analysis of the DCSP is required to determine if propagation delay times of the NAND gates and pulse stretcher would cause circuit malfunctions.

Referring to the DCSP schematic and starting at point 3, a logical-0 signal from the pulse stretcher initiates a new cycle. In order for the DCSP to function properly, flip-flop (1) must latch, i.e., signal at point 6 must be "0" before point 3 returns to a "1" condition. For worst case conditions, assume NAND (1), upper gate of flip-flop (2), and pulse stretcher (1) all have minimum delays and the lower gate of flip-flop (2) has the maximum delay.

A timing diagram describing this phenomenon is provided. Here, t = 0 when point 5 changes state. $t_T = t_1 + t_2 + t_3$ = minimum switching times for two gates and the pulse stretcher = 150ns.

t_4 = maximum swtiching time of one gate = 100ns

Consequently, the worst case shortest t_T is still longer than the worst case longest t_4, resulting in still longer than the worst case longest t_4, resulting in point 6 changing state before point 3. Proper operation of the DCSP is assured.

DESIGN CRITERIA AND DESCRIPTION OF DCSP (CONT'D)

(2) For Parallel-Inverter Converter

CIRCUIT DESCRIPTION

Although based on the same principle, the detail mechanization of the DCSP for the parallel-inverter converter is slightly different from that of the two types of converters previously described. The basic difference is caused by the fact that the DCSP now has to provide pulses to control both power switches (Q2 and Q4) instead of a single power switch Q2. Refer to sketch shown in page 120.

Pulse stretchers (1), (2), and R-S flip-flop (1) from a free running oscillator. The time interval of the oscillation is determined by their respective RC networks. The interval may be shortened by either (A) the peak-current sensor signal, or (B) the two-core ttransformer signal indicating pending saturation. These two signals are fed to the proper flip-flop NAND gates.

When the regulator signal applied to DCSP NAND gates ND(1) and ND(2) is a logical 1, there is no inhibit effect, and the DCSP engages in free-running mode. In other words, the turn-off of power transistor Q2 is immediately followed by the turn-on of Q4 and vice versa.

When the regulator signal is a logical 0, the two input signals to flip-flop are logical 1, thus, the output state of flip-flop (2) remains unchanged. Consequently, the change of output state of flip-flop (1) is unable to induce a state change in one of the NAND gates ND(3) or ND(4). The ND with a logical 1 output will remain logical 1, while the ND with a logical 0 output will become logical 1. This corresponds to a time interval when both power switches are in their respective off condition.

Pulse stretchers (3), (4), and NAND gates ND(5) and ND(6) are added to provide a time delay between the output signal of flip-flop (1) and the inputs to ND(3) and ND(4). The delay thus creates a minimum off-time following the turn-off of one switch before the turn-on of the other switch can occur, thus, eliminating the overlap. The utility of these added elements in enhancing a controlled converter startup and overload-protection characteristics was experimentally demonstrated.

The input signals to the DCSP include:

(a) The Converter Input Voltage Applied to R97 and R98. Input voltage E, along with $R_{97}C_{92}$, R_{98} C_{93}, and the internal threshold level of pulse stretchers (1) and (2), determines the maximum T_n of Q2 and Q4 if it is not shortened by signals from the peak-current sensor and the core saturation sensor.

(b) The Regulated 12V Supply. It is used to bias all DCSP gates.

(c) The Regulator Signal From Input/Output Isolation. A logical -0 regulator signal causes a T_f for both power switches.

(d) The Two-Core Transformer Saturation-Sensor Signal. The signals across VR3 and VR4 via windings N_{12} and N_{34} of the two core transformer are applied to flip-flop (1). The one originating from VR3 (VR4) is used to turn off Q2 (Q4). See Figure 10 on page 36.

(e) The Peak Current Sensor Signal. The signals from R6 (Sensing I_{Q2}) and R7 (Sensing I_{Q4}) are applied to flip-flop (1) for the turn-off of Q2 and Q4. See Figure 10.

(f) The Overload Signal. A logical-0 resulting from the overload protection circuit and applied to ND(3) and ND(4) will turn off power transistors Q2 and Q4.

(g) The Under Voltage Signal. A logical-0 applied to ND(3) and ND(4) keeps both power transistors off when the converter input voltage is lower than 21V

During normal operation, the T_n is determined by the two-core transformer. The maximum T_n occurs at the minimum input voltage and was designed to be less than 50μs.

DESIGN CRITERIA

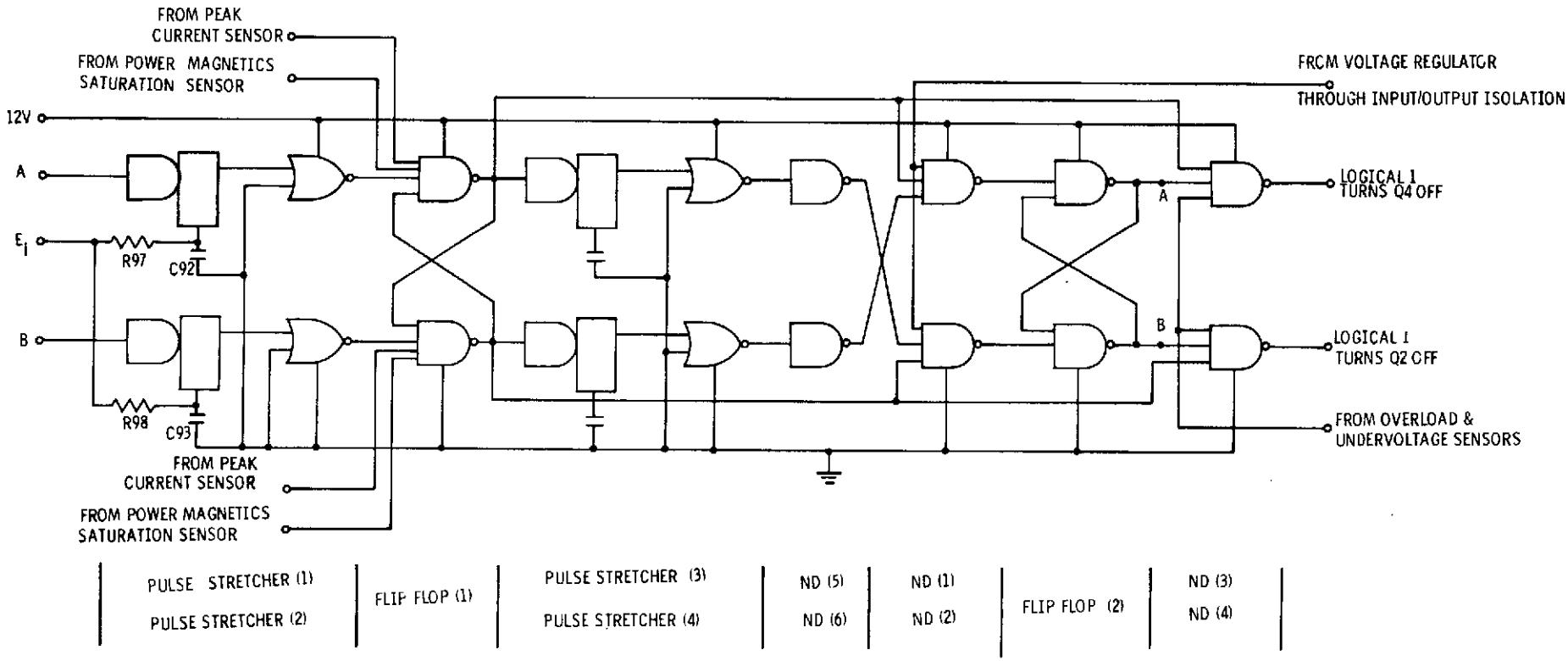
The RC time constant was selected such that, in conjunction with the internal threshold level of pulse stretchers (1) and (2), the time interval in the pulse stretcher, T_n, be greater than 50μs.

Let the internal threshold be E_T, and the converter input be E_i, then the design equation becomes

$$T_n = RC \ln \frac{E_i}{E_i - E_T} > 50\mu s$$

APPENDIX G4

DESIGN CRITERIA AND DESCRIPTION OF DCSP (CONT'D)



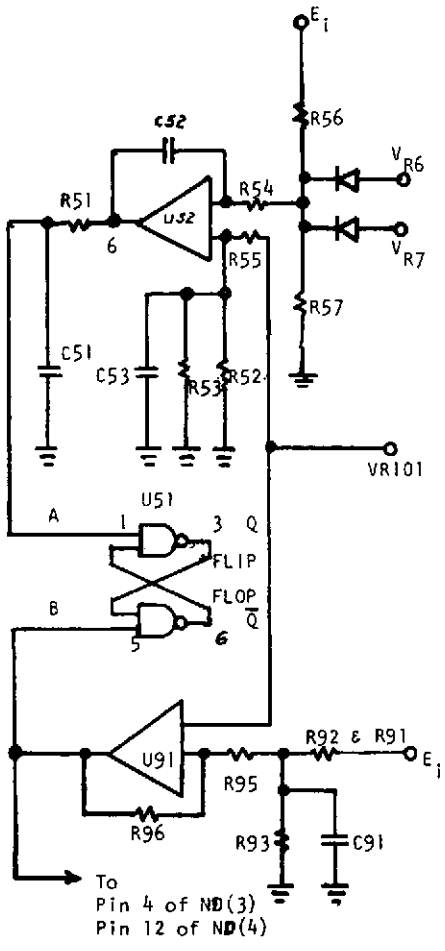
TWO-CHANNEL DIGITAL CONTROL SIGNAL PROCESSOR

APPENDIX G5

DESIGN CRITERIA AND DESCRIPTION OF PARALLEL-INVERTER CONVERTER PROTECTION CIRCUITS

CONTROL CIRCUIT BLOCKS

OVERLOAD AND UNDERVOLTAGE PROTECTION FOR PARALLEL-INVERTER CONVERTER ONLY



CIRCUIT DESCRIPTION

Instead of designing an active current regulator on each of the multiple outputs, which will increase significantly the parts count of the converter, an average "input current limiter" is selected.

The instantaneous input current in each power transistor is accurately represented by the voltages across resistors R6 and R7 of the respective peak-current sensor and, therefore, is conveniently available without additional sensing network. These two voltages are summed to appear across R_{57}. Derivation of V_{R6} and V_{R7} can be seen in Figure 10.

The unidirectional voltage pulse across R_{57} is averaged by the operational amplifier U52 with a time constant $R_{54}C_{52}$, and compared to a reference set by zener VR101 (of the input/output isolation), resistors R_{55}, R_{53}, and R_{52}, and capacitor C_{53}. The logical-1 signal at the output (pin 6) of U52 becomes instantly logical-0 when the input current reaches the reference level. Neglecting the effect of R_{51} and C_{51} for the time being, the logical-0 signal is applied to an R-S flip-flop, pin 1 of U51.

The undervoltage protection is implemented to prevent any uncontrolled converter startup characteristics under a slowly-increasing input voltage. The input voltage is sensed, and compared with reference VR101 through a comparator U91. When the sensed voltage is below the reference, a logical-0 signal is applied to pin 4 of ND(3) and pin 12 of ND(4), keeping Q2 and Q4 off. A logical-1 signal, of course, releases this inhibit when the input becomes sufficiently high. The output of U91 also feeds pin 5 of the flip-flop. The output of the flip-flop, Q, is coupled into pin 5 and Pin 13 of the last NAND gates ND(3) and ND(4).

DESIGN CRITERIA

(A) The RC network between the flip-flop and the integrator amplifier is needed to prevent a false turn-off when there is only a high input current transient. It was decided that a 20ms time interval is sufficiently long to identify a true overload. The $R_{51}C_{51}$ time constant is therefore designed to discharge C_{51} from E_K (i.e., the bias supply) to E_T (i.e., the flip-flop threshold) in 20ms. Using

$$RC = \frac{20 \times 10^{-3}}{\ln \frac{E_K}{E_T}}$$

and with E_K = 11V, E_T = 8V, the RC time constant is found to be about 66×10^{-3} seconds. In actual design, R_{51} = 10K and C_{51} = 6.8μF were chosen.

(B) Capacitor C91, used in the UV protection, serves multiple purposes:

(a) In conjunction with input E_i and resistors R91 through R94, the capacitor creates a time constant when the converter is "knifed" on. Since the 12V logic bias supply is not available at the instant of knife-on, no converter startup is possible in the absence of C91, as the overload-protection network will always act to disallow a normal startup. Capacitor C91 thus accomplishes the function of delaying the converter turn-on following the input-voltage knife-on until a 12V is charged across C51 of the overload protection network.

(b) Capacitor C91 also absorbs whatever mechanical bouncing that may occur when the converter is turned on, either through a knife-on or a command-on switch.

APPENDIX G5

DESIGN CRITERIA AND DESCRIPTION OF PARALLEL-INVERTER CONVERTER PROTECTION CIRCUITS (CONT'D)

CONTROL CIRCUIT BLOCKS

OVERLOAD AND UNDERVOLTAGE PROTECTION FOR PARALLEL-INVERTER CONVERTER ONLY (CONT'D)

REFER TO SKETCH ON THE PREVIOUS PAGE

CIRCUIT DESCRIPTION

The behavior of $\overline{Q}$ can be summarized as the following:

FAULT CONDITIONS	WITHOUT OVERLOAD	WITH OVERLOAD
Without under-voltage	A = 1 B = 1 $\overline{Q} = \overline{Q}$	A = 0 B = 1 $\overline{Q} = 0 \rightarrow$ Converter OFF
With under-voltage	A = 1 B = 0 {Converter OFF $\overline{Q} = 1$	A = 0 B = 0 {Converter OFF Q = {Indeterminate

With the R-S flip-flop and the NAND gate (of the DCSP) working in unison, no converter switching can occur in the event of an undervoltage at the converter input or an overload at the converter output.

Since the overload protection acts essentially as an average input-current threshold detector, proper means must be incorporated to prevent the overload protection from false triggering during short transient, such as converter starting and sudden line or loading changes, when the input current may temporarily register a higher level than the reference. It is for this reason that R_{51} and C_{51} were added. Whenever an apparent overload occurs, which may be real or unreal, capacitor C_{51} will maintain a no-trip voltage for a sufficient time interval to delay $\overline{Q}$ from being a logical-0. Thus, in this way, short transients are overlooked by the overload protection, and sources of false triggering are avoided. During this delay time, the stress on the power transistor is limited by the peak current sensor and the energy-recovery network.

DESIGN CRITERIA

This description suggests that the time constant involved in charging C91 from zero to E_{ru} (the reference level of the undervoltage detector) should be longer than that required to change C_{51} from zero to E_{ru}(the threshold level of the R-S flip-flop in the overload protection network). Mathematically, the design can be expressed as:

$$\frac{C_{91}(R_{91} + R_{92}) \ln \frac{E_i}{E_i - E_{ru}(1 + P)}}{1 + P} > C_{51} R_{51} \left(\ln \frac{11}{11 - E_T}\right)$$

$$P = \frac{(R_{91} + R_{92})(R_{93} + R_{94})}{R_{93} R_{94}}$$

and the TTV is the effective bias supply voltage, i.e., the 12V bias less an internal diode drop.

(C) Since the protection network detects the average input current as a voltage across R_{57}, and compares it with a fixed reference, a larger power dissipation would occur for a higher input voltage. To prevent this linear increase of power dissipation, resistor R_{56} is added between the converter input and R_{57}. The divider action of R_{56} and R_{57} as the converter input voltage is increased, causes the protection network to trip with a lower input current.

(D) Once the overload protection is triggered by a true overload of sufficient duration, the converter will turn off. A reset of the turn-on command is needed to restart the converter. No restarting can be achieved unless the overload is cleared.

APPENDIX H

NOMENCLATURES

A	Cross-sectional area of core, m^2
A_C	Copper conductor area per turn, cir mil
A_T	Filter attenuation requirement, db
A_W	Window area of toroid core, m^2
A_I	Integrator amplifier internal rolloff frequency, Hz
B_P	Peak flux density, weber/m^2
B_S	Saturation flux density, weber/ m^2
C_o	Output capacitor, μF
D	Damping factor
D_c	Density of copper conductor, Kg/m^3
D_i	Density of magnetic core, Kg/m^3
e	Efficiency
e_o	Instantaneous converter output voltage, V
e_{o1}	Loop I signal voltage, V
e_{o2}	Loop II signal voltage, V
E_D	Threshold-detector output voltage, V
E_i	Converter input voltage, V
E_I	Integrator output voltage, V
E_K	Logic bias voltage,regulated, V
E_L	AC inductor voltage, V
E_o	Average converter output voltage, V
E_P	Pulse-generator output voltage, V
E_R	Reference voltage, V
E_{ru}	Reference level of under-voltage detector, V
E_T	Threshold level, V
F	Converter switching frequency, Hz
F_c	Pitch factor
F_n	Negative-peaking frequency, Hz
F_w	Winding factor
g	Voltage divider ratio of the modified ASDTIC
h_{FE}	Transistor current gain
i_C	Instantaneous source current, A
I_F	Rated full-load current, A

I_o Average converter output current, A

I_p Peak transistor power-switch current, A

I_{in} DC input current, A

K Integrator-amplifier open-loop dc gain, db

K_d Voltage divider ratio of the original ASDTIC

L_ℓ Leakage inductance, μH

L_o Output inductor

L_p Primary winding inductance, μH

N Number of turns

O_I Instantaneous Integrator output voltage, V

P_o Converter output power, W

P_1 First-stage filter resonant peak, db

P_2 Second stage filter resonant peak, db

Q Transistor power switch

R_c Equivalent ESR of C_o, ohms

R_K Critical load resistance for L_o to exhibit discontinuous MMF, ohms

R_L Load resistance, ohms

R_{in} Pulse stretcher internal bias resistance, ohms

R_{dc} DC winding resistance of L_o, ohms

T Period of one cycle, sec.

T_f Power-switch off time, sec.

T_m Minimum off time set by the pulse generator, sec.

T_n Power switch on time, sec.

μ Permeability, Weber/ Amp-Turn Meter

V_{BE} Base-emitter voltage drop, V

V_{CE} Collector-emitter voltage drop, V

W Total inductor weight, Kg

Z Mean length of magnetic path, m

ΔE_o Output voltage ripple, V

ΔI_{in} Input current ripple, A

ΔV_r Integrator output ramp amplitude, V

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