P
2UP

CALIFORNIA INSTITUTE OF TECHNOLOGY

JET PROPULSION LABORATORY
4800 OAK GROVE DRIVE
PASADENA, CALIFORNIA 91103

CHARGE COUPLED DEVICE IMAGE SENSOR STUDY

CONTRACT NO. 953674
(SUBCONTRACT UNDER NASA CONTRACT NAS7-100)
(TASK ORDER NO. RD-65)

FINAL REPORT

FEB 1974

FAIRCHILD CAMERA & INSTRUMENT CORPORATION
Semiconductor Components Group
464 Ellis Street, Mountain View, California 94042

CALIFORNIA INSTITUTE OF TECHNOLOGY

JET PROPULSION LABORATORY
4800 OAK GROVE DRIVE
PASADENA, CALIFORNIA 91103

CHARGE COUPLED DEVICE IMAGE SENSOR STUDY

CONTRACT NO. 953674
(SUBCONTRACT UNDER NASA CONTRACT NAS7-100)
(TASK ORDER NO. RD-65)

FINAL REPORT

FEB 1974

This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, sponsored by the National Aeronautics and Space Administration under Contract NAS7-100.

FAIRCHILD CAMERA & INSTRUMENT CORPORATION
Semiconductor Components Group
464 Ellis Street, Mountain View, California 94042

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

1.0 INTRODUCTION

This report presents the results of a four-month study program conducted by Fairchild Camera and Instrument Corporation to evaluate charge-coupled device (CCD) image sensors for use in spacecraft-borne imaging systems specified by the Jet Propulsion Laboratory of the California Institute of Technology. This study resulted in design recommendations for two sensors, an approximately 500 x 500 element imaging device and a 1 x 190 element linear imaging device with a 190 x 121 buffer store. Emphasis was placed on the higher resolution, area-image sensor.

Although Fairchild had at the start of the program developed both 100 x 100 element and 1 x 500 element prototype CCD sensors that demonstrated the potential of superior performance of charge-coupled devices over other silicon photosensitive arrays, a number of basic questions were raised which concerned the performance of CCD sensors under operating conditions required for the JPL application, namely, a low temperature to -40°C and a slow scan rate of 10 KHz. Experiments conducted in this study with 1 x 500 linear arrays have shown that the dark current, as expected, is substantially reduced and charge-transfer efficiency is not degraded at this temperature and at slow scan rates. A more qualitative experiment with a 100 x 100 area array also showed improved performance at low temperature.

Experimental evidence was also sought in this study to establish the merit of employing a buried channel under these operating conditions. A number of 1 x 500 linear surface-channel arrays were constructed, i.e., without a buried channel in the photosensor and transfer-register regions of the device. The best of these

devices demonstrated lower charge-transfer efficiency than those with a buried channel under the specified operating conditions.

Another basic consideration of this study was to examine whether the interline-register design possessed any advantages over a "conceptually simplest" frame-transfer design with no buffer store in the desired snapshot mode of operation. A conclusion was reached that the interline-transfer by virtue of separating the photosensor function from the transfer process offers a number of operational features in the snapshot mode: a) exposure of an image may be made while part of the previous image is being transferred out; b) element blooming control can be obtained; c) a means of exposure control is available.

After the objectives for the proposed sensors are briefly listed in Section 2 of this report, results of experiments, design considerations and estimates of device performance are given in Section 3. The report is concluded with a summary discussion of the major technical recommendations in Section 4.

2.0 PROGRAM OBJECTIVES

The objective of this study program was to recommend approaches to the development of an area and a linear CCD sensor for application to future spacecraft-borne imaging systems. Guideline performance goals were divided with two priority groups. First priority goals are those performance specifications that must be met in an eighteen-month development program. Second priority objectives are features of the devices which although desirable, may risk implementation of the eighteen-month program; they may be incorporated in the development program if the risk is minimal, or they may appear in subsequently modified device designs if the risk is great.

2.1 Performance Goals for the Area-Sensor Array

2.1.1 First Priority Objectives

Sensor Configuration

The monolithic CCD chip shall contain approximately 500 x 500 matrix (2.5×10^5) of photosensor elements. The photosensitive sampling apertures shall be on not greater than 25 micron centers in both horizontal and vertical directions.

Data Rate

All other goals must be achieved at a readout rate of not higher than 10^4 picture elements per second. Cooling to -40°C is acceptable to obtain good performance for this and related goals.

Exposure Time

The array shall meet all other specifications when operated at exposure times ranging from one millisecond to five seconds.

Sensitivity

For a uniform exposure of 100 $\mu J/M^2$ from a 2854°K source, the ratio of peak signal to RMS noise at the output of a preamplifier shall be at least ten to one.

Gamma

Over the linear range of the light transfer curve, the gamma shall be 1 ± 0.2.

Dynamic Range

At any fixed sensitivity, dynamic range shall be at least 1000:1, defined as nominal saturation exposure divided by noise equivalent exposure, where nominal saturation exposure shall be defined as the highlight exposure at which gamma is 0.8. Also, the number of gray level steps spaced at $\sqrt{2}$ steps in radiance shall be at least ten.

Signal and Dark Current Uniformity

The output signal non-uniformity for uniform exposures of 5% and 80% respectively, of nominal saturation exposure, shall not exceed 15% and 5% respectively over the entire array. Dark current uniformity shall not exceed 20% over the entire array. Non-uniformity shall

be defined as the standard deviation from the mean, excluding these elements allowed under Blemishes, below.

Blemishes

A blemish shall be defined as an output signal variation equal to 20% of the output at nominal saturation exposure amplitude (as defined under Dynamic Range), when the sensor is unilluminated, or is exposed to a flat field which produces nominal saturation amplitude. Blemishes shall be limited to two entire lines plus 50 additional photosensor elements.

Residual Image

The second readout of an image containing highlights up to the saturation level shall produce a residual signal no greater than 1.0% of the amplitude of the highlight signal obtained at first readout. If necessary, this may be achieved by interposing between the two readout periods an erasure operation. The duration of the erasure operation shall not be greater than one frame readout time.

Modulation Transfer Function

When imaging from a 2854°K source, the array shall have an MTF of at least 60% for an image spatial frequency of 20 lp/mm. The MTF shall not vary more than 10% across the entire area.

Spectral Response

The spectral response shall be at least as broad as that which is characteristic of silicon vidicons, such as the RCA 4532, GEZ7975, or TI Tivicon.

Image Plane Flatness

The maximum deviation from true flatness over the image plane area shall not exceed ± 0.02 mm.

Operating Temperature

The array shall meet all imaging performance requirements while operating at a recommended temperature above -40°C. Operation at temperatures between -60°C and +45°C for a continuous period of ten hours shall not cause permanent degradation.

2.1.2 Second Priority Objectives

Electronic Exposure Control (Elimination of a Mechanical Shutter)

Electronic exposure control shall be incorporated.

Sensitivity Control

Sensitivity shall be electronically controllable from the value required under sensitivity down to one-tenth of that value.

Blooming Control

At any fixed sensitivity, the array shall be capable of accepting a small circular optical image (.25 mm in

diameter) at an exposure level of 100 times the nominal saturation exposure as defined under Dynamic Range, and producing at the video output an apparent circular image diameter not to exceed twice the apparent image width resulting from an equal optical diameter input at 0.1 times nominal saturation exposure.

Operating Life

The array shall not exhibit any degradation in performance while operating continuously at the recommended temperature and voltages at an input irradiance of two watts/M^2, for a period of not less than 2500 hours.

Non-Operating Life

The non-operating life, defined as the time during which power is not applied, shall be in excess of five years at any temperature between -40°C and +25°C. The array shall not exhibit any degradation in performance following this duration of accumulated non-operating time.

Shock and Vibration

The array shall meet all imaging performance requirements after a non-operating exposure to each of the following environments:

a) Sinusoidal Vibration - Vibration in all three axis of one octave per minute at the following levels:

- 5 to 30 Hz at 0.75 g rms,
- 30 to 200 Hz at 15 g rms,
- 200 to 1000 Hz at 9 g rms,
- 1000 to 2000 Hz at 6 g rms.

b) Random Vibration - Vibration along all three axis for 60 seconds per axis at 18.1 g rms shaped spectra as shown in Figure 2 of the Study Guideline.

c) Mechanical Shock - Two 250 g, 0.5 ± 0.1 ms terminal peak saw-tooth shocks along three axes (12 tests).

Radiation

The sensor shall not fail to meet performance specifications after either a cumulative dose of 10^5 rads of ionizing radiation or after dislocation damage equivalent to that induced by a fluence of 10^{11} 1 MeV equivalent n/cm^2.

2.2 Performance Goals For The Linear Sensor Array

2.2.1 First Priority Objectives

Sensor Configuration

The CCD sensor shall consist of a 100 x 1 element linear array of photosensor elements with a self-contained storage buffer capable of storing 100 lines of data (10^4 element capacity). The sensor chip may contain buffers, preamplifiers, cooling provisions, and other elements necessary to meet these performance goals. The photo-sensitive sampling apertures shall be not greater than 25 micron centers.

Data Rates

Data shall be transferred from the photosensor array into the self-contained data storage buffer at a rate of 100 lines/second. It will, therefore, require one second to fill the buffer. Data shall be read out of the storage buffer

at a rate of 100 elements/second. It will require 100 seconds to empty the buffer. The last picture element will therefore, have been stored over 100 seconds before it is converted to digital form and transmitted.

All other first-priority goals are identical to those for the Area Sensor Array except under Residual Image "the duration of the erasure operation shall not be greater than one millisecond" rather than "greater than one frame readout time".

2.2.2 Second Priority Objectives

All second-priority objectives are essentially identical to those for the area sensor array.

3.0 TECHNICAL APPROACHES

3.1 Introduction

This section of the report is devoted to the design considerations specified under the contract for this study as well as the results of experiments undertaken to investigate the behavior of dark current and transfer efficiency at low temperature. Emphasis is placed on those factors involved in the first-priority objectives of the area sensor array.

Section 3.2.1 presents experimental evidence for the merit of employing a buried-channel structure under the low temperature and slow scan rate operational conditions for the proposed device.

Section 3.2.2 is a discussion of the many factors related to photosensitivity and noise in the photosensor and transfer-register regions of the device. A short subsection is devoted to quantum efficiency and responsivity. This is followed by a description of noise sources. The final three subsections describe experimental results on behavior of dark current at low temperature and the application of these results to obtain an estimate of noise equivalent signal and dynamic range for the proposed area sensor array.

Section 3.2.3 is a description of charge-transfer efficiency measurements carried out from room temperature to various low temperatures for different sets of linear CCD's at different operating frequencies.

Section 3.2.4 is a comprehensive treatment of our recommended optimum configuration of the area sensor array. In the first subsection a "conceptually simplest" frame-transfer type of design is introduced to arrive at the recommended CCD cell structure and clocking mode. The next subsection describes the operational advantages of employing the interline-transfer device configuration. The third subsection discusses the use of butted-chips to make arrays with larger numbers of elements. The final subsection reviews the trade-offs involved for front-side vs. backside illumination.

Section 3.2.5 is a brief description of three types of on-chip amplifier available on Fairchild image sensors. Emphasis is given to the noise limits for each.

Section 3.2.6 is a discussion of the optical and electrical properties of polysilicon gate structures.

Section 3.2.7 briefly indicates the various structures that may be employed to obtain element anti-blooming.

The design features and the estimate performance of the proposed area array sensor are presented in a series of tables in Section 3.3; a similar set of tables for the linear sensor array appears in Section 3.4

3.2 Design Considerations

3.2.1 Buried Channel CCD

3.2.1.1 Buried Channel Concept

A surface-channel charge-coupled device (CCD) may be thought of as an array of MOS capacitors where the gate electrodes are isolated by a low conductivity dielectric. When a p-type substrate is used, a sufficiently large positive potential applied to a particular gate of the array initially depletes the surface region of the silicon of all free carriers. The potential well thus formed may be filled by minority carriers, i.e., electrons in this case, which are either thermally generated in and near the depletion region, optically generated or electronically injected. The charge packet thus formed may be moved from well to well in shift register fashion by suitable clocking of the gate potentials. Since the charge is moved along the $Si-SiO_2$ interface, transfer efficiency is reduced by the interaction of the electrons with interface-state traps.

One method of minimizing this effect is to implant in the silicon a donor layer to a depth of approximately 0.5 microns. When a positive potential is applied to the gate of this structure, a potential profile schematically shown in Figure 3-1 is developed. The energy minimum then lies a distance x_{Max} beneath the surface. Electrons which are stored and transferred along this buried channel eliminates interaction with the surface. Transfer of electrons

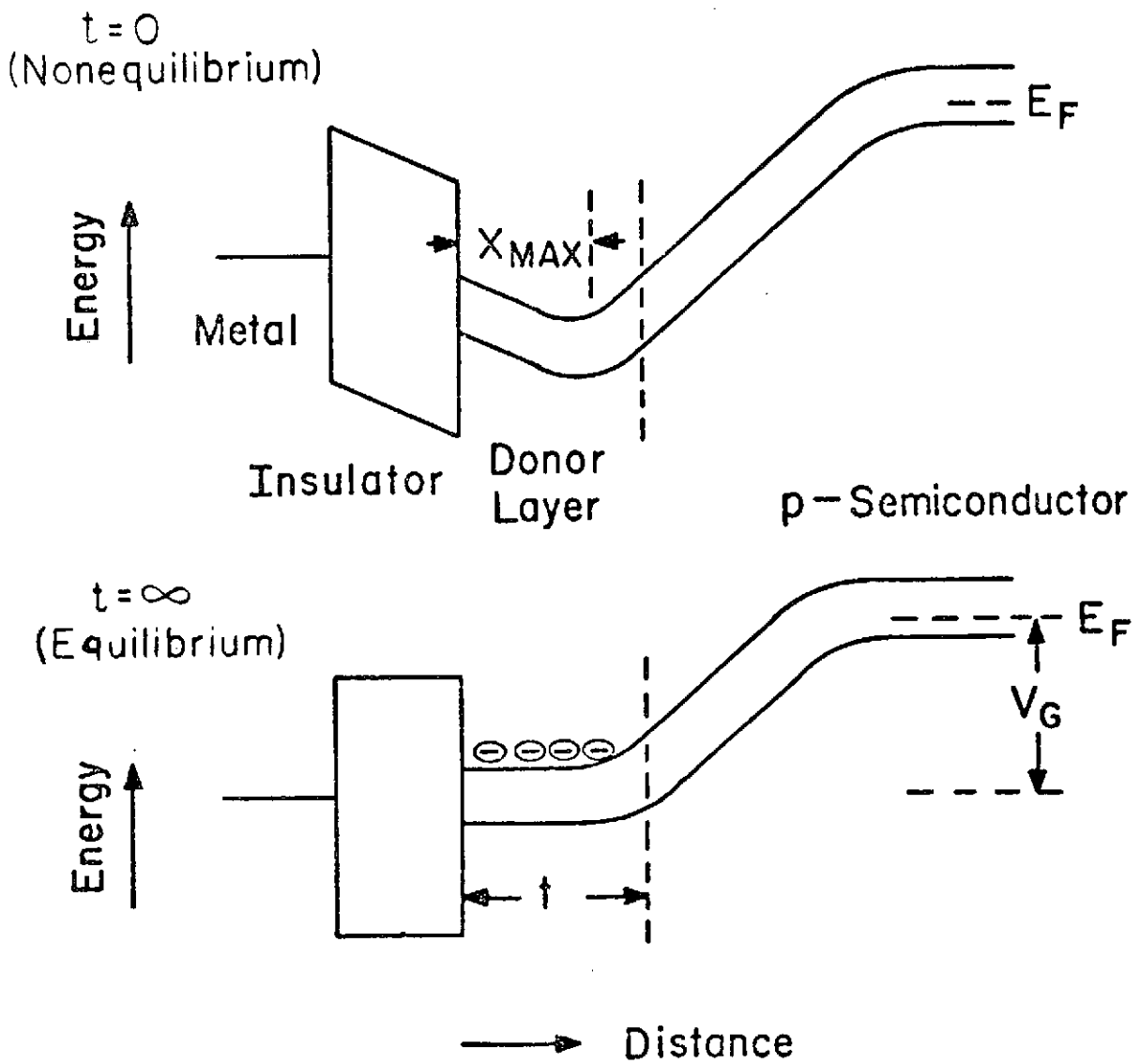


FIGURE 3-1 MIS Capacitor With Donor Layer

is also aided by broadened fringing fields in the electrode-gap region because of the increased distance of the electrons from the gate plane. The high transfer efficiency and excellent low-light-level imaging achieved with buried channel CCD arrays confirms the validity of this concept.

3.2.1.2 Experimental Comparison of Surface and Buried-Channel Devices

In order to provide a comparison between the imaging performance of surface and buried-channel devices, units of the CCLID-500A, a 500 element linear imaging device were fabricated with and without a buried-channel in all regions except the on-chip amplifier. The process had earlier been optimized for the buried-channel performance of the on-chip amplifier. By fabricating the surface-channel version in this way, it was possible to operate the amplifier at precisely the same bias levels as were used for the buried-channel version. The surface-channel devices fabricated in this program were judged to be of high quality by all criteria.

Preliminary Testing

Six wafers from the surface-channel wafer-fabrication run were tested for oxide integrity, preamplifier gain, drain current and gate-to-gate leakage. The video response of those devices which passed these tests was monitored when the devices were on the wafer. Devices with poor imaging characteristics were rejected prior

to dicing and bonding. Transfer efficiency was also qualitatively determined. At room temperature and 500 KHz all 30 devices tested showed substantial reduction in transfer efficiency when the average image intensity was reduced below a critical level which ranged from 6% to 50% of saturation.

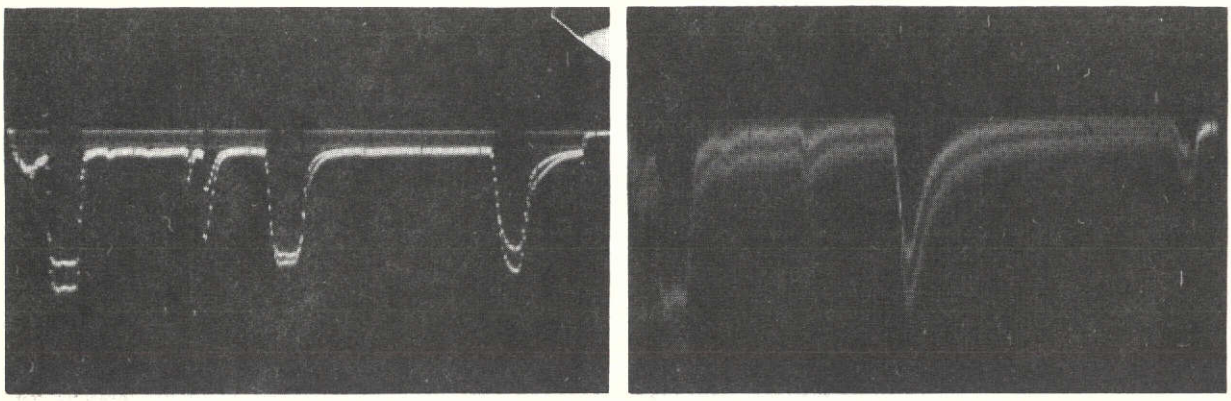
Performance at Room Temperature and at 1 MHz

Figure 3-2 shows the video response of a typical surface and buried channel 500 element CCLID. The test pattern consisted of three white bars in a black field. The test was conducted at an output frequency of 1 Mhz and at room temperature. Photographs (a) and (b), show respectively the response of the surface array at a near-saturation output level and at approximately 6% of saturation output level. Although at the higher light level the image quality of the surface-channel device was at the lower light level, the transfer efficiency became poor. In contrast Figures (c) and (d) indicate high quality imaging and good transfer efficiency for the buried channel device at both saturation and at the same low light level. Transfer efficiency for the buried channel array at low light level is estimated to be in excess of 0.9998.

Performance at Low Temperature and 10 KHz

For these measurements, a surface-channel device was selected which had typical transfer properties and low dark current. The response of the device to a light spot

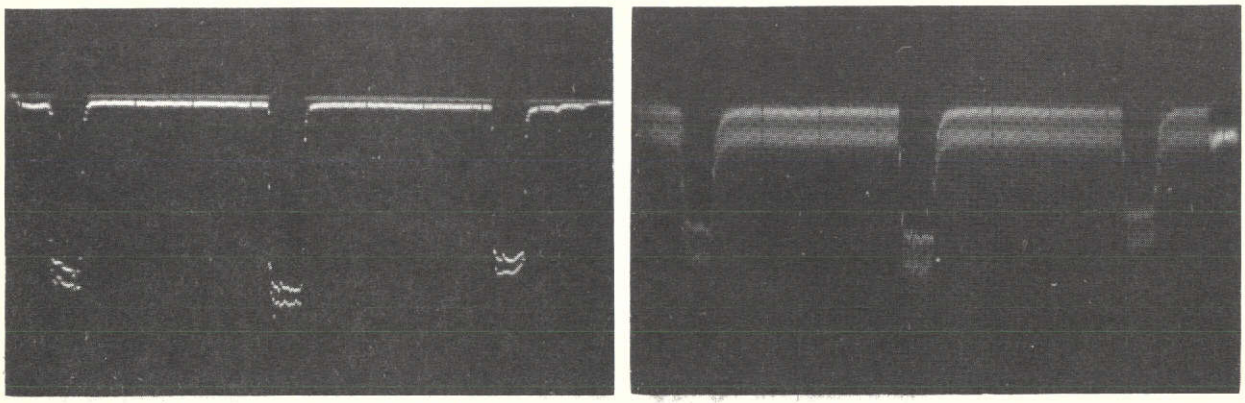
SURFACE CHANNEL



(a)
200 mV/cm

(b)
20 mV/cm

BURIED CHANNEL



(c)
200 mV/cm
Near-Saturation Response

(d)
20 mV/cm
Low-Light-Level Response

FIGURE 3-2 COMPARISON OF SURFACE AND BURIED CHANNEL DEVICE RESPONSE TO DIFFERENT LIGHT LEVELS

50 μs/cm ——————→

imaged onto a single photoelement was measured as a function of temperature at 10 KHz; the magnitude of the trailing pulse was used to calculate transfer efficiency. No "fat zero" was used except that caused by the dark current. Figure 3-3 compares the transfer efficiency of this surface-channel device with the transfer efficiency of a buried-channel device with approximately equal background dark signal.

High transfer efficiency for both the surface-channel device and the buried-channel device was observed at room temperature. On cooling from 25°C to -50°C the transfer efficiency of the surface-channel device dropped by an order of magnitude, whereas that of the buried-channel device increased slightly. This rapid degradation for the surface-channel transfer efficiency was probably caused by a reduction at low temperature of a thermally generated fat-zero dark current.

3.2.2 Photosensitivity and Noise

3.2.2.1 Quantum Efficiency and Responsivity

Charge coupled devices fabricated on single-crystal silicon wafers can have a high quantum efficiency in the visible and near infrared spectral range compared to high performance photocathodes such as the S-20 or the extended-red multialkali surfaces. For example, designs with thin single or double polysilicon gates covering the active area have been fabricated with peak quantum efficiency in excess of 50% in the range 0.5 to 1.1 micrometers.

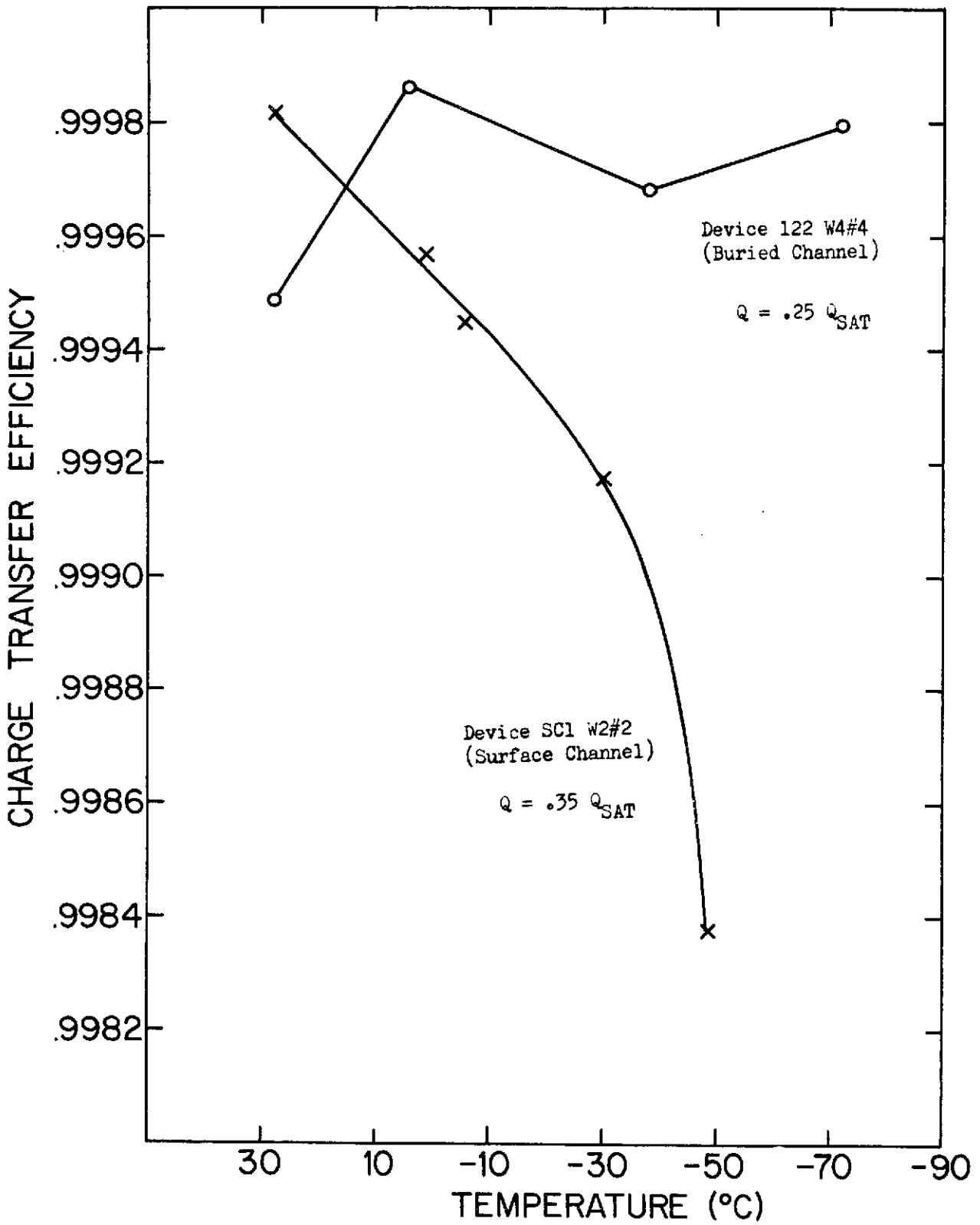


FIGURE 3-3 Temperature Dependence Of Charge Transfer Efficiency For 500 Element CCLID's At 104 HZ

Table 3-1 compares the measured response of a simple silicon p-n junction with the measured and projected response of CCD arrays with one and two layers of polysilicon gates, as well as values projected for polysilicon-silicon dioxide layer structures that are optimized for optical transmission.

Table 3-1

Responsivities to 2854°K Illumination

Device	Measured (A/watt)	Projected (A/watt)
Simple p-n junction	0.13	
CCLID-500A (1-layer polysilicon)	0.10	0.11
CCAID-100A (2-layer polysilicon)	0.068	0.10

3.2.2.2 Noise Sources

The several types of noise in buried-channel CCD's are as follows:

Quantum noise or photoelectron shot noise produces a noise-equivalent signal which is equal to the square root of the signal level.

$$NES_Q = \sqrt{n_s}, \quad n_s = \text{number of signal electrons}$$

Transfer noise is a manifestation of the statistical variation in the amount of charge lost after N_t transfers. If it is assumed that a constant fraction of signal ϵ is lost during each transfer, the total fraction of charge lost is $N_t\epsilon$. The noise equivalent signal is

$$NES_t = N_t\epsilon\ (N_S + B)$$

where B is the background charge introduced by thermal excitation.

Amplifier noise is discussed in Section 3.2.6.

Dark-current noise may be classified as (1) uniform background dark current caused by statistical variation in the number of electrons generated per pixel during a single scan; (2) non-uniform background dark current, i.e., element-to-element variations in the dark current generation rate; and (3) defects which are regions of high dark current. For the purposes of this report, a typical blemish is assumed to be an element with a dark current of greater than ten times the average background.

The two most important sources of uniform background dark current are (1) charge carriers generated in the depletion region at a rate,

$$J_{gd} = \frac{1/2\ n_i W}{\tau_o}$$

τ_o = bulk lifetime
W = depletion width
n_i = intrinsic carrier conc.

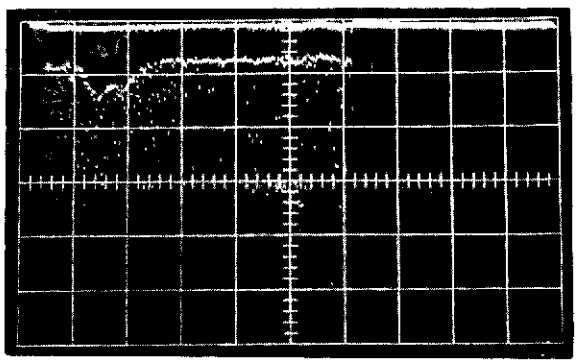
and (2) charge carriers generated at the Si-SiO_2 surface at a rate,

$$J_{gs} = 1/2qn_1S_o, \quad S_o = \text{surface recombination velocity}$$

Given typical measured values of $\tau_o = 0.5$msec, $S_o =$ 1cm/sec and W = 10μm, the total dark current, $J_D =$ $1/2qn_i\left(\frac{W}{\tau} + S_o\right)$, is approximately 3nA/$cm^2$. Some 1 x 500 element linear arrays with dark current densities as low as this have been fabricated. The noise equivalent signal associated with a uniform dark charge of D electrons per pixel can be written.

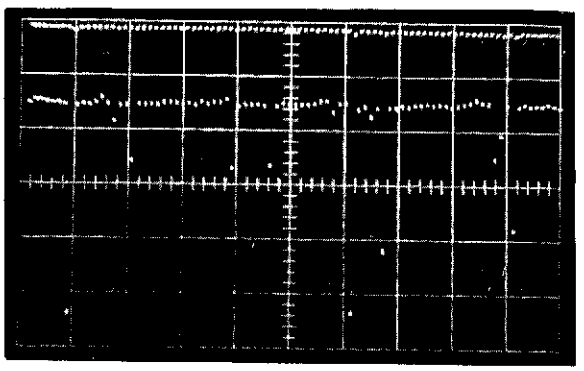
$$NES_D = \sqrt{D}$$

Non-uniform background dark current arises from variations in the amount of dark charge generated from well to well caused by spatial variations in depletion width, sensor area, and generation site density. Non-uniformities of ±5% of the dark charge are typically observed. Figure 3-4 is a photograph of the dark signature of a 1 x 500 linear array, operated at 100KHz with an integration time of 0.5 sec. Photograph (a) shows the full 500 element scan. The following two photographs are expanded portions (100 elements wide) of a noisy region (A) and a quiet region (B) of the video trace. The average dark-current density in region A was approximately 5 nA/cm^2; the average dark current density in region B was approximately 10 nA/cm^2. The mean nonuniformity was estimated to be 1.7% of background in region B, and 17% in region A.



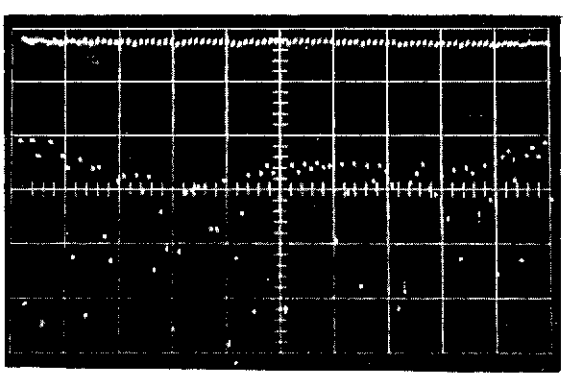
(a) 500-element FULL SCAN

→ 1ms/sq. , 100mV/sq ↑



(b) 100-element AREA A

→ .1ms/sq. 50mV/sq. ↑



(c) 100-element AREA B

→ .1ms/sq. 50 mV/sq. ↑

Figure 3-4 DARK SIGNAL NON-UNIFORMITY AT ROOM TEMPERATURE

Device #127 W1#4, f_o = 100 kHz, t_i = 0.5 sec., V+ = 10.0 V,

V^- = 0 V, V_{PX} = 6 V

Two types of blemish or defect have been observed in 1 x 500 element linear devices: single elements with a high dark signal or spikes, and dark signal bands (10 to 50) elements wide. Although the exact nature of the defect associated with these high dark currents is not well understood, they have been associated with precipitates of metal impurities at dislocations. Processing techniques such as backside gettering have reduced the blemish density of devices to very low values, i.e., less than 10 per 10,000 elements in the 100 x 100 element imaging device.

3.2.2.3 Temperature Dependence of Dark Current in Linear Arrays

The temperature dependence of the uniform dark background signal for five CCLID 500A buried-channel arrays and one surface channel device is plotted in Figure 3-5. Variations in absolute levels are caused in part by different operating frequencies and integration times. The solid line gives the predicted temperature dependence for a linear device with $3nA/cm^2$ dark current density at 24°C. The slope of the semilogarithmic plots give the activation energy associated with the dark charge generation process. For all samples tested, this energy is approximately 0.5 eV in the temperature range 24°C to -40°C. At lower temperatures the apparent activiation energy for some devices decreases.

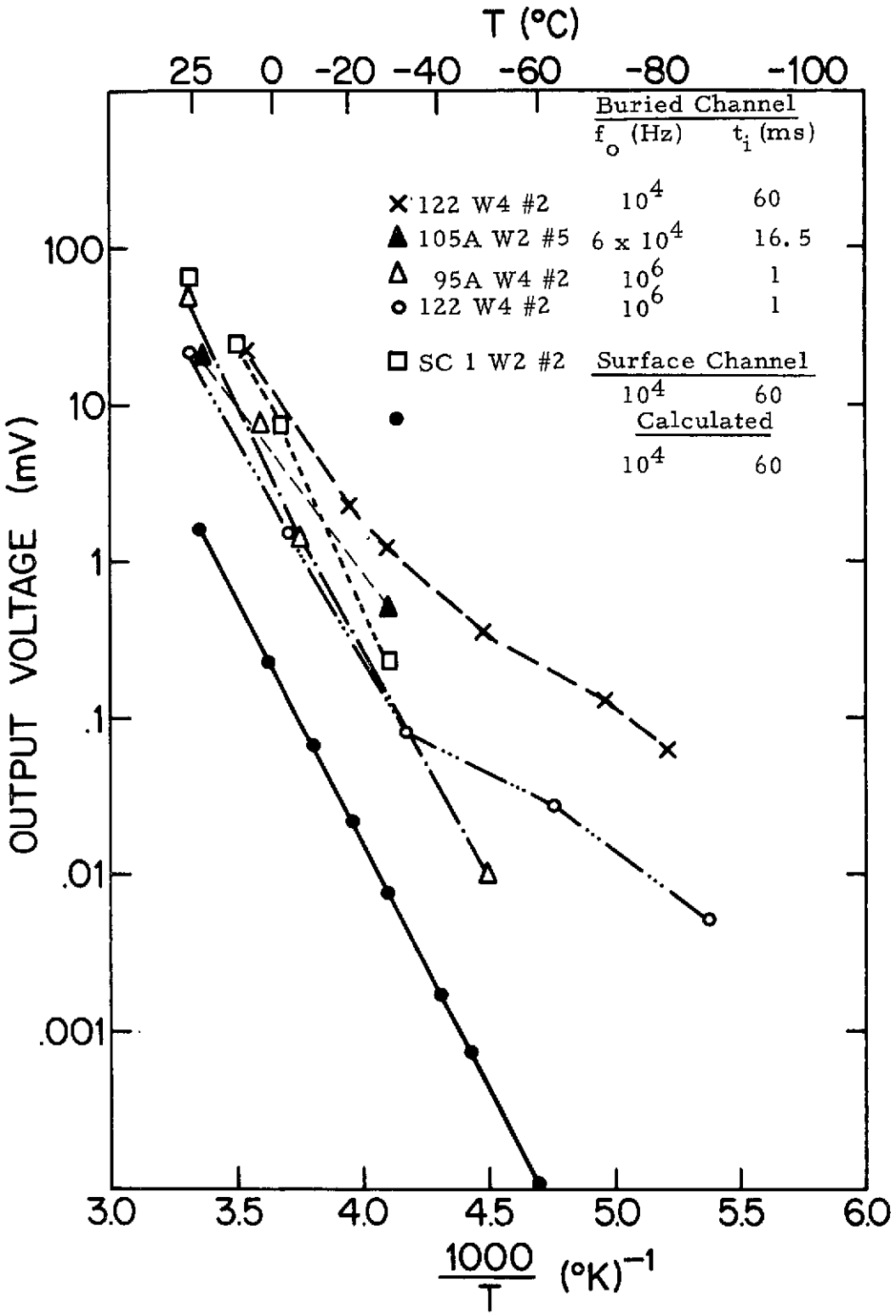


FIG. 3-5 DARK SIGNAL BACKGROUND AS A FUNCTION OF TEMPERATURE

Figure 3-6 shows the temperature dependence of the two background dark current components in a particular CCLID-500A. The background dark current level is considered here to refer to the average dark current excluding occasional high dark-current elements. These components were measured using different integration periods for the photoelements while the register was operated continuously. It may be that the temperature dependence of the photoelement background corresponds to a single activation energy (0.5eV) down to approximately -60°C while that of the register is significantly more gradual below -40°C. The excess register current at the lower temperatures may be a perimeter effect on the device; low temperature measurements on area CCD devices may show a different behavior.

Large dark current non-uniformities such as spikes and bands have been observed to scale with temperature as does the uniform dark current, namely, with a 0.5eV activation energy. This is shown in Figure 3-7 in the temperature range 25°C to -35°C. It can be inferred that the smaller element-to-element dark-current non-uniformity which is difficult to observe at low temperature also scales at the dark charge.

3.2.2.4 Image Quality of an Area Arrays at Low Temperature

A 100 x 100 area imaging device with a large dark-current background was tested at 24°C and -85°C. An image obtained with this sensor was displayed at an output rate of

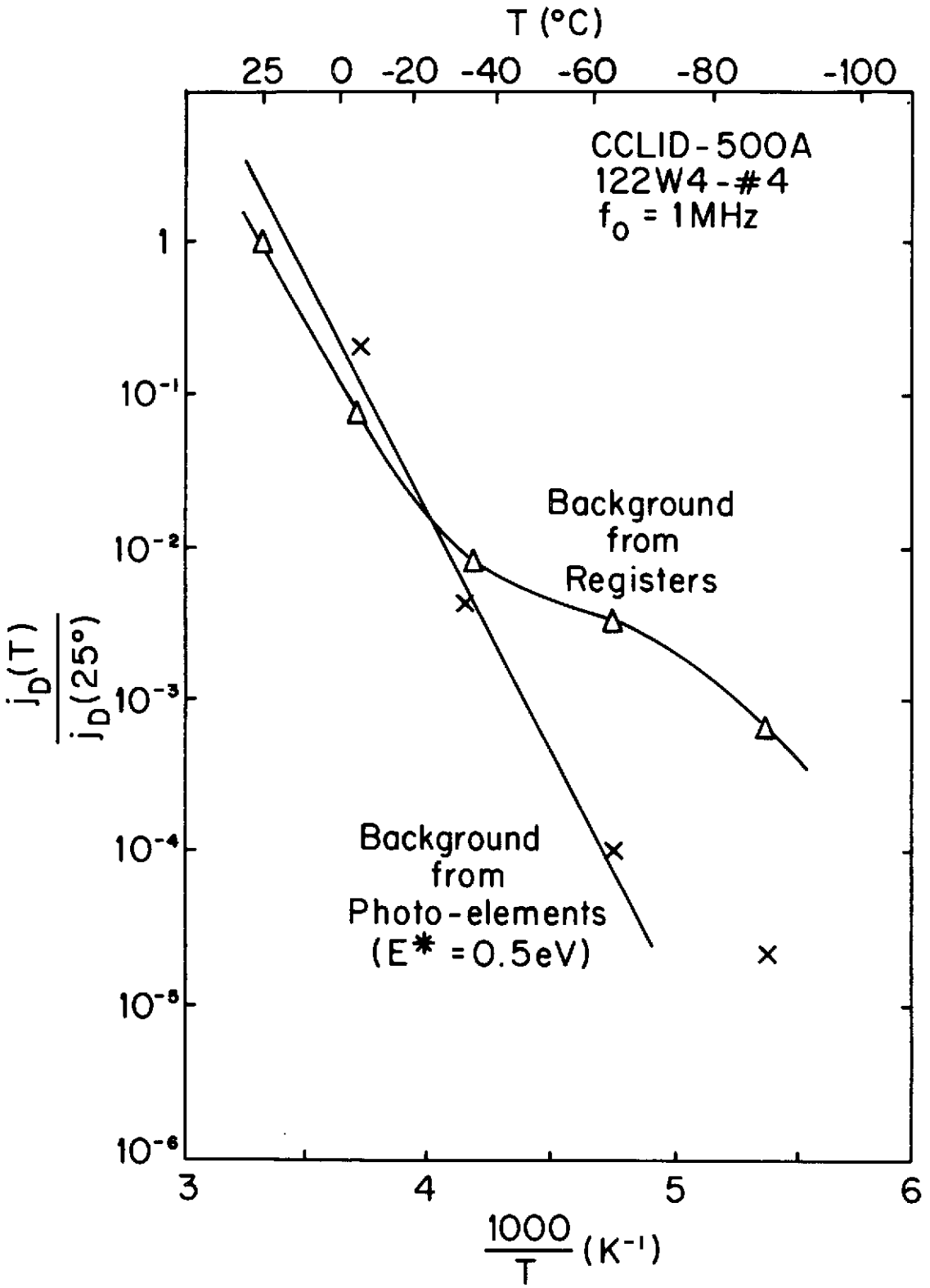


FIGURE 3-6 Temperature Dependence of Dark Current Background Components In The CCLID-500A

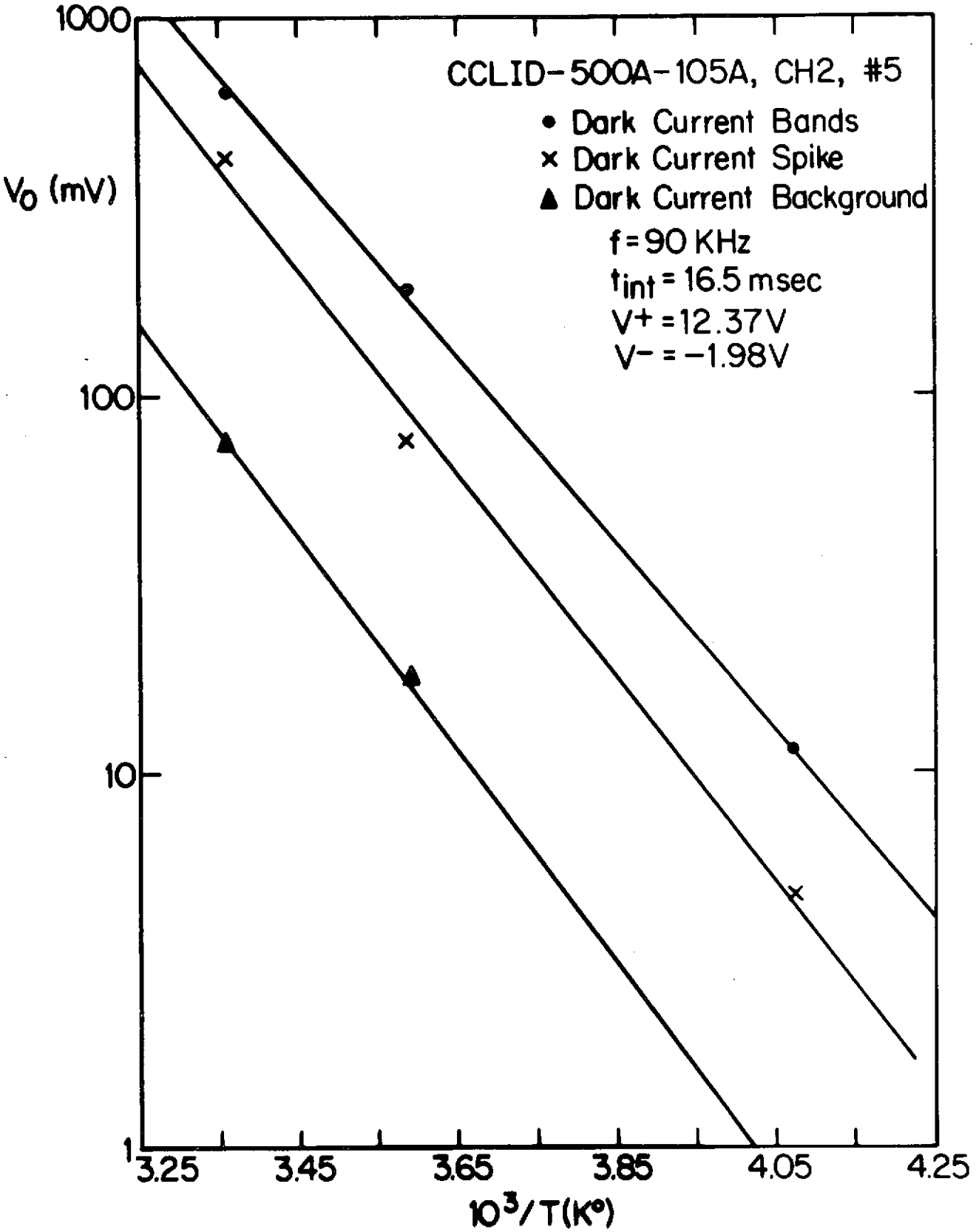


FIGURE 3-7 Temperature Dependence of Dark Current Bands, Spikes and Background

500KHz on a CRT monitor and photographed with high resolution type 107 Polariod film. Photographs thus obtained are shown in Figure 3-8. The highlight level for both photographs was approximately 1/6th of saturation. Approximately 30 dark current spikes greater than 20% of saturation and one vertical streak are present in the displayed image at room temperature. All but two defects disappear at the low temperature and the image quality is improved.

3.2.2.5 Estimated Performance Of A 500 x 500 Element Sensor

Dark current and defect or blemish signals for a buried-channel 500 x 500 element device with geometry and operating conditions that meet JPL requirements are given in Table 3-2 as a function of temperature. The design which is discussed in Section 3.2.4.1 has two polysilicon-layers, implanted barriers and silicon oxide as the gap dielectric which provides the sensor pitch specified by JPL. The room temperature dark-current level density is taken as $J_{D1} = 3nA/cm^2$ and a single photoelement defect is assumed to generate at room temperature a current density $J_{D2} = 30nA/cm^2$. A signal current density $J_S = 0.135nA/cm^2$ was calculated for an irradiance level of 2×10^{-5} watts $/m^2$ (which corresponds to an incident energy of $100\mu J/m^2$ with a 5 sec integration time) using the intrinsic responsivity determined for a double-layer polysilicon 100 x 100 sensor of 0.068 A/watt.

Device 100D3W8#4

f_o = 500kHz

t_i = 25 ms

Highlight Level = 15% of Saturation

24°C

-85°C

FIGURE 3-8 100x100 CCAID Image Quality at Low Temperatures

TABLE 3-2

TEMPERATURE DEPENDENCE OF DARK CURRENT AND S/N FOR A 500 x 500 AID

$A_p = 6.45 \times 10^{-6} cm^2$ $\quad t_{tr} = 25$ sec. $\quad E1 = 100\ \mu J/m^2$

$A_R = 6.45 \times 10^{-6} cm$ $\quad f_o = 10^4$ bits/sec. $\quad H = 2 \times 10^{-5}$ watts/m^2

$p = 25\ \mu m$ $\quad J_{D1} = 3\ nA/cm^2$ (T=300°K) $\quad N_{SAT} = 10^6$ el/bit

$t_i = 5$ sec. $\quad J_{D2} = 30 nA/cm^2$ (T=300°K) $\quad N_S = 2.7 \times 10^4$ el/bit

$J_S = 0.135 nA/cm2$

T(°C)	n_i (cm^{-3})	N_{DP}	N_{DR}	N_{DSP}	NES_D	$J_{DI}(\frac{nA}{cm^2})$	$J_{D2}\frac{nA}{cm^2}$	$\frac{N_{SAT}}{NES_D}$	$\frac{N_s}{NESP}$
25°	1.2×10^{10}	7×10^5	3.5×10^6	6×10^6	2050	30	3	487	13
0°	2×10^9	1.16×10^5	5.8×10^5	1×10^6	834	5.0	0.5	1200	32
-10°	4.5×10^8	2.62×10^4	1.31×10^5	2.25×10^5	396	1.12	0.112	2500	68
-20°	1.5×10^8	8.75×10^3	4.38×10^4	7.5×10^4	229	0.375	3.75×10^{-2}	4367	118
-30°	4.5×10^7	2.62×10^3	1.31×10^4	2.25×10^4	125	0.1125	1.12×10^{-2}	8000	216
-40°	1.15×10^7	7×10^2	3.5×10^3	5700	65	2.85×10^{-2}	2.85×10^{-3}	15,400	402
-50°	2×10^6	1.16×10^2	5.83×10^2	1000	26	5.00×10^{-3}	5.00×10^{-4}	38,500	1,038
-60°	4×10^5	23	116	200	12	1.00×10^{-3}	1.00×10^{-4}	83,300	2,250
-70°	1.1×10^5	6.4	32	55	6	2.75×10^{-4}	2.75×10^{-5}	166,000	4,050
-80°	1.7×10^4	1	5	8.52	2	4.26×10^{-5}	4.26×10^{-6}	500,000	13,500

Glossary for Table 3-2

A_p	Area of photosensor element
A_R	Area of transport register/bit
p	Pitch of array
t_i	Integration time
t_{tr}	Transfer time
f_o	Output frequency
E_l	Incident energy density
H	Irradiance
N_{sat}	Nominal saturation
n_i	Intrinsic carrier concentration
N_{DP}	Dark charge generated during photointegration time per bit
N_{DR}	Dark charge generated during transfer time per bit
N_{DSP}	Dark charge generated at blemish site during photointegration time
N_S	Signal charge per bit for uniform irradiance H
NES_D	Noise equivalent signal $= \sqrt{N_{DP} + N_{DR}}$
J_{D1}	Uniform dark current density
J_{D2}	Current density at the blemish site
JS	Signal current density

A continuous snapshot and scan mode of operation is assumed with a transfer time of 25 sec an integration time of 5 sec and an operating frequency of 10 KHz. A N_{sat} of 10^6 electrons per photosensor was determined by scaling the typical saturation charges observed for linear CCD's to a photosensor area of 6.45×10^{-6} cm^2.

At an operating temperature of -40°C the ratio of the signal charge to the noise equivalent signal attributed to the total dark current and shot noise is 400:1; the dark-current for the defect is a factor of 5 smaller than this signal level. Other noise sources contribute; the temperature dependence of these are shown in Figure 3-9 with the dark current and signal level. An effective total noise equivalent signal may be calculated using the expression,

$$NES = \sqrt{(NES_Q)^2 + (NES_C)^2 + (NES_D)^2 + (\Delta D_{RMS})^2 + (NES_t)^2}$$

At -40°C the values from Figure 3.2.2.3-6 are:

$$NES = \sqrt{27,000 + 28,900 + 4225 + 289 + 5900} = 258 \text{ electrons}$$

The dynamic range can then be written as $\frac{N_{SAT}}{258}$ if the nominal saturation is within a factor of two of the total well capacity of 10^6 electrons. The dynamic range is thus

$$\frac{10^6}{2 \times 258} = 2016$$

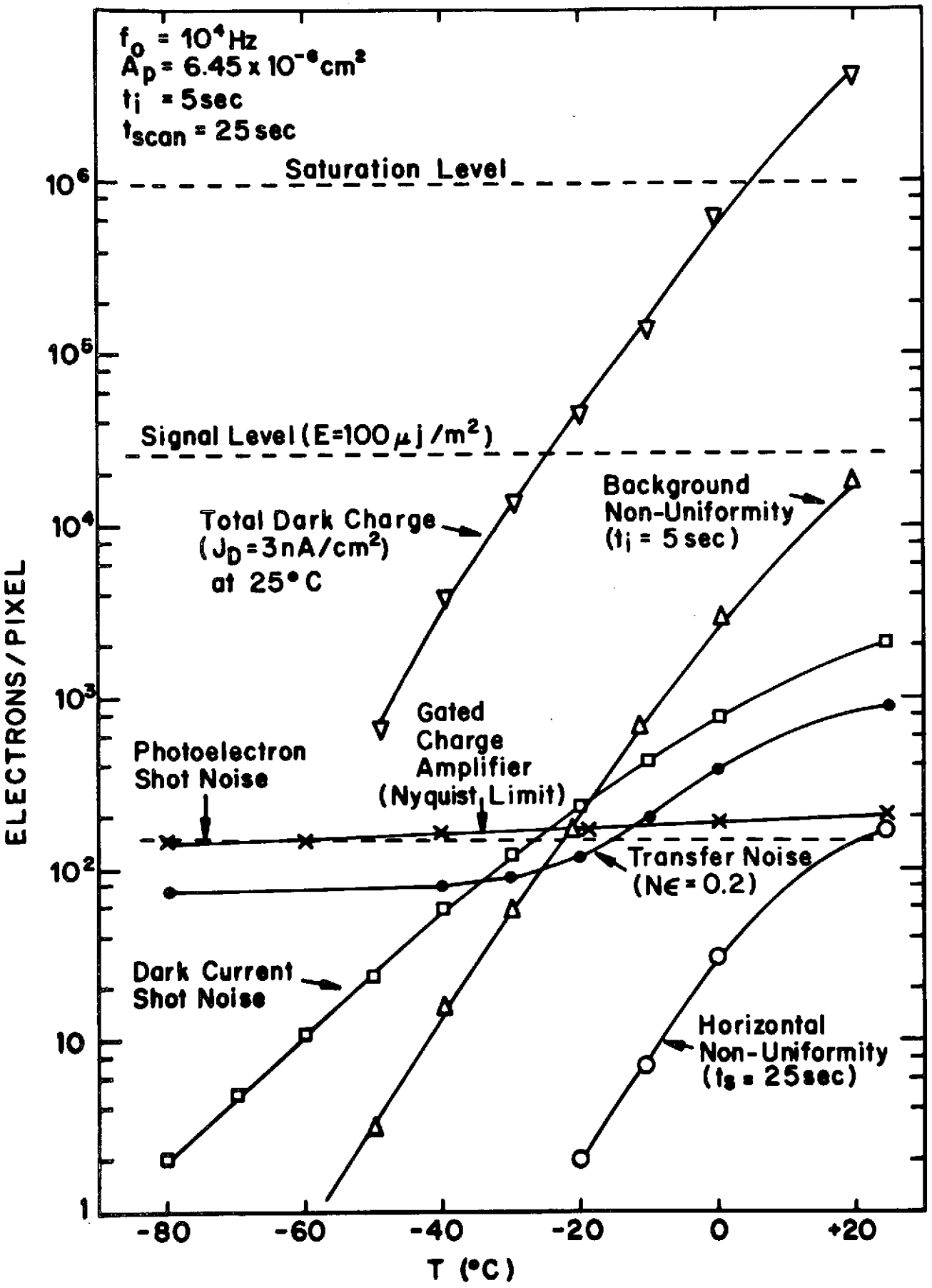


FIGURE 3-9

Calculated Magnitudes of Various Noise Sources Compared to Signal Level, and Saturation Level For a 500X500 CCAID as a Function of Temperature

The signal to noise ratio is $\frac{27000}{258} = 100$ at the specified irradiance level. The largest single noise contribution at this temperature is the gated-charge-integration amplifier noise followed closely by photoelectron shot noise. If a preamplifier such as the distributed floating gate amplifier (DFGA) (discussed in Section 3.2.5) is used, the device is essentially photoelectron shot noise limited, at an illumination level of $100\mu J/m^2$. The proposed 500 x 500 array includes both types of preamplifier.

3.2.3 Charge Transfer Efficiency (CTE)

3.2.3.1 Room Temperature Characteristics of Buried-Channel CCD Registers

Buried-channel CCD registers have the property of high CTE over a large analog signal range without the need of "fat zero" bias current. Data which illustrates this is shown in Figure 3-10. This data was obtained with the CCLID-500A, a linear imaging device with two long 3-phase CCD registers with a limiting charge transfer rate of approximately 1.5×10^6 transfers per second. At a charge transfer rate slightly below this limiting rate, i.e., 7.5×10^5 transfers per second, the transfer efficiency is shown to remain high over a charge-level range of 1000:1.

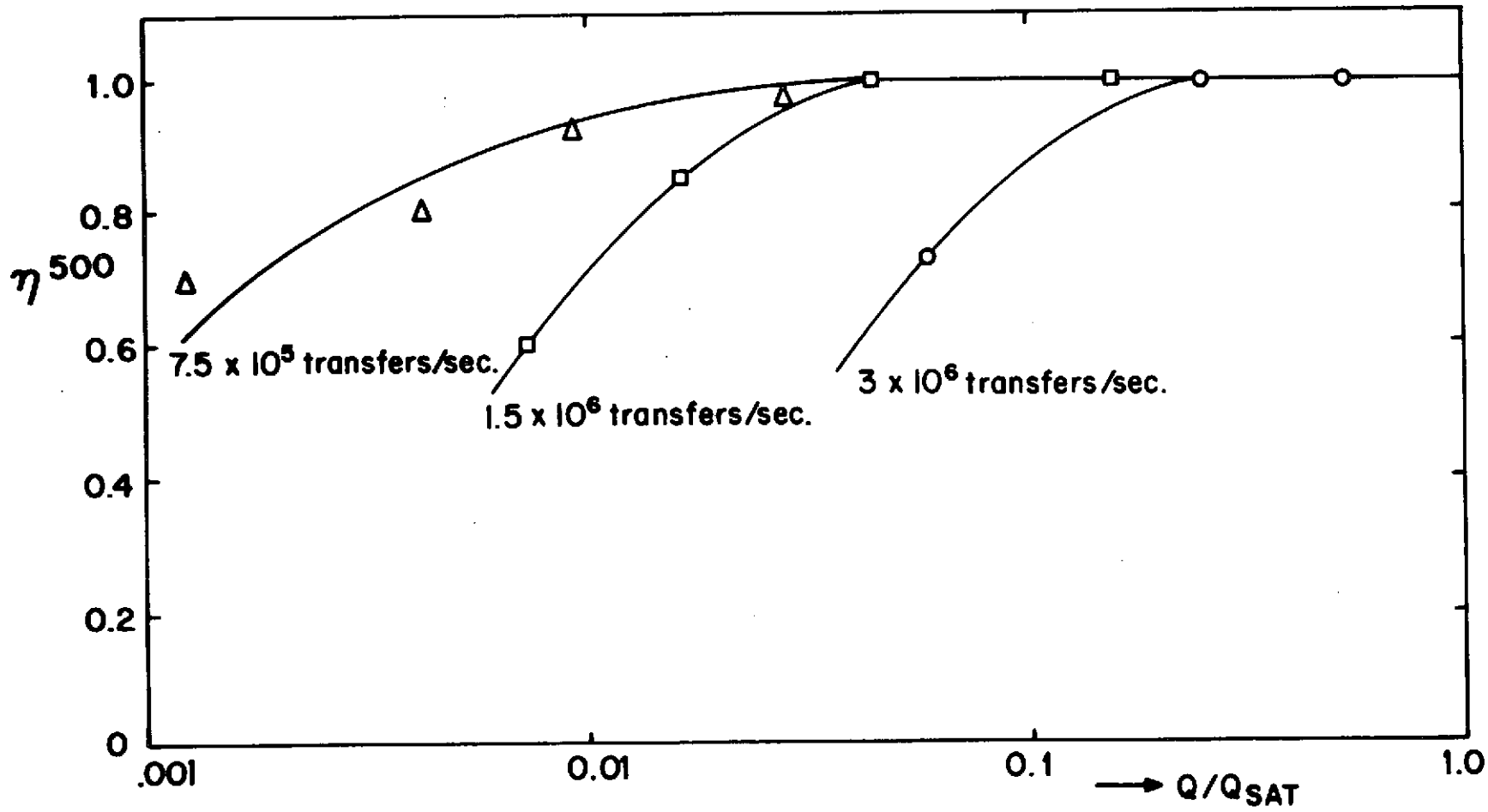


FIGURE 3-10 Transfer Efficiency For Various Charge Levels At Different Frequencies. (The Measurement Was Made On A CCLID-500-A Using A Light Spot.)

3.2.3.2 Low Temperature Characteristics of Buried-Channel CCD Registers

All CTE measurements were made on the CCLID-500A linear imaging device. Although a number of units were tested, time permitted checks on reproducibility of characteristics for only one or two devices. Nevertheless, the results are believed to be representative of the device.

Three methods were used to measure an average transfer efficiency per transfer. These are designated in Table 3-3 as: 1) the trailing pulse method with a dark-current spike, 2) the trailing pulse method with a light spot, and 3) the charge loss method.

Trailing Pulse Methods

Both trailing pulse techniques were substantially the same whether a charge was introduced into a photoelement optically by a light spot or by a localized dark current spike. The amplitude of the principal charge packet, P_m and the amplitude of the next charge packet in the same register, T_1, were measured. The transfer efficiency was calculated using the expression

$$\eta = 1 - \frac{T_1}{P_m N} \quad \text{(N is the number of transfers)}$$

The method gives a low-limit value of η because it includes transfer inefficiency in the output register and at the junction of the two registers.

Charge Loss Method

The charge loss technique is based on the ratio of the amplitude of the initial output pulse when a light spot is focused on an element (N_1) near the front of the array, to the output pulse when the light spot is focused on an element (N_2) at the rear of the array. The CTE is calculated using the expression,

$$\eta = \exp\left[\frac{\ln\left(\frac{PN_1}{PN_2}\right)}{\frac{3}{2}(N_2 - N_1)}\right]$$

Care was taken that the optical response was uniform at the front and rear photoelements; any difference in pulse amplitudes was solely from charge loss during the transfer process. Non-uniformities of response limited the accuracy of this method. The denominator in the exponential, $3/2(N_2-N_1)$, is the difference in the number of transfers for the front and rear charge packets for the 500A devices.

Results

Table 3-3 presents a chronological summary of the low temperature measurements of transfer efficiency for the buried-channel CCLID-500A devices; the last entry shows a comparable surface-channel device result. Throughout this study it was the practice not to change clock voltages as the temperature was reduced from room temperature. In the earlier experiments no optimization of clock decay time-constant was made at lower temperatures; later it became standard practice. No

SUMMARY OF CHARGE TRANSFER EFFICIENCY TESTS BELOW 25°C

TABLE 3-3

Device	Frequency (Hz)	Optimization Temperature (°C)	Temperature Range (High)	(Low)	Type of Measurement	Sign of Transfer Efficiency (Temperature Coefficient)	Transfer Efficiency Range
105BW #1	5.4×10^4	24.5°	24.5°C	to -50°C	(1)	Positive (no adjustment of spike amplitude)	.99989 - .99959
93AW2 #20	3.3×10	30°	30°C	to -26°C	(1)	Negative (spike amplitude constant)	.99959 - .99984
111AW4#11	1.2×10^6	25°	25°C	to -10°C	(2)	Positive	.995 - .989
	2.6×10^5	25°	25°C	to -10°C	(2)	Negative	.992 - .9982
95W4 #2	10^6	25°	25°C	to -6°C	(2)	~0	.999948 - .999948
			25°C		(3)		.99979
122W4 #4	10^6	All	28°C	to -96°C	(2)	Negative	.99972 - .999982
		All	28°C	to -96°C	(3)	Negative	.9984 - .99992
122W4 #4+	10^4	All	24°C	to -72°C	(2)	~0	.99948 - .99986
		All	24°C	to -72°C	(3)	~0	.9988 - .9990
122W4 #2	10^4	All	-15°C	to -56°C	(2)	~0	.99957 - .99964
	10^4	All	-24°C	to -50°C	(3)	~0	.9990 - .9985
	2.3×10^5	All	-15°C	to -50°C	(2)	Negative	.9985 - .99938
SC1W1 #2	10^4	All	28°C	to -50°C	(2)	Positive	.99949 - .9984
(Surface Channel)					(3)	Positive	.99980 - .9981

(1) Trailing pulse calculation using dark current spike.
(2) Trailing pulse calculation using light spot.
(3) Charge loss method.

performance penalty was paid when this adjustment was made. Therefore the best results were obtained on devices 122W4-#2 and #4 where optimization was performed at each temperature. Once optimization was done at the lowest temperature for a given device, re-optimization at subsequent higher temperatures proved unncessary. In general only a small adjustment was needed.

All quantitative results are for primary pulse heights 10 to 80% of saturation. The major effects observed may be summarized as follows:

1. With optimization at each temperature, the transfer inefficiency at 10kHz varies by less than a factor of two over the temperature range +25° C to -50° C.
2. With optimization at each temperature, the transfer inefficiency at 1MHz characteristically improves by a factor of five to ten on cooling from +25° C to -96° C.
3. Both the total transfer inefficiency and the trailing pulse transfer inefficiency measurements tend to have the same temperature dependence.

In addition to these quantitative results, qualitative observations were made for primary pulse heights in the range 1 to 10% of saturation. These observations are tentatively summarized as follows:

1. Trailing pulse trains cannot be characterized by a single inefficiency parameter, i.e., the tail of the pulse train is more elongated than expected.
2. The magnitude and relative pulse height of the trailing pulse trains do not change markedly over the temperature range investigated.

Measurement of charge transfer efficiency as a function of temperature for linear devices with doped-undoped polysilicon gate structures indicate that no reduction in resolution at low temperatures caused by transfer efficiency degradation is expected. However, operating conditions necessary to obtain the best transfer efficiency may change with temperature.

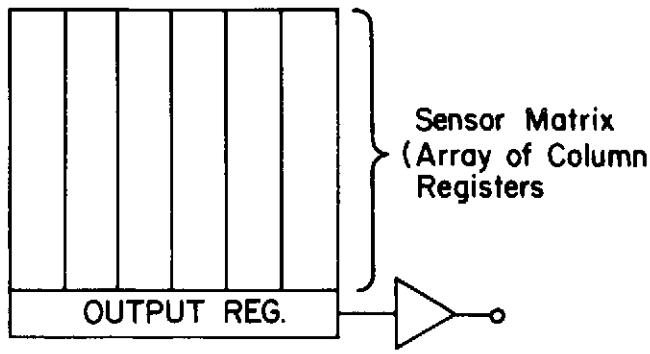
Significant differences have been found between total transfer inefficiencies and trailing pulse measurements. This suggests that it may be more difficult than originally believed to relate transfer inefficiency to degradation of imaging resolution, i.e., to effects on MTF.

3.2.4 Optimum Configuration of An Area CCD Sensor

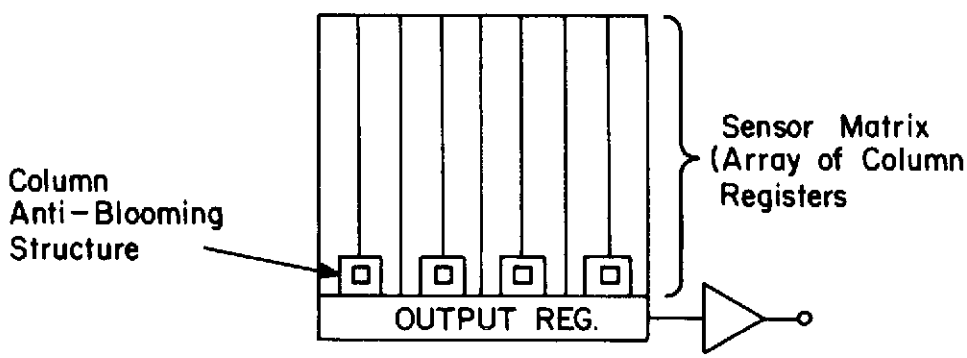
3.2.4.1 "Conceptually Simplest" Area Sensor For The JPL Requirement

Conceptually, the simplest type of CCD array configuration for the JPL requirement consists of (1) a sensor matrix made up of an array of vertical CCD registers, and (2) an opaque horizontal output register. This configuration is shown in Figure 3-11. Because of the use of a mechanical shutter and because the basic JPL guideline does not specify a sensing capability during the readout period of the previous frame, there is no requirement for either a sensor matrix separate from a transfer register or a buffer store.

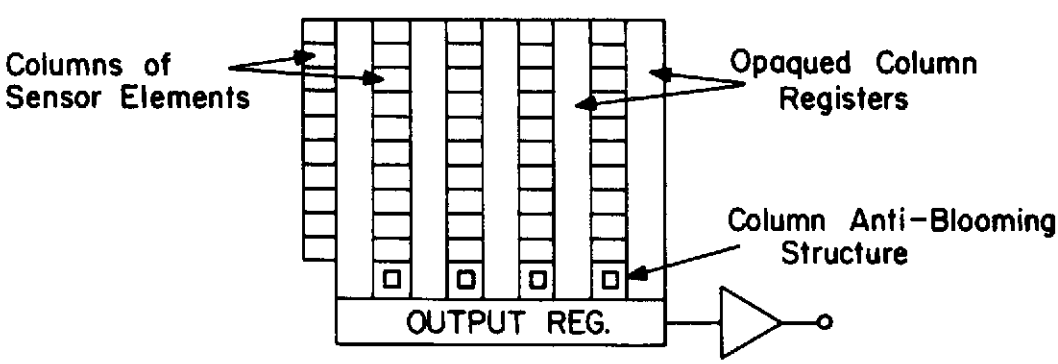
Even though design details are primarily treated in other sections of this report, it is of interest to consider various details here in order to focus on key-problem areas in the over-all design. One attractive structural approach for this "conceptually simplest" configuration is to form all the CCD gates in one plane of poly-silicon, much as is done in other Fairchild CCD imaging devices, i.e., the CCLID-500A and the CCAID-100B. This is attractive because it avoids the need for a second layer of poly-silicon and because high performance, top-side illumination, imaging is obtained. A problem with a single-layer poly-silicon design is that it is difficult to achieve the desired element pitch of 25 micrometers because, for fabrication simplicity, a three-phase construction is preferred over the two-phase, implanted barrier



(a) CONCEPTUALLY SIMPLEST JPL CONFIGURATION



(b) CONFIGURATION OF (a) ABOVE WITH COLUMN ANTI-BLOOMING



(c) INTERLINE TRANSFER CONFIGURATION

FIGURE 3-11 Area Imaging Device Configurations

construction. The minimum pitch of a three-phase design in the JPL case is of the order of 42 micrometers, i.e., 7 micron gates and 7 micron gaps.

The 7 μm gap dimension is determined by the non-linear, resistive characteristics of the undoped poly-silicon. If the gap is less than 7 μm, at typical voltage drops between gates the high-field conductivity of the undoped poly-silicon can become so high that substantial power dissipation occurs. The nature of this high-field conductivity is shown in Figure 3-12.

From this figure it can be seen, for example, that a half-inch wide 500 x 500 element matrix with 3-phase gates, which is operated at room temperature with a 10 volt clock amplitude, is predicted to have typically a gate-to-gate leakage current of 3 mA with 7.5 μm gaps or 8 mA with 5.0 μm gaps. When cooled to -20°C and again operated at a clock amplitude of 10 volts, the corresponding leakage currents are 0.8 mA and 5 mA, respectively. It is significant to compare the on-chip power dissipation caused by this leakage to the only other major source of power dissipation, the preamplifier. This is projected to be approximately 10 to 30 mW for any of the preamplifiers under consideration. Table 3-4 shows the power dissipation caused by leakage in the undoped poly-silicon for several different cases. Only when the wider gaps are incorporated and when the device is cooled, can this power dissipation be made less than that in the preamplifier.

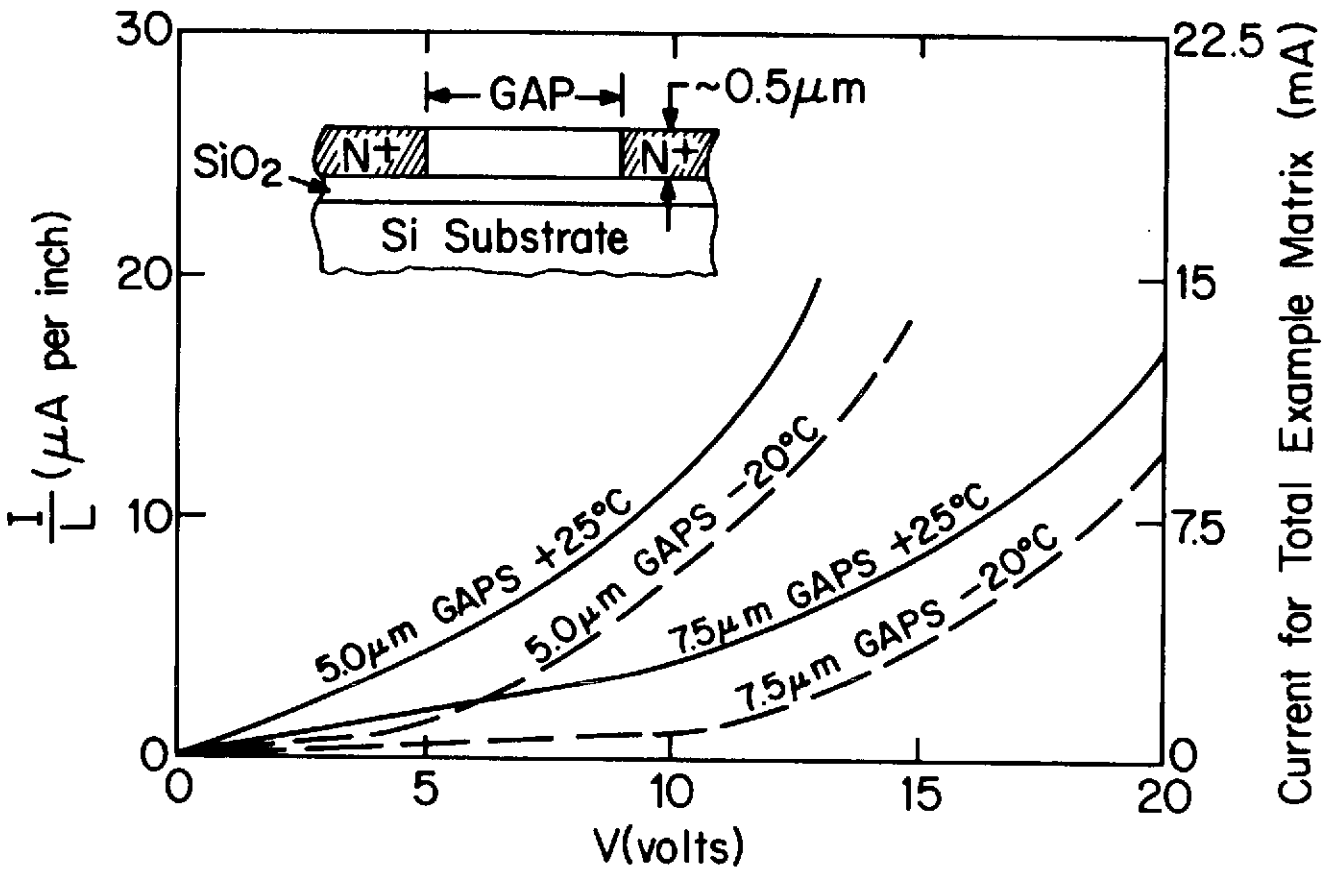


FIGURE 3-12 Typical gate-to-gate leakage current in undoped poly-silicon films. The 7.5 μm gap data was taken on the CCAID-100A imaging device. The 5.0 μm gap data was taken on the CCLID-500B imaging device. The gap dimensions are for the masks; final dimensions are somewhat smaller. The example matrix considered here is a 3-phase, 500-vertical-bit, half-inch wide matrix.

TABLE 3-4

Power Dissipation in a 500 x 500 Element, 0.5" Wide Matrix Due to Current Leakage in the Undoped Poly-Silicon

Condition: Clock amplitude = 10 v.

Gap width	5.0 μm	7.5 μm
3-phase array		
+25°C	80 mW	30 mW
-20°C	50 mW	8 mW
2-phase array		
+25°C	53 mW	20 mW
-20°C	33 mW	5 mW

Next, designs of the "conceptually simplest" configuration which require two layers of poly-silicon for their fabrication may be considered. Both two-phase and three-phase designs are considered here. The two-phase design incorporates self-aligned implanted barriers. The barriers are formed by ion implantation of acceptors into the n-type layer of the buried channel structure after masking of the first poly-silicon layer and before deposition of the second poly-silicon layer; no implantation mask is required. The three-phase design incorporates alternating first and second layer poly-silicon gates for any given clock phase of the structure. The three-phase design process is slightly simpler in that a barrier implantation is not required. The two-phase design, however, requires fewer clocks and probably its operation is less critical with respect to driving waveform, i.e., the clock decay times are probably less critical. These considerations make the two-phase device preferrable.

In operation, this configuration requires an external shutter so that it can be scanned in darkness. The preferred 2-phase embodiment of this configuration can be scanned more rapidly in the standby period thus minimizing dark signal in the slower signal read-out scan.

Figure 3-11 shows schematically how a column anti-anti-blooming structure may be incorporated in this configuration. For a detailed discussion of this structure see Section 3.2.7.

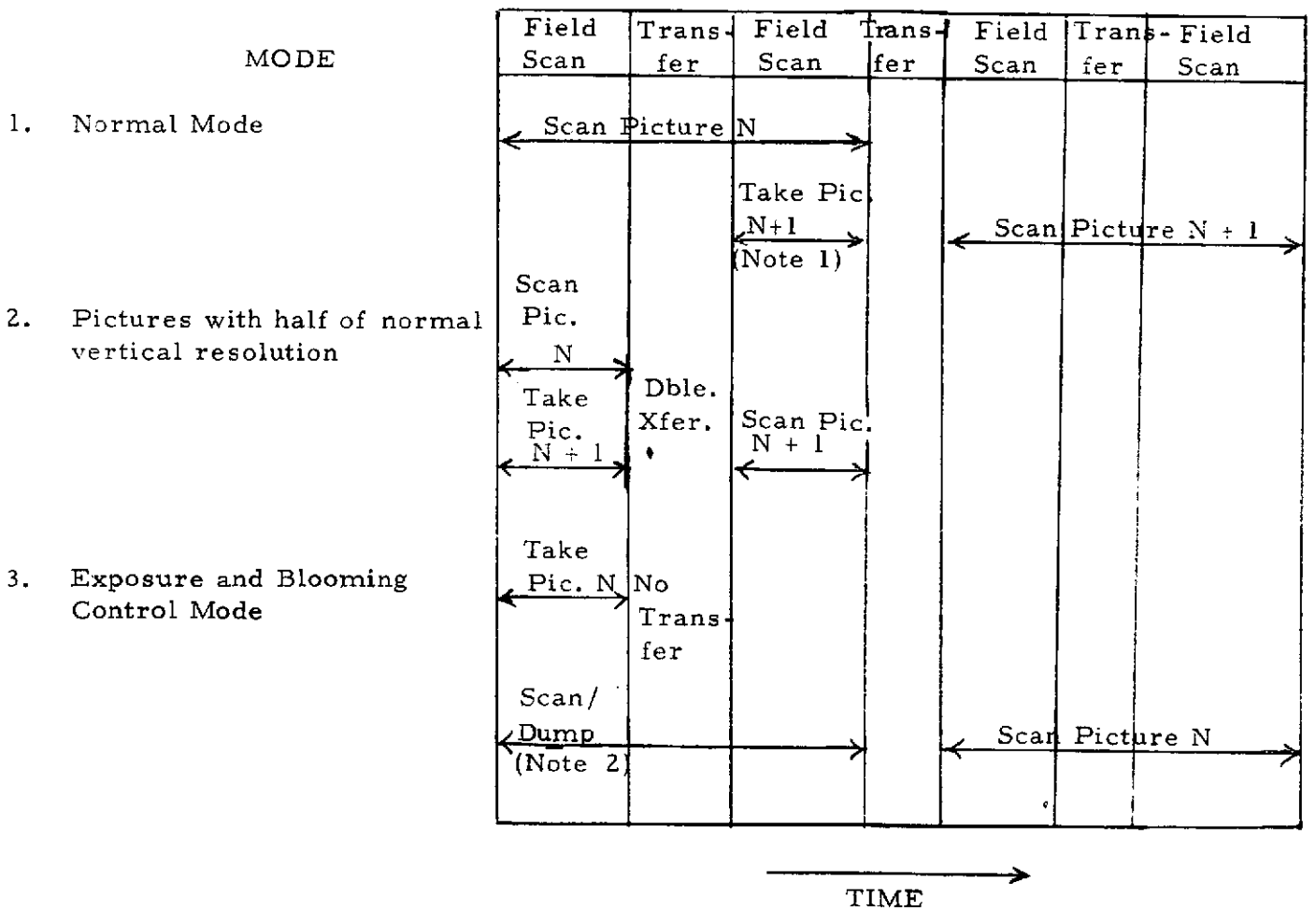
3.2.4.2 Interline-Transfer Configuration

Figure 3-11 (c) shows schematically the interline-transfer configuration, which is comprised of inter-digitated colums of sensors and column registers together with an output register. Figure 3-13 is a photograph of a device of this configuration, the 100 x 100 element CCAID-100A. Figure 3-14 shows the mask design in the region of the output circuitry. It depicts two sensor elements where the vertical stripe ϕ_F crosses (under) the horizontal stripes ϕ_{V1} and ϕ_{V2}. Adjacent to these sensors are the associated well-sites of column registers. A major feature of this configuration is that a pair of sensor elements share one stage of a column register. One sensor element of the pair is first read out in one field; the other is read out in a second field. The two fields are interlaced at the display. This organization results in a design capable of twice the vertical packing density of sensor elements compared to simpler designs.

An operational feature of this design is that one picture may be taken while part of the previous picture is being scanned out. In fact, several interesting modes of operation are possible. These are listed in Table 3-5 The third mode listed in the table is of interest for two reasons. First, it offers full element-by-element blooming control. If, for example, a 500 x 500 element array is scanned at its maximum scanning rate, which may be approximately 60 vertical scans per second, and

TABLE 3-5

Modes of Operation of the Interline Transfer Configuration



NOTE 1: Picture N+1 could just as easily be taken at a later time provided that dark current is transferred and scanned out of the array in the standby period.

NOTE 2: The scan/dump operation can be performed to advantage at a much increased frequency.

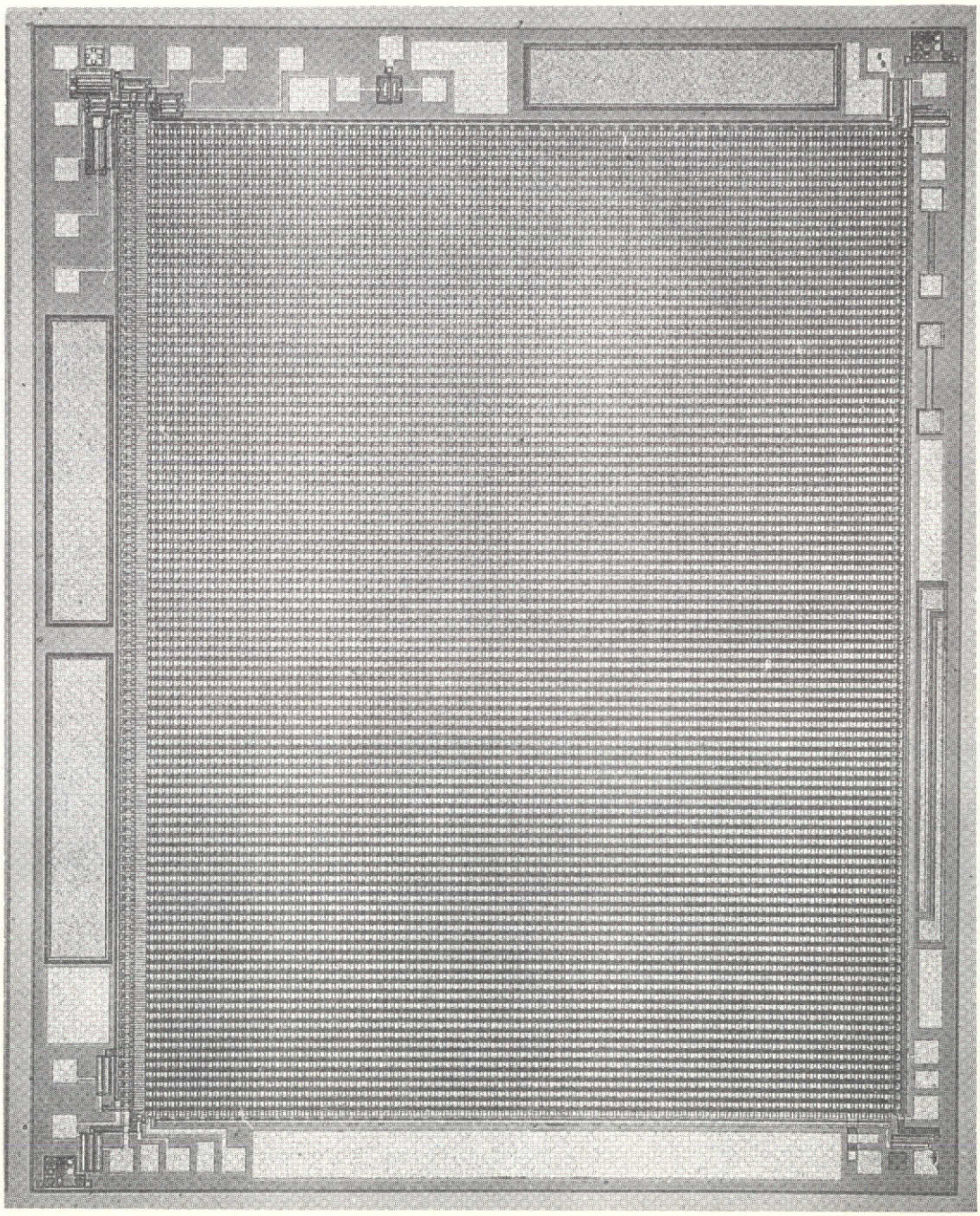


FIG. 3-13 Photo of the CCAID-100B. This is a 100 x 100 element version of the interline transfer configuration.

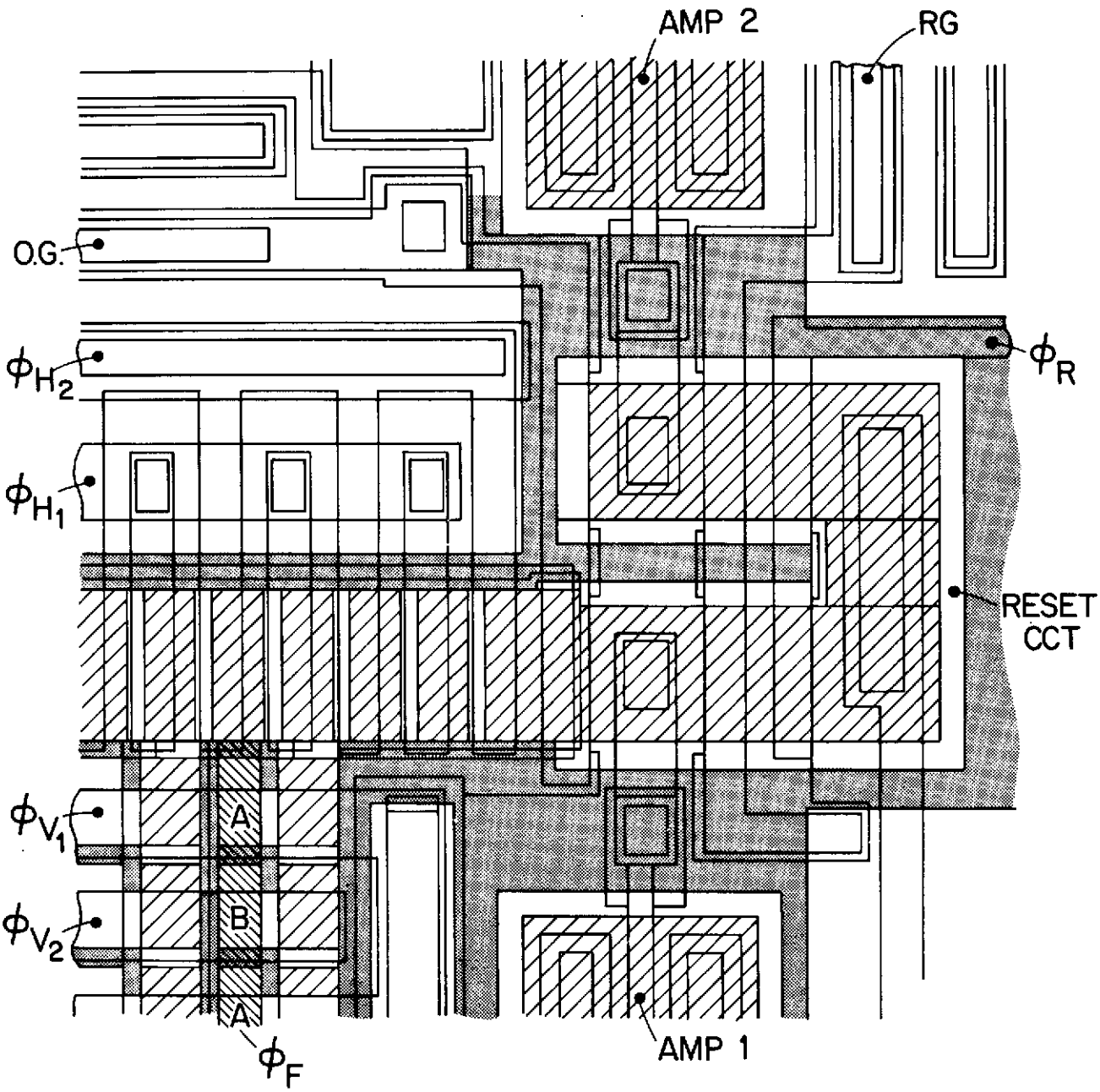


FIGURE 3-14 Mask drawings of the CCAID-100B in the region of the output circuitry

if the exposure time is of the order of 5 seconds, the array would have a 300-fold overload capability as a worst case; it would be capable of commencing the image read-out cycle in 1/60 second after the end of the exposure. Secondly, this third mode of operation allows the possibility of exposure control in the camera system. By scanning the array at its maximum rate of the order of 60 vertical scans per second, the onset of saturation at any small region of the picture can be sensed at the output in no more than 1/60 second.

3.2.4.3 Multichip Butted Mosaics

Very large linear and area image sensors can conceivably be fabricated in mosaic fashion with two or more sensor chips. Such mosaic sensors can in turn be of two types: (1) where optical techniques are incorporated to break up the image into the necessary number of portions; (2) where the chips and the mosaic are designed so that optical partitioning is not required. This section treats the latter type of mosaic sensors.

An example of an area image sensor made up of more than one chip would be a 2 x 2 mosaic of four 500 x 500 element sources. In the JPL type of application the scanning directions need not, in general, have a particular interrelationship. Thus a configuration such as that in Figure 3-15 can be employed. This configuration makes use of four identical chips of a design which is basically that shown in Figure 3.11 (a). Two sides of the active sensor

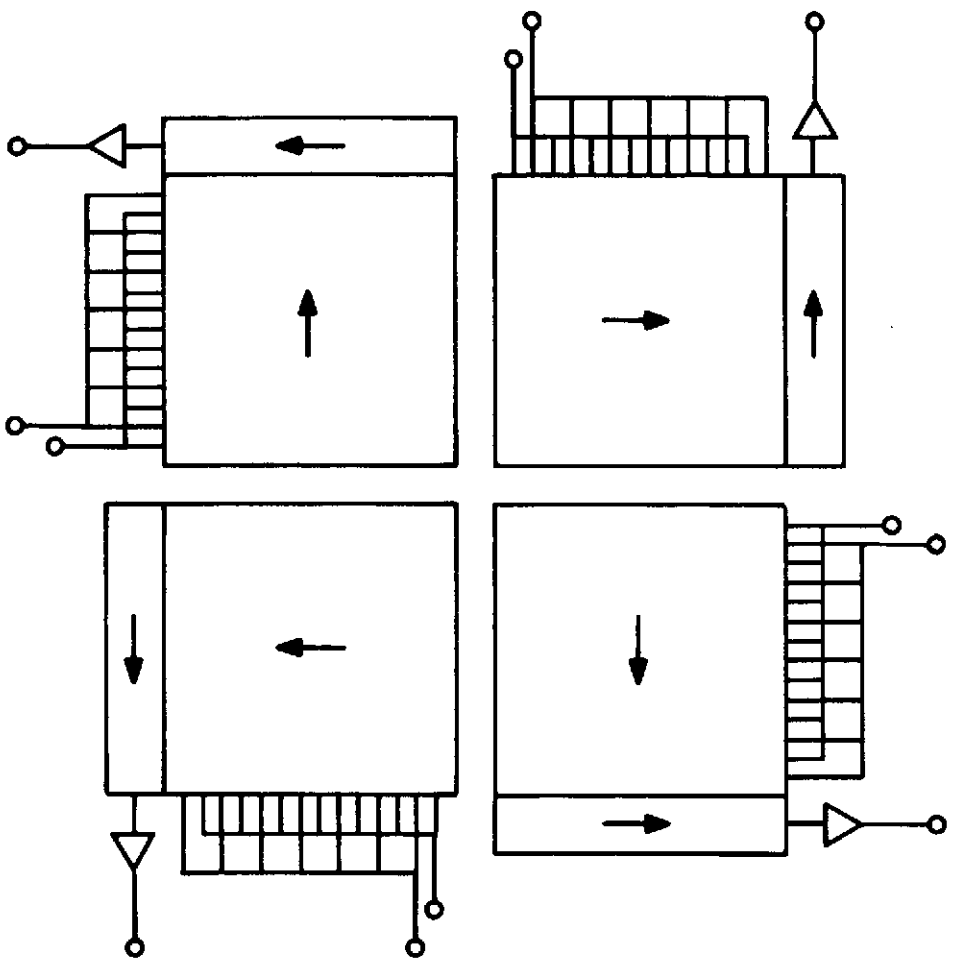


Fig. 3-15 A 1000 x 1000 element butted mosaic image sensor composed of four identical 500 x 500 element chips. The different readout directions are indicated by arrows.

area of a given chip are used for the output register and the gate drive leads. Since the other two sides require no output structures, these edges of the chip can be set as close as a few micrometers from the photosensing area. Standard integrated circuit practice, however, requires a margin of at least 50 μm for standard scribing and breaking procedures. Using refined micromachining methods, this margin can be held to approximately 10μm.

Dark current specifications and photoresponse uniformity specifications ultimately determine specification of the margin and the side-walls of the chip. These parameters are related through the variables of optical refraction and scattering at the micromachined edges, and the surface-recombination velocity.

Placement of the four chips with respect to each other can be determined either by putting them in direct contact with each other or by aligning the sensor areas to each other to predetermined dimensions. In the latter case, experience in our laboratory has shown that it is practical to align large sensor arrays to a precision of approximately ± 5 μm with the proper mechanical jigging.

For all but the most exotic optical systems it is satisfactory to have the planarity of the mosaic held to ± 25 μm or better. This precision is feasible with proper care in assembly.

3.2.4.4 Frontside versus Backside Illumination

Comparison of frontside and backside illumination device designs can be made in various ways. Basically, the problem is to appraise the differences in spectral responsivity and spectral MTF, and to compare this appraisal with factors affecting manufacturability. These factors are primarily the large die size and the thinning process required for the backside illumination option.

Both designs suffer from reduced blue responsivity. For frontside illumination the loss is primarily a function of the polysilicon layer thickness as well as the thicknesses and refractive indices of the adjacent layers. For the low frequency JPL application, the polysilicon layer thickness is not determined by the internal relaxation time requirements on the gate structure but rather on how thin a layer can practically be fabricated. Thicknesses down to 0.15 μm have been incorporated successfully in CCD structures; a significant further reduction is possible. Both silicon dioxide (n = 1.47) and silicon nitride (n = 1.9) are available as dielectric film materials in the design. Loss of blue responsivity for backside illumination is caused by the inherent high surface-recombination velocity of the back surface and the finite thickness of the built-in-field region which generally is required.

With regard to the effect of backside thinning on the size of the die, an unthinned border of at least 50 mils is probably required for reinforcement, and an allowance of an extra 50 mils is probably required for the transition

from one thickness to the other to give a total border of at least 100 mils. From these considerations it can be shown that for a 500 x 500 element device one cannot have more than two patterns on a two-inch wafer. In contrast, a topside illuminated structure with a die size of 500 x 500 mils to 600 x 600 mils allows four to six patterns on a two-inch wafer.

Additional discussion of the optical properties of frontside illuminated CCD structures appears in Section 3.2.6.1.

3.2.5 On-Chip Detector-Preamplifiers

There are three amplifier configurations which will be used in the proposed design: the gated-charge integrator, the floating-gate amplifier (FGA), and the distributed floating-gate amplifier (DFGA). Any one of the these may be employed; the choice of amplifier depends on the light level of the image to be sensed.

The gated-charge integrator uses a CCD output diode as the gated-charge integrator. In this mode, the diode is charged to some fixed value of reverse voltage by a reset MOSFET during a time when no signal is being transferred from the register. The reset switch is then opened, which allows the output diode to function as a charge-storage detector for minority (signal-charge) carriers. At the next transfer, the signal charge is thus stored on the equivalent diode capacitor, which results in a corresponding change in the voltage across the diode.

The noise limitations of the simple gated-charge integrator are twofold. First, from a practical standpoint, the output is subject to a strong component of coherent noise from the reset transistor gate. This noise consists of a feed-through of the reset pulse to the output through the gate-to-source capacitance C_{GS} of the reset switch. The magnitude of this feedthrough is proportional to the amplitude of the reset pulse and the ratio of C_{GS} to the output capacitance.

Since the CCD output diode capacitance is intentionally made as small as possible, the coherent reset noise may, therefore, be comparable to the maximum output signal. Although this noise does not limit S/N in the strictest theoretical sense, it nevertheless adds to the complexity of the signal processing task and hence is undesirable. Use of a differential amplifier can reduce this component of amplifier noise.

The second and more fundamental limitation of this technique arises from the mixing which occurs between the signal of interest and the majority carrier population of the sensing diffusion. This mixing leads to transfer noise in connection with the discharging (or resetting) of the sensing diffusion. Stated briefly, the consequences of these contaminating effects are: 1) a limit on the precision to which the voltage of the sensing region can be set, and 2) a randomness in the resetting process.

The noise-limited signal detection levels for the gated-charge-integrator structures are a strong function of the

complexity of signal processing equipment external to the CCD device itself. Detection limits with simple external circuitry are estimated at approximately 250 signal electrons; with complex external circuitry this can possibly be reduced by a factor of 5.

The floating gate amplifier, shown conceptually in Figure 3-16 is a device which fully exploits and conserves the low-noise characteristics of the CCD channel. In operation the charge to be sensed is brought under the floating gate by manipulation of the potentials of adjacent charge-coupling electrodes. This signal charge electrostatically produces a change of potential on the floating gate. It may be noted that the floating gate provides a capacitive coupling between the signal electrons in the CCD channel and the channel current of the MOS transistor without physically making contact to either of them; the signal electrons remain isolated even after detection.

The floating gate amplifier provides a much more sensitive technique for charge detection than the previously discussed gated-charge integrator. Using the FGA, it is estimated that detection limits in the range of 20 to 50 electrons are possible.

The signal electrons in a CCD channel are seen to remain isolated after they have been detected by an FGA. They can, however, be moved downstream and detected repeatedly by other FGA's. This leads to the concept of the DFGA, shown in Figure 3-17. For an N stage DFGA, the signal power is amplified by a factor of N^2 from that of a single

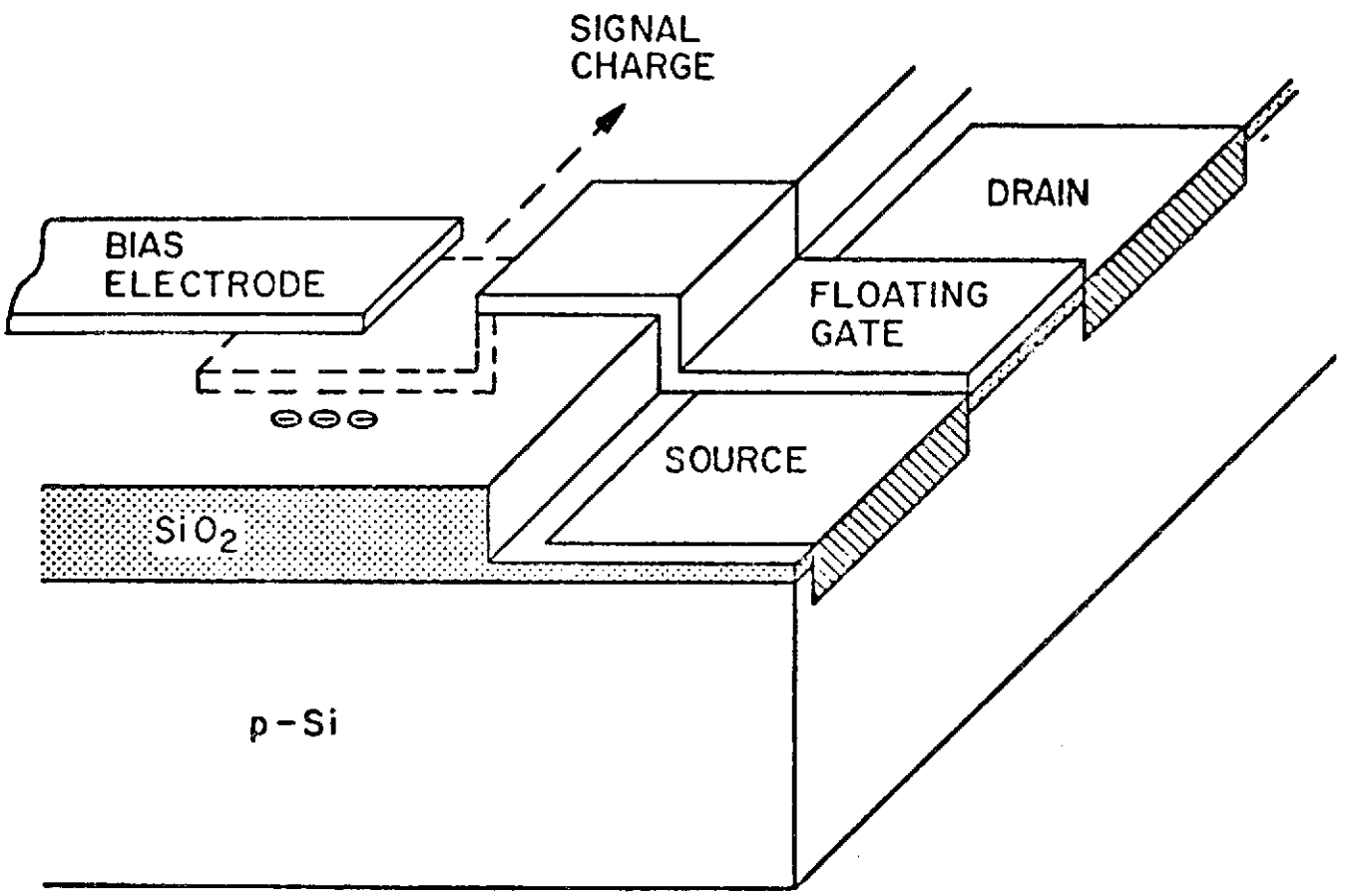


FIGURE 3-16 Single Stage Floating Gate Amplifier

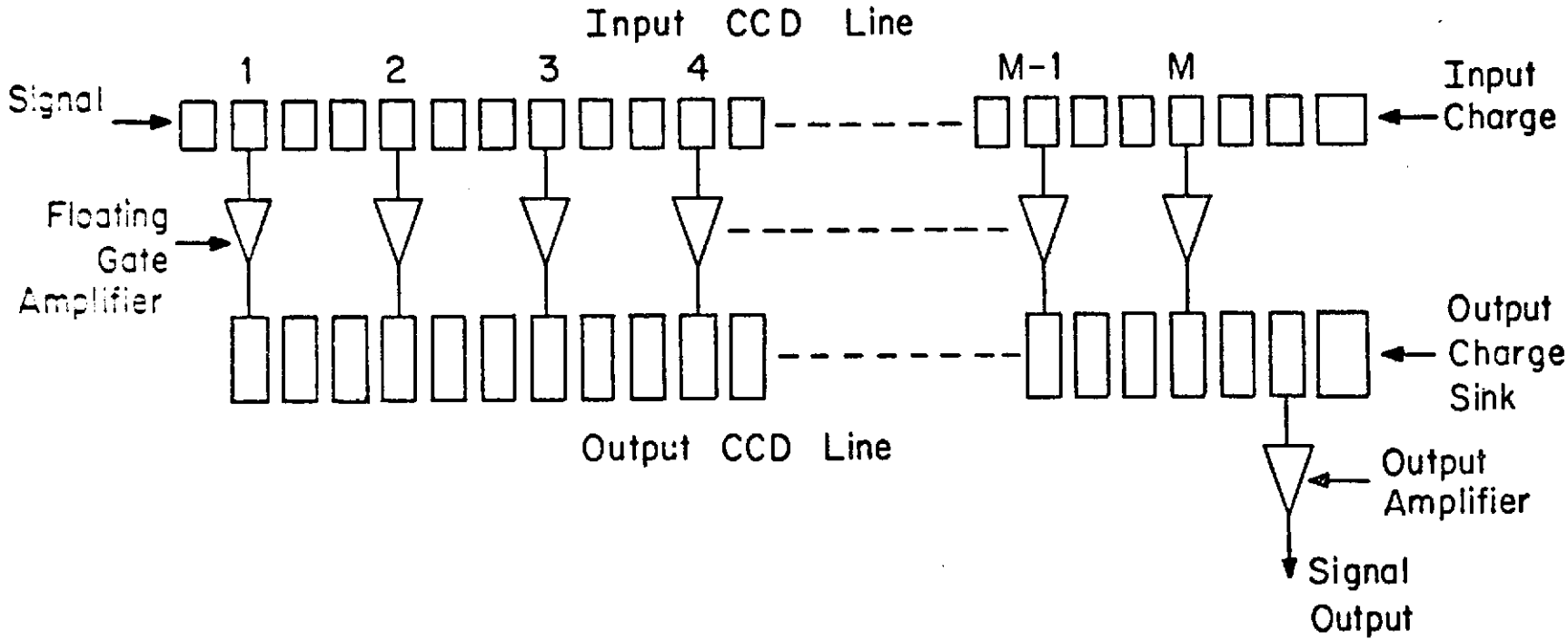


FIGURE 3-17 Distributed Floating Gate Amplifier

stage FGA, while the noise power is amplified by a factor of N. The net signal-to-noise power ratio can thus be increased N-fold without decreasing bandwidth. Expected noise characteristics of a twelve-stage DFGA, which will be on the proposed sensor, are shown on Table 3-6. The DFGA should be capable of detecting as few as two or three signal electrons.

3.2.6 Silicon-Gate Technology

Silicon-gate technology provides several attractive features in the design and fabrication of charge-coupled imaging devices. First, it provides gate electrodes which are optically transparent over most of the visible spectrum and in the near infrared. Second, polysilicon layers have been doped selectively using oxide masking to form many gates in one continuous layer to provide a simple means of forming a sealed-channel CCD structure, i.e., a structure where the electrical potential in the plane of the gates is effectively controlled. Third, it is feasible with this technology to form multilayer structures where necessary, providing powerful design flexibility.

3.2.6.1 Optical Properties of Silicon-Gate Structures

Since the optical properties of polysilicon layers are virtually the same as those of bulk silicon, the transmittance spectrum of multi-layer structures incorporating polysilicon can be determined directly from the layer thickness. Polysilicon layer thicknesses are commonly in the range of 0.15 to 0.50 μm. Apart from interference

TABLE 3-6

DFGA NOISE ANALYSIS

TYPE OF NOISE	FUNCTIONALITY	NOISE VOLTAGE (UV)			
Bandwidth (MHz)		1	2	10	40
Shot Noise	$(V_n^2) = 2\,qf\,I_d/g_m^2$	175	247	553	1106
Thermal Noise	$(V_n^2) = \frac{8}{3}kTf\,\frac{1}{gm}$	72.7	103	230	460
Total Noise		190	268	597	1194
Signal per electron		137	137	137	137
Minimum Detectable Number of Electrons(1)		2	3	7	14

NOTES:

(1) Values depend on bias point of the FGA transistor.
(2) Gate Dimension = 5 um x 20 um.
(3) 1/f noise is neglected.
(4) Temperature = 300°K.
(5) Total noise computed on power basis.

phenomena, the 50% absorption edge for this range of thicknesses varies between 0.41 and 0.48 μm. By proper choice of the several layer thicknesses of polysilicon and dielectrics, it is possible to achieve various types of transmittance optima. Some examples of these are: 1) maximization of the responsivity to a particular illumination spectrum, 2) maximization of the photopic responsivity when the imaging device is filtered to approximate the eye response, and 3) minimization of the spectral peak-to-valley fluctuations in some spectral band.

It has been found from a combination of experimental and theoretical data that broadband averaged transmittances of over 50% are achievable with both single and double polysilicon layer structures. The broad spectral band in such cases can cover close to a factor of two range of wavelength. In calculations which assume perfectly collimated radiation, large variations in transmittance occur over relatively narrow spectral ranges. However, in measurements, the radiation is usually convergent to such an extent that substantial smoothing of the spectrum results. Examples of these effects are shown in Fig. 3-18 for an area imaging device with two polysilicon layers.

3.2.6.2 Electrical Properties of Silicon-Gate Structures

Silicon-gate structures are typically formed by depositing undoped polysilicon and then by doping the gate regions selectively with the aid of oxide masking.

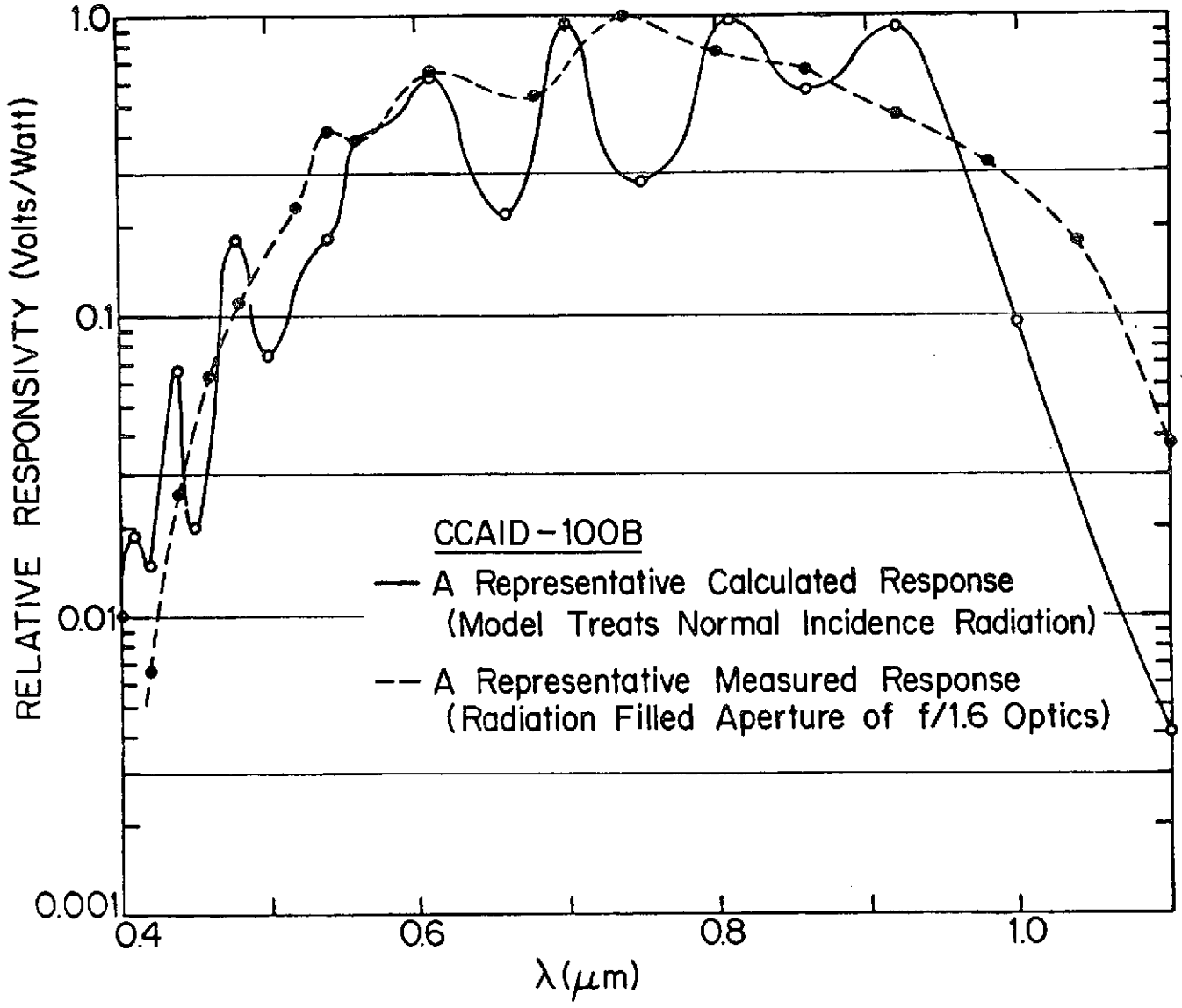


FIGURE 3-18 SPECTRAL RESPONSE OF A DEVICE IN WHICH RADIATION PASSES THROUGH TWO POLY-SILICON LAYERS BEFORE ENTERING THE ACTIVE SENSING REGION.

The sheet resistivities of the doped and undoped regions are typically 20 ohms per square and 10^6 ohms per square, respectively, at room temperature. The temperature dependence of the first value is negligibly small over the range of -90°C to +25°C; the dependence of the second is large. The resistivity doubles for each 10 to 12°C decrease in temperature. It should be noted that the conductivity of undoped polysilicon increases at high electric fields. Furthermore, the temperature dependence of the conductivity at high fields is not the same as at low fields. More details are presented in Section 3.2.4.1 where these properties are treated in a design trade-off discussion.

3.2.7 Anti-Blooming

In connection with a previous discussion of two alternative area array configurations (Section 3.2.4), anti-blooming was a consideration. In the case of the "conceptually simplest" configuration of Fig. 3-12 a straightforward incorporation of column anti-blooming control elements was indicated in (b) of that figure. Similarly, in the case of the interline-transfer configuration, (c) of that figure, column anti-blooming control was incorporated. Column anti-blooming control prevents blooming in one column from extending to other portions of the array.

Element anti-blooming control can be implemented in a CCD structure by forming a long narrow sink diode between each column of sensors. It may be possible to locate this sink diode below the sensors using epitaxial techniques.

However, these techniques appear ill-advised for inclusion in large area arrays during the early phases of development because larger die sizes are involved.

3.3 Design Features and Estimated Performance of the Area Sensor Array

3.3.1 Design Features

The principal design features and parameters of the proposed area sensor array are given in Table 3-7. It may be seen that the format of the sensor is compatible with standard television. This results in two minor deviations from the JPL Study Guidelines. The array consists of 486 x 378 elements rather than 500 x 500 and the format is rectangular with a 4:3 aspect ratio rather than square.

The proposed interline-transfer configuration is designed to be driven by a sync generator already developed for standard television applications. Even though JPL frame rates are anticipated to be much slower than those of standard television, the drive timing and logic remain the same.

3.3.2 Estimated Performance

A conventional listing of the basic performance characteristics is given in Table 3-8. Comparisons with first and second priority objectives are presented in Tables 3-9 and 3-10.

TABLE 3-7

Design Features And Parameters Of The Area Sensor Array

Configuration	interline transfer
No. of elements	486 rows x 378 columns
Cell size	18 μm vertical x 30 μm horizontal
Cell sensor area	18 μm vertical x 15 μm horizontal
Approx. raster size	0.35 in. x 0.45 in.
Approx. chip size	0.42 in x 0.47 in.
Vertical register type	2-phase, implanted barrier
Output register type	4-phase, overlapping gates
On-chip preamplifiers	(1) differential gated-charge amplifier (2) floating gate amplifier (3) distributed floating gate amplifier
Total number of pins	33
Number of pins required for operation with pre-amplifier (1) only	15
Saturation charge	0.07 pC
Saturation electron count	4.4×10^5
Column - antiblooming	Yes
Input register	Yes

TABLE 3-8

Projected Performance of the Proposed Area Sensor

Operating Conditions:	
Temperature	$-40^{\circ}C$
Output frequency	10KHz
Frame time	20 sec.
Exposure time	≤9 sec.
Illuminating	$2854^{\circ}K$ tungsten
Responsivity, internal	> 35 mA/watt
* Responsivity, external	> 29 V per J/M^2
* Preamp. conversion gain	1.5 V/pC
Saturation exposure level	$< 3.5 \times 10^{-3} J/M^2$
* Saturation output signal level	100 mV
* Background dark signal level (j_D ($25^{\circ}C$)≤10nA/cm^2)	< 1.5 mV
* Peak-to-peak dark signal level (excludes a small number of dark signal spikes)	< 0.15 mV
* Random noise background, RMS	< 0.05 mV
* Gamma, i. e., linearity of response	1.00 ± 0.03
MTF at 300 TV lines, vertical and horizontal ($\lambda \leq 0.60$ μm)	> 50%
Range of MTF	$MTF_{min.}$ to 100%

* Values are estimated for preamplifier (1), the gated-charge integrator which has been characterized with data from existing devices. Although preamplifiers (2) and (3) have not been thoroughly characterized, they offer the advantage of reduced random noise referenced to the input.

TABLE 3-9

Proposed Area Sensor Array Compared To First Priority Objectives

		JPL Goal	Proposed Sensor *
1.	Configuration	500 x 500 element square format ≤25 μm square elements	486 x 378 element 3:4 raster format 18 x 15 μm sensor elements on 18 x 30 μm centers
2.	Data rate	10 KHz	10 KHz
3.	Exposure time	1 msec to 5 sec	0 to 9 sec.
4.	Sensitivity	S/N >10 at 100 $\mu J/m^2$	S/N >50
5.	Gamma	1 ± 0.2	1 ± 0.03
6.	Dynamic range	>1000:1	>2000:1
7a.	Signal Nonuniformity	≤15% S. D. ** at 5% saturation	~5%
		≤5% S. D. at 80% saturation	~5%
7b.	Dark current Non-uniformity	≤20% S. D.	≤20%
8.	Blemishes	2 lines, 50 elements	2 lines, 50 elements
9.	Residual image	<1%	<0.5%
10a.	MTF (2854°K)	>60% at 20 lp/mm	>50% at 15 lp/mm
10b.	MTF Nonuniformity	≤ 10%	MTF_{min} to 100%
11.	Spectral Response	Full Si vidicon response	Approx. Si vidicon response (see Fig. 3.2.7-1)
12.	Image Plant Flatness	$\leq \pm 0.02$ mm	$\leq \pm 0.01$ mm
13.	Operating Temp.	-60°C to +45°C	-100°C to +75°C

* All performance figures are projections.

** S. D. = Standard Deviation

TABLE 3-10

Proposed Area Sensor Array Compared To Second Priority Objectives

		JPL Goal	Proposed Sensor
1.	Electronic Exposure Control	Yes	No
2.	Sensitivity Control	Yes	No
3.	Blooming Control	Element-type	Column type; also element-type in one mode of operation
4.	Operating Life	≥ 2500 hours	No problems anticipated.
5.	Non-operating Life	> 5 years	No problems anticipated.
6.	Shock and Vibration	(see guideline)	No information available.
7.	Radiation resistance	(see guideline)	No information available.
8.	Higher LLL sensitivity	------	Much higher, provided that a lower operating temperature and the DFGA are employed
9.	Larger number of elements	------	No

3.4 Design and Estimated Performance of the Linear Sensor Array

3.4.1 Description of the Proposed Design

It is proposed that the linear-sensor array with its accompanying storage matrix for line-by-line readout be implemented by a modification of a recently designed 190 x 244 interline-transfer area sensor. A schematic layout of the device is shown in Figure 3-19. Only the top row of 190 elements will be exposed to receive illumination. The remaining photosensors will be opaqued and not used. Light signals in the top row of photosensors will be transferred to adjacent column registers, which will constitute a 190 x 121 element storage matrix; the signals will then be shifted line-by-line down the columns to the collection register, where they will be clocked out at the specified 100 Hz data rate.

The usually employed electronic input register shown at the top of the array in Figure 3.4-1 can be used either to provide element anti-blooming or electronic exposure control.

The principal design features and parameters are given in Table 3-11. With respect to the JPL Guideline, there are 190 rather than 100 photoelements. There is also the minor deviation of a 30 μm horizontal cell dimension which is slightly in excess of the specified 25 μm limit.

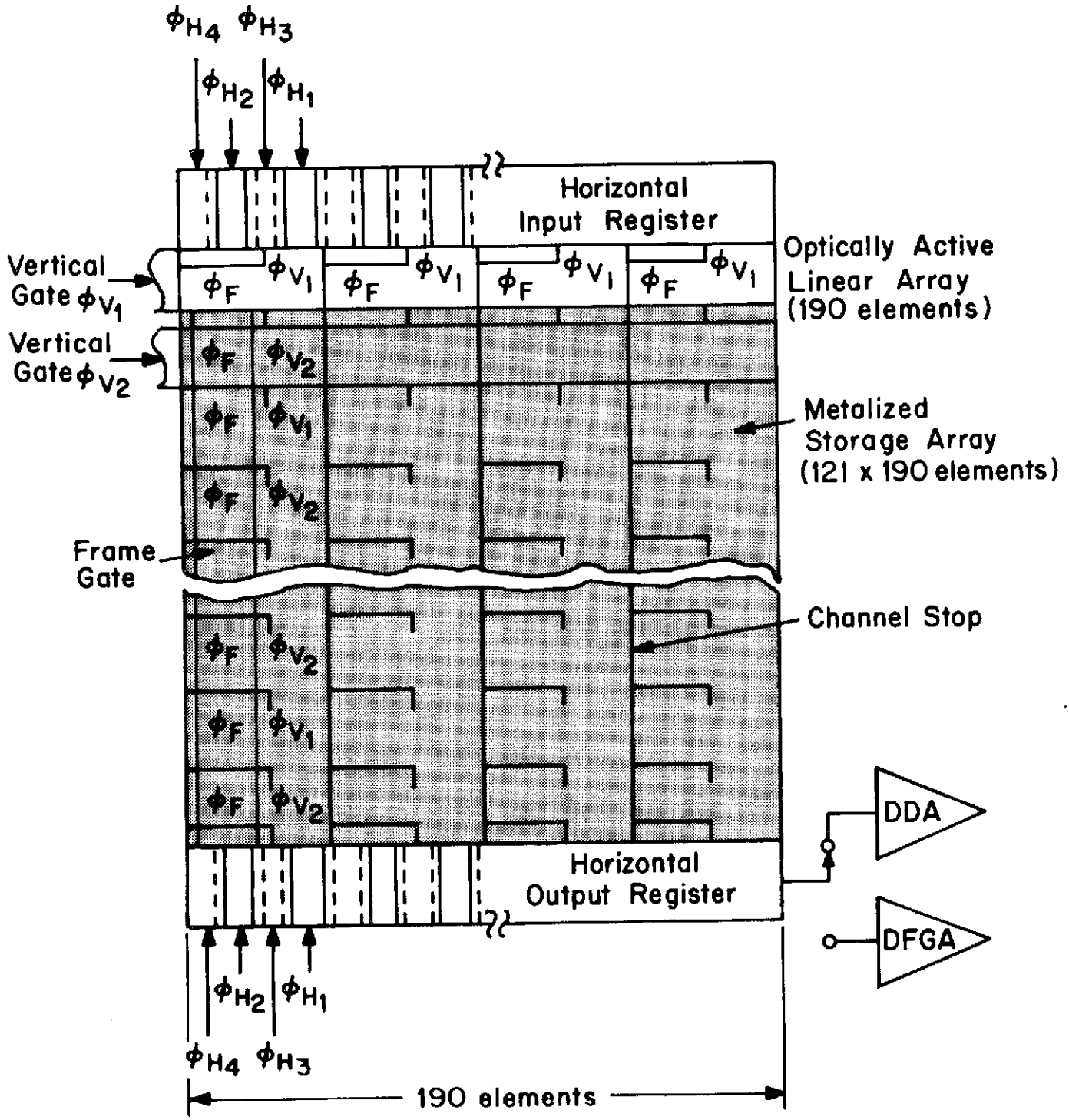


FIGURE 3-19 Schematic Diagram Of Proposed 190 Element Linear Sensor With 121 X 190 Element Storage Matrix

3.4.2 Estimated Performance

The projected performance characteristics of the proposed device are given in Table 3-12. It may be noted that an operating temperature of -50° C rather than the desired -40° C is shown. At -40° C the dark charge accumulated during the 230 sec scan time would severely limit the dynamic range of the photosignal. At -50° C the dark charge signal is six percent of saturation. This dark charge signal can be subtracted by off-chip circuits.

The projected performance of the linear sensor is compared with first-priority objectives in Table 3-13 and with second-priority objectives in Table 3-14.

TABLE 3-11

Design Features and Parameters of the Proposed Linear Sensor Array with a Storage Matrix

Configuration	Linear array with shielded storage array
Number of elements	
Linear sensor array	190
Storage array	121 rows x 190 columns
Cells size	
Linear sensor array	18μm vertical x 30μm horizontal
Storage array	36μm vertical x 30μm horizontal
Cell sensor area	18μm x 30μm horizontal
Vertical register	2 phase, implanted barrier
Output register type	4 phase, overlapping gates
On-chip preamplifiers	(1) differential gated charge amplifier (2) floating gate amplifier (3) distributed floating gate amplifier
Total number of pins	33
Number of pins required for operation with pre-amplifier (1)	15
Saturation charge	0.07 pC
Saturation electron count	4.4×10^5
Element antiblooming	Yes

TABLE 3-12

Projected Performance of the Proposed Linear Sensor with Storage Array

Operating Conditions:

Temperature	$-50^{\circ}C$
Output frequency	100 Hz
Input frequency	100 lines/sec
Scan time	230 sec
Exposure time	0.01 sec
Illumination	$2854^{\circ}K$ tungsten lamp
Responsivity, internal	>70 mA/watt
* Responsivity, external	>58 V per J/m^2
* Preamp conversion gain	1.5V/pc
Saturation exposure level	$<1.8 \times 10^{-3}$ J/m^2
* Saturation output signal level	100 mV
* Background dark signal level (J_D ($25^{\circ}C$) = 10 nA/cm^2)	<6 mV
* Peak-to-peak dark signal level (excludes a small number of dark signal spikes)	<0.6 mV
* Random noise background, RMS	<0.1 mV
* Gamma, i. e., linearity of response	1.00 ± 0.03
MTF at 150 TV lines, horizontal ($\Lambda < 0.6$ μm)	>50%
Range of MTF	($MTF_{min.}$ to 100%)

* Values are estimated for preamplifier (1), the gated charge preamplifier, which has been characterized with data from devices. Although preamplifiers (2) and (3) have not been thoroughly characterized, they offer the advantage of reduced random noise referenced to the input.

TABLE 3-13

Linear Sensor Array Projected Performance vs. First Priority Objectives

		JPL Goal	Modified CCAID
(1)	Configuration	100 element linear sensor on 25 μm centers with 100 x 200 storage array	190 element linear sensor on 30 μm centers with 190 x 121 storage array
(2)	Data Rate	100 Hz	100 Hz
(3)	Exposure time	0.01 sec	0.01 sec
(4)	Sensitivity	S/N > 10 at 100 $\mu J/m^2$	S/N > 50
(5)	Gamma	1 ± 0.2	1 ± 0.03
(6)	Dynamic range	>1000:1	>1000:1
(7)	Signal nonuniformity	<15% S. D. **at 5% of nominal saturation	≈5%
		<5% S. D. at 80% of saturation	≈5%
(7b)	Dark current non-uniformity	≤ 20% S. D.	≤ 20% *
(8)	Blemishes	1 line and 25 elements maximum	1 line and 25 elements maximum
(9)	Residual image	<1%	<0.5%
(10a)	MTF (2854°K)	>60% at 20 lp/mm	>50% at 15 lp/mm
(10b)	MTF nonuni-formity	≤10%	MTF min to 100%
(11)	Spectral response	Full Si vidicon response	Approximate Si vidicon response - See Figure 3.2.7-1
(12)	Image Plane Flatness	± 0.02 mm	≤±0.01 mm
(13)	Operating temperature	-60°C to +45°C	-100°C to +75°C

* The uncorrected output contains a dark current which can be as high as 6% of saturation. The values given here are obtained by subtraction of this current by off-chip circuits.

** S. D. = standard deviation

TABLE 3-14

Linear Sensor Array Projected Performance Compared To Second Priority Objectives

	JPL Goal	Proposed Device
(1) Electronic Exposure Control	Yes	Yes
(2) Sensitivity Control	Yes	Yes
(3) Blooming control, element type	Yes	Yes
(4) Operating life	2500 hours	No problems anticipated
(5) Non-operating life	5 years	No problems anticipated
(6) Shock and vibration	(See Guideline)	No information available
(7) Radiation resistance	(See Guideline)	No information available
(8) Higher LLL sensitivity	———	Obtainable at lower operating temperatures
(9) Larger number of elements	———	121 x 190 elements

4.0 SUMMARY DISCUSSION

The proposed area sensor array is an interline-transfer design with 486 x 378 photoelements. Two-phase, double polysilicon gates with cell dimensions within the specified 25 μm are used. Although three types of on-chip amplifier are available, the gated-charge integrator, which has been well characterized on existing CCD sensors, provides the responsivity specified in the JPL Study Guideline. It is felt that this proposed area-sensor design with the high level of confidence established by low temperature measurements of dark current and transfer efficiency on existing devices will perform as predicted and will more than satisfy the JPL first-priority objectives.

With regard to second-priority objectives, the proposed design has the capability of element blooming control. Although the design does not employ structures that can eliminate the mechanical shutter in the camera system, it can be operated to adjust automatically the exposure time to prevent over-exposure. The JPL goals that are concerned with operating and non-operating life appear at this time to present no problem. The remaining goals involve shock-and-vibration and radiation resistance tests which have not been performed to the best of our knowledge.

Should a lower light level capability be desired, it can be obtained by employing a lower operating temperature and the DFGA, which will be on the chip.

Finally, there is the question of difference in design approach if larger numbers of photoelements were specified. In view of the performance Fairchild has achieved with area CCD sensors under

the Naval Electronics Command program, which are of the basic design we are recommending to JPL, there would be at this time no difference in design approach.

THE FOLLOWING PAGES ARE DUPLICATES OF ILLUSTRATIONS APPEARING ELSEWHERE IN THIS REPORT. THEY HAVE BEEN REPRODUCED HERE BY A DIFFERENT METHOD TO PROVIDE BETTER DETAIL