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DUKE UNIVERSITY

STATIC DC TO DC POWER CONDITIONING-ACTIVE RIPPLE FILTER,
1 MHZ DC TO DC CONVERSION, AND NONLINEAR ANALYSIS

by

William August Sander, III

Eruditio et Religio

Errata

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Page No.	Line No.	Correction
11	Fig. 1(c)	line from S2 to source ground should be removed and that side of S2 should be connected to the positive end of source E
20	17	insert "negative of the" after "to the" and before "feedback"
21	13	insert " - " after "to" and before "$Z_F(s)/Z_S(s)$."
24	Eqs. (16),(17)&(19)	change " = " to " $\cong$ "
33	Eq. (20)	insert " - " after " $\cong$ "
34	Eq. (22)	insert " - " after " = "
41	Eq. (24)	change " = " to " $\cong$ "
45	Last line	delete "the" after "therefore"
94	16	change "V_N" to "V_{N5}"
106	2	change "19" to "21"

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March 23, 1973

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Department of Electrical Engineering
Duke University

Date:_____

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Thomas G. Wilson, Supervisor

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A dissertation submitted in partial fulfillment of
the requirements for the degree of Doctor of
Philosophy in the Department of Electrical
Engineering in the Graduate School of
Arts and Sciences of Duke University

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ABSTRACT
(Electrical Engineering)

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ABSTRACT

Dc to dc static power conditioning systems on unmanned spacecraft have as their inputs highly fluctuating dc voltages which they condition to regulated dc voltages. These input voltages may be less than or greater than the desired regulated voltages. Also, these systems should have high reliability, small size and weight, and high efficiency. This dissertation discusses the design of two circuits which address specific problems in the design of these power conditioning systems and a nonlinear analysis of one of the circuits.

One area of concern in spacecraft power conditioning systems is the low reliability of large-capacitance capacitors commonly used in the L-section or pure-capacitance output filters of dc to dc converters. In spacecraft applications these capacitors are usually tantalum electrolytic capacitors and are normally the least reliable electronic component. The first circuit design discussed is for a nondissipative active ripple filter for dc supplies which uses an operational amplifier to amplify the sensed ripple voltage. The output of the amplifier is connected to the primary winding of a mutual inductor which has its secondary connected in series with the main power path. The closed-

loop gain and phase shift of the amplifier are designed so that
the voltage on the secondary of the mutual inductor is of the
same amplitude and phase as the ripple voltage at the input to
the filter. The secondary voltage has the effect of cancelling
the ripple voltage. One configuration of the ripple filter re-
quires only 4.87 μF and has approximately the same attenuation
as a low pass L-section filter with a break frequency of 100 Hz
requiring 84 times more capacitance. The small required capaci-
tance for this filter can be obtained using the more reliable
ceramic capacitors.

Normal optimum switching for dc to dc power conditioning
circuits is in the range of 2 to 50 kHz. However, in the future,
experiments for spacecraft are anticipated which will make meas-
urements in this frequency range. Therefore, a dc to dc convert-
er operating at a switching frequency of 1 MHz is the second cir-
cuit discussed. The type of circuit chosen is an energy-storage
converter using an isolated two-winding mutual inductor as the
energy storage element and a triangular waveform clock signal to
produce a constant switching frequency of 1 MHz. This circuit
is designed to demonstrate the feasibility of operation at 1 MHz;
therefore, the design does not include self-starting and requires
several power supplies. However, the circuit operates at an out-
put power of 20 watts with a peak efficiency of 79 percent and
output-voltage regulation of approximately 1.5 percent. Because
of the high switching frequency of 1 MHz, this circuit also re-
quires less filter capacitance and should have smaller size and

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weight than lower frequency converters.

The third subject of this dissertation is a nonlinear analysis of the type of dc to dc converter utilized in designing the 1 MHz converter. This type of circuit adds the output voltage to the triangular clock signal and subtracts this sum from the reference voltage resulting in an error voltage. The analysis is performed on this error voltage assuming instantaneous switching. The period of oscillation is divided into segments described by linear differential equations which are represented in a limit cycle in a normalized phase plane of the time derivative of the error voltage versus the error voltage. The theoretical phase plane compares closely with an experimental phase plane determined from a 2 kHz converter. Piecewise linear transformations are made around the limit cycle to obtain two sequence functions defining the time periods of a cycle. The accuracy of these sequence functions is verified using data from the experimental 2 kHz converter.

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William A. Sander, III

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STATIC DC TO DC POWER CONDITIONING-ACTIVE RIPPLE

FILTER, 1 MHZ DC TO DC CONVERSION,

AND NONLINEAR ANALYSIS

Chapter I

INTRODUCTION

The subject of this dissertation is static electrical dc
to dc power conversion for spacecraft power conditioning systems.
The most commonly used power system on spacecraft has been and
continues to be a system which consists of a dc source and a
battery. The battery is used to store energy during periods of
high output from the source and to supply energy during periods
of low output from the source. Typical sources are fuel cells,
solar cells, thermoelectric sources, and thermionic sources.
The battery, by its nature, acts as a filter; however, the bat-
tery voltage fluctuates depending on whether it is in a fully
charged or discharged state and whether it is being charged or
discharged. The power conditioning system uses this battery as
its source and conditions the battery voltage by conversion,
regulation, and filtering to voltages which can be utilized by
the various electrical equipment aboard the spacecraft.

Unmanned scientific satellites are continually being de-
veloped for a variety of scientific experiments. The power con-
version equipment on each of these satellites generally has
three common requirements which are high reliability, high

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efficiency, and small size and weight. Other characteristics
of the conversion equipment such as voltage levels, ripple volt-
age, switching frequency, and regulation may vary depending on
the specific tasks or experiments which must be performed.
Many of these requirements are becoming more stringent requir-
ing continued applied research to develop equipment which pro-
vides the characteristics required by the increasingly more so-
phisticated experiments.

Scope

One area of concern in spacecraft power conditioning
systems is the low reliability of large-capacitance capacitors
commonly used in the L-section or pure-capacitance output fil-
ters of dc to dc converters. Capacitors greater than a few mi-
crofarads in value require the use of electrolytic capacitors.
In spacecraft applications, tantalum electrolytic capacitors
are used. These capacitors are normally the least reliable
electronic component on the spacecraft and thus affect the over-
all reliability of the power conditioning system significantly.
Chapter II discusses the design of a nondissipative active fil-
ter which uses an operational amplifier to amplify the sensed
ripple voltage. The output of the amplifier is connected to
the primary winding of a mutual inductor which has its second-
ary connected in series with the main power path. The closed-
loop gain and phase shift of the operational amplifier are

designed so that the voltage on the secondary of the mutual inductor is of the same amplitude and phase as the ripple voltage at the input to the filter. The voltage on the secondary of the mutual inductor thus has the effect of cancelling the ripple voltage. This filter requires only a few microfarads of capacitance and uses the more reliable ceramic type of capacitor achieving approximately the same attenuation characteristic as an L-section filter requiring hundreds of microfarads. The design procedures and experimental characteristics are given in detail in Chapter II.

The normal optimum switching frequency for dc to dc electrical power conversion considering size and weight, reliability and efficiency is in the approximate range of two to fifty kHz. In the near future, however, it is anticipated that spacecraft experiments will include electromagnetic measurements at frequencies up to hundreds of kilohertz. In order that the spacecraft power conditioning equipment not interfere with the experimental measurements, it becomes necessary to design the switching frequencies of the power conditioning equipment at least as high as 1 MHz. This design presents many problem areas such as obtaining semiconductor diodes and transistors with adequately fast switching speeds and designing circuits which can effectively utilize these switching speeds. Core materials must be found which can be used to design transformers that operate efficiently at switching frequencies at least as high as 1 MHz. These problems are discussed in Chapter III where the design of

a basic dc to dc converter operating at a constant frequency of 1 MHz is discussed in detail. The design does not include an automatic starting circuit and requires several auxiliary supplies; however, the basic objective to operate a converter at a switching frequency of 1 MHz with reasonable efficiency is demonstrated. This converter is designed with electrical isolation between the source and the load and operates with good efficiency and a maximum output power of 20 watts. The output power can be increased simply by increasing the base drive to the power transistor. This converter provides a regulated output voltage of 28 volts while operating with a source voltage variation from 21 to 31 volts. The high switching frequency of this converter enables the designer to use the more reliable capacitors of only a few microfarads, therefore offering a second possible means for reducing the output filter capacitance in dc to dc converters.

Every new spacecraft seems to generate a new set of requirements for its power conditioning system. The challenge to design these systems is greatly aided by an analytical ability to predict the performance of the circuits used in the systems prior to designing them. There are a number of different types of circuits used for dc to dc energy conversion and only a small number of these have been thoroughly analyzed. A complete analysis of converters which utilize switching techniques usually requires nonlinear analysis. Chapter IV of this dissertation contains a nonlinear analysis of the error voltage for the type of

dc to dc converter circuit used for the 1 MHz converter in Chapter III. The basic regulation concept of the converter is verified by the analysis and by an experimental confirmation of the analysis using a converter operating at a frequency of 2 kHz. The analysis assumes instantaneous switching and divides the full period of oscillation into segments which are described by linear differential equations. These equations are represented in the phase plane by segments of continuous curves and instantaneous switching is represented by jumps. This converter has a triangular waveform as a clock signal which results in nonautonomous differential equations which cannot be directly plotted in the phase plane; however, an approximation is used which makes the equations autonomous. These equations and analytic expressions for the jumps at switching are used to perform piecewise linear transformations from point to point around the limit cycle resulting in a pair of sequence functions. These sequence functions are expressed in terms of the known circuit parameters and unknown time periods of the limit cycle. An experimental limit cycle for a circuit operating at 2 kHz and the theoretical phase-plane trajectory compare very closely. The accuracy of the sequence functions is also verified by the experimental data. The analysis thus shows that systems with triangular driving functions can be analyzed using the method of piecewise linear transformations in the phase plane.

Chapter V provides a summary of the work described in the dissertation and describes certain conclusions concerning this work.

Chapter II

NONDISSIPATIVE ACTIVE FILTER FOR DC SUPPLIES

Power sources used on spacecraft typically produce widely-fluctuating dc voltages which cannot be used directly to supply electronic equipment. Consequently, dc to dc converters are employed to provide the various regulated dc supply voltages required by the spacecraft equipment. These converters must be capable of meeting very stringent requirements such as tightly-regulated output voltages with small ripple voltage, high operating efficiency, high reliability, small size, and low weight. Nondissipative switching-mode converters instead of series-dissipative or shunt-dissipative regulators are commonly used because they are more efficient when applied to systems with widely-fluctuating input voltages and because they can be used to obtain regulated voltage levels higher than the source voltage [1]. The output current of a switching-mode converter usually includes rapid large-amplitude changes which require a significant amount of filtering. Dc to dc converters commonly operate at switching frequencies in the range of two to fifty kHz and, in order to achieve high efficiencies, require output filters with nondissipative dc paths. Nondissipative L-section or pure-capacitance filters are commonly used to provide the

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filtering required to produce smooth dc voltages. In the frequency range of two to fifty kHz, these filters require large amounts of capacitance.

In order to provide these large amounts of capacitance the designer is required to use electrolytic capacitors. These large-microfarad dc filter capacitors are less than ideal in satellite static power converter applications. They occupy a large volume and have a relatively low reliability compared to low-microfarad capacitors, such as ceramic, mica, and solid tantalum, and other circuit components. In applications such as spacecraft where size and weight are important factors, the type of capacitor which is usually chosen from among the many different types currently available is the dry slug or wet slug tantalum electrolytic capacitor which has large capacitance per unit volume. However, these capacitors tend to fail due to inherent dielectric breakdown, internal heating, and electrolyte leakage particularly in the severe operating conditions of outer space [2,3,4]. The low-microfarad types of capacitors have better reliability but if used to provide hundreds of microfarads of capacitance would occupy an exhorbitantly large volume due to their small capacitance per unit volume. Consequently, there is a definite need to reduce the amount of capacitance required in the output filters of dc supplies, even by increasing circuit complexity, so that the more reliable low-microfarad capacitors can be used to improve filter reliability.

Various techniques for reducing the required capacitance
have been developed; however, they generally do not have dc
paths or they have dissipative elements in the dc paths [5,6].
As is later explained in Chapter III, the required capacitance
can also be reduced at the expense of other circuit performance
characteristics, such as efficiency, by going to a much higher
switching frequency in the vicinity of one MHz.

Scope

The active ripple filter configuration discussed in
this chapter has a non-dissipative dc path and operates in the
frequency range of two to fifty kHz. It utilizes an operational
amplifier, a mutual inductor, and more reliable low-microfarad
capacitors to provide the same ripple attenuation that is ob-
tained using conventional L-section or pure-capacitance filters.

The basic principles of L-section and pure-capacitance
filters and of the active ripple filter configuration are ex-
plained using block diagrams of the converter system. Then, the
complete schematic diagram for the active ripple filter config-
uration is given along with a brief description of the purpose
of each component. The transfer characteristic of the opera-
tional amplifier is derived separately and then combined with
the remainder of the circuit to obtain an analytical transfer
function. Some circuit principles, or design considerations,
are given next which should be considered when designing an

active ripple filter. Three types of active ripple filters all derived from the same basic configuration are discussed. The special case of the basic configuration which yields an active filter having a narrow bandwidth of attenuation and its transfer function are discussed first. Next, the special case of a wide-bandwidth filter and its transfer function are discussed. Feedback is then added from the output of the wide-bandwidth filter and a new transfer function is derived which is the third special case with an attenuation characteristic significantly better than the attentuation characteristic of the wide-bandwidth filter without feedback. The theoretical and experimental characteristics of each of these three active ripple filters are discussed individually. In addition, the capacitance advantage of the wide-bandwidth filter with feedback as compared to an L-section filter is discussed; and some possible applications and additional conclusions are given.

Circuit Principles

Background. Before an active filter can be designed to attenuate the load ripple voltage generated by nondissipative switching dc to dc converters, the manner in which this voltage is generated should be fully understood. Fundamental examples of three types of dc to dc switching converters are shown in Fig. 1. Figs. 1(a) and 1(b) show voltage step-up and voltage step-down energy-storage converters, respectively [7,8,9,10].
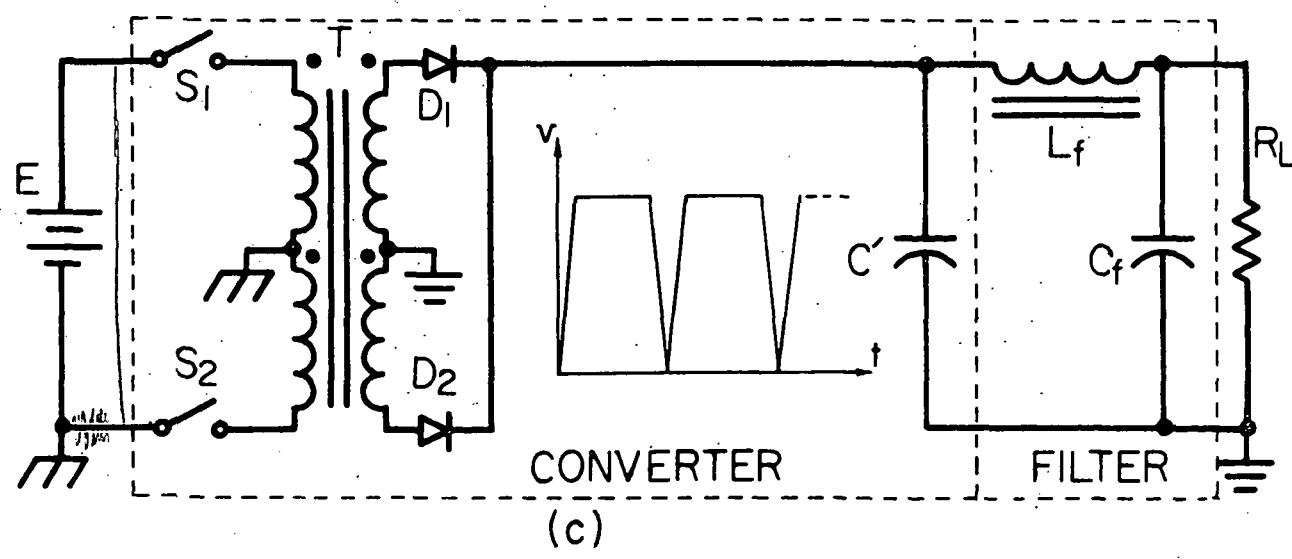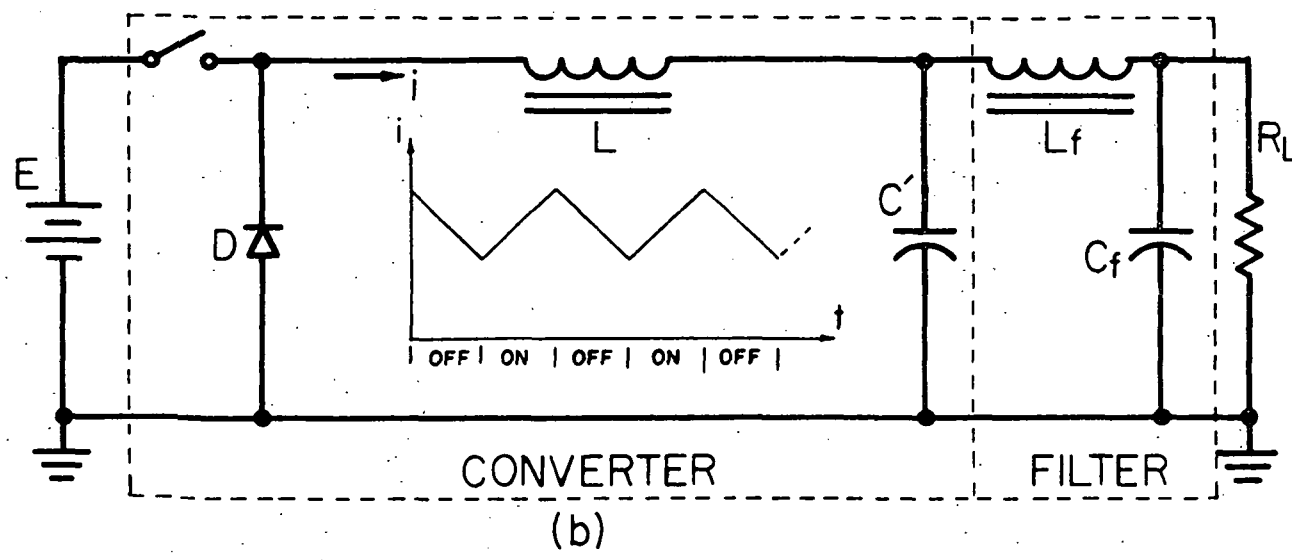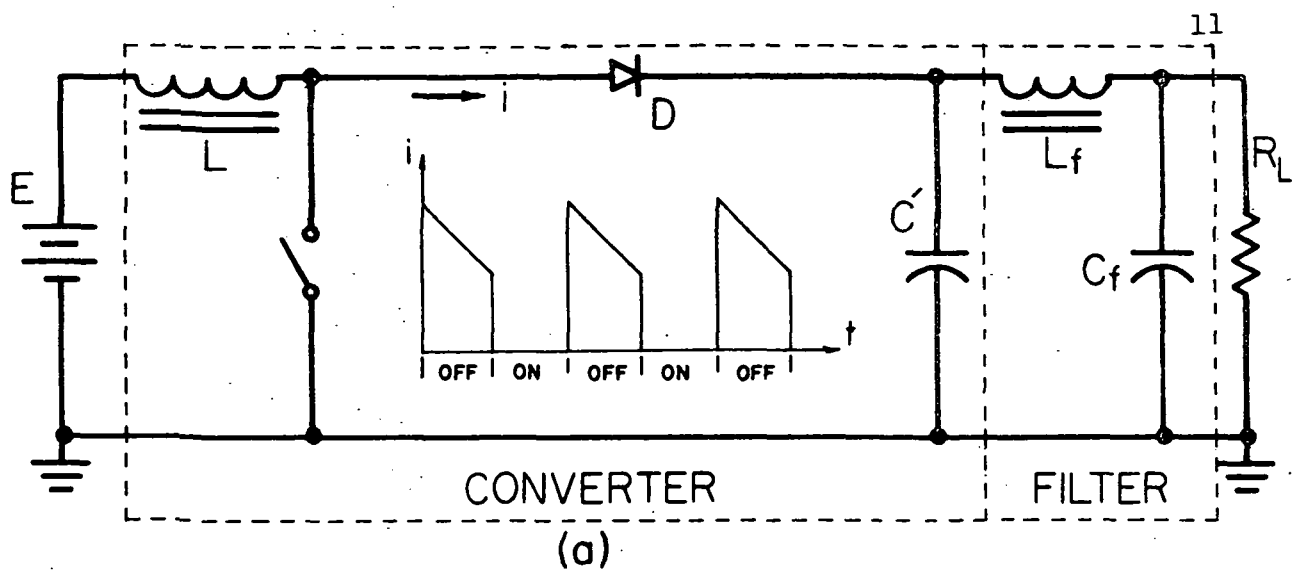
Fig. 1. Basic converter configurations.

In both cases, when the switch is closed, energy from the source E is stored in the inductor L; and when the switch is opened, the energy is released through diode D forming the current waveforms shown. These waveforms are subsequently filtered by capacitance C' and the L-section filter made up of L_f and C_f to produce the ripple voltage on the load R_L. Fig. 1(c) employs two controlled switches which switch in such a manner as to apply the source E alternately to the primary windings of the non-saturating transformer T. The voltage on the secondary is rectified to obtain the voltage v which is filtered by C' and the L-section filter L_f and C_f to obtain the ripple voltage on the load R_L [11]. The waveform for v in Fig. 1(c) is the full-wave rectified voltage without any filtering due to C', L_f, or C_f; and the voltage is shown to dip to zero during the finite switching times. Whereas the circuits in Figs. 1(a) and 1(b) generate current waveforms which require a capacitive input filter, the circuit in Fig. 1(c) generates a full-wave rectified voltage waveform for which a capacitance C' may not be required. In either case, it is possible to remove the L-section filter, made up of L_f and C_f, and have a pure-capacitive filter utilizing a single large-microfarad capacitance C'.

The nature of the ac voltage on C' is of significance when designing the filter. This ac voltage is generated when the capacitance charges and discharges during the switching cycle of the converter. The converter is basically a nonlinear circuit. A Fourier analysis of the switching waveform would

yield a large amplitude fundamental component with the same frequency as the switching frequency. The nonlinear nature of the circuit would also produce numerous large-amplitude higher-order harmonics. The most desirable filter is, therefore, a lowpass filter which must be capable of passing a large direct current and which must have a cutoff frequency less than the switching frequency.

A basic dc to dc converter system is shown in Fig. 2(a). The dc to dc converter is represented by the block appropriately labelled. Capacitance C' is included as part of the converter since many types of converters do require some output capacitance. The source E is shown as well as its internal resistance r_e. Inductor L_f and capacitor C_f make up the conventional L-section filter and R_L is the load resistance. The direct voltage on C' is V'; and the converter output ripple voltage is v_c. $V' + v_c$ is the complete converter output voltage. After passing through the filter, the direct voltage at the load R_L is V; and the ripple voltage is v_L. In the following development of the active filter, it is important to remember that the objective of the active filter is to replace the conventional L-section filter with circuitry that: (1) passes the required direct current with high efficiency, (2) requires only small-microfarad filter capacitance so as to improve the filter reliability, (3) does not significantly increase the size and weight of the filter, and (4) achieves approximately the same ripple-voltage attenuation as the L-section filter. One of the changes which must be
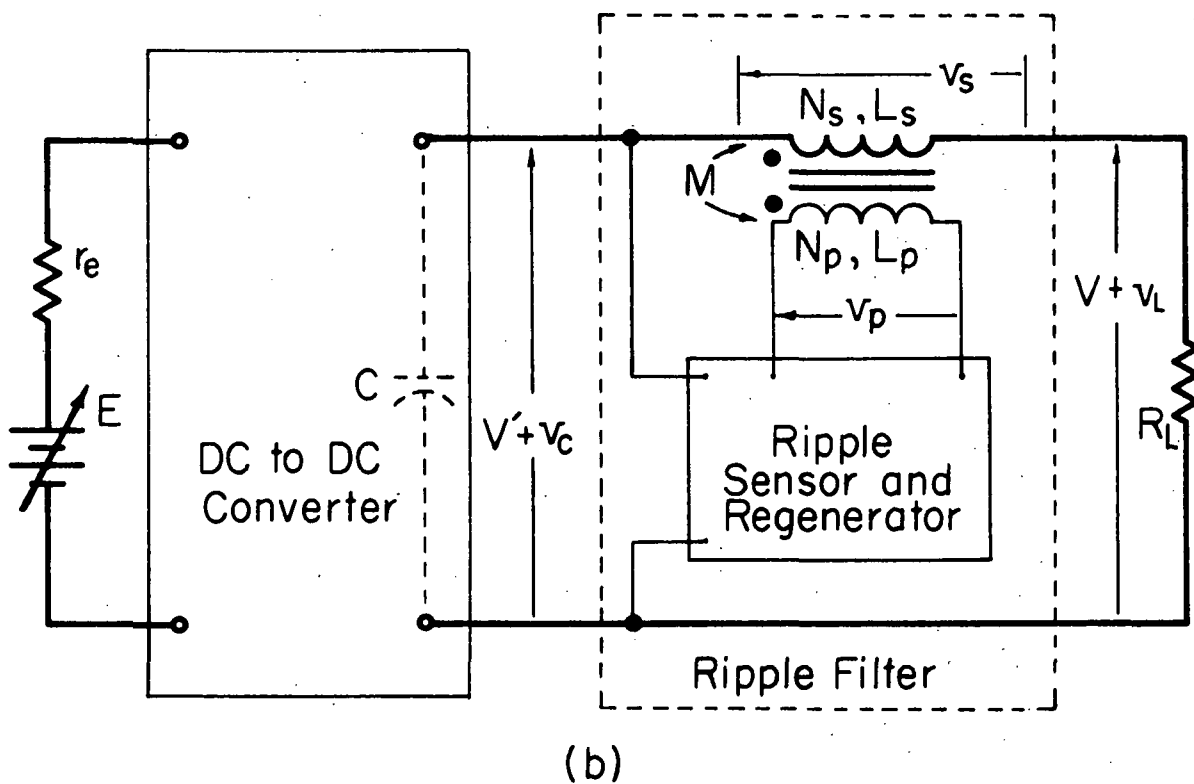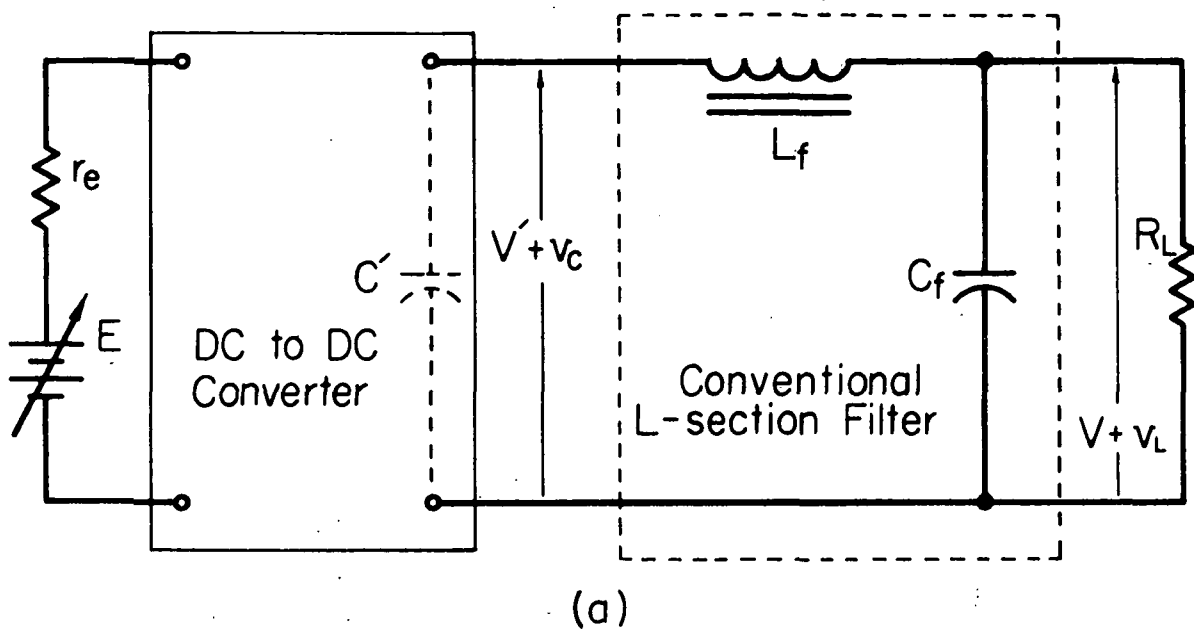
Fig. 2. (a) Dc to dc converter using a conventional L-section filter. (b) Dc to dc converter using the ripple filter configuration.

made to the filter shown in Fig. 2(a) in order to meet the objectives is that the capacitance requirement for C' and C_f must either be reduced or removed.

The basic configuration for the active ripple filter which is discussed in this chapter is shown in Fig. 2(b). Capacitor C_f is removed and inductor L_f is replaced by mutual inductor M. Capacitor C may be only a few microfarads instead of the hundreds of microfarads required for C' in Fig. 2(a). The effect of the capacitance reduction is an increase in the magnitude of the converter output ripple v_c. The active ripple filter uses the principles of Kirchhoff's Law to reduce v_c to an acceptable small amplitude for v_L. The converter output ripple voltage v_c in Fig. 2(b) is sensed and regenerated, by the block so labelled, on the primary winding N_p of the mutual inductor so as to induce a voltage v_s on the secondary winding N_s. By Kirchhoff's Law, v_L is equal to the difference between v_c and v_s as

$$v_L = v_c - v_s \quad . \tag{1}$$

If the waveform of v_s is exactly the same as the waveform of v_c, then v_L is zero. However, this condition is impractical to obtain; and v_L always has some magnitude. The following discussion is concerned with the schematic diagram of one example of this type of active filter and a discussion of some of the design considerations.

The active filter circuit. The complete schematic diagram for the active filter is given in Fig. 3 and the component values are given in Table 1. In this diagram, a battery is used to represent the dc component V' of the converter output voltage; and an ac voltage source is used to represent the converter output ripple voltage v_c. Resistor r_c is the equivalent series output resistance of the converter. The dc load-current path through the mutual inductor M and load R_L is indicated by heavy lines. The operational amplifier with its associated components is employed as the ripple sensor and regenerator referred to in Fig. 2(b). Capacitor C_1 is the coupling capacitor which blocks the dc voltage V' and should have a negligible effect on the ac input signal to the operational amplifier. Resistor R_S is the series resistance of the operational amplifier and R_F is the feedback resistor. The closed-loop gain of the amplifier is therefore approximately R_F/R_S. Resistor r_p is the equivalent series resistance of the primary winding N_p of the mutual inductor M which has its secondary winding N_S in series with the dc path. L_p, L_s, and M are the primary, secondary, and mutual inductance, respectively. It should be noted that the negative input to the amplifier is used which puts the amplifier in the inverted mode and that the polarities of the primary and secondary windings of the mutual inductor are therefore reversed. Bias resistor R_Z and zener diodes D_{Z1} and D_{Z2} provide the plus and minus voltage supplies for the amplifier. Capacitors C_S
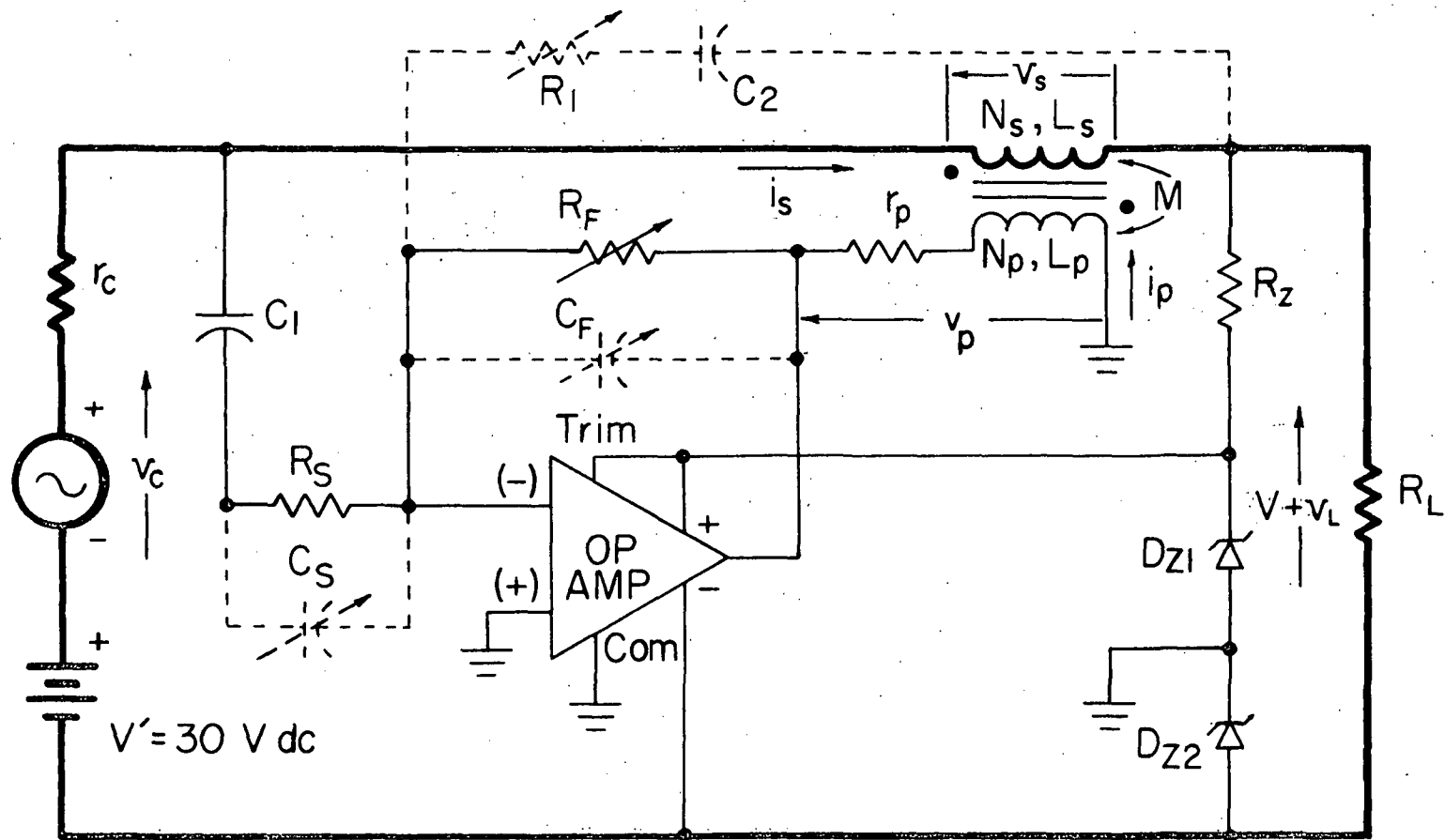
Fig. 3.   Schematic diagram for the active ripple filter.

Table I. Components list for the active filter.

OP AMP	Analog Devices Model 148A
C_1	4.77 µF
D_{Z_1}, D_{Z_2}	1N964A
R_F	28 kΩ fixed + 5 kΩ trimpot
R_S	5110 ohms
R_Z	100 ohms
R_L	45 to ∞ ohms
r_p	52.22 ohms
r_c	source internal resistance
L_p	203 mH (1000 turns AWG no. 36)
L_s	6.2 mH (176 turns AWG no. 22)
M	34.95 mH
Core	Magnetics, Inc. no. 55928
	Permalloy powder core

	C_S	C_F	C_2	R_1
Narrow bandwidth	147 pF	67 pF	0	0
Wide bandwidth	0	0	0	0
Wide-bandwidth with feedback	0	0	0.1 µF	5 kΩ trimpot

and C_F are used to compensate the transfer characteristic of the amplifier. They are shown dashed because it is not always necessary to utilize them. Likewise, R_1 and C_2 may not always be used so they are shown dashed. The functions of these components are explained in more detail later in the chapter.

Active ripple filter power dissipation. It is important that the active filter be essentially nondissipative. For this reason, it is necessary to show that the load on the operational amplifier is essentially non-dissipative and that all other dissipation is very small compared to the power passing through the filter to the load. First, the load ripple voltage v_L should be very small so that v_s essentially cancels v_c and negligible load is reflected to the primary winding N_p. Second, the primary inductance L_p must have a high Q to minimize phase shift as is explained later. This means that r_p must be small and the dissipation in r_p is negligible. Under these two conditions the load on the output of the operational amplifier is essentially a pure inductance L_p. The output stage of most operational amplifiers is a class A amplifier; and, when a class A amplifier is used to drive a pure inductive load such as L_p, there is no real power delivered from the output of the amplifier. This means that the power dissipated in the active ripple filter in Fig. 3 that is not present in a conventional L-section filter is: (1) the negligible power dissipation in R_L due to a nonzero v_L (2) the negligible dissipation due to r_p and (3) the quiescent power required by the operational amplifier and its bias sources. The

first and second of these are usually much smaller than the
quiescent dissipation, and the quiescent dissipation is usually
much less than the dc power passing through the filter to the
load.

Derivation of the transfer function. The purpose of the
following analysis is to derive the analytical expression for
the transfer function $V_L(s)/V_c(s)$ between the input voltage v_c
and the output voltage v_L of the filter. The analysis is pri-
marily an ac analysis and does not include any dc or transient
analyses. The transfer function $K_{op}(s)$ for the operational am-
plifier is found first. Then a circuit analysis is performed
using $K_{op}(s)$ to obtain the overall transfer function
$V_L(s)/V_c(s)$ for the active filter.

When the operational amplifier has an open loop gain
significantly higher than the closed loop gain at all frequen-
cies of interest, the closed loop gain is assumed to be equal
to the feedback impedance $Z_F(s)$ divided by the series impedance
$Z_S(s)$ [12]. In the diagram of Fig. 3, Z_S is the combination of
C_1, R_S, and C_S; and Z_F is the combination of C_F and R_F so that

$$Z_S(s) = \frac{1}{sC_1} + \frac{R_S}{1 + R_S C_S s} \tag{2}$$

and

$$Z_F(s) = \frac{R_F}{1 + R_F C_F s} . \tag{3}$$

Using (2) and (3), the transfer function $K_{op}(s)$ of the

operational amplifier is

$$K_{op}(s) = \frac{V_p(s)}{V_c(s)} = -\frac{Z_F(s)}{Z_S(s)} = -\frac{\left(1 + R_S C_S s\right) R_F C_1 s}{\left[1 + R_F C_F s\right]\left[1 + R_S\left(C_1 + C_S\right)s\right]} \quad . (4)$$

Since C_1 is a coupling capacitor, it normally has a much larger value compared with C_S; therefore C_S may be neglected in the denominator of (4) yielding

$$K_{op}(s) \cong -\frac{\left(1 + R_S C_S s\right) R_F C_1 s}{\left[1 + R_F C_F s\right]\left[1 + R_S C_1 s\right]} \quad . (5)$$

As mentioned earlier, the transfer function for the operational amplifier is derived on an assumption that the loop gain, which is the difference between the open-loop gain and the closed-loop gain of the operational amplifier is so large that the closed-loop gain can be assumed to be equal to $Z_F(s)/Z_S(s)$. This assumption limits the frequency of validity of (5) to frequencies well below the unity-gain-bandwidth frequency of the amplifier. At high frequencies, the loop gain of the operational amplifier becomes small; and the ideal approximation $K_{op}(s) = Z_F(s)/Z_S(s)$ is no longer accurate. The Analog Devices 148A operational amplifier used in Fig. 3 has a unity-gain-bandwidth product of at least 10 MHz. Since most all converters operate at switching frequencies well below this frequency the approximation is acceptable.

The operational amplifier gain $K_{op}(s)$ can be used to relate v_p and v_c as

$$V_p(s) = K_{op}(s)V_c(s) \quad . \tag{6}$$

Knowing this, Fig. 3 can be analyzed to obtain the transfer function $V_L(s)/V_c(s)$. The internal resistance of L_s and r_c are in series with R_L along the dc path. These resistances are considered to be negligible compared to R_L for all reasonable loads. Also, R_Z is large with respect to typical values of R_L so the current i_s which flows through the secondary winding N_s is assumed to flow entirely through R_L which yields

$$\frac{v_L}{v_c} = \frac{i_s R_L}{v_c} \quad . \tag{7}$$

The loop equations for the secondary and primary circuits of the mutual inductor are

$$V_c(s) = \left(sL_s + R_L\right)I_s(s) + sMI_p(s) \tag{8}$$

and

$$V_p(s) = -sMI_s(s) - \left(sL_p + r_p\right)I_p(s) \tag{9}$$

where $V_c(s)$, $V_p(s)$, $I_p(s)$, and $I_s(s)$ are the Laplace forms of the converter output voltage v_c, the primary voltage v_p, the primary current i_p, and the secondary current i_s. Solving (8) and (9) by Cramer's rule yields

$$I_s(s) = \frac{\begin{vmatrix} V_c(s) & sM \\ V_p(s) & -\left(sL_p + r_p\right) \end{vmatrix}}{\begin{vmatrix} \left(sL_s + R_L\right) & sM \\ -sM & -\left(sL_p + r_p\right) \end{vmatrix}} \quad . \tag{10}$$

Reducing the determinants in (10) yields

$$I_s(s) = \frac{-\left(sL_p + r_p\right)V_c(s) - sMV_p(s)}{-\left(sL_s + R_L\right)\left(sL_p + r_p\right) + s^2M^2} \quad . \tag{11}$$

Substituting for $V_p(s)$ by using (6) yields

$$I_s(s) = \frac{sL_p + r_p + sMK_{op}(s)}{\left(sL_s + R_L\right)\left(sL_p + r_p\right) - s^2M} V_c(s) \quad . \tag{12}$$

Rearranging (12) yields

$$I_s(s) = \frac{1 + \left(\dfrac{L_p + K_{op}(s)M}{r_p}\right)s}{\left(\dfrac{L_sL_p - M^2}{r_pR_L}\right)s^2 + \left(\dfrac{L_p}{r_p} + \dfrac{L_s}{R_L}\right)s + 1} \cdot \frac{V_c(s)}{R_L} \quad . \tag{13}$$

As previously given in (7), the load ripple voltage can be ex-
pressed as $v_L = i_s R_L$ in the time domain and as $V_L(s) = I(s)R_L$
in the Laplace form. Therefore the Laplace form of the overall
filter transfer function is

$$\frac{V_L(s)}{V_c(s)} = \frac{I_s(s)R_L}{V_c(s)} \quad . \tag{14}$$

By substituting (13) into (14) and cancelling $V_c(s)$ and R_L in
the numerator and denominator, the complete transfer function
for the active ripple filter is obtained in terms of the cir-
cuit parameters and $K_{op}(s)$ as

$$\frac{V_L(s)}{V_c(s)} = \frac{1 + \left[\dfrac{L_p + K_{op}(s)M}{r_p}\right]s}{\left[\dfrac{L_s L_p - M^2}{r_p R_L}\right]s^2 + \left[\dfrac{L_p}{r_p} + \dfrac{L_s}{R_L}\right]s + 1} \quad . \quad (15)$$

In (15) the coefficient $\left[L_s L_p - M^2\right]/\left[r_p R_L\right]$ is much smaller than $\left[L_p/r_p\right] + \left[L_s/R_L\right]$ and $L_s/R_L \ll L_p/r_p$. Also it was determined experimentally that $V_L(s)/V_c(s)$ is independent of the magnitude of R_L except when R_L takes values less than ten ohms. So if R_L is allowed to approach infinity (15) yields

$$\frac{V_L(s)}{V_c(s)} = \frac{1 + \left[\dfrac{L_p + K_{op}(s)M}{r_p}\right]s}{1 + \dfrac{L_p}{r_p}s} \quad . \quad (16)$$

Equation (5) is now substituted into (16) to obtain the approximate transfer function as

$$\frac{V_L(s)}{V_c(s)} = 1 - \frac{MR_F C_1}{r_p} \cdot \frac{\left[1 + R_S C_S s\right]s^2}{\left[1 + \dfrac{L_p}{r_p}s\right]\left[1 + R_S C_1 s\right]\left[1 + R_F C_F s\right]} \quad . \quad (17)$$

Since $V_L = V_c - V_s$, then

$$\frac{V_L(s)}{V_c(s)} = \frac{V_c(s) - V_s(s)}{V_c(s)} = 1 - \frac{V_s(s)}{V_c(s)} \quad . \quad (18)$$

A comparison of (17) and (18) yields

$$\frac{V_s(s)}{V_c(s)} = \frac{MR_F C_1}{r_p} \cdot \frac{\left[1 + R_S C_S s\right]s^2}{\left[1 + \dfrac{L_p}{r_p}s\right]\left[1 + R_S C_1 s\right]\left[1 + R_F C_F s\right]} \quad . \quad (19)$$

Equation (17) is the theoretical transfer function for the circuit shown in Fig. 3 excluding the components R_1 and C_2. The purpose of R_1 and C_2 is discussed later and another transfer function is derived which includes these components. Fig. 3 and Equation (17) will be used in the following discussion.

Design considerations. This subsection discusses certain principles of design which must be considered when designing the active filter. The discussion of these principles should contribute toward the comprehension of the circuit functions.

The coupling capacitor C_1 which is the largest capacitor in the active filter is used to block the dc voltage V' of the converter output and should have negligible effect on the ac input signal to the operational amplifier. In order to accomplish this, the reactance of C_1 must be much smaller than the input impedance of the amplifier. The closed-loop input impedance of the inverting operational amplifier is approximately the input series resistance R_S [13]. Since it is desired to keep the total capacitance in the ripple filter small, R_S should be as large as possible within the limits of amplifier performance so that C_1 may be small. C_1 is the largest capacitance in the active filter; and yet with R_S = 5110 ohms, C_1 is less than 5 μF compared with hundreds of microfarads commonly used in filters in dc to dc converters and power supplies. Therefore C_1 may be a ceramic or mica capacitor instead of the electrolytic capacitor

required when hundreds of microfarads are needed.

A variety of amplifiers can be used for the amplifier function. The operational amplifier is selected because of its versatility and because its characteristics can be easily described analytically. When the amplifier is designed, its gain should be equal to the voltage ratio v_p/v_s of the mutual inductor since the overall gain from v_c to v_s should be unity. The output voltage swing of the operational amplifier is limited by the supply voltage. Therefore, for a given voltage v_c, the voltage transformation ratio v_p/v_s of the mutual inductor must be small enough so that the amplifier gain does not have to be so large that the output voltage limit is exceeded. The ripple amplitude v_c at the output of the converter in Fig. 2(b) depends on R_L, C, the switching frequency, and the duty cycle. The converter output ripple amplitude must be determined before the closed-loop operational amplifier and the mutual inductor can be designed. If difficulty is encountered in designing the operational amplifier and mutual inductor so that the amplitude of v_c does not saturate the amplifier, the converter output capacitance C may be increased in order to reduce the amplitude of v_c.

The operational amplifier should have a wide bandwidth with the highest possible cutoff frequency. Since it is desirable that R_S is large, the feedback resistance R_F must also be large. These large resistors make the stray feedback capacitance in parallel with R_F and the stray input capacitance which

is effectively in series with R_S more significant especially at high frequencies. For these reasons, it may be necessary to add capacitors C_F or C_S in order to cancel, or balance, the effects of one or the other stray capacitances.

As mentioned earlier, the operational amplifier should have a high open-loop gain to minimize the closed-loop gain variation with frequency and should have a low quiescent power dissipation to maximize the filter effeciency. The operational amplifier may be either the integrated-circuit type or the module type. The integrated circuit is smaller and has less quiescent dissipation but the module type has higher open-loop gain to lower and higher frequencies.

All amplifiers have a limit, or peak, output current at which the amplifier is said to saturate. If it is assumed that the maximum output voltage for the amplifier has been determined, then the output current limit determines a minimum value for the primary inductance L_p at the lowest frequency of operation. For this reason, the design of the mutual inductor is discussed next keeping in mind that a minimum inductance for L_p must be established.

There is a nonlinear variation of inductance with dc bias which causes the inductance of a given winding on a core to decrease as the dc bias due to a direct current in any winding increases. This decrease in inductance affects both windings of the mutual inductor and requires that more alternating output

current be delivered by the operational amplifier. For this reason, the minimum inductance discussed in the last paragraph should be defined for full-load direct current flowing in N_s. With this condition met, the variation of the direct current does not significantly affect the performance of the filter. The inductance change due to a change in current is so small that the coefficient of coupling changes very little. It is also desirable that r_p be as small as possible so that the mutual inductor has minimum phase shift at lower frequencies.

There are two additional factors to be considered in the design of the mutual inductor. One is leakage inductance and the other is winding capacitance. Leakage inductance is important because it affects the coupling coefficient of the mutual inductor. The coupling coefficient is a maximum, near to unity, when the leakage inductance is a minimum. The design techniques used to minimize leakage inductance increase the winding capacitance. For example, the technique of bifilar winding a mutual inductor puts each turn of one winding in close proximity to each turn of the other winding and thus increases the winding capacitance. If the windings are wound separately, separated by a layer of insulation, the winding capacitance is minimized; but the leakage inductance increases due to the physical separation of the windings. It is a known fact that leakage inductance is a much more significant parameter at low frequencies than is winding capacitance [14]. Since the frequency range of interest for most dc to dc converters in which large microfarad

capacitors are used is approximately two to fifty kHz, the mutual inductor should be designed to minimize the leakage inductance of the mutual inductor.

This section has discussed some of the properties of the components of the active filter, particularly the operational amplifier and the mutual inductor. The effect that these properties have on the performance of the active filter were discussed and design techniques which can be used to minimize these effects were given. An analysis to obtain the transfer function of the basic filter configuration has already been given. The next three sections of this chapter are devoted to the derivation of the transfer functions of three specialized configurations for a narrow-bandwidth filter, a wide bandwidth filter, and a wide-bandwidth filter with feedback. In each of these sections, the theoretical transfer characteristic is compared with the experimental transfer characteristic for the filter shown in Fig. 3.

Narrow-bandwidth Filter

The characteristics of the narrow-bandwidth filter are discussed first because they best illustrate the effects of the important parameters of phase shift and gain. As the name implies, this filter has a narrow frequency bandwidth over which the attenuation is significant. This filter does not have as important applications with regard to dc supplies as the wide-

bandwidth filter. Some examples of applications are a filter
for a constant frequency dc to dc converter or a notch filter
in a system which must pass direct current with little or no at-
tenuation.

The circuit for the narrow-bandwidth filter is the cir-
cuit in Fig. 3 with C_F and C_S included but with R_1 and C_2 ex-
cluded. This circuit is the same one for which the approximate
transfer function (17) has been derived. It can be determined
by examining (18) that the attenuation of the filter approaches
a maximum when $V_S(s)/V_C(s)$ as defined in (19) approaches unity
with zero phase shift. When C_S and C_F are included in the cir-
cuit, their values are chosen to obtain maximum attenuation at
a chosen frequency. Then R_F is adjusted to obtain a maximum at-
tenuation at this frequency. The calculation of the break fre-
quencies of (19) and the magnitude of (19) at a frequency of one
Hz are given in Table II. The break frequencies due to the time
constants $R_S C_1$ and L_p/r_p are at low frequencies because C_1 and
L_p have relatively large values. Also C_S and C_F are relatively
small values of capacitance and the break frequencies due to
$R_S C_S$ and $R_F C_F$ are high.

A sketch of the Bode diagram for (19) and its asymptotic
approximation are plotted in Fig. 4 for the component values
given in Table I. From these curves, it can be seen that
$|V_S(s)/V_C(s)|$ approaches unity over a finite band of frequencies.
If only the magnitude of $V_S(s)/V_C(s)$ were considered, it would

Table II. Calculation of the break frequencies of (19).

$$\frac{V_s(s)}{V_c(s)} = \frac{MR_F C_1}{r_p} \cdot \frac{\left(1 + R_S C_S s\right)s^2}{\left(1 + R_S C_1 s\right)\left(1 + \frac{L_p}{r_p} s\right)\left(1 + R_F C_F s\right)} \qquad (19)$$

$$20 \log \frac{MR_F C_1}{r_p} \omega^2 = 20 \log \frac{35 \times 10^{-3} \times 29 \times 10^3 \times 4.7 \times 10^{-6}}{52} (2\pi)^2$$

$$= -48.84 \text{ db}$$

$$\omega_1 = \frac{1}{R_S C_1} = \frac{1}{5.1 \times 10^3 \times 4.7 \times 10^{-6}} = 41.7 \text{ rad/sec}$$

$$\omega_2 = \frac{r_p}{L_p} = \frac{52}{.203} = 256 \text{ rad/sec}$$

$$\omega_3 = \frac{1}{R_F C_F} = \frac{1}{30 \times 10^3 \times 67 \times 10^{-12}} = 4.98 \times 10^5 \text{ rad/sec}$$

$$\omega_4 = \frac{1}{R_S C_S} = \frac{1}{5.1 \times 10^3 \times 1.47 \times 10^{-10}} = 1.33 \times 10^6 \text{ rad/sec}$$

$$f_1 = \frac{\omega_1}{2\pi} = 6.64 \text{ Hz}$$

$$f_2 = \frac{\omega_2}{2\pi} = 40.8 \text{ Hz}$$

$$f_3 = \frac{\omega_3}{2\pi} = 79.2 \text{ kHz}$$

$$f_4 = \frac{\omega_4}{2\pi} = 212 \text{ kHz}$$
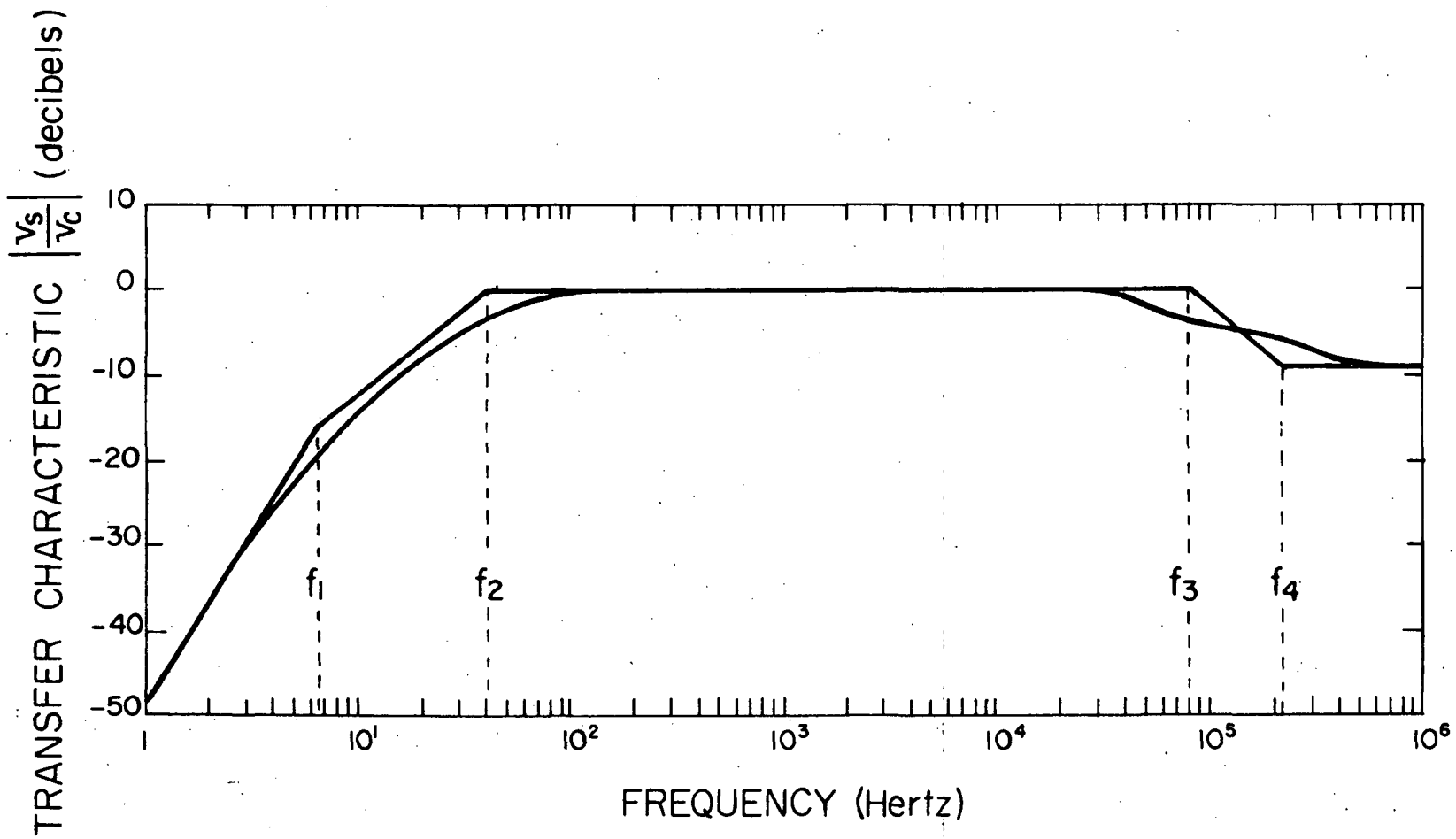
Fig. 4. The theoretical transfer characteristic for v_s/v_c in (19) with $R_L = \infty$, $C_S = 147$ pF, and $C_F = 67$ pF.

be expected that the filter attenuation would reach a maximum and stay constant over the same finite bandwidth over which (19) is equal to unity. However, the phase shift in the mutual inductor in the vicinity of f_2, and the phase shift in the operational amplifier in the vicinity of f_3 have a significant effect. When v_c and v_s have very large amplitudes, such as a few volts, compared to the millivolts of ripple desired for v_L, a tenth of a degree of phase shift between v_c and v_s can result in a significant amplitude for v_L.

Since small amounts of phase shift are so significant, the phase shifts of the operational amplifier and mutual inductor are examined separately. The 180 degree phase shifts due to inversion in the operational amplifier and the mutual inductor offset each other and therefore are not considered to be part of either phase shift. The phase shift of the operational amplifier in the frequency range of normal interest from two kHz to fifty kHz can be found by examining the expression for $K_{op}(s)$ in (5). Since $f_1 = 1/\left(2\pi R_S C_1\right) = 6.64$ Hz is very much less than the frequency range of interest, $R_S C_1 s >> 1$ and the term $1 + R_S C_1 s$ in (5) can be approximated by $R_S C_1 s$ with (5) becoming

$$K_{op}(s) \cong \frac{\left(1 + R_S C_S s\right)}{\left(1 + R_F C_F s\right)} \cdot \frac{R_F}{R_S} \quad . \tag{20}$$

Since the break frequency $f_3 = 1/\left(2\pi R_F C_F\right) = 79.2$ kHz is much lower than $f_4 = 1/\left(2\pi R_S C_S\right) = 212$ kHz, the phase shift of the

operational amplifier passes from approximately zero at 2 kHz to a lagging phase shift as the frequency increases toward 79.2 kHz. This behavior can be seen in the experimental phase characteristic for the operational amplifier in Fig. 5.

The phase shift of the mutual inductor is found by deriving the transfer function of the mutual inductor with the secondary open-circuited. The secondary voltage is

$$V_s(s) = MsI_p(s) \tag{21}$$

where $I_p(s)$, the current in the primary winding N_p, is

$$I_p(s) = \frac{V_p(s)}{r_p + sL_p} \tag{22}$$

where $V_p(s)$ is the output voltage of the operational amplifier. Substituting (22) into (21) and dividing by $V_p(s)$ yields the transfer function

$$K_M(s) = \frac{V_s(s)}{V_p(s)} = -\frac{M}{r_p} \cdot \frac{s}{1 + \frac{L_p}{r_p}s} \; . \tag{23}$$

It is obvious from (23) that the mutual inductor has approximately zero phase shift at high frequencies but has an increasing leading phase shift as the frequency is decreased toward $f_2 = r_p / \left(2\pi L_p \right) = 40.8$ Hz. The experimental phase characteristic for the mutual inductor is also given in Fig. 5. The total phase shift which is the sum of the operational amplifier and mutual inductor phase shifts is shown dashed.
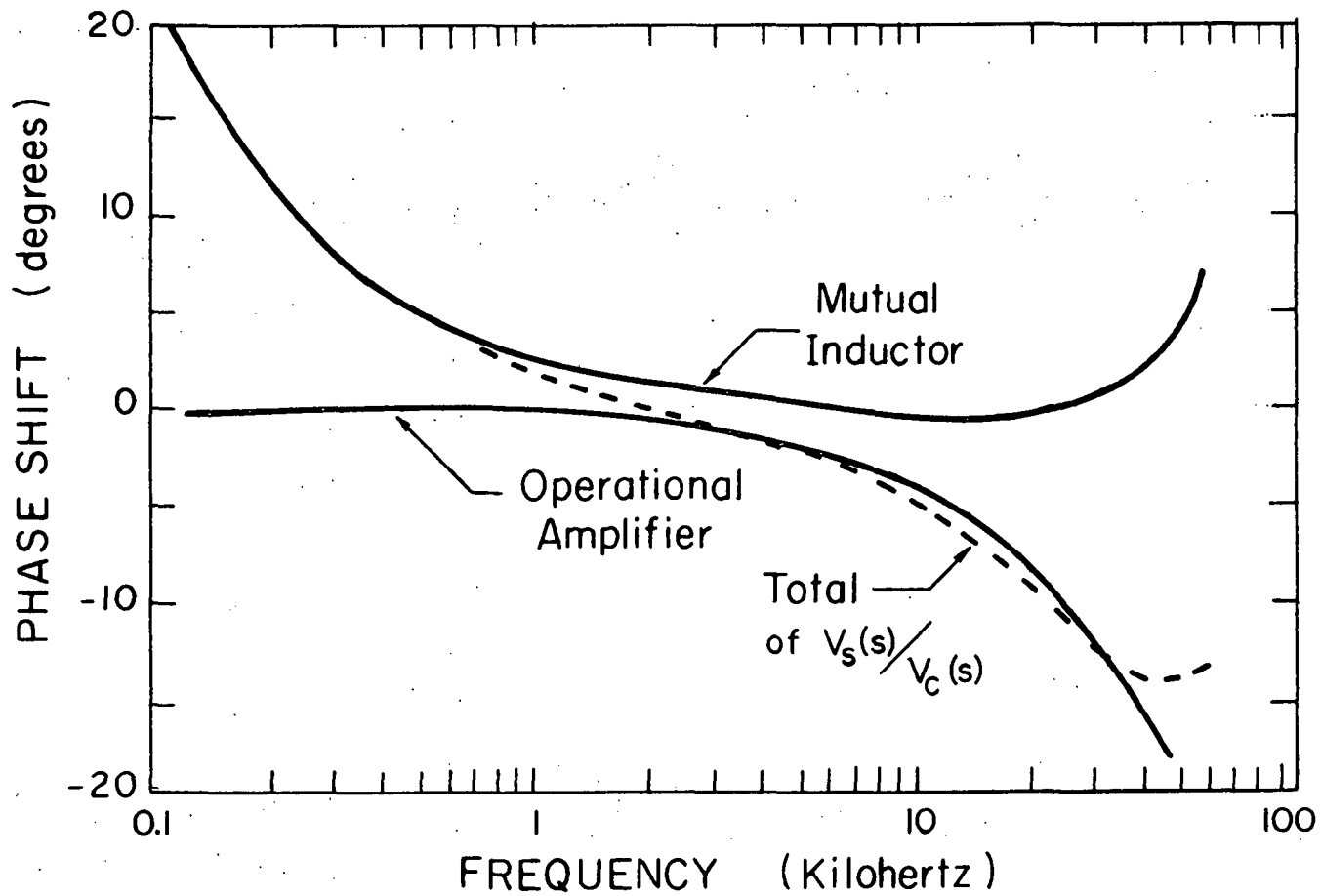
Fig. 5. Experimental phase characteristics for the narrow-bandwidth filter with $R_L = \infty$, $C_S = 147$ pF, and $C_F = 67$ pF.

Equation (15) is the complete transfer function for the narrow-bandwidth filter including R_L. Equation (17) is the approximate transfer characteristic for the narrow-bandwidth filter under the approximation that R_L can be assumed to approach infinity. Equation (17) is evaluated using the component values given in Table I and is plotted in Fig. 6. In order to verify the accuracy of the assumption that R_L may be assumed to approach infinity, transfer curves were calculated using (15) for a wide range of values of R_L. Only when R_L is 10 ohms or less, is there any significant deviation from the theoretical curve calculated using (17). Since these curves agree so closely, only (17) is plotted. Experimental data for the same circuit conditions with $R_L = \infty$ are also plotted in Fig. 6. It can be seen that the theoretical and experimental curves agree quite closely. The only significant difference being in the value of the maximum attenuation. By examining Fig. 5, it can be seen that the frequency at which the total phase shift from v_c to v_s equals zero is 2.5 kHz which is also the frequency at which maximum attenuation occurs in Fig. 6.

In this section, the configuration for the narrow-bandwidth filter has been discussed. The circuit configuration and analytical transfer function are given; and the role that the phase shifts in the operational amplifier and mutual inductor have in producing the null in the gain curve is discussed. The experimental and theoretical gain characteristics compare very closely. This configuration is discussed primarily to show the
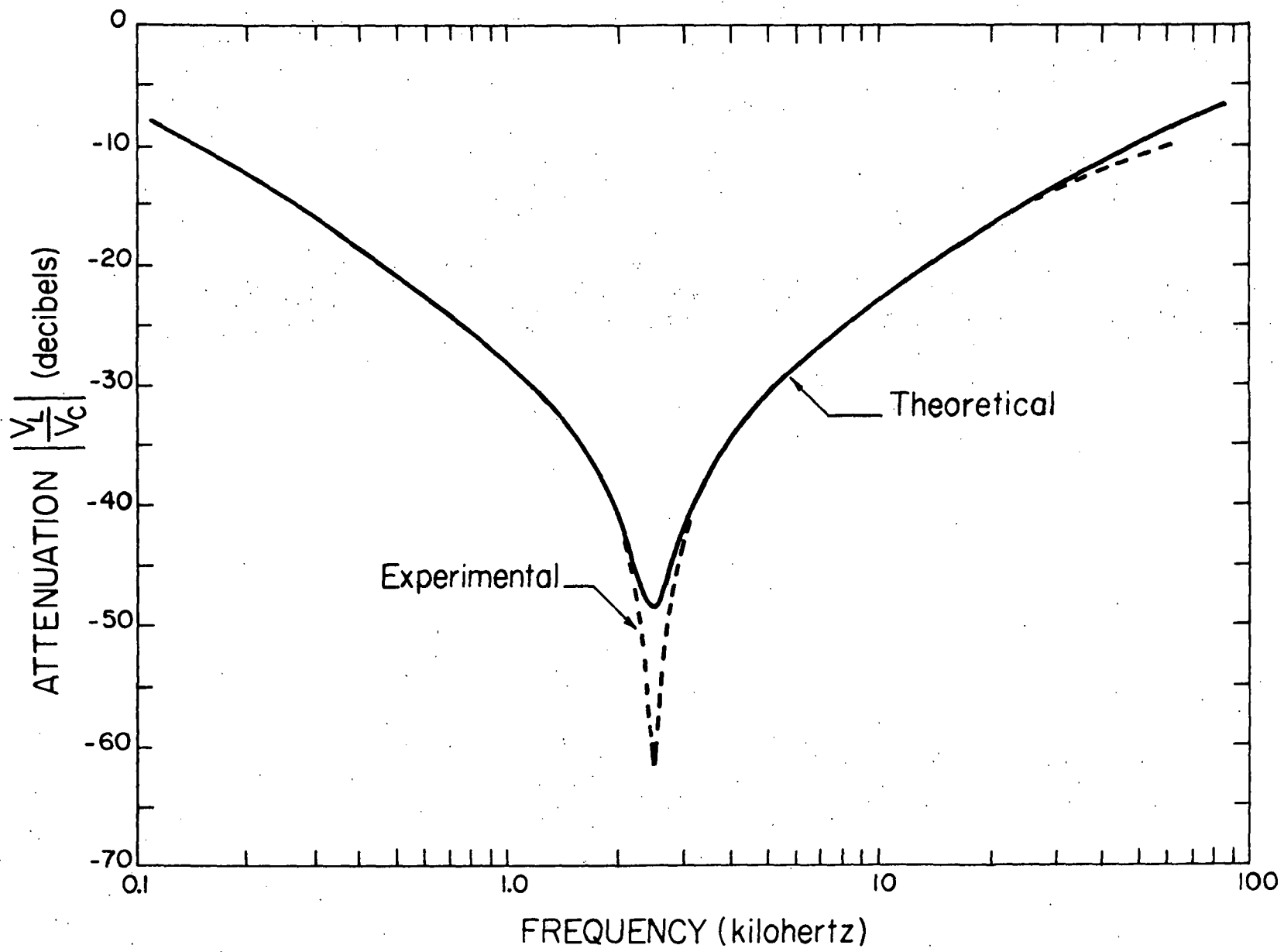
Fig. 6. Attenuation characteristics for the narrow-bandwidth filter.

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effect of phase shift on the performance of the filter. The
next section is concerned with a filter in which the phase
shift is minimized to obtain a wide-bandwidth of attenuation.

Wide-bandwidth Filter

The wide-bandwidth filter has a wide range, or bandwidth
of frequencies over which the attenuation is below a certain
specified value. The particular case which this dissertation is
concerned with is the case of a low-pass filter. A circuit con-
figuration is described in this section which achieves a close
approximation to the gain characteristic of such a filter.

In the section on the narrow-bandwidth filter, it was
shown that the dependence of the attenuation on frequency is re-
lated to the variation of the phase shifts of the operational
amplifier and mutual inductor with frequency. If the total
phase shift from these two components can be made zero over the
bandwidth desired for the filter, then the result is a wide-
bandwidth filter with a constant attenuation in that bandwidth.

The approximate transfer function for the operational
amplifier is given in (20). This equation indicates that if
$C_S = 0.0$ and $C_F = 0.0$ then the transfer function $K_{op}(s)$ of the
amplifier becomes a constant. Since $K_{op}(s)$ is then independent
of s, the amplifier should have no phase shift. The experimen-
tal phase characteristic for the operational amplifier with C_S

and C_F removed is shown in Fig. 7. The small variation from zero for the phase shift could be caused by stray parameters in the wiring or in the amplifier, or it could be instrument error especially since the angle is so small.

The transfer function $K_M(s)$ for the mutual inductor is given in (23). An examination of this function reveals that the phase shift of the mutual inductor is zero when the resistance r_p of the primary winding N_p approaches zero. However, there is a practical limit to the minimum value of r_p which makes the low-frequency attenuation dependent on the time constant L_p/r_p with a break frequency $f_2 = r_p/\left(2\pi L_p\right) = 40.8$ Hz. The experimental phase characteristic for the mutual inductor is shown in Fig. 7. This mutual inductor is the same one listed in Table I and used in the narrow-bandwidth filter. The phase shift of the mutual inductor and the operational amplifier with $C_S = 0.0$ and $C_F = 0.0$ are summed, and the total phase shift is shown dashed in Fig. 7. It can be seen that the total phase shift remains fairly close to zero over a relatively wide bandwidth compared to the total phase shift in Fig. 5.

From the preceding discussion, $C_S = 0.0$ and $C_F = 0.0$ for the wide-bandwidth filter; therefore the theoretical transfer function can be obtained by letting $C_S = 0.0$ and $C_F = 0.0$ in the transfer function (17) for the narrow-bandwidth filter yielding
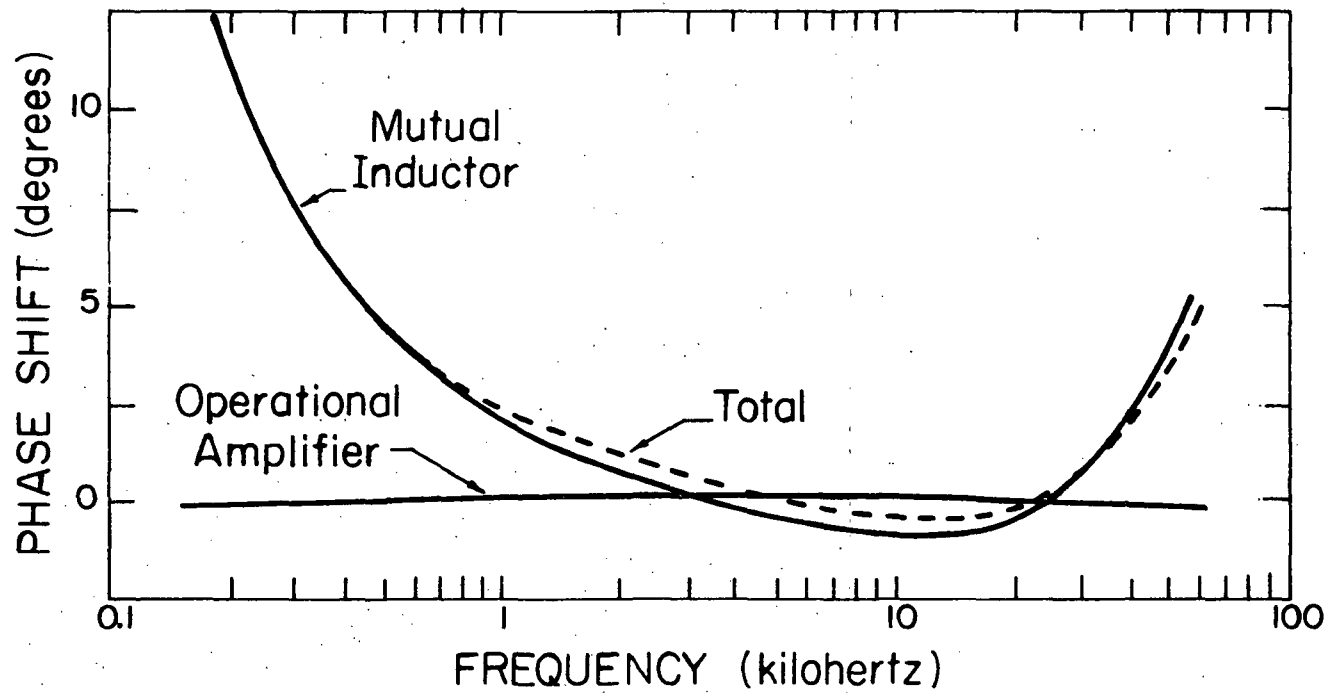
Fig. 7.   Experimental phase characteristics for the wide-band-width filter with $R_L = \infty$, $C_S = 0$ and $C_F = 0$.

$$\frac{V_L(s)}{V_c(s)} = 1 - \frac{MR_FC_1}{r_p} \cdot \frac{s^2}{\left(1 + \frac{L_p}{r_p} s\right)\left(1 + R_SC_1 s\right)} \quad . \quad (24)$$

The theoretical gain characteristic calculated using (24) and the experimental gain characteristic are shown in Fig. 8. The two curves agree closely except above thirty kHz as the phase shift increases above zero causing the experimental attenuation to decrease. This phase shift is probably caused by stray capacitance which is not included in the theoretical curve (24). It is also noted that the slope of these characteristics at low frequencies is -20 db per decade. This slope is only half that of a low-pass L-section filter. It is desirable therefore that the filter be improved in order to increase its attenuation which is the purpose of the filter configuration discussed in the next section.

Wide-bandwidth Filter with Feedback

The wide-bandwidth filter with feedback is the one out of the three filters that is the most important from the viewpoint of an application as a filter for a dc to dc converter because its transfer characteristic has the greatest attenuation. The circuit configuration is the same as the wide-bandwidth filter with $C_S = 0.0$ and $C_F = 0.0$ in Fig. 3 except that a second input is added to the operational amplifier. This input is feedback from the load ripple voltage v_L to the input of the
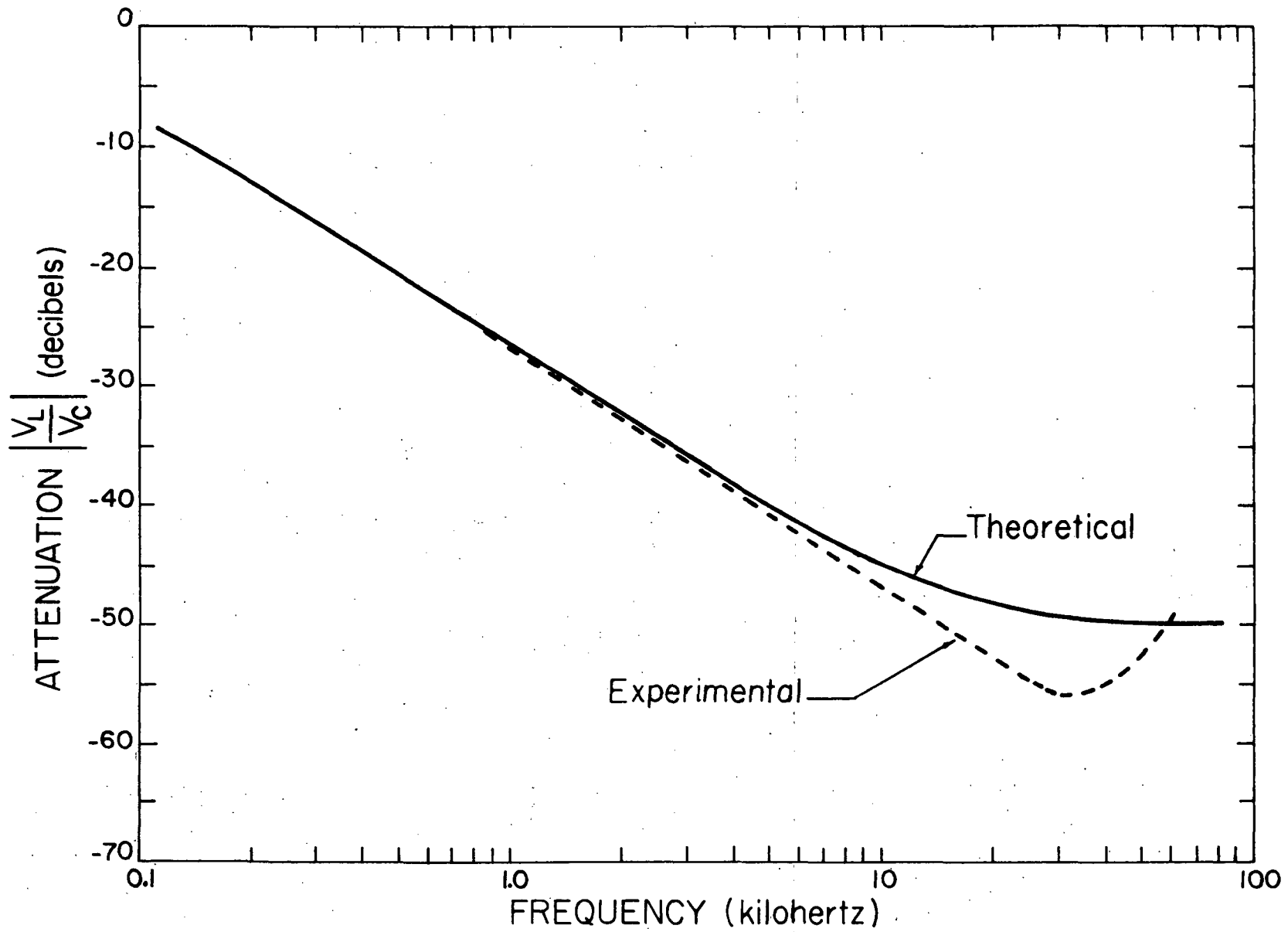
Fig. 8. Attenuation characteristics for the wide-bandwidth filter.

operational amplifier. The feedback path that is added is made up of R_1 and C_2 shown dashed in Fig. 3 so that the wide-bandwidth filter with feedback is the circuit in Fig. 3 including R_1 and C_2 but not including C_S or C_F.

The feedback works in the following manner. The load ripple voltage v_L is non-zero when v_c and v_s are not exactly equal in magnitude and phase. Since v_L is the difference $v_c - v_s$, v_L can be thought of as an error voltage. The converter output voltage v_c is the known voltage to be eliminated; therefore, if v_L is nonzero then v_s is the voltage in error. The addition of feedback through R_1 and C_2 adds the error voltage v_L, times a gain factor, to v_s in such a manner as to decrease the amplitude of v_L. This qualitative explanation may be better understood by examining the following derivation of the transfer function of the wide-bandwidth filter with feedback.

The transfer function $K_{op}(s)$ in (5) for the operational amplifier and the transfer function $K_M(s)$ in (23) for the mutual inductor have been derived. At this time, a new transfer function $K_F(s)$ for the feedback path through R_1 and C_2 is derived from the ratio of the impedance of the feedback elements R_F and C_F and the impedance of the series elements R_1 and C_2 as

$$K_F(s) = \frac{V_p(s)}{V_L(s)} = \frac{-R_F C_2 s}{\left(1 + R_F C_F s\right)\left(1 + R_1 C_2 s\right)} \quad . \quad (25)$$

Since the two inputs are summed through the operational

amplifier, the output voltage $V_p(s)$ of the amplifier is

$$V_p(s) = K_{op}(s)V_c(s) + K_F(s)V_L(s) \quad . \qquad (26)$$

The secondary voltage $V_s(s)$ of the mutual inductor is obtained by using $K_M(s)$ in (23) and $V_p(s)$ in (26) as

$$V_s(s) = K_M(s)V_p(s) = K_M(s)\left[K_{op}(s)V_c(s) + K_F(s)V_L(s)\right]. \quad (27)$$

Starting with

$$V_L(s) = V_c(s) - V_s(s) \qquad (28)$$

and substituting $V_s(s)$ from (27) into (28) yields

$$V_L(s) = V_c(s) - K_M(s)K_{op}(s)V_c(s) - K_M(s)K_F(s)V_L(s) \qquad (29)$$

which can be reduced into the form

$$\frac{V_L(s)}{V_c(s)} = \frac{1 - K_M(s)K_{op}(s)}{1 + K_M(s)K_F(s)} \quad . \qquad (30)$$

Equation (30) is the transfer function for the wide-bandwidth filter with feedback. When $K_F(s) = 0.0$, (30) becomes the transfer function for the wide-bandwidth filter without feedback. Also, it can be seen that the attenuation of the filter with feedback is greater than the attenuation of the filter without feedback whenever $|1 + K_M(s)K_F(s)| > 1$. When $K_{op}(s)$ from (3), $K_M(s)$ from (23), and $K_F(s)$ from (25) are substituted in (30), (30) becomes

$$\frac{V_L(s)}{V_c(s)} = \frac{\left(1 + R_F C_F s\right)\left(1 + R_S C_1 s\right)\left(1 + \frac{L_p}{r_p} s\right) - \frac{MR_F C_1}{r_p}\left(1 + R_S C_S s\right)s^2}{\left(1 + R_F C_F s\right)\left(1 + R_S C_1 s\right)\left(1 + \frac{L_p}{r_p} s\right) + \frac{MR_F C_2\left(1 + R_S C_1 s\right)s^2}{r_p\left(1 + R_1 C_2 s\right)}}$$

$$(31)$$

Using the values of the circuit parameters given in Table I, the theoretical characteristic curve for (31) is calculated; and the resulting theoretical curve as well as the experimental curve are shown in Fig. 9. Both curves have a steep initial negative slope; and at approximately 2 kHz, the slope begins to increase toward zero more sharply for the experimental curve than for the theoretical curve. At high frequencies, the experimental attenuation decreases while the theoretical attenuation reaches a constant level. The experimental curve for the wide-bandwidth filter without feedback showed the same property which is attributable to stray parameters in the circuit of the amplifier. The initial slopes of the two curves are approximately -40 db per decade which is the slope of the characteristic for an L-section filter. A comparison of these two filters is given later.

By comparing Figs. 6, 8, and 9, it can be seen that the attenuation characteristic for the wide-bandwidth filter with feedback reaches a greater attenuation at a lower frequency and maintains a large attenuation for at least a decade of frequencies. The wide-bandwidth filter with feedback is therefore the
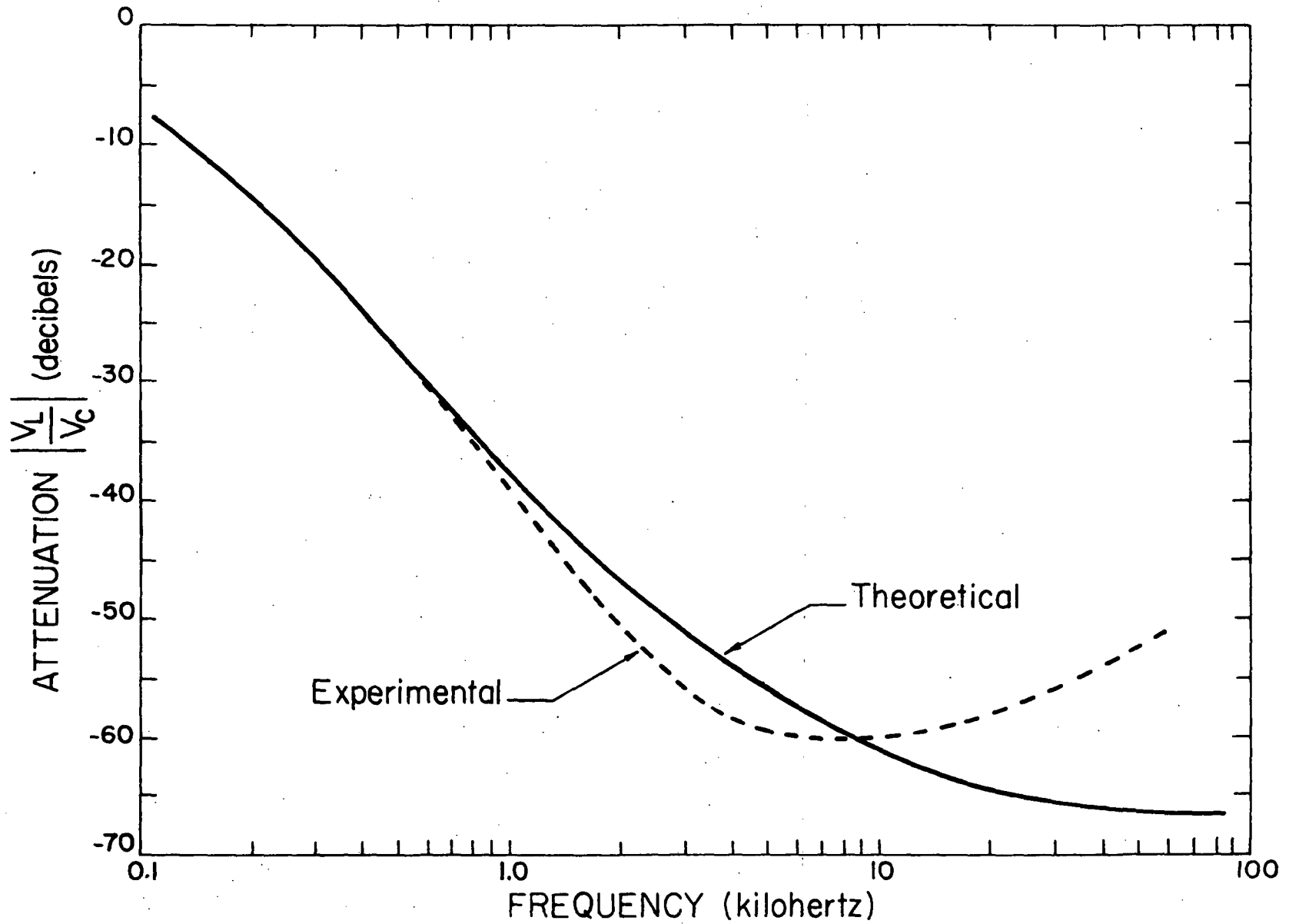
Fig. 9. Attenuation characteristics for the wide-bandwidth filter with feedback.

the most logical choice for use with dc to dc converters because practically all of these circuits either have a variable frequency of operation or a highly nonlinear output ripple waveform which contains a number of large-amplitude harmonics. This filter is slightly more complex than the narrow-bandwidth filter or the wide-bandwidth filter; nevertheless, it is still the best choice. For this reason, the emphasis in the next section is on the wide-bandwidth filter with feedback.

Conclusions

This chapter begins with background information on the necessity for reducing the hundreds of microfarads of capacitance needed in the output filters for switching dc to dc converters. A brief description is given describing the basic principles of switching dc to dc converters. The function of the passive L-section output filter and the basic principle of the active filter are then given using block diagrams. The circuit diagram of the active filter is given next and its transfer function is derived. Principles which should be followed when designing the active filter are given and each of the three filter configurations are then discussed. The narrow-bandwidth filter configuration is discussed first. The narrow-bandwidth of attenuation is shown to be a function of the phase characteristics of the operational amplifier and the mutual inductor. The wide-bandwidth filter configuration is developed next by

minimizing the phase shift in the operational amplifier. Finally, feedback is added from the load to the input of the operational amplifier to produce the wide-bandwidth filter with feedback. This last filter is the most important in applications with dc to dc converters because it has the widest bandwidth of attenuation and its attenuation characteristic most nearly approximates that of an L-section filter. The theoretical attenuation characteristics obtained from the derived transfer functions and the experimental characteristics for each configuration are plotted. The theoretical and experimental curves compare favorably in each case.

An attempt is not made to analyze the active filter in a closed-loop converter system. The mathematical relations in such a system would be at least fourth order relations. The transient performance and the ripple attenuation of the active filter in Fig. 3, however, were tested by replacing the existing passive filter in a breadboard converter with the wide-bandwidth filter with feedback. The ripple attenuation was found to be commensurate with the characteristics given in Fig. 9 and the output ripple amplitude was essentially the same as the ripple amplitude when the original passive filter is used. The transient response of the output voltage to step changes in source voltage and load was tested using the active filter and was found to be essentially the same as the transient response when the original passive filter was used. An intuitive justification of the close comparison of the transient response may be

that the attenuation characteristic of the passive L-section filter has a -40 db per decade slope and the attenuation characteristic for the wide-bandwidth filter with feedback in Fig. 9 also has a -40 db per decade slope. The original L-section filter with large capacitance has therefore been replaced by the active filter which even though it requires only small capacitance has approximately the same characteristic as the L-section filter.

The similarity between the attenuation characteristic of an L-section filter and that of the wide-bandwidth filter with feedback in Fig. 9 suggests comparing the required capacitance for each filter that yields approximately the same attenuation characteristic. The slope of the experimental curve in Fig. 9 is -40 db per decade from 0.1 to 4 kHz. If the slope is extended toward lower frequencies, it intersects the zero db axis at 100 Hz. An L-section filter with the same attenuation characteristic over that frequency range requires that $\left[L_f C_f\right]^{-1/2} = 2\pi(100)$. The same value of secondary inductance $L_s = 6.2$ mH used in the mutual inductor of the active filter is used in the L-section filter so that $L_f = 6.2$ mH. Then it follows that $C_f = 408.5$ μF which can be compared with a total capacitance in the active filter of $C_1 + C_2 = 4.87$ μF. This represents an 84 to 1 saving in capacitance.

The discussion that was given on the effect that the phase shift of the operational amplifier and the mutual inductor have on the attenuation characteristic suggests possible

improvements that might be made to the filter. The high-frequency portion of the attenuation characteristic can be improved by using an amplifier which has a higher frequency response and smaller magnitudes of stray parameters. Stray parameters might also be reduced if the filter were built on a printed circuit board instead of a breadboard to minimize the lengths of connecting paths. The high-frequency attenuation of the filter can also be improved by adding a small capacitor on the order of C_1 in parallel with the load. The low frequency performance is determined by break frequency $f_2 = L_p/\left(2\pi r_p\right)$. This indicates that the attenuation can be improved by designing the primary inductance L_p with a higher $Q = \omega L_p/r_p$. The discussion in this paragraph has indicated that improvement in the attenuation characteristic of the active filter can also be obtained by using more exact phase compensation.

In summary, it is known that the active filter uses a mutual inductor which provides a highly efficient dc path and that the operational amplifier dissipates only a small amount of fixed quiescent power so that the active filter has a high efficiency especially at high dc power levels. Also it is obvious from Table I that the circuit requires only small amounts of capacitance. The secondary winding N_s and the core of the mutual inductor are essentially the same size as an L-section filter using an inductance L_f equal to the secondary inductance L_s of the mutual inductor. The additional size and weight of the primary winding N_p and the operational amplifier with components

is no more than the additional size and weight of the tantalum capacitors required in the L-section filter; therefore the active filter does not have a greater size and weight than the L-section filter. The theoretical and experimental attenuation characteristics for the wide-bandwidth filter with feedback indicate that the wide-bandwidth filter with feedback achieves approximately the same attenuation as an L-section filter; and a comparison of the capacitances required for the active and L-section filters shows a significant capacitance advantage for the wide-bandwidth filter with feedback. These characteristics satisfy all of the objectives given in the first part of the chapter.

The primary advantage of this active filter is the reduction in the microfarads of capacitance required in output filters for dc power supplies. The reduction in capacitance enables the designer to use capacitors such as ceramic or mica. These capacitors are much more reliable than the electrolytic types of capacitors such as tantalum. The active filter is essentially non-dissipative requiring only a small amount of quiescent power for the bias of the amplifier. Because the attenuation characteristic of this filter is so similar to that of an L-section filter, it can be used in applications where highly reliable power supplies are required. One of these applications is in dc to dc converters especially those used in outer space where the vacuum and the extreme variations in temperature are known to cause failures in electrolytic capacitors. They can be

used in other dc supplies where long life is essential such as
in unmanned Arctic and oceanic stations. The active filter may
also be used in dc to dc converters and power supplies in com-
puters to improve their reliability. Reliability is important
to the operating expense of large computers since improved reli-
ability results in less maintenance which is expensive. The
wide-bandwidth filter with feedback can be used in virtually any
dc to dc converter or power supply to reduce the required capac-
itance and in so doing to improve the reliability.

Chapter III

DESIGN OF A MEGAHERTZ DC TO DC CONVERTER

This chapter discusses the design of a 20 watt dc to dc converter operating with high efficiency at a switching frequency of approximately 1 MHz and a regulated output voltage of 28 volts. The output power and voltage are typical values used in unmanned spacecraft and some other aerospace applications; but the switching frequency of 1 MHz is unusually high. DC to dc converters are normally designed to operate in the frequency range of 2 to 20 kHz in order to accomplish a compromise between high efficiency and small size and weight. There are several reasons for designing this converter at a switching frequency of 1 MHz. The first is that an increase in frequency is usually accompanied by a reduction in the size and weight of the circuitry. This size and weight reduction is especially pronounced in the output filter where large amounts of capacitance and inductance are required when switching frequencies are from 2 to 20 kHz. A second reason is that the reduced amount of capacitance required to filter the 1 MHz switching waveform can result in eliminating the need for relatively low reliability electrolytic filter capacitors. Ceramic or mica capacitors could be used to improve the reliability of the converter. Reduction in

(53)

size and weight and improved reliability are desirable proper-
ties for any converter if an unacceptable loss in efficiency is
not created by increasing the switching frequency. The third
and most important reason for designing a 1 MHz converter is
that there are experiments planned for satellites to measure
electromagnetic radiation in outer space within the frequency
range of 0.2 to 100 kHz [15]. A converter operating at a switch-
ing frequency of 1 MHz would not emit electromagnetic radiation
that would interfere with these experiments. An additional ad-
vantage of the 1 MHz converter is that since the operating fre-
quency of the converter is so high the system should be capable
of responding faster to source voltage and load transients than
the low-frequency converters. The major reason dc to dc con-
verters have not been designed to operate at frequencies ap-
proaching 1 MHz is that components have not been available that
would operate at that frequency at a sufficiently high effi-
ciency. These components are becoming available but the task
remains to devise adequate design techniques at these frequen-
cies.

This chapter discusses the design of a 1 MHz energy-
storage type converter. The discussion begins with information
on the properties of the components to be used and design con-
siderations at 1 MHz. Reasons for choosing an energy-storage
type circuit and the design of the converter are given next.
Finally some experimental results are given followed by the con-
clusions.

Design Principles at High
Switching Frequencies

The design of a 1 MHz converter begins with a study of circuit components in order to determine the type of each component needed to obtain adequate efficiency and switching times. Each of these components has an upper frequency limit below which it must operate. The lowest of these frequencies is the highest frequency at which the converter may operate.

Capacitors. At frequencies near 1 MHz the lead inductance and internal resistance of electrolytic capacitors become significant. One MHz can easily exceed the resonant frequency of a large-microfarad electrolytic capacitor so that it appears inductive [16]. The internal power loss of electrolytic capacitors increases significantly at high frequencies [17]. Both of these factors cause the filtering ability and response of the capacitor to be impaired. For these reasons, high-Q capacitors such as ceramic, mica, or solid tantalum must be used. These capacitors are only available in values up to several microfarads; but as mentioned in Chapter II, they are significantly more reliable than electrolytic capacitors. Since the converter frequency is so high, the required microfarads for filter, bypass, and coupling capacitors are small; and, consequently, the microfarads of the low-capacitance high-Q capacitors are adequate.

Magnetic components. If the capacitors must be high-Q,
then the magnetic components such as inductors, mutual induc-
tors, and transformers must also be low-loss, or high-Q. Ex-
perimental data in manufacturers' catalogs indicates that total
magnetic material losses, including hysteresis and eddy-current
losses, increase significantly with frequency. For this reason,
eddy-current losses are more significant at very high frequen-
cies. Typical converters have used square B-H characteristic
materials which are either tape-wound in toroids or stacked lam-
inations. These components have high eddy-current losses at
high frequencies and are not recommended for use above 500 kHz
[8]. Another commonly used magnetic core material is powdered
permalloy which has a linear B-H characteristic; however, this
material has high losses above 200 kHz [19]. There are two ma-
terials remaining to choose. One is air and another is ferrite.
Both of these materials exhibit linear B-H characteristics and
are used to design high-frequency inductors and mutual inductors
in the megahertz range. The high reluctance and low permeabil-
ity of air result in a large amount of leakage inductance which
makes it undesirable for use in switching applications. The en-
ergy stored in the leakage inductance must be dissipated in the
circuit components during switching. These circuit losses eas-
ily become much greater than the core loss which would be pres-
ent if a ferrite material were used. Also, the stray magnetic
field associated with the leakage inductance by coupling with
other parts of the circuit can cause false triggering of

switching circuits. Therefore, an air core inductor would have to be shielded. A ferrite pot core has less leakage flux and inherent shielding as a result of its physical configuration.

Winding capacitance also may have a detrimental effect on the high frequency performance of an inductor. Unfortunately, most of the design principles used to reduce leakage inductance bring the windings in closer proximity which causes an increase in winding capacitance. However, when large currents are switched at high frequencies and the source impedance and load are small, the effect of leakage inductance is much more significant than the effect of winding capacitance [14]. This effect is directly related to the inductive time constants found by dividing the leakage inductance by the source resistance or load. Since large currents are switched in the inductors of energy-storage converters, the design is primarily concerned with reducing the leakage inductance, or maximizing the coupling coefficient.

Wire. Frequencies near 1 MHz also produce significant skin effect. Litz wire may be used up to sine-wave frequencies of 0.5 to 2 MHz to reduce skin effect. However, as the frequency increases above these frequencies, irregularities in stranding and capacitance between individual strands causes Litz wire to become progressively less advantageous [20]. Switching at a rate near 1 MHz requires a much faster response than a sinusoidal signal at 1 MHz does, due to the rapid rise and fall

times of the waveform. For this reason, Litz wire is not any better than solid copper wire at switching frequencies near 1 MHz.

Semiconductors. Now that the considerations for the passive components have been studied, it is necessary to find semiconductors which operate efficiently at the required voltage, current, and frequency. Semiconductors are required that switch several amperes with very fast rise and fall times and block at least thirty to fifty volts reverse voltage. Since a switching element must switch at least once in every half cycle, a rough estimate of the switching times for turning-on and turning-off can be obtained as fifty nsec by taking ten percent of a half period of 1 MHz. This means that the rise and fall times of a transistor or diode must be less than fifty nsec when switching several amperes if efficient switching is to be accomplished.

A comprehensive search of conventional diode specifications reveals that ion-implanted diodes are available which have reverse recovery times of 9 nsec, with a forward current of 0.6 amperes (Isofilm International 10A26) and 10 nsec with a forward current of 3 amperes (Isofilm International 10R2). They have forward recovery times of 0.5 nsec and 1.0 nsec respectively and peak reverse voltages PRV of 100 volts. These diodes are more than adequate for use in the converter.

An investigation of controlled switching devices quickly reveals that the response of devices such as unijunction transistors and thyristors are well below that required for operation near 1 MHz. There are field-effect transistors with very fast switching speeds but they are not capable of processing adequate power levels. The remaining devices to be examined are the other types of transistors. Unfortunately, transistor technology is lagging diode technology in the area of switching time; and the switching time of the transistor is the factor which determines the upper limit on the switching frequency of the converter. Manufacturers are developing ion-implanted transistors which should be very useful in increasing the switching frequencies of converters. A continuing search of transistor specifications yields several transistors designed for computer circuits which can switch up to approximately 1.5 amperes efficiently at a frequency of 1 MHz. However, these transistors are not designed for power applications. Further searching has uncovered two Solitron NPN power transistor switches. One (SDT6106) switches 2 amperes on or off in 50 nsec, and has a maximum collector current rating of 5 amperes and a collector to emitter blocking voltage of 50 volts. This transistor is ideal as the driver for the second transistor (SDT6116) which switches 5 amperes on or off in 75 nsec and has a maximum collector current rating of 10 amperes and a collector to emitter blocking voltage of 50 volts. The saturation voltages of these transistors are sufficiently low (0.8 to 1.0 volts) to permit efficient power conversion.

In any regulated energy storage dc to dc converter, it is necessary to generate a controlled duty cycle. At a frequency near 1 MHz, problems with stray pickup between parts of the circuit would be expected if the circuit is constructed of discrete components. Particular care would have to be taken in planning the physical layout of such a circuit. However, since the duty cycle generator is normally required to deliver a low power signal, this problem can be minimized if integrated circuits are used. There are a number of circuits available that are designed for use in computer logic circuits which are ideal for a duty cycle generator at 1 MHz. One of these is the 710 series of differential voltage comparators. These devices have an output current capability of 10 ma and dissipate typically only 110 mw. These circuits can operate as hysteretic or Schmitt trigger circuits capable of producing an output voltage which switches from -0.5 volts to -3.2 volts with switching times on the order of 40 nsec.

Physical layout. The physical layout of a circuit operating near 1 MHz is very important. As has been mentioned before, it is easy to have stray magnetic induction which results in undesirable coupling causing false-triggering, oscillations, or other deterioration of the performance of the circuit. In order to avoid these problems, shielded cables should be used whenever possible and especially when long leads are required, all connecting wires both shielded and unshielded should be kept as short as possible, and circuit complexity should be minimized.

Other shielding besides shielded cables should be used to isolate the sensitive small-signal parts of the circuit from the high-current switching parts of the circuit. Ground return paths should be well planned to avoid having high-current paths near the sensitive circuits and also to minimize the lengths of the high-current switching paths which are most likely to have stray magnetic fields which could interfere with the normal operation of the circuit. In addition, all points in the circuit easily affected by stray noise such as the input to an amplifier having a high input impedance should be bypassed with high-Q high frequency capacitors.

So far in this chapter, background reasons for designing a 1MHz dc to dc converter and some principles of design at this high frequency have been discussed. In addition, the transistors, diodes, and magnetic material have been selected in accordance with these principles. The components and principles discussed in this section are utilized in the next section to obtain the complete circuit design.

Block Diagram of a Regulated 1 MHz DC to DC Power Converter

The design is presented by dividing the converter into functional circuits and discussing each separately. Initially a block diagram of the converter is given and discussed to provide a better understanding of the function of each circuit and its

contribution to the operation of the whole converter. Each circuit is discussed in greater detail in subsections of the dissertation. These subsections contain theoretical explanations, design procedures, and design examples yielding the actual components used for each circuit.

The block diagram. The block diagram is shown in Fig. 10. The dc source in an unmanned spacecraft is normally a battery charged from solar cell panels. The voltage of this source fluctuates significantly. For experimental measurements for this dissertation a regulated power supply is used for the battery and solar cells. The power circuit block contains the power conversion circuits. In order to accomplish a change in dc voltage, the dc energy must be converted to ac energy and rectified [21]. The power circuit block performs these functions using a saturating power transistor as an oscillating power switch to generate the ac and a diode to rectify.

The dc or rectified waveform from the power circuit must be filtered in order to obtain a low-ripple output voltage. This function is performed by the output filter block which is normally either a pure capacitance or a pi-network low-pass filter. The load in this circuit is simply a pure resistive element.

Regulation is obtained by a combination of the functions of the three blocks in the lower part of the diagram. The differential voltage comparator circuit has two direct-voltage input thresholds with a difference of only millivolts. When the
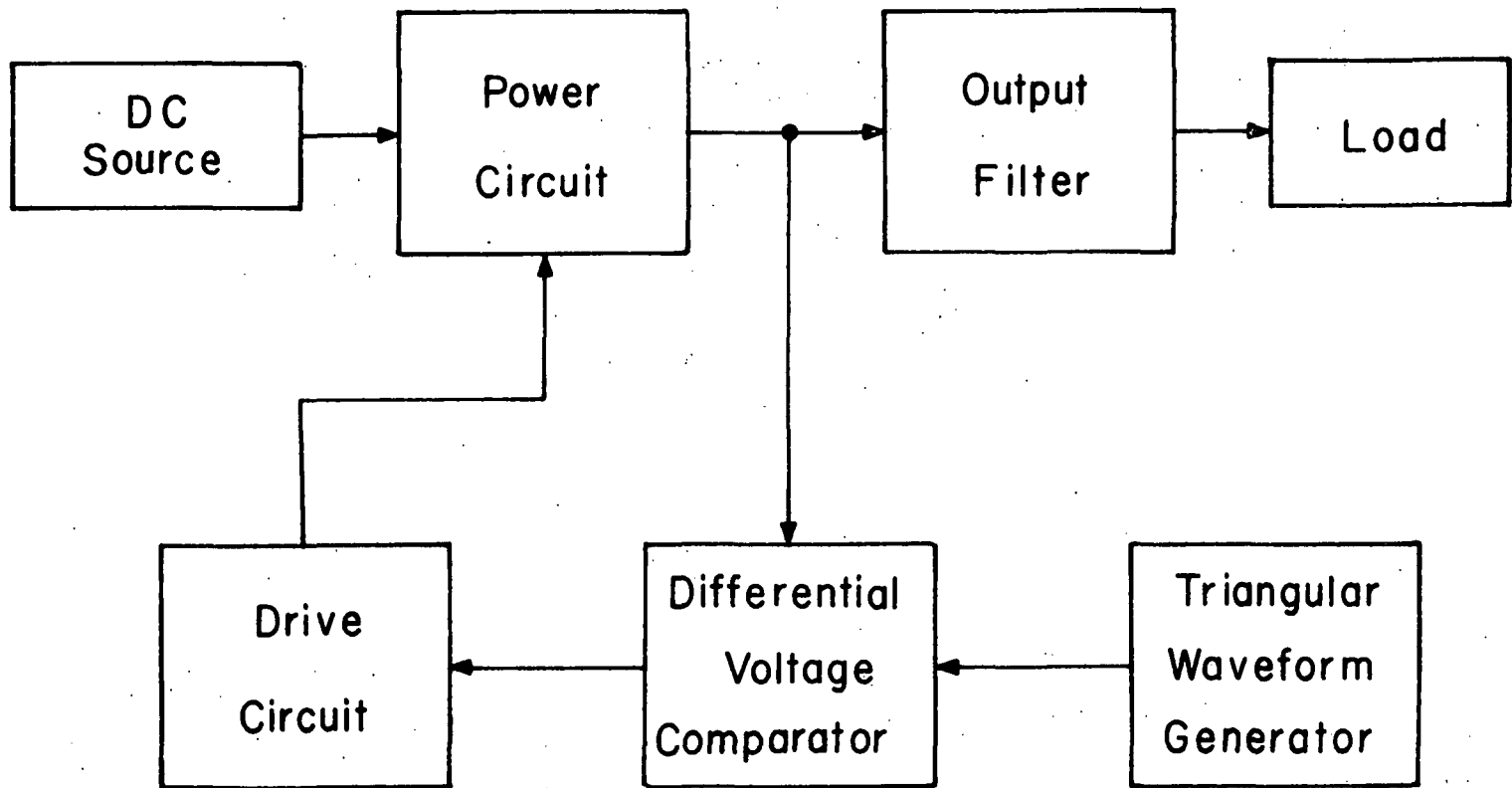
Fig. 10.   Block diagram of the converter.

applied direct voltage rises above the higher threshold, the comparator output voltage is positive and remains in this state until the applied dc voltage falls below the lower threshold when its output voltage either becomes zero or negative.

In order to obtain a constant frequency of oscillation of 1 MHz, a 1 MHz triangular waveform generator is added to the input of the comparator circuit as shown in Fig. 10. The output of the comparator becomes a pulsed voltage with a constant frequency of 1 MHz. The duty cycle of the pulsed voltage which controls the power switch in the power circuit varies inversely with the dc voltage applied to the input of the comparator circuit and thus maintains regulation.

The comparator circuit does not supply enough current to drive the power transistor in the power circuit. The drive circuit is designed, therefore, to provide sufficient forward bias to hold the power transistor in saturation and to provide a rapidly switched reverse bias to enable the power transistor to switch rapidly and efficiently.

It can be seen that the block diagram in Fig. 10 forms a closed loop capable of maintaining a regulated output voltage. A complete schematic diagram is shown in Fig. 11 and the component parts list is given in Table 3. Dotted lines are used to separate each section of the schematic diagram corresponding to a block in Fig. 10 and each section is labelled. Figs. 10 and 11 can be used to relate the schematic diagrams of the circuit
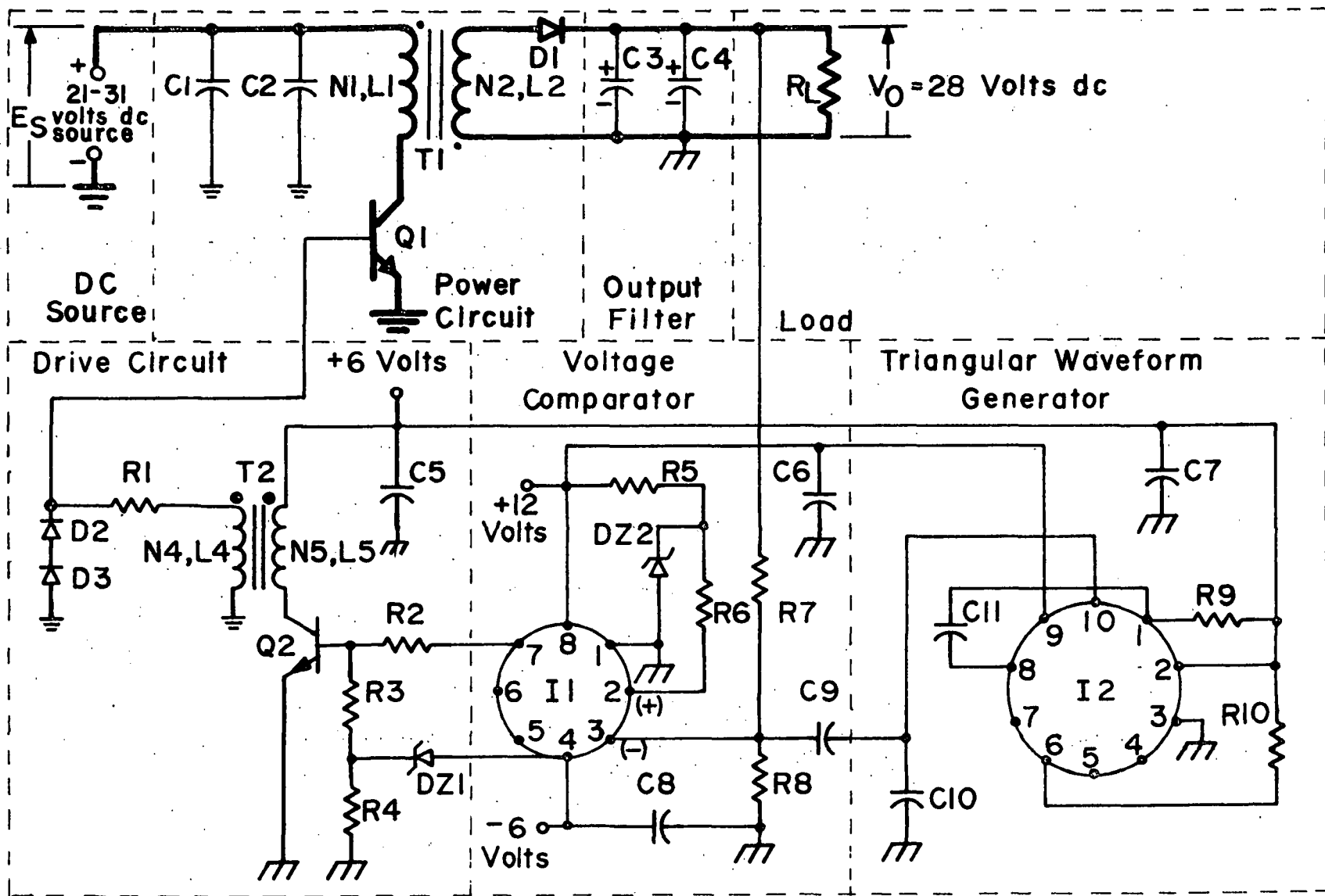
Fig. 11. Schematic diagram of the converter.

Table III. Components list for the converter.

C1,C2	0.5 μF 100 V disc ceramic
C3,C4,C5	4.7 μF 50 V solid tantalum (Erie)
C6,C7,C8,C9	0.1 μF 500 V disc ceramic
C10	1500 pF 1000 V disc ceramic
C11	33 pF 1000 V disc ceramic
D1	10R2 (Isofilm International)
D2,D3	10A26 (Isofilm International)
DZ1	1N750
DZ2	1N751
I1	SN72710L Differential Comparator (TI)
I2	CA3000 DC Amplifier (RCA)
L1	33 μH
L2	131.5 μH
L4,L5	1 mH
N1	4 turns #19 AWG
N2	8 turns #21 AWG
N4,N5	49 turns #26 AWG bifilar wound
Q1	SDT6115 (Solitron Devices, Inc.)
Q2	SDT6106 (Solitron Devices, Inc.)
R1	10 Ω
R2	22 Ω
R3	470 Ω
R4	1.8 kΩ
R5	2.7 kΩ
R6	12 kΩ
R7	69.8 kΩ
R8	14.3 kΩ
R9,R10	1.0 kΩ
R_L	26 Ω to ∞
T1	2616P-3D3 UG (Ferroxcube, Corp.)
T2	768T188/3D3 (Ferroxcube, Corp.)

blocks which are discussed separately in the following subsections.

The Power Circuit

The first step in designing a nondissipative switching converter that operates near a frequency of 1 MHz with a relatively high efficiency is to decide which of the current types of power converters is best suited for operation at these high frequencies. From among the possible dc to dc converter configurations including energy-storage converters [22] and parallel inverters with voltage-feedback [11] or current-feedback [23], the energy-storage converter is chosen for the following reasons: (1) The circuit is less complex requiring a minimum number of components including only one transistor switch used in conjunction with a switching diode. (2) Power dissipation should be high in the switching power transistor for any converter. Since the energy-storage converter requires only one power transistor, it is most likely to have smaller total switching losses than the parallel inverter which requires two switching transistors and, additionally, some form of full-wave rectification. (3) The energy-storage converter uses inductive transformation which does not require driving the magnetic material to saturation and uses a core material with a linear B-H characteristic which is available in materials such as ferrite which are designed for efficient operation at frequencies near 1

MHz. (4) Since the transistor and diode currents are transfer-
red one for the other during the switching times in the energy-
storage converter, delay time and storage time in the power
switching transistor do not produce switching loss but are im-
portant only so far as they are concerned with the duty cycle,
the time of a period of the oscillation, and the equilibrium,
or steady-state, of the closed-loop system. The conclusion is
that the energy-storage converter is the most versatile, most
efficient, and least complex of dc to dc power converters and is
best suited for use at frequencies near 1 MHz.

There are three basic types of dc to dc energy-storage
converters from which to choose. One is the voltage step-up
converter shown in Fig. 1(a); a second is the voltage step-down
converter shown in Fig. 1(b); and the third, often called an
isolated energy-storage converter, is shown in Fig. 12. There
are two basic disadvantages to the first two circuits. One is
that they can perform only a singular function which is either
voltage step-up or voltage step-down. Another is that they do
not provide electrical isolation between the source and the
load. The third circuit uses a mutual inductor which provides
isolation between the source and the load and, in addition,
provides the capability of operating as a voltage step-up or
step-down converter. The isolated energy-storage converter is
chosen because it can perform all of these functions.
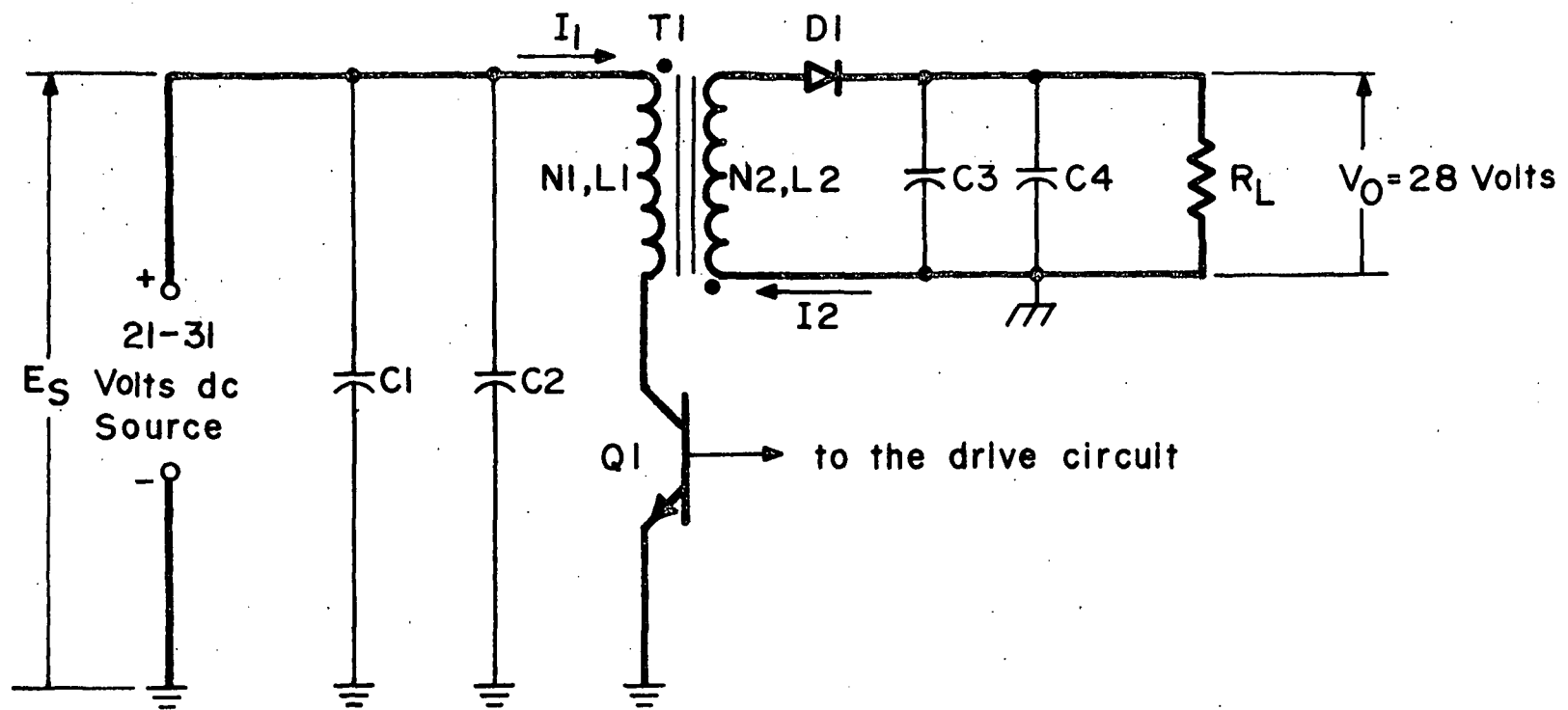
Fig. 12.   Schematic diagram of the power circuit and output filter.

Design considerations. The source voltage E_S variation of 21 to 31 volts commonly occurs in orbiting satellites whose batteries are charged from solar cell panels. The load voltage V_O on the load R_L was chosen to be 28 volts because this is a typical source voltage for aerospace electrical equipment.

Capacitors Cl and C2 are high-Q high-frequency capacitors which have several uses. The low impedance of these high-frequency capacitors shunts any spurious high-frequency signal from the source and also provides a path for current spikes generated during the switching of Ql so that they do not return through the source. Since Cl and C2 are mounted inside the converter on the converter end of the line from the source, they enable the collector current of Ql to rise faster when turn-on occurs by shunting the inductance of the source line during the switching time.

The actual isolated energy-storage converter consists of transistor Ql, mutual inductor Rl, and diode Dl and is shown in Fig. 12 as the main part of the power circuit. It should be noted that there are different grounds for the source side and the output side of Tl to achieve isolation. Because the isolated energy-storage converter has been described previously in the open literature, the operation and design of the circuit is only summarized in this text. The design procedures given use relations which were derived previously [22].

Circuit functioning. The discussion of the sequence of circuit operation begins by assuming that the circuit has reached a steady-state condition and that Q1 has just reached saturation. While Q1 is on, the source voltage E_S is applied to winding N1 of mutual inductor T1. The total series resistance around the path through E_S, N1, and Q1 is negligible. Therefore, if E_S is constant during the time Q1 is on, the flux rate of change $d\phi/dt$ is constant; and the current in N1 increases linearly. During this time, diode D1 is reverse-biased by the voltage on N2; and the current supplying the load comes from energy stored in capacitors C3 and C4. When Q1 turns off, the voltage polarities of N1 and N2 reverse; and the energy stored in T1 during the on-time is discharged through D1 into C3, C4, and R_L. C3 and C4 are chosen so that V_O does not vary more than the desired ripple voltage amplitude. They then provide an effective filter for the current pulses passing through D1 to yield a constant dc voltage V_O on the load resistance R_L.

Circuit design. In order to choose components for Q1 and D1 and design T1, the operating currents and voltages for these elements must be known. To compute these, it is necessary to start with the desired output voltage V_O, output power P_O, source voltage E_S, and the efficiency η. The largest currents exist when the circuit is delivering the maximum output power $P_{O(max)}$ of 20 watts and the source voltage E_S is a minimum of 21 volts. If η is assumed to be 80 percent, then the maximum input power $P_{in(max)}$ can be computed as

$$P_{in(max)} = 100 \, P_{O(max)} / \eta = 100 \times 20/80 = 25 \text{ watts} . \quad (32)$$

Maximum average primary current $\overline{I}_{1(max)}$ occurs when P_{in} is a maximum and E_S is a minimum; therefore

$$\overline{I}_{1(max)} = P_{in(max)} / E_{S(min)} = 25/21 = 1.19 \text{ amperes} . \quad (33)$$

$\overline{I}_{1(max)}$ is the source current averaged over the entire period in which time $i_1(t)$ is zero during the off-time t_{off} and finite during the on-time t_{on} as is shown in Fig. 13(a). The current $i_2(t)$ in winding N2 is zero during t_{on} and finite during t_{off} as shown in Fig. 13(b). Since V_O is regulated and constant, $d\phi/dt$ is constant during t_{off}; and since the energy stored in T1 is being discharged, $d\phi/dt$ is negative. It follows that $di_2(t)/dt$ is constant and negative.

Since the physical parameters of T1 are constant, the current waveforms for $i_1(t)$ and $i_2(t)$ are linearly related to the field intensity H. Also it is known that under steady-state conditions the increment $\Delta\phi$ in flux ϕ during t_{on} must equal the decrement in flux during t_{off}. These ideas are represented in Fig. 13(c) which shows the idealized linear B-H characteristic of the core used in T1. The subscripts ℓ, a, and h in Fig. 13 correspond to the lowest, average, and highest flux levels respectively in the core. The saturation flux level and field intensity are ϕ_S and H_S, respectively. Therefore, during t_{on}. the flux level goes from ϕ_ℓ to ϕ_h; and during t_{off}, the flux level goes from ϕ_h to ϕ_ℓ.
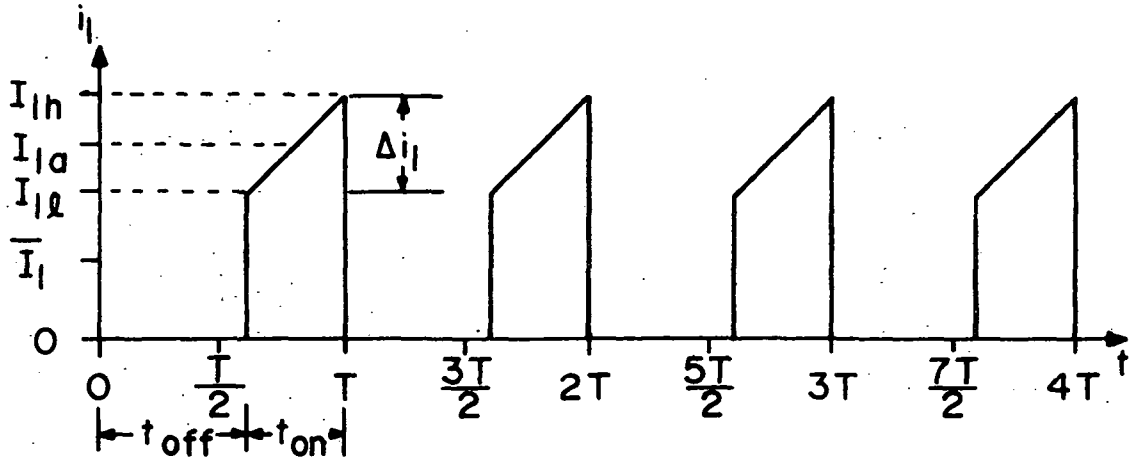
(a)
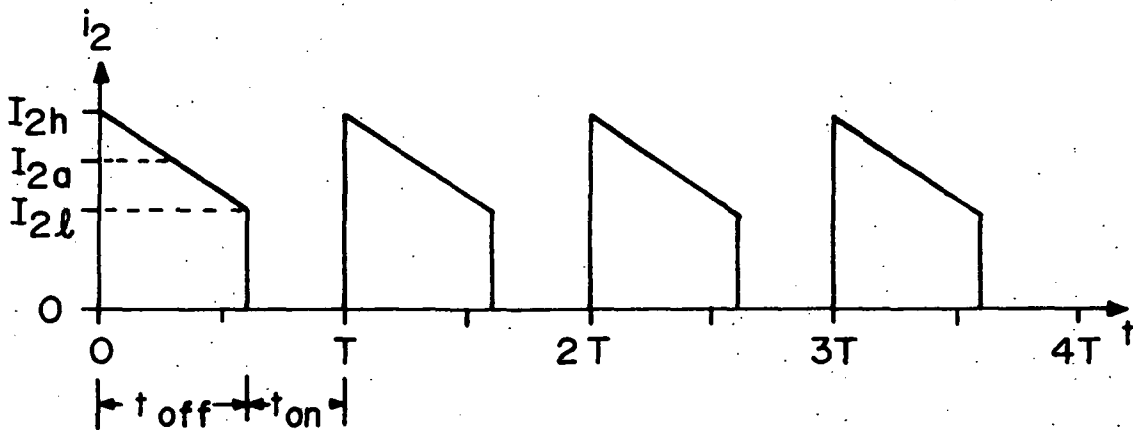
(b)
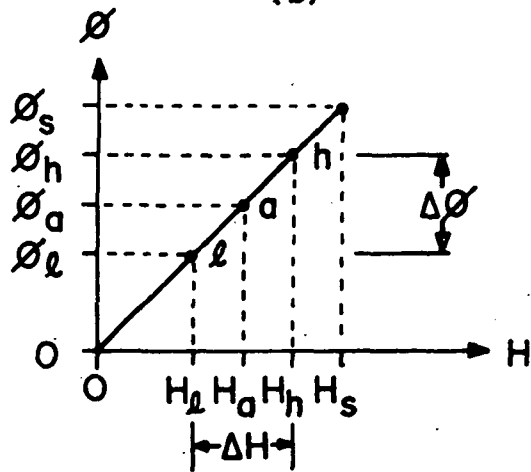
(c)

Fig. 13. Current waveforms and B-H characteristic for T1.

Design of mutual inductor Tl. The first step in the de-
sign of Tl is to determine the turns ratio N1/N2. The limiting
factor on the turns ratio is the breakdown voltage BV_{CEO} of Q1
during t_{off} when E_S is maximum. BV_{CEO} is expressed as

$$BV_{CEO} > V_O \times N_1/N_2 + E_{S(max)} \qquad . \qquad (34)$$

From (34) the maximum turns ratio is

$$N_1/N_2 < \left[BV_{CEO} - E_{S(max)}\right]/V_O = \frac{(50-31)}{28} = 0.68 \qquad (35)$$

where $BV_{CEO} = 50$ volts for Solitron transistor SDT6115 which is
chosen for Q1. A turns ratio of 0.5 is used in order to allow
for a margin of safety.

Before the core for Tl can be selected, point a or the
bias point in Fig. 13(c) must be determined. First the expres-
sion for maximum t_{on}/t_{off} which is derived in Reference 23 is
given as

$$\frac{t_{on}}{t_{off}} = \frac{V_O}{E_{S(min)}} \times \frac{N_1}{N_2} = \frac{28}{21} \times \frac{1}{2} = \frac{2}{3} = 0.67 \qquad . \qquad (36)$$

From this expression, the maximum duty cycle D.C. can be found
as

$$D.C. = \frac{t_{on}}{t_{on} + t_{off}} = \frac{t_{on}/t_{off}}{\left[t_{on}/t_{off}\right] + 1} = \frac{2/3}{(2/3) + 1} = \frac{2}{5} = 0.40 \qquad .$$
$$(37)$$

Using this duty cycle and $\overline{I}_{1(max)}$ from (33), maximum I_{1a} which is
the maximum average current in N1 during t_{on} can be obtained as

$$I_{1a} \approx \frac{\overline{I}_1 (max)}{D.C.} = \frac{1.19}{0.40} = 2.98 \text{ amperes} \quad . \tag{38}$$

Since di_1/dt is constant during t_{on} and t_{off}, the approximate formula for Δi_1 during t_{on} as shown in Fig. 13(a) can be obtained from Lenz's Law as

$$E_S = L_1 \frac{di_1}{dt} = L_1 \frac{\Delta i_1}{\Delta t} \quad . \tag{39}$$

Which when rearranged yields Δi_1 as

$$\Delta i_1 = E_{S(min)} t_{on}/L_1 \quad . \tag{40}$$

From Ampere's Law, where N is the number of turns, I is the current, and ℓ is the mean-free-path length

$$H = 0.4\pi NI/\ell \quad . \tag{41}$$

ΔH shown in Fig. 13(c) can be expressed as a function of Δi_1 as

$$\Delta H = 0.4\pi N_1 \Delta i_1/\ell \tag{42}$$

also

$$H_a = 0.4\pi N_1 I_{1a}/\ell \quad . \tag{43}$$

In Fig. 13(c), it is easy to determine that

$$H_h = H_a + \frac{1}{2} \Delta H \tag{44}$$

which after substituting (42) for ΔH and (43) for H_a becomes

$$H_h = 0.4\pi N_1 \left(I_{1a} + \frac{1}{2} \Delta i_1 \right)/\ell \quad . \tag{45}$$

Substituting (40) into (45) yields

$$H_h = 0.4\pi N_1 \left(I_{1a} + \frac{E_{S(min)} t_{on}}{2L_1} \right) / \ell \qquad . \qquad (46)$$

The inductance factor A_L for a given linear core is usually given as mH for 1000 turns which yields

$$L_1 = \frac{N_1^2}{(1000)^2} \times A_L \times 10^{-3} = N_1^2 \times A_L \times 10^{-9} \text{ henries} \qquad (47)$$

and substituting (47) into (46) yields

$$H_h = \frac{0.4\pi}{\ell} \left(I_{1a} N_1 + \frac{E_{S(min)} t_{on}}{2N_1 A_L \times 10^{-9}} \right) \qquad . \qquad (48)$$

The first criterion which must be met when designing T1 is that H_h does not reach saturation magnetic intensity H_S or

$$H_h < H_S \qquad . \qquad (49)$$

Before H_h in (48) can be used in (49), the on-time t_{on} must be computed using D.C. = 0.40 from (37) and f = 1 MHz as

$$t_{on} = D.C. \times T = D.C./f = 0.40 \times 10^{-6} \text{ seconds} \qquad . \qquad (50)$$

Substituting I_{1a} from (38), t_{on} from (50), and $E_{S(min)}$ = 21 volts into (48) yields

$$H_h = \frac{0.4\pi}{\ell} \left(2.98 N_1 + \frac{4.2 \times 10^3}{N_1 A_L} \right) \qquad . \qquad (51)$$

Equations (49) and (51) are used in a trial and error procedure to determine the core and the number of turns for N1. This is done by choosing a core, substituting for ℓ and A_L in (51), and solving (51) for N1. Then N2 must be calculated

knowing N1/N2 = 0.5, the wire size for N1 and N2 must be chosen, and N1 and N2 must be checked for fit in the window area of the core. This procedure follows.

It has already been determined that for purposes of reducing leakage flux and consequently leakage inductance an ungapped pot core should be chosen. One such core is pot core #2616P-3D3 UG manufactured by Ferroxcube Corp. which has A_L = 2340 mH/1000 turns, ℓ = 3.73 cm, and H_S = 5 oersteds. Substituting $H_h = H_S$, ℓ, and A_L into (51) yields

$$N_1^2 - 3.31N_1 + 0.407 = 0 \quad . \tag{52}$$

The roots of (52) are N1 = 0.125 or 3.13 turns. The maximum turns for N1 is then 3 turns and for N2 is 6 turns using N1/N2 = 0.5 chosen from (35). If N1 = 3 turns, ℓ = 3.73 cm, and A_L = 2340 mH/1000 turns is substituted into (51), H_h is found to be 3.24 oersteds which is less than H_S = 5 oersteds.

From (33), the full-cycle average current in N1 is 1.19 amperes which requires #19 AWG wire based on 1000 circular mils per ampere. The maximum average current in N2 is simply $P_{O(max)}/V_O$ = 20/28 = 0.714 amperes which requires #21 AWG wire based on 1000 circular mils per ampere. Now it is necessary to check N1 and N2 for fit in the cross sectional area A_{CB} of the core through which the windings must pass. This area for core 2616P-3D3-UG is 0.406 in^2. In order to allow for the space and insulation between conductors, the total cross-sectional area

A_{cu} of the turns should not exceed 40 percent of A_{CB} which is 0.163 in². AWG #19 wire has a cross-sectional area A_{N_1} of 0.00101 in² and AWG #21 wire has a cross-sectional area A_{N_2} of 0.000638 in². A_{cu} can now be calculated as

$$A_{cu} = 3A_{N_1} + 6A_{N_2} = 3(0.00101) + 6(0.000638) = 0.006912 \text{ in}^2 \quad .$$

(53)

Since $A_{cu} = 0.006912$ in² is less than $0.4A_{CB} = 0.163$ in², N1 = 3 turns AWG #19 and N2 = 6 turns AWG #21 can be wound; and the mutual inductor is designed. The 3 turns of N1 are bifilar wound with the first 3 turns of N2. The remaining 3 turns of N2 are wound normally.

Before the design is complete maximum instantaneous current I_{1h} must be compared with the maximum ratings for Q1. Since field intensity H is linearly related to I_{1h}

$$I_{1h} = I_{1a} + \frac{1}{2} \Delta i_1 \quad .$$

(54)

The inductance L_1 is calculated from (47) as

$$L_1 = N_1^2 A_L \times 10^{-9} = 3^2 \times 2340 \times 10^{-9} = 21.06 \ \mu H \quad .$$

(55)

Substituting $E_{S(min)} = 21$ volts from Fig. 12, $t_{on} = 0.40 \times 10^{-6}$ seconds from (50), and $L_1 = 21.06 \ \mu H$ from (55) into (40) yields

$$\Delta i_1 = E_{S(min)} t_{on}/L_1 = 21 \times 0.40 \times 10^{-6}/(21.06 \times 10^{-6}) = 0.40 \text{ amperes} \quad .$$

(56)

Substituting $\Delta i_1 = 0.40$ amperes from (56) and $I_{1a} = 2.98$ amperes from (38) yields

$$I_{1h} = 2.98 + \frac{0.40}{2} = 3.18 \text{ amperes} \quad . \tag{57}$$

Since I_{1h} is less than the rated 10 amperes maximum collector current for Q1, the design is complete.

The output filter capacitors C3 and C4 are chosen experimentally from non-electrolytic high-frequency capacitors. This capacitance is increased until the load ripple voltage amplitude is within acceptable limits resulting in values of 4.7 μF each for C3 and C4.

The Control Circuits

The control circuits consist of the differential voltage comparator and the triangular waveform generator as shown in Fig. 10. The purpose of the control circuits is to sense the output voltage and provide a duty-cycle signal which when used to control Q1 results in a regulated output voltage V_O. Integrated circuits are used where possible in the design of the control circuits because they are small, efficient, and switch very fast. The control circuits can be built with discrete components; however, shielding, grounding, pickup, and delay time at this high frequency become greater problems than with integrated circuits. One disadvantage of using integrated circuits is the need for multiple low-voltage power supplies. These supplies should be readily available in most applications; but if they are not, a system of Zener diodes or small high-frequency

switching regulators would provide the necessary voltages.

The schematic diagram of the control circuits is shown in Fig. 14. They consist of a threshold circuit, which is built around the integrated circuit I1 and is commonly called a differential voltage comparator circuit, and a triangular waveform generator which is built around integrated circuit I2. A brief description of the means by which these circuits generate a duty cycle is given first, then the design of each circuit is discussed.

Functioning of the control circuits. The voltage on DZ2 in Fig. 14 acts as the reference voltage V_R for the voltage comparator I1 and is applied to the positive input at pin 2 of I1 through R6. The direct output voltage V_O is applied to the negative input at pin 3 of I1 by means of a voltage divider made up of R7 and R8. In addition, a 1 MHz triangular waveform v_t is obtained by integrating the output of I2 which is utilized as a 1 MHz square wave oscillator. Integration is accomplished through the RC combination of the output resistance of I2, R7, R8, and C10. C9 has negligible effect because the time constant resulting from the product of the parallel combination of R7 and R8 and C9 is approximately three orders of magnitude longer than the period of 1 MHz. The resulting v_t on C10 is coupled through capacitor C9 and is added to the fraction of V_O on pin 3 of I1 resulting in a voltage v_A at pin 3 of I1 given by
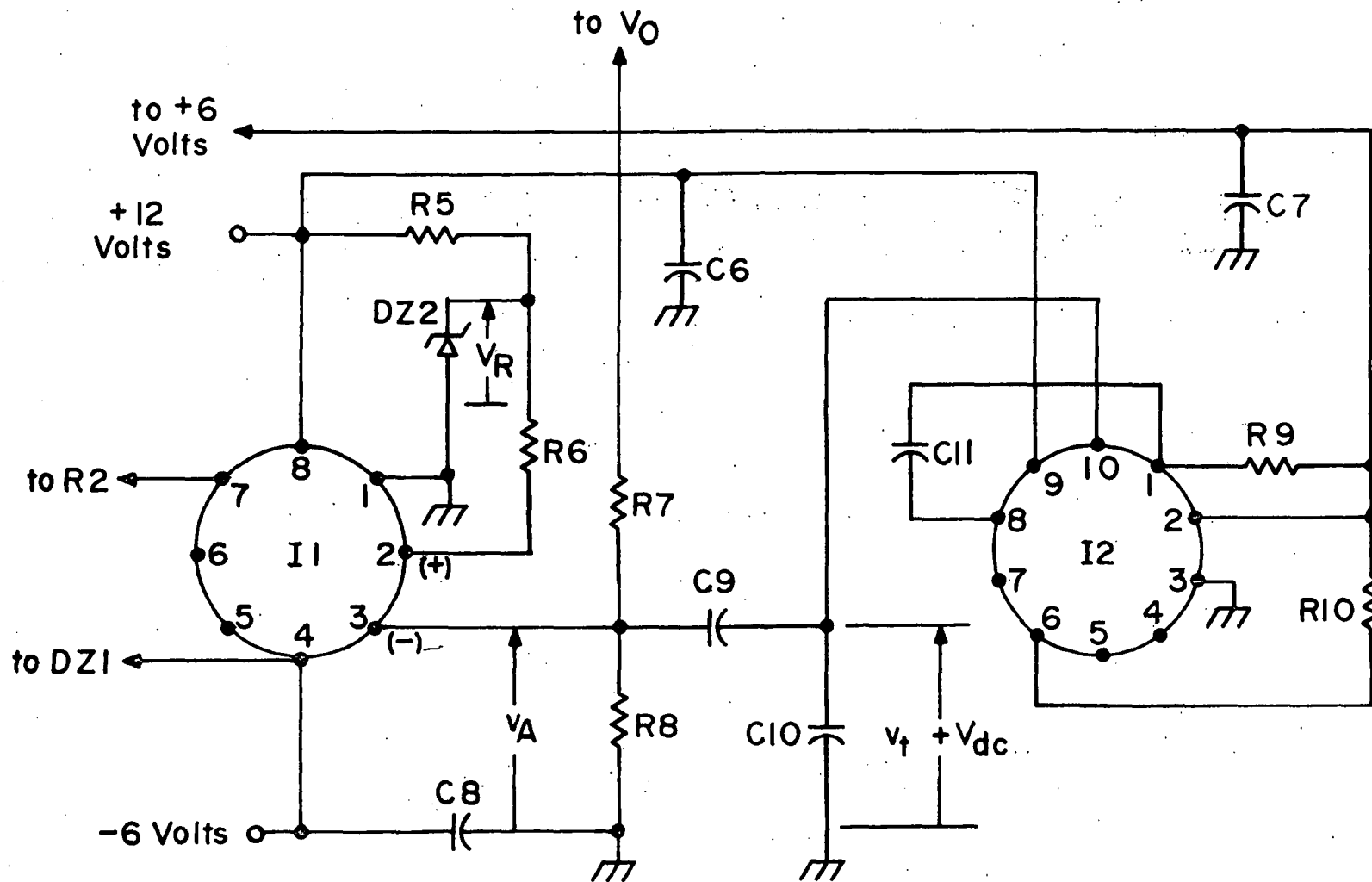
Fig. 14. Schematic diagram of the differential voltage comparator and the tri-
angular waveform generator.

$$v_A = \frac{R_8}{R_7 + R_8} \, V_O + v_t \quad . \tag{58}$$

The differential input to voltage comparator I1 is $V_R - v_A$; therefore whenever v_A is less than V_R the differential input is positive so there is a positive output signal at the comparator output terminal, pin 7 and vice versa. An examination of Fig. 11 reveals that Q1 is turned on when Q2 is turned on, and Q2 is turned on when the voltage at pin 7 is positive. This means that Q1 turns on whenever v_A is less than V_R. For purposes of simplifying this explanation, it is assumed that the voltage comparator has no hysteresis. It is also assumed that the ac ripple voltage component of V_O is negligible compared to v_t; and the frequency f is constant at 1 MHz so the period $T = t_{on} + t_{off}$ is constant.

Keeping these factors in mind, the manner in which a duty cycle capable of maintaining a regulated output voltage is obtained can be explained. Fig. 15 shows three examples of v_A each at different direct voltage levels. It has already been established that when $v_A < V_R$ the power transistor Q1 is on; and when $v_A > V_R$, Q1 is off. So in Fig. 15, the times during which v_A is above the dashed line at $v = V_R$ correspond to t_{off} and the times v_A is below this line correspond to t_{on} as it is so labelled. In Fig. 15, the voltage v_A at pin 3 of I1 is assumed to consist of two components, the direct voltage $V_A = V_O R_8 / \left(R_7 + R_8 \right)$ and the alternating triangular voltage v_t.

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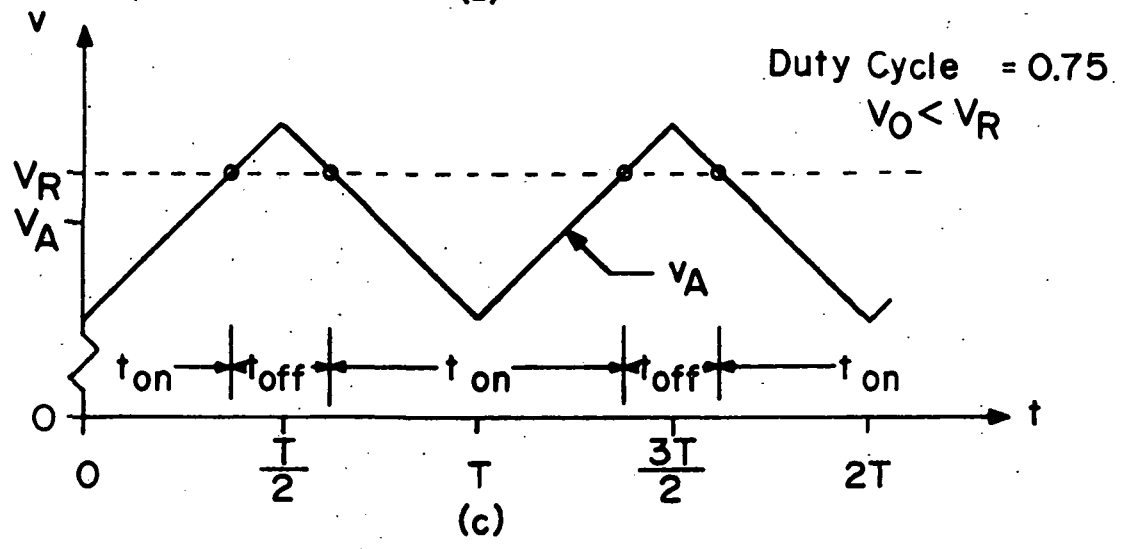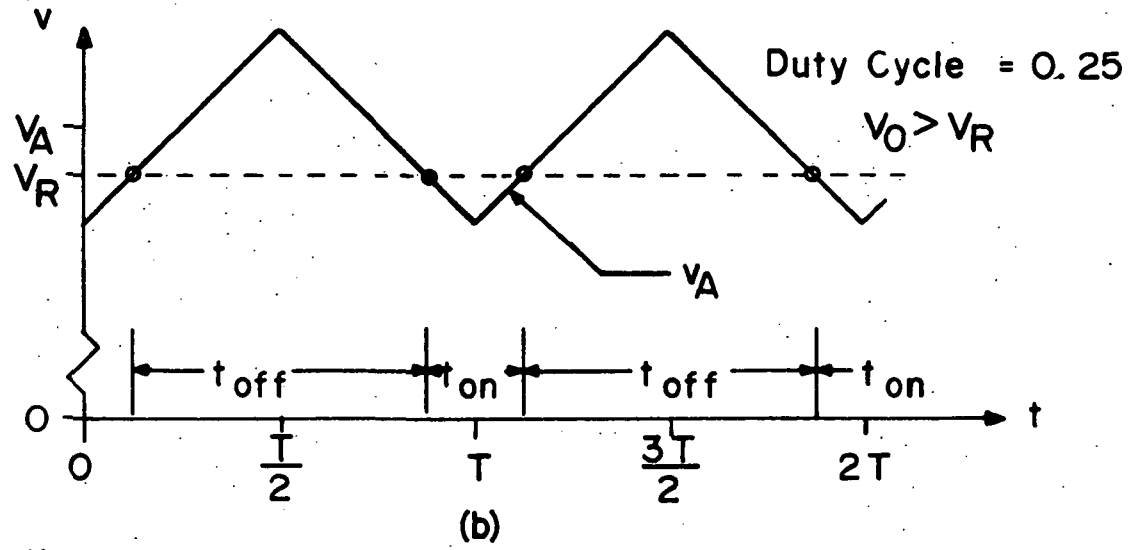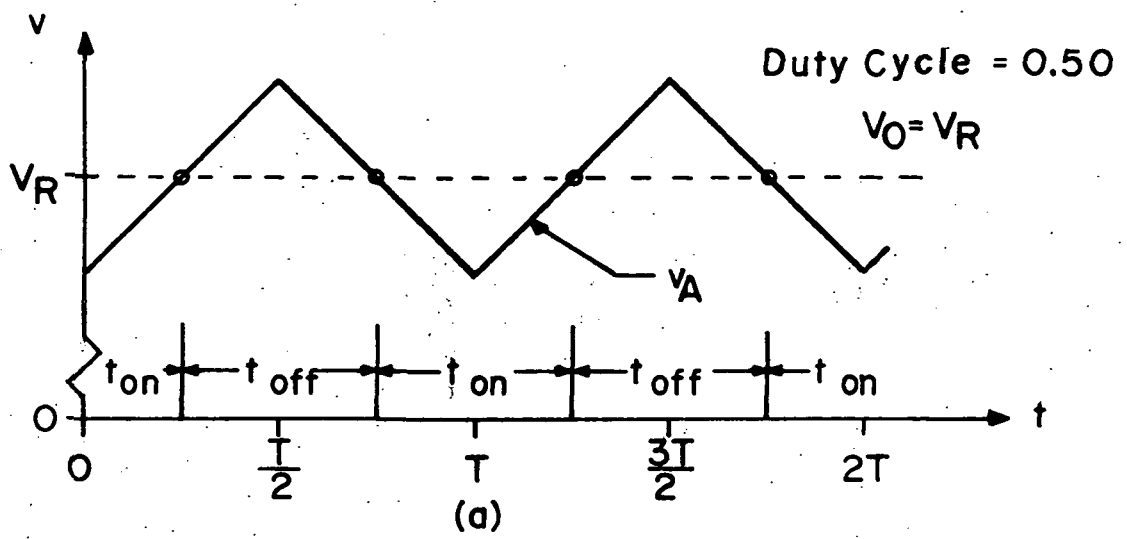
Fig. 15. Voltage waveforms of v_A at different duty cycles.

In Fig. 15(a), V_A equals the direct reference voltage V_R, $t_{on} = t_{off}$, and the duty cycle D.C. = 0.50. If the load is de-creased or E_S is increased, V_A tends to increase to a condition shown in Fig. 15(b) in which t_{on} is shortened lowering the duty cycle and tending to decrease V_A to its original value. If the load is increased or E_S is decreased, V_A tends to decrease cre-ating the condition shown in Fig. 15(c) in which t_{on} is length-ened increasing the duty cycle and tending to increase V_A to its original value. This system operating in a closed-loop condi-tion tends to maintain a regulated output voltage. A much more detailed non-linear analysis of this type of regulating mechan-ism is given later in Chapter IV which includes the effects of hysteresis and the ripple voltage component of V_O. Now that a brief explanation has been given on the operation of the control circuits the design procedures are discussed.

Design of the comparator. The integrated circuit chosen for I1 in Fig. 14 is the 710 series of differential voltage com-parators. This device is chosen because it dissipates typically only 110 mw internally while supplying a +3.2 volt and 10 ma positive output that switches on or off in 40 nsec. I1 requires two power supplies of +12 volts and -6 volts. Capacitors C6, C7, and C8 are placed between the power sources and ground in order to bypass any noise or voltage spikes that may adversely affect the operation of the comparator and to provide a low im-pedance source during the transient time when the comparator switches. These capacitors are chosen experimentally to provide

optimum comparator performance. In this example, C6, C7, and C8 are 0.1 µF as given in Table III. Resistor R5 is used to bias Zener diode DZ2, and DZ2 provides the reference voltage for voltage comparator I1. The value of R5 is determined by finding a bias point with good regulation on the characteristic of DZ2. It is desirable that this bias point have a minimum current level in order to minimize power dissipation; and it must have a voltage value of less than 5 volts which is the maximum input voltage for I1. From these requirements, Zener diode 1N751 is chosen for DZ2. From an examination of the characteristic of DZ2 on a transistor curve tracer, a bias point at 4.5 volts and approximately 2.8 ma. is chosen. The current through R6 is negligible since the input impedance to the comparator is high; therefore R5 is computed as

$$R_5 = \left(12 - V_{DZ2}\right)/I_{DZ2} = (12 - 4.5)/(2.8 \times 10^{-3}) = 2.7 \text{ k}\Omega \quad (59)$$

as is given in Table III. R7 and R8 are determined by assuming that the comparator is regulating and in a balanced state. Under these conditions, V_R equals the dc component V_A of v_A given as

$$V_A = V_O R_8/\left(R_7 + R_8\right) = V_R \quad . \quad (60)$$

Substituting V_R = 4.5 volts and V_O = 28 volts yields

$$R_7 = \frac{23.5}{4.5} R_8 \quad . \quad (61)$$

Since the input to I1 at pin 3 has a very high impedance and draws negligible current, the current through R7 and R8 may be

very small. It is still desirable to minimize power dissipation so an arbitrary negligible power dissipation P_d of 10 mw is chosen. This yields a total resistance of

$$R_7 + R_8 = \frac{V_O^2}{P_d} = \frac{28^2}{10^{-2}} = 78.4 \text{ k}\Omega \quad . \tag{62}$$

Substituting R7 from (61) into (62) yields R_8 = 12.6 kΩ and substituting R8 into (62) yields R_7 = 65.8 kΩ. These resistors should be temperature compensated to keep V_O from drifting with changes in temperature. Values as close as possible to those calculated were chosen from stock and adjusted experimentally to obtain an output voltage V_O of 28 volts. The resulting final values were R_7 = 69.8 kΩ and R_8 = 14.3 kΩ as given in Table III. In order to obtain the best possible regulation, the accuracy of the comparator must be maximized. This is done by making the source resistance of the reference voltage V_R equal to the dc source resistance of the signal v_A. With equal source resistances, the bias currents at the inputs create nearly equal voltage drops minimizing the offset voltage. The dc source resistance for v_A is the parallel combination of R7 and R8 so

$$R_6 = \frac{R_7 R_8}{R_7 + R_8} = \frac{14.3 \times 69.8}{14.3 + 69.8} \times 10^3 = 11.9 \text{ k}\Omega \quad . \tag{63}$$

The nearest discrete resistor to this value in stock is 12.0 kΩ which is used for R6 as given in Table III. This completes the design of the differential voltage comparator.

Design of the triangular waveform generator. The triangu-
lar waveform generator is built around the dual operational am-
plifier I2 shown in Figs. 11 and 14. I2 is a type CA3000 IC
differential amplifier by RCA. This amplifier has a typical in-
ternal power dissipation of 30 mw which is desirable from the
viewpoint of maximizing efficiency. Also it is capable of oper-
ating at frequencies to 30 MHz which is well beyond the switch-
ing frequency of the converter. I2 requires power supplies of
+6 volts at pin 9 and -6 volts at pin 3 with respect to pin 2.
These supplies are obtained in Fig. 14 by using the existing
+12-volt supply on pin 9, grounding pin 3, and providing an addi-
tional +6 volt supply so that pin 9 is +6 volts and pin 3 is -6
volts with respect to the +6 volt supply at pin 2.

A square wave oscillator circuit is formed with I2 using
R9, R10, and C11 as given in the manufacturer's application man-
ual. This oscillator produces a square wave at the output at
pin 10. The frequency of oscillation is adjusted to 1 MHz by
experimentally varying C11 until it is 33 pF. R9 and R10 are
chosen to be 1 kΩ because these are typical values used by the
manufacturer [24].

The open-circuit output v_{10} at pin 10 switches from
$V_{10}' = 11.2$ volts to $V_{10}'' = 5.0$ volts and vice versa. When pin
10 is connected to C10, this voltage produces a dc voltage
$V_{dc} = 8.1$ volts on C10. Since V_{dc} does not normally equal the
dc component of v_A, coupling capacitor C9 is required to keep

V_{dc} from upsetting the balance of I1. In order that v_t is coupled to R8 without any significant distortion, C9 must be chosen so that

$$\frac{1}{2\pi f\, C_9} << \frac{R_7 R_8}{R_7 + R_8} \quad . \tag{64}$$

This relation is satisfied at $f = 1$ MHz when $C9 = 0.1\ \mu F$. The triangular waveform v_t is generated by the charging and discharging of C10 during alternate half cycles of the square-wave output on pin 10 of I2. The time constant of this circuit is found by assuming that V_O and C9 are shorted, that pin 10 returns to the neutral through an internal resistance r_O, and that the input impedance at pin 3 of I1 is large enough to be assumed an open circuit. These assumptions mean that R7, R8, r_O, and C10 are effectively in parallel which yields a time constant τ of

$$\tau = \frac{R_7 R_8 r_O}{R_7 R_8 + r_O R_7 + r_O R_8} C_{10} = RC_{10} \tag{65}$$

where $R = R_7 R_8 r_O / \left(R_7 R_8 + r_O R_7 + r_O R_8 \right)$ is the parallel combination of R7, R8, and r_O.

With these assumptions, the load on pin 10 of I2 can be thought of as the parallel combination of R and C10. Across C10 there is an average dc bias of V_{dc}. If it is assumed that the open circuit voltage v_{10} on pin 10 of I2 switches to $V'_{10} = 11.2$ volts at $t = 0$, the equation for $v_t(t)$ during the half cycle, $t = 0$ to $t = 1/2f$, when C10 is charging is

$$v_t(t) = \left[V'_{10} - V_{dc} + V_{tm}\right]\left(1 - e^{-\frac{t}{\tau}}\right) + V_{dc} - V_{tm} \quad . \qquad (66)$$

Where at $t = 0$, (66) yields $v_t(0) = V_{dc} - V_{tm}$; and at $t = \infty$, (66) yields $v_t(\infty) = V'_{10}$. The peak value of $v_t(t)$ occurs at $t = 1/2f$ and is $V_{dc} + V_{tm} = v_t(1/2f)$. The peak value V_{tm} of $v_t(t)$ can be computed by substituting $t = 1/2f$ and $\tau = RC_{10}$ into (66) and evaluating

$$V_{tm} = \frac{1}{2}\left[v_t(1/2f) - v_t(0)\right] = \frac{1}{2}\left(V'_{10} - V_{dc} + V_{tm}\right)\left(1 - e^{-\frac{1}{2fRC_{10}}}\right) \quad .$$

$$(67)$$

Rearranging, taking the natural logarithm of both sides of (67), and solving for C_{10} yields

$$C_{10} = \frac{-1}{2fR \, \ell n\left(1 - \dfrac{2V_{tm}}{V'_{10} - V_{dc} + V_{tm}}\right)} \qquad (68)$$

which is the value of C10 which yields V_{tm}.

For I2, the typical value of r_o is 8 kΩ; and R7 and R8 have been determined as 69.8 kΩ and 14.3 kΩ respectively. Substituting into (65) yields

$$R = \frac{69.8 \times 14.3 \times 8.0 \times 10^9}{(69.8 \times 14.3 + 8.0 \times 69.8 + 8.0 \times 14.3)10^6} = 4.78 \text{ k}\Omega \quad .$$

$$(69)$$

Substituting $f = 10^6$ Hz, $R = 4.78$ kΩ, $V_{tm} = 0.1$ volts, $V_{10} = 11.2$ volts, and $V_{dc} = 8.1$ volts in (68) yields

$$C_{10} = \cfrac{-1}{2 \times 10^6 \times 4.28 \times 10^3 \times \ln\left(1 - \cfrac{0.2}{11.2 - 8.1 + 0.1}\right)} = 1620 \text{ pF .}$$

<div align="right">(70)</div>

A 1500 pF disc ceramic capacitor as given in Table III was chosen from stock for C10.

This concludes the design of the control circuits. The final section of the converter to be discussed next is the drive circuit.

The Drive Circuit

This part of the converter boosts the power available from the duty cycle output of differential comparator I1 to a power sufficient to control the power switching transistor Q1. The schematic diagram is shown in Fig. 16. The output from pin 7 of the differential comparator I1 is used to drive the base of Q2 through R2. Bias resistor R4 and Zener diode DZ1 supplied by the -6 volts on pin 4 of I1 provide a negative voltage at b which serves to reverse bias the emitter-base junction of Q2 through R3 during the off-time. When Q2 is on, the +6 volt supply is applied to the primary winding N5 so that the dotted ends of windings N5 and N4 are positive. The voltage coupled to the secondary winding N4 during the time Q2 is on is of such a polarity to drive Q1 through R1 so that when Q2 turns on, Q1 turns on. The time that Q1 is on is designated t_{on}, and the time that Q2 is on is designated t'_{on}.

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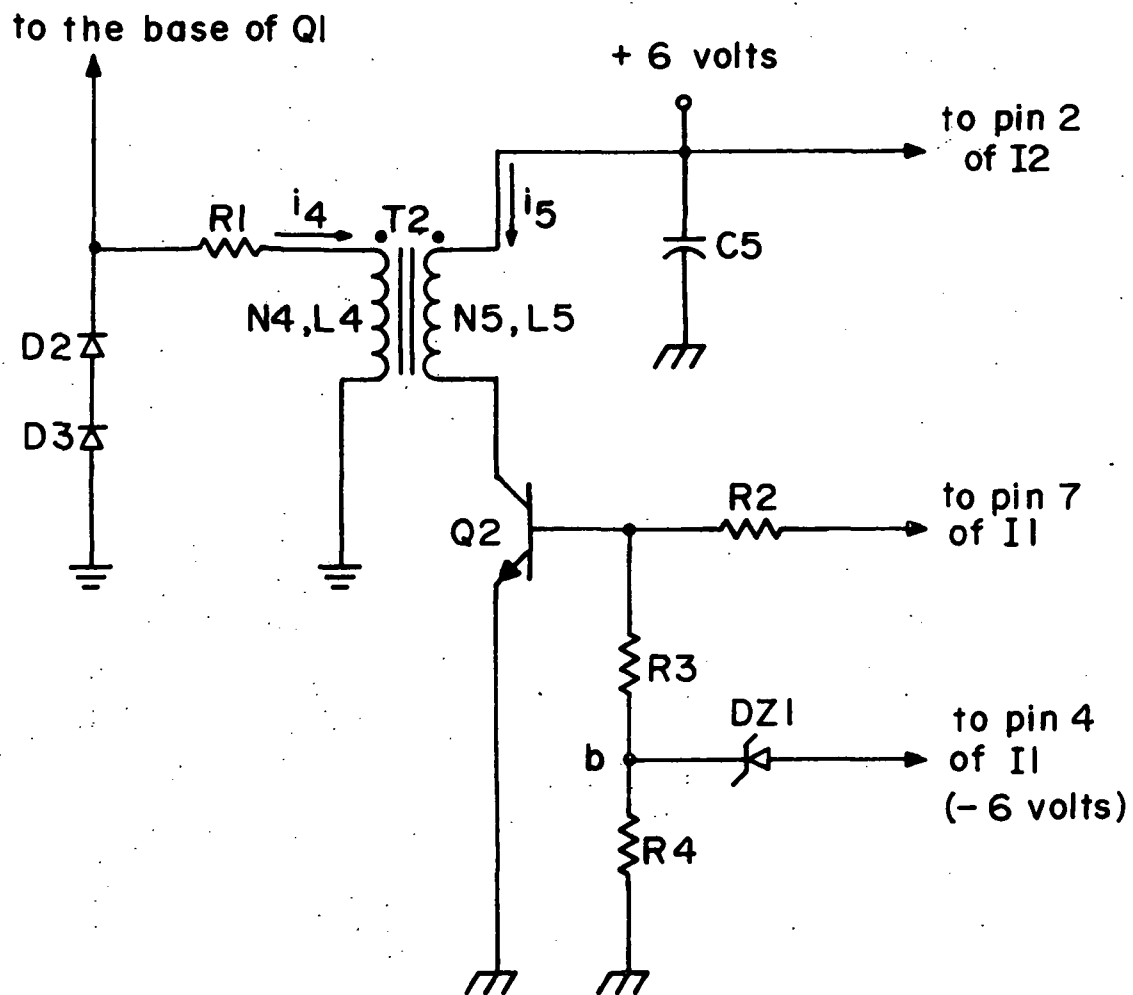
Fig. 16. Schematic diagram of the drive circuit.

The time t'_{on} may not be the same as t_{on} because the response times of Q2 and Q1 are normally different. The voltage applied to N5 during the on-time of Q2 causes energy to be stored in T2. When Q2 turns off, the energy stored during the on-time of Q2 is discharged through R1, D2, D3, and N4; and the voltage drop on D2 and D3 provides a reverse bias on the emitter-base junction of Q1 to reduce the storage and fall times of Q1. It should be noted that T2 serves three functions. One is to provide isolation between the source and the load. The second function is to provide base drive to Q1. The third function is to store energy during the on-time of Q2 which can be used to reverse-bias Q1 during the off-time of Q2 to speed turn-off of Q1.

Primary and secondary current relations for T2. The design of the drive circuit begins with an analysis of the current waveforms of mutual inductor T2. T2 is a mutual inductor wound on a toroidal ferrite core with a linear B-H characteristic. In the following analysis, it is assumed that Q1 and Q2 switch instantaneously with the exception of the storage time of Q1 and that the primary inductance L5 is large enough so that the variation of the primary current is linear. Fig. 17(a) shows the waveform for the primary current $i_5(t)$ and Fig. 17(b) shows the waveform for the secondary current $i_4(t)$. Since the resistance in the primary circuit is negligible, the voltages $v_5(t)$ on N5 and $v_4(t)$ on N4 are constant during t'_{on}; consequently, $i_4(t)$ is constant and equal to $-I_4$ given by
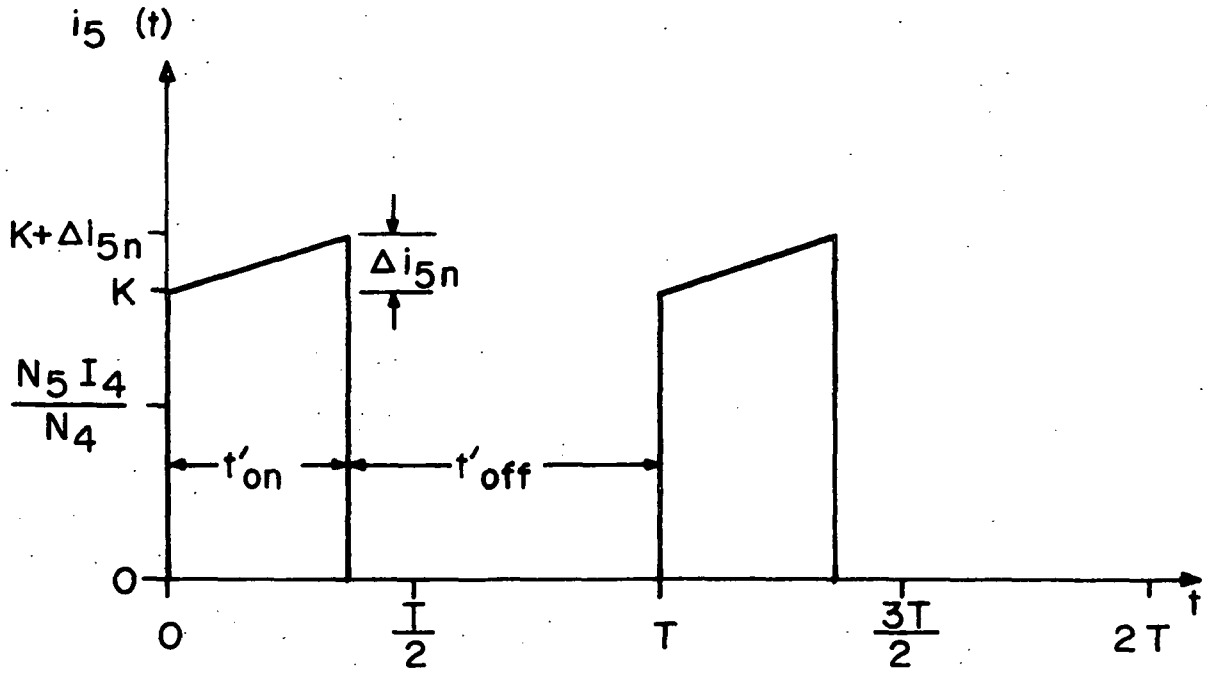
(a)
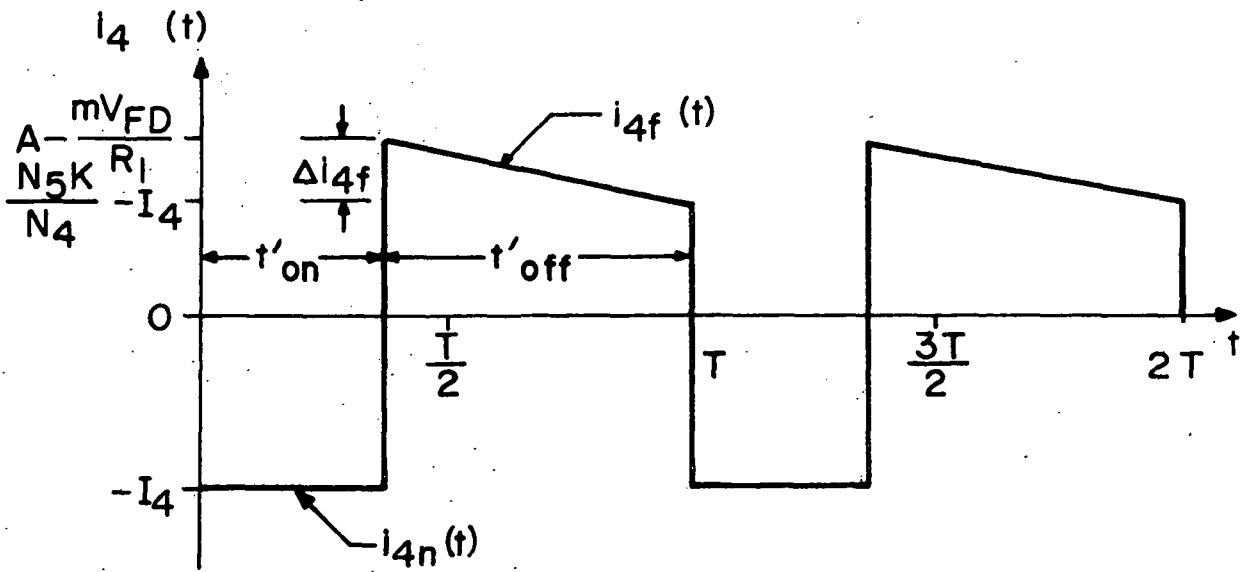
(b)

Fig. 17. Current waveforms for T2.

$$i_{4n}(t) = -I_4 = -\frac{\left[N_4\left(6-V_{CE2}\right)/N_5\right] - V_{BE1}}{R_1} \qquad 0 \le t \le t'_{on} \tag{71}$$

where the subscript n designates $i_4(t)$ during t'_{on}, V_{CE2} is the collector-emitter saturation voltage on Q2 during t'_{on}, and V_{BE1} is the base-emitter saturation voltage on Q1 during t'_{on}. Symbols such as V_{CE2} and V_{BE1} are used in lieu of $V_{CE(sat)2}$ and $V_{BE(sat)1}$ to represent the saturation voltages of transistors in order to eliminate lengthy and cumbersome subscripts on these variables. Also during t'_{on}, the primary current $i_{5n}(t)$ consists of a constant component $N_5 I_4/N_4$ which is I_4 reflected to the primary and a component which represents the energy stored in T2 and increases approximately linearly during t'_{on} by Δi_{5n} as shown in Fig. 17(a). Assuming that $i_{5n}(t)$ varies linearly during t'_{on}, the voltage of self induction is

$$V_{N5} = L_5 \, \Delta i_{5n}/t'_{on} \, . \tag{72}$$

Since V_N must equal $6-V_{CE2}$, the slope $di_{5n}/dt = \Delta i_5/t'_{on}$ of $i_{5n}(t)$ during t'_{on} must be $\left(6-V_{CE2}\right)/L_5$ which yields

$$i_{5n}(t) = \frac{6 - V_{CE2}}{L_5} \, t + K \qquad 0 \le t \le t'_{on} \tag{73}$$

where K is the value of $i_{5n}(t)$ at t = 0 as shown in Fig. 17(a). The subscript f designates variables during the time period t'_{off}. During t'_{off}, $i_{5f}(t) = 0$; but $i_{4f}(t)$ is nonzero flowing into the dotted end of N4 and passing through D2, D3, and R1. The differential equation for $i_{4f}(t)$ around this loop is

$$\frac{di_{4f}(t)}{dt} + \frac{R_1}{L_4} i_{4f}(t) - \frac{mV_{FD}}{L_4} = 0 \qquad t'_{on} \le t \le T \qquad (74)$$

where V_{FD} is the forward voltage on diode D2 or D3 and the number of diodes m is as yet undetermined. Solving (74) for $i_{4f}(t)$ yields

$$i_{4f}(t) = A e^{-\frac{R_1}{L_4}\left(t - t'_{on}\right)} - \frac{mV_{FD}}{R_1} \qquad t'_{on} \le t \le T \quad . \qquad (75)$$

Expressions for the primary and secondary currents during both t'_{on} and t'_{off} have been derived. During t'_{on}, $i_{4n}(t)$ is given by (71) and $i_{sn}(t)$ by (73). During t'_{off}, $i_{sf}(t) = 0$ and $i_{4f}(t)$ is given by (75).

There are two unknown constants, K in (73) and A in (75). Their values are related to the steady-state energy levels in mutual inductor T2. One set of conditions is found by equating the total ampere turns just prior to turn-on to the total ampere turns just after turn-on to obtain

$$\frac{N_5 i_{sn}(0)}{N_4} + i_{4n}(0) = i_{4f}(t) \quad . \qquad (76)$$

Another set of conditions is obtained by equating the ampere turns just prior to turn-off to the ampere turns just after turn-off to obtain

$$\frac{N_5 i_{sn}\left(t'_{on}\right)}{N_4} + i_{4n}\left(t'_{on}\right) = i_{4f}\left(t'_{on}\right) \quad . \qquad (77)$$

Substituting (71), (73), and (75) into (76) yields

$$\frac{N_5 K}{N_4} - I_4 = A e^{-\frac{R_1}{L_4} t'_{off}} - \frac{mV_{FD}}{R_1} \quad . \tag{78}$$

Substituting (71), (73), and (75) into (77) yields

$$\frac{N_5}{N_4}\left[\frac{6 - V_{CE2}}{L_5} t'_{on} + K\right] - I_4 = A - \frac{mV_{FD}}{R_1} \quad . \tag{79}$$

Solving (78) for K and substituting into (79) yields

$$A = \frac{\frac{N_5}{N_4}\left(\frac{6 - V_{CE2}}{L_5} t'_{on}\right)}{1 - e^{-\frac{R_1}{L_4} t'_{off}}} \quad . \tag{80}$$

Substituting (80) into (78) and solving for K yields

$$K = \frac{\frac{6 - V_{CE2}}{L_5} t'_{on}}{e^{\frac{R_1}{L_4} t'_{off}} - 1} - \frac{N_4}{N_5}\left(\frac{mV_{FD}}{R_1} - I_4\right) \quad . \tag{81}$$

The constant K given in (81) can be substituted into (73) to find $i_{5n}(t)$ during t'_{on}. During t'_{off} $i_{5f}(t) = 0.0$. The base drive $i_4(t)$ for Q1 during t'_{on} is given by (71), and the constant A in (80) can be substituted into (75) to find $i_{4f}(t)$ during t'_{off}. Now that relations for the currents in T2 have been determined, the design of the drive circuit can continue.

Base drive for Q1. The next step in the design is to determine the magnitude of the base current required by Q1 as

$$i_{1b(max)} = i_{1C(max)}/h_{1fe} \tag{82}$$

where $i_{1b(max)}$ is the maximum instantaneous base current corresponding to the maximum instantaneous collector current $i_{1C(max)}$ in Q1. A current gain h_{1fe} of 10 is assumed, as used in the manufacturer's specification sheet for switching five amperes, to insure that Q1 is driven into saturation. The maximum instantaneous collector current occurs when the output power P_O is a maximum at 20 watts, the source voltage E_S is a minimum at 21 volts, and $t = t'_{on}$. It has been calculated in (57) as 3.18 amperes. Using (82), the maximum base current $i_{1b(max)}$ for Q1 is

$$i_{1b(max)} = \frac{3.18}{10} = 0.318 \text{ amperes} \quad . \tag{83}$$

The drive current I_4 given in (71) must have a magnitude at least as large as $i_{1b(max)}$ in (83) so that

$$I_4 = \frac{N_4 \left(6 - V_{CE2}\right)/N_5 - V_{BE1}}{R_1} \geq 0.318 \text{ amperes} \quad . \tag{84}$$

From the specification sheets for Q1 and Q2, $V_{CE2} = 0.8$ volts and $V_{BE1} = 1.7$ volts.

At this time, it is necessary to determine the turns ratio for T2. It is desired that R1 be as small as possible to minimize power dissipation; consequently, the voltage on N4 during t'_{on} should be small. Also, the same principles of design are

applied to T2 as were applied to T1. Because the source imped-
ances of T2 are small, leakage inductance degrades the switching
performance of T2 more than winding capacitance so T2 should be
bifilar wound to reduce leakage inductance. In consideration of
these principles, a unity turns ratio is chosen for T2 so that
the voltage on N4 is $6-V_{CE2}$ volts during t'_{on} and N4 and N5 are
wound turn for turn to minimize leakage inductance.

Solving for R1 in (84) and substituting for V_{CE2}, V_{BE1},
I_4, and n yields

$$R_1 = \frac{N_4 \left(6 - V_{CE2}\right)/N_5 - V_{BE1}}{I_4} = \frac{(6 - 0.8) - 1.7}{0.318} = 10.1 \ \Omega \ . \quad (85)$$

The value chosen from stock for R1 is 10 Ω as given in Table III.

Reverse bias. The next step in the design is to consider
$i_{4f}(t)$ during t'_{off}. This current should be sufficient during the
first part of t'_{off} to provide the current to sweep the charge
stored during t'_{on} from the emitter-base junction of Q1 so that
storage time and fall time are minimized. The current $i_{4f}(t)$
should also be nonzero during all of t'_{off} since reverse-biased
transistors can block greater collector voltage spikes. The
current $i_{4f}(t)$ is obtained from the energy stored in T2 during
t'_{on}. This stored energy should not be too great since $i_{5n}(t)$
must increase in magnitude proportionately. When $i_{5n}(t)$ in-
creases, $i_{b2}(t)$ must increase to maintain Q2 in saturation re-
sulting in more power dissipation and possibly a requirement for
another stage of amplification. This means that the energy

stored in T2 should be minimized to maintain a high efficiency, but enough energy must be stored to reverse bias Q1 and reduce the storage time of Q1.

Determination of L4, L5, and m. Under the condition of maximum source current, $i_{sn}(0)$ must be at least equal to I_4/n if Q1 is to be driven into saturation. In order to determine L4, L5, and the number of diodes m, t = 0 and K from (81) are substituted into (73) to obtain

$$i_{sn}(0) = K = \frac{\frac{6 - V_{CE2}}{L_5} t'_{on}}{e^{\frac{R_1}{L_4} t'_{off}} - 1} - \frac{N_4}{N_5}\left(\frac{m V_{FD}}{R_1} - I_4\right) \geq \frac{N_4 I_4}{N_5} \qquad (86)$$

where V_{CE2} = 0.8 volts, R_1 = 10 ohms, V_{FD} = 0.66 volts at 200 ma, N_4/N_5 = 1, $L_4 = L_5$, and I_4 = 0.318 amperes from (84). If switching response times are neglected, then $t'_{on} = t_{on}$ = 0.4 µsec from (50) and $t'_{off} = t_{off}$ = 0.6 µsec. Substituting these values into (86) yields

$$i_{sn}(0) = \frac{2.08 \times 10^{-6}}{L_5} \left[e^{\frac{6 \times 10^{-6}}{L_4}} - 1\right]^{-1} - 0.066 \, m + I_4 \geq I_4$$

$$(87)$$

which can be solved by trial and error for $L_4 = L_5$ and m. The number of diodes m must be less than 6 since the maximum emitter-base voltage $m V_{FD}$ for Q1 is 4 volts.

Since K is constant, the expression for Δi_{sn} is derived as

$$\Delta i_{sn} = \frac{6 - V_{CE2}}{L_5} t'_{on} \quad .$$
(88)

If it is assumed that $\Delta i_{sn} = 2$ ma to minimize the energy stored in T2, then solving (88) for L_5 yields

$$L_5 = \frac{6 - V_{CE2}}{\Delta i_{sn}} t'_{on} = \frac{6 - 0.8}{2 \times 10^{-3}} \, 0.4 \times 10^{-6} = 1.04 \text{ mH} \quad .$$
(89)

Letting $L_4 = L_5 = 1$ mH and substituting into (87) yields

$$\frac{2.08 \times 10^{-6}}{10^{-3}} \left(e^{\frac{6 \times 10^{-6}}{10^{-3}}} - 1 \right)^{-1} \geq 0.066 \text{ m}$$
(90)

and solving for m yields

$$m \leq 5.25 \text{ diodes} \quad .$$
(91)

If it is assumed that the current $i_{4f}\left(t'_{on}\right)$ at turn-off is 0.2 amperes, then the number of diodes needed to obtain this current can be computed by substituting $t = t'_{on}$ into (75) to obtain

$$i_{4f}\left(t'_{on}\right) = 0.2 \leq A - \frac{mV_{FD}}{R_1} \quad .$$
(92)

Solving (92) for m yields

$$m \le \frac{R_1}{V_{FD}} (A - 0.2) = \frac{R_1}{V_{FD}} \left[\frac{\frac{N_5}{N_4}\left(\frac{6 - V_{CE2}}{L_5} t'_{on}\right)}{1 - e^{-\frac{R_1}{L_4} t'_{off}}} - 0.2 \right] \quad . \quad (93)$$

Substituting known values into (93) yields

$$m \le \frac{10}{0.66} \left[\frac{\frac{6 - 0.8}{10^{-3}}(0.4 \times 10^{-6})}{1 - e^{-\frac{10}{10^{-3}}(0.6 \times 10^{-6})}} - 0.2 \right] = 2.24 \quad . \quad (94)$$

The lesser of the two values for m in (91) and (92), or m = 2, is chosen. Two 10A26 diodes are used for D2 and D3. The last step in the design of the drive circuit is to design T2 so that L_4 and L_5 are 1 mH.

Mutual inductor T2. As mentioned earlier a toroidol core configuration with $N_4 = N_5$ and bifilar winding is chosen to reduce the leakage inductance. In addition, Ferroxcube Corp. type 3D3 ferrite material is chosen because it has the lowest loss factor at a frequency of 1 MHz. The final procedure is to choose a core size, compute the number of turns which is required to make 1 mH, check the mmf to be certain that the core is not saturated, determine the wire size, and check to be certain that the turns for N4 and N5 fit in the window area. This procedure is repeated by trial and error until the smallest core that meets the requirements is found. For this converter, Ferroxcube Corp. toroidal core 768T188/3D3 is chosen. This core has an inductance factor A_L of 4.5 mH/1000 turns, a mean free

path length ℓ_e of 3.03 cm, and a window area A_C of 0.40 in^2.
The number of turns for N4 and N5 is calculated as

$$N_4 = N_5 = \left[L_5 (1000)^2/415 \right]^{1/2} = 10^3/(415)^{1/2} = 49.1 \text{ turns} \quad (95)$$

N4 and N5 are therefore chosen to be 49 turns. The mmf corres-
ponding to $i_{4f}\left(t'_{on}\right)$ is calculated as

$$H = 0.4\pi \; \frac{N_4 \, i_{4f}\left(t'_{on}\right)}{\ell_e} = 0.4\pi \; \frac{N_4 \left(A - \dfrac{mV_{FD}}{R_1}\right)}{\ell_e}$$

$$= 0.4\pi \; \frac{49\left[0.348 - \dfrac{2(0.66)}{10}\right]}{3.03} = 4.39 \text{ Oersteds .} \quad (96)$$

Since the saturation mmf for 3D3 material is 5 Oersteds, the
core is not driven to saturation. In order to determine the re-
quired wire size, the maximum full-cycle average value of the ab-
solute value of $i_4(t)$ and $i_5(t)$ must be determined. The maximum
values of $i_4(t)$ and $i_5(t)$ occur when $t'_{on} = 0.4$ μsec and
$t'_{off} = 0.6$ μsec. From Fig. 17 knowing that $\Delta i_{5n} = 2$ ma, $\overline{i_5(t)}$
is

$$\overline{i_5(t)} = \frac{t'_{on}}{T}\left(K + \frac{\Delta i_{5n}}{2}\right) = \frac{0.4}{1.0}\left(0.532 + \frac{0.002}{2}\right) = 0.213 \text{ Amperes} \quad (97)$$

Again using Fig. 17

$$\overline{i_4(t)} = \left[I_4 t'_{on} + \frac{1}{2} \left(A - \frac{mV_{FD}}{R_1} + \frac{N_5 K}{N_4} - I_4 \right) t'_{off} \right] / T$$

$$= \left\{ 0.318(0.4) + \frac{1}{2} \left[0.348 - \frac{2(0.66)}{10} + 0.532 - 0.318 \right] 0.6 \right\} / 1.0$$

$$= 0.1272 + \frac{1}{2}(0.430)0.6 = 0.256 \text{ Amperes} \quad . \tag{98}$$

Based on 1000 circular mils per ampere N4 and N5 can be wound using AWG 26 wire. This wire with heavy formvar insulation can be wound with 2932 turns per in^2. Assuming a winding factor of 0.4, the number of turns N of AWG 25 that can be wound on core 768T188/3D3 is

$$N = 0.4 \left(A_c \right) 2932 = 0.4(0.4)2932 = 469 \text{ turns} \quad . \tag{99}$$

Since N4 + N5 = 98 is much less than 469, the design of T2 and the converter has been completed. The next section gives the experimental results and some conclusions.

Experimental Results

This section discusses experimental data obtained from the 1 MHz dc to dc converter shown in Fig. 11. Regulation and efficiency characteristics for the converter are given. Photographs of selected waveforms in the circuit are used to show properties such as voltage and current amplitudes and switching times. Throughout the section, design techniques which could improve the performance of the converter are discussed.

Fig. 18 shows the output voltage V_O regulation charac-
teristics for load conditions from light to heavy. The conver-
ter should not be operated with no load because the voltage on
C3 and C4 could exceed safe operation limits causing the destruc-
tion of one or more components. A 50 to 100 KΩ resistor could be
added in parallel with R_L to prevent no-load conditions. The
addition of this resistor would cause additional power loss of
only 8 to 16 mw. Fig. 18 shows a family of three curves; one
each for the minimum source voltage E_S of 21 volts, an E_S of 26
volts, and the maximum E_S of 31 volts. Over the full range of
data, V_O varied from 27.48 to 28.30 volts for a mean value of
27.89 volts. The output voltage regulation can be expressed as
±1.47 percent about the mean of 27.89 volts. When P_O increases,
the average source current must increase. Consequently, output
voltage V_L decreases as the output power P_O increases and as the
source voltage E_S decreases because losses in the main power
path caused by greater currents are not fully compensated by the
converter. Regulation can be improved by decreasing the ampli-
tude of the triangular waveform v_t. However, when this is done,
it may also be necessary to reduce the comparator hysteresis for
example by using a feedback resistor from the output to the pos-
itive input of the comparator. Additionally, it may be neces-
sary to reduce the magnitude of the output ripple voltage at the
input to the comparator if it is on the order of the new magni-
tude of v_t.
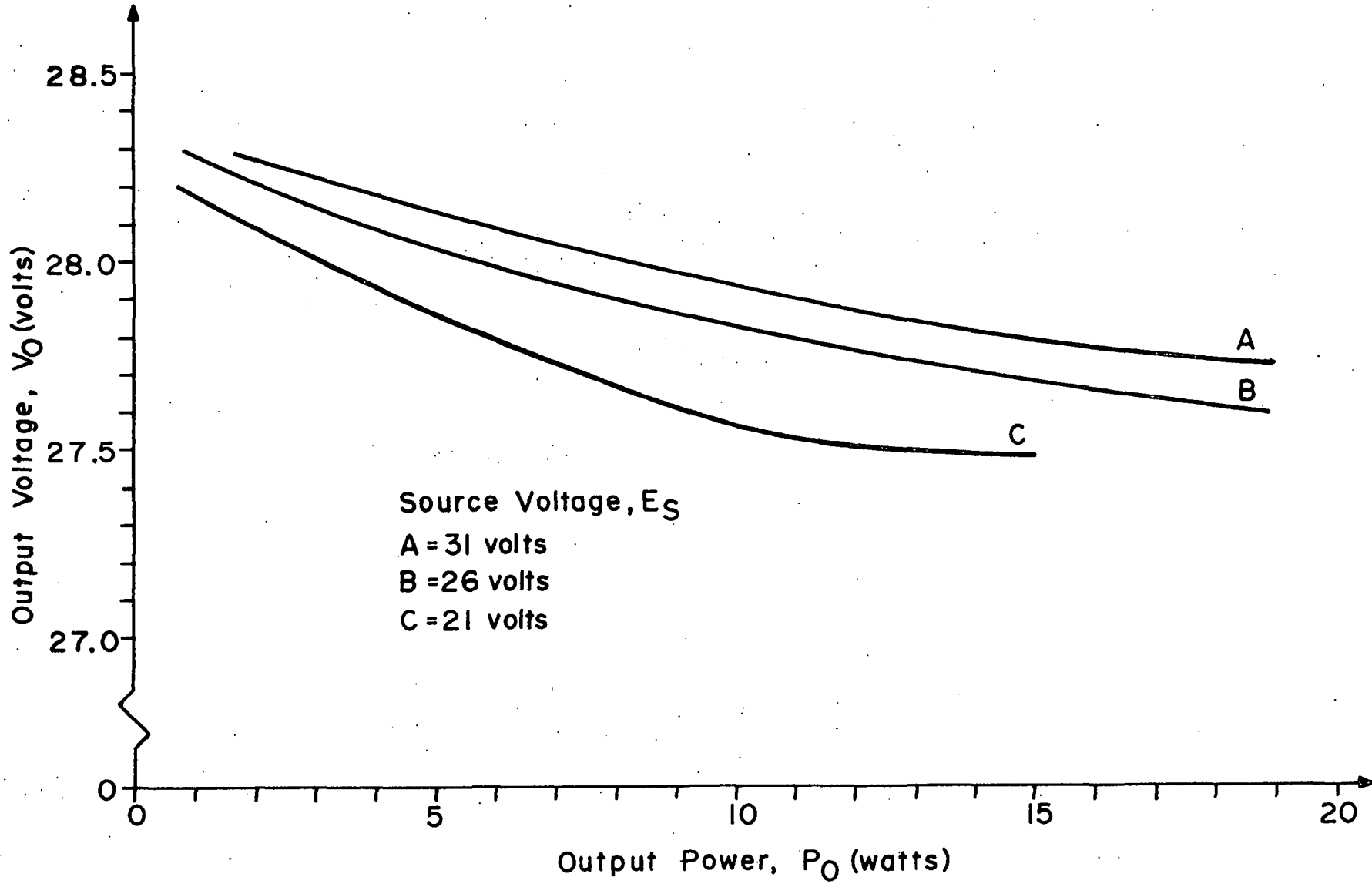
Fig. 18. Converter regulation characteristics.

Source Voltage, E_S

A = 31 volts

B = 26 volts

C = 21 volts

The converter efficiency characteristics shown in Fig. 19 were obtained by measuring the current and voltage of each source E_S, +12 volts, +6 volts, and -6 volts and computing the input power to the converter as the sum of the power from these four sources. The output power P_O was computed as the square of the output voltage V_O divided by the load R_L. The efficiency shown is the ratio of these power computations. Three curves are shown; one each for E_S = 21, 26, and 31 volts. Each curve has the same general shape. Efficiency is lower for higher source voltages and is a minimum at light load. Efficiency increases as load increases passing a maximum at $P_O \cong 10$ watts and decreasing slightly as P_O increases.

Power losses occur in several major areas of the converter. These are semiconductor static and switching losses, core losses, and power transistor Q1 drive circuit losses. Other areas where power losses are not as significant are the power supplied to the comparator and triangular waveform generator, the copper loss in the circuit wiring, and the filter capacitor series and shunt resistances.

Transistor Q1 static power loss includes the product of collector current I_1 during the on time, saturation voltage $V_{CE(sat)}$, and the duty cycle. This loss increases when the collector current or duty cycle increases, that is when P_O increases or E_S decreases. Static loss also includes the product of the blocking voltage and leakage current during the off time

Fig. 19. The collector-emitter voltage $v_{CE1}(t)$ and
the collector current $i_1(t)$ when $E_S = 21$
volts and $R_L = 100$ ohms.

multiplied by 1-duty cycle and this loss increases when E_S increases or the duty cycle decreases. Dynamic losses occur during the switching times and are the integrals of the products of $v_{CE}(t)$ and $i_C(t)$ during turn-on and turn-off multiplied by the respective time periods of the integrations and divided by T. Dynamic losses also increase as E_S and P_O increase. Static and dynamic losses in diode D1 behave the same as the losses in Q1 except that D1 is off when Q1 is on. This means that static power loss when D1 is on decreases with duty cycle and vice versa.

Core losses are highly dependent on frequency which is constant in this converter; however, hysteresis losses increase as the flux excursion increases and copper losses increase as the current levels increase. This means that core loss increases as P_O increases.

Power required to supply the base drive to Q1 is the third major area of power dissipation. The drive circuits dissipate more power when Q1 and Q2 are on so the power dissipated in these circuits increases as the duty cycle increases, or as P_O increases and E_S decreases.

Figs. 19 and 20 show the collector-emitter voltage V_{CE1} and the collector current i_1 waveforms of power switching transistor Q1. The waveforms in Fig. 19 are for the conditions $E_S = 21$ volts and $R_L = 100$ ohms. In both figures, (a) shows a full period of the waveform, (b) shows the turn-on portion

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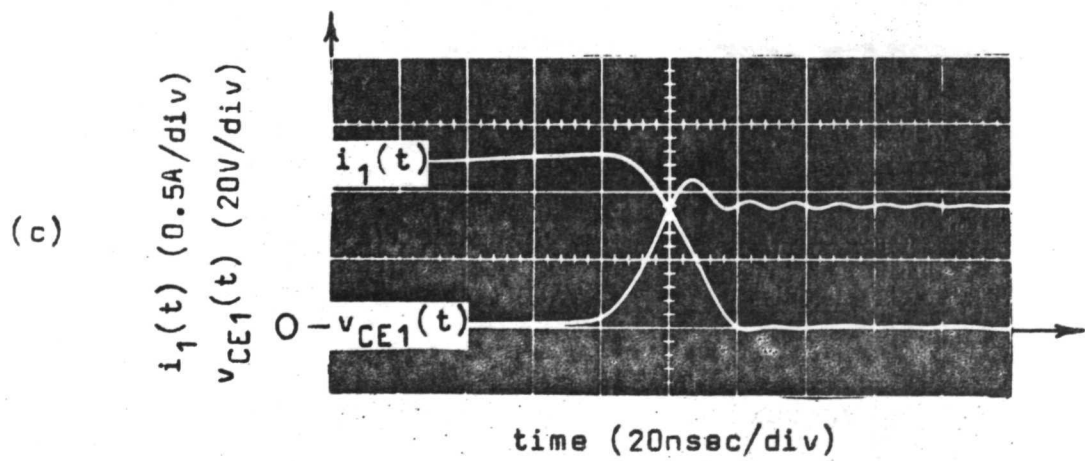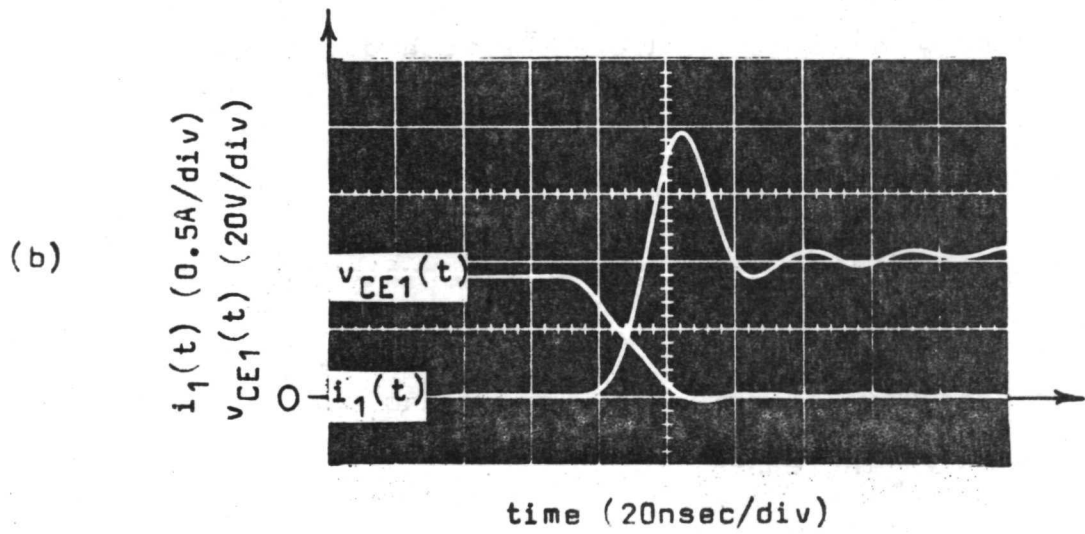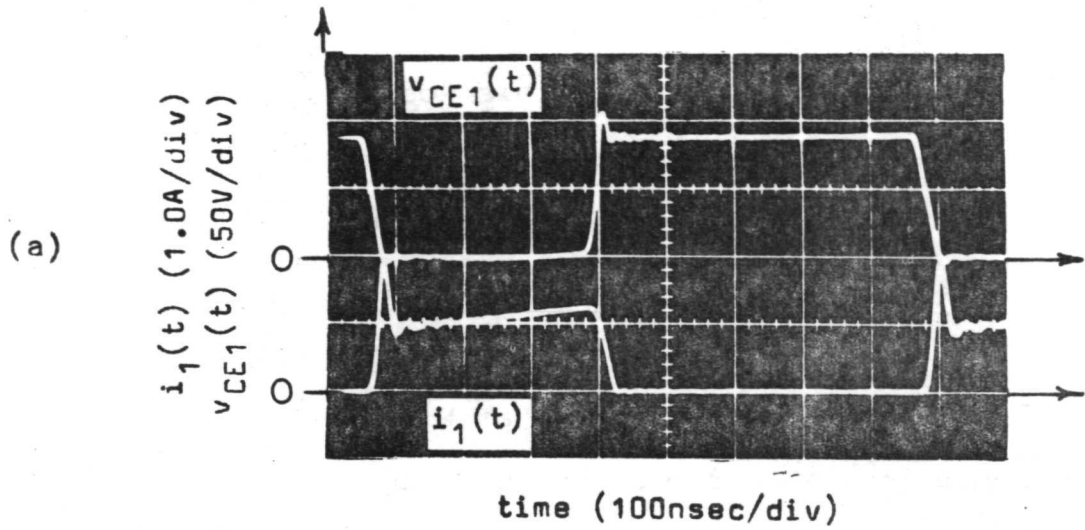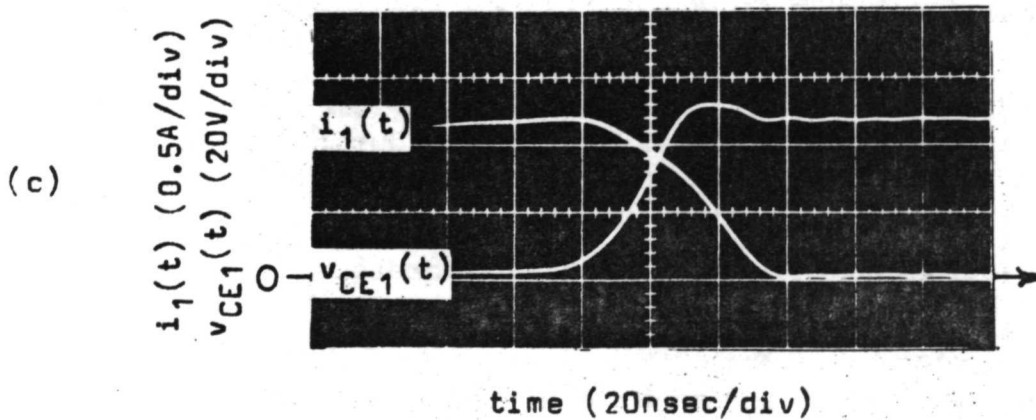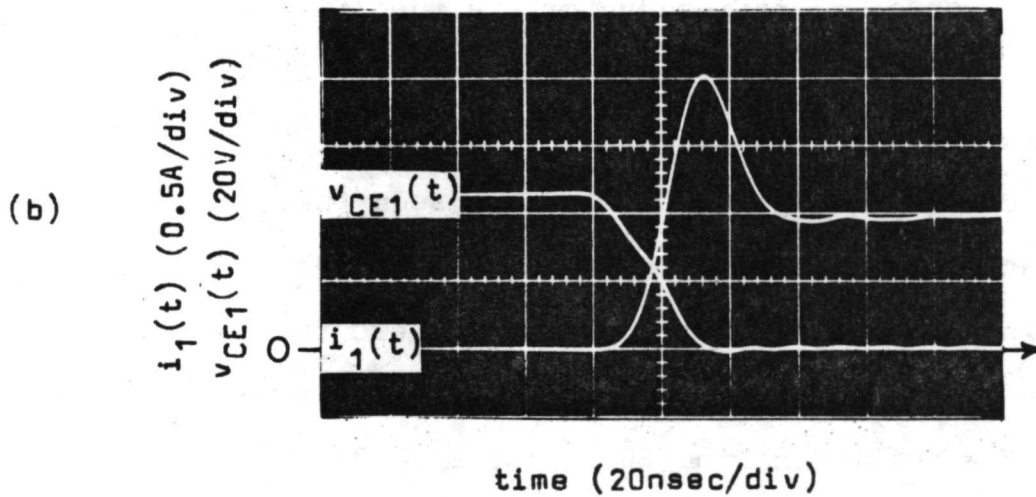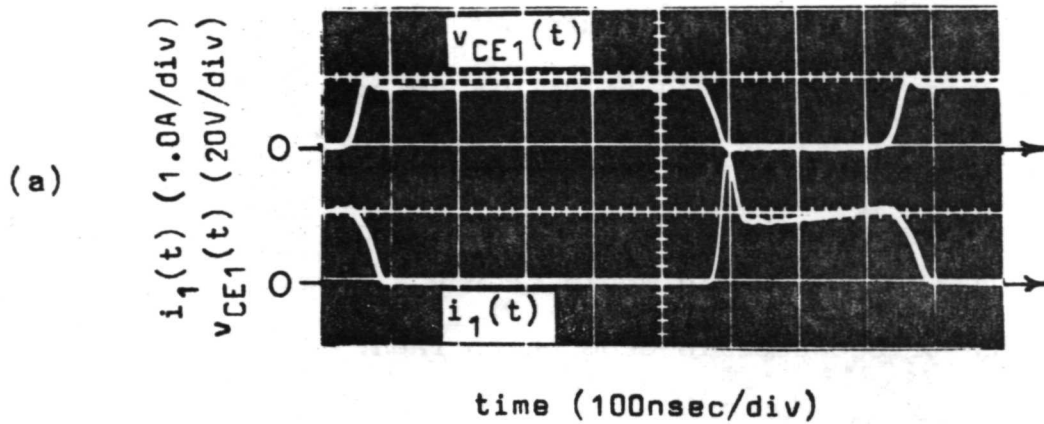

Fig. 20. The collector-emitter voltage $v_{CE1}(t)$ and the collector current $i_1(t)$ when $E_S = 31$ volts and $R_L = 100$ ohms.

expanded, and (c) shows the turn-off portion expanded. By examining Figs. 19(a) and 20(a), it is determined that the time T for a full period is 0.8 μsec resulting in a switching frequency of 1.25 MHz. The frequency was increased slightly above 1 MHz so that the entire period would occupy slightly less than the full width of one oscilloscope photograph.

In the beginning of this chapter, the fact that the switching speed of semiconductors is the limiting factor for designing switching converters at a frequency as high as 1 MHz was discussed. This limitation shows up in the experimental efficiency curves in Fig. 21. It can be seen that efficiency is lower at higher values of E_S. This phenomena occurs because switching loss in D1 and especially Q1 are the major power losses in the converter and these losses increase as E_S increases. The waveform in Fig. 20(c) for E_S = 31 volts shows a significant increase in the switching time as well as the magnitude of voltage switched in comparison to the waveform in Fig. 19(c) for E_S = 21 volts. The increase in semiconductor switching losses and semiconductor static losses during the off time exceeds the decrease in saturated semiconductor losses, drive circuit losses, and core loss when E_S increases. The fact that the majority of the converter power loss is in Q1 is supported by the fact that this component operates at a higher temperature than any other in the converter even though it is mounted on a heavy copper heat sink. Fig. 19(b) indicates that v_{CE1} switches from 90 to 10 percent of the blocking voltage in 25 nsec. The
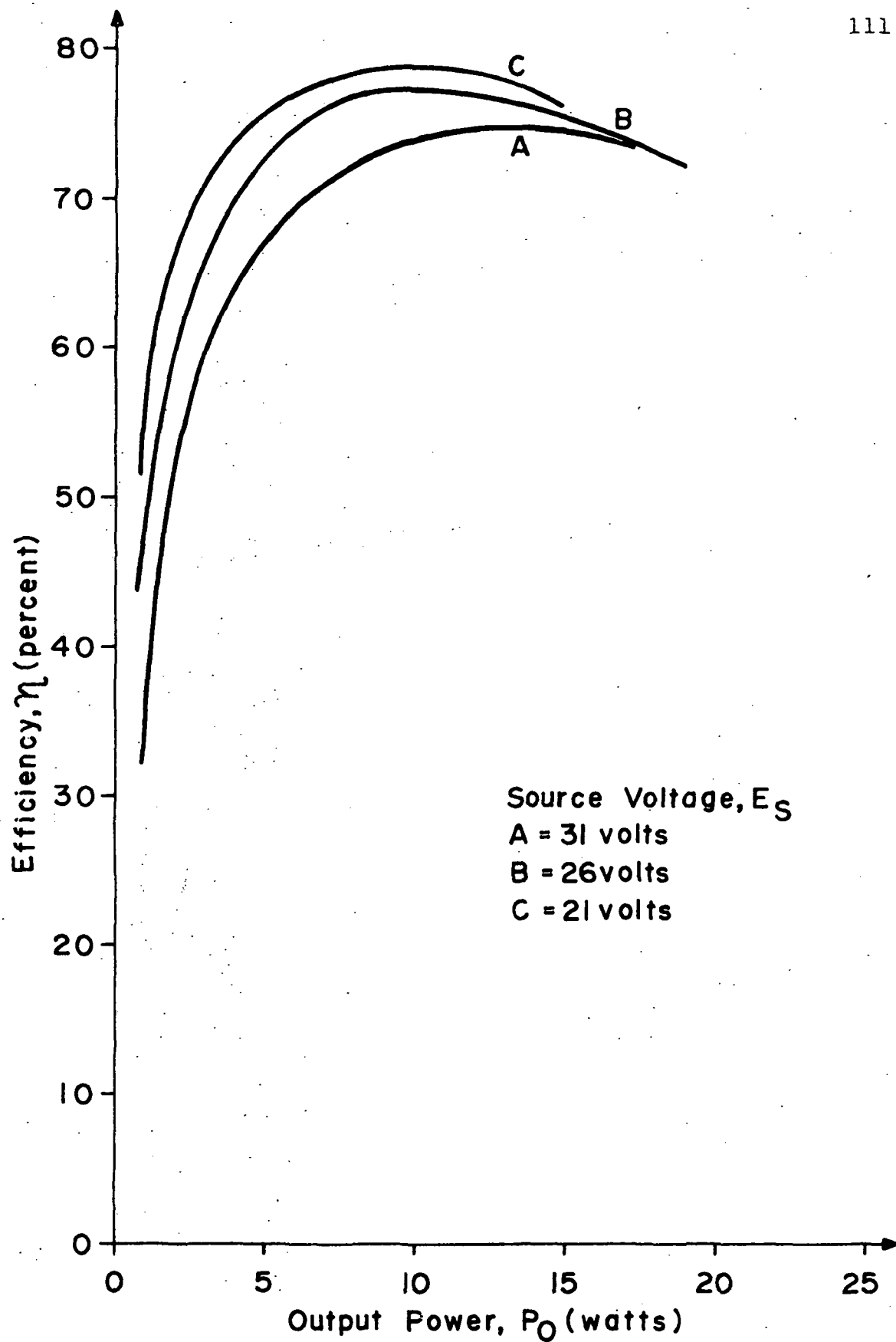
Fig. 21. Converter efficiency characteristics.

collector current i_{C1} switches from 10 to 90 percent of the linearly extrapolated initial current in 10 nsec. The collector current appears to switch much faster than v_{CE1} and reaches a peak much higher than the initial current. This peak is coupled through T1 and is inverted in the waveform for i_2. In addition, the peak increases if external capacitance is added in parallel with D1; therefore, it is assumed that the current peak is the current required to charge the junction capacitance of D1 when Q1 turns on. This suggests that switching losses in Q1 during turn-on may be reduced if the junction capacitance of D1 can be reduced.

In general, the performance characteristics of this 1 MHz dc to dc converter are good. Regulation is less than 1.5 percent and efficiency approaches 80 percent at power outputs from 5 to 20 watts. Switching in the main power path is accomplished in less than 10 percent of the full period at a switching frequency of 1 MHz. Some conclusions about the 1 MHz converter are given in the next section.

Conclusion

Most dc to dc converters are designed with typical operating frequencies from 2 to 20 kHz and maximum operating frequencies in the vincinty of 100 kHz. The design of a 1 MHz converter was begun because of requirements for satellites to measure electromagnetic radiation in outer space within the

frequency range of 0.2 to 100 kHz. In order that the power conditioning equipment on the satellites does not interfere with the measurements, the switching frequencies must be well above the 0.2 to 100 kHz range, for example 1 MHz. The converter design discussed in this chapter demonstrates the feasibility of designing converters at megahertz switching frequencies.

The chapter begins with a discussion of design principles which must be considered when designing circuits to switch at frequencies near 1 MHz. In general, stray inductance, capacitance, and coupling must be kept small by shielding and keeping circuit lead length to a minimum. Also, the circuit components must meet special high-frequency requirements. Magnetic materials with low loss factors at 1 MHz and high-frequency capacitors must be used. Leakage inductance in the mutual inductors has to be minimized to prevent large voltage spikes on the switching elements. In addition, high-frequency bypass capacitors are required at various points in the circuit to reduce switching spikes. Integrated circuits are needed in the control circuits for the differential voltage comparator and the triangular waveform generator in order to reduce the effects of stray parameters and to obtain faster switching speeds. The power switching diodes and transistors used in the design need to switch the required voltage and current at least as fast as 50 nsec. The switching speed of the power transistor is considered to be the most significant factor limiting an additional increase in switching frequency and only a few diodes and

transistors are available which switch the required voltage and current as fast as 50 nsec.

The design of the converter is approached by dividing the converter into five basic circuits excluding the DC Source and the Load. These circuits are shown in Fig. 10 as the Power Circuit, Output Filter, Drive Circuit, Differential Voltage Comparator, and Triangular Waveform Generator. The Triangular Waveform Generator oscillates at a constant frequency of 1 MHz which determines the operating frequency of the converter and, in conjunction with the Comparator, determines the duty cycle required to maintain regulation. The Drive Circuit amplifies the duty cycle signal from the Comparator to a sufficient power level to drive the power transistor in the Power Circuit. The Power Circuit converts the dc power from the Source to ac power and back to dc power with a regulated average direct voltage level which can be at either a higher or lower voltage level than the source. The Output Filter averages the switched direct voltage from the Power Circuit to a constant value on the Load with sufficiently small ripple voltage.

The particular circuit configuration utilized for this converter was chosen because it provides electrical isolation between the source and the load and a regulated output voltage which may be either greater than or less than the source voltage. The choice of a megahertz switching frequency reduces the values of required capacitors, especially the filter capacitors, and

permits the use of ceramic capacitors instead of electrolytic capacitors. This is an advantage since electrolytic capacitors are considerably less reliable than ceramic capacitors as was discussed in the previous chapter. The high switching frequency reduces the size and weight of the circuitry especially in the areas of magnetic components and capacitors in the output filter and power circuit.

The power output of the converter was designed to be 20 watts; however, the power switching transistor Q1 is capable of processing more power. The converter power output can be increased by redesigning mutual inductor T1 to process the additional power and by increasing the output capability of the Drive Circuit so that more base drive is provided to Q1. The output voltage regulation is ±1.47 percent and might be able to be improved by reducing the hysteresis of the Comparator and the magnitude of the triangular waveform v_T. The maximum efficiency of 79 percent occurs at P_O = 10 watts and decreases to 72 percent at the full power output of 20 watts. The efficiency is not as high as efficiencies of the lower-switching-frequency converters which are in the range of 90 percent but should be considered good for a switching frequency of 1 MHz. The majority of the power losses are the static and switching losses of transistor Q1. Therefore, the efficiency of this converter will be improved with the availability of power transistors with faster switching speeds, lower saturation voltages, and higher current gains.

This converter is not inherently self-starting. By the nature of the regulation means, Q1 remains on as long as V_A is below its level at regulation. This means that Q1 will remain on continuously as long as V_A is less than V_{tm} plus its value when the converter is regulating. To make the converter self-starting, a circuit which switches Q1 at a fixed duty cycle adequate to achieve at least $V_O = 28$ volts under the conditions of minimum R_L and E_S must be included in the design. The starting circuit must also be designed to turn off when V_O reaches 28 volts. Starting is an important subject but this dissertation does not address it. The emphasis is on designing a converter to operate at a switching frequency of 1 MHz with reasonable efficiency.

The next chapter of this dissertation is purely analytical. The method of closed loop regulation with a triangular waveform and a voltage comparator as used in the converter discussed in this chapter is analyzed using the technique of nonlinear analysis which employs the phase plane and sequence functions.

Chapter IV

PHASE-PLANE ANALYSIS OF A SWITCHING REGULATOR

SYSTEM DRIVEN BY A SMALL-AMPLITUDE

TRIANGULAR WAVEFORM

Because of the mathematical difficulties encountered
the nonlinear analysis of switching systems is usually restricted
out of necessity to those systems which yield autonomous equa-
tions. The equations of these systems depend on time only
through the derivative with respect to time and on the circuit
parameters which must be independent of time. Often, however,
one encounters systems which have one or more properties that are
dependent on a driving function.

The last chapter presented the design of a circuit which
uses a triangular driving function in a dc to dc converter to
determine a duty cycle which, in the closed-loop system, main-
tained a regulated output voltage. This system serves as a model
of the type of circuit which is the subject of the nonlinear
analysis presented in this chapter. The system is a switching
system which is linear during each state of the switch.

The nonlinear analysis of switching systems may be per-
formed by the method of point transformations in piece-wise

linear systems [25]. In this method, each mode of the switching system is considered a linear system. A set of initial conditions are assumed and are transformed using the linear system equations into the final conditions of the first mode. These final conditions are assumed as the initial conditions of the second mode and the second mode final conditions are derived. This process continues until the final conditions of the final mode are determined. These conditions may then be equated to the assumed first set of initial conditions to determine the system equations for the steady-state system. A total phase plane can then be drawn which consists of segments which are defined by the linear systems' equations for each mode of the switching system. The analysis performed in this chapter shows that a periodic triangular driving function in a regulator system can be analyzed using the method of point transformations in piece-wise linear systems. The application of this method to a regulator system utilizing a triangular driving function is shown to be dependent on the amplitude voltage of the triangular function being small compared to the reference voltage and on the fact that the time derivative of a triangular function is constant during fixed periods of time.

The first section of this chapter develops the model for the analysis and gives the assumptions which are made. In addition, the means by which regulation is maintained is briefly discussed to expand the explanation given in Chapter III to include hysteresis. The next section is devoted to developing the

system equations for each linear state of the system. These
equations are used to sketch the limit cycle in the phase-plane
for the system, and the method of point transformations is ap-
plied to obtain the sequence functions defining the steady-state
conditions. The final section is devoted to conclusions which
can be made about the analysis. An experimental limit cycle
for a converter operating at a switching frequency of 2 kHz is
compared to the theoretical limit cycle and the accuracy of the
sequence functions are experimentally verified in Appendix C.
Parameters and circuit conditions for this converter are shown
in Table C.2.

Development of the System Model

The circuit for which the analysis of this chapter is
performed is a regulated dc to dc converter using inductive-
energy storage and having electrical isolation between the
source and load. The 1 MHz converter discussed in detail in the
previous chapter is an example of a converter of this type.
However, the high operating frequency prohibits a direct appli-
cation of the analysis to this specific converter since a fre-
quency of 1 MHz would require the inclusion of effects such as
stray capacitance, leakage inductance, and finite switching
times which would overly complicate the analysis but which can
be neglected at lower operating frequencies. It is for this
reason that the experimental verification in Appendix C is made

using a 2 kHz converter.

In order to perform the analysis, a model must be established and assumptions must be made. Fig. 22 shows a diagram of the model which is to be used. This diagram is used in the next section of this chapter to develop the system equations. In order to develop the model depicted in Fig. 22, it is assumed that the mutual inductor is unity coupled so that it has no leakage inductance and that it has no distributed capacitance. Also, transistor Q and diode D are assumed to switch instantaneously. Any internal series resistance in the source E and primary inductance L_p is combined with the effective saturation resistance of power transistor Q to form R_p. Similarly, the internal series resistance of the secondary inductance L_s is combined with the forward resistance of diode D to form R_s. It is also necessary to include in the analysis the internal series resistance R_C of filter capacitor C. The load resistance is R. The primary current is i_p, the secondary current is i_s, the load current is i_L, and the output current of the hysteresis block which drives Q is i_H. The collector-emitter voltage on Q is v_{CE}, the anode-cathode voltage on D is v_D, and the output, or load, voltage is v.

The system operation is described in detail in Chapter III and is described only briefly here. Energy from the source E is stored in L_p as i_p increases during the time t_{on} when Q is in saturation. It should be observed that the relative
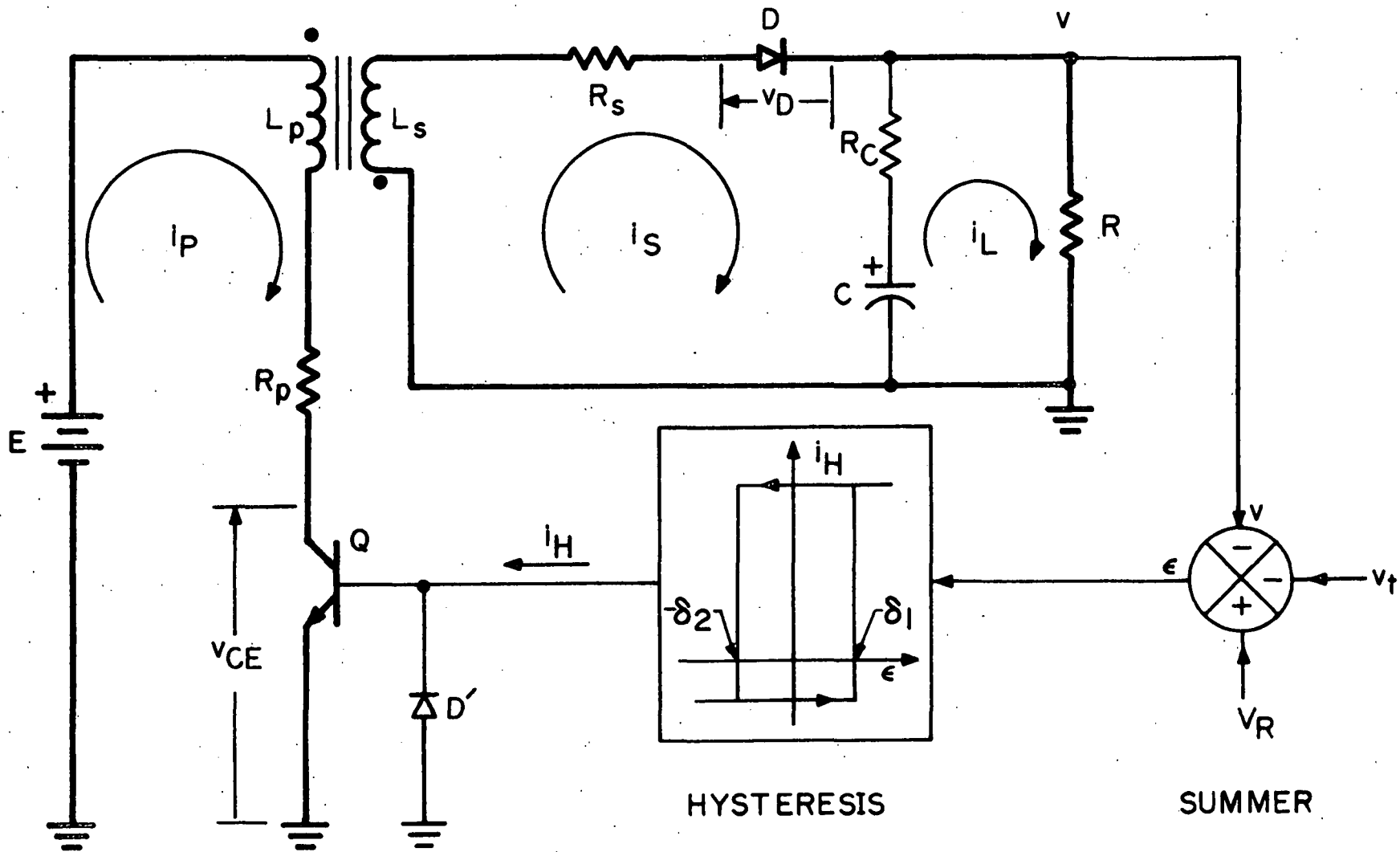
Fig. 22.   The system model.

polarities of the voltages across L_p and L_s are such that diode D is reverse-biased during t_{on} and i_s must be zero; however, C is discharging into R so that the output voltage v is maintained. During t_{off} when Q is blocking and D is conducting, i_p is zero and the energy stored in the mutual inductor is discharging through L_s into C and R by means of i_s. In this manner, capacitance C and L_s act as a filter which smooths the secondary current pulses i_s producing a dc voltage with small amplitude ripple on R.

The summer shown in Fig. 22 is used to add a triangular waveform v_t to the output voltage v and to compare this sum with the reference voltage V_R. The difference of V_R and $v + v_t$ is the error voltage ϵ which is given by

$$\epsilon(t) = V_R - v(t) - v_t(t) \quad . \tag{100}$$

In typical applications, the summer is part of a differential voltage comparator. This circuit switches between two modes whenever ϵ exceeds a certain voltage level or falls below another voltage level. The two modes are forward current i_H and reverse current $-i_H$. Diode D' provides a path for the reverse current during t_{off}. This type of switching has a hysteresis characteristic as shown in Fig. 22 where δ_1 and $-\delta_2$ are the switching levels for ϵ.

The means of regulation can best be understood by examining Fig. 23. This figure shows the time variation of $v + v_t(t)$
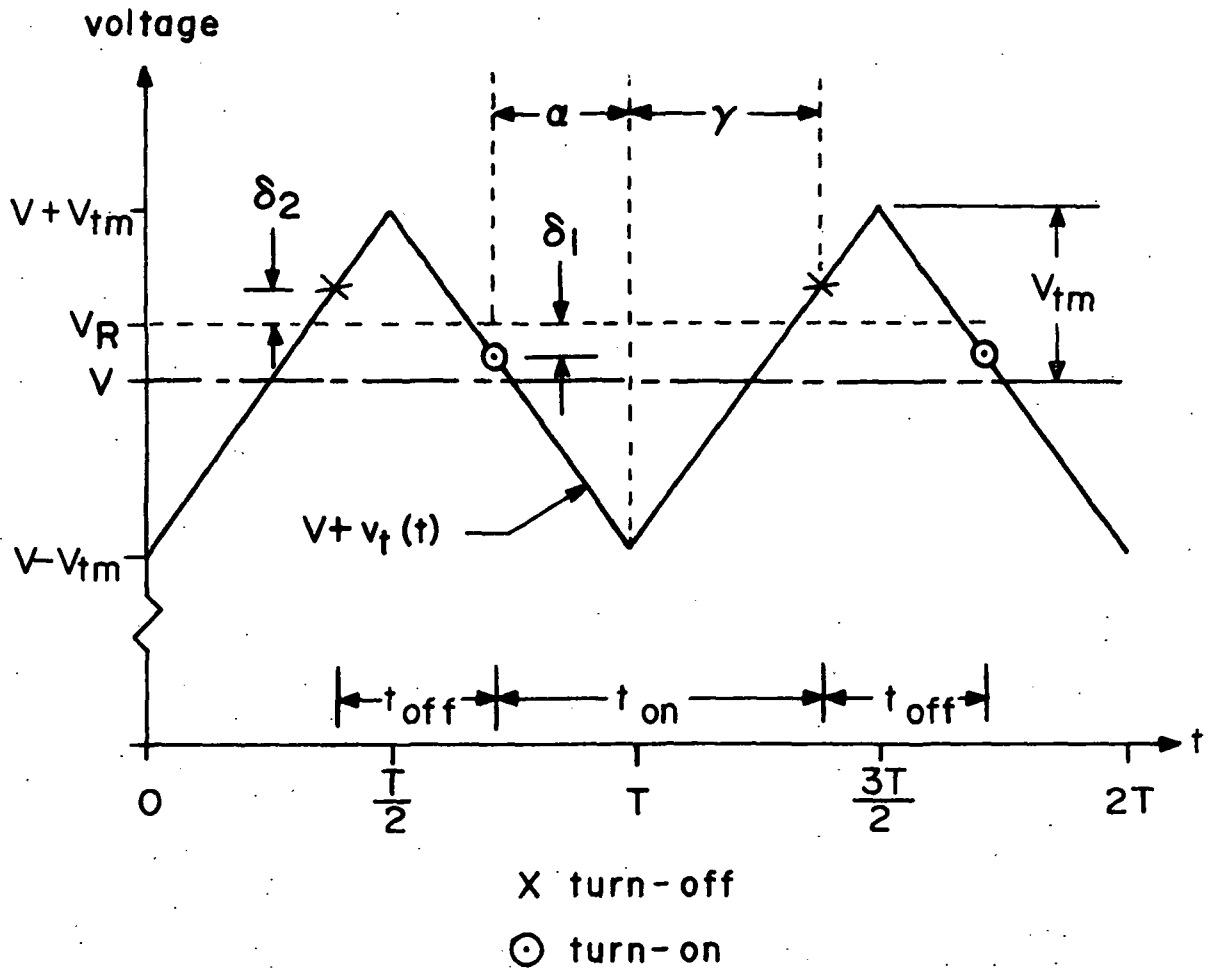
Fig. 23. Utilization of the triangular waveform to determine duty cycle.

where v is assumed to have a constant value V which is equiva-
lent to assuming negligible ripple voltage on the load R and
steady-state conditions. This assumption is made only to sim-
plify the explanation of regulation and is not required in the
analysis. The error voltage ϵ at the input terminals of the
hysteresis block is portrayed as the difference between the
dotted reference line V_R and any arbitrary point on the $V + v_t(t)$
waveform. ϵ is positive when V_R is greater than $V + v_t(t)$ and is
negative when $V + v_t(t)$ is greater than V_R. The period of $v_t(t)$
is shown to be T. The instant when turn-off occurs is marked
by a cross where $V + v_t(t)$ is greater than V_R by δ_2 and must al-
ways occur on the positive slope of $v_t(t)$. If the waveform
$V + v_t$ always lies below $V_R + \delta_2$, i.e., if $V + V_{tm} < V_R + \delta_2$ or
$\epsilon = V_R - V - v_t > -\delta_2$, then Q will never turn off. The instant of
turn-on is marked by a circle and occurs when $V + v_t(t)$ is less
than V_R by δ_1 and must always occur on the negative slope of
$v_t(t)$. If the waveform $V + v_t$ always lies above $V_R - \delta_1$, i.e.,
if $V - V_{tm} > V_R - \delta_1$ or $\epsilon < \delta_1$, then Q will never turn on. Upon
studying Fig. 23 further, it can be seen that as V increases t_{on}
decreases and t_{off} increases. This is the same phenomenum ex-
plained in Chapter III using Fig. 15 where the hysteresis was
neglected. The approximate dc or steady-state relationship be-
tween the source voltate E and the output voltage V can be de-
rived by equating the expressions for the flux excursions during
t_{on} and t_{off} as [22]

$$V \cong \left(N_s/N_p\right)\left(t_{on}/t_{off}\right)E \quad . \tag{101}$$

The derivation of this equation assumes that there is negligible resistance in the dc current paths for i_p and i_S, that V remains constant, that v_{CE} during t_{on} and v_D during t_{off} are negligible compared respectively to E and V, and that switching occurs instantly.

Formulation of the System Equations

The objective of this section is to develop differential equations which can be used to describe trajectories on the phase plane for which the method of point transformations can be applied. The development begins with the differential equations for the output voltage v for the two states, t_{on} and t_{off}, of the system derived for the circuit in Fig. 22 assuming instantaneous switching and a linear B-H characteristic for the mutual inductor. During t_{on}, diode D is reverse-biased and $i_S = 0$; therefore, v is described by a simple first-order differential equation for the current loop for i_L where $v = Ri_L$ as

$$\frac{dv}{dt} + \frac{1}{\left(R + R_C\right)C} v = 0 \quad . \tag{102}$$

During t_{off}, D is forward-biased and i_S is nonzero. Since i_L is now dependent on two energy-storage components, L_S and C, the derived equation for v during t_{off} is a second-order differential equation given by

$$\frac{d^2v}{dt^2} + \left[\frac{1}{RC} + \frac{R_C + R_s}{L_s}\right]\frac{dv}{dt} + \frac{1}{L_s C}\,v = -\frac{V_D}{L_s C} \tag{103}$$

where it has been assumed that V_D is constant and R_C and R_s are negligible compared to R. Equations (102) and (103) are derived in detail in Appendix A.

If a phase plane for dv/dt versus v is considered, the switching points must be described by solving (100) for v(t) as

$$v(t) = V_R - v_t(t) - \epsilon(t) \quad . \tag{104}$$

The switching points for v(t) are found by substituting $\epsilon(t) = \delta_1$ and $-\delta_2$. When this is done, it is obvious that the switching lines drawn in the dv/dt versus v phase plane do not have fixed positions since v is still a function of the time-varying triangular waveform v_t. In order to obtain fixed switching lines in the phase plane, a change of dependent variable from v to ϵ is made using (104). Substituting v(t) from (104) into (102) yields

$$\frac{d\epsilon}{dt} + \frac{1}{T_C}\,\epsilon = \frac{V_R - v_t}{T_C} - \frac{dv_t}{dt} \tag{105}$$

where $T_C = \left(R + R_C\right)C \approx RC$; and substituting v(t) into (103) yields

$$\frac{d^2\epsilon}{dt^2} + \left[\frac{1}{RC} + \frac{R_C + R_s}{L_s}\right]\frac{d\epsilon}{dt} + \omega_0^2\,\epsilon = \omega_0^2\left(V_D + V_R - v_t\right) - \left[\frac{1}{RC} + \frac{R_C + R_s}{L_s}\right]\frac{dv_t}{dt}$$

$$\tag{106}$$

where $\omega_0^2 = \left[L_s C\right]^{-1}$. Since switching occurs whenever $\varepsilon = \delta_1$ or $-\delta_2$ which are constants, switching points are located on fixed lines in the phase plane.

Equations (105) and (106) can be put in a more compact form which is more easily analyzed by normalizing the variables. In this case, time is normalized with respect to the period of the natural frequency ω_0 as

$$\tau = \omega_0 t \quad . \tag{107}$$

Also, the error voltage ε is normalized to the reference voltage V_R as

$$x = \varepsilon/V_R \quad . \tag{108}$$

When the changes in variables defined in (107) and (108) are made in (105) and (106), they become

$$\frac{dx}{d\tau} + \frac{1}{\tau_C} x = \frac{V_R - v_t}{V_R \tau_C} - \frac{dv_t}{d\tau} \tag{109}$$

$$\frac{d^2 x}{d\tau^2} + 2h \frac{dx}{d\tau} + x = \frac{V_D + V_R - v_t}{V_R} - 2h \frac{dv_t}{d\tau} \tag{110}$$

where τ_C is the normalized time constant of the i_L current loop during t_{on} and is defined by

$$\tau_C = \omega_0 \left(R + R_C\right) C = \omega_0 T_C \tag{111}$$

$v_t = v_t/V_R$ is the normalized triangular waveform, $dv_t/d\tau$ is the normalized derivative of the triangular waveform defined by

$$\frac{d\nu_t}{d\tau} = \frac{1}{\omega_0 V_R} \frac{dv_t}{dt} \qquad (112)$$

and h is the normalized damping factor during t_{off} defined by

$$h = \frac{1}{2\omega_0}\left(\frac{1}{RC} + \frac{R_C + R_s}{L_s}\right) . \qquad (113)$$

It can be seen that (109) and (110) are the generalized first and second order linear differential equations in terms of the normalized error voltage x with time-dependent driving functions on the right-hand sides of the equations. These driving functions result from the addition of the time-dependent periodic triangular voltage $v_t(t)$ to the output voltage v at the summer shown in Fig. 22. Equations (109) and (110) are nonautonomous equations which are difficult to analyze, especially using phase-plane techniques. In the $dx/d\tau$ versus x phase plane, (109) is represented as a straight line with a slope of $-1/\tau_C$ and the ordinate intercept equal to the value of the right-hand side; therefore this line moves parallel to itself with the ordinate and abscissa intercepts varying as v_t and dv_t/dt vary. If $0 < h < 1$ in (110), the solution of this equation in the phase plane is a stable focus whose equilibrium point is located on the abscissa at the value of x equal to the right-hand side of (110); therefore the equilibrium point of this focus moves along the x-axis as v_t and dv_t/dt vary with time.

Equations (109) and (110) can be simplified if the nature of $v_t(t)$ is examined. The peak value V_{tm} of $v_t(t)$ can always be much smaller than V_R so that $V_{tm} << V_R$. Because of this, v_t in the numerators of the first terms on the right-hand sides of (109) and (110) can be neglected. Additionally, by the nature of a triangular waveform, dv_t/dt and $dv_t/d\tau$ are constant and have equal magnitudes but opposite signs during half of the total time period T of v_t so that for $0 \leq t \leq T/2$ using the time reference given in Fig. 23

$$\frac{dv_t}{dt} = \frac{4V_{tm}}{T} \tag{114}$$

and for $T/2 \leq t \leq T$

$$\frac{dv_t}{dt} = \frac{-4V_{tm}}{T} \quad . \tag{115}$$

Substituting (114) and (115) respectively into (112) yields the normalized derivatives for $0 \leq t \leq T/2$ as

$$\frac{dv_t}{d\tau} = \frac{4V_{tm}}{\omega_0 V_R T} \tag{116}$$

and for $T/2 \leq t \leq T$ as

$$\frac{dv_t}{d\tau} = \frac{-4V_{tm}}{\omega_0 V_R T} \quad . \tag{117}$$

By neglecting v_t and substituting (116) and (117) into (109) and (110) the following equations are obtained

DURING t_{on}:

$$\frac{dx}{d\tau} + \frac{1}{\tau_C} x = \frac{1}{\tau_C} - \frac{4V_{tm}}{\omega_0 V_R T} \qquad \begin{array}{l} 0 \le t \le T/2 \\[6pt] 0 \le \tau \le \omega_0 T/2 \end{array} \tag{118}$$

$$\frac{dx}{d\tau} + \frac{1}{\tau_C} x = \frac{1}{\tau_C} + \frac{4V_{tm}}{\omega_0 V_R T} \qquad \begin{array}{l} T/2 \le t \le T \\[6pt] \omega_0 T/2 \le \tau \le \omega_0 T \end{array} \tag{119}$$

DURING t_{off}:

$$\frac{d^2 x}{d\tau^2} + 2h \frac{dx}{d\tau} + x = 1 + \frac{V_D}{V_R} - \frac{8hV_{tm}}{\omega_0 V_R T} \qquad \begin{array}{l} 0 \le t \le T/2 \\[6pt] 0 \le \tau \le \omega_0 T/2 \end{array} \tag{120}$$

$$\frac{d^2 x}{d\tau^2} + 2h \frac{dx}{d\tau} + x = 1 + \frac{V_D}{V_R} + \frac{8hV_{tm}}{\omega_0 V_R T} \qquad \begin{array}{l} T/2 \le t \le T \\[6pt] \omega_0 T/2 \le \tau \le \omega_0 T \end{array} \tag{121}$$

It can be seen that t has been eliminated from the right-hand sides of these equations so that they are constants. The elimination of t has made the equations autonomous so that they can be plotted on the phase plane as is done in the next section.

Plotting in the Phase Plane $dx/d\tau$ Versus x

The first step in determining the phase plane trajectory is to determine the nature of (118) through (121) in the phase plane. Equations (118) and (119) are linear functions of $dx/d\tau$ and x. This means that the phase plane trajectory during t_{on} is made up of straight lines with slopes equal to $-1/\tau_C$ and $dx/d\tau$ intercepts equal to the right-hand sides of (118) and (119).

Equations (120) and (121) are second order differential equations in x whose solutions are damped sinusoidal waveforms

which are represented in the phase plane by spirals with focuses located on the x-axis at values of x equal to the right-hand sides of (120) and (121).

It is concluded that there are four segments of the phase-plane trajectory. During t_{on}, there are two linear segments which are portions of the lines defined by (118) and (119). During t_{off}, there are two segments of spirals defined by (120) and (121). The positions of the two linear segments defined by (118) and (119) are always fixed being defined by their slopes $1/\tau_C$ and their $dx/d\tau$ intercepts which do not change. The positions of the two spiral segments defined by (120) and (121) are not fixed and depend on the phenomena which occur at switching. By reason of the hysteresis, it is known that turn-on occurs when $\epsilon = \delta_1$ and turn-off occurs when $\epsilon = -\delta_2$. These values of ϵ normalized with respect to V_R are at turn-on

$$x = \lambda_1 \qquad (122)$$

and at turn-off

$$x = -\lambda_2 \qquad (123)$$

where

$$\lambda_1 = \delta_1/V_R \qquad (124)$$

$$\lambda_2 = \delta_2/V_R \qquad (125)$$

Since δ_1, δ_2, and V_R are constants, (122) and (123) are vertical lines in the phase plane perpendicular to the x-axis and, because of the nature of hysteresis, are confined to the first

and third quadrants of the phase plane. These lines are called switching lines; and whenever the phase plane trajectory crosses one, switching must occur. For $x = \lambda_1$ turn-on occurs; and for $x = -\lambda_2$, turn-off occurs.

A representation of the phase-plane trajectory is shown in Fig. 24, and Fig. 25 contains sketches of the normalized waveforms for $v_t(\tau)$, $v(\tau)$, $x(\tau)$, and $dx(\tau)/d\tau$ where $\tau_{on} = \omega_0 t_{on}$ and $\tau_{off} = \omega_0 t_{off}$. The $dx/d\tau$ intercepts for practical circuit parameters have much larger numerical values than the extremities of the x-axis excursions. The magnitude of the output ripple voltage component of $v(t)$ is normally much smaller than the peak voltage V_{tm} of the triangular waveform; therefore, the positive and negative x-axis extremities of the phase-plane trajectory should be approximately equal to the normalized peak-to-peak magnitude $2V_{tm}/V_R$ of $v_t(t)$. The values of δ_1 and δ_2 are usually much smaller than V_{tm}; therefore λ_1 and λ_2 for practical circuits are extremely close to the $dx/d\tau$ axis. These characteristics result in a phase-plane trajectory drawn to scale that is very tall and narrow. For example, the ratio of height to width for the case of the 2 kHz converter described in Appendix C is approximately 30 to one. For this reason, the $dx/d\tau$ axis in Fig. 24 is compressed and the values of λ_1 and λ_2 are shown to be larger than typical so that the behavior of the trajectory is clearly depicted.
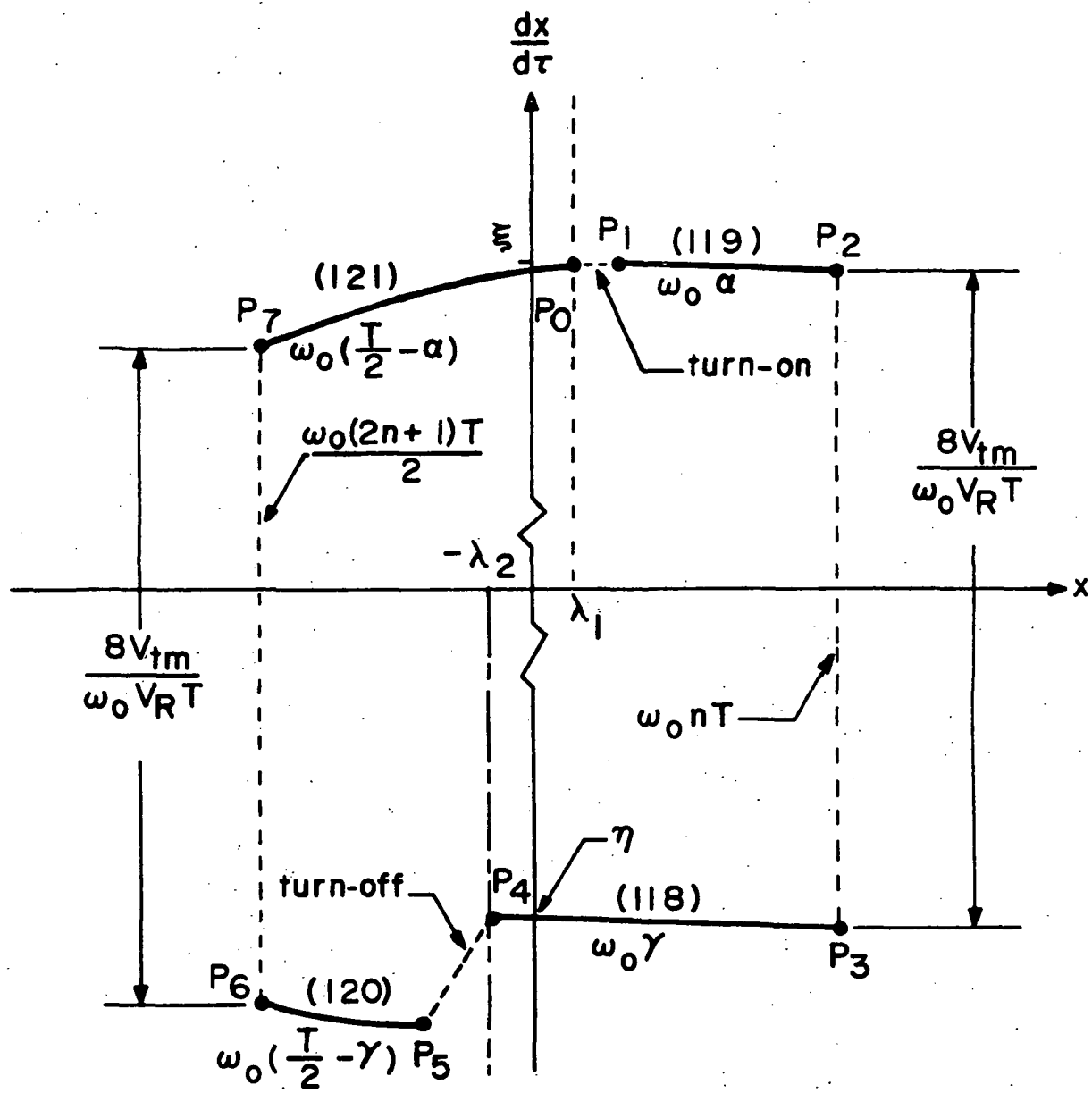
Fig. 24. The phase plane trajectory.
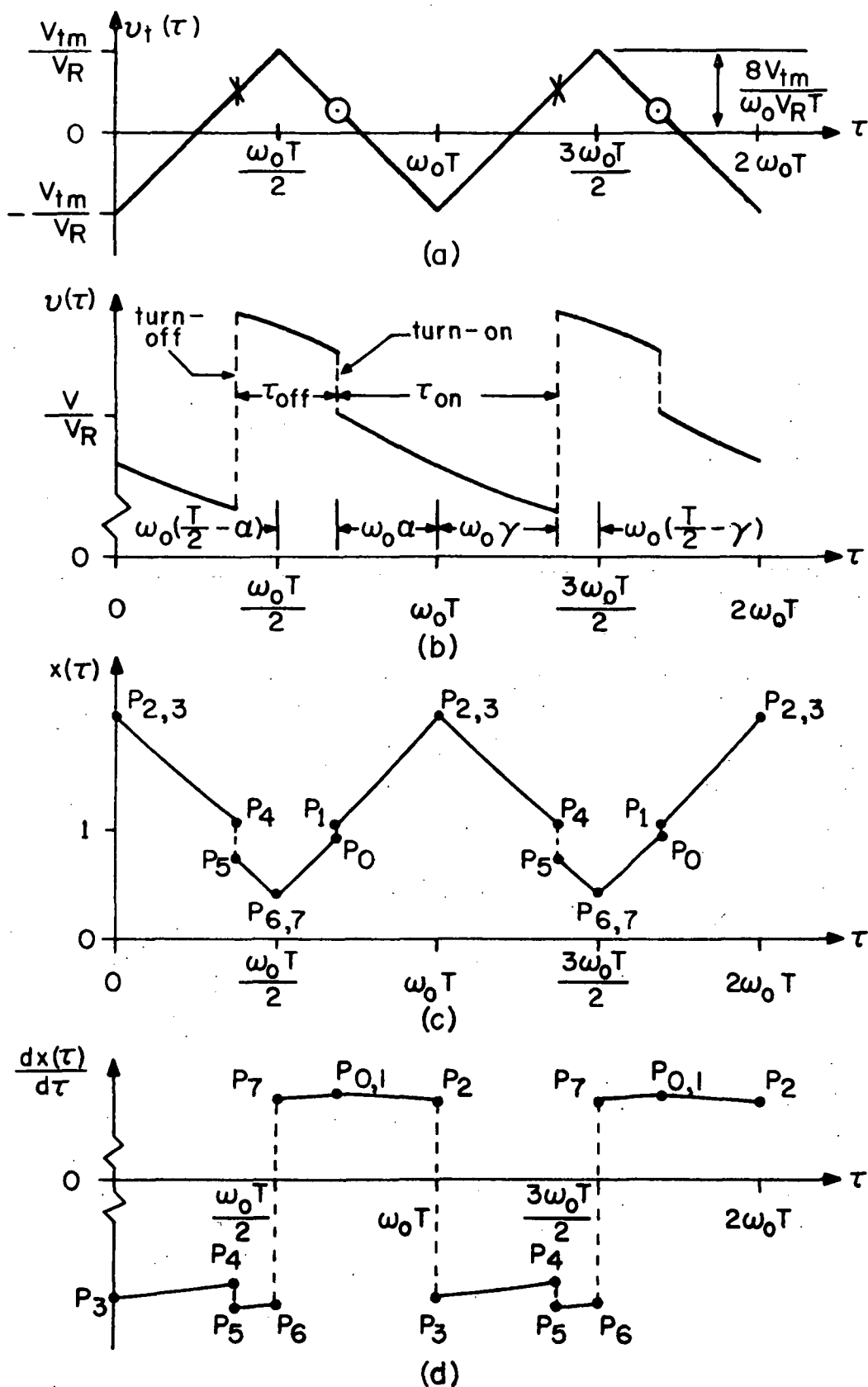
Fig. 25. Normalized waveforms for $v_t(\tau)$, $v(\tau)$, $x(\tau)$ and $dx(\tau)/d\tau$.

The solid-line portions of the trajectory are determined by (118) through (121). The dotted-line portions are used to indicate jumps in the coordinates at times when switching occurs [26]. The magnitudes of these jumps are derived in the next section. These jumps represent changes in conditions which occur during real switching and must be included in the phase-plane trajectory when instantaneous switching is assumed. The alternative to assuming instantaneous switching is to assume a linear, exponential, or another appropriate function for the variable during switching. However, these assumptions increase the complexity of the expressions which must be manipulated in this example to such an extent that instantaneous switching is the preferable assumption.

A brief explanation of the trajectory is given now by taking one segment at a time, beginning at point P_0 which is at the time immediately before turn-on. At the intersection P_0 of the λ_1 line, turn-on occurs and a jump in the direction indito P_1 occurs. The direction and magnitude of this jump are dependent on the circuit conditions just prior to turn-on and the value of R_C. During τ_{off}, i_S is greater than i_L since C is charging. During τ_{on}, i_S is zero and C is discharging by i_L. This means that at turn-on the change in current $\Delta\left(i_S - i_L\right)$ in R_C is negative so that a negative jump appears in the output voltage v. The magnitude of the jump is dependent on the value of R_C and the jump $\Delta\left(i_S - i_L\right)$. From (100) and (108), the corresponding jump in x at turn-on is positive as shown in Fig. 24 from P_0 to P_1.

The dependence of the jump in $dx/d\tau$ on circuit conditions, such as load and source voltage, is such that it cannot be easily described in a general qualitative manner. The segment of the trajectory from P_1 to P_2 is defined by (119) and occurs during the first portion of t_{on} called α. Points P_2 and P_3 occur at the time $\omega_0 nT$ where $n = 0,1,2,3,\ldots$ at which the slope of $v_t(\tau)$ changes instantaneously from a negative to a positive value. This instantaneous change in slope accounts for the negative jump in the $dx/d\tau$ direction while x remains constant. The segment from P_3 to P_4 is defined by (118) and occurs during the second part of τ_{on} called $\omega_0\gamma$. When the trajectory reaches the $-\lambda_2$ line at P_4, turn-off occurs. At turn-off, a jump to P_5 occurs in the direction indicated. At turn-off, the status of C changes from discharging to charging which is opposite to the change at turn-on. As a result, there is an instantaneous increase in $\left(i_S - i_L\right)$ through R_C which causes an instantaneous increase in v. Therefore from (100) and (108), the jump in x at turn-off is negative as shown in Fig. 24 from P_4 to P_5. As in the case of the jump at turn-on, the jump in $dx/d\tau$ at turn-off is dependent on circuit conditions and cannot easily be described in a general qualitative manner. The trajectory segment from P_5 to P_6 occurs during τ_{off} for the normalized time interval of $\omega_0(T/2-\gamma)$ and is defined by (120). Points P_6 and P_7 occur at $\omega_0(2n+1)T/2$ when the slope of $v_t(\tau)$ changes again this time from positive to negative so that there is a positive jump in $dx/d\tau$ while x remains constant. The trajectory segment

from P_7 to P_0 occurs during τ_{off} for the time interval of $\omega_0(T/2-\alpha)$ and is defined by (121). This completes the motion about the phase-plane trajectory for one complete limit cycle. The next section of this chapter applies the mathematical expressions for the segments to a point transformation, or sequence function, analysis of the limit cycle.

The Sequence Function Analysis of the Phase Plane Trajectory

This section describes the point transformation, or sequence function, analysis of the limit cycle trajectory in the phase plane given in Fig. 24. The analysis begins by giving the solutions to the differential equations for the various segments of the phase plane and by determining analytical expressions for the jumps at the switching points. These expressions are then used to derive the sequence function using a modified version of the method of point transformation in the phase plane.

A normal point transformation analysis begins with an assumed initial point such as $P_0(x_0, y_0)$ and transforms the coordinates of this point in sequence to each succeeding point around the limit cycle until the final point is reached. The expressions for the coordinates of the final point are then equated to x_0 and y_0, which must be the same point if a limit cycle exists, to determine the unknown parameters which in this case are the time intervals $\omega_0\alpha$ and $\omega_0\gamma$. The system being analyzed in this

chapter has certain properties which can be used to simplify the analysis. The nature of the switching which occurs between points P_2 and P_3 and points P_6 and P_7 requires that the x-coordinates of these points are equal, respectively, so that $x_2 = x_3$ and $x_6 = x_7$. In addition, the x and $dx/d\tau$ coordinates of points on the segments between points P_1 and P_2 and between points P_3 and P_4 are linearly related by (119) and (118) respectively; and $x_0 = \lambda_1$ at P_0 and $x_4 = -\lambda_2$ at P_4. The jumps from P_0 to P_1 and from P_4 to P_5 are derived in Appendix B from linear differential circuit equations. For these reasons, expressions for x_3 and x_6 in terms of $\omega_0\gamma$ are determined by point transformations from P_4; and expressions for x_2 and x_7 in terms of $\omega_0\alpha$ are determined by point transformations from P_0. The expressions for x_2 and x_3 are equated and the expressions for x_6 and x_7 are equated to obtain the sequence functions determining the limit cycle. This procedure simplifies the mathematical manipulations required to obtain the sequence functions. The simplification is important in the analysis of this system since the expressions are complex.

The solutions of the differential equations. The general solution for (118) is

$$x(\tau) = \left(x_3 + \tau_c\eta\right)e^{-\tau/\tau_c} - \tau_c\eta \tag{126}$$

$$y(\tau) = \left(-\eta - \frac{x_3}{\tau_c}\right)e^{-\tau/\tau_c} \tag{127}$$

and for (119) is

$$x(\tau) = \left(x_1 - \tau_C \xi\right) e^{-\tau/\tau_C} + \tau_C \xi \tag{128}$$

$$y(\tau) = \left(\xi - \frac{x_1}{\tau_C}\right) e^{-\tau/\tau_C} \tag{129}$$

where $y(\tau)$ is used to represent $dx/d\tau$, x_0 is the x-coordinate of P_0, x_3 is the x-coordinate of P_3,

$$-\eta = \frac{1}{\tau_C} - \frac{4V_{tm}}{\omega_0 V_R T} \tag{130}$$

and

$$\xi = \frac{1}{\tau_C} + \frac{4V_{tm}}{\omega_0 V_R T} \quad . \tag{131}$$

It can be seen that $-\eta$ and ξ are the $dx/d\tau$ axis intercepts of (118) and (119) respectively in the phase plane.

The general solution for (120) is

$$x(\tau) = e^{-h\tau}\left[\frac{y_s + h\left(x_s - \delta\right)}{k} \sin k\tau + \left(x_s - \delta\right)\cos k\tau\right] + \delta \tag{132}$$

$$y(\tau) = e^{-h\tau}\left[\frac{-hy_s - x_s + \delta}{k} \sin k\tau + y_s \cos k\tau\right] \tag{133}$$

where

$$\delta = 1 + \frac{V_D}{V_R} - \frac{8hV_{tm}}{\omega_0 V_R T} \tag{134}$$

and

$$k = (1 - h^2)^{1/2} \quad . \tag{135}$$

The general solution for (121) is

$$x(\tau) = e^{-h\tau}\left[\frac{y_7 + h\left(x_7 - \rho\right)}{k} \sin k\tau + \left(x_7 - \rho\right)\cos k\tau\right] + \rho \qquad (136)$$

$$y(\tau) = e^{-h\tau}\left[\frac{-hy_7 - x_7 + \rho}{k} \sin k\tau + y_7 \cos k\tau\right] \qquad (137)$$

where

$$\rho = 1 + \frac{V_D}{V_R} + \frac{8hV_{tm}}{\omega_0 V_R T} \qquad . \qquad (138)$$

Equations (120) and (121) are represented as spirals in the phase plane with focuses on the x axis at values equal to the right-hand sides of (120) and (121). It should be observed that the parameters δ and ρ are the x values of the focuses and that these focuses are located symmetrically on either side of $1 + V_D/V_R$.

Determination of expressions for the jumps. The jumps which occur from P_2 to P_3 and P_6 to P_7 are a result of the instantaneous change in the slope of $v_t(t)$ at $t = nT$ and $t = (2n + 1)T/2$. The slope of $v_t(t)$ is

$$\frac{dv_t(t)}{dt} = \pm \frac{4V_{tm}}{T} \qquad (139)$$

which is positive when $nT < t < (2n + 1)T/2$ and negative when $(2n + 1)T/2 < t < nT$. The normalized slope is

$$\frac{dv_t(\tau)}{d\tau} = \pm \frac{4V_{tm}}{\omega_0 V_R T} \qquad (140)$$

which is positive when $\omega_0 nT < \tau < \omega_0 (2n + 1)T/2$ and negative when $\omega_0 (2n + 1)T/2 < t < \omega_0 nT$.

Solving (104) for ϵ and substituting into (108) yields

$$x = \frac{\epsilon}{V_R} = \frac{V_R - v_t(t) - v(t)}{V_R} \; . \tag{141}$$

Differentiating with respect to τ yields

$$\frac{dx}{d\tau} = -\frac{dv_t(\tau)}{d\tau} + \frac{dv(\tau)}{d\tau} \tag{142}$$

which is the ordinate coordinate in the phase plane and is a function of the normalized derivatives of the triangular wave-form $v_t(t)$ and the output voltage $v(t)$. Whenever the derivative of $v_t(\tau)$ switches instantaneously, the converter is between turn-on and turn-off, or vice versa. At these times, $v(\tau)$ is continuous and $dv(\tau)/d\tau$ cannot change instantaneously. Since $dv_t(\tau)/d\tau$ changes from positive to negative or vice versa at the instant of the jump, the magnitude of the jump in the phase plane is twice the magnitude of $dv_t(\tau)/d\tau$ which is $8V_{tm}/\omega_0 V_R$ as shown in Fig. 24. Since (142) has a negative sign on the right-hand side, the jump is negative from P_2 to P_3 at $\tau = \omega_0 nT$ and positive from P_6 to P_7 at $\tau = \omega_0(2n+1)T/2$ when $v_t(\tau)$ is as shown in Fig. 25(a). The jumps from P_2 to P_3 and P_6 to P_7 have been determined. Now the jumps from P_0 to P_1 at turn-on and from P_4 to P_5 at turn-off will be determined.

Fig. 26(a) shows $v_t(t)$ and the location of typical turn-on and turn-off points. Fig. 26(b) shows the approximate output voltage waveform $v(t)$ for the same time periods and at a scale

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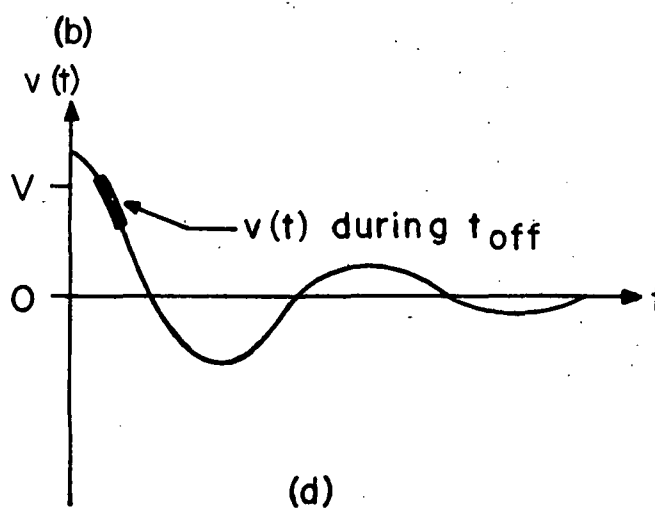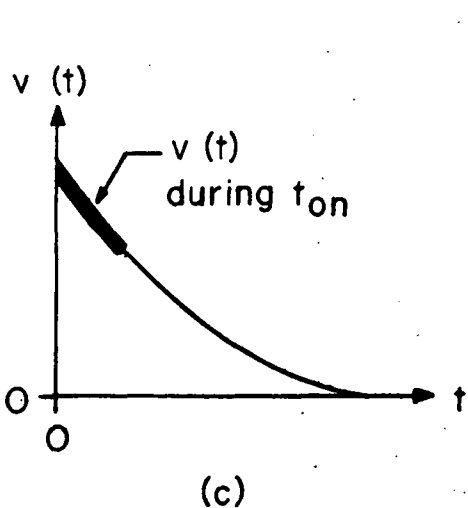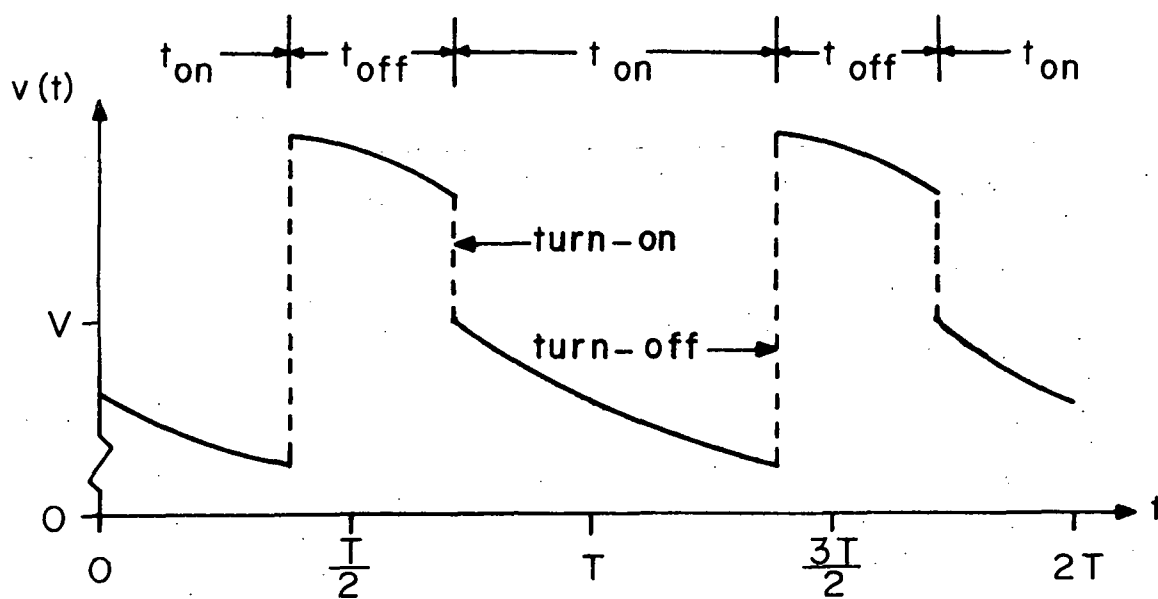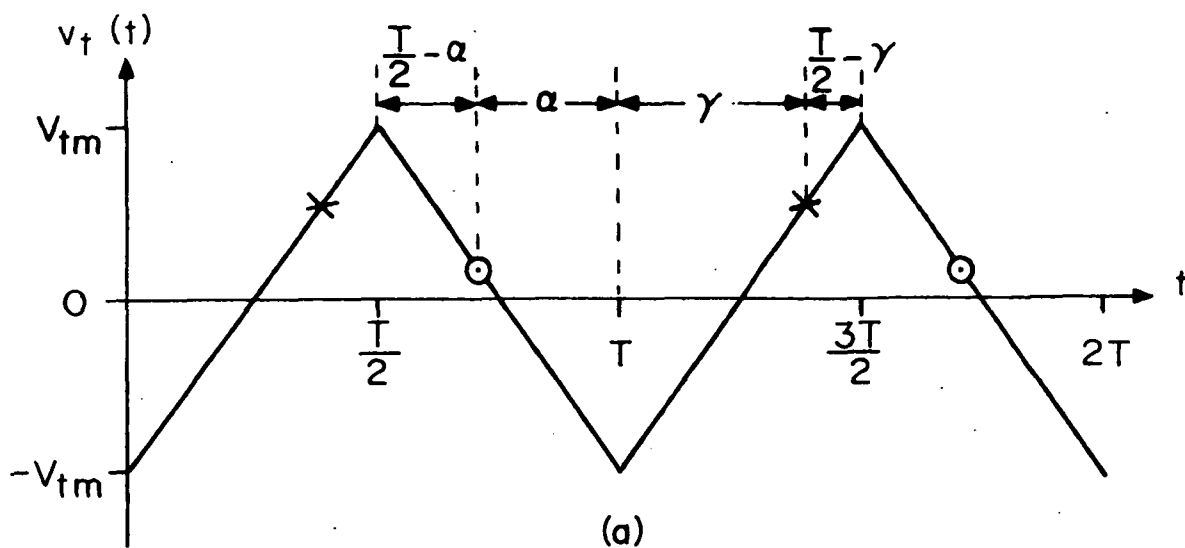
Fig. 26. Converter voltage waveforms (a) $v_t(t)$, (b) $v(t)$,
(c) $v(t)$ during t_{on}, (d) $v(t)$ during t_{off}.

five to six times greater than $v_t(t)$ in Fig. 26(a). Equation (103) yields a simple exponentially decaying voltage for $v(t)$ during t_{on}. This voltage is shown in Fig. 26(c) and the segment marked heavy is the portion of the whole that is typically $v(t)$ during t_{on} in Fig. 26(b). Equation (103) results in an exponentially damped sinusoidal general solution for $v(t)$ as shown in Fig. 26(d). The portion marked heavy is that part that is typically $v(t)$ during t_{off}. These segments of $v(t)$ during t_{on} and t_{off} are depicted by solid lines in Fig. 26(b). The jumps in $v(t)$ at switching, depicted by dotted lines, result as the current through R_C changes directions. The following analysis concerns the current $i_S - i_L$ through R_C and C shown in Fig. 22. During t_{on}, $i_S - i_L = -i_L < 0$; and during t_{off}, $i_S - i_L > 0$. Therefore at turn-on, $\Delta \left(i_S - i_L \right) < 0$; and the jump Δv is negative. Similarly at turn-off, $\Delta \left(i_S - i_L \right) > 0$; and the jump Δv at turn-off is positive. Since

$$x = \frac{e}{V_R} = \frac{V_R - v - v_t}{V_R} \qquad (143)$$

the jumps in v appear in x with opposite signs and reduced amplitude. These jumps can be seen in Fig. 24 where at turn-on from P_0 to P_1 the jump in x is positive and at turn-off from P_4 to P_5 the jump in x is negative. The directions of the jumps in $dx/d\tau$ can be explained qualitatively by examining Fig. 26(b). At turn-on, dv/dt changes very little as shown in Fig. 26(b); therefore, at turn-on in Fig. 24, the jump from P_0 to P_1 is

represented as being approximately zero in dx/dτ. The slope dv/dt is more negative at the end of t_{on} in Fig. 26(b) than it is at the beginning of t_{off}. This results in a positive jump in dv/dt and a negative jump in dx/dt as shown in Figs. 24 and 25(d). There is no reason, however, that under the right circuit conditions, the jump in dx/dτ at turn-off cannot be positive. The quantitative expressions for the jumps in x and dx/dτ at turn-on and turn-off are derived in Appendix B. At turn-on, from (B.55) and (B.35)

$$\Delta x_0 = \frac{-\Delta v_0}{V_R} = \left[1 - \frac{V_{tm}}{V_R}\left(\frac{4\gamma}{T} - 1\right) + \lambda_2\right] e^{\frac{-\alpha + \gamma}{(R+R_C)C}} - \left[1 - \frac{V_{tm}}{V_R}\left(\frac{4\alpha}{T} - 1\right) - \lambda_1\right]$$

(144)

and from (B.59) and (B.52)

$$\Delta y_0 = \left.\frac{dx}{d\tau}\right|_0 = -\frac{1}{\omega_0 V_R} \Delta \left.\frac{dv}{dt}\right|_0$$

$$= \frac{-1}{\omega_0 V_R}\left\{\frac{RR_C}{L_s(R+R_C)}\left(V_D + v_{0-}\right) + \left[\frac{1}{R_C C} - \frac{R_s}{L_s} - \frac{1}{(R+R_C)C}\right]\Delta v_0\right\}$$

(145)

where v_{0-} is given in (B.30). The quantitative expressions for the jumps at turn-off are from (B.56) and (B.51)

$$\Delta x_f = -\Delta v_f/V_R = -\frac{\Delta v_0}{V_R} e^{\frac{-R_p t_{on}}{L_s}} + \frac{RR_C}{R+R_C}\frac{N_p}{N_s}\frac{E-V_{CE}}{V_R R_p}\left(1 - e^{\frac{-R_p t_{on}}{L_s}}\right)$$

(146)

where Δv_0 is given in (B.35), and from (B.60) and (B.53)

$$\Delta y_f = \Delta \left.\frac{dx}{d}\right|_f = \frac{-1}{\omega_0 V_R} \left.\Delta \frac{dv}{dt}\right|_f$$

$$= \frac{-1}{\omega_0 V_R} \left\{ \frac{-RR_C}{\left(R+R_C\right)L_s}\left(V_D + v_{f+}\right) + \left[\frac{R^2}{\left(R+R_C\right)^2 C} - \frac{RR_C R_s}{\left(R+R_C\right)L_s}\right]\left[\left(i_{S0} - \right.\right.\right.$$

$$\left.\left.\left. - \frac{N_p}{N_s}\frac{E-V_{CE}}{R_p}\right)e^{\frac{-R_p t_{on}}{L_p}} + \frac{N_p}{N_s}\frac{E-V_{CE}}{R_p}\right]\right\} \tag{147}$$

where $\Delta(dv/dt)|_f$ is given in (B.53), v_{f+} is given in (B.15), and i_{S0-} is given in (B.38). The four jumps in the normalized phase plane shown in Fig. 24 have now been defined. The final derivation of the sequence function expressions is given in the next section.

The sequence functions. This section utilizes the solutions of the differential equations and the expressions for the jumps given in the previous two sections to derive the sequence functions for the normalized phase plane in Fig. 24. From all the circuit parameters, there are two that are undetermined; α and γ. Two unknown circuit parameters require two independent relations to adequately define the behavior of the circuit. These independent relations are called the sequence functions because they are normally derived by transforming in sequence the coordinates of the points of the phase-plane trajectory such as shown in Fig. 24. The transformations begin at an assumed initial point and continue to the final point of one cycle of operation for the circuit. If it is assumed that the circuit has

reached steady-state conditions, the final point should be the same as the initial point; therefore the expressions for the co-ordinates of these two points can be equated to obtain two sequence functions defining the nature of the circuit.

The nature of the phase plane in Fig. 24 allows for the sequence functions to be determined in a simpler manner. The x-coordinates of points P_0 and P_4 are always fixed at λ_1 and λ_2, respectively. In addition, the x-coordinates of P_2 and P_3 and the x-coordinates of P_6 and P_7 must be equal due to the assumed instantaneous switching as explained previously. For these reasons, P_2 and P_7 can be expressed in terms of $\omega_0 \alpha$ and the coordinates of P_0; and P_3 and P_4 can be expressed in terms of $\omega_0 \gamma$ and the coordinates of P_4. The sequence functions can then be found by equating x_2 and x_3 and by equating x_6 and x_7. This procedure is performed in the remainder of this section.

The first step in finding the first sequence function is to find x_2 starting with

$$x_0 = \lambda_1 . \tag{148}$$

The transformation from P_0 to P_1 yields

$$x_1 = x_0 + \Delta x_0 = \lambda_1 + \Delta x_0 \tag{149}$$

where Δx_0 is the jump in x at turn-on given by (144). During the normalized time period $\omega_0 \alpha$, x is governed by (119) whose solution is (128). Substituting $\tau = \omega_0 \alpha$ and x_1 from (149) into (128) yields

$$x_2 = \left(\lambda_1 + \Delta x_0 - \tau_C \xi\right) e^{-\frac{\omega_0 \alpha}{\tau_C}} + \tau_C \xi \quad . \tag{150}$$

The next step is to find an expression for x_3. The expression for x during the normalized time period $\omega_0 \gamma$ from P_3 to P_4 is given in (126). Substituting $\tau = \omega_0 \gamma$ and $x_4 = -\lambda_2$ into (126) and solving for x_3 yields

$$x_3 = \left(\tau_C \eta - \lambda_2\right) e^{\frac{\omega_0 \gamma}{\tau_C}} - \tau_C \eta \quad . \tag{151}$$

Since the x-coordinate does not change from P_2 to P_3 the first sequence function can be obtained by equating x_2 and x_3 from (150) and (151), respectively, yielding

$$\left(\tau_C \eta - \lambda_2\right) e^{\frac{\omega_0 \gamma}{\tau_C}} = \left(\lambda_1 + \Delta x_0 - \tau_C \xi\right) e^{\frac{-\omega_0 \alpha}{\tau_C}} + \tau_C (\xi + \eta) \quad . \tag{152}$$

The first step in finding the second sequence function is to find x_6. To do this the coordinates of P_4 must be transformed to P_6. The coordinates of P_4 in Fig. 24 are

$$x_4 = -\lambda_2 \tag{153}$$

$$y_4 = \frac{\lambda_2}{\tau_C} - \eta \tag{154}$$

where (154) is derived by substituting x_4 from (153) and $-\eta$ from (130) into (118) and solving for $dx_4/d\tau = y_4$. The jump from P_4 to P_5 at turn-off is defined by (B.56) and (B.60) in

the x and y-coordinate directions, respectively. Therefore, the coordinates of P_5 are

$$x_5 = x_4 + \Delta x_f = -\lambda_2 + \Delta x_f \qquad (155)$$

$$y_5 = y_4 + \Delta y_f = \frac{\lambda_2}{\tau_c} - \eta + \Delta y_f \quad . \qquad (156)$$

During the time period from P_5 to P_6, the x and y-coordinates of the phase plane are governed by differential equation (120). The solution to (120) is given in (132) and (133). Substituting x_5 from (155), y_5 from (156), and $\tau = \omega_0(T/2 - \gamma) = \beta$ into (132) yields

$$x_6 = e^{-h\beta}\left[\frac{\frac{\lambda_2}{\tau_c} - \eta + \Delta y_f + h\left(-\lambda_2 + \Delta x_f - \delta\right)}{k} \sin k\beta \right.$$
$$\left. + \left(-\lambda_2 + \Delta x_f - \delta\right)\cos k\beta\right] + \delta \quad . \qquad (157)$$

Now an expression for x_7 must be found. The differential equation defining the phase-plane trajectory from P_7 to P_0 during $\omega_0(T/2 - \alpha)$ is (121). The solution to (121) is given in (136) and (137). Substituting $\tau = \omega_0(T/2 - \alpha) = \theta$ yields

$$x_0 = e^{-h\theta}\left[\frac{y_7 + h\left(x_7 - \rho\right)}{k} \sin k\theta + \left(x_7 - \rho\right)\cos k\theta\right] + \rho \qquad (158)$$

$$y_0 = e^{-h\theta}\left(\frac{-hy_7 - x_7 + \rho}{k} \sin k\theta + y_7 \cos k\theta\right) \quad . \qquad (159)$$

Substituting

$$Y_0 = Y_1 - \Delta y_0 = \xi - \frac{\lambda_1 + \Delta x_0}{\tau_C} - \Delta y_0 \tag{160}$$

into (159) and solving for y_7. Then substituting y_7 and $x_0 = \lambda_1$ into (158) and solving for x_7 yields

$$x_7 = \left[\frac{\left(\xi - \dfrac{\lambda_1 + \Delta x_0}{\tau_C} - \Delta y_0 \right) + \left(h - \dfrac{k}{\tan k\theta} \right)\left(\lambda_1 - \rho \right)}{-k\left(\sin k\theta + \dfrac{\cos^2 k\theta}{\sin k\theta} \right)} \right] e^{h\theta} + \rho \; . \tag{161}$$

Equating x_6 in (157) and x_7 in (161) yields the second sequence function as

$$\left[\frac{\dfrac{\lambda_2}{\tau_C} - \eta + \Delta y_f + h\left(-\lambda_2 + \Delta x_f - \delta \right)}{k} \sin k\beta + \right.$$

$$\left. \left(-\lambda_2 + \Delta x_f - \delta \right) \cos k\beta \right] e^{-h\beta} + \delta =$$

$$\left[\frac{\left(\xi - \dfrac{\lambda_1 + \Delta x_0}{\tau_C} - \Delta y_0 \right) + \left(h - \dfrac{k}{\tan k\theta} \right)\left(\lambda_1 - \rho \right)}{-k\left(\sin k\theta + \dfrac{\cos^2 k\theta}{\sin k\theta} \right)} \right] e^{h\theta} + \rho \; . \tag{162}$$

Conclusion

The regulated switching converter analyzed in this chapter is of the type discussed in Chapter III. The converter uses

a triangular driving function to obtain regulation at a constant switching frequency. The first section of this chapter contains the development of the system model for the converter as shown in Fig. 22 and explains the means by which regulation is obtained. In the next section, the total period is divided into segments during which the system is linear; and normalized linear differential equations are derived to describe the circuit operation during each segment. In the derivation, it is necessary to assume that the amplitude V_{tm} of the triangular waveform is negligible compared to the reference voltage V_R and that the derivative of $v_y(t)$ is constant for half cycle periods. These equations are then used to plot the phase plane shown in Fig. 24 and to sketch the waveforms in Fig. 25 where switching is assumed to occur instantaneously creating jumps whenever power transistor Q switches or the derivative of $v_t(t)$ changes sign. In the final section, solutions are obtained for the phase plane equations and expressions for the jumps which are used to derive the sequence functions given in (152) and (162) which completely describe the steady-state conditions of the converter by defining the unknown time periods α and γ. Therefore, by assuming that $V_{tm} << V_R$ and that $dv_t(t)/dt = $ constant, equations describing the steady-state operation of a nonlinear system with a triangular driving function have been derived.

Since α and γ are defined, numerical values can be assigned to the circuit parameters; and they can be substituted into (152) and (162) to find α and γ. Since $t_{on} = \alpha + \gamma$ and T

is fixed and known, the duty cycle t_{on}/T can then be computed from the values of α and γ determined from the sequence functions.

Appendix C contains an experimental verification of the theoretical limit cycle computed using the equations of a converter operating at a frequency of 2 kHz. Photographs of experimental waveforms and an experimental limit cycle are given. The experimental limit cycle is normalized and plotted on the same set of axes with the theoretical limit cycle. These two limit cycles are shown to compare closely. Also, experimental circuit conditions are substituted into (152) and (162) and the accuracy of the sequence function is verified.

The sequence functions given in (152) and (162) are highly complex transcendental equations. Before this analysis can be practically expanded to be quantitative, the values of the circuit parameters must be known and approximations must be sought which simplify the complexity of the sequence functions so that they can be solved for α and γ. It is also possible, knowing values of the circuit parameters, to use a digital computer to calculate and plot characteristic curves involving α and γ. These analyses are suggested as extensions of the work presented in this chapter whose scope is to show that regulated dc to dc energy storage converters using triangular driving functions can be analyzed using piecewise linear analysis in the phase plane.

Chapter V

CONCLUSION

This dissertation presents techniques for improving spacecraft power conditioning systems and for meeting new requirements for these systems. All spacecraft equipment generally needs to have minimum size and weight, maximum efficiency, and maximum reliability. Research and development for spacecraft equipment must continually strive to improve these characteristics. In addition, space technology is advancing continuously. Each new spacecraft has more sophisticated equipment designed to perform more sophisticated experiments. This sophistication and advanced technology is transferred down to the most basic electronic system on the spacecraft. The one without which none of the other systems can function is the power conditioning system. Chapter I begins the dissertation by providing the background and scope of the research to be presented.

In order to achieve low output ripple voltage for dc to dc converters operating at typical switching frequencies of 2 to 50 kHz, the designer is required to use the large-microfarad electrolytic capacitors. Unfortunately these capacitors have large size and weight and are the least reliable component when

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compared to the other components used on spacecraft. Chapter II
discusses an active ripple filter designed to replace the pi-
network, L-section, and pure capacitance output filters for dc
to dc converters and to reduce the amount of capacitance re-
quired so that more reliable capacitors can be used. The filter
schematic diagram and the circuit design are given first. The
filter consists basically of a mutual inductor and an operational
amplifier. The mutual inductor secondary winding is in series
with the main power path and permits dc current to flow through
the filter with little or no dissipation. The operational am-
plifier is used to amplify the ripple voltage sensed at the input
to the filter. This signal is conditioned by the amplifier and
impressed on the primary so that the secondary voltage is identi-
cal in magnitude and phase to the ripple voltage at the input,
thus cancelling the ripple. The transfer function for this fil-
ter is derived next and is shown to be equivalent over the fre-
quency range of interest to the transfer function for an L-sec-
tion filter. The result of this research is an active ripple
filter with a nondissipative dc path which filters ripple volt-
ages from 2 to 50 kHz. The ripple filter requires a total of
only 4.87 μF which can be obtained using the more reliable cer-
amic and mica capacitors. The equivalent L-section filter using
the same inductance as the secondary inductance of the active
filter requires 408.5 μF to achieve the same attenuation charac-
teristic. Thus the active filter essentially eliminates the
need for the less reliable electrolytic filter capacitors by

requiring approximately 84 times less capacitance than an equiv-
alent L-section filter.

Chapter III discusses the design of a 1 MHz dc to dc
switching converter which was designed to provide 20 watts of
output power at a regulated output voltage of 28 volts operating
from a dc source voltage varying from 21 to 31 volts. Operation
at 1 MHz is desirable for several reasons. The high frequency
will result in a reduction in the size and weight of the trans-
formers, inductors, and capacitors. The amount of capacitance
required in the output filter is greatly reduced thereby permit-
ting the use of the more reliable mica and ceramic capacitors as
was done with the ripple filter in Chapter II. A more specific
reason is that experiments are planned for measuring electromag-
netic radiation in outer space in the frequency range from 0.2
to 100 kHz which require the design of the system to use switch-
ing frequencies of at least 1 MHz in order to avoid interference
between the switching in the power conditioning system and the
experiments. The first part of Chapter III gives the background
and reasons for choosing the energy-storage type of circuit with
electrical isolation. In addition, the choice of ferrite mag-
netic material and high-speed transistors, diodes, and inte-
grated circuits is discussed. Considerations to be used in de-
signing power switching circuits at high frequencies are then
given before the actual converter circuit design is discussed.
Experimental results in the form of the regulation and efficiency
characteristics and oscillograms of the switching waveforms are

given. The converter operates over the full range of source and load conditions with the regulation better than 1.5 percent of the mean output voltage and a maximum efficiency of 79 percent. The majority of the power dissipation was found to be in the power switching transistor and diode. The feasibility of such circuits to operate in the 1 MHz frequency range has been demonstrated by the circuit discussed in Chapter III. Before such a circuit can be considered for practical application, additional consideration needs to be given to providing a reliable means for self-starting and to providing a means to return the circuit to normal regulating operation if a disturbance large enough to cause the circuit to leave the normal operating range is encountered.

Regulated inverters and converters constitute a highly complex group of closed-loop nonlinear feedback control systems. For this reason, there has been only a small amount of analytical work on these circuits. The analysis performed in Chapter IV illustrates the complexity that the expressions can attain when analysis is attempted. Chapter IV contains an analysis of the type of circuit presented in Chapter III. Because operation at frequencies of 1 MHz require analytical work to consider stray parameters not considered in this analysis, the results of Chapter IV may not be directly applicable to the 1 MHz converter of Chapter III. For this reason, an experimental verification of the analysis is made using a converter designed to operate at a switching frequency of 2 kHz. Both circuits use a constant

frequency triangular waveform as a driving function to generate the duty cycle needed for regulation. The analysis uses the method of point transformations in the phase plane. The system differential equations contain time dependent functions resulting from the triangular waveform driving function which make these equations nonautonomous. However, approximations can be made which make the differential equations autonomous. These approximations are that the magnitude of the triangular waveform is much smaller than the value of the reference voltage and that the slope, or time derivative, of the triangular waveform is constant.

Having made these approximations, system equations are developed and normalized. These normalized differential equations are used to sketch the phase plane trajectory in the normalized phase plane. To minimize the complexity of the analysis, instantaneous switching is assumed for the power transistor at turn-on and turn-off. Additionally, it is assumed that the slope of the triangular waveform changes instantaneously. Since instantaneous switching is assumed for all of these cases, there are four jumps in the phase plane represented by dotted lines. Expressions for these jumps are derived and solutions for the differential equations describing the linear segments of the phase plane trajectory are obtained. The validity of these equations is verified experimentally by comparing experimental and theoretical limit cycles.

These equations are also used to make point transformations around an assumed limit cycle to obtain two equations called the sequence functions. The sequence functions define the relationship between the known circuit parameters and the two unknown time parameters of the total period of the full cycle which have to be known to define the limit cycle. The accuracy of the equations defining the sequence functions is verified experimentally using the circuit conditions of the 2 kHz converter. The sequence functions can be used to fully define the nature of the oscillations for a set of circuit parameters. Therefore, the original objective, to accomplish a nonlinear analysis of a regulated dc to dc closed-loop switching converter with isolation which utilizes a triangular waveform driving function, has been accomplished.

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Appendix A

DERIVATION OF EQUATIONS (102) AND (103)

Equation (102) for the time period t_{on}. Since $i_S = 0$ during t_{on}, the voltages summed around the i_L current loop in Fig. 22 yield

$$\frac{1}{C} \int i_L \; dt + \left(R + R_C\right) i_L = 0 \quad . \tag{A.1}$$

When differentiated with respect to t, (A.1) becomes

$$\frac{di_L}{dt} + \frac{1}{\left(R + R_C\right)C} \; i_L = 0 \quad . \tag{A.2}$$

(A.2) is multiplied by R and $Ri_L = v$ is substituted to obtain

$$\frac{dv}{dt} + \frac{1}{\left(R + R_C\right)C} \; v = 0 \tag{A.3}$$

which is the differential equation describing the variation of v during t_{on} and is identical to (102).

Equation (103) for the time period t_{off}. During t_{off}, $i_P = 0$ and I_S and I_L are nonzero. This means that there are two current loops with a common branch yielding two linear first order differential equations which can be combined to obtain one second order differential equation in i_L or $v = Ri_L$.

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The sum of the voltages around the i_S current loop in Fig. 22 during t_{off} can be written as

$$L_S \frac{di_S}{dt} + R_S i_S + V_D + v = 0 \quad . \tag{A.4}$$

Dividing (A.4) by L_S yields the first differential equation

$$\frac{di_S}{dt} + \frac{R_S}{L_S} i_S = \frac{-v-V_D}{L_S} \quad . \tag{A.5}$$

The sum of the voltages around the i_L current loop in Fig. 22 is

$$\frac{1}{C} \int \left(i_L - i_S \right) dt + R_C \left(i_L - i_S \right) + Ri_L = 0 \quad . \tag{A.6}$$

Differentiating (A.6) and letting $Ri_L = v$ yields the second differential equation

$$\frac{di_S}{dt} + \frac{1}{R_C C} i_S = \frac{R + R_C}{RR_C} \frac{dv}{dt} + \frac{1}{RR_C C} v \quad . \tag{A.7}$$

Equation (A.7) is solved for i_S to obtain

$$i_S = \frac{\left(R + R_C \right) C}{R} \frac{dv}{dt} + \frac{1}{R} v - R_C C \frac{di_S}{dt} \quad . \tag{A.8}$$

Equation (A.5) is solved for di_S/dt to obtain

$$\frac{di_S}{dt} = - \frac{1}{L_S} \left[R_S i_S + V_D + v \right] \quad . \tag{A.9}$$

Equation (A.9) is substituted in (A.8) which is then solved for i_S to obtain

$$i_S = \frac{1}{\frac{1}{C} - \frac{R_C R_s}{L_s}} \left[\frac{R + R_C}{R} \frac{dv}{dt} + \left(\frac{1}{RC} + \frac{R_C}{L_s} \right) v + \frac{R_C}{L_s} V_D \right] \quad . \quad \text{(A.10)}$$

Equation (A.10) is differentiated to obtain

$$\frac{di_S}{dt} = \frac{1}{\frac{1}{C} - \frac{R_C R_s}{L_s}} \left[\frac{R + R_C}{R} \frac{d^2 v}{dt^2} + \left(\frac{1}{RC} + \frac{R_C}{L_s} \right) \frac{dv}{dt} \right] \quad . \quad \text{(A.11)}$$

Equations (A.10) and (A.11) are now substituted into (A.5) to obtain

$$\frac{d^2 v}{dt^2} + \left[\frac{1}{\left(R + R_C\right)C} + \frac{R R_C}{\left(R + R_C\right)L_s} + \frac{R_s}{L_s} \right] \frac{dv}{dt} + \left[\frac{R + R_s}{\left(R + R_C\right)L_s C} \right] v$$

$$= \frac{-R}{\left(R + R_C\right)L_s C} V_D \quad . \quad \text{(A.12)}$$

Equation (A.12) can be simplified by assuming that $R_C \ll R$ and $R_s \ll R$ to obtain

$$\frac{d^2 v}{dt^2} + \left(\frac{1}{RC} + \frac{R_C + R_s}{L_s} \right) \frac{dv}{dt} + \frac{1}{L_s C} v = \frac{-V_D}{L_s C} \quad \text{(A.13)}$$

which is the linear second order differential equation describing v during t_{off} and is identical to (103).

Appendix B

DERIVATION OF THE EXPRESSIONS FOR THE JUMPS

AT TURN-ON AND TURN-OFF IN FIG. 24

Using unnormalized variables the error voltage is

$$\epsilon(t) = V_R - v_t(t) - v(t) \quad . \tag{B.1}$$

Since switching at turn-on and turn-off occurs instantaneously, $v_t(t)$ is constant during switching and

$$\Delta\epsilon = -\Delta v \quad . \tag{B.2}$$

Differentiating (B.1) yields

$$\frac{d\epsilon(t)}{dt} = -\frac{dv_t(t)}{dt} - \frac{dv(t)}{dt} \quad . \tag{B.3}$$

Since $dv_t(t)/dt$ is constant during switching

$$\Delta\frac{d\epsilon}{dt} = -\Delta\frac{dv}{dt} \quad . \tag{B.4}$$

For these reasons, this appendix derives the end points of the jumps in terms of $v(t)$ and $dv(t)/dt$.

Turn-off. During $t_{on} = \alpha + \gamma$, diode D is reverse-biased and the secondary circuit of Fig. 22 is equivalent to Fib. B.1(a).

(162)
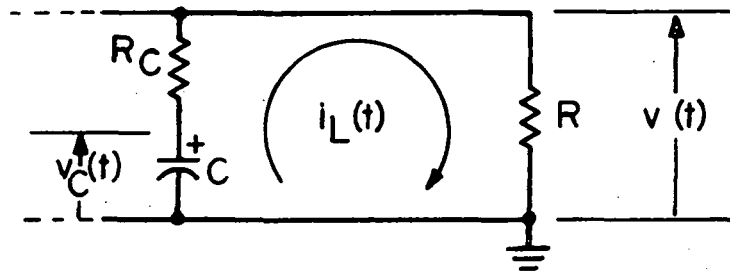
(a)
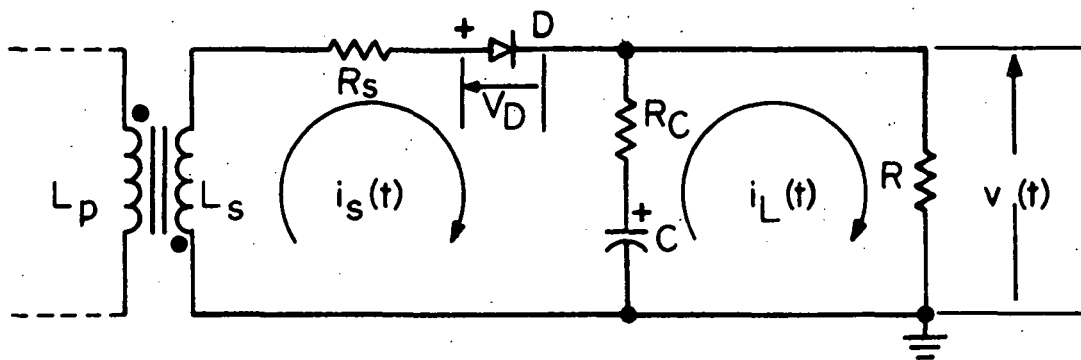
(b)

Fig. B.1.   The secondary circuits of Fig. 22 during
(a) t_{on} and (b) t_{off}.

The output voltage v is defined by

$$v(t) = V_R - v_t(t) - \epsilon(t) \quad . \tag{B.5}$$

At a time immediately prior to turn-off, at P_4

$$\epsilon(\gamma) = -\delta_2 \tag{B.6}$$

$$v_t(\gamma) = V_{tm}\left(\frac{4\gamma}{T} - 1\right) \quad . \tag{B.7}$$

Using the subscript f- to denote the conditions at P_4 in Fig. 24, v(t) at P_4 is derived from (B.5) substituting (B.6) and (B.7) as

$$v_{f-} = V_R - V_{tm}\left(\frac{4\gamma}{T} - 1\right) + \delta_2 \quad . \tag{B.8}$$

The differential equation for v(t) in Fig. B.1(a) during t_{on} is derived as

$$\frac{dv(t)}{dt} + \frac{1}{\left(R + R_C\right)C} v(t) = 0 \quad . \tag{B.9}$$

Substituting v_{f-} from (B.8) for v(t) in (B.9) yields

$$\left.\frac{dv}{dt}\right|_{f-} = -\frac{1}{\left(R + R_C\right)C}\left[V_R - V_{tm}\left(\frac{4\gamma}{T} - 1\right) + \delta_2\right] \quad . \tag{B.10}$$

During $t_{off} = T - \alpha - \gamma$, diode D is forward-biased and the secondary circuit of Fig. 22 is equivalent to Fig. B.1(b).

The instantaneous addition of i_S, which normally is greater than i_L, at turn-off causes a positive jump as a result of the instantaneous change Δi_S in the current through R_C. Using

the subscript f+ to denote conditions at P_5, i_L at P_5 is

$$i_{Lf+} = v_{f+}/R \quad .$$
(B.11)

Also, $v(t)$ during t_{off} is

$$v(t) = R_C\left[i_S(t) - i_L(t)\right] + v_C(t) \quad .$$
(B.12)

Therefore v_{f+} just after turn-off can be expressed as

$$v_{f+} = R_C\left(i_{Sf+} - i_{Lf+}\right) + v_{Cf} \quad .$$
(B.13)

Where v_{Cf} is the capacitor voltage during turn-off. Since switching is instantaneous v_{Cf} is constant from P_4 to P_5 and is expressed by

$$v_{Cf} = \frac{R + R_C}{R} v_{f-} = \frac{R + R_C}{R}\left[V_R - V_{tm}\left(\frac{4\gamma}{T} - 1\right) + \delta_2\right] \quad .$$
(B.14)

Substituting (B.11) and (B.14) into (B.13) yields

$$v_{f+} = \frac{R}{\left(R + R_C\right)}\left(R_C\ i_{sf+} + v_{Cf}\right) = \frac{RR_C}{R + R_C}\ i_{sf+} + v_{f-} \quad .$$
(B.15)

Taking the derivative of (B.12) evaluated just after turn-off yields

$$\left.\frac{dv}{dt}\right|_{f+} = R_C\left(\left.\frac{di_S}{dt}\right|_{f+} - \left.\frac{di_L}{dt}\right|_{f+}\right) + \left.\frac{dv_C}{dt}\right|_{f+} \quad .$$
(B.16)

During t_{off}, $v_C(t)$ is expressed by

$$v_C(t) = \frac{1}{C}\int\left[i_S(t) - i_L(t)\right]dt + \frac{Q_0}{C}$$
(B.17)

where Q_0 is the charge on C at the beginning of t_{off}. Substituting $i_L(t) = v(t)/R$ in (B.17) and taking the derivative of (B.17) evaluated just after turn-off yields

$$\left.\frac{dv_C}{dt}\right|_{f+} = \frac{1}{C}\left(i_{Sf+} - \frac{1}{R}v_{f+}\right) \quad . \qquad (B.18)$$

Substituting v_{f+} in (B.15) for v_{f+} in (B.18) yields

$$\left.\frac{dv_C}{dt}\right|_{f+} = \frac{1}{C}\left(\frac{R}{R+R_C}i_{Sf+} - \frac{v_{f-}}{R}\right) \quad . \qquad (B.19)$$

Taking the derivative of $i_L(t) = v(t)/R$ evaluated just after turn-off yields

$$\left.\frac{di_L}{dt}\right|_{f+} = \frac{1}{R}\left.\frac{dv}{dt}\right|_{f+} \quad . \qquad (B.20)$$

Substituting (B.19) and (B.20) into (B.16) and rearranging yields

$$\left.\frac{dv}{dt}\right|_{f+} = \frac{RR_C}{R+R_C}\left.\frac{di_S}{dt}\right|_{f+} + \frac{R^2\,i_{Sf+}}{\left(R+R_C\right)^2 C} - \frac{v_{f-}}{\left(R+R_C\right)C} \quad . \qquad (B.21)$$

The jump in $v(t)$ at turn-off is

$$\Delta v_f = v_{f+} - v_{f-} = \frac{RR_C}{R+R_C}i_{Sf+} \qquad (B.22)$$

where v_{f+} and v_{f-} are defined by (B.15) and (B.8), respectively.

The jump in $dv(t)/dt$ at turn-off is

$$\Delta\left.\frac{dv}{dt}\right|_f = \left.\frac{dv}{dt}\right|_{f+} - \left.\frac{dv}{dt}\right|_{f-} = \frac{RR_C}{R+R_C}\left.\frac{di_S}{dt}\right|_{f+} + \frac{R^2\,i_{Sf}}{\left(R+R_C\right)^2 C} \quad . \qquad (B.23)$$

The jumps in (B.22) and (B.23) are expressed in terms of the circuit parameters and i_{Sf+} and $\left(di_S/dt\right)\big|_{f+}$.

Turn-on. The secondary circuit acts as a simple RC circuit discharging C during t_{on}. So that the voltage v_{Cf} on C at turn-off can be related to the voltage v_{C0} on C at turn-on by

$$v_{Cf} = v_{C0}\; e^{-\dfrac{\alpha + \gamma}{\left(R + R_C\right)C}} \; . \tag{B.24}$$

Solving for v_{C0} and substituting v_{Cf} from (B.14) into (B.24) yields

$$v_{C0} = v_{Cf}\; e^{\dfrac{\alpha + \gamma}{\left(R + R_C\right)C}} = \frac{R + R_C}{R}\left[V_R - V_{tm}\left(\frac{4\gamma}{T} - 1\right) + \delta_2\right] e^{\dfrac{\alpha + \gamma}{\left(R + R_C\right)C}} \; . \tag{B.25}$$

The voltage on C is constant during turn-off and turn-on and is defined by (B.14) and (B.25) respectively.

Just after turn-on, before C begins to discharge, the output voltage v_{0+} can be obtained from voltage division as

$$v_{0+} = \frac{R}{R + R_C}\, v_{C0} = \left[V_R - V_{tm}\left(\frac{4\gamma}{T} - 1\right) + \delta_2\right] e^{\dfrac{\alpha + \gamma}{\left(R + R_C\right)C}} \tag{B.26}$$

where v_{C0} in (B.25) has been substituted into (B.26). Solving (B.9), the differential equation for $v(t)$ during t_{on}, for $dv(t)/dt$ and evaluating $dv(t)/dt$ just after turn-on yields

$$\left.\frac{dv}{dt}\right|_{0+} = -\frac{1}{\left(R+R_C\right)C}\, v_{0+} = -\frac{1}{\left(R+R_C\right)C}\left[V_R - V_{tm}\left(\frac{4\gamma}{T}-1\right)+\delta_2\right]e^{\frac{\alpha+\gamma}{(R+R_C)C}}$$

(B.27)

The conditions of $v(t)$ just after turn-on have been determined in (B.26) and (B.27). The conditions of $v(t)$ just prior to turn-on will now be derived.

The output voltage just prior to turn-on can be found by substituting $v_t(t)$ and $\epsilon(t)$ at the end of t_{off} into (B.5). At the end of t_{off}, $t = T - \alpha$ so that

$$v_t(T-\alpha) = V_{tm}\left(\frac{4\alpha}{T}-1\right)$$

(B.28)

and from Fig. 23

$$\epsilon(T-\alpha) = \delta_1 \quad .$$

(B.29)

Substituting (B.28) and (B.29) into (B.5) yields

$$v_{0-} = V_R - V_{tm}\left(\frac{4\alpha}{T}-1\right) - \delta_1 \quad .$$

(B.30)

To compute $dv(t)/dt$ evaluated just prior to turn-on, the derivative of (B.12) evaluated just prior to turn-on at P_0 is computed as

$$\left.\frac{dv}{dt}\right|_{0-} = R_C\left(\left.\frac{di_S}{dt}\right|_{0-} - \left.\frac{di_L}{dt}\right|_{0-}\right) + \left.\frac{dv_C}{dt}\right|_{0-} \quad .$$

(B.31)

The derivative of $v_C(t)$ given by (B.17) during t_{off} evaluated just prior to turn-on is

$$\left.\frac{dv_C}{dt}\right|_{0-} = \frac{1}{C}\left(i_{S0-} - \frac{v_{0-}}{R}\right) \ . \tag{B.32}$$

Taking the derivative of $i_L(t) = v(t)/R$ evaluated just prior to turn-on yields

$$\left.\frac{di_L}{dt}\right|_{0-} = \frac{1}{R}\left.\frac{dv}{dt}\right|_{0-} \ . \tag{B.33}$$

Substituting (B.32) and (B.33) into (B.31) yields

$$\left.\frac{dv}{dt}\right|_{0-} = \frac{RR_C}{R+R_C}\left.\frac{di_S}{dt}\right|_{0-} + \frac{R}{\left(R+R_C\right)C}\left(i_{S0-} - \frac{v_{0-}}{R}\right) \ . \tag{B.34}$$

The jump in $v(t)$ at turn-on is

$$\Delta v_0 = v_{0+} - v_{0-} = \left[V_R - V_{tm}\left(\frac{4\gamma}{T} - 1\right) + \delta_2\right]e^{\frac{\alpha+\gamma}{\left(R+R_C\right)C}} -$$

$$\left[V_R - V_{tm}\left(\frac{4\alpha}{T} - 1\right) - \delta_1\right] \ . \tag{B.35}$$

The jump in $dv(t)/dt$ at turn-on is

$$\Delta\left.\frac{dv}{dt}\right|_0 = \left.\frac{dv}{dt}\right|_{0+} - \left.\frac{dv}{dt}\right|_{0-}$$

$$= -\frac{v_{0+}}{\left(R+R_C\right)C} - \frac{RR_C}{R+R_C}\left.\frac{di_S}{dt}\right|_{0-} - \frac{Ri_{S0-} - v_{0-}}{\left(R+R_C\right)C}$$

$$= -\frac{RR_C}{R+R_C}\left.\frac{di_S}{dt}\right|_{0-} - \frac{Ri_{S0-} + \Delta v_0}{\left(R+R_C\right)C} \ . \tag{B.36}$$

The jump from P_4 to P_5 at turn-off has been derived and is defined by (B.22) and (B.23) and the jump from P_0 to P_1 is

defined by (B.35) and (B.36). Four unknown parameters remain to be defined. These are the conditions of $i_S(t)$ just after turn-off, i_{Sf+} and $\left(di_S/dt\right)\big|_{f+}$, and just prior to turn-on, i_{S0-} and $\left(di_S/dt\right)\big|_{0-}$. Expressions for these conditions are derived in the next section.

Conditions of $i_S(t)$. Since transistor Q in the primary circuit is blocking for both sets of conditions of $i_S(t)$, the primary current $i_p(t)$ is zero. Since $i_p(t) = 0$, the flux ϕ in the mutual inductor and the secondary current are linearly re-lated. Also, since switching is instantaneous, ϕ must be con-stant during switching and is equal to the value of ϕ just prior to switching and just after switching.

Solving (B.12) for $i_S(t)$ and evaluating $i_S(t)$ just prior to turn-on yields

$$i_{S0-} = \frac{v_{0-} - v_{C0}}{R_C} + i_{L0-} \quad . \tag{B.37}$$

Substituting $i_{L0-} = v_{0-}/R$ into (B.37), yields

$$i_{S0-} = \frac{R + R_C}{RR_C} v_{0-} - \frac{v_{C0}}{R_C} \tag{B.38}$$

where v_{0-} is defined in (B.30) and v_{C0} is defined in (B.25).

The solution of the differential equation for the pri-mary current i_p during t_{on} as shown in Fig. 22 is

$$i_p(t) = \left(i_{P0+} - \frac{E-V_{CE}}{R_p}\right)e^{-\frac{R_p t}{L_p}} + \frac{E-V_{CE}}{R_p} \quad . \qquad (B.39)$$

The elapsed time from turn-on to turn-off is $t_{on} = \alpha + \gamma$ which when substituted into (B.39) for t yields

$$i_{Pf-} = \left(i_{P0+} - \frac{E-V_{CE}}{R_p}\right)e^{-\frac{R_p t_{on}}{L_p}} + \frac{E-V_{CE}}{R_p} \quad . \qquad (B.40)$$

Since the flux level ϕ does not change during instantaneous switching,

$$i_{P0+} = \frac{N_s}{N_p} i_{S0-} \qquad (B.41)$$

and

$$i_{Sf+} = \frac{N_p}{N_s} i_{Pf-} \quad . \qquad (B.42)$$

Substituting (B.41) into (B.40) and (B.40) into (B.42) yields

$$i_{Sf+} = \left(i_{S0-} - \frac{N_p}{N_s}\frac{E-V_{CE}}{R_p}\right)e^{-\frac{R_p t_{on}}{L_p}} + \frac{N_p}{N_s}\frac{E-V_{CE}}{R_p} \qquad (B.43)$$

where i_{S0-} is given in (B.38).

The differential equation around the secondary current loop for $i_S(t)$ is

$$L_s \frac{di_s(t)}{dt} + R_s i_S(t) + V_D + v = 0 \quad . \qquad (B.44)$$

Solving (B.44) for di_S/dt and evaluating just prior to turn-on yields

$$\frac{di_S}{dt}\bigg|_{0-} = \frac{-1}{L_S}\left(v_{0-} + V_D + R_S\, i_{S0-}\right) \quad . \tag{B.45}$$

Substituting i_{S0-} in (B.38) into (B.45) yields

$$\frac{di_S}{dt}\bigg|_{0-} = \frac{-1}{L_S}\left\{\left[1 + \frac{R_S\left(R + R_C\right)}{RR_C}\right]v_{0-} - \frac{R_S}{R_C}\,v_{C_0} + V_D\right\} \tag{B.46}$$

where v_{0-} is given in (B.30) and v_{C_0} is given in (B.25).

Solving (B.44) for $di_S(t)/dt$ and evaluating just after turn-off yields

$$\frac{di_S}{dt}\bigg|_{f+} = \frac{-1}{L_S}\left(R_S\, i_{Sf+} - V_D + v_{f+}\right) \tag{B.47}$$

where i_{Sf+} is defined by (B.43) and v_{f+} by (B.15).

The jumps. The jump in $v(t)$ at turn-on is given explicitly by (B.35) as

$$\Delta v_0 = \left[V_R - V_{tm}\left(\frac{4\gamma}{T} - 1\right) + \delta_2\right]e^{\frac{\alpha + \gamma}{(R + R_C)C}} - \left[V_R - V_{tm}\left(\frac{4\alpha}{T} - 1\right) - \delta_1\right]$$
$$\tag{B.35}$$

The jump in $v(t)$ at turn-off is obtained by substituting (B.43) into (B.22) to yield

$$\Delta v_f = \frac{RR_C}{R + R_C}\left[\left(i_{S0-} - \frac{N_p}{N_s}\frac{E - V_{CE}}{R_p}\right)e^{-\frac{R_p t_{on}}{L_p}} + \frac{N_p}{N_s}\frac{E - V_{CE}}{R_p}\right] \quad . \tag{B.48}$$

Substituting (B.38) into (B.48) yields

$$\Delta v_f = \frac{RR_C}{R+R_C}\left[\left(\frac{R+R_C}{RR_C}v_0- - \frac{v_{C0}}{R_C} - \frac{N_p}{N_s}\frac{E-V_{CE}}{R_p}\right)e^{-\frac{R_p t_{on}}{L_s}} + \frac{N_p}{N_s}\frac{E-V_{CE}}{R_p}\right].$$
(B.49)

Rearranging (B.49) gives

$$\Delta v_f = \left(v_{0-} - \frac{Rv_{C0}}{R+R_C}\right)e^{-\frac{R_p t_{on}}{L_s}} + \frac{RR_C}{R+R_C}\frac{N_p}{N_s}\frac{E-V_{CE}}{R_p}\left(1 - e^{-\frac{R_p t_{on}}{L_s}}\right).$$
(B.50)

where v_{0-} is given by (B.30) and v_{C0} is given by (B.25). If substitution is made for v_{0-} and V_{C0} in (B.50), Δv_f can be expressed as

pressed as

$$\Delta v_f = -\Delta v_0 e^{-\frac{R_p t_{on}}{L_s}} + \frac{RR_C}{R+R_C}\frac{N_p}{N_s}\frac{E-V_{CE}}{R_p}\left(1 - e^{-\frac{R_p t_{on}}{L_s}}\right).$$
(B.51)

where Δv_0 is given in (B.35).

The jump in $dv(t)/dt$ at turn-on is obtained by substituting (B.38) and (B.46) into (B.36) and rearranging to obtain

$$\Delta \frac{dv}{dt}\bigg|_0 = \frac{RR_C}{L_s(R+R_C)}\left(V_D + v_{0-}\right) + \left[\frac{1}{R_C C} - \frac{R_s}{L_s} - \frac{1}{(R+R_C)C}\right]\Delta v_0 .$$
(B.52)

where again v_{0-} is given in (B.30) and v_{C0} is given in (B.25)

The jump in $dv(t)/dt$ at turn-off is obtained by substituting (B.43) and (B.47) into (B.23) to obtain

$$\Delta \frac{dv}{dt}\bigg|_f = \frac{-RR_C}{\left(R + R_C\right)L_s}\left(V_D + V_{f+}\right) + \left[\frac{R^2}{\left(R + R_C\right)^2 C} - \frac{RR_C R_s}{\left(R + R_C\right)L_s}\right]\left[\left(i_{S0-} - \right.\right.$$

$$\left.\left.\frac{N_p}{N_s}\frac{E-V_{CE}}{R_p}\right)e^{-\frac{R_p t_{on}}{L_p}} + \frac{N_p}{N_s}\frac{E-V_{CE}}{R_p}\right] \tag{B.53}$$

where v_{f+} is given in (B.15) and i_{S0-} is given in (B.38).

The jumps are in the output voltage $v(t)$ and are expressed in terms of unnormalized parameters. In order to utilize these expressions in the sequence function analysis, they must be transformed to jumps in the normalized error voltage.

The error voltage is

$$\varepsilon(t) = V_R - v_t(t) - v(t) \quad . \tag{B.54}$$

The reference voltage V_R is constant; and since switching is assumed to occur instantaneously $v_t(t)$ is constant during switching. Therefore, the jump in $\varepsilon(t)$ is the negative of the jump in $v(t)$ which when normalized results in

$$\Delta x_0 = -\Delta v_0 / V_R \tag{B.55}$$

$$\Delta x_f = -\Delta v_f / V_R \quad . \tag{B.56}$$

Since V_R is a constant the derivative of the error voltage is

$$\frac{d\varepsilon(t)}{dt} = -\frac{dv_t(t)}{dt} - \frac{dv(t)}{dt} \quad . \tag{B.57}$$

Since $dv_t(t)/dt$ is constant,

$$\Delta \frac{d\varepsilon(t)}{dt} = - \Delta \frac{dv(t)}{dt} \tag{B.58}$$

which when normalized results in

$$\Delta y_0 = \Delta \frac{dx}{d\tau}\bigg|_0 = - \frac{1}{\omega_0 V_R} \Delta \frac{dv}{dt}\bigg|_0 \tag{B.59}$$

and

$$\Delta y_f = \Delta \frac{dx}{d\tau}\bigg|_f = - \frac{1}{\omega_0 V_R} \Delta \frac{dv}{dt}\bigg|_f \tag{B.60}$$

where $\omega_0 = 1/\left(L_s C\right)^{1/2}$.

Appendix C

EXPERIMENTAL CONFIRMATION OF THE

ANALYSIS OF CHAPTER IV

Many effects such as switching speeds and stray capacitance exist at a frequency of 1 MHz which make the 1 MHz converter in Chapter III unsuitable to use in making an experimental verification of the analysis in Chapter IV. For this reason, a converter, to be used experimentally to verify the analysis in Chapter IV, is designed to operate at a much lower switching frequency of 2 kHz. The complete schematic diagram of this converter circuit is given in Fig. C.1 and the complete components list is given in Table C.1.

Simplified operational concept. The basic regulation concept for the 2 kHz converter is the same as that for the 1 MHz converter; however, the circuitry used to implement this concept is different. A simplified operational diagram of the circuit in Fig. C.1 is shown in Fig. C.2. In this diagram the dc output voltage $v(t)$ is reduced by OP AMP I3 to a level compatible to the reference voltage V_R and is summed with the triangular voltage $-v_t(t)$ at the input to OP AMP I2. I2 is a unity gain inverting amplifier which returns $v(t)$ to the normal

(176)
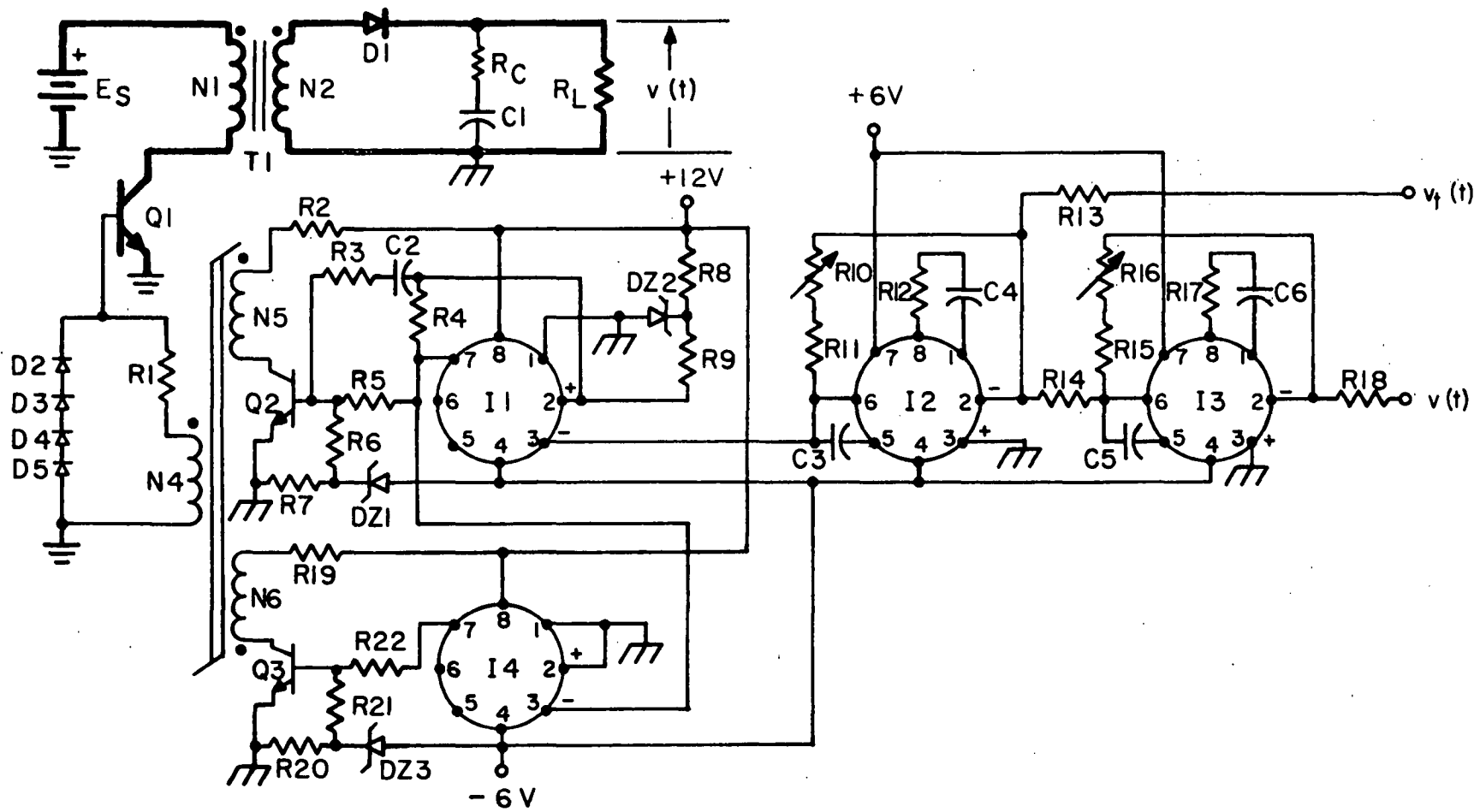
Fig. C.1.   Schematic diagram of the 2 kHz converter.

Table C.1. Components list for Fig. C.1.

C1	1875 µF	6- 300 µF 30 V tantalum electrolytic
C2	0.00022 µF	1 kV disc ceramic
C3,C5	0.00025 µF	1 kV disc ceramic
C4,C6	0.005 µF	1 kV disc ceramic
D1	10R2 (Isofilm International)	
D2-D5	UTR-12 (Unitrode Corp.)	
DZ1	1N750A	
DZ2,DZ3	1N751A	
E_S	Source Voltage, 21-31 volts	
I1,I4	SN72 710L Differential Comparator (TI)	
I2,I3	µ709 Operational Amplifier (Fairchild)	
N1	100 turns #19 AWG	
N2	150 turns #21 AWG	
N4	23 turns #25 AWG	
N5	113 turns #25 AWG	
N6	10 turns #25 AWG	
Q1	DTS-410 (Delco)	
Q2	2N3501 (Motorola)	
Q3	2N3499 (Motorola)	
R_C	0.145 Ω	
R1	8.2 Ω	
R2,R5,R19,R22	22 Ω	
R3	220 KΩ	
R4	580 KΩ	
R6,R21	470 Ω	
R7,R8,R20	1.8 KΩ	
R9	12 KΩ	
R10,R16	10 KΩ trimpot	
R11,R15	5110 Ω 1%	
R12,R17	1.5 KΩ	
R13,R14	10 KΩ	
R18	71.5 KΩ 1%	
T1	55436 (Magnetics, Inc.)	
T2	52176-1A (Magnetics, Inc.)	

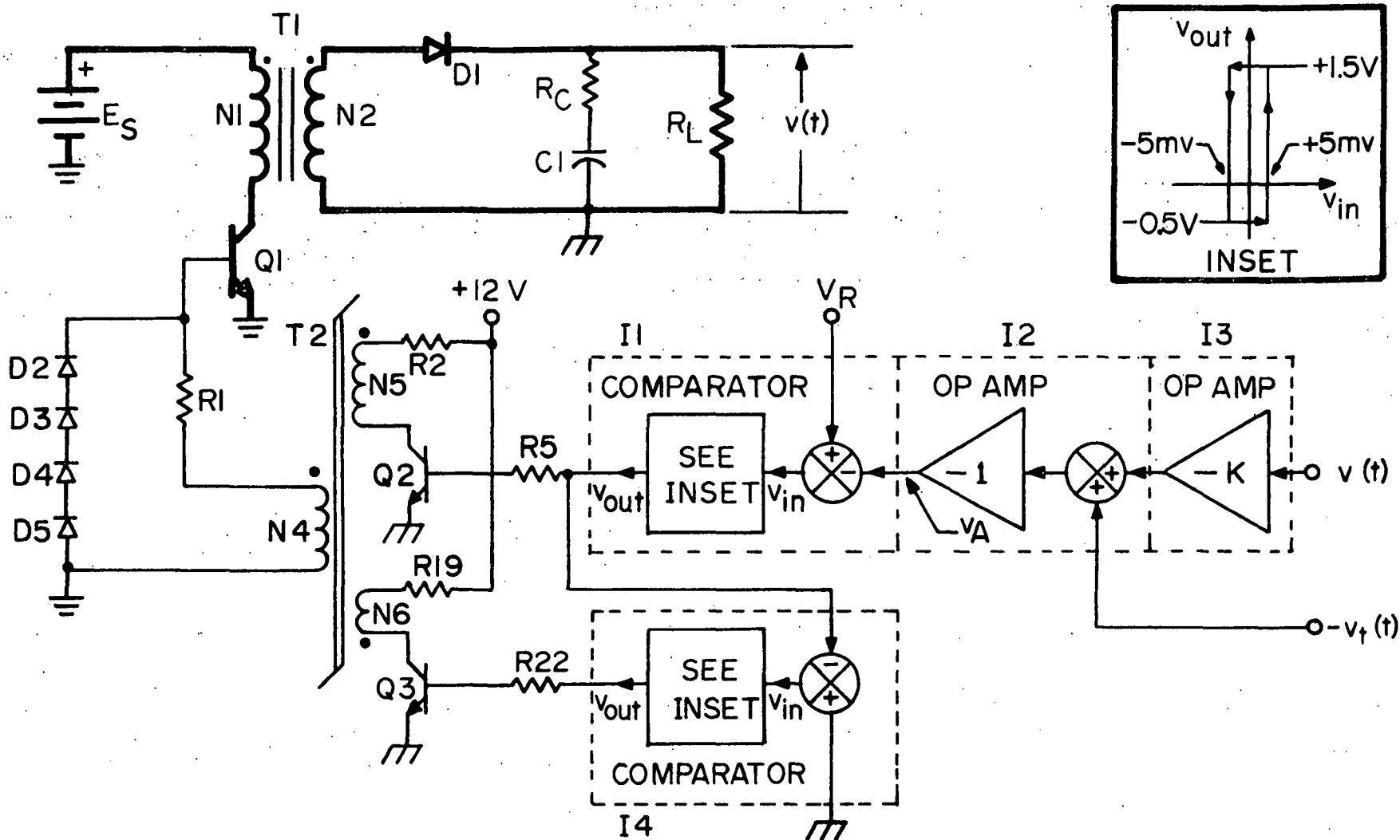Fig. C.2 Simplified operational diagram of the 2 kHz converter.

polarity and acts as a summing junction for $-v_t(t)$ and $-Kv(t)$. Since $v_t(t)$ is a symmetrical signal, its inversion does not modify circuit functioning. Voltage $v_t(t)$ has a negative sign at its input to the converter to maintain correct mathematical representation. The output $v_A(t)$ of I2 is thus $v_t(t) + Kv(t)$.

Signal $v_A(t)$ is the input to the comparator I1 which compares $v_A(t)$ with the reference voltage V_R. The inset shows the hysteresis and output voltage levels which control Q2 which, in turn, controls the power transistor Q1. Regulation is accomplished by the same manner as explained in Chapter III. When v_A is greater than $V_R - 5\,mV$, comparator I1 output is $-0.5V$ and Q1 is OFF. When V_A is less than $V_R -5\ mV$, comparator I1 output is $+1.5V$ and Q1 is ON.

T2 is a saturable reactor and has to be reset when Q2 is OFF. Reset is accomplished by Q3 and comparator I4. The input to I4 is the output of I1 such that when I1 has a $+1.5V$ output I4 has a $-0.5V$ output and vice versa. This means that Q3 is ON when Q2 if OFF resetting the magnetic flux excursion which occurs in T2 when Q2 is ON.

Experimental waveforms. Pictures of experimental waveforms for the ac components of $v(t)$ and $v_A(t)$ are shown in Fig. C.3. These waveforms were taken under the circuit conditions of $E_S = 21.0V$ and $R_L = 40.155$ ohms. Complete measured circuit conditions and parameters for the same operating conditions as existed for Fig. C.1. are shown in Table C.2. The general shape
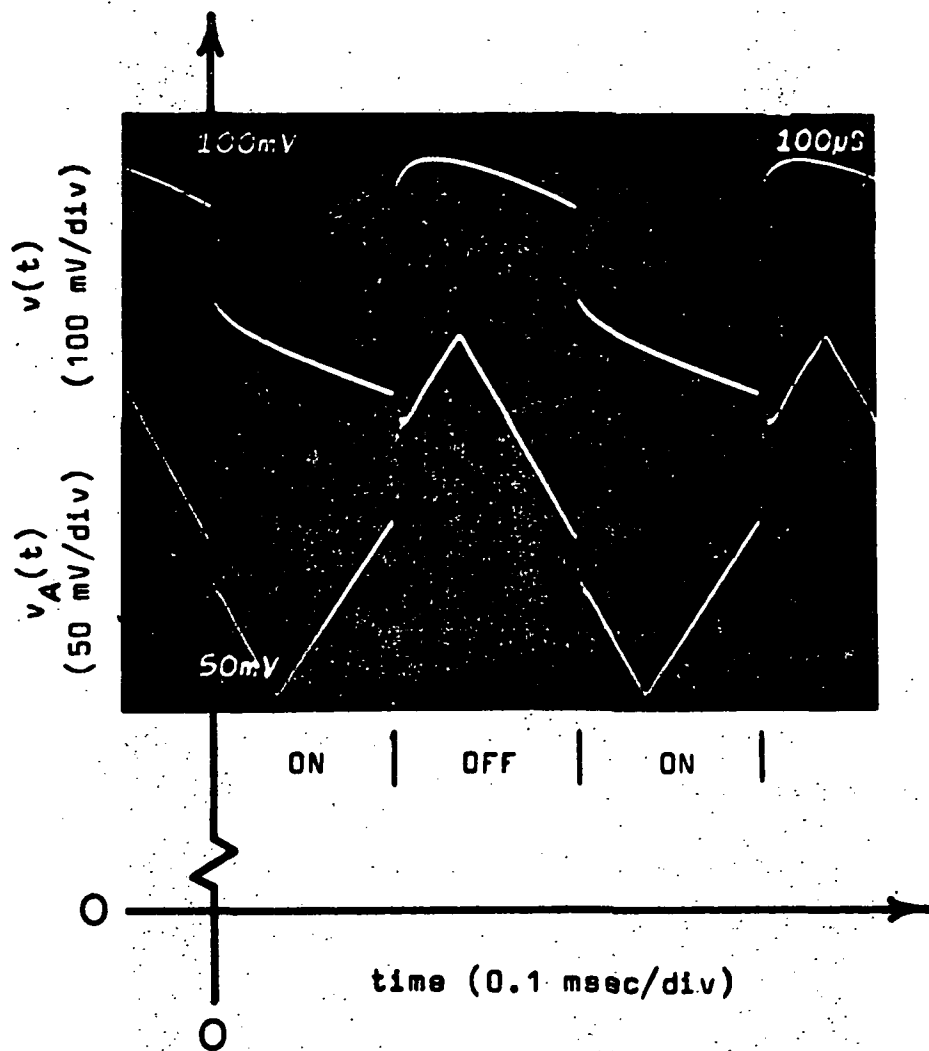
Fig. C.3. Experimental waveforms of the ac
components of $v(t)$ and $v_A(t)$.

Table C.2. Numerical values for the experimental
2 kHz converter used to evaluate the
theoretical expressions.

E_S	21.0	volts
V_O	28.26	volts
V_{tm}	0.10	volts
V_R	4.926	volts
V_D	0.725	volts
V_{CE}	0.40	volts
δ_1	0.005	volts
δ_2	0.005	volts
R	40.155	ohms
R_C	0.145	ohms
R_S	0.432	ohms
R_p	0.175	ohms
C	1875	μF
L_S	7.65	mII
L_p	3.05	mH
N_p	100	turns
N_S	150	turns
T	0.500	msec
α	0.091	msec
γ	0.155	msec
t_{on}	0.246	msec
t_{off}	0.254	msec

of v(t) in Fig. C.3 agrees with the shape depicted in Fig. 26(b) except immediately after turn-on and turn-off where Fig. C.3 exhibits more curvature which is likely to be caused by parasitic capacitance or inductance.

Fig. C.4 is a photograph of the experimental limit cycle in the phase plane which is the time derivative of $v_A(t)$ versus $v_A(t)$ shown in Fig. C.3. This experimental limit cycle is normalized and shown in Fig. C.5 along with the normalized theoretical limit cycle.

Computation of the theoretical limit cycle. The theoretical limit cycle is determined by assuming an initial point P_0 just prior to turn-on to be the same as the corresponding experimental point. P_7 is determined by evaluating the magnitude of the jump from P_0 to P_1 by substituting the appropriate values from Table C.2 into (B.35) and (B.52). The jumps ΔV_0 and $\Delta dv/dt|_0$ are normalized and added to the x and y coordinates of P_0 to obtain P_1.

The trajectory from P_1 to P_2 is determined by solving (119) for $x(\tau)$ as

$$x(\tau_1) = A\, e^{-\tau_1/\tau_C} + 1 + \frac{4V_{tm}\tau_C}{\omega_0 V_R T} \quad . \tag{C.1}$$

Time t_1 is the real time variable and τ_1 is the normalized time variable during movement on the trajectory from P_1 to P_2. This notation is used throughout the following discussion. The
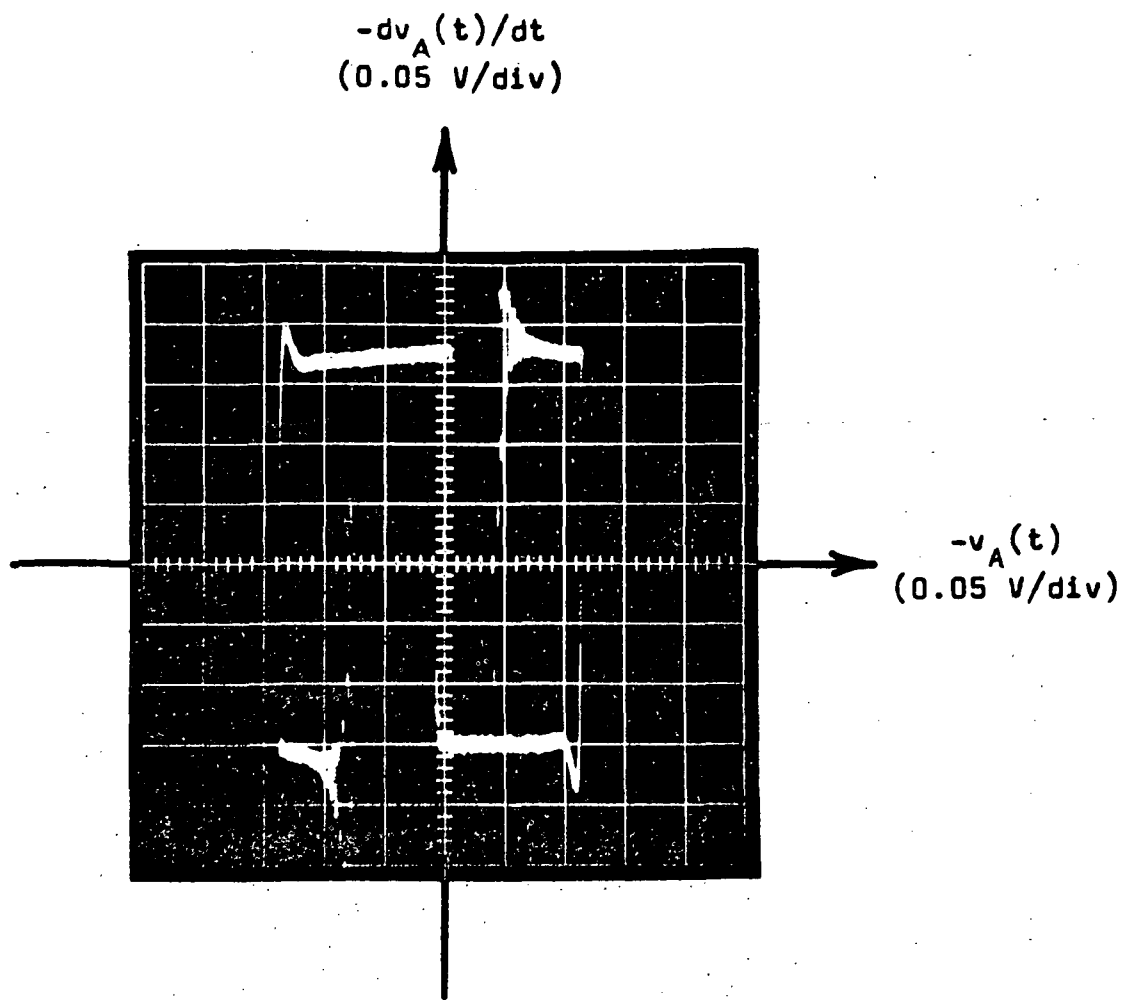
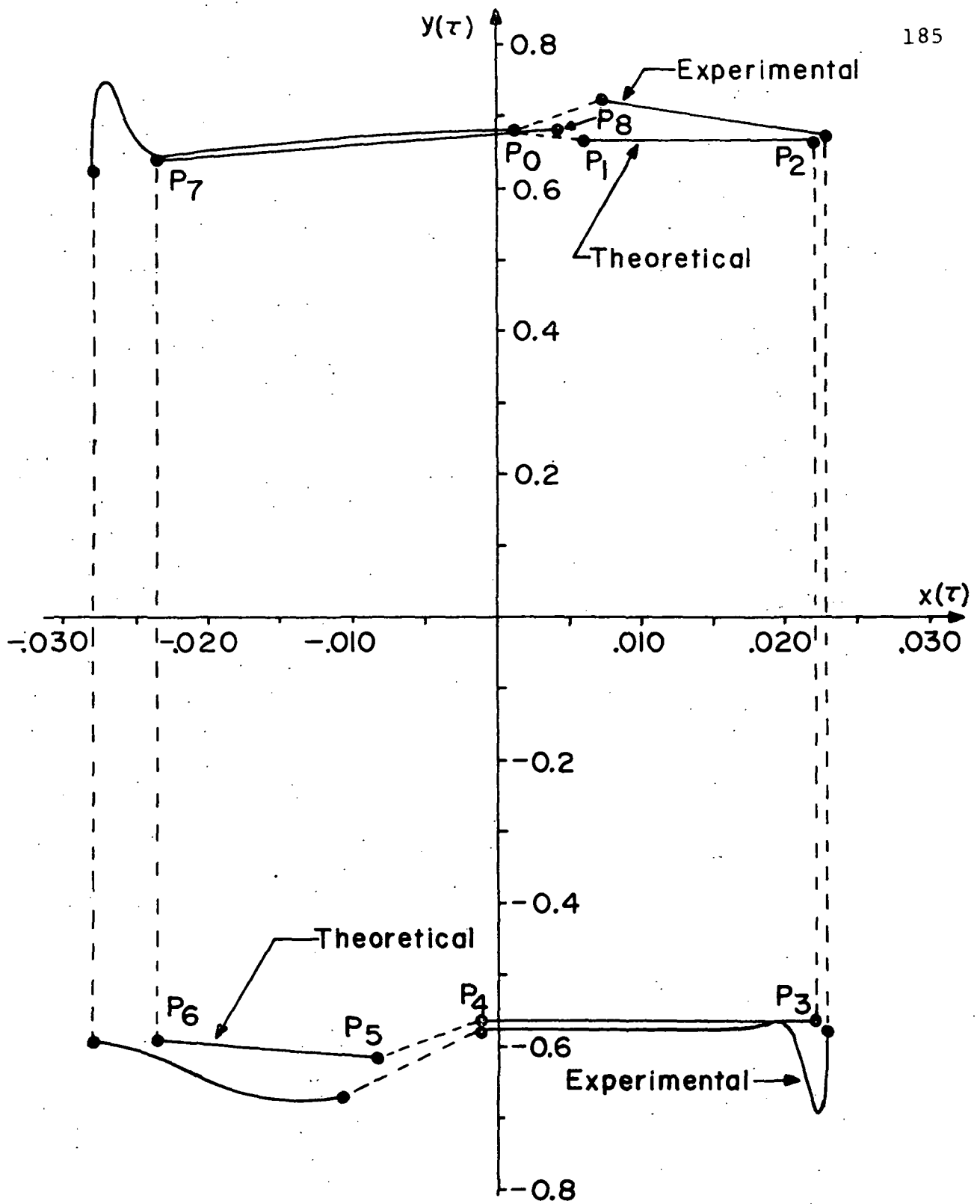Fig. C.4. Experimental limit cycle $-dv_A(t)/dt$ versus $-v_A(t)$.

Fig. C.5. Experimental and theoretical limit cycles for the 2 kHz converter.

numerical subscript on t or τ is the same as the subscript of the point at which the time variable is zero. The final value of the variable is reached when the next higher integer sub-scripted point is reached. The unknown constant A is evaluated by letting $x(0) = x_1$ where x_1 is the x-coordinate of P_1 at $t_1 = 0.0$, or $\tau_1 = 0.0$. The y-coordinate is simply the deriva-tive of (C.1) which is

$$y(\tau_1) = -\frac{A}{\tau_C} e^{-\tau_1/\tau_C} \; . \qquad (C.2)$$

Equations (C.1) and (C.2) are evaluated at increments of τ_1 from $\tau_1 = 0.0$ to $\tau_1 = 0.024$ when P_2 is reached. The final value of τ_1 is calculated by $\tau_1 = \omega_0 t_1 = \omega_0 \alpha$ where ω_0 is calculated using values from Table C.2 and α is measured in Fig. C.3 and given in Table C.2.

The jump from P_2 to P_3 occurs at the instant when the slope of $v_A(t)$ changes from negative to positive by an amount equal to twice the slope of $v_t(t)$. At this jump, the x-coordi-nate and τ do not change; and the y-coordinate changes by $-8V_{tm}/\omega_0 V_R T$ as shown in Fig. 24. The jump in the y-coordinate is negative because $y(\tau) = \left(-1/\omega_0 V_R\right) dv_A/dt$. P_3 is thus defined by $x_3 = x_2$ and $y_3 = y_2 - 8V_{tm}/\omega_0 V_R T$.

The trajectory for P_3 to P_4 is determined by solving (118) for $x(\tau_3)$ as

$$x(\tau_3) = B e^{-\tau_3/\tau_C} + 1 + \frac{4V_{tm}\tau_C}{\omega_0 V_R T} \qquad (C.3)$$

where τ_3 is the normalized time variable during movement from P_3 to P_4. The unknown constant B is evaluated by letting $x(0) = x_3$ where x_3 is the x-coordinate of P_3 at $t_3 = 0.0$, or $\tau_3 = 0.0$. The y-coordinate is simply the derivative of (C.3) which is

$$y(\tau_3) = -\frac{B}{\tau_C} e^{-\tau_3/\tau_C} \quad . \qquad (C.4)$$

Equations (C.3) and (C.4) are evaluated at increments of τ_3 from $\tau_3 = 0.0$ to $\tau_3 = 0.041$ when P_4 is reached. The final value τ_3 is determined by $\tau_3 = \omega_0 \gamma$ where ω_0 has been previously computed and γ is given in Table C.2.

The jump from P_4 to P_5 occurs at turn-off and is determined by evaluating (B.51) and (B.53) for Δv_f and $\Delta dv_f/dt|_f$, respectively. The jumps are then normalized to yield Δx_f and Δy_f which are added to x_4 and y_4, respectively, to yield the x and y-coordinates of P_5.

The segment of the limit cycle from P_5 to P_6 is defined by (120). The solution to (120) which defines the x-coordinate is

$$x(\tau_5) = G e^{-h\tau_5} \cos\left(\omega \tau_5 - \delta\right) + 1 + \frac{V_D}{V_R} - \frac{8hV_{tm}}{\omega_0 V_R T} \qquad (C.5)$$

where h is given in (113) and $\omega = (1 - h^2)^{1/2}$. The derivative of (C.5) is

$$y\left(\tau_5\right) = -G\ e^{-h\tau_5}\left[\omega\ \sin\left(\omega\tau_5 - \delta\right) + h\ \cos\left(\omega\tau_5 - \delta\right)\right] \qquad (C.6)$$

and (C.6) defines the y-coordinate. G and δ are unknown constants which are evaluated by substituting $x(0) = x_5$ and $y(0) = y_5$ into (C.5) and (C.6). Equations (C.5) and (C.6) are evaluated for incremental values of τ_5 from 0.0 to 0.025 to obtain the trajectory from P_5 to P_6. The final value of $\tau_5 = 0.025$ at P_6 is obtained from $\tau_5 = \omega_0\left[(T/2) - \gamma\right]$.

The jump from P_6 to P_7 occurs at the instant when the slope of $v_A(t)$ changes from positive to negative. There is no change in x and the change in y is of equal magnitude but opposite sign as the jump from P_2 to P_3. P_7 is thus defined as $x_7 = x_6$ and $y_7 = y_6 + 8V_{tm}/\omega_0 V_R T$.

The segment of the limit cycle from P_7 to P_8 is defined by (121). The solution to (121) is

$$x\left(\tau_7\right) = H\ e^{-h\tau_7}\ \cos\left(\omega\tau_7 - \theta\right) + 1 + \frac{V_D}{V_R} - \frac{8hV_{tm}}{\omega_0 V_R T} \qquad (C.7)$$

which defines the x-coordinate. The derivative of (C.7) is

$$y\left(\tau_7\right) = -H\ e^{-h\tau_7}\left[\omega\ \sin\left(\omega\tau_7 - \theta\right) + h\ \cos\left(\omega\tau_7 - \theta\right)\right] \qquad (C.8)$$

and (C.8) defines the y-coordinate. H and θ are unknown constants which are evaluated by substituting $x(0) = x_7$ and $y(0) = y_7$ into (C.7) and (C.8). Equations (C.7) and (C.8) are evaluated for incremental values of τ_7 from $\tau_7 = 0.0$ to 0.042 to obtain the trajectory from P_7 to P_8. The final value of

$\tau_7 = 0.042$ at P_8 is obtained from $\tau_7 = \omega_0 \left[(T/2) - \alpha \right]$. P_8 is the final point in the limit cycle and for steady-state conditions should have the same coordinates as P_0.

Comparison of the experimental and theoretical limit cycles. The experimental and theoretical limit cycles in Fig. C.5 compare very closely. The experimental jumps from P_0 to P_1 at turn-on and from P_4 to P_5 at turn-off are slightly greater than the theoretical jumps. This difference could be caused by inaccuracies in the measurements of the numerical values given in Table C.2 or by parasitic circuit elements that were present but not considered in the analysis. This difference may also be caused by the finite switching time which exists experimentally and for which the theoretical analysis assumes instantaneous switching. The effect of the parasitic circuit elements should be the greatest effect because the differences in the slopes of the trajectories from P_1 to P_2 and the general difference in the nature of the trajectories from P_5 to P_6 is the result of the unpredicted curvature in $v(t)$ immediately after turn-on and turn-off as shown in Fig. C.3 and is attributed to parasitic circuit elements.

It is interesting to note that the theoretical trajectory passes directly through the initial point P_0 in attaining point P_8. This phenomenum is probably coincidental; however, if P_5 and the entire lift side of the limit cycle were displaced in the negative x direction until the theoretical x_5 equals the

experimental x_5, P_8 would be closer to P_0. This leads to the conclusion that the difference in the jump at turn-off may at least be partially responsible for P_8 not being the same point as P_0.

Experimental verification of the sequence functions. There are two equations (152) and (162) in Chapter IV which are derived using sequence function analysis. These equations completely define the steady-state conditions of the converter analyzed in Chapter IV. Equation (152) is obtained by equating x_2 and x_3 from (150) and (151).

To verify (152), x_2 and x_3 are evaluated using (150), (151), and the conditions given in Table C.2 yielding $x_2 = 0.02209607$ and $x_3 = 0.02212789$. The difference, $x_3 - x_2 = 3.182 \times 10^{-5}$, is practically negligible.

Equation (162) is verified by substituting the circuit conditions from Table C.2 into (157) and (161) to obtain $x_6 = -0.023485052$ and $x_7 = -0.026003728$. The difference $x_6 - x_7$ is 2.518676×10^{-3}. The differences $x_3 - x_2$ and $x_6 - x_7$ are small enough to conclude that the sequence function equations are experimentally verified.

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