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PLANAR ELECTROLUMINESCENT PANEL TECHNIQUES

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February 1973

Final Report

Contract No. NAS 5-10192

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PLANAR ELECTROLUMINESCENT PANEL TECHNIQUES

By
Charles Kerr and Robert E. Kell

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FINAL REPORT

Contract No. NAS 5-10192

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FOREWORD

The work described in this report was initiated at Calspan (then the Cornell Aeronautical Laboratory, Inc.) in early 1967 as a follow-on to prior CAL work on electroluminescent displays. While the research was in progress, the principal investigator, T. L. Robinson, left the employ of Calspan and established a separate firm under the name of ASTRONICS. The development of the multipurpose display panel with latch-in memory was interrupted by this transition. A subcontract was let by Calspan to ASTRONICS to complete the investigation. After a lapse of many months, during which several unsuccessful attempts were made to achieve practicable solutions to the PEL-EL-PC latch-in memory problem, it was decided that attempts to solve the latch-in memory problem should not be continued under this contract, and the significant results of the research should be assembled in this final report.

ABSTRACT

Investigations of planar electroluminescent multipurpose displays with latch-in memory are described. An 18" x 24" flat, thin address panel with elements spacing of 0.100" was constructed which demonstrated essentially uniform luminosity of 3-5 foot lamberts for each of its 43200 EL cells. A working model of a 4-bit EL-PC (electroluminescent photoconductive) electrooptical decoder was made which demonstrated the feasibility of this concept. A single-diagram electroluminescent display device with photoconductive-electroluminescent latch-in memory was constructed which demonstrated the conceptual soundness of this principle. Attempts to combine these principles in a single PEL multipurpose display with latch-in memory were unsuccessful and were judged to exceed the state-of-the-art for close-packed (0.10" centers) photoconductor-electroluminescent cell assembly.

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I. INTRODUCTION

This report describes research in planar electroluminescent (PEL) panel techniques supported by NASA under Contract No. NAS5-10192 to provide a versatile, compact visual display unit to present subsystem status and operating data of space vehicles. This research was a continuation of NASA-supported investigations initiated at Calspan (then the Cornell Aeronautical Laboratory) in mid-1966 to develop system configuration displays using PEL techniques. The earlier work established some of the basic parameters of PEL cell design (including choice of operating frequency, electrode structure, and methods of applying the electroluminescent phosphor) and developed techniques for design and assembly of single-diagram and multiple-diagram (now commonly called multifunction) PEL displays. The multifunction display developed on that program contained several PEL modules, each of which could be separately caused to glow by connecting a suitable voltage between its terminals.

For a small number of display modules, and for control of the luminescence of each module by manual or electromechanical switching, the task of switching the module voltage on or off, and especially of leaving the switch in the "on" position indefinitely, posed no particular problem. As the desired number of functions to be displayed increased, however, the complexity of direct manual or other mechanical switching was expected to become impractical. It therefore appeared desirable to develop a means for latching the display module in the "on" position after momentary switch contact or after a brief voltage pulse commanded by a central computer; a similar "erase" command should be effective in returning the display module to its quiescent state. This feature was designated "latch-in memory" and was the primary topic investigated in the work reported herein.

The initial objective of the present program was to provide a multifunction display with latch-in memory for each individual function module. The requirement that the latch-in memory should respond to commands from existing space support computers necessitated the construction of a

suitable decoding unit which would accept binary coded input signals and translate them to suitably switched outputs.

The logic for a binary decoder combining electroluminescent cells and photocells was developed and a working model to accept a four-bit binary input was constructed and tested.

At this point in the program, the construction of the latch-in memory display matrix to provide greater flexibility and versatility by using simply an electroluminescent array of dots began to appear feasible. The illumination pattern shape and orientation would be determined by commands from a central computer. With the concurrence of the sponsoring agency, it was decided to designate this more general display a "multi-purpose display with latch-in memory" and to concentrate effort on this device. One complete 6" x 6" multipurpose display panel module with latch-in memory was to be constructed, and twelve 6" x 6" electroluminescent modules (without the latch-in memory feature) were to be assembled in an 18" x 24" address panel. The research described in the following pages thus was directed to the following three major components, which are shown diagrammatically in Figure 1.

1. An electro-optical binary to decimal Decoder for the X and Y axes.
2. An 18" x 24" electroluminescent (EL) X-Y Address Panel able to light and thus address over 43,000 individual points.
3. A partial Display Panel having photoconductive-electroluminescent (PC-EL) dots, which would register with the addressing dots and test the "memory" concept. This was to provide a latching PC-EL memory to maintain a discrete EL point on the system Display Panel. This would stay lit when addressed and thus have memory until display power was interrupted.

The EL, EL-PC combination, which is the basis of this report, is shown schematically in Fig. 2. It shows one composite element of the multi-purpose display consisting of an electroluminescent cell, EL_1 , on the Address Panel and EL_2 -PC on the Display Panel. The arrows shown in Figure 2 indicate the optical coupling of an EL cell to the photoconductive

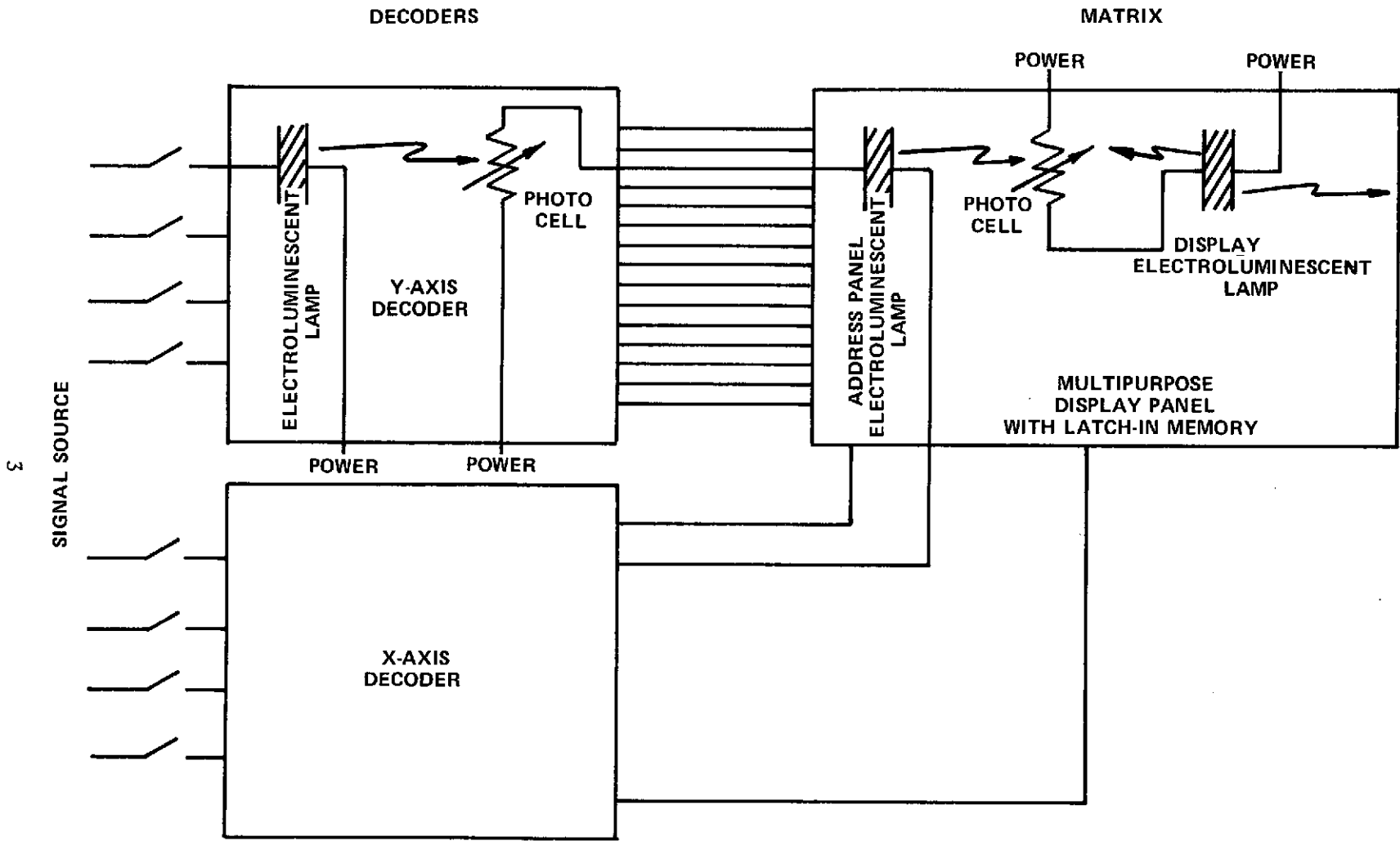


Figure 1 MULTIPURPOSE DISPLAY

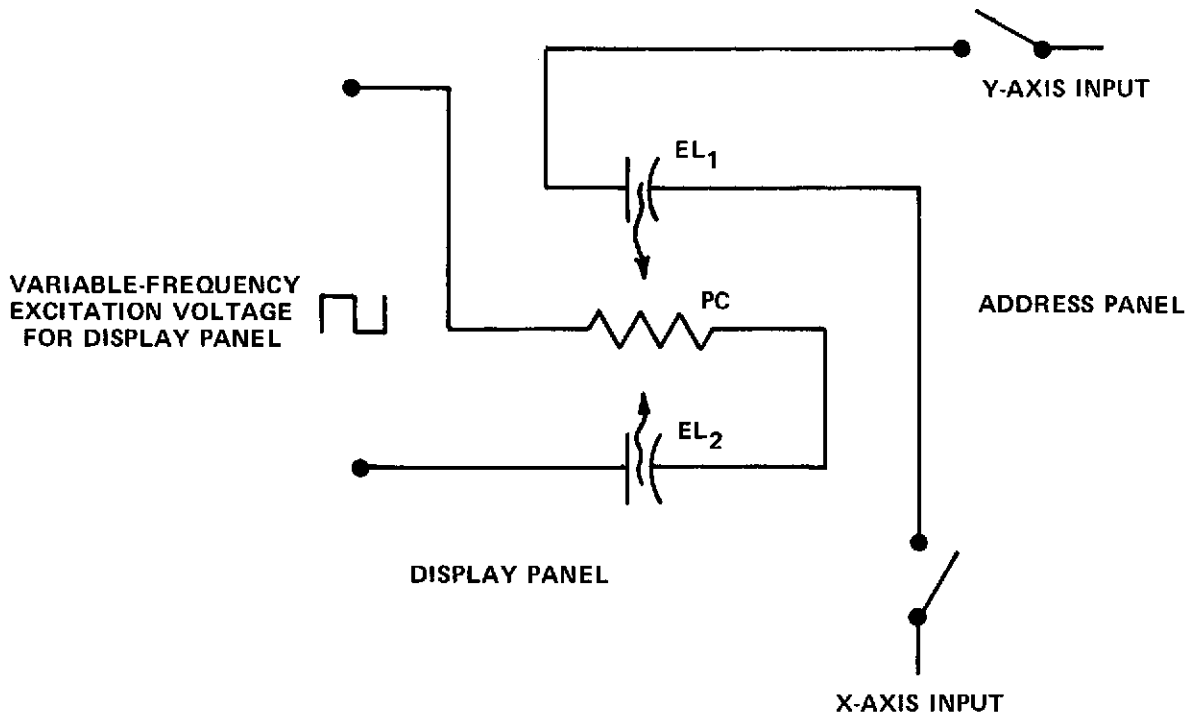


Figure 2 SCHEMATIC OF ONE ELECTROLUMINESCENT PC CELL ASSEMBLY WITH MEMORY CAPABILITY

element. The switches represent the terminal output signals from the Decoders. It can be seen that only the Address Panel, composed of EL cells arranged in an X-Y coordinate array, is connected to the decoders. These two separate panels and the Decoder comprise the display system. The function of the Address Panel is to activate EL cells on the Display Panel, which in turn latch themselves in the "on" state. PC and EL₂ cells on the Display Panel are connected to a separate 275V, 400Hz supply. The function of the Display Panel is to display and latch EL information as optically directed to it by the Address Panel. By momentarily interrupting this supply, erasure of the EL diagram is effected. Figure 3 shows, schematically, the X-Y mosaic of EL Address cells. Figure 4 shows, schematically, the memory Display Panel mosaic.

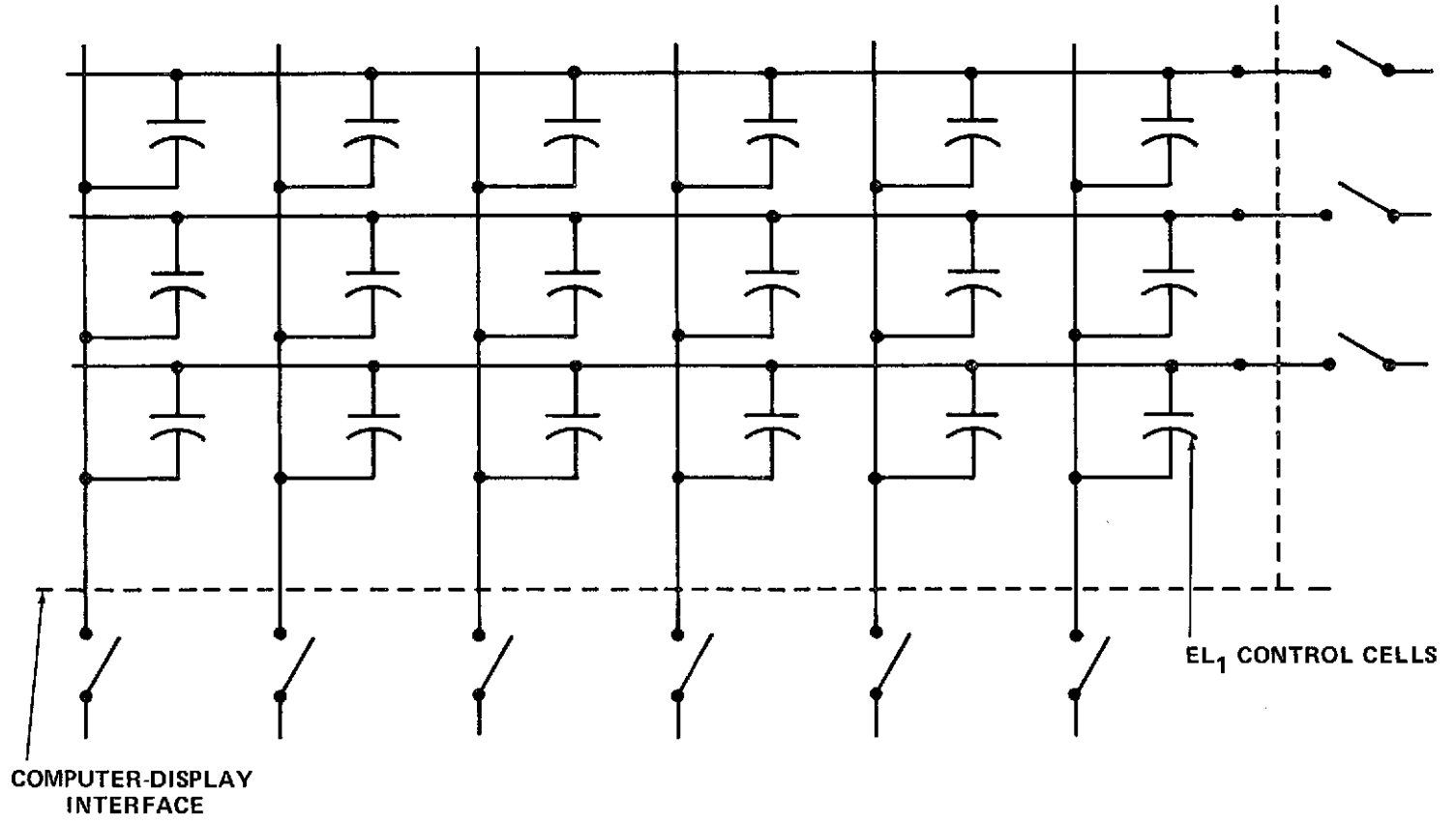


Figure 3 SCHEMATIC DIAGRAM OF ADDRESS PANEL

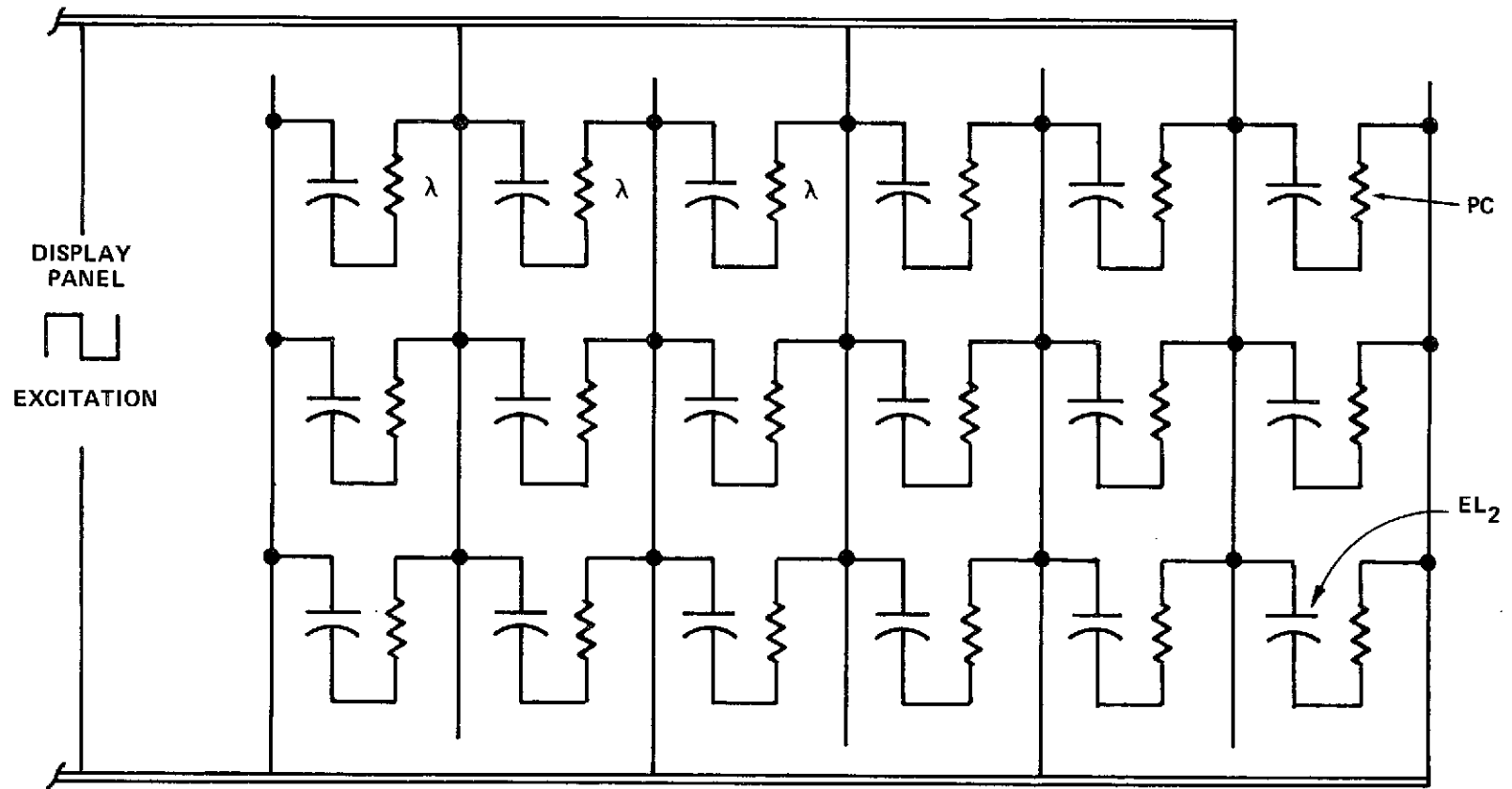


Figure 4 SCHEMATIC OF MULTIPURPOSE DISPLAY PANEL

II. INDIVIDUAL COMPONENTS OF THE MULTIPURPOSE DISPLAY

1. Electro Optical Decoder, Using EL Lamps and Photocells

Figure 5 is a schematic diagram of a Decoder for energizing one axis. The Decoder produces a momentary pulse to light an EL lamp at the intersection of two axes. The Decoder requires a 6-bit binary input to effect control of 64 switch positions; therefore, two 6-bit decoders would be required for a 64 x 64 switching function. The 64-count decoder is composed of cells, each controlled by one bit. These EL cells are rectangular in shape and cover an area large enough to control the resistance of photoconductive elements, optically coupled to them as seen in Figure 5. To avoid complexity in the schematic, only the photoconductors required for a count of 0-18, 31-33, 62 and 63 have been drawn. The EL-PC decoder operates as follows: In the unexcited state all photoresistors, R1, R2, ... etc., are effectively open circuits. The binary number for closing switch 1 in a 6-bit code is (000001). Referring to the schematic of Figure 5, the line numbered 1 on the right-hand side of the diagram is shown connected in series with photoconductor R14 in series with the excitation voltage and ground. When the binary code (000001) appears, representing bit 1, EL cell 1 lights up and causes the high resistance of R14 to drop to a low value, thus shifting the supply voltage across any load connected in series with line 1 to the supply return line. To close switch 2, the binary code (000010) appears as bit 2, thus lighting EL 2. Photoconductor R13 is then reduced to a low resistance value. Any EL element in a matrix in series with R21 lights up because of the increase in voltage drop across it. Referring back to line 1, it is seen that while R13 is irradiated and in its low resistance state, R14 is not irradiated because the bit controlling EL 1 is in the (0) state while the bit controlling EL 2 is in the (1) state. Thus far, the switching has been straightforward. Conditions for closing switch 3 requires the binary code (000011). At this stage both EL 1 and EL 2 are commanded to light up since their respective control bits are in state (1). In this situation, R14 and R20 will close; but for the binary count of 3, it is not desired to have any switch closed except switch 3. This ambiguity

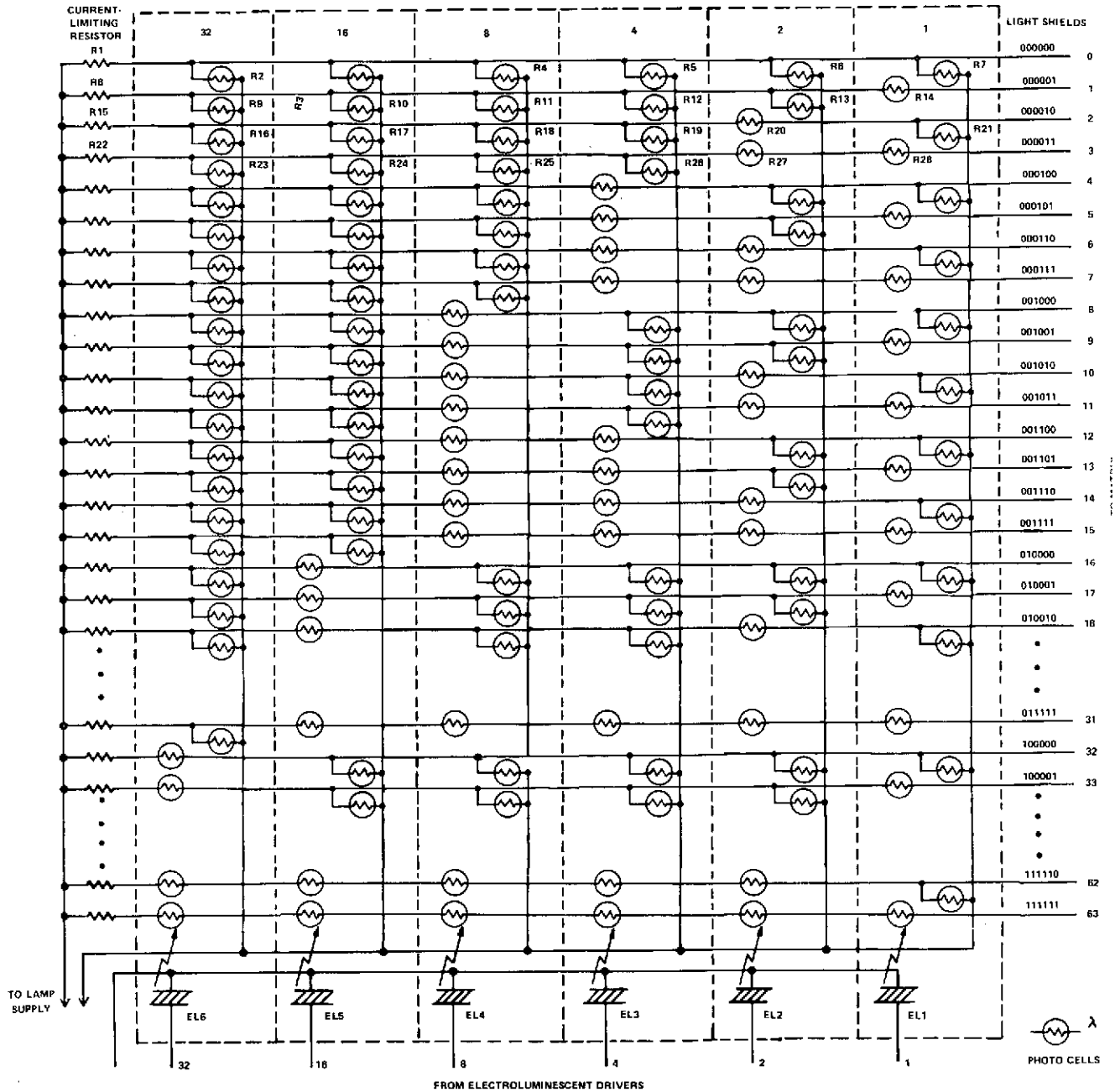


Figure 5 SCHEMATIC OF ELECTRO-OPTICAL DECODER USING ELECTROLUMINESCENT LAMPS AND PHOTO CELLS

is remedied by placing R23 in radiation coupling with EL1, and R27 in radiation coupling with EL 2; EL elements on Line 3 now light up. EL elements on Line 1 and 2 are prevented from lighting by coupling R13 to EL 2 so that it shunts Line 1 in series with R1, thereby reducing the voltage below the threshold required to activate the EL element. Therefore, in this case, EL element 1 does not light. R21 is coupled to EL 1 in order to shunt Line 2 so that it, too, will not light. Recapitulating, the Decoder can now count up to three without ambiguity, made possible by the addition of auxiliary photoconductors to shunt out the unwanted EL elements.

Extension of this same principle permits counting to any number of lines. For 64 lines, 6 photocells are required for each line; for up to 256 lines, 8 photocells would be required for each line. Other methods are also available using a number of smaller identical Decoders and switching entire Decoders on and off.

2. EL-PC Decoder Construction

A breadboard model of the EL-PC optical decoder was fabricated with the ability to count up to ten. Four EL cells, representing the binary bits, were mounted in light tight enclosures, each one being optically coupled to a group of PC cells. Discrete photocells, mounted on a printed circuit card were employed. Figure 6 shows a photograph of this device. In this view, one of the four enclosures is opened to show the EL cell (the long, rectangular, white strip) and the set of photocells.

3. Address Panel

The Address Panel was proposed to be 18" high x 24" long, and was initially composed of twelve 6" x 6" EL panel modules. The total panel has 43,200 EL elements on approximately one-tenth inch centers in each axis. Access to the X and Y axis terminals would be along the sides of the display frame. It is important to note that the initial Address Panels were based upon EL lamps having both electrodes on the face of the lamp. This electrode arrangement was called "interdigital" and was, in effect, a two-sided, printed circuit board, but both circuits were placed on one side of a plastic substrate. A photograph of the interdigital panel is shown in

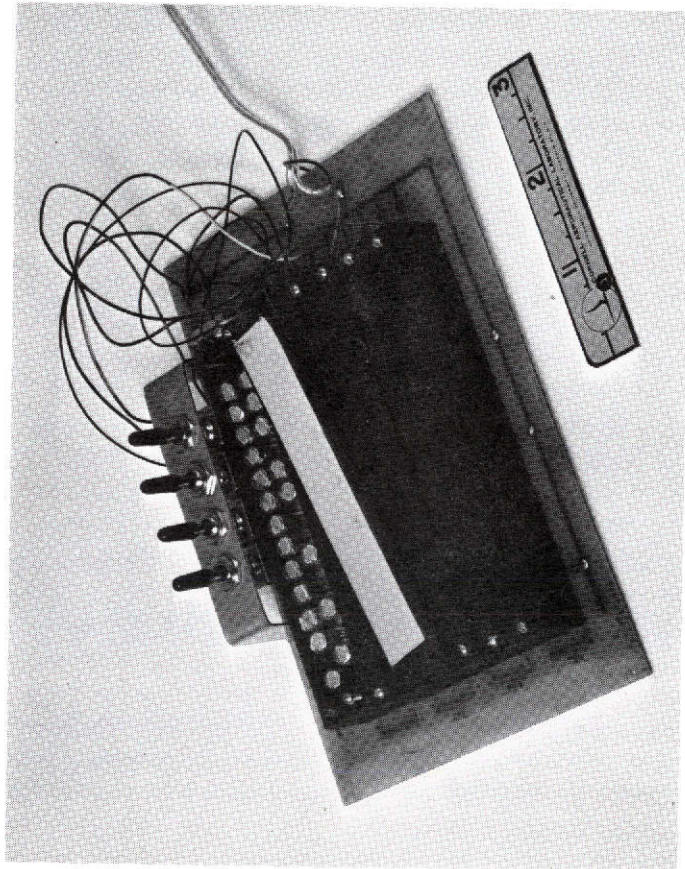


Figure 6 FOUR-BIT ELECTROLUMINESCENT PC DECODER



Figure 7; a corner detail of this panel is shown in Figure 8. The heavy lines in Figures 7 and 8 are the bus bars, each of which connects to one connection tab at the edge of the panel. Each two orthogonal bus bars are insulated at their intersection point by deposited dielectric crossover pads. A great many 6" x 6" X-Y Address Panel modules were fabricated in an attempt to get twelve workable units. Nevertheless, not one was without some shorted cells. The main causes of rejects were due to the following:

1. The EL Cells utilized interdigital electrode structures, typically with 2-1/2 mil line widths on 6 mil centers. Many of the fine lines shorted to others of the opposite polarity or were open-circuited.
2. Feed lines to the X-axis were applied over deposited dielectric crossover pads. A great number of crossovers shorted through the dielectric pads to the Y-axis feed lines.
3. Due to multiple processing steps, the Mylar substrates often shrunk out of registration with other mating modules.

However, an important development in the construction of EL panels* has made it possible to fabricate the present 18" x 24" X-Y Address Panel which was delivered in just two sections, each measuring 12" x 18", shown in Figure 9. The same process could produce the 18" x 24", or larger, panel in one piece.

The two pieces were assembled on a backing material without undesirable spacing which would break the continuity of the EL Address Panel. This was an improvement over the original plan to piece together twelve modules in which discontinuities between modules could be noticed.

This Address Panel is made up of horizontal and vertical electrodes separated by a thin flexible dielectric. The back electrode, the Y axis, is 240 individual vacuum-deposited metallic strips on 0.100 inch centers. The

*See, for example, ASTRONICS Corporation Patent No. 3531676.

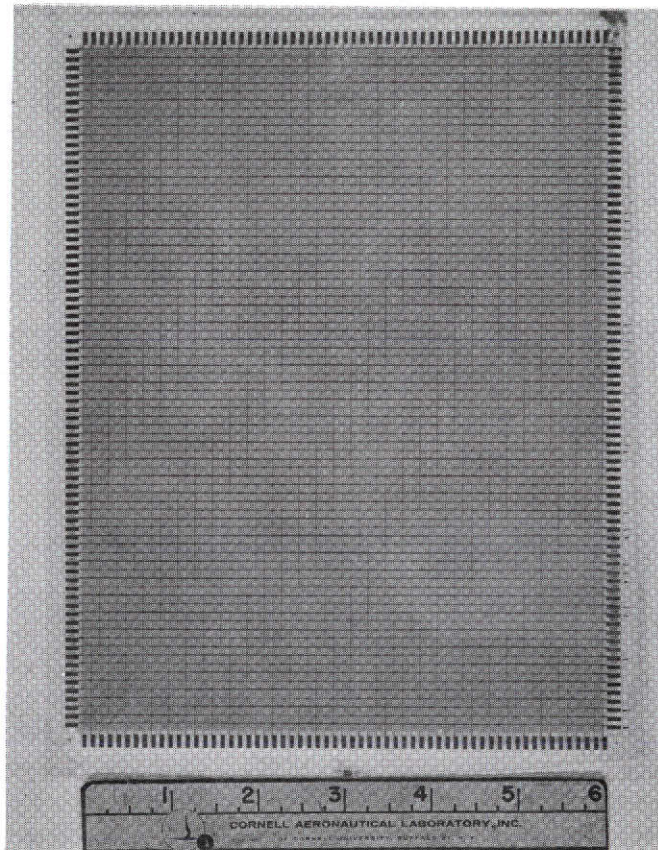


Figure 7 INTERDIGITAL PANEL

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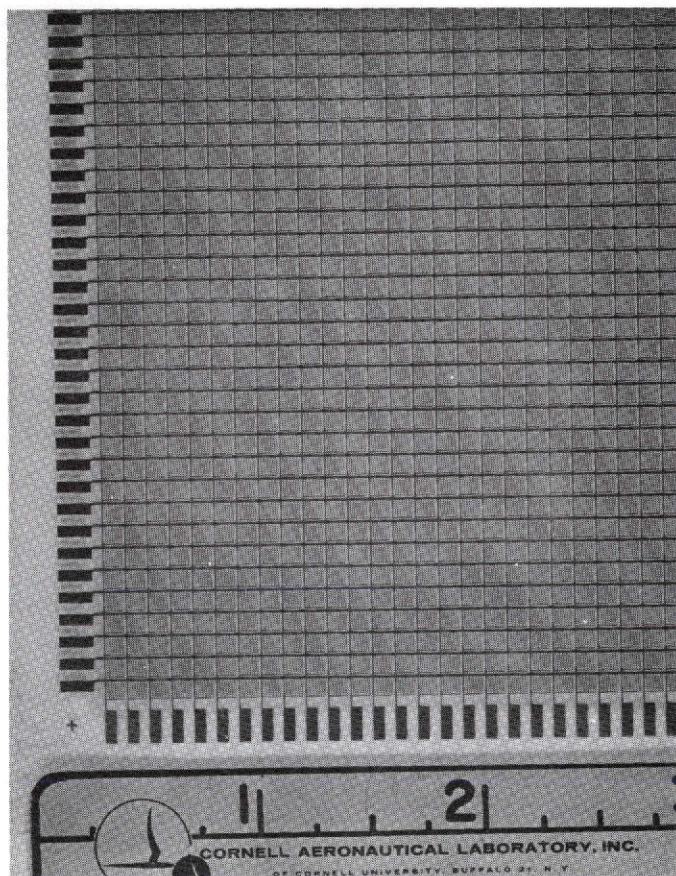


Figure 8 CORNER OF THE INTERDIGITAL PANEL OF FIGURE 7

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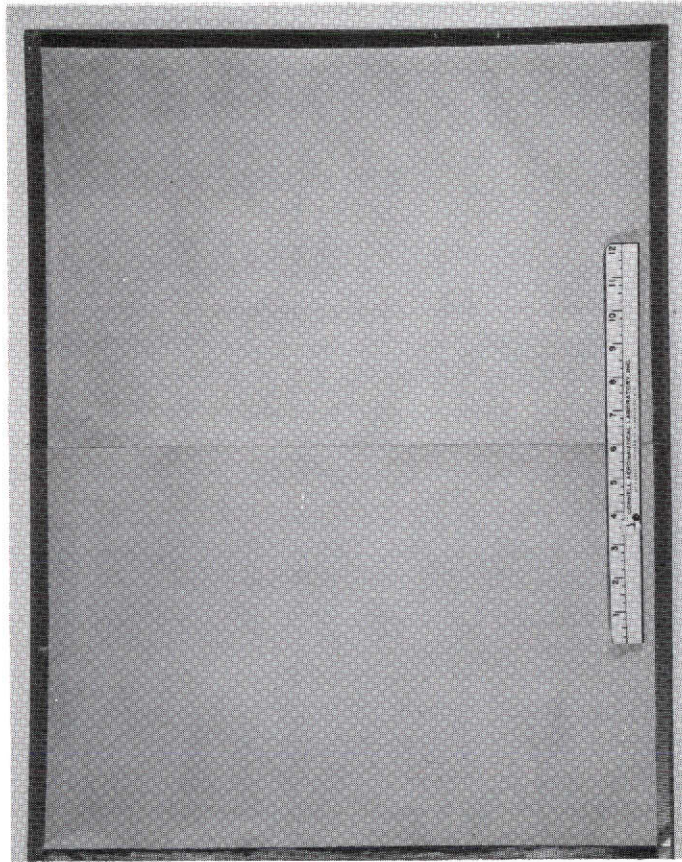
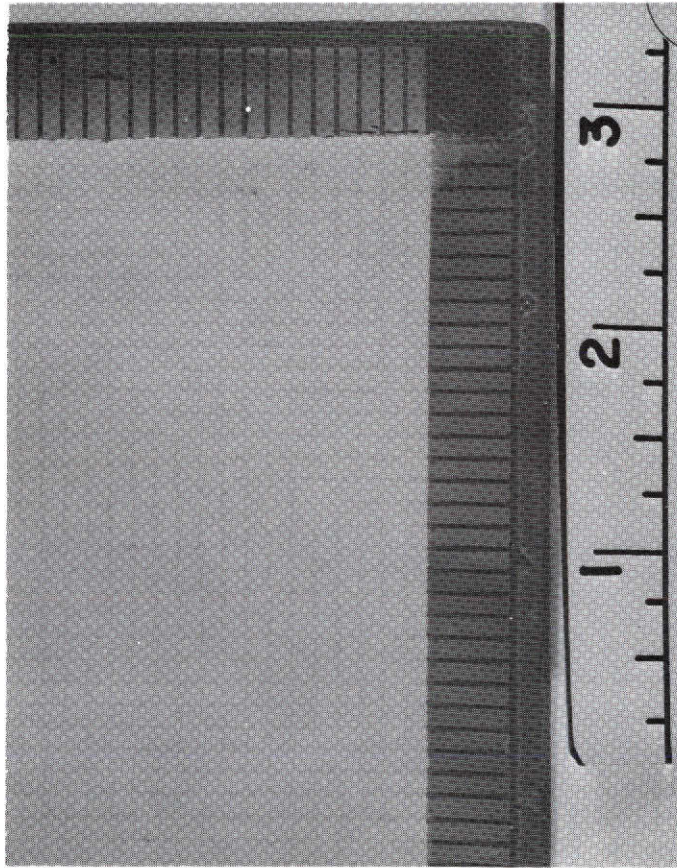


Figure 9 CROSS-STRIP 18" x 24" TWO-SECTION ADDRESS PANEL



front electrode, the X axis, is 180 individual strips in the form of screens. These also are on 0.100 inch centers, making 43,200 intersections on the Address Panel. A phosphor binder mix covers the entire panel which means that when both an X and Y strip are energized by the Decoder the lamp at the intersection lights. The details of the orthogonal sets of strips, covered by phosphor, can be seen in Figure 10. The brightness was designed to be about 2- to 3-foot lamberts, but could as well be 5- to 10 fL. The brightness of each dot was about the same when lit, varying no more than 20%. This was adequate to excite a photocell. Some crosstalk is evident on the other lamps on the X and Y axis being energized as a result of capacitive coupling. In a square panel the other lamps in the lines energized see a voltage one-half that of the lamp at the intersection and therefore are about one-fifth as bright. If the pattern becomes rectangular, the crosstalk increases on the shorter line and decreases on the longer. In the case of the two 12" x 18" sections of the Address Panel, the brightness ratios were 3.5:1 and 7:1. Studies have shown that brightness varies with voltage, as shown in Figure 11. As the dielectric is operated closer to rated voltage the relative crosstalk decreases.

A 3" x 3" corner section of the Address Panel was built to demonstrate a simplified manner of making connections to it, as shown in Figure 12. This photograph was taken with excitation voltage applied at X=3, Y=13; the bright spot at this coordinate and the correspondingly lower brightness along the Y=13 and Y=3 lines is clearly shown. This panel was very successful and is probably one of the largest EL X-Y panels ever built. There is no reason why considerably larger Address Panels cannot be made using the same techniques.



**Figure 10 CORNER DETAIL OF 18" X 24" TWO-SECTION ADDRESS
PANEL SHOWING CROSS-STRIP AND CONNECTION TABS**

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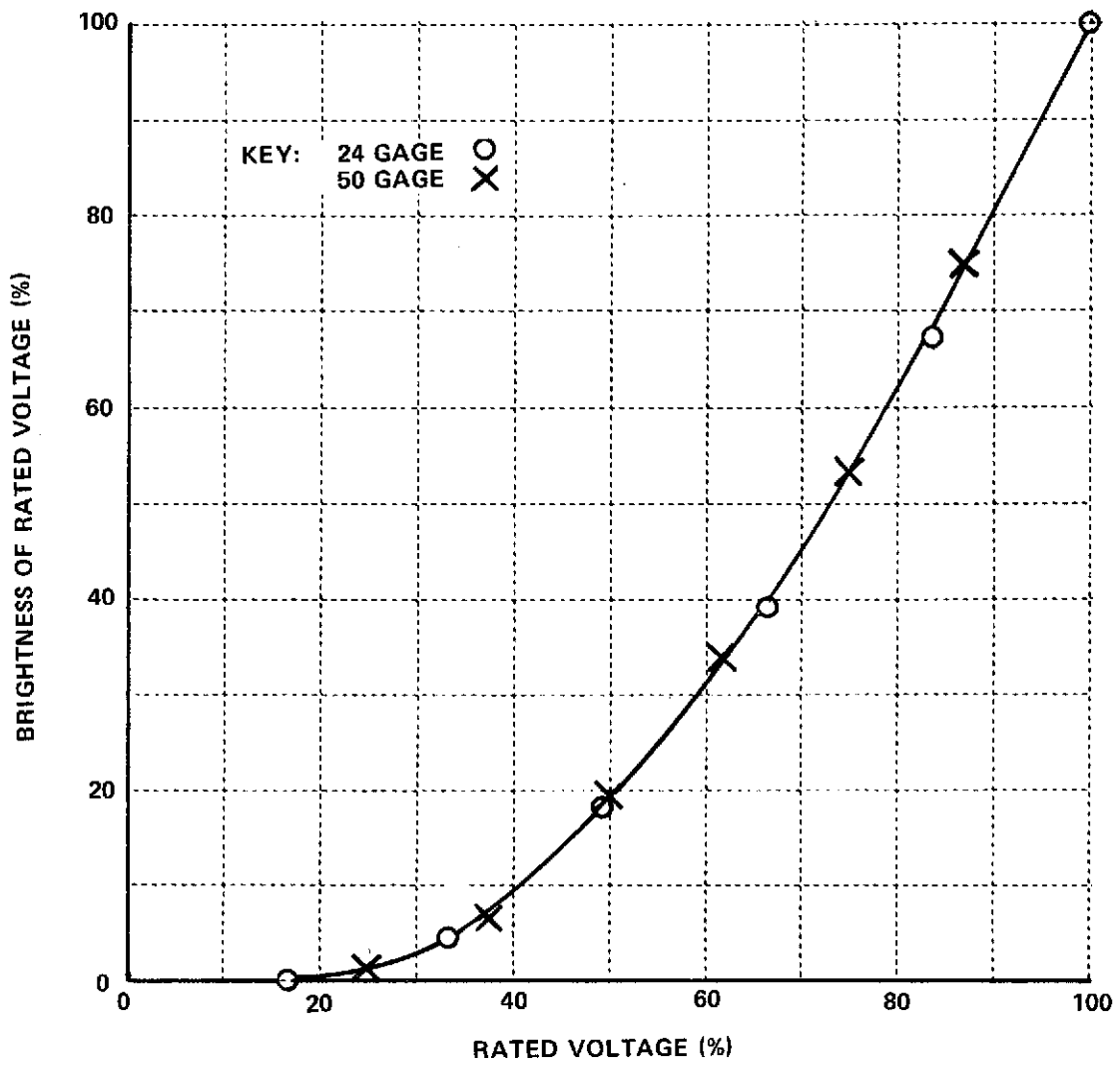
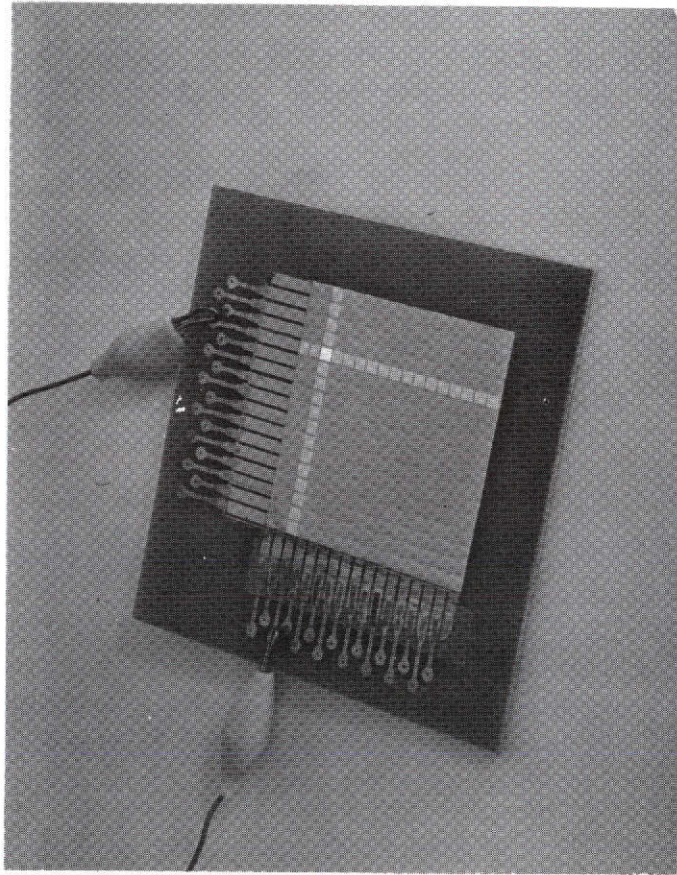


Figure 11 PERCENT OF BRIGHTNESS VS PERCENT OF RATED VOLTAGE



**Figure 12 CORNER SECTION OF CROSS-STRIP ADDRESS PANEL
WITH EXCITATION AT $X = 3$ AND $Y = 13$**

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III. EXPERIMENTAL EL-PC DISPLAY PANEL HAVING MEMORY

To prove the concept of the electroluminescent-photoconductor (EL-PC) latching principle, a large experimental working model of a single cell was constructed. The operating principle is as follows: Figure 13 shows one element of a simple latching, or memory, structure composed of a trigger cell EL_1 optically coupled to a photoconductor R. Latching cell EL_2 (also optically coupled to R) is connected in parallel with Display cell EL_3 . The enclosed portions of the schematic indicates that EL, R and EL_2 are shielded optically from the outside ambient light. Only Display cell EL is exposed externally. Operation of the latching structure according to Figure 13 is as follows:

When the Address cell EL_1 is off, the greater part of voltage appears across the high resistance of photoconductor R. Hence, the output cells EL_2 and EL_3 are held below the threshold of visible light. When a trigger pulse of proper amplitude is applied to EL_1 , the radiation thus generated impinges on photoconductor R causing its resistance to change from a high to low value. Simultaneously, the larger fraction of the display voltage is shifted across EL_2 , causing it to radiate. When the light from the triggering cell is extinguished, the low resistance state will be maintained providing a latching action as long as excitation voltage is applied. EL_3 provides an external indication of the display. In a latching structure such as shown in Figure 11, it is necessary to remove the display excitation voltage for erasure; in this case, if they are connected in parallel across a common supply, all of the display elements will be erased simultaneously. However, the cells could be erased individually if separate excitation leads were connected to each one.

This experimental model successfully demonstrated the concept of a latching EL-PC. Photographs of this model are shown in Figures 14 and 15.

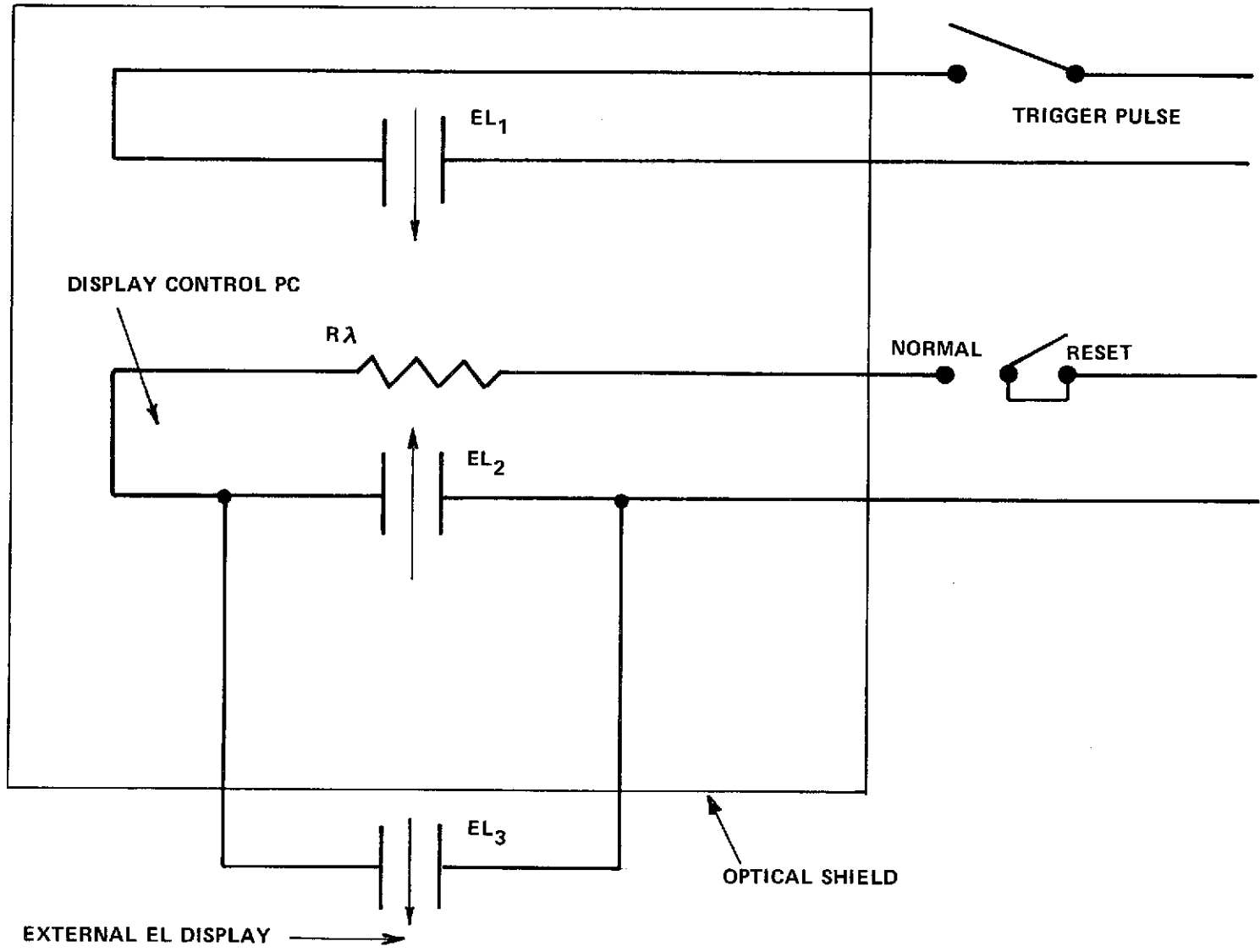


Figure 13 EXPERIMENTAL ELECTROLUMINESCENT PC LATCHING UNIT

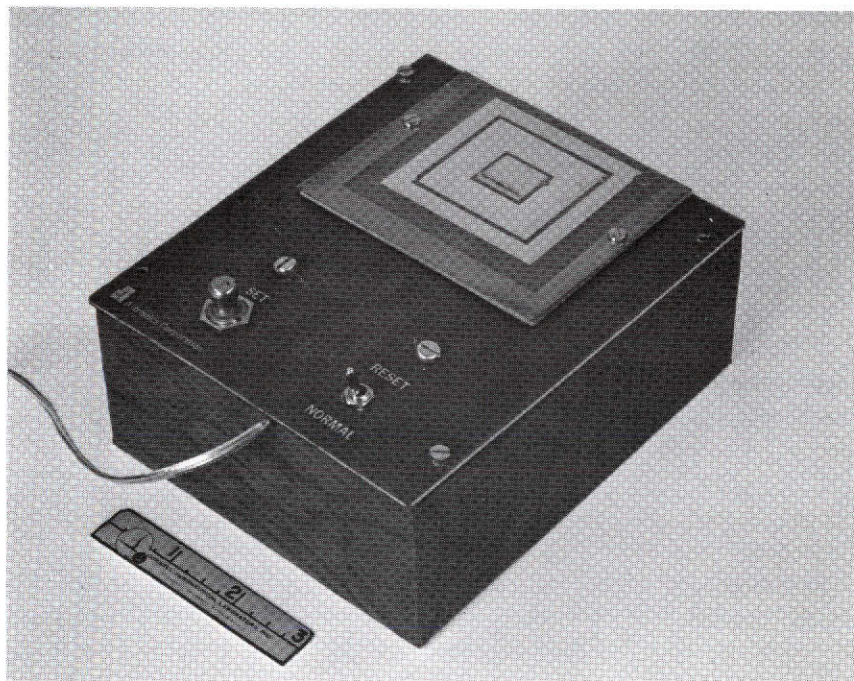
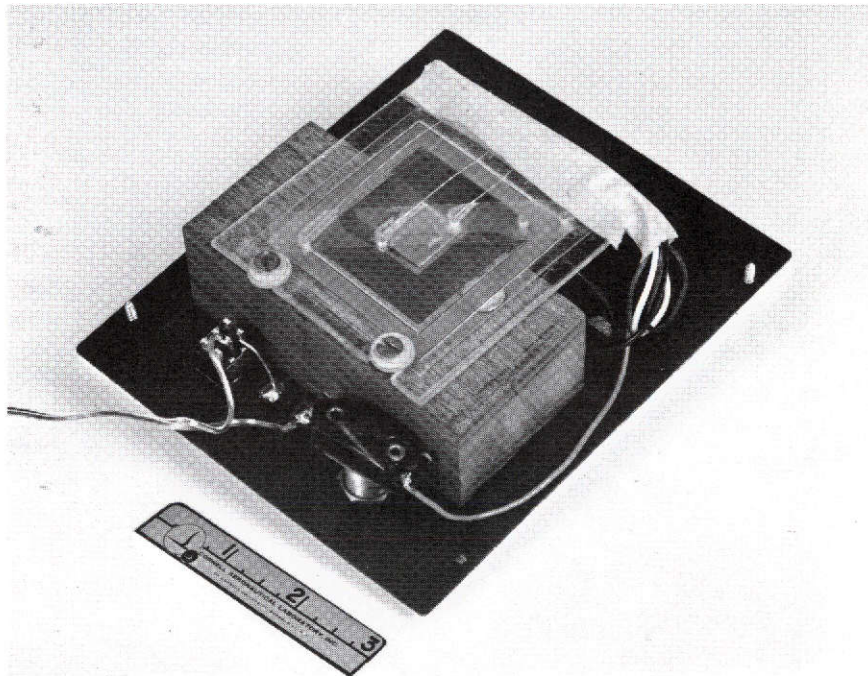


Figure 14 SINGLE CELL ELECTROLUMINESCENT LATCHING UNIT

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**Figure 15 REAR VIEW OF ELECTROLUMINESCENT
LATCHING UNIT WITH CASE REMOVED**

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A major effort was made to construct a matrix of EL-PC cells located on 0.100 inch centers. Most of this effort was directed toward depositing a photoconductor on the dot areas on the Display Panel. As was the original Address Panel, this was a complicated "interdigital" structure with its attendant problems. The photoconductors employed were formulations of cadmium selenide (CdSe) in a photosensitive binder (KPR-KMER). Many units were processed to check photosensitivity in the presence of EL radiation. Initially, Mylar (Polyester) substrates were used for the photoconductor tests. The sensitivity (change in resistivity) of the photoconductive (PC) layers was not great enough with the original level of EL brightness produced by the Address Panel. It appeared that the plastic-bound CdSe material suffered from poor particle-to-particle contact. In order to solve the PC particle contact problem, test layers of CdSe were applied on glass substrates and sintered in a furnace at 500° C for 15 minutes. Sintering the PC material improved the dark-to-light resistance markedly, enough to control the EL from threshold to a substantial brightness. It was therefore decided to use glass for the EL-PC substrate. However, sintered CdSe photocells were degraded in sensitivity when left unprotected. A considerable amount of sensitivity was still lost even when the CdSe layer was coated with a resin. Corning "micro-glass" was tried as the substrate for EL-PC memory display panels. The thin glass (about 0.02 inch thick) distorted under the high sintering temperatures necessary for processing the photoconductor layer. It was then decided to employ a thicker, Pyrex glass panel, cut to size by the vendor. In no case was uniformity of life of the photoconductive formulation deemed to be adequate. It was reluctantly concluded that, at this time, we were unable to successfully fabricate an EL-PC Display Panel with latch-in memory.

IV. ALTERNATE LATCHING MEMORY INVESTIGATION

Several alternate latching memories were considered. First, was a magneta-mechanical latching matrix in which an iron core was circled by two small wire coils (Figure 16), one addressed by energization in the X direction and one in the Y. When both were energized, a conductive rubber piece attached to a flapper was repelled upward where it magnetically latched to the back electrode of an ASTRONICS EL dot (Figure 17). Reverse polarity on the coils would unlatch the flapper. Construction of the device was difficult in even relatively large size and impractical when considering 43,200 dots on 0.100 inch centers, and driving impedance and current would have required additional decoding system development.

A second approach contemplated a piston driven by two coils which would replace the flapper. A model for 3 x 3 element line representation was constructed, as shown in Figure 18. Again, the manufacturing and reliability of such a device ruled it out.

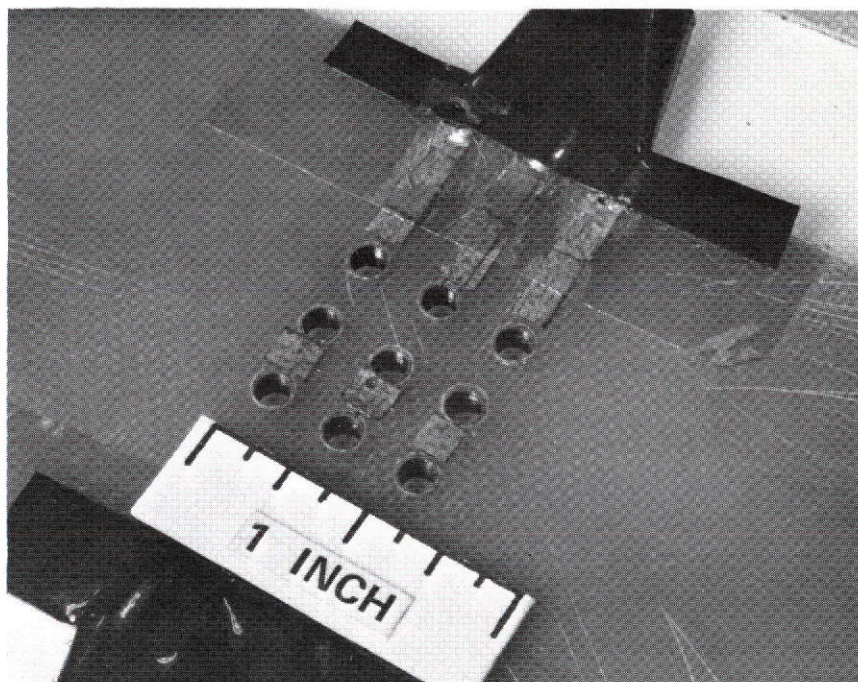


Figure 16 COILS FOR MAGNETIC LATCHING MATRIX

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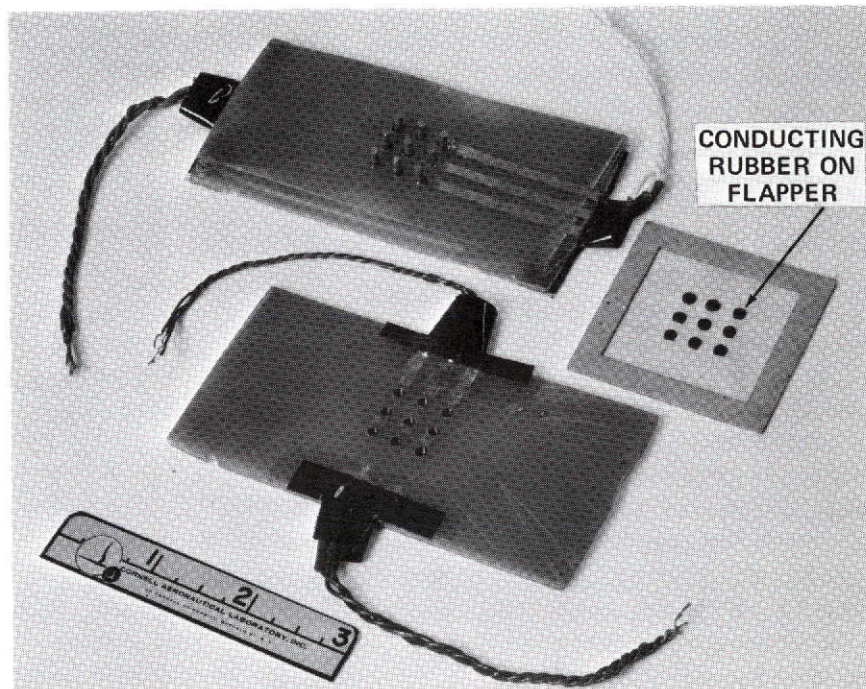


Figure 17 MAGNETIC LATCHING MATRIX

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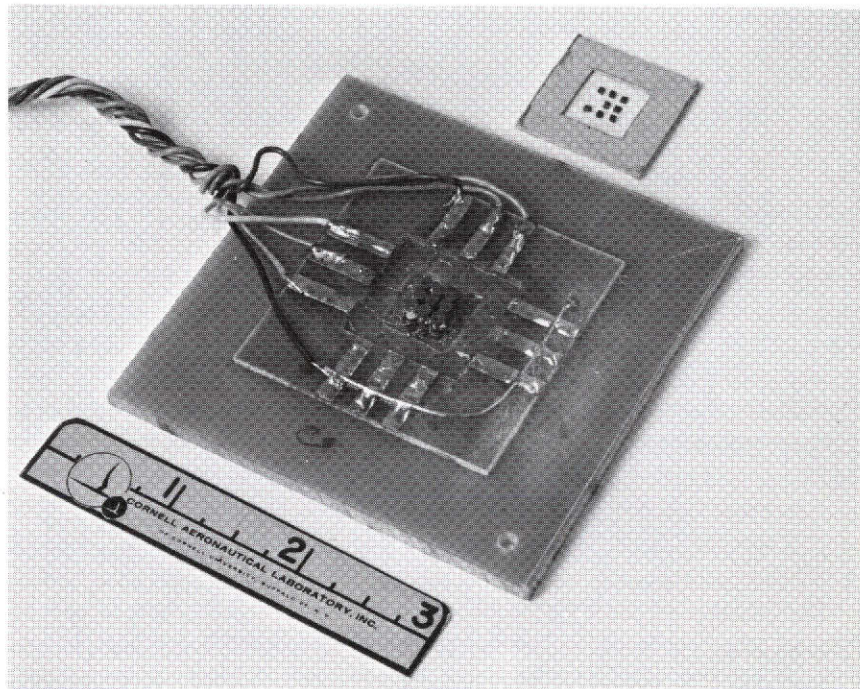


Figure 18 MAGNETIC PISTON LATCHING MATRIX

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V. CONCLUSIONS

The concept of a multifunctional Display based upon an EL-PC structure to provide an internal memory appears to be sound. As originally stated, the successful operation of such a Display requires that each component function correctly. Therefore, the conclusions reached from this project are stated in terms of the three major components.

1. The Decoder demonstrates that an EL binary input can actuate photocells to produce an output signal for an X-Y matrix. For a large matrix it may be an economically attractive approach.
2. The EL Address Panel required to cause the individual EL-PC Display point to light and latch was markedly advanced by this project and the Address Panel problem essentially solved. A large panel having many individual EL dots has been made using the ASTRONICS' EL design. This has "crosstalk" of only 20%, which gives a wide threshold for addressing an EL-PC Display Panel.
3. The Display Panel with latch-in memory has been successfully demonstrated in a single latching cell where sufficient area was available to use a discrete photocell. The attempt to fabricate an EL-PC Display Panel on 0.100 inch centers was beyond our capability and we believe beyond the state-of-the-art. It should be possible, eventually, to fabricate such a structure.

Several additional important conclusions can be reached. EL lamps provide an ideal method of constructing a display. The ASTRONICS' EL provides many opportunities for matrix design, including dots on small center distances and the ability to economically replace the entire lamp. Further, a Display contemplating these many individual dots must be a static device, as a mechanical approach requires too many individual parts. In this case, a 1% incorrect operation could show 400 dots illuminated incorrectly.

THE FOLLOWING PAGES ARE DUPLICATES OF
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A DIFFERENT METHOD TO PROVIDE BETTER DETAIL