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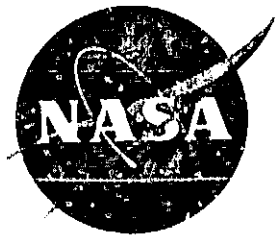
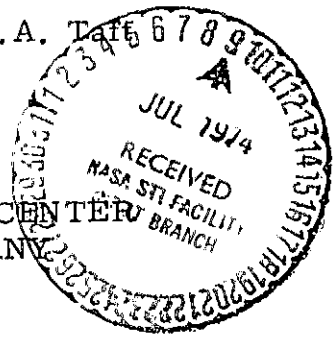


DEVELOPMENT AND FABRICATION OF IMPROVED SCHOTTKY POWER DIODES

by

L. F. Cordes, M. Garfinkel, and E. A. Taft

RESEARCH AND DEVELOPMENT CENTER
GENERAL ELECTRIC COMPANY



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16. Abstract

Reproducible methods for the fabrication of silicon Schottky diodes have been developed for the metals tungsten, aluminum, conventional platinum silicide and low temperature platinum silicide. Barrier heights and barrier lowering have been measured permitting the accurate prediction of ideal forward and reverse diode performance. Processing procedures have been developed which permit the fabrication of large area (~1 cm^2) mesa-geometry power Schottky diodes with forward and reverse characteristics that approach theoretical values.

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Section 1

INTRODUCTION AND SUMMARY

Schottky diodes have long been attractive for high power applications by virtue of their reduced power loss in forward conduction and their rapid recovery time compared with p-n junction rectifiers. These virtues are balanced by the disadvantages of greater reverse leakage current, lower reverse bias breakdown voltage, and far greater variability in electrical characteristics due to processing problems. Severe compromises must thus be made in balancing forward drop against reverse leakage current and voltage. The dominant material parameter determining both forward drop and reverse leakages is φ_b, the metal-silicon Schottky barrier height. Notwithstanding this, reliable data for the barrier heights of various metals against silicon, obtained from well characterized metal-silicon interfaces fabricated by a reproducible process, have not hitherto been available, with but a few exceptions. The basic data required to make the design compromises needed for optimum Schottky rectifier design have thus not been available. The reason for this is the same as for the variability in Si Schottky diode electrical characteristics--the great difficulty in removing the last fraction of a monolayer of native SiO_2 inevitably present upon a silicon surface and getting intimate, direct, contact between the barrier metal and the silicon.

Phase I of the present effort comprised the acquisition of the barrier data and processing parameters required to design the diode of the contract specifications. Phase II was concerned with the actual fabrication and testing of devices built applying the technology and following the design of Phase I.

Our efforts were focused upon the contract specification goals. These were (a) Reverse D.C. blocking capability of 200 volts, (b) 0.6 volt max forward drop at 25 amp forward D.C. current, (c) maximum reverse leakage of 50 ma at 100°C, and (d) 50 nsec reverse recovery time.

We have developed reproducible methods for the fabricating of Schottky diodes for the metals tungsten, aluminum, conventional platinum-silicide and low temperature platinum silicide. We have measured barrier heights and barrier lowering for these materials thereby allowing us to predict accurately the reverse junction leakage and the ideal forward characteristics for any specific diode design. We have, further, developed a processing procedure which results in high-yield fabrication of large area mesa geometry Schottky diodes with reverse breakdown capability that is upwards of 50% of theoretical values. We have, in brief, generated the baseline data--ideal material parameters; processing sequences; and knowledge of practical limits--that are required for the design and fabrication of high power-high voltage Schottky diode wafers. Additional effort is required in assembly procedures.

Section 2

INTRODUCTORY TECHNICAL DISCUSSION

2.1 General Characteristics of Schottky Diodes

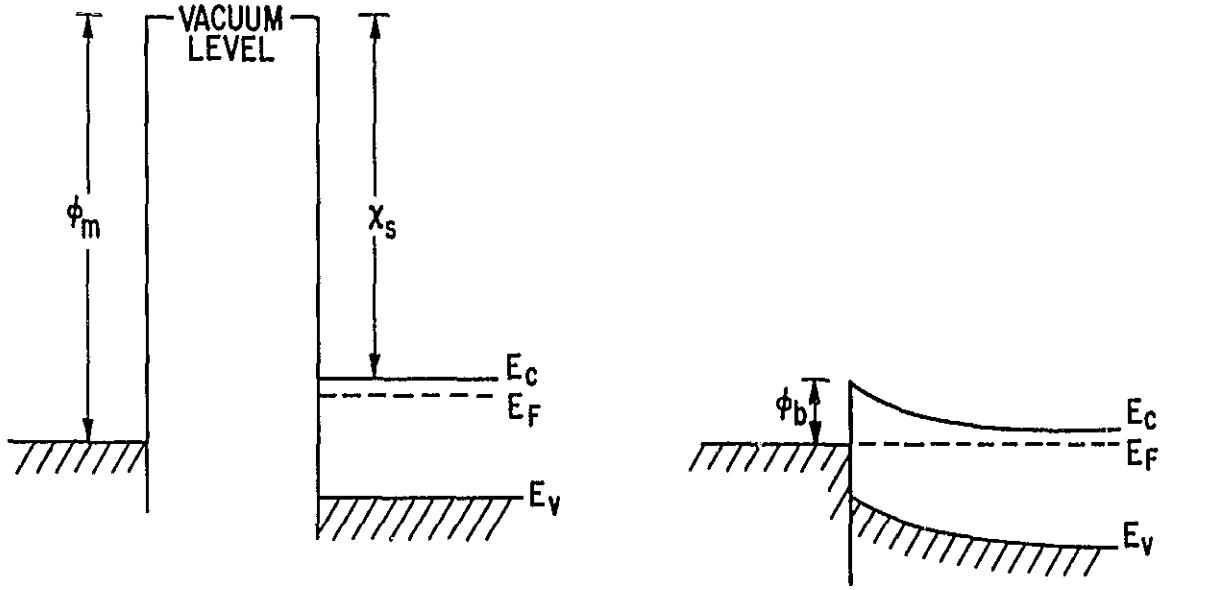
In order to provide a framework for discussion, it will be beneficial to consider some of the basic physics of metal-semiconductor contacts. Whenever a metal contacts silicon, a potential barrier is formed between the two. The situation for n-type Si is illustrated schematically in Fig. 1. In the Schottky theory of barrier formation, [1, 2]

$$\varphi_b = \varphi_m - \chi_s \tag{1}$$

where φ_m is the metallic work function and χ_s is the electron affinity of the Si. A second model of barrier formation, due to Bardeen, [3] gives

$$\varphi_b = \varphi_g - \varphi_0 \tag{2}$$

where φ_g is the Si energy gap and φ_0 is the energy of the highest filled surface states, measured with respect to the top of the valence band at the surface.



(a) METAL- SEMICONDUCTOR BARRIER PRIOR TO CONTACT.

(b) METAL- SEMICONDUCTOR BARRIER, AFTER CONTACT AND IN THERMAL EQUILIBRIUM.

Fig. 1 Metal-semiconductor interface before and after contact formation.

Experimental data[4, 5] seem to indicate that the true barrier height lies somewhere between the values predicted by (1) and (2).

In general, the current-voltage characteristic of a Schottky diode is represented by

$$J = J_s \left[\exp \left(\frac{e(V-IR)}{nkT} \right) - 1 \right] \tag{3}$$

where V is the applied voltage, I is the total current, R is the sum of all series resistances in the device, n is a " slope" factor which indicates a deviation from " ideality" in a given device, and J_s is the " saturated emission current" given by

$$J_s = A^* T^2 \exp \left[- \frac{e\varphi_b}{kT} \right] \tag{4}$$

where A^* is the effective Richardson constant and φ_b is the barrier height. Equations (3) and (4) assume that thermionic emission over the barrier is the dominant transport mechanism and the deviation of n from unity is a measure of the departure from this assumption. It is seen from (3) that large values of n will be responsible for excessive voltage drops in the forward direction, as well as large values of R.

Although (3) and (4) accurately describe most forward characteristics, reverse leakages in excess of that predicted by (3), i.e., $J > J_s$ are frequently observed, particularly at high values of reverse bias. This effect is due to three separate sources. The first of these sources is the presence of a generation-recombination current. The second contribution to the " excess" reverse leakage is due to an image lowering of the barrier at high fields[6] and the value of φ_b used in (4) should be modified to $\varphi_b - \Delta\varphi_b$ where $\Delta\varphi_b$ is given by[7]

$$\Delta\varphi_b = \left(\frac{q\mathcal{E}_m}{4\pi\epsilon_s} \right)^{1/2} + \alpha\mathcal{E}_m \tag{5}$$

where $\mathcal{E}_m$ is the maximum electric field existing at the metal-semiconductor interface, ϵ_s is the dielectric permittivity of the semiconductor, and α is an empirical parameter. Unfortunately, the $\alpha\mathcal{E}_m$ term in (5) is not always negligible and therefore it is not possible to calculate the barrier lowering accurately. Since the " excess" device leakage current depends exponentially on $\Delta\varphi_b$, it becomes necessary to make a precise measurement of $\Delta\varphi_b$ in order to specify the leakage current for a given device design. A third contribution to the " excess" reverse current may arise from surface leakage currents.

2.2 Experimental Determination of Schottky Diode Parameters

These preceding considerations show that the important parameters in Schottky diode design are φ_b, n and if high reverse voltages (V_r) are required, a knowledge of $\Delta\varphi(V_r)$ is also required. Of these, n is most easily obtained. From (3) it is seen that n can be obtained from the slope of a log J vs (V-IR) plot for $eV > \sim 3nkT$. J_s can be obtained from the zero voltage intercept of the same plot, and can then be used to calculate φ_b, using (4). There may be some doubt as to the correct value of A* to be used,[8, 9] but the value of φ_b determined in this manner, is not particularly sensitive to the value of A* used. A second method of determining φ_b is from a measurement of depletion capacitance vs reverse bias.[10] This method also yields the value of N_d (or N_a) the density of donors (acceptors) in the semiconductor. A final method of determining φ_b is by photoemission over the barrier.[11] With this method, the interface is illuminated through the Si, and the zero current intercept of the extrapolated photocurrent (into the Si) vs photon energy plot gives the barrier height. Illumination through the Si is possible because the barrier heights are less than the band gap of Si. It is desirable to measure φ_b by several methods on the same device. Any significant variation in the value determined by the independent measurements is an indication of a faulty measurement, or the presence of complicating factors (such as a nonintimate metal-Si contact) in the interface regions. Whatever the cause of these complicating factors, the result is to produce an essentially noncharacterizable device and thus all measurements made on such a device are to be distrusted.

Of the three parameters discussed, the measurement of $\Delta\varphi_b(V_r)$ is by far the most difficult. It is possible to make photo-measurements as a function of reverse bias and thus obtain $\Delta\varphi_b(V_r)$, but for large values of V_r, the presence of a large thermionic current over the barrier so dominates the photo current that even ac measurement techniques are often unreliable. The problem is further compounded if a measurement of $\Delta\varphi_b(V_r)$ is attempted at elevated temperatures.

A second method of obtaining $\Delta\varphi_b(V_r)$ is to measure the reverse leakage current as a function of reverse bias. The "excess" leakage current can then be used to obtain $\Delta\varphi_b$ using Eq. (4). Although this is a relatively quick and simple measurement it is somewhat unreliable since the implicit assumption is made that all the reverse leakage current is due to thermionic current over the barrier. The presence of other contributions to the reverse leakage current will lead to erroneously high values of $\Delta\varphi_b(V_r)$.

A third method of determining $\Delta\varphi_b(V_r)$ involves measurement of the reverse leakage current (I_r) at a fixed value of reverse bias as a function of junction (contact) temperature. The slope of a plot of log I_r vs $1/T$ will then give φ_b at the given value of reverse bias. A complete knowledge of $\Delta\varphi_b(V_r)$ requires measurement of I_r as a function of temperature at a series of reverse bias values. Care must be taken to insure that the junction temperature is measured accurately. Once again the assumption is made that all of the reverse

current is due to thermionic current over the barrier. However, with this method the validity of that assumption can be checked, since the presence of other contributions to the reverse current will in general produce a nonlinear log I_r vs $1/T$ plot. This can then be used as an indication that a false value of $\Delta\varphi_b$ has been measured.

2.3 Reverse Breakdown Considerations

Under reverse bias conditions, the Schottky barrier supports the external voltage in a way quite similar to a p-n junction under similar conditions. In the underlying silicon, a depletion region is formed from which essentially all mobile charge is removed leaving the ionized impurities to create a space-charge region. The resulting electric field supports the applied voltage. The numerical values of resistivity and thickness of depletion layer encountered in Schottky rectifier design are quite comparable to those found in p-n junction rectifiers. Figure 2 illustrates the design of such blocking layers.[11] Here we have plotted a family of curves showing the relationship between resistivity and depletion layer thickness for various choices of breakdown voltage.

Figure 2 applies for designs in which the depletion layer is considered to be plane parallel. If, however, the depletion layer takes the shape normally associated with a planar junction, then the curves of Fig. 3 must be used.[12] Here we see that for a hemispherical approximation to a planar junction the curvature, because of the increased field intensity, causes the breakdown

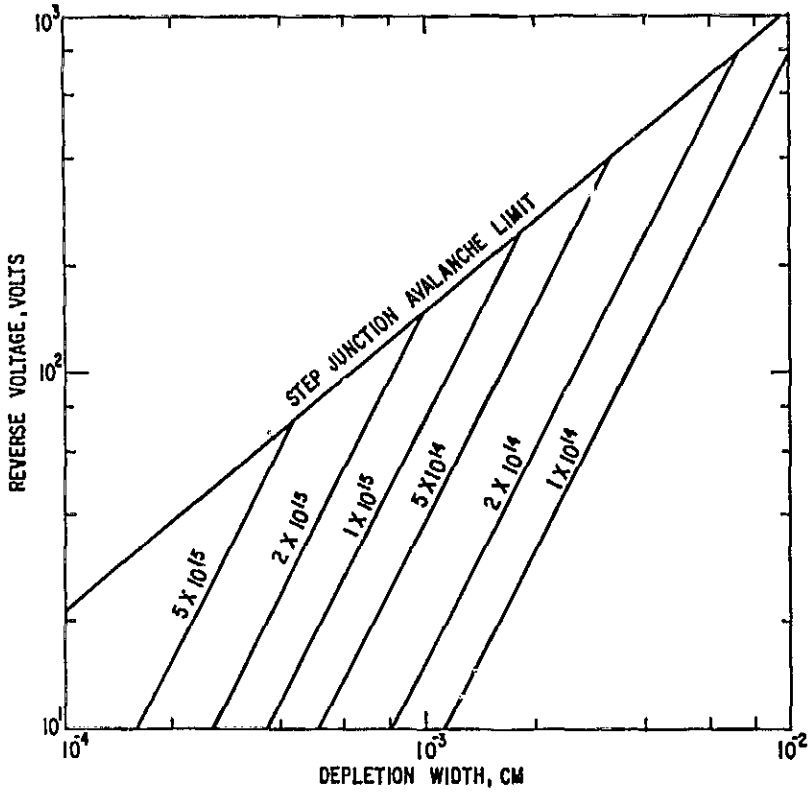


Fig. 2 Voltage variation of depletion width and avalanche breakdown voltage for ideal planar step junction.

voltage for the junction to be lower than it would be otherwise. Theoretically, it is possible to make planar junctions of reasonable dimensions up to about 1000 volts breakdown. More frequently one uses the planar technique for lower voltage applications.

The effect of junction or depletion layer curvature becomes increasingly significant as the radius of the curved portion becomes smaller, as Fig. 3 illustrates. In Schottky barrier devices this difficulty becomes acute because the effective radius of the depletion layer near the edges of the Schottky metal layer becomes very small indeed. The electric field, therefore, is greatly enhanced and may exceed the avalanche field intensity of silicon (see Fig. 4). This difficulty can be avoided by providing a diffused guard ring region under the periphery of the metal-semiconductor interface as is illustrated in Fig. 5. In effect, a junction diode is placed in parallel with the Schottky diode. It does not contribute in any important way to forward conducting characteristics because the on-state voltage drop of the Schottky diode is less than that of the junction diode. In the reverse direction, however, this diffused region acts to increase the radius of curvature of the depletion layer at the place where, without its presence, the radius would be very small. A significant reduction in electric field is thus accomplished and the reverse characteristics of the diodes so made are considerably improved.

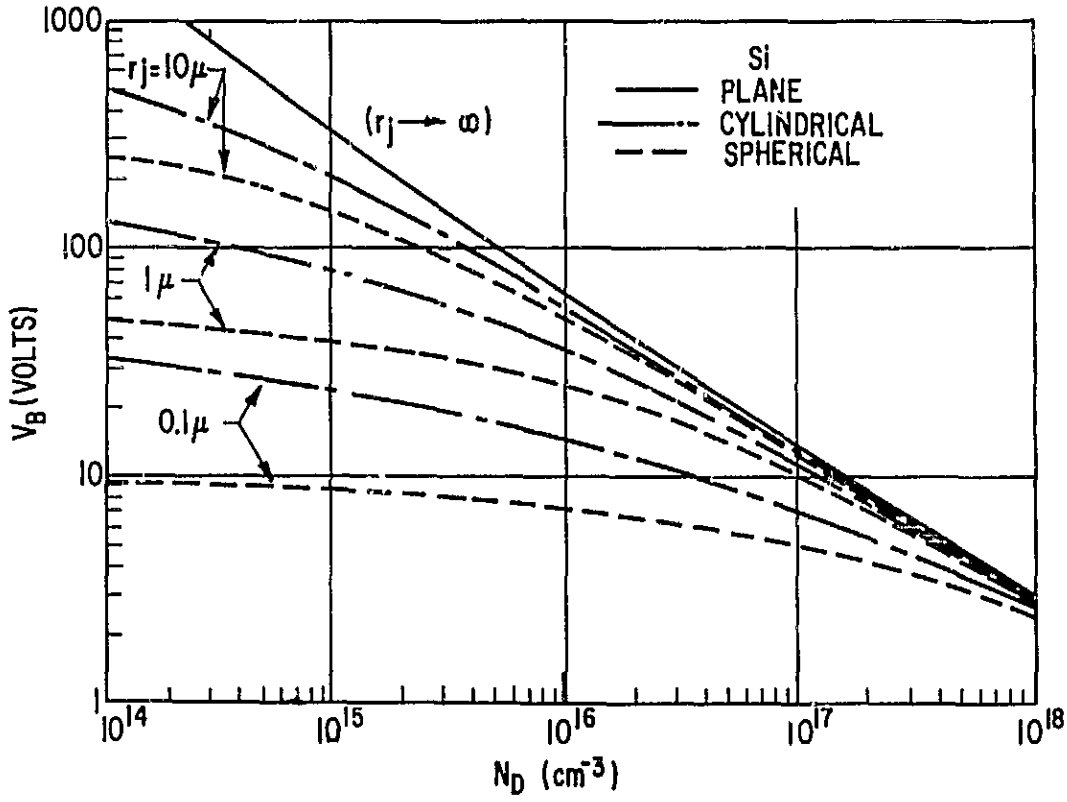


Fig. 3 The effects of junction curvature upon avalanche breakdown voltage.

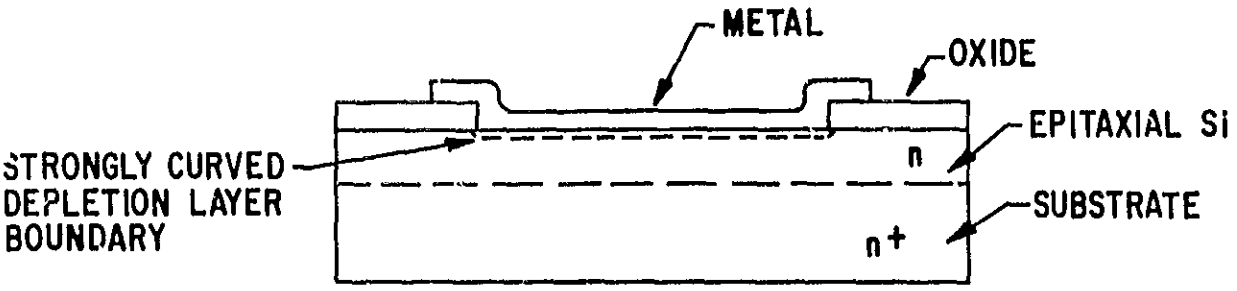


Fig. 4 Idealized simple planar Schottky diode structure.

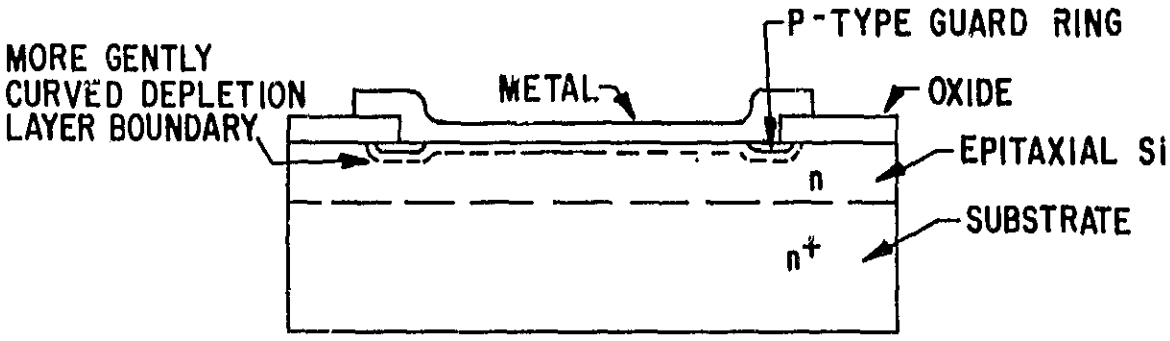


Fig. 5 Schottky diode with p-n junction guard ring.

A similar effect can be obtained by use of the MOS effect as illustrated in the device of Fig. 6. Here the oxide surrounding the metal-semiconductor contact is made of an appropriate thickness so that under reverse bias conditions inversion of the surface of the silicon can occur and the depletion layer is thus extended laterally beyond the region of Schottky action. By properly shaping the oxide near the edge of the contact, this action can spread the depletion layer across the surface much more rapidly than it spreads vertically away from the surface and low surface electric field can be maintained. This technique is difficult to implement in practice, however, because the detailed shape of the oxide edge at the boundary of the Schottky metallization is crucial.

Still another approach to reducing the surface field[13] of the edge of the Schottky junction is illustrated in Fig. 7. This technique applies principally to power Schottky devices where the dimensions of the device permit beveling of the edge of the pellet without requiring a large increase in the area of the silicon pellet. This technique is directly analogous to that used in many p-n junction diodes where reduced surface electric fields are provided by properly shaping the edge of the silicon pellet.

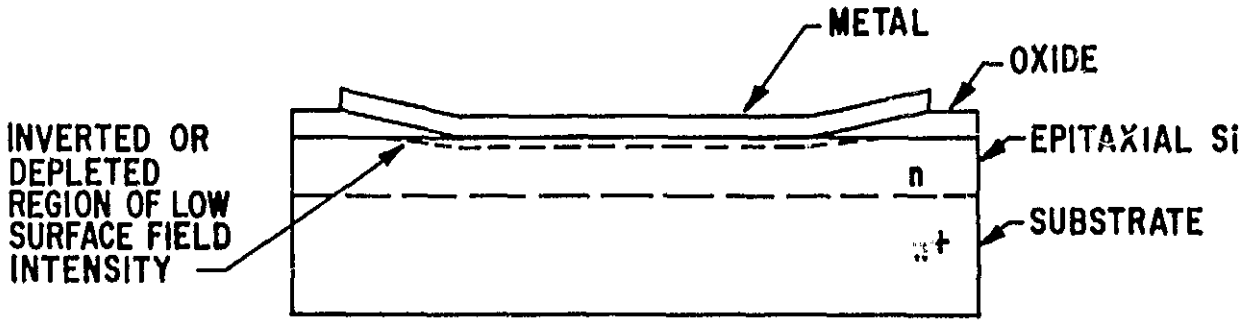


Fig. 6 Schottky diode with beveled oxide to reduce field concentration.

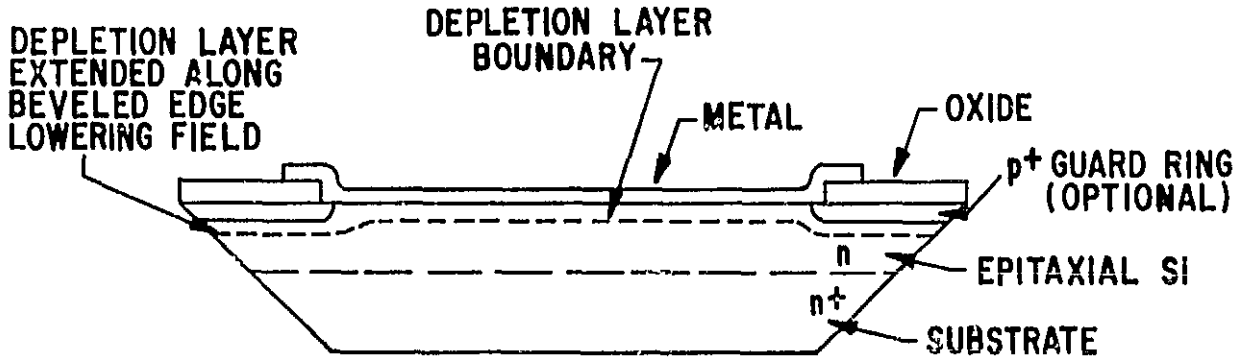


Fig. 7 Schottky diode with both p+ guard ring and edge beveling.

Yet another approach to reducing the surface field at the edge relies on forming the contact on a "mesa" as is shown in Fig. 8. This method incorporates some of the features of the MOS technique and the beveling technique in a manner which offers great advantages in terms of device fabrication. The extension of the metallization over the oxide, combined with the "mesa" shape, results in the equipotentials in the Si being displaced away from metal-Si contact edge rather than "crowding" toward it as is the case illustrated in Fig. 4. This results in a decrease rather than an enhancement of the electric field at the contact edge. It is true that the field is enhanced at the edge of the metallization, but this edge is over the oxide which is easily capable of supporting the increased electric field there. This technique has a further advantage over the guard ring approach in that it eliminates several process steps (cutting the guard ring in the oxide, diffusing the guard ring, and etching the Si to minimize the series drop as is discussed in Sec. 2.5.2).

All of the above techniques, whether singly, or in combination, can be employed to minimize the concentration of electric fields at the perimeter of the Schottky metal-semiconductor interface region and thus provide suitable low current reverse blocking characteristics. The influence of surface impurities is also much reduced in this way.

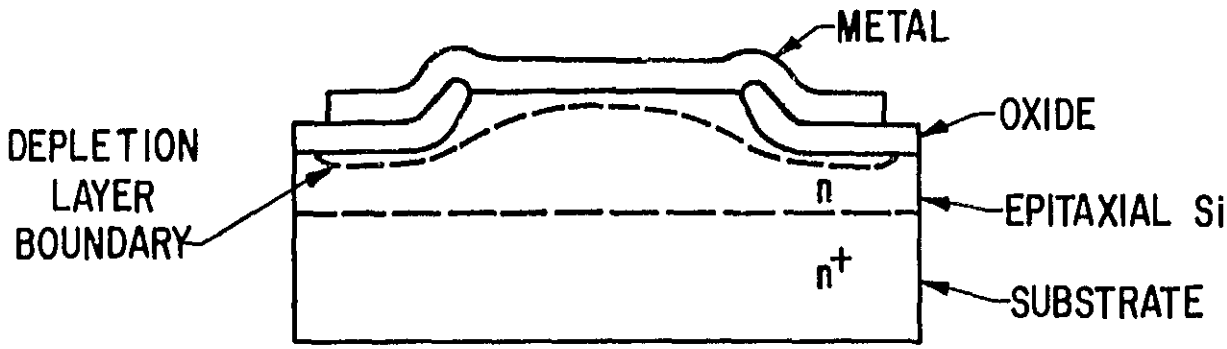


Fig. 8 Mesa Schottky diode.

It was our opinion at the outset of the contract effort that the mesa geometry represented the best approach to meeting the contract goals. Most important, this approach affords a way to fabricate a power Schottky diode with the minimum possible series resistance. The reason for this is that the breakdown voltage observed with this structure is that for a planar device, since the field is reduced rather than enhanced at the contact edges. Thus the required Si resistivity for a given breakdown voltage is the minimum possible value, and is determined solely by the required breakdown voltage, and not by the radius of curvature of the guard ring junction. In addition, the fact that there is no deep guard ring diffusion implies that the required thickness of the epitaxial layer is just equal to the depletion width at breakdown, as given by the curves in Fig. 2. This means that the minimum possible epitaxial thickness can be employed, without using the acid etching technique to reduce thickness described by Heymann and Petruzella.[14] Since the series resistance of a Schottky diode is proportional to the product of the epitaxial thickness and resistivity, the mesa geometry offers the theoretical minimum series resistance for a given breakdown voltage, and presents the designer with the opportunity to achieve the nearest approach possible to ideal forward characteristics.

2.4 Effect of Barrier Height on Schottky Diode Performance

Most carefully done metal depositions on good quality, clean Si with proper contact geometry result in n values [in (3)] between 1.0 and 1.1, and thus n is not of primary importance in determining device performance. Because of the exponential dependence of J_S on φ_b, φ_b is by far the most important factor in determining diode performance. This fact is evident from the results of Heymann and Petruzella,[14] who noted that with W-Si Schottky diodes ($\varphi_b \approx 0.67$ eV), they could easily meet the required 25A at 0.5V forward condition (I > 30A at 0.5V was obtained) but failed to meet the 100 ma at 100V reverse leakage criterion at 100°C. They also noted that using conventional PtSi-Si Schottky diodes ($\varphi_b \approx 0.85$ eV), they could easily meet the required reverse leakages at 100°C ($I_r < 0.4$ ma was obtained) but that with these devices they experienced difficulty meeting the forward requirements. From these observations it is

clear that the ideal device would employ a barrier intermediate to that of W and conventional PtSi. This would allow one to "trade" some of the "excess" forward current capability for reverse leakage at 100°C.

In concluding their report, Heymann and Petruzella[14] suggest that the limitation of the conventional PtSi-Si guard ring structure has been reached. They state that:

> "A forward voltage drop of 0.5 V for a 100°C Schottky device with blocking capability of 100V or higher would always be a problem regardless of size due to the inherent high voltage of the barrier required. In the case of (conventional) platinum silicide, the barrier voltage is about 0.4 volt for a 100 volt device. When the voltage due to solders and contacts of about 0.1 volt is added, the desired limit of the forward voltage is reached without even considering the resistive drop in the silicon."

These considerations make it clear that a continuous range of φ_b values between W (0.67 eV) and conventional PtSi (0.85 eV) would be desirable in order to provide for the optimum Schottky design over a wide range of reverse voltages and temperatures. Obviously such a continuous range is not physically possible, but our research at GE Corporate Research and Development has provided a number of acceptable contact materials and deposition processes which span this desired range and provide us with a unique capability for Schottky diode design and fabrication. These materials and processes are discussed in Sections 2.5.4 and 2.6.

2.5 Effect of Silicon Properties on Schottky Diode Performance

2.5.1 Effect of Minority Carrier Lifetime

Certain material properties which affect the forward voltage characteristics of conventional junction rectifiers have much less significance when considering design of Schottky devices. The minority carrier lifetime, for example, which affects the forward conducting voltage drop of a p-n junction diode due to its influence on the diffusion length of minority carriers, has relatively little effect on the forward characteristics of a Schottky diode. Of course, in the reverse blocking condition, since recombination centers act as charge generation sites, one would expect similar behavior for both devices; that is, low lifetime material would cause increased space-charge generation current and thus a higher leakage current under reverse bias. But in the forward bias condition, since the Schottky diode is a majority carrier device, recombination and lifetime considerations need not be considered.

2.5.2 Effect of Si Resistivity (doping density) and Carrier Mobility

To take the place of lifetime as a determining factor in the conducting voltage drop, one must take into account the series resistance of the silicon and

other layers used in the device. Conductivity modulation plays an important role in p-n junction rectifiers in reducing the effective series resistance of the silicon layers present in the active areas of the device. In a Schottky diode, however, conductivity modulation plays practically no part. Therefore, a series resistance is encountered in the Schottky diode which may be a significant fraction of the total resistance of the active device. One cannot reduce the series resistance below a certain point, because this implies reducing the resistivity of the silicon under the barrier, and thus reducing the reverse breakdown capability of the device. On the other hand, if the resistivity of the silicon is higher than necessary, the series resistance will be unduly raised, and either the forward conducting drop will rise, or the area of the device would have to be increased to compensate.

One approach toward minimizing the series resistance of a power Schottky diode is that adopted by Heymann and Petruzella, [14] who used epitaxial material and then further thinned the high resistivity Si under the contact to provide a structure with minimum series resistance consistent with the required reverse breakdown specifications. Another approach is the mesa technique discussed in Sec. 2.3.

A second effect of Si resistivity on Schottky diode performance has already been discussed, in Sec. 2.3 (effect of ρ on the reverse breakdown). Two other possible effects of resistivity must also be considered. They are the effect of ρ on barrier height and the effect of ρ on the image lowering of the barrier under high reverse bias. A study has indicated that the barrier height in silicon is independent of doping density over the range 0.15 ohm-cm $< \rho <$ 20 ohm-cm. Since this range includes the resistivities normally employed in Schottky diode fabrication, we may conclude that φ_b is independent of ρ. The dependence of $\Delta\varphi_b$ on ρ results from the dependence of $\mathcal{E}_m$ (Eq. 5) on ρ, and is of the form[7] $\mathcal{E}_m \propto 1/\sqrt{N_d}$.

The carrier mobility does not exert a direct influence on Schottky diode performance. However, it must be remembered that the mobility is a function of doping density, and therefore the usual studies which involve a variation of resistivity also include a variation of mobility as a result.

2.5.3 Effect of Dislocation Density and Surface Defects

One effect of high dislocation density has already been discussed in Sec. 2.5.1. A second, more subtle, effect occurs when etch down processes are employed to minimize the series resistance. Preferential etching may occur at the site of a crystal defect, leading to a reduced epitaxial thickness at that point. A second effect of preferential etching is to create etch pits which give rise to high field points in reverse bias. Both of these effects can significantly reduce the reverse breakdown voltage of a given device. These considerations become more important for large area barriers.

2.5.4 Si Orientation Effects

One area of possible importance which has received little attention is the effect of Si orientation on device performance. The orientation of Si used to fabricate the barrier might be expected to influence three diode parameters, all of which have an influence on J_s, as given by Eq. (4); these are A^*, $\Delta\varphi_b(V_r)$, and φ_b itself. Effects of orientations on A^* have been shown[8] to be small for Si [A^* varies by less than 5 percent from ⟨100⟩ to ⟨111⟩] and since device characteristics are only weakly influenced by the value of A^* this effect is unimportant. Possible effects of orientation on $\Delta\varphi_b(V_r)$ would come through the $\alpha\mathcal{E}_m$ term in (5). This term arises from " the presence of a bound charge distribution near the metal-semiconductor interface" [7] and thus might be sensitive to the detailed atomic arrangement of the Si at the interface.

Such effects are not well understood, and require careful study, because of the profound effect barrier lowering has on reverse leakage currents. Equally important is the effect of orientation on φ_b, and the resultant effect on diode performance as discussed in Sec. 2.4.

Research previously done at GE Corporate Research and Development has indicated that an orientation effect on barrier height does exist and should prove valuable in the design of a wide range of Schottky devices. Our results for Al have been confirmed by Gutknecht and Strutt.[15] Preliminary data showing the barrier heights and orientation effects of the materials we have studied to date are shown in Fig. 9. Figure 9 shows that use of the orientation effect enables us to choose the barrier material and Si orientation which results in the most nearly optimum diode design to meet the required specifications. In Fig. 9 we have plotted two sets of data for PtSi, one labeled " conv." for PtSi contacts formed in a conventional manner, i.e., sputter-depositing 400Å of Pt onto Si, then heating the samples to 600°C for 20 min in a high purity argon atmosphere. The data labeled " low" refer to contacts formed by our low temperature process, described in Sec. 2.6.

The only barrier heights we have listed on Fig. 9 are for those materials for which reliable processes for contact formation exist. We exclude from this list materials and processes which produce diodes with large n values, or result in a large variation of barrier heights from device to device. The principal cause of this variation is the presence of a thin " native" oxide on Si.

2.6 New Barrier Materials

A new technology which we feel provides a significant advantage is the " low temperature" PtSi-Si contact system which we have developed and which, when used in conjunction with the ⟨111⟩ Si orientation provides us with a material having a barrier height of 0.78 eV. Although we do not understand how this material is different from conventionally formed PtSi-Si contacts, we have shown that we can reproducibly form this new contact.

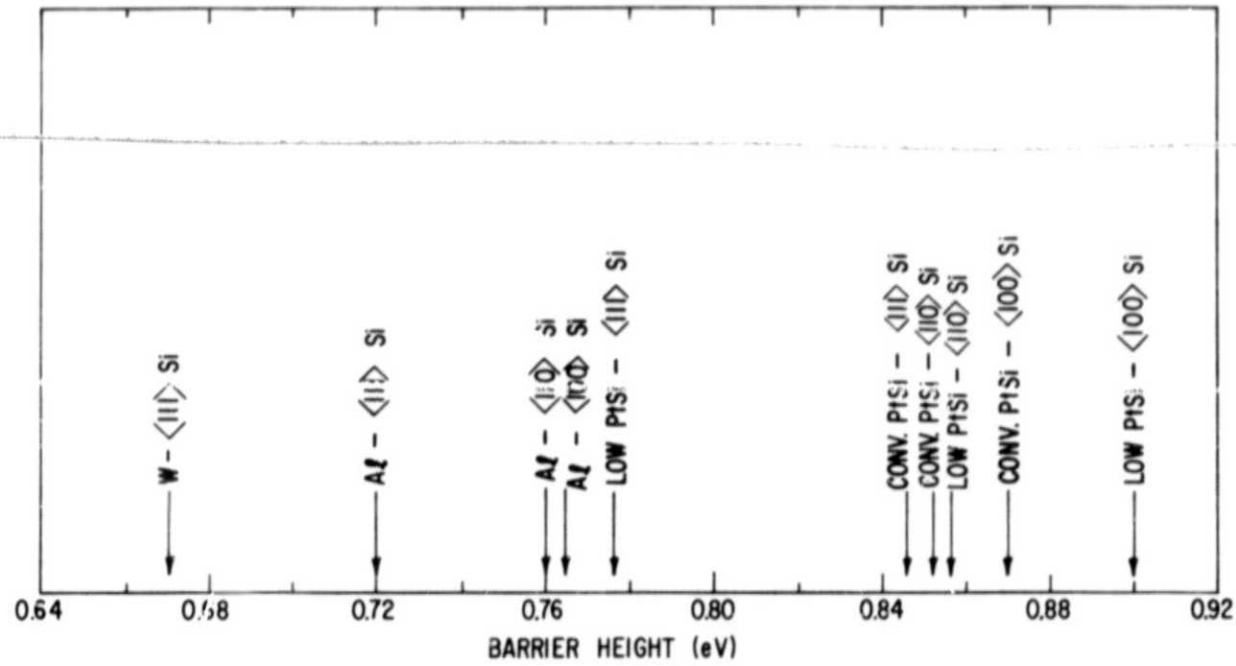


Fig. 9 Barrier heights of W, Al, conventionally formed Pt-Si and low temperature Pt-Si for major n-Si crystallographic orientations.

As discussed in Sec. 2.5.4 PtSi contacts are conventionally formed by sputter depositing Pt onto Si and then heating the wafer in an inert atmosphere to a temperature of approximately 600°C to allow the Pt to react with the Si. In our new process, we sputter deposit the Pt onto a heated Si wafer so that the reaction proceeds simultaneously with deposition. The normal thickness of the deposited Pt layer is 400Å.

Although this new material appears attractive because it offers a barrier height intermediate to that of W and conventional PtSi, two other important factors must be considered before we can accept it as a useful barrier material. The first question one must ask is how reproducibly can this material be formed, and the second is are the n values suitably low to yield high-quality Schottky diodes. Experimental data bearing on these two points will be presented in Sec. 3.

Section 3

ACQUISITION OF BARRIER DATA

One aspect of the program which received a great deal of attention in Phase I was the acquisition of barrier data. These efforts can be conveniently divided into two primary areas: first, the verification of the variation of Schottky barrier height with crystal orientation of the silicon substrate, for several potentially useful barrier materials; and, second, the determination of the magnitude of the barrier lowering under reverse bias for these barrier materials.

3.1 Barrier Height and Quality

As was discussed in Sec. 2.1, a knowledge of the barrier height φ_b is of prime importance in describing the performance of a Schottky diode. In addition to this information, a knowledge of the variation of φ_b across an area comparable to that of the proposed diode is important. This is especially true for large area, high current devices since those areas with low values of φ_b will tend to conduct the highest current density [in accord with Eqs. (3) and (4)] and this effect could conceivably result in device failure because of localized "burnout." Also of importance is the n value of the contact, since excessively large n values result in excessive forward voltage drops. This section deals with the measurement of these three parameters.

The most reliable (and simplest) method of determining the barrier height was found to be the extrapolation of log I vs V plot to the origin as detailed in Sec. 2.2. This procedure also has the advantage that the n value can be determined from the slope of the curve. Typical results are shown in Fig. 10 for small area (9.3×10^{-4} cm^2), low temperature PtSi-Si contacts to the three crystal faces investigated, ⟨111⟩, ⟨110⟩, and ⟨100⟩. A computer least squares fitting procedure was employed to determine the n and φ_b values shown in the figure. The value of φ_b was also checked in a few cases by the reverse capacitance-voltage method, but the precision was found to be far less by this latter method. Measurements of the barrier height were made for Al, W, "conventionally" formed PtSi, and low temperature PtSi contacts to silicon. For the "conventionally" formed PtSi, a 600°C, 20-minute heat treatment in argon was employed to react the Pt and Si subsequent to deposition. The results of the barrier height and n value measurements are summarized in Table I.

3.2 Reproducibility

Table I also shows the results of a number of measurements which were made in order to determine the spread of φ_b values across a wafer. The spread was determined by fabricating a number of small ($A = 9 \times 10^{-4}$ cm^2) Schottky contacts on 0.020-inch centers on a wafer. A constant current source

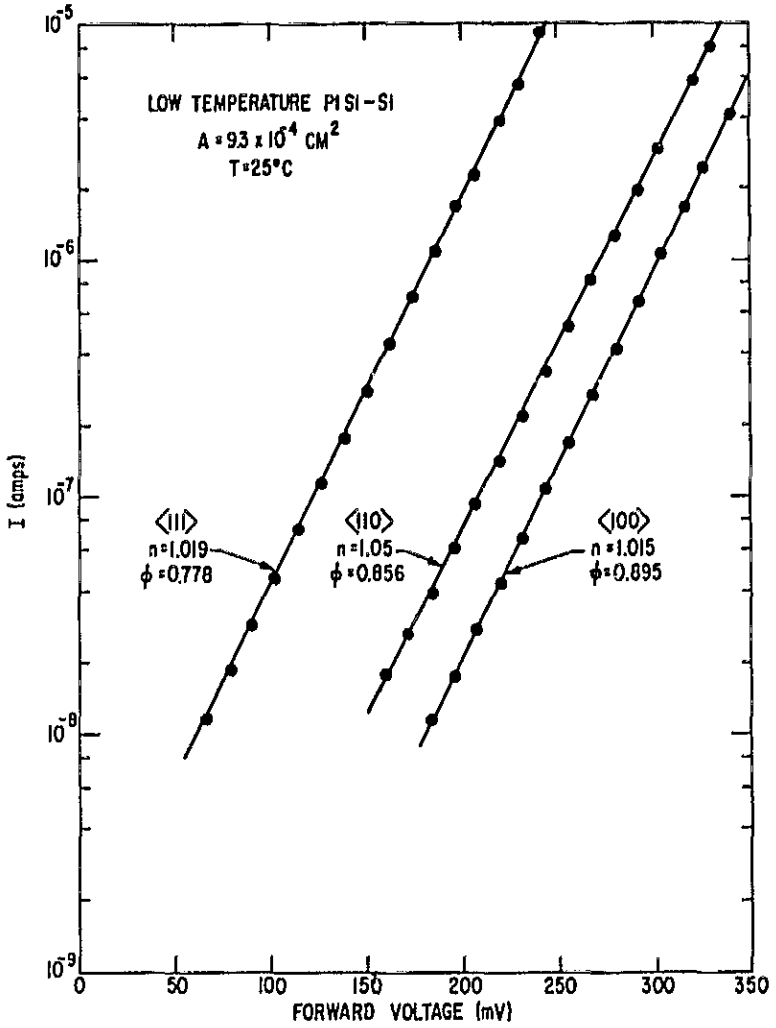


Fig. 10 Forward bias current-voltage characteristics of low temperature Pt-Si on the three major crystallographic faces of silicon. The effects of crystal face upon barrier height are evident.

was used to pass a fixed current ($I = 10^{-6}$ amp in this case) through each device and the forward drop across the diode was measured. In the ideal case ($n = 1$, $R = 0$), Eqs. (3) and (4) show that the variation in forward drop is just equal to the variation in φ_b across the wafer provided $V > \sim 3$ kT. Since R is never zero, the value of I was selected to satisfy the two inequalities,

$$V > 3\ kT$$

$$V >> IR.$$

Non-unity n values are still a problem, however, and so the variation in forward drop actually includes both variations in φ_b and variations in n and

TABLE I

BARRIER HEIGHTS, n VALUES AND FORWARD DROP RANGE FOR SEVERAL CONTACT SYSTEMS

CONTACT MATERIAL	CRYSTAL ORIENTATION	ϕ (eV)	ΔV (volts)	NUMBER OF SAMPLES	TYPICAL n
Al	<100>	.760	± .014	231	1.04
Al	<111>	.732	± .012	530	1.02
Al	<111>	.708	± .008	601	1.04
Al	<110>	.760	± .008	105	1.05
W	<100>	.690	± .018	531	1.05
W	<111>	.688	± .012	623	1.02
W	<110>	.685	± .017	358	1.02
Conv. PtSi	<100>	.871	± .018	217	1.08
Conv. PtSi	<111>	.846	± .016	291	1.08
Conv. PtSi	<110>	.851	± .022	215	1.13
Low PtSi	<100>	.900	± .003*	10	1.02
Low PtSi	<111>	.780	± .002	1750	1.03
Low PtSi	<110>	.856	± .002*	20	1.05

* On account of the small number of samples of these orientations, the ΔV values represent the range of the entire lot, rather than 90% of the samples as for the other entries in the table.

thus represents a " worst case" estimate of the variation in φ_b, assuming φ_b and n to be essentially independent. This latter assumption was found to be the case for all samples investigated, with the exception of the conventionally formed PtSi contacts where a correlation between high n and low φ_b values was observed.

The reason for using this procedure to determine the variation in φ_b was that in this case only a single measurement was required, whereas to determine φ_b from the I-V characteristic required at least 3 and preferably 10 measurements; thus the time required was greatly reduced. To insure that no systematic error crept into this procedure, however, φ_b and n were determined independently for 10 to 20 randomly selected diodes for each of the contact combinations listed in Table I. The ΔV values shown in Table I represent the voltage range which included 90% of the samples investigated; the sample size is also listed. The only exceptions to this rule are for the low temperature PtSi contacts to ⟨100⟩ and ⟨110⟩ Si where only a small number of samples were measured and the ΔV values shown represent the range for the entire lot. Although only a small number of samples of low temperature PtSi to ⟨100⟩ or ⟨110⟩ Si were measured, the uniformity of this type of contact is clearly demonstrated by the ⟨111⟩ results where 1750 diodes were measured, representing the spread across an entire 1 1/4-inch diameter wafer. The actual distribution of measured forward voltage drop for the low temperature PtSi-⟨111⟩ Si case is shown in Fig. 11. There is no reason to expect that the variation of barrier height across other crystal faces will be significantly different than that across the ⟨111⟩ face.

It should be noted in Table I that there are two entries for Al - ⟨111⟩ Si contacts; these represent samples from different wafers, which were " sintered" in separate runs. The variation in barrier height from one sample to the other is most probably due to small differences in the actual sintering conditions, and this run to run variation is typical of what was observed in the Al measurements. The " sintering" procedure for the Al samples consisted of heating the sample at ~450°C for 1/2 hour in a reducing atmosphere.

3.3 Barrier Lowering

Equation (5) indicates that barrier lowering is a function of $\mathcal{E}_m$, the electric field at the metal-semiconductor interface. Unfortunately $\mathcal{E}_m$ is not directly measurable, but must be determined from the reverse voltage, V_r, and the net impurity concentration in the semiconductor. Thus a description of barrier lowering requires two essentially independent measurements, the first to determine $\mathcal{E}_m(V_r)$ and the second to determine $\Delta\varphi_b(V_r)$. The procedure used in this study was to determine $N_d(X_D)$ and $X_D(V_r)$ by measuring the depletion capacitance of the Schottky barriers as a function of V_r. Here N_d is the net donor concentration at X_D, the depletion length when V_r is applied. $\mathcal{E}_m(V_r)$ can then be determined from

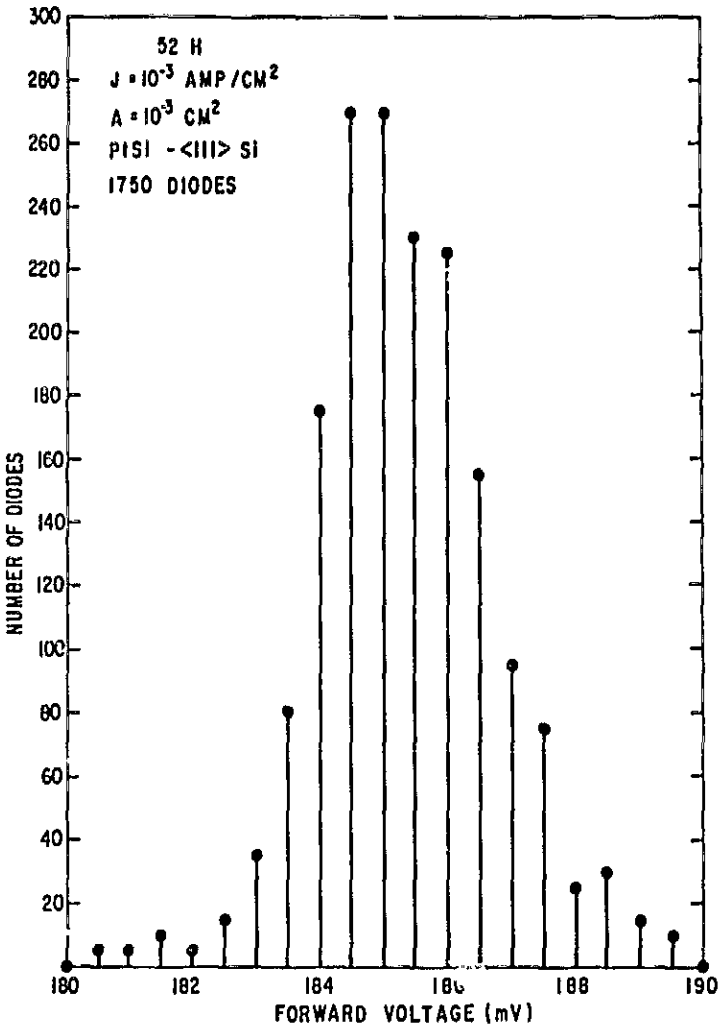


Fig. 11 Histogram showing distribution of forward voltages corresponding to a current density 10^{-3} A/cm^2 for all the diodes of 1 1/4 inch wafer.

$$\mathcal{E}_m = \mathcal{E}_0 + \frac{q}{\epsilon}\int_0^{X_D} N_d(X)dX \ , \qquad (6)$$

where $\mathcal{E}_0$ is the " built-in" field due to the barrier. A typical $\mathcal{E}_m(V_r)$ curve obtained in this manner is shown in Fig. 12, for an average net donor concentration of $\sim 8 \times 10^{14}$ cm^{-3}. Local variations in the net donor concentration, although visible in the $N_d(X)$ data, were too small to appreciably influence this curve and so it retains the parabolic shape ($\mathcal{E} \propto V^{1/2}$) characteristic of a constant value of N_d.

The determination of $\Delta\varphi_b(V_r)$ was not as straightforward. A combination of the second and third methods of Sec. 2.2 for determining $\Delta\varphi_b(V_r)$ was used to obtain accurate results.

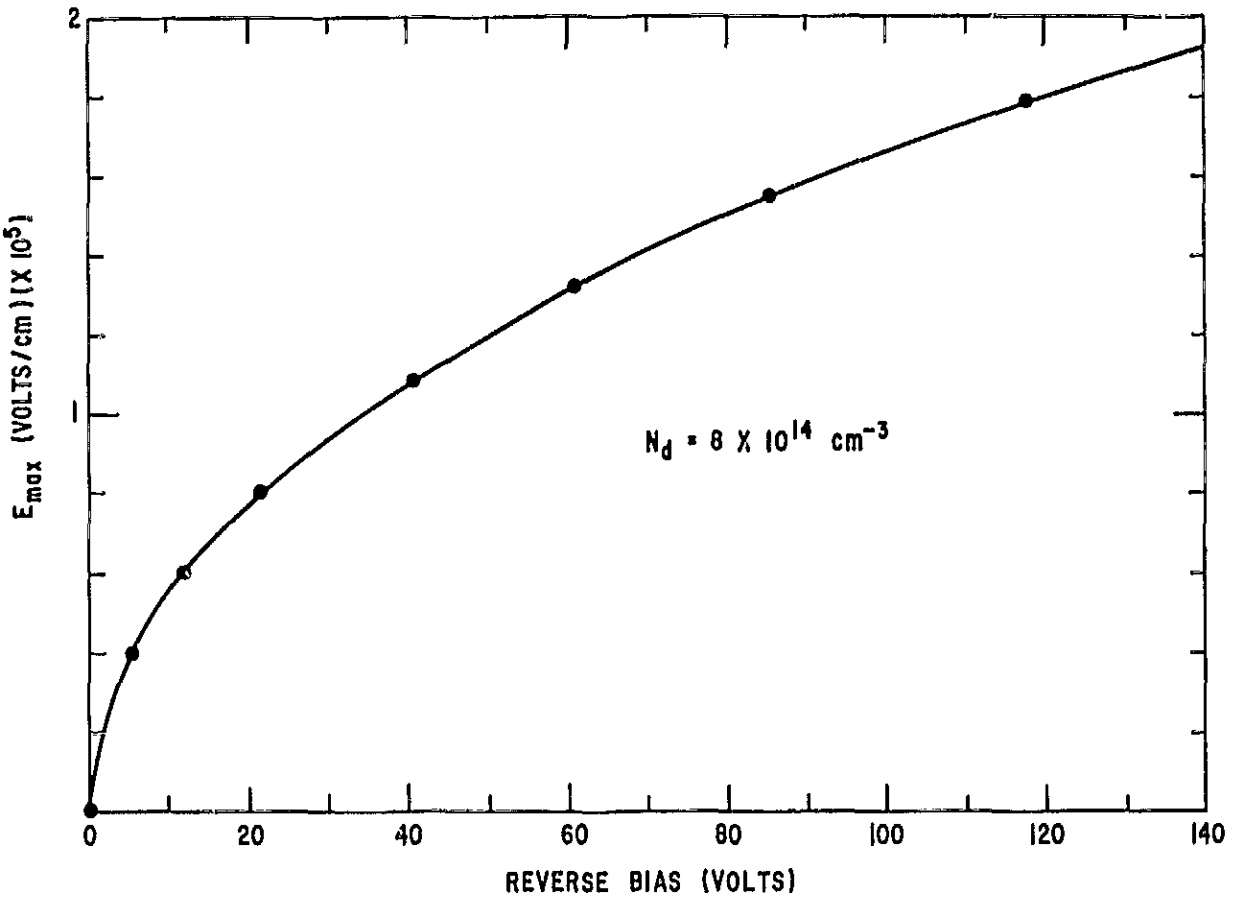


Fig. 12 Variation of $\mathcal{E}_m$, the maximum electric field of a reverse biased Schottky diode, with reverse bias. The curve is obtained by stepwise integration of capacity - voltage data.

Consider the equation

$$J_S = AT^2 \exp-(q\varphi_b(V_r)/ kT) \quad . \tag{7}$$

If $\varphi_b(V_r)$ is to be determined by varying T (for a fixed V_r) and observing J_S, variations in φ_b as a function of T must also be considered. These variations are predominantly due to a variation of the Fermi level with temperature. The variation which is usually assumed is of the form

$$\varphi(V_r, T) = \varphi_0(V_r) + \alpha(V_r)T \quad , \tag{8}$$

where

$$\alpha(V_r) = \left.\frac{\partial\varphi}{\partial T}\right|_{T=0} \quad .$$

Substituting (8) into (7), one obtains

$$J_S = AT^2 \exp(-q(\varphi_0 + \alpha T)/kT) \tag{9}$$

or

$$J_S = AT^2 \exp\left(\frac{-q\alpha}{k}\right) \exp\left(\frac{-q\varphi_0}{kT}\right) \tag{10}$$

Rearranging terms and defining

$$A_{eff} = A \exp\left(\frac{-q\alpha}{k}\right) \tag{11}$$

one obtains

$$J_S/T^2 = A_{eft} \exp\left(\frac{-q\varphi_0}{kT}\right) \tag{12}$$

or, taking natural logarithms

$$\ell n\,(J_S/T^2) = \ell n(A_{eff}) - q\varphi_0/kT \quad . \tag{13}$$

If we assume that all the reverse leakage is due to thermionic emission over the barrier, then the measured current, J_r, is exactly the saturation current, J_S;

$$J_S = J_r \quad . \tag{14}$$

If a plot is now made of $\ell n(J_r/T^2)$ as a function of $1/T$ Eqs. (13) and (14) show a straight line with slope $-q\varphi_0/k$ and intercept (at $1/T = 0$) of $\ell n(A_{eff})$. This latter intercept may be used with Eq. (11) to give α. Eq. (8) may then be used with the value of φ_0 determined from the slope to calculate φ at the given value of V_r and the temperature of interest. This is essentially method 3 of Sec. 2.2.

In practice several problems arise when $\Delta\varphi$ is determined in this manner. First of all, data are obtained over a relatively small temperature range, typically 25° to 160°C, (298° to 423°K) corresponding to a $1/T$ range of $\sim 2.4 \times 10^{-3}$ to $\sim 3.4 \times 10^{-3}$. The intercept must thus be determined by extrapolating the curve over approximately 2.5 times the range over which data are available. Any error in this procedure greatly affects the measured value of α. A second problem encountered with this procedure is that it is desirable to measure $\Delta\varphi$ with a precision of ± 0.005 eV or better. Our experience was that it was not possible to measure the slope of the curve nearly that precisely; thus the measurement of both φ_0 and α are in doubt by amounts greater than can be tolerated.

For these reasons we adopted the following procedure. Rather than hold V_r fixed and vary temperature, we kept the temperature fixed and measured J_r as V_r varied. Data were still plotted as before, i.e., log J_r/T^2 versus $1/T$, but now only to insure that a straight line fit did result. If a straight line was obtained, the assumption that all the current is due to thermionic emission over the barrier is probably valid. We then used Eq. (7) to determine φ_b.

Reverse bias I-V data were taken at various fixed values of junction temperature. The temperature was kept fixed to better than 0.1°C throughout the course of measurement of each of the I-V characteristics. The "true" absolute junction temperature cannot, of course, be measured directly. There may well be differences between it and our measured thermocouple values due to calibration errors and the effects of heat flow. These types of discrepancy are quite difficult to identify in detail and correct for. It is far easier to hold a fixed temperature than to know its precise value. We estimate that our measured temperatures are correct to 0.5°C. Nevertheless, this uncertainty does not affect in any serious way a determination of $\Delta\varphi_b(V_r)$ from Eq. (7) when T is held fixed and V_r is varied.

This result is easily obtained from Eq. (7). The barrier at no reverse bias is given by

$$\varphi_b(0) = \frac{kT}{q} \ln \frac{J_S(0)}{AT^2} \tag{15}$$

and that at some value of reverse bias, V_r, is

$$\varphi_b(V_r) = \frac{kT}{q} \ln \frac{J_S(V_r)}{AT^2} \quad . \tag{16}$$

When the procedure just described is followed the two values of "true" junction temperature are the same even though they may deviate from the measured values. A simple subtraction gives us

$$\Delta\varphi(V_r) = \varphi_b(0) - \varphi_b(V_r) = \frac{kT}{q} \left[\ln \frac{J_S(0)}{AT^2} - \ln \frac{J_S(V_r)}{AT^2} \right] \tag{17}$$

Any error in temperature, δT, now contributes, in linear fashion, a corresponding error in $\Delta\varphi(V_r)$

$$\frac{\delta\Delta\varphi}{\Delta\varphi} = \frac{\delta T}{T} \quad . \tag{18}$$

Thus, our 1 percent knowledge of temperature yields a 1 percent measurement of barrier lowering due to electric field. In this manner, the entire $\varphi_b(\mathcal{E}_m)$ curve could be obtained.

A typical reverse current vs voltage curve (with temperature as the parameter) is shown in Fig. 13. The particular data shown are for a W - ⟨111⟩ Si contact ($A = 9.3 \times 10^{-4}$ cm^2, $N_d = 8 \times 10^{14}$ cm^{-3}). Figure 14 is a plot of log J_r/T^2 vs $1/T$ for a field of 1×10^5 v/cm. For this sample, a reverse bias of 34 volts was required to produce this field at the contact. It should be noted that in this case an excellent fit is obtained and one can be confident that the reverse current is predominantly due to thermionic current over the barrier. Such was not always the case, however, as is illustrated by the results shown in Fig. 15. These results were obtained from a low temperature PtSi - ⟨111⟩ Si contact; the three curves were obtained at reverse biases of 10, 70, and 140 volts, corresponding to electric fields of 7×10^4, 1.6×10^5, and 2.2×10^5 v/cm, respectively. It should be noted that while the data for the two lower values of field give a good fit, the data for the highest field show a systematic deviation from a straight line, which is most evident at lower temperatures. It appears that an extra component of leakage current was present in this sample; thus data obtained from this sample for fields in excess of 1.6×10^5 volts/cm were suspect and were not used to generate the

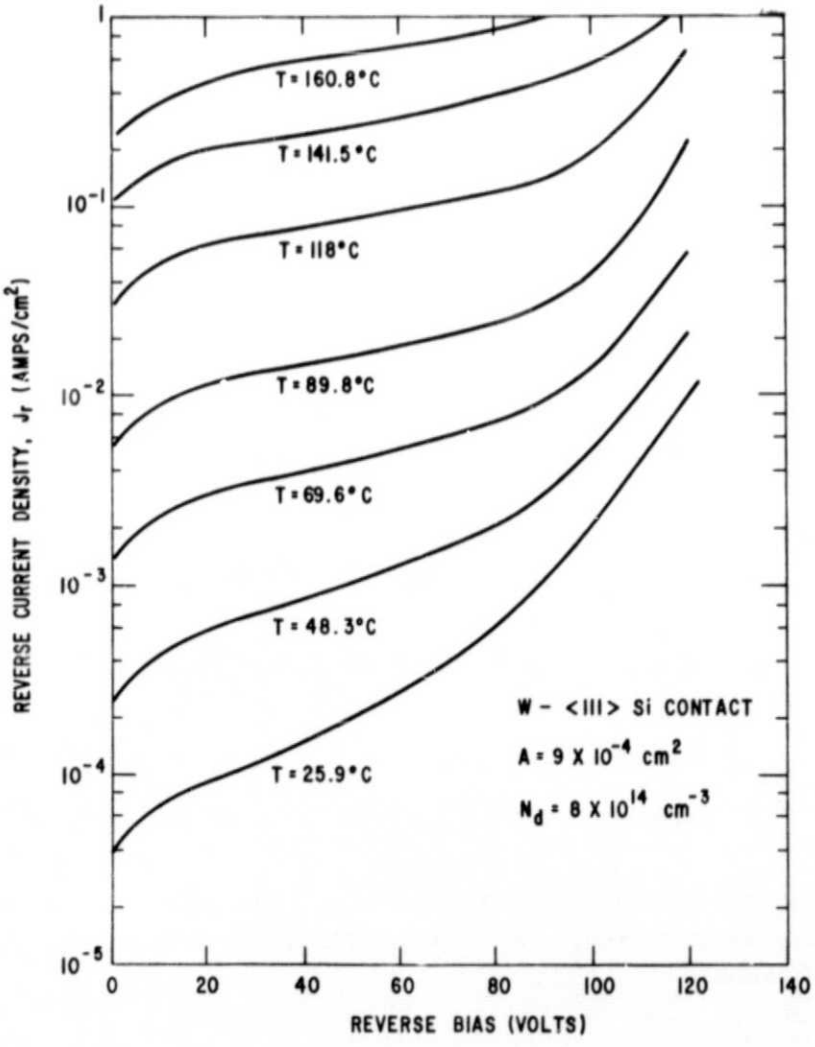


Fig. 13 Typical set of data used to determine the effects of reverse bias upon barrier height.

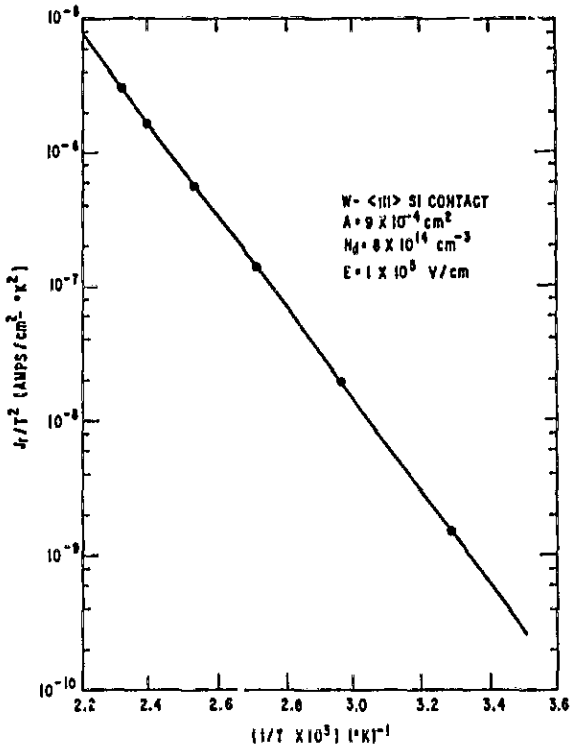


Fig. 14 Typical plot of log J_r/T^2 vs T^{-1} used to verify the assumption that the measured values of J_r, the reverse current, are indeed thermionic. The data for this curve are the same as those of Fig. 13 at reverse bias corresponding to $E_{max} = 1 \times 10^5$ volt/cm.

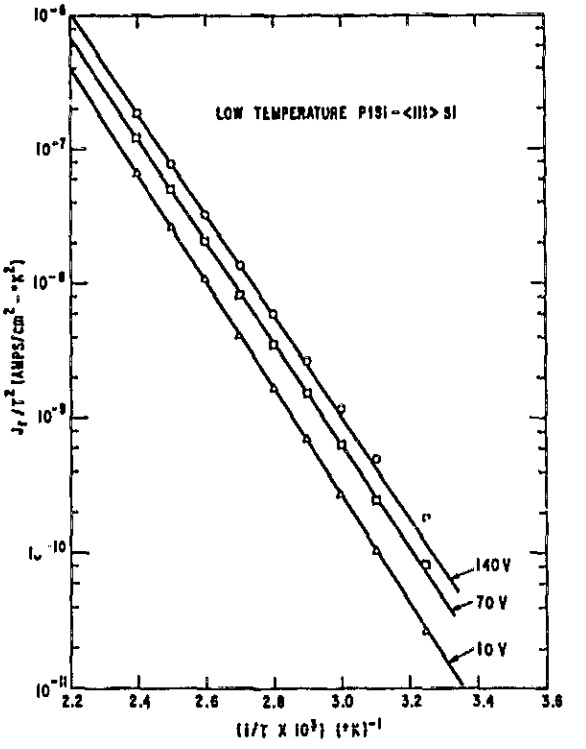


Fig. 15 Variation of log (J_r/T^2) vs. T^{-1} for three different values of reverse bias ($\mathcal{E}_m$).

$\varphi_b(\mathcal{E}_m)$ curves. Whenever a deviation from a straight line fit was observed, it was always in the manner shown in Fig. 15, i. e., it was always an " excess" current, which was most evident at low temperatures and high fields.

The results of the barrier lowering measurements are presented in Figs. 16 through 22, for W, Al, and low temperature PtSi contacts. In each case, the zero field barrier value is that which was obtained from the forward I-V characteristic of the diode; the fact that most of the curves join smoothly to this point is a further argument that the measurement procedure was valid. The curves are all similar; they show an upward curvature at low fields followed by a linear decrease in barrier height with electric field at the higher values of field, which is consistent with the prediction of Eq. (5).

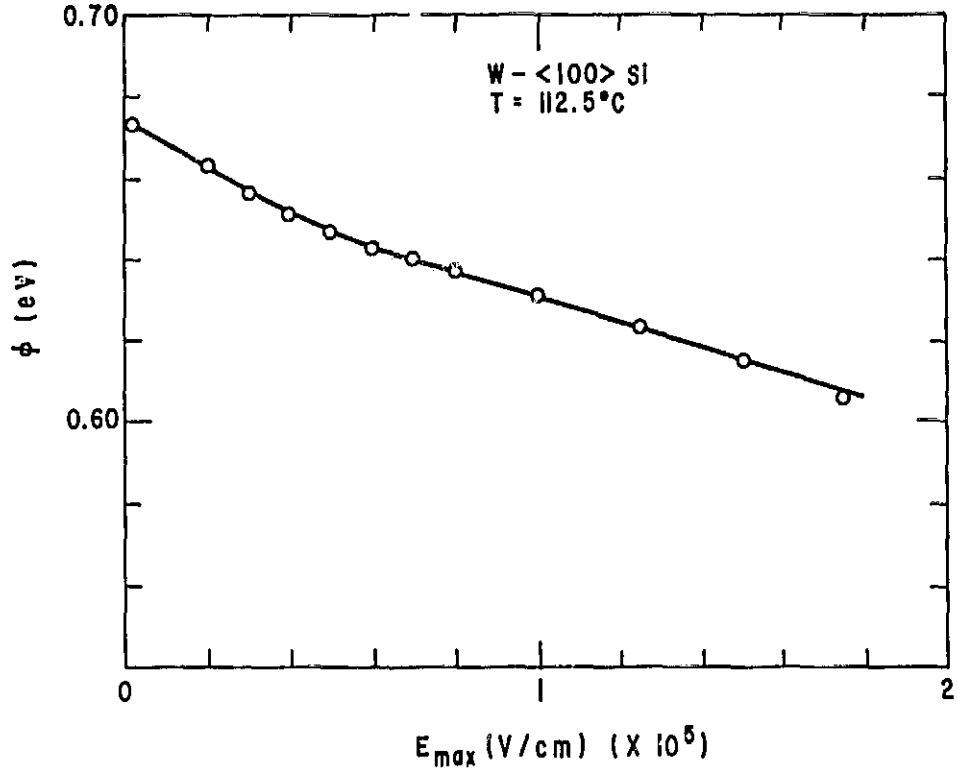


Fig. 16 Reverse bias lowering of the tungsten barrier on ⟨100⟩ silicon at 110°C

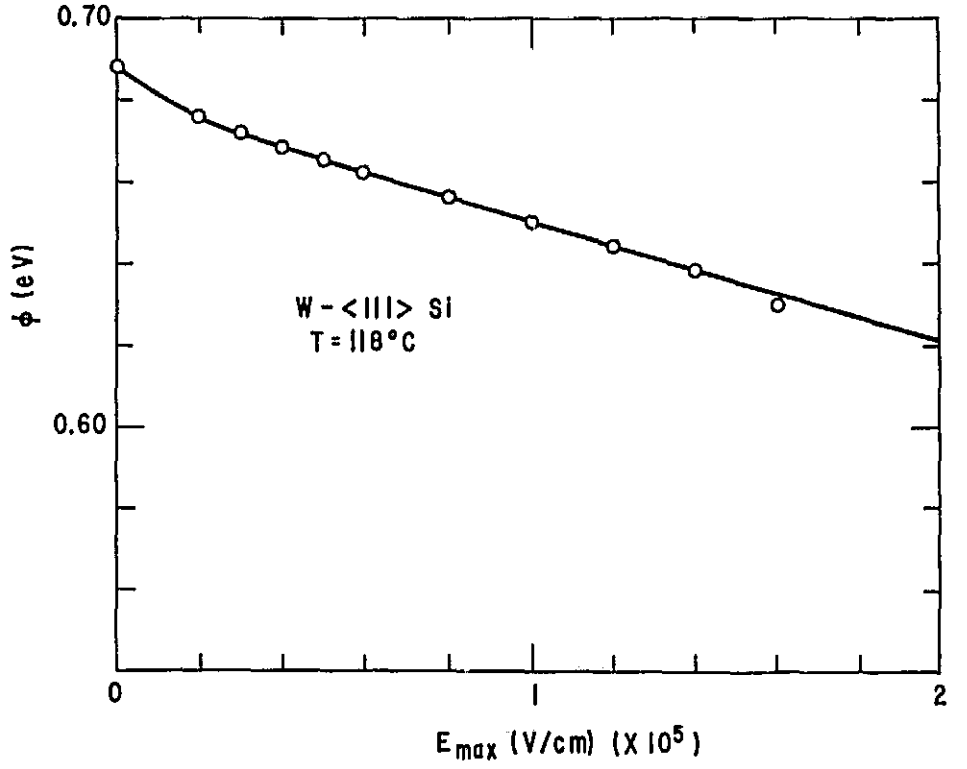


Fig. 17 Reverse bias lowering of the tungsten barrier upon ⟨111⟩ Si at 120°C

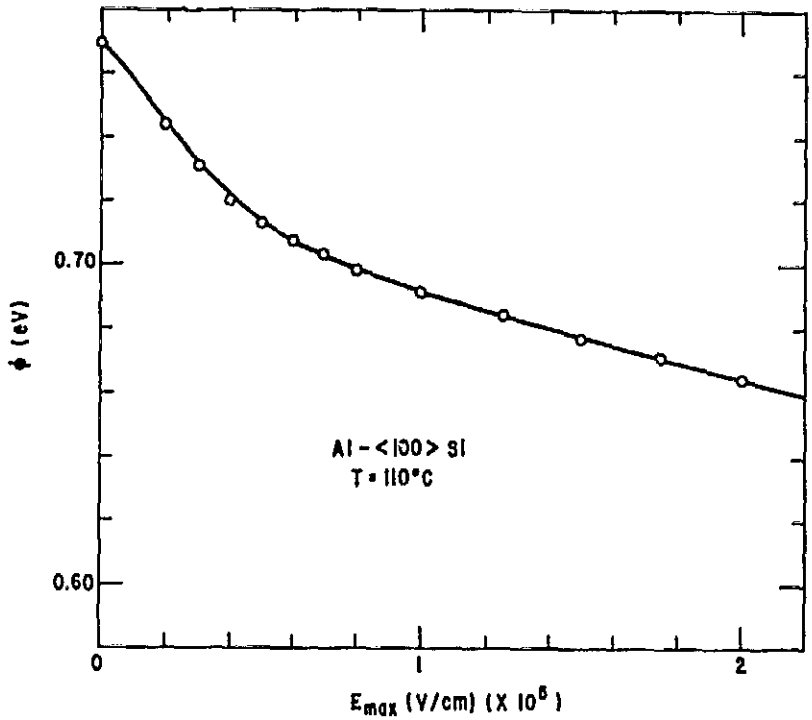


Fig. 18 Reverse bias lowering of the aluminum barrier upon ⟨100⟩ Si at 110°C

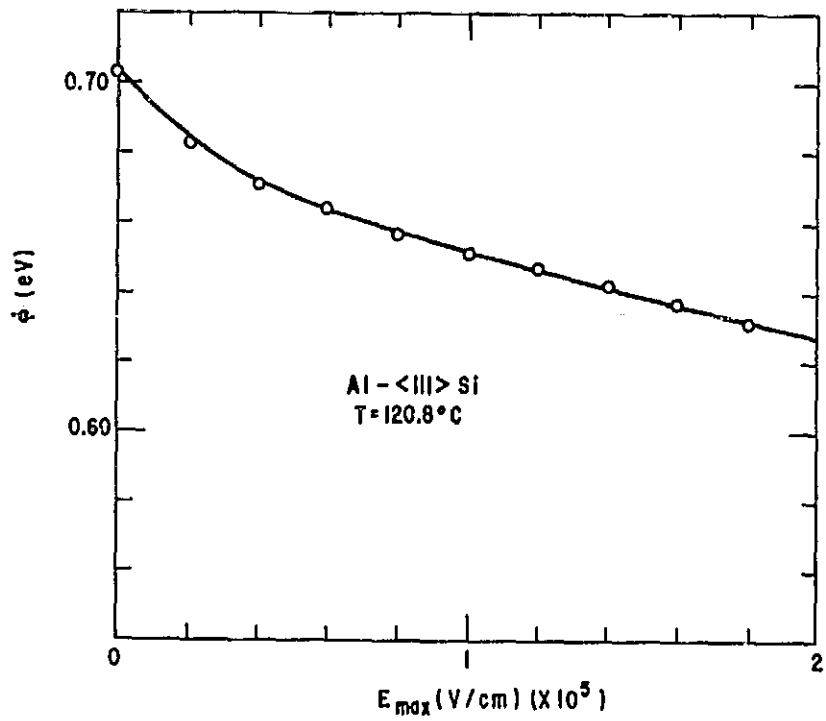


Fig. 19 Reverse bias lowering of the Al barrier upon ⟨111⟩ Si at 120°C

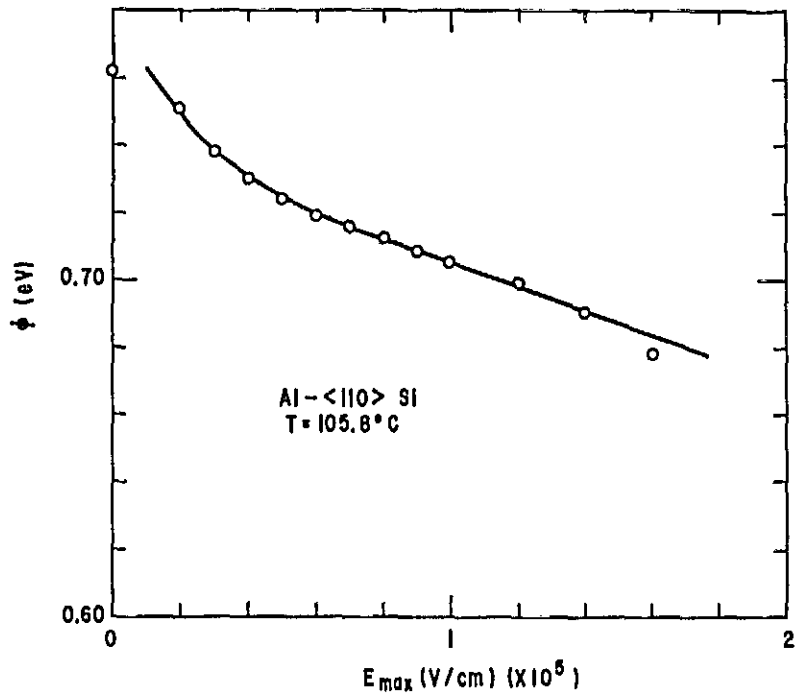


Fig. 20 Reverse bias lowering of the aluminum barrier upon ⟨110⟩ Si at 110°C

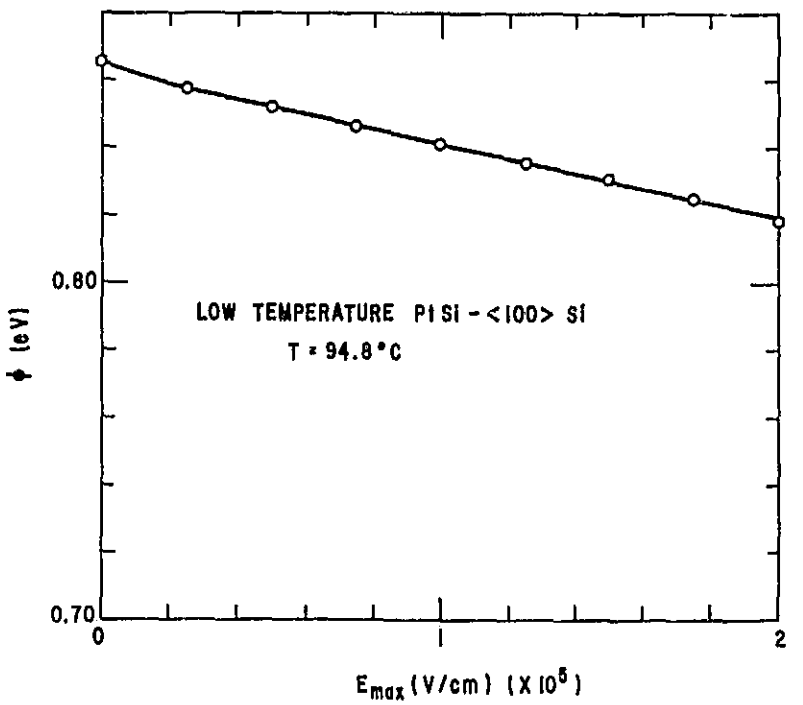


Fig. 21 Reverse bias lowering of the low temperature Pt-Si barrier upon ⟨100⟩ Si at 95°C

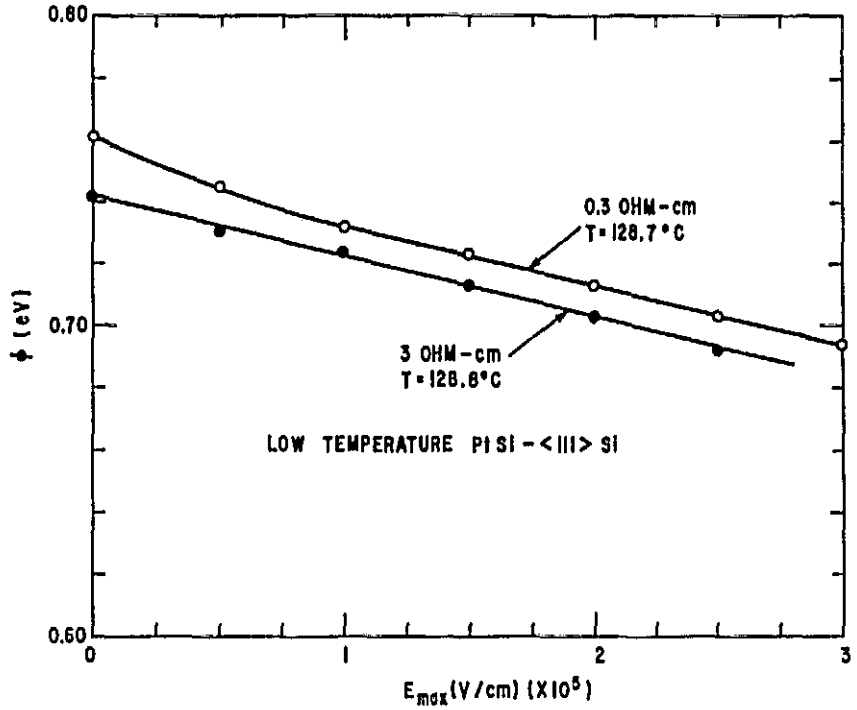


Fig. 22 Reverse bias lowering of the low temperature Pt-Si barrier upon ⟨111⟩ Si at 130°C for two different resistivity substrates.

Figure 22 shows the barrier lowering for low temperature PtSi - ⟨111⟩ Si contacts for two different Si resistivities, 0.3 and 3 ohm-cm. The fact that the curves are essentially parallel demonstrates that the barrier lowering does depend on field rather than applied voltage. For example, at a field of 3.0×10^5 volts/cm, the applied voltage in the 3 ohm-cm case is 125 volts while for the 0.3 ohm-cm device it is only 40 volts (the difference in the two curves arises principally from the difference in the zero field barrier height). Thus a single curve can be used for design purposes, and the barrier lowering at a given voltage can be determined from the voltage and Si resistivity. The curves given in Figs. 16 through 22 were obtained at the temperatures shown, all near 100°C. Since most power rectifiers will operate at or near this temperature, the curves should provide the necessary information for estimating the reverse leakage current of any potential W, Al, or PtSi Schottky diode. The data shown in Fig. 22 were used to estimate the reverse leakage for the large area diodes discussed in Sec. 4.

Section 4

DIODE DESIGN

4.1 Forward Specifications

Let us first consider the forward specifications. All calculations in this section will be based on Eqs. (3), (4), and (5) of Sec. 2.1. A value of A = 120 amp/cm^2 will be used throughout and the barrier parameters used will be those of Table I. In Fig. 23 we have plotted a number of diode voltage drop curves as a function of the diode area. The curve labeled "barrier drop" is the required barrier voltage to produce a current of 25 A at 25°C assuming a low temperature PtSi - ⟨111⟩ Si Schottky contact. In order to calculate the series resistance of the epitaxial Si layer, we assume the geometry to be that of a mesa structure. For this case we may use the curves of Fig. 3 (plane junction curve) to determine the maximum donor concentration which will support 100V and 200V. The values are 5×10^{15} cm^{-3} and 2×10^{16} cm^{-3}, respectively, and the corresponding

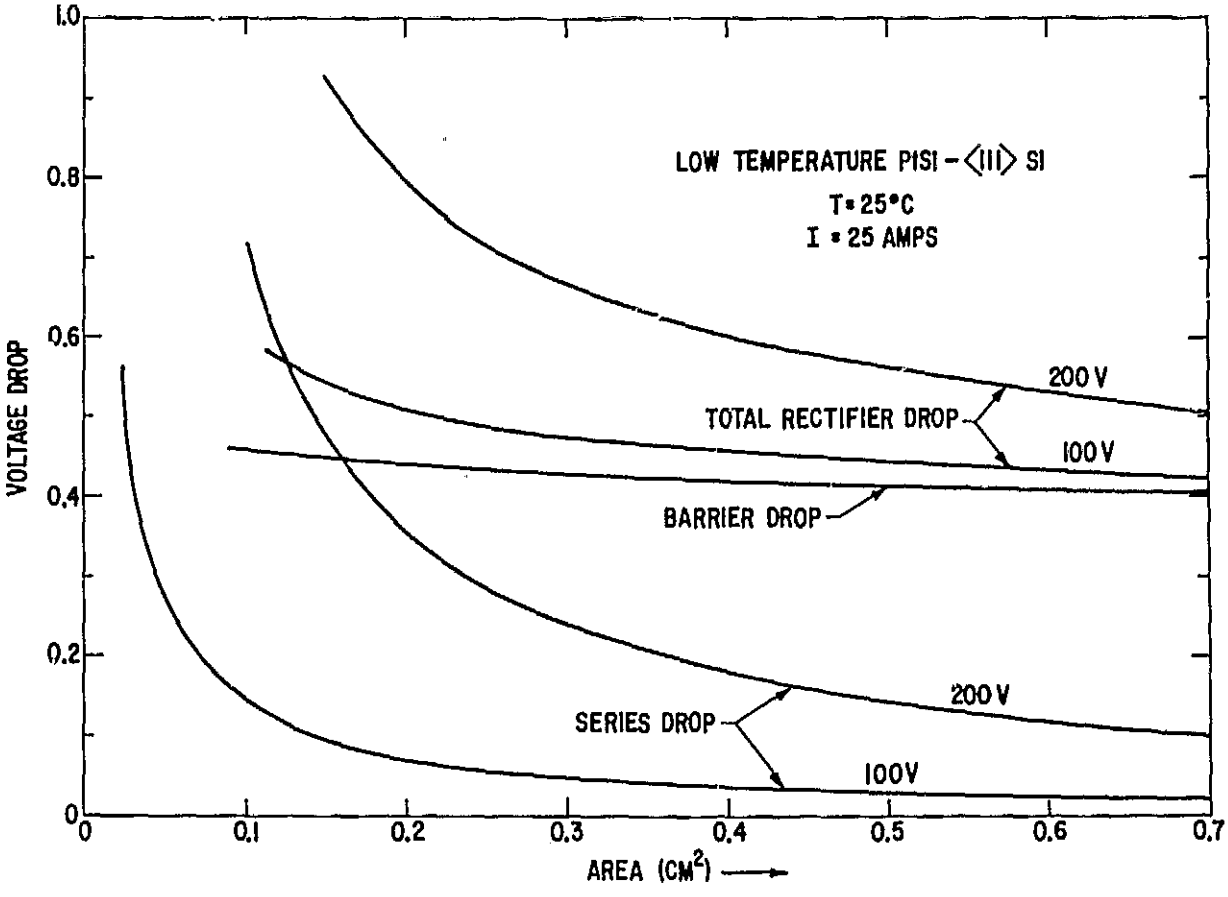


Fig. 23 Ideal design curves for 25 A mesa Schottky diodes for both 100 and 200 volt breakdown. It is assumed that avalanche breakdown will occur at the theoretical maximum, the microplasma free bulk avalanche value.

resistivities are 1.1 Ω-m and 2.5 Ω-cm. The required epitaxial thickness for the mesa geometry is just equal to the depletion width; for the 100V device this is 5.1μ and for the 200V device the required thickness is 12μ. The corresponding volt-drop in the silicon is then given by $V = J \rho t$ where J is the required current density, ρ is the epitaxial resistivity, and t is the epitaxial thickness. These results are plotted in the curves labeled " series drop" for the two cases in question. The curves labeled " total rectifier drop" are the respective sums of the barrier drop and the series drop. If we ignore the contact losses, we see that the minimum area possible which will allow us to meet the new forward specification goals is 0.22 cm^2 for the 100V device and 0.4 cm^2 for the 200V device. If we assume that the packaging losses add 0.04 to 0.05 volt, the new minimum required area becomes 0.4 cm^2 for the 100V device and 0.55 cm^2 for the 200V device.

Similar total rectifier drop curves for other choices of contact material or crystal orientation are easily obtained from Fig. 23. The parasitic series drop is independent of barrier since it depends only upon reverse blocking capability. The barrier drop, however, is linear in barrier height. Total rectifier drop for other barriers are thus obtained by merely shifting the ⟨111⟩ PtSi curve vertically by the appropriate amount.

4.2 Reverse Specifications

We now calculate reverse leakage currents at breakdown and 100°C to determine whether reverse goals are attainable with devices of area large enough to meet forward requirements.

Barrier heights at 100°C and $\mathcal{E}_m = 3 \times 10^5$ volts/cm are presented in Table II for Al, W, and low temperature PtSi. These values were obtained from the data of Sec. 3.3. Table II also gives the reverse leakage current density corresponding to thermionic emission at 100°C over these field lowered barriers. The field chosen, 3×10^5 v/cm, is the maximum field that can be sustained by silicon at $N_D \cong 10^{15}$. This value varies very slowly with doping and since $\Delta\varphi_b$ depends only upon electric field and not voltage, the values of leakage current density listed in Table II are applicable to diodes of any voltage rating.

We see from Table II and Fig. 23 that a low temperature Pt-Si barrier on ⟨111⟩ silicon is the most desirable choice for meeting the contract specification for the 200 volt device. Selecting a junction area of 0.6 cm^2 ideally yields a forward drop of 0.52 volt and reverse leakage of 6.6 ma. A choice of tungsten as the barrier metal allows one to go to 0.25 cm^2 and still keep to 0.6 volt forward for the 200 volt device. This decrease in size, however, is not enough to reduce the reverse current to acceptable levels. The leakage for a tungsten diode made on ⟨100⟩ material is 85 ma and on ⟨111⟩ silicon it is 44 ma. Aluminum devices meeting the specifications are also ideally possible. We did not pursue this approach, however, as the aluminum-silicon

TABLE II

Barrier Height and Reverse Thermionic Current at 100°C and Junction Field of 3×10^5 v/cm

Contact Material	Crystal Orientation	φ (volts)	J_s $\frac{ma}{cm^2}$
Al	⟨100⟩	0.636	42
Al	⟨111⟩	.602	120
Al	⟨110⟩	.636	42
W	⟨100⟩	.570	330
W	⟨111⟩	.591	175
Low temp Pt-Si	⟨100⟩	.798	0.27
Low temp Pt-Si	⟨111⟩	.680	11

interface is metallurgically unstable. There is a substantial literature on the migration of silicon onto the aluminum metallizations of integrated circuits. This problem is apt to be even more serious in power devices which are normally run at elevated temperatures. We thus selected low temperature Pt-Si on ⟨111⟩ Si as the barrier material and the mesa geometry as the device structure for Schottky diode fabrication.

Section 5

WAFER PROCESSING

Conventional planar processing procedures are inadequate to fabricate high-voltage structures because of field crowding, as was discussed in the Introductory Technical Discussion. The basic structure chosen in order to meet the reverse voltage requirements was a mesa structure. Diode fabrication proceeded as follows:

5.1 Epitaxial Growth

N type silicon is grown epitaxially upon heavily doped n+ substrates. Resistivity ranges covered were 1 to 4 Ω-cm and thicknesses of growth varied from 10μ to 15μ. The specific design objectives for the 200 volt rectifier were 2.5 Ω-cm resistivity and 12μ final thickness.

5.2 Initial Oxidation

A 700Å thick layer of SiO_2 is next grown upon the epitaxial layer. This is necessary so as to prevent slip from occurring in the wafer when the wafer which is next coated with Si_3N_4 is subsequently heated to temperatures greater than 1000°C.

5.3 Si_3N_4 Deposition

The wafer is next coated with a Si_3N_4 layer 1300Å thick. This Si_3N_4 layer provides the masking material for later mesa diode definition.

5.4 SiO_2 Deposition

Six thousand angstroms of SiO_2 are next deposited in order to serve as a transfer mask material for patterning of the Si_3N_4. This is necessary since the usual photoresists will not stand up to the hot phosphoric acid etch necessary to pattern silicon nitride. This SiO_2 also serves as a protective coat for the silicon nitride layer preventing it from being attacked by the phosphorus-rich oxidizing atmosphere that we next use to getter impurities from the wafer.

5.5 Getter Cycle

At an early stage in our development program we learned that it was necessary to introduce an explicit gettering step in the device processing sequence even though in principle it should not be required. In practice, epitaxial material, while varying widely, contains substantial amounts of deep-level impurity centers. These act as generation centers which, if not removed from the device structure, produce excessive leakage in reverse

bias. Even worse is the interaction of these deep level impurities with crystalline defects and interfaces in the silicon. Heavy metal impurities may precipitate out upon vacancy clusters, dislocation lines, and stacking faults. This leads to geometric local electric field enhancement and thus to breakdown under reverse bias occurring at prematurely low voltage levels.

These problems are more serious in Schottky devices than in p-n junction devices. There are no boron-rich or phosphorus-rich silica glasses which are normally incidentally formed in the course of Schottky diode fabrication as is the case for p-n junction formation. These glasses are well known in the industry to be getters for metals such as Cu, Fe, and Au although detailed knowledge of gettering mechanisms is not available and scientific studies are only recently beginning to be made. Junction devices thus have the benefit of a measure of heavy metal gettering which occurs in an inadvertent, incidental way during the course of their fabrication. Notwithstanding this, it is often necessary to do a final explicit getter diffusion cycle, usually taking the form of a very heavy phosphorus surface diffusion.

The getter cycle used in our Schottky diode fabrication is similar to those used in junction device preparation. It was not possible in the course of this work to do a detailed study of gettering. Our approach, instead, was strictly a utilitarian one. We wanted only to find a cycle which worked and allowed us to fabricate Schottky diodes whose breakdown voltages approached bulk planar values and where generation current was not excessive. We developed a cycle which indeed worked not only upon the lot of epitaxial material used in its definition--but also upon selected other lots of epitaxial material obtained from at least two other sources. There was, however, some epitaxial material for which our cycle simply didn't work. We believe that the reasons for this failure are connected with inferior crystalline quality of this latter material.

The wafers next had the 700Å thermal oxide removed from the back surface and were put through our getter cycle. Wafers were preheated in nitrogen for 5 minutes. Next they were exposed to a vapor stream containing N_2, O_2, and $POCl_3$ for 30 minutes. The quantities used in diode formation were 1000 cc/min, 90 cc/min, and 3 cc/min, respectively, flowing through a tube 63 mm in diameter. At the end of the 30 min the $POCl_3$ was shut off while the N_2 and O_2 continued for 5 more minutes. O_2 was next shut off and the furnace was flushed with pure N_2 for 5 minutes longer after which the samples were removed. The furnace temperature was in all cases 1040°C.

This procedure grows an oxide glass approximately 1500Å thick upon silicon and gives a "predep" having sheet resistance of about 3 to 4 $\Omega/\square$ with phosphorus depth as obtained from p-type test wafers of 1μ to 2μ. The glass as formed on polished surfaces is clear and there is no sign of attack of the original silicon surface.

We arrived at these specifics after a series of experiments performed upon polished p-type 1 Ω-cm test wafers. The oxygen and $POCl_3$ concentrations

were varied in order to determine the maximum phosphorus concentration which could be achieved in both glass and silicon without doing gross damage to the silicon surface. We were guided in this effort by the attitude that the more heavily doped was the phosphorous glass the more effective would it be in gettering heavy metals. Figure 24 shows the quantity ρx_j, the product of sheet resistance and junction depth, for various flow rates of carrier N_2 gas through liquid $POCl_3$ kept at both 0°C and room temperature for two different oxygen concentrations. The surface concentration obviously saturates near the value of 6×10^{-4} Ω-cm which corresponds to a surface concentration greater than 5×10^{20} phosphorus per cm^3. Throughout the entire range of Fig. 24 there is no gross attack of the Si surface.

This " predep" cycle was followed by a long slow cooling in O_2 to approximately, 250°C, after which the wafers are quickly brought to room temperature. Figure 25 shows the time-temperature cycle.

5.6 Mesa Definition

The next step is to pattern the Si_3N_4 film using standard photolithographic techniques. Photoresist covers the wafer in those areas where the barrier is to be formed and which will eventually comprise the Schottky diode. The patterning oxide is etched in the usual buffered HF, the photoresist is removed by means of a hot (200°C) H_2SO_4 immersion, and the silicon nitride is etched away in hot (180°C) H_3PO_4. We found it desirable to remove the photoresist

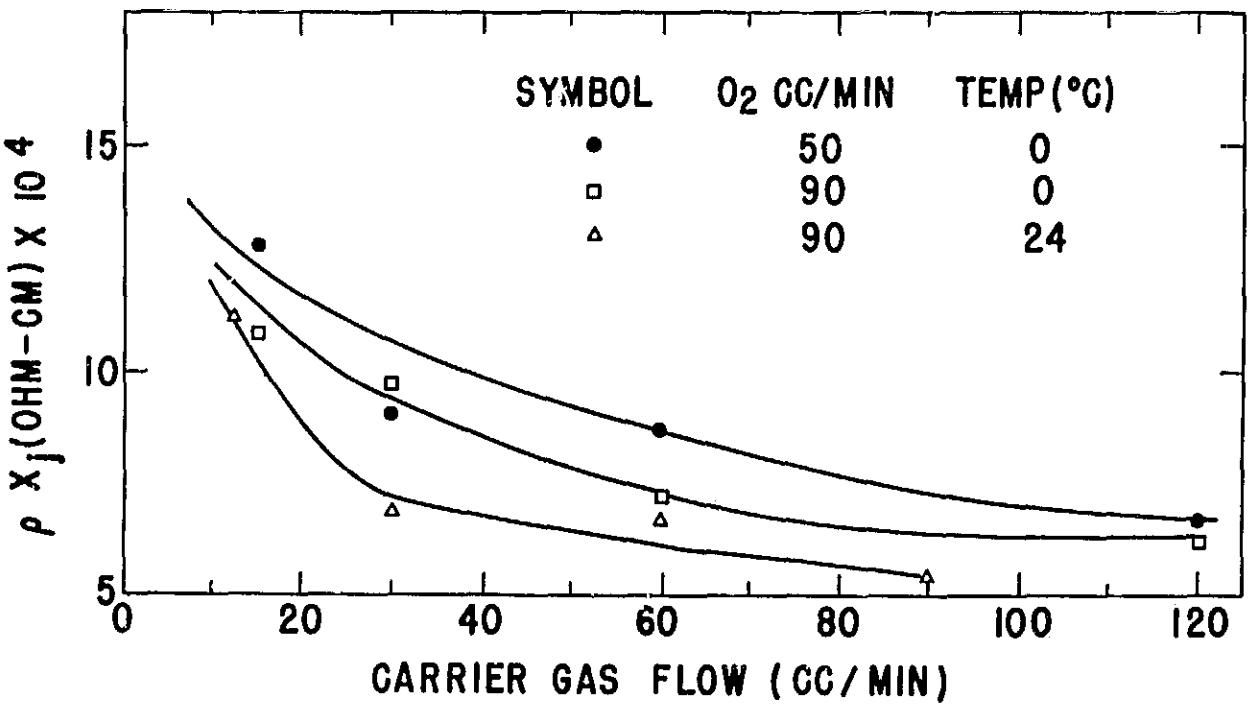


Fig. 24 Product of junction depth and sheet resistance for several different gettering conditions.

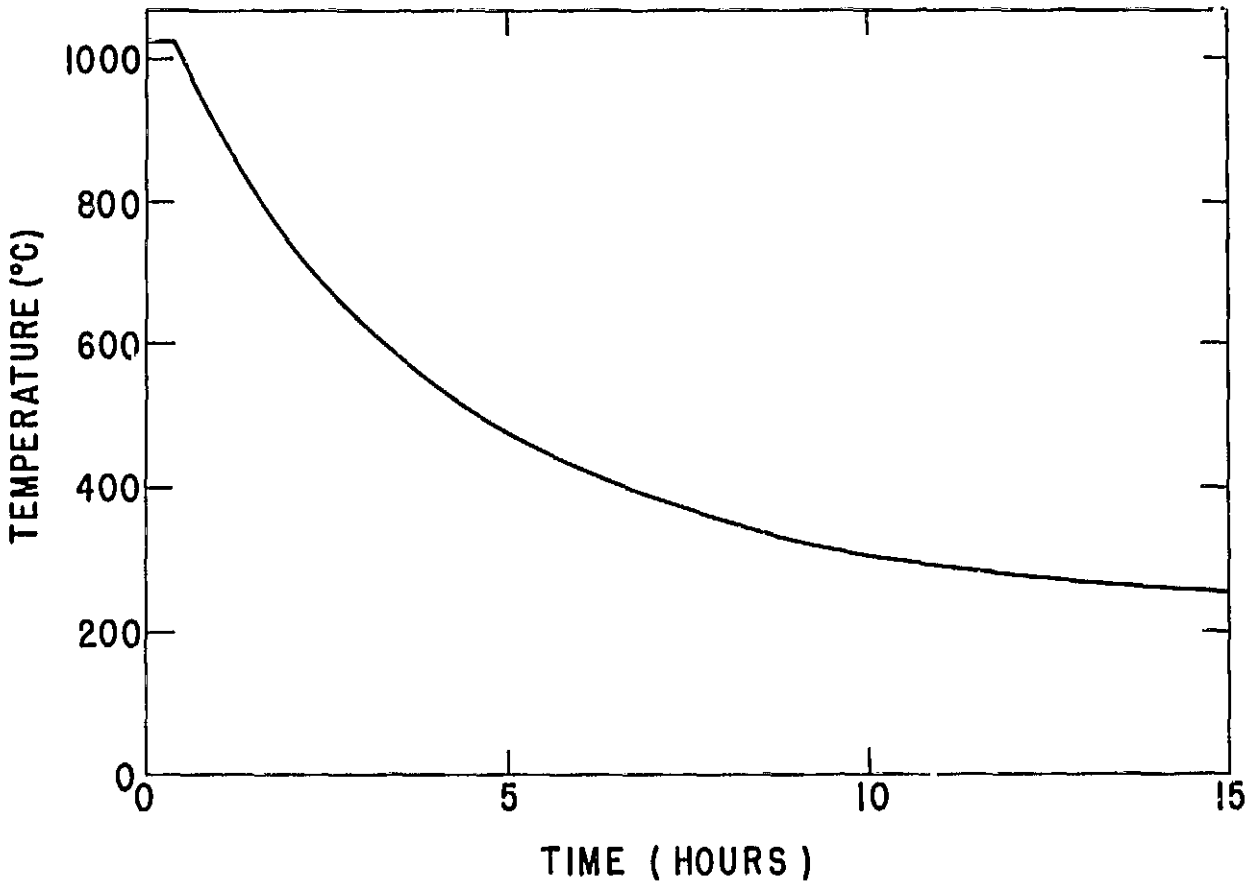


Fig. 25 Temperature-time profile of slow cool cycle.

before the Si_3N_4 etch to maintain cleanliness. At this point, Si_3N_4 remains on the wafer in those areas which will end up as mesa Schottky diodes.

5.7 Mesa Formation

We investigated two methods of mesa formation; oxide etching and acid etching. In the former a 2μ layer of SiO_2 is grown upon the exposed Si areas by means of a high-temperature long steam oxidation. This layer is then removed by a buffered HF etch. The oxidation rate of Si_3N_4 is very slow as compared with that of Si and a layer of Si_3N_4 1500Å is adequate to prevent the Si underneath it from being oxidized. The thickness of Si removed is 40 percent of the oxide thickness, so this procedure gives a mesa 8000Å high. The second method was simply to etch the Si_3N_4 patterned wafers in an acid bath containing HF and HNO_3 in the ratios 1:20. In this case too, the Si_3N_4 is essentially not attacked by the etch and protects the silicon lying beneath it. The unprotected Si, however, is attacked by this etch. This etch is slow (~2 μ/min) and not selective so a smooth surface is obtained. Etch times were chosen to etch down through the epitaxy. For the final devices the etch times were 5 to 7 minutes.

We found no advantage to the oxide etch over the acid etch, and since it took longer and required thicker Si_3N_4 layers we dropped it after satisfying ourselves that the acid etch procedure worked.

5.8 Passivation

A passivating oxide approximately 5000Å thick is next grown upon the mesa sides. This is done by means of a 3.5 hour wet oxidation followed by a 0.5 hour dry O_2 oxidation, both performed at 1000°C.

5.9 Mesa Strip

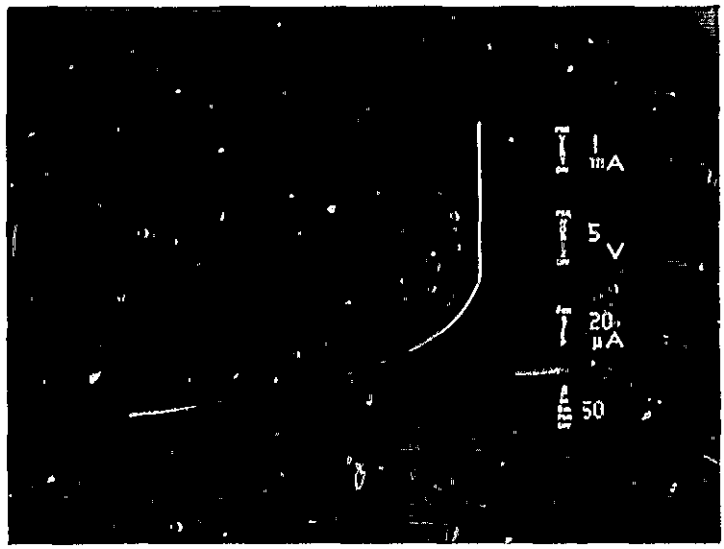
The wafer is now ready for barrier formation except for the fact that the barrier region is still covered by the original nitride and oxide layers. These are etched away by means of the usual hot phosphoric acid and buffered hydrofluoric acid etches.

We found that at this point it is advantageous to etch between 1μ and 2μ off the mesa top. This step was originally introduced at an earlier stage of process definition when the sequence was somewhat different. The getter cycle then followed mesa formation and passivating oxidation. With this procedure, every diode subsequently fabricated was a short. We found it necessary to deposit an additional SiO_2 layer, 6000Å thick, over the already formed mesa tops and edges in order to protect them from the $POCl_3$ environment of the getter furnace. Even with this additional protection, however, 5 percent to 10 percent of the diodes formed still showed large ohmic shunt leakage which saturated with increasing reverse bias.

These experiments were performed with diodes of 10^{-2} cm^2 area, whereas 25 amp diodes require approximately 0.5 cm^2 area. Assuming that the density of shorts is randomly distributed over the area of any wafer even a 95 percent yield of small diodes results in only 7 percent good large diodes.

An example of this behavior is shown in Fig. 26. This diode shows reverse leakage current which, at the outset, increases linearly with applied voltage and which finally saturates at a level far higher than the thermionic value. This behavior may be understood by means of the model shown in Fig. 27.

We believe that the protective 6000Å SiO_2 cover is not perfect and that some component of the phosphorus-rich gas mixture of the $POCl_3$ getter furnace penetrates it, attacks the Si_3N_4 on the mesa top, and dopes the silicon surface heavily n type. This very likely occurs at mesa edges, since this is the place where mechanical stresses arising from thermal expansion and geometry are greatest. When the mesa is subsequently stripped and the Schottky barrier formed, contact is also made to the heavily doped n+ region. This contact is a tunneling Schottky and is thus ohmic. Its conductance at low applied voltage is determined by the spreading resistance from the



$$\rho = 2.5 \ \Omega - CM$$

$$a = \frac{\rho}{2R} = 5\mu$$

Fig. 26 Current-voltage characteristic of a diode exhibiting a getter-induced ohmic barrier shunt.

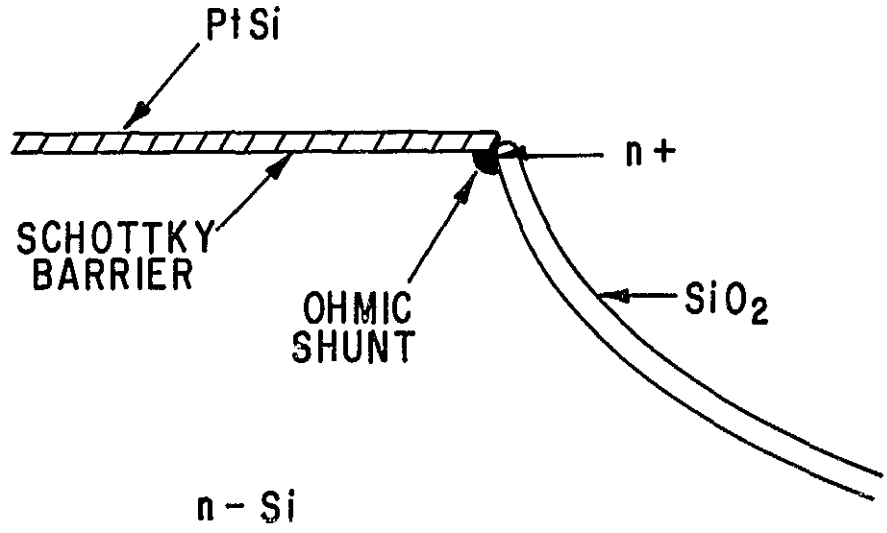


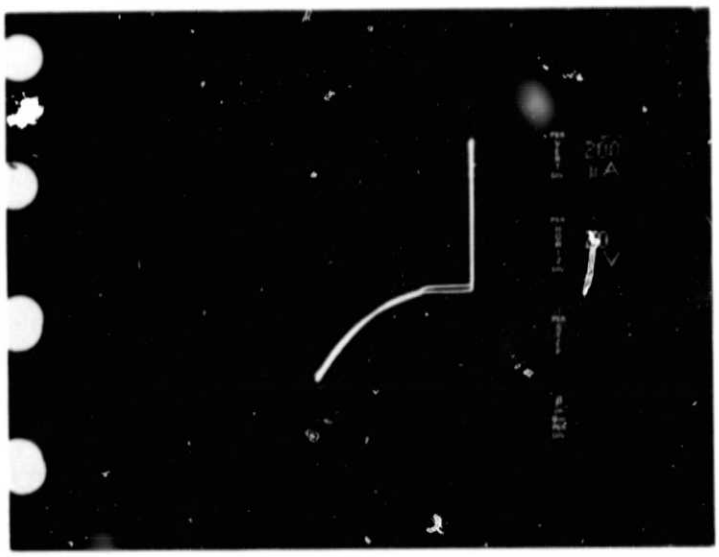
Fig. 27 Idealized model of barrier shunt.

heavily doped region. The current saturates due to the pinching off of the conductance path by the spreading depletion width of the proper Schottky region. The specifics of Fig. 26 are consistent with this model. The shunt resistance calculated from the initial slope at V = 0 is $2.5 \times 10^3 \Omega$ which corresponds to the spreading resistance of a pinhole 5μ in diameter. It is noteworthy that the current saturates at about 50 volts which corresponds to the depletion width of the 2.5 Ω-cm material.

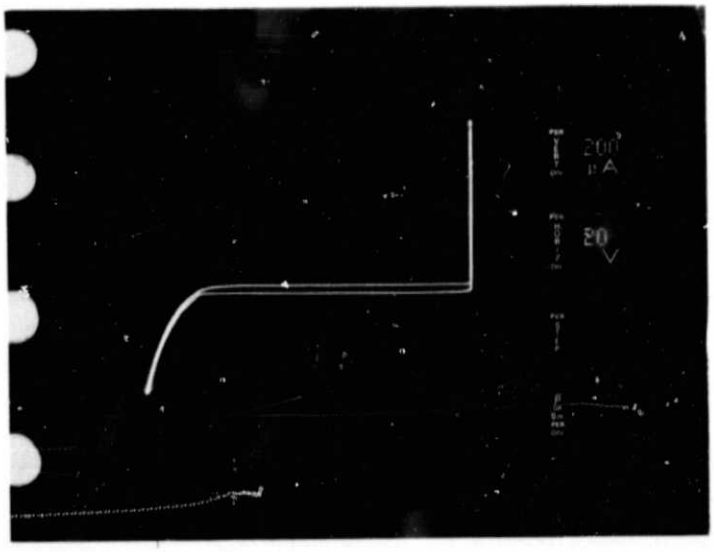
This difficulty was completely eliminated for the 10^{-2} cm^2 area diodes by adding the step of etching 1μ to 2μ off the mesa tops after the getter cycle and before the barrier formation. This step etches away any heavily doped regions which may occur, thus removing the cause of the short. This etch step was found to be useful even in the absence of any n+ shunts. An example is shown in Fig. 28 which compares reverse characteristics obtained from typical diodes from two halves of a single wafer. The upper trace, characteristic of diodes which have been gettered, slow cooled but not mesa etched, shows no leakage at low values of reverse bias but exhibits microplasma breakdown starting at 30 volts. The mesa etched devices, on the other hand, do not show any reverse current other than thermionic out to 160 volts where they break down via microplasmas. Evidently our getter cycle does not dissociate and remove all of the heavy metal complexes that are located near the original Si-SiO_2 interface. Etching away the Si near the interface clearly removes the impurities.

The effects of the getter cycle and mesa etching may be seen in statistical fashion by means of Figs. 29, 30, and 31. Several otherwise identical wafers were processed in slightly different ways in an attempt to define the most nearly optimal procedure. The reverse bias corresponding to 1 ma leakage (10^{-1} amp/cm^2) was measured for each diode. The results are plotted in Fig. 29. Samples 881 and 881E are two halves of a wafer that was gettered but not slow cooled. Sample 881E was mesa etched before barrier formation whereas 881 was not. It is clear that the mesa etching was useful in shifting the distribution to higher breakdown voltages. Samples 883E and 882E were both slow cooled and mesa etched differing only in that the phosphorous glass remained on 882E until after the Pt Si deposition, whereas 883 had its phosphorous glass removed before Pt-Si formation. The time of removal of the phosphorous glass doesn't seem to make any difference. A comparison of 882E or 883E with 881E, however, shows that slow cooling is beneficial. Figure 30 shows a similar distribution for 1.3Ω material having lower bulk breakdown which was gettered, slow cooled, and mesa etched. These results are quite similar to those of 883E or 882E. Another comparison is shown in Fig. 31. Sample 951 was ungettered but mesa etched, and 952 was gettered, slow cooled, and mesa etched. Again, the combination of gettering, slow cooling, and mesa etching gives the superior results.

The process was thus defined by means of experiments on diodes with 10^{-2} cm^2 area. The original sequence had the getter cycle appearing after the passivating oxidation. In the course of fabricating the large 25 amp size



GETTERED
SLOW COOLED
NO MESA ETCH



GETTERED
SLOW COOLED
MESA ETCHED

Fig. 28 Comparison of two diodes showing the effects of mesa etching.

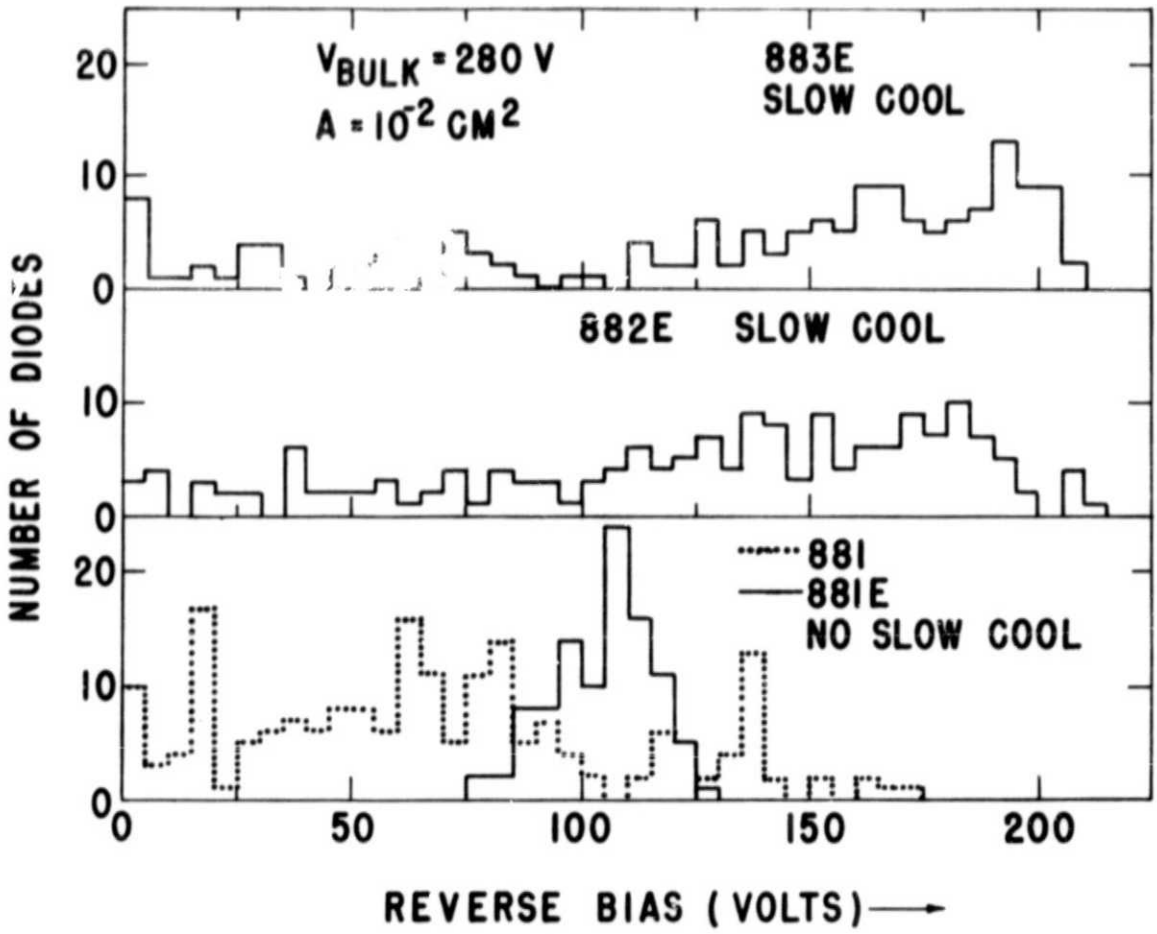


Fig. 29 Histograms of breakdown voltage showing the effects of slow cooling and mesa etching.

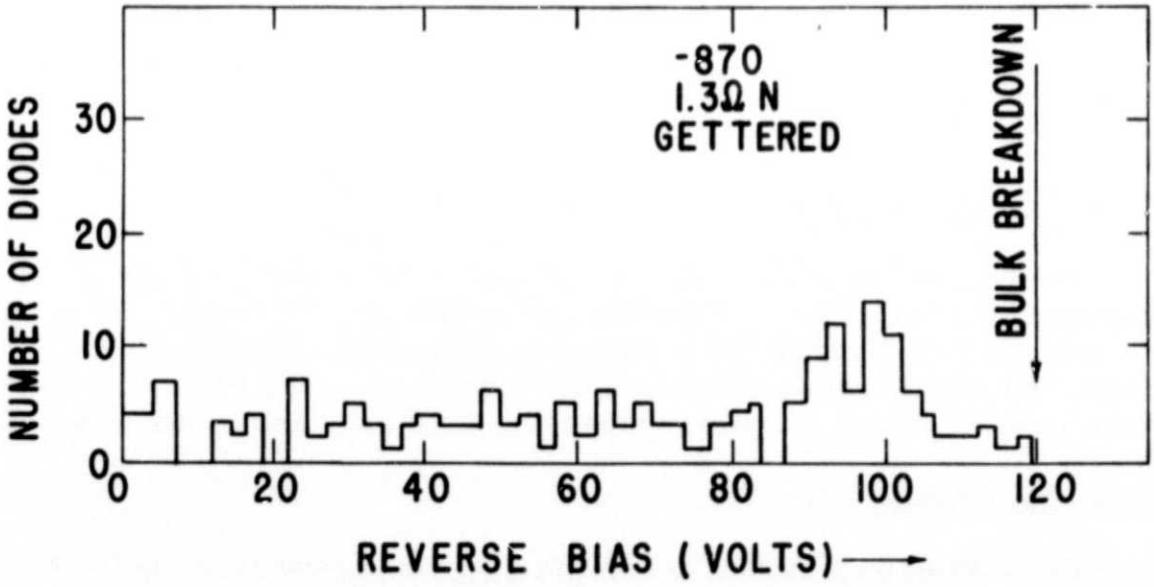


Fig. 30 Distribution of breakdown voltages for 1.3 Ω-cm material.

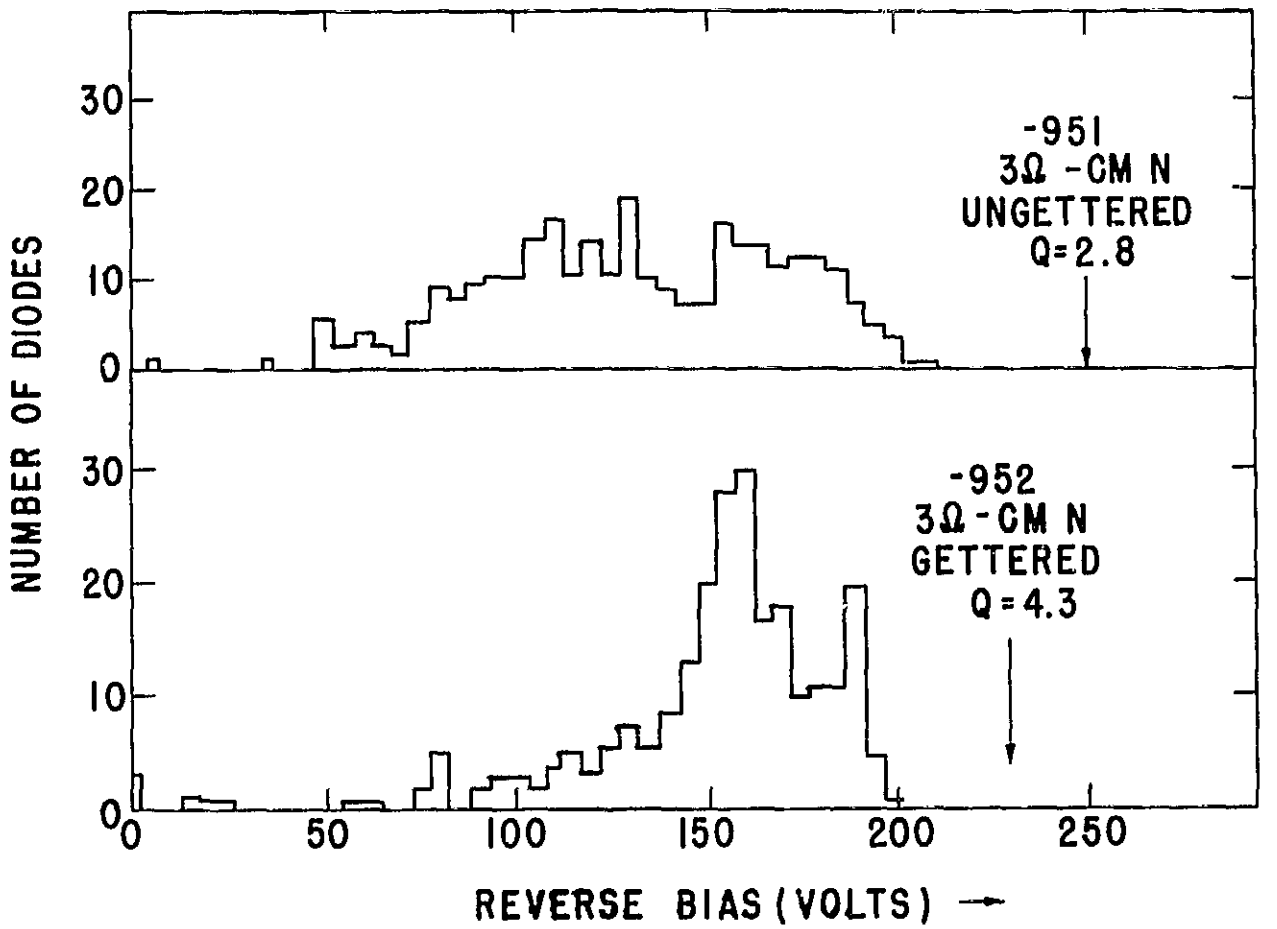


Fig. 31 Histograms showing the effects of gettering upon the distribution of breakdown voltages.

devices, however, we found that yields of large diodes and diode quality were greatly improved by gettering before mesa definition. This, then, is the process as finally defined.

5.10 Barrier Formation

The barrier is now formed by sputtering 600Å of Pt onto the wafer while keeping the wafer at an elevated temperature. The Pt reacts with the exposed silicon on the mesa tops and the barrier is formed in a way which automatically aligns the metal contact with the SiO_2 passivation. The Pt-Si Schottky metallization covers the entire mesa top, thus preventing edge breakdown.

5.11 Aqua Regia Etch

The unreacted platinum is removed by etching the wafer in hot (50°C) aqua regia; the platinum is dissolved while the Pt-Si is unaffected.

5.12 Final Metallization

The Schottky contact is now built up with successive depositions of 5000Å of Mo, 1μ of Ni and 1000Å of silver. The back of the wafer is metallized with 1000Å of Ti and 2μ of gold. The upper metallizations were chosen for the following reasons: Mo to seal and protect the thin barrier metal, Ni to serve as a solderable metal and also to act as a barrier to solder penetration, and Ag to prevent the oxidation of the Ni surface. The metallization on the substrate allows the diode to be eutectic bonded to tungsten. The upper metallization is then patterned photolithographically. The etch used is HNO_3: H_2SO_4: H_2O in the ratios 1: 1: 3.

5.13 Cleave

Diodes are then separated by conventional cleaving.

5.14 Assembly

Rectifier assembly proceeded in two stages. The final 25 amp diodes have an active area of 0.6 cm^2(0.307 in)^2 the chip being (0.333 in)^2. Completed, pretested chips were first eutectic bonded to 0.460 inch diameter tungsten backup plates at a bonding temperature of 500°C. The resulting subassembly is easy to handle and is thus easily checked for reverse characteristics at this stage. We considered this check to be a desirable one to do since this temperature is the highest one that the completed diode sees in assembly. We anticipated that this cycle would result in significant losses, and wanted to discard bad diodes before final assembly. We were pleasantly surprised, however, with almost perfect yields through this step.

The completed tested subassembly is then mounted to its copper header and has its top lead applied. A completed assembly is shown schematically in Fig. 32. A tungsten top piece (0.280 in)^2 is used to spread the current from the copper lead-in wire to the metallized Schottky barrier. The solders used were (a) Au-Sn eutectic to bond the tungsten backup plate to the copper stud, (b) high-lead soft solder to bond the top tungsten piece to the metallized Schottky diode, and (c) either the soft solder or the Au-Sn to solder the copper lead to the top tungsten piece. The entire assembly of Fig. 32 was soldered together in one step by heating it in hydrogen to a temperature of 350°C. The diode is now ready for standard hermetic sealing. We chose, instead, to encapsulate the mounted diode in silicone rubber, leaving the top Cu lead accessible for measurements. This was done in order to avoid any problems connected with possible contact resistance between the copper lead and the crimped stainless steel tube of the standard package.

We found it possible to assemble large-area mesa Schottky diodes by means of the procedure described without degrading their reverse bias characteristics in any serious way. Figure 33 shows the reverse bias characteristics of two diodes both in chip form and after final assembly. Diode 6-1-5

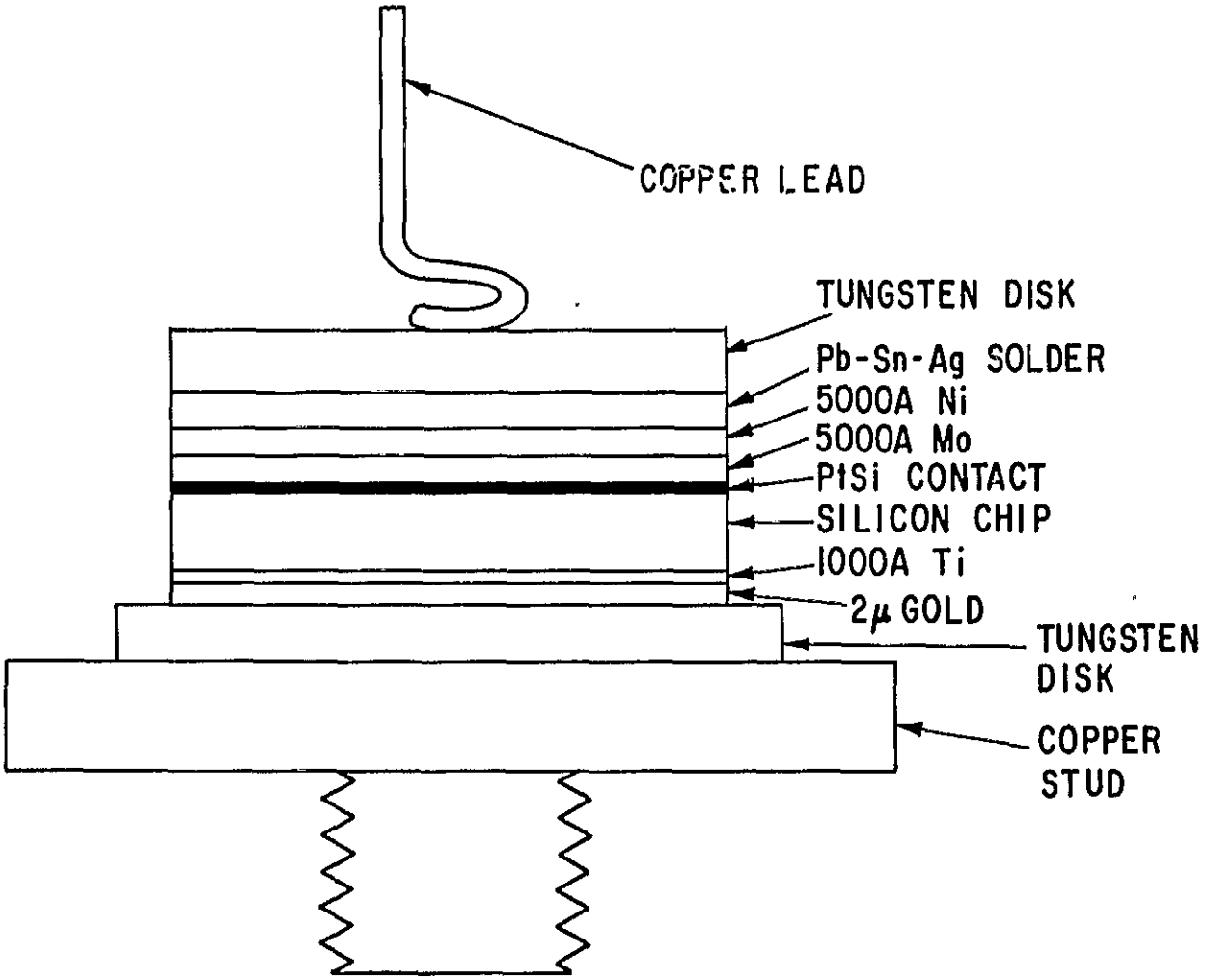
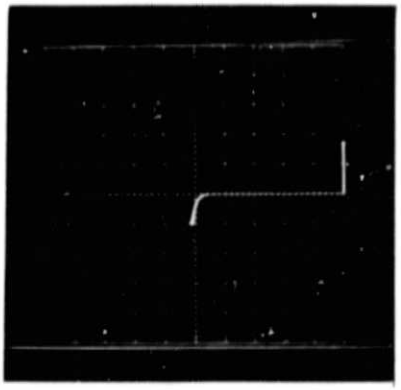
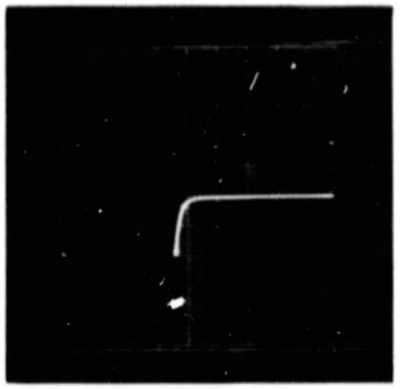


Fig. 32 Schematic view of diode assembly.

shows no change in leakage current and no effects of assembly except for a slightly higher final breakdown voltage. This is likely due to the field shielding effect of the overlapping contact metallization. Diode 17-1(1, 3) also exhibits an increase of breakdown voltage in assembled form. It also shows a slight increase in leakage beyond 70 volts after assembly. As may be seen from the characteristic jogs in the I-V trace of Fig. 33 (d), this current is due to the onset of microplasma breakdown. We do not understand the reasons for the appearance of microplasmas after assembly, but it is not a common occurrence. In any event, this additional leakage current is not excessive and does not appear to be the factor determining the diode breakdown.

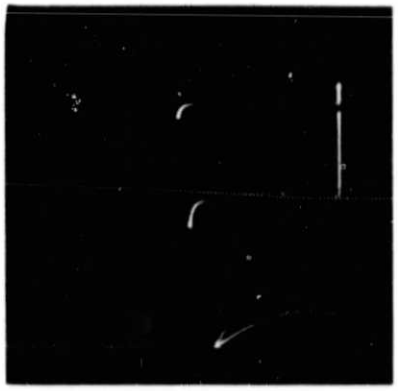


20 VOLT/DIV
A. 6-1-5 BEFORE ASSEMBLY



10 ma/DIV

20 VOLT/ DIV
B. 6-1-5 AFTER ASSEMBLY



20 VOLT/ DIV
C. 17-1 (1,3) BEFORE ASSEMBLY

10 ma/DIV

1 ma/DIV

0.1 ma/DIV

20 VOLT/ DIV
D. 17-1 (1,3) AFTER ASSEMBLY

Fig. 33 Comparison of diode reverse characteristics before and after final assembly.

Section 6

RESULTS OBTAINED ON LARGE AREA DIODES

6.1 Reverse Bias--Yield and Quality

While barrier parameters were determined from experiments done upon diodes having area 10^{-3} cm^2 and wafer processing procedures were developed using diodes of 10^{-2} cm^2 area, the bulk of our actual wafer fabrication was done for diodes having 0.6 cm^2 area. This is the size appropriate for the 25 amp, 200 volt diode of the specification as has been described above. Epitaxial material varying in resistivity from 0.8 to 3.4 Ω-cm was processed. Sixteen lots of 3-6 wafers per lot have been processed in all. The major focus of effort in the fabrication of large diodes has been on the improvement of reverse characteristics.

The mesa process as initially developed with small (10^{-2} cm^2) diodes was not capable of producing high yields of high quality diodes. Initial yields were at best 1-4 diodes per wafer out of a possible 14 per 2-inch wafer, and the reverse characteristics of these diodes were typically soft as shown in Fig. 34 (a), or leaky from the outset as shown in Fig. 34 (b). An example of one such early wafer is shown in Fig. 35. The I-V characteristics of each of the 14 diodes on the wafer is shown in the picture at the position corresponding to its actual location on the wafer. Most of the diodes break down at low voltages with only four having blocking capability greater than 50 volts. A room temperature reverse bias characteristic of one of these diodes is shown in Fig. 34 (b) where a nonthermionic component of current is seen even at low voltage. This extra current is not very temperature dependent, increasing, as may be seen in Fig. 36, by no more than a factor of 2 at 107°C. While this type of leakage was thus not overly serious insofar as the 100°C reverse leakage contract specifications were concerned, we felt it desirable to eliminate it and achieve more nearly ideal room temperature reverse currents. Small adjustments were made in the processing sequence which had the eventual result of improving yield, uniformity, and diode quality. The final process sequence resulting was described above in Sec. 5.

The last three lots were all processed in a disciplined manner. No process variations were made and material was put through in a sustained manner in order to get some feeling for reproducibility and yield. A typical wafer from these three last lots is shown in Fig. 37 (a) and the best wafer is shown in Fig. 37 (b). These wafers show that high-quality diodes can be fabricated even in this large diode size at yields greater than 70 percent.

Figure 38 shows the distribution of breakdown voltages for all seven wafers of these last three lots. In no case was the yield of diodes having breakdown voltage above 100 volts less than 50 percent. For the best wafer

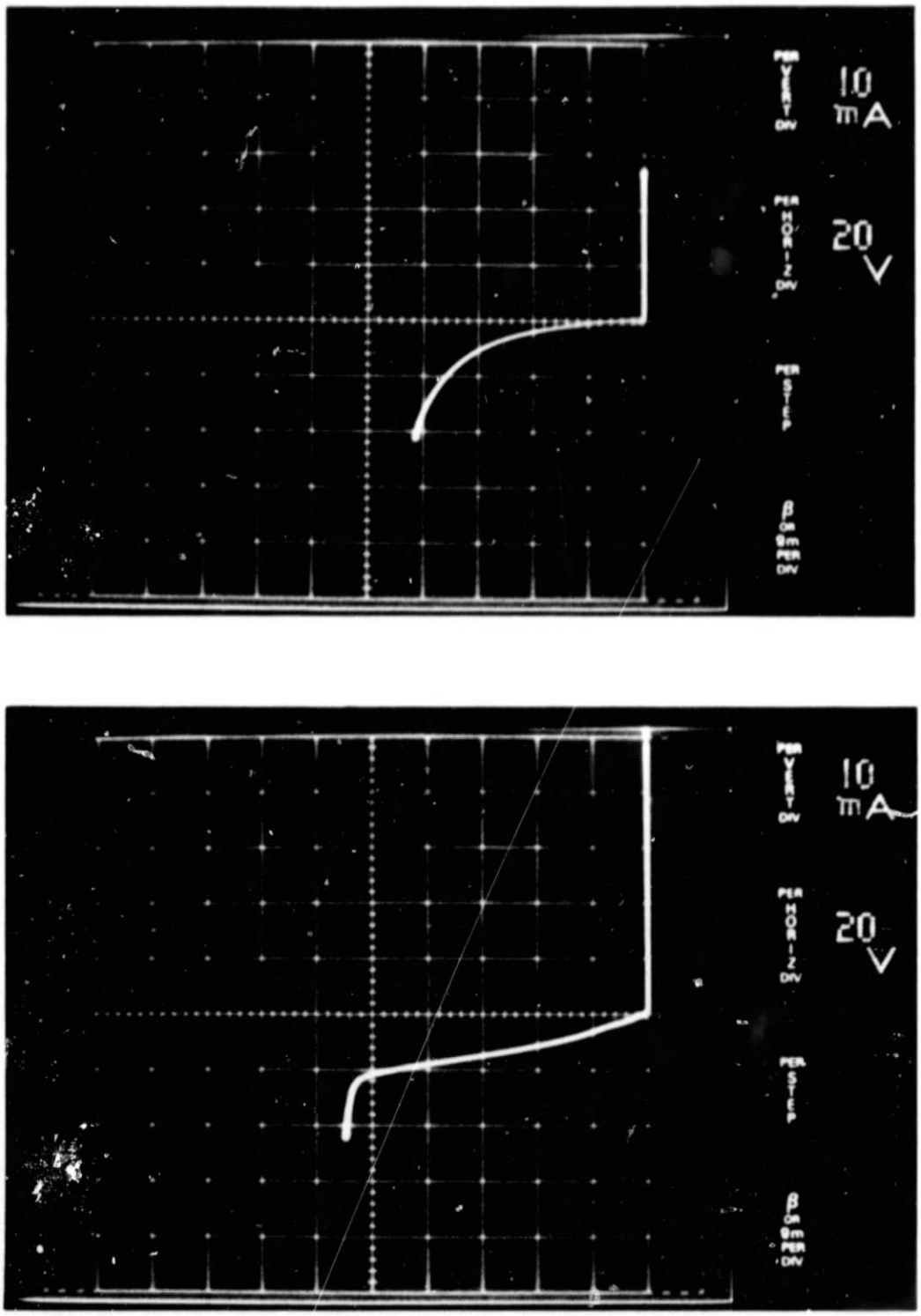


Fig. 34 Reverse characteristics illustrating soft characteristics and excess leakage at low voltage.

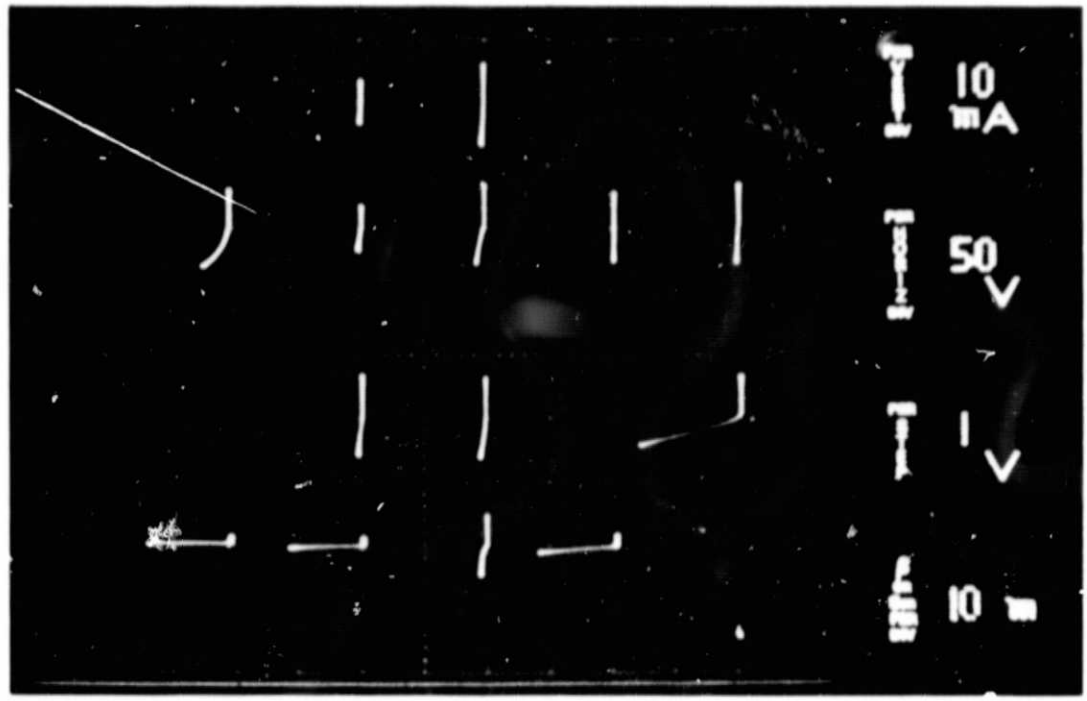


Fig. 35 Spatial distribution of reverse diode characteristics for a wafer from one of the early lots.

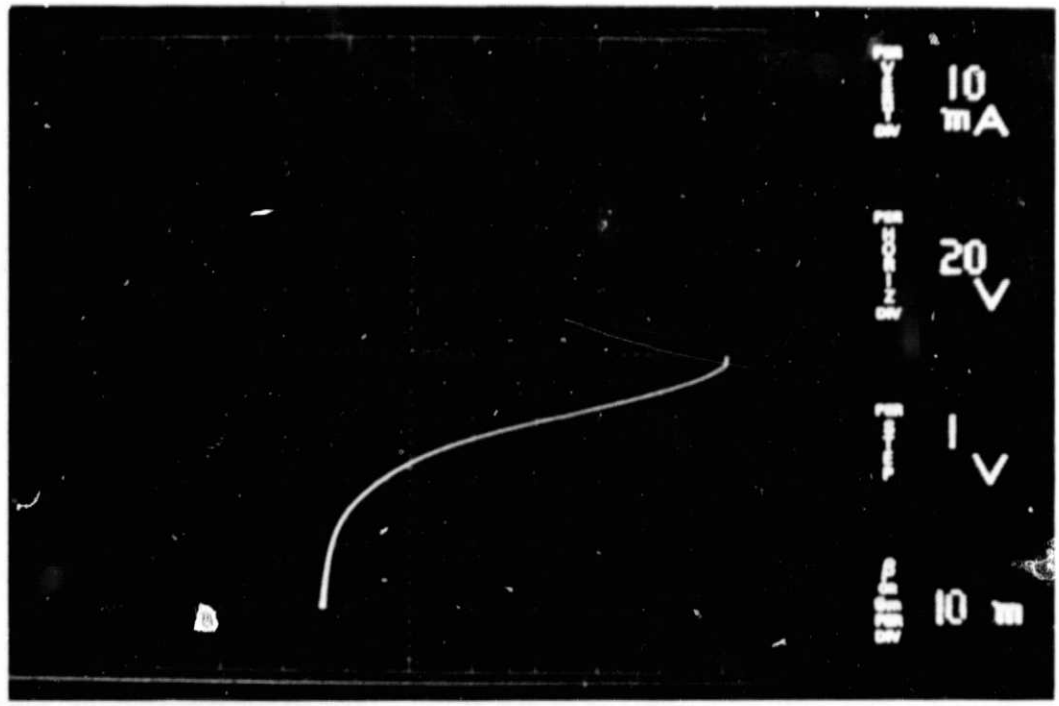


Fig. 36 Reverse bias characteristic at 107°C for the leaky diode of Fig. 34 (b). The leakage current is essentially unchanged from its room temperature value.

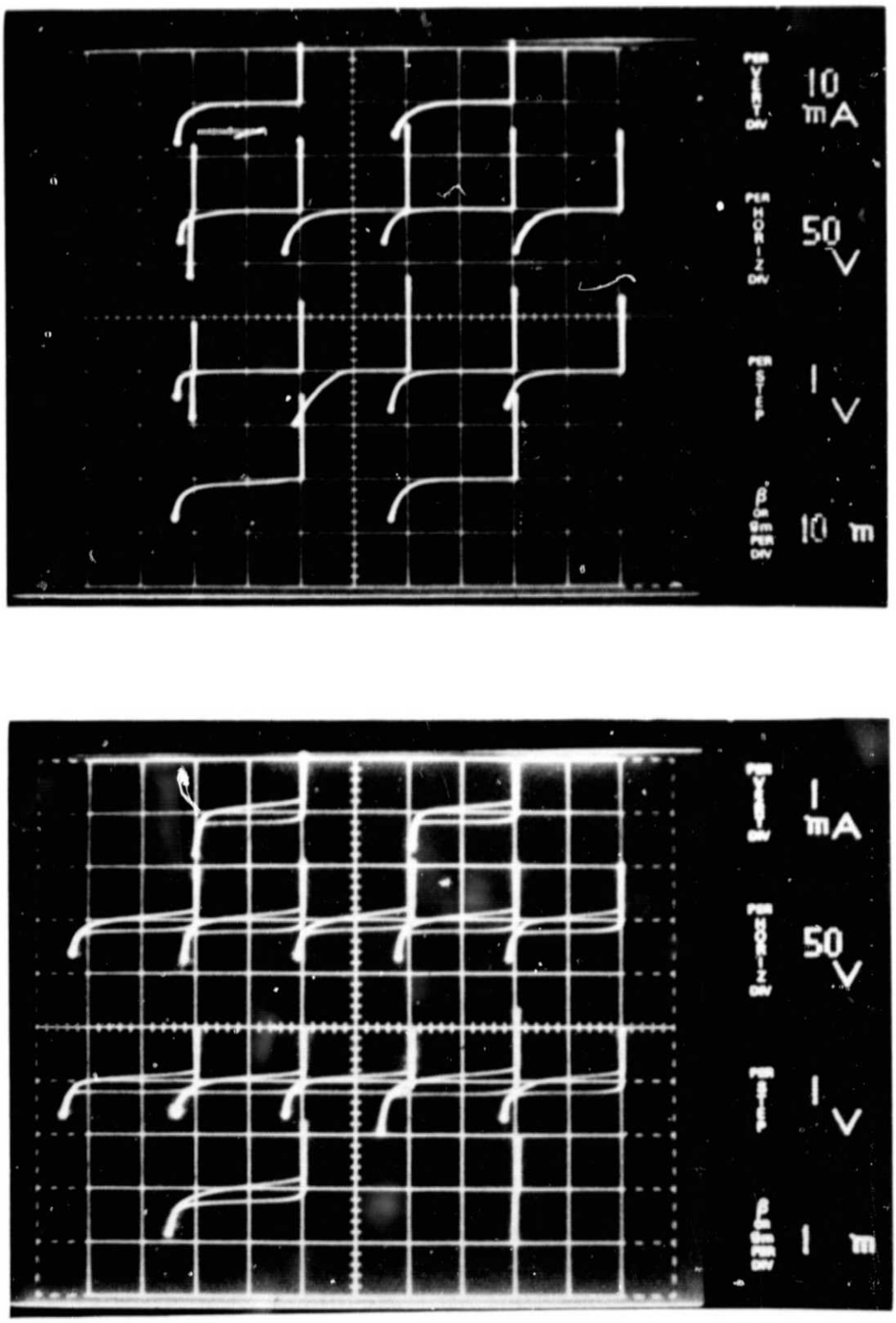


Fig. 37 Wafer maps of reverse diode characteristics for a typical and the best wafer from the later lots.

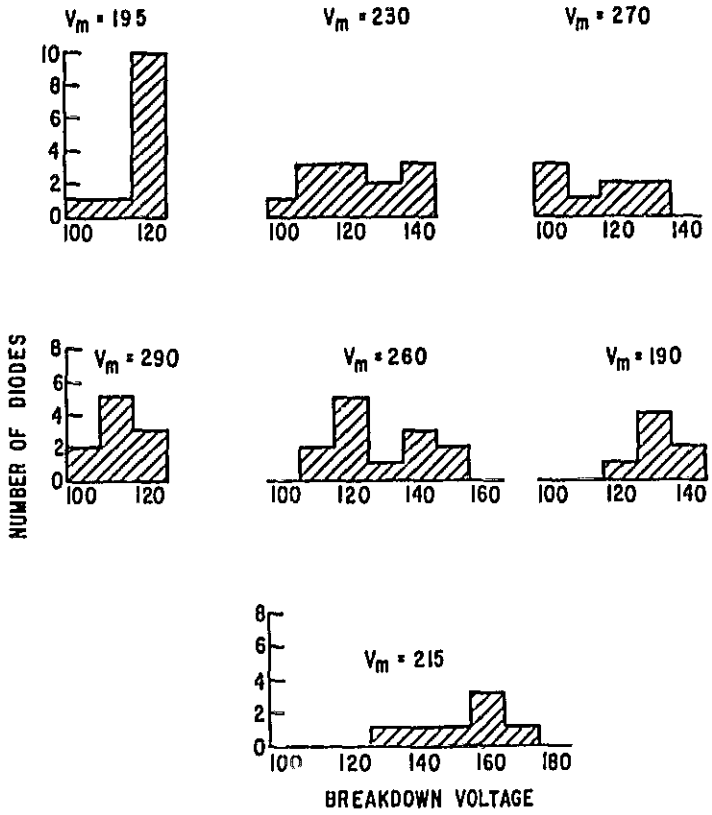


Fig. 38 Distribution of breakdown voltages for the wafers of the later lots.

the yield was 93 percent. The measured breakdown voltage distributions of some typical early diodes and those of the last three lots are shown again in Fig. 39 where a comparison is made between them and V_{max}, the theoretical maximum value. V_{max} is the microplasma free bulk avalanche breakdown voltage corresponding to the resistivity of each diode. There is some indication in Fig. 39 that it becomes progressively more difficult to achieve large fractions of V_{max} in practice as the voltage rating increases. The results of the early lots cluster near the line $V = 0.5\ V_{max}$ for diode voltages greater than 100 volts. The last three lots are somewhat better with some wafers exhibiting diode breakdown voltages that exceed 70 percent of V_{max}.

Many of the diodes exhibited "pushiness" in their room temperature reverse bias characteristics. That is, the device avalanche breakdown slowly moves out to higher values through the course of measurement, finally saturating after a minute or so at values 10 to 20 volts higher than at the outset. This is a well-known phenomenon in reverse biased passivated p-n junctions. It is characteristic of diodes where for some reason or other, avalanche multiplication takes place at the silicon surface where the p-n junction intersects the SiO_2 passivation. As the multiplication process continues, electrons from the avalanching region are accelerated towards the passivating oxide, tunnel into it, and are trapped. These trapped electrons act to reduce

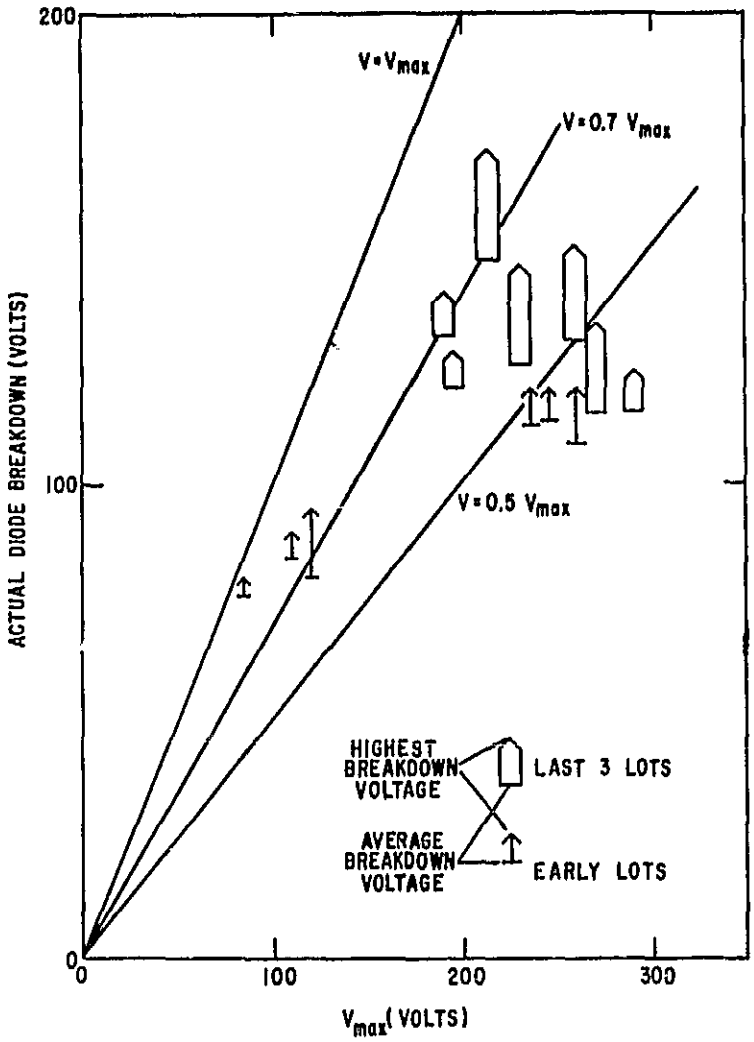


Fig. 39 Comparison of actual measured diode breakdown voltages with theoretical maxima.

the local electric field, thereby allowing greater applied bias to be applied before avalanche occurs. We conclude that our " pushy" mesa Schottky diodes likewise have their highest electric field region at the intersection of the Schottky barrier with the passivating oxidation.

When avalanche breakdown occurs it takes place there, right at the periphery of the mesa top. We do not know the reason for this field enhancement at the diode periphery. A possible cause, however, is an increased concentration of dopant near the passivated silicon surface produced during the step of mesa passivation due to rejection of phosphorus from the growing oxide. Fast, wet oxidations, such as we have used in our mesa passivation step, enhance this phosphorus pileup. Additional work is required to clarify this point. If surface pileup is indeed at fault, its elimination may extend practical values of breakdown voltage to larger fractions of V_{max}.

The reverse characteristics of two diodes are shown in Figs. 40 and 41. Figure 40 is typical of the results obtained in our early lots, and Fig. 41 is typical of the last three lots. Results are shown for both room temperature and for 125°C. The diode of Fig. 41 shows very low leakage at room temperature and an ideal characteristic at 125°C out to approximately 100 volts reverse bias. The reverse current begins at 1 ma near V = 0 and increases to 11 ma at 100 volts. These values are completely accounted for by calculating the thermionic emission current over the Schottky barrier. The low voltage value of 1 ma corresponds to thermionic current over a barrier of 0.79 eV as determined by forward current measurements made on test diodes on the same wafer. The reverse thermionic current increases to 7 ma at 80 volts reverse bias due to 55 mv of barrier lowering associated with the barrier field of 1.8×10^5 v/cm at 80 volts. Above 80 volts, additional nonideal current appears and the diode finally breaks down at 120 volts. Thermionic barrier current is also seen in Fig. 40 (b). It is the same magnitude as that in Fig. 41, except here it is added to the nonideal leakage component which appears to be unchanged from room temperature. All of the good diodes from the last three lots as well as many of the early diodes exhibited theoretical saturation current out to electric fields of approximately 2×10^5 v/cm for temperatures above 100°C.

In the course of our fabrication of large diodes we processed epitaxial material produced in many separate runs obtained from three entirely different sources. It is not possible for us to come to any precise conclusions about the correlation between epitaxial quality and reverse breakdown. Nevertheless, some comments are in order. As was stated above, we were unable to get reasonable yields from material supplied by one of our sources while getting good results from other suppliers' wafers processed in the same way. We conclude from this that there is some minimum level of epitaxial crystalline quality and purity required for the successful fabrication of mesa Schottky diodes. There was no explicit specification on the crystalline quality of the other two suppliers' material. This leads us to the belief that ordinary, production run material of reasonable quality is adequate for high yield fabrication, and ultrahigh quality is unnecessary.

A specific example buttressing this belief is given in Fig. 42 where photomicrographs of several different regions of diode (1, 2) of wafer 17-1 are shown. At least three different kinds of crystalline defect are present in this diode as well as a process induced defect. Dislocations occurring near and at the mesa edge may be seen in Fig. 42 (c); dislocation lines are visible in 42 (d); and unidentified fine scale growth defect is shown in 42 (a); and a hole in the mesa caused by a pinhole in the Si_3N_4 layer is evident in Fig. 42 (b). Notwithstanding all these defects, this diode is the best diode of wafer 17-1, exhibiting voltage breakdown greater than 130 volts. This may be seen in Fig. 43 (a). Needless to say, there are defects that will result in shorted diodes. Each of the diodes of wafer 17-1 that exhibit low voltage breakdown; (4, 1), (4, 2), and (5, 3), has a gross defect associated

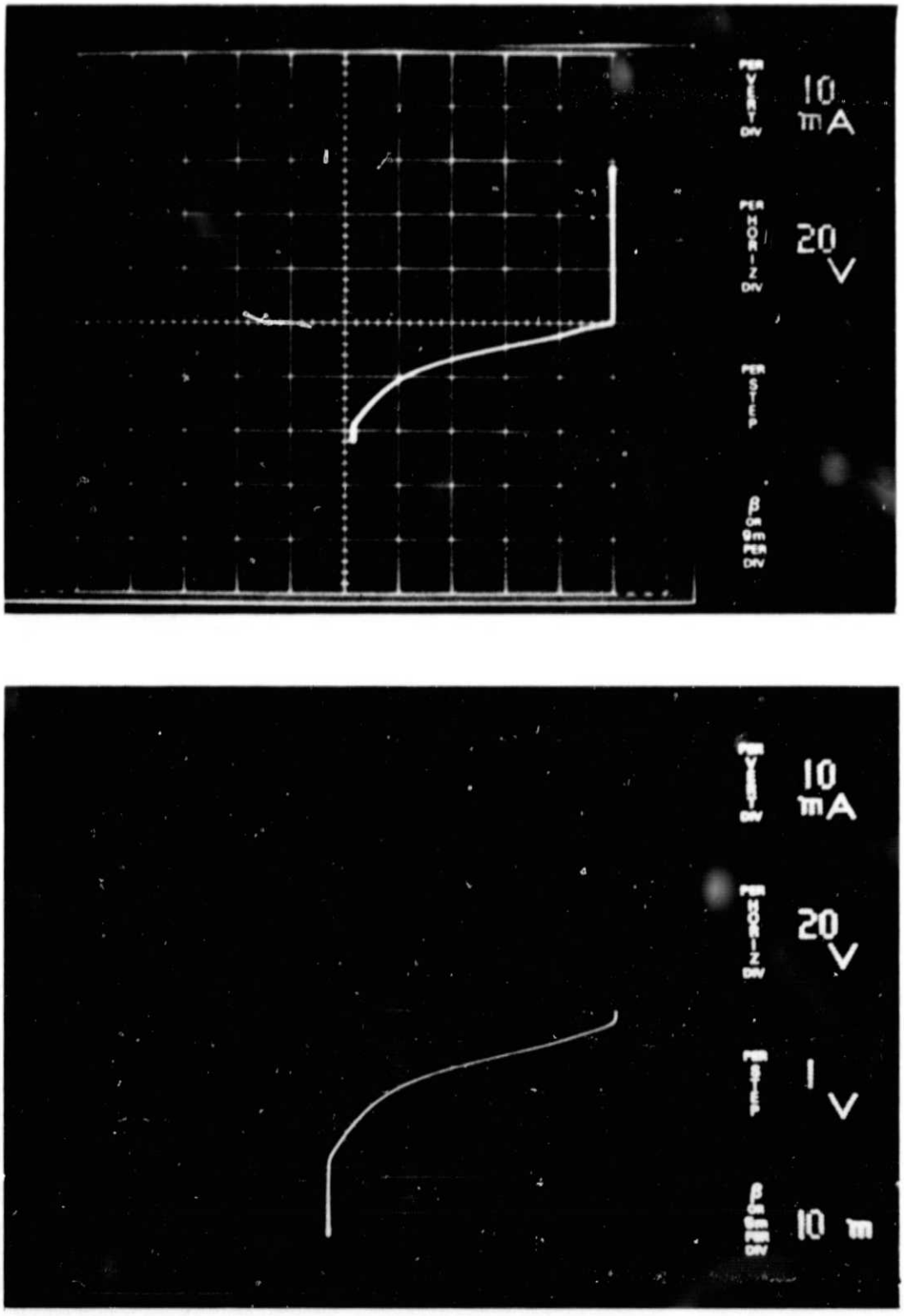


Fig. 40 Comparison of room temperature leakage of a leaky diode with that at 125°C.

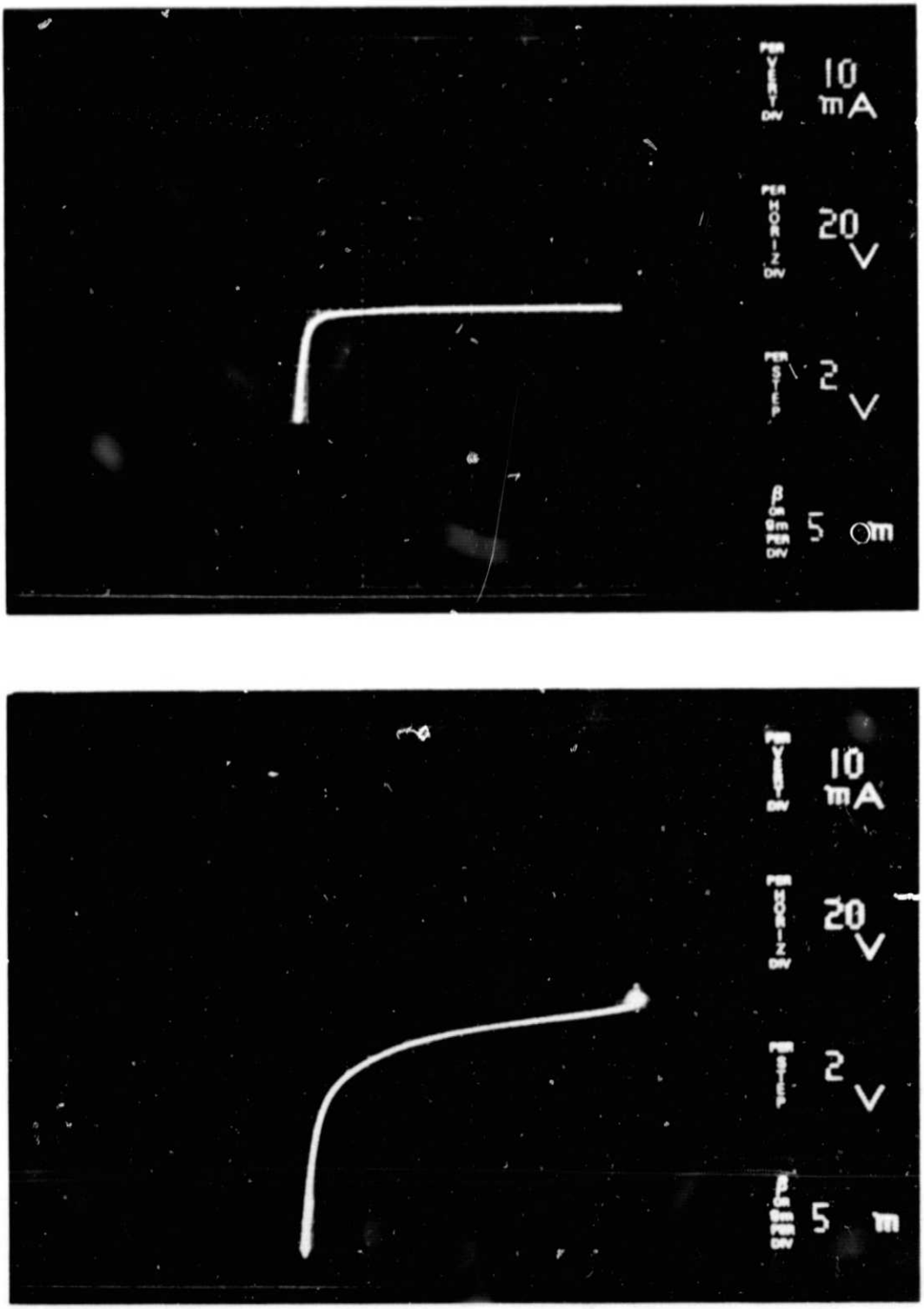
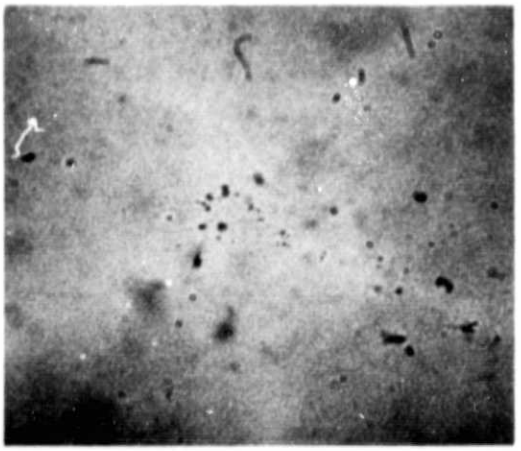


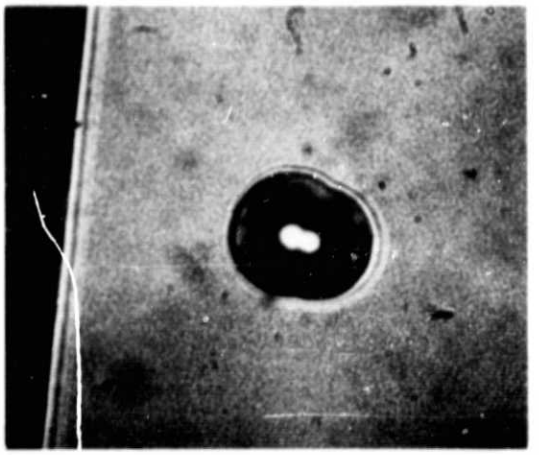
Fig. 41 Room temperature and 125°C reverse characteristics for nearly ideal diode.

WAFER 17-1
(700X)

DIODE 1, 2

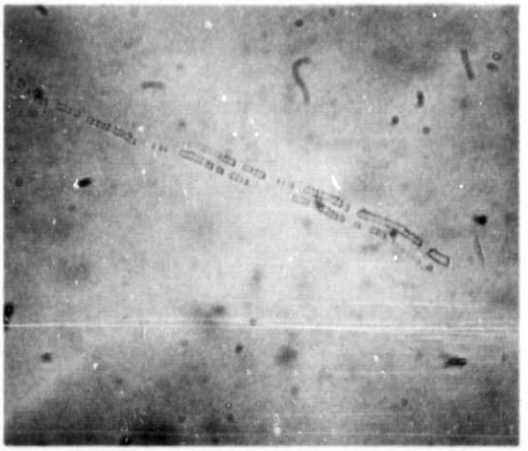


a) FINE GROWTH DEFECT



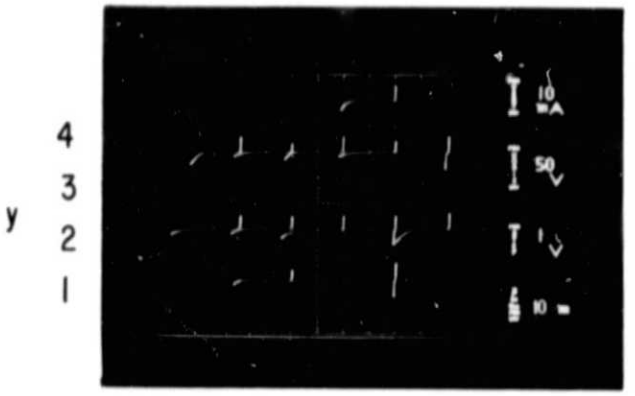
b) PINHOLE IN Si_3N_4

c) DISLOCATIONS

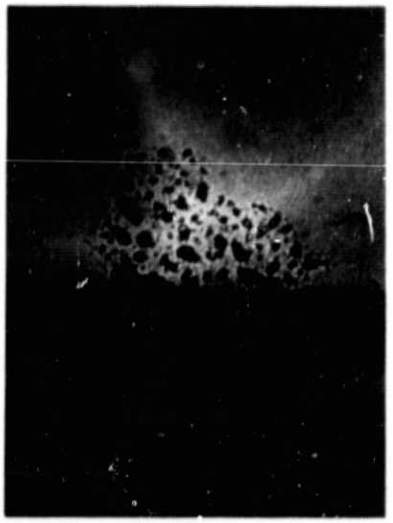


d) EXTENDED DISLOCATION NETWORK

Fig. 42 Photomicrographs of various crystalline defects that do not contribute leakage current.



a) WAFER 17-1



b) DIODE 5, 3 CHIPPED DIODE (700X)

c) DIODE 4, 1 GROWTH HILLOCK (700 X)

d) DIODE 4, 2 EXTENDED DEFECT PRECIPITATES ? (700X)

Fig. 43 Wafer map of reverse diode characteristics for wafer 17-1 and photomicrographs of gross defects in shorted diodes.

with it. Diode (5, 3) has had a corner chipped off [Fig. 43 (b)], diode (4, 1) has an epitaxial growth hillock [Fig. 43 (c)], and (4, 2) shows an assembly of micron-sized defects which may be impurity precipitates localized in a well-defined area [Fig. 43 (d)].

We judged that the major uncertainties as to basic device feasibility were connected with the problems of reverse bias, as discussed above. Reverse bias data are acquired most conveniently and quickly on diodes which have been completely processed but which are still in wafer form. Accordingly, we devoted the bulk of our processing effort to wafer fabrication and were able to assemble only a limited number of finished diodes. It is, unfortunately, impossible to measure the forward characteristics of unmounted diodes. We thus do not have enough experience to be able to project the same kind of yield and quality data for forward as for reverse. We do, however, have quite enough data on assembled diodes to (a) demonstrate device feasibility and (b) indicate problem areas which will require additional effort.

6.2 Forward Characteristics

Detailed forward I-V characteristics for three assembled diodes are given in Figs. 44 and 45. Diode 2-15-3, shown in Fig. 44, was fabricated on 1 Ω-cm epitaxial material 10μ thick. The current increases at room temperature exponentially with applied voltage from 10 μamp to 1 amp forward at the rate of 64 mv per decade. This leads to an "n" value in the

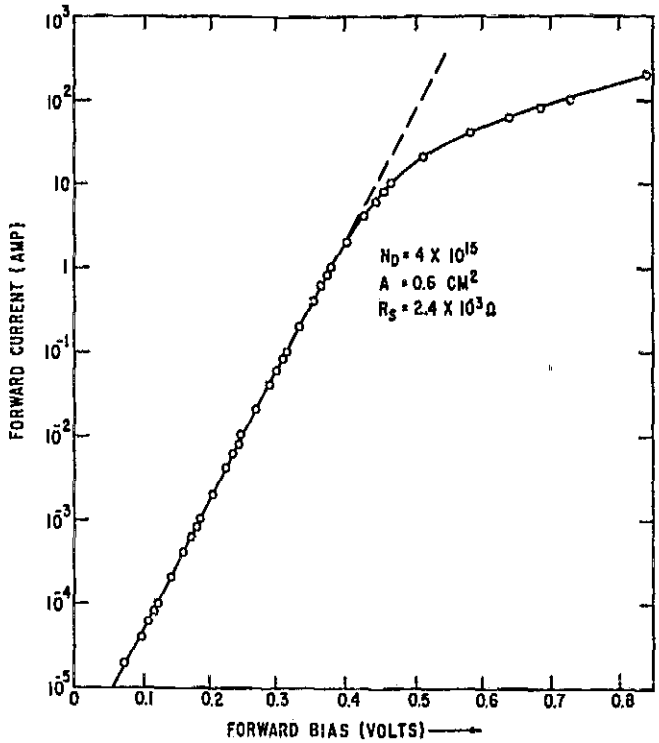


Fig. 44 Forward bias I-V characteristics for relatively heavily doped diode.

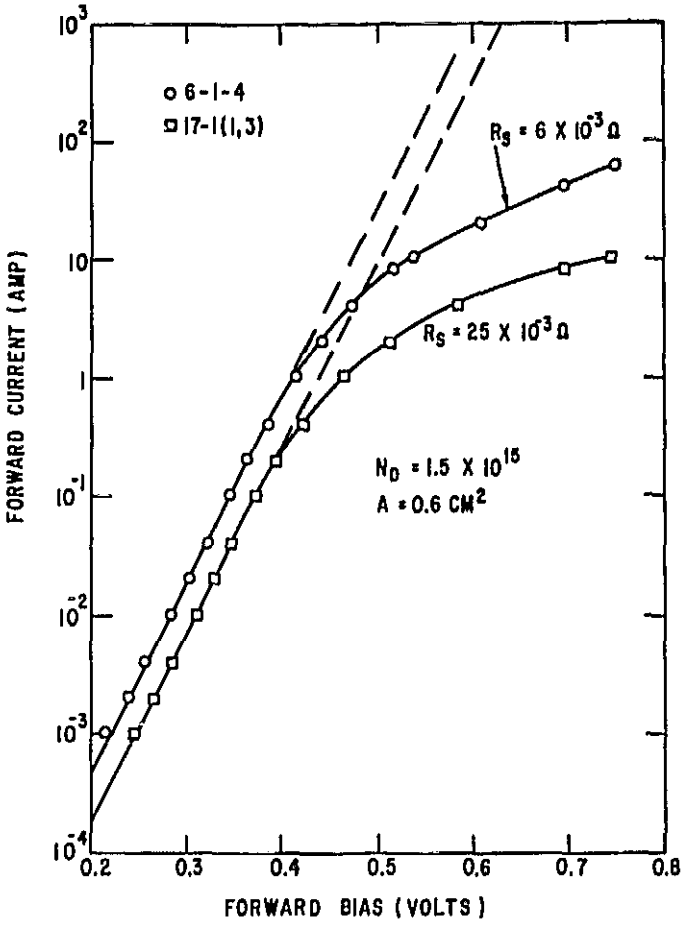


Fig. 45 Forward I-V characteristics of two diodes demonstrating the effects of extra series resistance.

expression

$$I = I_s \exp \frac{qv}{nkT}$$

of 1.08. Above 1 amp the current increases less rapidly than exponentially due to the series resistance of the diode. The measured value of series resistance, R_S, obtained from the data of Fig. 44 is 2.4×10^{-3} ohm. The value of the semiconductor bulk series resistance calculated from the measured resistivity and epitaxial thickness is 1.8×10^{-3} ohms. This Schottky rectifier is thus near ideal in its forward characteristics; having an "n" value close to unity, and exhibiting a series resistance very close to the bulk value. This diode has current handling capability greater than 100 amp since its epitaxial voltage drop is so small.

Diode 6-1-4, shown in Fig. 45, was made on 2.9 Ω-cm epitaxial material 12μ thick. The "n" value in this case is 1.07, and the measured ohmic series resistance is 6×10^{-3} ohms. This value, once again, corresponds very closely to the value of 5.8×10^{-3} ohms calculated from the resistivity and thickness of the epitaxy. A comparison of this diode with 2-15-3 shows how much more serious the parasitic epitaxial voltage drop is for this higher resistivity.

Also shown in Fig. 45 is the I-V characteristic of diode 17-1-(1, 3). This diode is quite similar in construction to 6-1-4. The epitaxy here is 3.2 ohm cm 11.3μ thick, giving a diode epitaxial resistance of 6×10^{-3} ohms. The forward characteristic of this diode, however, is far from ideal. Current rises exponentially with applied voltage at the reasonable rate of 63.8 mv per decade for an "n" of 1.06. The measured series resistance in this case, however, is 25 milliohms.

There is clearly extra resistance in this rectifier over and above that of the epitaxial silicon which introduces very large parasitic voltage drops at high currents. At 10 amp, for example, the series drop for this rectifier is 250 mv, more than four times the proper value.

This additional resistance shows up on many, but not all, of our assembled diodes. Independent measurements of the epitaxial thickness and resistivity were made on test elements from most of the wafers that yielded finished, assembled diodes. Table III lists these values and the epitaxial resistance, R_{epi}, derived from them together with the experimental values of, R_S, the diode series resistance. These are also plotted in Fig. 46. Several things are noteworthy. First, there is variation from wafer to wafer in the degree to which R_S approaches R_{epi}. Second, there is also considerable variability even within a single wafer. Wafer 7-1, for example, exhibits a resistance variation of nearly a factor of 2. Finally, while the data are quite sparse, there is a slight indication from Fig. 46 that the deviation of R_S from R_{epi} increases with epitaxial resistivity.

We did not anticipate this difficulty and were unable in the course of the contract period to do enough additional work to determine its origin and to eliminate it. We, thus, do not know the detailed nature and specific origin of this extra resistance. It must, however, arise from imperfect electrical contact somewhere between the top tungsten electrode and the Schottky barrier. Consider the diode contact metallization shown schematically in Fig. 47. All of its constituent metal layers, PtSi, Mo, Ni, Ag, can form high resistance oxide or sulfide films. These films, if formed at any point in the course of the contact buildup, will not be reduced at the moderate temperature of the subsequent assembly in hydrogen and will contribute additional resistance.

From the variability in R_S we suspect that the basic problem is one of patchiness. While there may be good low-resistance metal-to-metal contact over some of the diode area, there is poor contact over the rest. The entire contact metallization is less than 2μ thick with lateral sheet resistance of approximately 50 milliohms per square. Thus, for example, if the top solder wets only part of the metallized mesa top, the lateral IR drop in the 50 milliohms per square metallization essentially biases off those regions of the rectifier not directly under the wetted area. The effective diode area is thus directly reduced and the resistance increased. The situation is even worse if there is only partial contact between the constituent layers of the metallization. In this case the lateral sheet resistance is higher still.

TABLE III

Resistance of Mounted Diodes

Diode No.	Measured Resistance (milliohm)	ρ (ohm-cm)	t (microns)	R_{epi} (milliohm)
1-34-2	2	0.77	11.5	1.5
1-34-3	2			
2-15-3	2.4	1	11	1.8
6-1-1	10	2.9	12	5.8
6-1-2	6			
6-1-3	6			
6-1-4	6			
6-1-6	7			
6-2-1	10	2.9	12	5.8
6-2-2	10			
6-3-2	8	2.9	11	5.3
6-3-3	8			
6-3-4	8			
6-3-6	7			
6-5-4	10	2.9	12	5.8
7-1-3	15	3.0	13	6.5
7-1-5	15			
7-4-1	13	3.0	13	6.5
7-4-2	9			
7-4-4	7			
7-4-6	9			
7-4-8	7			
7-5-1	9	3.0	13	6.5
7-5-2	7			
17-1(1, 2)	16	3.2	11.3	6
17-1(1, 3)	25			6
17-4(2, 2)	15	3.4	11.5	6.5

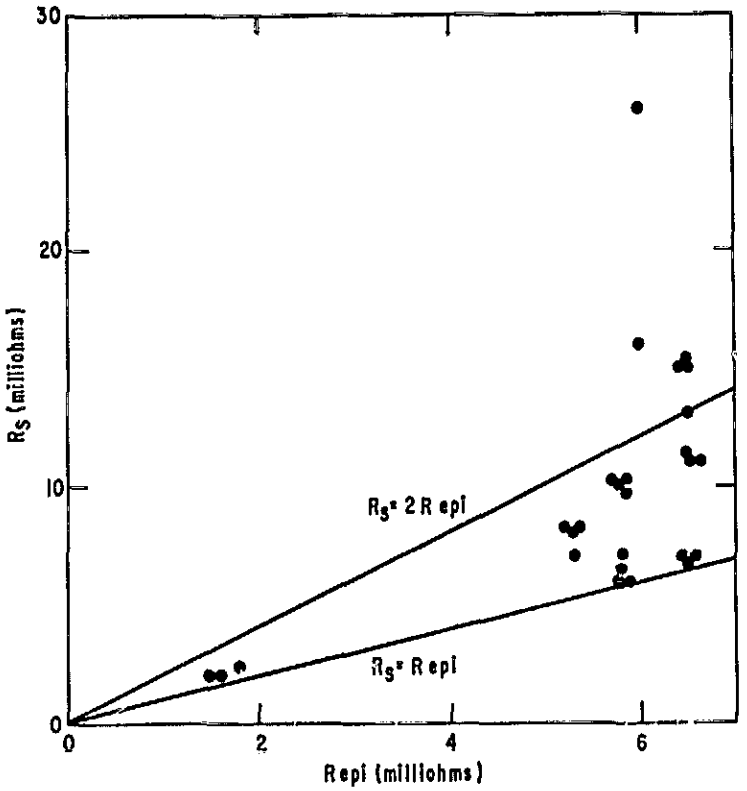


Fig. 46 Comparison of the measured series resistance of assembled diodes with the theoretical ohmic epitaxial value.

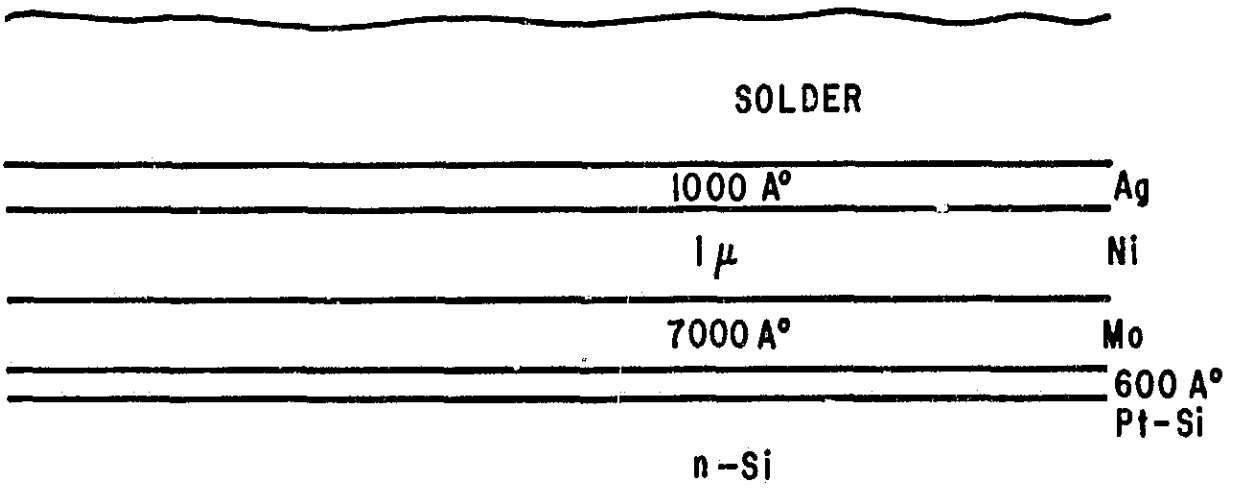


Fig. 47 Schematic view of contact metallization.

This problem is more serious for Schottky diodes than for junction devices. In the case of junction devices, minority carriers are injected across the barrier. These diffuse laterally a substantial distance in the course of their lifetime before recombination; thus nonuniformities in electrical contact are smoothed out even at low injection levels. At high levels of injection, of course, the entire active region is flooded with a highly conducting electron-hole plasma. Schottky devices have little hole injection so this mechanism of making up for nonuniform electrical contact doesn't operate. In addition, the usual p-n junction power device has deep diffusions and thus several microns of heavily doped silicon to help laterally spread current.

This problem of Schottky contact metallization is thus a unique and critical one. It may in principle be attacked by making the diode area larger. Our diodes are, however, 0.6 cm^2 in area already. Any additional increase that would scale down the resistance by a substantial factor would result in very low yields. These metallization problems must therefore be approached head-on and the factors leading to the additional resistance and its variability identified and eliminated. We have demonstrated feasibility in that several of our diodes do indeed have resistances that are within several percent of R_s. There is thus nothing inherent in either the Schottky diode or our metallization which prevents good contact. More work devoted specifically to this area is required.

6.3 Test Results

Each of the diodes delivered was characterized in both forward and reverse directions. The results are presented in tabulated form in Table IV. Data presented are: (1) detailed current-voltage characteristics out to 40 amp forward; (2) measured value of diode series resistance; (3) calculated value of epitaxial resistance for those wafers measured; (4) the reverse bias at which the current is 50 ma at room temperature; (5) the reverse bias at which the current is 50 ma at temperatures greater than 100°C measured prior to final assembly; (6) the barrier drop at 25 amp forward obtained by subtracting the ohmic drop from the measured diode bias at 25 amp; (7) V_{max}, the theoretically maximum breakdown voltage, and (8) F, the ratio of V (50 ma) to V_{max}.

As was discussed above, we were unable to reach V_{max}, the theoretically maximum breakdown voltage for these mounted diodes. Except for the more heavily doped material where values near 0.8 were achieved, the fraction of V_{max} that was attained was near 0.5.

The forward characteristics of many of the assembled diodes exhibited series resistance greater than R_s, the epitaxial resistance, as was discussed above. This problem is especially serious for high-voltage diodes where R_s is substantial since the extra resistance seems to scale with R_s. An actual

TABLE IV

Electrical Characteristics of Delivered Diodes

V (mv)														
(1)														
I (amp)														
1×10^{-3}	1-34-2	1-34-3	1-35-2	6-1-1	6-1-2	6-1-3	6-1-4	6-1-6	6-2-1	6-2-2	6-3-2	6-3-3	6-3-4	
2	225	236	214	221	170	214	215		229	231	215	221	234	
4	247	256	238	247	210	244	238	164	248	248	249	247	253	
1×10^{-2}	266	274	257	268	242	279	257	218	266	266	279	271	273	
2	291	302	282	296	276	299	283	261	290	291	314	303	298	
4	312	321	304	317	300	319	303	286	310	311	338	325	318	
1×10^{-1}	331	339	325	337	323	345	323	310	329	330	358	346	338	
2	355	364	347	363	348	364	347	338	354	355	386	373	363	
4	374	383	367	384	368	384	367	357	373	374	407	394	382	
1×10^{0}	399	402	387	405	389	414	387	378	394	395	429	415	404	
2	421	429	416	437	419	440	416	408	424	426	459	445	434	
4	442	450	440	467	450	472	442	435	450	453	486	471	459	
8	465	474	468	510	475	519	474	467	484	488	522	506	494	
10	495	494	503	572	522	538	519	514	535	540	565	553	542	
20	507	512	522	600	539	610	534	534	554	561	584	571	560	
40	549	552	584	710	638	695	607	694	635	643	[illegible]9	642	634	
(2)	615	614	674	865	694	697	694		730	740	[illegible]44	724	718	
R_s (mΩ) (3)	2	2	6	10	6	6	7	10	10	8	8	8	8	
R_{epi} (mΩ) (4)	1.5	1.5	5.8	5.8	5.8	5.8	5.8	5.8	5.8	5.3	5 [illegible]	5.3		
V (50 ma) 25°C M (5)	76	66	86	112A	110A	115	105	104A	95A	110A	117A	108A	102	
V (50) >100°C (6)					112A			108A		110A	110A	125A	120A	
V_{ext} (25 amp)	518	510	497	497	507	503	499	490	502	503	538	527	515	
V_m	85	85		245							235			
F	.89	.78		.46	45	.47	.43	.44			50	.53	.51	

TABLE IV (Continued)

V (mv)													
I (amp)	6-3-6	6-5-4	7-1-3	7-1-5	7-3-1	7-3-2	7-4-1	7-4-2	7-4-4	7-4-6	7-4-8	7-5-1	7-5-2
$1x10^{-3}$	222	226	212	203	149	217	206					206	227
2	244	244	230	224	202	248	238			221		230	249
4	266	262	249	242	228	272	263	231	254	256		254	269
$1x10^{-2}$	295	286	274	267	276	305	293	276	292	294		281	296
2	316	306	293	286	304	327	323	306	318	319	251	304	318
4	336	325	314	306	329	349	337	333	340	342	318	324	337
$1x10^{-2}$	362	350	339	334	360	376	364	362	368	369	351	350	362
2	381	370	359	354	384	399	385	384	389	390	376	370	388
4	403	391	381	377	414	425	408	407	412	414	400	392	403
1	433	424	407	414	446	466	443	440	443	445	433	424	434
2	458	463	448	448	514	512	476	469	469	474	460	454	460
4	491	491	493	496	592	576	525	508	506	514	494	492	495
8	538	548	542	570	708	675	596	561	554	566	542	550	546
10	556	570	593	602	750	717	628	584	574	589	562	575	566
20	628	660	718	725	907	858	742	670	650	680	638	676	648
40	708	762	895	870	1.080	1.022	884	759	739	785	724	814	743
R_s (mΩ)	7	10	15	15	30	22	13	9	7	9	7	9	7
R_{epi} (mΩ)	5.3	5.8	6.5	6.5			6.5	6.5	6.5	6.5	6.5	6.5	6.5
V (50 ma) 25°CM	120A	100	100A	140A	112	130A	115A	110A	122	115A		108	120
V (50) >100°C	120A	104A	105A	105A	110	125A	108A	108A	108A	110A	110A	110A	120
V_{ext} (25A) mv	513	498	486	485	527	544	526	526	531	531	520	507	520
V_m							260				260		
F	.51						.44	.42	.47	.44	42	.42	.46

value of R, 30 percent greater than R_S at 1.5 milliohms, adds only 13 mv extra voltage drop at 25 amp. Even a factor of 2 is not too serious a matter for a low resistance diode such as 1-34-2. In this case the extra resistance would increase the diode drop at 20 amp forward by only 20 mv from the actual value of 549 to 569 mv. With higher resistivity material, it is quite another matter. A comparison of diode 6-1-4 with R_S of 6 milliohm with its sister diode 6-1-1 having 10 milliohms shows a full 100 mv extra parasitic drop at 20 amp.

A histogram showing the distribution of barrier voltages at 25 amp is shown in Fig. 48. As expected, these large diodes show more spread in forward characteristics than do the $10^{-3}cm^2$ and $10^{-2}cm^2$ devices used for material characterization. The observed spread is only about 40 mv, however. We expect that disciplined processing will reduce this number.

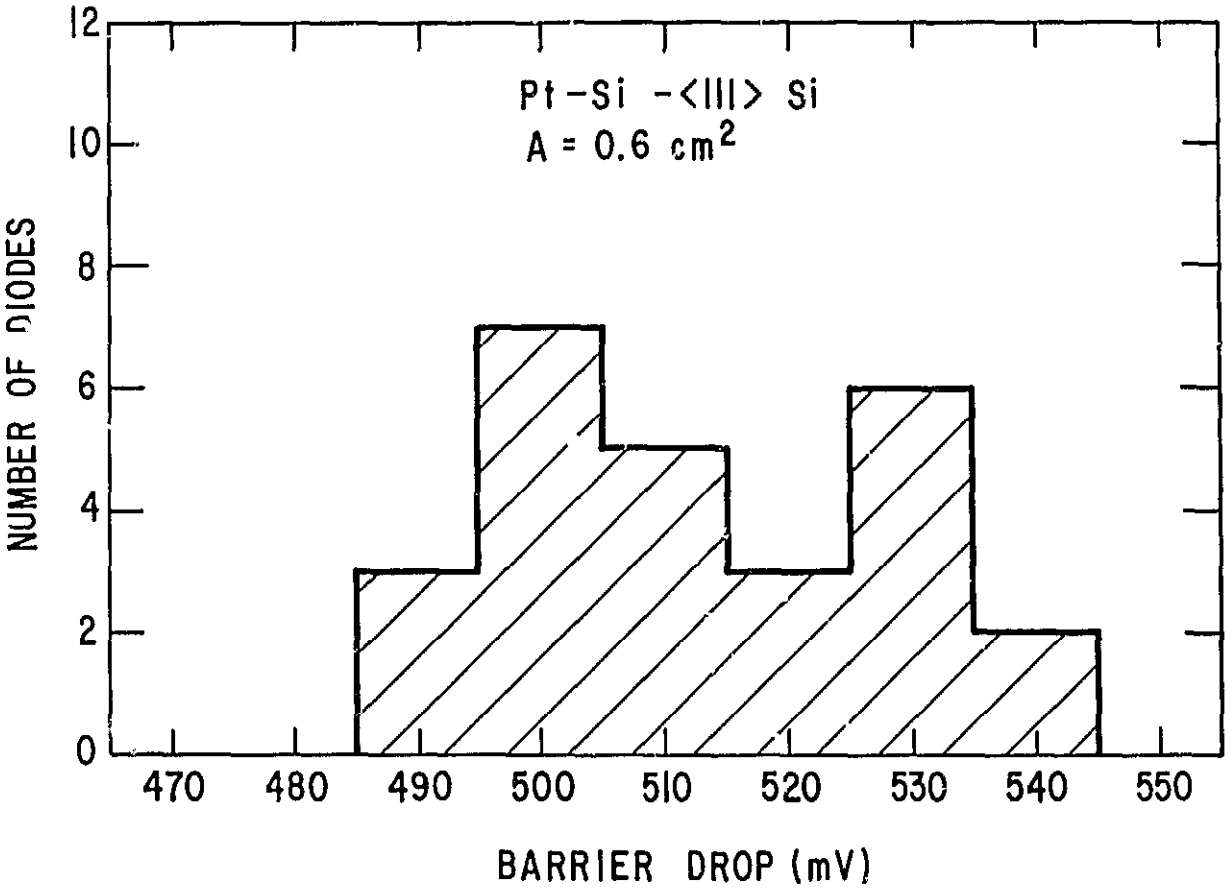


Fig. 48 Distribution of measured barrier drops for assembled diodes.

Section 7

REVERSE RECOVERY TIME

It is extremely difficult to measure short recovery times at large current values. We therefore did not measure the reverse recovery times of the final 25 amp rectifiers. We did, however, measure recovery times for several smaller (10^{-2} cm^2) mesa Schottky rectifiers that were processed in exactly the same manner as were the large diodes. These measurements were made at current density equal to or greater than the 42 amp/cm^2 corresponding to the rated 25 amp of the large diodes. A typical result is shown in Fig. 49. The circuit used for the measurement is also shown. The diode header used was not properly matched to 50Ω, so severe reflections are seen. Nevertheless, there is a small difference between the zero reverse bias and the 10 volt reverse bias current waveforms.

The -10 volt curve lies below the zero bias curve after the forward current pulse ends indicating a small amount of charge being swept out by the -10 volt reverse bias. There is thus some small amount of minority carrier insertion. This reverse recovery current is, however, gone within 20 to 30 nsec.

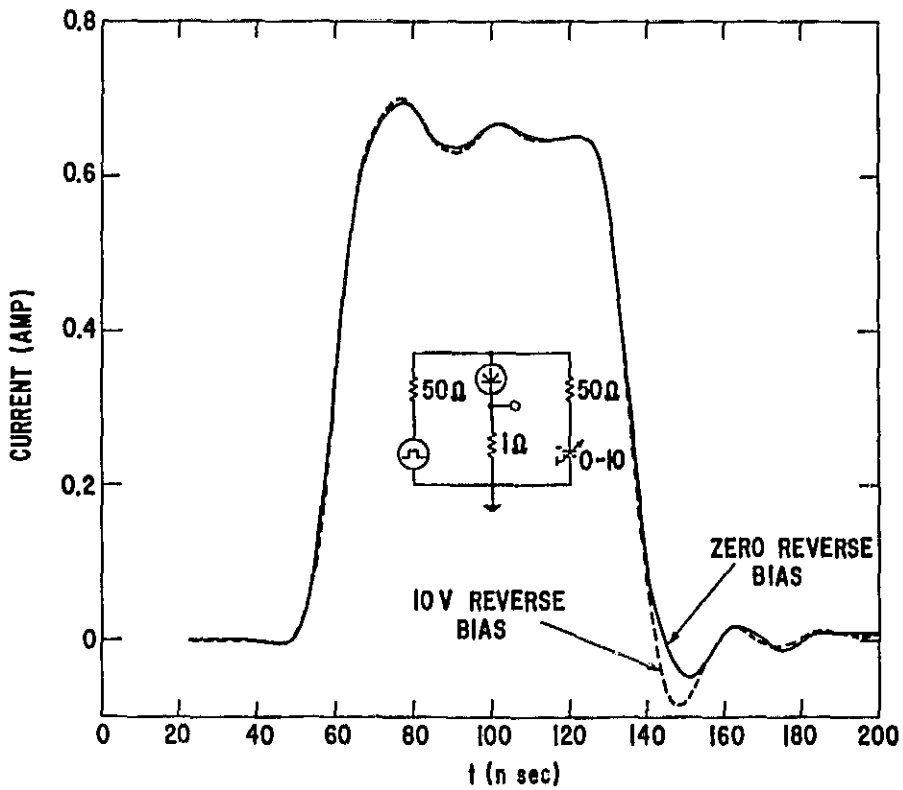


Fig. 49 Reverse recovery time after 60 A/cm^2 forward pulse.

Section 8

SUMMARY AND CONCLUSIONS

Our progress in Schottky diode development to date may be summarized as follows:

8.1.1 Barrier Fabrication

We have developed manufacturable, reproducible methods for fabricating Schottky diodes and for the metals W, Al, low temperature Pt-Si and conventional Pt-Si.

8.1.2 Barrier Height Measurements

Barrier heights for the above metals have been determined for the major crystallographic directions of n-silicon.

8.1.3 Barrier Lowering

Barrier lowering under reverse bias for W, Al, and low temperature Pt-Si has been measured allowing us to accurately predict reverse junction leakage for any specific diode design.

8.1.4 Processing

We have developed a processing sequence which results in the fabrication, at high yields, of large area (0.8 cm^2), high-quality, mesa geometry Schottky diodes exhibiting only thermionic leakage current. This process has worked sucessfully on several different lots of epitaxial material obtained from several sources.

8.1.5 Practical Breakdown Values

Test data for large area mesa diodes show that under practical processing conditions avalanche breakdown occurs at reverse voltages that are between 50 and 80 percent of the theoretical values. These values represent practical design limits.

8.1.6 Effects of Assembly on Reverse Characteristics

We have demonstrated the feasibility of an assembly procedure which does not degrade the reverse characteristics of near ideal Schottky pellets of large area.

8.1.7 Diode Resistance

We have demonstrated that it is feasible to assemble power Schottky diodes exhibiting ohmic resistance within a few percent of the theoretical epitaxial value.

8.2 Conclusions

The dominant thrust of our development program to date has been directed towards improving reverse Schottky characteristics. We have, we believe, succeeded in this effort to the point where additional major process development is not necessary. The mesa Schottky structure is the most desirable configuration for high voltage ratings (> 50 volts) and we have high confidence that our process can fabricate it with high yields. Our experience that practical values of avalanche breakdown are no more than 80 percent of theoretical at 200 volts lead us to conclude that it is not practically feasible to make a 200 volt Schottky diode which meets the contract design goals. Attractive practical designs are, nevertheless, still feasible at lower voltage ratings where the epitaxial resistance is not quite as large.

There is one area where additional wafer process refinement is most desirable. We believe that it would be advantageous to more nearly optimize the step of mesa passivation. This will likely result in diodes that break down at a consistently higher fraction of the theoretical voltage limit.

We have learned from our assembly work that there are unforeseen problems connected with the diode metallization and with diode soldering procedures. Contact buildup is an important requirement for Schottky diodes in general and an especially critical one for large area diodes. With the main focus of our phase 1 and 2 efforts on wafer fabrication, we have not been able to address sufficient effort toward studying and optimizing metallization and soldering. We have shown the feasibility of low resistance assembly for the mesa structure. We do not, however, have enough experience as yet to be able to define an assembly procedure that will consistently yield diodes exhibiting theoretical values of ohmic resistance. Additional effort is most desirable here.

Section 9

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