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A POWER CONDITIONING SYSTEM FOR RADIOISOTOPE THERMOELECTRIC GENERATOR ENERGY SOURCES

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FOREWORD

The purpose of this document is to delineate the particular requirements of conditioning the power available from a Radioisotope Thermoelectric Generator energy source, and to describe the design and operation of a complete power conditioning system to perform this function. The system described herein was designed as part of some preliminary work on the Outer Planetary Explorer. Performance is discussed under both static and dynamic modes of operation.

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INTRODUCTION

The use of scientific unmanned spacecraft to probe the furthest reaches of our planetary system, and beyond, is a distinct probability as a part of the future operations of NASA. These spacecraft will invariably require operating lifetimes of several years, perhaps in excess of ten years. Therefore the use of Radioisotope Thermoelectric Generators as the primary source of energy will in all likelihood become more common than is presently the case. In view of this, greater emphasis must be placed on the practical engineering aspects of the power system, particularly in the areas of reliability and simplicity.

RADIOISOTOPE THERMOELECTRIC GENERATOR (RTG)

The operation of an RTG is based on the principle of the thermoelectric effect. Briefly, this principle states that if two dissimilar metals (conductors) are joined together at both ends, and the two junctions are exposed to different temperatures, a current will flow. The thermocouple has a characteristic open loop voltage and short circuit current, the ratio of which gives the thermocouple output impedance. The voltage and current (or power) capable of being delivered to a load in the thermocouple loop is a function of, among other things, the difference in temperature between the two junctions .

An RTG is made up of several thermocouples, each representing an electrically independent low voltage energy converter. The energy input into these converters is derived from the heat given off by the decay of an isotope fuel. The voltage-current output characteristic of the complete RTG is dependent upon the particular series-parallel arrangement of the individual thermocouple elements going into its makeup, much as a solar array output is the net total of its individual solar cells. For design purposes, it was assumed the power source consists of four RTG's in parallel, each with an output characteristic as shown in Figure 1. Note here that there are two output characteristics shown; one for the beginning of life (BOL), and one for the end of life (EOL).

Generally, the output impedance of the RTG increases with time due to degradation of the thermocouples. The decay of the isotope fuel also contributes to a reduced RTG output with time. A factor of great importance in the operation of RTG's is the thermocouple hot junction temperature. With a constant heat input energy source, this temperature can typically vary 310°F from open circuit to

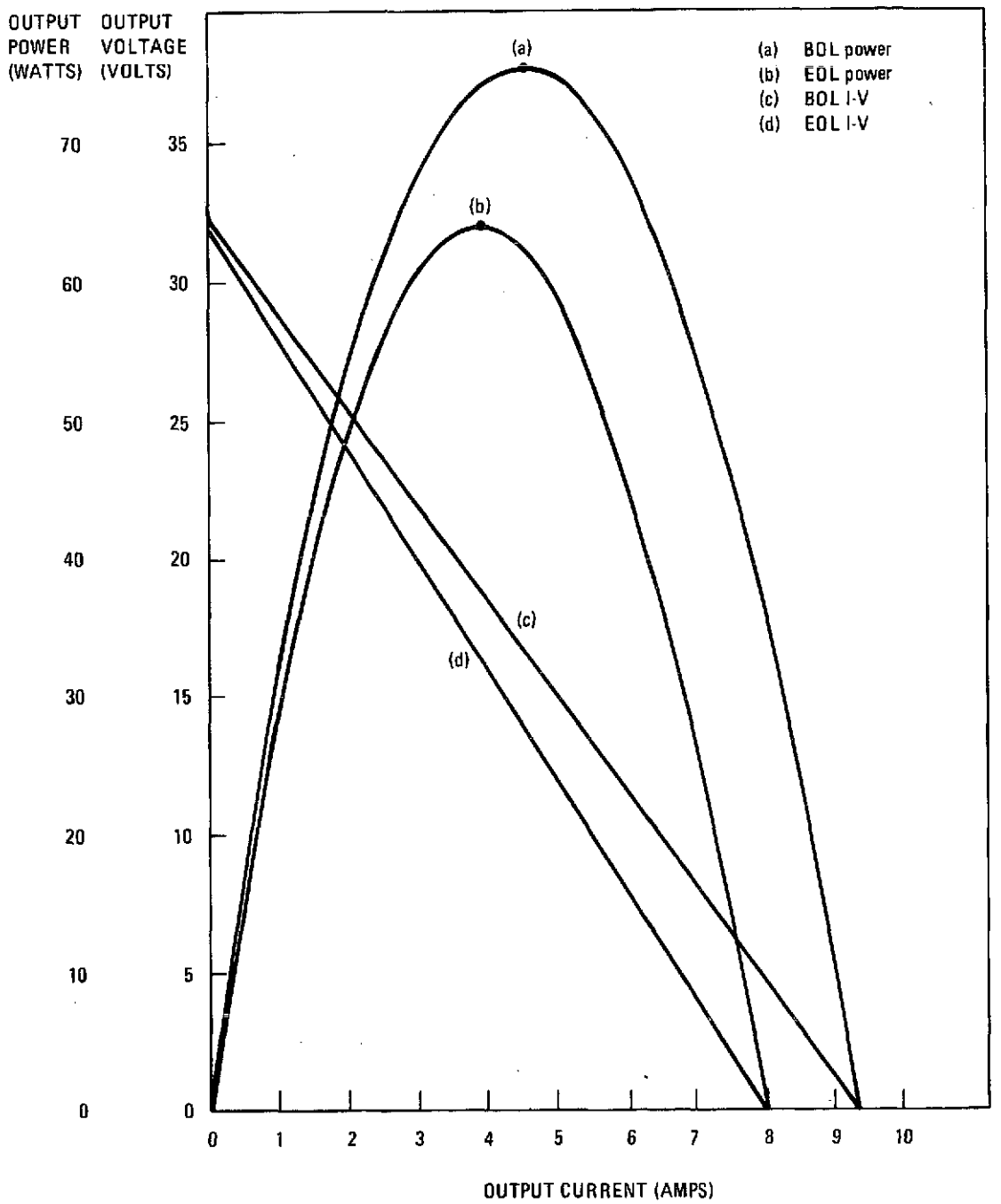


Figure 1. Typical output characteristics of the RTG assumed in this design. Since four are used in parallel, multiply current and power scales by four to obtain total output.

short circuit, with the open circuit case the hottest and the short circuit case the coolest. This cooling of the hot junction with current flow is known as the Peltier Effect. Thermocouple degradation can increase by a factor of three or four if the thermocouple hot junction temperature increases by 50°F, which will rapidly decrease the RTG's output power capability. The beginning and end of life I-V and power curves of Figure 1 are based on the RTG operating at 16 volts output for a period of approximately six years.

RTG OUTPUT CONTROL

It is obvious from the foregoing that any power conditioning system used with an RTG source must cause the RTG to continuously operate on a fixed point of its output characteristic. The best operating point (voltagewise) will most likely always be such as to wind up at the end of life peak power point (point b of Figure 1). This means that considerably higher power can be used or must be dumped at the beginning of life, (point a of Figure 1). A series type regulator would not be readily applicable for use with an RTG since it would have to be the input voltage or current which was regulated in order to remain at a desired fixed power point. In this case the load voltage would be determined by the load itself, which would have to sink whatever current was necessary to maintain the power transfer balance. This would be true whether a dissipative or non-dissipative regulator were used.

A shunt regulating system, on the other hand, would allow for a fixed voltage, variable current load bus, and still maintain the RTG at a fixed output power. A shunt system is shown in block form in Figure 2, along with the main bus voltage as a function of load current.

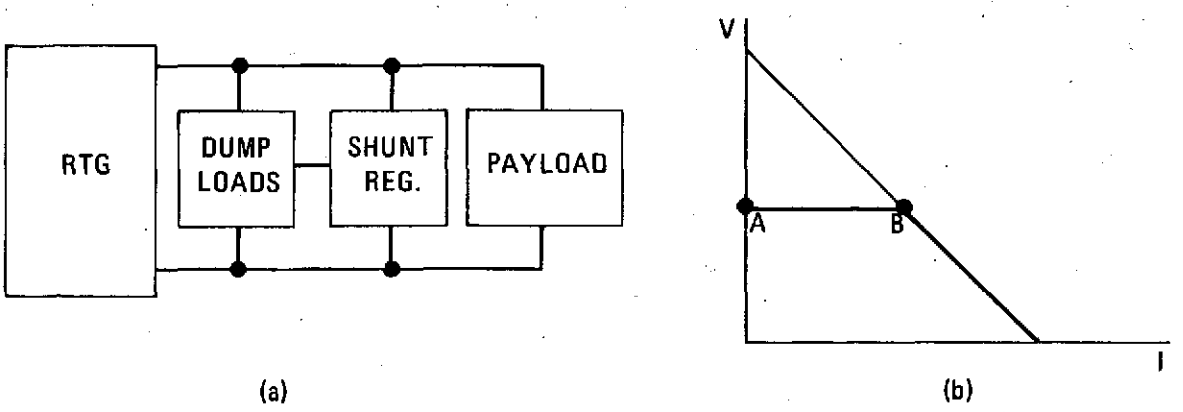


Figure 2. (a) Shunt Regulator System,
(b) Bus Voltage as a Function of Load Current

An RTG system has no inherent overload capability, either long or short (transient) term. If the load current demand should exceed that corresponding to point B of Figure 2b, the load voltage will drop rapidly. An energy storage system can be provided by either battery pack or capacitor bank to temporarily maintain the bus voltage during overload conditions. The decision to have such a storage system, with its added complexity, cost and weight will depend on the loads capability to withstand reduced bus voltages, the overload duration and frequency of occurrence, the nature of the overloading device.

POWER CONDITIONING SYSTEM REQUIREMENTS

The specifications for the power conditioning system presented here are as follows:

Bus Voltage:	16 Volts ± 2%
Maximum steady state load:	250 Watts
Shunt Regulator Capacity:	300 Watts
Overload capability (with bus remaining within ± 2%):	32 Amps for 5 msec
Energy source:	4 independent RTG's in parallel

The four RTG's each have a power capability as shown in Figure 1. Their combined power capability will therefore be 300 watts at the beginning of life, and at the end of life 256 watts.

The block diagram of the overall system is shown in Figure 3. The power conditioning system consists of two identical halves, only one of which will normally be in use handling the total load. Should a load fault appear, causing an undervoltage situation, the bus would automatically split into two independent halves, with the command and data subsystem or-gated to either bus. Hopefully, only one bus would still be in a faulted condition and the particular load causing the problem could then be isolated. It is important to note that an RTG can run in the shorted state indefinitely without any difficulties, if necessary.

For purposes of laboratory testing only one complete half system was breadboarded.

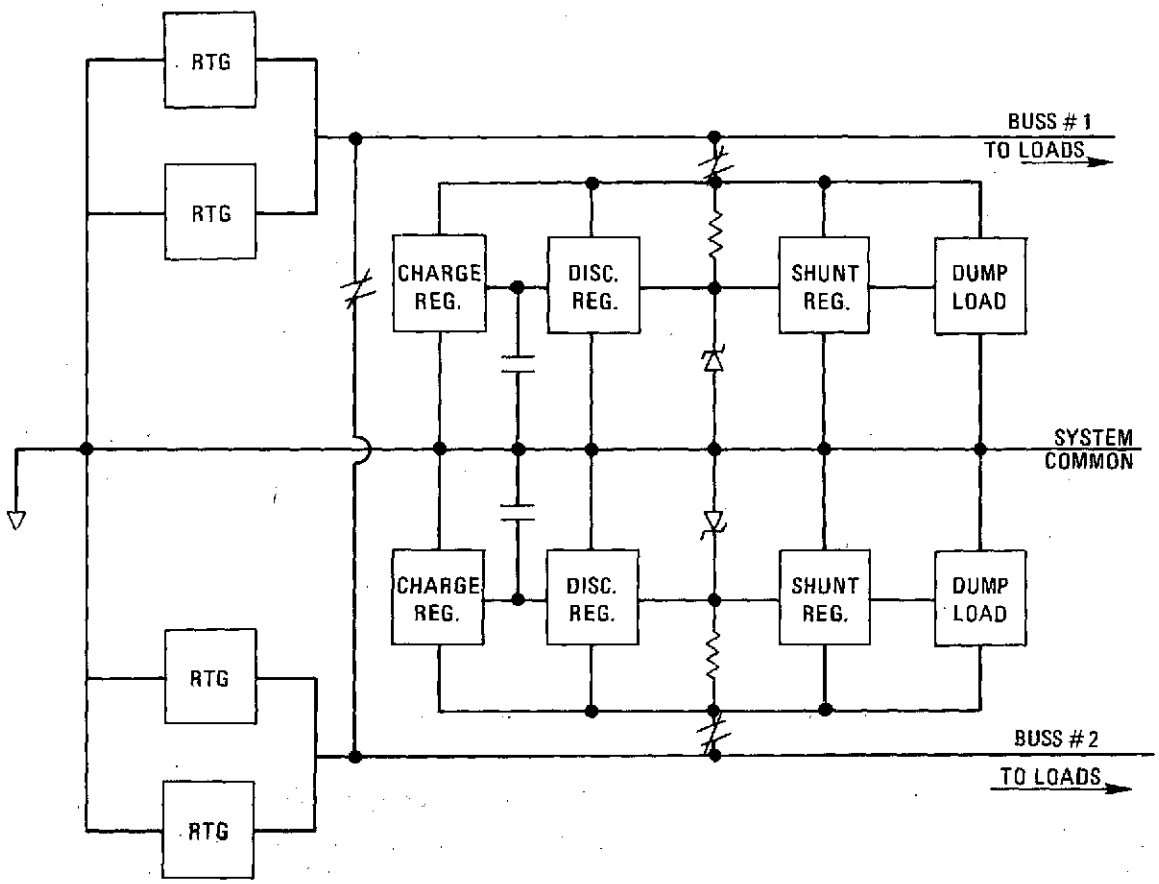


Figure 3. Complete Power Conditioning System Block Diagram

ELECTRICAL DESIGN

Shunt Regulator

The shunt regulator is a basic design used successfully on several solar array spacecraft (Ref. 1). The design lends itself to flexibility in that the number of shunt paths and dump capacity per path are readily changeable to meet different power requirements. The design, shown simplified in Figure 4, uses twelve shunt paths of which only ten are needed to dissipate the entire 300 watts available at the beginning of life. This allows for increases in power handling

Ref. 1–Solar Array Regulators of Explorer Satellites XII, XIV, XV, XVIII, XXI, XXVI, XXVIII, and Arial 1, John Paulkovich, NASA TN D-3983 July 1967.

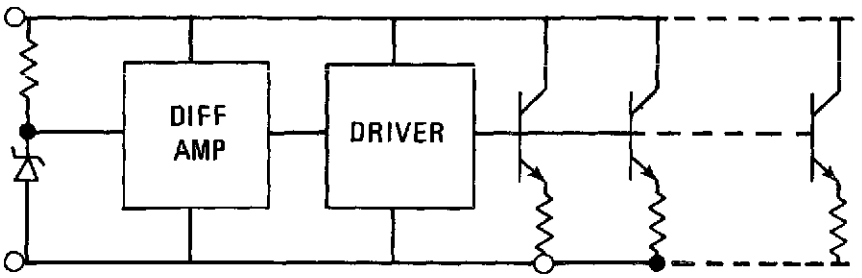


Figure 4. Shunt Regulator Simplified Diagram

capability if necessary, and also gives the capability of removing up to two shunt paths after launch should a malfunction occur. During later periods of spacecraft life, more shunt paths could be removed if necessary or shifted around if desired to heat different areas of the spacecraft. Figure 5 shows the power dissipated in both the dump transistors and resistors at beginning of life as a function of payload current for both ten paths and 12 paths.

Energy Storage Charge Control and Discharge Regulator

The mechanism for supplying power to a load in excess of that available from the RTG's could be based on a battery pack storage system or a capacitor bank storage system. While batteries have a much higher energy density than do capacitors, they tend to be unreliable over long periods due to their more complex nature. For this reason, and since excess loads would be of a transient, low duty cycle nature, a capacitor bank energy storage system was deemed desirable. A capacitor bank could be placed directly across the main bus and thereby provide a degree of transient load capability. This approach is not too feasible since to provide the transient load specified previously (32 amps for 5 milliseconds) would require an extremely large amount of capacitance. The scheme settled upon is depicted in Figure 6.

The capacitor bank, shown as C in Figure 6, is charged to, and maintained at, 32 volts by the charge regulator. The discharge regulator senses the main bus voltage, and, in the event the voltage drops below a predetermined value, supplies power to the bus as necessary to maintain voltage as long as sufficient energy is available in the capacitor bank.

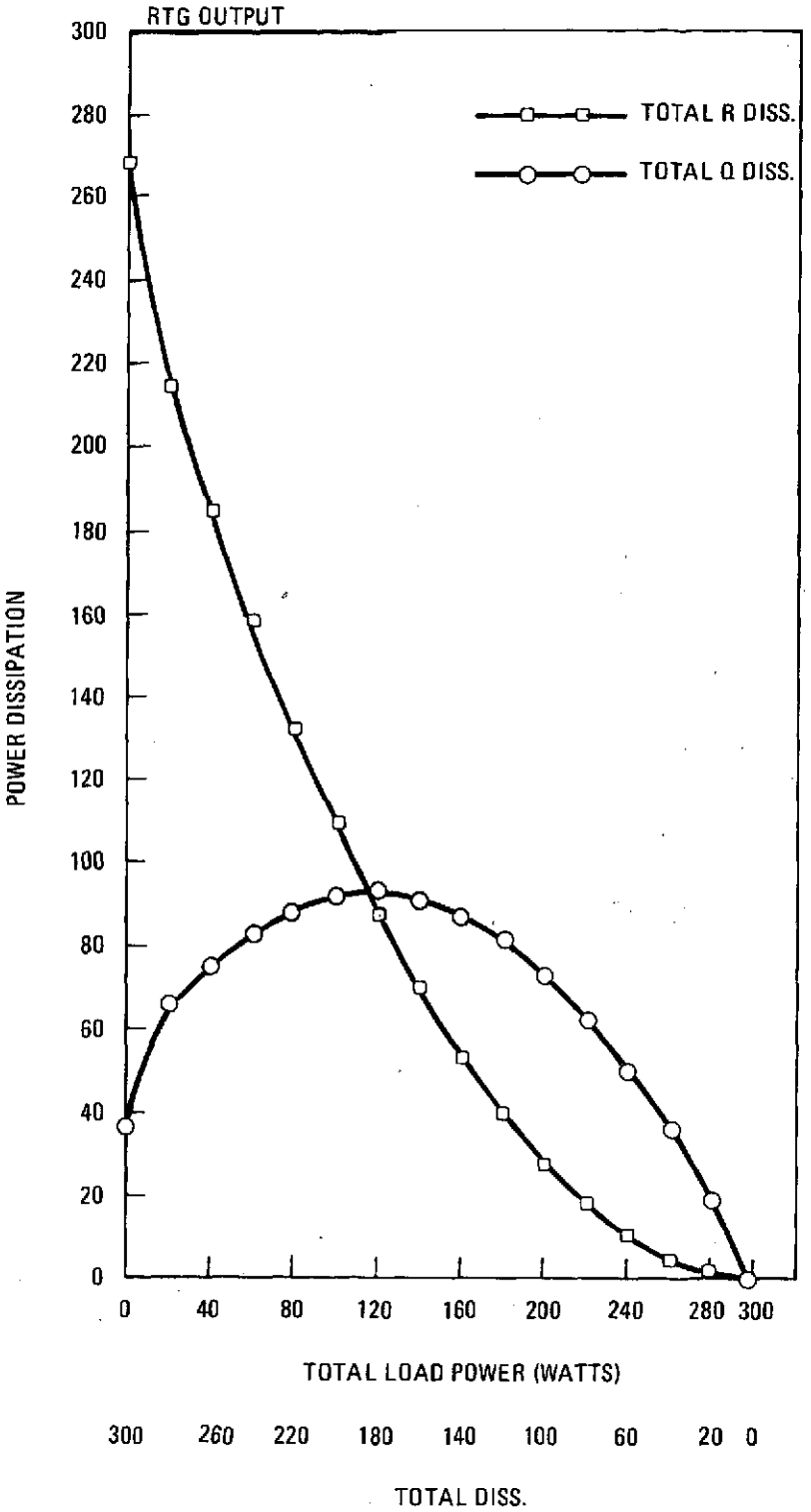


Figure 5(a). Power Dissipation, 10 Paths

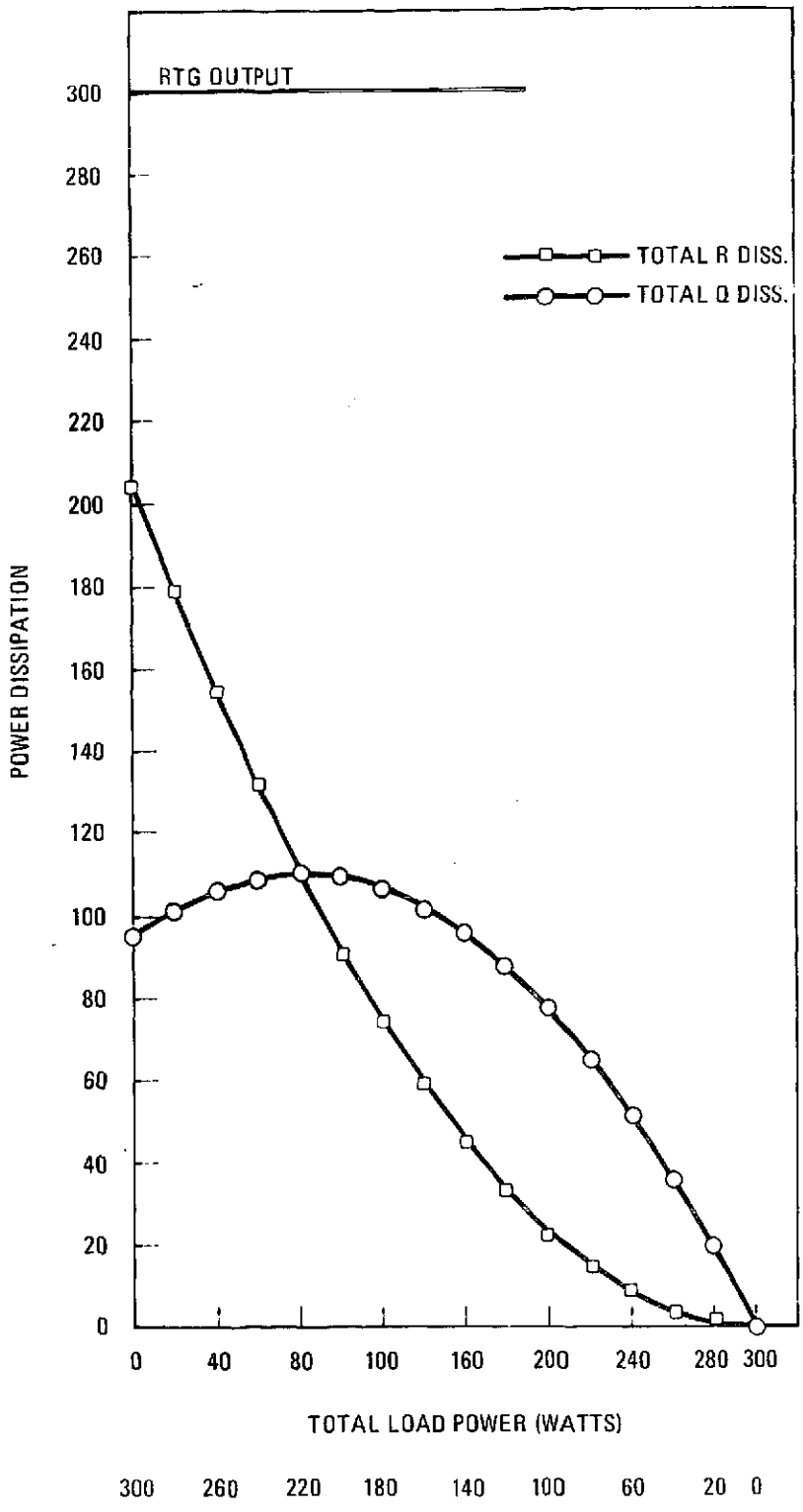


Figure 5(b). Power Dissipation, 12 Paths

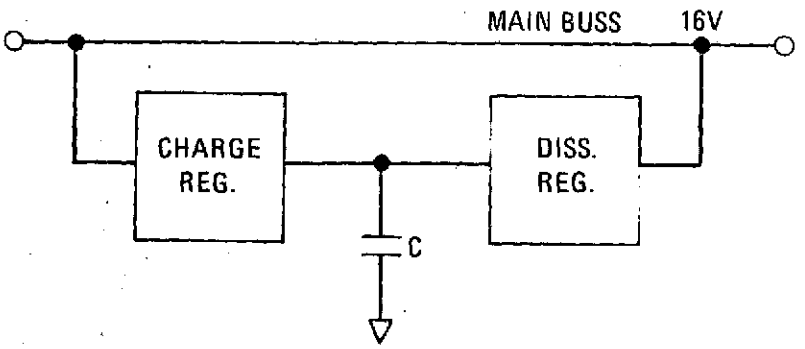


Figure 6. Energy Storage and Discharge System

Design Considerations

The capacitor bank is made up of twenty 660 uf, 75 volt General Electric type 29F capacitors. These are tantalum foil electrolytics capable of handling essentially unlimited peak surge currents.

The total capacitance is 13,200 uf, which when fully charged will contain 6.76 joules of energy. If it is assumed the capacitor bank, acting as an energy source, can maintain the bus voltage while discharging from 32 volts to 18 volts, the total energy given up is:

$$\Delta E = 1/2C\Delta(V^2) = 1/2(13.2 \times 10^{-3})(1024 - 324)$$
$$= 4.62 \text{ joules} \quad (1)$$

This represents, say, 462 watts for 10 milliseconds, or 924 watts for 5 milliseconds, etc. The actual rate of energy loss from the capacitor bank is, of course, not constant; although the energy delivered to the load may be at a constant rate. The difference is the energy dissipated in the discharge regulator, which is a standard series dissipative type. A non-dissipative regulator would not be practical here due to its inherently slower response time and more complex design. It would allow a somewhat reduced capacitor bank size for an equal load capability, but this will generally not be a practical consideration.

The discharge regulator is shown in simplified form in Figure 7.

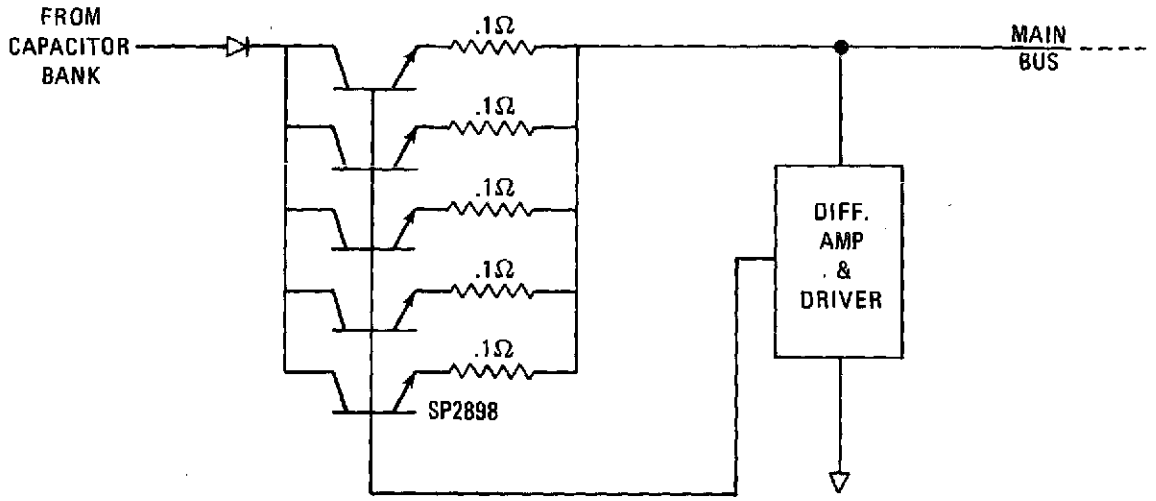


Figure 7. Discharge Regulator

Five SP2898's in parallel are used to handle the transient current. The .1 ohm emitter resistors are used to ensure equal sharing of the current, particularly at the higher current levels. The input diode protects the pass transistors when the bus voltage is present but the capacitor bank is not yet charged. SP2898's were used because of their availability. A preferred part here might be the 2N5575, where perhaps only two in parallel (or just one) would suffice.

The discharge regulator and shunt regulator differential amplifiers share the same reference voltage, as shown in Figure 8(a).

The differential amplifier resistive dividers are adjusted to produce control as shown in Figure 8(b). Neither the discharge regulator or shunt regulator receive any drive signal if the bus is between 15.9 volts and 16.1 volts. By sharing the same references, the two controlling circuits should not interfere with one another despite slight changes in the reference voltage with temperature and time. In actual operation, the bus voltage will be in the region above 16.1 volts all the time except when transients occur. An improved control circuit using operational amplifiers is shown in Appendix A.

CIRCUIT PERFORMANCE

Figure 9 shows a graph of overload capability versus time. Figure 10 shows a trace photograph of the main bus voltage, discharge regulator output current,

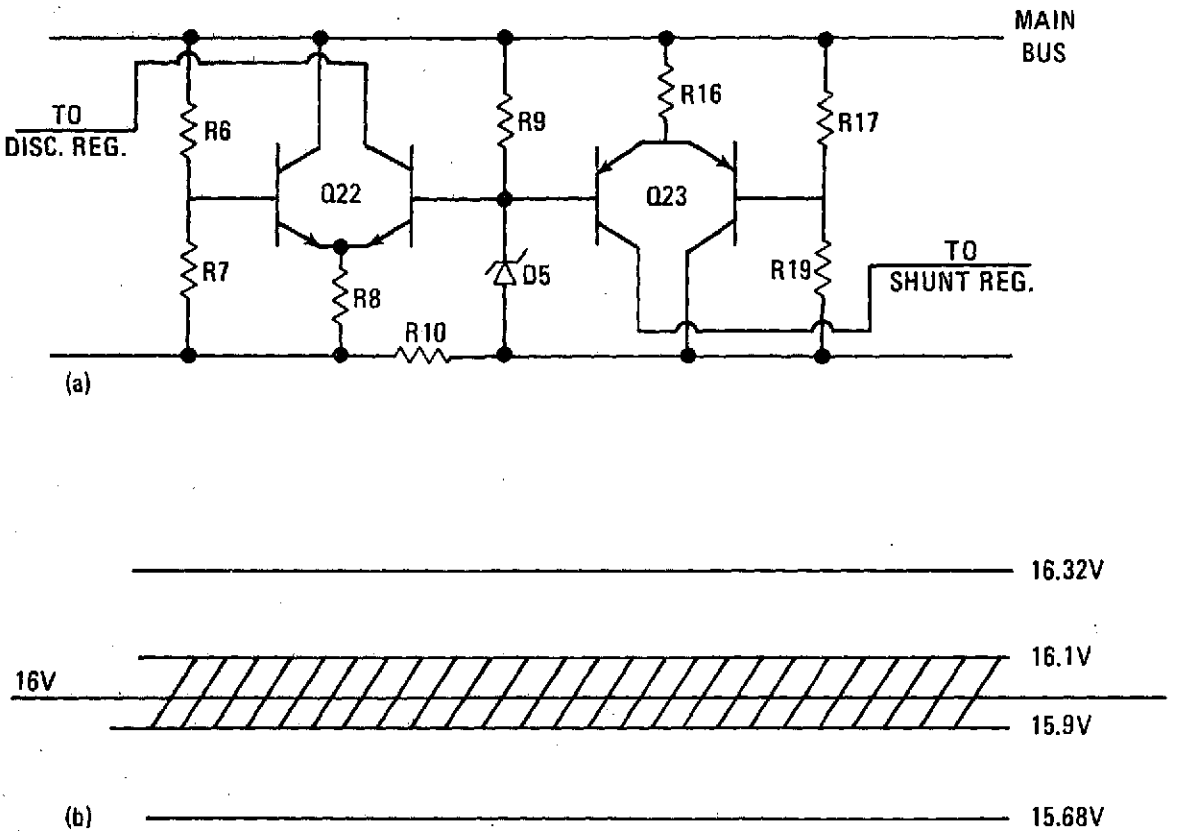


Figure 8. (a) Discharge regulator and shunt regulator differential amplifiers. (b) Separate regions within the bus voltage regulation band.

and capacitor bank voltage. Figure 10(a) is with a step load approximately 32 amperes in excess of the RTG 16 volt output capability. As can be seen, the bus voltage is maintained for about 5.5 milliseconds. Figure 10(b) is with approximately 8 amperes excess load applied, with a duration capability of approximately 22 milliseconds. The fuzziness on the waveforms is caused by switch noise.

The discharge regulator efficiency may be calculated fairly accurately by using the energy given up by the capacitor bank and that delivered to the load. Equation 1 shows the energy given up by the capacitor bank to be 4.62 joules. The charge given up is

$$\Delta Q = C\Delta V = (13.2 \times 10^{-3})(14) = .185 \text{ coulombs} \qquad (2)$$

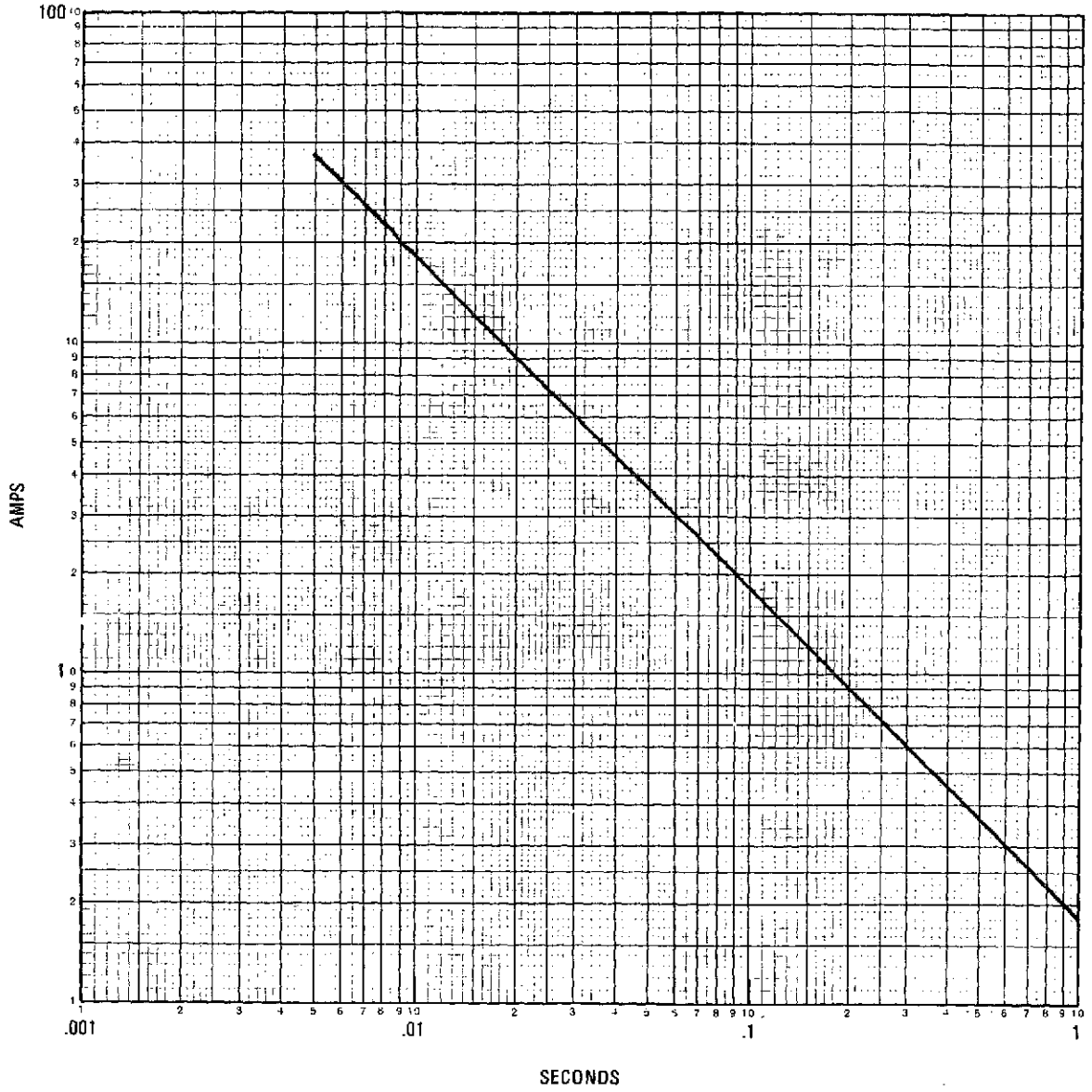


Figure 9. Discharge Regulator Output Current Amplitude Capability vs. Time.

This could represent 37 amperes for 5 milliseconds. Therefore, the energy to the load is:

$$E = 37 \times 16 \times 5 \times 10^{-3} = 2.94 \text{ joules}$$

Therefore, % efficiency $= 2.94/4.62 \times 100 = 63.6\%$

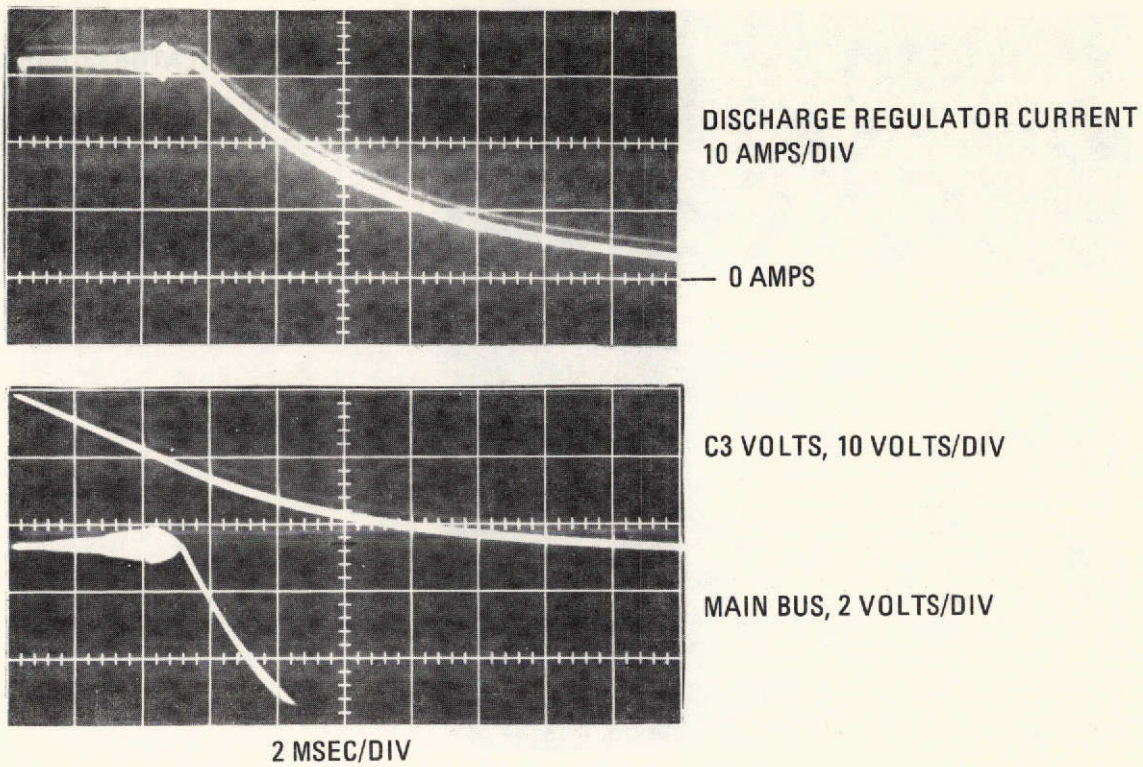


Figure 10(a). Discharge Regulator Waveforms, 32 Amp Overload

The capacitor bank charge control circuit consists of a flyback energy storage transformer type regulator. This regulator uses as its reference voltage the 16 volt main bus, and keeps the capacitor bank topped off at 32 volts. The charger is shown in the overall schematic of Figure 11, and consists of L1; C1, C2 and C4; D1, D2, D6, and D19; Q1 and Q2; R1 thru R5; T1 and T2. As may be seen, the circuit is very simple. The frequency of operation during charge is fixed at about 8.5 khz by the relaxation oscillator R1, C2 and D1. Charging current for C2 flows through R1 and Q1 (normally full on when charging). When the voltage gets high enough on C2, D1 breaks down, sending a turn on current pulse through winding 5-6 of T1. Regeneration from winding 3-4 of T1 rapidly turns Q2 full on. Q2 remains on for a fixed period until T1 saturates. This is set so that when T1 saturates, the collector current of Q2 has reached 1.5 amperes. T1 has a square permalloy 80 tape wound core. After T1 saturates, Q2 rapidly regenerates off and the T1 flux returns to its residual density level. No reset current is required. Since the Q2 on time and frequency are fixed, the input current to the charger is fixed at about 130 milliamperes when charging the capacitor bank from 18 volts to 30 volts. After the capacitor bank reaches about thirty volts, the feedback voltage from divider R3, R4 starts to

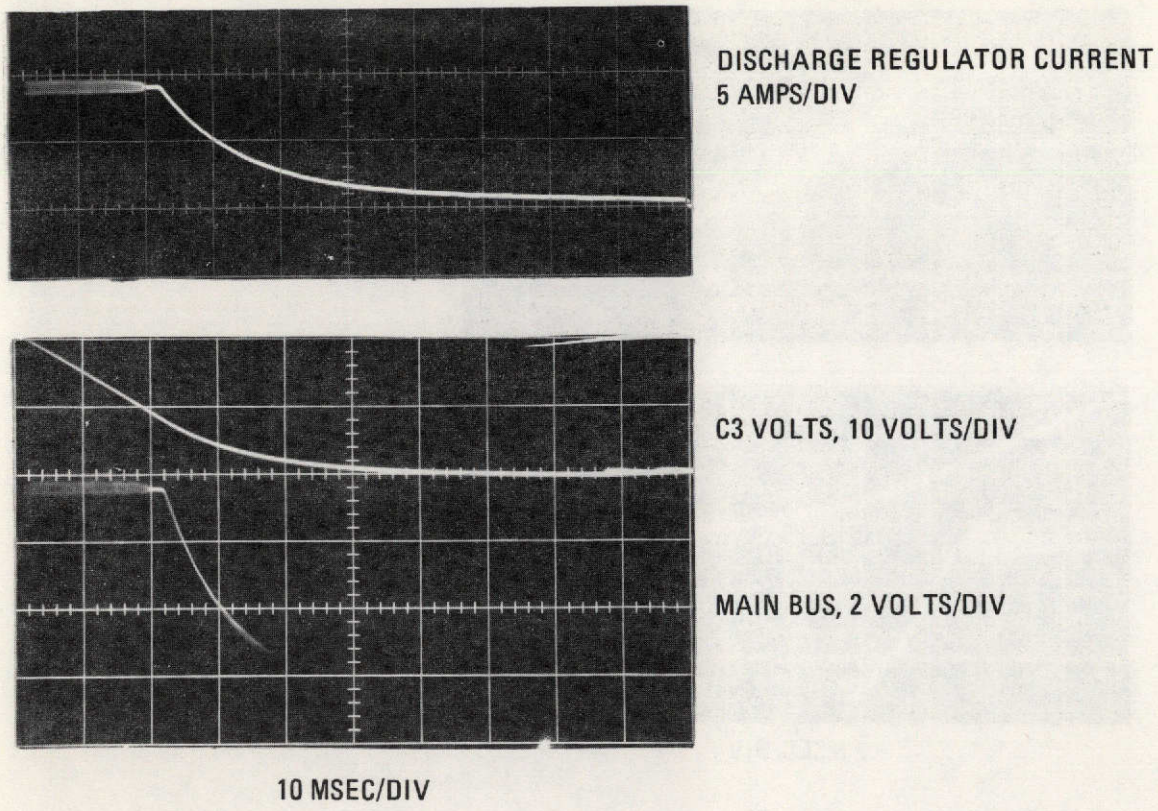


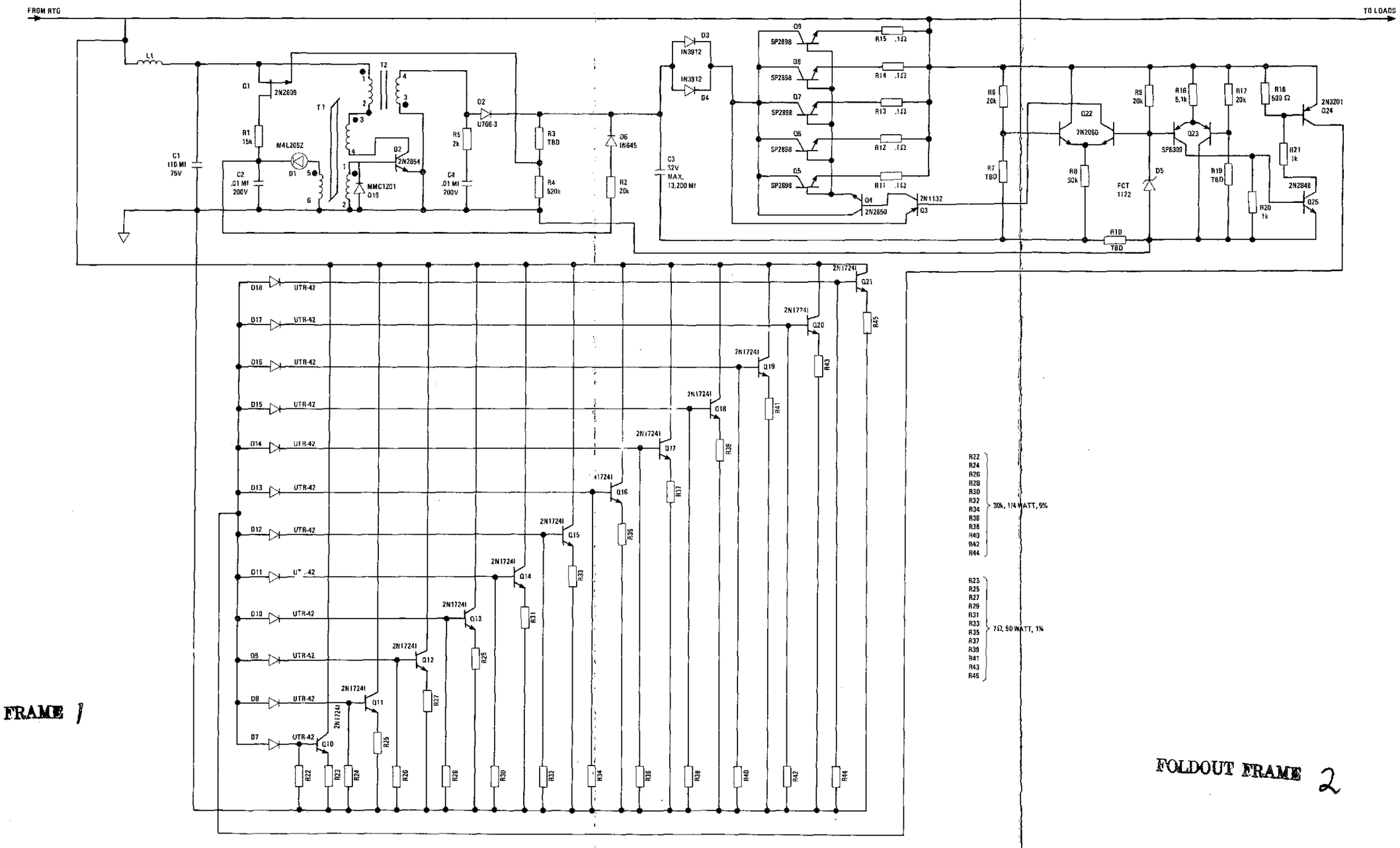
Figure 10(b). Discharge Regulator Waveforms, 8 Amp Overload

turn off Q1, reducing the frequency of operation, and eventually turning off the oscillator. Voltage divider R3, R4 is set so that the capacitor bank voltage will be twice the main bus voltage. In the steady state the capacitor bank remains at 32 volts with the charger coming on periodically to replace charge lost by internal capacitor leakage and the feedback divider current. The circuit has an inherent hysteresis, coming on at intervals of from one to two minutes for about 1 second. The voltage on the capacitor bank changes 200 to 300 millivolts during this cycling. A modified version of the charging circuit is shown in Appendix A which would allow positive control over the hysteresis time.

Figure 12 shows some charging circuit waveforms.

The charging circuit is quite flexible in that the output charge level and rate of charge are easily modified. Diode D6 and resistor R2 are used to reduce the oscillator frequency during periods when the capacitor bank voltage is very low (10 volts). This will limit the input current to the charger during initial starting and in the event of shorts or very heavy transients at the charger output.

FOLDOUT FRAME 1

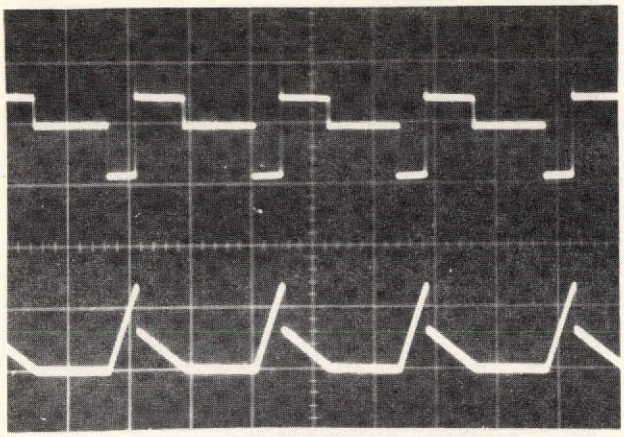


R22, R24, R26, R28, R30, R32, R34, R36, R38, R40, R42, R44 } 30k, 1/4 WATT, 5%

R23, R25, R27, R29, R31, R33, R35, R37, R39, R41, R43, R45 } 7Ω, 50 WATT, 1%

FOLDOUT FRAME 2

Figure 11

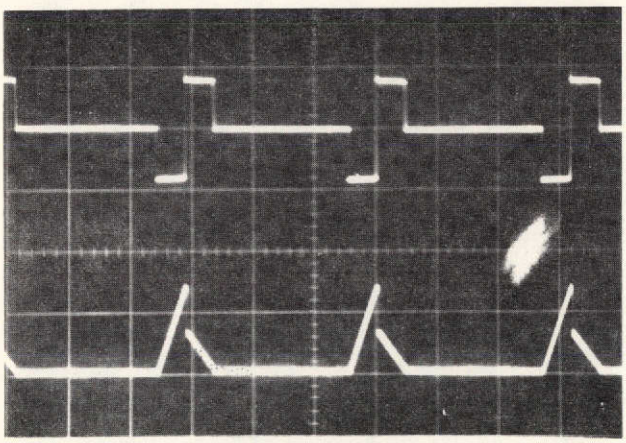


(a) Charger Waveforms with C3 Voltage 18 Volts

Q2 COLLECTOR VOLTS
20 VOLTS/DIV

T2 PRIMARY AND SECONDARY CURRENT
1 AMP/DIV

50 USEC/DIV

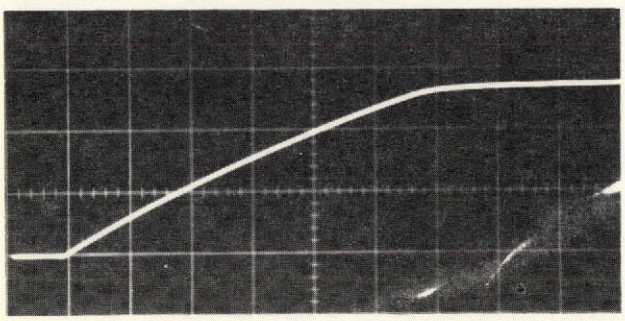


(b) Charger Waveforms with C3 Voltage 31 Volts

Q2 COLLECTOR VOLTS
20 VOLTS/DIV

T2 PRIMARY AND SECONDARY CURRENT 1 AMP/DIV

50 USEC/DIV



(c) C3 Voltage During Charge, 18 to 32 Volts

C3 VOLTAGE
5 VOLTS/DIV

.5 SEC/DIV

Figure 12. Charger Circuit Waveforms

Figure 12(a) and (b) show Q2 collector volts and the current into T2 terminal 1 and out of terminal 4. In Figure 12(a) the capacitor bank voltage is 18 volts. In Figure 12(b) the voltage is 31 volts, the frequency is down and the charger is headed for turn off. Figure 12(c) shows the capacitor bank voltage going from 18 volts to 32 volts, which takes about 3 seconds.

The use of a flyback power converter offers advantages over a conventional DC to DC converter which could be used to charge capacitor bank C3 through a resistor. The flyback technique gives essentially a constant current source capacitor charge, with its inherent efficiency (probably around 90%) and smooth operation. A conventional DC to DC converter would present a constant voltage source capacitor charge technique, with its inherent inefficiency ($<50\%$) and large initial current surges.

APPENDIX A

POSSIBLE DESIGN MODIFICATIONS AND ALTERATIONS

Figure A-1 shows a possible modification to the charger circuit to control the oscillator off time while keeping the capacitor bank topped off. Transistor Qa will come on when Q2 first starts to oscillate. This will drop the feedback voltage, turning Q1 on hard. When the proper voltage level is reached on C3, Q2 will turn off, turning off Qa. The feedback voltage is thereby raised, causing Q2 to remain off for a predetermined time, depending on the value of R_d.

Figure A-2(a) shows a modified shunt regulator and discharge regulator control circuit. This has an advantage over the one previously shown in that both control signals use the same reference voltage and feedback divider. In addition, setting the control levels and separation band is much easier. Figure A-2(b) shows the control voltage outputs using the component values shown in Figure A-2(a). The slope of the output voltages is controlled independently by the gain of their respective operational amplifiers, while the width of the separation band is controlled by the value of R_b relative to R_a and R_c.

Another technique which could be used to regulate the main bus during heavy transient loads is the use of an AC sensing discharge regulator. This regulator

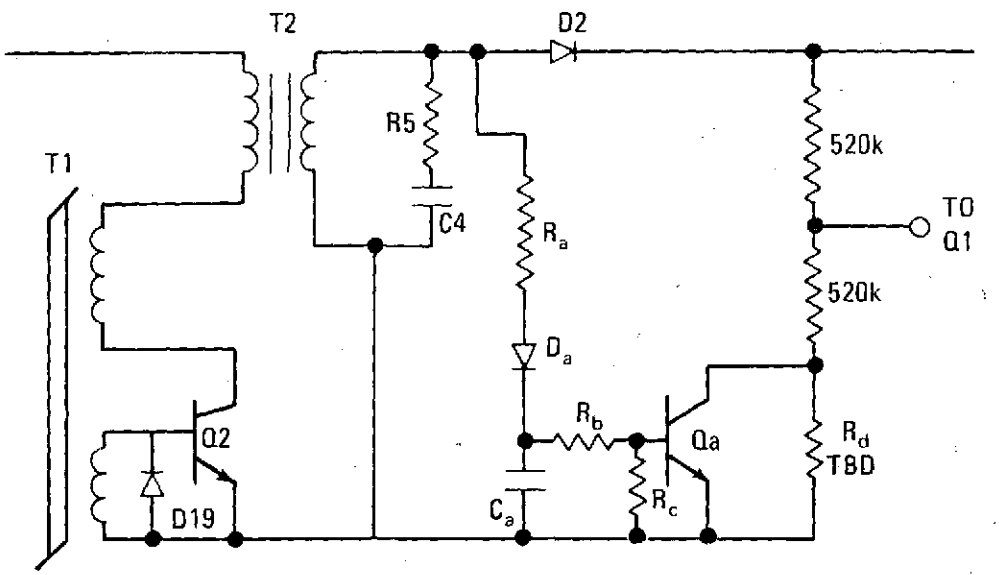


Figure A-1. Modification to the Charger Circuit.

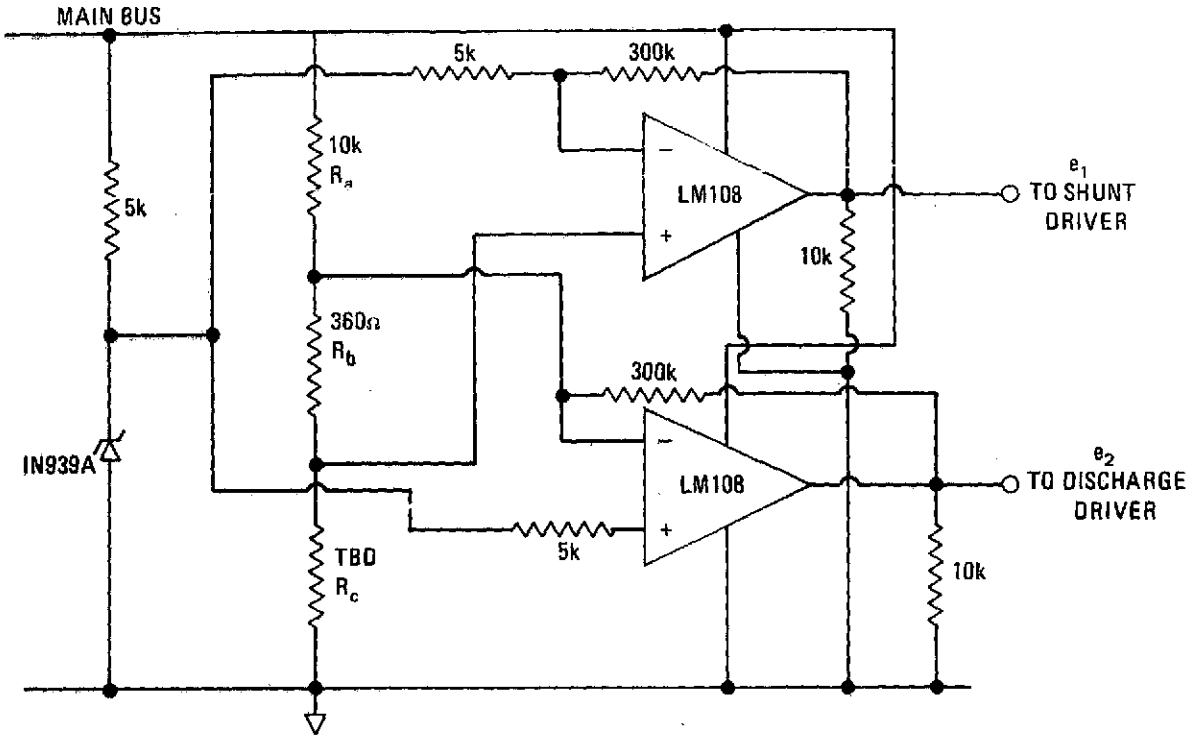


Figure A-2(a). Improved Shunt, Discharge Regulator Control

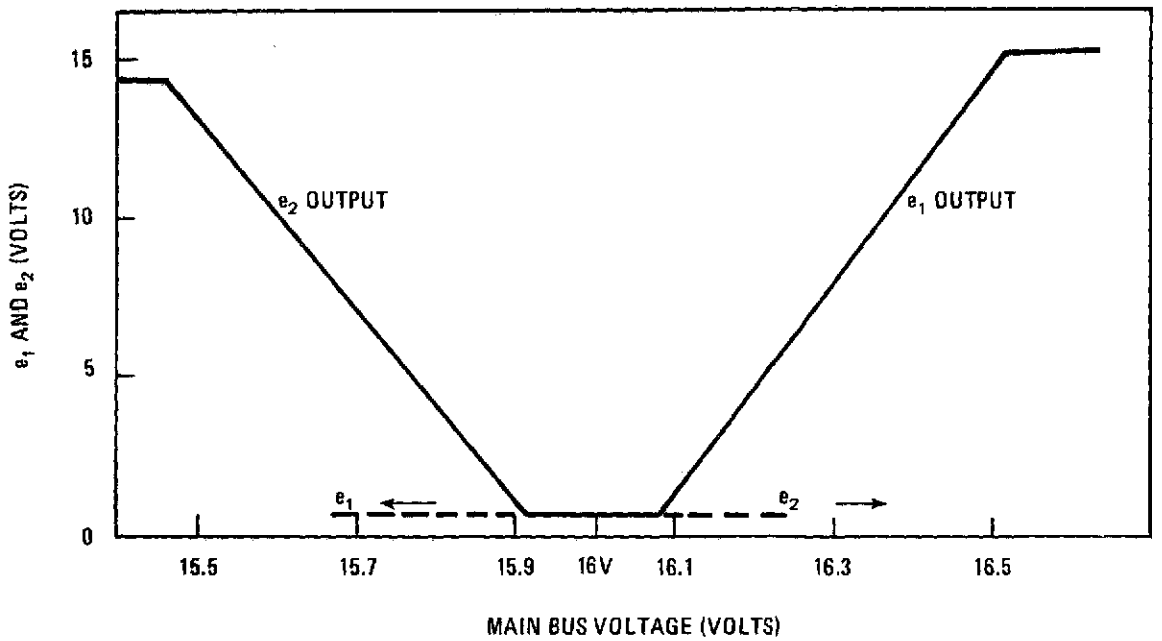


Figure A-2(b). Shunt and Discharge Control Circuit Output Voltages

would respond to changes in the main bus, rather than to its fixed DC level. This would have the advantage of not having to be concerned with separation between the shunt regulating band and discharge regulating band. This would allow the shunt regulator to operate within the entire - 16 volt ±2% region. Figure A-3 shows a possible AC connection for the discharge regulator control operational amplifier.

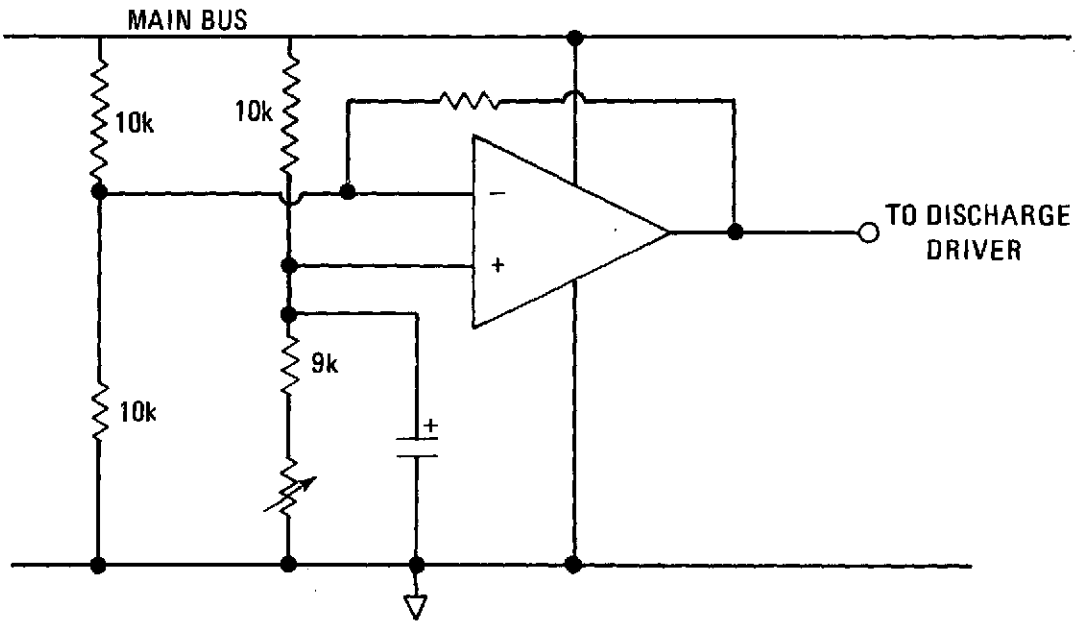


Figure A-3. AC Connected Discharge Regulator Control

The divider is adjusted to the point such that no output is present. DC, or very low frequency changes in the bus would not turn on the operational amplifier. However, heavy transient loads would cause the bus to drop rapidly, causing instant reaction from the operational amplifier to turn on the discharge regulator. The operational amplifier output could also be AC coupled to the discharge regulator driver stages so that its DC output would not be critical, as long as it had room to change sufficiently during transients.

APPENDIX B

MAGNETIC DESIGN INFORMATION

L1	Magnetics 55202		75 turns	AWG 26
T1	Magnetics 52402-1D	N_{1-2}	75 turns	AWG 25
		N_{3-4}	2 turns	AWG 20
		N_{5-6}	12 turns	AWG 25
T2	Magnetics 55928	N_{1-2}	37 turns	AWG 21
		N_{3-4}	74 turns	AWG 24