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ATS-54102

NASA CR-132456

EXPERIMENTAL INVESTIGATION OF A SHIELDED COMPLEMENTARY METAL-OXIDE SEMICONDUCTOR (MOS) STRUCTURE

By

H.C. Lin and J.L. Halsor

Prepared under Contract No. NAS 1-11369

By

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Systems Development Division
Advanced Technology Laboratories
P.O. Box 1521
Baltimore, Maryland

For

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
Langley Research Center
Hampton, Virginia

FINAL REPORT

for

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March 1972 - June 1974

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Introduction

Semiconductor surfaces are sensitive to electric fields. In order to avoid surface inversion due to stray electric fields such as the electric fields created by either high voltages appearing in the interconnections or stray electric charges resting on the oxide, it is necessary that the oxides (other than the oxide under the gate area) be thick (usually $\gtrsim$ 10,000 angstroms). When the surface is inverted, a conductive path exists between the isolated sources and drains and causes excessive power dissipation and malfunction of the circuits. If multilayer interconnections are used, an even thicker oxide must be deposited. Such a thick oxide consumes long processing time, sometimes requires two or more depositions, may cause metal interconnect discontinuity at the oxide steps and may suffer from cracking. The quality of the oxide must also be good so that no trapped charges or mobile ions are present to cause instability. This surface inversion problem is particularly severe in complementary MOS transistors due to the low surface concentration of the p-"well" where n-channel devices are fabricated. Many conventional CMOS integrated circuit designers have resorted to the use of a heavily doped guard ring (e.g. a p^+ ring around the p-well or an n^+ ring in the n-substrate) to break up the spurious conductive path. However, such a measure has the drawback that the chip area is increased. This study describes a shielded CMOS integrated structure which is used to prevent field inversion in the region not occupied by the gates and which permits the use of a

thinner field oxide, reduces the chip area, and has provision for simplified multilayer interconnections. The structure is used in the design of a static shift register.

Structure

The underlying principle of the shielded structure[1] is to use an electrostatic shield over all the region that is not occupied by the gate. The structure is shown in Figure I.1.Silicon gate technology[2] is used. The shield is fabricated simultaneously with the same polycrystalline silicon as the gate. The polycrystalline silicon covering the area between the source and drain serves as the gate, while the polycrystalline silicon in the remaining area is not removed but serves as an electrostatic shield.

In operation, the shield can be connected to a convenient d-c potential, such as the background potential. Thus any potential on the aluminum interconnection cannot affect the underlying silicon.

In the shielded complementary MOS structure the n-doped polycrystalline silicon layer is used for the gates, the shields, and if necessary, crossunder interconnections. The shields can be polarized to different potentials with respect to the background. A convenient scheme is for the background and the shield to be equi-potential. Therefore, the shield for the p-channel region is separated from the shield for the n-channel region. This separation should not adversely affect the isolation because the inversion layer which may be created in the unshielded region becomes discontinuous under the shield.

In order to have the same n-doped gate for both complementary channels, only the n-channel gate is self-aligned. The source and the drain for the p-channels are diffused prior to the gate oxidation as in conventional aluminum gate MOS transistors.

Design of Shielded CMOS Integrated Shift Register

The chip area using the shielded structure can be reduced by eliminating the guard rings as shown in Figure I.2. Figure I.2(b) is the shielded version, while Figure I.2(a) is the conventional guard-ring structure. It can be seen that the spacing between two neighboring complementary diffused regions is substantially reduced (from 40μ to 32μ assuming each minimum demarkation of 8μ).

The other factor contributing to area reduction is due to the multilayer interconnection provided by the shield layer and the metal layer.

The exact reduction in area depends on the topology of the lay-out. The saving in area is sometimes offset by the need to isolate the polysilicon gate and the shield. It is also necessary to allow some area to make ohmic contact from the metal interconnection to the poly-silicon gate.

Figure I.3 shows how two complementary transistors may be connected as an inverter. Figure I.3(a) is the conventional design with both p+ and n+ guard rings. The p+ channel MOS transistor located on the left-hand side is somewhat wider than the n-channel transistor on the right-hand side to equalize the transconductance. For the shielded version shown in Figure I.3(b), the polysilicon gate and the polysilicon shielded must be isolated by etching away the polysilicon which is the shaded region. However the spacing between two isolated polysilicon regions is made smaller than two isolated diffused regions due to the absense of lateral diffusion. Portions of the polysilicon gate areas for both tran-sistors are enlarged for contact windows. The enlargement increases the source-to-drain distance for that portion of the n-channel transistor. To compensate for the difference in transconductance, the n-channel width should be increased.

Major area reduction for circuits requiring crossing of interconnection can be realized by the extra layer of interconnection provided by the polysilicon. In a static shift register stage as shown in Figure I.4, the crossing of interconnections is required to furnish the feedback path. The layout of the conventional shift register is shown in Figure I.5 (a). The locations of the various transistors are labeled and correspond to that of Figure I.4. The aluminum interconnection is indicated by the shaded outlines. Note that the width of the shift register cell is widened by the two U-shaped interconnections which correspond to the feedback paths F1 and F2.

In the shielded version of the shift register as shown in Figure I.5(b), the feedback path F2 crosses over the gate of Q3 instead of circumventing around the outskirt of the cell. As a result of this multilayer interconnection and the shielded design, the width of the shift register cell is now reduced to 142μ meters as compared to 180μm for the conventional design.

The complete shift register has 128-bits. The block diagram of the complete shift register[3] is shown in Figure I.6. It consists of selected logic gates, clock amplifiers, logic to permit information to be loaded into the shift register or be recirculated around the shift register, drivers, etc. These peripheral circuits are placed around the 128-bit shift registers matrix as shown in Figure I.7. The peripheral circuits for the shielded design are made the same size as the conventional circuits; however, the width of the p-channel transistors is made wider than the conventional design to better equalize the transconductance.

The layouts for the different levels of the shielded shift register are shown in Figure I.7a-f. For comparison, the conventional CMOS versions are shown in Figure I.8a-f.

The resultant integrated circuit for the shield design is 3110 x 2885 μ^2 in comparison with a dimension of 3718 x 2885 μ^2 for the conventional design. In this design, the saving in chip area is over 20%.

Processing

The processing steps of the shielded integrated complementary MOS transistor structure is shown in Figure I.9. The process follows as much as possible the conventional complementary MOS integrated fabrication steps, except for the provision for incorporating the polycrystalline silicon shield. The detailed steps are as follows:

1. Substrate: ⟨1,0,0⟩, n-type 4-7Ω-cm
2. Thermal oxidation: 5000Å thick
3. Photoengraving for p-well windows (see Figure I.9a)
4. Boron diffusion of p-well: 475Ω/sq, 13.5μ meter
5. Photoengraving for p+ source and drain windows (see Figure I.9b)
6. p+ boron diffusion: 125Ω/sq, 1μ meter
7. Stripping of oxide
8. Gate dielectric: 1000Å SiO_2 + 400Å Si_3N_4
9. Vapor growth of polycrystalline silicon by decomposition of silane (see Figure I.9c): 5000Å
10. Silicon Nitride deposition 500Å.
11. Photoengraving for n+ source and drain windows (see Figure I.9d).
12. n+ phosphorous diffusion: 10Ω/sq, 1μ meter in silicon substrate
13. Photoengraving for etching the polycrystalline silicon to isolate the gate from the shield and the shields for the p-channel and n-channel regions, (see Figure I.9e)

14. Phosphorus doping of polycrystalline silicon: 10Ω/sq, 0.5μ meter
15. Oxidation: 2000Å
16. Photoengraving for contact windows (see Figure I.9f)
17. Aluminization: 7000Å
18. Photoengraving for interconnection (See Figure I.9g)
19. Sintering

The processing steps have evolved considerably during the course of the contract. Improvements incorporated in the polycrystalline silicon deposition process affected the etching characteristics of the poly layer. Modifications in the deposition apparatus permitted a 200°C lower temperature of 600°C to be used. At this lower temperature, the polycrystalline silicon grain structure was finer and tighter, the layer thickness was more uniform across each wafer and the appearance was that of a polished wafer. However, the larger grain structure of the former layers apparently aided the etching process in subsequent photoengraving steps. Longer etching times become necessary with the improved layers aggravating the already significant undercutting problem. The course of action taken was to solve the photoengraving problems since the improved polycrystalline layers exhibited properties necessary for high resolution.

After the processes were developed with test wafers and device runs were started, it became apparent that the photoengraving techniques behaved differently when applied to device runs.

Response of the polycrystalline silicon layers to acid depended

on the history of prior operations on the device wafers. Subsequently, it was found that subjecting the poly layers to a high temperature operation with either a nitrogen or an oxidizing atmosphere caused the silicon grains to become coated with silicon nitride or silicon dioxide. In this event, the time required to etch completely through a 3000Å polysilicon layer would increase from 30 seconds to 10 minutes. The times could be reduced by alternating between the polysilicon etch (12 parts Acetic Acid, 5 parts Nitric Acid and 1 part Hydrofluoric Acid) and an oxide or nitride etch. Although this could not be considered a realistic solution since multiple dips in either oxide or nitride etch would be incompatible with existing masking techniques, the nature of the problem is demonstrated.

The effort to develop a viable silicon gate process continued with the purchase of plasma etching equipment to photoengrave silicon and silicon nitride layers. This apparatus is capable of etching undoped polysilicon layers into high resolution with very little undercutting.

Since the best photoengraving results are obtained with undoped polysilicon layers, the processing sequence was modified to incorporating a silicon nitride layer over the polysilicon. The silicon nitride prevents the phosphorous from diffusing into the polysilicon during the n^+ source and drain diffusion without affecting the self aligning feature. The overcoating with silicon nitride does not complicate the photoengraving since the plasma device etches nitride and silicon with equal ease. After the last remaining polysilicon etching step immediately following the phosphorus diffusion, the overcoat of nitride is stripped by chemical means and the poly layer is doped by phosphorus diffusion. This is the

process used to fabricate the shielded shift register device shown in Figure I.10.

The standard unshielded shift register was made using similar processing parameters to permit a meaningful comparison. The standard chip is shown in Figure I.11.

Characteristics of Shielded CMOS Integrated Devices

The completed test devices in an experimental integrated circuit were evaluated. Some of the salient characteristics are as follows:

Threshold Voltage: The threshold voltage was obtained by connecting the gate to the drain and measuring the drain to source diode characteristics. Typical p-channel and n-channel characteristics are shown in Figure I.12a and I.12b, respectively. In Figures I.12 and I.13, unit #1 and unit #2 are representative of the two extremes of low and high threshold voltages. If the threshold voltage is taken as the gate voltage corresponding to 10μa of current, then the threshold voltages for the p-channel are -1.5V and -2.2V and that for the n-channel are 1.7V and 3.3V. The spread in threshold voltages within the same run is of the order of 0.1V. The values of the threshold voltages and the spread in these values from run to run are those typically obtained with conventional aluminum-gate CMOS integrated circuits, thus implying that the n-doped silicon gate has essentially the same work function as the aluminum gate.

Output Characteristic: The typical output characteristics of the p-channel transistors and the n-channel transistors are shown in Figures I.13a and I.13b. The n-channel transistor has a higher transconductance (more than 2 times) than the p-channel transistor as expected from the difference in mobilities of electrons and holes. The drain breakdown

voltage of 18 volts is somewhat lower than the conventional 20+ volts. This is probably due to the shallow n+ junction resulting in a sharper curvature.

Effectiveness of the Shield: The effectiveness of the shield was tested on a test transistor with the silicon gate shorted to the background and the aluminum field plate biased to the voltage steps supplied by the Tektronix 575 Curve Tracer. Up to 18v was applied to the field plate and a negligible amount of current could be observed for either p-channel or the n-channel.

No higher voltage can be applied to the field plates of the n-channel transistors because the aluminum field plate is clamped by a protective diode. A much higher field plate voltage can be applied to the p-channel transistors, because the protective diode has a higher breakdown voltage (>50V).

In the design of the test transistor the shield is isolated from the substrate. Both the field plate potential and the shield potential can be varied independently. Figure I.14a shows the n-channel drain characteristics with the field plate potential at zero and the shield potential as running parameter. Figure I. 14b shows the characteristics with the field plate at 18V. Figures I. 15a and I.15b show corresponding characteristics for the p-channel device. Note that the two sets of curves are indistinguishable. Note also that the current is zero when the shield potential is below the threshold voltage of the transistors. From these observations, one can conclude that the field shield is very effective in preventing surface inversion beneath the interconnections.

Stability: The stability of the n-doped silicon gate CMOS structure can best be tested by observing the C-V curves. C-V measurements were made on the capacitors on the chip.

Figure I.16 shows the C-V curves of an n-doped gate on p-type and an n-doped gate on n-type backgrounds. The curves show that the capacitance for n-substrate drops to a low value with negative gate voltage, meaning that the p-channel device is in enhancement mode. Similarly, the flat-band voltage for the p-background is positive, meaning that the n-channel is also in enhancement mode. The n-substrate capacitance drops to lower value than the p-background capacitance, because the n-substrate has a lower impurity concentration than the surface concentration of the p-well.

Figure I.17 shows the C-V curve of an n-doped gate on n-type substrate under various conditions. In addition to room temperature bias, the sample was subjected to temperature-bias test at ± 20 volts and $200^{\circ}C$. All readings were taken at room temperature. Note that there is very little shift in the characteristic with respect to room temperature bias conditions, indicating that the characteristics are very stable.

For comparison, a p-doped gate MOS capacitor was fabricated on an n-type substrate using similar processing steps and subjected to temperature bias. The C-V curve is shown in Figure I.18. Note that there is approximately a half-volt shift in the characteristics. This instability was also reported by other investigators[4].

From this comparison, we can see that the n-doped gate is more stable than the p-doped gate. This stability is probably due to the diffusion of phosphorous into the gate oxide, thereby complexing any mobile ions and preventing them from moving[5].

Inverter Operation: The input-output characteristic of two typical inverters is shown in Figure I.19 corresponding to the transistors in Figure I.12. Note that the output voltage drops to zero when the input

voltage exceeds 2-3V, indicating that the operation of the inverter should be satisfactory from 3V up to the breakdown voltage of either transistor. Since the n-channel transistor has a lower breakdown voltage of 18V, the maximum operating voltage limit should be set at a lower value, perhaps 15V.

Testing of Shift Register

A tester was built to evaluate the shift register. It is suitable for both the conventional shift register and the shielded shift register. The shift register is designed such that two conditions are met to shift data into and out of the register:

POWER ON: The Power On must be low in order for the clock to be gated into the register. When Power On goes high, $\emptyset$ is held high, which inhibits shifting and retains the data in the register.

SELECT DECODING: The four Exclusive-Nor gates perform selection decoding for the register. By hard-writing one set of inputs (i.e., $Y_1 - Y_4$), one out of 16 shift registers can be selected. Full identity at each of the X-Y pairs is necessary; when any $X_i \neq Y_i$, then $\emptyset$ is held high and the shifting is inhibited.

When these conditions are met, the following operations can be performed:

TRANSFER: With "Load" =1 and "Transfer" = 0, data is transferred into the register from the FAS input. The data entering the register also appears at the Q and $\bar{Q}$ outputs. By connecting TAS to FAS, data in the register can be recirculated, under control of the "Transfer" command.

LOAD: With "Transfer" = 1 and "Load" = 0, new data can enter the register via the INFO terminal. Q output = 1; $\bar{Q}$ = 0.

STORE: With "Load" = 1 and "Transfer" = 1 no shifting takes place. The FAS input appears on Q and $\bar{Q}$.

CLEAR: With "Load" = 0 and "Transfer" = 0, Q will be high; $\bar{Q}$ will be low. The clock will load "0"s into the register.

Description of the Tester. The tester is designed to test the 128 Bit CMOS Statis Shift Register only. The testing circuit (Fig.I.20) generates the two control and the clock waveforms required by the Device Under Test (DUT). The clock wave form is generated by two NOR gates connected as an astable multivibrator; the clock frequency is $\frac{1}{2}$ the astable frequency. Internal control of the TRANSFER and LOAD control inputs, and generation of the INFO waveform, the test data to be stored, is accomplished by a 7-stage shift register and decoding gates. This shift register has two outputs, one of which, the SYNC output, is high once every 128 clock pulses. The other output is the INFO output. The SYNC output is used as a timing pulse for LOAD and TRANSFER, since these control inputs can only change state once every 128 pulses. The SYNC output can also be used as the Sync for an oscilloscope.

Figure I.21 shows the chassis of the tester. The DUT terminals are connected to the multi-prong prober to the right. Figure I.22(a) shows the generated INFO waveform (top) and the CLOCK waveform (bottom). Figure I.22(b) shows the INFO waveform (top) recirculating in an integrated shift register and the output CLOCK signal (bottom) of the shift register.

Operating Conditions.

A. Power Supply - use a negative ground power supply, V_{SS} as ground, with $V_{DD} - V_{SS} = 10$ volts.

B. Connections to oscilloscope - For direct comparison of waveforms, a dual trace scope works best. Scope Sync connects to SYNC terminal on left side of case. Vertical input terminals connect to any of the output terminals on the left side of the case.

C. Operation - Before data can be entered into the register, each Xi must equal each Yi, the CLK and INFO switches must be low, and PWR must be high. To view the data on the scope, it must recirculate thru the SR, therefore, the REC switch must be low.

1.) With the TRANS switch low, data is entered into the register whenever the LOAD switch is moved from low to high.

2.) To view the data on the oscilloscope, the REC switch must first be low. Data is entered into the register as in part 1. With LOAD switch still high, set the TRANS switch from low to high. Data should now be recirculating in the register, and should be visible on scope.

Evaluation. The completed conventional shift register as well as the completed shielded vervion were tested. For the conventional shift register, it was revealed by probing that there are operational individual logic gates for every gate, from G, through G_{17} in Fig. I.7. Clock outputs were observed at the output terminals of many chips. When the signal was injected with a probe at the "DATA IN" point in Fig. I.9, it was found that the signal can propagate through many stages of the matrix. However, the yield of the shift register is so low that no chip was found that can have the signal propagate through the 128 stages. Nor have we found any unit that has the signal propagate from "INFO" input to the "DATA IN" point of the shift register.

Modified Design. Due to the low yield of processing, it was decided to fabricate one version with a fewer number of cells. For convenience in topology, a sixteen-bit was chosen using two columns of the shift register bits. Another modification allows a signal to be injected at the "DATA IN" point of the shift register instead of all the way from the "INFO" input, thus bypassing most of the control logic.

The modifications involved some changes in the "Contact" and "Interconnection" masks. The modified interconnection mask is shown in Figure I.3.

For the same reasons, the shielded shift register was also modified. The interconnection mask layout is shown in Fig. I.22.

Summary

A shielded complementary MOS integrated circuit structure was developed. N-doped polycrystalline silicon was used for all the gates and the shield. The threshold voltages obtained on a ⟨1,0,0⟩ oriented silicon substrate ranged from 1.5V to 3V for either channel -- nearly the same as conventional CMOS integrated circuits.

The effectiveness of the shield was demonstrated by constructing a special field plate over certain transistors. When high potentials were applied to the field plates, no drain current could be observed when the gate was connected to the background.

Integrated inverters performed satisfactorily from 3 to 15 volts, limited at the low end by the threshold voltages and at the high end by the drain breakdown voltages of the n-channel transistors.

The stability of the new structure with an n-doped silicon gate as measured by the shift in C-V curve under 200°C + 20V temperature-bias

conditions was better than conventional aluminum gate or p-doped silicon gate devices presumably due to the doping of the gate oxide with phosphorous.

In a 128-bit shift register design, the shielded structure results in a 20% reduction in area.

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LIST OF FIGURES

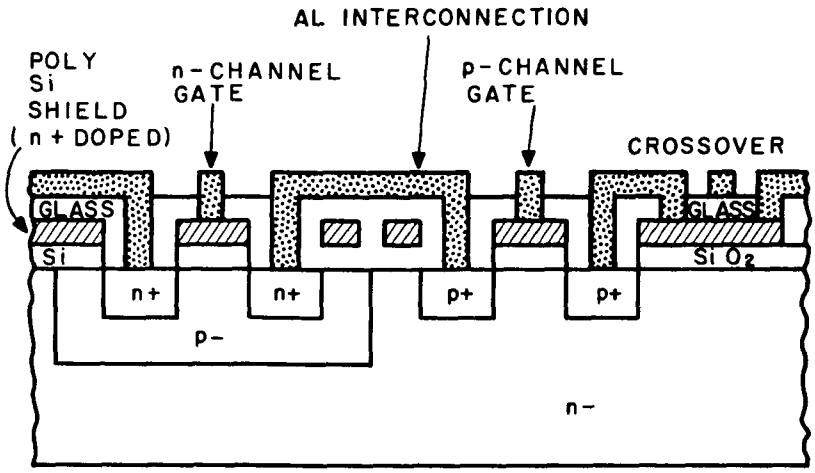


Figure I.1. Shielded CMOS Structure with N-Doped Gate

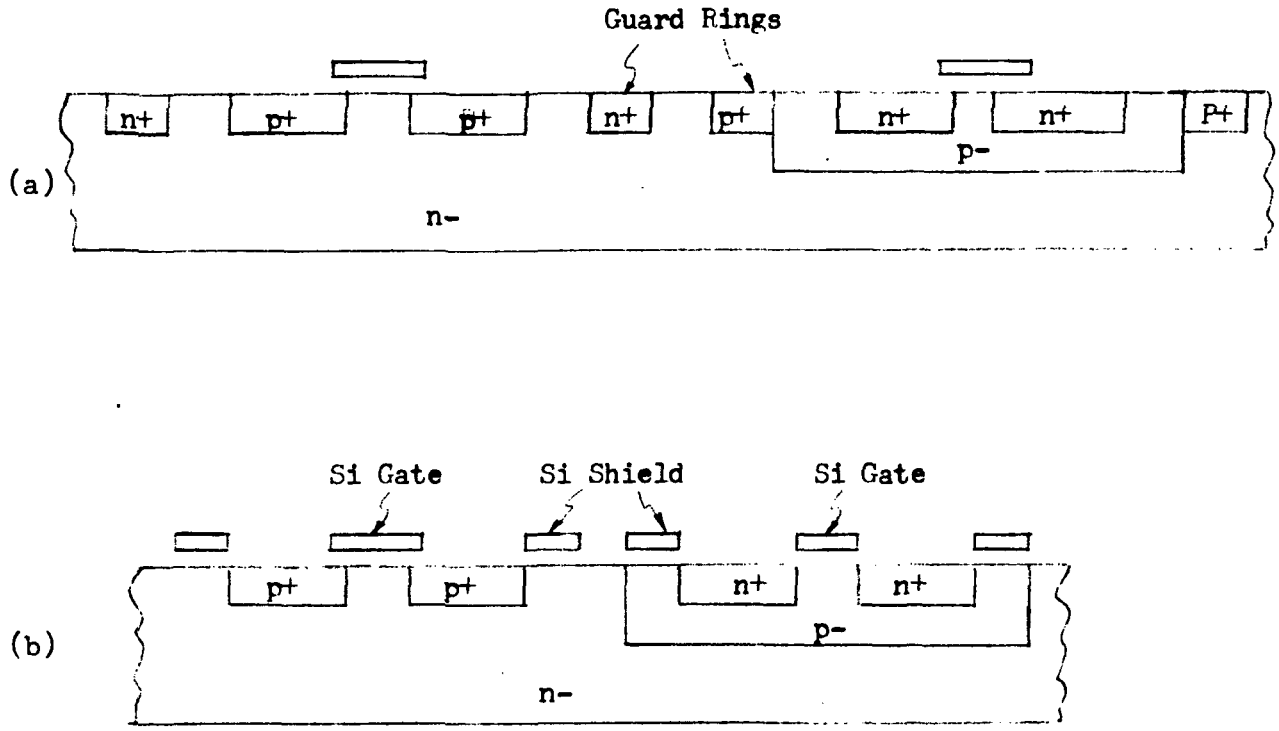
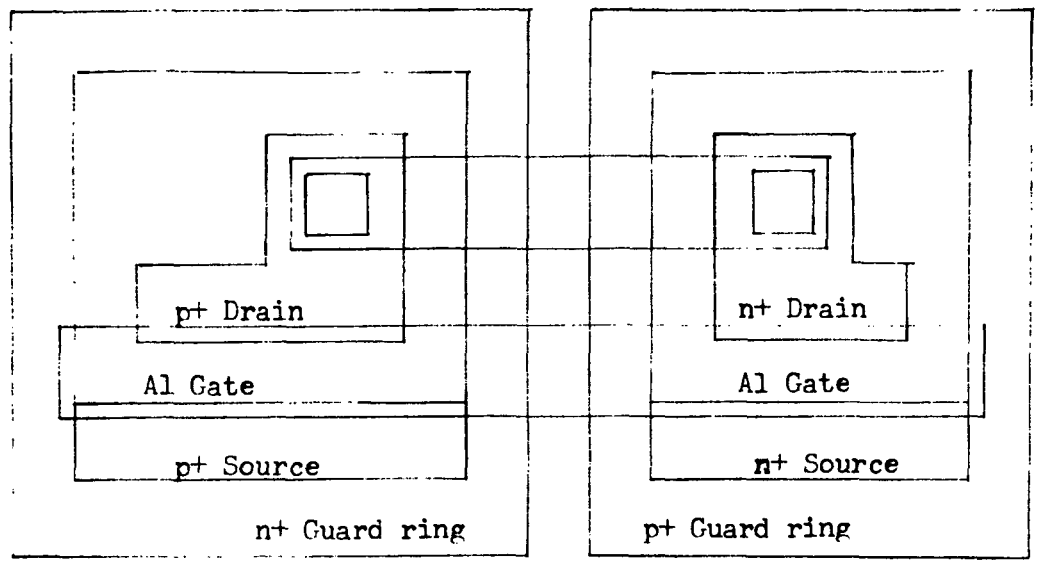
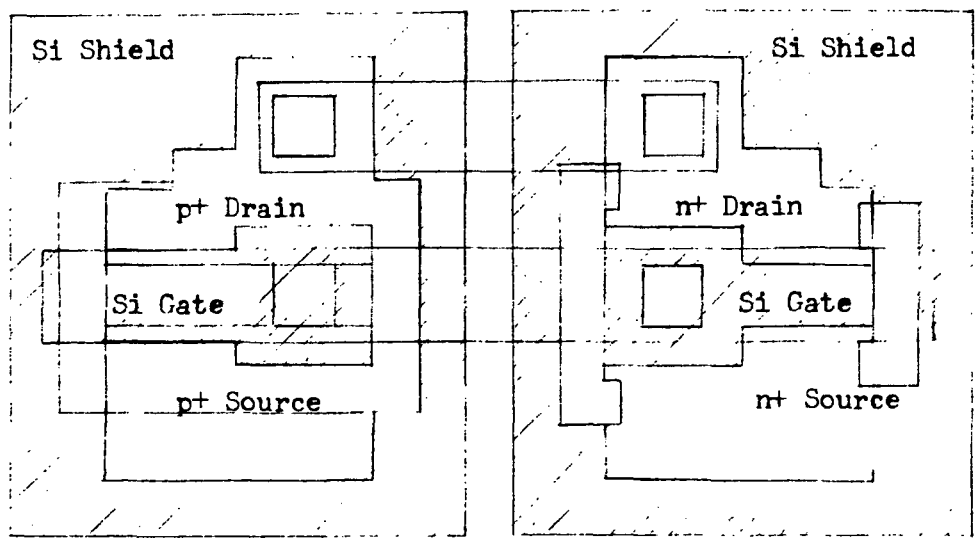


Figure I.2. Guard Ring for Conventional Integrated Circuit vs. Field Shield



(a) Conventional CMOS inverter



(b) Shielded CMOS inverter

Figure I.3. CMOS Inverter

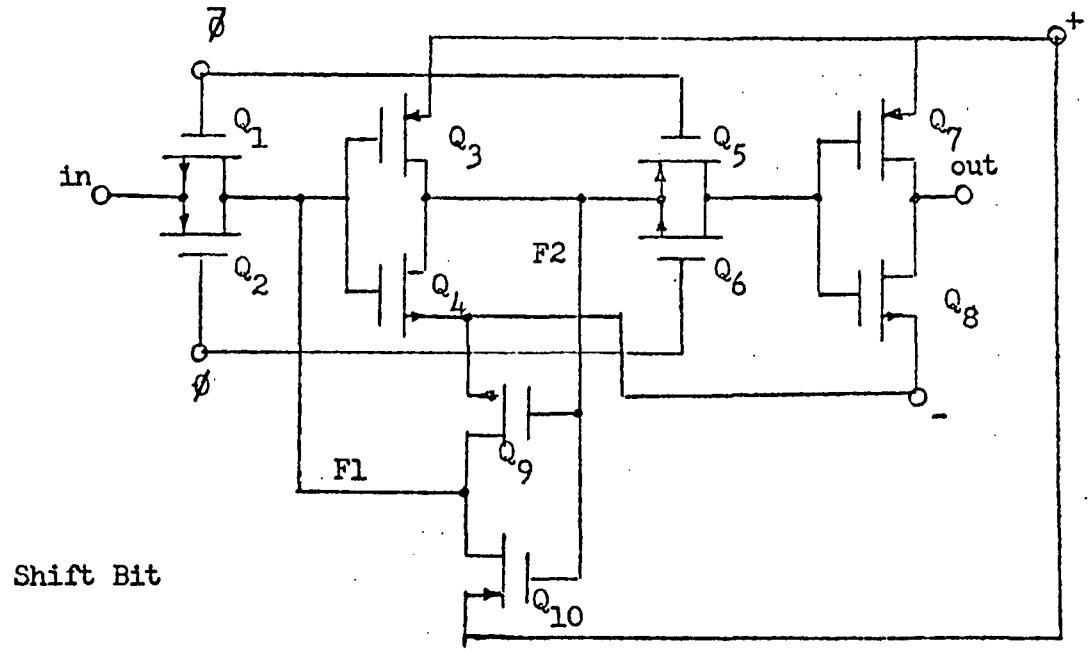


Figure I.4. 1-bit Shift Register

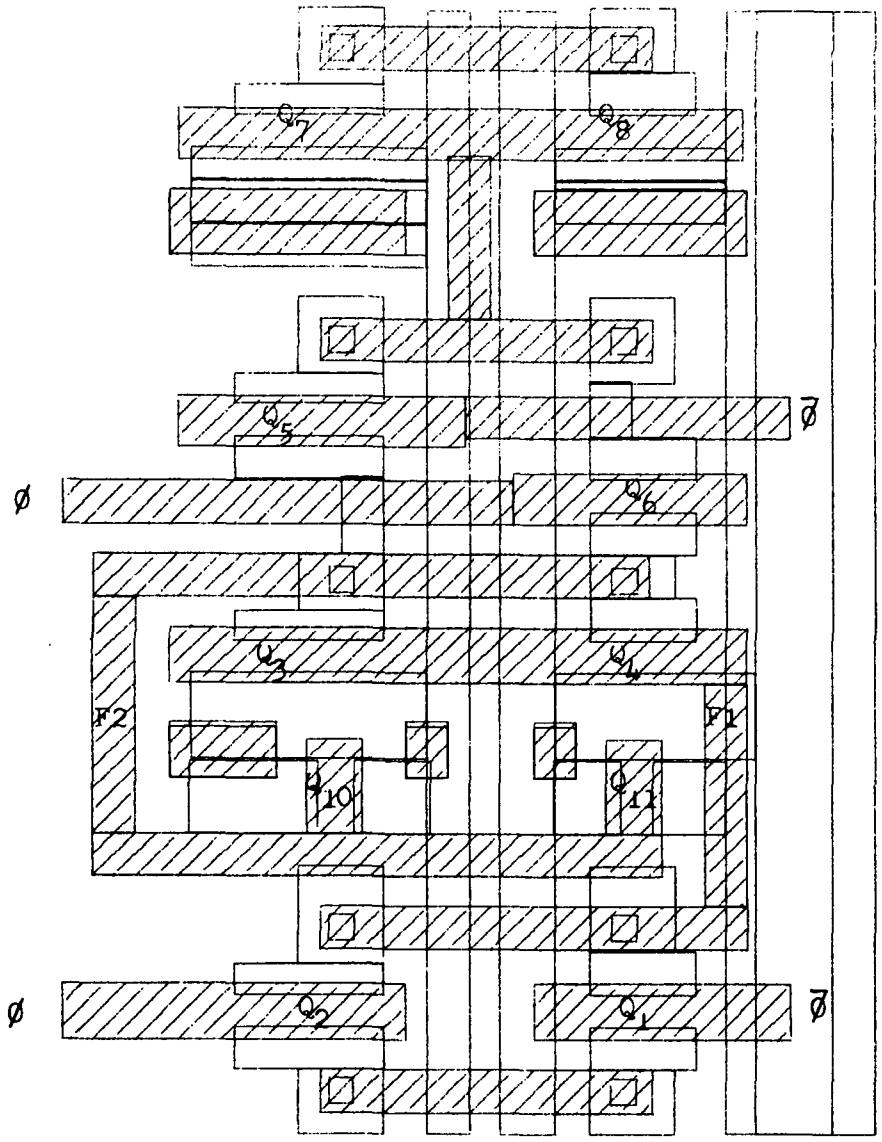


Fig. I.5(a)

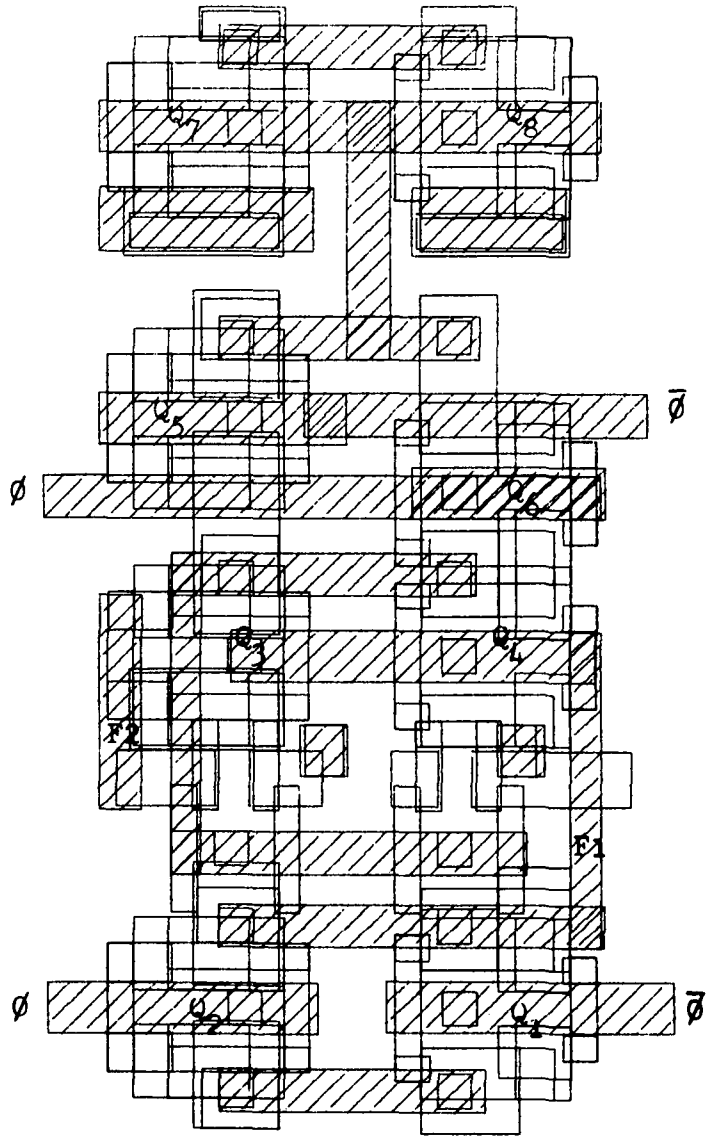


Fig. I.5(b)

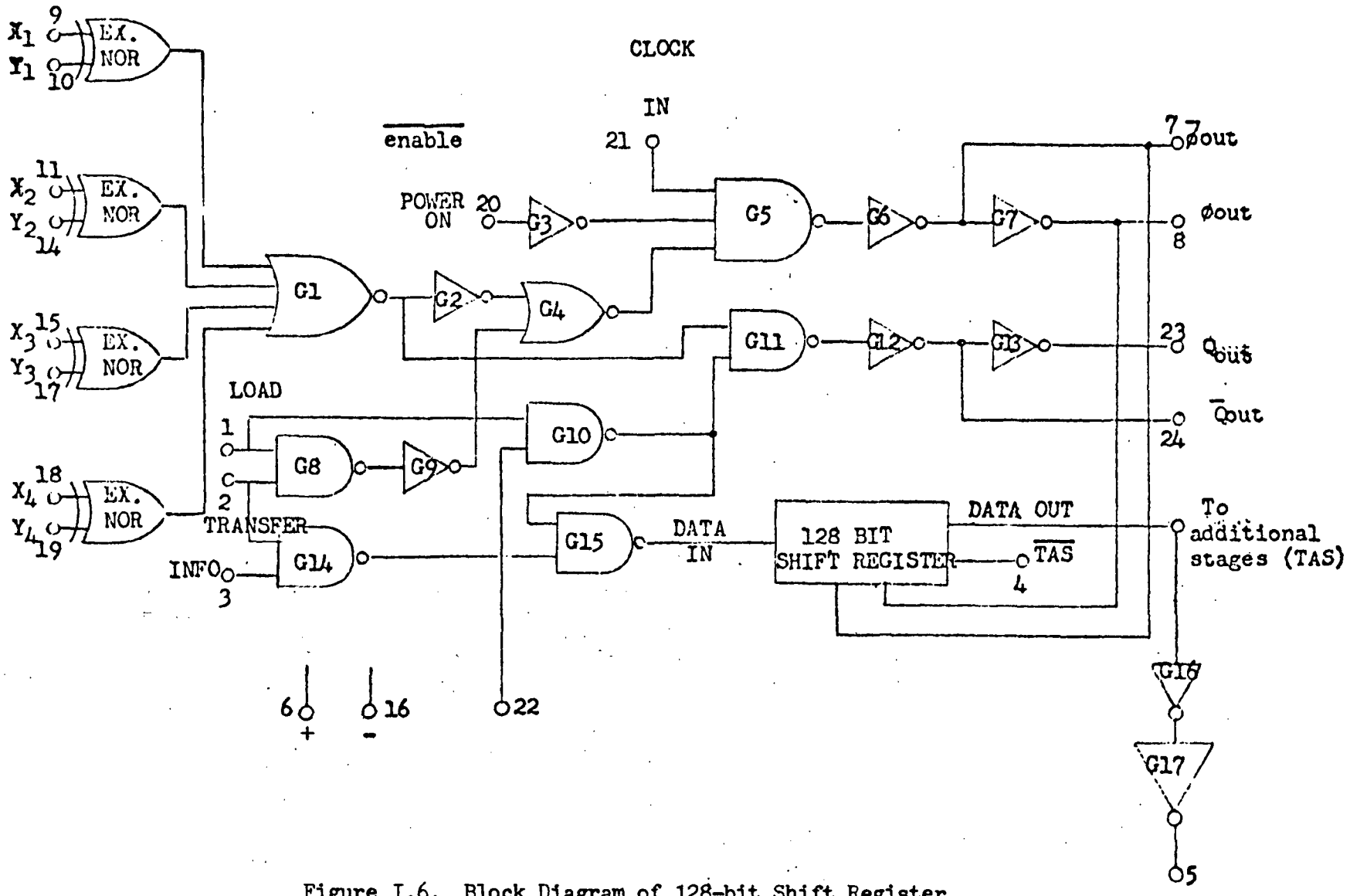


Figure I.6. Block Diagram of 128-bit Shift Register

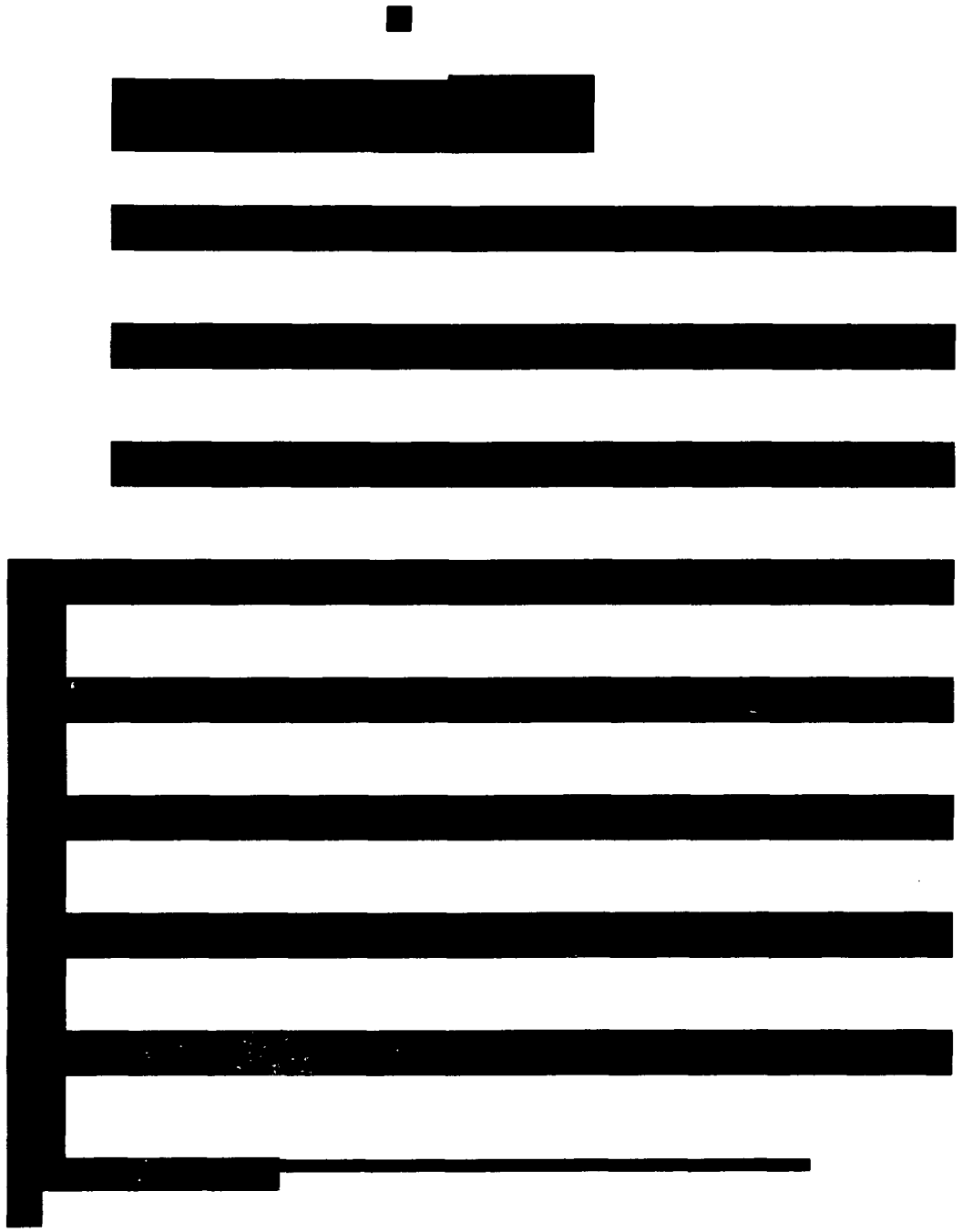


Figure I.7a. P-Diffusion

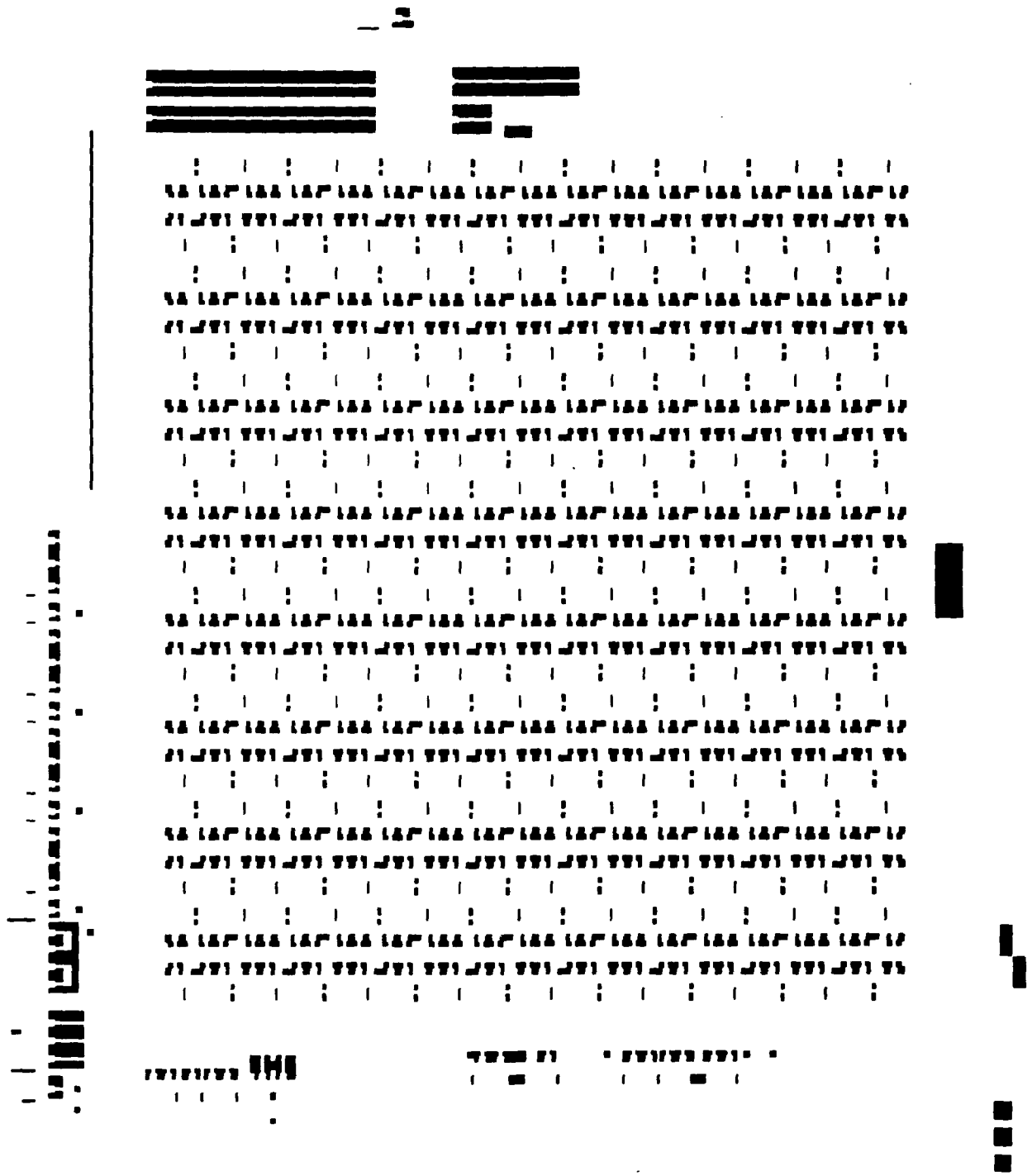


Figure I.7b. N+ Diffusion Mask

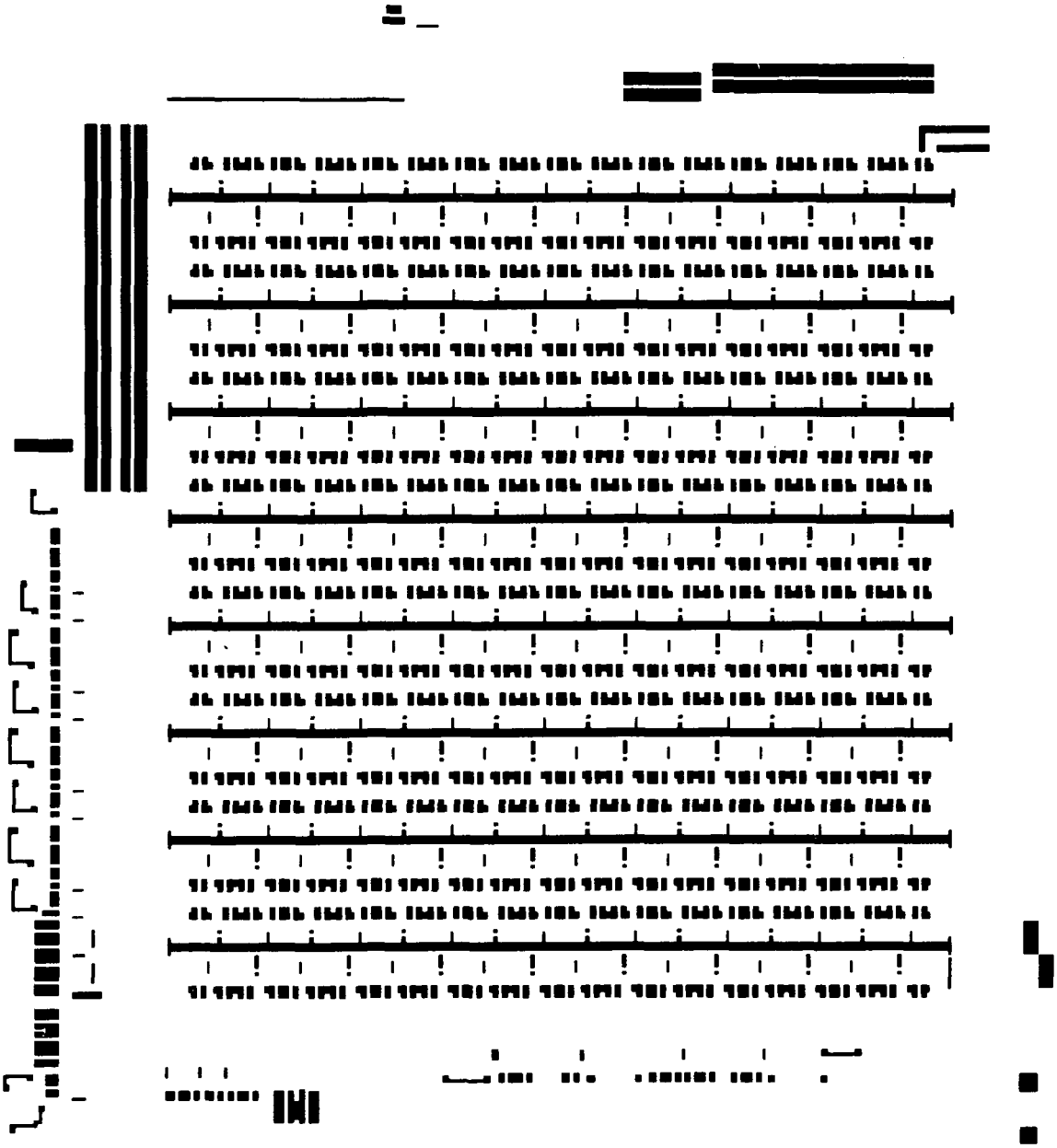


Figure I.7c. P+ Diffusion Mask

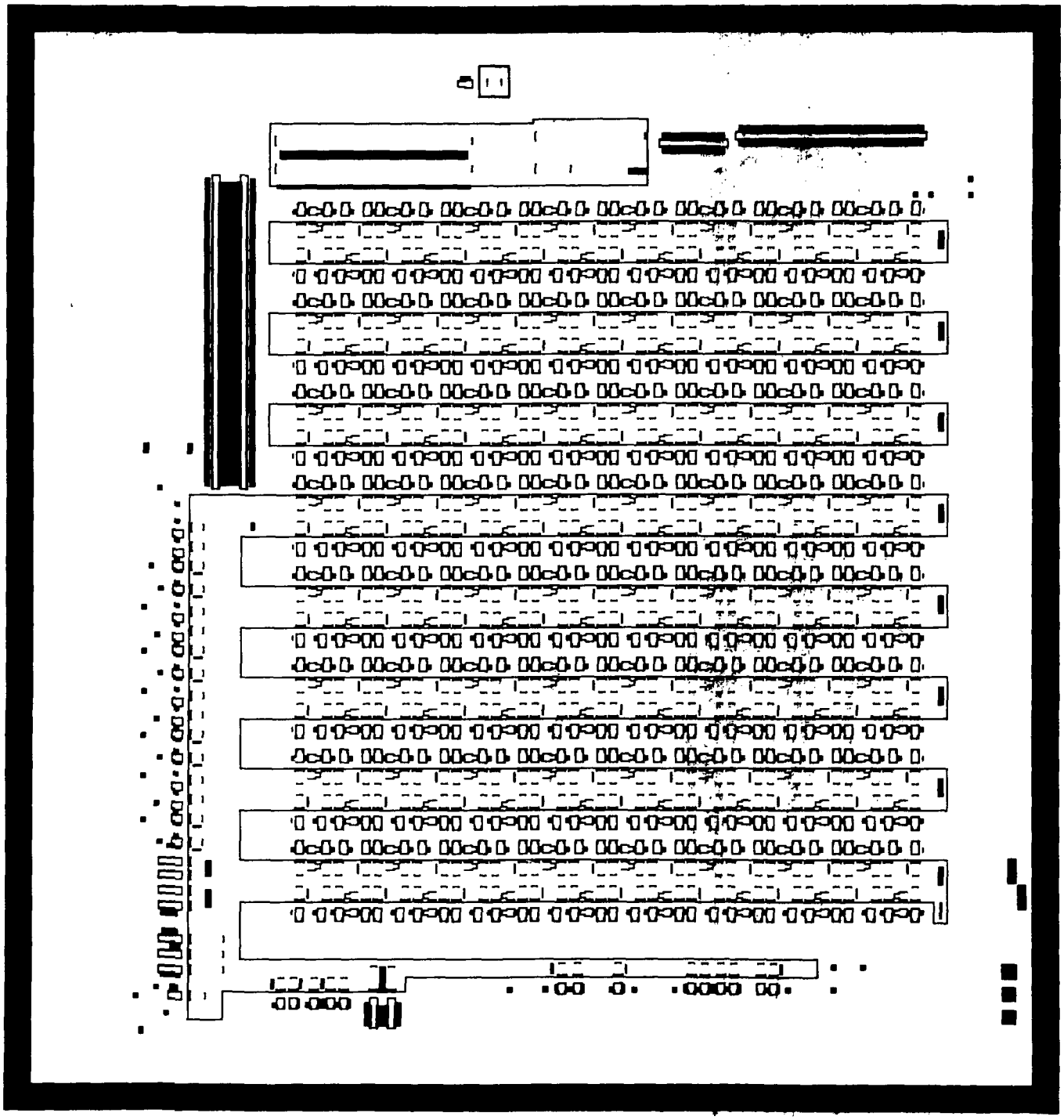


Figure I.7d Si Etch Mask

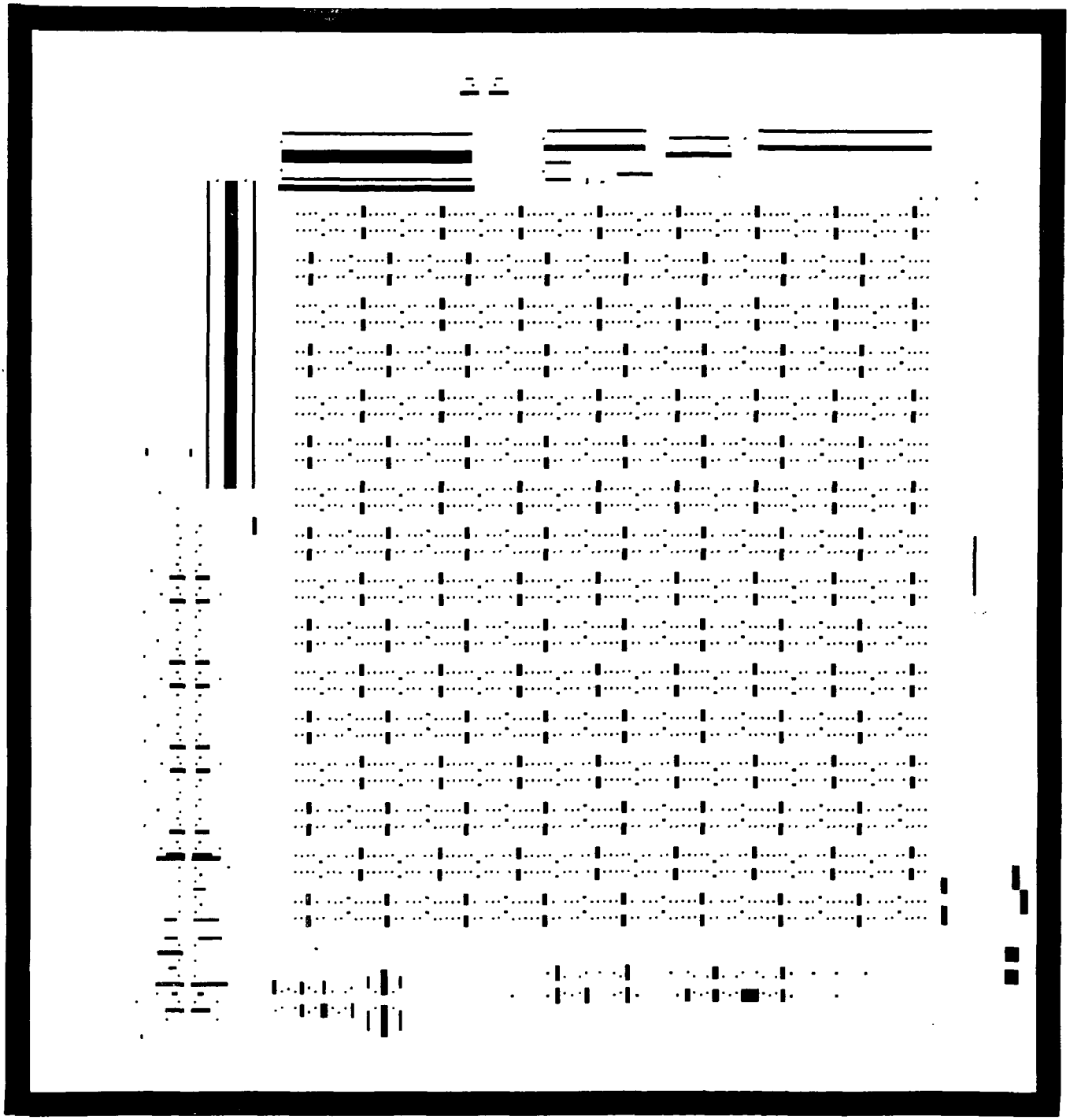


Figure I.7e Contact Mask

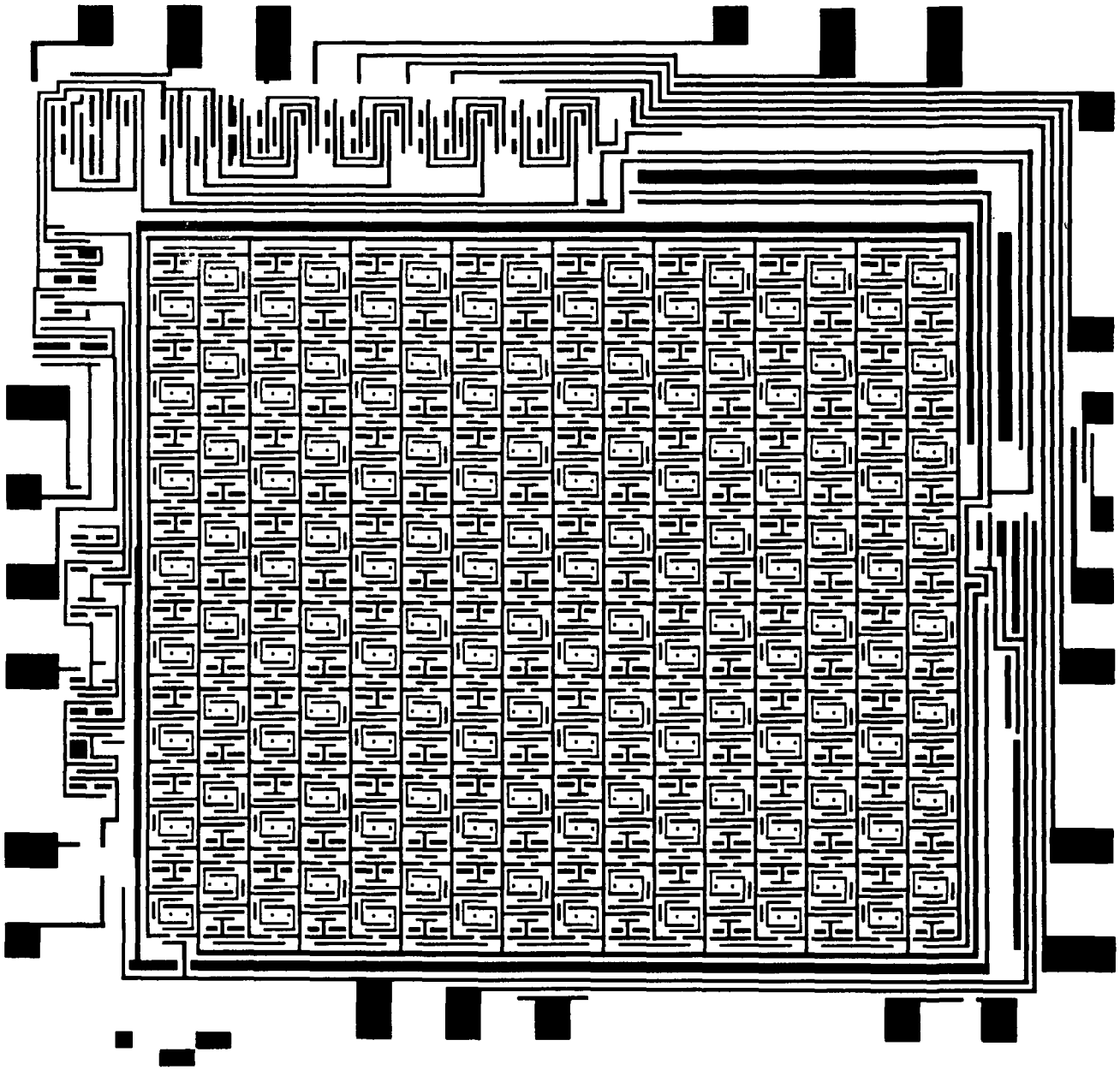


Figure I.7f Interconnection Mask

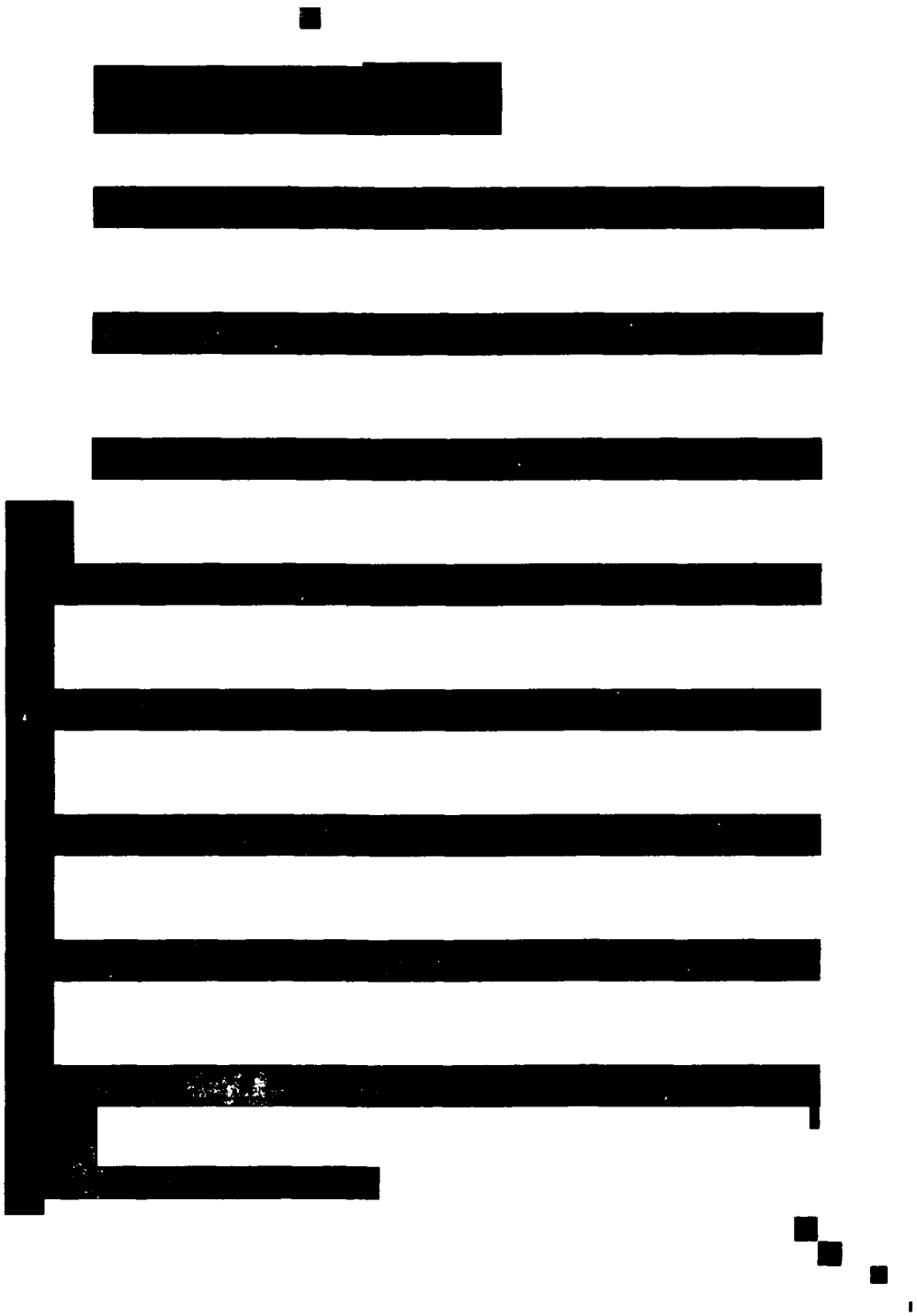


Figure I.8a P-Diffusion Mask

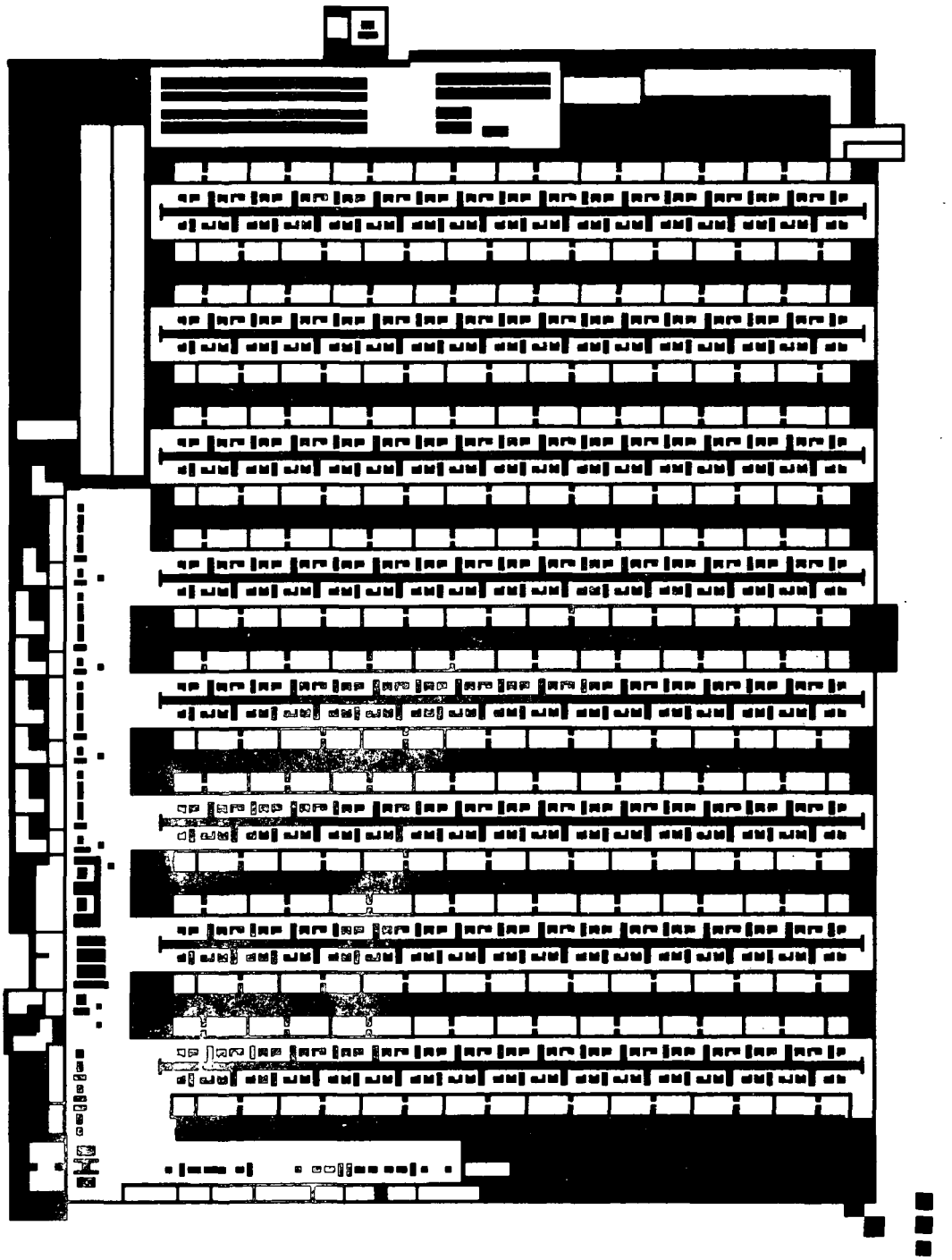


Figure I.8b N+ Diffusion

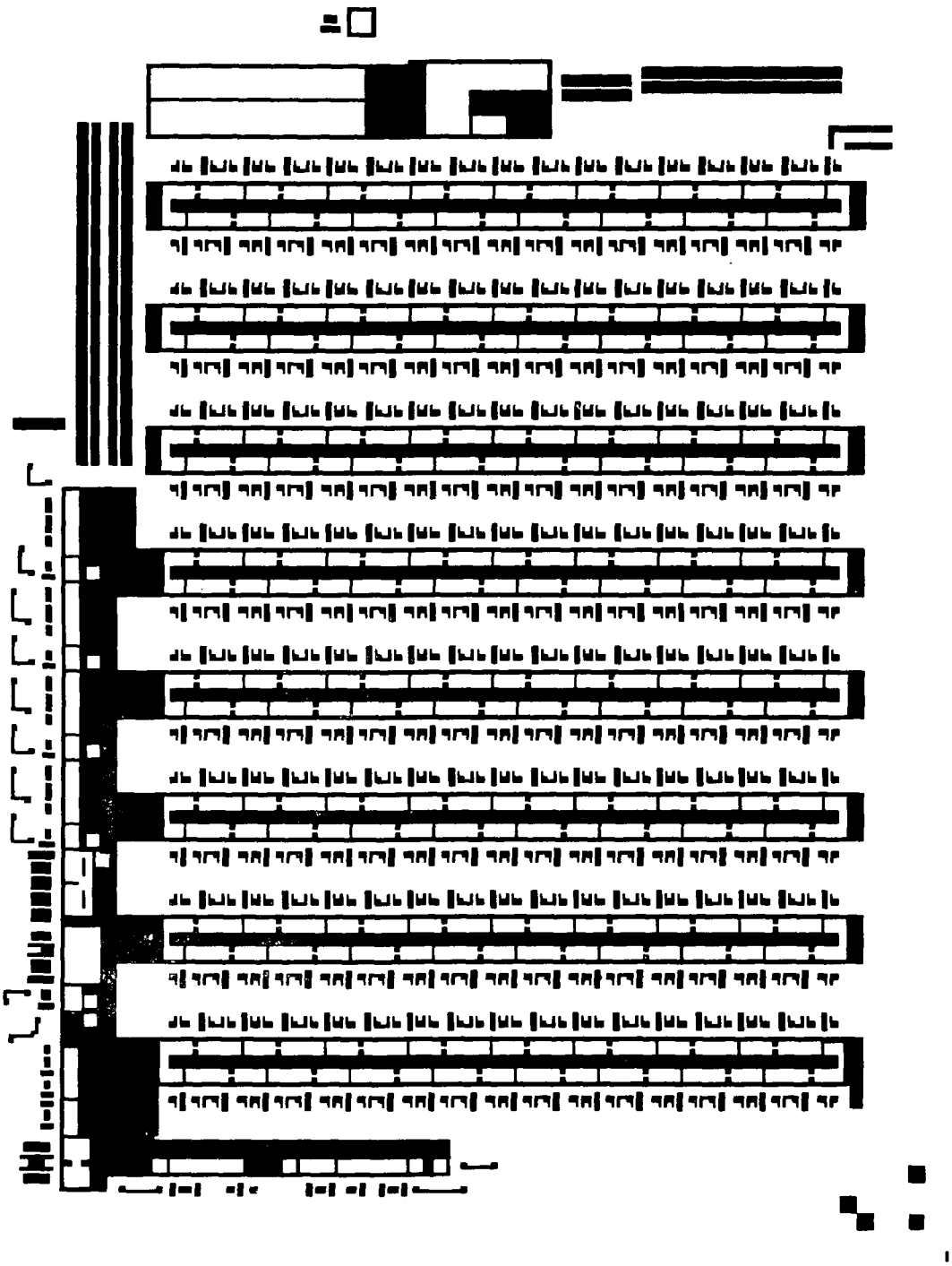


Figure I.8c P+ Diffusion Mask

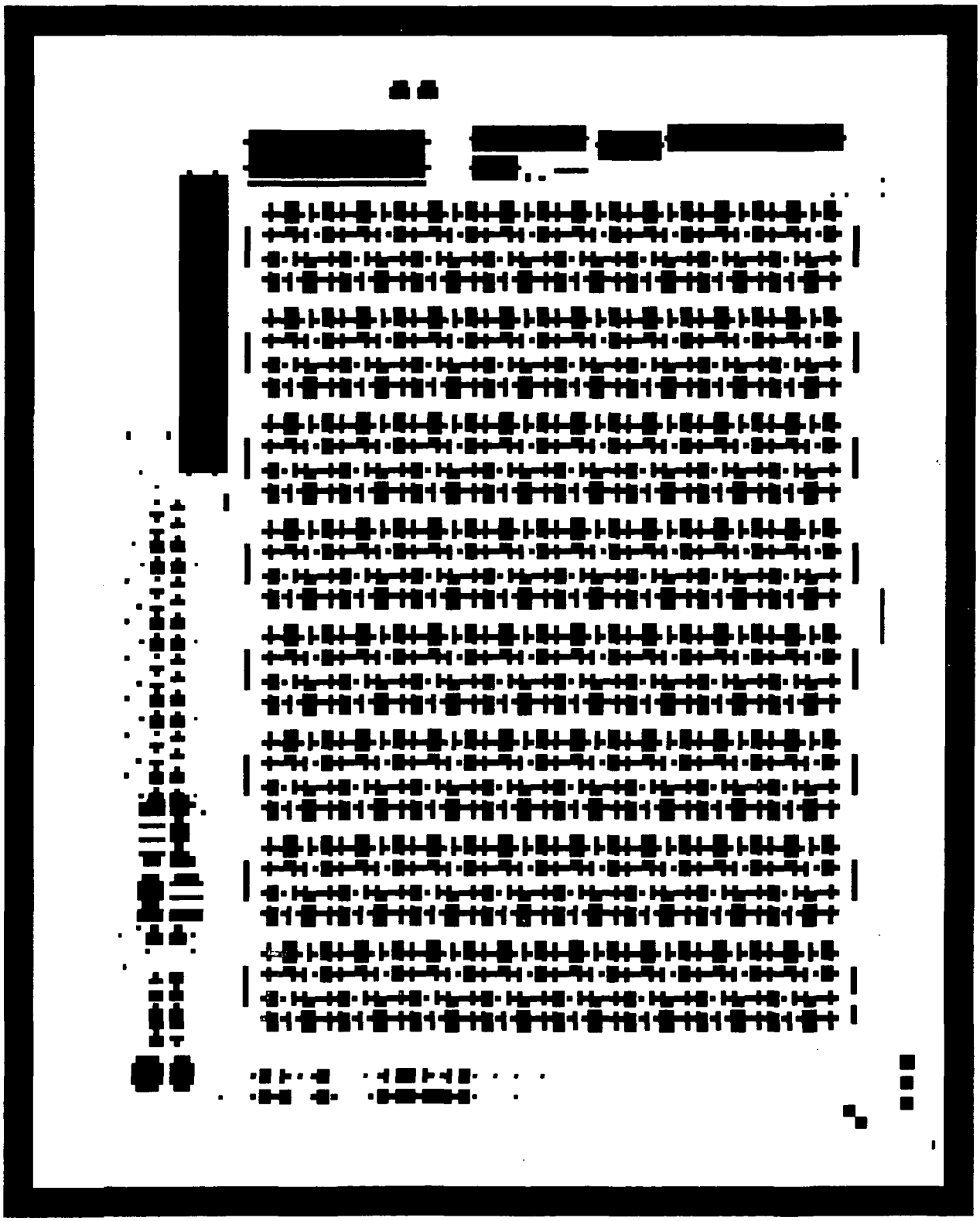


Figure I.8d Gate Oxide Mask

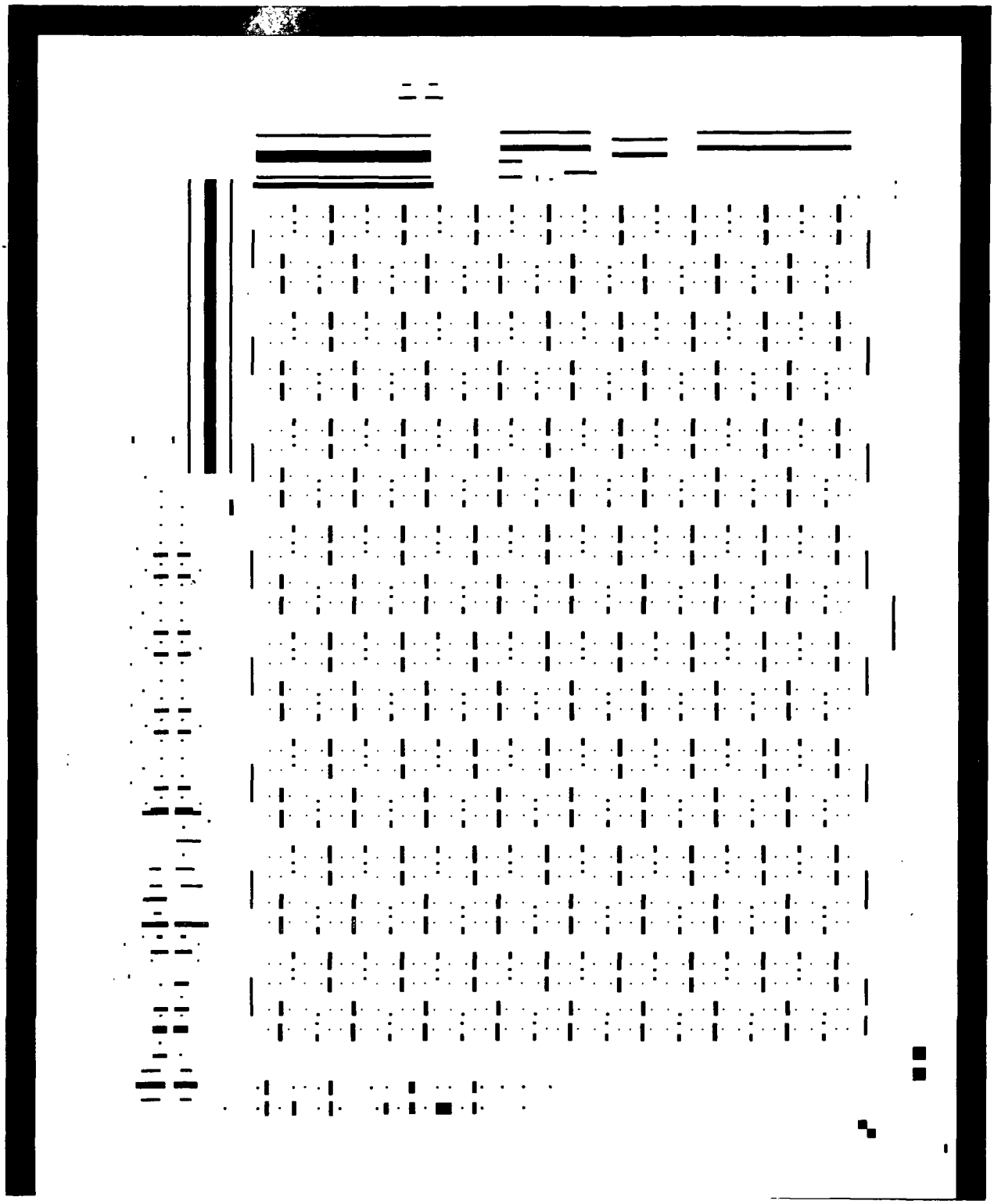


Figure I.8e Contact Mask

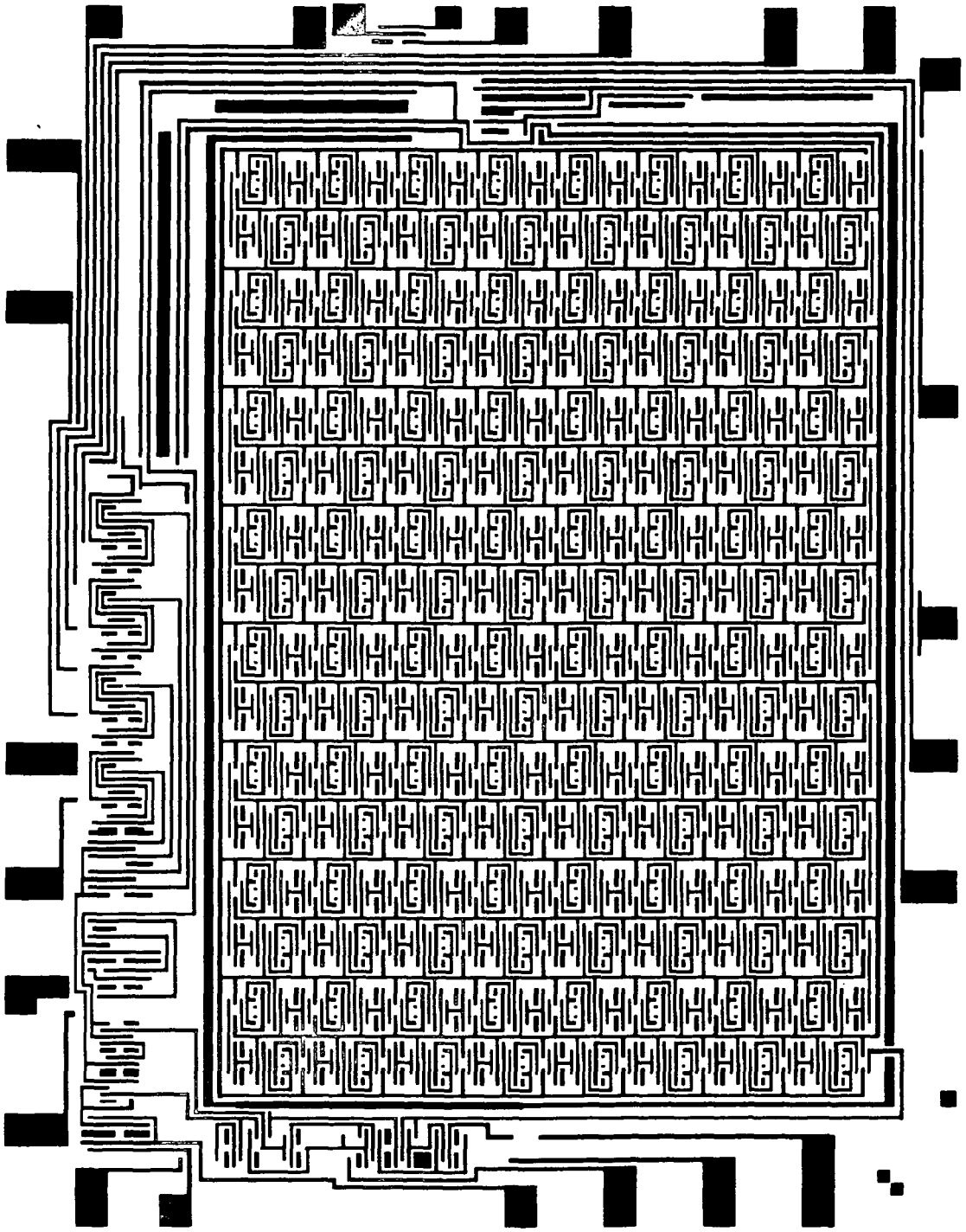


Figure I.8f Interconnection Mask

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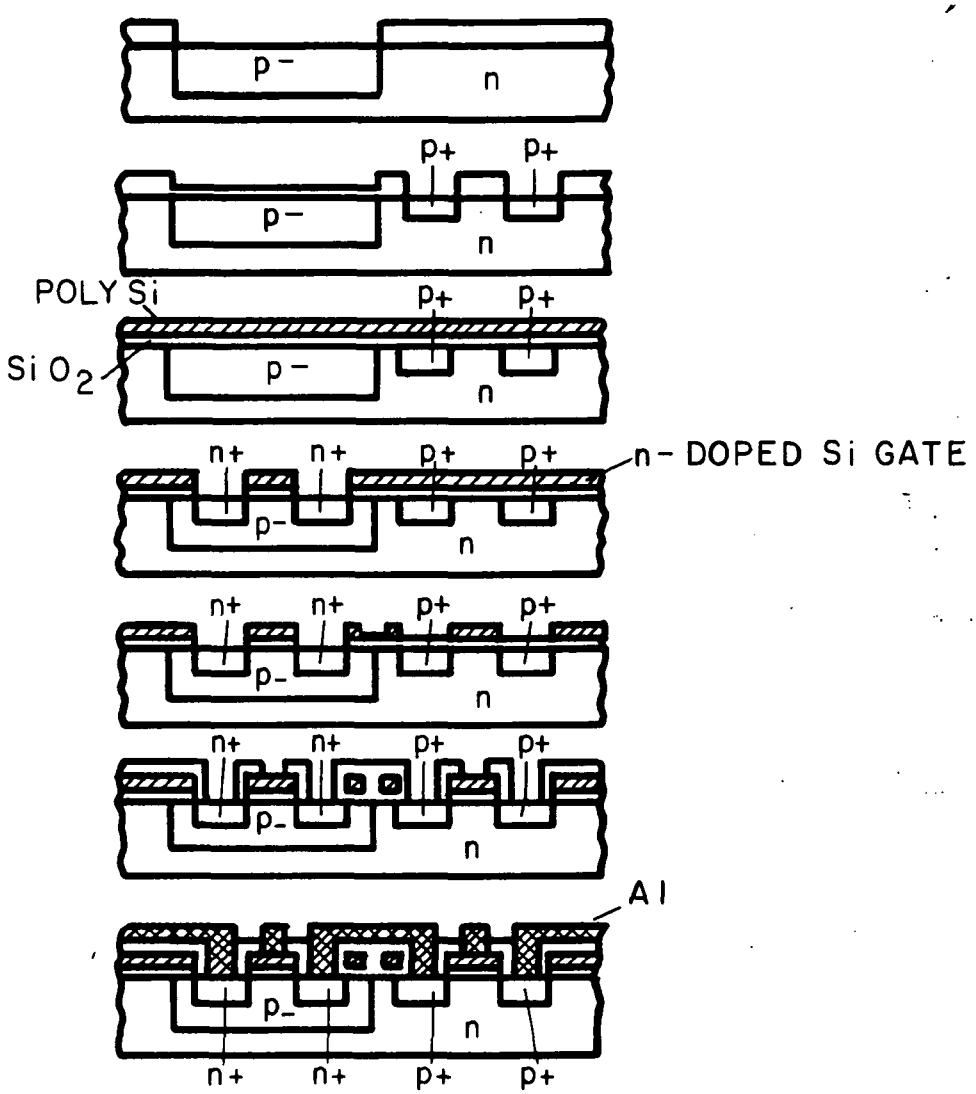

p−
n
p+
p+
p−
n
POLY Si
p+
p+
Si O2
p−
n
n+
n+
p+
p+
n- DOPED Si GATE
p-
n
n+
n+
p+
p+
p-
n
n+
n+
p+
p+
p-
n
Al
p-
n
n+
n+
p+
p+

Fig. I.9

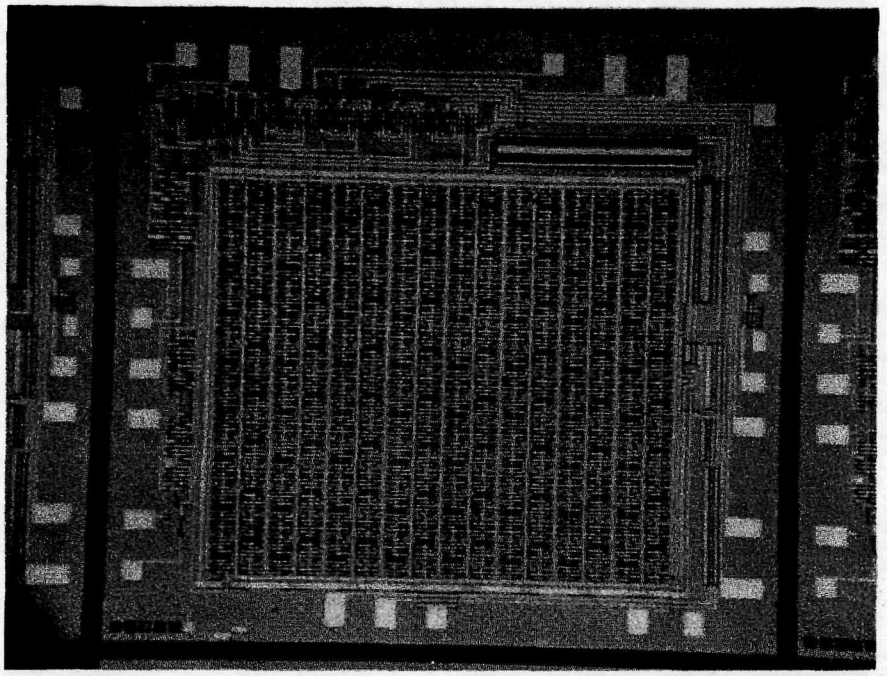


Figure I.10

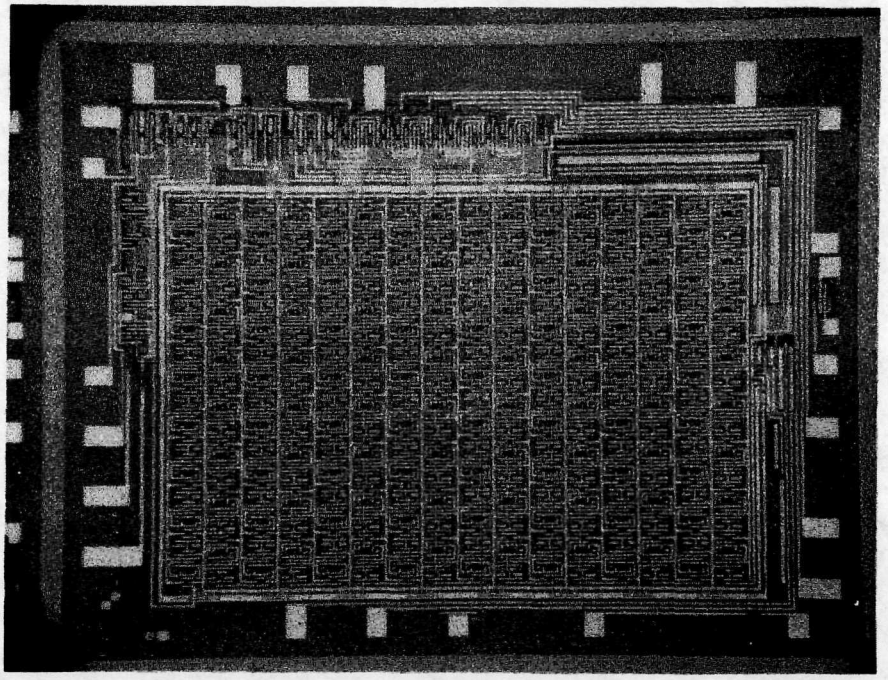


Figure I.11

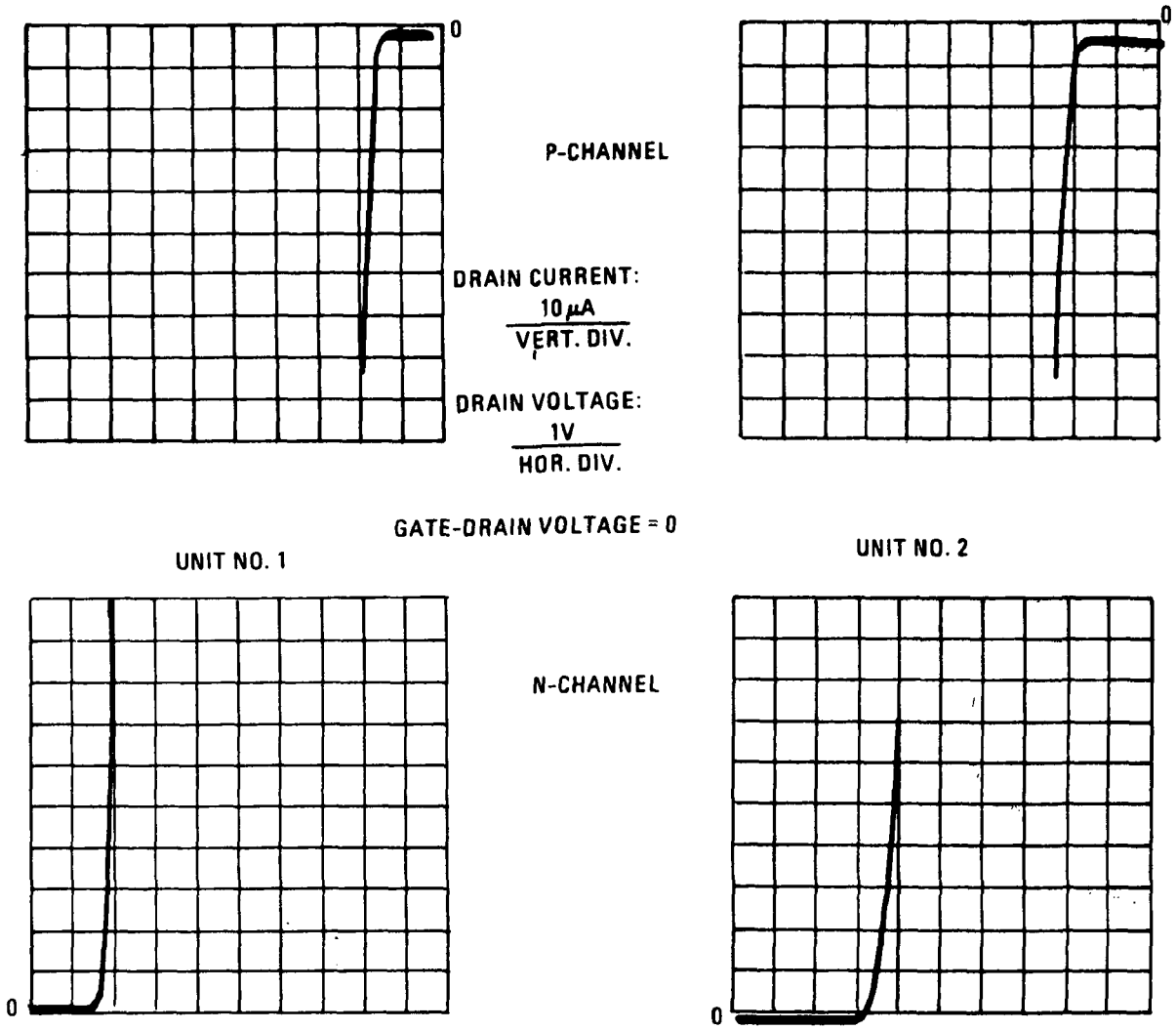
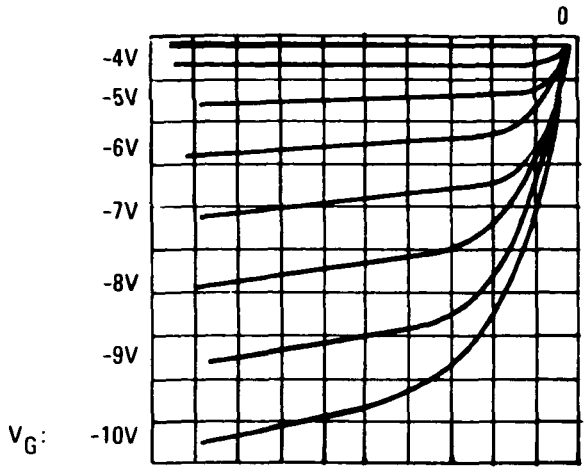
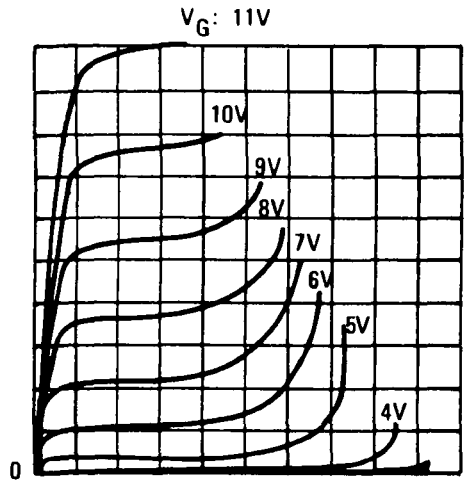

0
P-CHANNEL
DRAIN CURRENT:
10 μA
VERT. DIV.
DRAIN VOLTAGE:
1V
HOR. DIV.
0
GATE-DRAIN VOLTAGE = 0
UNIT NO. 1
UNIT NO. 2
N-CHANNEL
0
0

Fig. I.12

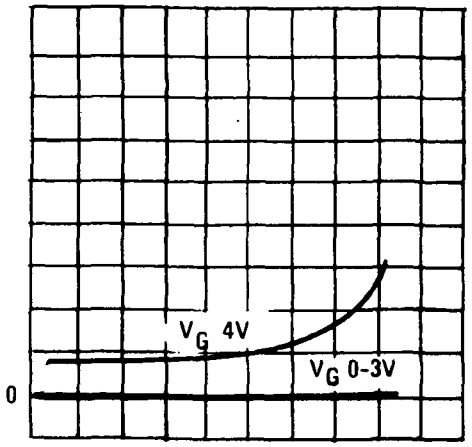


(a)



(b)

Fig. I. 13

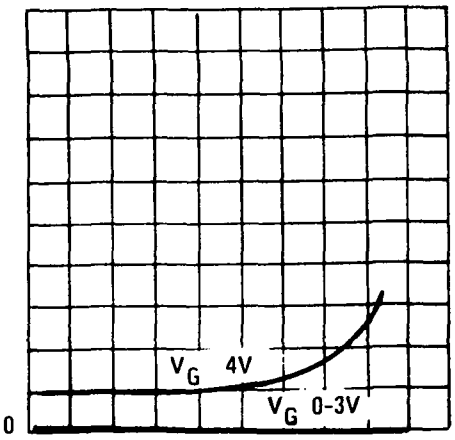


Drain Current: 5mA/vert.div.

Drain Voltage: 2V/Hor. div.

$V_{field\ plate} = 0$

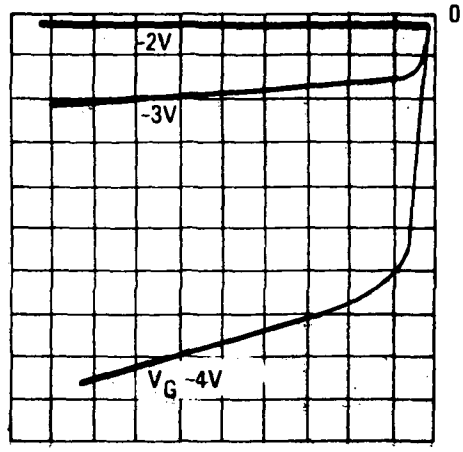
(a)



$V_{field\ plate} = 18V$

(a)

Fig. I.14

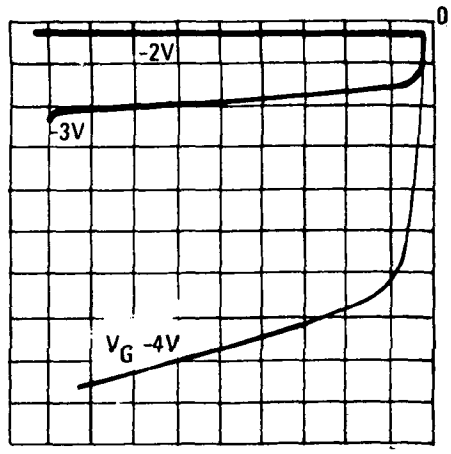


(a)

Drain current = 0.1mA/ vert. div.

Drain voltage = 2V/hor.div

$V_{field\ plate}$ = 0V



(a)

$V_{field\ plate}$ = 18V

Fig. I.15

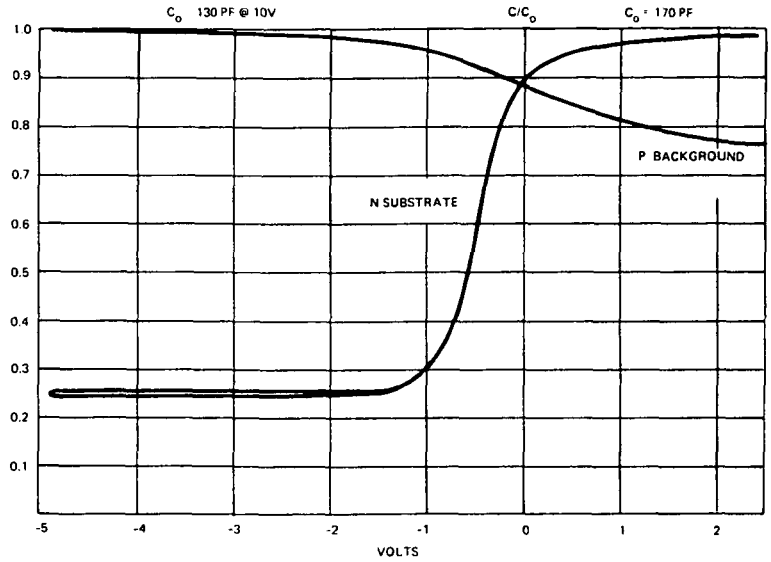

C_o 130 PF @ 10V
C/C_o
C_o = 170 PF
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
P BACKGROUND
N SUBSTRATE
-5
-4
-3
-2
-1
0
1
2
VOLTS

Fig. I.16

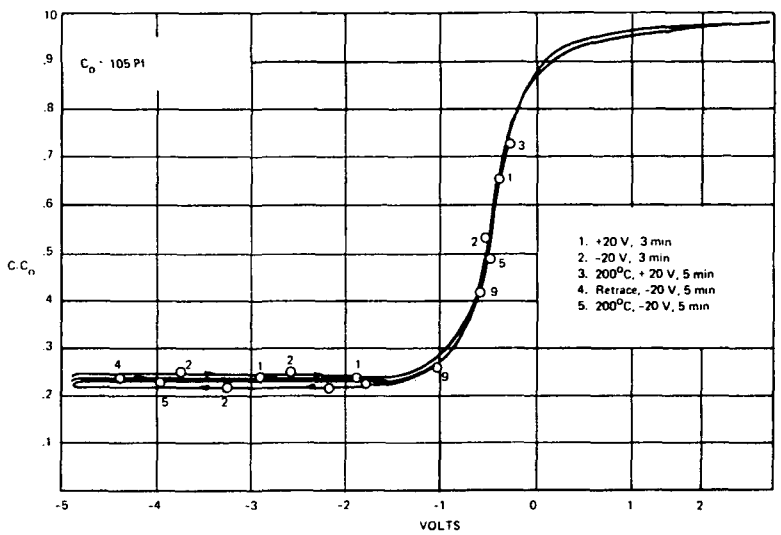

C_o - 105 Pf
C/C$_o$
VOLTS
1. +20 V, 3 min
2. -20 V, 3 min
3. 200°C, + 20 V, 5 min
4. Retrace, -20 V, 5 min
5. 200°C, -20 V, 5 min

Fig. I.17

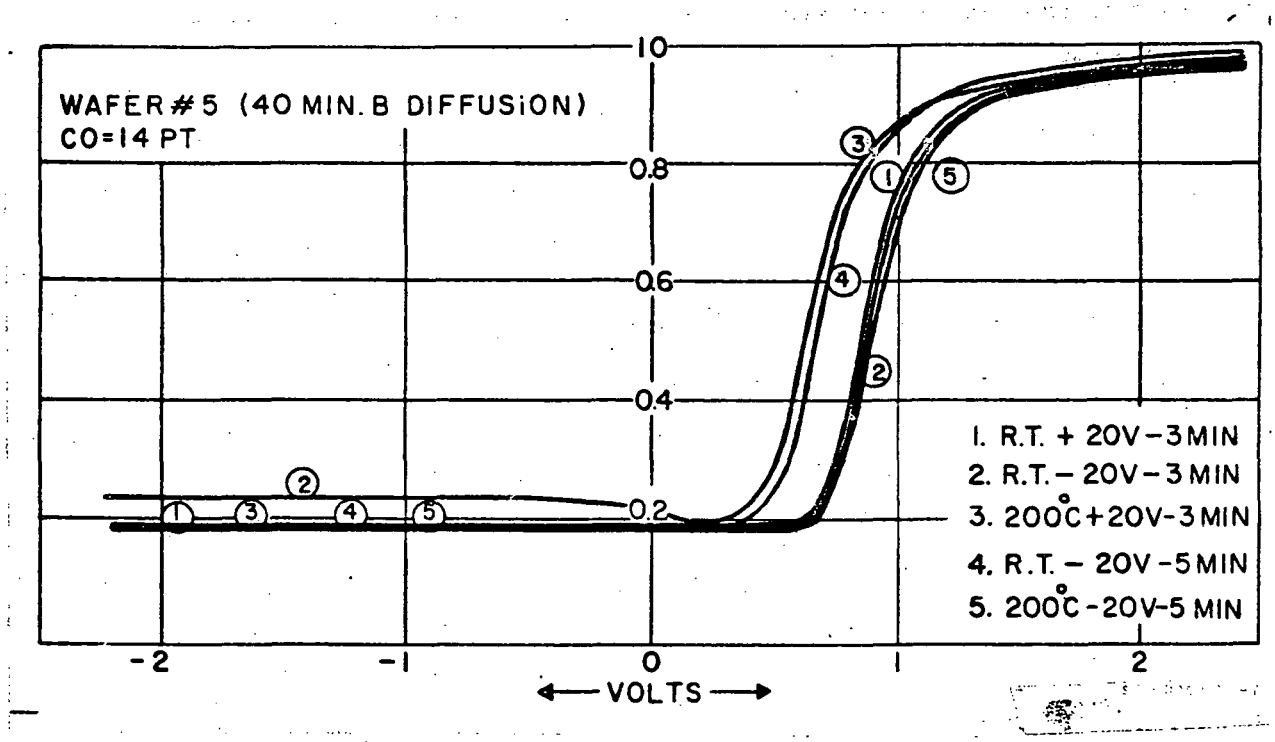
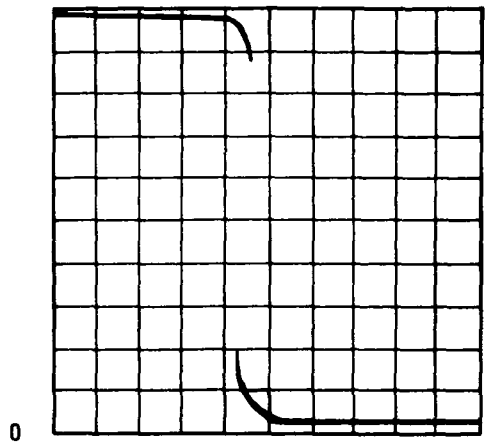
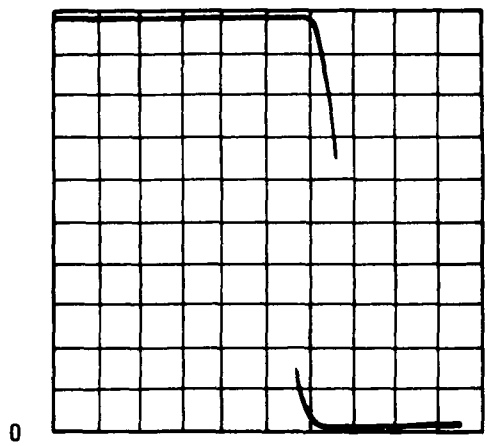

WAFER #5 (40 MIN. B DIFFUSION)
CO=14 PT
1.0
0.8
0.6
0.4
0.2
-2
-1
0
1
2
VOLTS
1. R.T. + 20V-3 MIN
2. R.T. - 20V-3 MIN
3. 200°C+20V-3 MIN
4. R.T. - 20V-5 MIN
5. 200°C-20V-5 MIN

Fig. I.18



(a)



(b)

Fig. I.19

SKETCH SHEET
Form BA 5635

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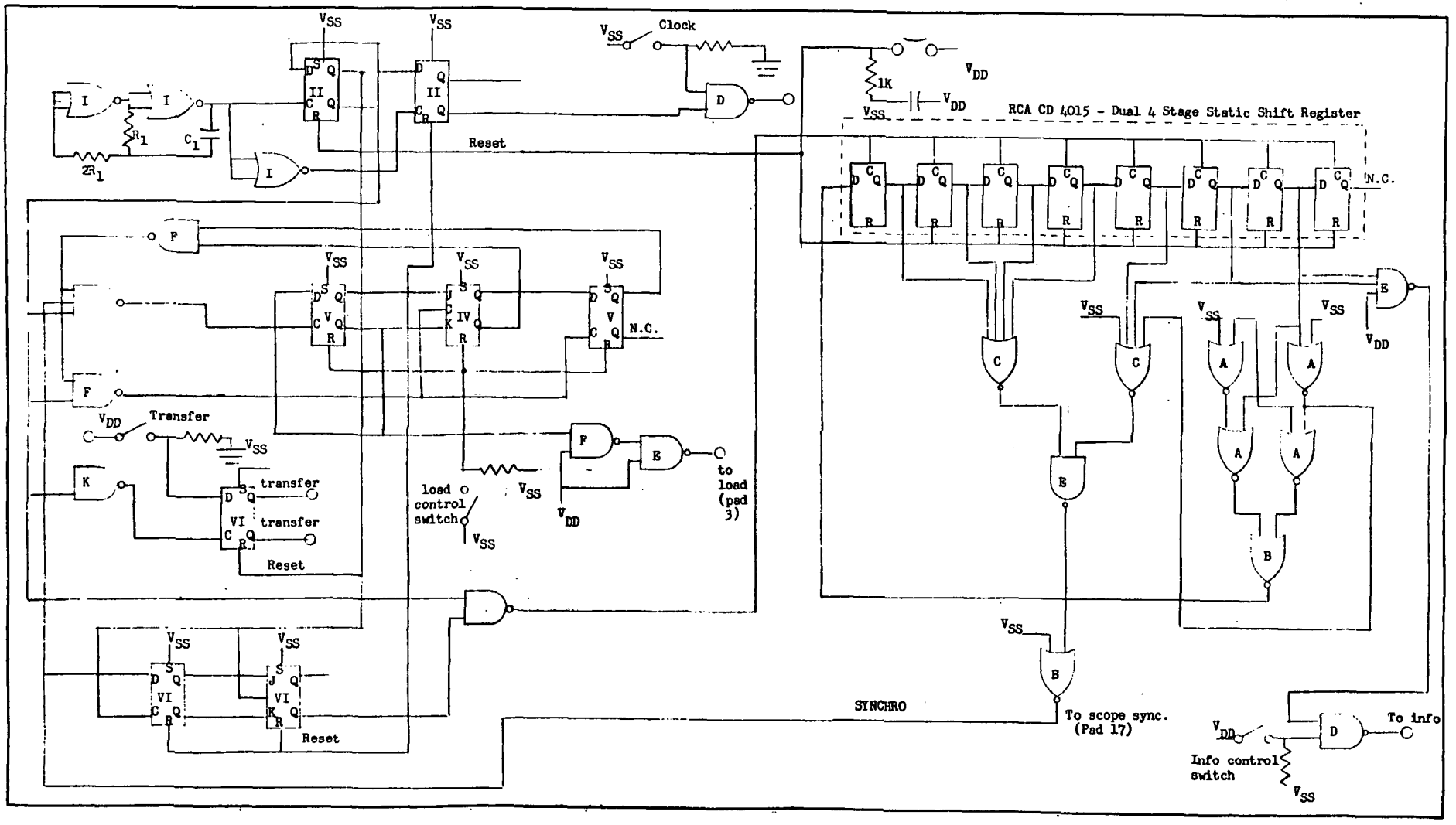


Figure I.20

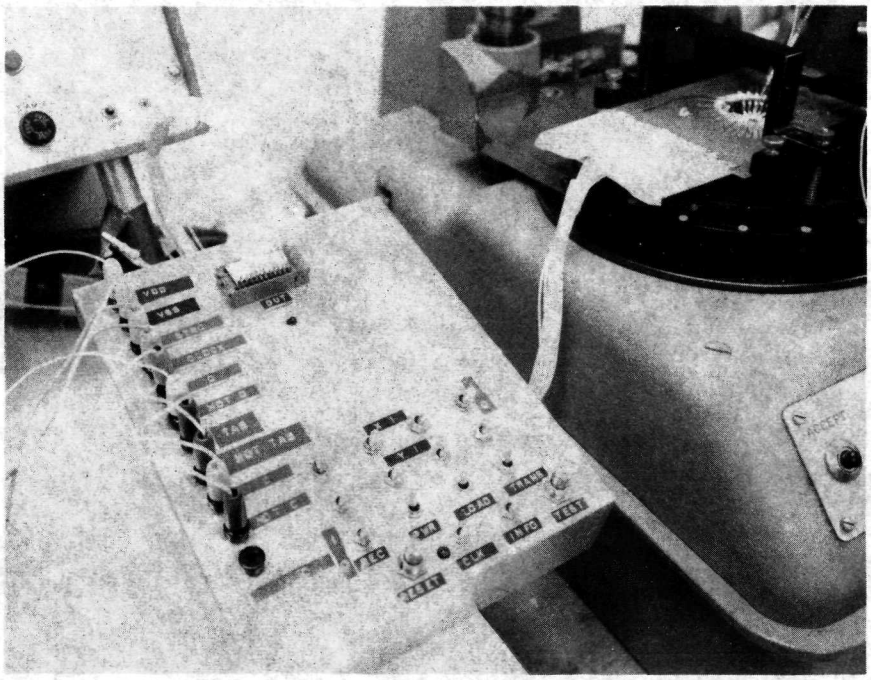
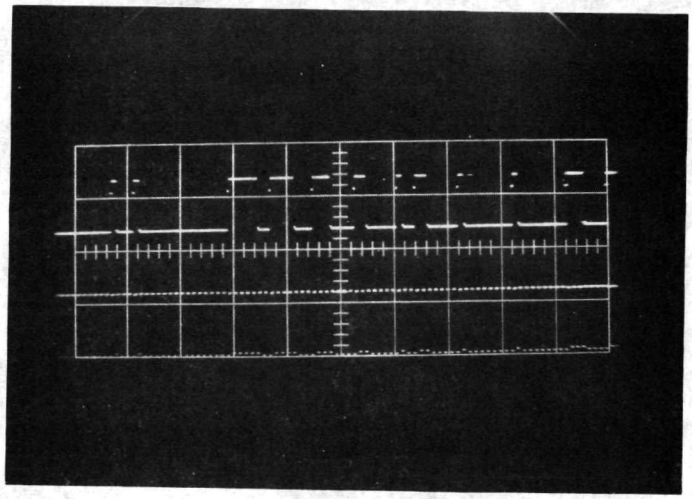
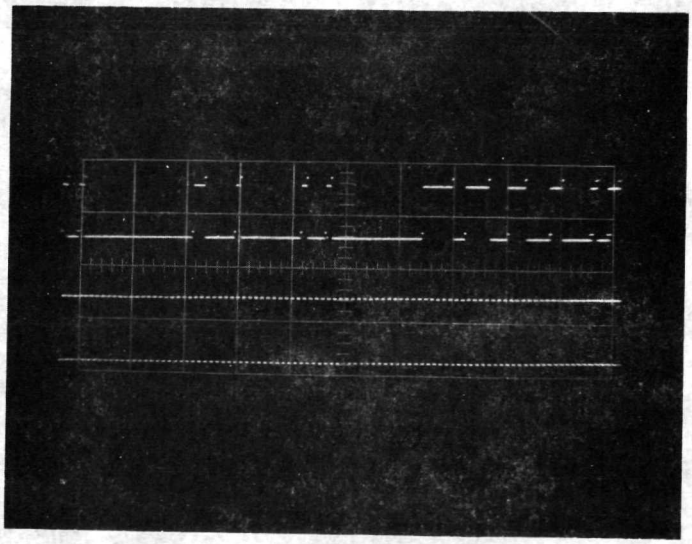


Fig. I.21



(a)



(b)

Fig. I.22

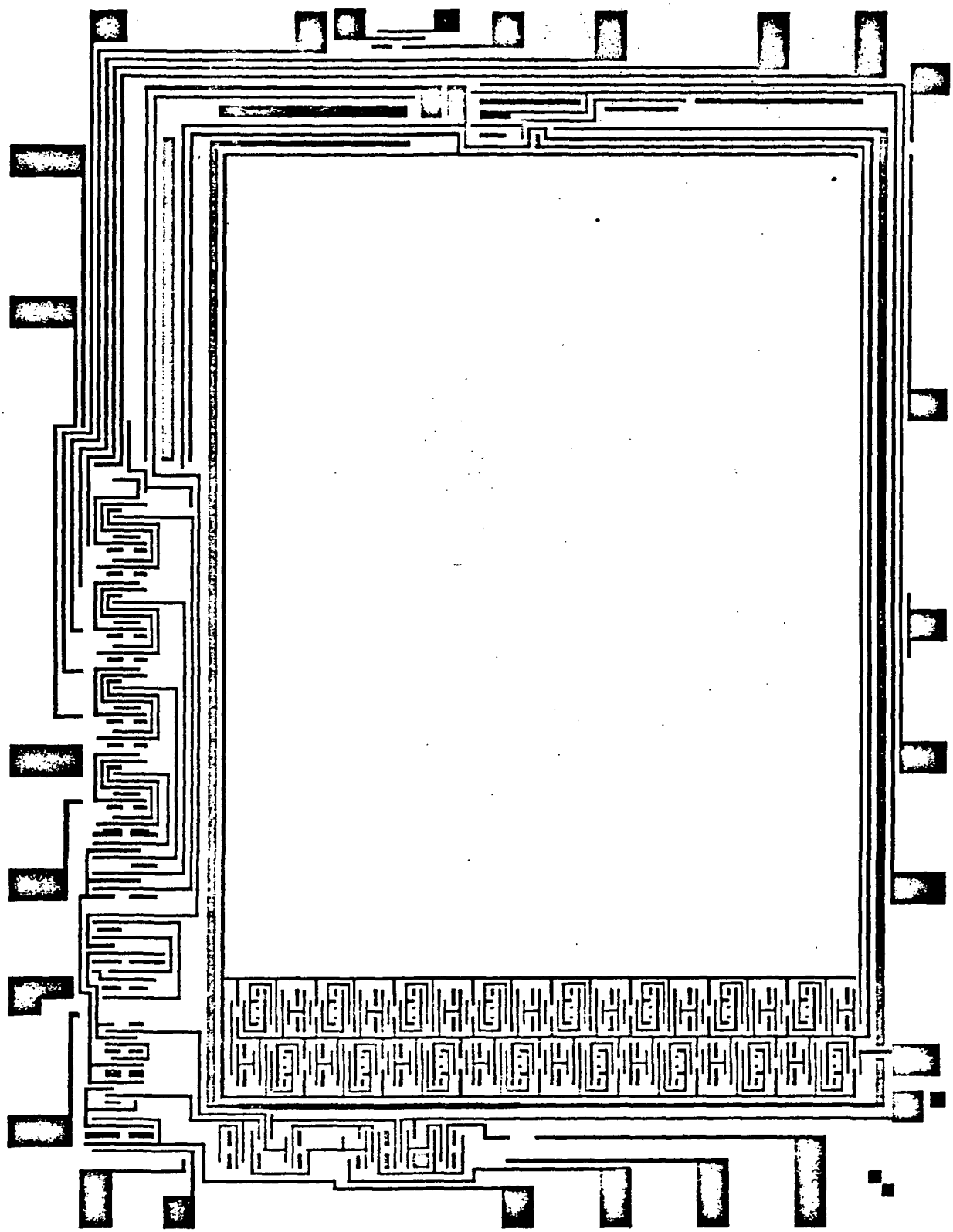


Figure I.23

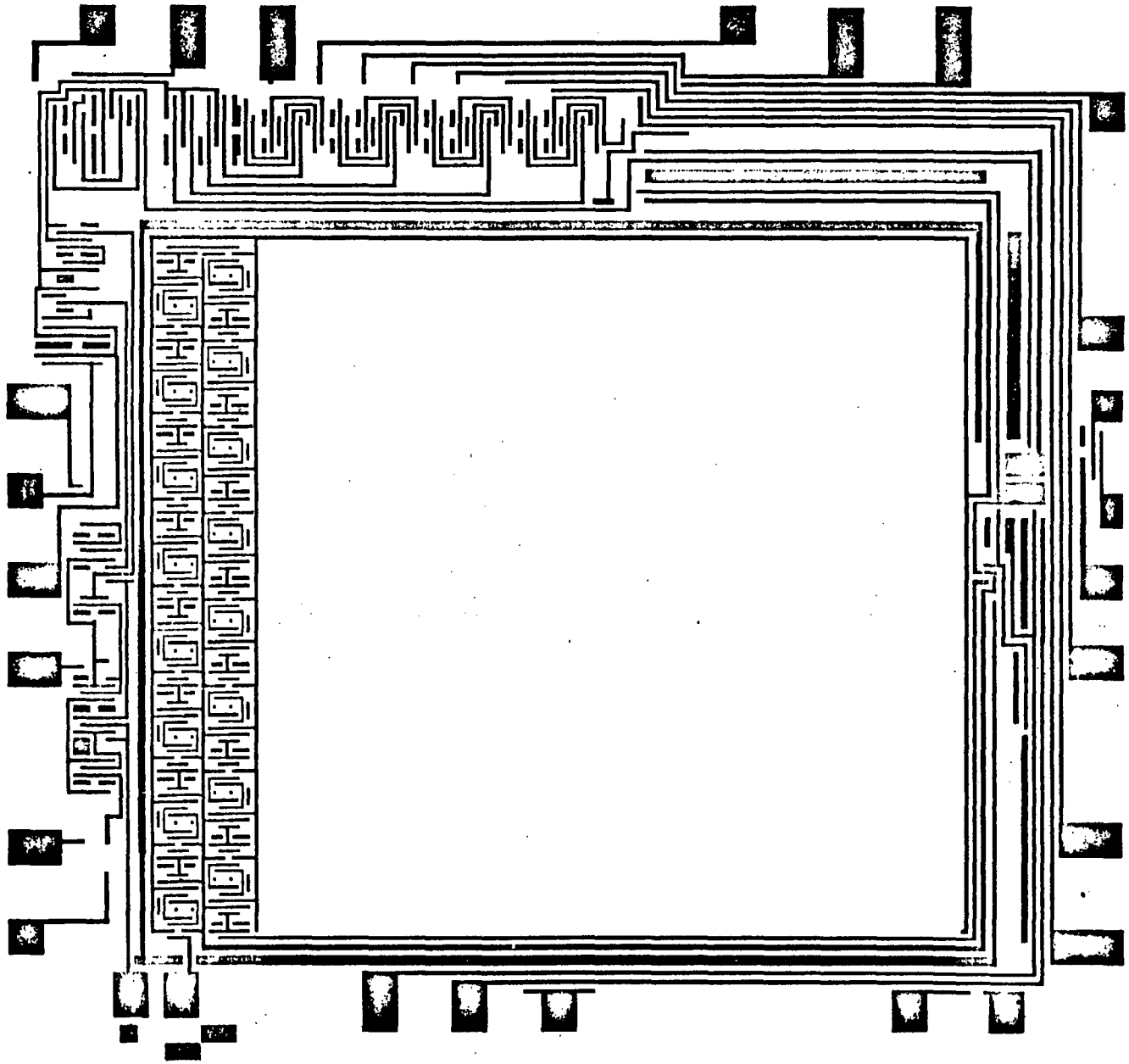


Figure I.24

Part II: Shielded Double-Diffused MOS Inverter

Introduction:

In the realm of semiconductor active devices, field effect transistors have generally been considered as inferior to the bipolar transistor in high frequency response. In the state-of-the-art FET's, the channel length L is much larger than the base-width W_b of bipolar transistor , because the lateral L dimension is determined by photolithographical techniques, while W_b is controlled by diffusion techniques. In practice, W_b can be well controlled in the fractional micron range while L can only be controlled to one order of magnitude higher. Since the gain-bandwidth product has a reciprocal square-law dependence on these dimensions, the net results is that bipolar transistors are faster than field effect transistors.

A narrow channel length can be achieved by double diffusion like the conventional bipolar transistor.[1,2] In addition to transistors, simple integrated switching circuits having double-diffused switching MOS transistors, and depletion mode load device were fabricated to achieve higher speed, smaller size and lower power dissipation than conventional MOS integrated circuits.

Integrated Double-Diffused MOS Structure

An integrated double-diffused n-channel MOS structure is shown in Figure II.1 The substrate can be either p-type or n-type. The window defining the source regions is diffused with both n-type dopant and a lower-concentration p-type dopant. The window defining the drain region is diffused with an n-type dopant as in conventional transistors. With double diffusion, the channel length is of p-type region and can be made very narrow,

less than 1μm. At the same time, the p-type doping is more concentrated toward the source, and thus reduces the punch-through effect.

The structure shown in Figure II.1 can be either depletion mode or enhancement mode. It is merely a matter of choice of a p-type diffused layer concentration and substrate crystal orientation. A depletion mode device requires a low concentration p-background and a high surface state density, i.e. ⟨1,1,1⟩ oriented crystals. An enhancement mode device requires either a moderate concentration background or a low surface state density. A surface concentration of the order of 10^{16} atoms/cm^3 on a low surface state ⟨1,0,0⟩ oriented crystal is appropriate for an enhancement mode device. Alternatively, a high p-type surface concentration in the low 10^{17} atoms/cm^3 range and a high surface state density ⟨1,1,1⟩ crystal orientation can also be used for an enhancement mode device.

It has been pointed out[2] that it is desirable to use a depletion mode load device and an enhancement mode active transistor in switching circuits to reduce the power dissipation and to increase the switching speed. With double-diffused structures, it becomes feasible to integrate this kind of switching circuit. An integrated inverter can be fabricated in a π-type or low concentration p-type substrate. The depletion mode load device can be obtained by eliminating the p-type diffusion used for the active device as shown in Figure II.2. For such a structure, a p-type diffusion should also be applied to all the inactive areas to obtain isolation.

In addition to double-diffusion, it is desirable to incorporate self-aligned gates for high speed, planar surface for ease of interconnection in an integrated circuit and electrostatic shield for preventing surface inversion. All these featured were incorporated in a shielded structure developed in the previous contract with NASA.[3]

Computer Analysis of Double-Diffused MOS Transistor

Due to the non-uniformity of the background concentration, the characteristics of such a device are not as obvious as a conventional MOS transistor. Computer analysis has been used to find out these characteristics. When the grading of the background is accomplished by a double-diffused structure as shown in Figure II.1 the impurity concentration distribution N(x) in the channel background can be approximated as an exponential function. (see appendix)

$$N(x) = N_e(N_b/N_e)^{(x/x_b)} + N_b \qquad (1)$$

where N_e is the concentration of the channel at the junction, N_b is the π-type concentration and x_b is the junction depth.

The threshold voltage is a function of x, the distance from the edge of the source, and is given as

$$V_T(x) = \phi_{GS} - \frac{qN_{ss}}{c_{ox}} + 2\,\phi_F + \frac{\sqrt{2\epsilon_{si}qN(x)\,|\,2\phi_F + V(x)\,|}}{c_{ox}} \qquad (2)$$

where

ϕ_{GS} = the gate-background work function difference

$$= \frac{kT}{q} \ln \frac{4 \times 10^{20} N(x)}{n_i^2}$$

(for an n-doped Si gate with an assumed effective doping concentration of 4×10^{20} atoms/cm^3)

n_i = intrinsic concentration = 1.5×10^{10} at/cm^3 at 27°C

N_{ss} = surface state density

ϕ_F = Fermi level associated with a given doping concentration

$$= \frac{kT}{q} \ln \frac{N(x)}{n_i}$$

c_{ox} = gate capacitance per unit area

$$= \epsilon_{ox}/t_{ox}$$

ϵ_{ox} = dielectric constant of oxide

$$= 4 \times 8.85 \times 10^{-14} \text{ f/cm}$$

t_{ox} = gate oxide thickness

ϵ_{si} = dielectric constant of silicon

$$= 11.7 \times 8.85 \times 10^{-14} \text{ f/cm}$$

$V(x)$ = the potential of the channel at any point x with respect to the substrate

The drain current I_D can be found by substituting the threshold voltage given in Equation (2) into the relationship

$$I_D = \frac{\mu C_G}{L} \left[V_G - V_T(x) - V(x) \right] \frac{dV(x)}{dx} \qquad (3)$$

The voltage at $x = L$ is the drain voltage V_D.

In this computation, the mobility is assumed to be constant. The carrier velocity saturation effect is not taken into account so that we can have an insight of the effect of a double-diffused structure. The effect of carrier velocity saturation was investigated by Sigg etal[4] and can be incorporated in the computation by modifying the program. If this velocity saturation effect were taken into account, the calculated d-c drain current and the transconductance would be somewhat lower.

The V-I characteristics of the devices have been evaluated for several cases. The flow chart of the program is shown in Figure II.3. Increments of drain current less than the maximum are selected and equation (3) is solved for the resulting values of V(x). A numerical integration is performed to obtain the drain voltage by summing the voltage drops across each increment of x. A maximum current corresponding to the saturated drain current if the channel had no diffused background is used as an upper limit, i.e.

$$I_{max} = \frac{\mu C_G}{2L^2} \left[V_G - V_T (L) \right]^2 \qquad (4)$$

where $V_T(L)$ is the threshold corresponding to the background concentration at $x = L$ without any substrate bias. The different drain currents assumed are different fractions of I_{max}. Figure II.4 shows the computed result of a double-diffused MOS transistor with ⟨1,1,1⟩ crystal orientation and a threshold voltage of 1.0V. The following parameters are used:

$N_{ss} = 2.5 \times 10^{11}$ states/cm^2 for ⟨1,0,0⟩ orientation

$= 10^{12}$ states/cm^2 for ⟨1,1,1⟩ orientation

$t_{ox} = 0.1$ μm

$\mu = 200\ cm^2/V\text{-}sec$

$N_b = 10^{15}\ atoms/cm^3$

Gate Width = 10 μm

Discussion of Computer Results

Effect of Gradient of the Channel: By grading the background impurity concentration of the channel, the effective length of the channel is reduced. Also the low background concentration near the drain reduces the substrate biasing effect. As a result, the d-c current and hence the transconductance are greatly increased. The amount of increase depends on a number of factors which will be discussed in the following paragraphs. Figure II.5 shows the comparison of a graded background and a uniform background.

Note that the percentage increase is greater at low gate voltages. The impurity gradient in the channel causes the threshold to vary with location. Near the source junction the threshold is negative because of compensation, however a short distance from the junction the p diffusion dominates and causes a positive peak in the threshold voltage. Further away from the source region the threshold decreases until the background concentration dominates. The device behaves somewhat as if a number of devices with differing threshold voltages were connected in series with their gates tied to the same potential. A simplified version of this situation is shown in Figure II.6a. Here the transistor which is dominated by the p diffusion (the enhancement-mode device) represents the performance in the p diffused region, while the transistor which is not influenced by the diffusion (the depletion-mode device) represents the remainder of the gate.

(It should be recognized that both devices may, in fact, be depletion-mode devices under some doping conditions, however this only affects absolute voltage levels.) The enhancement-mode device has a relatively high transconductance and saturation current because it has a relatively short channel. However, it requires positive gate voltages in order to be in the operating region. The depletion-mode device, on the other hand has a relatively long channel, and therefore has lower transconductance and saturation currents. However, it conducts fairly heavily even with negative gate voltages. This action can be explained by considering the double-diffused structure as equivalent to two MOS transistors connected in series as shown in Figure II.6b. Q_1 near the source is an enhancement-mode transistor and Q_2 near the drain is a depletion mode transistor. The enhancement mode Q_1 with a short channel length has a higher transconductance than the depletion mode Q_2 which can be taken as a load device for Q_1 in an inverter circuit. The operating points of the inverter can be obtained by plotting the drain characteristics of Q_1 and Q_2 as if they were independent transistors as shown in Figure II.7. When Q_1 is first turned on, say with $V_G = 2V$, the drain current of Q_1 intersects the characteristics of Q_2 at I_2 before the current of Q_2 is saturated. The transconductance is essentially equal to that of Q_1. Further increase in gate voltage to say $V_G = 3V$ makes the currents intersect at I_3 where Q_2 is nearly saturated. Now, the transconductance is essentially equal to that of Q_2 and is less than that for the first gate voltage step. At low gate voltages the enhancement-mode transistor conducts only slightly or may even be cutoff. The depletion-mode transistor is already well into its conducting region. Since the transistors are in series, the depletion-mode transistor is in the triode region and has very little effect

on the net drain current. Drain current and transconductance are determined by the enhancement-mode transistor; transconductance is high because this transistor has a very short channel. At larger gate voltages, however, the enhancement-mode transistor is capable of passing more current than the depletion mode transistor can supply, therefore it moves into the triode region and the performance of the combination is determined by the depletion mode transistor. The result is that the transconductance of the combination is relatively large at lower gate voltages. Note that the two series transistors can maximize the transconductance even without any velocity saturation of the carriers as discussed by Sigg etal.[4] This characteristic contrasts with conventional MOS transistor characteristics, where a uniform background is present and maximum transconductance usually occurs at high gate voltages. For the example illustrated, the saturated d-c current and transconductance of the graded background transistor is larger than the uniform background transistor by an order of magnitude for gate voltages up to 6V. It should be pointed out that the improvement is not so drastic if the background concentration is lower and the substrate biasing effect is less, because the difference in threshold voltage between $V_T(L)$ and $V_T(0)$ is less pronounced, as depicted by Equation (2). This feature suggests that the double-diffused transistor can be operated efficiently at low operating voltages.

Effect of the Diffusion Distance: The diffusion distance may be defined as the distance at which the concentration of the diffused layer is equal to the concentration of the substrate. The shorter this distance, the shorter the low conductance portion of the channel and the higher the transconductance. This effect is clearly demonstrated in Figure 8. Note that

when the diffused distance x_b is shrunk from 1 μm to 0.5 μm, the d-c current at $V_G = 5V$ is increased by 10%. Again the percentage increase is greater at lower gate voltage for the reason given in the previous paragraph. Actually, the case of uniform background can be considered as having a diffused distance $x_b = \infty$, which was the way the computer analysis was done.

Effect of Surface State Densities: The substrate orientation has a marked effect on the surface state densities. The ⟨1,1,1⟩ orientation gives rise to high surface state densities of the order of 10^{12} charges/cm^2, while ⟨1,0,0⟩ orientation gives rise to low surface state densities in the range of 10^{11} charges/cm^2. A high surface state density yields a lower or even negative threshold voltage. For the same threshold voltage of the transistor, high surface state density renders the channel near the drain junction more conductive. Thus, the ⟨1,1,1⟩ orientation gives a higher transconductance than the ⟨1,0,0⟩ orientation. The result of the computation is shown in Figure II.9. However, the background concentration for the same threshold voltage is higher for the ⟨1,1,1⟩ orientation than the ⟨1,0,0⟩ orientation, and the resultant breakdown voltage between the source and the background is lower for the ⟨1,1,1⟩ crystal. As shown in the computation, a concentration of 1.5×10^{17} atoms/cm^3 for ⟨1,1,1⟩ crystals gives approximately the same threshold voltage (1 volt) as a concentration of 3×10^{16} atoms/cm^3 for ⟨1,0,0⟩ crystals. The corresponding breakdown voltages for a junction depth of 2 μm are 12 volts for ⟨1,1,1⟩ crystals and 24 volts for ⟨1,0,0⟩ crystals for the same threshold voltage.

Effect of Gate Length: For a given diffused distance x_b of the channel, a larger gate length increases the distance between the diffusion front and the drain junction and hence the effect of the depletion mode region.

Thus, a shorter gate length increases the saturated current. The computed difference is shown in Figure II.10. The percentage increase is smaller at lower gate voltages, because the enhancement region is dominant.

Thus, geometrically, the transconductance is both a function of the channel length and the diffusion distance. In practice, it is easier to form a shallow junction which is controlled by a diffusion technique than to fabricate a short gate which is controlled by a photo-engraving technique.

For high frequency operation, a longer gate increases the gate capacitance. This capacitance contributes to the Miller feedback capacitance and the input capacitance. For the case shown in Figure II.5, the transconductance g_m at $V_G = 5V$ is 0.25×10^{-3} mhos and the input capacitance $c_{in} = 8.85 \times 10^{-15}$f; the gain-bandwidth product is $g_m/2\pi c_{in} = 4.5$ GHz.

Effect of Substrate Conductivity: The double diffused MOS transistor can be fabricated on either a p-type substrate or an n-type substrate. When a p-type substrate is used, the n-type sources and drains are isolated from one another and hence the transistors are self-isolating. The p-type substrate is therefore desirable for integrated circuits. On the other hand, the n-type substrate has the same conductivity type as the channel, and can hence increase the conductivity of the channel near the drain. It is interesting to find out the quantitative difference in performance of an n-type substrate and a p-type substrate.

When the substrate is n-type, the threshold voltage is reduced, because the p-type diffusion is compensated by the n-type background and becomes less concentrated. The increased conductance of the channel can be represented by an equivalent negative threshold voltage V_p. If the conductance beyond the diffused junction is a rectangular bar of thickness t_s, then the V_p for depleting the electron charge in this section of the channel is equal to:

$$V_p \cong \frac{qN_b t_s}{c_{ox}} \tag{5}$$

For practical devices, the equivalent thickness is of the order of the n+ drain region depth. N_b must be low enough for the diffused p-type channel to convert. If we take $t_s = 2\ \mu m$, $N_b = 10^{15}$ atoms/cm^3 and $c_{ox} = 3.54 \times 10^{-8}$ f/cm^2 (corresponding to an oxide thickness of 1000Å) then $V_p = -1V$. The threshold voltage for the n-type background portion of the channel can now be written as

$$V_{Tn} = \phi_{GS} - \frac{qN_{ss}}{c_{ox}} - 1 \tag{6}$$

for $N_{ss} = 10^{12}$ charges/cm^2, $V_{Tn} = -5.85V$.

On the other hand, when p-type background is used, the threshold voltage at $x = L$ in the absence of any self-bias effect in the depletion layer is given by Equation (5). For a p-type substrate with the same background concentration = 10^{15} atoms/cm^3, the threshold voltage is approximately the same, i.e. -5V Thus, the only effect decreasing the conductance of the channel with a p-type substrate is the extra charge stored in the depletion layer of the reverse-biased junction.

The results of the computation are shown in Figure II.11.

Operation of Depletion Mode Load Device

When a depletion mode load device is used in conjunction with an enhancement mode double diffused MOS transistor to reduce power dissipation and to increase speed,[5] the operation can also be analyzed by a similar computer program. There are two configurations for the depletion mode load device: (a) the common drain configuration with the gate short-circuited to the drain as shown in Figure II.12a, and (b) the common source configuration[6] with the gate short-circuited to the source as shown in Figure II.12b.

For the common drain characteristics the drain current can be computed by substituting V_D as V_G in Equation (a). For the load device, V(x) in Equation (3) should refer to the source which is now a voltage V_{out} relative to the substrate. Thus,

$$V_D = V_{DD} - V_{out} \tag{7}$$

where V_{DD} is the supply voltage.

Equation (3) should now be modified as

$$I_D = \frac{\mu C_G}{L}\left[V_D - V_T(x) - V(x)\right]\frac{dV}{dx} \tag{8}$$

where the threshold voltage $V_T(x)$ is defined as:

$$V_T(x) = \phi_{GS} - \frac{qN_{ss}}{c_{ox}} + 2\,\phi_F + \frac{\sqrt{2\epsilon_{si}\, q\, N(x)\left|2\phi_F + V(x) + V_{out}\right|}}{c_{ox}} \tag{9}$$

The results of the computation are plotted in Figure II.13a as the "b" set of curves with V_{out} as running parameters. When the load device characteristic is superimposed on that of the double-diffused switching transistor as shown in Figure II.14, the logic level can be solved by finding the intersection of curve (a) and curve (b). Note, that the "0" state voltage level is a substantial fraction of the supply voltage V_{DD}. Such a high "0" state logic level is undesirable from the standpoint of noise margin. If the "0" state logic level is to be lowered, either the load device should be made with a longer channel length or the channel of the active transistor should be made wider. Either alternatives results in an enlargement of area.

For the common source configuration, the computation can be performed by setting $V_G = 0$ in Equation (3) and using $V_T(x)$ as defined by Equation (9).

Thus,

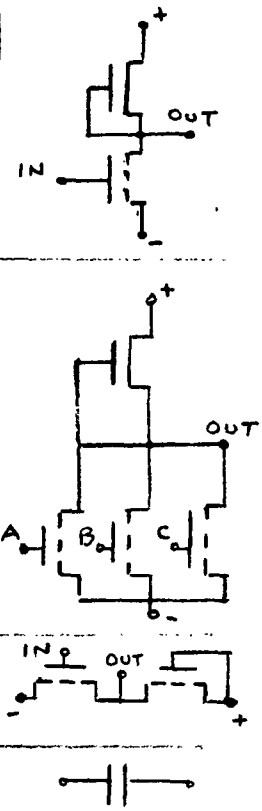
$$I_D = \frac{\mu C_G}{L}\left[- V_T(x) - V(x)\right]\frac{dV}{dx} \qquad (10)$$

The results of the computer analysis is also plotted in Figure II.13 as the set of curves "c" with V_{out} as running parameter. Since the drain current saturates for the common source configuration, the "0" state voltage level, as indicated by the intersection of curve (a) and curve (c) in Figure II.14, is near zero, Thus the logic level is well defined. This fact implies that the load device can be made the same size as the double-diffused active transistor.

Design

An integrated circuit incorporating DMOS transistors was designed for testing the speed and power dissipation. There are seven DMOS test devices on the chip. Devices #1, #2, #3 are inverters of DMOS switching transistors and depletion mode load device with different channel widths. Another inverter (#4) is a conventional inverter with enhancement mode load device. Device #5 is a 3-input NOR gate using the depletion mode load device and enhancement mode input DMOS transistors. Device #6 is another 3-input NOR gate with aluminum as one of the input gates. Device #7 is a silicon gate capacitor for C-V measurement. The dimensions of these devices are listed in Table 1.

Name	Switching Device		Load Device			Gate Configuration
	L	W/L	L	W/L	Mode	
1. Inverter A	7μ	60	7μ	60	D	Poly Si
2. Inverter B	5μ	60	5μ	60	D	"
3. Inverter C	3μ	70	3μ	70	D	"
4. 3-Input NOR	(a)5μ	34	5μ	34	D	"
	(b)5μ	34	5μ	34	D	"
	(c)5μ	34	5μ	34	D	"
5. 3-Input NOR	(a)5μ	34	5μ	34	D	"
	(b)5μ	34	5μ	34	D	"
	(c)5μ	34	5μ	34	D	Al
6. Inverter (Conventional)	5μ	104	5μ	14	E	Poly Si
7. Capacitor	590μ x 80μ					



The masks for the different levels are shown in Figure II.15.

Mask #1 P-isolation diffusion

Mask #2 Source-drain diffusion

Mask #3 P channel enhancement diffusion

Mask #4 Polycrystalline Si gate and shield separation etch

Mask #5 Contact

Mask #6 Al interconnection delineation

Figure II.15g shows the terminals labeled for the different devices.

Processing

The original substrate is π-type silicon. The low acceptor concentration of the π-type silicon together with the surface state charges at the Si - SiO_2 interface creates an inversion layer suitable for producing depletion mode devices. However, means should be provided to isolate the inversion layers and to prevent cross-talk. This can be accomplished by introducing a p-type isolation diffusion. This p-type concentration should not be too high, as premature breakdowns may result when coming into contact with subsequent n + source and drain diffusions. To further insure against inversion, the silicon shield is incorporated.

The fabrication steps are shown in Figure II.16. After first masking, p-type isolation regions are first selectively diffused into a π-type substrate (Figure II.16a). The masking oxide is removed. The substrate is next deposited with a thin layer of gate oxide (say, 1K Å), followed by a layer of polycrystalline silicon gate (say, 5K Å) and then a layer of silicon nitride (Figure II.16b).

In the second masking step, windows for the outlines of source and drain are opened through the $Si_3 N_4$ and poly Si layers (Figure II.16b). In the third masking step the mask for the source window is opened through the gate oxide. This mask is made slightly larger than the window of the first mask to insure alignment of the double-diffusions of the source. During photoetching, the Si_3N_4 prevents the polycrystalline layer from being exposed.

With the source window opened, p-type dopant is diffused into the substrate as shown in Figure II.16c. During the drive-in diffusion, the exposed polycrystalline silicon becomes oxidized. After the drive-in diffusion, all the oxide on top of the polycrystalline silicon and that covering the drain region is removed and n+type dopant is diffused into the source and drain regions as shown in Figure II.16b.

After the fourth masking, the polycrystalline silicon is selectively etched to isolate the gate leaving the rest of the polycrystalline silicon to serve as an electrostatic shield. Then another layer of glass is grown over the structure. In the fifth masking step, contact windows are opened. After aluminum evaporation and sintering the last masking step is applied to delineate the interconnection.

The structure thus fabricated is graded in resistivity to prevent punch-through and has a very narrow channel length to increase the frequency response. The contacts are on the top to permit a planar integrated circuit structure. The polycrystalline shield will prevent the creation of inversion layers in the isolation regions.

During the process development for this phase, the lower temperature polysilicon process was incorporated. The same problems described in the section on the shielded shift register was encountered. However, the redistribution cycle of the second boron diffusion, about 3 hours, affected the poly layer even more. If an oxidizing atmosphere was used, the poly layer was completely oxidized. On the other hand, if a nonoxidizing nitrogen atmosphere was used, the layer became almost impossible to acid etch. Fortunately, the solution to the shielded shift register problems were effective when applied to this structure. By covering the poly layer with successive layers of nitride and oxide, the layer was shielded from the effects of oxygen and nitrogen at high temperatures. In addition, the phosphorus doping of the poly layer was not performed until after the last polysilicon etching step was completed. As with the shift register, the plasma etching technique was utilized and undercutting was minimized to an acceptable degree.

Experimental Results

The processing steps of the double diffused MOS are as follows:

1) Substrate: ⟨111⟩, p type 10 to 30Ω cm.

2) Thermal Oxidation: 5000Å thick.

3) Photoengraving for P+ guard ring.

4) p+ boron diffusion: 100Ω/sq, 5μm.

5) Oxide Removal

6) Gate dielectric: 800Å, SiO_2 plus 400Å silicon nitride.

7) Vapor growth of polycrystalline silicon by decomposition of silane: 3000Å.

8) Diffusion Mask Growth: 1000Å silicon nitride plus 500Å silicon dioxide.

9) Photoengraving for n+ source and drain windows through top oxide.

10) Photoengraving for p+ source window to substrate.

11) p+ boron diffusion: 125Ω/sq, 3μm

12) Plasma etch of polycrystalline silicon from drain windows and then removal oxide from both source and drain windows.

13) n+ phosphorus diffusion: 10Ω/sq., 1μm.

14) Photoengraving of contact windows.

15) Aluminization: 7000Å.

16) Photoengraving of interconnect pattern.

17) Sintering.

The experimental self-aligned silicon gate DMOS integrated inverter is shown in Figure II.17. The DMOS transistor Q_1 has a length of 7μm and a width of 420μm. The depletion mode load device Q_2 has the same dimensions.. In DMOS integrated circuits, it is possible to design both

devices to have the same dimension (ratio less) because of the higher conductance of the depletion-mode load device. This ratioless feature allows for higher density.

The VI characteristics of the DMOS transistor and the load device are shown in Figure II.18a and II.18b. Note that the transconductance of the DMOS transistor at 5mA of drain current and 8V of drain voltage is greater than 3mmho. From a theoretical standpoint, the maximum achievable transconductance = $WC v_s$.

where W = channel width = 420×10^{-4}cm.

C = gate capacitance per unit area.
= dielectric constant of oxide/gate oxide thickness.
= 3.4×10^{-13}(F/cm)/0.15×10^{-4} (cm)

v_S = scattering limited velocity = 6×10^{6}cm/s

The theoretical g_m max using our parameters should be about 5mmhos. Thus our result is approaching the theoretical value.

Note also that the drain current for the load device is 15mA which is larger than the drain current of the DMOS transistor turned on with more than 4V of gate bias.

Similar DMOS inverters with channel length of 5μm and similar width/length ratio were also fabricated. The results are comparable.

Summary

The effective length of an MOS transistor can be made narrow by using double-diffusion similar to a bipolar transistor. Computations were conducted for n-channel double diffused transistor with different surface concentrations, channel lengths, channel gradients, surface state densities and substrate concentrations. A shorter channel length and a higher surface state density, e.g. ⟨1,1,1⟩ crystal, gave a higher drain current and trans-

conductance. The maximum transconductance in many cases occurs at low gate voltages. The computations indicate that a gain-bandwidth product in the gigahertz range can be expected when the graded channel region is less than 1μm. The difference in n-type substrate and p-type substrate is not substantial.

The analysis is also useful in predicting the performance of any integrated logic circuit using the diffused enhancement transistor as the active switch and a depletion mode transistor (without a diffused channel) as the load device. The computation indicates that satisfactory performance can be obtained using a load device with the same geometry and an ON voltage of only a fraction of a volt. This revelation indicates that double-diffused channel MOS transistors not only give higher speed but also smaller chip-area for integrated circuits and a lower supply voltage (hence less power dissipation).

Experimental shielded DMOS integrated inverters were designed and fabricated. New process techniques were developed to achieve self-aligned gate, enhancement-mode DMOS switching transistor and depletion mode load device in an integrated structure. The performances of these DMOS transistors and inverters show high transconductance and speed as expected.

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3. H. C. Lin, J. L. Halsor, P. J. Hayes, "Shielded Silicon Gate Complementary MOS Integrated Circuit," IEEE Trans. Electron Devices, ED-19, pp. 1109-1207, Nov. 1972.

4. H. G. Sigg, G. D. Vendelin, T. P. Cauge, and J. Kocsis, "D-MOS Transistor for Microwave Applications," IEEE Trans. Electron Devices, vol. ED-19, pp. 45-54, Jan. 1972.

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6. Y. Tarui, Y. Hayashi, and T. Sekigawa, "Diffusion self aligned Enhancement-Depletion MOS-IC," in Proc. 2nd Conf. Solid State Devices, supplement to J. Japan Soc. Appl. Phys., vol. 40, pp. 193-198, 1971.

List of Figures

Appendix

Impurity Concentration Distribution of Double-Diffused Channel

The impurity concentration of a diffused layer driven in from a plane source as shown in Figure II.1 can be approximated* as a gaussian function. Thus the acceptor concentration at any point x can be expressed as

$$N(x) = N_o \exp\left[-\frac{(x + x_e)^2}{4Dt}\right] \qquad \text{(i)}$$

where x_e is the lateral distance of the n + source diffusion, N_o is the surface concentration at the source, D is the diffusivity and t is the diffusion time.

At the source channel junction, the acceptor concentration N_e is

$$N_e = N_o \exp\left(-\frac{x_e^2}{4Dt}\right) \qquad \text{(ii)}$$

Similarly the acceptor concentration at x_b is

$$N_b = N_o \exp\left[-\frac{(x_e + x_b)^2}{4Dt}\right] \qquad \text{(iii)}$$

Dividing Equation (iii) by Equation (ii)

$$4\,Dt = \frac{2x_b x_e + x_b^2}{\ln\,(N_e/N_b)} \qquad \text{(iv)}$$

*Strictly speaking, the lateral diffusion has a complementary error function profile because the source is long in comparison with the diffused distance.

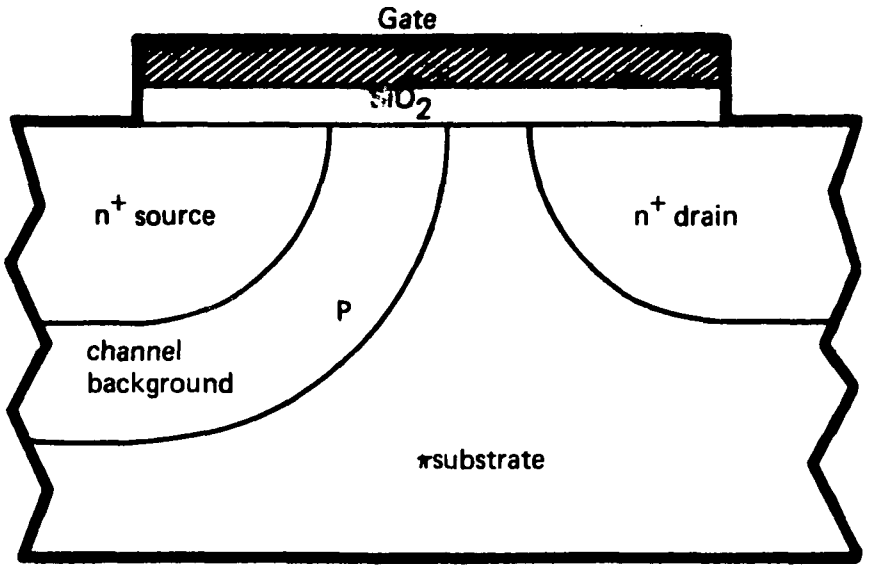
Dividing Equation (i) by Equation (ii) and substituting Equation (iv) into the quotient, one obtains

$$\frac{N(x)}{N_e} = \left(\frac{N_b}{N_e}\right) (x^2 + 2xx_e)/x_b^2 + 2x_b x_e) \qquad (v)$$

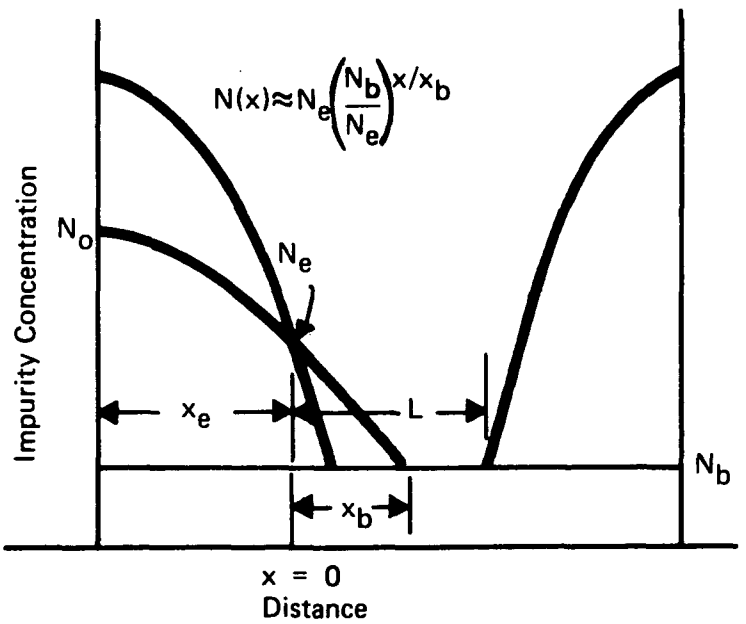
When $2x_e \gg x_b$ as is usually the case, the square terms in the exponent become insignificant and equation (v) can be approximated as

$$\frac{N(x)}{N_e} \cong \left(\frac{N_b}{N_e}\right)^{x/x_b} \qquad (vi)$$

Equation (vi) indicates that the impurity concentration of the channel background can be approximated by an exponential function and is not dependent on the source junction depth to a first degree of approximation.



(a)



(b)

Fig. II.1

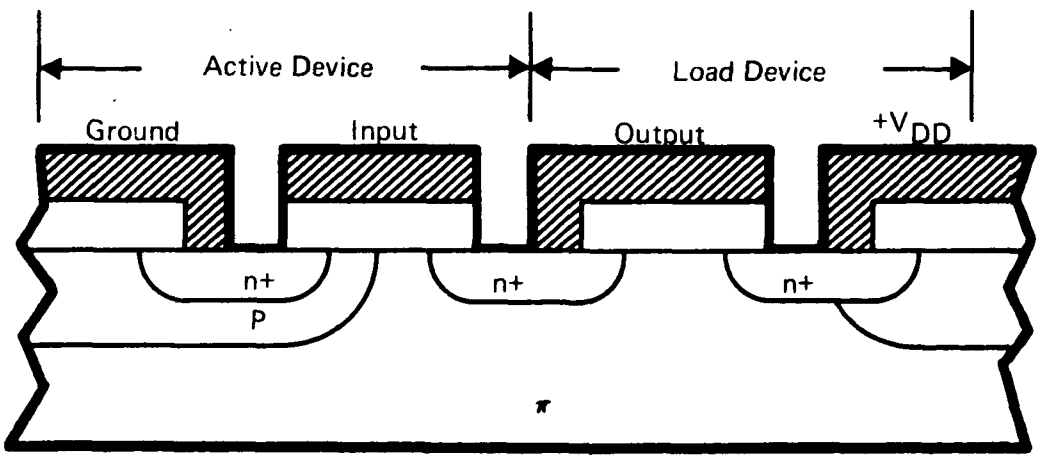


Fig. II.2

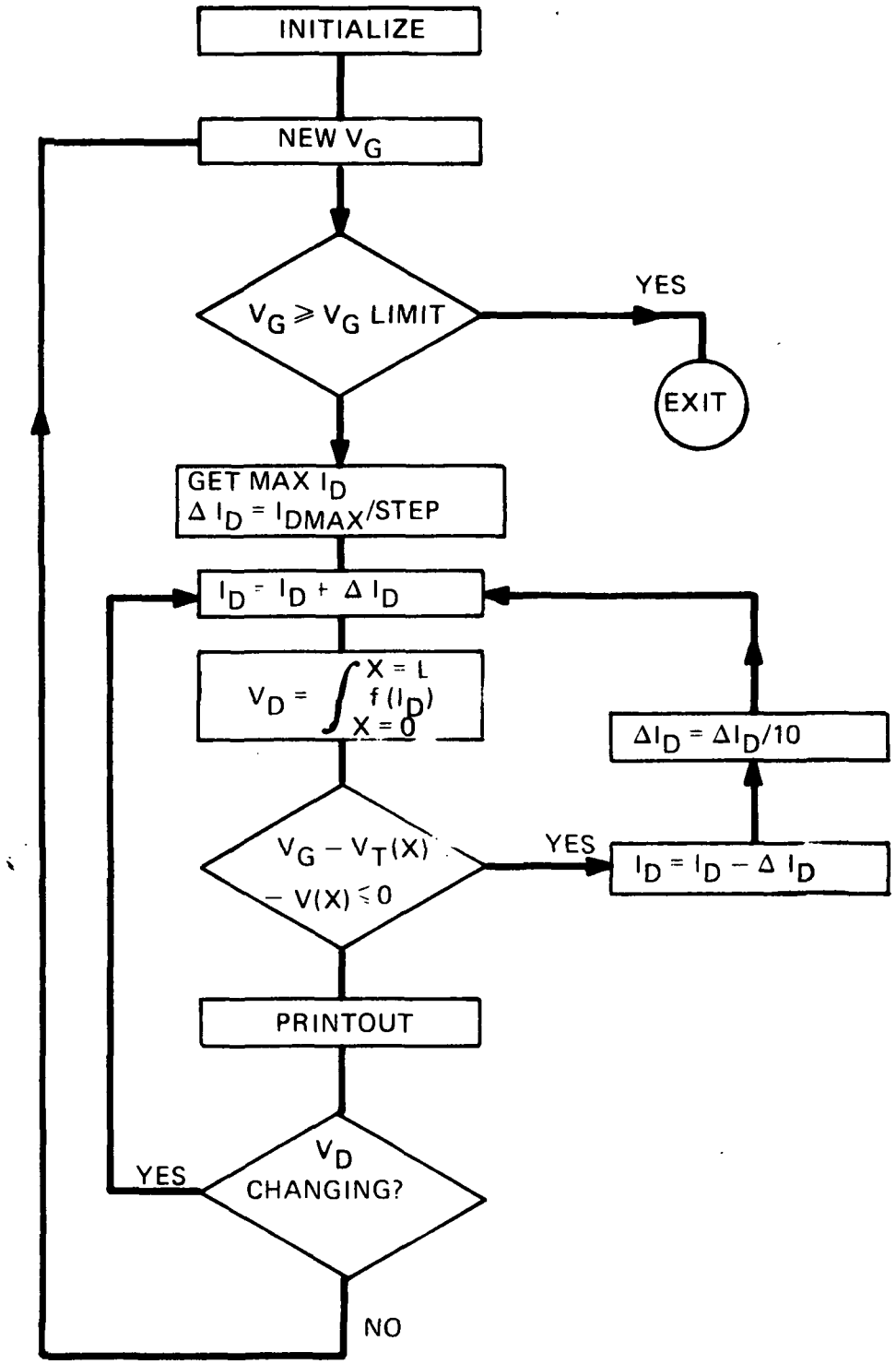

INITIALIZE
NEW V_G
$V_G \geq V_{G\ LIMIT}$
YES
EXIT
GET MAX I_D
$\Delta I_D = I_{DMAX}/STEP$
$I_D = I_D + \Delta I_D$
$V_D = \int_{X=0}^{X=L} f(I_D)$
$\Delta I_D = \Delta I_D/10$
$V_G - V_T(X) - V(X) \leq 0$
YES
$I_D = I_D - \Delta I_D$
PRINTOUT
V_D CHANGING?
YES
NO

Fig. II.3

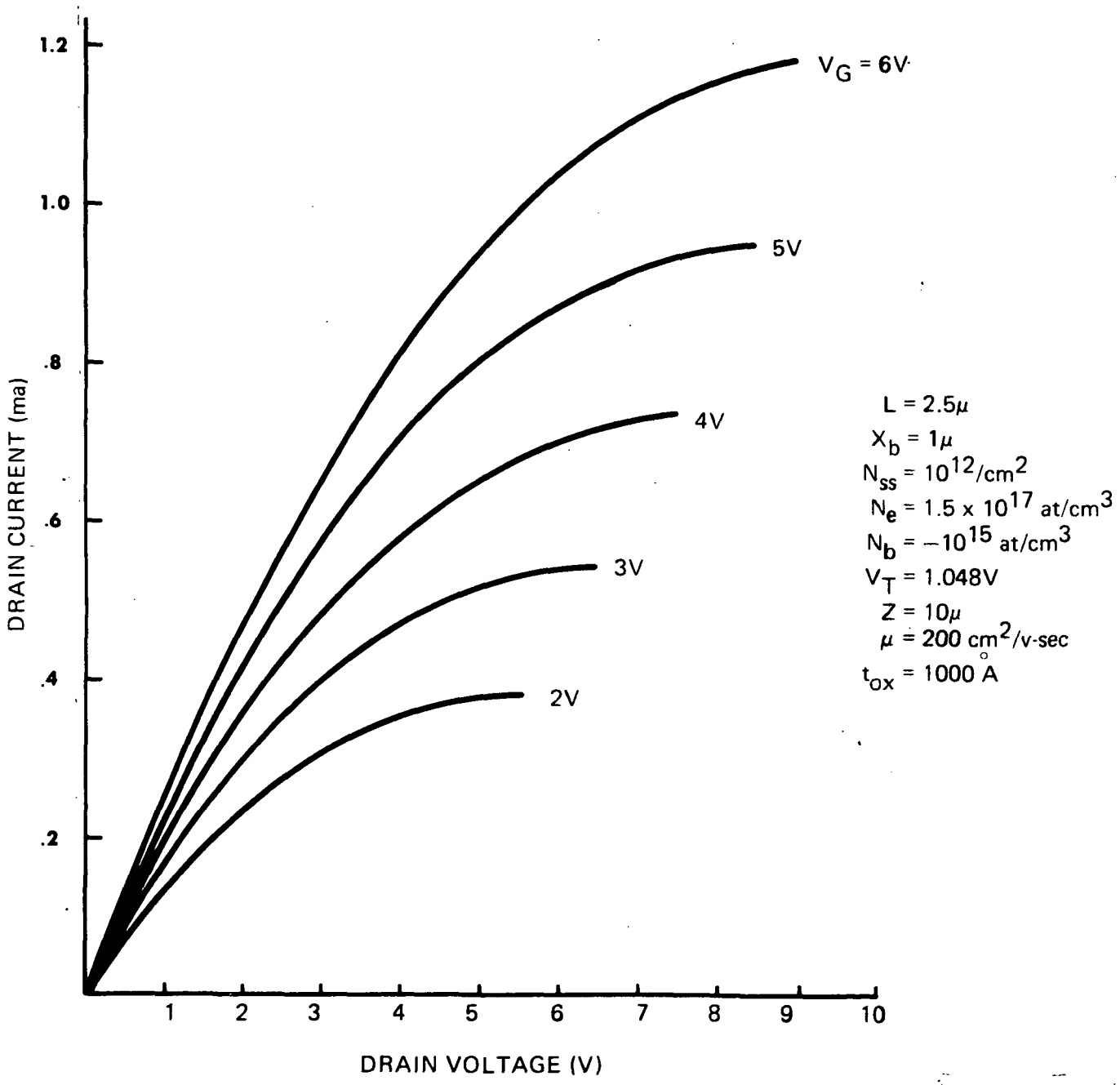

1.2
1.0
.8
.6
.4
.2
DRAIN CURRENT (ma)
V_G = 6V
5V
4V
3V
2V
L = 2.5μ
X_b = 1μ
N_{ss} = 10^{12}/cm^2
N_e = 1.5 x 10^{17} at/cm^3
N_b = -10^{15} at/cm^3
V_T = 1.048V
Z = 10μ
μ = 200 cm^2/v-sec
t_{ox} = 1000 Å
1
2
3
4
5
6
7
8
9
10
DRAIN VOLTAGE (V)

Fig. II.4

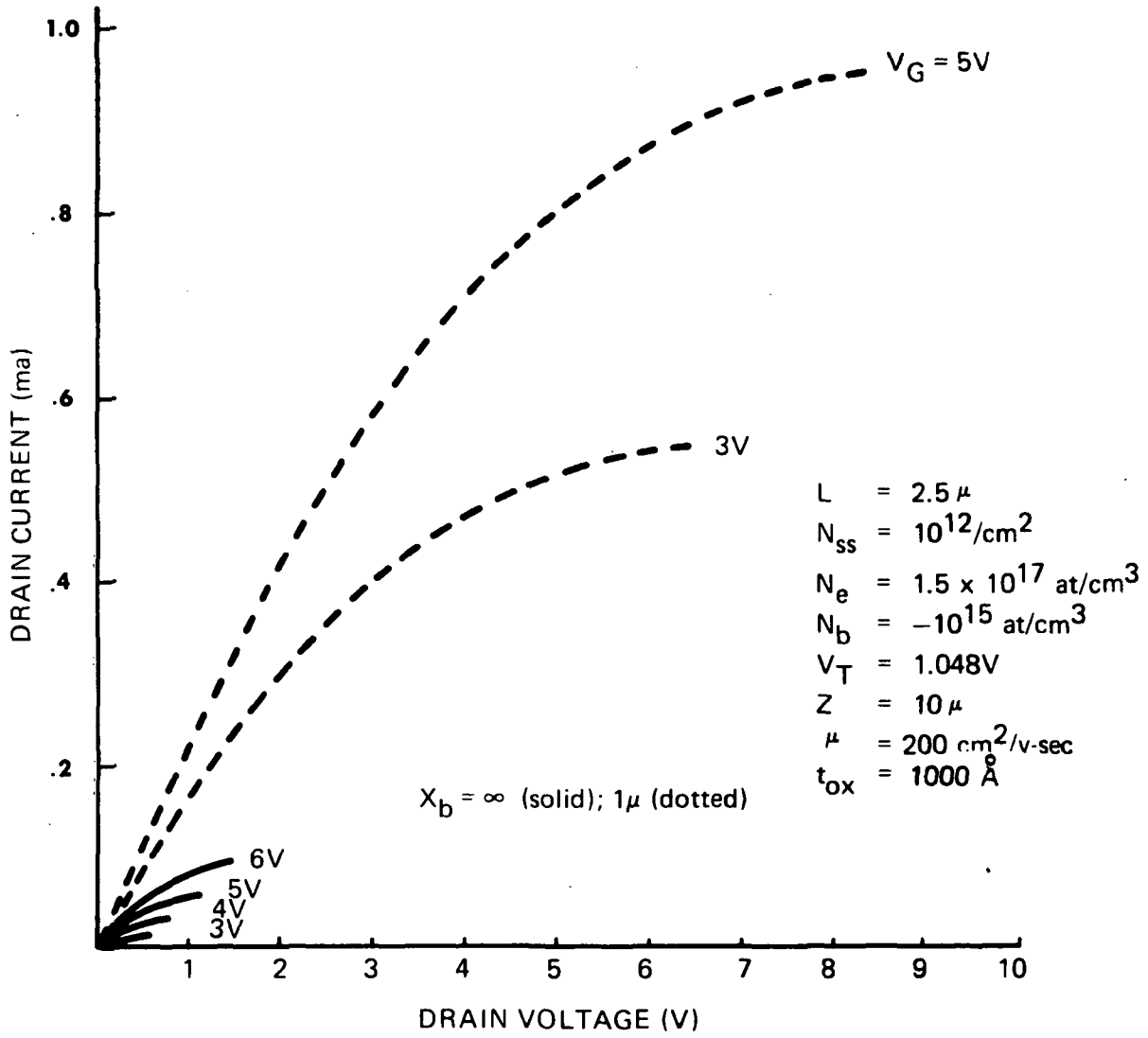

1.0
.8
.6
.4
.2
DRAIN CURRENT (ma)
V_G = 5V
3V
L = 2.5 μ
N_{ss} = 10^{12}/cm^2
N_e = 1.5 x 10^{17} at/cm^3
N_b = -10^{15} at/cm^3
V_T = 1.048V
Z = 10 μ
μ = 200 cm^2/v-sec
t_{ox} = 1000 Å
X_b = ∞ (solid); 1μ (dotted)
6V
5V
4V
3V
1
2
3
4
5
6
7
8
9
10
DRAIN VOLTAGE (V)

Fig. II.5

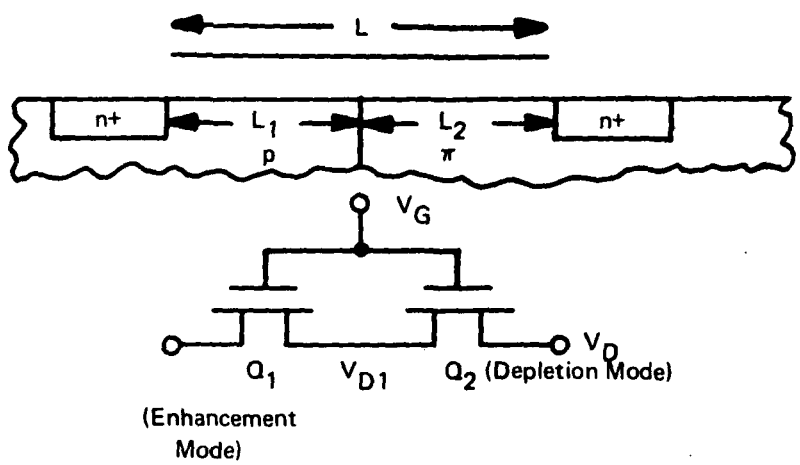


Fig. II.6

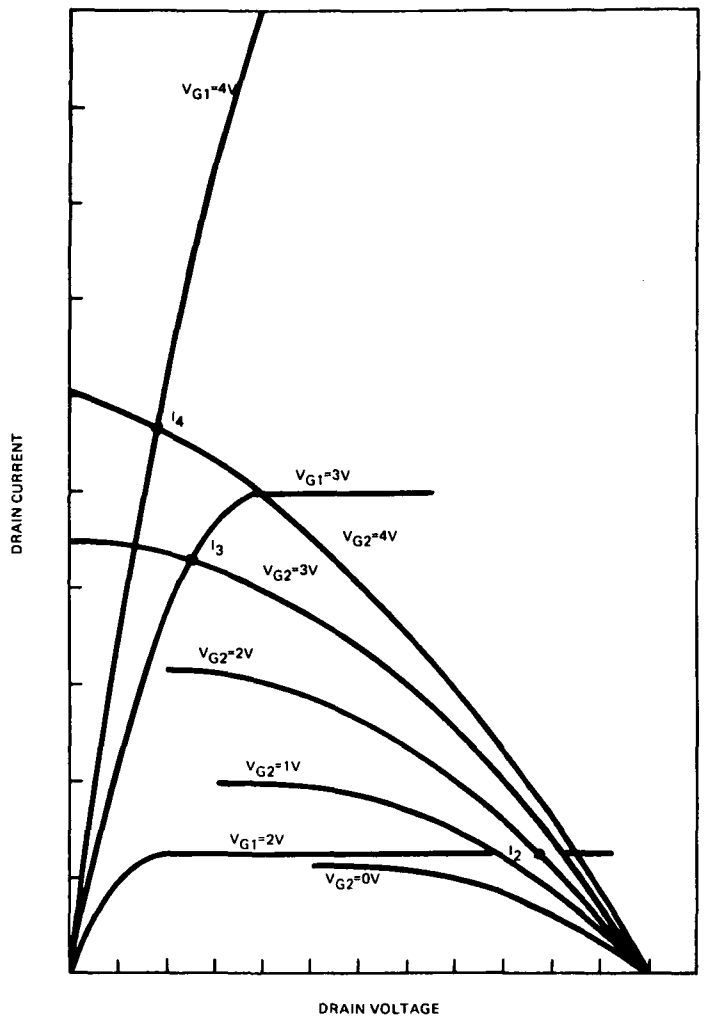

V_{G1}=4V
I_4
V_{G1}=3V
V_{G2}=4V
I_3
V_{G2}=3V
V_{G2}=2V
V_{G2}=1V
V_{G1}=2V
I_2
V_{G2}=0V
DRAIN CURRENT
DRAIN VOLTAGE

Fig. II.7

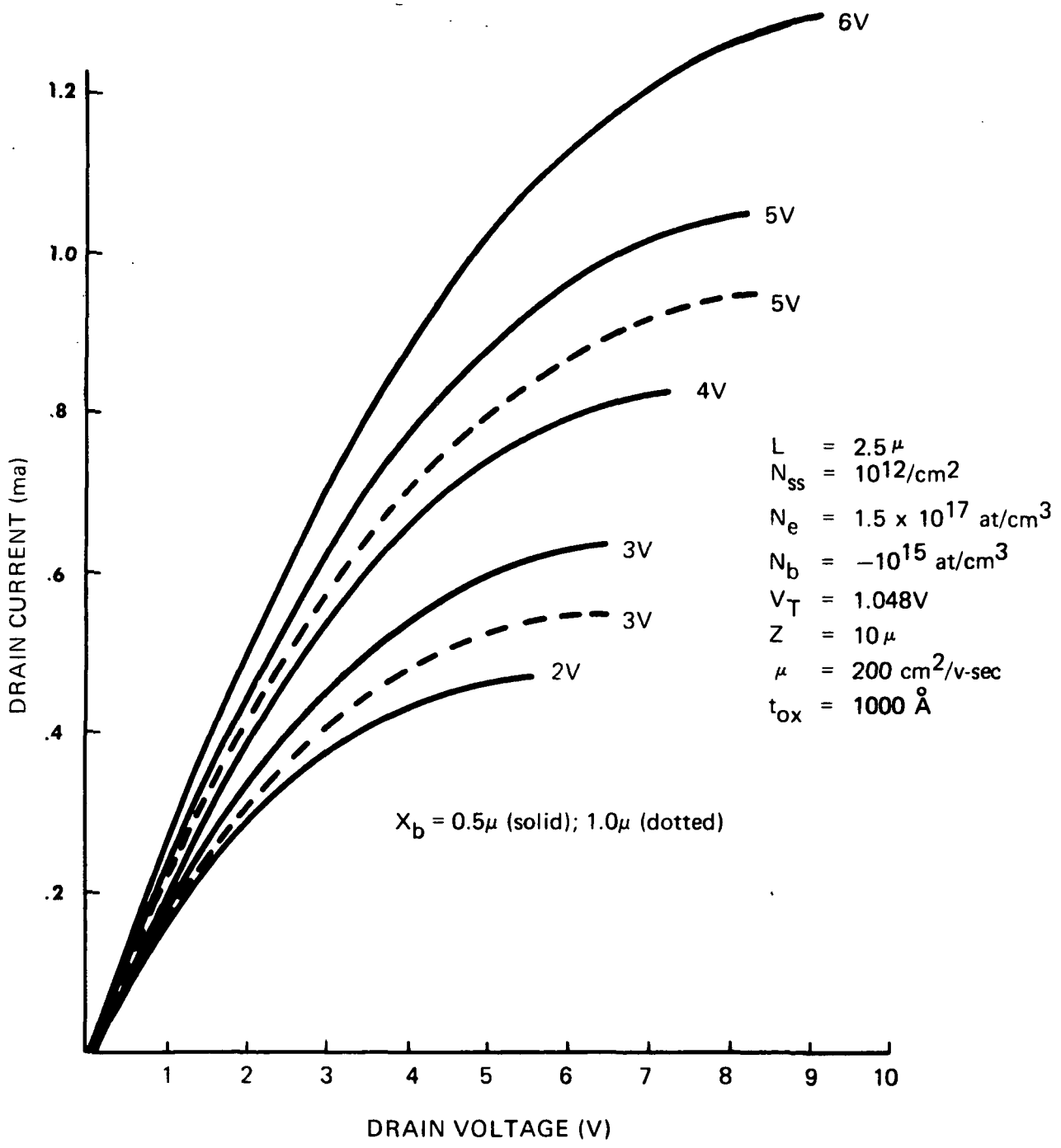

6V
5V
5V
4V
3V
3V
2V
1.2
1.0
.8
.6
.4
.2
DRAIN CURRENT (ma)
1
2
3
4
5
6
7
8
9
10
DRAIN VOLTAGE (V)
L = 2.5μ
N_{ss} = 10^{12}/cm2
N_e = 1.5 x 10^{17} at/cm^3
N_b = -10^{15} at/cm^3
V_T = 1.048V
Z = 10μ
μ = 200 cm^2/v-sec
t_{ox} = 1000 Å
X_b = 0.5μ (solid); 1.0μ (dotted)

Fig. II.8

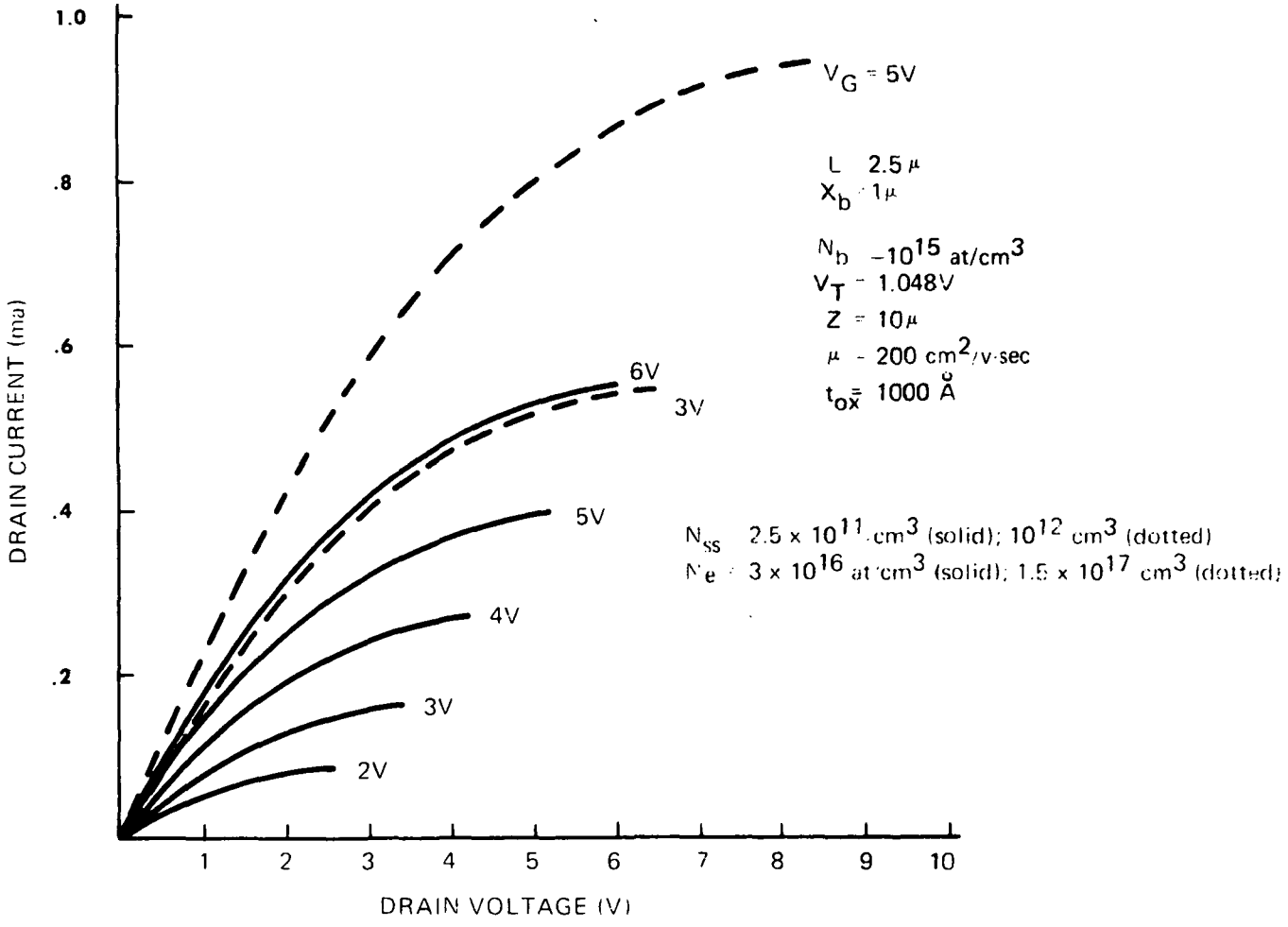

1.0
.8
.6
.4
.2
DRAIN CURRENT (ma)
1
2
3
4
5
6
7
8
9
10
DRAIN VOLTAGE (V)
V_G = 5V
6V
3V
5V
4V
3V
2V
L 2.5 μ
X_b 1μ
N_b -10^{15} at/cm^3
V_T - 1.048V
Z = 10μ
μ - 200 cm^2/v·sec
t_{ox} 1000 Å
N_{ss} 2.5 x 10^{11} cm^3 (solid); 10^{12} cm^3 (dotted)
N_e 3 x 10^{16} at cm^3 (solid); 1.5 x 10^{17} cm^3 (dotted)

Fig. II.9

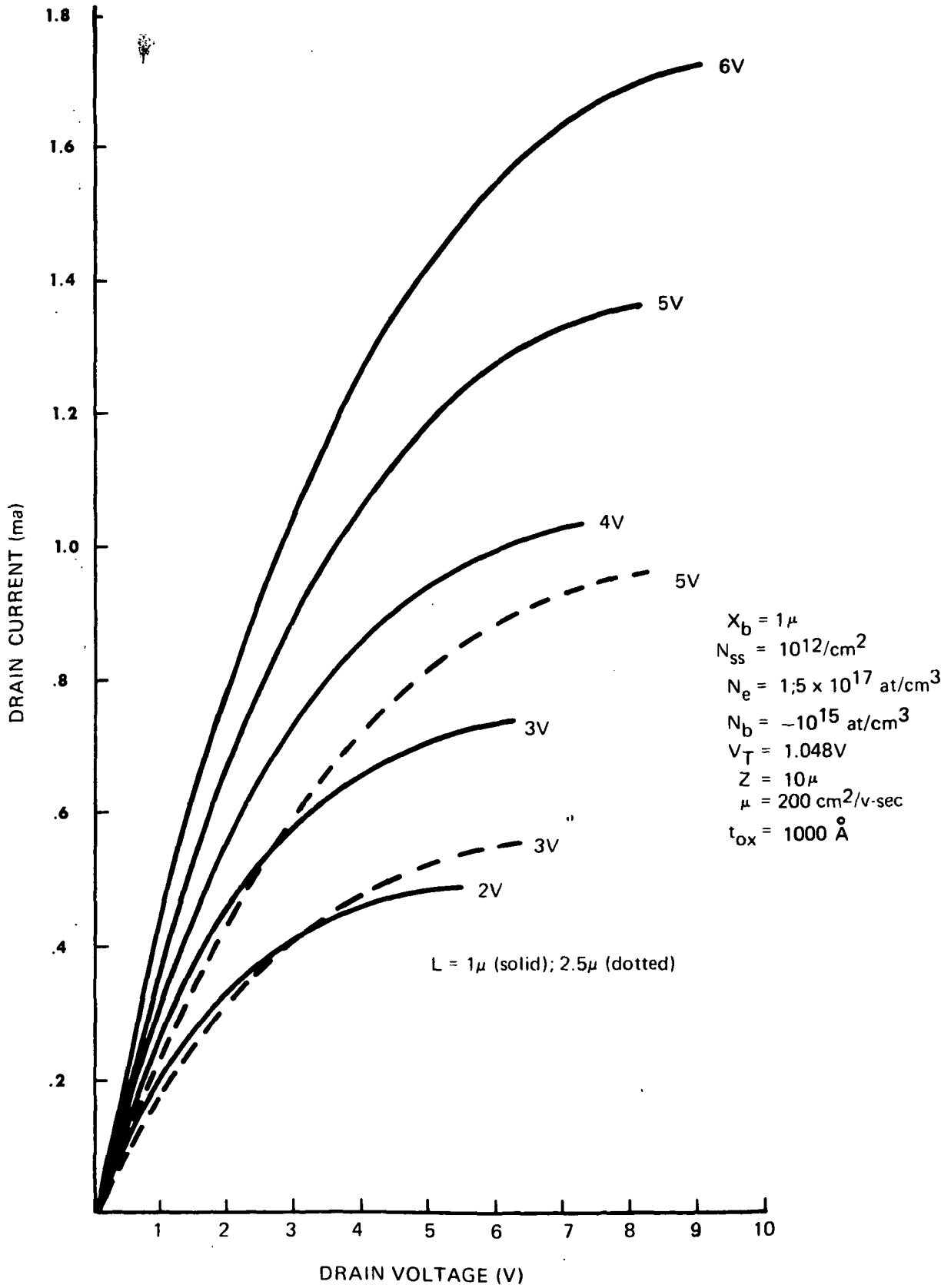

DRAIN CURRENT (ma)
1.8
1.6
1.4
1.2
1.0
.8
.6
.4
.2
1
2
3
4
5
6
7
8
9
10
DRAIN VOLTAGE (V)
6V
5V
4V
5V
3V
3V
2V
L = 1μ (solid); 2.5μ (dotted)
X_b = 1μ
N_{ss} = 10^{12}/cm^2
N_e = 1;5 x 10^{17} at/cm^3
N_b = -10^{15} at/cm^3
V_T = 1.048V
Z = 10μ
μ = 200 cm^2/v-sec
t_{ox} = 1000 Å

Fig. II.10

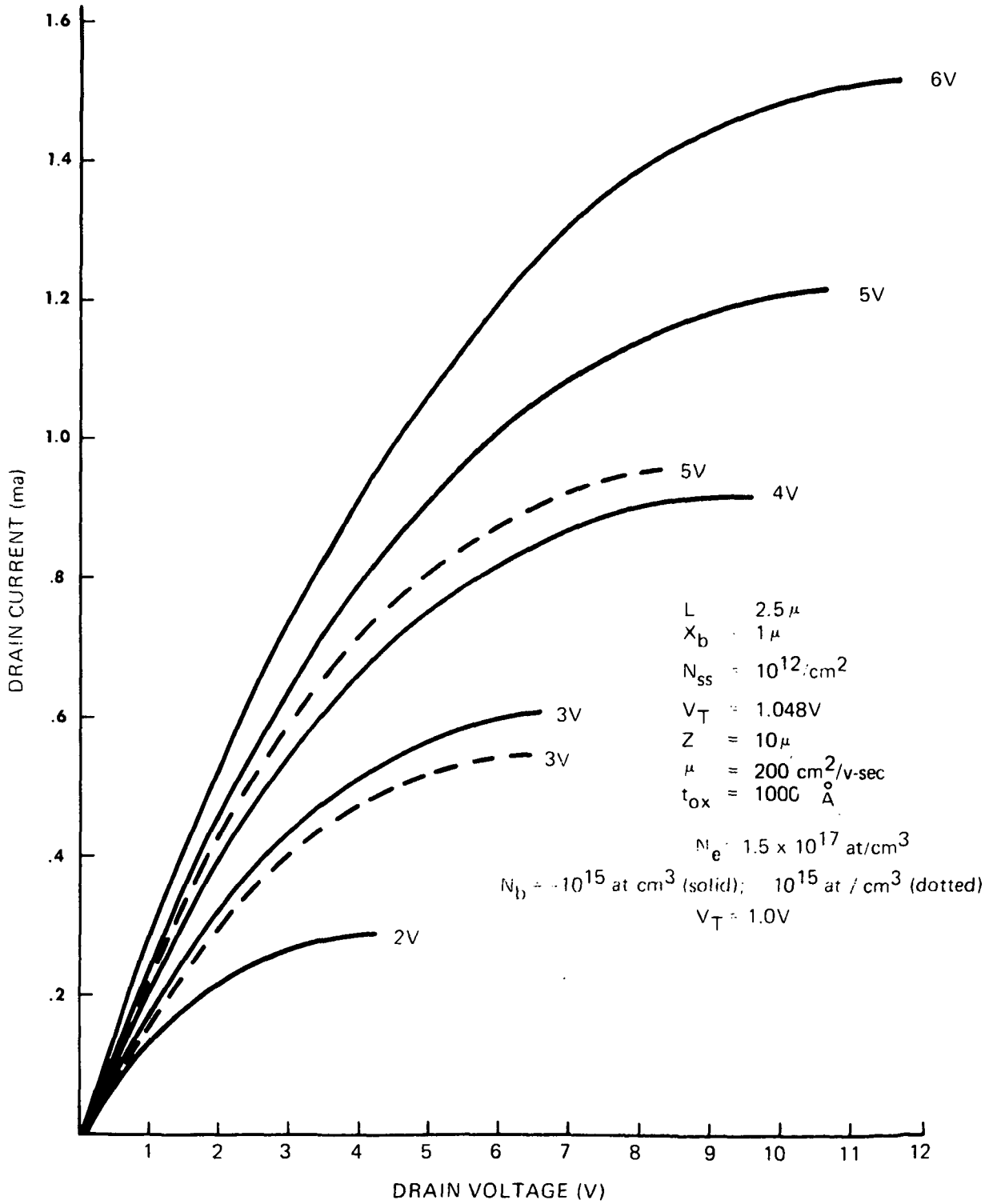

DRAIN CURRENT (ma)
1.6
1.4
1.2
1.0
.8
.6
.4
.2
1
2
3
4
5
6
7
8
9
10
11
12
DRAIN VOLTAGE (V)
6V
5V
5V
4V
3V
3V
2V
L 2.5 μ
X_b 1 μ
N_{ss} = 10^{12}/cm^2
V_T = 1.048V
Z = 10μ
μ = 200 cm^2/v-sec
t_{ox} = 1000 Å
N_e = 1.5 x 10^{17} at/cm^3
N_b = 10^{15} at cm^3 (solid); 10^{15} at / cm^3 (dotted)
V_T = 1.0V

Fig. II.12

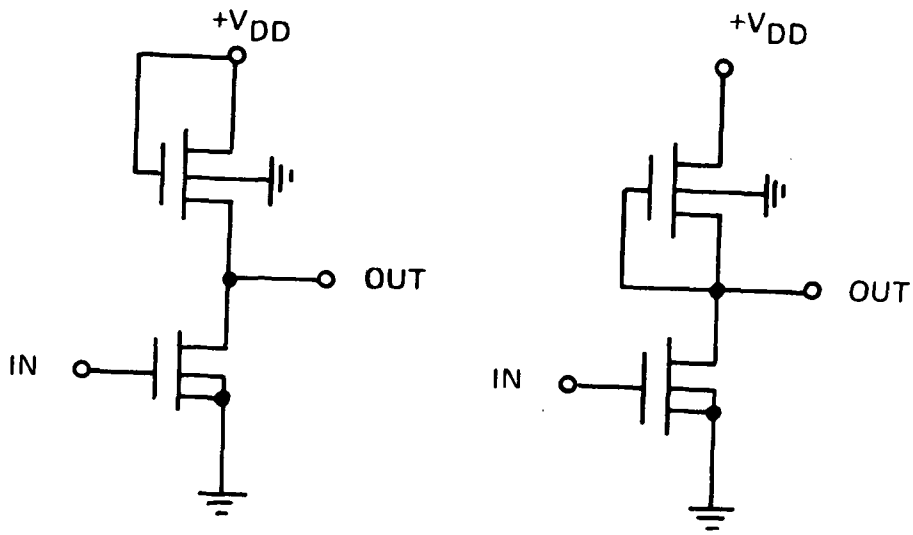


Fig. II.12

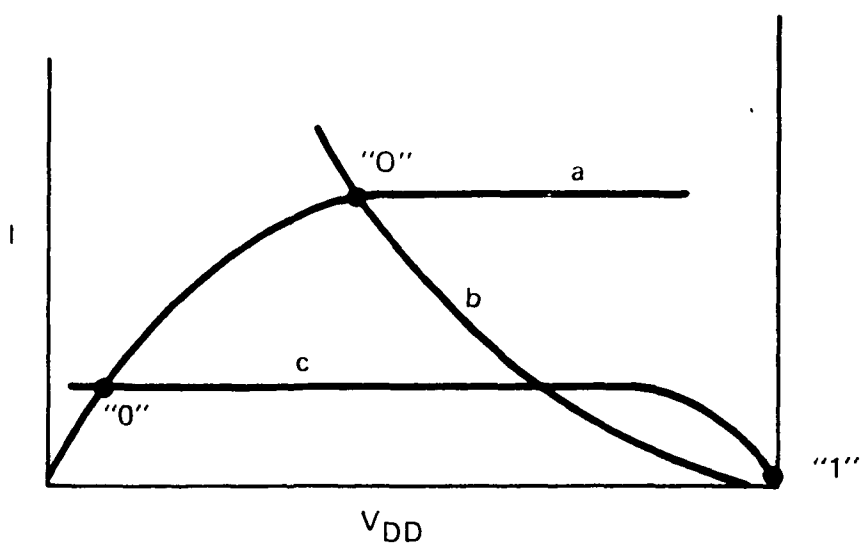


Fig. II.13

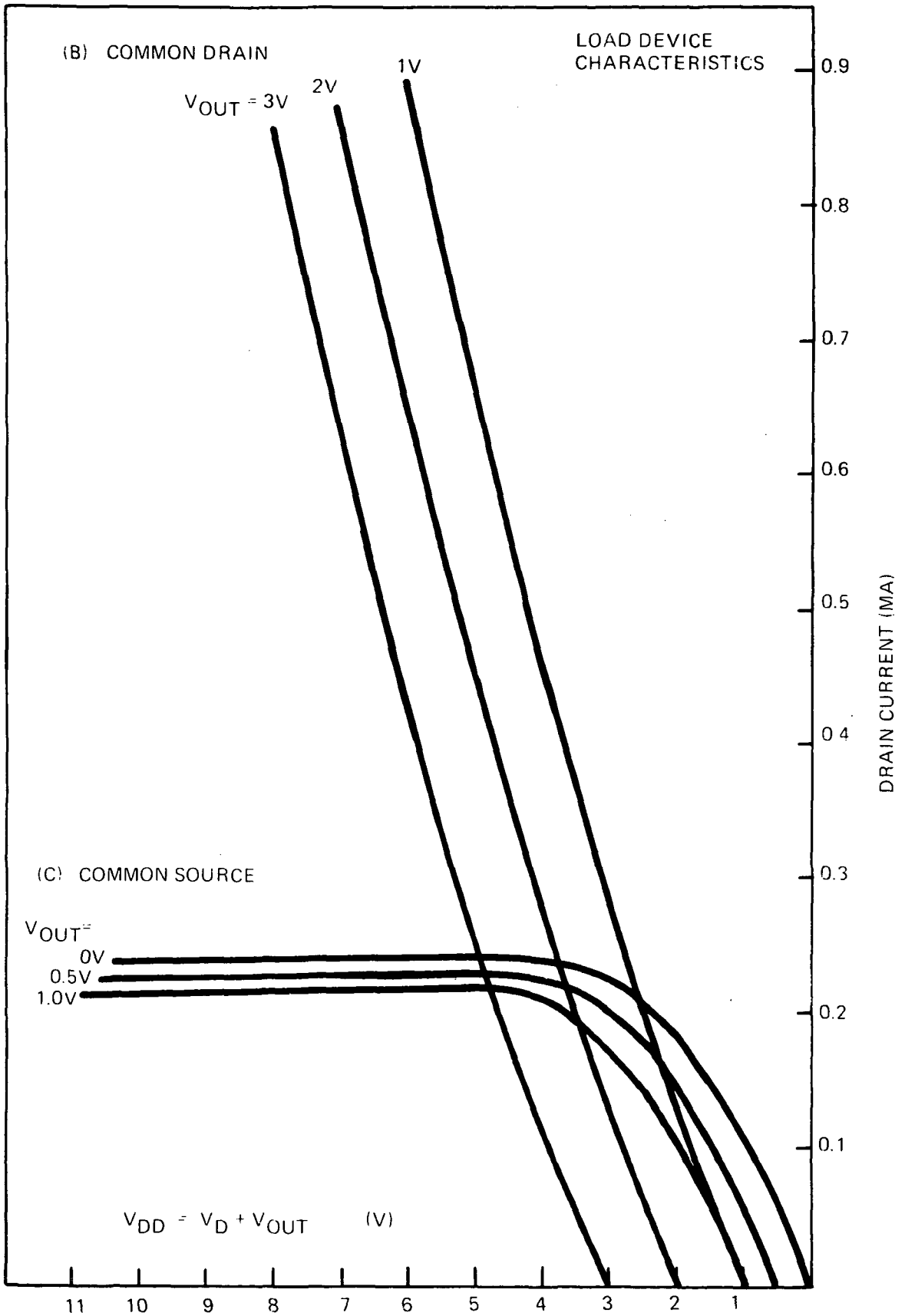
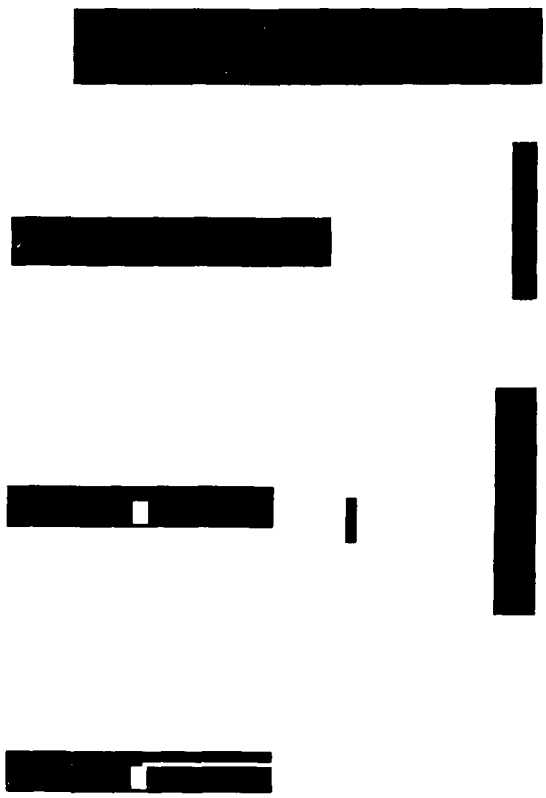
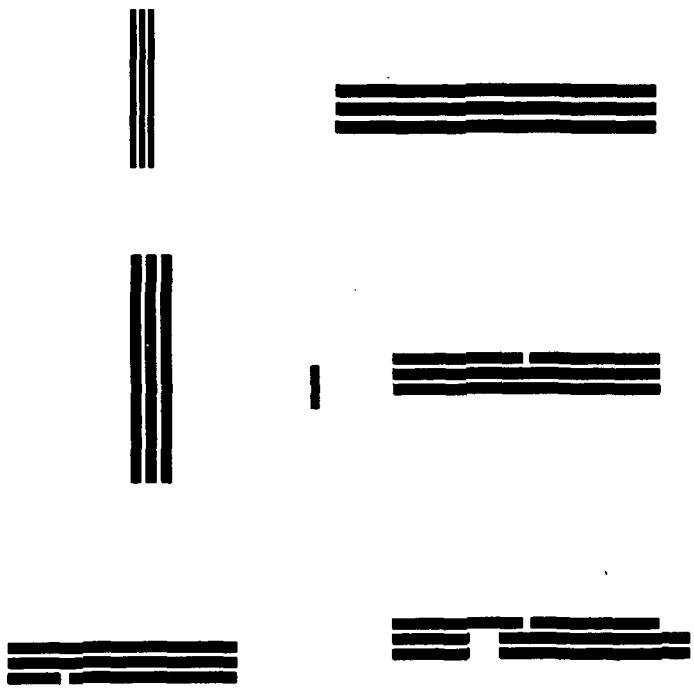

(B) COMMON DRAIN
LOAD DEVICE CHARACTERISTICS
1V
2V
V_{OUT} = 3V
0.9
0.8
0.7
0.6
0.5
0 4
0.3
0.2
0.1
DRAIN CURRENT (MA)
(C) COMMON SOURCE
V_{OUT}=
0V
0.5V
1.0V
$V_{DD} = V_D + V_{OUT}$ (V)
11 10 9 8 7 6 5 4 3 2 1

Fig. II.14



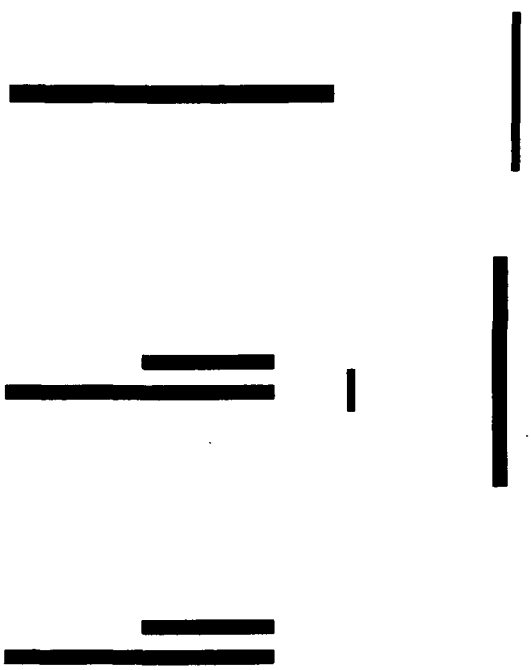
Mask #1

Figure II.15a



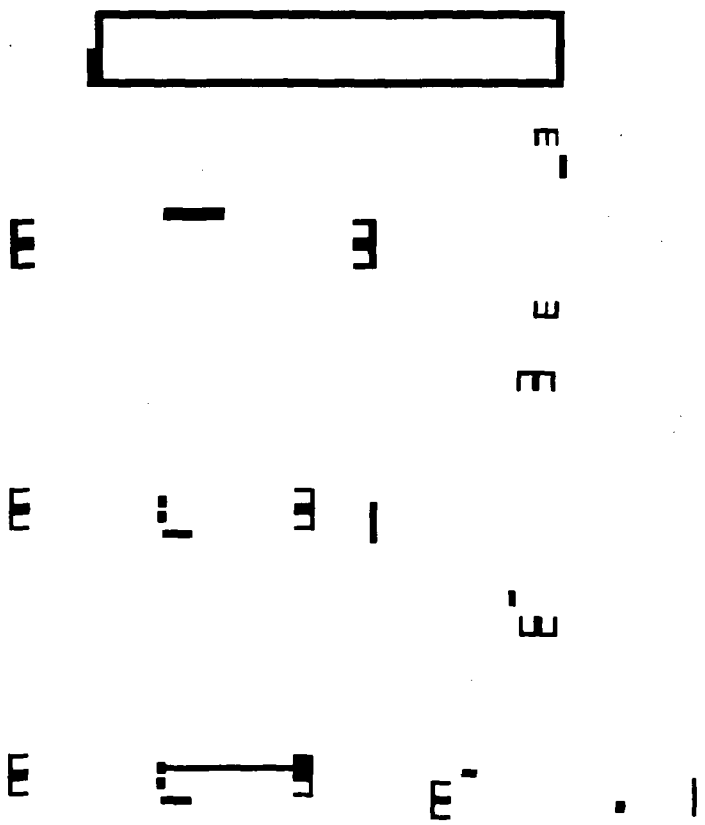
Mask #2 (reversed)

Figure II.15b



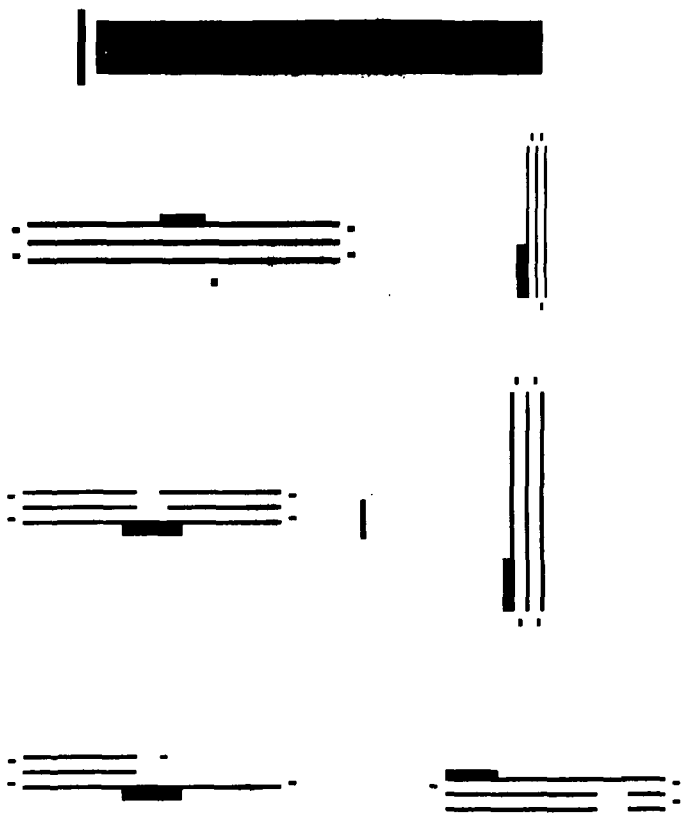
Mask #3

Figure II.15c



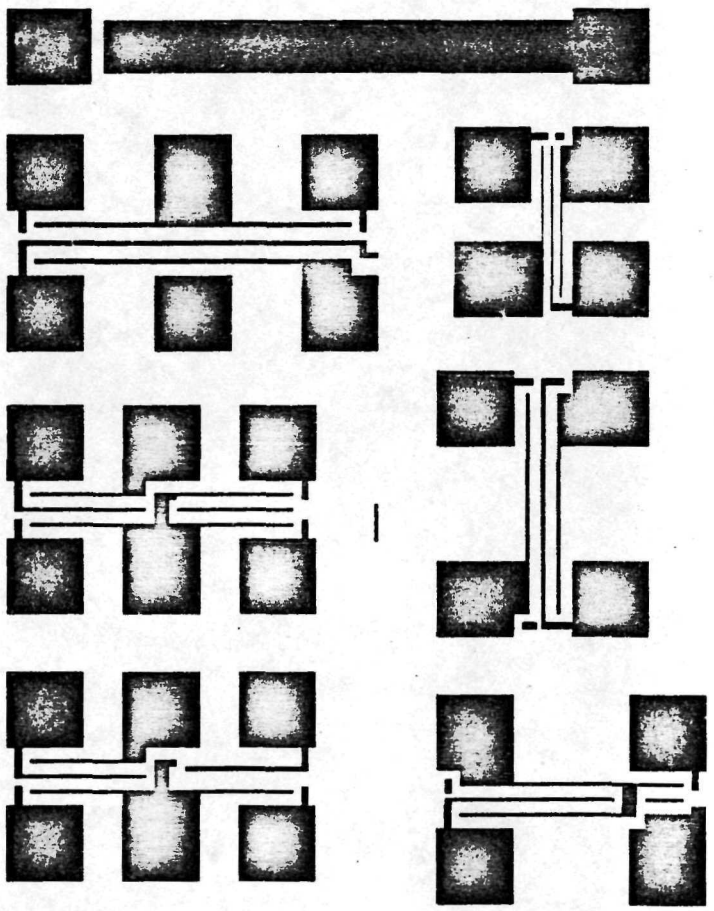
Mask #4

Figure II.15d



Mask #5

Figure II.15e



Mask #6

Figure II.15f

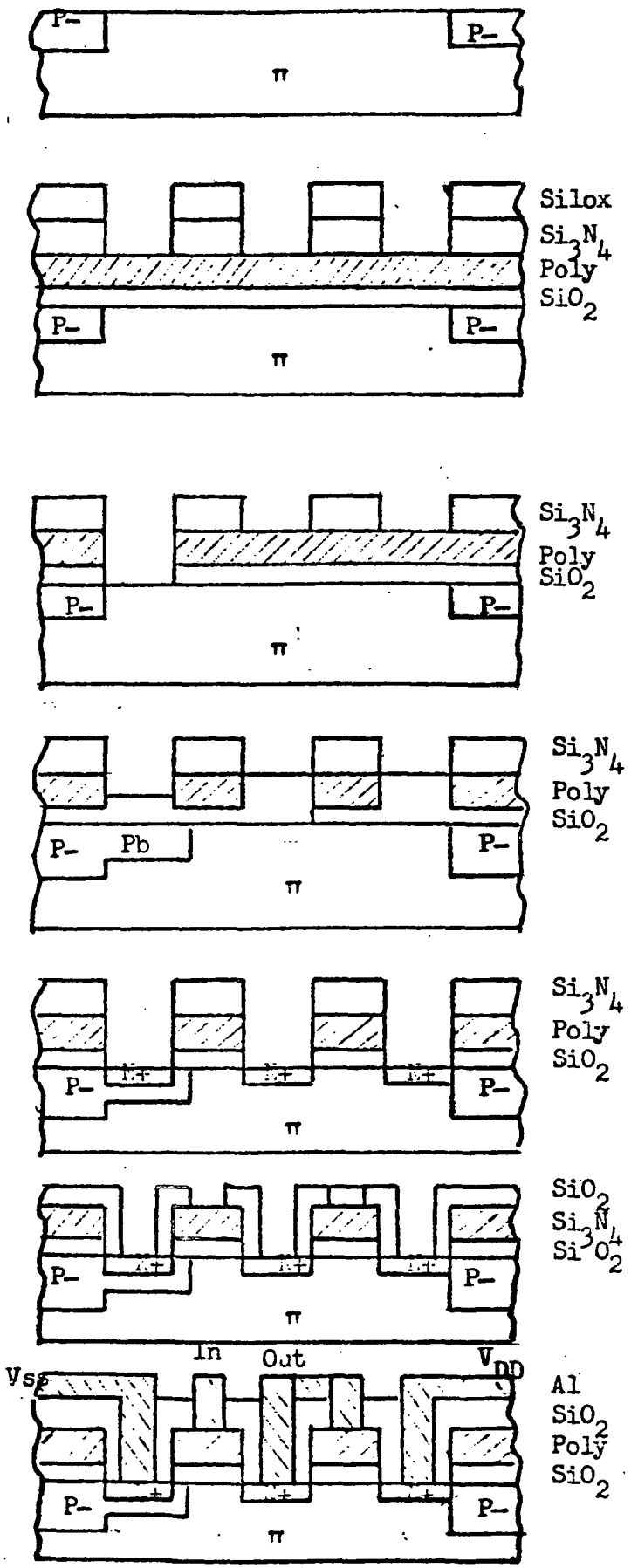


Fig. II.16

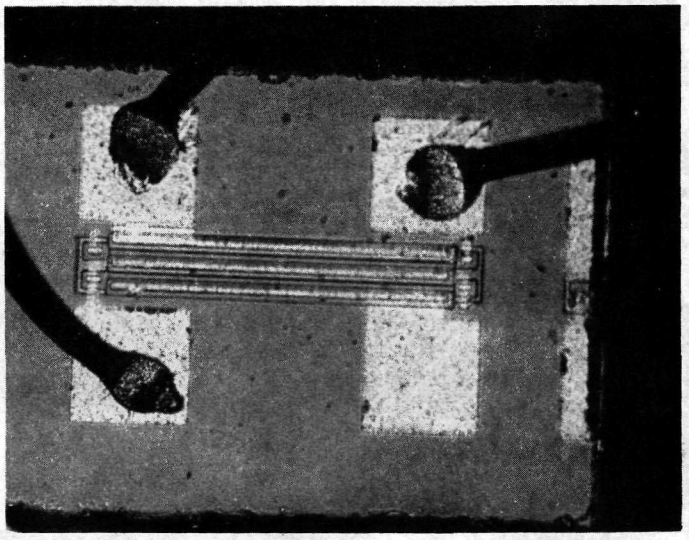
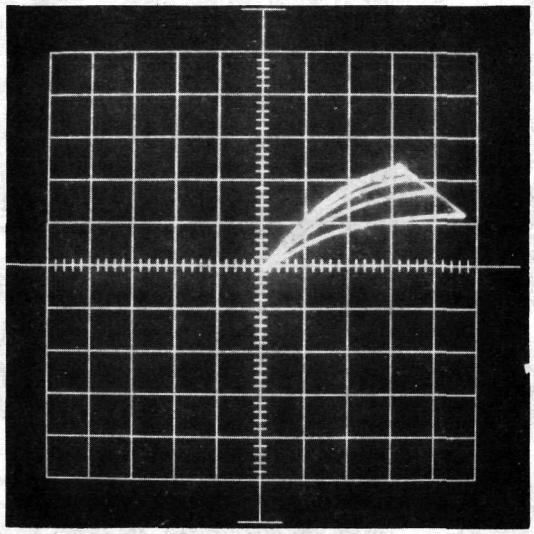
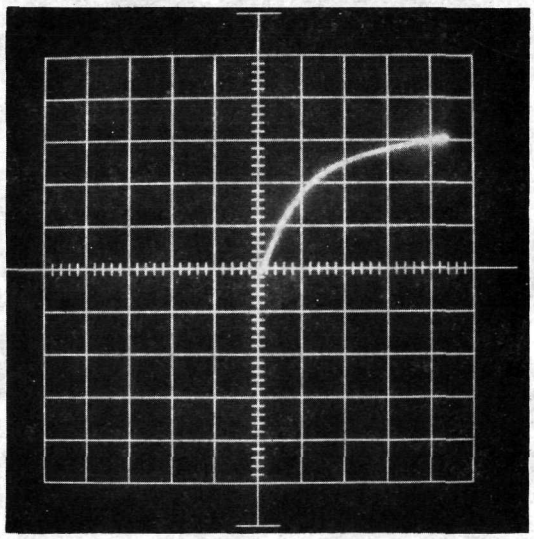


Figure II.17



(a)
DMOS



(b)
Load Device

Fig. II.18 V-I Characterisitcs (2V/horizontal Div;5 mA/vertical Div)