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DESIGN, DEVELOPMENT, AND FABRICATION OF A MICROMINIATURIZED ELECTRONIC ANALOG SIGNAL TO DISCRETE TIME INTERVAL CONVERTER

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TRW SYSTEMS GROUP

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16. Abstract

The microminiaturization of an electronic Analog Signal to Discrete Time Interval Converter (ASDTIC) was completed. Discrete components and integrated circuits comprising the converter were assembled on a thin-film ceramic substrate containing nichrome resistors with gold interconnections.

The finished assembly is enclosed in a flat package measuring 3.30 by 4.57 centimeters.

The module can be used whenever conversion of analog to digital signals is required, in particular for the purpose of regulation by means of pulse modulation. In conjunction with a precision voltage reference, the module was applied to control the duty cycle of a switching regulator within a temperature range of -55°C to +125°C, and an input voltage range of 10V to 35V. The output-voltage variation was less than ±300 parts per million, i.e., less than ±3mV for a 10V output.

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FOREWORD

The authors wish to express grateful acknowledgment of major contributions to this program by Dr. F. C. Schwarz and Mr. R. Cocosa of NASA/ERC, and by Mr. J. J. Biess and Mr. W. T. Ruhl of TRW Systems. Dr. Schwarz originated the conceptual design of the Analog Signal to Discrete Time Interval Converter system, and has provided technical direction throughout the program effort. Mr. Cocosa conducted exploratory system development at NASA/ERC. Mr. Biess performed a significant portion of the work on the system design and development at TRW. Mr. Ruhl was responsible for a considerable part of the microelectronic network development, fabrication, and tests.

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SUMMARY

The objective of this effort was to devise an electronic control system in microcircuit form which can be used to effect pulse-modulation control for a variety of power switching regulators.

The electronic network consists of four major functional blocks: the series regulator, the dc amplifier, the integrator amplifier, and the threshold detector. Fabrication of these functional blocks was accomplished by use of state-of-the-art hybrid-circuit techniques. The finished microcircuit assembly is enclosed in a flat package measuring 3.30 by 4.57 centimeters.

All circuits designed, developed, assembled, and tested as a result of this program effort fully met the specified goals for voltage gain, frequency response, stability, temperature drift, and other performance requirements.

The application of the microminiaturized ASDTIC module to a test converter circuit shows that the 0.1 percent regulation requirement over an input-voltage range of 10 to 35V and a temperature range of -55°C to +125°C can be readily met. Typically, the voltage regulation at room temperature is $\pm$30 parts per million. The temperature drift, attributable to the microelectronic module over the specified temperature range, is $\pm$150 parts per million.

1. INTRODUCTION

The Analog Signal to Discrete Time Interval Converter Program (ASDTIC) was initiated at NASA/ERC in 1966.[1,2] Its objective was to devise an electronic circuit to be used wherever conversion of analog to digital signals is required, in particular, for the purpose of transmission of an analog signal through the technique of pulse modulation. By virtue of this basic function, the network is directly applicable for controlling the duty cycle of the switching type dc to dc converter regulators. The control system, as developed, collects information from the power system in the form of significant analog signals and produces a sequence of control signals at discrete time intervals. The control signals cause rectangular voltage pulses to be generated in the power network for voltage transformation and regulation.

The ASDTIC concept initiated at NASA/ERC was envisioned to offer the following inherent merits: (1) the control system performance is immune to component parameter changes with the regulator, and (2) the control system is capable of achieving simultaneously regulator stability, static performance, and dynamic response. Based on the ASDTIC control concept, preliminary circuits were breadboarded and tested at NASA/ERC to substantiate the high performance envisioned. Subsequently, the control circuit was further developed and refined at TRW to improve the power drain, the current limiting, the flexibility, and other control-circuit performances.

The component parts of this electronic control circuit consist of various IC's, which lent themselves readily to circuit miniaturization. The micro-circuit development was performed at TRW Systems under contract NAS12-2017. Through this effort, discrete components and IC's comprising the circuit were assembled on a thin-film ceramic substrate containing thin-film nichrome resistors with gold interconnections. [3]

This report covers work accomplished on Design, Development, and Fabrication of a Microminiaturized Electronic Analog Signal to Discrete Time Interval Converter. Contract work during the period 1 July 1968 to 15 October 1969, was performed through the following tasks:

1. ASDTIC Module Electrical Design and Development

   Tasks of this phase include the following:

   - o Define detail control-parameter requirements for the ASDTIC module.
   - o ASDTIC Module Circuit Design.
   - o ASDTIC Module Component Testing, Evaluation and Selection.
   - o ASDTIC Module Breadboard and Test.

2. ASDTIC Module Fabrication and Test

   The tasks include:

   - o Microelectronic network ASDTIC module component testing and package design.
   - o Layout and photomask fabrication for the thin-film resistor and interconnect assembly.
   - o Fabrication and assembly of the microelectronic ASDTIC module.
   - o Testing of the ASDTIC module.

3. Precision DC Voltage Reference Fabrication

   The tasks include the circuit development, the worst-case analysis, and the fabrication of a precision voltage reference.

4. Test Circuit Switching Regulator Utilizing the ASDTIC Module and the Precision Reference

The tasks include the development of a test circuit switching regulator and the analysis of control system errors.

The effort of the first two tasks led to the assembly of the microminiaturized ASDTIC module, which is enclosed in a flat package measuring 3.30 by 4.57 centimeters. In conjunction with Task 3, a single-sided PC board measuring 8.2 by 14.6 centimeters was fabricated, which contains both the ASDTIC module and the precision dc voltage reference.

All circuits designed, developed, assembled, and tested as a result of this work fully met contract specifications for voltage gain, frequency response, linearity, tracking, stability, temperature drift, input and output impedances, and system performance.

The program thus successfully demonstrated the feasibility of microminiaturizing the Analog Signal to Discrete Time Interval Converter and the precision reference, which paved the way for future converter control-circuit standardization.

2. DESCRIPTION OF ASDTIC CONTROL CONCEPT

A dc to dc converter shown in Figure 1 consists of three subsystems; the control subsystem, the interface subsystem, and the power subsystem. Starting with the converter output at point A and tracing clockwise, the analog signal at A is processed by the control subsystem, and is transformed into a digital output signal at point C. This digital signal, along with other protection and command signals, is being processed by the interface subsystem to provide the proper on/off control of the power switch. The output of the power switch at point D of Figure 1 forms a voltage pulse train. The digital pulses are converted back to an analog signal by the energy-storage block, thus returning the signal to point A.

The microelectronic network package and the precision reference were developed in this program to serve as the control subsystem for all types of dc to dc converters. Its unique feature is the capability of processing two feedback control signals, rather than processing a single feedback control signal sensing exclusively the specific converter quantity to be regulated. Using a switching series regulator as an example, the essential network elements comprising this two-loop ASDTIC control subsystem is illustrated in Figure 2.

The error-processing component of the ASDTIC concept is a high-gain error amplifier with a capacitor feedback, i.e., an integrator. Two input signals are applied to the integrator-amplifier through two feedback control loops. The first loop senses the dc output voltage e_o of the converter, divides it by a factor $K_d \leqq 1$, and compares $K_d e_o$ to the amplifier reference E_R. The difference $e_{dc} = K_d e_o - E_R$ becomes the dc error input. In conjunction with a threshold-detector level E_T, the dc output level of the integrator-amplifier is determined by e_{dc}. The second loop senses the ac component of $(e_i - e_o)$ across the filter inductor, transforms it by a factor $n \gtreqless 1$, and feeds $e_{ac} = n\,(e_i - e_o)$ differentially to the integrator-amplifier. The rectangular ac voltage e_{ac}, along with the much smaller dc error e_{dc}, are integrated. The

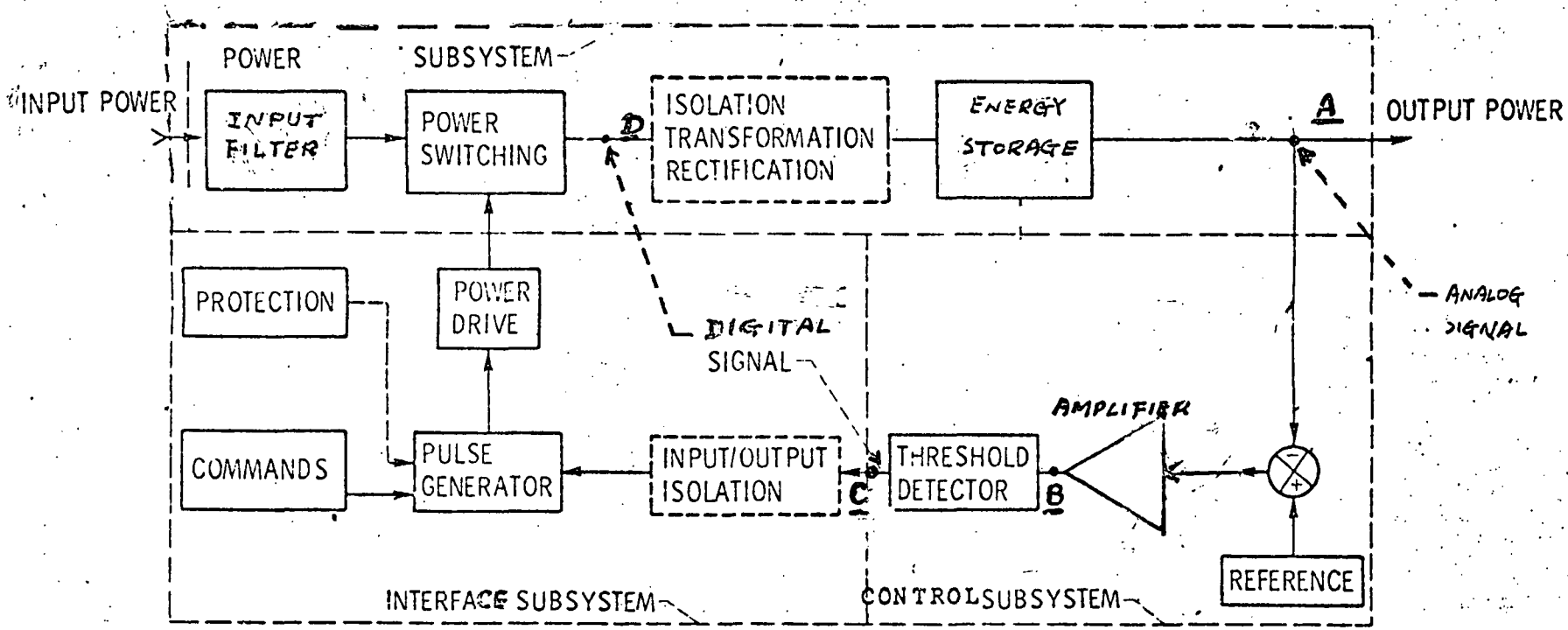


Figure 1 A Generalized Dc to Dc Converter Block Diagram

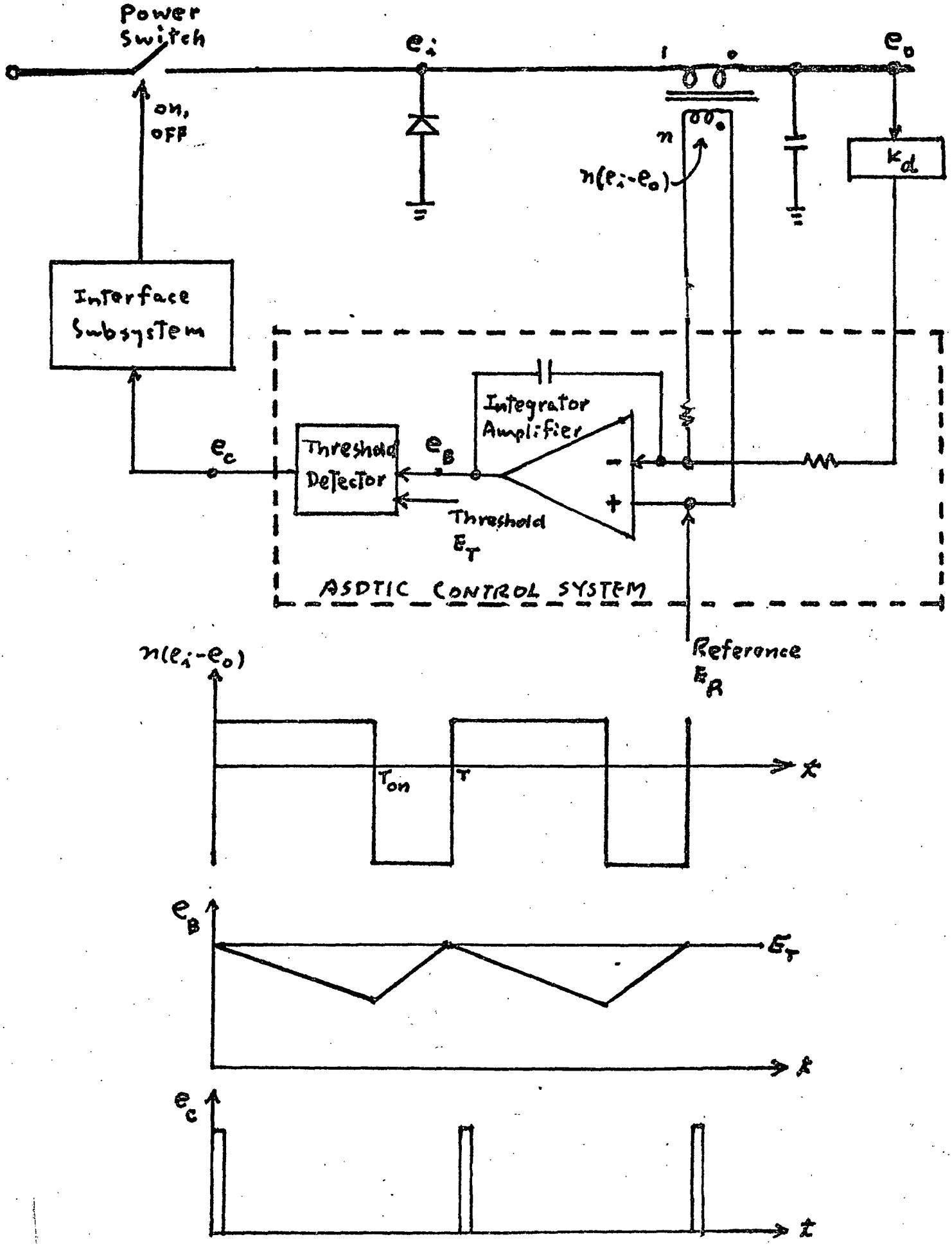


Figure 2. ASDTIC Control and the Signal Waveform.

integrator triangular output, severing as the ramp function, is superimposed on the amplified dc error to intersect the threshold-level E_T. The threshold detector output e_c actuates the interface subsystem to control the duty cycle of the power switch.

The ASDTIC control thus includes, basically, the dc- and ac- loop sensing, the integrator-amplifier for error processing and ramp generation, and the threshold detector. Its adaptability to all switching regulators is apparent. For as long as there exists within the regulator an inherent ac waveform suitable for ramp-function generation, the ASDTIC control can be conveniently applied.

As stated previously in Section 1, the two-loop control concept was breadboarded preliminarily and tested. In relation to a conventional single-loop control, the performance improvement as a result of using this control concept was experimentally substantiated. This performance advantage, in conjunction with its universal appeal for controlling all types of switching regulators, prompted the decision to reduce this control concept into a microelectronic network package. The package, along with the precision voltage reference, fulfills a standardized control subsystem, shown in Figure 1.

The microelectronic package contains four major network elements:

- Integrator Amplifier
- Threshold Detector
- Unity-Gain Amplifier
- Series Regulator

The electrical functions served by the integrator amplifier and the threshold detector have been previously described.

The unity-gain amplifier is used between the integrator amplifier and the sensed converter output (usually the output voltage). Its function is to eliminate the loading effect of the integrator amplifier to the resistive voltage divider sensing the regulated output. This function can be optional when dealing with a low-voltage output where the divider resistances are low and the integrator loading effect is negligible. However, it is indispensible when the regulated output

voltage is high (e.g., 10KV for high power TWT) where the divider resistance is in the order of hundreds of megohms.

The series regulator is needed to provide a regulated bias voltage for all aforementioned operational amplifiers.

Having identified these major network elements, the design, development, fabrication, and test of the ASDTIC module containing these elements, are presented in the subsequent sections. The presentation, supplemented by that of a precision dc voltage reference, completely describe a microminiaturized control subsystem applicable to all types of switching regulators.

3. ASDTIC MODULE DESIGN AND DEVELOPMENT

The schematic diagram of the microelectronic ASDTIC module, consisting of the integrator-amplifier, threshold detector, series regulator, and the unity-gain amplifier, is shown in Figure 3. The schematic also shows the relevant pin assignment of the module. The parts list for components shown in Figure 3 is given in Table I.

3.1 Control Parameter Requirements, Selection and Testing.

The control parameter requirements, the network component selection, and the breadboard testing for each of the four major networks are summarized in Table II.

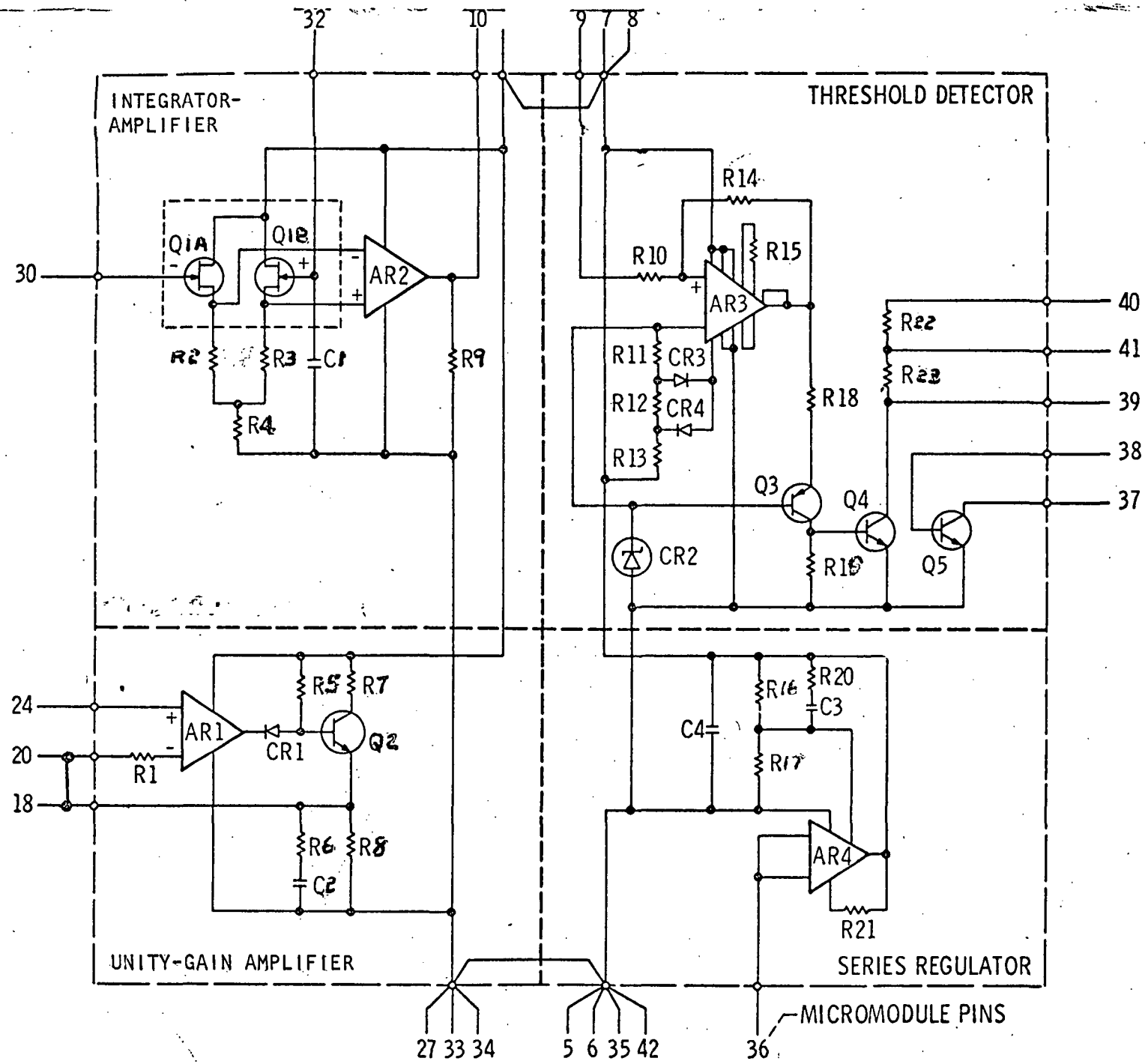


Figure 3. - ASDTIC MODULE SCHEMATIC DIAGRAM

TABLE I. PARTS LIST, MICROMINIATURIZED ASDTIC MODULE

Circuit Description	Part Type	Vendor
AR1	RM4101-Q	Raytheon
AR2	RA909A	Radiation, Inc.
AR3	RA238	Radiation, Inc.
AR4	LM100F	National Semiconductors
Q1	KY3956	Union Carbide
Q2	TIS23	Texas Instruments
Q3	MMT3906	Motorola
Q4, Q5	MMT2369	Motorola
CR1, CR3, CR4	LP100	General Instrument
CR2	PD6209	TRW
C1	1BX050S222J, 2200pf	Varadyne
C2	1BN050S101J, 100pf	Varadyne
C3	1BN050S470J, 47pf	Varadyne
C4	WX22394J, 0.39uf	JFD Electronics
R1	10K	*
R2	4.5K	*
R3	4.5K	*
R4	22K	*
R5	2C754F, 750K	Varadyne
R6	5K	*
R7	1C224F, 220K	Varadyne
R8, R14	2C204F, 200K	Varadyne
R9	20K	*
R10	1K	*
R11	1K	*
R12	4K	*
R13	3.3K	*
R15	13K	*
R16	22K	*
R17	1.8K	*
R18	2K	*
R19	2K	*
R20	6.8K	*
R21	6 ohms	*
R22	39K	*
R23	39K	*

*Thin-Film Nichrome Resistors

TABLE II. SUMMARY OF ASDTIC MODULE CONTROL PARAMETER REQUIREMENTS, CIRCUIT IMPLEMENTATION, COMPONENT SELECTION, AND BREADBOARD TESTING.

	CONTROL PARAMETER REQUIREMENTS	CIRCUIT IMPLEMENTATION	COMPONENT SELECTION & BREADBOARD TESTING
Integrator-Amplifier	o 10-to-1 imbalance allowable for input impedance to two integrator terminals. o +1.5mV maximum for total input drift due to both current and voltage offset temperature coefficient. o 20db gain at 100KHz with slew rate 1V/us. o dc gain greater than 100db, phase margin greater than 45 degree over the temperature range. o Maximum and minimum peak-to-peak integrator output voltage of 8V and 200mV. o These requirements must be met by a circuit with only modest power demands.	o The circuit configuration contains a field effect transistor source follower (Q1) driving an operational amplifier AR2. o The driver stage is required to maintain low input current and to eliminate the input current offset temperature coefficient. o Minimization of the input-voltage offset temperature coefficient is accomplished by trimming resistors R2 and R3.	o A matched N-channel junction FET pair (KY3956) manufactured by Union Carbide is utilized as the driver stage. o The integrator-amplifier selected was the RA909A from Radiation, Inc. o The drift characteristic was tested over the temperature range, and was found to be within the requirement. o Testing of open-loop frequency response of the composite FET-Amplifier over the temperature range gives a minimum phase margin of 45 degrees at 125°C.

Table II. (Cont'd)

	CONTROL PARAMETER REQUIREMENTS	CIRCUIT IMPLEMENTATION	COMPONENT SELECTION & BREADBOARD TESTING
Threshold Detector	o ±4uA maximum input current. o Power to its output circuitry can be provided by an external source voltage ranging from 5V to 32V. o Negative-going output pulse falls within 0.1us. Positive-going pulse rises within 0.3us. o The delay of the threshold detector is less than 1us. o Capable of sinking 10mA peak at 0 to 0.5V.	o It consists of a dc amplifier AR3, a reference diode CR2, and a three-transistor level-shift driver Q3, Q4, and Q5. o To prevent the amplifier from saturating and exhibiting long storage time, the output swing of the threshold-dector amplifier is limited by diode clamping. o A small amount of hysteresis is controlled by R14 and R18 to approximately 25mV. o Transistors Q4 and Q5 provide the flexibility of having either a logical-0 or a logical-1 signal at the threshold-dector output.	o RA238 was selected as the threshold-detector amplifier, which represents an optimum compromise between the switching speed and the power consumption.

Table II. (Cont'd)

	CONTROL PARAMETER REQUIREMENTS	CIRCUIT IMPLEMENTATION	COMPONENT SELECTION & BREADBOARD TESTING
Series Regulator	o Input voltage 24V to 32V, output voltage at 20V ±2%. o Output Current 12mA. o Output impedance less than 2 ohms from dc to 100KHz. o Stable under all operating conditions.	o It consists of a dc amplifier AR4, sensor resistors R16 and R17, compensating network C3, C4, and R20, and current-limiting resistor R21. o The combination of C3, C4, and R20 provides the low output impedance and regulator stability. o This configuration differs from that recommended by the manufacturer, which resulted in high output impedance at high frequencies.	o The LM100 voltage regulator was selected as the best flat pack in production at the time. o A worst-case output-voltage regulation of +1.5% was measured at +125°C at high line and heavy load. o In testing the open-loop frequency response, a minimum phase margin of 45 degrees was obtained at +125°C. o Worst-case output impedance occurs at -55°C, and stays very much constant from 10KHz up to 100KHz at about 1.7ohms.

Table II. (Cont'd)

	CONTROL PARAMETER REQUIREMENT	CIRCUIT IMPLEMENTATION	COMPONENT SELECTION & BREADBOARD TESTING
Unity-Gain Amplifier	o The driving source resistance less than 10,000 ohms. o Input voltage for normal operation was 6V to 8V. During transient, the voltage it can take is between 0 and 10.5V. o The voltage gain is 1 $\pm$ 0.01 from dc to 10KHz. o 5 megohms input impedance or greater. o Less than an output impedance of 25 ohms from dc to 10KHz when output is not current-limiter. o Greater than 45-degree phase margin over the temperature range. o (V_{out} - V_{in}) is less than 5mV at 25°C. The temperature tracking over -55°C to +125°C and 6V to 8V of input voltage is $\pm$0.5mV. o Drift at constant temperature is less than 10μV/Hour and 50μV/day.	o The unity-gain amplifier consists of amplifier AR1, a diode-transistor gate CR1-Q2, the associated resistances, and the compensating network R6-C2. o The emitter follower output stage Q2 provides low output impedance when operated in its linear range. It also provides current limiting by saturating or cutting off when its output-current limit is exceeded.	o Raytheon's RM4101-2 was used as AR1. o Results of actual ac gain measurements showed the low frequency gain to be much closer to unity than the analysis would indicate. The difference is resolved by considering the common-mode rejection ratio. o For 6V $<V_{in}<$8V, the deviation in V_{out} from linearity is about 15μV for the worst-unit tested. o The input impedance is in the order of 50 megohms. The output impedance is about 7.5 ohms at 10KHz. o Due to the leakage current of diode CR1 at 125°C, the output current of transistor Q2 is more than 50μA (about 57μA) at an output voltage of 6V. o A phase margin of 43 degrees was measured for resistive loads over the complete temperature range.

3.2 ASDTIC Module Current Demand

The current demand from the various microelectronic circuits is listed in Table III. At high duty cycle of 0.9 to 0.95, the pwoer demand increased slightly because the threshold detector remains in on-state a large percentage of the time. The maximum total current through the series regulator is 13 milliamps. In conjunction with a series regulator output voltage of 20V, the maximum total power drain is 260 milliwatts.

TABLE III

ASDTIC MODULE CURRENT DRAIN

Item	Current 0.3 to 0.9 Duty Cycle	Current 0.9 to 0.95 Duty Cycle
Series Regulator	200mA	2.0mA
Reference and Divider	1.5mA	1.5mA
DC Amplifier	1.3mA	1.3mA
Integrator	2.5mA	2.5mA
Threshold Detector (Low Level)	4.2mA	5.7mA
Total through Series Regulator	11.5mA	13.0mA

4. ASDTIC MODULE FABRICATION AND TEST

Subsequent to the cricuit design and breadboard testing to verify preliminarily all electrical characteristics, the program proceeded toward the manufacturing of the microminiaturized ASDTIC module. Specifically, the program effort can be described in the following tasks: (1) Component testing, (2) Layout and Packaging, (3) Subsrate fabrication, (4) Assembly, and (5) Testing.

4.1 COMPONENT TESTING

All component parts and integrated circuits for each ASDTIC module were thoroughly tested prior to assembly. Special test fixtures were fabricated, and detailed test procedures were prepared. Components tested include KY3956 as the FET pair associated with the integrator amplifier, RA238 of the threshold detector, RM4101 -2 of the unity-gain amplifier, and LM100F of the series regulator. The test fixture and the test procedure involved for each component are presented in Appendix 9.1 Significant characteristics obtained from the testing are summarized in Table IV.

TABLE IV. A SUMMARY OF COMPONENT TESTING RESULTS PRIOR TO ASSEMBLY

Components	Typical Test Results				Assemblies
	Bandwidth (MHz)	Phase Margin (degree)	Drift (mV)	Switching Speed (μs)	
RA909A	1 - 1.5	45 - 53	1 - 3	-	
KY3956	-	-	Properly controlled by trimming source resistors	-	Three units exhibited erratic temperature drift characteristics, and were rejected before assembly started.
RA238	-	-	-	Input-output negative transition delay: 1.5-2.2 Input-output positive transition delay: 1.0-1.5 Rise time = 0.3 Fall time = 0.1	
RM4101-Q	0.27	43	±0.5		
LM100F	0.05 - 0.35	44	±80mV regulation for a 20V output		One unit did not regulate well at low temperatures, and was rejected.

4.2 LAYOUT AND PACKAGING

4.2.1 Package Description

Proper selection of the protective package is critical for the microcircuit performance and fabrication. The package configuration is selected based on the following considerations:

- Since the integrated circuits for the converter were already packaged in hermetically sealed flatpacks, hermeticity is not imperative.
- The package has to provide proper RF shielding in order to meet the noise requirements of the system.
- Package size has to be adequate to accommodate the substrates on which the components are assembled.
- Accessibility to the internal circuit terminals of the microcircuit must be adequately available.

Based on these considerations, a 42-pin metal base, metal lid flat package shown in Figure 4 measuring 3.30 by 4.57 centimeters (1.3 by 1.8 inches) was selected.

4.2.2 Layout and Mask Design

This was accomplished through the following steps:

- Preparation of a layout drawing of all components, interconnections, and terminals. The layout was prepared at 50 times actual size.
- After inspection of the layout for proper dimensions, tolerances, interconnections, resistor values, registration marks, and other details, the art work was prepared on Mylar laminate (Rubylith) material. A coordinatograph is used for this process which allows precise location of all elements to a tolerance of ±50 microns.
- Artwork is then photographically reduced. Copy prints of the master mask, produced after the reduction, are used as working masks for the various processing steps. Since they are used in sequence, precision is required to register each pattern with the previous one in the process sequence.
- To facilitate production processing, the substrate was designed as two separate pieces shown in Figures 5, each measuring 2.49 by 1.85 centimeter (0.98 by 0.73 inch). The two pieces fit onto two flat mounting surfaces of 2.54 by 3.81 centimeters (1 by 1.5 inch).

- The two substrates shown in Figures 5 are designated as ASC-1 and ASC-2. Substrate ASC-1 accommodates the unity gain amplifier and the integrator amplifier. Substrate ASC-2 accommodates the threshold detector and the series regulator.
- Care was taken in routing interconnections to avoid placement of sensitive components in areas where high current spikes may be expected and to make high impedance paths as short as possible.

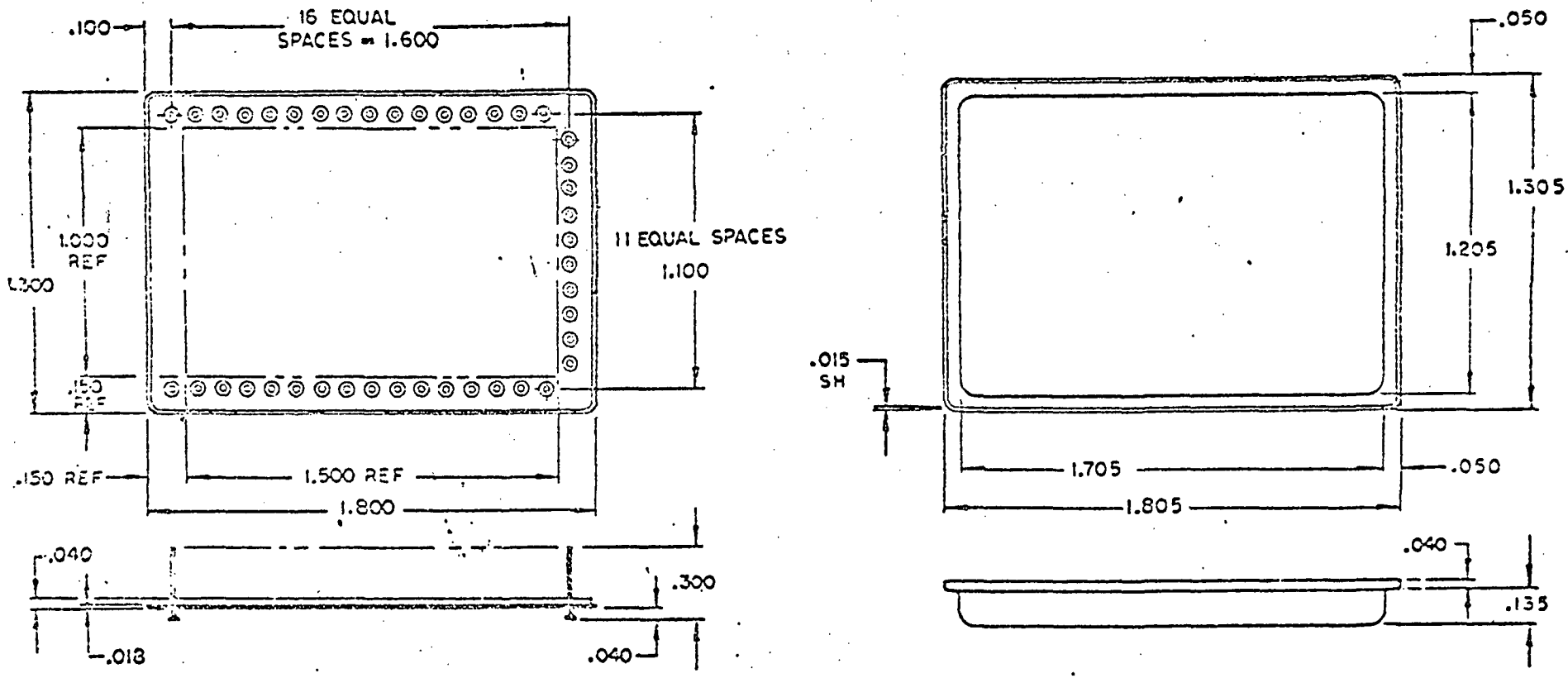


Figure 4.- Package Configuration

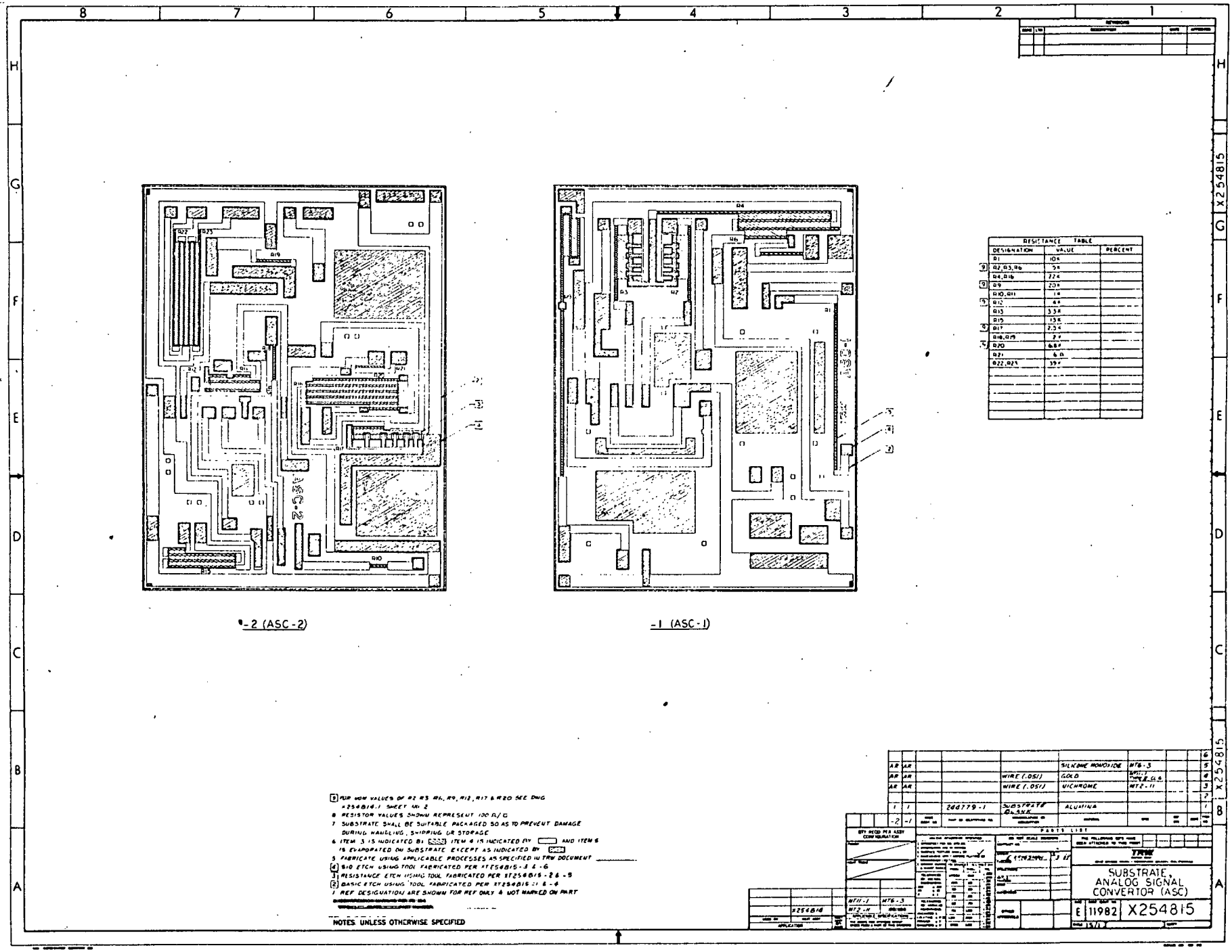


Figure 5 The Two Substrates Comprising the ASDTIC Module

4.3 SUBSTRATE FABRICATION

4.3.1 Substrate Material

Requirements of the thin film substrate material are:

Surface Smoothness 1 microinch
Flatness
High resistivity 10^8 ohm cm
Low thermal conductivity
Chemical resistance
Free of surface defects

For a hybrid circuit with the power dissipation requirement of the converter, a glazed alumina substrate material was selected. The size of the substrate material was 6.35 by 3.81cm with a thickness of 0.038 to 0.051cm.

4.3.2 Substrate Fabrication

The manufacturing flow chart for the substrate fabrication can be described as the following:

(1) Kit Per Parts List and Kit Inspection (Procedure MOI-1-001)

(2) Clean Substrate (Procedure QI-E4.0.7.1)

(3) Nichrome and Gold Deposition (Procedure MFI-333)

The substrates were loaded into a vacuum chamber and heated to about 300°C. After reading a vacuum of better than 10^{-6} Torr, NiCr was evaporated from a hot filament. A resistance monitor is used to determine the resistance of the NiCr film. After reaching a predetermined value, a shutter between the source and substrate is closed. Sheet resistivity used for the NiCr film is 100 ohms/square.

(4) Gold Plating (Procedure MFI-457)

The deposited NiCr films are annealed under vacuum for several hours and coated with a gold film which is used for the conductors. Resistivity of conductor films is in the 0.10 to 0.01 ohm/square range. Resistor films must adhere to the substrate and form a good bond to the conductive film. By proper heat treatment, extremely stable resistive films with temperature

coefficients as low as ±25 ppm have been obtained. Drift is in general less than 0.5% per 1000 hours at 150°C.

(5) Photoengrave Thin Film Resistor/Conductor (Procedure MFI-003)

(6) Photoengrave Lacquer Removal (Procedure MFI-004)

(7) Substrate Inspection (Procedure MFI-007)

(8) Photoengrave Thin Film Resistor (Procedure MFI-003)

(9) Photosensitive Lacquer Removal (Procedure MFI-004)

Substrates were etched to define resistor and conductor geometries and pads for wire bonding and component mounting. Etching requires photolithographic masking to expose only those parts of the substrate to be etched away.

(10) Substrate Inspection (Procedure MFI-007)

(11) Test Resistance and Trimming (Procedure MFI-467)

(12) Photoengrave SiO A21350H (Procedure MFI-260)

(13) SiO Deposition (Procedure MFI-009)

The coating of a SiO film provided the substrates with protection and improved stability.

(14) Photosensitive Lacquer Removal (Procedure MFI-004)

(15) Stabilize Matrix (Procedure MFI-332)

The substrate, with the coated SiO, was again subjected to a high-temperature annealing process. After final testing and inspection for visual defects, the substrates are trimmed to final size.

(16) Test Per Resistance Table (Procedure MFI-355A)

Thin film resistors are able to be adjusted to a precise value after fabrication (Table V). This provides resistors with tighter tolerances than those available as discrete components, and also permits resistive compensation for other components in the completed circuit, a function associated with potentiometers or trimming resistors in conventional circuitry.

For the resistor trimming, some resistors are shunted by deposited metal links which are evaporated by a current pulse or removed by physically cutting them open.

Another technique used at TRW employs a laser to alter thermally the resistance of the material itself. Pulses of the high-intensity laser radiation focused on the resistor create extremely high temperatures at localized spots of the resistive material. Since nichrome films show increased resistance after laser trimming, film resistors are deposited with a resistance somewhat below that desired and then trimmed to the prescribed value.

Electrical tests of the substrate resistors are performed at three fabrication stages: (1) before SiO deposition, (2) after SiO deposition, and (3) after thermal stabilization. Resistor change between the first and second tests is about 1 to 2 percent, between the second and third tests, less than +0.2 percent.

(17) Scribe Substrate (Procedure MF1-261)

(18) Final Clean (Procedure MF1-223

(19) Inspection of Complete Circuits (Procedure MF1-018)

(20) Package and Identify (Procedure MF1-340)

(21) Inspection (QOI-4.102)

(22) Substrate Storage (Procedure MO1-001)

TABLE V. THIN-FILM RESISTOR VALUES FOR ASDTIC MODULE SUBSTRATES

	Nominal	Minimum	Maximum	Tolerance Range
R1	10K	9K	11K	
R2	4.5K	3.6K	5.4K	Must be within ±200Ω of matching
R3	4.5K	3.6K	5.4K	
R4	22K	20K	24K	
R5	Chip Resistor			
R6	5K	4K	6K	
R7	Chip Resistor			
R8	Chip Resistor			
R9	20K	16K	24K	
R10	1K	800	1200	
R11	1.1K	1.0K	1.2K	Must Match
R12	3K	2.7K	3.3K	Within
R13	3.3K	3.0K	3.6K	5 Percent
R14	Chip Resistor			
R15	13K	10.5K	15.5K	
R16	22K	19K	25K	
R17	1.8K	1.5K	2.1K	
R18	2K	1.8K	2.2K	
R19	2K	1.8K	2.2K	
R20	6.8K	5.4K	8.2K	
R21	6Ω	5Ω	9Ω	
R22	39K	31K	47K	
R23	39K	31K	47K	

4.4 ASSEMBLY

The assembly procedure for the converter is shown in Table V. The assembly drawing is shown in Figure 6. The open view of a completed assembly is given in Figure 7(A), which is contained within the metal-lid flat package shown in Figure 7(B). Chip capacitors and chip resistors are attached to the substrate utilizing DuPont 5504A silver epoxy. This material requires a curing cycle of ten minutes at 65°C followed by sixty minutes at 125°C.

Packaged components such as transistors, diodes and integrated circuits are attached to the substrate by bonding with Dow Corning 3140 RTV silicone compound. This material cures in about 30 minutes at room temperature. This material is also utilized to bond the substrate to the package.

Wire interconnections from components to substrate, from substrate to package pins, and from one substrate to the other are made by thermocompression bonding with 4 mil gold wire.

Electrical functional tests over the temperature range from -55°C to +125°C were performed after completing the component and substrate attachment and wire conding prior to sealing the package.

4.5 ADJUSTMENT AND TEST

Following the completion of the converter assembly, the final tests were performed. These consisted of initial adjustment and a general overall check followed by a complete microcircuit temperature check. The adjustment and test were conducted in the following sequence:

Functional Check

When the converter units were initially energized, a check was made to determine that the various blocks were functional and that continued testing was merited.

TABLE V. MANUFACTURING FLOW CHART; CONVERTER ASSEMBLY

PROCEDURE	PROCESS
MOI-1-001	Kit per PAL
QOI 4.46	Inspect
MF1-341	Bond Chip Capacitors and Resistors Dupont No. 5504A Silver Epoxy
MF1-080	Adhesive Temperature Cure
MF1-081	Trim Component Leads
MF1-087	Attach Leads to Components
MF1-020	Adhesive Bonding Transistors, Diodes, Integrated Circuits (Dow Corning 3140 RTV)
MF1-080	Adhesive Cure
MF1-087	Attach Leads to Substrate
MF1-291	Lead Bond Inspection
MF1-019	Clean Package
MF1-087	Attach Leads to Package Pins
MF1-020	Adhesive Bonding Substrate to Package (Dow Corning 3140 RTV)
MF1-080	Adhesive Cure
MF1-087	Attach Leads to Package Pins and to Substrate
MF1-291	Inspect Assembly
MF1-	Electrical Functional Test I
MF1-355A	Trim Resistors
MF1-	Electrical Functional Test II
MF1-291	Final Visual Inspection
MF1-344	Seal Package
MF1-112A	Part Identification
MF1-	Electrical Functional Test III
MOI-1-001	Stores

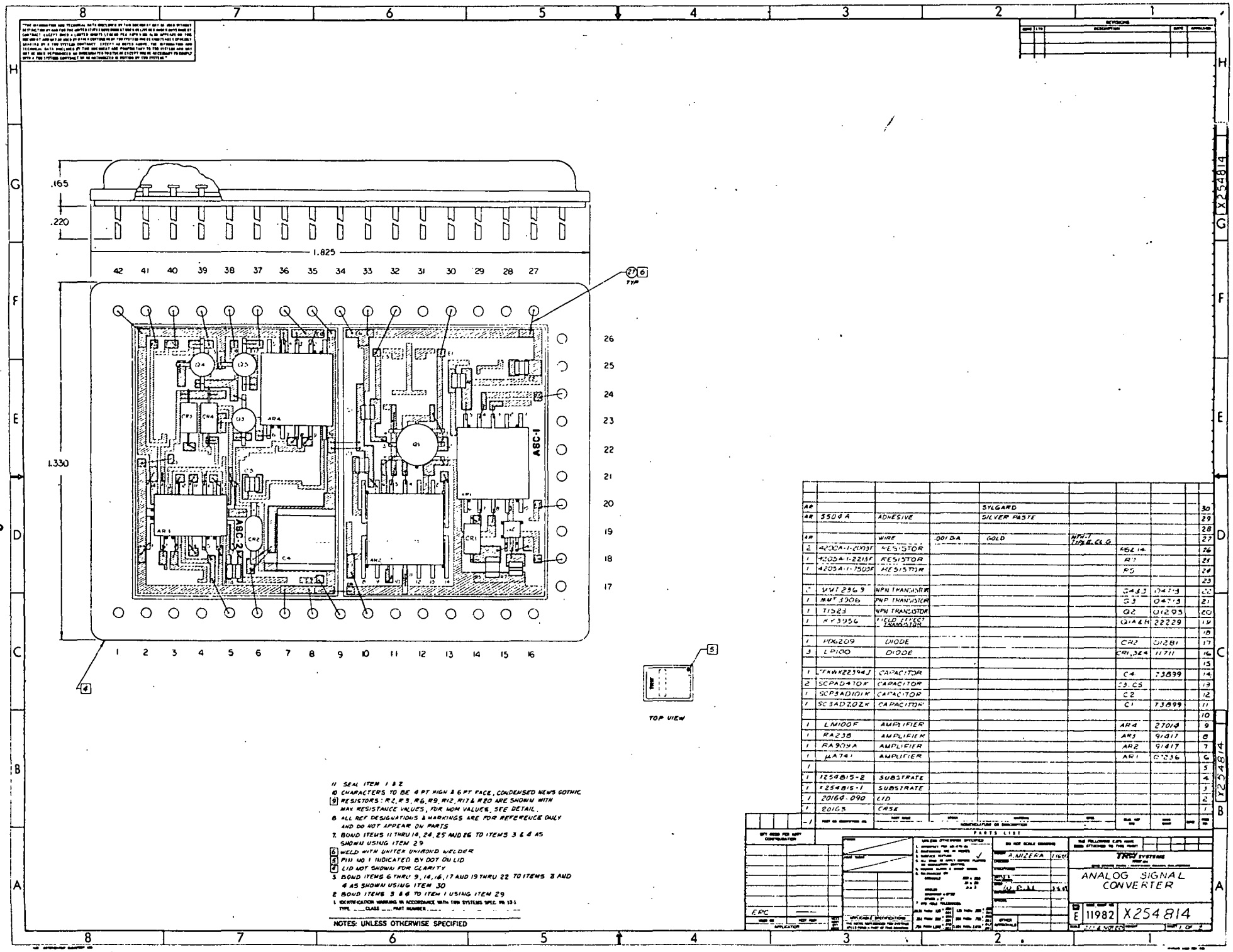


Figure 6 ASDTIC Module ASSembly Drawing.

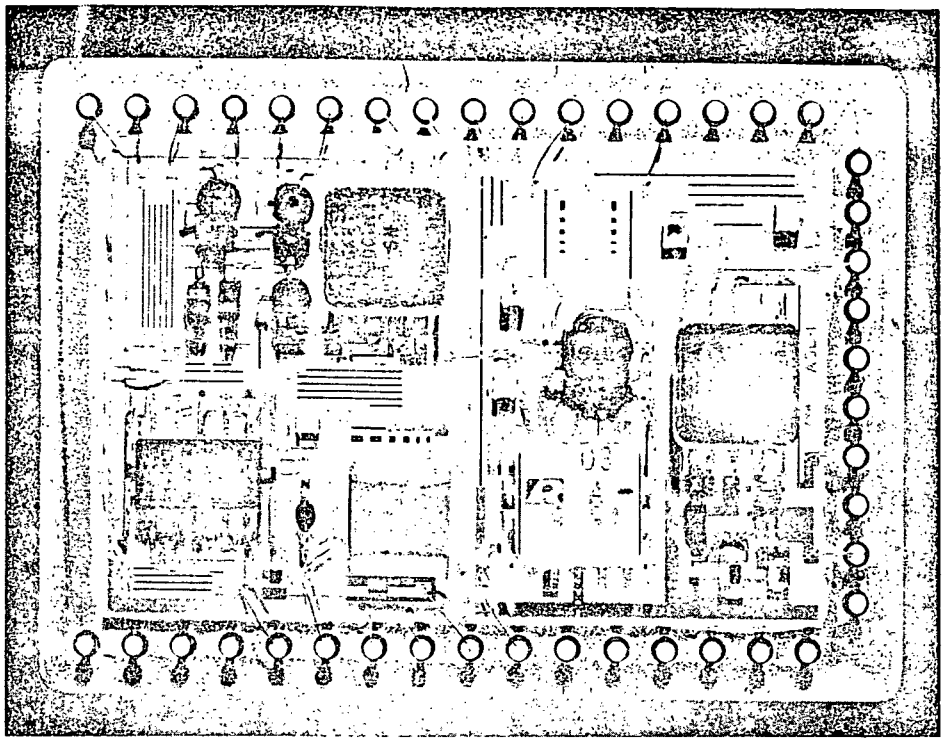


Figure 7(A) Open View of a Complete ASDTIC-Module Assembly

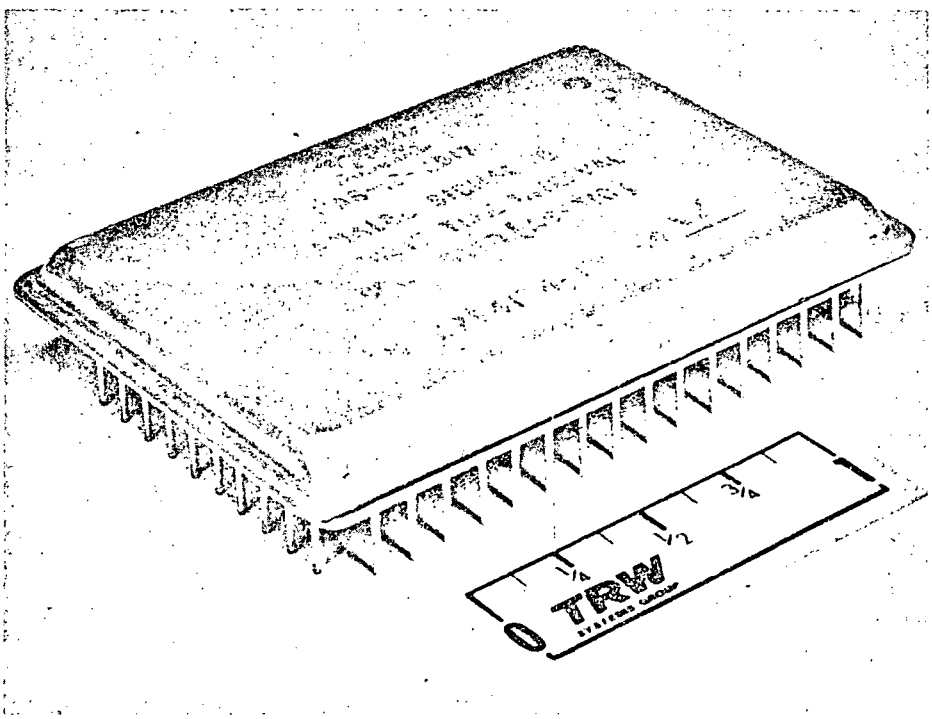


Figure 7(B) ASDTIC Module Enclosed in the Metal-Lid Flat Package.

Series Regulator Trim

The output of the internal voltage regulator was checked. The specification calls for an output level of 20 ±0.4 volts. This adjustment was made by trimming resistor R17 of *Figure 3*. This resistor is initially deposited at 1.8K and always reuslts in a high regulator output voltage. Adjustments to this resistor were made in steps of 50, 100, or 200 ohms by scribing away the gold shorting bars around the increment to be added.

Preliminary Test of Microcircuit Duty Cycle Control

This test was performed by incorporating the microcircuit package into a dc to dc converter power circuit to control the duty cycle of the converter's power switch. The converter power-circuit breadboard will be described later. In the meantime, it suffices to note that a change of less than 1 millivolt at the converter output as a result of an input-voltage variation from 10V to 50V indicated an acceptable ASDTIC module, which would merit a continued testing.

Unity-Gain Amplifier Operation

Proper operation of the unity-gain amplifier was tested by connecting a nominal +7 volt DC level through a 10K resistor to the non-inverting input and checking for a maximum differential of ±5 millivolts between the input and output terminals while the dc input was changed from +6 to +8 volts.

FET Trim

Prior to actual temperature testing of the completed package, source resistors R2 and R3 of the field effect transistor must be balanced for the lowest temperature drift. The system drift is plotted versus temperature and, if necessary, a second adjustment is made for maximum flatness.

Unity-Gain Amplifier Current Limiting

The amplifier is required to operate in a normal manner as long as the input and output are between 6V and 8V. It is also required to provide current limiting in both directions when these limits are exceeded. The positive current limit is 28μA to 50μA and the negative current limit is -28μA to -50μA.

DC Amplifier Drift and Linearity

The drift and linearity of the DC Amplifier are checked over the temperature range by placing a high impedance meter between the amplifier non-inverting input terminal and its output terminal. The differential readings are recorded at discrete input-voltage levels of 6, 7 and 8 volts. Linearity deviations are held to less than 50 micro-volts in the linear operating range. The average temperature coefficient of offset voltage is required to be less than $\pm$5μV/°C over the temperature range. Both of the above measurements are obtained in the same test.

The greater majority of all dc amplifiers tested exhibited the steep increase in the offset voltage from 100°C to 125°C. This is apparently an inherent characteristic of the RM4101-Q operational amplifier.

5. FABRICATION OF PRECISION DC VOLTAGE REFERENCE SOURCE

The requirements of the precision voltage reference source include:

- o Zener Diode Voltage: 6V to 8V
- o Initial Adjustment: 25 ppm resolution
- o Input Current: 2mA maximum
- o Temperature Drift: ±3mV maximum, -55°C to +125°C
- o Input Supply Voltage: 20V ±2%
- o Voltage Drift due to input supply variation: ±1mV maximum
- o Output Impedance: 100K or less

The circuit developed to meet the requirements is shown in Figure 8. Precision reference diode CR3 is used to keep a constant potential across R3 and generates a current of approximately 250 microamperes. Transistor Q2B is connected as a diode and compensates for the temperature variations of the V_{BE} of Q2A. Except for small temperature tracking variations, the CR3 voltage is across R3. The collector circuit of Q2A is a high-impedance current source and CR1 is a precision reference diode. In a manner similar to that described for Q2, Q1A is a diode and compensates largely for the temperature variations of Q1B, thus placing the CR1 potential effectively across R4. The choice of the value for R4 determines the value of the constant current generated by Q1B. In the final design, the values of both R4 and R7 were able to be selected at final functional test. In this manner, variations on the initial values of CR1 and CR3 can be minimized in their effect on the CR3 current value and on the current into the load connected across CR3.

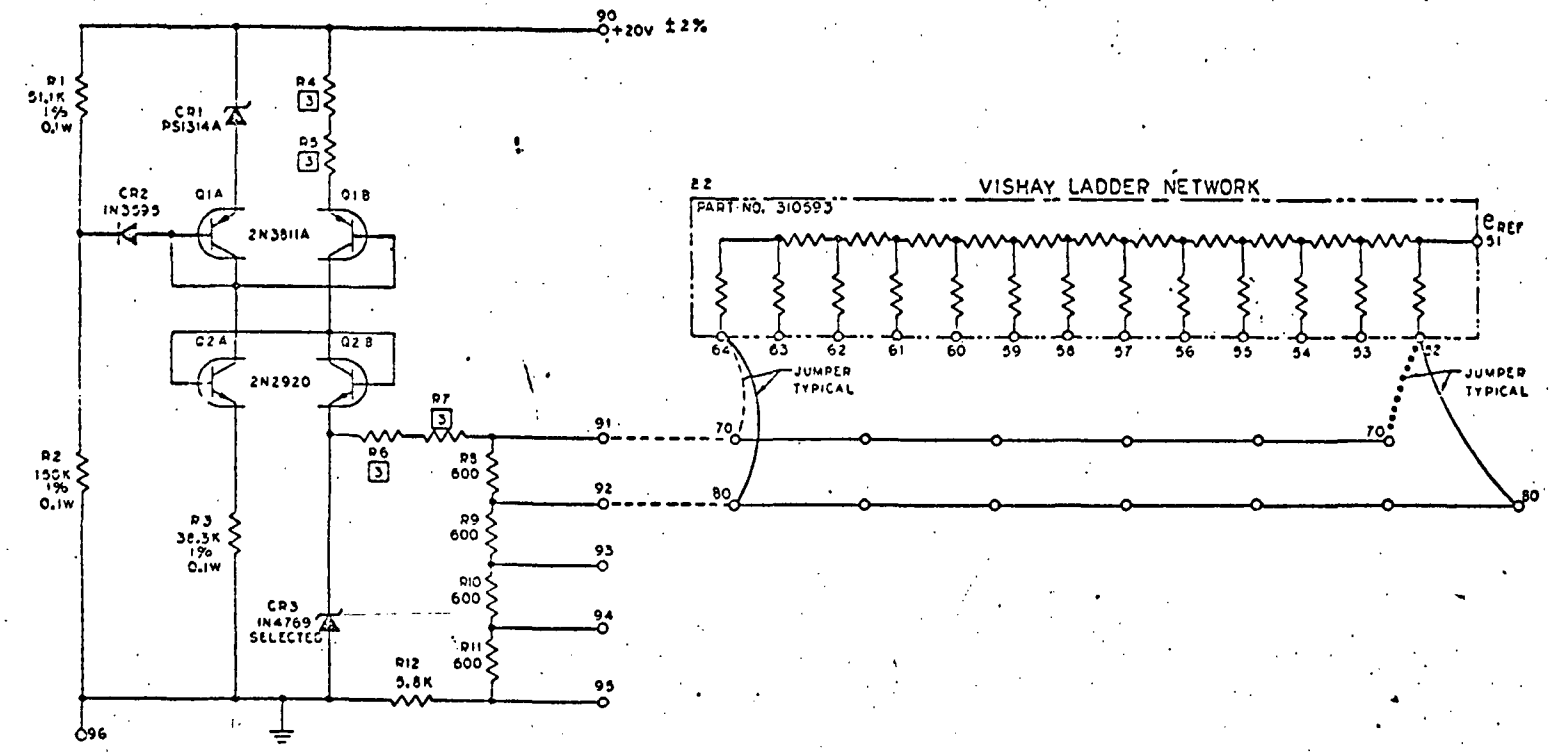


Figure 9. Schematic Diagram, Variable Precision DC Voltage Reference Source

The complete reference is a loop type double current reference with each part controlling the current in the adjacent loop. The normal currents for reference diodes CR1 and CR3 are 250 microamperes and 500 microamperes respectively. The values of R4 to R7 are chosen so that the proper current will flow into CR3 and that, with the expected variation in the normal value of CR3, the 6 volt to 8 volt range can be realized across the four 600-ohm resistor taps connected across CR3. The typical emitter current in Q1 is 1.5 milliamperes.

The precision 9.1 volt reference diode CR3 is a selected version of 1N3769A, providing for a tolerance of 0.0001% per °C.

All resistor values except those of R1 to R3 are critical, and are procured to a temperature tracking tolerance of 1 ppm/°C. Diode CR1 is an off-the-shelf unit specified at a current of 250 microamperes. Resistors R1 and R2 provide a base current path for Q1B under initial start-up conditions. After start-up, diode CR2 is back biased by the resistor divider to prevent current loss from the main circuit. Diode CR2 has a maximum reverse current specification of 0.3 microamperes at +125°C and at 30V. Both Q1 and Q2 are extremely close matched linear devices with very high current gains.

Four 600 ohm resistors are provided across the output reference diode CR3. The ladder network previously described may be placed across any combination of these resistors. Approximately 600 millivolts appear across each of these resistors and the ladder network will provide for a resolution of $600/2^{12}$ = 0.15 millivolts. A ladder network was chosen over a potentiometer due to the difficulty in obtaining a mechanical potentiometer with an adequate temperature tracking capability.

An ECAP analysis was performed to determine the worst-case variation of the output voltage caused by parameter variations due to temperature. The detailed analysis is presented in Appendix 9.2.

Analytical results indicate that the worst-case output-voltage variation is ±4.276mV. The corresponding 3σ standard-deviation calculation result is ±1.427mV.

The precision voltage reference source is contained on one-half of a single-sided printed circuit card. The card measures 8.255 x 14.605CM (3.25 x 5.75 inches). The ASDTIC package is mounted on the remainder of the card. To maintain maximum flexibility, the two halves are not connected electrically. During manual operation, the precision reference is powered from the ASDTIC package by connecting the appropriate terminals. Other jumpers connect the ground, output and ladder network bits to the proper points. The complete assembly for the entire printed circuit card is shown in Figure 9.

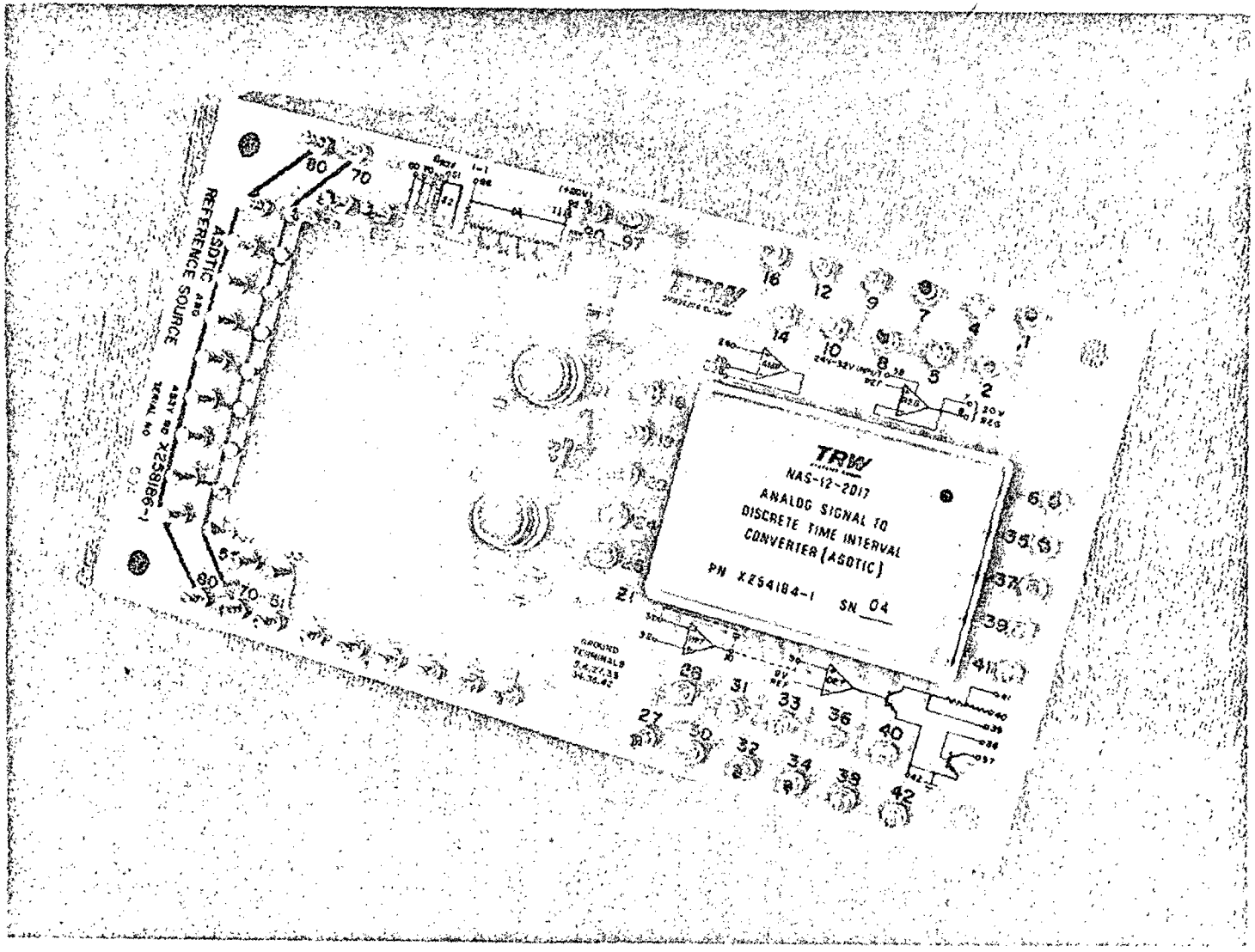


Figure 9 Printed Circuit Board (3.25 by 5.75 inches) Containing Variable Precision DC Voltage Reference Source and ASDTIC Module.

6. THE MICRO-CIRCUIT ASDTIC MODULE APPLIED TO CONTROL A TEST CIRCUIT SWITCHING REGULATOR

The basic objective of the Analog Signal to Discrete Time Interval Converter (ASDTIC) program was to devise a microminiaturized electronic network for controlling an electronic power switch operating in an on-off mode, thus controlling the average value of a train of voltage pulses. Described in this section is the application of ASDTIC control to a switching regulator which demonstrates the utility of the fabricated ASDTIC module through the accomplished precision regulation of the converter output voltage.

In this section, the ASDTIC-controlled dc to dc converter block diagram and the corresponding schematics are identified. Test data of the converter system was obtained to substantiate the high performances facilitated by the ASDTIC control.

6.1 CONVERTER TEST CIRCUIT BLOCK DIAGRAM

Enclosed in the dashed line of the converter system block diagram shown in Figure 10 is the ASDTIC module micro-circuit previously described. Those blocks external to the dashed line work in unison with the ASDTIC module to establish the performance capability of the converter system in terms of the output-voltage regulation. The circuits and components involved with these blocks external to the ASDTIC module are classified herein as the peripheral circuitry.

The circuitry includes a precision dc reference source, pulse generator, integrating capacitor C_{int}, transistor switch, current limiting resistor R_s, and output voltage divider resistors R1 and R2.

The overall operation of the converter is briefly described:

(1) A supply voltage E_s is alternately switched to the output or to ground to produce a squarewave pulse train having an average V_o closely controlled to a desired value.

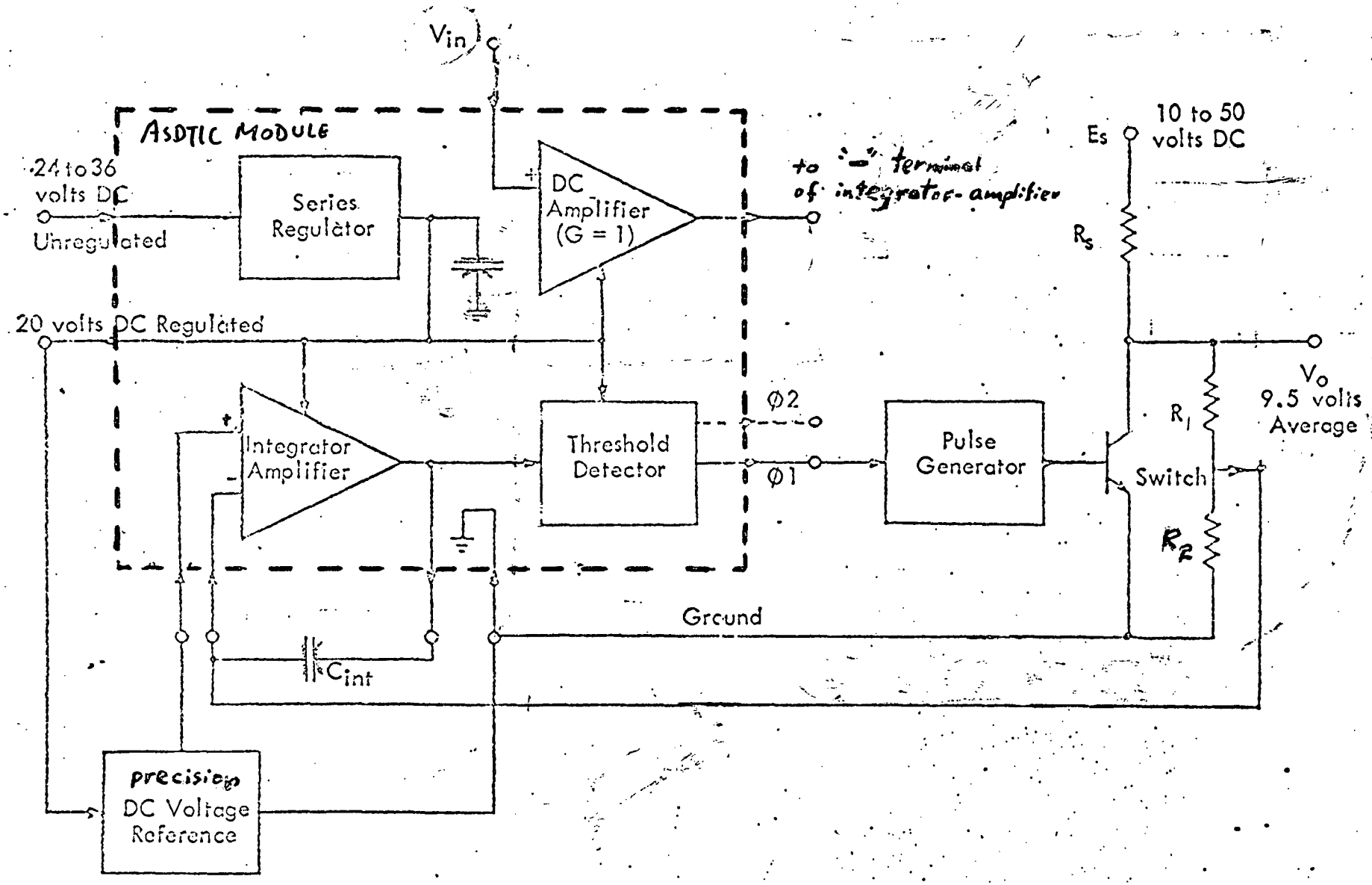


Figure 10 Block Diagram, Analog Signal to Discrete Time Interval Converter System

(2) The squarewave output is divided down, fed to an integrator, and compared with an adjustable precision reference voltage. The difference is amplified and integrated.

(3) The output of the integrator is monitored by the threshold detector, producing a binary output.

(4) The control loop is completed by the pulse generator which receives its input from the threshold detector. The output from the pulse generator controls the output switch. The pulse generator produces a constant pulsewidth signal or a variable pulsewidth signal to drive the base of the power switch. When the pulse is terminated, the pulse generator will wait for a controlled amount of time as determined by the ASDTIC before being retriggered to generate a succeeding pulse.

Depending on how the pulse generator is mechanized, the power switch duty cycle control can be accomplished through either a constant or a variable pulse repetition frequency to maintain an average regulated voltage V_o.

It is noted that the objective of the test converter is for demonstrating the performances of the microcircuit ASDTIC module. The power-circuit optimum design related to quantities such as converter efficiency and output ripple, although important elsewhere, are not the focal points of concern here. Consequently, dissipative types of current limiting and filtering are used to achieve power-circuit simplicity.

6.2 Converter System Requirements

The converter system specification requirements were the following:

Average Input Voltage:	9.5V
Input Voltage:	10V to 50V for constant frequency system
	10V to 30V for variable-frequency system
Regulation:	$\pm$0.1%
Ambient Temperature:	-55°C to +125°C
Pulse Repetition Frequency:	2, 5, 10, 20 and 50KHz
Integrator-Amplifier Input Average Error:	Less than 1mV

6.3 CONVERTER SYSTEM ERROR ANALYSIS

Sources of error influencing the system regulation performance are analyzed. Table VI shows the breakdown of typical and worst-case errors for different circuit component parts due to temperature and input voltage changes. These errors are described categorically as the following.

Zener Diode Reference

A reference error is generated by the temperature coefficient of the zener diode, the variation of input voltage to the reference circuit (to a small degree), and by variations in the zener diode current. The change in operating current is held to a very low value by using a current source to supply the reference diode.

Reference Voltage Adjustment

The voltage adjustment is made by changing taps on a ladder network. Resistors in the ladder network track to an accuracy of 0.5 parts per million per degree centigrade.

Output Voltage Divider

The error caused by the output voltage divider is due to temperature tracking variations of the resistors. Resistors are matched for a tracking accuracy of 0.5 parts per million per degree centigrade.

Integrating Amplifier

The integrating amplifier has five sources of error:

(1) Input offset voltage temperature coefficient
(2) Input offset current temperature coefficient
(3) Amplifier dc gain change with temperature
(4) Leakage resistance of integrating capacitor
(5) AC gain.

The offset errors are maintained low by procuring units with low specified offset voltages and by using a matched pair of FET's preceding the amplifier, as described in Section 3. The integrating amplifier uses stable thin-film resistors in place of the more common diffused resistors. The dc gain is therefore less of a temperature variant. High quality, low leakage mica capacitors are used for amplifier feedback. The ac gain determines the accuracy of the pulse train integration as well as the line regulation due to input voltage change.

Threshold Detector

The threshold detector errors are its offset current and voltage variations with temperature. These errors are reduced by the integrator-amplifier gain. When reflected back to the input of the integrator, these errors become extremely small.

TABLE VI. SUMMARY OF REGULATION ERRORS

ITEM	Reflected to input of Integrator at 7 Volts	
	Typical mV*	Worst mV*
ZENER DIODE REFERENCE		
a. Temperature coefficient	± 1.8	± 4.0
b. Input voltage variation (dynamic resistance) Using Current Source	± 0.4	± 0.8
REFERENCE VOLTAGE DIVIDER		
a. Tracking temperature coefficient of resistors		± 0.3
b. Tracking temperature coefficient of potentiometer		± 0.6
c. Shift of potentiometer wiper	± 0.5	± 0.3
OUTPUT VOLTAGE DIVIDER		
a. Tracking temperature coefficient of resistors		± 0.3
INTEGRATOR		
a. Current and voltage temperature drift	± 1.0	± 1.5
b. Line regulation error	± 0.2	± 0.5
D. C. AMPLIFIER (VOLTAGE FOLLOWER)		
a. Current and voltage temperature drift	± 0.3	± 0.5
TOTAL	± 4.2	± 8.8

*± 0.1% equals ± 7 mV

6.4 PERIPHERAL CIRCUIT SCHEMATICS AND DESCRIPTION

Included in the peripheral circuitry are:

- o Precision dc voltage reference source.

  Voltage reference and constant current source.
  Reference adjustable voltage divider.
- o Output voltage divider, output averaging filter and transistor power switch.
- o Pulse generator
- o Integrating capacitor

The design requirements of each individual circuit are summarized in Table VII.

Precision DC Voltage Reference Source

The design and analysis of the precision dc voltage reference source has been presented in Section 5.

Output-Voltage Divider, Output Averaging Filter, and Transister Power Switch

The output transistor , the output-voltage divider, and the output averaging filter are shown in Figure 11.

Transistor type 2N2369, with a selected voltage rating of 60V and good switching characteristics, is used. The divider resistors are Vishay resistors produced by photo-etching bulk metal film. They are stable resistors with normal temperature coefficient of ±2 ppm/°C. The standard temperature tracking accuracy is ±1.5 ppm/°C.

The output filter averages the output pulse train so that accurate dc voltage measurements can be made. A film resistor was selected for its low temperature coefficient and low inductance. A ceramic capacitor was chosen for its high leakage resistance.

Pulse Generator

The pulse generator shown in Figure 12 is mechanized using a second generation Fairchild TTμL9601 as the timing element. This element may be used as a one-shot or, with feedback and appropriate delay, as an oscillator. The one-shot has an inherent delay of less than 0.05μsec and a pulsewidth or frequency variable by a factor of 10 to 1 without replacing the timing capacitor.

TABLE VII. A SUMMARY OF PERIPHERAL CIRCUIT REQUIREMENTS

Individual Circuits	Design Requirements
Voltage Reference	o Zener diode voltage: 9.1 volts ±5 percent o Zener current: 0.5mA o Voltage drift due to temperature: ±4.5mV maximum o Voltage drift due to input supply variation: ±1mV maximum
Reference Divider	o Maximum input current: 1 milliamp o Output source impedance: 100K or less o Output voltage: Adjustable from 6 to 8 volts with a resolution of ±25 ppm o Output tracking voltage: ±1.2 millivolts allowed
Output Divider	o Input voltage: 9.5 volts o Output voltage: 7 volts o Output source impedance: 100K o Output voltage tracking: ±0.3 millivolts
Pulse Generator	o Fixed output pulse: 19 to 100μsec with a maximum frequency of operation of 50KHz at the 19μsec pulse o Pulsewidth modulated signal: With a fixed frequency of 2, 5, 10, 20 or 50KHz, the duty cycle should be controllable from 0.95 to 0.2. o Input and Output matching: Compatible with threshold detector and power switch.

TABLE VII. A SUMMARY OF PERIPHERAL CIRCUIT REQUIREMENTS
(Cont'd)

Individual Circuits	Design Requirements	
Transistor Switch	o Supply voltage:	10 to 50 volts dc
	o Maximum collector current:	10 milliamps
	o Rise and fall time:	200 nanoseconds maximum
	o Base drive:	Compatible with output of pulse generator
	o Storage time:	Less than 200 nanoseconds
Integrating Capacitor	o Leakage resistance (dc):	100 megohms or greater

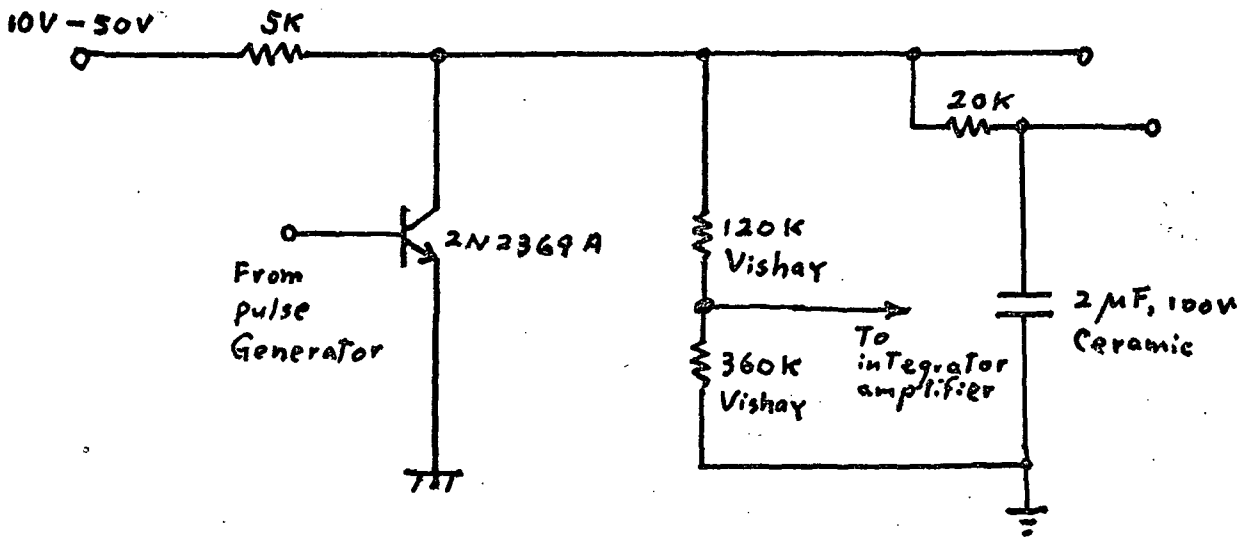


Figure 11. Schematic Diagram of Transistor Power Switch, Output Divider, and Output Filter.

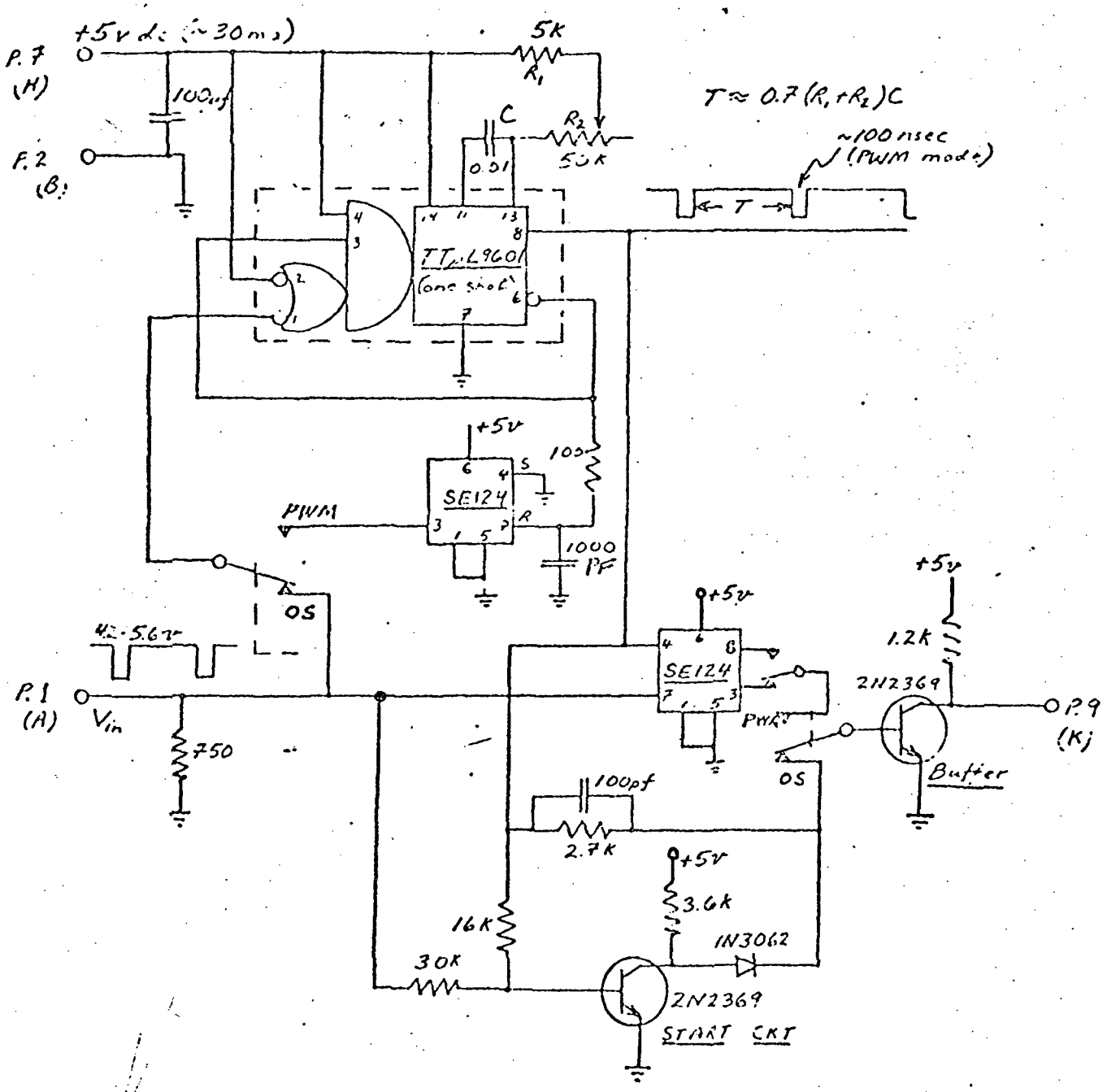


Figure 12 Pulse Generator Schematic, One Shot Pulse Width Modulator

In the one-shot mode, selectable by a toggle switch, the pulse generator is triggered by a low-going signal from the threshold detector, producing a fixed pulsewidth "off" pulse to the transistor power switch.

In the oscillator mode, the pulse generator produces a fixed-frequency variable pulsewidth output. The oscillation is accomplished by feeding the one-shot back to its input to form an oscillator. This sets a control flip-flop with the oscillator, and resets the flip-flop with the threshold detector output. The oscillator (one-shot) output pulse should be sufficiently wide to reliably set the flip-flop and, therefore, a delay of about 0.1μsec is needed. This is accomplished by using an RC network and Signetics SE124 flip-flop as buffer in the oscillator feedback loop.

In the pulse generator configuration shown in Figure 12, the converter operated in the fixed frequency mode is unstable for duty cycles of less than 50 percent. If the threshold detector output is inverted and the oscillator control flip-flop output inverted, the converter becomes unstable for duty cycles of more than 50 percent. The instability observed was explained mathematically, and is presented in Appendix 9.3.

6.5 SWITCHING REGULATOR TEST CIRCUIT PERFORMANCE

As described previously, the ASDTIC microcircuit and the precision dc voltage reference source were placed on a common printed circuit board. A total of ten completed assemblies were made. In conjunction with the other peripheral circuitries presented in Section 5.3, five of the ten boards were tested over the input-voltage and temperature range for regulation performance, with the pulse generator operating in the 95-microsecond constant pulsewidth mode. The typical output variation in ppm versus temperature is shown in Figure 13. The plot shows the output deviation at four constant temperatures as a function of input-voltage. The maximum output-voltage variation shown here is less than ±3 millivolts (±300 ppm) for the combined temperature and input-voltage changes, which is within the overall specification of ±9.5 millivolts. Similar results were obtained for the other four assemblies tested.

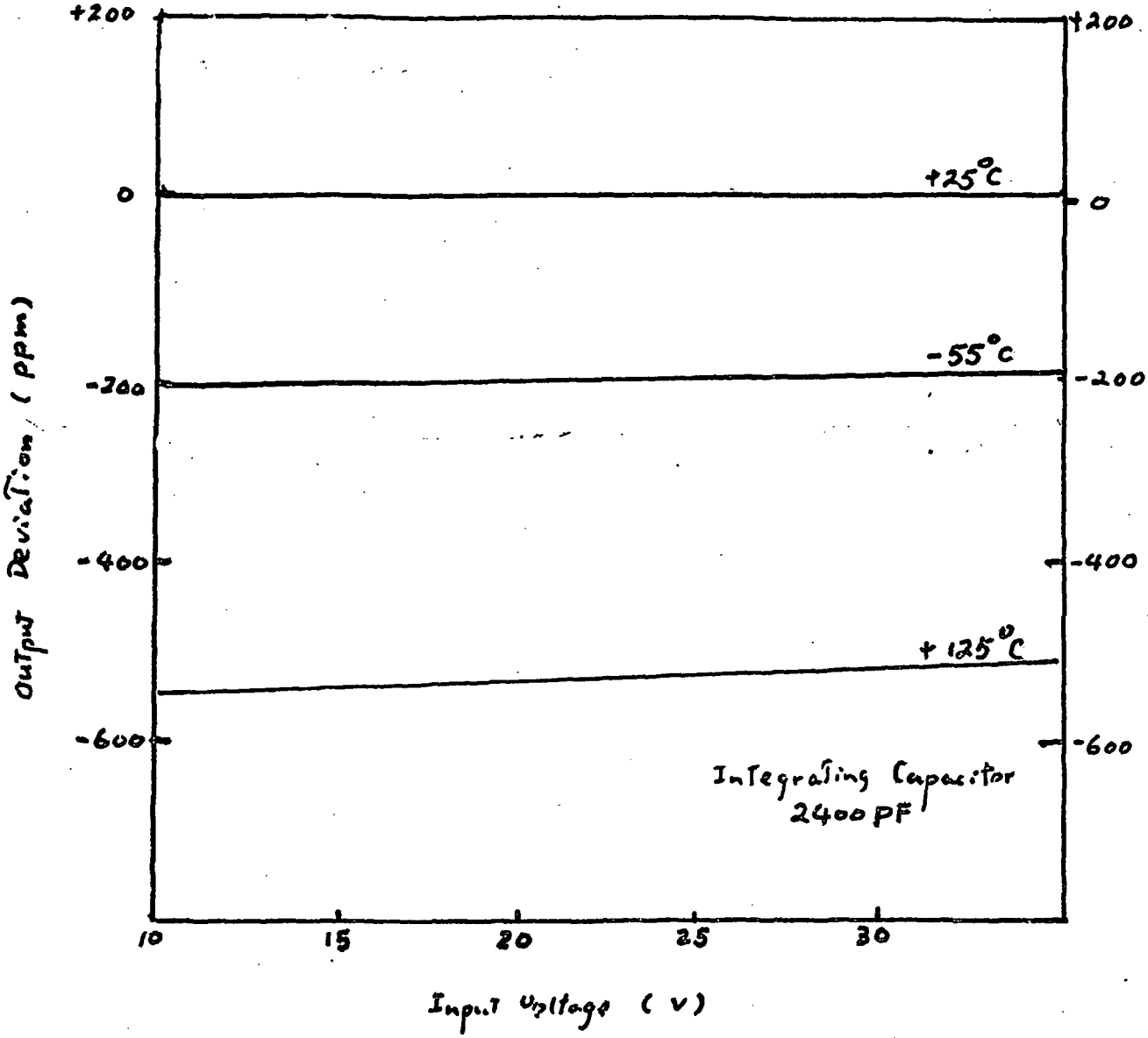


Figure 13 Regulation Performance of Test Converter Using Micro-ASDTIC Module and Precision Voltage Reference.
(Variable Frequency Pulse Generator)
T_{on} = 95 μsec.

7. CONCLUSIONS

The design, development, and microminiaturization of an electronic Analog Signal to Discrete Time Interval Converter was successfully completed in this program. Using the state-of-the-art microcircuit techniques, discrete components and integrated circuits comprising the converter were assembled on thin-film ceramic substrates containing nichrome resistors. All circuits, assembled and tested as a result of this program effort fully met the specified goals for frequency response, stability, temperature drift, and other performance requirements.

A precision adjustable dc reference source was also fabricated. In conjunction with the microminiaturized ASDTIC module, an extremely accurate analog-to-digital signal conversion system was achieved, which is particularly useful for the purpose of regulation through various techniques of pulse modulation. The accuracy was substantiated by the $\pm$0.030% output-voltage regulation of a test switching regulator over a temperature range of -55°C to +125°C.

The microminiaturized control subsystem can be used to program virtually all electronic control functions that are required in a broad class of power converters. The feasibility of microminiaturization, fully demonstrated in this program through the production of the ASDTIC module, has contributed to the size/weight reduction and reliability improvement of high performance, duty-cycle controlled power processing equipment.

8. REFERENCES

[1]. F. C. Schwarz, "Power Processing," NASA SP-244, 1971.

[2]. F. C. Schwarz, "Analog Signal to Discrete Time Interval Converter (ASDTIC)," U. S. Patent 3,659,184, 1972.

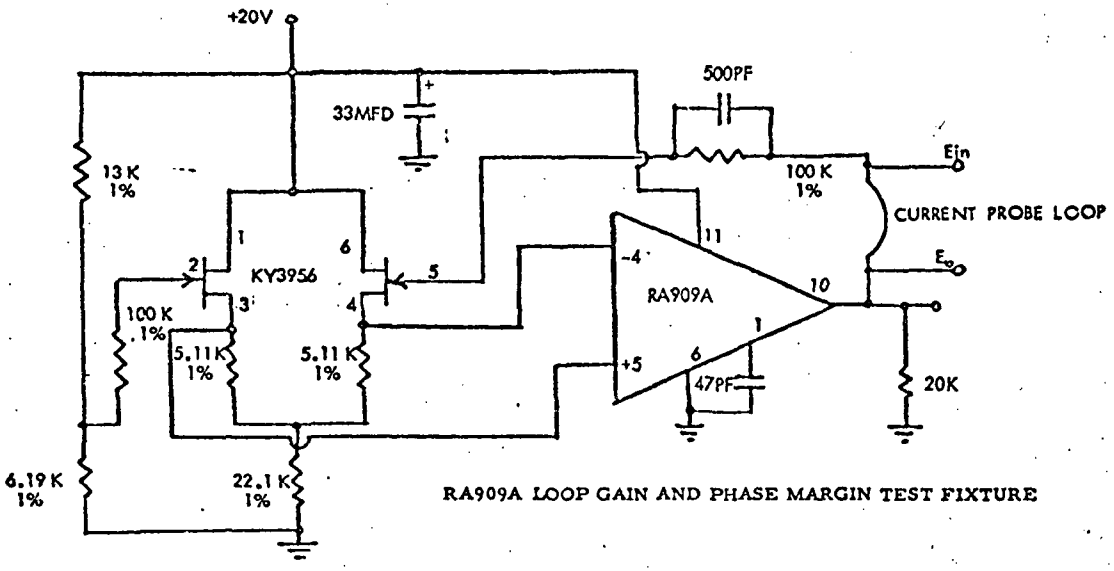
[3]. A. D. Schoenfeld and K. K. Schuegraf, "Design, Development, and Fabrication of a Microminiaturized Electronic Analog Signal to Discrete Time Interval Converter," report prepared by TRW Systems for NASA Electronics Research Center, Contract NAS12-2017.

9. APPENDICES

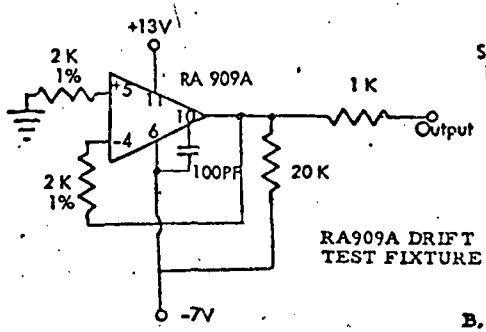
9.1 Test Fixtures and Test Procedures for ASDTIC-Module IC Components

The test fixtures and test procedures used to qualify all IC components prior to their assembly are presented. The components involved are: (1) the RA909A used in the integrator-amplifier, (2) the KY2956 FET pair used in conjunction with the RA909A in the integrator-amplifier, (3) the RA238 used in the threshold detector, (4) the RM4101-Q used in the unity-gain amplifier, and (5) the LM100F used in the series regulator.

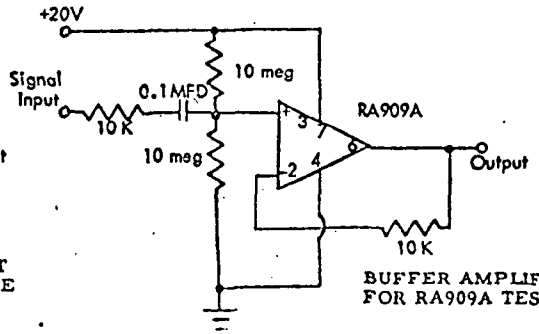
Test results obtained for the integrator-amplifier are presented at the end of this Appendix as examples. For a complete set of test results of all IC components, the reader is referred to Reference [3].



RA909A LOOP GAIN AND PHASE MARGIN TEST FIXTURE



RA909A DRIFT TEST FIXTURE



BUFFER AMPLIFIER FOR RA909A TEST

A. DRIFT TEST

1. Connect the RA909A into the test fixture and apply +13V ±50 MV and -7V ±30 MV.
2. Connect a Fluke DC voltmeter from the output to ground and record the output voltage as a function of temperature from -55°C to +125°C. The +25°C offset should be less than 2.0 mV. Throughout the drift test, the output should be observed with an oscilloscope to insure the circuit does not oscillate.

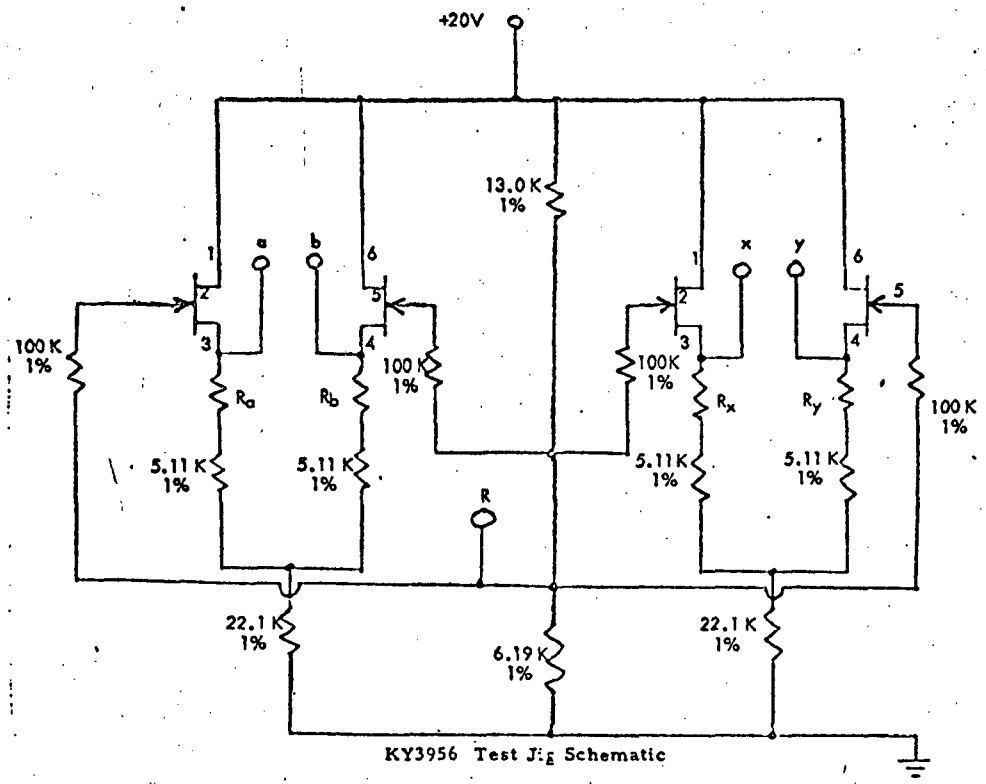
B. LOOP GAIN TEST

Connect the RA909 into the Loop Gain and Phase Margin Test Fixture. Connect a current probe from the output of a HP310A signal generator as shown and record E_{in} and E_{out} with the tuned input of the 310A. Take readings from 10 KHz to the crossover frequency ($E_{in} = E_{out}$) and compute the phase margin.

Caution: Observe the output voltage wave shape to insure the circuit is not overdriven and that distortion is not present.

The buffer amplifier should be used to isolate the E_{in} and E_{out} points from the relatively low impedance of the HP310A tuned input.

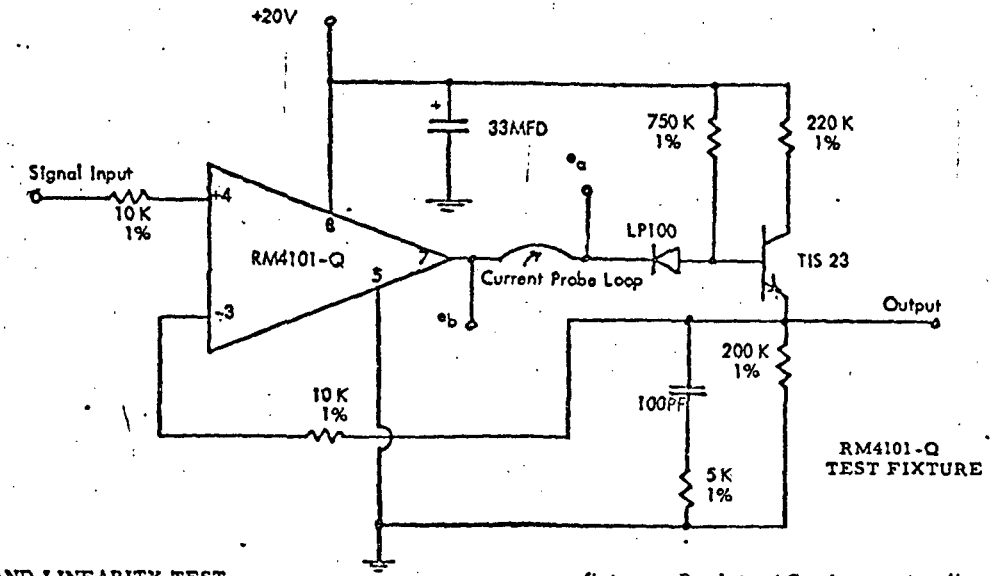
Figure 14. Test Procedure, RA909A Integrated Circuit Amplifier



KY3956 Test Jig Schematic

1. Place the KY3956 FET in the test fixture with Ra = Rb = Rx = Ry = 0 and apply +20V to the fixture. Monitor the supply level to assure it remains constant throughout the run.
2. Using a Fluke meter, record the voltages E_{ab} and R_{xy}.
3. Record E_{aR} and E_{xR} and the voltage from R to ground.
4. With the test fixture in a temperature chamber, change the temperature from +25°C to +125°C and record the voltages E_{ab}, E_{xy}.
5. If a change of 2 mV or greater is observed, change the appropriate resistor (Ra, Rb, Rx, Ry) and repeat the run.
6. When Step 5 is complete, vary the chamber temperature from -55°C to +125 and record E_{ab} and E_{xy} for -55°C, -30°C, 0°C, +25°C, +75°C, +100°C, and +125°C.

Figure 15. Test Procedure, KY3956 Field Effect Transistor Pair

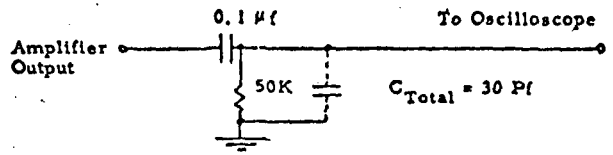


A. DRIFT TEST AND LINEARITY TEST

1. Connect the circuit into the test fixture, apply +20 volts to the power supply inputs and +7 volts to the signal input.
2. Connect a Cimron Model 7650 or a Fluke Meter from the (+7V) input to the output and record the +25°C offset and the offset voltage (e_{os}) as a function of temperature from -55°C to +125°C. The initial e_{os} at +25 should be less than 5 mV. At each recorded temperature, take readings of e_{os} for input signal voltages of +6 V, +7 V and +8 V.

B. OPEN LOOP GAIN AND PHASE MARGIN TEST

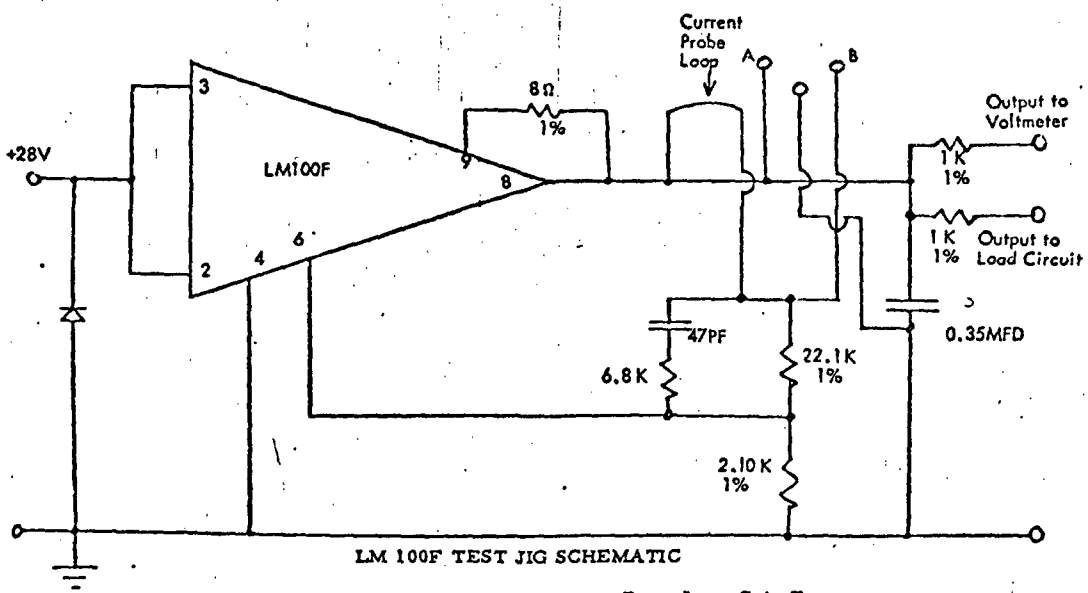
1. Adjust the input signal to +7 V dc and connect a current probe from a HP310A generator to the loop in the test fixture. Read the AC voltages at e_a (input) and e_b (output) through a buffer amplifier into the 310A voltmeter input. Connect a load onto the amplifier output as shown:



When a frequency is reached where $e_a = e_b$, read the voltage e_{ab} for a phase margin calculation.

Caution: Monitor the output across the load for possible oscillation and distortion.

Figure 16. Test Procedure, RM4101-Q Integrated Circuit Amplifier



LM 100F TEST JIG SCHEMATIC

A. DC Regulation

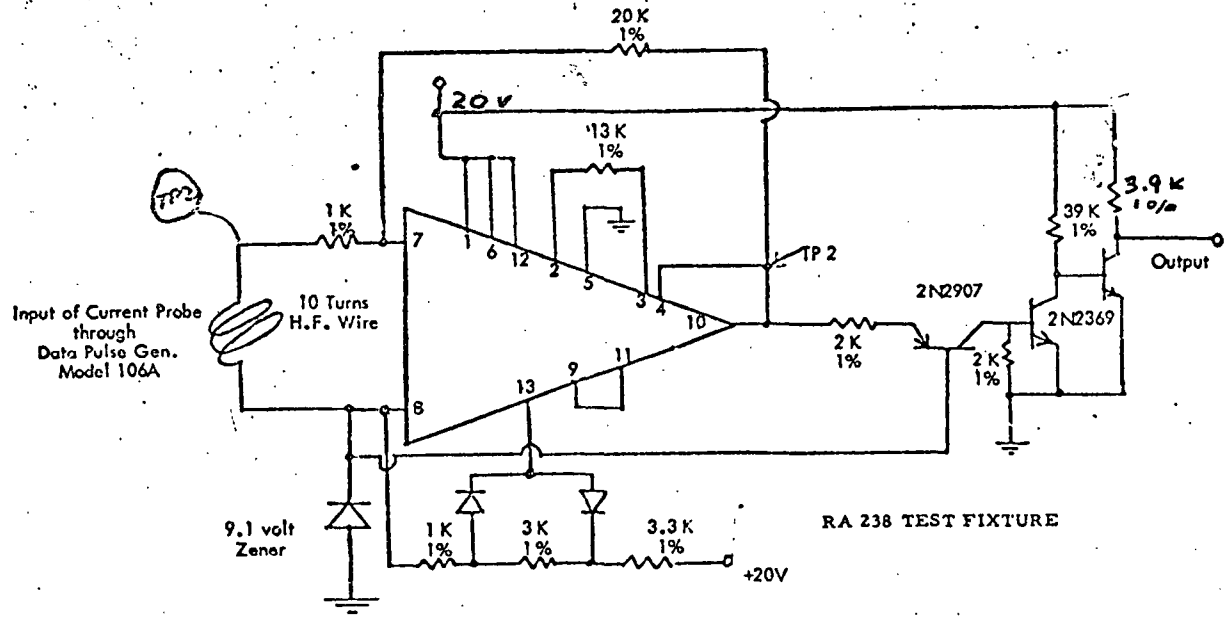
1. Place the LM100F in the test fixture and connect a decade resistance box in series with a milliammeter between one of the output terminals and ground.
2. Connect a DVM or a Fluke meter between the other output and ground.
3. Adjust the input voltage level to +24V.
4. Vary the decade resistance box for load currents of 4 mA, 8 mA and 12 mA; record the output voltage for each current.
5. Repeat Step 4 for input voltages of 28V and 32V and for temperatures of -55°C, +25°C and +125°C.

B. Loop Gain Test

1. Place the LM100F in the test fixture and connect a 1K ohm 1% resistor from one of the outputs to ground. (Note: Load current will be approximately 10 mA.)
2. Using a Hewlett Packard 310A wave analyzer, connect a current probe from the 310A "output" to the loop on the test fixture.
3. Vary the input frequency and read the voltage at "A" and "B" for each frequency with the voltmeter section of the 310A.

   CAUTION: Observe the output waveshape, Point "A", with an oscilloscope to prevent overdrive and distortion.
4. When the voltage at "A" is equal to that at "B", read the voltage from "A" to "B" for a phase margin calculation.

Figure 17. Test Procedure, LM100F Integrated Circuit Voltage Regulator



1. Place the RA238 in the test fixture and turn on the +20V.

2. Connect a current probe from the input of the test fixture to a Model 106A Datapulse Generator or equivalent. Adjust the frequency for 50 KHz and for a 50% duty cycle at TP1. Adjust the rise and fall times to less than 0.1 microseconds and the pulse amplitude to 100 millivolts.

3. The output shall be in phase with the input and will swing between $0^{+.5}_{-0}$ V to +20 $\pm$0.5V. The delay between the positive input transition and 90% of the positive output transition shall be less than 1.5 microseconds from -55°C to +125°C. The delay between the negative input transition and 90% of the negative output transition shall be less than 1.5 microseconds from -55°C to +125°C. The delay between the negative input transition and 90% of the negative output transition shall be less than 2.0 microseconds from -55°C to +125°C.

4. The positive transition time of the output shall be less than 0.3 microseconds between the 10% and 90% points and the negative transition time shall be less than 0.1 microseconds between the 10% and 90% points. The total capacitive load on the output shall be less than 10 pico farad.

Figure 18. Test Procedure, RA 238, Threshold Detector

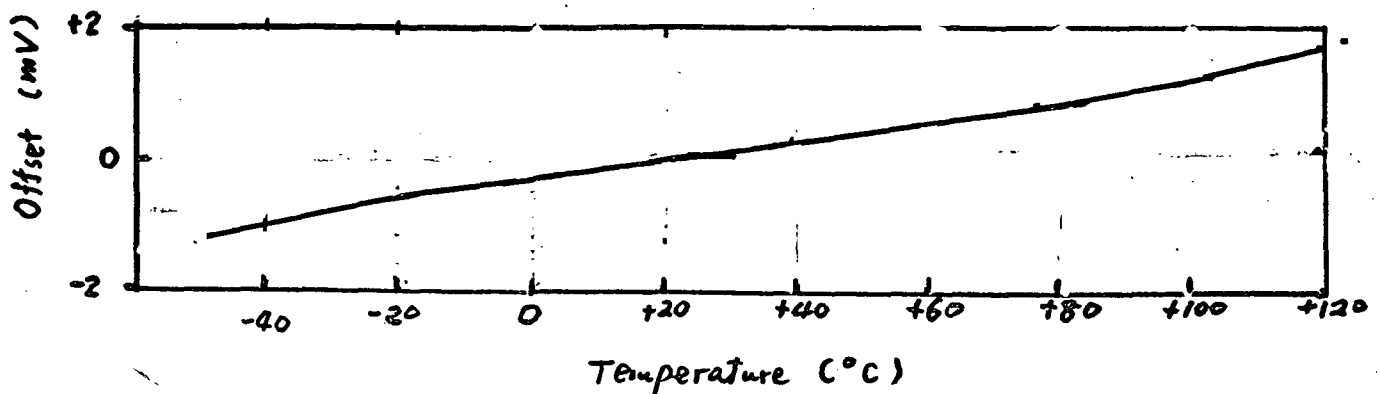


Figure 19. Input Drift of Integrator Amplifier RA909A

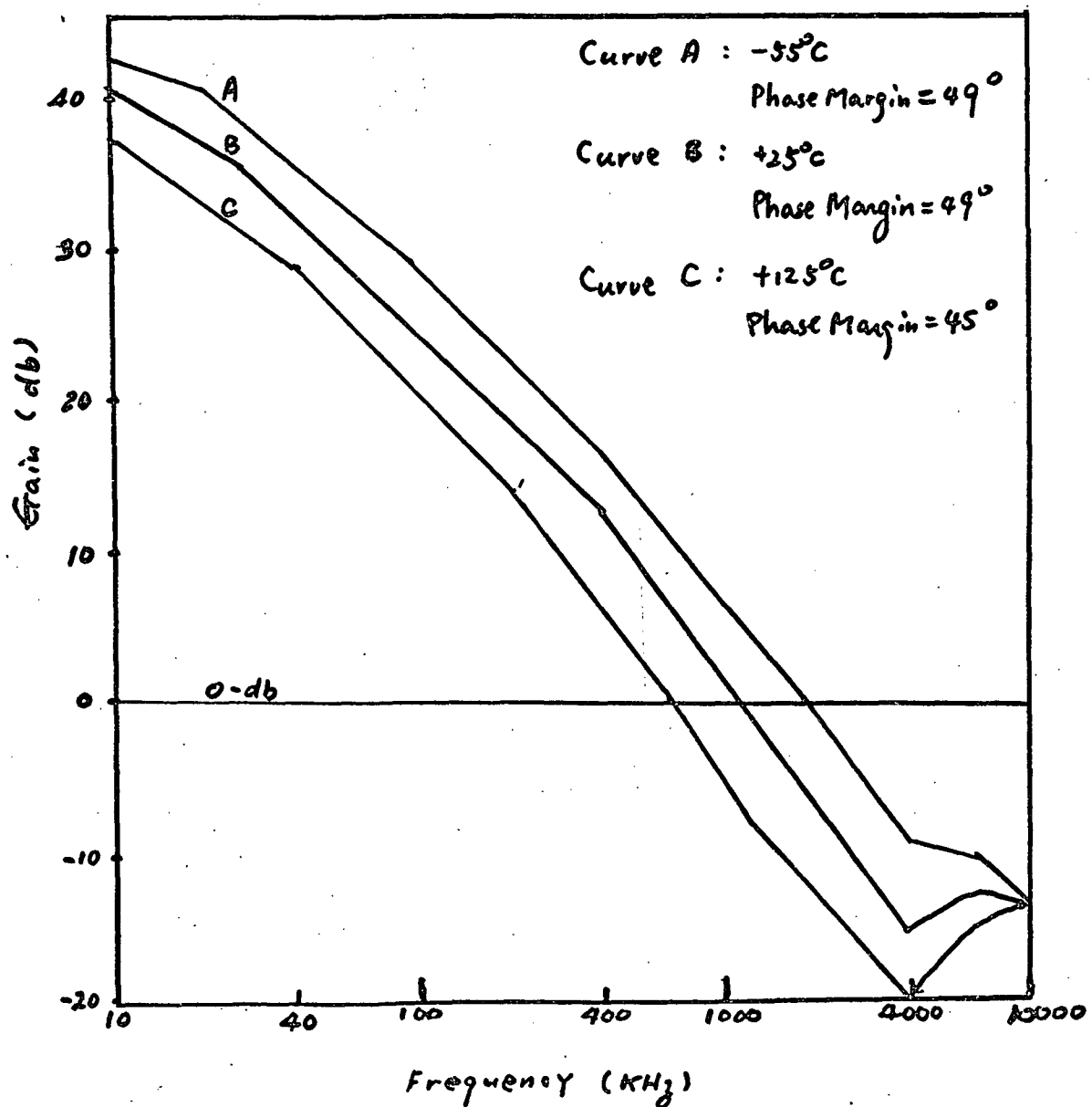


Figure 20. Open Loop Gain of Integrator Amplifier RA909A

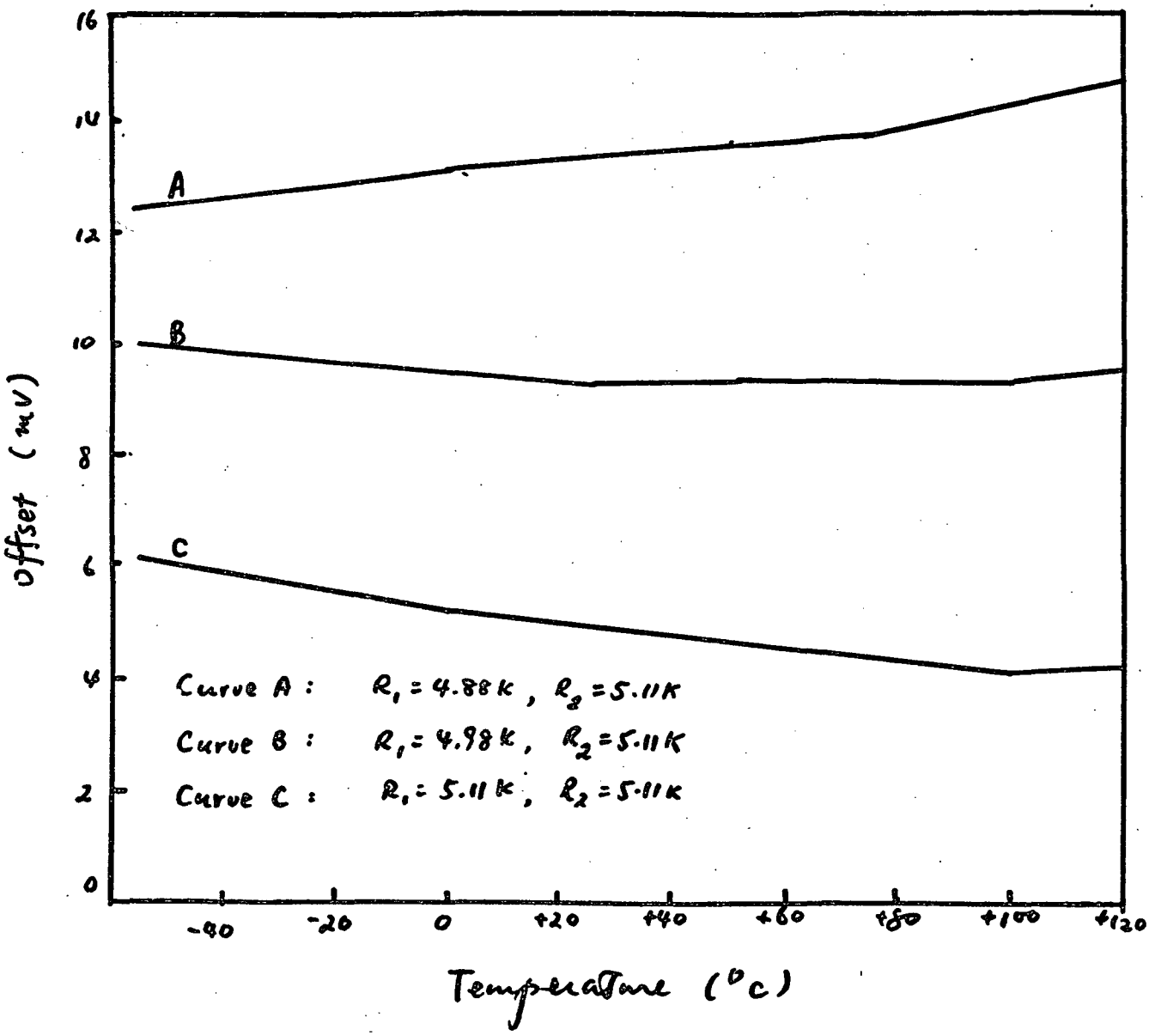


Figure 21 Field Effect Transistor (KY3956) Source Follower Drift

9.2. WORST-CASE VARIATION OF PRECISION REFERENCE VOLTAGE SOURCE

An analysis was performed on the Precision Reference Source to determine the worst case variation of the output voltage with parameter variations due to temperature. The circuit was analyzed with the help of a computer using ECAP (Electronic Circuit Analysis Program).

The circuit to be analyzed is borken down into a set of standard electrical elements which computer program recognizes. Once the input for ECAP is prepared, the statements are entered into the computer. The worst case DC solution is done automatically by the computer when worst case is called out.

In ECAP the worst case maximum and worst case minimum node voltages of a circuit can be calculated. ECAP defines the worst case maximum solution at the kth node of a circuit, as the sum

$$e_k + \sum \frac{\partial e_k}{\partial P_i} \Delta P_i$$

where all the terms

$$\frac{\partial e_k}{\partial P_i} \Delta P_i$$

are positive. Similarly, the worst case minimum solution is obtained when all of the terms are negative. The variable e_k is the nominal value of the node voltage at the kth node, P_i is the nominal value of a parameter in the ith branch, and ΔP_i is the tolerance of the parameter. Thus, in the worst case maximum calculation, positive partial derivatives are multiplied by positive tolerances, and negative partial derivatives by negative tolerances. In the worst case minimum calculation, positive partial derivatives are multiplied by negative tolerances, and negative partial derivatives by positive tolerances.

The standard deviation of the node voltages can be calculated by ECAP for a circuit which contains circuit parameters that can be reasonably assumed to be statistically independent, random, and normally distributed about their nominal values. This calculation is similar to the worst case analysis in that it is based upon the node voltage partial

derivatives. The output of the standard deviation calculation is the nominal node voltage, nominal node voltage minus the standard deviation, and the nominal node voltage plus the standard deviation.

The dc analysis was conducted in three steps: room temperature condition, high temperature condition, and low temperature condition. This was necessary in order to take into account the temperature drift of h_{FE} and diode forward drops.

The computer print-out on the dc analysis program provides the steady-state solutions for voltages and currents, also the partial derivatives and sensitivity coefficients of the network voltages with respect to the input parameters. Both a worst-case analysis and a standard deviation analysis of the network voltages are provided.

The schematic for the circuit to be analyzed has been shown in Figure 8. From it, an equivalent circuit suitable for solution by ECAP is generated and is shown in Figure 22.

The input voltage variation was specified as ±2%. The component parameter variations due to a temperature range of -55°C to +125°C were obtained from the manufacturer's data sheets, and are as follows:

1N4796A Zener	$\frac{\Delta V}{V} = \pm 0.00018$
Ladder Network	$\frac{\Delta R}{R} = \pm 0.00009$
Differential Amplifier Transistors	$\Delta \frac{h_{FE1}}{h_{FE2}} = \pm 0.075$
Vishay Resistors	$\frac{\Delta R}{R} = \pm 0.00027$
1% Resistors	$\frac{\Delta R}{R} = \pm 0.009$
PS1314A Zener	$\frac{\Delta V}{V} = \pm 0.0009$

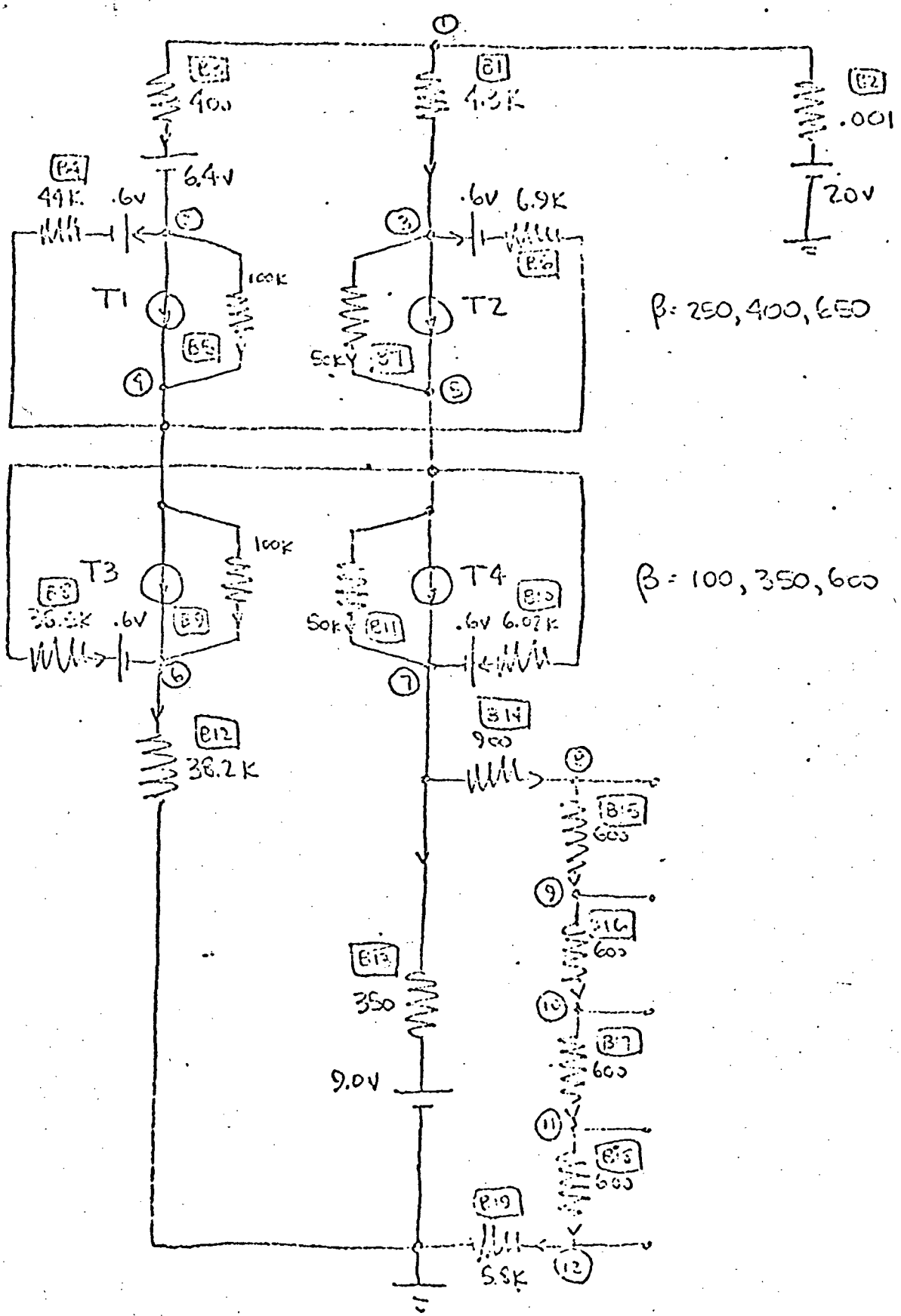


Figure 22 Equivalent Circuit of Precision Reference Source for Computer Analysis

Based on these parameter variations, a sample ECAP program, calculating the worst-case reference voltage change over the 180°C temperature range, is shown in Figure 23 . Represented by the voltage at node #8, the reference voltage is found analytically to vary between the following worst-case limit and standard deviation:

	Lowest	Nominal	Highest
Worst-Case Limit (V)	8.2621658	8.2669898	8.2707166
Standard Deviation (V)	8.2652209	8.2669898	8.2680755

Consequently, the worst-case reference change is ±4.276mV, and the standard deviation is ±1.427mV.

TRW SYSTEMS GROUP | PROJECT | PAGE

SUBJECT: Precision Reference Source | PREPARED BY | DATE

```
C       PRECISION REFERENCE SOURCE
C       6-19-69
C
        DC ANALYSIS
C
B1      N(1,3), R=4.3E3(.00027)
B2      N(0,1), R=.001, E=20(.02)
B3      N(1,2), R=400, E=-6.4(.0009)
B4      N(2,4), R=44E3, E=-0.6(.005)
B5      N(2,4), R=100E3
B6      N(3,4), R=6.9E3, E=-0.6(.005)
B7      N(3,5), R=50E3
B8      N(5,6), R=38.5E3, E=-0.6(.005)
B9      N(4,6), R=100E3
B10     N(5,7), R=4.02E3, E=-0.6(.005)
B11     N(5,7), R=50E3
B12     N(6,0), R=38.2E3(.009)
B13     N(7,0), R=350, E=-9.0(.00018)
B14     N(7,8), R=900(.00027)
B15     N(8,9), R=600(.00027)
B16     N(9,10), R=600(.00027)
B17     N(10,11), R=600(.00027)
B18     N(11,12), R=600(.00027)
B19     N(12,0), R=5.8E3(.00027)
T1      B(4,5), BETA=400(.075)
T2      B(6,7), BETA=400(.075)
T3      B(8,9), BETA=350(.075)
T4      B(10,11), BETA=350(.075)
        W8,8,9,10,11,12
        PRINT,VV,BA,W3
        EXECUTE
```

Figure 23. Computer Analysis Input Data

9.3. SERIES SWITCHING REGULATOR INSTABILITY RELATED TO CONSTANT-FREQUENCY ASDTIC DUTY-CYCLE CONTROL

When ASDTIC control was applied to regulate the test converter described in Section 5.3 of this report, it was observed that the converter became unstable for duty cycles less than 50 percent when the converter was operated with a fixed switching frequency. This instability us mathematically explained as the following.

The test converter block diagram is shown in Figure 24A. The unidirectional voltage pulse at point A is compared with a reference voltage E_R. The reference voltage divides the voltage pulses into two equal shaded areas shown in Figure 24B. These areas are integrated by the integrator-amplifier to form a triangular waveform at point B of Figure 24 A. Corresponding to Figure 24B, the triangular waveform is shown in Figure 24 C.

Thus the transistor is turned on for a time interval T_{on} within a fixed period T. During the interval T_{on}, the slope of the triangular output waveform in Figure 24C is $(E_i - E_R)/RC$, where RC is the time constant of the integrator. The average value of the rectangular voltage e_A and the triangular voltage e_B is therefore

$$\bar{e}_A = E_R$$

$$\bar{e}_B = E_T - \frac{(E_i - E_R)T_{on}}{2RC}$$

Since

$$E_i T_{on} = E_R T$$

Combining these three equations gives:

$$\bar{e}_B = E_T - \frac{T}{2RCE_i}(E_i - \bar{e}_A)\bar{e}_A$$

Differentiating $\bar{e}_B$ with respect to $\bar{e}_A$ for a given E_i and a fixed T yields

$$\frac{d\bar{e}_B}{d\bar{e}_A} = -\frac{T}{2RCE_i}(E_i - 2\bar{e}_A)$$

$$= -\frac{T}{2RC}\left(1 - \frac{2T_{on}}{T}\right)$$

Consequently, the small-signal gain from point B of Figure 24A, tracing clockwise to point A, becomes

$$[Gain]_{B\,to\,A} = \left(\frac{d\bar{e}_B}{d\bar{e}_A}\right)^{-1} = \frac{-2RC}{1 - \frac{2T_{on}}{T}}$$

Therefore,

$$[Gain]_{B\,to\,A} > 0 \quad as \quad \frac{T_{on}}{T} > 0.5$$

$$[Gain]_{B\,to\,A} < 0 \quad as \quad \frac{T_{on}}{T} < 0.5$$

Since there exists a phase inversion associated with the integrator amplifier (i.e., from point A to point B clockwise), a further inversion such as caused by $T_{on}/T < 0.5$ would result in positive feedback, which leads inevitably to system instability. The instability would persist for all duty cycles that are less than 0.5, as was demonstrated by the test converter.

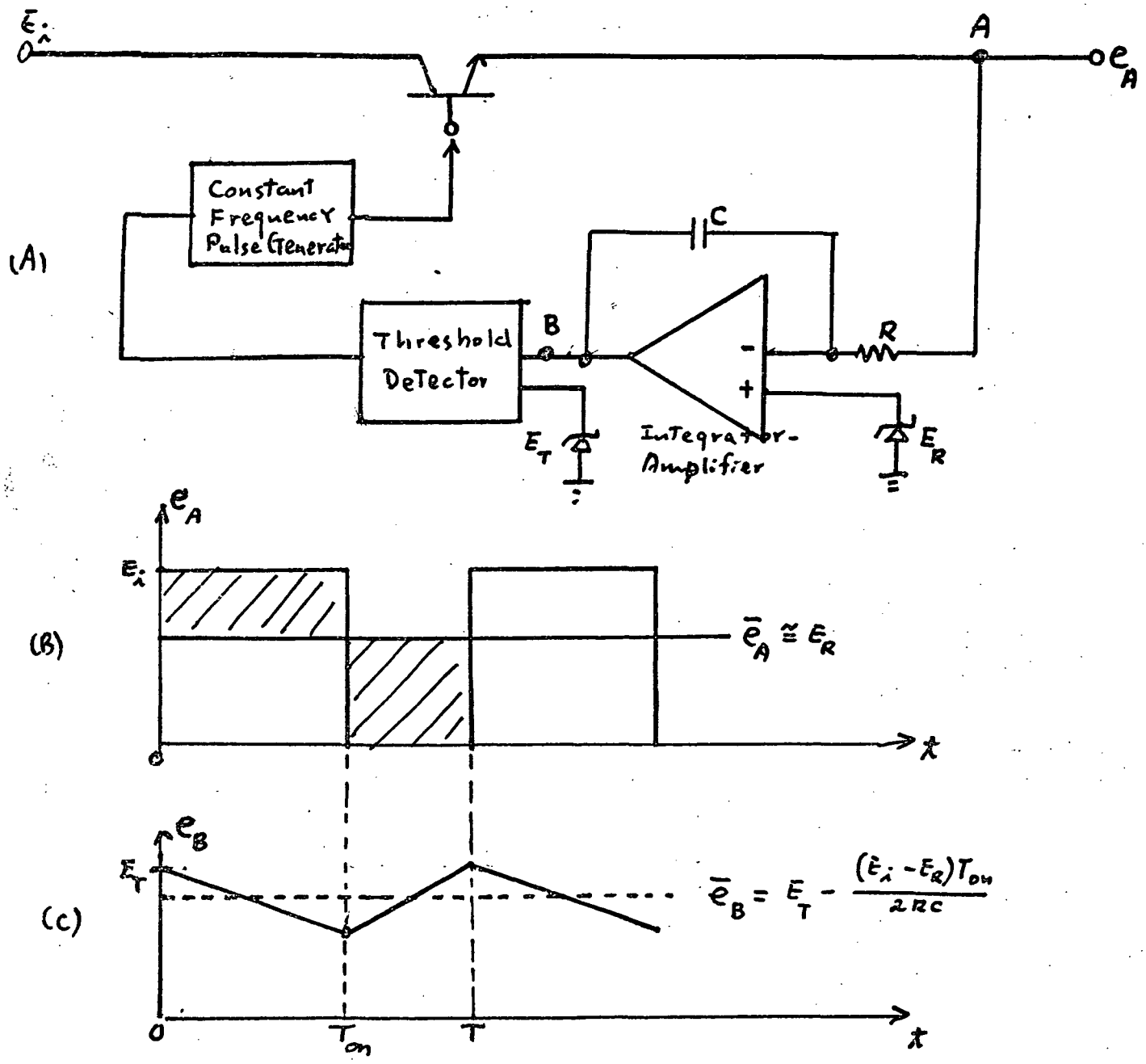


Figure 24 Simplified Test Converter Block Diagram And Its Waveform