PROCESS DEVELOPMENT OF BEAM-LEAD SILICON-GATE COS/MOS INTEGRATED CIRCUITS

Final Report

9 November 1970 to 31 December 1973

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Contract NAS8-26594

Prepared By

RCA, SOLID STATE DIVISION

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ABSTRACT

Two processes for the fabrication of beam-leaded COS/MOS integrated circuits are described. The first process utilizes a composite gate dielectric of 800 Å of silicon dioxide and 450 Å of pyrolytically deposited Al_2O_3 as an impurity barrier. The second process utilizes polysilicon gate metallization over which a sealing layer of 1000 Å of pyrolytic Si_3N_4 is deposited.

The following three beam-lead integrated circuits have been implemented with the first process:

CD4000BL	three-input NOR gate
CD4007BL	triple inverter
CD4013BL	dual D flip flop

An arithmetic and logic unit (ALU) integrated circuit was designed and implemented with the second process. The ALU chip allows addition with four bit accuracy. Processing details, device design and device characterization, circuit performance and life data are presented.

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SECTION I
INTRODUCTION

In order to fabricate reliable COS/MOS integrated-circuit logic and memory chips that can be interconnected on a small substrate to form a variety of subsystems, beam-leaded chips are mandatory. Unfortunately the normal bipolar beam-lead process, whose worth has been proven on life and stress tests over the years, cannot be applied directly to COS/MOS devices. The more severe requirements for the use of the hermetic seal in MOS processing require additional development. In addition, the standard sputtering process used in bipolar device processing introduces charge into the gate oxide which cannot be removed by annealing. Both of these cause the threshold voltages to wander from device to device and to be unstable. For these reasons variations have been introduced from the standard bipolar beam-lead process to solve these problems. The general philosophy guiding such variants, however, is that they be few, and that the process itself be kept as close to the standard beam-lead scheme as possible. It is hoped that by following such a procedure, the long-term documented bipolar life-test data may be applicable to COS/MOS beam-lead devices.

The work was performed in two phases. Section II of this report covers the work with conventional non-self-aligned metal gates over a composite gate dielectric of SiO_2:Al_2O_3. The aluminum oxide layer is used for sealing the critical gate dielectric from sodium penetration. Section III of this report covers the work with self-aligned polysilicon gates that are sealed by a much heavier layer of silicon nitride. In both cases an identical metal system for the beam leads has been used that allows deposition by evaporation.

SECTION II

PHASE 1: DEVELOPMENT OF BEAM-LEAD SEALED-JUNCTION PROCESSING TECHNOLOGY FOR COS/MOS CIRCUITS

A. BEAM-LEAD PROCESSING OF COS/MOS CIRCUITS

The beam-lead approach followed in this program differs from the standard bipolar type of beam-lead process in only two particulars:

a. The hermetic seal, Al_2O_3, that is placed between the gate oxide and the metallization must be deposited clean. Any deviation of the flatband voltage of the deposit from theory, whether due to interfacial charge, mobile charge, or potential discontinuities, will shift the device thresholds. These shifts must be avoided so that reasonably matched and stable thresholds are obtained. In bipolar beam leading, few or no controls are needed on the silicon nitride.

b. The metallization used is Pd_2Si-Ti-Pd-Ti-Au instead of PtSi-Ti-Pt-Ti-Au. This change is made to avoid the necessity of sputtering which introduces charge and, hence, threshold shifts into the devices. Palladium can be evaporated with standard equipment.

The process being used at RCA to fabricate beam-lead devices is as follows:

a. The IC wafer is processed normally by using the well known standard COS/MOS process until the gate oxide growth step has been completed (topologically depicted in Figure 1).

b. Immediately after the 800 Å SiO_2 film has been grown, the wafer is placed in an aluminum oxide deposition chamber in which a 400 Å film is deposited at 850°C. The deposition time is approximately 4 minutes. The layer acts as the hermetic seal, protecting the devices not only from the environment, but even more importantly from future processing contamination (see Figure 2).

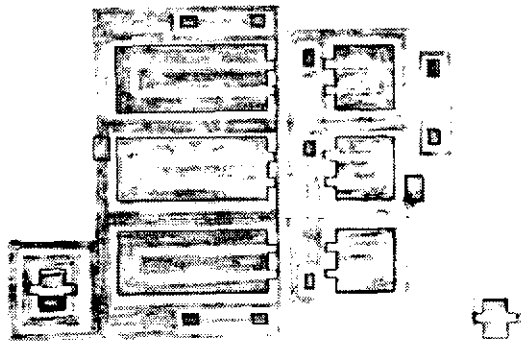

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Figure 1. IC Wafer After Gate-Oxide Growth

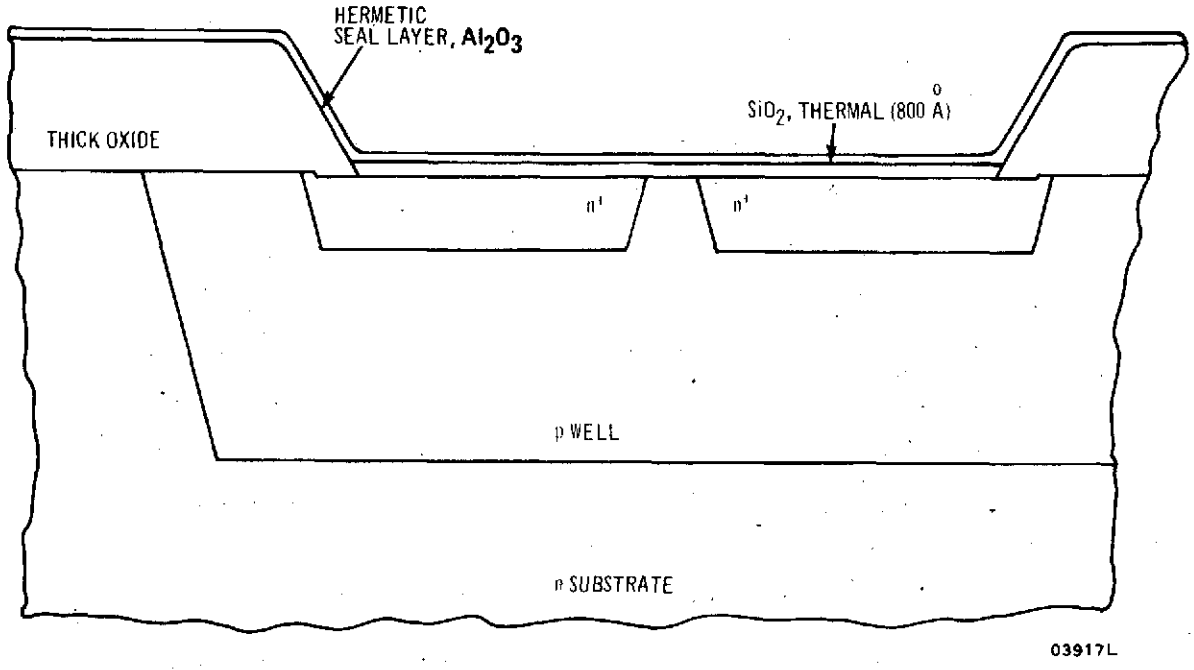

Figure 2. Channel Oxide Grown, and Al_2O_3 Deposited

c. A 3000 Å oxide is deposited over the wafer to act as an etchant mask. Photoresist is applied and contact holes are etched into the oxide mask. The wafer is etched in phosphoric acid, which removes the Al_2O_3 covering. The wafer then is etched with buffer HF to open the contact holes in the underlying SiO_2 to sources, drains, and substrate contacts. The oxide mask also is removed during the HF etch. The topology is shown in Figure 3, and Figures 4, 5, and 6 depict the sequential cross sections.

d. A 500 Å layer of palladium is evaporated over the wafer and then sintered at 450°C for 30 minutes. This causes the palladium and the silicon in the contact windows to react and form palladium silicide for the ohmic contact. The palladium over the hermetic seal is etched off (see Figures 7 and 8).

e. Next, layers of 1500 Å titanium and 1500 Å palladium are consecutively evaporated over the wafer. A photoresist beam-lead metal-mask operation is performed and the metal pattern is defined in the palladium layer. The etching stops at the titanium layer so that the titanium layer can be used for current carrying in the subsequent plating operations, since it covers the entire substrate (see Figures 9 and 10).

f. A photoresist negative metal-mask operation is next employed so that only the metallization is exposed to the ambient. The wafer is placed in a gold plating bath and a 1.5-micrometer layer of gold is plated in the exposed regions (see Figure 11).

g. A photoresist operation next opens up the beam areas and a 12-micrometer gold layer is plated over the beam pads using the photoresist as the plating mask.

h. The titanium layer is etched open with the gold pattern acting as the etch mask (see Figure 12).

i. A protective 10,000 Å layer of SiO_2 is deposited over the wafer and opened at the beams. The oxide is deposited from silane at 250°C.

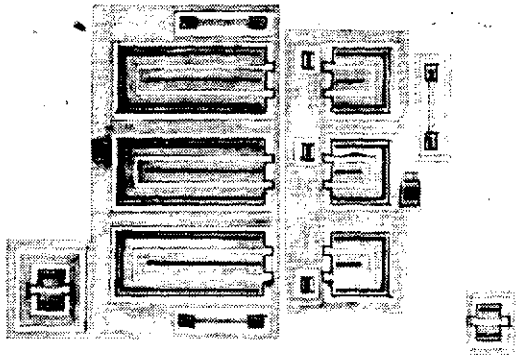

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Figure 3. IC Wafer After Oxide Mask Removed by HF Etch.

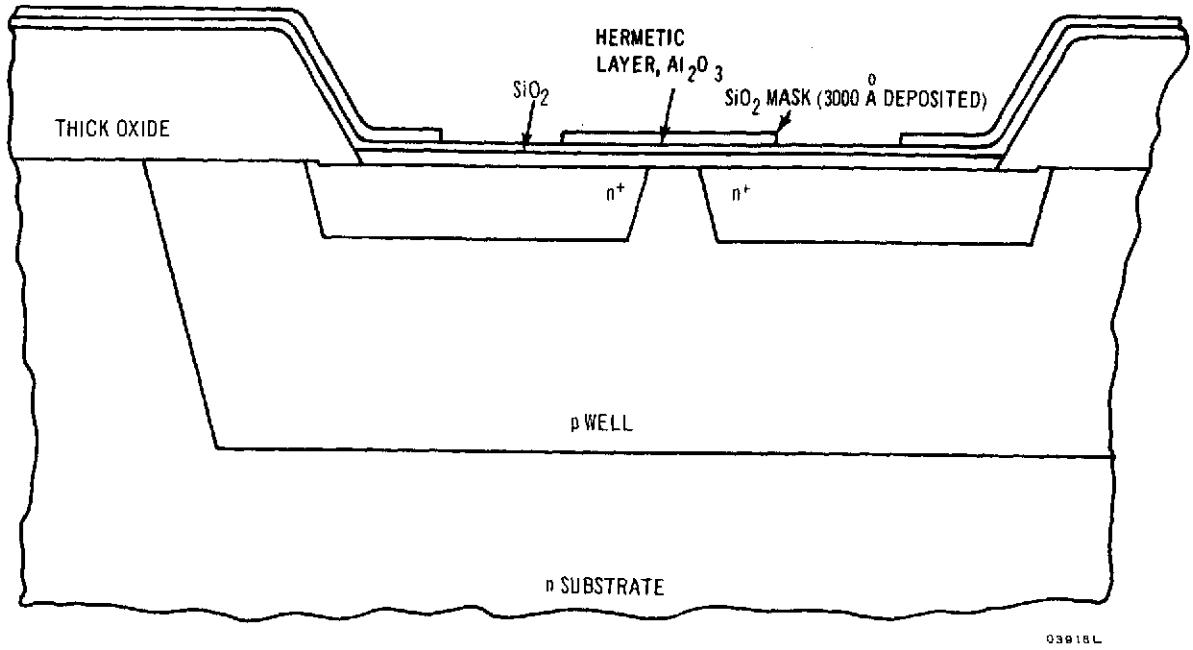


Figure 4. SiO_2 Etch Mask Deposited, Photolithographically Defined, and Etched in Contact Area

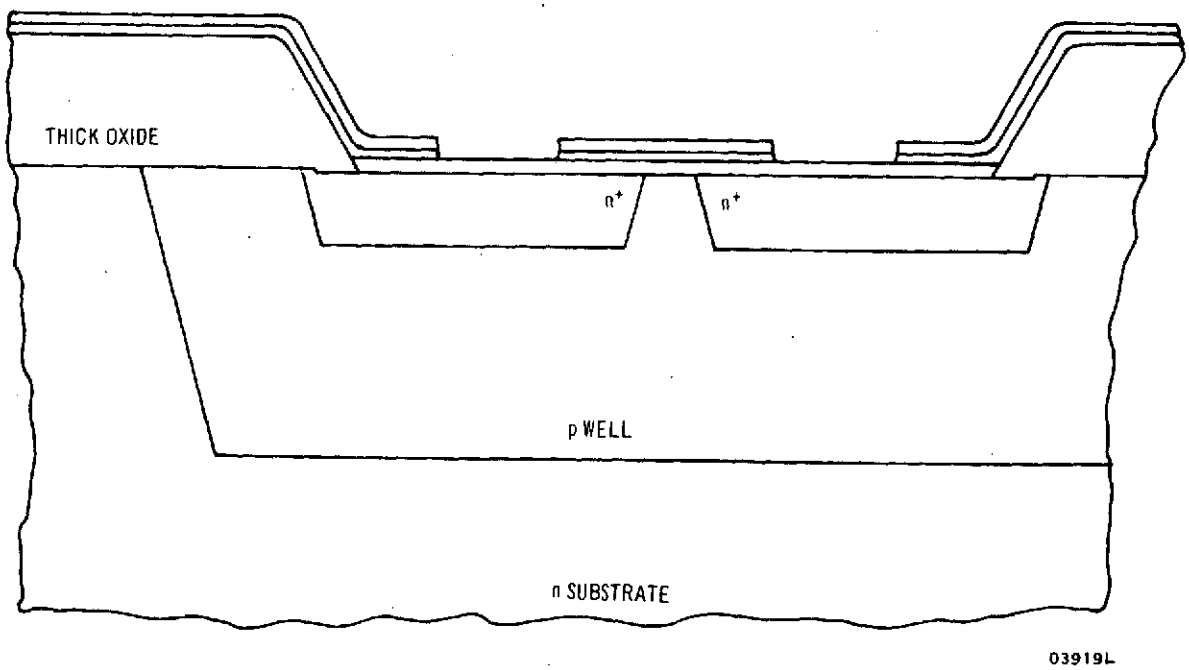


Figure 5. Hermetic Layer Etched in Contact Layer

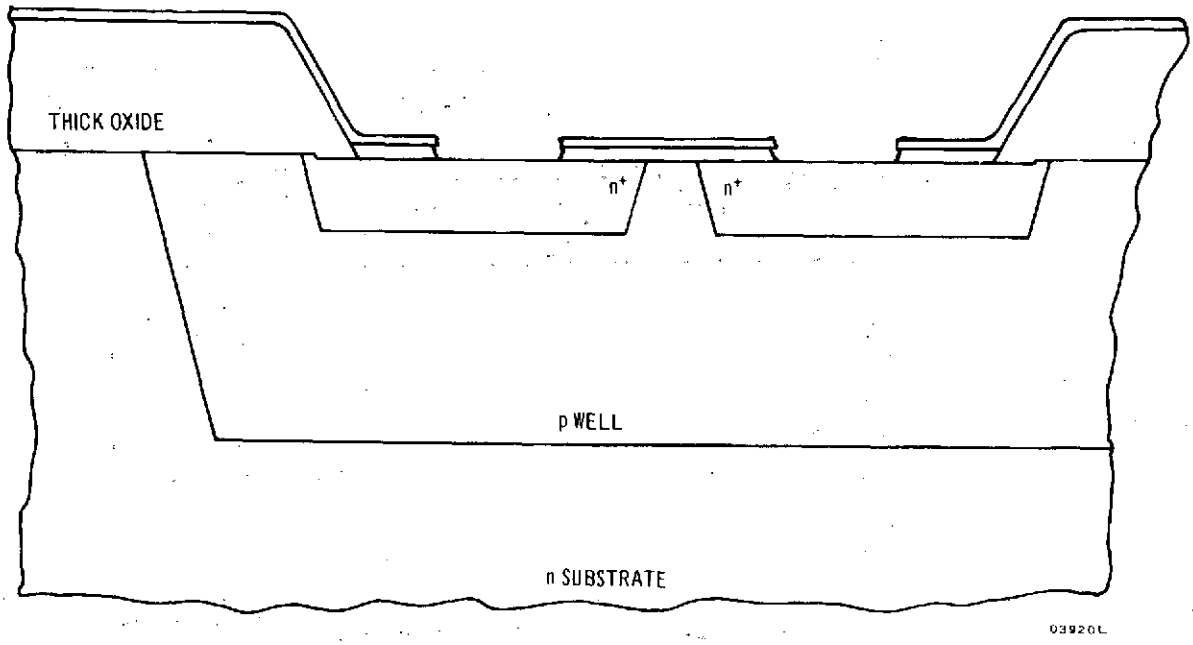


Figure 6. Contact Area Etched Through Channel Oxide, and SiO_2 Etch Mask Layer Removed

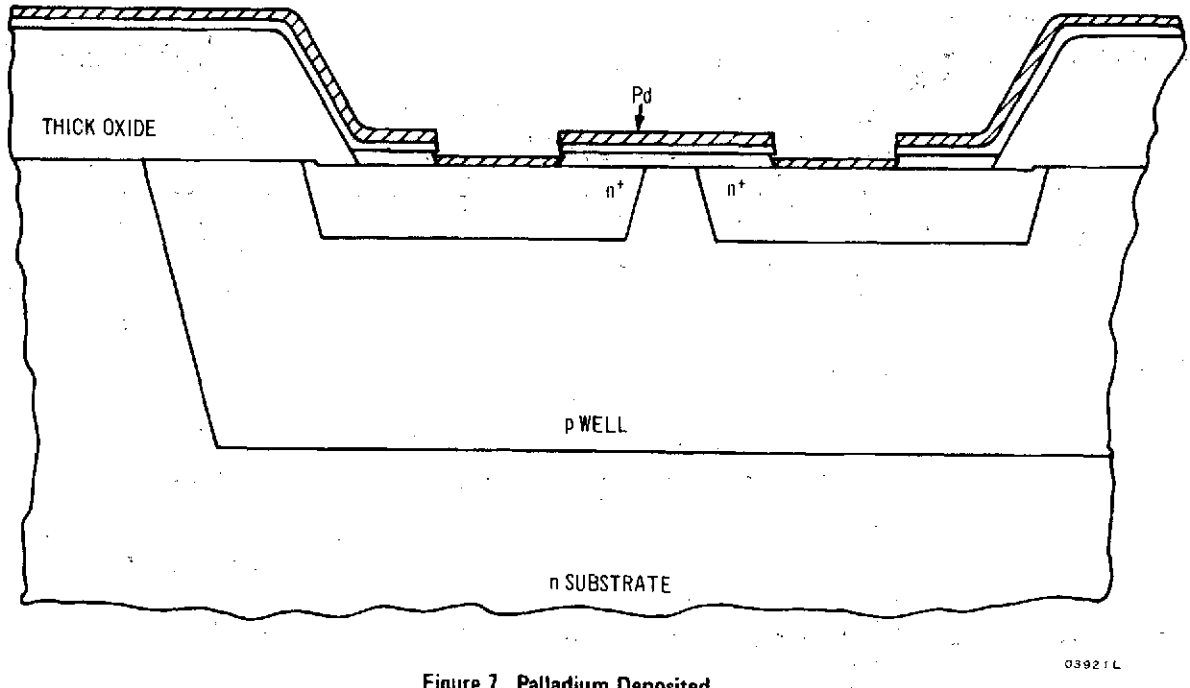


Figure 7. Palladium Deposited

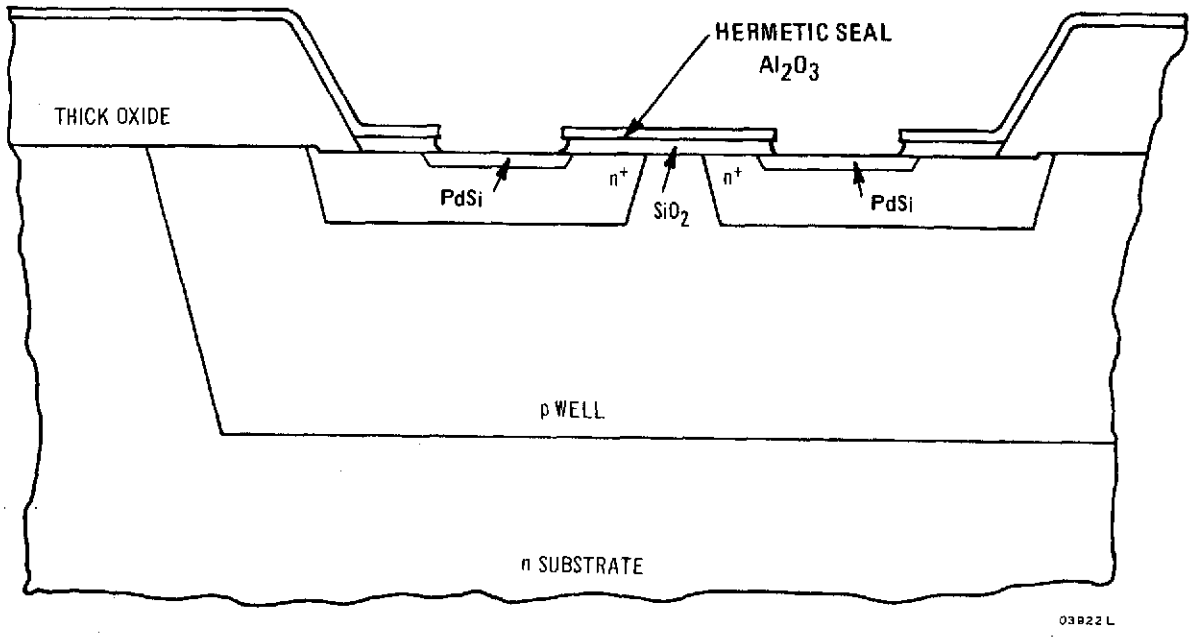


Figure 8. Palladium Sintered into Contact Areas, and Removed From Oxide

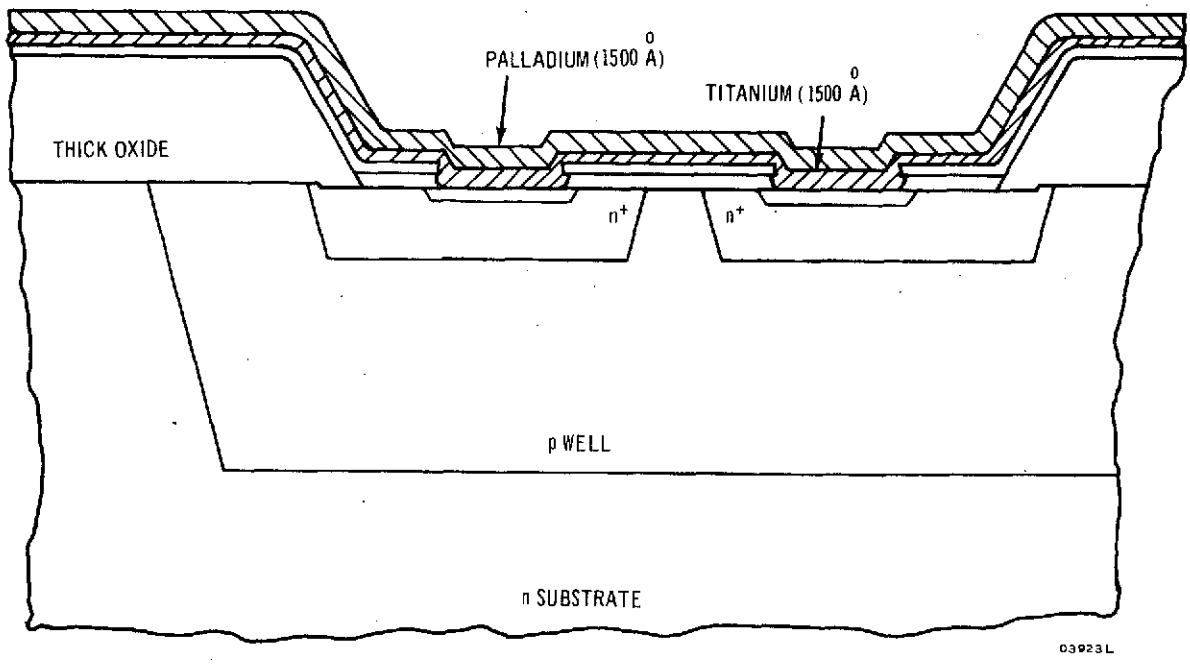


Figure 9. Titanium and Second Palladium Layer Deposited

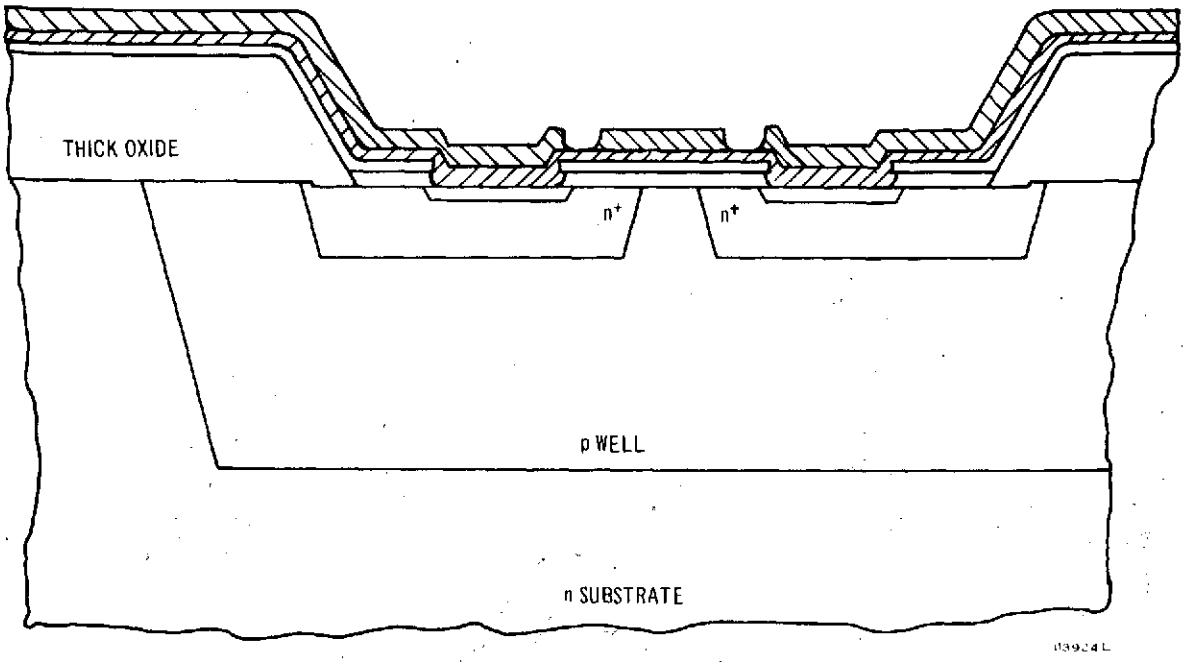


Figure 10. Palladium Layer Defined into Interconnection Pattern

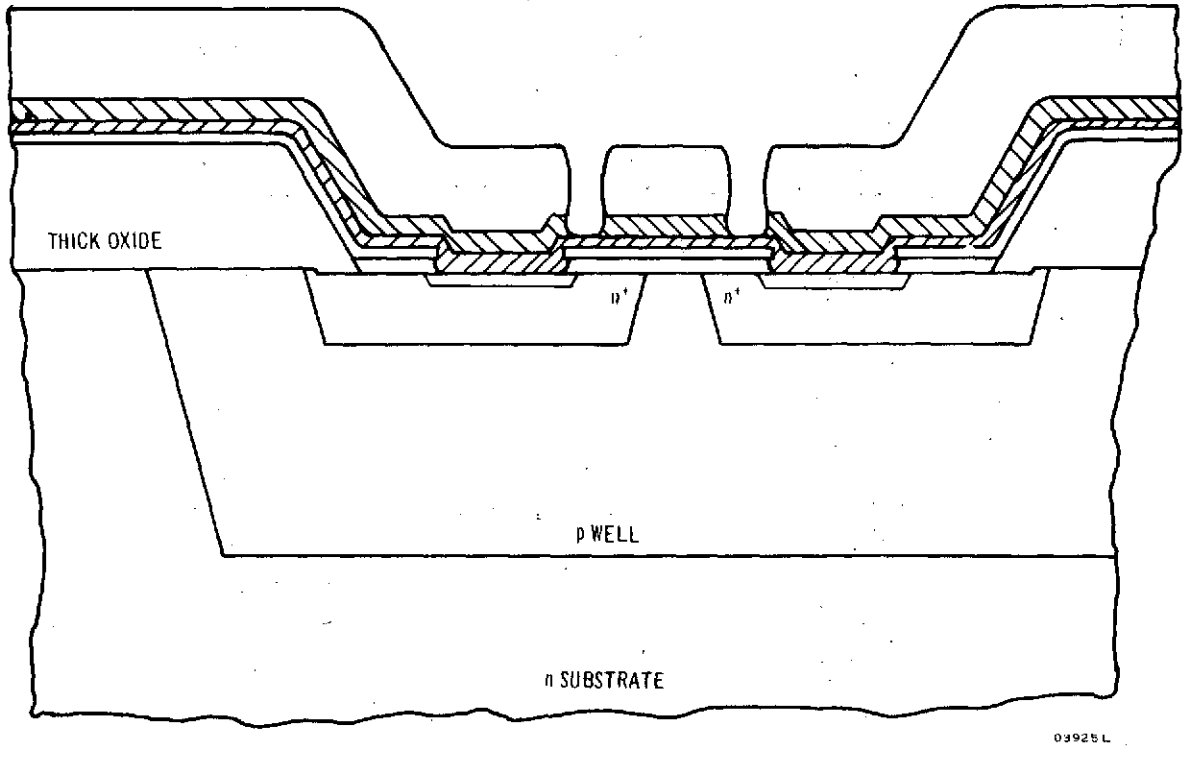


Figure 11. First Layer of Gold Electroplated

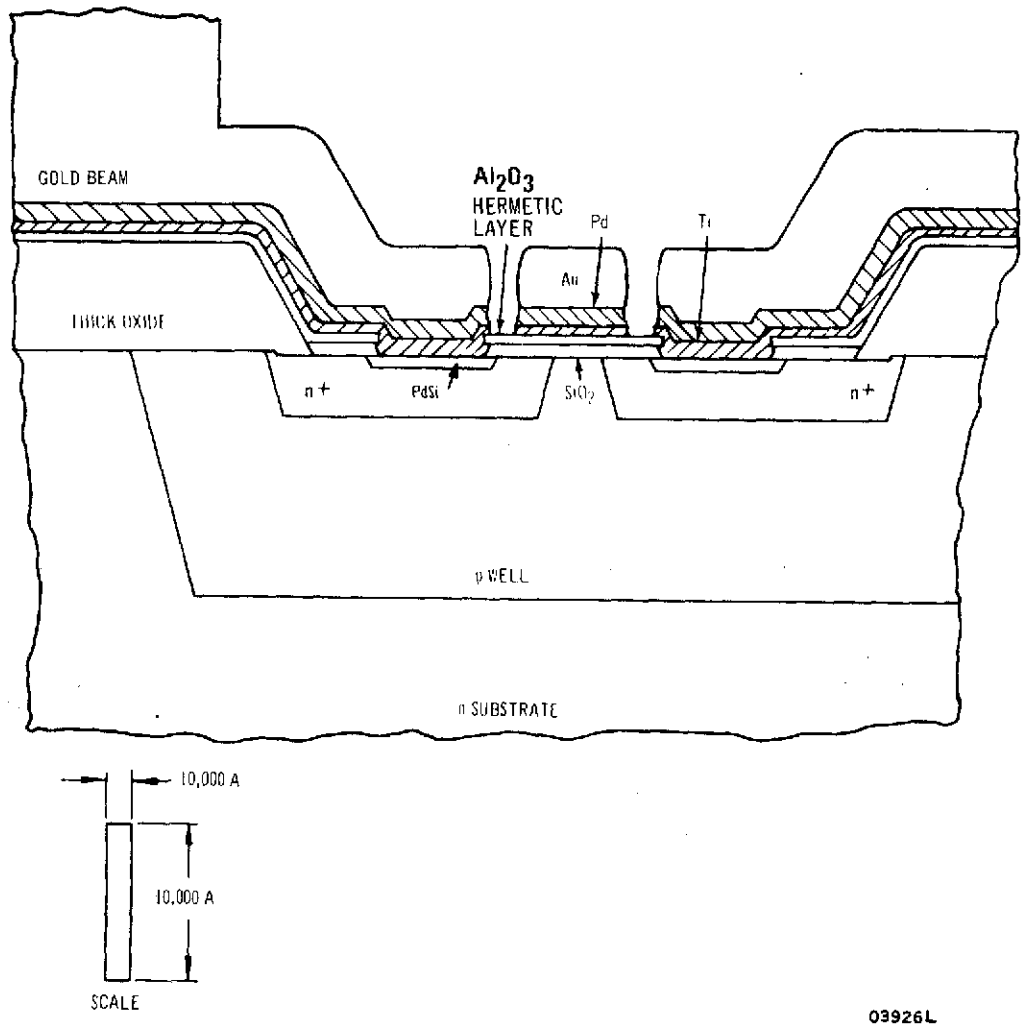


Figure 12. Gold Beams Plated Up and Titanium Removed

j. The wafer is backlapped to 5 mils, back coated with photoresist, and the streets are opened up. The silicon grid is etched through to the beams, thus separating the pellets.

The result of these operations is the beam-leaded sealed-junction COS/MOS chip shown in Figure 13. The photograph is of a beam-lead, sealed-junction version of the RCA CD4007, used as the test vehicle in the early stages of process development. The connection diagram for the CD4007BL is illustrated in Figure 14. The CD4007 was chosen because the three n and three p transistors can be accessed individually and the beam-leaded devices can be studied in detail and the process and any process changes can be readily evaluated. These devices are measured both on curve tracers qualitatively and on a computer-controlled test set statistically. Subsequent designs have been using two n-MOS and two p-MOS transistors with thin and thick gate oxide in the perimeter of the integrated circuit. Appendix A details the statistical technique utilized in determining these parameters. The parameters measured for both n- and p-type transistors include:

a. Threshold voltage (V_{Th}) at I_{DS} = 10 microamperes.

b. Drain-to-source leakage current (I_{DSS}) at $|V_{DS}|$ = 10 and 17 volts.

c. DC forward transconductance (g_{fs}) at $|V_{GS}|$ = 10 volts and $|V_{DS}|$ = 3 volts.

d. Gate leakage (I_G) at $|V_{GS}|$ = 10 and 17 volts.

In addition, the p- and n-drain contact-resistance leakage currents between the n substrate and the p well are measured and a set of 12 continuity tests are made.

B. METALLIZATION PROCESS DEVELOPMENT

Although many areas for potential improvement, process simplification, and increased reliability remain, the process developed has proven to have a good yield and, as will be seen, produces very stable devices.

The metallization system evaporator includes rotating domed planetary substrate fixturing and a completely self-contained control system for the evap-

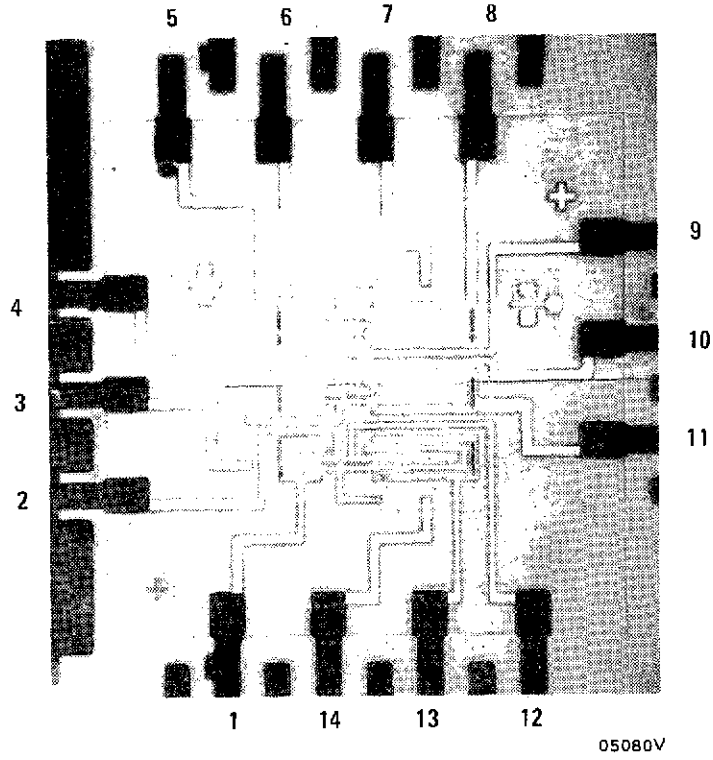


Figure 13. Beam-Lead Test Vehicle (CD4007BL)

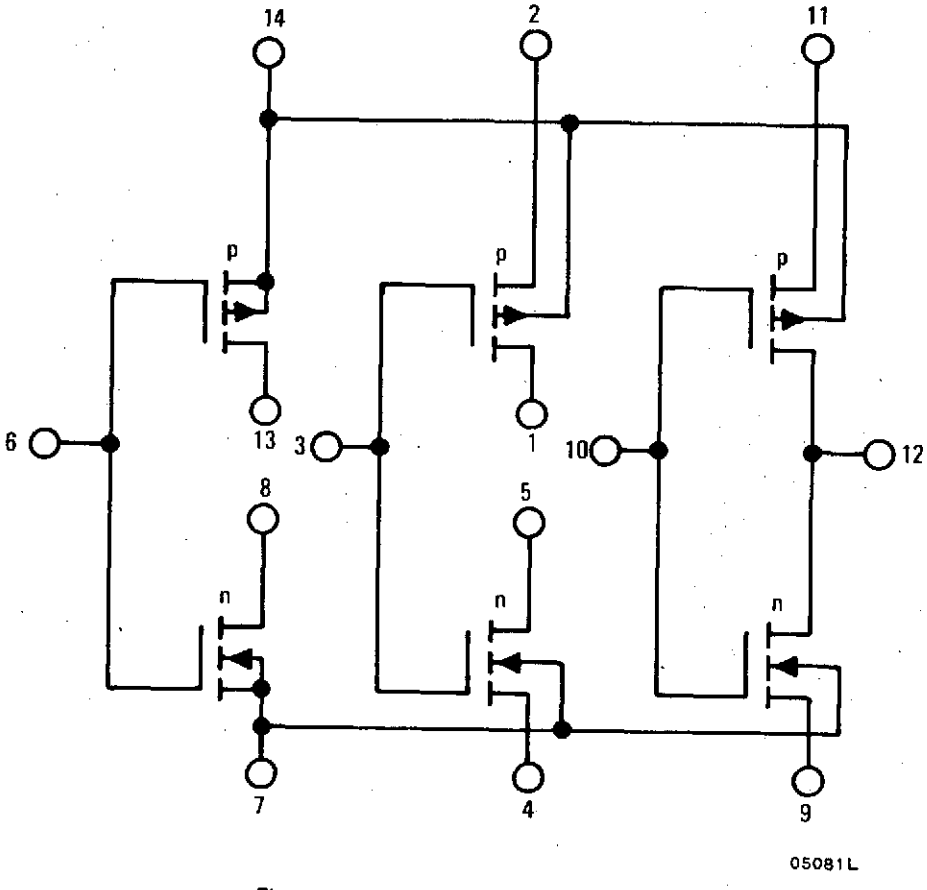


Figure 14. Connection Diagram (CD4007BL)

oration and monitoring of the Ti and Pd thin films. The fixturing will accommodate up to 28 2-inch wafers. Runs have shown good film uniformity with thickness running within ±5 percent variation within a run.

1. PROCESS FLOW

Using the CD4007BL devices as test vehicles, a metallization process was defined. The process flow chart is shown in Figure 15.

While the processing outlined is self-explanatory, the following points bear a more fully detailed discussion.

a. The palladium sintering operation can take place at any temperature in the 400°C to 600°C range. The time duration is on the order of 15 to 40 minutes.

b. In the wafer cleaning operation, a critical process step exists between ensuring cleanliness and low contact resistance. Overcleaning in HCl can remove part of the Pd_2Si contact, while undercleaning often results in high leakages.

c. Titanium must be evaporated at the lowest possible pressure, otherwise a titanium oxide is formed and this results in lifting of the metal pattern after definition.

d. An iodine-based commercial etch is used for the interconnect pattern. This palladium etch reacts with the titanium underlayer and colors it. This coloration shows when the palladium layer has been defined over the wafer and thus eliminates the problems of either overetching (undercutting) or underetching (metal bridging).

2. IN-PROCESS CONTROLS

Major emphasis is given to controls on the following items:

a. Palladium thickness is measured during evaporation by a quartz crystal oscillator and after evaporation by either a Talysurf or an interference microscope. This control is essentially single-ended, having a lower limit specification only.

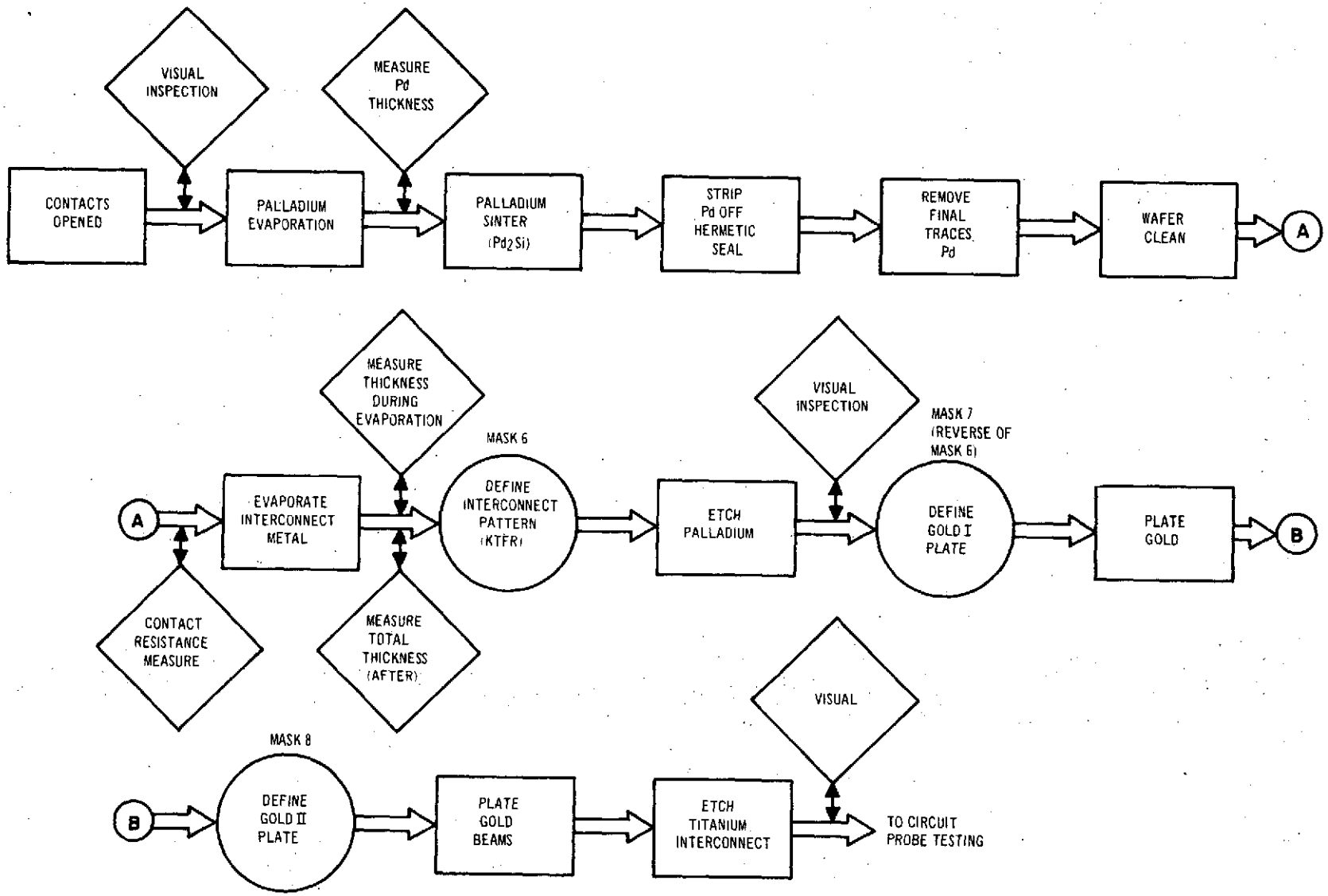


Figure 15. Process Flow Chart for Metallization Sequence

b. The Ti:Pd thicknesses are similarly monitored. The total thickness is greater than twice the thickness of the channel oxide to ensure that the contact holes are completely metal filled.

c. After palladium definition, the visual inspection is keyed at maintaining an overlap of the interconnect metal to the contacts to prevent the subsequent gold plate from entering the contact region and reaching the silicon itself.

d. After etching the titanium, particular attention is paid to make sure that etching of the regions between source-gate and drain-gate metal lines is complete.

3. BEAM-LEAD ADHESION TESTS

A series of CD4007 devices were beam-lead bonded to a 14-lead DIC fashioned such that the chip was over a 40-mil hole in the ceramic. This permitted the use of the push-off test, in which a rod is pushed through the hole against the bonded chip. Pressure is gradually applied and the point at which the bonds fail is measured.

All chips exceeded the 20-gram specification and some exceeded the 100-gram limit of the apparatus.

C. HERMETIC SEAL

At the beginning of the program silicon nitride and aluminum oxide were the two dielectrics considered for sealing the critical MOS gate. Silicon nitride is more impervious to sodium than aluminum oxide and has a lower conductance. Both dielectrics are deposited at high temperatures in reactors that are inductively heated. Both dielectrics gave good seals and electronic properties that allowed MOS transistor threshold voltages in the range of 1 to 2 volts by adjusting the processing. Since there is a negative charge introduced at the Al_2O_3:SiO_2 interface (and zero charge for Si_3N_4:SiO_2), it was easier to adjust the p-MOS to a low threshold voltage with SiO_2:Al_2O_3. For this reason Al_2O_3 was chosen over Si_3N_4.

1. MIS CAPACITOR CONTROL

Metal-insulator-silicon capacitors have long been used to characterize semiconductor surface properties. The high-frequency capacitance equals the insulator capacitance (with an effective thickness t_{eff}) under heavy accumulation, and reduces to a lower value under inversion. The voltage at which this transition occurs is called the flatband voltage since no band bending in the silicon-band structure occurs. The stability of the structures has been tested at 300°C for 1 minute under +10 and -10 volt biases (10^6 volt/cm). This way test matrices with various ratios of gate dielectric 1 to gate dielectric 2 have been tested, see Table I.

TABLE I. HERMETIC SEAL-TO-CHANNEL OXIDE THICKNESS RATIOS

Silicon Nitride Matrix Thicknesses (Å)		Aluminum Matrix Thicknesses (Å)	
SiO_2	Si_3N_4	SiO_2	Al_2O_3
1000	0	1000	0
800	380	800	450
600	700	600	900
400	1050	400	1350
200	1400	200	1800

The effective thickness, t_{eff}, of the gate dielectric is

$$t_{eff} = t_{SiO_2} + t_{seal} \frac{\varepsilon_{SiO_2}}{\varepsilon_{seal}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$

and has been kept at 1000 Å, a value allowing for enough margin to prevent premature gate breakdown ($\varepsilon_{SiO_2} = 3.82$; $\varepsilon_{Al_2O_3} = 9.5$; $\varepsilon_{Si_3N_4} = 6.9$).

2. THRESHOLD VOLTAGE CONTROL

The threshold voltage is usually expressed as

$$V_t = \frac{qN_{ss}}{C_{ox}} \pm \frac{\sqrt{2q\varepsilon_o \varepsilon_{Si} N}}{C_{ox}} \sqrt{|2V_f| + |V_{sub}|} \pm V_f + \phi_{MS} \quad \ldots\ldots \quad (2)$$

use + sign for n-MOS

use - sign for p-MOS

where

C_{ox} = oxide capacitance = $\frac{\varepsilon_{SiO_2} \varepsilon_o}{t_{eff}}$

N = carrier concentration in the channel

N_{ss} = interface state density

ϕ_{MS} = metal-semiconductor work function

V_{sub} = substrate voltage

V_f = Fermi voltage

V_t = threshold voltage at $I_d = 0$

The presence of Si_3N_4 or Al_2O_3 in the gate structure influences the threshold voltage in two ways. First, the interface charges in the Si_3N_4 or Al_2O_3/SiO_2 interface will be reflected as effective surface-state concentrations, N_{ss}, in the SiO_2/Si interface, and a lower work function, ϕ_{MS}. Second, the effective channel thickness, t, is modified by the dual dielectric.

The effective ϕ_{MS} (including ϕ_{ii}) for the SiO_2:Al_2O_3:Ti:Pd:Au system is approximately 0.55 eV lower than that of n^+ silicon, while the corresponding value for the SiO_2:Si_3N_4:Ti:Pd:Au system is approximately zero. The surface-state densities on (100)-silicon are approximately:

$N_{ss} = 7 \times 10^{10}$ cm^{-2} for n-MOS; $N_{ss} = 1 \times 10^{11}$ cm^{-2} for p-MOS with Al_2O_3

$N_{ss} = 1 \times 10^{11}$ cm^{-2} for n-MOS; $N_{ss} = 8 \times 10^{10}$ cm^{-2} for p-MOS with Si_3N_4

The threshold-voltage-concentration design curves are plotted in Figures 16 and 17. As can be seen from Figure 17, p-MOS transistor threshold voltages below 1 volt cannot be obtained with SiO_2:Si_3N_4. On the other hand, the separation between the n-substrate and p-well concentration (overdoped by diffusion) is much larger, making this diffusion easier when compared to the SiO_2:Al_2O_3 system. Since MOS circuits run faster (at a given supply voltage) with lower threshold voltage, it was decided to use the SiO_2:Al_2O_3 system. The process was stablized with 800 Å of SiO_2 and 400 Å of Al_2O_3, corresponding to an effective insulator thickness of about 1000 Å.

For SiO_2:Al_2O_3, the set of parameters in Table II can be used. Since a light p diffusion is used for the n-type MOS, the ratio of surface-to-bulk concentration is somewhat low. A slight mismatch in threshold voltages that does not affect circuit performance might be more desirable.

A final consideration on low-threshold design is the effect of surface-state desnity on thresholds. In the foregoing analysis, a surface-state density that calculates out to a -0.47 volt potential for the p-MOS and one of -0.33 for the n-MOS was assumed (for t_{ox} = 1000 Å), as shown in Table III. This value appears reasonably constant.

3. HERMETIC-SEAL PROCESS FLOW

The process for fabricating the alumina-silica and the silicon-nitride-silica gate dielectric was defined and the process flow is given in Figure 18.

After a clean 800 Å SiO_2 film has been grown, the wafer is transported to the alumina or silicon nitride deposition system. This particular apparatus consists of series of four round silicon carbide-coated carbon susceptors each having a carbon shaft whose end point is affixed into a revolving quartz tube as shown in the schematic of Figure 19 for the Al_2O_3 deposition and Figure 20 for the Si_3N_4 deposition. The susceptors rest upon a seeond quartz tube, which is larger in diameter but concentric with the first tube. Revolving the quartz tube causes the susceptors to rotate and due to friction with the outer quartz they also rotate. This planetary arrangement assures uniform heating of the susceptors in the RF field generated by the concentric RF coil outside the

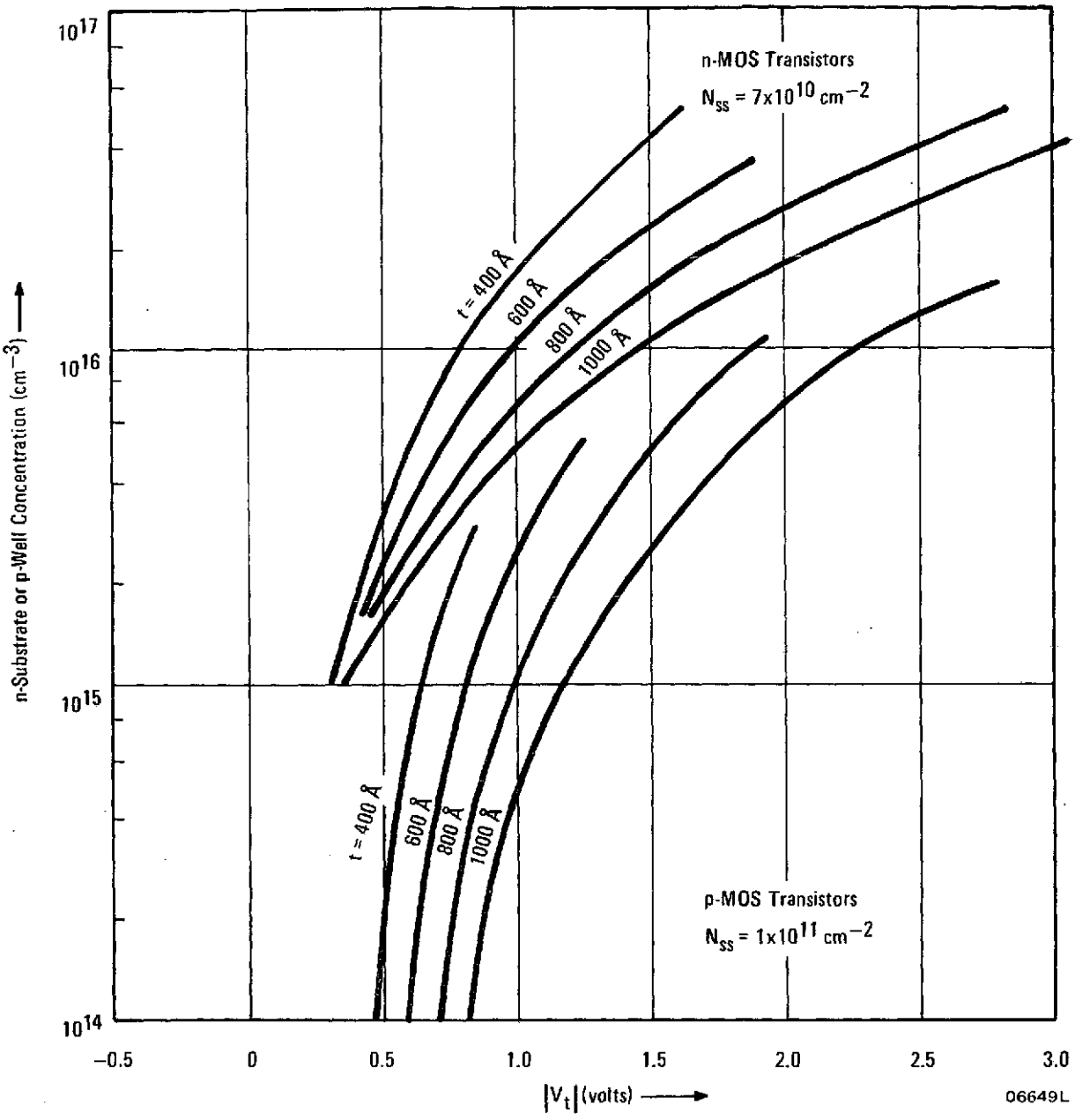


Figure 16. Variation of Threshold Voltage for Ranges of Effective Channel Oxide Thickness of SiO_2 : Al_2O_3 and for n-Substrate or p-Well Concentrations with Ti/Pd/Ti/Au Metal

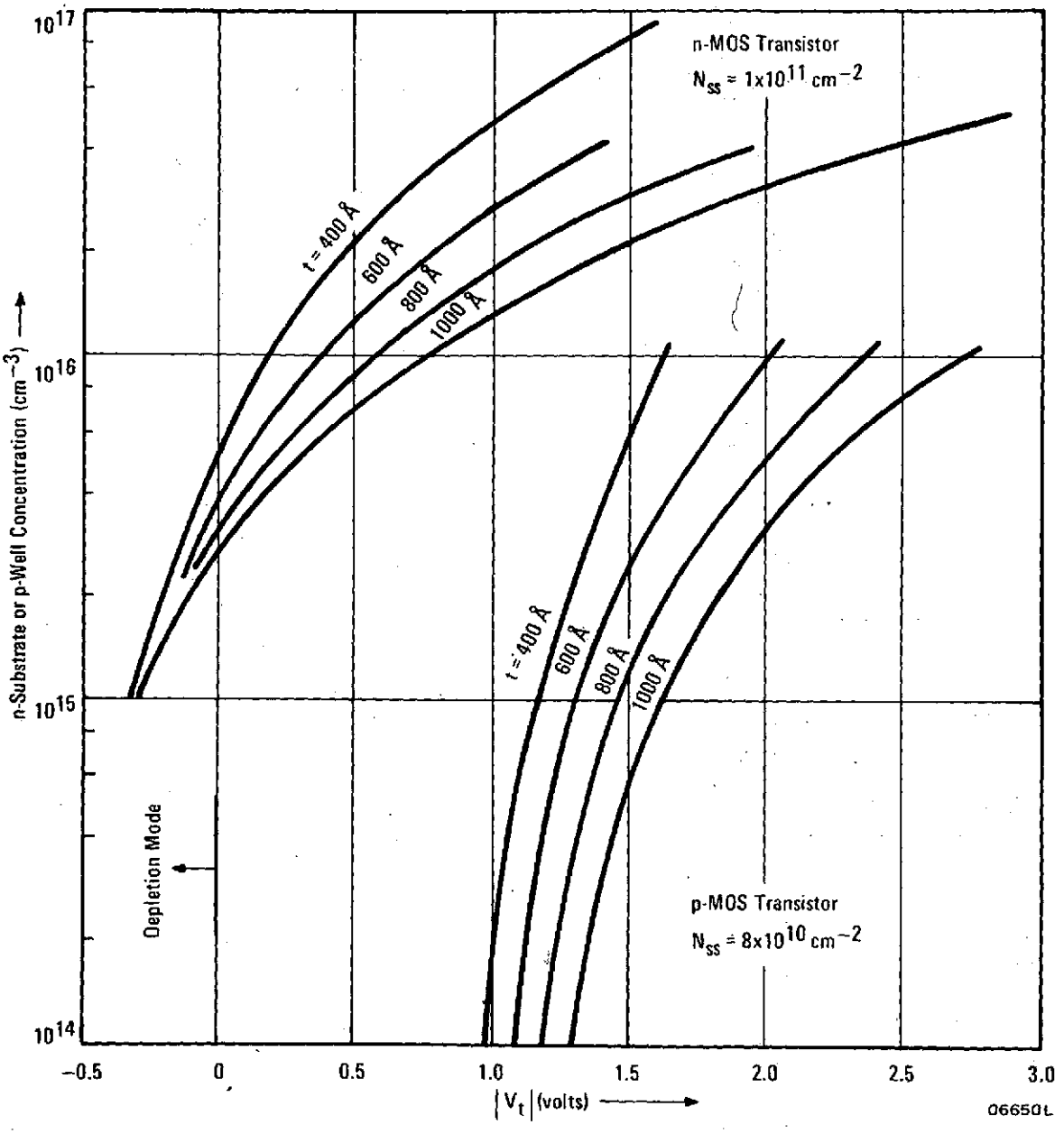


Figure 17. Variation of Threshold Voltage for Ranges of Effective Channel Oxide Thickness of $SiO_2 : Si_3N_4$ for n-Substrate or p-Well Concentration with Ti/Pd/Ti/Au Metal

TABLE II. DESIGN PARAMETERS FOR SiO_2:Al_2O_3 ($|V_t|$ = 1.2 V)

	p-MOS	n-MOS
Substrate Concentration	1.22×10^{15}*	7.30×10^{15}
SiO_2 Oxide Thickness	800 Å	800 Å
Actual Composite Thickness	964 Å	964 Å

*Corresponds to 4.02 ohm-cm of n silicon

TABLE III. THRESHOLD VOLTAGES FOR IDEAL INTERFACES (N_{ss} = 0) OF Al_2O_3:SiO_2 GATES

V_{tp}(Volts) n-substrate resistivity in ohm-cm						V_{tn}(Volts) p-well concentration in cm^{-3}			
	1	2	3	5	10	5.0×10^{15}	9.0×10^{15}	1.5×10^{16}	3.0×10^{16}
1000	-1.36	-1.00	-0.85	-0.70	-0.55	1.33	1.71	2.16	2.98

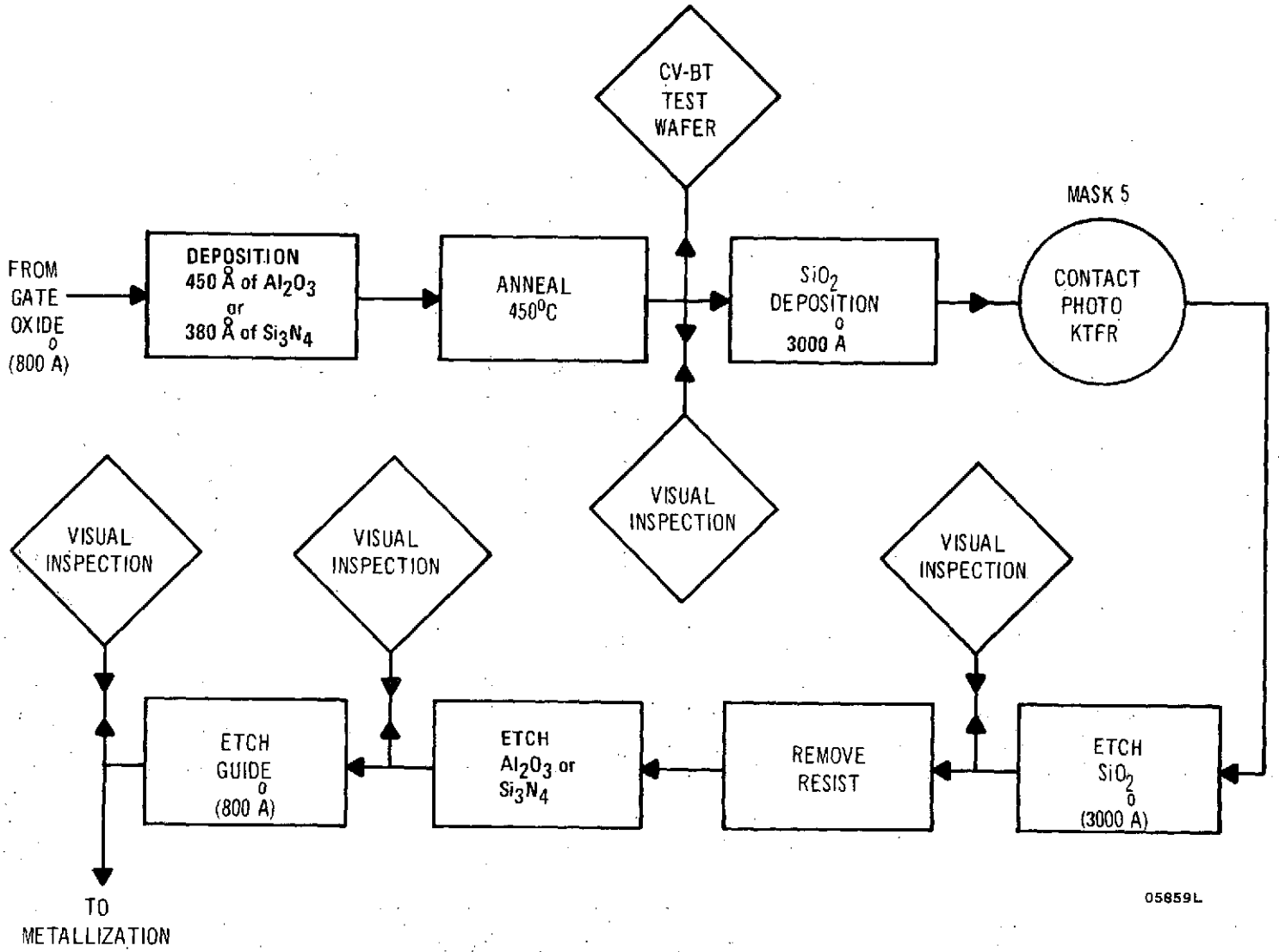


Figure 18. Process Flow Chart for Al_2O_3 or Si_3N_4

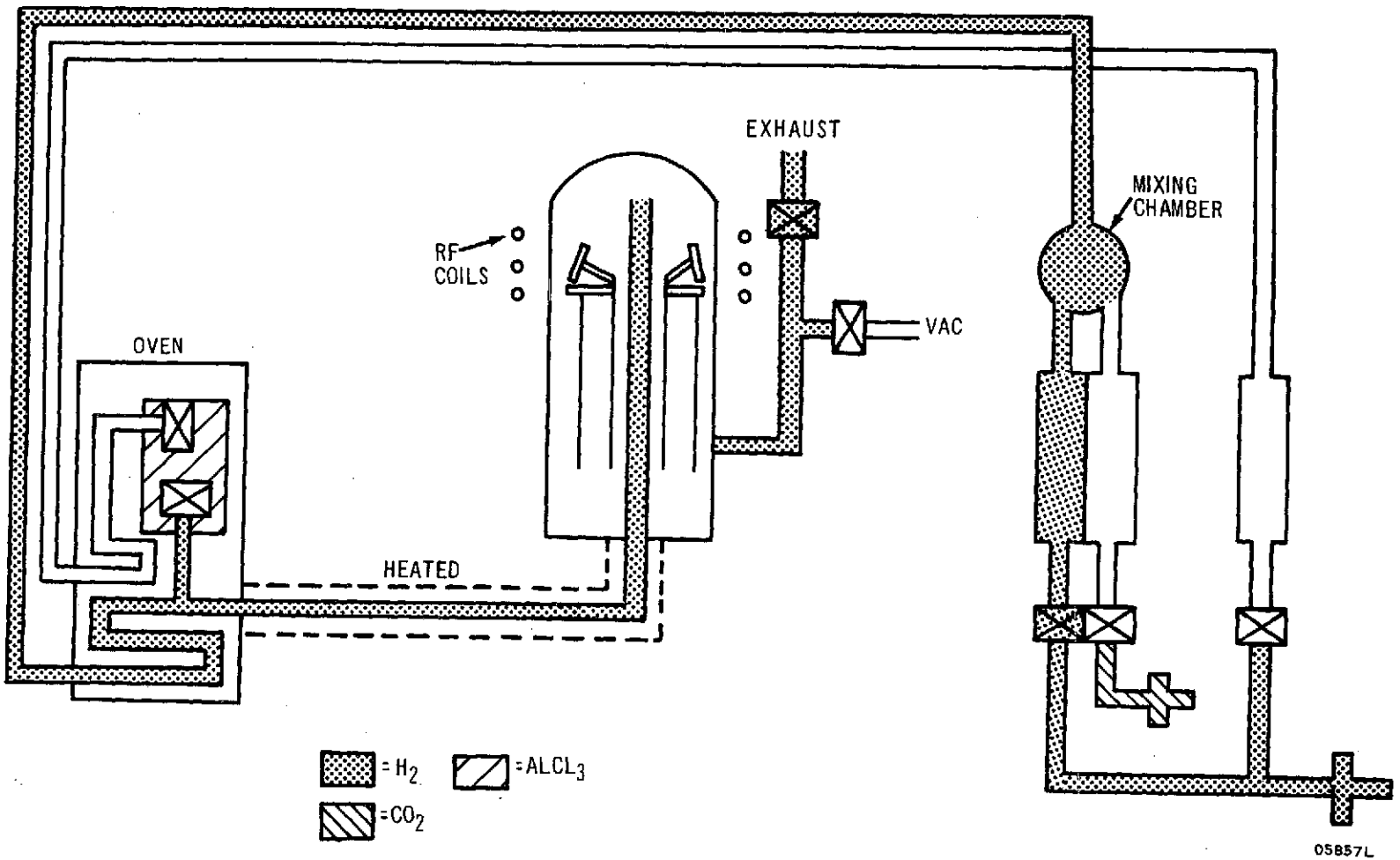


Figure 19. Schematic of Al_2O_3 Deposition Equipment

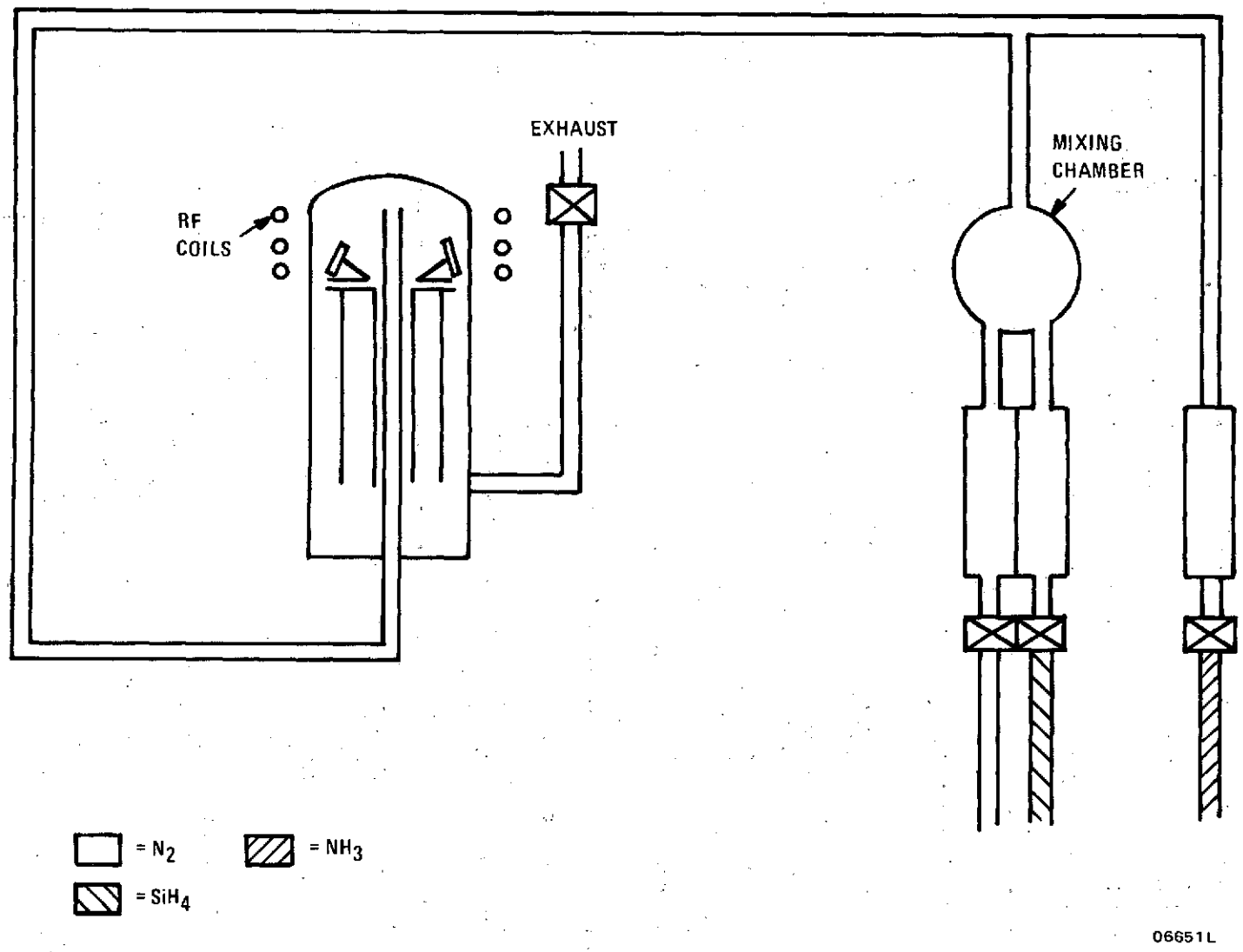


Figure 20. Schematic of Si_3N_4 Deposition Equipment

reaction chamber. The silicon wafers are placed upon the ledges inset into the susceptors. Since the susceptors are tilted, the slices do not fall off during rotation and make contact with the susceptors over their entire area ensuring good thermal contact and uniform heating.

By adjusting the RF generator output power, the susceptors and slices are heated to 850°C in a hydrogen atmosphere. At this point, carbon dioxide is introduced into the chamber causing the formation of water vapor by the reaction

$$H_2 + CO_2 \xrightarrow{850^\circ C} H_2O + CO$$

Since this reaction occurs only at temperatures above 700°C, these products are formed only near the heated susceptors. A minute after the carbon dioxide is introduced, the hydrogen flow line through the aluminum chloride sublimator is activated and aluminum chloride enters the chamber. The sublimator holds 1 pound of powder heated to 110°C over which the hydrogen is directed in a labyrinthian manner.

The chemical reacts with the water vapor near the susceptors to form the oxide. This is expressed as

$$2\ AlCl_3 + 3\ H_2O \longrightarrow Al_2O_3 + 6\ HCl$$

A deposition rate of 100 Å/minute is normal; when it drops below 80 Å/minute, the system is overhauled (approximately every 6 months).

The relative amounts of reagents in this process are:

Reagent	Flow Rate (Liters/Minute)	Percentage
H_2	10	99
CO_2	0.08	0.72
H_2 (through the $AlCl_3$ chamber)	1	0.036 of $AlCl_3$

The aluminum oxide layer is etched with phosphoric acid at 180°C. Because photoresist cannot take such treatment, a secondary mask is required. For

this case a thick masking oxide of about 3000 Å is deposited. This is opened up with the contact mask. This oxide then acts as a mask to open up the aluminum oxide portion of the contact during the phosphoric acid etch. The aluminum oxide then acts as a mask during the opening of the silica portion of the contact in the contact-etch sequence. The masking oxide is removed simultaneously with the silica contact opening by the action of the buffered hydrofluoric acid etch.

For Si_3N_4, the susceptor and the silicon slices are heated to 1050°C in a nitrogen atmosphere. At this point ammonia is introduced into the chamber. After 15 seconds silane is introduced and silicon nitride is deposited by the following reaction

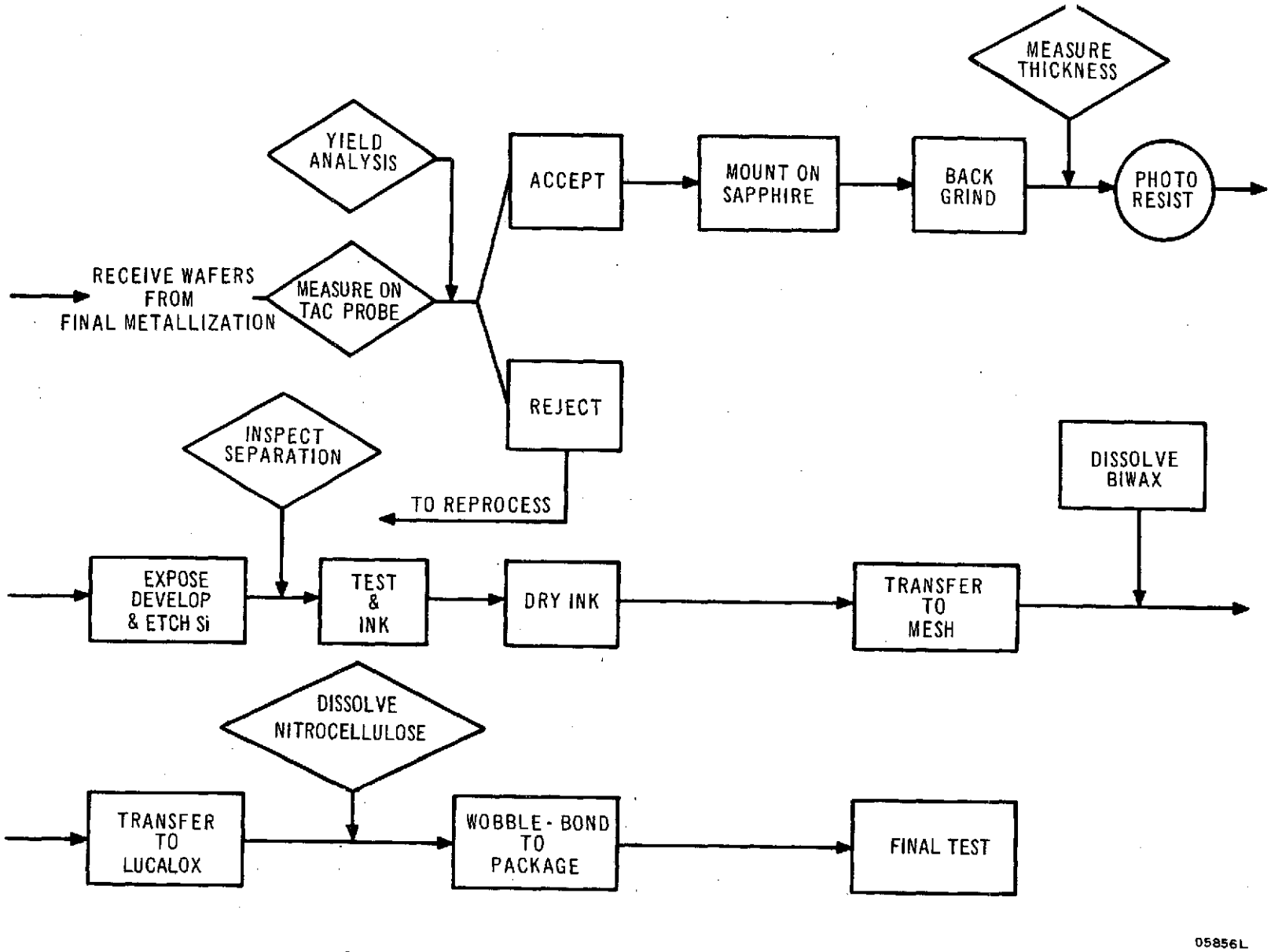
$$3\ SiH_4 + 4\ NH_3 \xrightarrow{1050^\circ C} Si_3N_4 + 12\ H_2$$

Since this reaction occurs only at temperatures above 700°C, these products are formed only near the heated susceptor. A deposition rate of 100 Å/minute is normal. The relative amounts of reagents in this process are:

Reagent	Flow Rate (Liters/Minute)	Percentage
N_2	10	80.3
NH_3	2.1	16.9
3% SiH_4 in N_2	0.35 ($10.5\ cm^{-3}$/minute of pure silane)	2.8

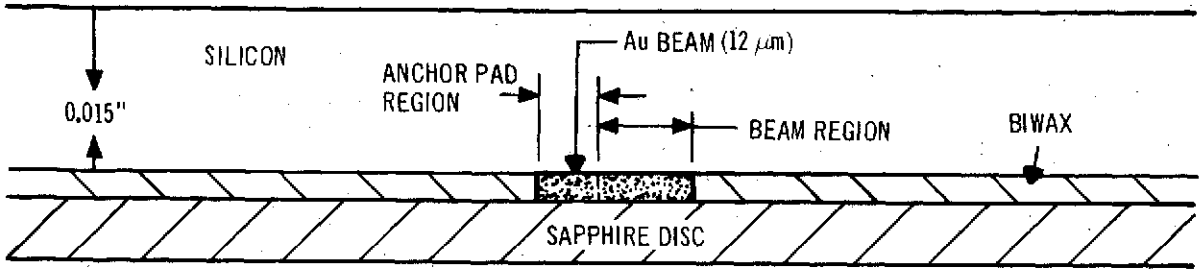
D. BEAM-LEAD CHIP SEPARATION

Since the devices being manufactured are interdigitated beam-lead types, the pellets cannot be separated simply by scribing as standard-processed pellets are. For separating beam-lead chips (one from another) a more complex but more reliable and higher yielding process is the back-lapping etch process. The process sequence for the transferring and bonding operations are shown in A, Figure 21. The details of the back-lapping etching process are illustrated in B, Figure 21. Following is a description of the separation process:

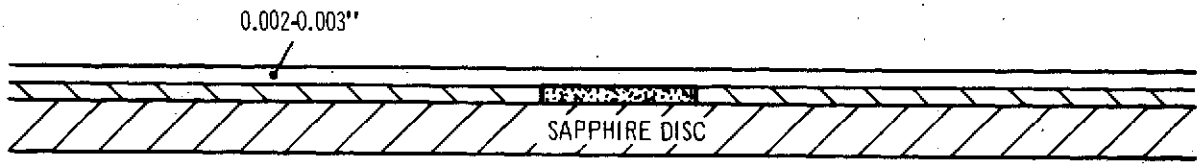


A. PROCESS SEQUENCE FOR TRANSFERRING AND BONDING OPERATIONS

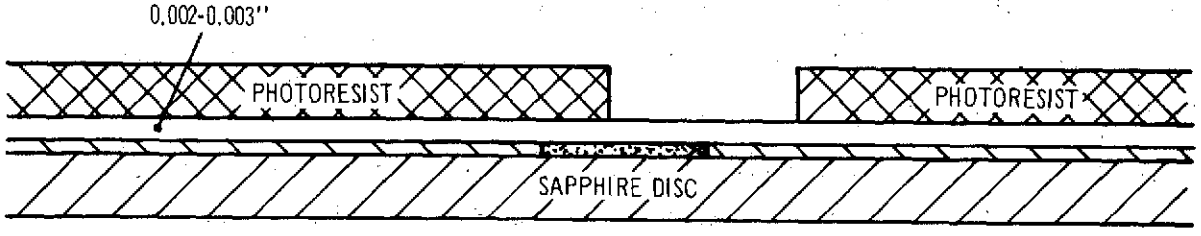
Figure 21. Pellet Separation (Sheet 1 of 2)



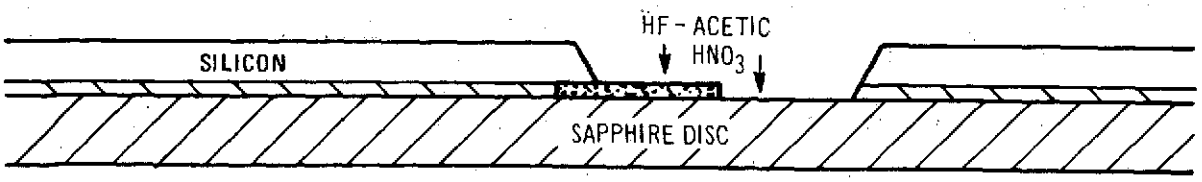
A. MOUNT SILICON WAFER ON SAPPHIRE DISC



B. BACK GRIND WAFER



C. BACK ALIGN



D. BACK ETCH

05856L

B. STEP-BY-STEP BACK-LAP PROCESS

Figure 21. Pellet Separation (Sheet 2 of 2)

a. The wafer is sample circuit probed and the yield projected.

b. Wafers having a satisfactory yield are waxed face down to either a sapphire or Lucalox disc. The disc is usually about 35 mils thick, is transparent and has a diameter 1 inch larger than the silicon wafer. The wax employed is Biwax.

c. The wafers, which are about 11 to 14 mils thick, are back ground to about 4 to 5 mils (depending on the chip size).

d. After back grinding, the wafers are photoresist coated on the back side (silicon surface), and aligned to the separation mask by back alignment. This alignment employs infrared light which transmits through the silicon layer and is absorbed by the metal patterns, thus permitting alignment to the mask. The photoresist (negative type) is exposed in the usual manner and developed.

e. After exposure, the wafers are etched in a hydrofluoric, acetic, and nitric acid solution until the anchor pads on the beam leads are exposed.

f. The wafers are 100-percent tested against the full range of specifications and the defective chips inked. The ink is then baked on.

g. Upon inking, the transferal operation is begun. The wafer and disc are glued onto a stainless steel mesh with a mixutre of nitrocellulose and acetone.

h. After glueing, the Biwax is dissolved with trichloroethylene from the sapphire disc and the back of the silicon, leaving only the chips on the screen.

i. A Lucalox disc, coated with silastic S2288, is pressed against the array of chips and then the nitrocellulose is dissolved away in acetone.

j. The chips on the silastic-coated Lucalox are picked up by the bonding tool and wobble bonded down to the ceramic substrate as required.

E. DEVICE EVALUATION

1. MIS CAPACITOR MEASUREMENTS

As mentioned in paragraph C several matrices were set up to study the flatband voltage and its shift under stress of MIS capacitors having various ratios of SiO_2 and Al_2O_3. The deposition temperature was also varied in a systematic way to obtain optimized conditions. The flatband voltages of each wafer were determined by using both Al and TiPd metals. Both n and p silicon wafers were tested. The results are shown in Figure 22 for Al and Figure 23 for TiPd. The graphs show that a ϕ_{MS} difference of above 0.3 volt exists between Al and TiPd.

A second matrix involved studying the flatband voltage of silicon nitride sandwiches deposited at temperatures of 800°C, 900°C, and 1050°C. The results are shown in Figure 24. The points recorded were only of flatband voltages. Bias temperature curves were also taken, but their deviations from flatband voltage were only 0.1 of a volt. Although a definite variation with temperature was found, almost the same variation was found in the SiO_2 control capacitors, so that at least part of the variation was due either to the quality of the SiO_2 or to the annealing conditions.

The time dependence of the flatband-voltage shift was also studied. Figure 25 shows the shifts for both Al_2O_3 and Si_3N_4 for up to 3000 seconds at 300°C. It can be seen that the two types of sandwich layers behave quite differently. First, the alumina silica shows threshold-voltage drift under negative bias, and at some later time the silicon nitride shifts become evident. The alumina shift saturates around ΔV - 0.7 volt, but the nitride continues to increase showing some sign of saturation near the end of the experiment. The shift of the nitride sample can be explained by charging taking place at the interface using the Frankel-Poole tunneling model. No such model pertains to the alumina, however.

The ratios of 800 Å of SiO_2 to about 400 Å of Al_2O_3 or Si_3N_4 are more stable than that of 200 Å of SiO_2 to about 1600 Å of Al_2O_3 or Si_3N_4 (see Figure 26). In either case the same situation exists, but the difference between the nitride and the alumina is amplified. Once again the alumina saturates and the nitride

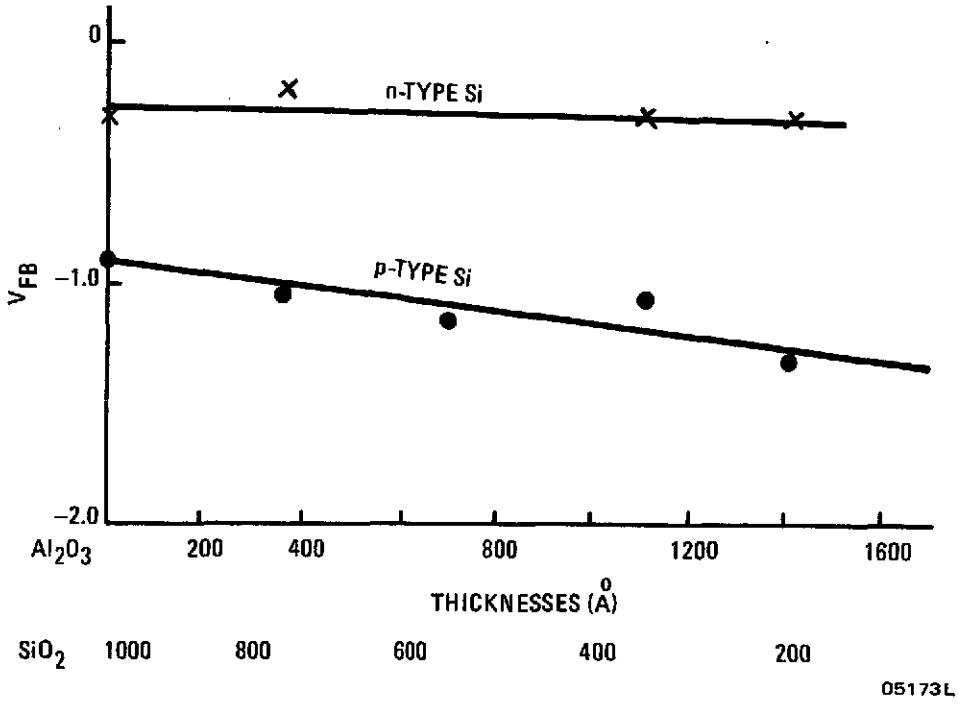


Figure 22. Variation of Flatband Voltage on n and p Wafers Using Various Composite Dielectrics: Al Metal

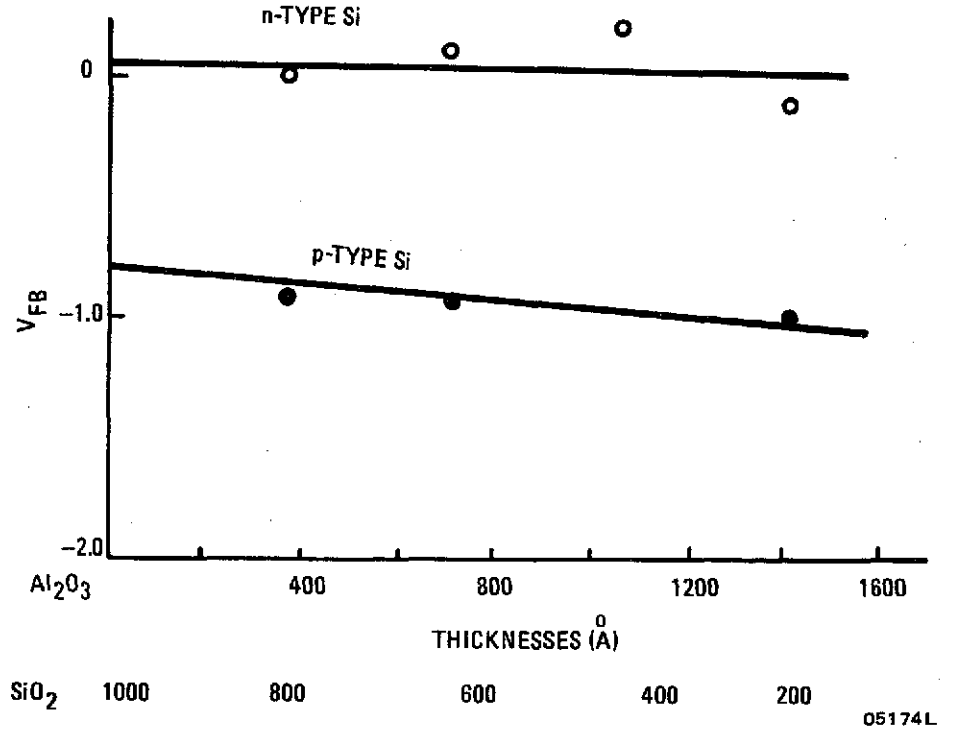


Figure 23. Variation of Flatband Voltage on n and p Wafers Using Various Composite Dielectrics: Ti Pd Metal

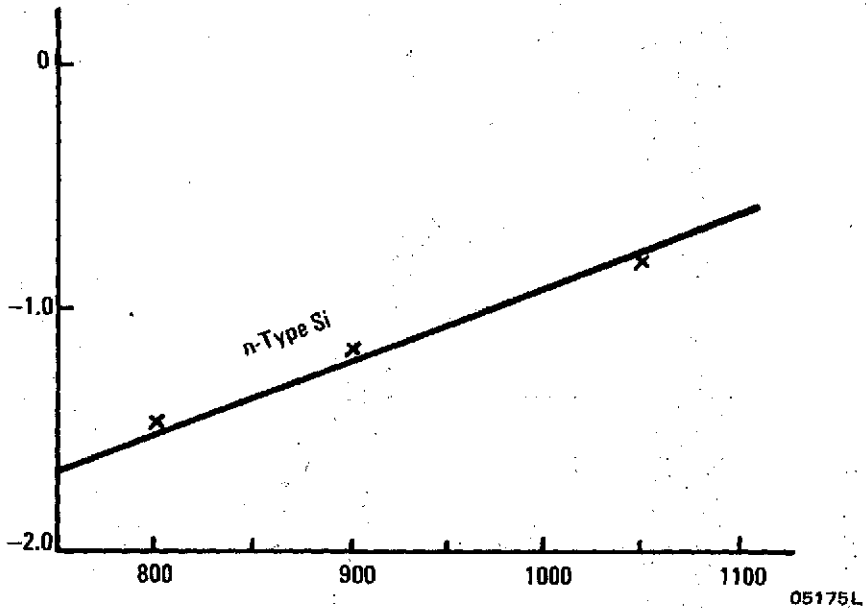


Figure 24. Variation of Si_3N_4/SiO_2 Flatband as Function of Deposition Temperature

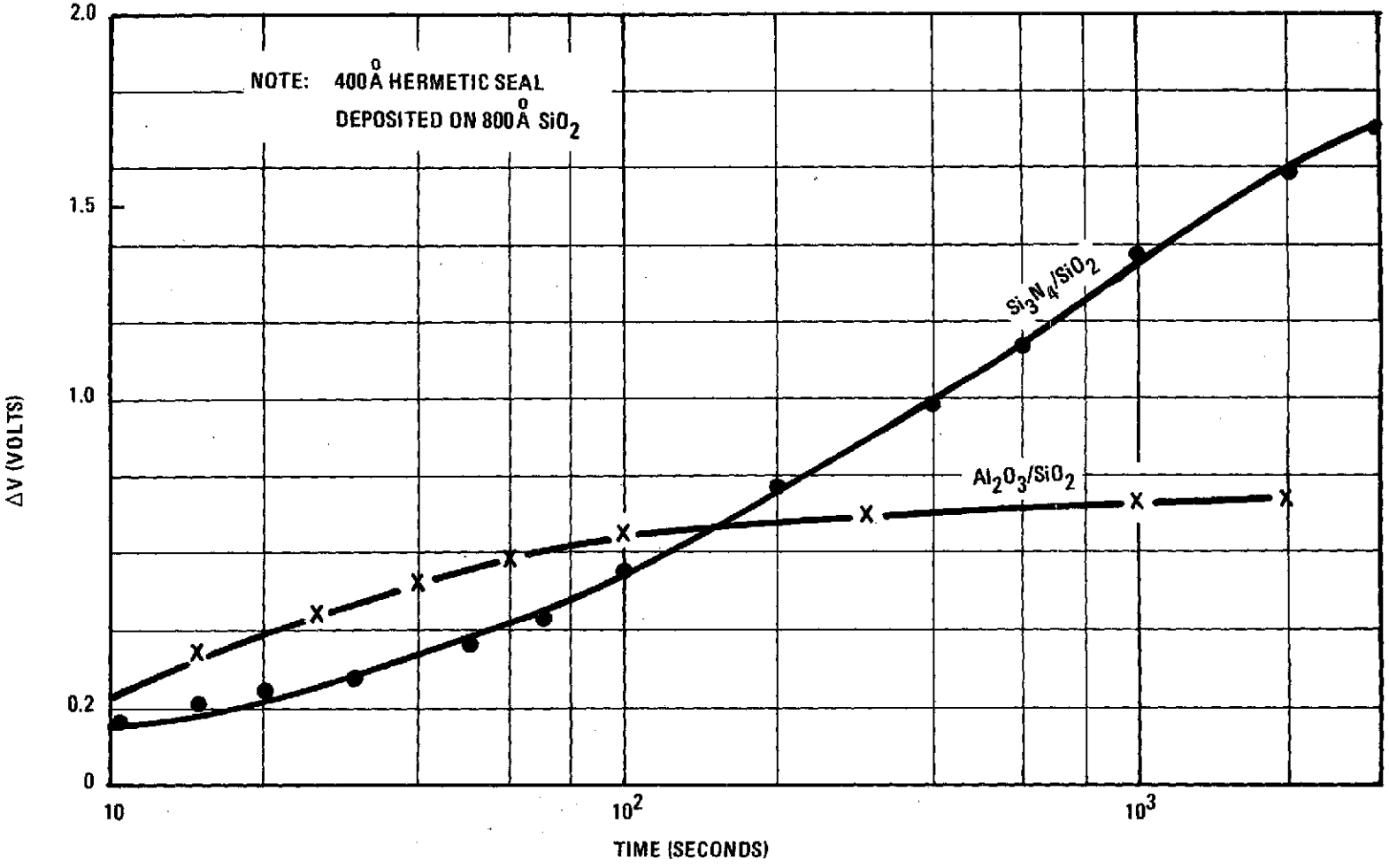


Figure 25. Thick SiO_2 Samples Tested at 300°C Under −10-Volt Bias

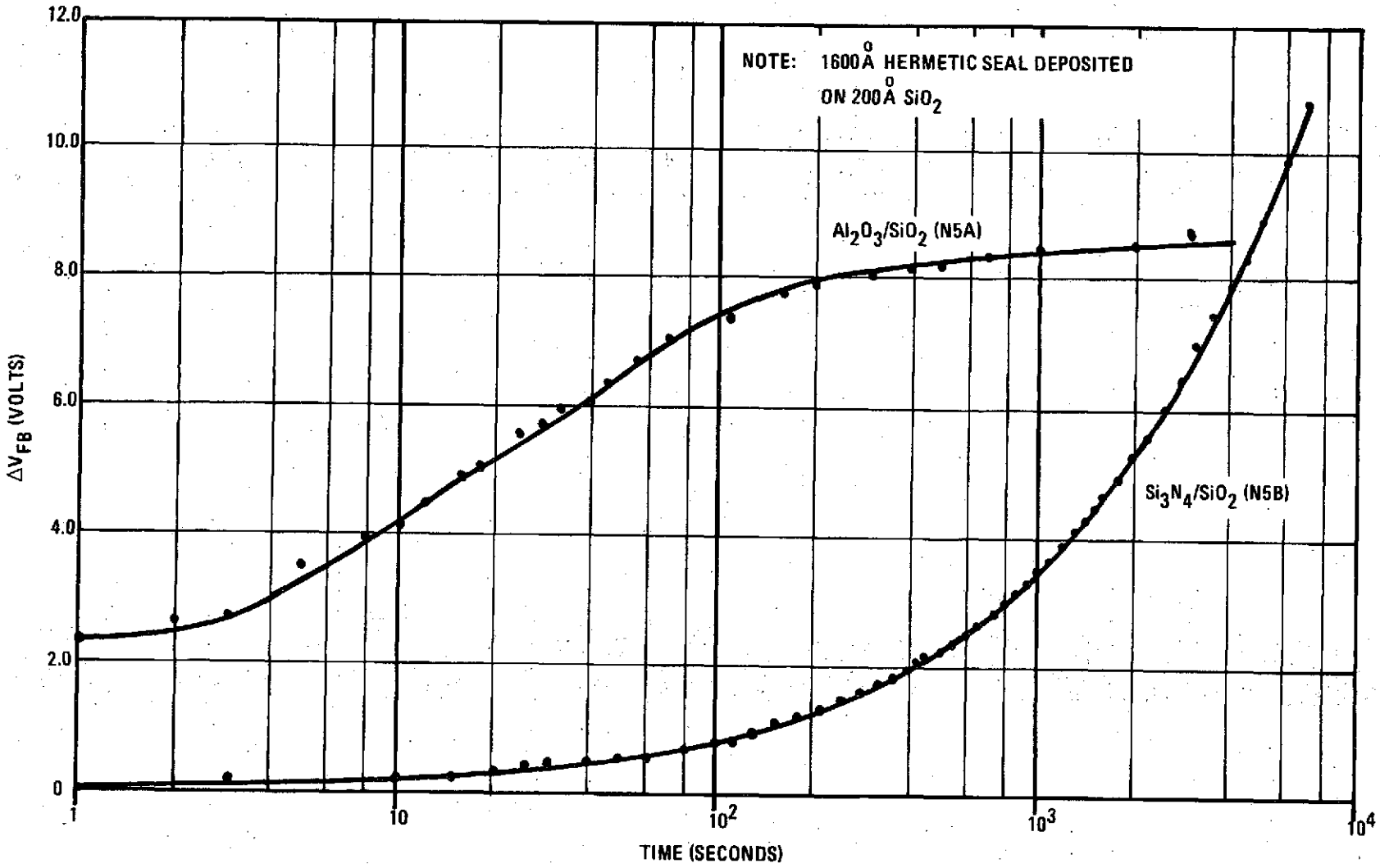


Figure 26. Thin SiO_2 Samples Tested at 300°C Under −10-Volt Bias

shifts are small for short test times. The increase of threshold with time can again be explained by charging at the interface. It should be noted that while some of these shifts seem severe, the test temperature is so high that shifts at room temperature may be immeasurably small and it might be many years under bias before the threshold shifts become noticeable. How important this problem is will depend upon its activation energy. Obtaining this information is not a simple matter as can be seen from Figure 27, which shows the variation of flatband with time for various heat-treatment temperatures. The sample shown was the least stable of the lots tested.

The high-temperature (300°C) stress tests have been correlated to 125°C operating-life data. The total time span was 3000 hours. Figures 28 and 29 show the shift in threshold voltage with time. The n-MOS transistors with Si_3N_4 show initially slightly less shift, reducing the threshold voltage, while those with Al_2O_3 increase the threshold voltage. In either case the total shift is approximately 0.15 volt at 3000 hours. The n-MOS transistors with Si_3N_4 seem to have a larger slope of change in threshold voltage at the end of the testing period. The p-MOS transistors in Figure 29 show that the Al_2O_3 units are far more stable than the Si_3N_4 units, showing decreases in threshold voltage of about 0.1 and 0.4 volt, respectively.

2. THRESHOLD-VOLTAGE AND CHANNEL-CONCENTRATION MEASUREMENTS

A statistical technique that is described in Appendix A has been used to characterize the MOS transistors precisely. The threshold voltage is obtained by extrapolation through a least square fit of $\sqrt{I_D}$ - V_G data points. These data are also measured (on automatic test equipment) as a function of n-substrate or p-well bias, see Table IV. The intercepts (Table V) again are used in a second linear regression to obtain the channel concentration, see Table VI. Further data obtained are the correlation coefficients (indicates mathematically how far the measured points are from the fitted straight line), the K-factor, and when used as a function of temperature, the temperature coefficient of the channel mobility.

Once threshold voltage and channel concentration are determined, it is possible to compare the self consistency of the data and assign the difference

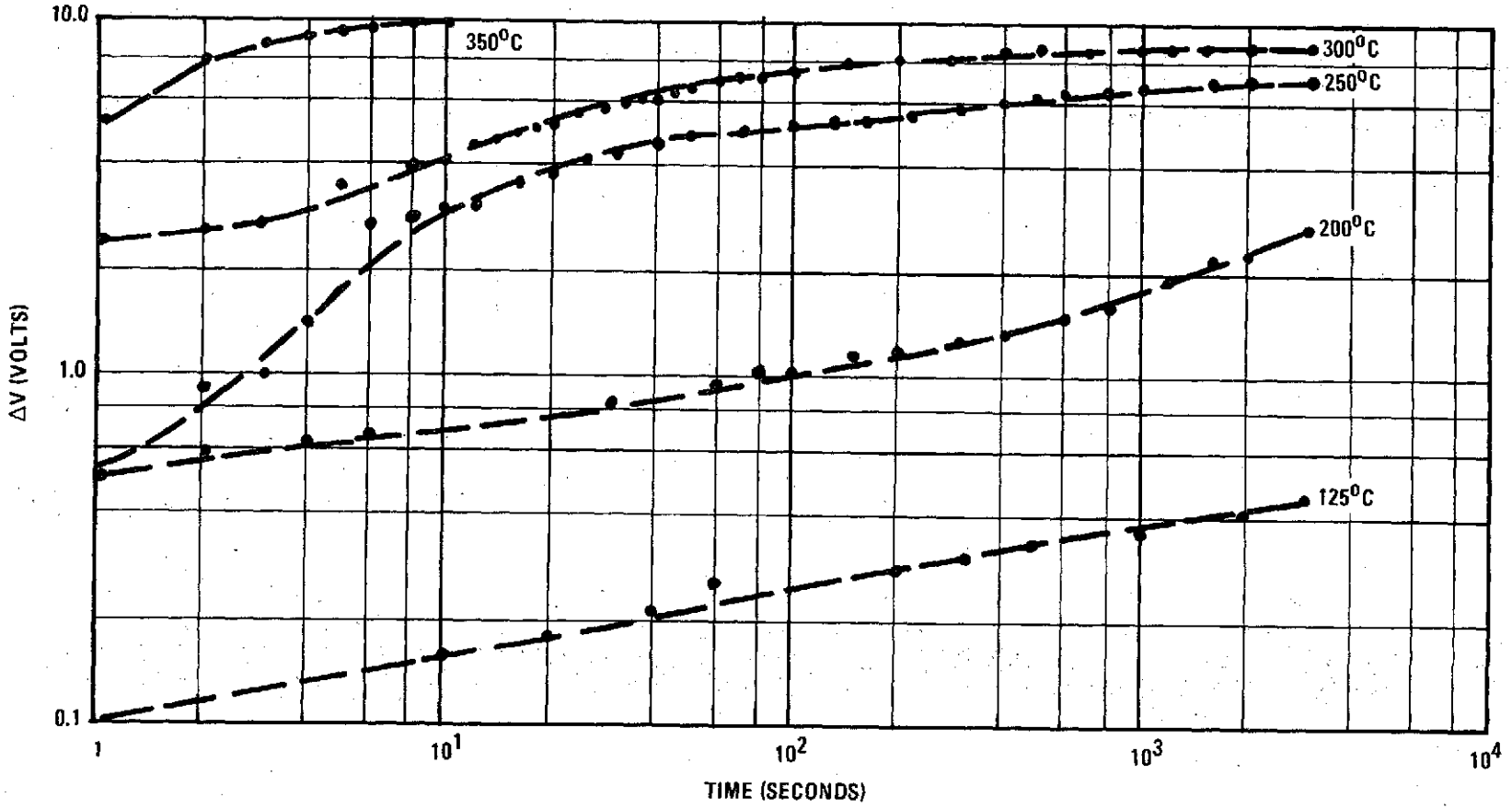


Figure 27. Variation of ΔV with Time for Various Temperatures

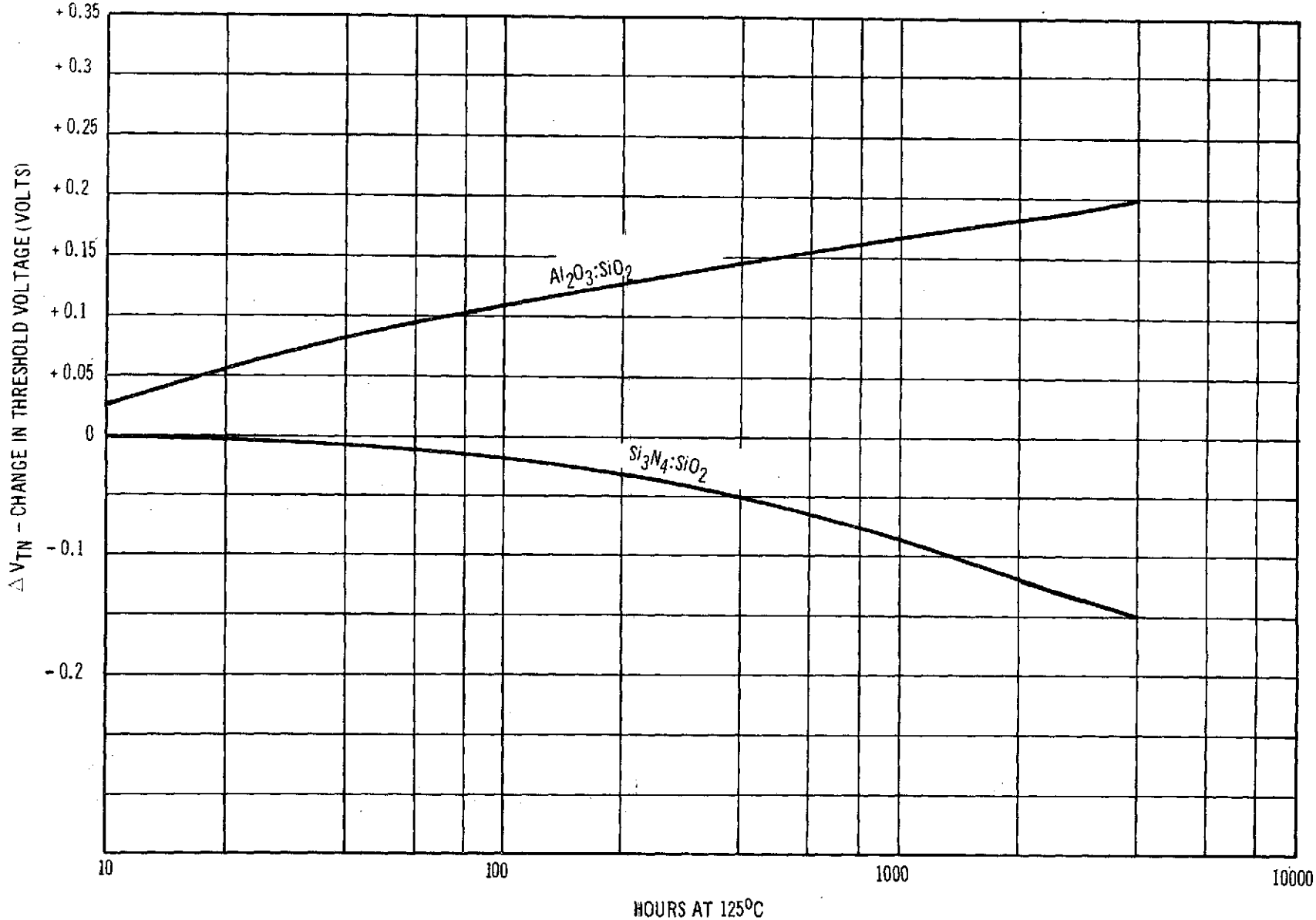


Figure 28. Threshold Voltage Change of n-MOS Units Under +10-Volt Bias at 125°C With Time at Temperature

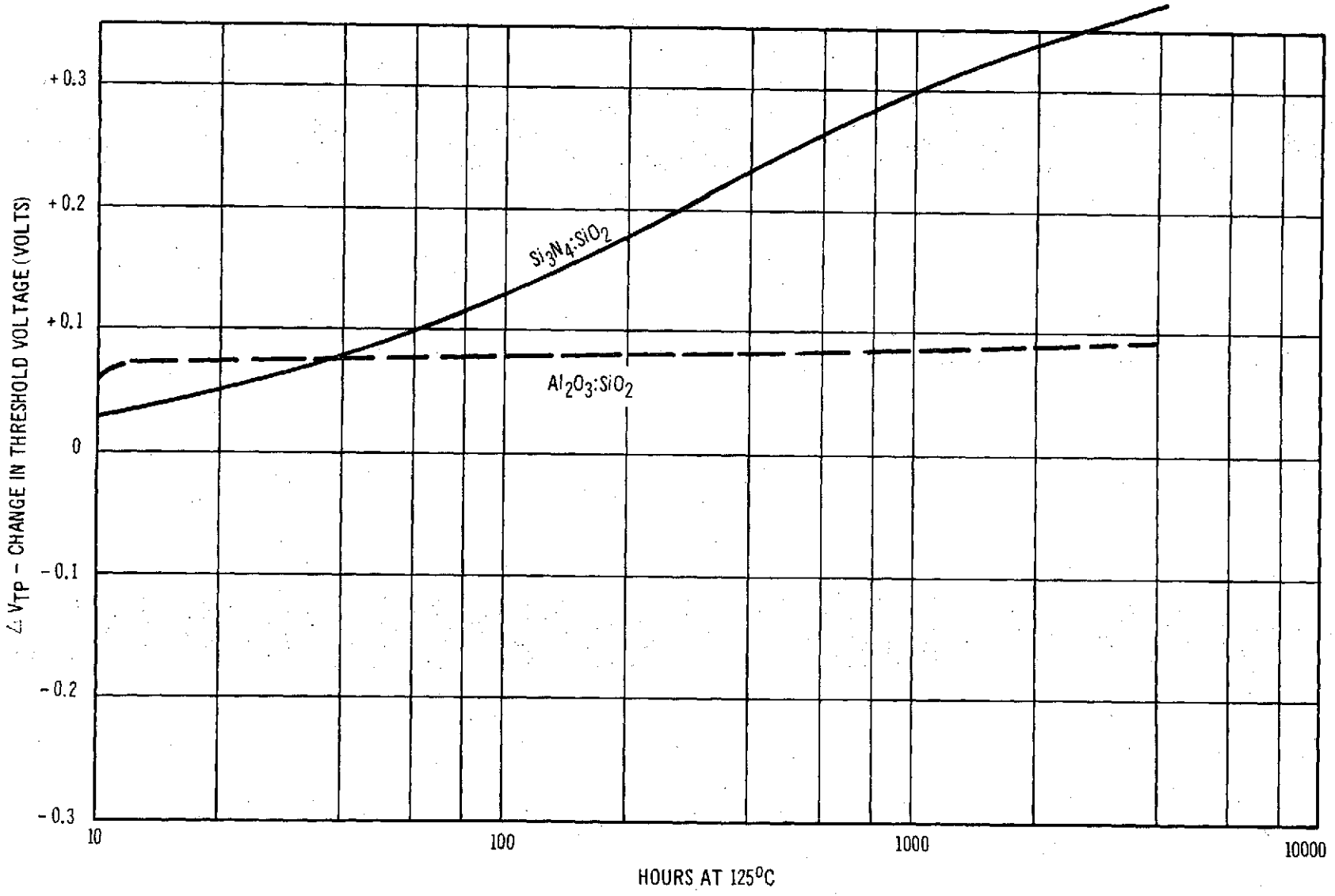


Figure 29. Threshold Change of the p-MOS Units Under −10-Volt Bias at 125°C With Time

TABLE IV. PRIMARY DATA FOR TYPICAL n-MOS AND p-MOS TRANSISTORS WITH COMPOSITE GATE DIELECTRIC

TC 1010 (800 A SIO2, 350 A AL2O3) LOT 219, WAFER 1, PELLET #20 N

TEMP DEG	VSUB VOLTS	VG (VOLTS) @ ID= 1	16	49	100	169	256	361	484	625 UA
25	0.0	1.36	1.60	1.78	1.94	2.08	2.23	2.39	2.53	2.68
25	0.4	1.66	1.88	2.04	2.19	2.34	2.49	2.64	2.78	2.93
25	1.0	2.01	2.22	2.39	2.53	2.67	2.81	2.96	3.10	3.24
25	1.8	2.40	2.61	2.76	2.90	3.04	3.18	3.32	3.46	3.60
25	3.0	2.90	3.09	3.24	3.39	3.51	3.65	3.78	3.91	4.07
25	5.0	3.57	3.76	3.90	4.05	4.18	4.31	4.44	4.56	4.70
25	8.0	4.40	4.59	4.72	4.85	4.97	5.09	5.22	5.34	5.47
25	12.0	5.29	5.48	5.60	5.72	5.84	5.96	6.08	6.20	6.32

TC 1010 (800 A SIO2, 350 A AL2O3) LOT 219, WAFER 1, PELLET #6 P

TEMP DEG	VSUB VOLTS	VG (VOLTS) @ ID= 1	16	49	100	169	256	361	484	625 UA
25	0.0	0.99	1.23	1.36	1.49	1.61	1.73	1.85	1.97	2.09
25	0.4	1.23	1.39	1.52	1.64	1.75	1.88	2.00	2.10	2.23
25	1.0	1.43	1.58	1.70	1.82	1.93	2.03	2.15	2.27	2.39
25	1.8	1.63	1.77	1.89	1.99	2.10	2.22	2.33	2.45	2.57
25	3.0	1.86	2.01	2.11	2.22	2.33	2.44	2.55	2.67	2.79
25	5.0	2.15	2.29	2.41	2.51	2.62	2.73	2.84	2.95	3.07
25	8.0	2.49	2.63	2.74	2.85	2.95	3.06	3.17	3.28	3.40
25	12.0	2.77	2.97	3.08	3.19	3.29	3.39	3.51	3.62	3.73

TABLE V. CALCULATED, ZERO CURRENT, THRESHOLD VOLTAGE AS A FUNCTION OF SUBSTRATE BIAS AND STATISTICAL BLOCK SIZE FOR n-MOS AND p-MOS TRANSISTORS OF PRECEDING TABLE

TC 1010 (800 A SIO2, 350 A AL2O3) LOT 219, WAFER 1, PELLET #20 N

ID RANGE UA	VT (VOLTS) @ VSUB= 0.0	0.4	1.0	1.8	3.0	5.0	8.0	12.0 VOLTS
TEMP= 25 DEG C								
1-625	1.374	1.658	2.010	2.398	2.892	3.567	4.400	5.292
1-484	1.367	1.653	2.005	2.394	2.892	3.563	4.397	5.289
16-625	1.417	1.689	2.043	2.428	2.917	3.594	4.428	5.320
16-484	1.413	1.687	2.040	2.427	2.922	3.593	4.426	5.320
49-625	1.439	1.697	2.056	2.433	2.926	3.605	4.431	5.320
49-484	1.433	1.695	2.056	2.433	2.936	3.605	4.434	5.320

TC 1010 (800 A SIO2, 350 A AL2O3) LOT 219, WAFER 1, PELLET #6 P

ID RANGE UA	VT (VOLTS) @ VSUB= 0.0	0.4	1.0	1.8	3.0	5.0	8.0	12.0 VOLTS
TEMP= 25 DEG C								
1-625	1.025	1.219	1.415	1.606	1.840	2.132	2.471	2.789
1-484	1.018	1.217	1.415	1.608	1.842	2.133	2.472	2.786
16-625	1.075	1.239	1.431	1.616	1.851	2.145	2.483	2.825
16-484	1.073	1.239	1.434	1.620	1.856	2.143	2.487	2.827
49-625	1.083	1.246	1.434	1.614	1.842	2.146	2.481	2.824
49-484	1.081	1.247	1.439	1.619	1.848	2.152	2.488	2.827

TABLE VI. CALCULATED CHANNEL CONCENTRATION AS A FUNCTION OF THE STATISTICAL BLOCK SIZE FOR n-MOS AND p-MOS TRANSISTORS OF PRECEDING TABLES. (COMPUTATION ERRORS INCREASE FOR THE n-MOS TRANSISTORS WITH DECREASING DIFFERENCES OF SUBSTRATE BIAS.)

TC 1010 (800 A SIO2, 350 A AL2O3) LOT 219,WAFER 1,PELLET #20 N

N (DIFFERENTIALS) X 1.0E+16 (CM-3) FOR VSUB2 - VSUB1

ID RANGE	12.0	8.0	5.0	12.0	8.0	5.0	12.0	8.0	5.0	
UA	0.0	0.0	0.0	-0.4	-0.4	-0.4	-1.0	-1.0	-1.0	VOLTS
TEMP=	25 DEG C									
										AVG=
1-625	1.66	1.65	1.61	1.42	1.35	1.21	1.15	1.02	0.80	1.32
1-484	1.66	1.65	1.61	1.42	1.35	1.21	1.16	1.02	0.80	1.32
16-625	1.64	1.63	1.59	1.42	1.35	1.21	1.15	1.01	0.80	1.31
16-484	1.65	1.64	1.59	1.42	1.35	1.21	1.15	1.02	0.80	1.31
49-625	1.63	1.62	1.57	1.41	1.34	1.21	1.14	1.01	0.79	1.30
49-484	1.63	1.62	1.58	1.41	1.35	1.21	1.14	1.01	0.79	1.30
AVG=	1.64	1.63	1.59	1.42	1.35	1.21	1.15	1.01	0.80	

TC 1010 (800 A SIO2, 350 A AL2O3) LOT 219,WAFER 1,PELLET #6 P

N (LEAST SQUARE FIT) X 1.0E+15 (CM-3) @ VSUB RANGE=

ID RANGE	0.0	0.0	0.0	0.4	0.4	0.4	1.0	1.0	1.0	
UA	-12.0	-8.0	-5.0	-12.0	-8.0	-5.0	-12.0	-8.0	-5.0	VOLTS
TEMP=	25 DEG C									
										AVG=
1-625	5.09	5.34	5.56	4.95	5.18	5.37	4.83	5.07	5.23	5.18
1-484	5.09	5.36	5.61	4.95	5.19	5.38	4.82	5.07	5.24	5.19
16-625	5.07	5.25	5.43	4.99	5.16	5.33	4.90	5.06	5.22	5.16
16-484	5.08	5.27	5.46	4.99	5.17	5.35	4.89	5.07	5.22	5.17
49-625	5.05	5.22	5.37	4.97	5.14	5.28	4.90	5.06	5.21	5.13
49-484	5.06	5.24	5.41	4.98	5.15	5.30	4.89	5.06	5.21	5.14
AVG=	5.07	5.28	5.48	4.97	5.17	5.33	4.87	5.07	5.22	

from the ideal MOS characteristics to an effective interface state density. (The interface voltage ϕ_{ii} between SiO_2 and Al_2O_3 is reflected into the silicon/SiO_2 interface due to a lack of better information on how to allocate its charge.) Table VII summarizes the data for 10 n-MOS and 10 p-MOS transistors from Lot 219. The effective interface state density calculates to about 3 to 5 x 10^{10} cm^{-2}, a value consistent with other measurements on (100) silicon. The interface states cause a shift in threshold voltage of + 0.1 volt for both n-MOS and p-MOS transistors. This is another indication of how well controlled the MOS process technology has become.

3. LIFE TESTS

a. Construction of Life-Test Facilities

In order to test out the processes and to obtain preliminary data, an in-group flexible life-test step-stress setup was constructed. The following describes the equipment and the test procedures.

The beam-leaded TC1010 (CD4007) triple-complementary inverter circuits were used to demonstrate the steady-state life testing as prescribed by MIL-STD-883. The devices converted as standard COS/MOS inverters, Figure 30, are subjected to a steady-state supply voltage of 10 volts (such that most junctions are reverse biased) and to an environmental test chamber temperature of 125°C. The units are mounted on 2-ounce copper-glass-epoxy printed circuit boards containing 30 14-lead sockets, as shown in Figure 31. The boards are designed so that half of the units have the n-channel and p-channel gates grounded and the other half have the gates tied to the supply voltage of 10 volts.

b. Life-Test Schedule

To fully characterize the beam-lead devices fabricated for this program, a broad life, step-stress, and environmental test program was set up, as shown in Figure 32. Standard life-testing and environmental-testing facilities using AQL standards are employed to test the best batches of devices made under "proven-out" processes.

TABLE VII. SUMMARY OF (EXTRAPOLATED) THRESHOLD VOLTAGES (V_t), CHANNEL CONCENTRATION (N), SURFACE STATE DENSITIES (N_{ss}), AND THRESHOLD VOLTAGES FOR ZERO SURFACE STATE DENSITIES FOR TC1010 LOT 219

V_T (V)	N_p (1) (cm^{-3})	N_{ss} (1) (cm^{-2})	$V_T(N_{ss} = 0)$ (1) (V)
1.27	1.39×10^{16}	4.33×10^{10}	1.393
1.36	1.68×10^{16}	5.22×10^{10}	1.509
1.45	1.75×10^{16}	2.99×10^{10}	1.535
1.41	1.65×10^{16}	3.06×10^{10}	1.497
1.37	1.36×10^{16}	-1.03×10^{10}*	1.381
1.39	1.65×10^{16}	3.77×10^{10}	1.497
1.42	1.77×10^{16}	4.30×10^{10}	1.542
1.45	1.86×10^{16}	4.41×10^{10}	1.575
1.47	1.79×10^{16}	2.80×10^{10}	1.550
1.39	1.44×10^{16}	8.41×10^{9}	1.414

V_T (V)	N_n (2) (cm^{-3})	ρ_p (2) (Ω cm)	N_{ss} (cm^{-3})	$V_T(N_{ss} = 0)$ (V)
-1.04	5.25×10^{15}	0.92	3.39×10^{10}	-0.947
-1.07	5.07×10^{15}	0.95	4.76×10^{10}	-0.935
-1.05	5.29×10^{15}	0.92	3.53×10^{10}	-0.950
-0.92	5.25×10^{15}	0.92	-9.50×10^{9}*	-0.947
-0.97	4.77×10^{15}	1.00	1.98×10^{10}	-0.914
-1.03	4.90×10^{15}	0.98	3.77×10^{10}	-0.923
-1.02	4.75×10^{15}	1.01	3.79×10^{10}	-0.912
-0.96	4.80×10^{15}	1.00	1.55×10^{10}	-0.916
-0.92	5.25×10^{15}	0.92	9.50×10^{9}	-0.947

Notes: 1. Derived from Eq. (12) of Appendix A for 0 to 12-volt bias.

2. Derived from Eq. (14) of Appendix A.

*Negative values of N_{ss} are due to slight inaccuracies in channel concentration.

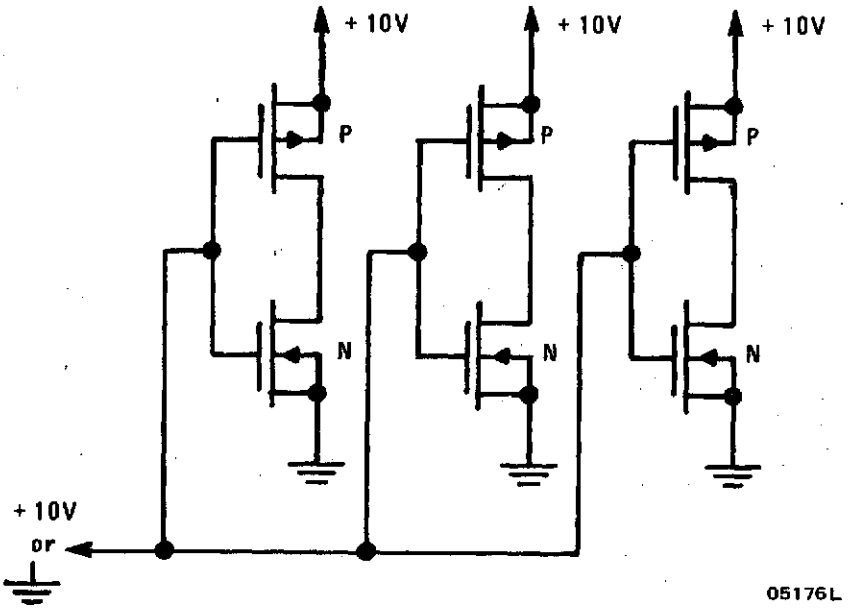
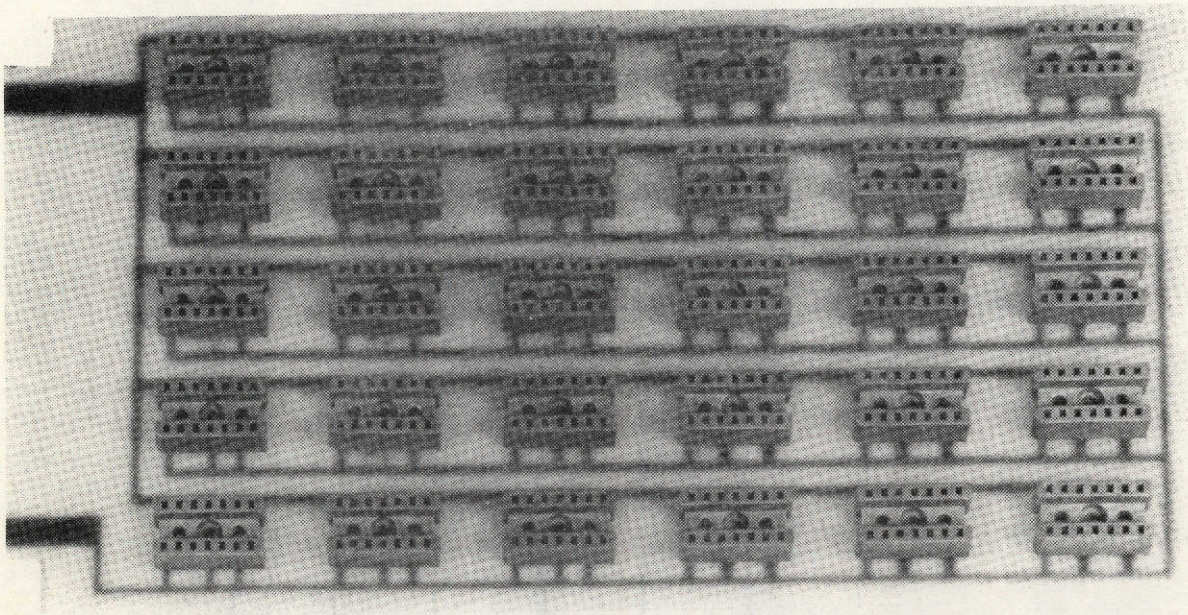
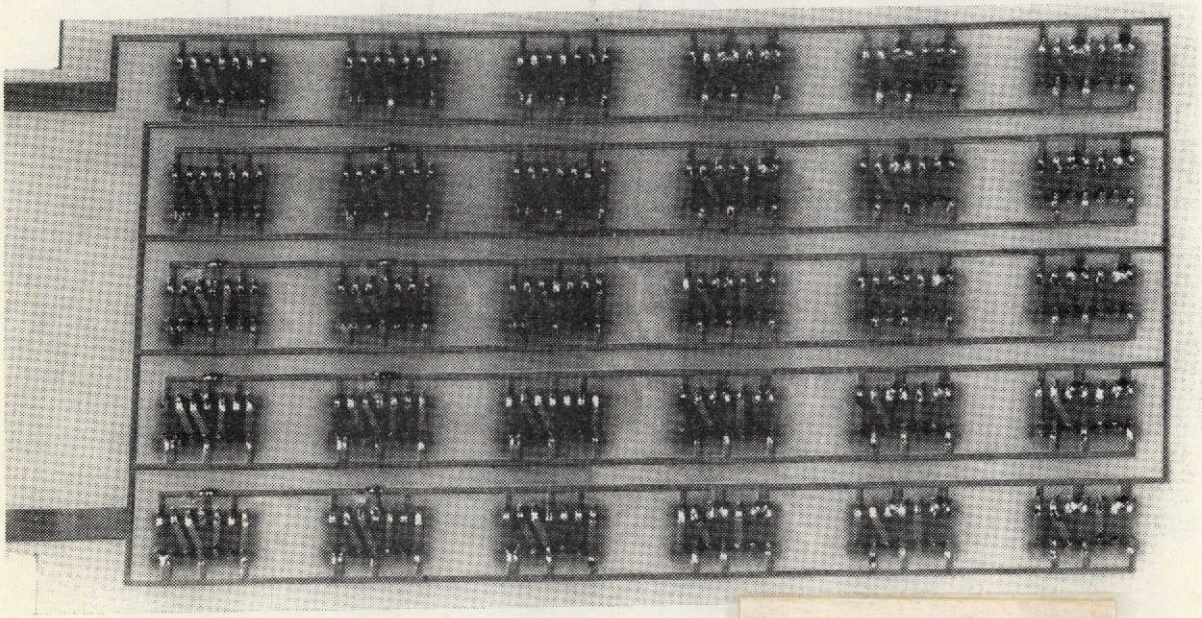


Figure 30. COS/MOS CD4007 Connected as Inverters for Life Testing



A. TOP VIEW



B. BOTTOM VIEW

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05181V

Figure 31. 125°C Life Testing Boards

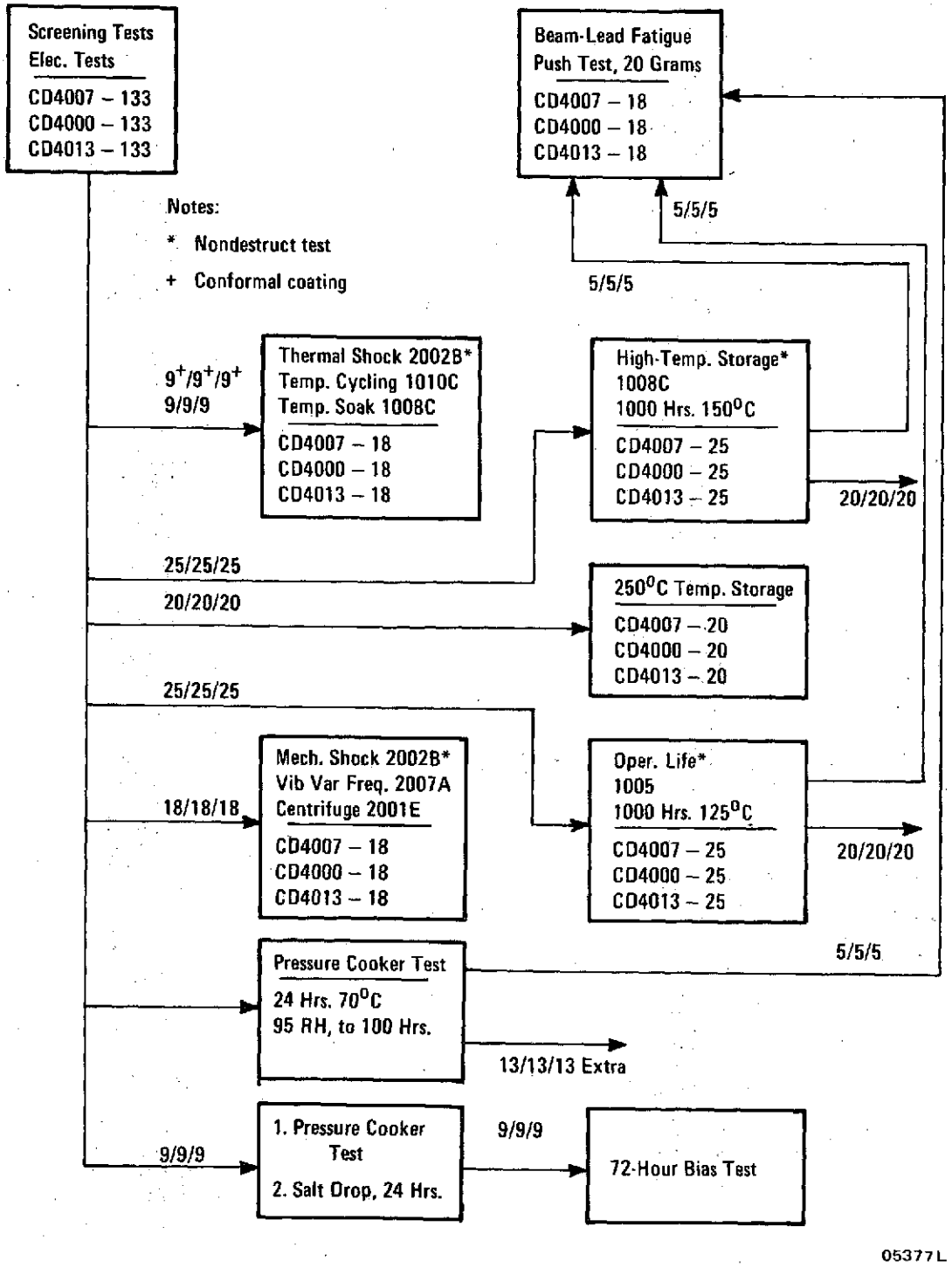


Figure 32. Environmental Test Program for CD4007, CD4000, and CD4013 Devices

The initial units (i.e., zero hour units) are subjected to the following tests at 25°C (using a computerized automatic tester):

a. Continuity test (establishing contact, diode forward drop, and other voltage drops of the unit)

b. Well-to-substrate leakage and breakdown checks

c. Diffusion leakages and breakdown checks

d. n-channel gate-to-well and p-channel gate-to-substrate leakages and breakdown checks

e. Channel (i.e., unit-off) leakages and breakdown check

f. Threshold levels

g. Transconductance

c. Life-Test Results

After passing all parameter tests, 133 units are selected as the sample size and exposed to the testing environment for a number of specified hours. The units are then moved and retested at 25°C. This procedure operates periodically until either the units fail or until a total of 2400 hours have elapsed. After the total testing procedure is completed, the mean time of failure (MTF) of the sample is established with a description of the plausible mode(s) of failure.

Of the 44 parameters tested on each device, only the thresholds which were under constant ±10-volt bias showed any significant and consistent change. The well leakage, however, showed an increase at the 2400-hour point, but this could have been due to measurement error caused by computer-system noise. The one-time increase in leakage was from 20 to 40 nanoamperes at 17 volts, which was well within the 100-nanoampere specification.

Threshold voltages were monitored at 10 microamperes before and after operation under bias at 125°C and the calculated changes are given in Figures 28 and 29. The former gives the changes for the n-type transistors (both nitride and alumina) which were tested under positive bias and the latter for the p-type transistors which were tested under negative bias. Those n- and p-type transistors tested under zero bias exhibited no changes in threshold.

Histograms of leakage current (I_{LP}, I_{LN}), threshold voltage (V_{tp}, V_{th}) at 10 microamperes drain current and output drive current (I_{DN}, I_{DP}) at V_{GS} = 10 volts and V_{DS} = 0.5 volt are shown in Figures 33 through 38. There were no device failures during this testing period. The only curve which shows any significant change is that for the threshold voltage of the p transistors. The threshold voltages of three of these units decreased to 0 volts after 168 hours. The lower value threshold devices, centered at 0.6 volt, shifted on the average of 0.1 volt. No significant changes were observed in the other parameters. As shown, there is no measurable difference between 168-hour and 408-hour data for all parameters, except V_{tp}, and all parameters remained unchanged at the 1000-hour measurement.

The following data summarize the results of the environmental tests performed on CD4007, hermetically sealed, beam-lead units. The numbers listed in the high-temperature-storage tests are push-off forces in grams.

			Quantity		
Test	Conditions	Duration	Total	Fails	Notes
Moisture Resistance	Mil-Std-883 Method 1004	20 days	25	0	
Mechanical Shock	1500g 0.5 MS	5 blows each plane	9	3	1
The following two tests were conducted in series using the same units.					
Pressure Cooker	15 psi with salt contamination	24 hrs.	20	2	2
Bias Life	200°C	24 hrs.	8	2	3

Notes:

1. One unit had a broken pellet.
   One unit had an open circuit.
   One unit had a low breakdown voltage.

2. One unit had an open circuit.
   One unit was degraded electrically.

3. Both units were electrically degraded.

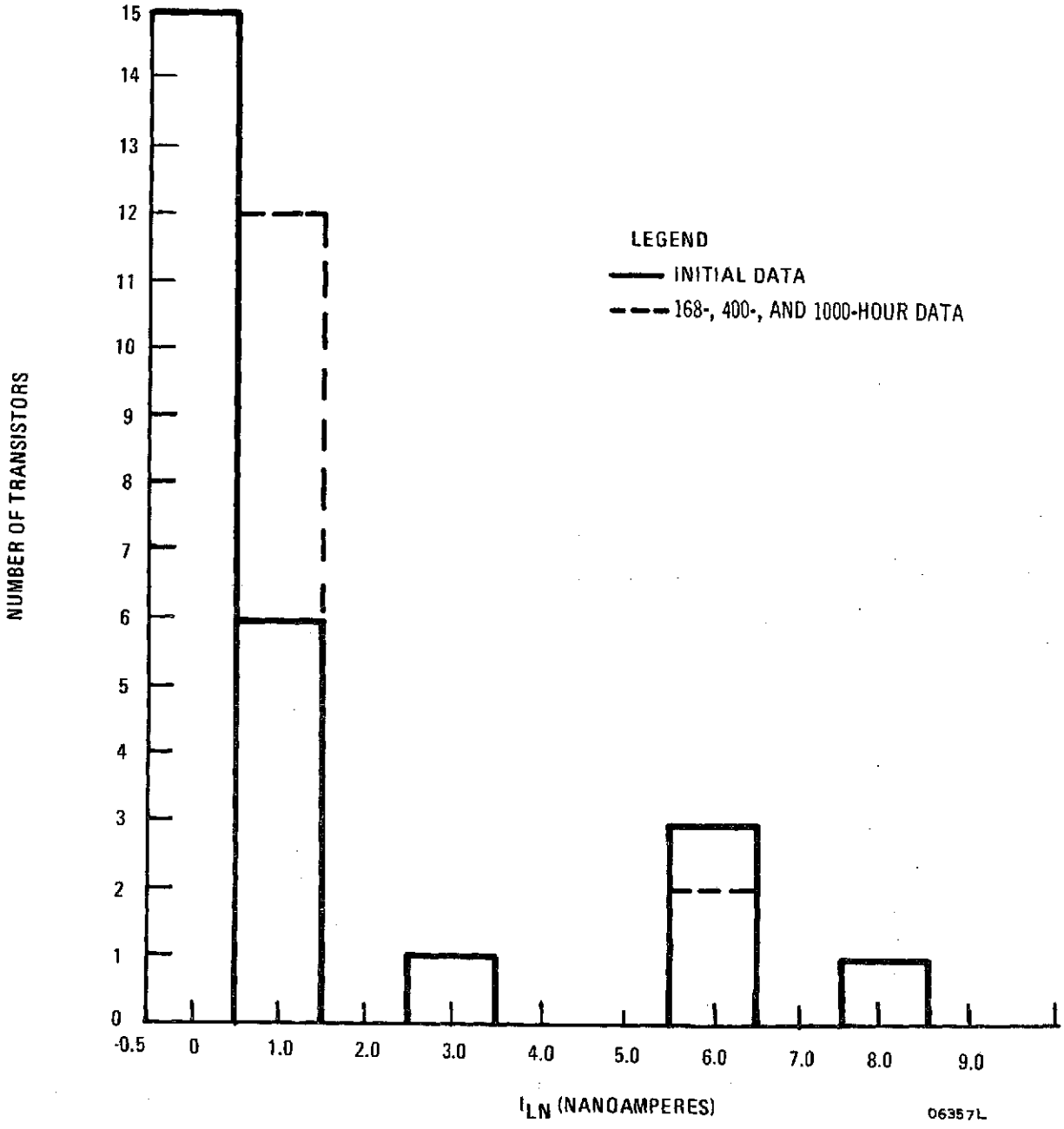


Figure 33. Operating Life, n-Transistor Leakage Current (I_{LN})

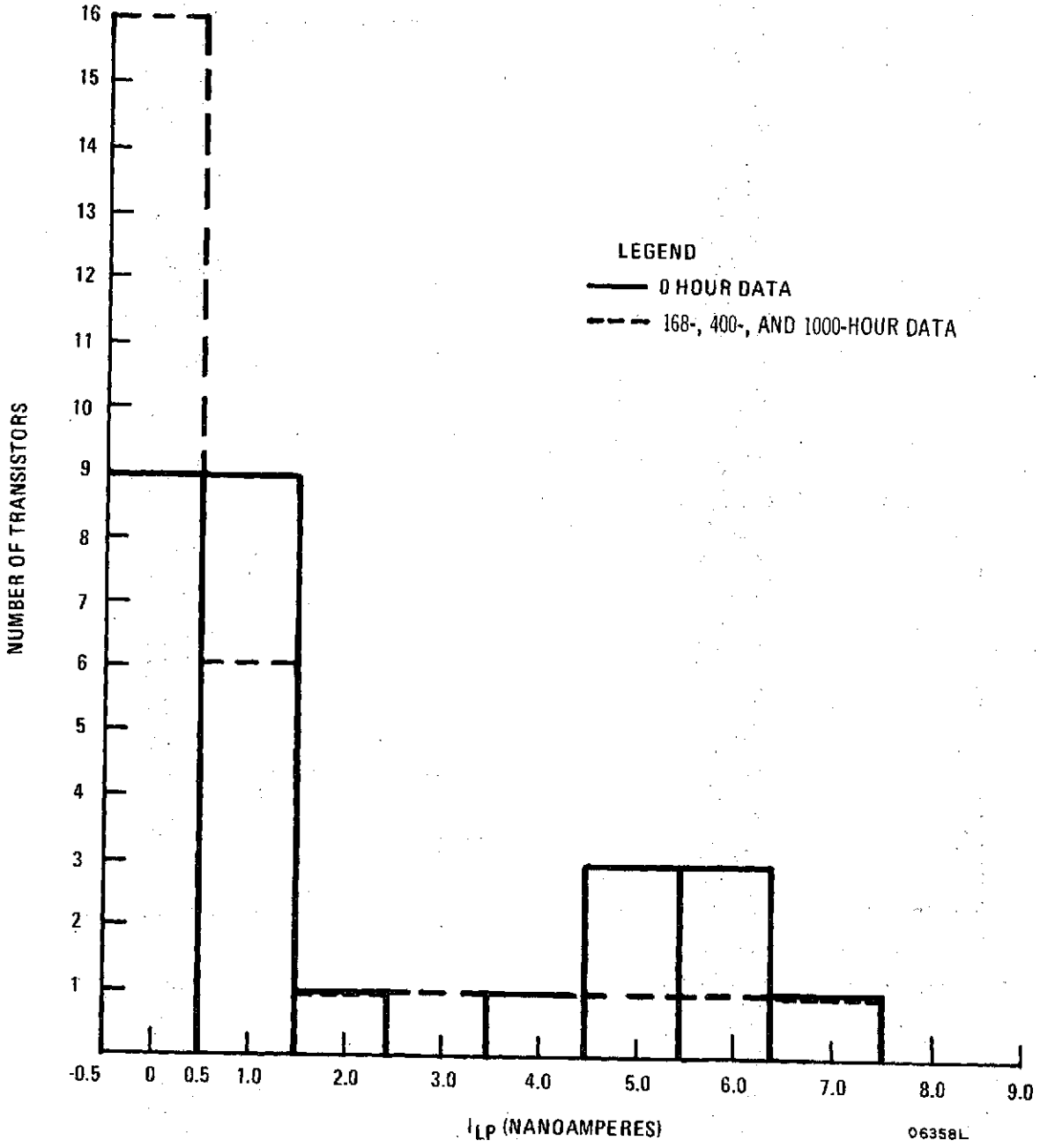
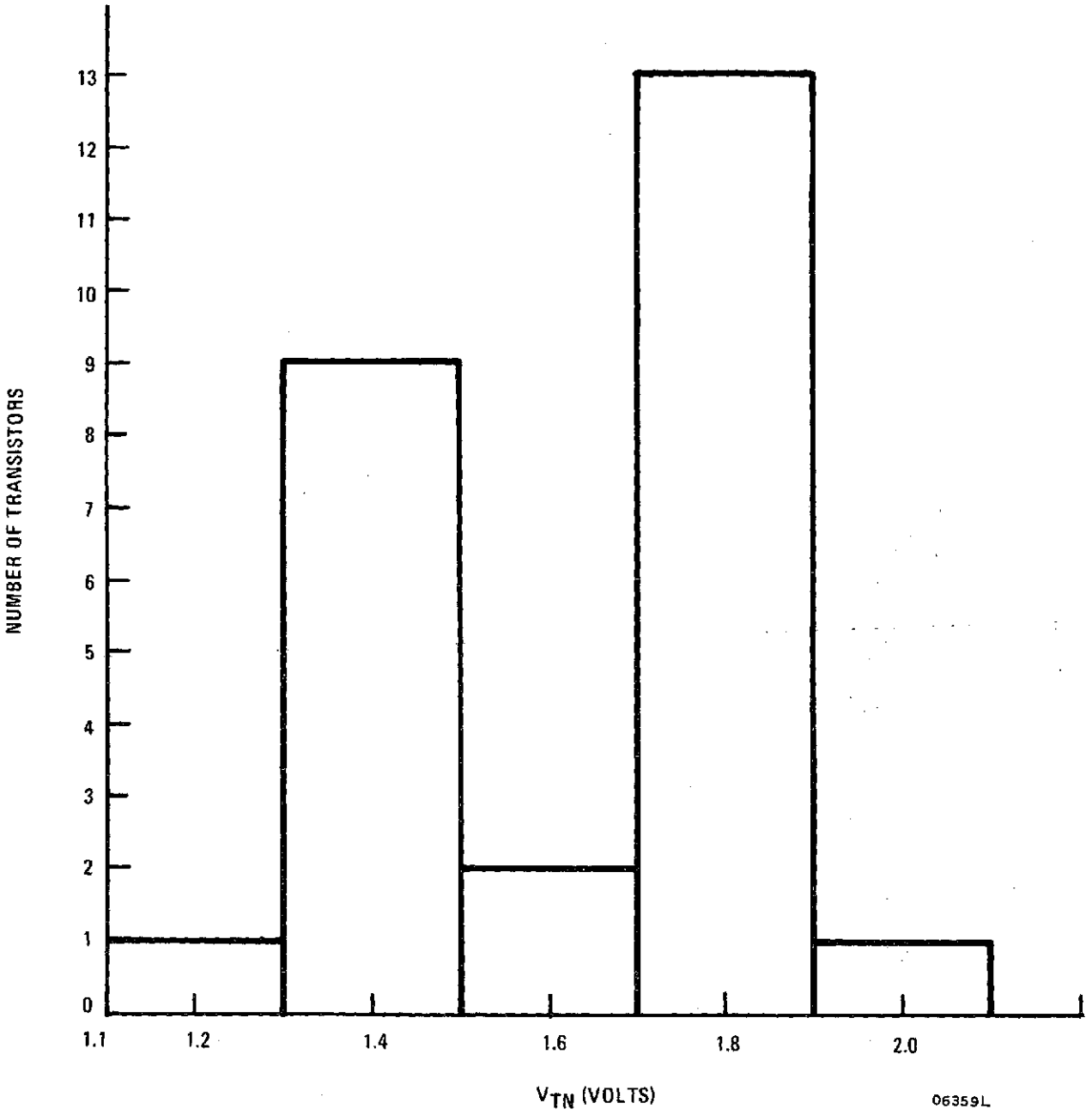


Figure 34. Operating Life, p-Transistor Leakage Current (I_{LP})



NOTE: NO MEASURABLE CHANGE
FROM INITIAL DATA AT
168, 408, AND 1000 HOURS

Figure 35. Operating Life, n-Transistor Thresholds (V_{TN})

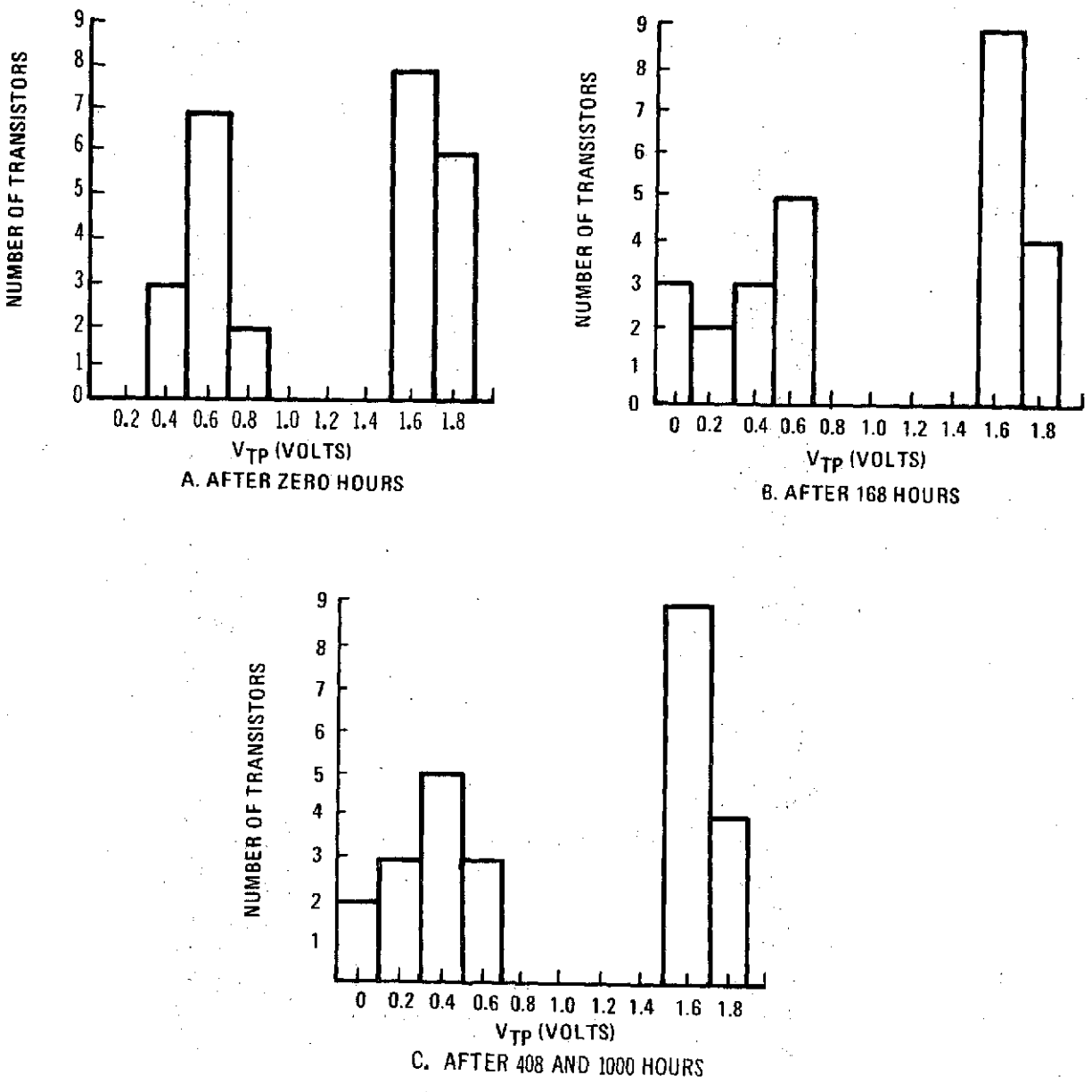


Figure 36. Operating Life, p-Transistor Threshold

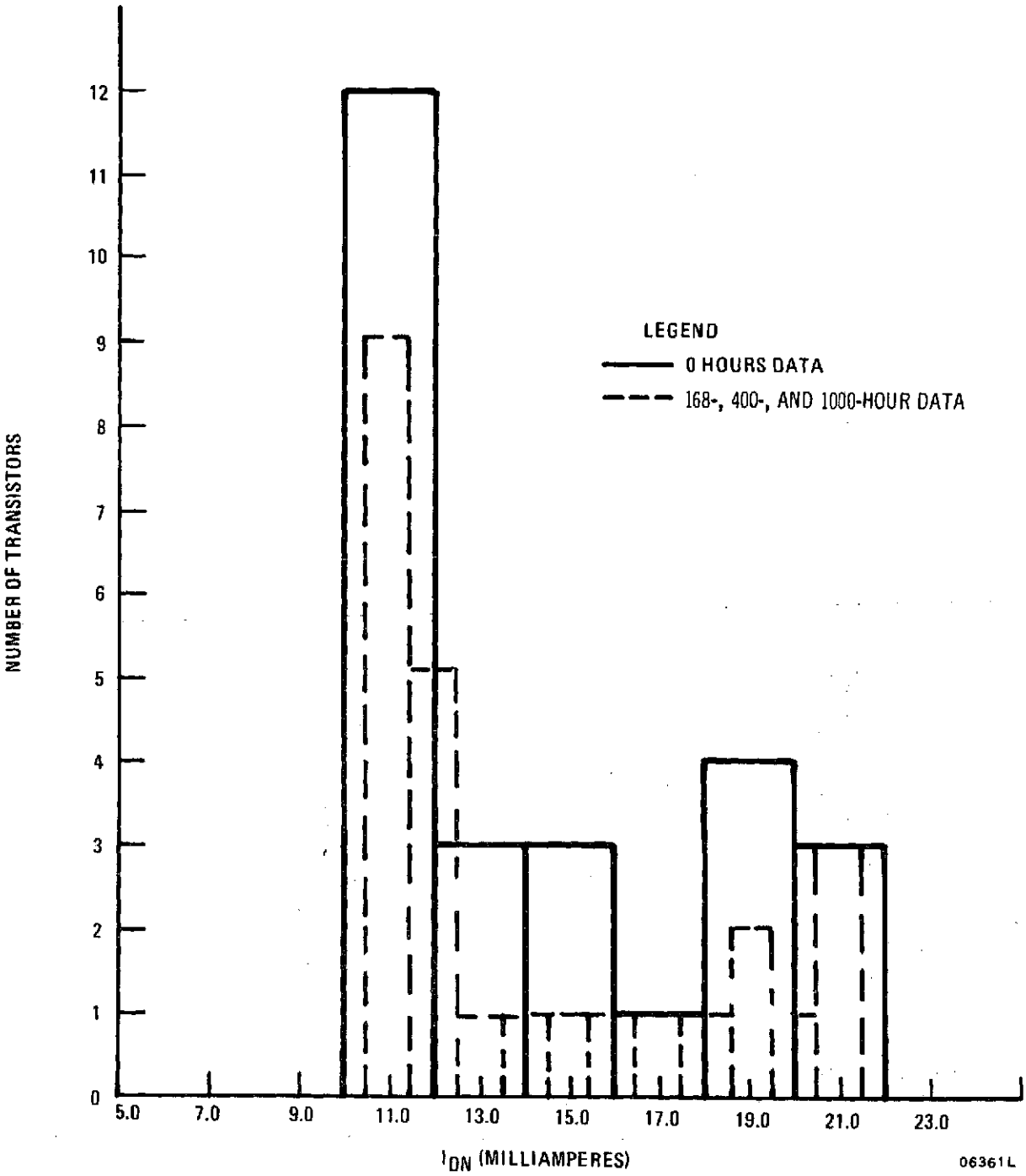


Figure 37. Operating Life, n-Transistor Output Current, I_{DN}

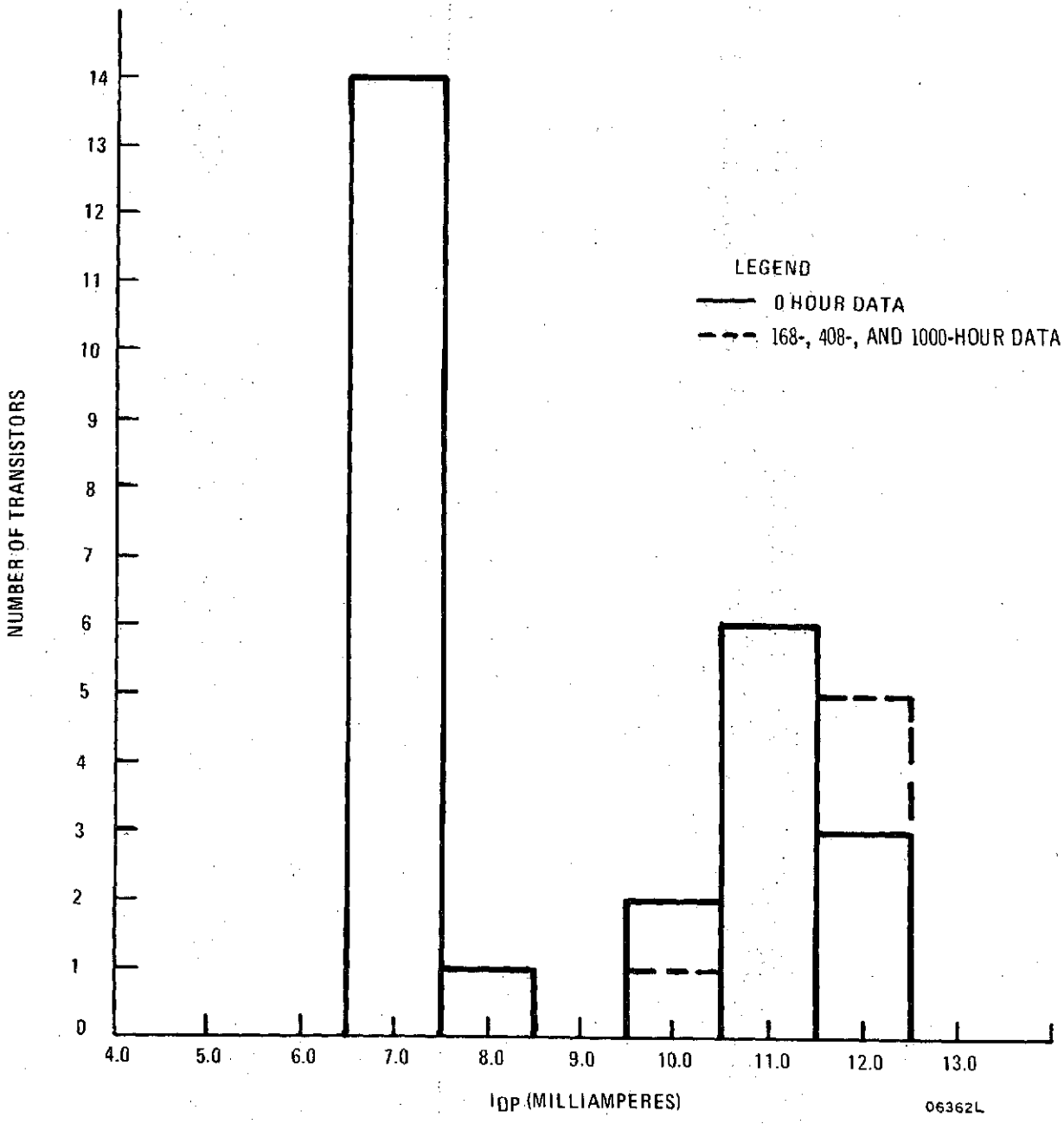


Figure 38. Operating Life, p-Transistor Output Current, I_{DP}

High-temperature-storage step stress (^{o}C) versus push-off force in grams. (1 wafer = 12 devices)

Step	Temp (^{o}C)	Time (Hrs.)	Push-off (grams)
1	150	250	68, 82
2	200	250	66, 68
3	250	250	60, 72
4	300	250	63, 70, 100, 100, 100+, 100+.

High-temperature storage (^{o}C) versus push-off force in grams (4 wafers)

Wafer	Temp (^{o}C)	Time (Hrs.)	Push-off (grams)
1	25	1000	18, 28, 34, 46, 48, 50, 52, 54, 58
2	150	1000	32, 42, 42, 46, 48, 54, 54, 58, 66, 70
3	200	1000	58, 62, 64, 78, 78, 80, 82, 84
4	250	1000	85, 85, 88, 88, 90, 90, 90, 90, 90, 90

Wafer	Min	Median	Max
1	18	38	58
2	32	51	70
3	58	70	82
4	85	87.5	90

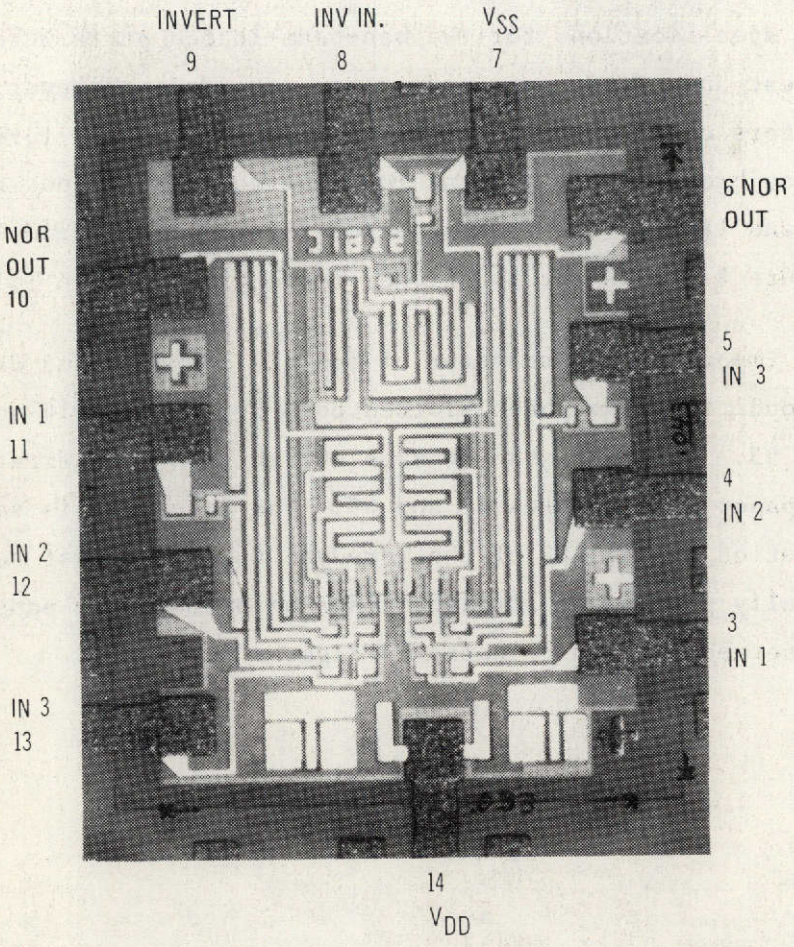
F. DELIVERED SAMPLES

On 28 March 1972 fifty (50) samples of the beam-leaded COS/MOS three-input NOR gate, designated TC1014 (CD4000BL), were delivered to the contracting agency. On 7 August 1972 fifty (50) samples of the beam-leaded COS/MOS dual D flip flop, designated TC1009 (CD4013BL), were delivered to NASA George C. Marshall Space Flight Center.

Photographs of the two types are shown in Figures 39 and 40. The dimensions are given in Figures 41 and 42. Two special packages were developed as shown in Figure 43. The pinouts are given in Figures 44 and 45. Figure 46 shows the logic diagram of the TC1009.

Testing was performed to assure that the circuits functioned correctly. Factory test specifications for the non-beam-leaded parts were used. This is a go/no-go test and no parametric data are recorded. However, there are two test transistors on each chip that can be tested in wafer form. (Leads, however, were not brought out, so that the mounted units cannot be tested). Tables VIII and IX show the test sequence for the TC1014 and TC1009, respectively. Figure 47 shows the functional tests given to the TC1014.

The most important DC-parameter of leakage currents and drain currents under various on-conditions have been plotted both for the TC1014 and TC1009 in Figures 48 thru 53. As usual, the leakage currents show an erratic behavior on probability paper, see Figures 48 and 49. The situation is somewhat aggravated by the resolution capability of the Teradyne automatic test set, i.e., the drain currents usually show up as straight lines on probability paper, but sometimes a bend is observed, as can be noted in Figures 51 and 52.



NOTE: MIRROR IMAGE OF MASKS IS BEING USED FOR FACE-DOWN-MOUNTED BEAM-LEAD CHIPS TO OBTAIN CONVENTIONAL LEAD CONFIGURATION

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Figure 39. TC1014 (CD4000BL) Chip

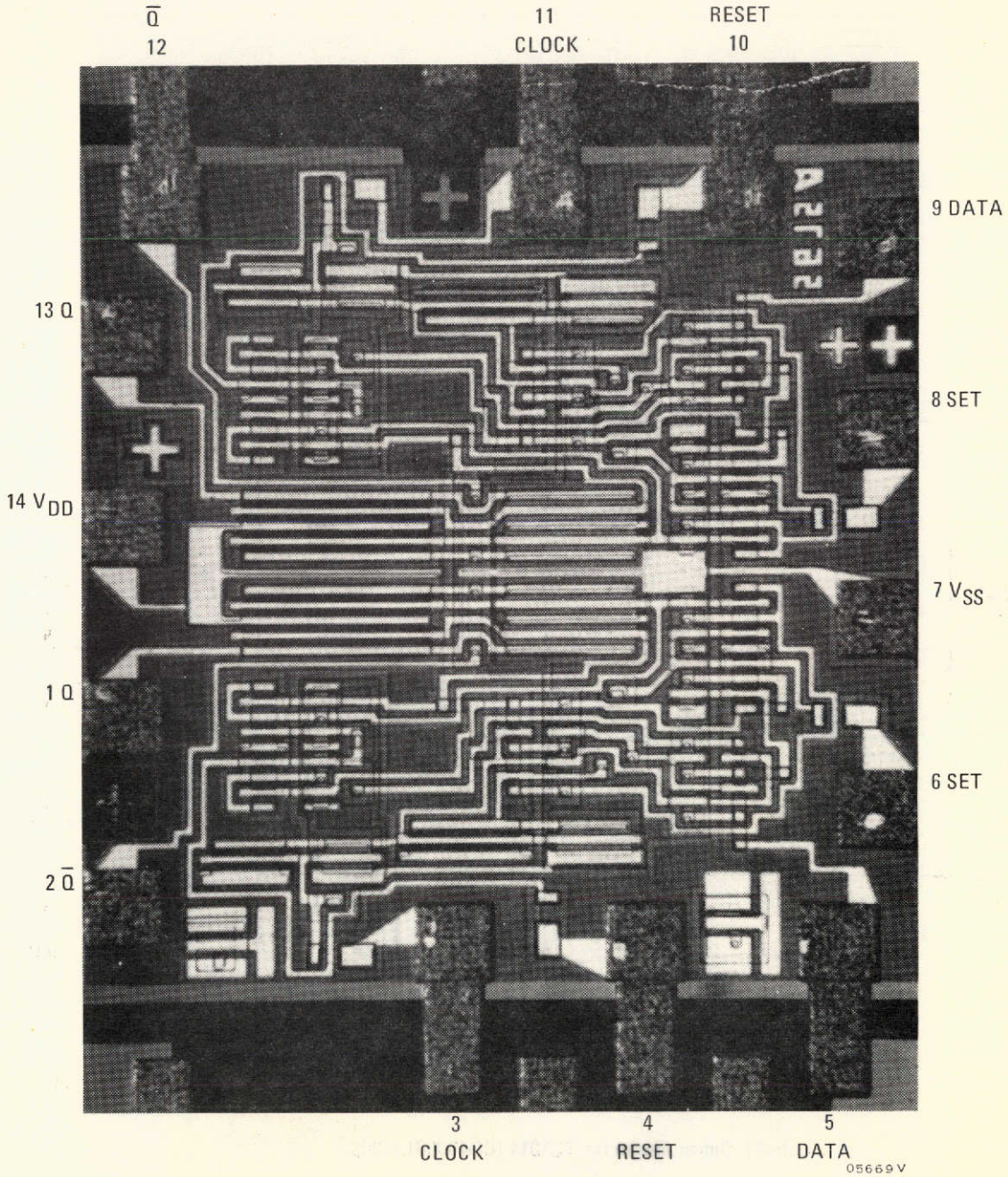

Figure 40. TC1009 (CD4013 BL) Chip

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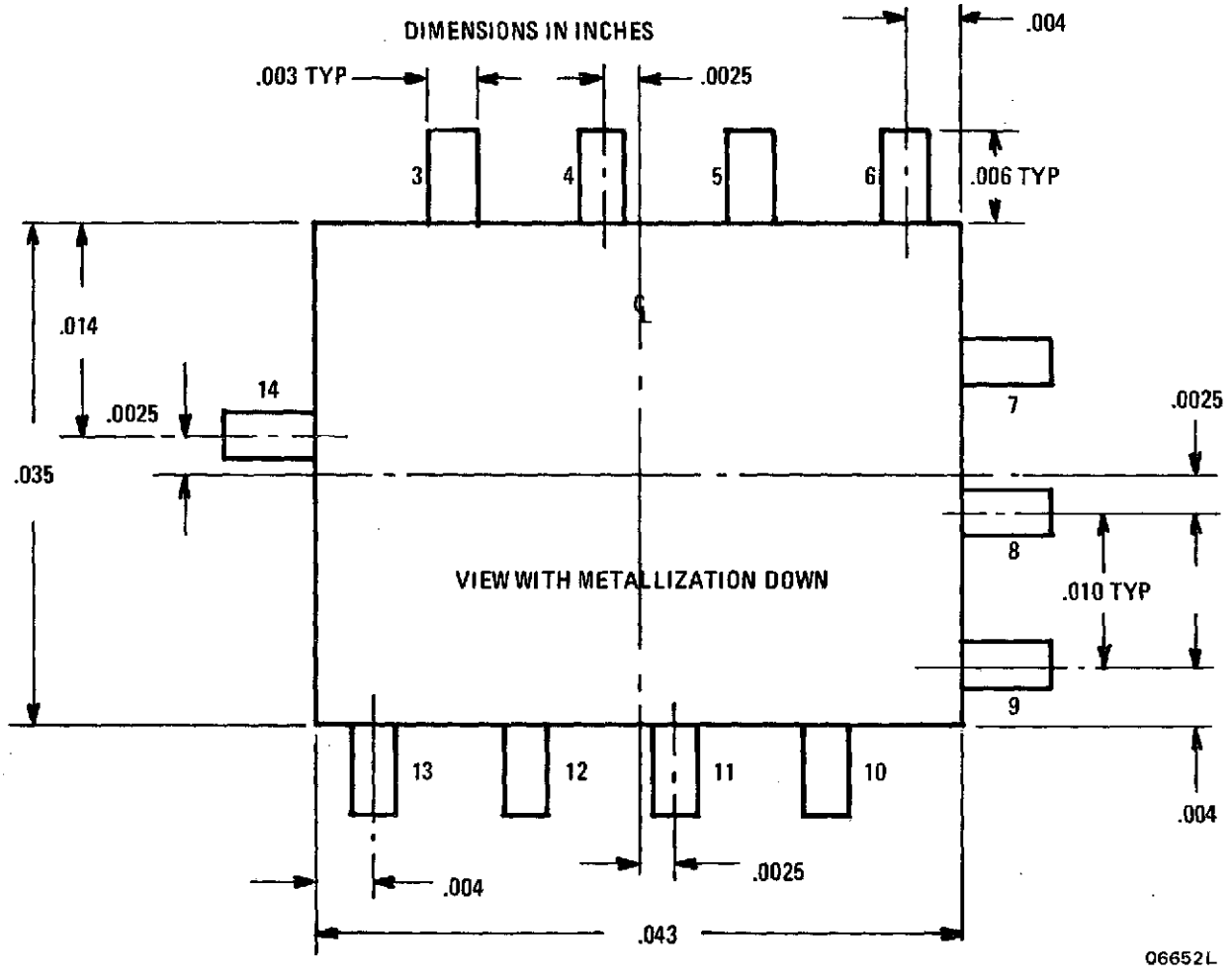


Figure 41. Dimensions of the TC1014 (CD4000BL) Chip

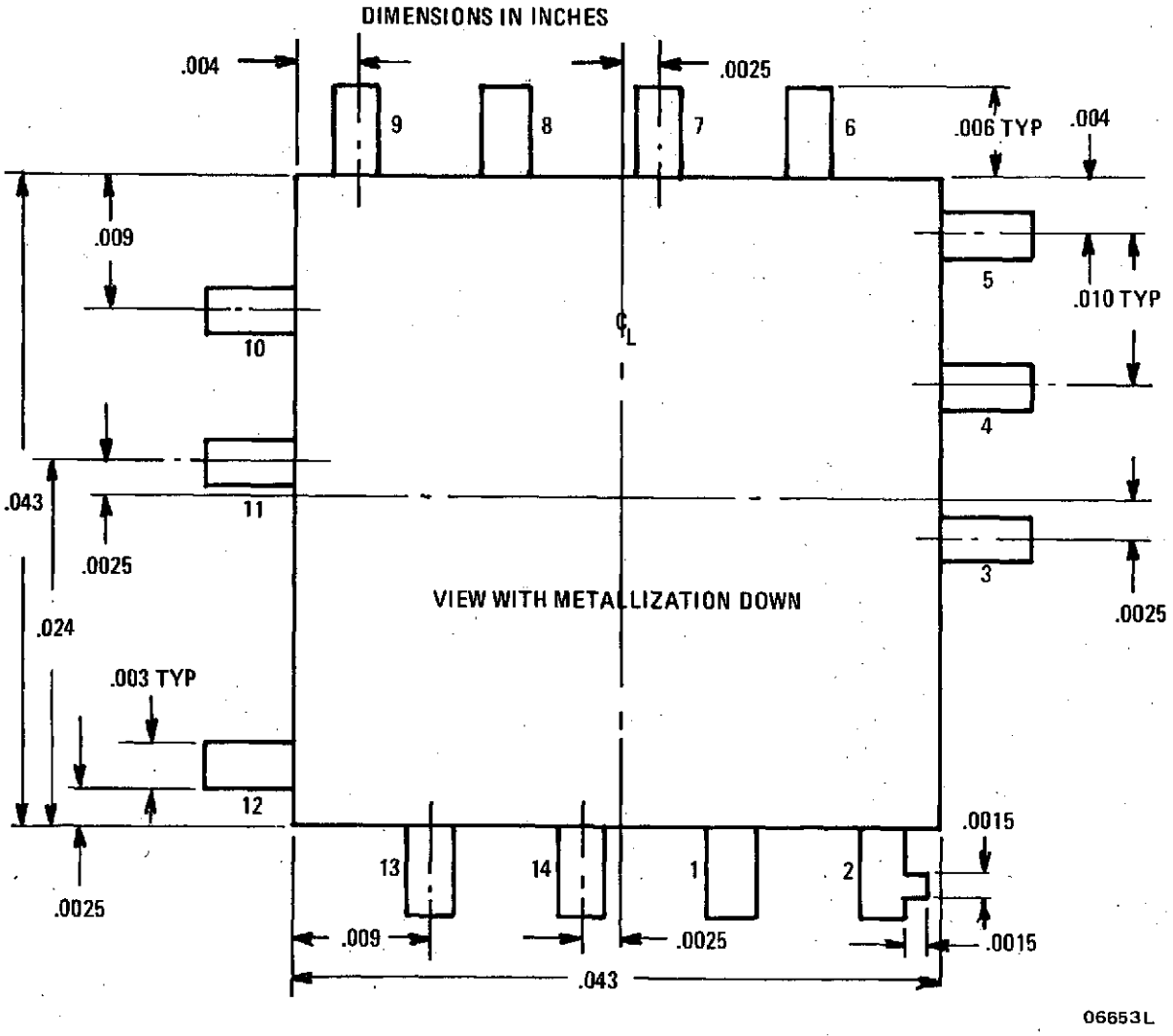
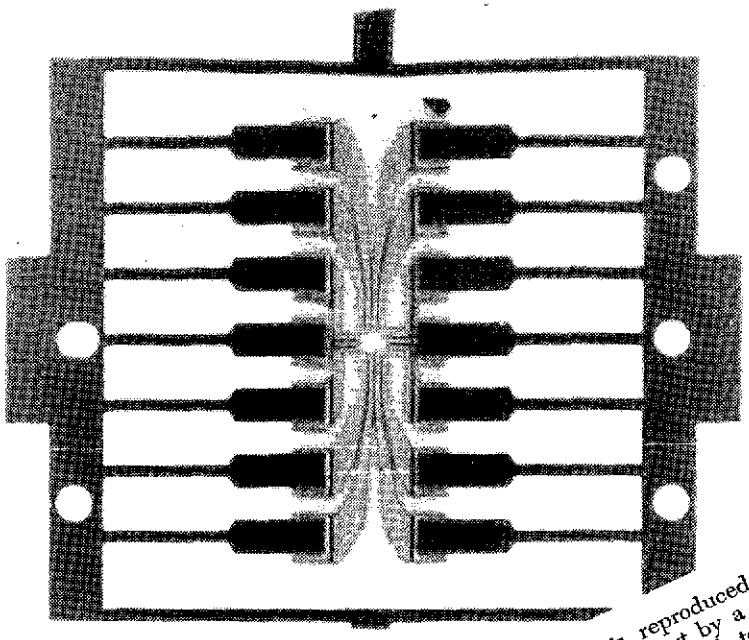
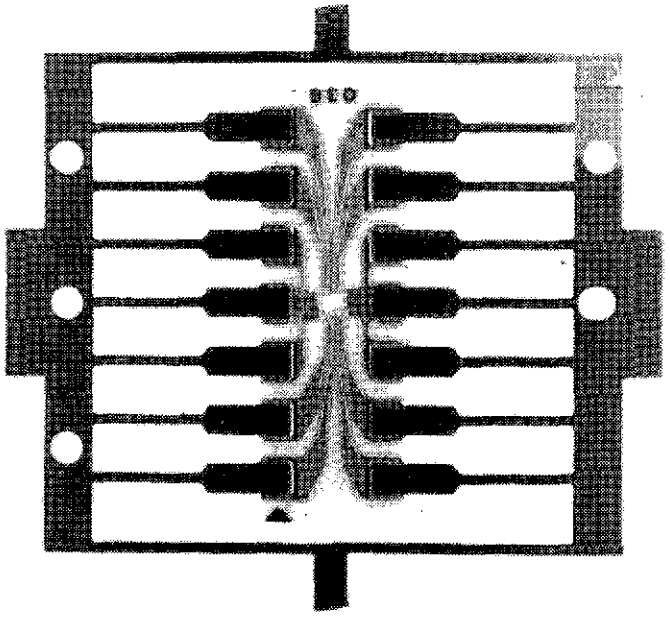


Figure 42. Dimensions of the TC1009 (CD4013BL) Chip



CD4000

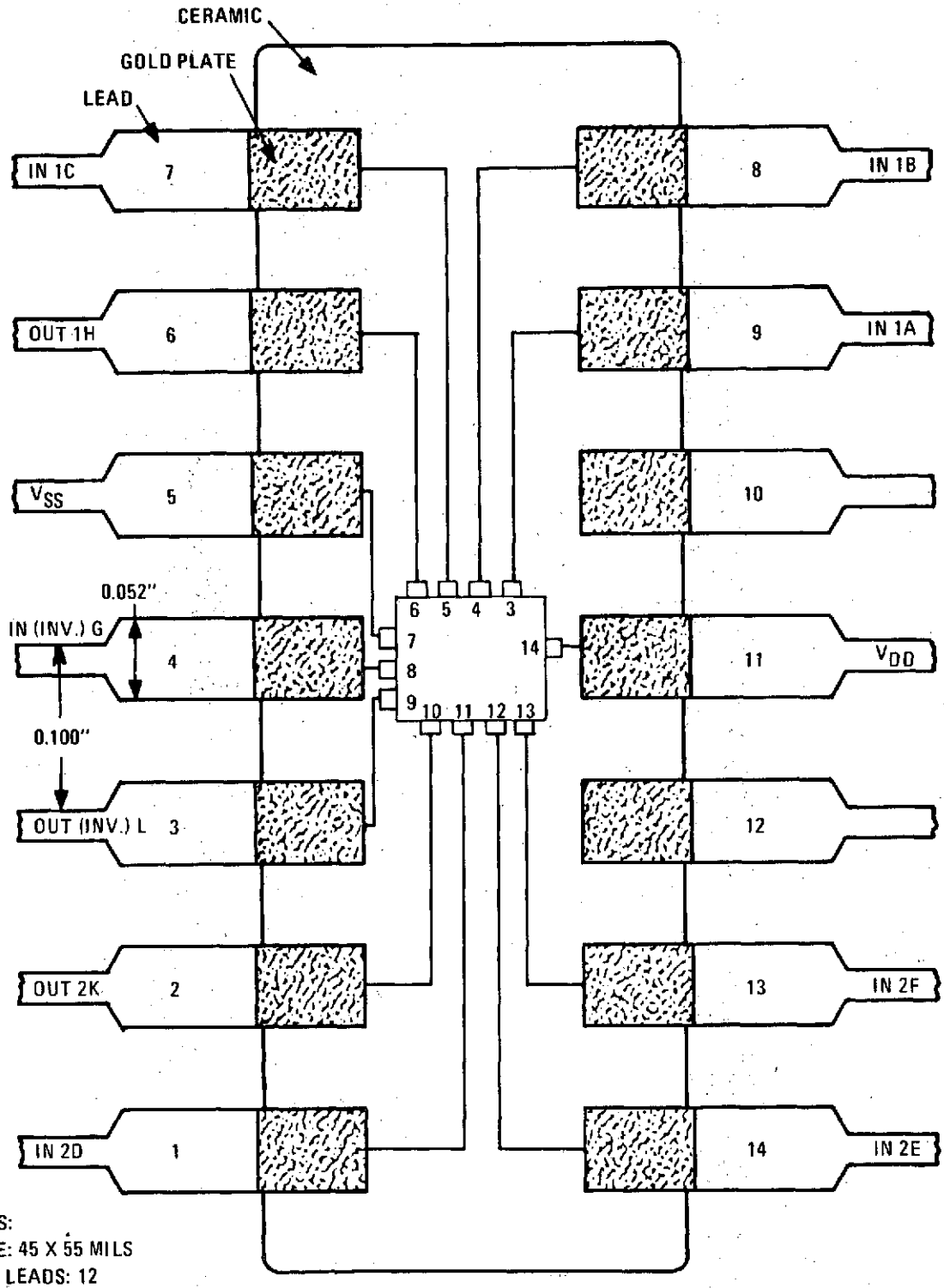


CD4013

05555V

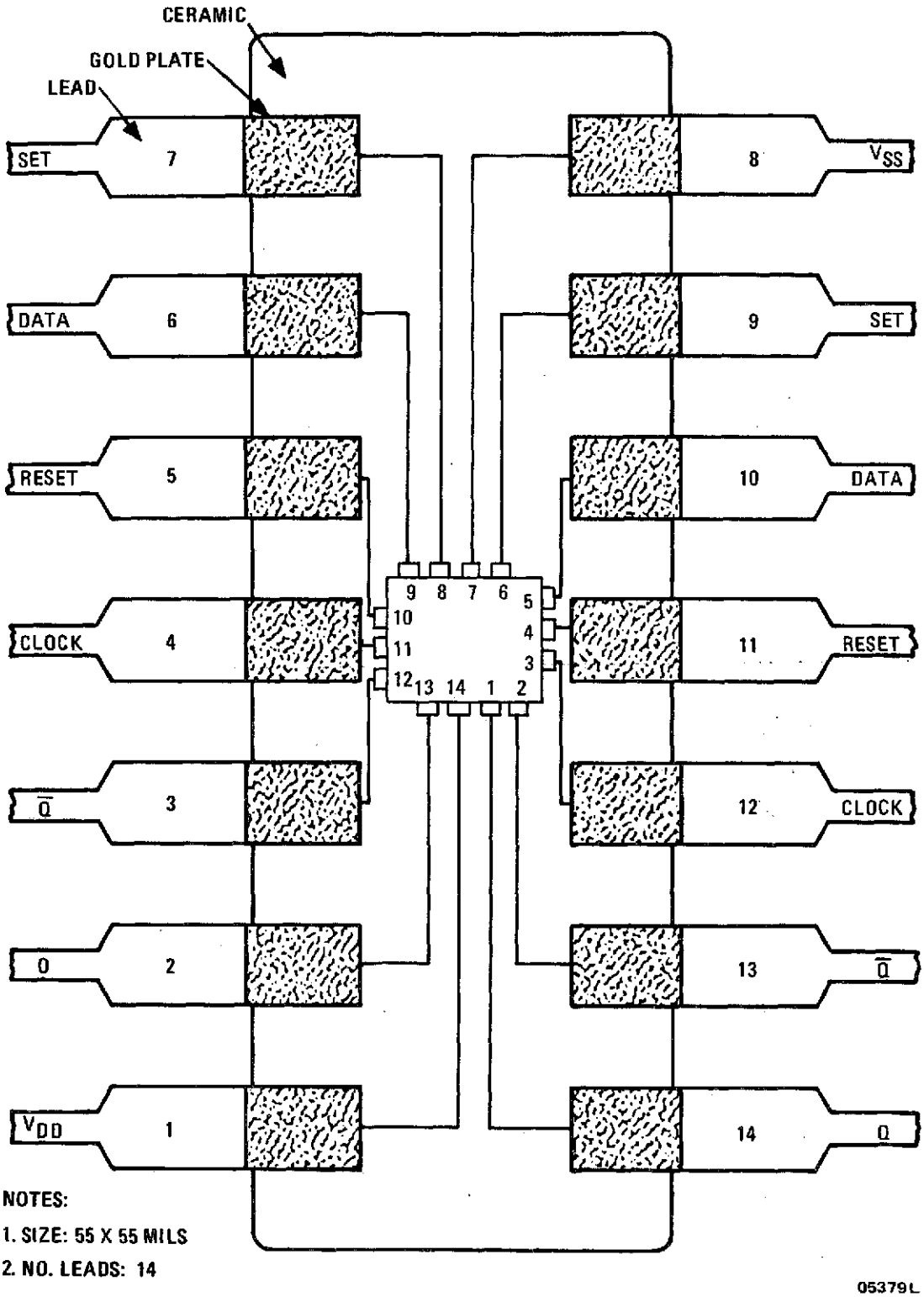
NOTE: CHIPS ARE MOUNTED FROM THE UNDERSIDE OF THESE PACKAGES

Figure 43. Beam-Lead Packages for the CD4000 and CD4013



NOTES:
1. SIZE: 45 X 55 MILS
2. NO. LEADS: 12
3. CHIP–BEAM-LEAD NUMBERING IS DIFFERENT FROM PACKAGE-LEAD NUMBERING

Figure 44. Bottom View of DIC Beam-Lead Package, Type CD4000



NOTES:

1. SIZE: 55 X 55 MILS
2. NO. LEADS: 14

05379L

Figure 45. DIC Beam-Lead Package, Type CD4013

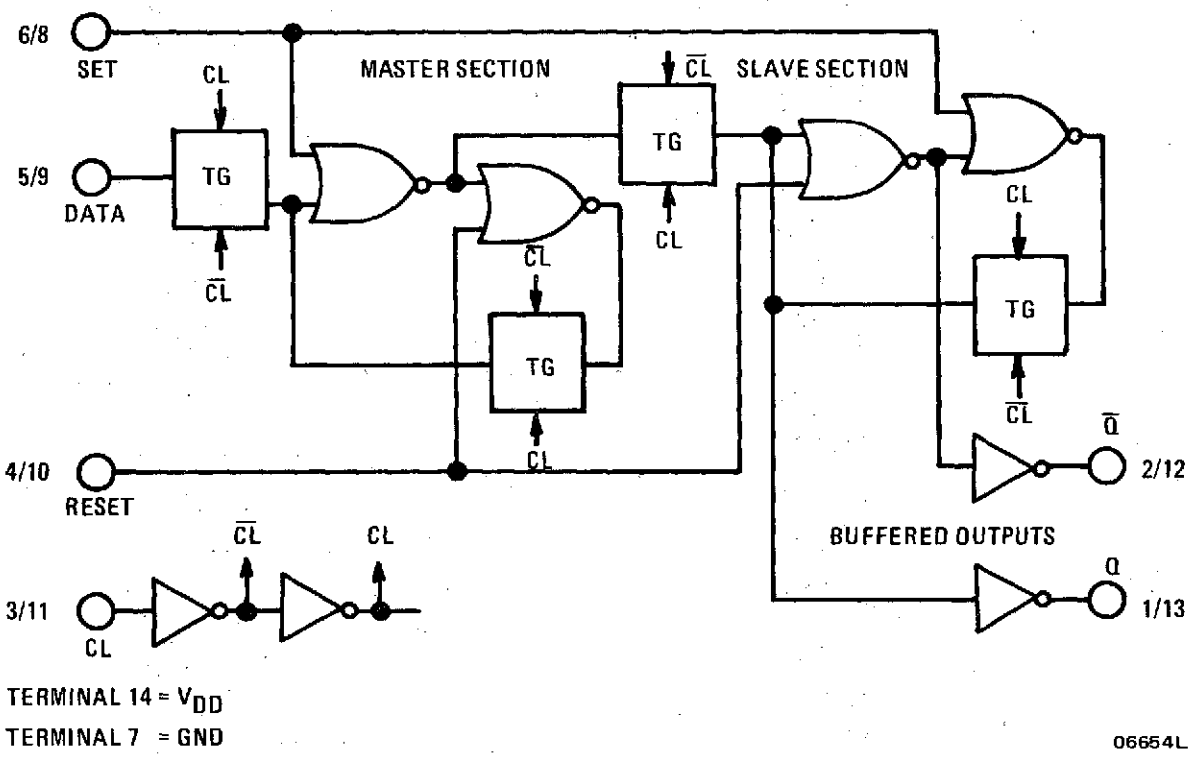


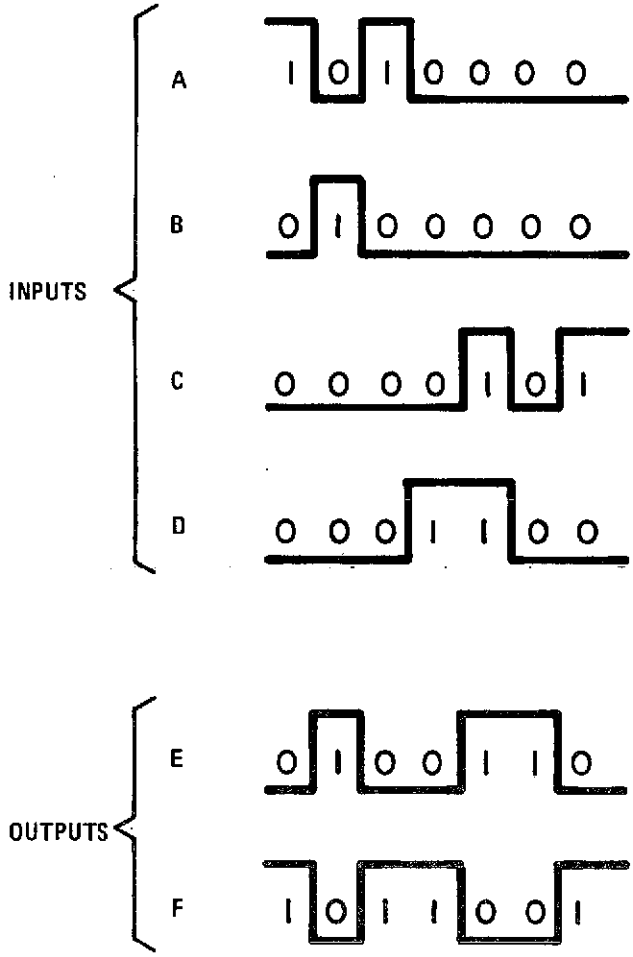
Figure 46. Logic Diagram of the TC1009 (CD4013BL)

TABLE VIII. TEST PROGRAM FOR TC1014 (CD4000BL)

Function Pin No.	IN 2D 1	OUT 2K 2	OUT(INV) L 3	IN(INV) G 4	V_{SS} 5	OUT 1H 6	IN 1C 7	IN 1B 8	IN 1A 9	V_{DD} 11	IN 2F 13	IN 2E 14	Test No.
10V Functional	0.5 To 9.5V				GND	0.5 To 9.5V				10V	0.5 To 9.5V		
5.0V Oper "1" P		Test 0V	Measured for Functional Only	0V	GND		0V	0V	0V	5V	0V	0V	3
5.0V "0" N	0V	Test 5V		0V	GND		0V	0V	0V	5V	0V	0V	4
10V LKG. IN 1 (3P)	10V			10V	GND		0V	0V	10V	Test 10V	0V	0V	5
10V LKG. IN 2 (3P)	0V			10V	GND		0V	10V	0V	Test 10V	0V	10V	6
10V LKG. IN 3 (3P)	0V			10V	GND		10V	0V	0V	Test 10V	10V	0V	7
LKG N's OFF	0V			0V	GND		0V	0V	0V	Test 10V	0V	0V	10
10V ID N	0V			0V	GND	Test 0.5V	0V	10V	0V	10V	0V	0V	11
10V ID P	0V			0V	GND	Test 9.5V	0V	0V	0V	10V	0V	0V	12
5V ID P	0V	Test 0.5V		0V	GND		0V	0V	0V	5V	0V	0V	13
5V ID N	5V	Test 5V		0V	GND		0V	0V	0V	5V	0V	0V	14

TABLE IX. TEST PROGRAM FOR TC1009 (CD4013BL)

Test No.	Test Condition	Pin / Test	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Limits		
																	Max.	Min.	Units
1	"1" = 16V "0" = 0V	16V Function	E	F	C	A	D	B	G	B	D	A	C	F	E	16V	0.4	15.6	V
2	"1" = 7V "0" = 3V	10V Noise imm.	E	F	C	A	D	B	G	B	D	A	C	F	E	10V	1	9	V
3	"1" = 3.5V "0" = 1.5V	5V Noise imm.	E	F	C	A	D	B	G	B	D	A	C	F	E	5V	0.8	4.2	V
4	"1" = 2.8V "0" = 0V	2.8V Function	E	F	C	A	D	B	G	B	D	A	C	F	E	2.8V	0.4	2.4	V
5		10V Leakage	-	-	G	P14	P14	G	G	G	P14	P14	G	-	-	Test 10V	1.6	-	μA
6		10V Leakage	-	-	G	P14	G	P14	G	P14	G	P14	G	-	-	Test 10V	1.6	-	μA
7		10V Leakage	-	-	G	G	G	P14	G	P14	G	G	G	-	-	Test 10V	1.6	-	μA
10		10V Leakage	-	-	P14	G	G	P14	G	P14	G	G	P14	-	-	Test 10V	1.6	-	μA
11		ID "N" CH 5V/0.5V	Test 0.5V		G	P14	G	G	G	G	G	G	G	-	-	5V	-	600	μA
12		ID "P" CH 5V/0.5V	Test 4.5V		G	G	G	P14	G	G	G	G	G	-	-	5V	-	260	μA
13		ID "P" CH 10V/0.5V	Test 9.5V		G	G	G	P14	G	G	G	G	G	-	-	10V	-	750	μA
14		ID "N" CH 10V/0.5V	Test 0.5V		G	P14	G	G	G	G	G	G	G	-	-	10V	-	1.1	mA



Output "one" levels are greater than or equal to the minimum limit of the test and Output "zero" levels are less than or equal to the maximum test limit.

NOTE: For the Functional Tests the letters represent the following Input and expected Output Pulse Wave forms.

06655L

Figure 47. Functional Test Sequence for the TC1014 (CD4000BL)

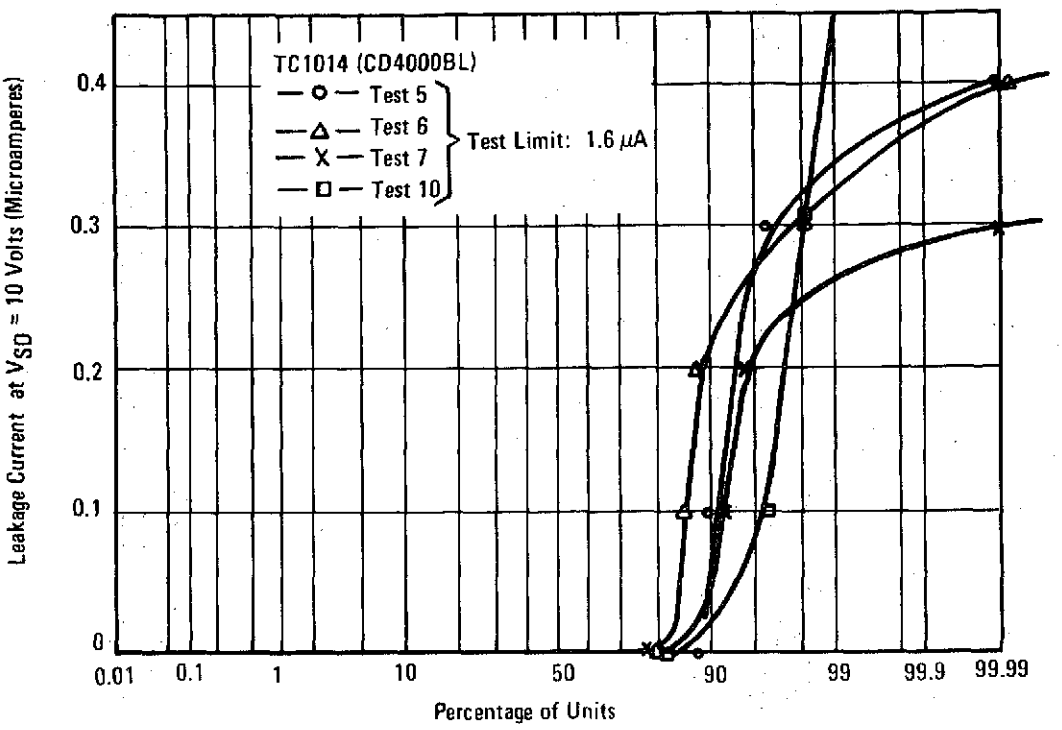


Figure 48. Distribution of Leakage Currents at V_{SD} = 10 V of TC1014 (CD4000BL) Delivered Samples

06656L

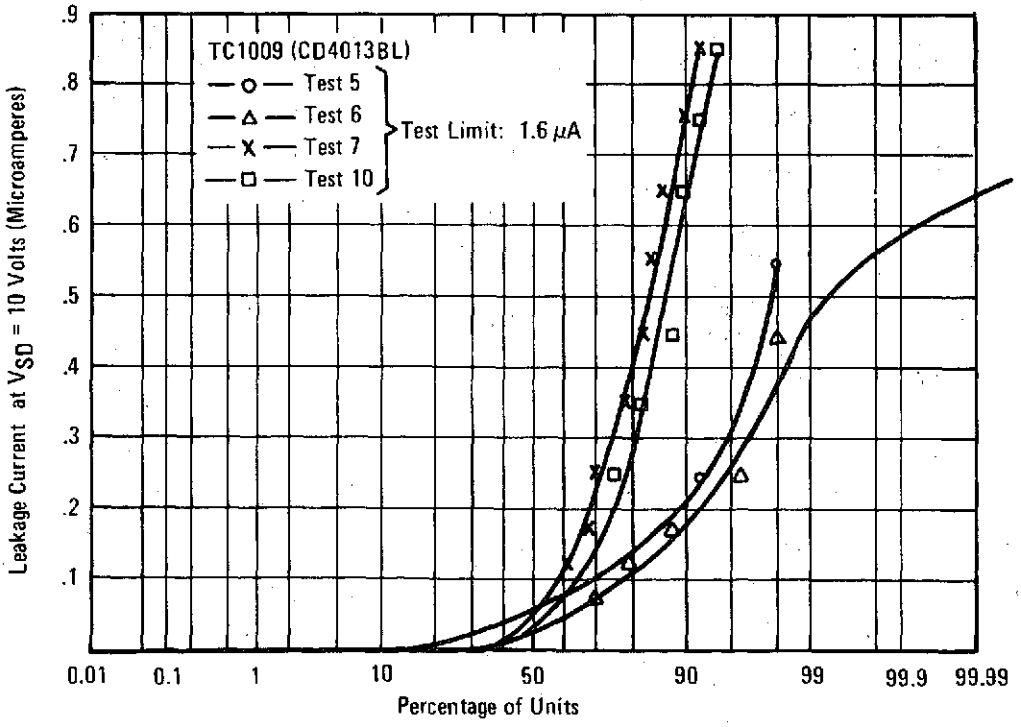


Figure 49. Distribution of Leakage Currents at V_{SD} = 10 V of TC1009 (CD4013BL) Delivered Samples

06659L

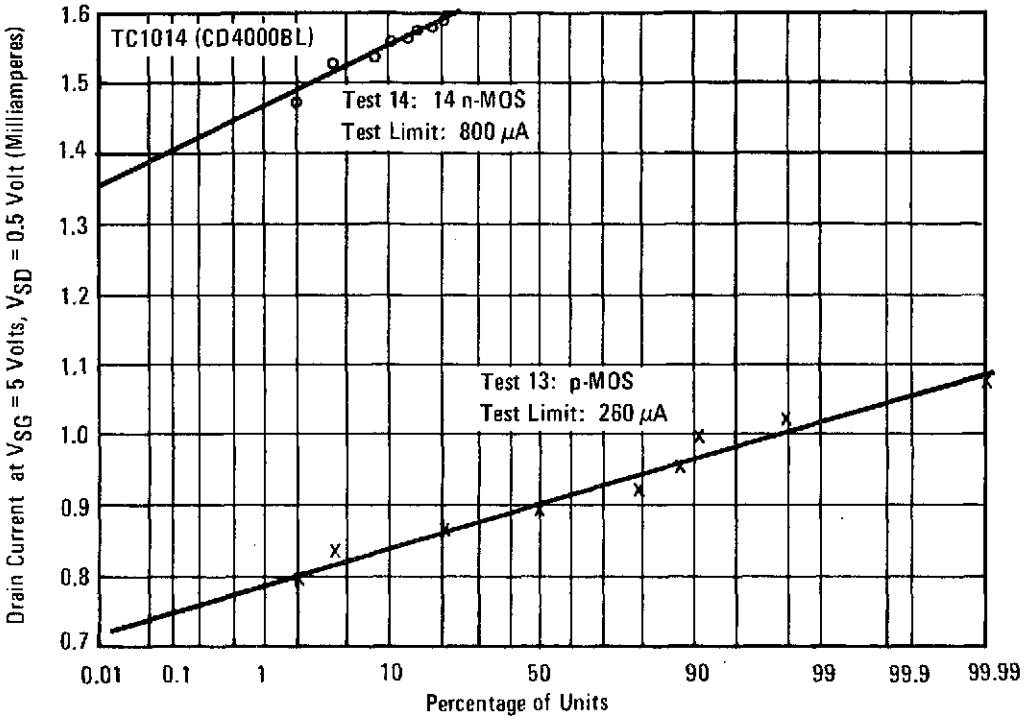


Figure 50. Distribution of Drain Currents at V_{SG} = 5 V; V_{SD} = 0.5 V of TC1014 (CD4000BL) Delivered Samples

06657L

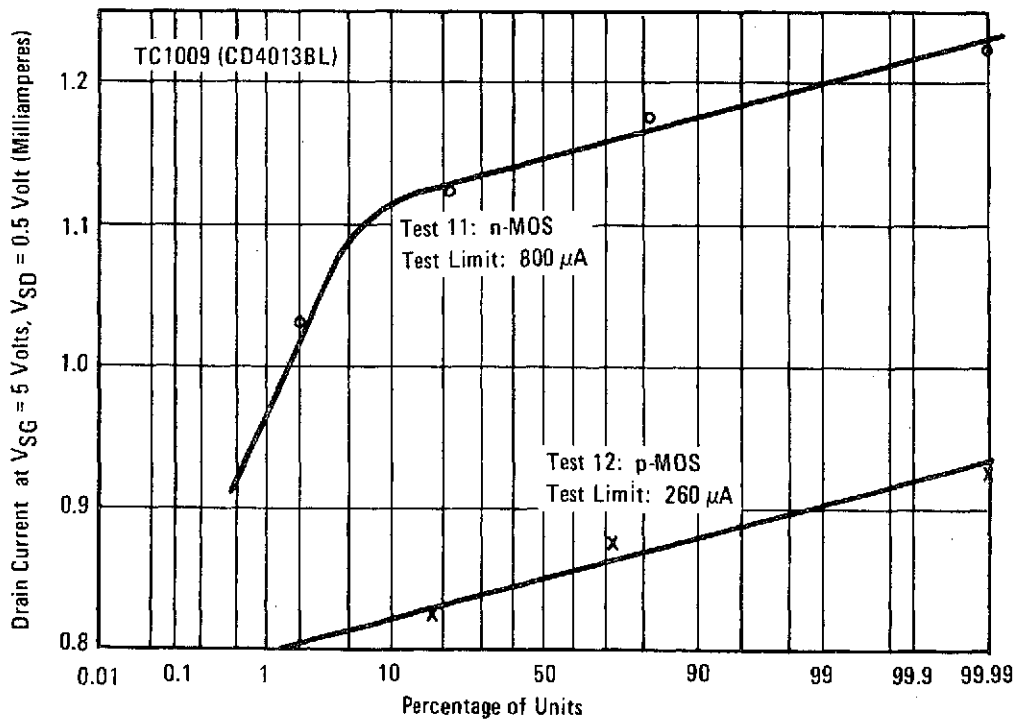


Figure 51. Distribution of Drain Currents at V_{SG} = 5 V; V_{SD} = 0.5 V of TC1009 (CD4000BL) Delivered Samples

06660L

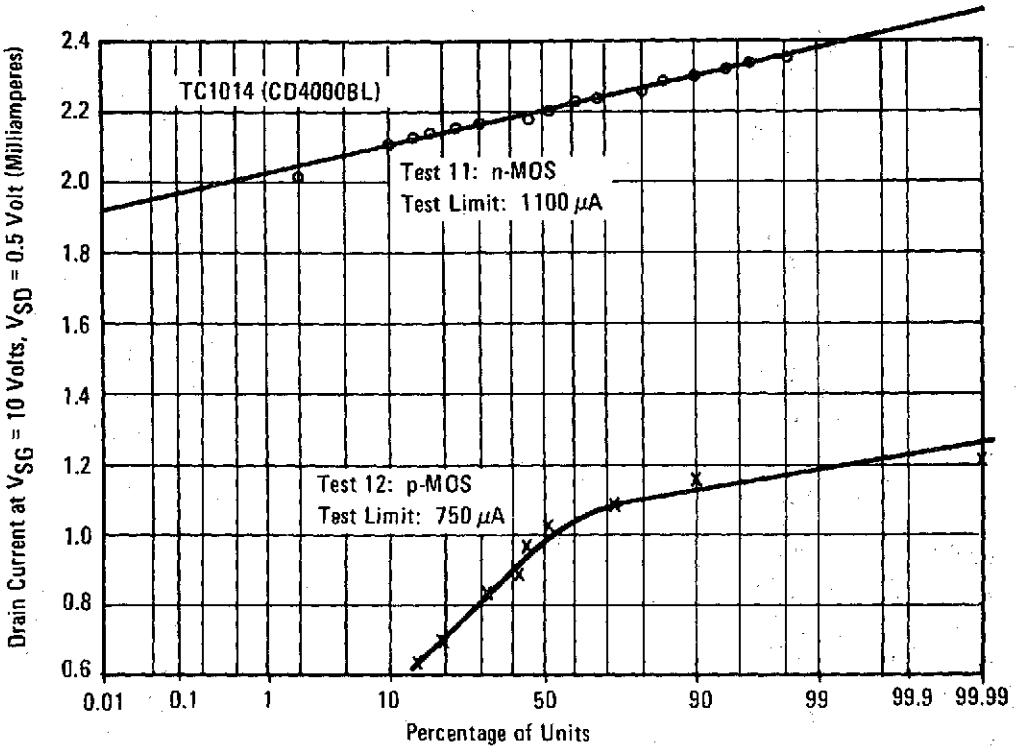


Figure 52. Distribution of Drain Currents at V_{SG} = 10 V; V_{SD} = 0.5 V of TC1014 (CD4000BL) Delivered Samples

06658L

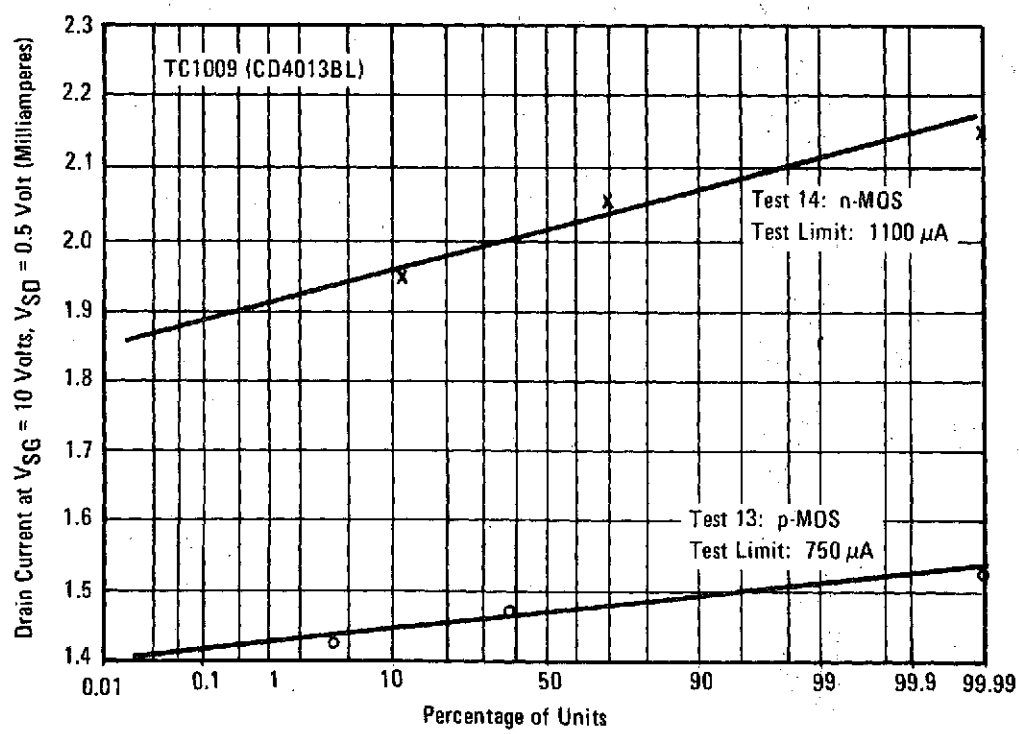


Figure 53. Distribution of Drain Currents at V_{SG} = 10 V; V_{SD} = 0.5 V of TC1009 (CD4013BL) Delivered Samples

06661L

SECTION III

PHASE 2: PROCESS DEVELOPMENT OF BEAM-LEAD, SILICON-GATE COS/MOS INTEGRATED CIRCUITS

The objective of this program was to develop a silicon-gate process compatible with COS/MOS, beam-leaded, hermetically sealed, integrated circuits. Hermetically sealed beam-lead circuits can be fabricated by using a composite gate dielectric as was described in Section II. As was mentioned, there are charges accumulating at the dielectric 1:dielectric 2 interface that change the behavior at the dielectric 2:silicon interface. (Dielectric 2 commonly is silicon dioxide.) The most commonly seen changes are in the threshold voltage of n-MOS transistors.

Another approach was investigated during the second phase of this contract. Only a single-gate dielectric (i.e., silicon dioxide) was used. To allow for high-temperature deposition of a sealing dielectric, a high-temperature gate conductor is needed. Polysilicon is a good choice because it can be doped either p^+ or n^+, thus allowing low threshold voltages for both the p-MOS and the n-MOS transistors. The polysilicon gates are then coated with a non-critical heavy layer of silicon nitride.

A further advantage in both speed and packing density is the use of self-aligned silicon gates for both polarity MOS transistors. The channel length can be shortened to give higher source-to-drain currents (under otherwise identical test conditions) and lower Miller feedback capacitances.

This silicon-gate effort was coupled with an approach that generates library elements, circuits and design-automation tapes for the MSFC SUMC computer. The "Arithmetic and Logic Unit" (ALU) 50M37933 was used as the test vehicle for the developed process.

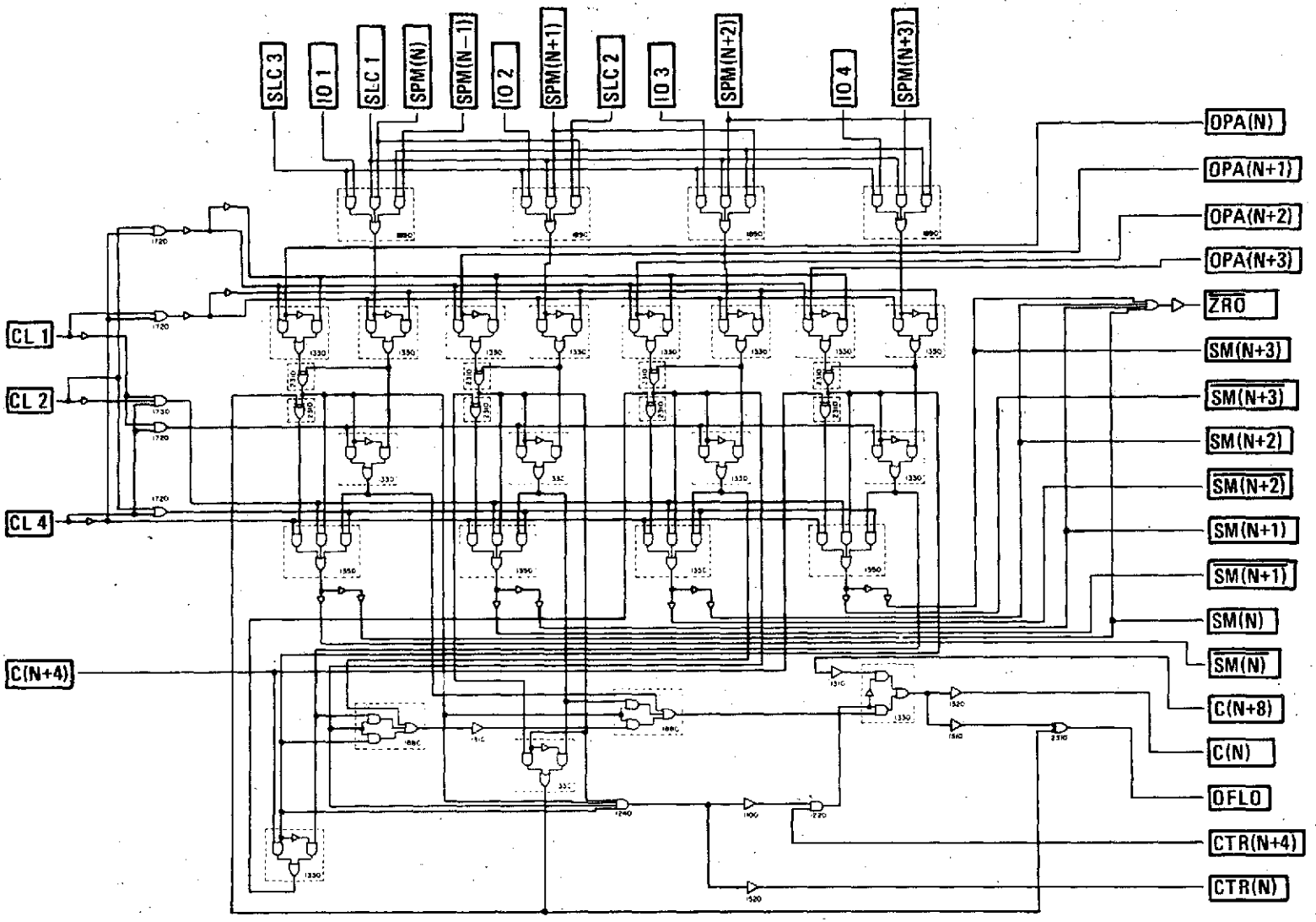
A. DESCRIPTION OF THE ARITHMETIC AND LOGIC UNIT (ALU)

The test vehicle for the process development was the "Arithmetic and Logic Unit" (ALU), the TCC-049A*. This is a 179-mil by 173-mil logic circuit with the capability of performing the following operations:

1. Add
2. Subtract
3. Reverse Subtract
4. Multiply
5. Divide
6. AND
7. OR
8. Exclusive OR
9. Compare
10. 1 and 2's complement
11. 1's complement

The chip is designed from standard library elements interconnected by a two-level metallization scheme of doped polysilicon and beam-lead Ti-Pd-Au (see Figures 54 and 55). Because of the cell-library approach, the chip is not as customized as its aluminum-gate counterpart, however, the 12 cells comprising the chip (ignoring interconnect distances) occupy an area 40 percent less than the equivalent aluminum-gate design. The longer interconnect distances inherent in the cell-library approach are largely negated by the lower capacitance per unit length of the polysilicon lines over the diffused tunnels which they replace. More importantly, the chip uses self-aligned silicon gates on both n-MOS and p-MOS transistors, and sealed-junction beam-lead metallization. This approach combines the increased reliability of beam-lead metalli-

*Also referred to as the four-bit adder.



06662L

Figure 54. ALU(TCC-049A) Logic Schematic Showing Cell Organization

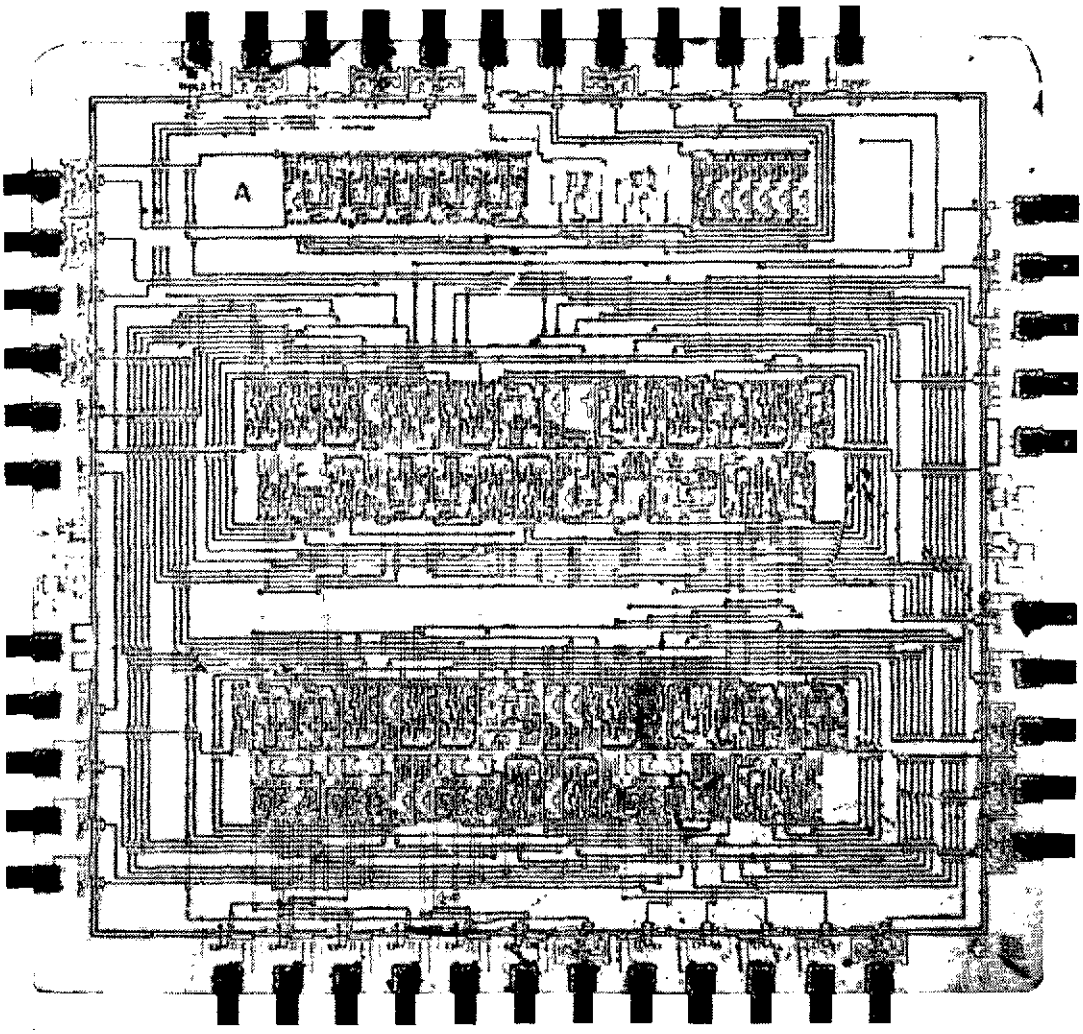


Figure 55. Photograph of ALU (TCC-049A)

zation with the lower thresholds, reduced Miller capacitance, and greater packing density of the silicon-gate process. From the above considerations, a total delay time of less than 200 nanoseconds was projected for this chip. This represents a 35-percent reduction over the aluminum-gate chip. Speed measurements to date have yielded somewhat longer delays than expected (see Section IV). This result is a direct consequence of the high n-MOS thresholds of most of the tested lots. As will be discussed later, the n^+ polysilicon doping level had to be decreased in order to obtain appreciable yield at a supply voltage of 10 volts.

In addition to the Adder circuit, a number of logic circuits have been provided on the chip for diagnostic purposes. These include:

1. A two-input NOR gate with 0.25 mil gate lengths
2. A two-input NOR gate with 0.20 mil gate lengths
3. An exclusive OR gate
4. A two-input NOR gate with inverter load
5. A simple inverter with self-aligned silicon gates
6. A self-aligned, silicon-gate thin-oxide p-MOS transistor
7. A non-self-aligned silicon-gate field-oxide p-MOS transistor
8. A self-aligned silicon-gate thin-oxide n-MOS transistor
9. A non-self-aligned silicon-gate field-oxide n-MOS transistor

These peripheral devices are similar in design to the interior of the chip and are brought out to beams so that functionality and dynamic measurements can be made to facilitate debugging and estimate the limits of the technology.

B. SILICON-GATE, BEAM-LEAD, COS/MOS PROCESS

1. ALU MASK SEQUENCE

The process, from bare wafer to separation of beam-lead chips, involves eleven (11) masks in the sequency shown below:

1. p-Well
2. p^+ Guardband

} Essentially Standard Low-Voltage COS/MOS Processing

3. n^+ Guardband
4. Stepped Oxide

} Essentially Standard Low-Voltage COS/MOS Processing

5. Polysilicon Definition
6. n^+ source-drain doped-oxide definition
7. Contact I
8. Contact II
9. Interconnect Metal
10. Gold-Beam Plate
11. Chip separation

2. PROCESSING STEPS

The processing steps employed to form the beam-lead, silicon-gate, COS/MOS device are shown in the process flow chart of Figure 56. The process can be divided into three main areas: COS/MOS, silicon gate and beam lead. Drawings depicting the primary processing steps (Steps 1 through 15) are shown in Figure 57.

a. COS/MOS

A modified COS/MOS processing technique, as outlined below, is employed.

1. An n-type wafer, with a <100> orientation and a resistivity of 1 to 2 ohm-cm is chemically cleaned.
2. The wafer is oxidized in a steam ambient (Step 1).
3. A well photoresist is performed and the oxide is removed from the well area.
4. Boron is implanted and diffused (Step 3).
5. A p^+ guard-band photoresist operation is performed and the oxide removed from the area.
6. Boron is deposited and diffused to form the p^+ guard band (Step 4).
7. An n^+ guard-band photoresist operation is performed and the oxide removed from the area.

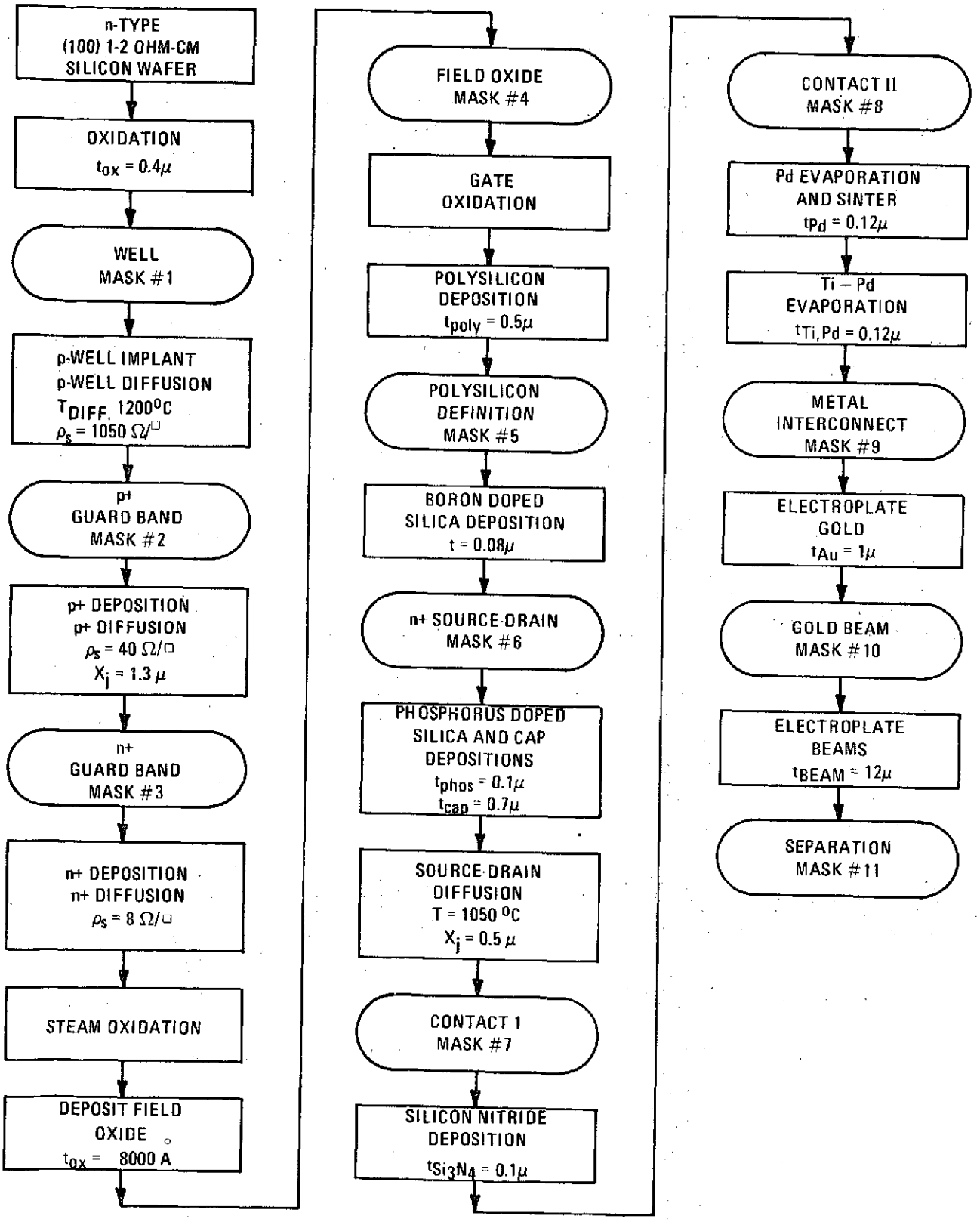
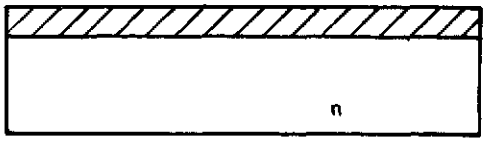
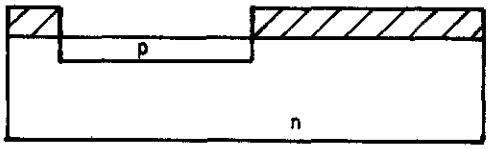


Figure 56. Self-Aligned Silicon-Gate Beam-Lead Process

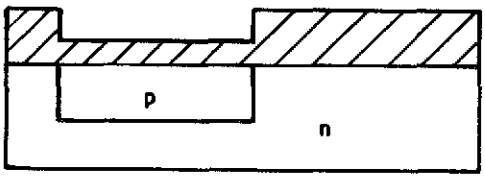
06366L



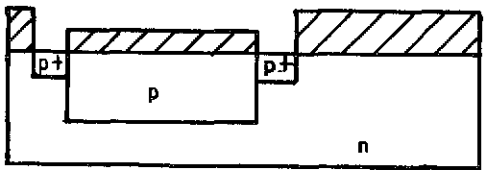
1. INITIAL OXIDATION



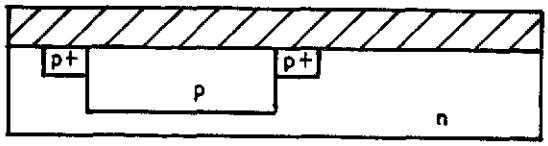
2. WELL MASK & BORON IMPLANT



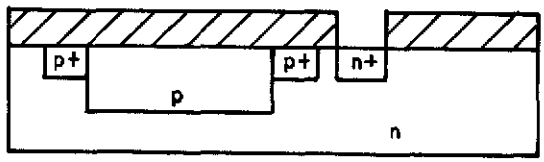
3. WELL DIFFUSION & REOXIDATION



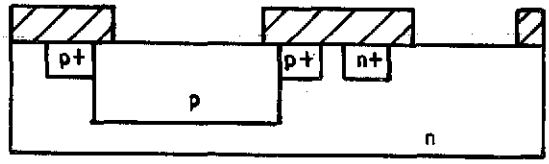
4. p+ GUARDBAND MASK & DIFFUSION



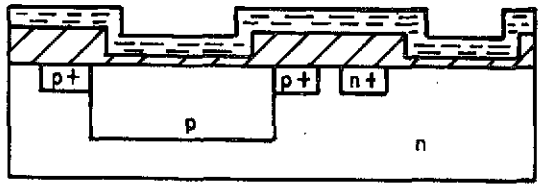
5. WAFER STRIP & OXIDE DEPOSITION



6. n+ GUARDBAND MASK & DIFFUSION



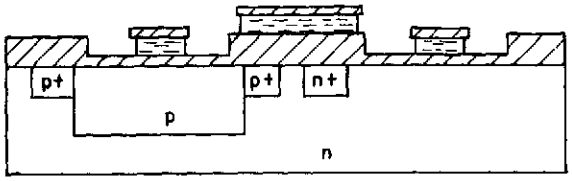
7. STEPPED-OXIDE DEPOSITION & MASK



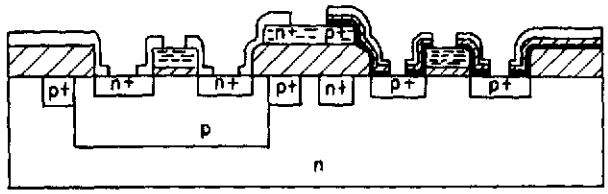
8. GATE OXIDATION & POLY DEPOSITION

06664L

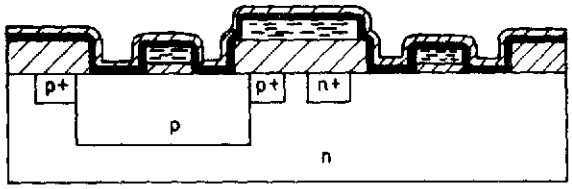
Figure 57. Profile of Self-Aligned Silicon-Gate Beam-Lead Process (Sheet 1 of 2)



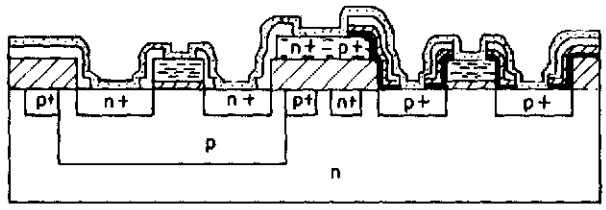
9. POLY OXIDATION & DEFINITION MASK



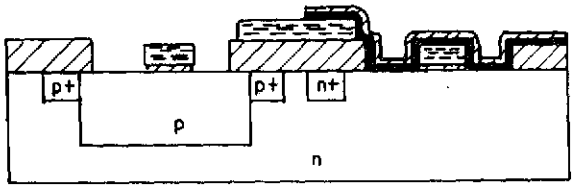
13. CONTACT 1 MASK



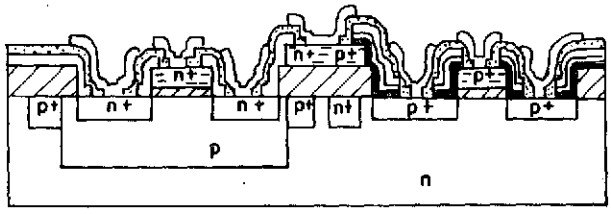
10. BORON-DOPED OXIDE-CAP OXIDE DEP.



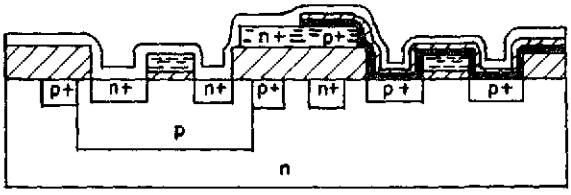
14. NITRIDE DEPOSIT



11. BORON OXIDE REMOVAL MASK & ETCH



15. CONTACT II AND METAL MASKS



12. PHOS OXIDE DEP. & S-D DIFFUSION

Figure 57. Profile of Self-Aligned Silicon-Gate Beam-Lead Process (Sheet 2 of 2)

8. Phosphorus is deposited and diffused to form the n^+ guard band. At this point a thick field oxide is formed.

b. Silicon-Gate

Under the conditions of deposition, the silicon gate is typically polycrystalline in nature. The silicon gate, therefore, can be more accurately described as the polysilicon gate. The silicon-gate process is as follows:

1. An active-area photoresist operation is performed and the oxide removed from those areas where p-MOS and n-MOS field-effect transistors are to be formed (Step 8).
2. A gate oxidation, 0.11 micrometer in thickness, is performed in all areas defined by the active-area.
3. Polysilicon, 0.5 micrometer in thickness, is deposited by the decomposition of silane (Step 9).
4. An oxide mask is formed on the polysilicon layer and a polysilicon photoresist is performed. The polysilicon is then etched.
5. Then, the 0.11 micrometer oxide is removed from those areas not protected by the polysilicon or the thick oxide.
6. Boron-doped silica is deposited (Step 10).
7. An n^+ photoresist operation is performed and boron-doped silica is removed from those areas where the n-MOS devices are to be formed.
8. Phosphorus-doped silica and a cap is deposited, and the S-D areas diffused (Step 12).
9. The first contact photo step is then put on and etched.

c. Beam Lead

The beam-lead processing of COS/MOS circuits was explained in detail in Section II.A of this report.

3. IN-PROCESS CONTROLS

The in-process controls were explained in detail in Section II.B.2 of this report.

4. ION-IMPLANTED p-WELLS

The boron ions for the well formation were introduced by ion implantation in the last five lots processed. As shown below, this technique saves several processing steps and allows for greater control of the final surface concentration, and, hence, the n-MOS thresholds.

Boron Nitride Well Process

1. Deposit Boron at 820°C for 30 Minutes; ρ_s = 300 to 450 ohms/□
2. Diffuse Boron at 1200°C for 30 Minutes; ρ_s = 350 to 550 ohms/□
3. Steam Oxidation, 1100°C for 6 to 7 Hours; ρ_s = 800 to 1000 ohms/□
4. Well Diffusion, 1200°C for 16 Hours; ρ_s = 950 to 1100 ohms/□

Ion-Implanted Well Process

1. Ion-Implant Boron; Etch Back Oxide
2. Well Diffusion, 1200°C for 16 hours; ρ_s = 950 to 1100 ohms/□

A program was written to calculate the dosage and expected surface concentration for our low-voltage process. The theoretical curves are shown in Figure 58. The final channel concentration is somewhat lower than the predicted value, as determined by techniques given in Appendix B. Figures 59 and 60 show the scatter in this parameter with lots processed and with sheet resistivity. The latter is a rather poor measure of actual surface concentration. Note that there is less scatter in the implanted samples.

C. DEVICE CHARACTERIZATION

1. TEST TRANSISTORS

Integrated circuits with thousands of MOS transistors are too complex for quick circuit analysis. The customary procedure is to test individual n- and p-MOS transistors both for the normal thin and the heavier field-oxide gate dielectrics. Each of the adders has these four transistors and potentially 74 measurements can be made with automatic test equipment. When test-time scheduling makes a quick turnaround impossible, these measurements are performed at a

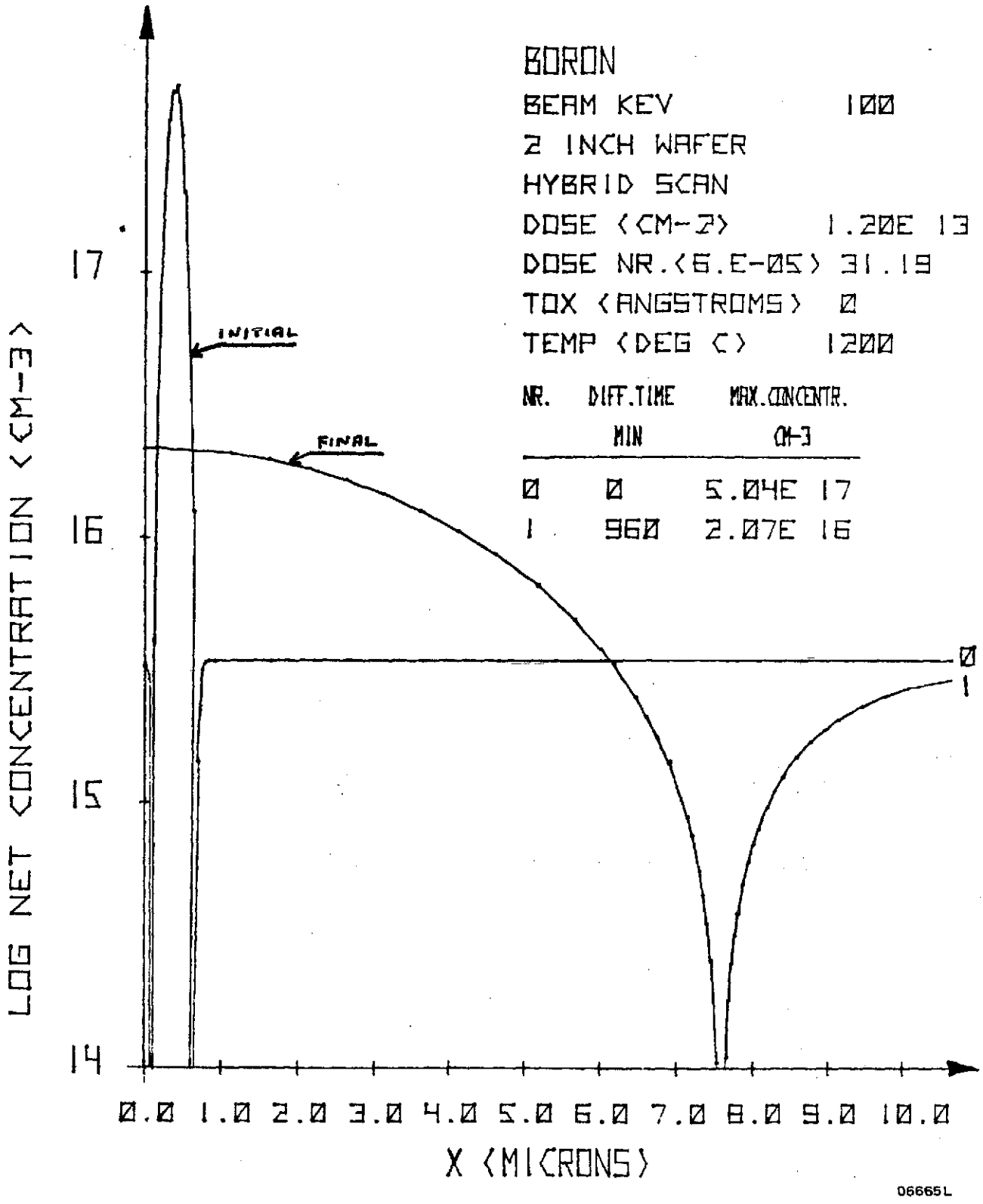


Figure 58. Theoretical Plots for Ion-Implanted Well

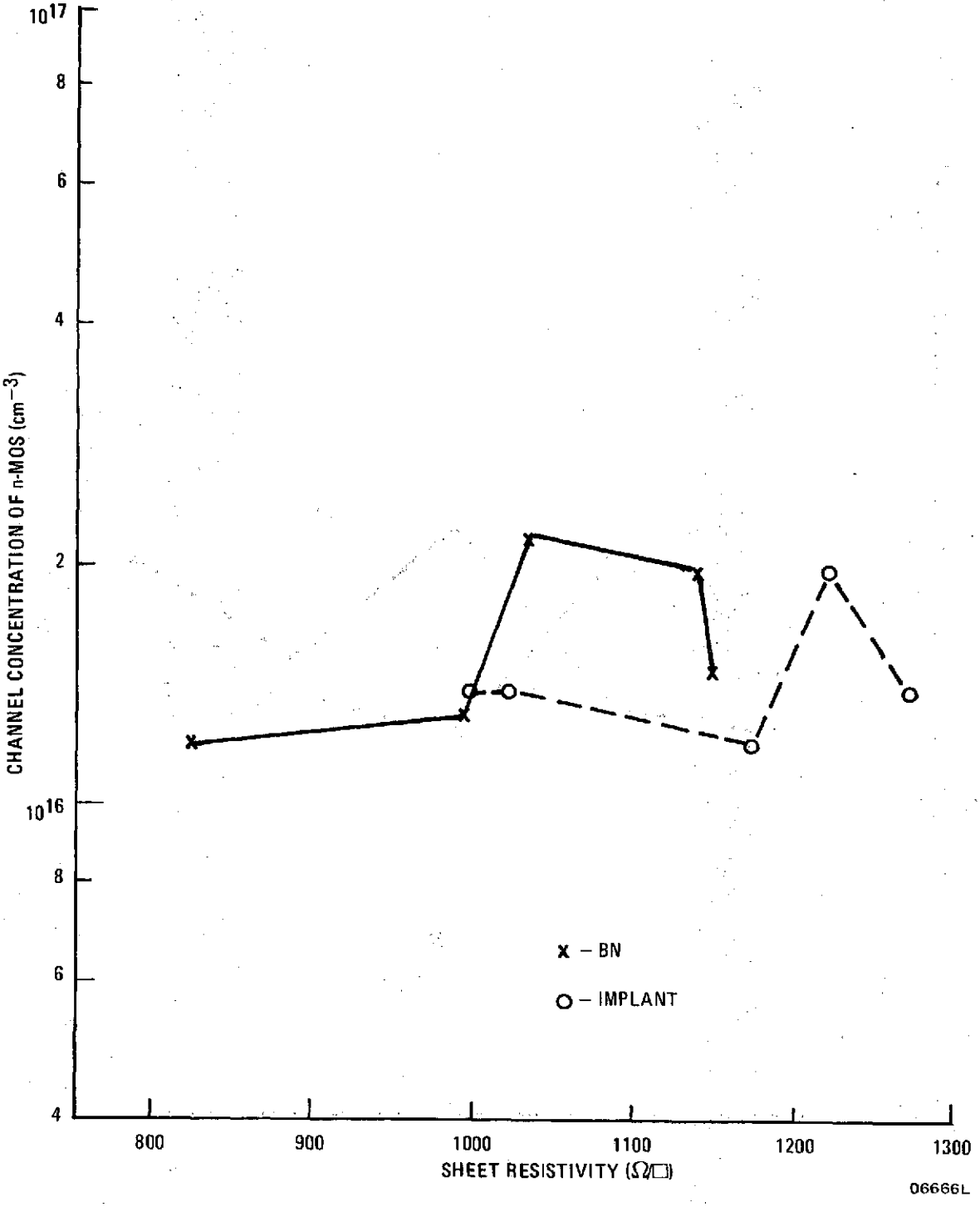


Figure 59. Well-Surface Variation

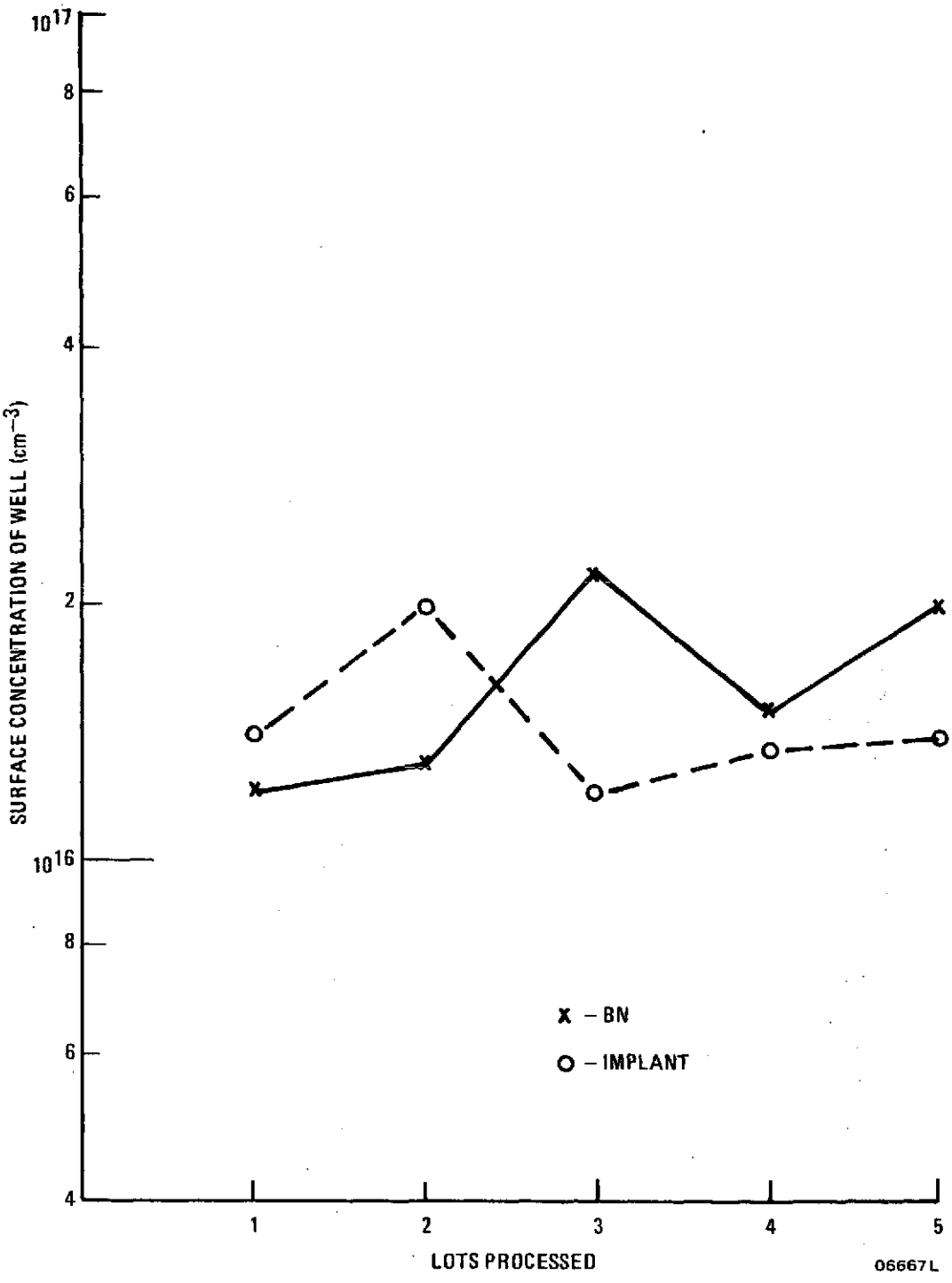


Figure 60. Well-Surface Variation

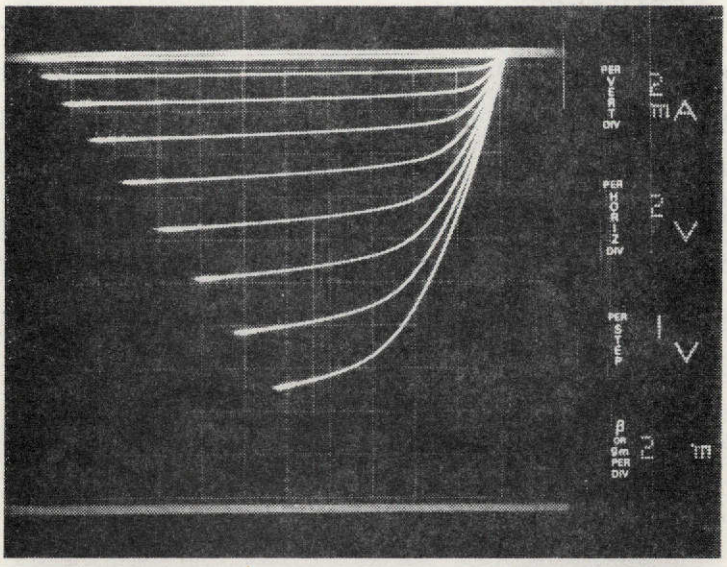
semi-automatic laboratory test set. In addition, the whole voltage-current characteristic of the four MOS transistors can be observed on a 576 Tektronix curve tracer. Typical curves are shown in Figures 61 through 64.

The test transistors (Figures 65 and 66) have a gate width of 2 mils and a nominal channel length of 0.25 mil. Actually, sideway diffusion will reduce this value by at least 0.08 mil. The sloping of the field oxide makes the actual gate width 2.35 mils. The actual gate length is difficult to determine with precision. It is easier to use the K-factor (adjusted for the actual gate width) rather than the K'-factor, which relates the device back to a channel mobility. During the course of this work a tapered stepped oxide was introduced.

Initial work included aluminum metallization. The threshold voltage and the K-factor depend on the removal of fast surface states at the $Si-SiO_2$ interface by a low-temperature alloy-anneal operation. During this alloy-anneal step the aluminum metallization alloys only into the silicon substrate. In the silicon-gate process the aluminum metal alloys into both the silicon substrate and into the polysilicon layer which is only 0.6 micrometer thick. To prevent the alloying of all of the polysilicon exposed in the contact aperture, an optimum-heat cycle had to be established. Figure 67, a plot of the n-MOS threshold (VT_{NN}) versus the alloy-anneal time (t_{alloy}-anneal) at 450°C in forming gas, shows that 15 minutes reduced the threshold voltage to minimum values. Analysis indicated that after 15 minutes of alloy-anneal time at 450°C, sufficient unalloyed polysilicon remained in the contact aperture to insure proper device operation. The K-factor increased, see Figure 68, reflecting its dependence upon majority-carrier mobility. This occurs because the annealing step simultaneously reduces the number of traps and lowers the contact resistance.

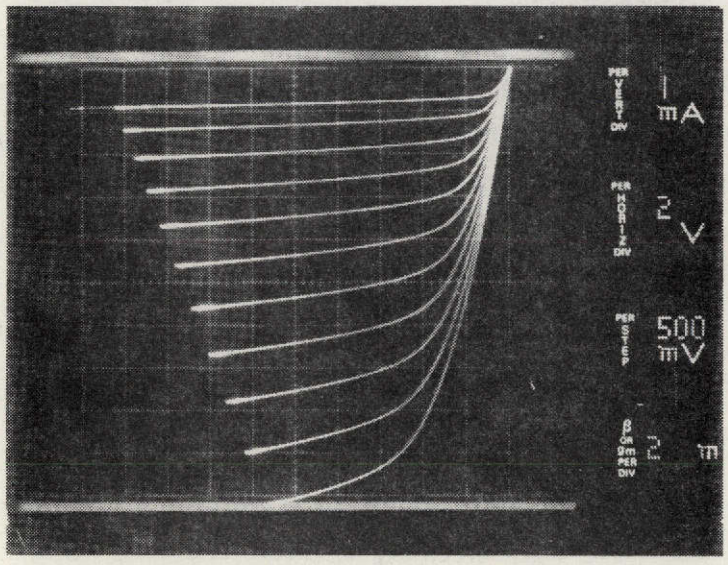
2. THRESHOLD VOLTAGE AND CHANNEL CONCENTRATION

Process parameters such as surface states, substrate resistivity, well surface concentration, etc. all vary from lot to lot. Meaningful diagnosis of our processing requires that each variable affecting the measured thresholds of the test transistors be isolated and checked for self consistency against the other measured data. To this end, test transistors were provided (on the



06172V

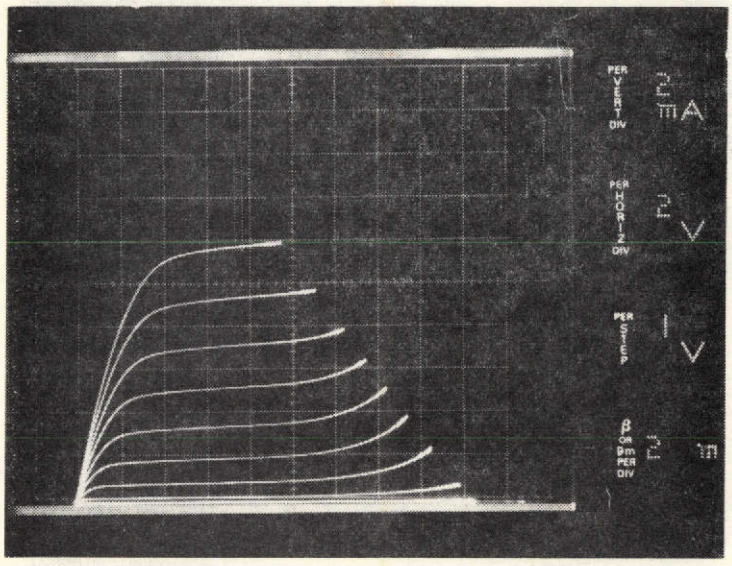
Figure 61. Typical Curve Display of Aluminum Metallized p-MOS Transistors



06173V

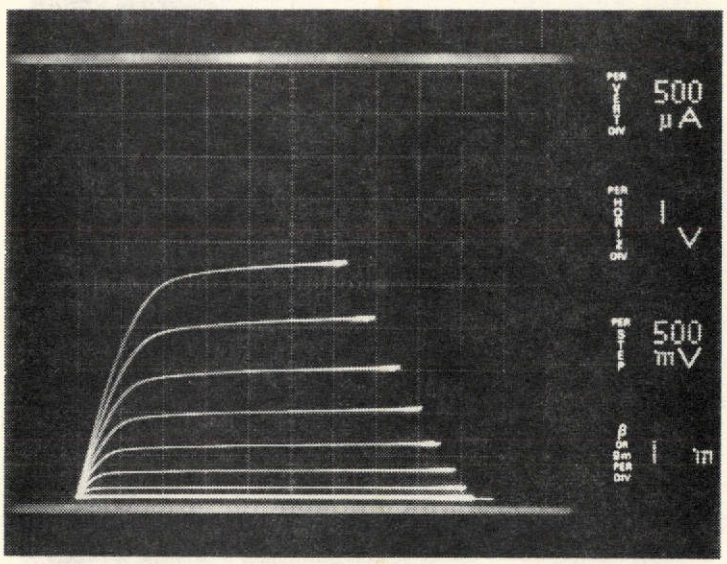
Figure 62. Typical Curve Display of Beam-Leaded p-MOS Transistors

Note: The currents in the on-condition vary between aluminum and beam-lead metallization due to differences in the annealing cycle for fast surface states.



06174V

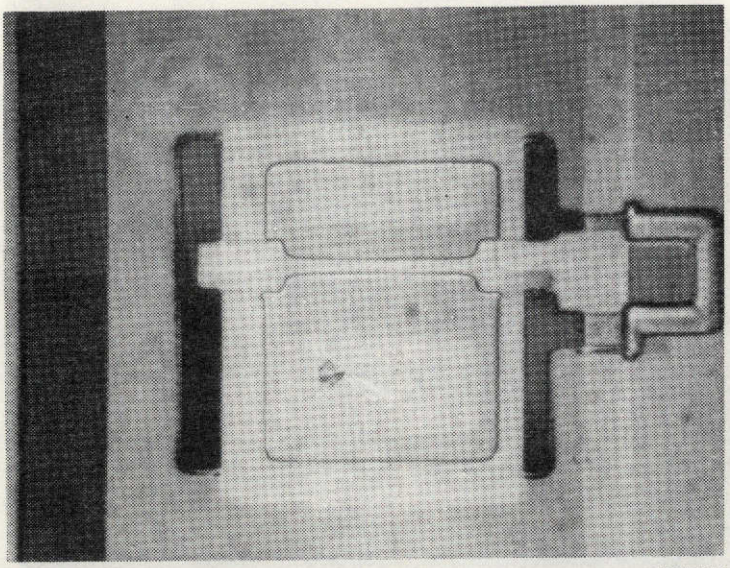
Figure 63. Typical Curve Display of Aluminum Metallized n-MOS Transistors



06175V

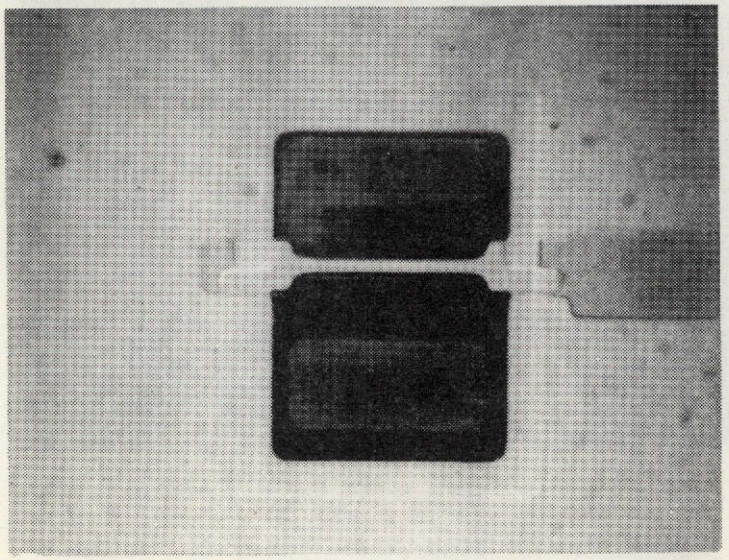
Figure 64. Typical Curve Display of Beam-Leaded n-MOS Transistors

Note: The drain currents in the on-condition vary between aluminum and beam-lead metallization due to differences in the annealing cycle to saturate fast surface states.



06374V

Figure 65. Stained n-MOS Test Transistor with Polysilicon Gate and All Oxides Removed; L (Effective) ≅ 0.20 MIL; Effective Gate Width 2.35 Mils



06375V

Figure 66. Stained p-MOS Test Transistor with Polysilicon Gate and All Oxides Removed; L (Effective) ≅ 0.22 MIL; Effective Gate Width 2.35 Mils

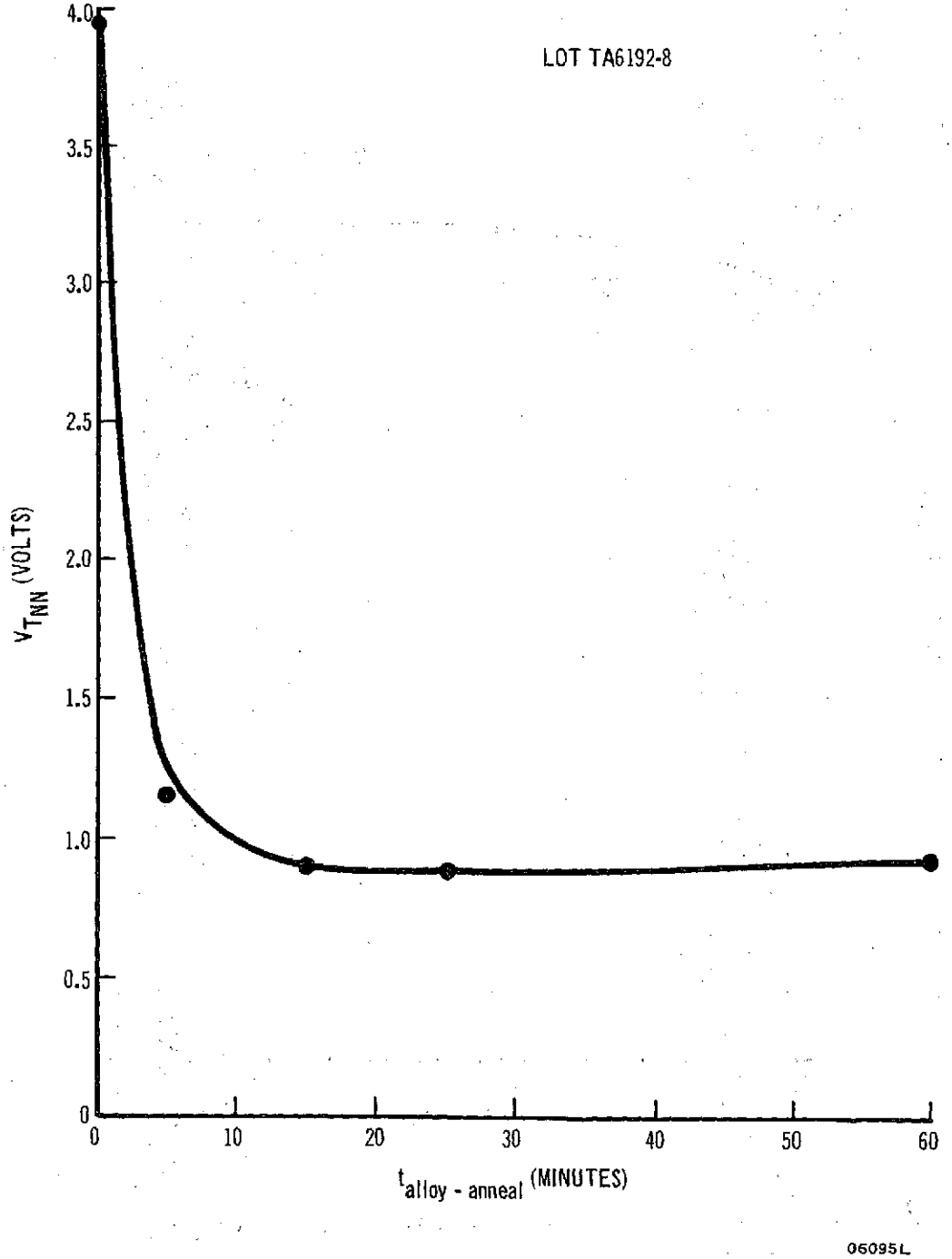


Figure 67. Variation of $V_{T_{NN}}$ as a Function of the Alloy-Anneal Time for an n-MOS Test Transistor

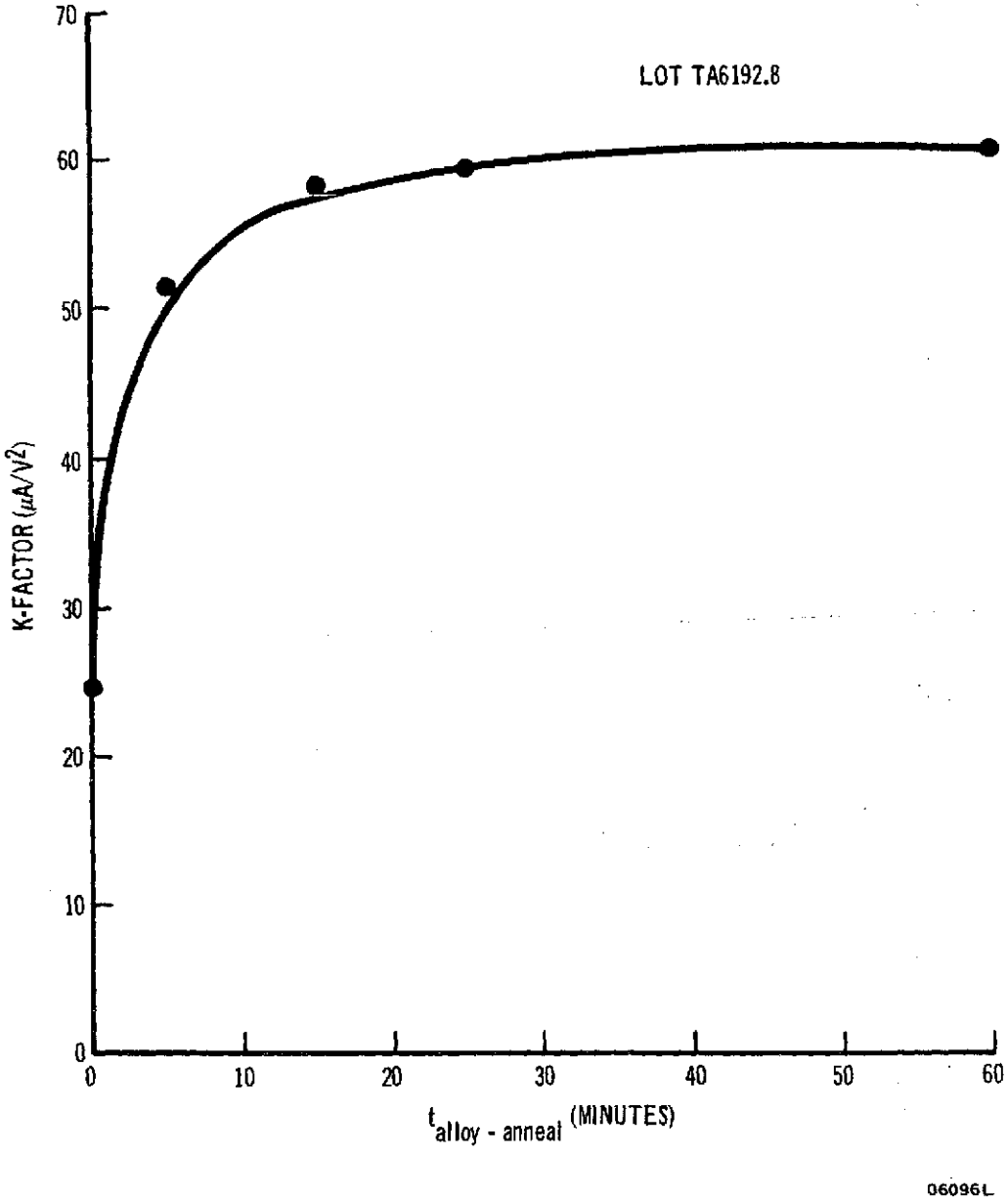


Figure 68. Variation of the K-Factor as a Function of the Alloy-Anneal Time for an n-MOS Test Transistor

ALU chip) which allow the measurement of p-MOS and n-MOS thin-oxide thresholds as a function of substrate bias, and p-MOS and n-MOS field-oxide thresholds were measured. The following data are taken on each completed lot:

1. The thin-oxide-transistor thresholds for currents between 1 microampere and 625 microamperes (see Appendix B), and substrate bias voltages of 0, 1, 3, 5, and 8 volts.
2. The field-oxide-transistor thresholds for currents between 1 microampere and 625 microamperes at zero substrate bias.

The matrix of values from the first set of data (1) is used to determine (see Appendix B):

1. V_{TO}, from the intercept of the "best fitted" $\sqrt{I_d}$ versus V_g curve.
2. N_{ss} corresponding to that threshold for 1100 Å oxide.
3. $\bar{N}_{well}$ from $V_t = V_o + \text{const}\sqrt{N}\left(\sqrt{|V_{sub}| + 2V_f}\right)$ . . . . . (3)

   by solving for two different values of substrate bias, subtracting to eliminate V_o, and solving for N.

   The result is

   $$N = F(V_f) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

   where

   $$V_f = \frac{KT}{q} \ell n \left[(N + n_i)/n_i\right] \ldots\ldots\ldots\ldots\ldots\ldots (5)$$

   Thus Eq. (4) implicitly contains N on both sides and is difficult to solve. An iterative procedure is used whereby an assumed value of V_f is used in Eq. (4) to get a first approximation for N; this value is then used in Eq. (5) to get a better value for V_f.

   The process is repeated until the values of N converge.

4. $\bar{N}_{sub}$ for the p-MOS devices using a technique similar to (3).

The field-oxide measurements from Eq. (4) are used to determine:

5. V_{TFO} in a manner similar to (1)

6. N_{ss} for the field oxide

The programs for threshold determination use the following equations:

1. For n-MOS (n^+ Polysilicon Gate)

$$V_{TN} = -0.55 - \frac{qN_{ss}}{C_{ox}} + \frac{\sqrt{2q\varepsilon_o \varepsilon_{si} N_A (2|V_f| + V_{sub})}}{C_{ox}} + V_f \quad \ldots\ldots\ldots (6)$$

2. For p-MOS (p^+ Polysilicon Gate)

$$V_{TP} = 0.55 - \frac{qN_{ss}}{C_{ox}} - \frac{2q\varepsilon_o \varepsilon_{si} N_D (2V_f + V_{sub})}{C_{ox}} - V_f \quad \ldots\ldots\ldots (7)$$

Examples of individual data from a typical lot are given in Tables X through XVI. Data taken from past lots are tabulated in Tables XVII and XVIII.

A nominal value of 1 volt ±0.5 volt was the design point for the absolute value of both p-MOS and n-MOS thresholds. This was met consistently in most lots after lot E-8. A surface-state density of $7 \times 10^{10}/cm^2$ was also targeted, as well as a p-well surface concentration of $1.4 \times 10^{16}/cm^3$. Tables X and XI show past results, and Tables XII and XIII show more recent test data which include ion-implanted wells.

3. PARAMETERS AFFECTING CHIP YIELD

The test-transistor data for wafer lots processed since the Tenth Quarterly Report are shown in Tables XIX and XX. The second column shows the yield to date which falls into two groups - chips that function at 10 volts and chips that function at 6 volts or lower. All lots were processed with the latest mask set which includes corrections for the stepped-oxide sloping, line-to-line p^+ and p-well diffusions, and elimination of most of the redundant notches.

TABLE X. ROOM-TEMPERATURE RAW DATA OF NEEDED GATE/DRAIN VOLTAGE TO ACHIEVE DRAIN CURRENTS FROM 1 TO 625 MICROAMPERES

TCC049N n-Poly-Silicon (1100 A SiO2, 1-2 Ohmcm N) Lot 37C, Wafer 5

TEMP DEG	VSUB VOLTS	VG (VOLTS) @ ID= 1	16	49	100	169	256	361	484	625 UA
25	0.0	1.26	1.67	2.00	2.32	2.64	2.97	3.29	3.63	3.96
25	1.0	2.17	2.56	2.87	3.17	3.47	3.78	4.10	4.42	4.75
25	3.0	3.49	3.86	4.16	4.44	4.73	5.03	5.33	5.64	5.96
25	5.0	4.54	4.91	5.19	5.47	5.75	6.04	6.34	6.64	6.95
25	8.0	5.87	6.24	6.51	6.78	7.05	7.34	7.62	7.92	8.22

TCC049P p-Poly-Silicon (1100 A SiO2, 1-2 Ohmcm N) Lot E116, Wafer 1

TEMP DEG	VSUB VOLTS	VG (VOLTS) @ ID= 1	16	49	100	169	256	361	484	625 UA
25	0.0	1.35	1.89	2.38	2.88	3.38	3.90	4.43	4.97	5.53
25	1.0	1.92	2.40	2.84	3.31	3.79	4.29	4.80	5.34	5.88
25	3.0	2.55	2.97	3.40	3.85	4.30	4.79	5.29	5.81	6.34
25	5.0	2.92	3.36	3.77	4.20	4.67	5.14	5.64	6.15	6.68
25	8.0	3.34	3.78	4.19	4.62	5.07	5.55	6.04	6.55	7.08

NOTE: Substrate bias is a parameter.

TABLE XI. EXTRAPOLATED THRESHOLD VOLTAGE FOR SIX STATISTICAL BLOCK SIZES

TCC049N n-Poly-Silicon (1100 A SiO2, 1-2 Ohmcm N) Lot 37C, Wafer 5

ID RANGE UA	VT (VOLTS) @ VSUB= 0.0	1.0	3.0	5.0	8.0 VOLTS
1-625	1.200	2.107	3.427	4.481	5.817
1-484	1.198	2.109	3.430	4.484	5.821
16-625	1.232	2.134	3.451	4.506	5.845
16-484	1.236	2.143	3.462	4.515	5.855
49-625	1.230	2.124	3.441	4.490	5.829
49-484	1.235	2.137	3.456	4.503	5.842

TCC049P p-Poly-Silicon (1100 A SiO2, 1-2 Ohmcm N) Lot E116, Wafer 1

ID RANGE UA	VT (VOLTS) @ VSUB= 0.0	1.0	3.0	5.0	8.0 VOLTS
1-625	1.168	1.706	2.316	2.697	3.121
1-484	1.181	1.726	2.338	2.720	3.145
16-625	1.161	1.674	2.266	2.654	3.079
16-484	1.182	1.701	2.295	2.685	3.112
49-625	1.128	1.619	2.210	2.588	3.014
49-484	1.154	1.649	2.245	2.624	3.053

NOTE: Substrate bias is a parameter.

TABLE XII. K-FACTOR AS A FUNCTION OF STATISTICAL BLOCK SIZE

TCC049N n-Poly-Silicon (1100 A SiO2, 1-2 Ohmcm N) Lot 37C, Wafer 5

ID RANGE UA	K-FACTOR (UA/V2) @ VSUB= 0.0	1.0	3.0	5.0	8.0 VOLTS
1-625	81.7	90.0	98.4	103.4	109.3
1-484	81.5	90.6	99.2	104.3	110.2
16-625	84.5	92.7	101.0	106.4	112.9
16-484	85.0	94.3	103.2	108.6	115.4
49-625	84.3	91.7	100.0	104.7	110.8
49-484	85.0	93.7	102.5	107.0	113.4

TCC049P p-Poly-Silicon (1100 A SiO2, 1-2 Ohmcm N) Lot E11o, Wafer 1

ID RANGE UA	K-FACTOR (UA/V2) @ VSUB= 0.0	1.0	3.0	5.0	8.0 VOLTS
1-625	33.5	37.1	40.2	41.1	41.6
1-484	34.2	38.2	41.7	42.6	43.3
16-625	33.4	36.3	38.8	39.8	40.4
16-484	34.2	37.5	40.3	41.4	42.1
49-625	32.7	35.0	37.4	38.1	38.7
49-484	33.6	36.1	38.8	39.6	40.3

NOTE: Substrate bias is used as a parameter.

TABLE XIII. COMPLEMENT OF CORRELATION COEFFICIENT IN PARTS PER MILLION (PPM) AS A FUNCTION OF STATISTICAL BLOCK SIZE AND SUBSTRATE BIAS

TCC049N n-Poly-Silicon (1100 A SiO2, 1-2 Ohmcm N) Lot 37C, Wafer 5

ID RANGE UA	(1-R) (PPM) @ VSUB = 0.0	1.0	3.0	5.0	8.0 VOLTS
1-625	329.	326.	326.	363.	460.
1-484	464.	455.	438.	495.	634.
16-625	30.	133.	172.	191.	233.
16-484	28.	85.	99.	132.	173.
49-625	42.	161.	215.	183.	217.
49-484	45.	119.	144.	136.	173.

TCC049P p-Poly-Silicon (1100 A SiO2, 1-2 Ohmcm N) Lot E116, Wafer 1

ID RANGE UA	(1-R) (PPM) @ VSUB = 0.0	1.0	3.0	5.0	8.0 VOLTS
1-625	177.	544.	859.	882.	905.
1-484	106.	423.	707.	703.	690.
16-625	246.	572.	702.	841.	899.
16-484	159.	488.	586.	718.	739.
49-625	212.	375.	532.	527.	617.
49-484	132.	306.	453.	416.	482.

TABLE XIV. CHANNEL CONCENTRATION (in 10^{16} cm^{-3}) FOR n-POLYSILICON-GATE n-MOS TRANSISTORS AS CALCULATED FROM EQ. (13), APPENDIX B

TCC049N n-Poly-Silicon (1100 A SiO2, 1-2 Ohmcm N) Lot 37C, Wafer 5

	N (DIFFERENTIALS) X 1.0E+16 (CM-3) FOR VSUB2 - VSUB1									
ID RANGE UA	8.0 0.0	5.0 0.0	3.0 0.0	8.0 -1.0	5.0 -1.0	3.0 -1.0	8.0 -3.0	5.0 -3.0	3.0 -3.0	VOLTS
										AVG=
1-625	1.33	1.25	1.17	0.86	0.64	0.40	0.35	0.12	0.00	0.77
1-484	1.34	1.26	1.18	0.86	0.64	0.40	0.35	0.12	0.00	0.77
16-625	1.33	1.25	1.16	0.86	0.64	0.40	0.35	0.12	0.00	0.76
16-484	1.34	1.25	1.17	0.86	0.64	0.40	0.35	0.12	0.00	0.77
49-625	1.32	1.24	1.15	0.86	0.64	0.40	0.35	0.12	0.00	0.76
49-484	1.33	1.24	1.16	0.86	0.64	0.40	0.35	0.12	0.00	0.76
AVG=	1.33	1.25	1.17	0.86	0.64	0.40	0.35	0.12	0.00	

NOTE: The seven rightmost columns should be considered inaccurate due to limited range of substrate biases used.

TABLE XV. CHANNEL CONCENTRATION (in 10^{15} cm^{-3}) FOR p-POLYSILICON-GATE p-MOS TRANSISTORS AS CALCULATED FROM EQ. (14), APPENDIX B

TCC049P p-Poly-Silicon (1100 A SiO2, 1-2 Ohmcm N) Lot E116, Wafer 1

	N (LEAST SQUARE FIT) X 1.0E+15 (CM-3) @ VSUB RANGE=									
ID RANGE UA	0.0 -8.0	0.0 -5.0	0.0 -3.0	1.0 -8.0	1.0 -5.0	1.0 -3.0	3.0 -8.0	3.0 -5.0	3.0 -3.0	VOLTS
										AVG=
1-625	2.52	2.69	2.86	2.36	2.52	2.69	2.16	2.26	0.00	2.51
1-484	2.54	2.71	2.89	2.37	2.53	2.71	2.16	2.26	0.00	2.52
16-625	2.48	2.62	2.76	2.35	2.49	2.61	2.18	2.30	0.00	2.47
16-484	2.50	2.64	2.78	2.36	2.50	2.62	2.19	2.31	0.00	2.49
49-625	2.44	2.57	2.70	2.33	2.46	2.61	2.16	2.24	0.00	2.44
49-484	2.46	2.59	2.72	2.34	2.48	2.63	2.17	2.24	0.00	2.45
AVG=	2.49	2.64	2.78	2.35	2.49	2.65	2.17	2.27	0.00	

TABLE XVI. n-SUBSTRATE RESISTIVITY AS CALCULATED FROM TABLE XV

TCC049P p-Poly-Silicon (1100 A SiO2, 1-2 Ohmcm N) Lot E116, Wafer 1

	RHO X 1.0E+00 (OHMCM) N-TYPE @ VSUB RANGE=									
ID RANGE UA	0.0 -8.0	0.0 -5.0	0.0 -3.0	1.0 -8.0	1.0 -5.0	1.0 -3.0	3.0 -8.0	3.0 -5.0	3.0 -3.0	VOLTS
										AVG=
1-625	1.84	1.73	1.63	1.96	1.84	1.73	2.14	2.04	0.00	1.86
1-484	1.83	1.72	1.62	1.95	1.84	1.72	2.13	2.04	0.00	1.86
16-625	1.87	1.77	1.69	1.97	1.87	1.78	2.12	2.01	0.00	1.89
16-484	1.86	1.76	1.68	1.96	1.86	1.77	2.11	2.00	0.00	1.88
49-625	1.90	1.81	1.72	1.99	1.88	1.78	2.14	2.06	0.00	1.91
49-484	1.89	1.80	1.71	1.98	1.87	1.77	2.13	2.06	0.00	1.90
AVG=	1.86	1.76	1.67	1.97	1.86	1.76	2.13	2.04	0.00	

NOTE: The nominal value of the silicon used is 1 to 2 ohms-cm

TABLE XVII. n-MOS TEST RESULTS OF PAST PROCESSED LOTS

TCC-049 Lot No.	Interconnect Metal	ρ_s Of Well ($\Omega/\square$)	Field-Oxide Transistor		Gate-Oxide Transistor				$\bar{n}_{well}$ From Sub. Bias
			V_{TFO} (Volts)	N_{ss} For Field Oxide	V_{TO} (Volts)	K	I-R (PPM)	N_{ss} For Gate Oxide	
1	Aluminum	1035	12.5	1.7×10^{11}	0.97	190	870	9×10^{10}	2.1×10^{16}
2	Aluminum	990	-	-	0.84	199	-	-	-
3*	Al + B.L.	1100	-	-	-2.4	78	-	-	-
4*	Aluminum	1140	8.5	3×10^{11}	-2.1	80	51	3×10^{11}	1.5×10^{16}
4E	Aluminum	1140	11.2	3.5×10^{10}	2.13	83	630	-	2×10^{16}
285*	Aluminum	994	3.3	3.4×10^{11}	0.51	39	54	2.3×10^{11}	1.3×10^{16}
2E	Al + B.L.	1280	17	-	2.89	45	398	2×10^{10}	2.5×10^{16}
303	Al + B.L.	824	18.2	5.4×10^{10}	1.15	68	164	1.2×10^{11}	1.2×10^{16}
E-8	Beam Lead		14.6	0	0.88	89	110	7×10^{10}	7.2×10^{15}
E-14	Beam Lead		18.3	**-9×10^{10}	1.17	80	92	6×10^{10}	9.5×10^{15}
10	Beam Lead		11.2	8×10	1.16	85	262	8.7×10^{10}	1.1×10^{16}
E-21	Beam Lead		15.8	7×10^{10}	1.1	64	37	1.3×10^{11}	1.3×10^{16}
31	Beam Lead		17.4	1×10^{10}	1.5	91	68	2×10^{10}	1.1×10^{16}
E-26A†	Beam Lead		12.4	6×10^{10}	0.82	59	15	1×10^{11}	8.7×10^{15}

* Depletion mode n-MOS transistors due to high surface-state density.

** Negative N_{ss} indicates inaccuracy in the $\bar{n}_{WELL}$.

† Corrected TCC049 Mask.

TABLE XVIII. p-MOS TEST RESULTS OF PAST PROCESSED LOTS

TTC-049 Lot No.	Interconnect Metal	ρ Substrate (Ωcm)	Field-Oxide Transistor		Gate-Oxide Transistor				$\bar{\rho}_{sub.}$ From Sub Bias
			V_{TFO} (Volts)	N_{ss} For Field Oxide	V_{TO} (Volts)	K	1-R (PPM)	N_{ss} For Gate Oxide	
1	Aluminum	1 to 2	-13	1.3×10^{11}	-1.03	60	880	8×10^{10}	-
2	Aluminum	1 to 2	-	-	-0.61	35	-	-	-
3*	Al + B.L.	1 to 2	-	-	-2.3	28	598	3.2×10^{11}	-
4*	Aluminum	1 to 2	-23.6	3.5×10^{11}	-2.4	23	490	3×10^{11}	-
4E	Aluminum	1 to 2	-12.3	3.3×10^{10}	-0.96	68	166	5.6×10^{10}	-
285*	Aluminum	1 to 2	-	-	-1.97	55	324	1.1×10^{11}	5 Ωcm
2E	Al + B.L.	1 to 2	-15.2	3.5×10^{10}	-0.87	32	206	5.4×10^{10}	2.4 Ωcm
303	Al + B.L.	1 to 2	-21.3	2×10^{11}	-1.45	33	420	1.4×10^{11}	2.1 Ωcm
E-8	Beam Lead	1 to 2	-14.7	1.6×10^{11}	-1.42	34	182	1.2×10^{10}	1.7
E-14	Beam Lead	1 to 2	-34.7	6×10^{11}	-1.49	30	93	1.3×10^{11}	1.6
10	Beam Lead	1 to 2	-12.2	1.4×10^{11}	-0.96	33	350	8×10^{10}	2.5
E-21	Beam Lead	1 to 2	-14.4	1.2×10^{11}	-1.2	30	74	1.3×10^{11}	2.3
31	Beam Lead	1 to 2	-20.3	2.4×10^{11}	-1.4	23	619	1.6×10^{11}	2.7
E-26A†	Beam Lead	1 to 2	-22.5	2.6×10^{11}	-1.35	24	127	1.4×10^{11}	2.3

* High-threshold p-MOS transistors - due to high surface-state density.

† Corrected TCC-049 mask.

TABLE XIX. TYPICAL n-MOS TEST TRANSISTOR PARAMETERS - RECENTLY PROCESSED LOTS

TCC-049A Lot No.	ALU Chip Yield	ρ_s ($\Omega/\square$) of n^+ Doped Oxide	Field-Oxide Transistor		Gate-Oxide Transistor						$\bar{n}_{WELL}$ From Sub. Bias
			V_{TFO} (Volts)	N_{ss} For Field Oxide	V_{TO} (Volts)	BV_{SD} (Volts)	K	I-R (PPM)	I_D (mA) $V_{DS} = V_{GS} = 10V$	N_{ss} For Gate Oxide	
35A	2	24			1.1	18	60	46	4.2	1.2×10^{11}	1.4×10^{16}
35B	17	150	8.9	3×10^{11}	1.7	18	63	56	3.5	1.1×10^{11}	2.3×10^{16}
37B	53†	18	14.2	4.5×10^{10}	1.2	21	85	31	4.8	6.3×10^{10}	1.2×10^{16}
37C	32†	31	12.8	1.2×10^{11}	1.4	20	79	55	4.5	6.0×10^{10}	1.4×10^{16}
E-105	2	25	10.3	1.5×10^{11}	0.86	20	59	45	4.1	1.5×10^{11}	1.3×10^{16}
38C	15†	77	9.5	1.8×10^{11}	0.94	20	61	174	4.0	1.6×10^{11}	1.4×10^{16}
39C	32	45	13.3	3×10^{11}	2.6	18	51	200	2.6	2×10^{10}	3.0×10^{16}

†6-volt operation only.

TABLE XX. TYPICAL p-MOS TEST TRANSISTOR PARAMETERS - RECENTLY PROCESSED LOTS

TCC-049A Lot No.	ALU Chip Yield	ρ_s ($\Omega/\square$) of p^+ Doped Oxide	Field-Oxide Transistor		Gate-Oxide Transistor						$\bar{\rho}_{sub}$ From Sub. Bias
			V_{TFO} (Volts)	N_{ss} For Field Oxide	V_{TO} (Volts)	BV_{SD} (Volts)	K	1-R (PPM)	I_D (mA) $V_{DS} = V_{GS} = 10V$	N_{ss} For Gate Oxide	
35A	2	23			-1.03	-23	35	132	-3.5	7.7×10^{10}	1.6
35B	17	18			-1.3	-24	19	117	-2.2	1.1×10^{11}	1.3
37B	53†	24	-10.8	6×10^{10}	-0.96	-25	34	126	-2.4	7.6×10^{10}	1.5
37C	32†	17			-0.65	-23	36	205	-2.5	5×10^{10}	1.6
E-105	2	20	-14.9	1.1×10^{11}	-1.6	-22	24	70	-1.9	1.7×10^{11}	1.3
38C	15†	25	-22.7	3×10^{11}	-1.3	-23	32	185	-2.0	2×10^{11}	3
39C	32	35	-8.9	6×10^{10}	-0.7	-25	35	250	-2.3	7×10^{10}	3

†6-volt operation only.

The problems associated with these omissions are discussed elsewhere. The maximum wafer yield was about 30 percent, but the average yield is much less than this. Also, comparison of columns two and three of Table XIX indicate that 10-volt yield is only appreciable when the n^+ doped-oxide resistivity exceeds 45 ohms/□. These facts indicate that the masks are still not optimum for high yield. Two problems remain. The first is mask runout, which makes for a large variation in yield between wafers of the same lot. Also, n^+-p^+ breakdowns of 6 volts indicate that a violation still exists in the distance between diffused areas of different doping types. A look at the large variation in supply leakage (I_L for V_{DD} = 10 volts) over a single wafer - from 1 microampere to 10 milliamperes - confirms that there is not enough margin between the process and the masks (see Figure 69). We have demonstrated, however, that by increasing the n^+ source-drain resistivity, the existing mask set can be used to produce 10-volt devices with resonable yield. But this is accomplished at the cost of a reduction in n-MOS current output and, hence, speed.

D. TEST-CIRCUIT PERFORMANCE

1. MOS ARRAY FUNCTIONAL TESTING

The MOS-array tester used is a rack-mounted test generator consisting of three separate panel-mounted units. The first unit is a 40-word by 100-bit word generator, the second unit is a clock generator, and the third unit is a work area. The word generator is capable of 40 separate outputs, each with a separately adjustable zero and one level. Each word is programmed by diode pins in matrix boards situated on the front of the generator. Each diode pin causes a transition from ground to -V level or vice versa. The clock generator was not used. The work area has four built-in power supplies and a 40-pin array socket which is connected to the appropriate probe card. Functional testing is done on an MOS-array tester. A functional-test pattern is generated and applied to the array under test (a) at wafer sort, using a face-up probe card; (b) after back etch and separation, using a face-down probe card; and (c) after packaging, prior to shipping. In addition to supplying the test inputs to the array, the pattern contains the expected outputs from the array for comparison with the actual array outputs. The test pattern exercises all the inputs to every gate in the array to assure that each input performs correctly. Comparison was made on a Hewlett-Packard 547 oscilloscope.

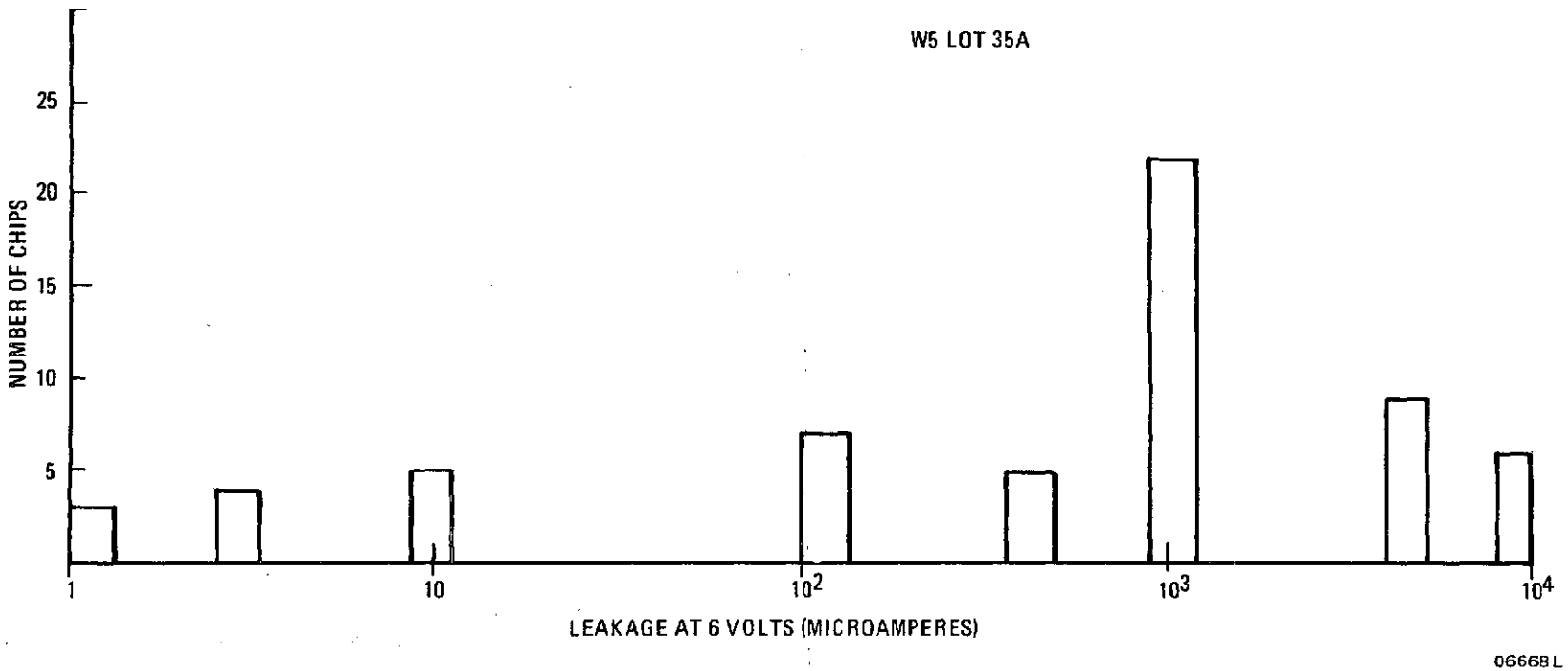


Figure 69. Typical Leakage Distribution on Wafer – All Chips

2. PROPAGATION-DELAY AND PAIR-DELAY MEASUREMENTS ON NOR CHAINS

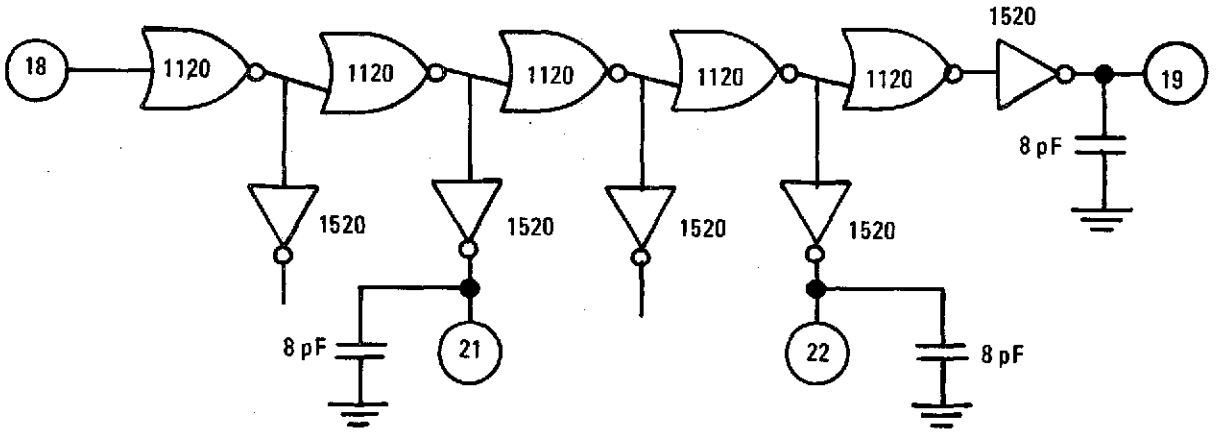
The five-stage NOR gate (silicon gate) test circuit shown in Table XXI consists of five 1120's and one 1520. The results of the propagation-delay measurements made with this circuit are given in Table XXI. Note that the average delay at 10 volts is 11 nanoseconds, as opposed to about 14 nanoseconds for the aluminum-gate design. About 2 to 3 nanoseconds of this 11-nanosecond total came from the polysilicon interconnect resistance, which is absent in the aluminum-gate circuit. The polysilicon gate length (as defined by the mask) was 0.25 mil on all devices. Table XXII shows the NOR gate pair-delay test circuit and the results of the measurements made with it. The delay per stage is about 12.5 nanoseconds due to the added complexity of this circuit.

Table XXIII shows several silicon-gate test transistor parameters for lots processed previously. Included at the bottom is some data for equivalent aluminum-gate devices. The most important performance parameter is the drain-current output, which is a strong function of effective channel length as shown. The only speed data taken were measured on lot E-8. A comparison of the drain-current output for each lot listed shows that lots 2 and 10 would have given much shorter delays. The higher drain currents of these lots were obtained at the expense of breakdown voltage and, to a smaller extent, overlap capacitance. These considerations are at variance with more recent yield data. n-MOS current output had to be depressed in order to obtain appreciable yield at 10 volts with the masks in hand (see Table XIX), and so slower than optimum speeds are to be expected from most, but not all of these lots. In the next paragraph, the factors affecting yield will be detailed.

E. YIELD ANALYSIS

When early wafer lots were processed with aluminum to reduce processing time, it was found that the most complicated circuits were not operational due to metal discontinuity. In some cases the polysilicon lines were marginal where they crossed the stepped (field) oxide (see Figures 70 and 71). A sloped stepped-oxide process, developed at RCA, was introduced to solve this problem. Scanning electron microscope pictures of our improved process (Figures 72 through 74) show the excellent polysilicon and beam-lead continuity now being achieved.

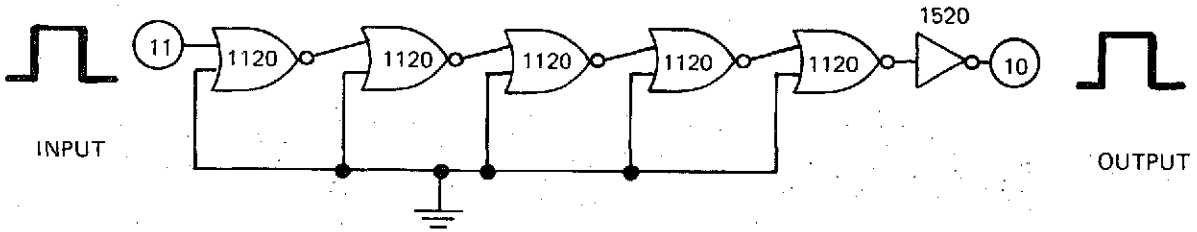
TABLE XXI. PERFORMANCE OF THE NOR GATE WITH PAIR DELAY



TCC-049 Chip No.	Delay 18 21	Delay 18 21	Delay 18 19	Delay 18 19	Pair Delay 21 22	Pair Delay 21 22
E8-10	31	32	70	67	23	24
E8-11	34	37	76	74	26	26
E8-14	33	35	74	72	25	25
E8-18	33	36	78	75	26	27

Notes: 1. All delay times are in nanoseconds.
2. The estimated delay for the 1520 output buffer is approximately ≈ 10 nanoseconds.

TABLE XXII. PERFORMANCE OF THE FIVE-STAGE NOR GATE WITH PROPAGATION DELAY



TCC-049 Chip No.	10 Volts		12 Volts		15 Volts		Output Capacitance Pin 10 (pF)
	Delay 11 ⎍ 10 ⎍	Delay 11 ⎏ 10 ⎏	Delay 11 ⎍ 10 ⎍	Delay 11 ⎏ 10 ⎏	Delay 11 ⎍ 10 ⎍	Delay 11 ⎏ 10 ⎏	
E8-3	66	56	57	53	56	50	7.7
E8-4	70	63	58	55	43	50	8.0
E8-5	69	61	58	54	57	53	7.8
E8-6	70	62	58	56	57	51	7.7
	$V_{SS} - V_{DD} = 10$ V ⎍ Avg. ≃ 69 ns ⎏ Avg. ≃ 60.5 ns Avg. Per Stage ≃ 11 ns		$V_{SS} - V_{DD} = 12$ V ⎍ Avg. ≃ 58 ns ⎏ Avg. ≃ 54.5 ns Avg. Per Stage ≃ 9.5 ns		$V_{SS} - V_{DD} = 15$ V ⎍ Avg. ≃ 53 ns ⎏ Avg. ≃ 51 ns Avg. Per Stage ≃ 8.6 ns		

Notes: 1. All delay times are in nanoseconds.

2. The propagation delay for the equivalent aluminum-gate circuit ≃ 80 nanoseconds or ≃ 14 nanoseconds per stage.

TABLE XXIII. TEST TRANSISTOR DATA SHOWING THE PROCESS PARAMETERS THAT AFFECT SPEED

TCC-049 Lot No.	n-MOS					p-MOS					
	BV_{SD} (V)	I_D $V_{GS} = V_{DS}$ = 10 V (mA)	g_m (μ℧)	K	$L_{eff.}$	BV_{SD} (V)	I_D $V_{GS} = V_{DS}$ = 10 V (mA)	g_m (μ℧)	K	$L_{eff.}$	$L_{geo.}$ (mil)
E-8	19	4.2	800	89	0.16	-26	2	320	34	~0.16	0.24
E-14	22	3.6	800	78	~0.15	-27	2.4	300	30	~0.18	0.23
E-21	22	3.5	650	49	~0.19	-27	1.6	300	24	~0.19	0.27
10	20	5.3	820	85	~0.13	-28	3.1	370	33	~0.13	0.21
2	13	9.0	1100	258	~0.09	-14	6		81	~0.09	0.19
Aluminum-Gate Equivalent	21	3.6	~700	-	-	-35	1.4	~270	-	~0.20	0.3

Notes: 1. $L_{eff} = L_{geo} - 2X_j$ is an estimate of actual channel length.

2. The junction depth is $0.03 \leq X_j \leq 0.05$ mil.

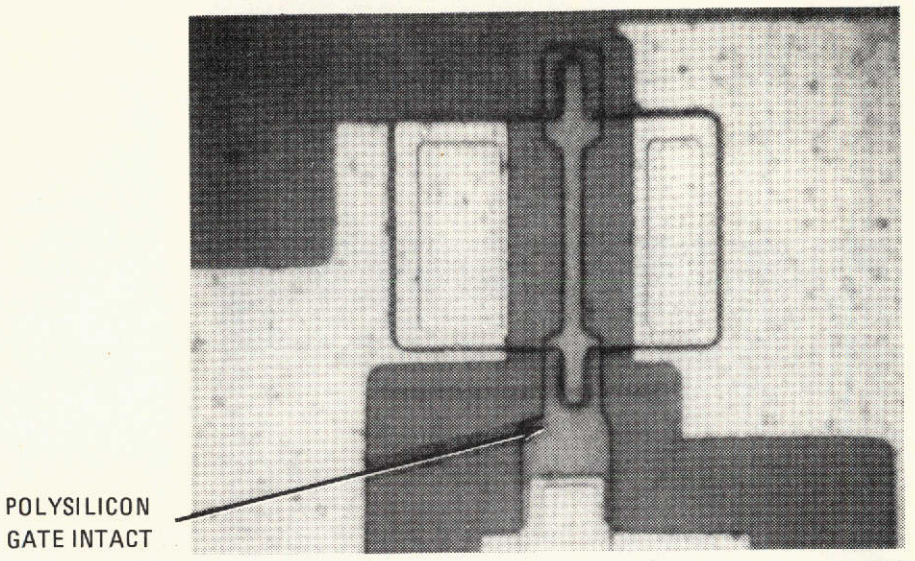


Figure 70. Tapered Stepped Oxide

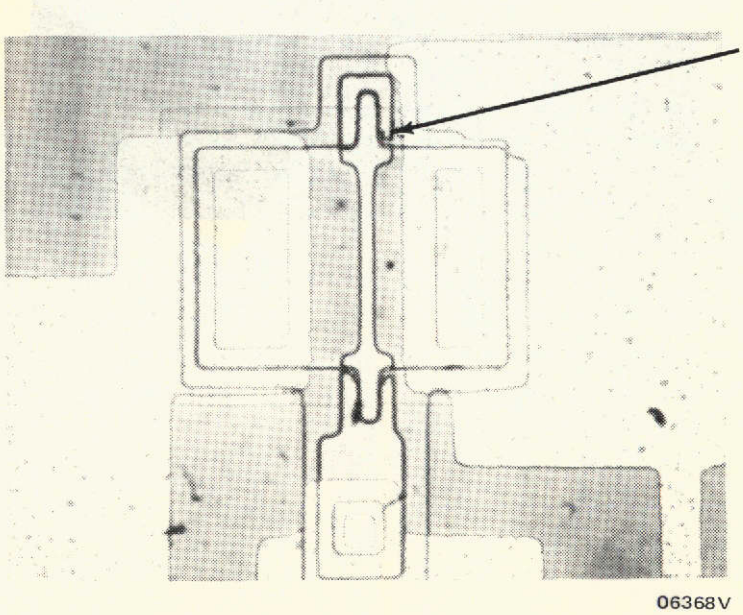


Figure 71. Standard Stepped Oxide

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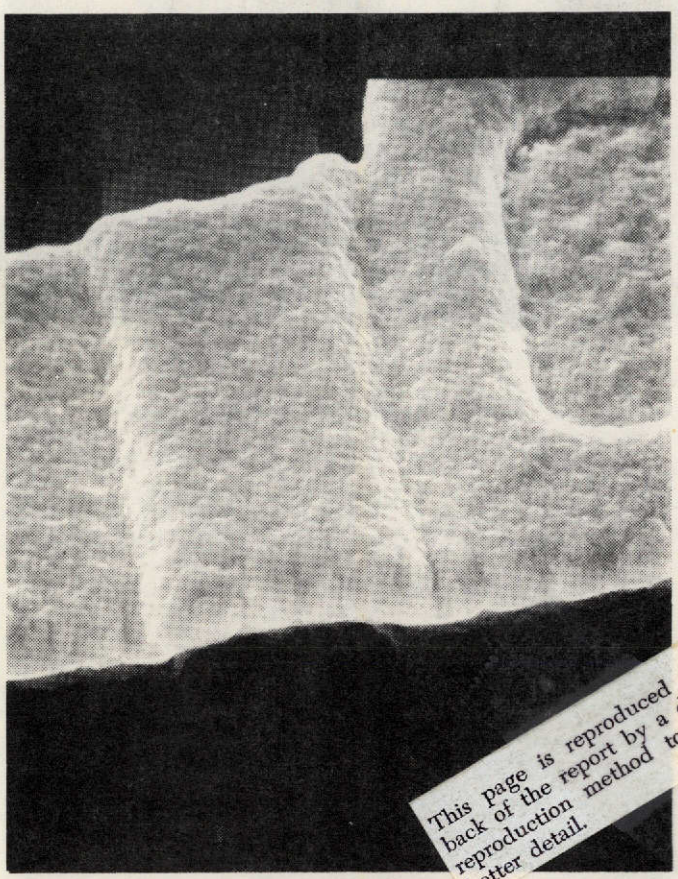
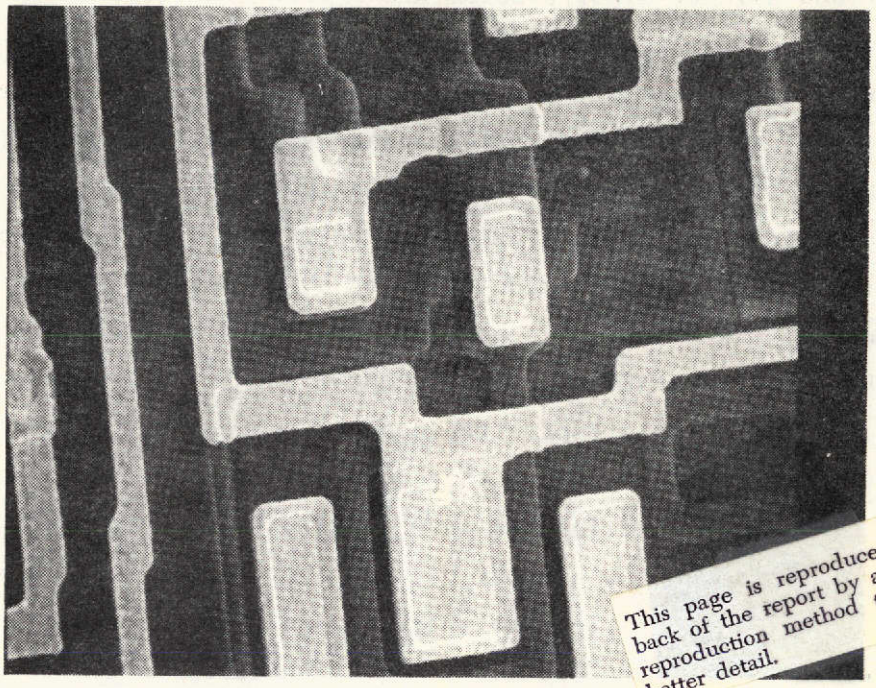


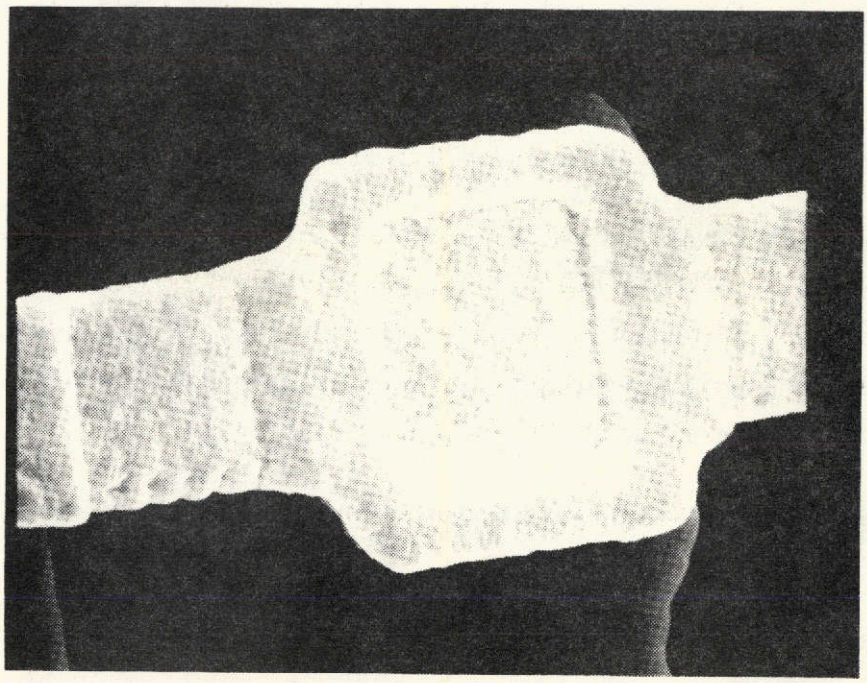
5000X 06369V

Figure 72. SEM Detail of Beam-Lead Metal Crossing Over Polysilicon



800X 06370V

Figure 73. SEM of a Portion of ALU Chip Showing Beam-Lead Interconnect Metal Crossing Polysilicon Lines.



06371V

Figure 74. SEM Detail Showing Beam-Lead Metal-to-Polysilicon Contact.

But several other problems kept the actual device yield of TCC-049 very low. Two major and several minor problem areas were identified. The first major problem was the result of the sloped-oxide etch that increases the hole in the thick oxide. Light emitting n^+p^+ junctions in the n^+ drain regions were observed. This indicated that the stepped-oxide edge had shifted so much from its original position (due to sloping) that both types of doped oxide (p^+ and n^+) were falling within a drain area, see Figure 75. This was rectified by tighter control of the sloped-oxide etch and by making the mask for the oxide hole 0.1 mil smaller all around. It had manifested itself electrically by low breakdown of the n^- MOS transistor. The second major problem was found in one particular cell. There, the ground strap contact between the p^+ guard band and the n^+ source was not fully covered with a deep well diffusion. Since the p^+ guard band and the n^+ source diffusion have roughly the same depth, process variations did or did not allow a short between the n^+ source and the n substrate, see Figure 76. Latest leakage currents are now in the microampere range as opposed to several hundred milliamperes on early lots.

Theoretical analysis indicates that only a 4.5-micron side-way diffusion is to be expected for an 8-micron deep well. At the corners of the oxide mask, only 2.5 microns are to be expected. The n-substrate areas between the well diffusions and the p^+ guard band were observed, especially around the corners. This increased the well leakage somewhat, but not catastrophically. A design rule change to increase the well mask by 0.1 mil was made.

A similar well-mask problem was caused by the library cell boundary conditions. The notches in the p-well areas, see Figure 77, allow cut-off of the n-MOS transistor even for somewhat "dirty" field oxide. For clean oxides they are not necessary and do increase the well perimeter and increase the p-well leakage to the n-substrate, however, not catastrophically.

Mask changes of the TCC-049 were made to correct all of the problems listed above.

F. LIFE TESTING

Beam-lead chips from various lots were packages in 24-lead DIC packages for life testing. The wiring of the life-test board is shown in Figure 78.

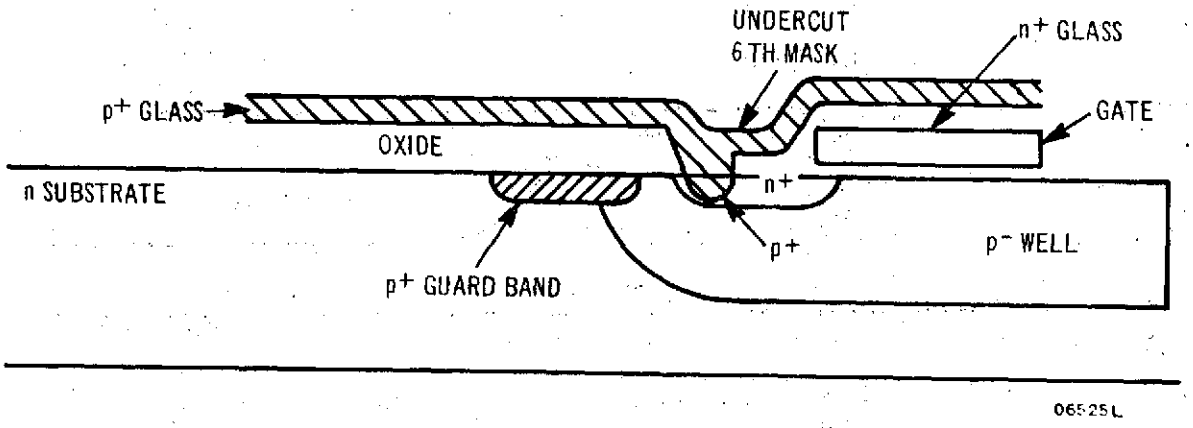


Figure 75. n^+ - p^+ Diode Resulting from Enlarged Stepped-Oxide Mask and Undercut Doped-Oxide Mask

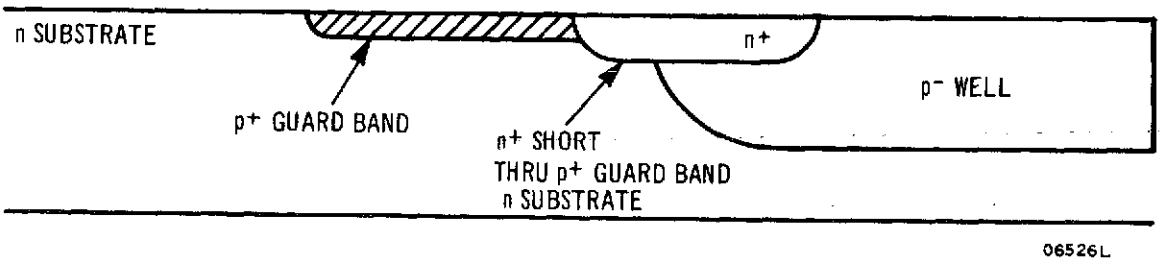


Figure 76. n^+ Source Diffusion Shorting out p^+ Guard Band

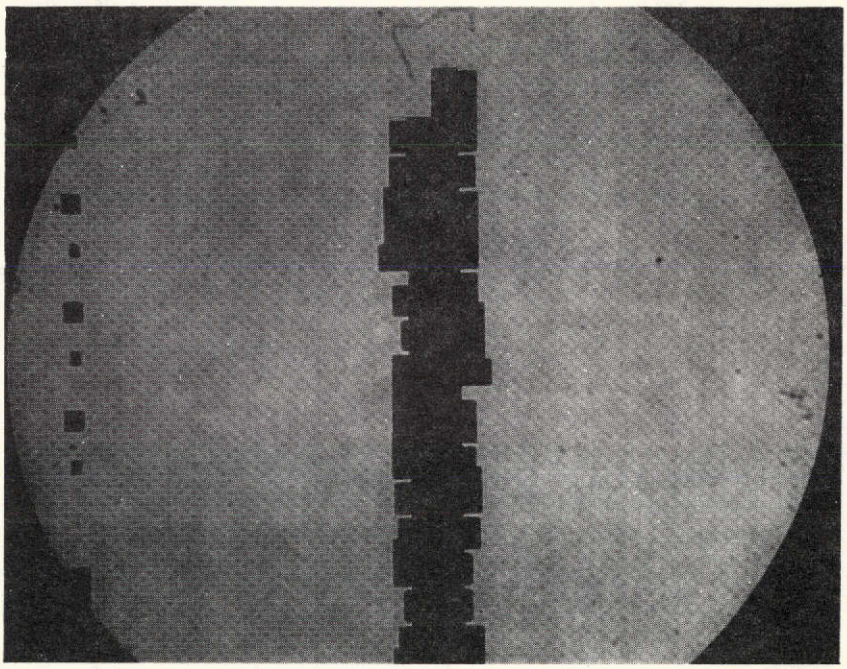


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Figure 77. TCC-049 Level-One Mask (Well)

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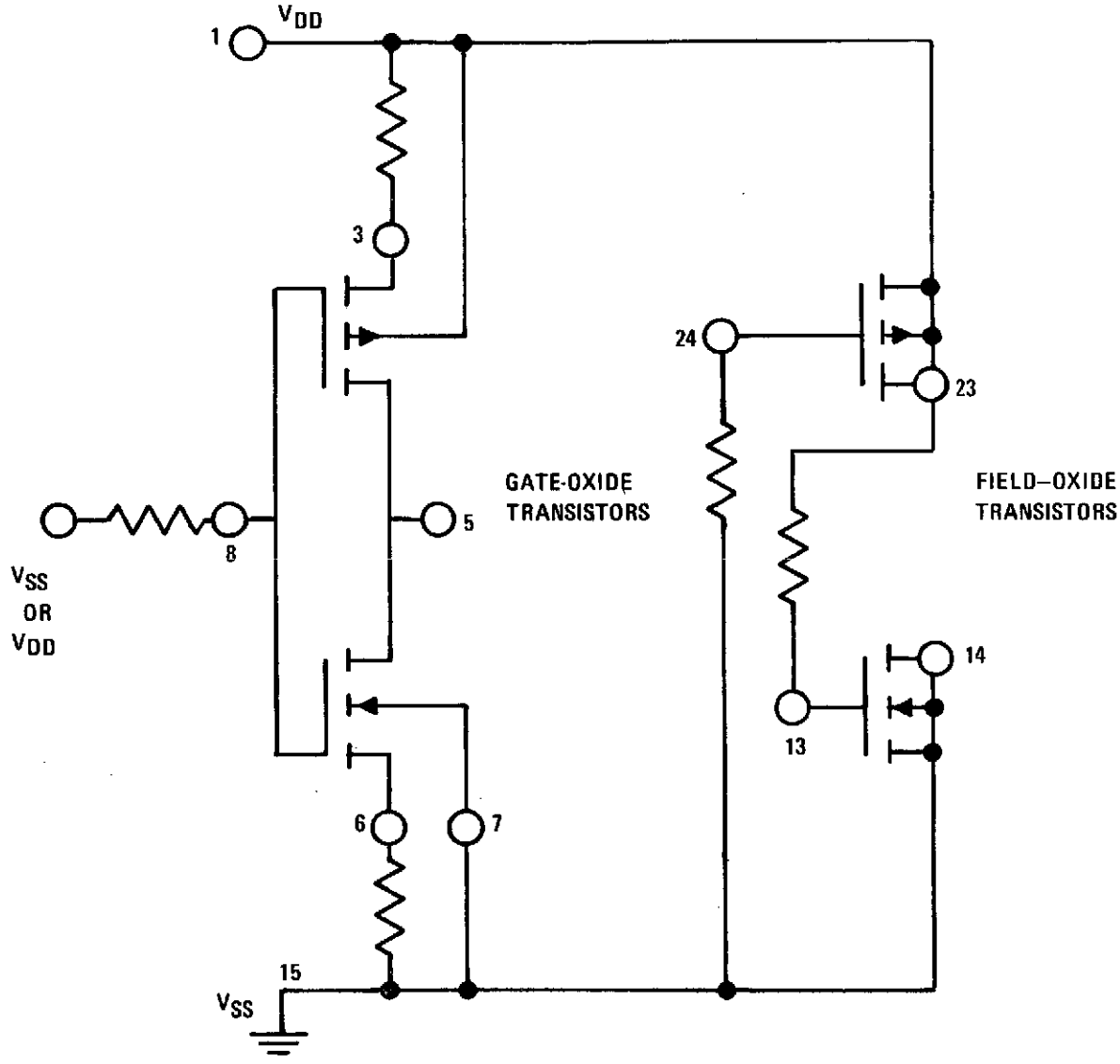

Figure 78. Bias Life-Test Circuit for TCC-049A Test Transistors

The two complementary-gate-oxide transistors are connected in the inverter mode. The common-gate connection (pin 8) is connected to V_{DD} for half the devices under test and to V_{SS} for the other half. Thus, the p-MOS devices are on in half the samples and the n-MOS devices are on the other half. The field-oxide devices are connected as capacitors during test to simulate the situation on the actual chip. Changes in the thresholds of these devices give us a measure of the amount of ion drift in the field oxide.

1. OPERATING LIFE-TEST DATA

Twelve units from lot E-14 were placed on life test at 125°C. The p-MOS and n-MOS thresholds, measured after intervals of 168 hours, 336 hours, and 500 hours on four typical units, are shown in Figure 79. The maximum shift on the n-MOS gates (n^+ doped polysilicon) is of the order of 12 percent. For the p-MOS gates (p^+ doped polysilicon), however, the shift after 500 hours under life is over 300 percent in the direction of increasing thresholds. This instability is now believed to originate from small amounts of impurities in the silane of the boron-doped oxides. In the case of the phosphorus-doped oxides, they are gettered out during the annealing cycle. Consequently, heavier levels of boron would make for less contaminants in the boron-doped silane. This has been ovserved. Recently, units from lot 37C were put on life test. The results appear more promising than the data for lot E-14. The boron-doping level was increased to about 18 ohms/□ (measured on the substrate) to improve stability.

2. TEMPERATURE BIAS STRESS

In order to better characterize the stability of the process, C-V plots were taken on several processed lots after stressing at 300°C for 1 minute at a positive bias of 12 volts. The results, shown superimposed in Figures 80 through 83, confirm the life-test findings of almost zero shift on the n^+ doped polysilicon gates and some negative shift on the p^+ doped gates. Lot 2E obviously had heavy ionic contamination of the gate oxide, since both p^+ and n^+ doped gates show large shifts. Lot E-105, which had lighter boron doping, shows a 6-volt shift on p^+ gates, but only a 0.2-volt shift on n^+ doped gates. This result is typical of contamination by light boron-doped polysilicon gates. Table XXIV shows the shifts in the minimum of the C-V curves after 1 minute at 300°C under +12 volts.

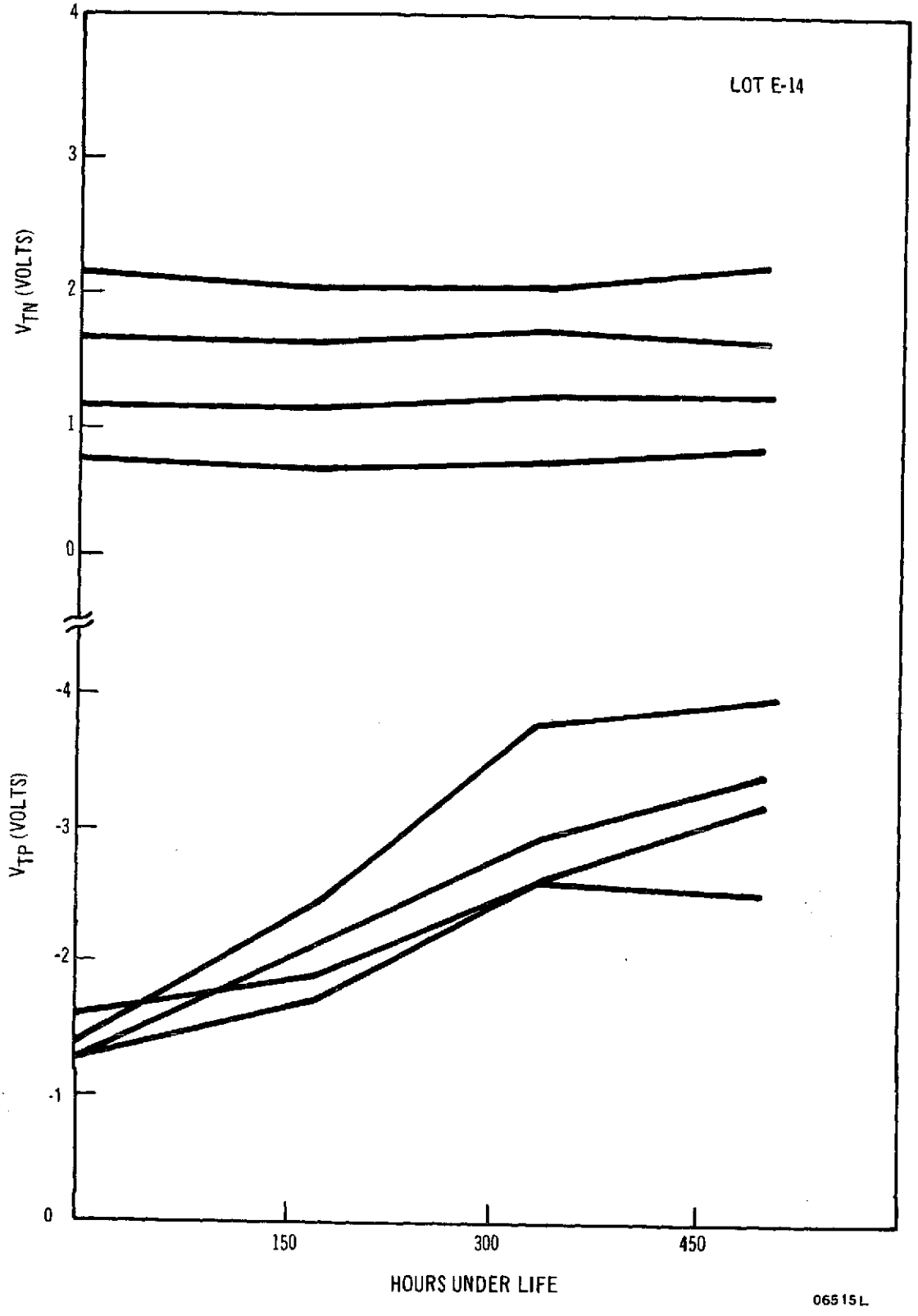

Figure 79. Initial Life Data from TCC-049A Test Transistors

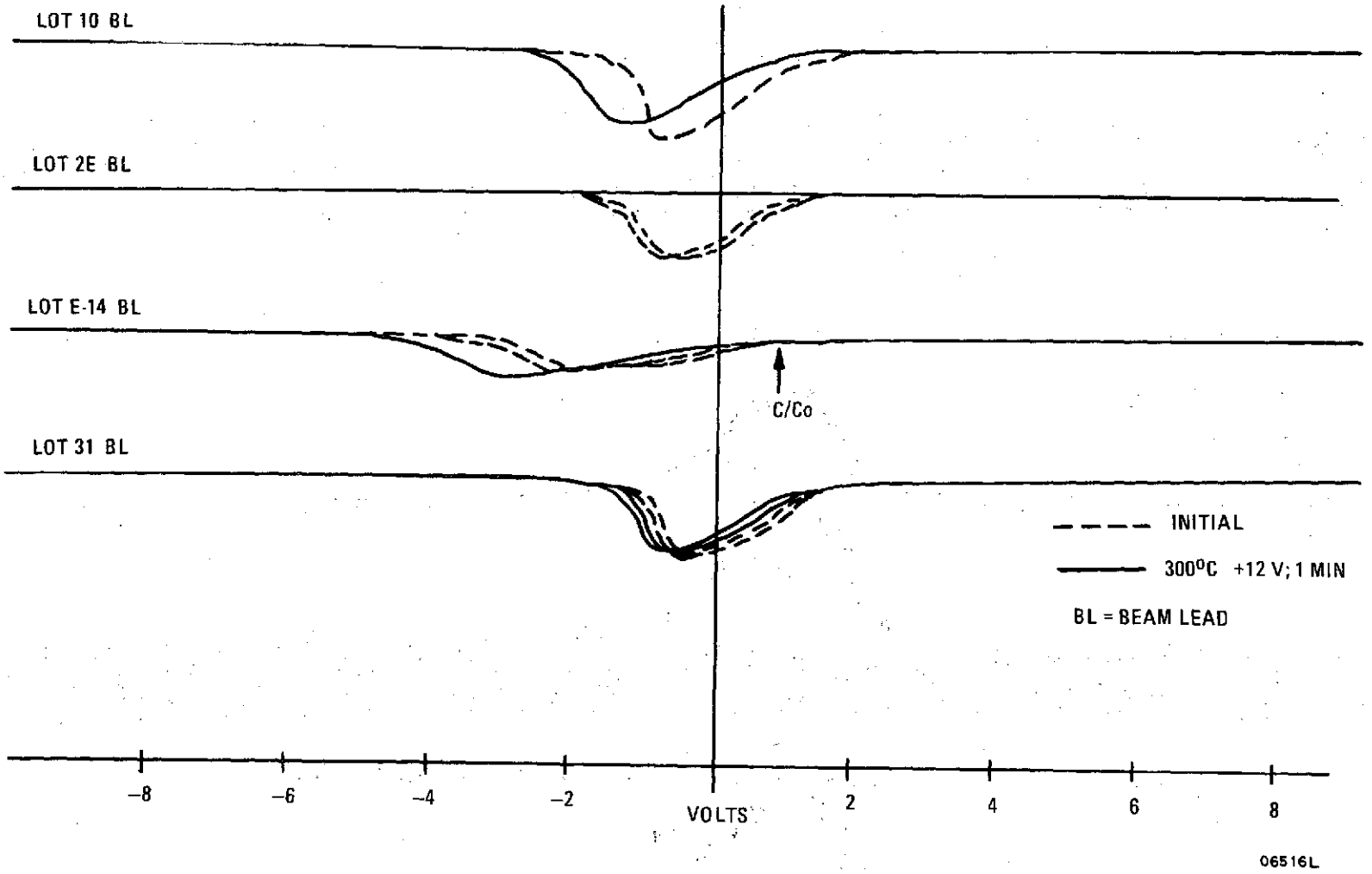

Figure 80. CVBT Curves of p^+ Doped Polysilicon p-MOS Test Transistor Gates

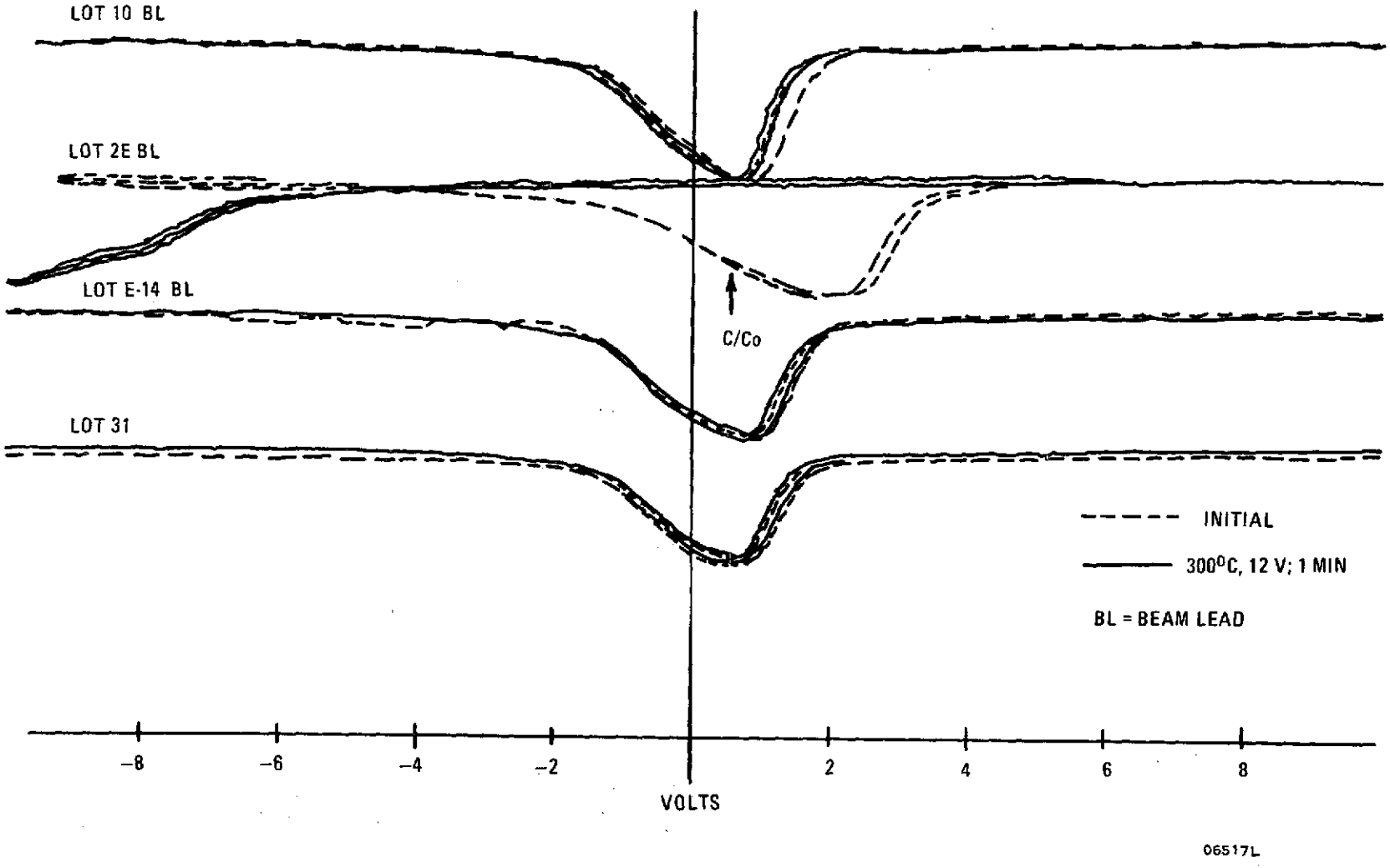

Figure 81. CVBT Curves of n^+ Doped Polysilicon n-MOS Test Transistor Gates

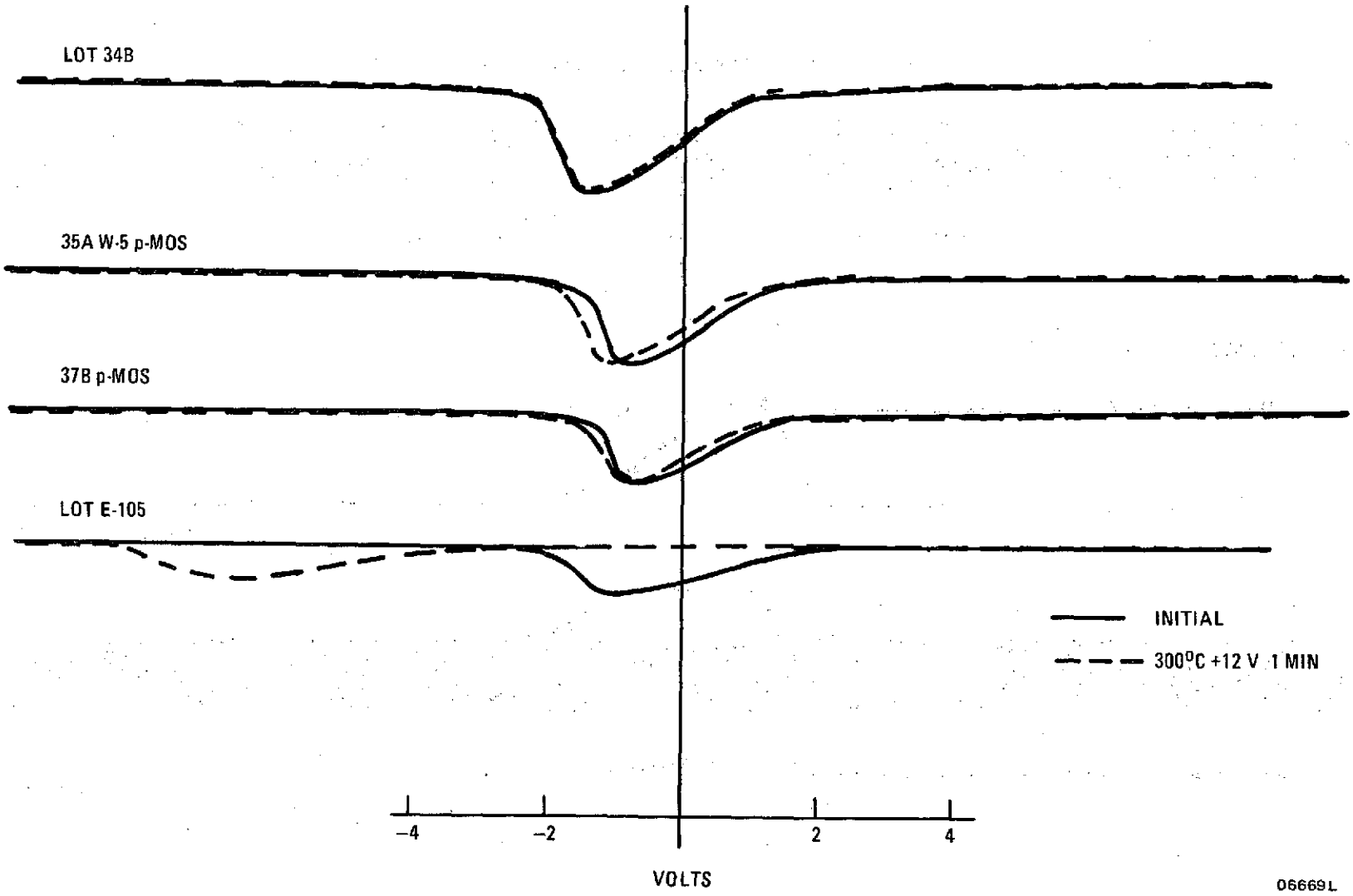

Figure 82. CVBT Curves of p+ Doped Polysilicon p-MOS Test Transistor Gates

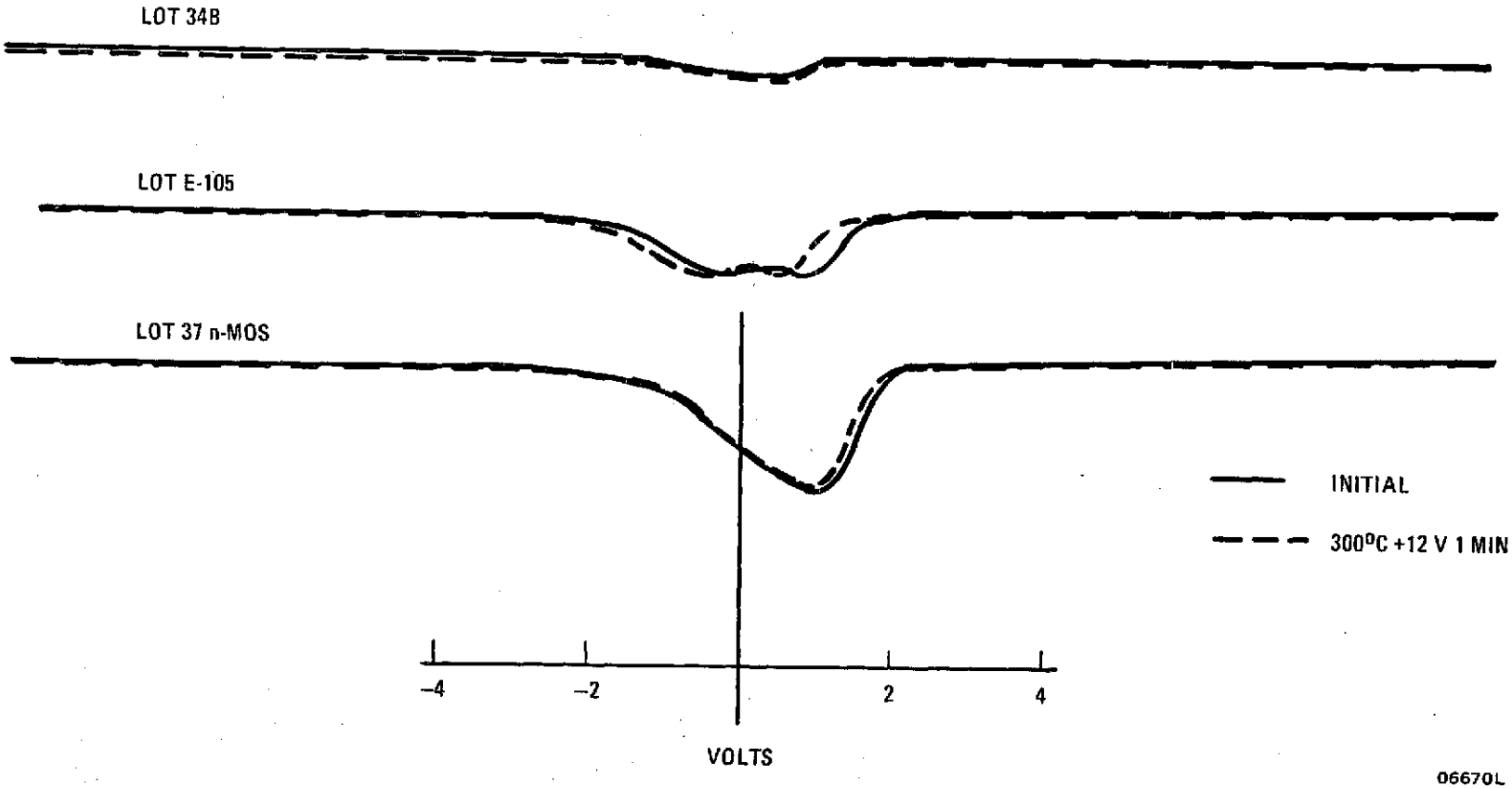

Figure 83. CVBT Curves of n+ Doped Polysilicon n-MOS Test Transistor Gates

TABLE XXIV. TEMPERATURE BIAS STRESS DATA

Lot No.	ΔV_{TN} @ +10V, 300°C (Volts)	ΔV_{TP} @ +10V, 300°C (Volts)	Boron Doping Level
10	0.1	0.6	Heavy
*2E	10	>10	Light
E-14	0.05	1	Light
31	0	0.2	Heavy
E-105	0.3	6V	Light
35A	-	0.3	Heavy
37B	0.05	0.2	Heavy
34B	0	0	Heavy

*Contaminated gate oxide.

G. DELIVERED SAMPLES

On 21 December 1973, 16 samples of the ALU chip were delivered to the contracting agency. The test-transistor data on the chips supplied are shown in Table XXV. One unit was packaged in an 80-lead universal beam-lead package as shown in Figure 84. Drawings of the pin-out data were also supplied as shown in Figure 85.

TABLE XXV. TEST-TRANSISTOR DATA OF DELIVERED TCC-049A SAMPLES FROM LOT 39C

	Gate-Oxide Transistors							Field-Oxide Transistors	
	V_{TO} (V)	BV_{SD} (V)	K-Factor ($\mu A/V^2$)	I_D @ V_{SG} = 10V V_{SD} = 10V (mA)	N_{ss} (cm^{-2})	$N_{p\text{-well}}$ (cm^{-3})	$\rho_{n\text{-substr}}$ (Ohm-cm)	V_{TFO} (V)	N_{ss} (cm^{-2})
n-MOS	2.6	18	51	2.6	2×10^{10}	3.0×10^{16}	-	13.3	3×10^{11}
p-MOS	-0.69	-25	35	-2.3	7×10^{10}	-	3.0	-8.9	6×10^{10}

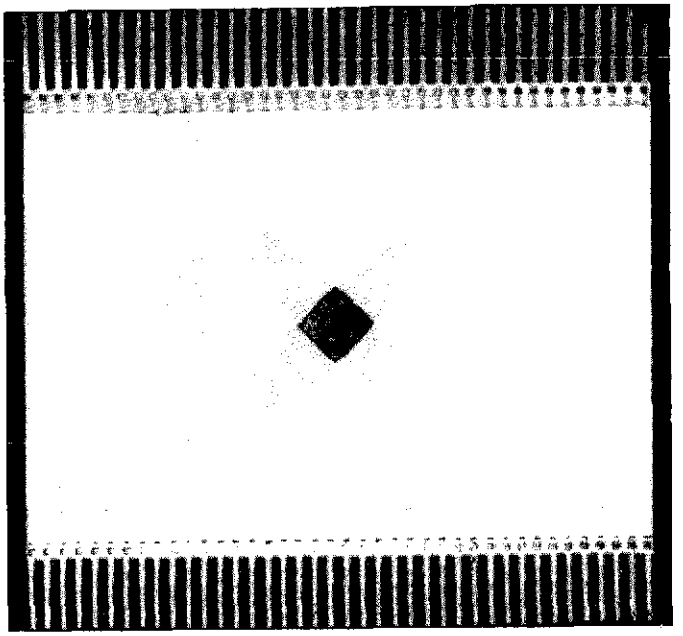

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Figure 84. Packaged TCC-049A Chip

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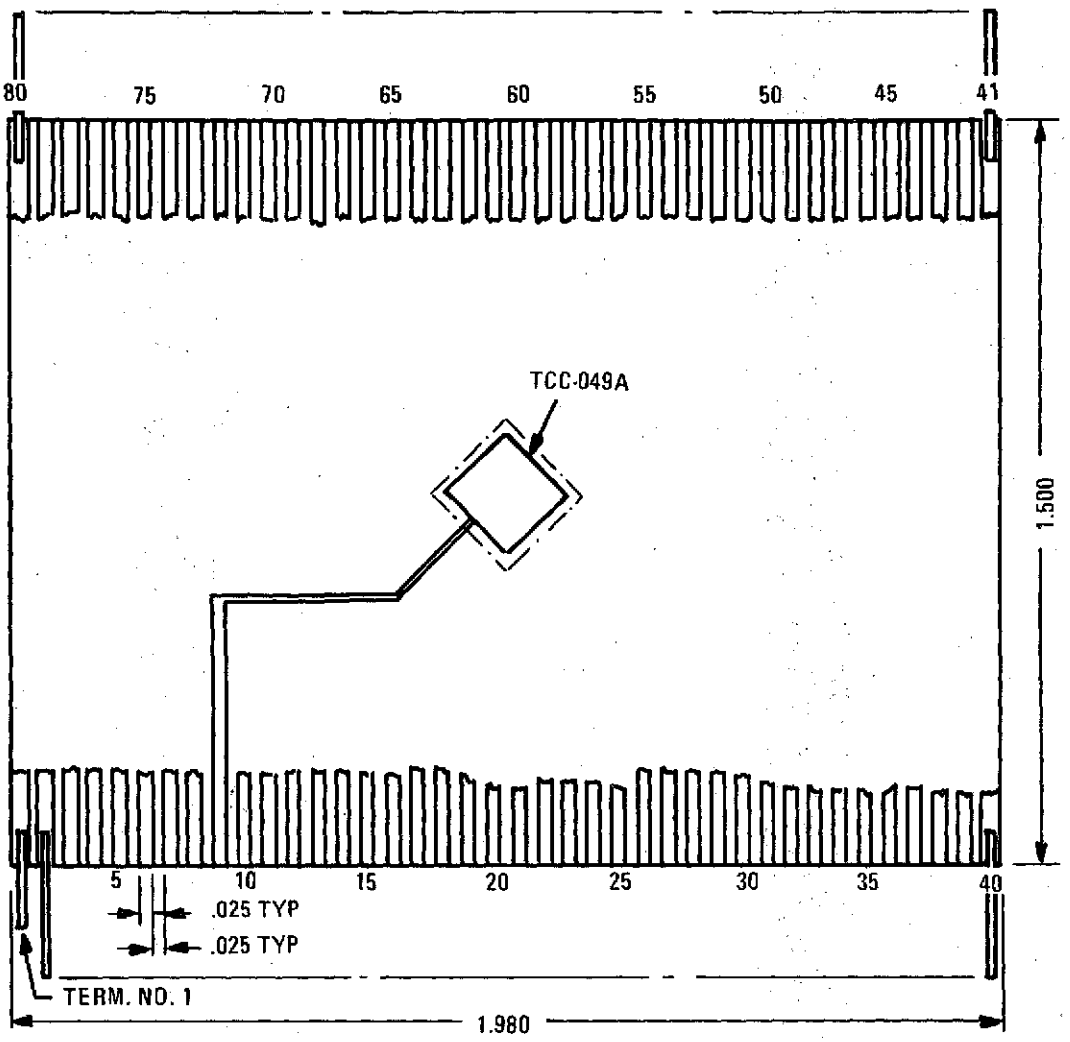

CHIP TO SUBSTRATE INTERCONNECTION								
BEAM NO.	SUBSTRATE TERMINAL	FUNCTION	BEAM NO.	SUBSTRATE TERMINAL	FUNCTION	BEAM NO.	SUBSTRATE TERMINAL	FUNCTION
1	9	MOST POS. VOLT	16	34	SPM (N + 1)	31	65	CTR (N)
2	12	CL2	17	35	$I\phi 1$	32	66	OFLO
3	13	CL1	18	36	SPM (N)	33	67	C (N)
4	14	127	19	45	SLC1	34	68	$\overline{\text{ZRO}}$
5	15	$\overline{\text{SM (N + 1)}}$	20	46	SLC2	35	69	122 GRD
6	16	126	21	47	SPM (N – 1)	36	70	123
7	25	$\overline{\text{SM (N)}}$	22	48	$\overline{\text{OPA (N)}}$	37	71	124
8	26	SLC3	23	49	MOST NEG GRD	38	72	128
9	27	$I\phi 4$	24	52	CL4	39	73	129
10	28	SPM (N + 3)	25	53	$\overline{\text{OPA (N + 1)}}$	40	74	C (N + 4)
11	29	SPM (N + 2)	26	54	$\overline{\text{SM (N + 3)}}$	41	75	$\overline{\text{OPA (N + 3)}}$
12	30	132	27	55	120	42	5	130
13	31	125	28	56	$\overline{\text{SM (N + 2)}}$	43	6	CTR (N + 4)
14	32	$I\phi 3$	29	57	121	44	7	$\overline{\text{OPA (N + 2)}}$
15	33	$I\phi 2$	30	64	131	45	8	C (N + 8)

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Figure 85. Pin-Out Data for the TCC-049A Chip

SECTION IV
CONCLUSIONS

A self-aligned silicon-gate beam-lead process for COS/MOS devices has been developed using deposited doped oxides as diffusion sources. The test vehicle, a four-bit adder, was designed from library cells interconnected by metal and polysilicon to form the desired circuit. These cells have been confirmed as correct, and a library of simple silicon-gate circuits is now in existence together with a set of design rules compatible with the process.

The fabrication process involves a metallization scheme of evaporated Pd-Ti layers instead of the sputtered Pt-Ti system which may cause threshold shifts. Although further refinement is necessary to maintain high yields at low supply leakage, several problems including metal over polysilicon continuity, metal over stepped-oxide continuity, and stability of boron-doped polysilicon gates have been solved. The question of speed has not been fully answered. Because of the integrated-cell library approach, speed depends appreciably on the resistance associated with the polysilicon interconnects. These cannot be reduced below 18 ohms/square. However, the low thresholds and relatively high current output per mil of device width make for a faster circuit.

The two-layer metallization scheme developed on this program has resulted in a 40-percent reduction in chip size compared to the aluminum-gate equivalent.

APPENDIX A

THEORETICAL DISCUSSION OF THE METAL-OXIDE-SILICON SYSTEM

1. ENERGY-BAND STRUCTURE

An important feature of the metal-oxide-silicon (MOS) system is its effect upon the threshold voltage. The Si-SiO_2-Si system can be viewed as a metal-silicon dioxide-silicon system whose metal has been replaced by silicon. Accordingly, a change in the work function difference would be expected because of the dissimilarities between the metal and the silicon.

The energy-band diagram of the general metal-insulator-semiconductor is shown in Figure A-1[1,2]. The semiconductor is p-type and the gate voltage is zero in this MIS system. The surface states and the oxide charges are assumed to be zero.

The work function of a material represents the energy required to move an electron from the Fermi level, in a given material, to a given reference level. In a system at equilibrium, i.e., no net transfer of energy, the Fermi level of the metal and the semiconductor must be level or constant throughout the energy band.

According to convention, the potentials are considered positive in the negative R direction. In addition, energy is expressed in electron volts and

1. S.M. Sze, Physics of Semiconductor Devices, Wiley-Interscience, 1969.

2. A.S. Grove, Physics and Technology of Semiconductor Series, Wiley, New York, 1967.

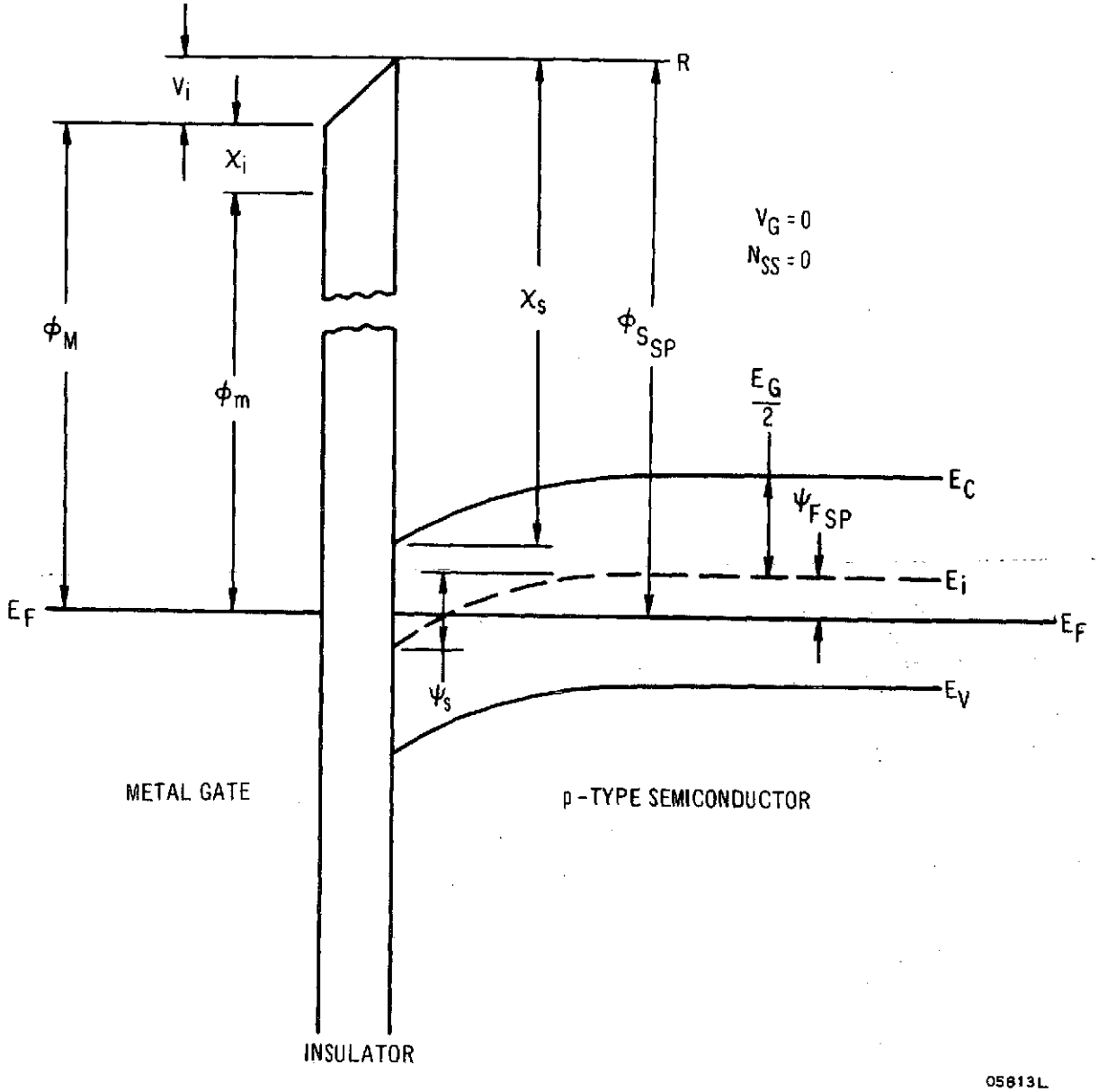

Figure A-1. Energy Band Diagram for the Metal Gate-Insulator – p-Type Semiconductor Substrate

potential in volts. Let R* be the reference level of a free electron, then the potentials from the Fermi level to line R for the metal and that of the semiconductor can be equated as

$$V_i + \chi_i + \phi_m = \chi_s + \frac{E_G}{2} - \psi_s + \psi_{F_{SP}} \quad \ldots\ldots\ldots\ldots\ldots \quad (1)$$

By definition

$$\phi_{MS} = \phi_M - \phi_S \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (2)$$

or, for a p-type semiconductor substrate

$$\phi_{MS_{SP}} = \phi_M - \phi_{S_{SP}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (3)$$

then, $\phi_{MS_{SP}}$ can be represented as

$$\phi_{MS_{SP}} = \chi_i + \phi_m - (\chi_S + \frac{E_G}{2} + \psi_{F_{SP}}) = - (V_i + \psi_S) \quad \ldots\ldots\ldots \quad (4)$$

Replacing the metal gate in Figure A-1 with an n-type semiconductor gate, we have represented in Figure A-2 the energy-band diagram of an n-type semiconductor gate-insulator-p-type-semiconductor substrate. If we assume that the band-gap theory is still applicable, we have, similar to Eq. (1)

$$V_i + \chi_s + \frac{E_G}{2} - \psi_{F_{GN}} = \chi_s + \frac{E_G}{2} - \psi_S + \psi_{F_{SP}} \quad \ldots\ldots\ldots\ldots \quad (5)$$

By definition

$$\phi_{S_{GN}S_{SP}} = \phi_{S_{GN}} - \phi_{S_{SP}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (6)$$

then, by Eq. (5), (6), and Figure A-2 (cancelling like terms and rearrangement) we have

*See Notation.

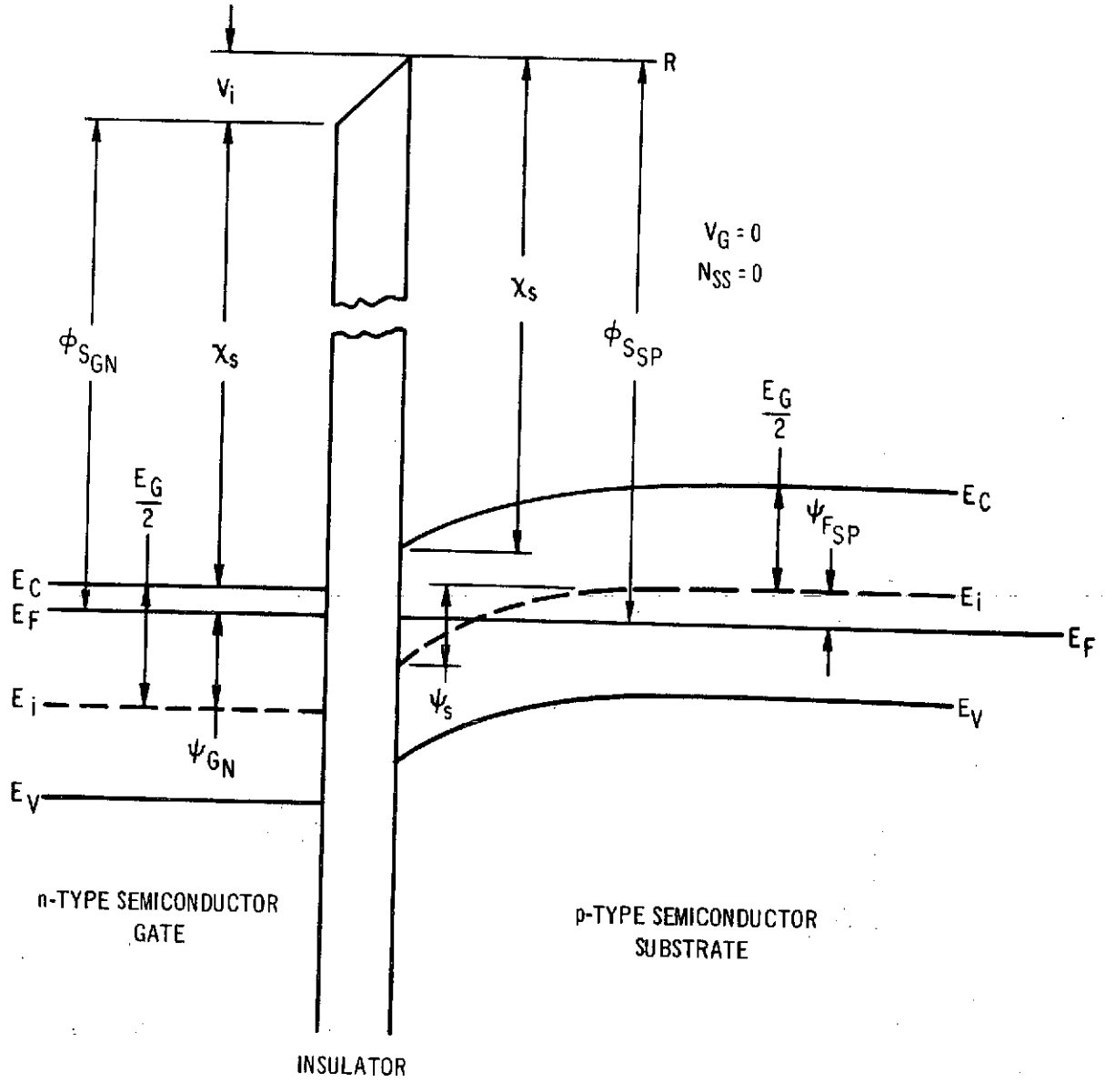

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Figure A-2. Energy Band Diagram for the n-Type Semiconductor Gate-Insulator – p-Type Semiconductor Substrate

$$\phi_{S_{GN}S_{SP}} = - \Psi_{F_{GN}} - \Psi_{F_{SP}} = - (V_i + \Psi_S) \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad (7)$$

or

$$\phi_{S_{GN}S_{SP}} = - (\Psi_{F_{GN}} + \Psi_{F_{SP}}) \quad . \quad (8)$$

For the case where the silicon gate is p-type and the silicon substrate is also p-type we find, utilizing the procedure outlined above, that

$$\phi_{S_{GP}S_{SP}} = \Psi_{F_{GP}} - \Psi_{F_{SP}} \quad . \quad (9)$$

Three conditions may exist:

a. The doping level of the gate is greater than that of the substrate since

$$\Psi_{F_{GP}} > \Psi_{F_{SP}} \quad . \quad (10)$$

then,

$$\phi_{S_{GP}S_{SP}} = \Psi_{F_{GP}} - \Psi_{F_{SP}} > 0 \quad . \quad (11)$$

b. The doping level of the gate is equal to that of the substrate since

$$\Psi_{F_{GP}} = \Psi_{F_{SP}} \quad . \quad (12)$$

then,

$$\phi_{S_{GP}S_{SP}} = \Psi_{F_{GP}} - \Psi_{F_{SP}} = 0 \quad . \quad (13)$$

c. The doping level of the gate is less than that of the substrate since

$$\Psi_{F_{GP}} < \Psi_{F_{SP}} \quad . \quad (14)$$

then,

$$\phi_{S_{GP}S_{SP}} = \Psi_{F_{GP}} - \Psi_{F_{SP}} < 0 \quad . \quad (15)$$

Replacing the metal gate in Figure A-3 with a p-type semiconductor gate, we have, as represented in Figure A-4, similar to Eq. (5)

$$\chi_s + \frac{E_G}{2} + \Psi_{F_{GP}} = V_i + \chi_S + \frac{E_G}{2} + \Psi_S - \Psi_{F_{SN}} \quad \ldots\ldots\ldots\ldots (16)$$

By definition

$$\phi_{S_{GP}S_{SN}} = \Psi_{F_{GP}} + \Psi_{F_{SN}} = (V_i + \Psi_S) \quad \ldots\ldots\ldots\ldots\ldots\ldots (17)$$

or

$$\phi_{S_{GP}S_{SN}} = \Psi_{F_{GP}} + \Psi_{F_{SN}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (18)$$

For the case where the silicon gate is n-type and the silicon substrate is also n-type, we find, utilizing the procedure outlined above, that

$$\phi_{S_{GN}S_{SN}} = - \Psi_{F_{GN}} + \Psi_{F_{SN}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (19)$$

Three conditions can then exist:

a. The doping level of the gate is greater than that of the substrate since

$$\Psi_{F_{GN}} > \Psi_{F_{SN}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (20)$$

then,

$$\phi_{S_{GN}S_{SN}} = - \Psi_{F_{GN}} + \Psi_{F_{SN}} < 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (21)$$

b. The doping level of the gate is equal to that of the substrate since

$$\Psi_{F_{GN}} = \Psi_{F_{SN}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (22)$$

then,

$$\phi_{S_{GN}S_{SN}} = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (23)$$

c. The doping level of the gate is less than that of the substrate since

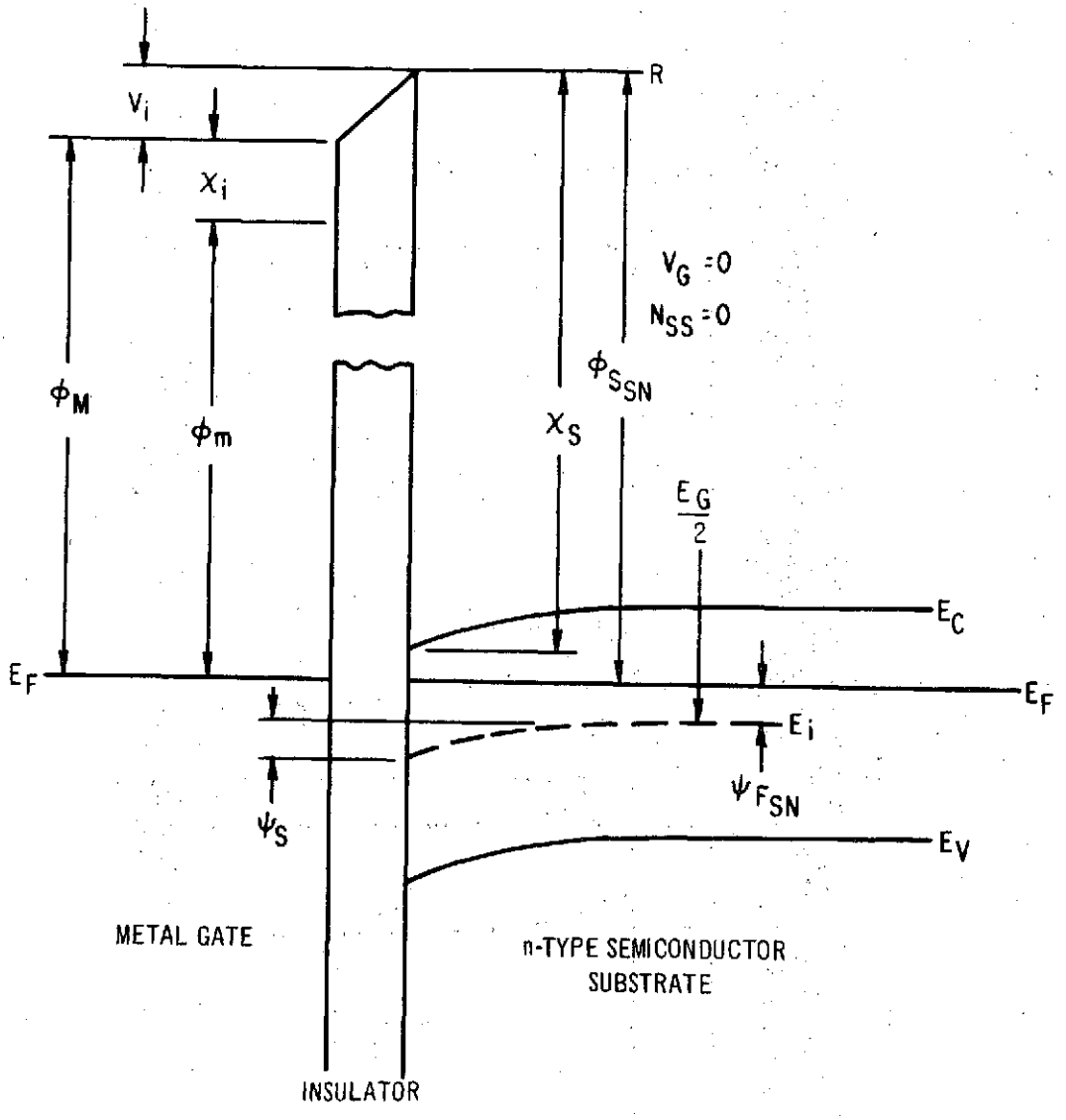

Figure A-3. Energy Band Diagram for the Metal Gate-Insulator – n-Type Semiconductor Substrate

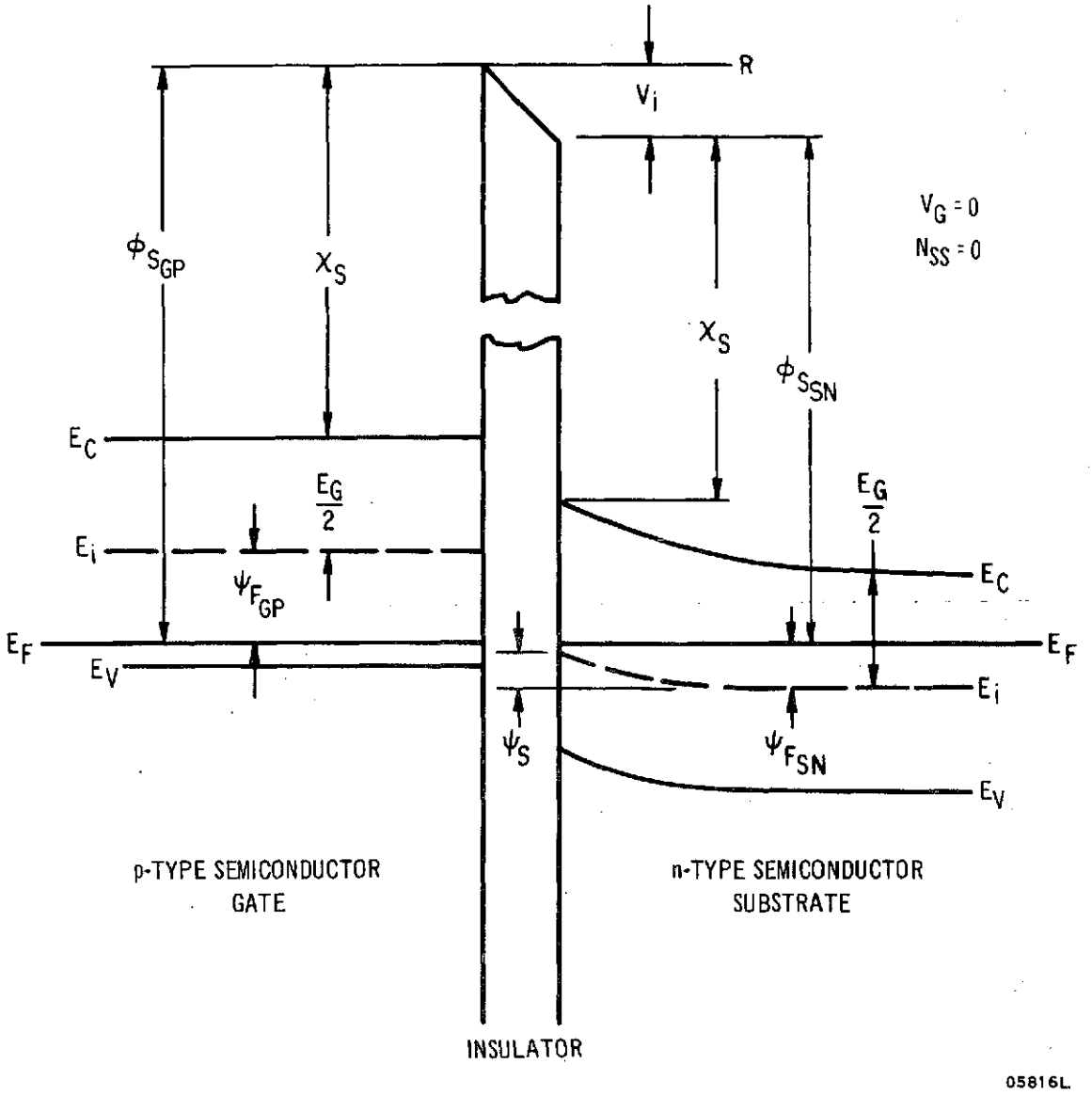

Figure A-4. Energy Band Diagram for the p-Type Semiconductor Gate-Insulator – n-Type Semiconductor Substrate

$$\Psi_{F_{GN}} < \Psi_{F_{SN}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (24)$$

then,

$$\phi_{S_{GN}S_{SN}} = - \Psi_{F_{GN}} + \Psi_{F_{SN}} > 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (25)$$

2. THRESHOLD VOLTAGE

In paragraph 1, the work function were derived for the four possible conditions of gate and substrate doping types. If we assume that the energy-band theory continues to apply for a silicon-gate structure, then the threshold voltage at $I_D = 0$ can be defined as[2]

$$V_T = \phi_{SS} \pm \frac{t_{ox}}{\epsilon_{ox}} \sqrt{4q\ \epsilon_S\ N_S\ \Psi_F} \pm \Psi_S - qN_{SS}\ \frac{t_{ox}}{\epsilon_{ox}} \quad \ldots\ldots\ldots\ldots \quad (26)$$

where ϕ_{SS}, depending on the conditions, is described by Eq. (8, 9, 18, or 19) and Ψ_F, the generalized $\Psi_{F_{GP}}$, $\Psi_{F_{GN}}$, $\Psi_{F_{SP}}$, $\Psi_{F_{SN}}$,

by

$$\Psi_F = \frac{KT}{q} \ln \frac{N + N_i}{N_i} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (27)$$

and, if $V_G = 0$,

$$\Psi_S = \pm \frac{2KT}{q} \ln \frac{N + N_i}{N_i} = \pm\ 2\ \Psi_F \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (28)$$

Because the silicon-gate layer can serve as an additional interconnection plane, its resistance is made as low as possible. If we assume that the impurity concentration of either the p- or n-doped silicon gates is greater than 3×10^{19}, the Fermi potential would then be greater than half the band gap of silicon, i.e., 0.55 eV. In this case, $\Psi_{F_{GN}}$ or $\Psi_{F_{GP}}$ would be equal to 0.55 eV.

Let us consider four combinations of silicon gate-silicon dioxide-silicon structure and assume the following for all cases:

substrate orientation <100>

oxide charge = 0

$V_G = 0$ and $\phi_S = 2\Psi_F$

$t_{ox} = 0.10$ micrometer

$N_{SS} = 5.00 \times 10^{10}$ cm^{-2}

$\epsilon_{ox} = 3.40 \times 10^{-13}$ F/cm

$\epsilon_{Si} = 1.04 \times 10^{-12}$ F/cm

$T = 298.1^{o}K$

$q = 1.60 \times 10^{-19}$ coulombs

$\Psi_{F_{GN}} = \Psi_{F_{GP}} = 0.55$ eV

CASE I: AN N-TYPE SILICON GATE AND A P-TYPE SUBSTRATE

Given:

$N_{SP} = 1.00 \times 10^{16}$ cm^{-3}

$N_{GN} = 3.00 \times 10^{19}$ cm^{-3}

From Eq. (27)

$$\phi_{F_{SP}} = 0.35$$

from Eq. (8)

$$\phi_{S_{GN}S_{SP}} = -(\Psi_{F_{GN}} - \Psi_{F_{SP}}) = -0.20$$

and Eq. (26) for V_T

$$V_{T_{NN}} = -\phi_{S_{GN}S_{SP}} + \frac{t_{ox}}{\epsilon_{ox}}\sqrt{4q\,E_S\,N_S\,\Psi_F} + 2\Psi_F - qN_{SS}\frac{t_{ox}}{\epsilon_{ox}}$$

$$V_{T_{NN}} = 1.00 \text{ volt}$$

CASE 2: A P-TYPE SILICON GATE AND A P-TYPE SUBSTRATE

$$N_{SP} = 6.80 \times 10^{15} \text{ cm}^{-3}$$

$$N_{GP} = 3.00 \times 10^{14} \text{ cm}^{-3}$$

Substituting the given values in Eq. (11) and the results and the assumed values in Eq. (26), we get

$$V_{T_{NP}} = 2.00 \text{ volts}$$

Comparing the results of Case 1 and Case 2, note that by changing the gate type from n to p, the threshold voltage is increased by 1 volt.

CASE 3: A P-TYPE SILICON GATE AND AN N-TYPE SUBSTRATE

$$N_{SN} = 5.00 \times 10^{15} \ (\text{cm}^{-3})$$

$$N_{GP} = 3.00 \times 10^{19} \ (\text{cm}^{-3})$$

From Eq. (27)

$$\Psi_{F_{SN}} = 0.33$$

from Eq. (18)

$$\phi_{S_{GP}S_{SN}} = 0.88$$

and Eq. (26) for $V_{T_{PP}}$

$$V_{T_{PP}} = \phi_{S_{GP}S_{SN}} - \frac{t_{ox}}{\epsilon_{ox}} \sqrt{4q \ \epsilon_S \ N_S \ \Psi_F} - 2\Psi_F - q \ N_{ss} \frac{t_{ox}}{\epsilon_{ox}}$$

$$V_{T_{PP}} = -1.01 \text{ volts}$$

CASE 4: AN N-TYPE SILICON GATE AND AN N-TYPE SUBSTRATE

$$N_{SN} = 2.50 \times 10^{15} \ (\text{cm}^{-3})$$

$$N_{GN} = 3.00 \times 10^{19} \ (\text{cm}^{-3})$$

Substituting the given values in Eq. (21) and the results and the assumed values in Eq. (26), we get

$$V_{T_{PN}} = -2.01 \text{ volts}$$

As in Case 1 and Case 2, the results for Case 3 and Case 4 show that by changing the gate type from p to n, the threshold voltage in increased by 1 volt.

In general, low thresholds are desired so as to achieve faster devices and lower supply voltages. Although it is possible to dope the silicon gates either n- or p-types, it can be seen from the four cases described that the lowest V_T value for n-MOS is $V_{T_{NN}}$ and for p-MOS $V_{T_{PP}}$. The $V_{T_{NN}}$ and $V_{T_{PP}}$ thresholds can be further reduced by lowering the doping level of the gate. However, this is process limited.

Table A-1 lists $V_{T_{NN}}$ and $V_{T_{PP}}$ as a function of the surface-impurity concentration under the gate dielectric and the number of surface states. The conditions are the same as for the above cases.

TABLE A-1. THRESHOLDS FOR n-GATE n-MOS AND p-GATE p-MOS AT ROOM TEMPERATURE

N_{SP} or N_{SN} (cm^{-3})	$V_{T_{NN}}$ (Volts)		$V_{T_{PP}}$ (Volts)	
	$N_{SS} = 5 \times 10^{10}$	1×10^{11}	$N_{SS} = 5 \times 10^{10}$	1×10^{11}
5.00×10^{16}	3.01	2.78	-3.49	-3.72
4.00×10^{16}	2.62	2.39	-3.10	-3.34
3.00×10^{16}	2.19	1.95	-2.66	-2.90
2.00×10^{16}	1.67	1.43	-2.14	-2.38
1.00×10^{16}	1.00	0.77	-1.48	-1.71
9.00×10^{15}	0.92	0.68	-1.40	-1.63
8.00×10^{15}	0.83	0.60	-1.31	-1.55
7.00×10^{15}	0.74	0.51	-1.22	-1.45
6.00×10^{15}	0.64	0.41	-1.12	-1.35
5.00×10^{15}	0.54	0.30	-1.01	-1.24
4.00×10^{15}	0.42	0.18	-0.89	-1.13
3.00×10^{15}	0.28	0.05	-0.76	-1.00
2.00×10^{15}	0.13	-0.11*	-0.60	-0.84
1.00×10^{15}	0.08	-0.32*	-0.39	-0.63

*Depletion mode operation.

NOTATION

Symbol	Definition
E_c	Energy of an electron at the conduction-band edge
E_F	Energy of an electron at the Fermi level
E_G	Energy of the band gap
E_i	Energy of an electron at the intrinsic Fermi level
E_v	Energy of an electron at the valence-band edge
N_i	Concentration of ionized intrinsic carriers
N	Concentration of ionized impurities
N_{SP}	Concentration of ionized p-type impurities in the channel
N_{SN}	Concentration of ionized n-type impurities in the channel
N_{ss}	Density of surface states
q	Magnitude of an electron charge
Q_{ss}	Charge density of surface state
R	Reference energy level of a free electron
t_{ox}	Thickness of the silicon dioxide gate insulator
T	Temperature
V_G	Voltage applied to the gate
V_i	Potential drop across the insulator
V_T	Threshold voltage at $I_D = 0$
$V_{T_{PP}}$	Threshold voltage of a PMOS transistor with a p-type silicon gate at $I_D = 0$

Symbol	Definition
$V_{T_{PN}}$	Threshold voltage of a p-MOS transistor with an n-type silicon gate at $I_D = 0$
$V_{T_{NP}}$	Threshold voltage of an n-MOS transistor with a p-type silicon gate at $I_D = 0$
$V_{T_{NN}}$	Threshold voltage of an n-MOS transistor with an n-type silicon gate at $I_D = 0$
ϵ_{ox}	Permittivity of the silicon dioxide gate insulator
ϵ_{Si}	Permittivity of silicon
ϕ_m	Potential barrier between the metal and insulator
ϕ_M	Work function of the metal
ϕ_{MS}	Work function difference between the metal and semiconductor
$\phi_{S_{GP}}$	Work function of a p-type semiconductor gate
$\phi_{S_{GN}}$	Work function of an n-type semiconductor gate
$\phi_{S_{SP}}$	Work function of a p-type semiconductor substrate
$\phi_{S_{SN}}$	Work function of an n-type semiconductor substrate
ϕ_{SS}	Work function difference between a semiconductor gate and a semiconductor substrate
$\phi_{S_{GP}S_{SP}}$	Work function difference between a p-type semiconductor gate and a p-type semiconductor substrate
$\phi_{S_{GN}S_{SP}}$	Work function difference between an n-type semiconductor gate and a p-type semiconductor substrate
$\phi_{S_{GP}S_{SN}}$	Work function difference between a p-type semiconductor gate and an n-type substrate
$\phi_{S_{GN}S_{SN}}$	Work function difference between an n-type semiconductor gate and an n-type substrate

NOTATION (Cont.)

Symbol	Definition
χ_i	Electron affinity of an insulator
χ_s	Electron affinity of a semiconductor
Ψ_F	Potential of the Fermi level
$\Psi_{F_{GP}}$	Potential of the Fermi level of a p-type semiconductor gate
$\Psi_{F_{GN}}$	Potential of the Fermi level of an n-type semiconductor gate
$\Psi_{F_{SP}}$	Potential of the Fermi level of a p-type semiconductor substrate
$\Psi_{F_{SN}}$	Potential of the Fermi level of an n-type semiconductor substrate
Ψ_S	Potential of the surface relative to the bulk

APPENDIX B

STATISTICAL CHARACTERIZATION TECHNIQUE

A statistical evaluation technique has been established that utilizes measurements made on MOS transistors by computer-controlled test equipment to provide a basis for in-process control. Devices are characterized in a single test setup. The test matrix has a maximum array size of 9 by 9 by 8 sets of drain currents, gate/drain voltages, and substrate bias voltages. Test values have been selected statistically: the drain current values are 1, 16, 49, 100, 169, 256, 361, 484, and 625 microamperes; and the substrate bias voltages are 0, 0.4, 1.0, 1.8, 3.0, 5.0, 8.0, and 12.0 volts.

A least-square fit of the data gives the (extrapolated) threshold voltage (V_t), the K-factor ($= \frac{C_{ox}\mu W}{2\ell}$), and a correlation coefficient - all as functions of the substrate bias voltage. The correlation coefficient is a measure of how well the measured I_d versus V_g characteristic follows the theoretical straight line relationship. In our case the agreement is so good that we use the deviation from the ideal factor (unity) for perfect fit and multiply it by a factor of 10^6. Therefore, a correlation coefficient of 0.999952 corresponds to 48 ppm.

A second least-square fit of the threshold voltage, V_t, with substrate bias has the channel concentration as its only unknown parameter and, therefore, the channel concentration can be obtained from this fit.

Excellent agreement is obtained both for n-MOS and p-MOS transistors when the channel concentration thus determined is inserted into the formulas for threshold voltage and I_d-V_d characteristics.

Test jigs are set up to permit 300°C bias - stress testing on MOS transistors in wafer form. Shifts are readily detected because the threshold voltage has millivolt resolution. The absolute value of the threshold voltage is compared with the theory. All deviations (usually very small for clean SiO_2 layers) can be explained by surface states usually in the low 10^{10} per-square-centimeter range. Interface charges in the Al_2O_3/SiO_2 interface usually lower the p-threshold voltages and increase the n-threshold voltages. They all can be reflected as effective surface-state concentrations in the SiO_2/Si interface and lower work function.

1. THRESHOLD AND K-FACTOR

The threshold voltage is usually expressed as

$$V_t = \frac{qN_{ss}}{C_{ox}} \pm \frac{\sqrt{2q\varepsilon_o \varepsilon_{Si} N}}{C_{ox}} \sqrt{|2V_f| + |V_{sub}|} \pm V_f + \phi_{MS} \quad \ldots\ldots \quad (1)$$

use + sign for n-MOS

use - sign for p-MOS

where N_{ss} is the interface state density (per square centimeter) and ϕ_{MS} is the metal-semiconductor work function. Inversion is assumed to have occurred when the surface voltage reaches two Fermi levels.

Basically the simplest formula for MOS transistors is

$$I_d = K\,[(V_g - V_t)^2 - (V_g - V_t - V_d)^2] \quad \text{for } V_d < V_g - V_t \quad \ldots\ldots \quad (2)$$

$$I_d = K\,(V_g - V_t)^2 \quad \text{for } V_d > V_g - V_t \quad \ldots\ldots \quad (3)$$

where $K\ (= \frac{C_{ox}\,\mu W}{2\,\ell})$ is called the K-factor, C_{ox} is the gate oxide capacitance per unit area, μ is the channel mobility, W is the channel width (in the direction of current flow) and ℓ is the channel length.

These formulas describe the $I_d - V_d$ characteristics reasonably well for low gate bias and zero substrate bias.

If the gate of the transistor is connected to its drain, then

$$V_d = V_g \text{ thus,}$$

$$V_d > V_g - V_t$$

and Eq. (3) can be used to characterize the transistor's behavior. This equation can be rewritten as:

$$V_g = V_t + \sqrt{\frac{I_d}{K}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (4)$$

and can be plotted as a straight line, with the threshold voltage being the intercept and $\frac{1}{\sqrt{K}}$ the slope. In order to determine the threshold voltage, a least-square fit is used to relate the measured data points to the predicted curve, Eq. (4).

For a least-square fit of Eq. (4) the following parameters have to be accumulated (n = 9):

$$\sum_{i=1}^{n} \sqrt{I_{di}}; \quad \sum_{i=1}^{n} V_{gi}; \quad \sum_{i=1}^{n} I_{di}; \quad \sum_{i=1}^{n} V_{gi}^2; \quad \sum_{i=1}^{n} \sqrt{I_{di}} \cdot V_{gi}$$

The average values are

$$\overline{\sqrt{I_d}} = \frac{1}{n} \sum_{i=1}^{n} \sqrt{I_{di}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (5)$$

$$\overline{V_g} = \frac{1}{n} \sum_{i=1}^{n} V_{gi} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (6)$$

Eq. (4) also holds for the averages:

$$V_t = \overline{V}_g - \left(\frac{1}{\sqrt{K}}\right) \overline{\sqrt{I_d}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (7)$$

$$\frac{1}{\sqrt{K}} = \frac{\sum_{i=1}^{n} \left(\sqrt{I_{di}} - \overline{\sqrt{I_d}}\right) (V_{gi} - \overline{V}_g)}{\sum_{i=1}^{n} 1 \left(\sqrt{I_{di}} - \overline{\sqrt{I_d}}\right)^2} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (8)$$

Equation (8) may be rewritten as:

$$K = \left\{ \frac{n\sum_{i=1}^{n} I_{di} - \left(\sum_{i=1}^{n} \sqrt{I_{di}}\right)^2}{n\sum_{i=1}^{n}\left(\sqrt{I_{di}}\, V_{gi}\right) - \sum_{i=1}^{n} \sqrt{I_{di}} \sum_{i=1}^{n} V_{gi}} \right\}^2 \quad \ldots\ldots\ldots \quad (9)$$

To measure how well a curve fitting is done, a correlation coefficient R is usually defined:

$$R = \frac{\sum_{i=1}^{n} \left(\sqrt{I_{di}} - \overline{\sqrt{I_d}}\right)(V_{gi} - \overline{V}_g)}{\sqrt{\sum_{i=1}^{n} (I_{di} - \overline{I}_d) \sum_{i=1}^{n} (V_{gi} - \overline{V}_g)^2}} \quad \ldots\ldots\ldots\ldots\ldots (10)$$

$$= \frac{n\sum_{i=1}^{n}(\sqrt{I_{di}}\, V_{gi}) - (\sum_{i=1}^{n} \sqrt{I_{di}})(\sum_{i=1}^{n} V_{gi})}{\sqrt{\left[n\sum_{i=1}^{n} I_{di} - (\sum_{i=1}^{n} \sqrt{I_{di}})^2\right]\left[n\sum_{i=1}^{n} (V_{gi})^2 - (\sum_{i=1}^{n} V_{gi})^2\right]}}$$

A perfect fit would have a correlation factor of +1.00 or -1.00 depending on the slope of the curve. Well designed and processed devices usually have a correlation coefficient of better than 0.9996. Therefore, it is better to use 1-R and express it in parts per million (ppm). A value of R = 0.9996 would be 400 ppm.

2. CHANNEL CONCENTRATION

In order to determine the surface concentration of the substrate and/or well, Eq. (1), which defines threshold voltage, is used. This equation can be rewritten as:

$$V_t = \text{constant} \pm c \left[|2V_f| + |V_{sub}|\right]^{1/2} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (11)$$

where

$$c = \frac{1}{C_{ox}} \left(2q\varepsilon_o\, \varepsilon_{si}\, N\right)^{1/2}$$

Equation (11) can be used to solve for channel concentration if V_t is measured as a function of substrate or well bias. For better accuracy this should be done for extreme values of substrate voltage, $V_{sub1} \tilde{\approx} 0$ and V_{sub2}.

$$V_1 = V_o + c\sqrt{V_{sub1} + 2V_f} \tilde{\approx} V_o + c\sqrt{2V_f} \quad \ldots\ldots\ldots\ldots \quad (12a)$$

$$V_2 = V_o + c\sqrt{V_{sub2} + 2V_f} \tilde{\approx} V_o + c\sqrt{V_{sub2}} \quad \ldots\ldots\ldots\ldots \quad (12b)$$

By subtraction V_o can be eliminated and the resulting equation can be solved for N:

$$N = \frac{C_{ox}^2 (V_2 - V_1)^2}{2q\varepsilon_o \varepsilon_{si}\left[\sqrt{V_{sub2} + 2V_f} - \sqrt{V_{sub1} + 2V_f}\right]^2} \quad \ldots\ldots\ldots \quad (13)$$

Equation (13) works very well for n-MOS transistors where the substrate or well concentration is in the order of 8×10^{15} to 3×10^{16} cm^{-3}. Then V_2 may be 6 to 10 times larger than V_1.

For p-MOS transistors, this is generally not the case and rather large inaccuracies result. It is better to determine the substrate concentration by a least-square fit of the measured threshold voltage, V_t, as a function of substrate bias to Eq. (11). As was the case for Eq. (4), V_t itself is found by a least-square fit of $\sqrt{I_d}$ vs V_g. If n sets of data V_{ti} (V_{sub}) and V_{subi} are used, then

$$N = \frac{C_{ox}^2}{2q\varepsilon_o\varepsilon_{Si}}\left\{\frac{n\sum_{i=i}^{n}\left[\sqrt{V_{subi} + 2V_f}\; V_{ti}(V_{sub})\right]}{n\sum_{i=i}^{n}(V_{subi} + 2V_f)\left[\sum_{i=i}^{n}\sqrt{V_{subi} + 2V_f}\right]^2} - \frac{\left[n\sum_{i=i}^{n}\sqrt{V_{subi} + 2V_f}\;\sum_{i=i}^{n} V_{ti}(V_{sub})\right]}{n\sum_{i=i}^{n}(V_{subi} + 2V_f)\left[\sum_{i=i}^{n}\sqrt{V_{subi} + 2V_f}\right]^2}\right\}^2 \quad \ldots\ldots\ldots \quad (14)$$

In our case there is a complication since N occurs on both sides of Eq. (7) through

$$V_f = \frac{kT}{q} \ln \left[(N + n_i)/n_i\right] \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (15)$$

and

$$n_i^2 = 1.5 \times 10^{33} T^3 \exp. \left(- \frac{1.21eV}{kT}\right) \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (16)$$

where k is Boltzmann's constant.

The approach taken is to solve Eq. (14) with an approximate value for V_f, then calculate V_f from Eq. (15), use this better value in Eq. (14) and iterate this procedure until the new V_f differs less than 0.1 millivolt from the previously calculated V_f.

3. PARAMETER CHOICE

As noted above, the drain currents have the values 1, 16, 49, 100, 169, 256, 361, 484, and 625 microamperes. These values guarantee statistically equal weight on the $\sqrt{I_d}$ $-V_g$ curves. The substrate bias values have been selected as 0, 0.4, 1.0, 1.8, 3.0, 5.0, 8.0 and 12.0 volts. This selection gives roughly equal statistical weight.

4. SIZE OF THE STATISTICAL BLOCK

The size of the statistical block depends upon the accuracy of the input data. The correlation coefficients as defined in Eq. (13) give a quantitative measure of how well the data points follow a linear I_d versus V_g relationship.

The matrix size used most often for I_d, V_g, and V_{sub} is 9 by 9 by 8, which seems to be more than sufficient. A matrix size of 6 by 6 by 6 is probably adequate. Then, the parameter choices for I_d and V_{sub} must have somewhat larger intervals than those listed above.

5. MEASUREMENT TECHNIQUE

The circuit configuration used for these measurements is shown in Figure B-1. It is simple and is relatively noise immune during testing. Gate and

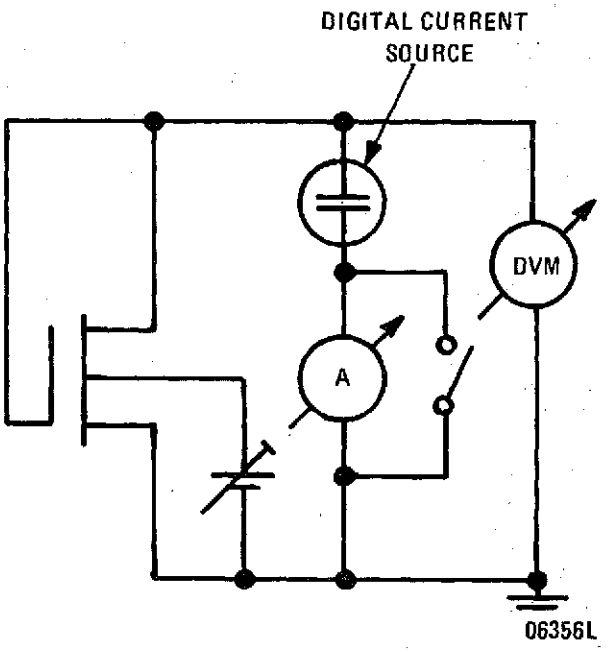

Figure B-1. Threshold Measurement Test Setup

drain are connected together and constant current is fed through the MOS transistors. This technique is easy to use on automatic test sets. The current flow through the DVM is accounted for in the software.

The channel concentration, as calculated from Eq. (11), is found to be very uniform for changes in temperature and statistical block size. Computer printouts of typical conventional n-MOS and p-MOS transistors with SiO_2 gate dielectric and aluminum gates are given in Tables I through VIII. Tables I and II give the full input data. The data were taken in 25°C intervals to prove this technique. The results are being presented only in 50°C intervals to avoid overloading the reader. Tables III and IV show the extrapolated threshold voltage of n- and p-MOS transistors. The threshold voltages decrease by 0.73 and 0.45 volts, respectively, when the temperature is increased from 25°C to 200°C. This is caused entirely by the Fermi level moving closer to midgap. Since the p-well has a higher doping concentration than the n-substrate, the increase is higher for the n-MOS transistors. With the exception of the first (1 microampere) data point there is little dependance on the statistical block size (its variation are shown in the vertical columns). The CD4007 is a rather large device and will show subthreshold leakage due to light inversion at the 1-microampere level. Normal test transistors are four to nine times smaller in gate width and should be compared at the same current per unit gate width. The substrate or body effect is much larger on the n-MOS than on the p-MOS transistors (horizontal rows). Again, this is caused by the larger channel doping density of the MOS transistors.

6. COMPARISON OF THRESHOLD VOLTAGES

As mentioned above, the extrapolated threshold voltages should be self-consistant with theoretical device calculations. In general, the threshold voltage V_t is a function of channel concentration N, oxide capacitance C_{ox}, surface-state density N_{ss}, substrate bias V_{sub} and temperature. There are four cases to be considered:

Table I: Measured matrix of 9 drain currents, 9 gate voltages, 8 substrate biasses and 8 temperature of n-MOS transistor of CD4007 geometry.

CD4007N LOT 021 WAFER 1W3 <100> 585 OHMS/SQUARE ON 3-5 OHMCM N

TEMP DEG	VSUB VOLTS	VG (VOLTS) @ ID= 1	16	49	100	169	256	361	484	625 UA
25	0.0	2.03	2.41	2.68	2.93	3.17	3.41	3.65	3.86	4.12
25	0.4	2.65	3.01	3.26	3.50	3.73	3.96	4.19	4.42	4.65
25	1.0	3.42	3.75	4.00	4.23	4.45	4.67	4.89	5.11	5.34
25	1.8	4.27	4.59	4.83	5.05	5.26	5.48	5.69	5.91	6.12
25	3.0	5.34	5.66	5.86	6.09	6.30	6.51	6.71	6.92	7.13
25	5.0	6.81	7.14	7.34	7.54	7.74	7.94	8.15	8.33	8.53
25	8.0	8.60	8.92	9.13	9.32	9.51	9.71	9.89	10.08	10.27
25	12.0	10.56	10.88	10.98	10.97	11.08	11.21	11.35	11.46	11.50
50	0.0	1.97	2.34	2.60	2.84	3.15	3.40	3.65	3.90	4.15
50	0.4	2.60	2.95	3.22	3.47	3.72	3.96	4.20	4.44	4.68
50	1.0	3.38	3.71	3.97	4.20	4.44	4.67	4.91	5.14	5.37
50	1.8	4.24	4.55	4.80	5.03	5.26	5.48	5.71	5.93	6.16
50	3.0	5.33	5.62	5.86	6.08	6.30	6.51	6.73	6.95	7.17
50	5.0	6.81	7.09	7.32	7.53	7.74	7.95	8.15	8.36	8.57
50	8.0	8.63	8.89	9.11	9.31	9.51	9.71	9.91	10.11	10.31
50	12.0	10.63	10.89	11.09	11.28	11.36	11.45	11.60	11.72	11.87
75	0.0	1.87	2.27	2.56	2.86	3.15	3.40	3.67	3.93	4.19
75	0.4	2.51	2.89	3.18	3.45	3.71	3.97	4.22	4.46	4.73
75	1.0	3.31	3.66	3.93	4.18	4.44	4.68	4.93	5.18	5.43
75	1.8	4.16	4.51	4.77	5.01	5.26	5.50	5.73	5.97	6.21
75	3.0	5.27	5.58	5.83	6.07	6.30	6.53	6.76	6.99	7.22
75	5.0	6.76	7.06	7.30	7.52	7.74	7.97	8.19	8.41	8.63
75	8.0	8.59	8.87	9.10	9.31	9.52	9.74	9.95	10.16	10.37
75	12.0	10.60	10.86	11.08	11.29	11.49	11.69	11.86	11.95	12.11
100	0.0	1.79	2.23	2.55	2.84	3.13	3.42	3.70	3.96	4.26
100	0.4	2.45	2.85	3.16	3.44	3.72	3.99	4.26	4.53	4.80
100	1.0	3.25	3.62	3.91	4.18	4.45	4.71	4.97	5.24	5.50
100	1.8	4.13	4.46	4.76	5.02	5.27	5.53	5.78	6.04	6.29
100	3.0	5.23	5.56	5.83	6.07	6.32	6.57	6.81	7.06	7.30
100	5.0	6.73	7.04	7.30	7.53	7.77	8.01	8.24	8.47	8.71
100	8.0	8.57	8.86	9.10	9.33	9.55	9.78	10.00	10.23	10.45
100	12.0	10.58	10.86	11.09	11.31	11.52	11.73	11.95	12.16	12.31
125	0.0	1.67	2.14	2.49	2.80	3.11	3.41	3.71	4.01	4.31
125	0.4	2.36	2.78	3.11	3.41	3.70	3.99	4.28	4.57	4.86
125	1.0	3.17	3.57	3.86	4.16	4.44	4.73	5.00	5.27	5.50
125	1.8	4.06	4.43	4.73	5.01	5.28	5.55	5.82	6.09	6.36
125	3.0	5.18	5.52	5.80	6.07	6.33	6.59	6.85	7.10	7.37
125	5.0	6.69	7.01	7.28	7.53	7.78	8.03	8.28	8.52	8.78
125	8.0	8.53	8.83	9.09	9.33	9.57	9.80	10.04	10.25	10.52
125	12.0	10.55	10.84	11.06	11.31	11.54	11.76	11.99	12.22	12.45
150	0.0	1.54	2.04	2.42	2.75	3.06	3.41	3.72	4.04	4.36
150	0.4	2.26	2.71	3.06	3.36	3.65	3.90	4.20	4.61	4.92
150	1.0	3.09	3.51	3.84	4.14	4.44	4.74	5.03	5.32	5.62
150	1.8	4.00	4.39	4.70	4.99	5.28	5.56	5.84	6.13	6.41
150	3.0	5.12	5.48	5.78	6.06	6.33	6.61	6.88	7.15	7.43
150	5.0	6.64	6.98	7.26	7.53	7.79	8.05	8.31	8.58	8.84
150	8.0	8.49	8.81	9.08	9.33	9.58	9.83	10.08	10.33	10.59
150	12.0	10.51	10.82	11.07	11.31	11.55	11.79	12.03	12.28	12.52
175	0.0	1.41	1.96	2.35	2.71	3.06	3.40	3.74	4.08	4.41
175	0.4	2.16	2.64	3.01	3.35	3.68	4.00	4.33	4.65	4.97
175	1.0	3.02	3.46	3.80	4.12	4.44	4.75	5.06	5.37	5.68
175	1.8	3.93	4.34	4.67	4.98	5.28	5.58	5.88	6.18	6.48
175	3.0	5.37	5.45	5.76	6.05	6.34	6.63	6.92	7.21	7.50
175	5.0	6.59	6.95	7.25	7.53	7.80	8.08	8.36	8.63	8.92
175	8.0	8.45	8.78	9.07	9.33	9.60	9.86	10.12	10.39	10.66
175	12.0	10.48	10.80	11.07	11.32	11.57	11.83	12.06	12.34	12.59
200	0.0	1.30	1.86	2.28	2.66	3.03	3.40	3.75	4.11	4.46
200	0.4	2.08	2.57	2.96	3.31	3.66	4.01	4.35	4.69	5.03
200	1.0	2.95	3.40	3.76	4.10	4.43	4.76	5.09	5.42	5.75
200	1.8	3.88	4.30	4.64	4.96	5.28	5.60	5.91	6.23	6.54
200	3.0	5.02	5.41	5.73	6.04	6.35	6.65	6.96	7.26	7.57
200	5.0	6.56	6.92	7.23	7.52	7.82	8.11	8.40	8.69	8.99
200	8.0	8.52	8.76	9.06	9.33	9.61	9.89	10.17	10.45	10.73
200	12.0	10.46	10.78	11.06	11.33	11.59	11.86	12.13	12.40	12.67

Table II: Measured matrix of 9 drain currents, 9 gate voltages, 8 substrate biasses and 8 temperatures of p-MOS transistor of CD4007 geometry.

CD 4007P LOT 021 WAFER 1S3 1C40 A 3-5 OHMCM <10C>

TEMP	VSUB	VG (VOLTS) @ ID=								
DEG	VOLTS	1	16	49	100	169	256	361	484	625 UA
25	0.0	1.21	1.42	1.60	1.77	1.94	2.11	2.28	2.46	2.63
25	0.4	1.35	1.55	1.72	1.89	2.05	2.22	2.39	2.57	2.74
25	1.0	1.50	1.69	1.86	2.03	2.19	2.36	2.53	2.70	2.87
25	1.8	1.66	1.85	2.01	2.17	2.34	2.50	2.67	2.84	3.01
25	3.0	1.85	2.04	2.19	2.35	2.51	2.66	2.84	3.01	3.18
25	5.0	2.10	2.28	2.43	2.59	2.75	2.91	3.07	3.24	3.41
25	8.0	2.38	2.56	2.71	2.87	3.02	3.18	3.35	3.51	3.68
25	12.0	2.68	2.85	3.00	3.16	3.31	3.47	3.63	3.80	3.97
50	0.0	1.16	1.39	1.58	1.76	1.94	2.13	2.31	2.50	2.69
50	0.4	1.31	1.52	1.70	1.88	2.06	2.24	2.42	2.61	2.80
50	1.0	1.46	1.67	1.85	2.03	2.20	2.38	2.56	2.74	2.93
50	1.8	1.63	1.83	2.00	2.18	2.35	2.53	2.71	2.89	3.07
50	3.0	1.82	2.02	2.19	2.36	2.53	2.70	2.88	3.06	3.24
50	5.0	2.07	2.26	2.43	2.60	2.76	2.94	3.11	3.29	3.47
50	8.0	2.35	2.54	2.71	2.87	3.04	3.21	3.38	3.56	3.74
50	12.0	2.65	2.84	3.00	3.16	3.33	3.50	3.67	3.85	4.03
75	0.0	1.11	1.35	1.56	1.75	1.95	2.15	2.34	2.54	2.74
75	0.4	1.26	1.49	1.69	1.88	2.07	2.26	2.46	2.65	2.85
75	1.0	1.42	1.65	1.84	2.03	2.21	2.40	2.59	2.79	2.99
75	1.8	1.59	1.81	1.99	2.18	2.36	2.55	2.74	2.93	3.13
75	3.0	1.78	1.99	2.18	2.36	2.54	2.73	2.92	3.11	3.30
75	5.0	2.04	2.24	2.42	2.60	2.78	2.96	3.15	3.34	3.53
75	8.0	2.32	2.52	2.70	2.88	3.06	3.24	3.42	3.61	3.81
75	12.0	2.62	2.82	2.99	3.17	3.35	3.53	3.71	3.90	4.09
100	0.0	1.05	1.32	1.53	1.74	1.95	2.16	2.37	2.58	2.80
100	0.4	1.21	1.46	1.67	1.87	2.08	2.28	2.49	2.70	2.91
100	1.0	1.38	1.62	1.82	2.02	2.22	2.42	2.63	2.83	3.04
100	1.8	1.55	1.78	1.98	2.18	2.37	2.57	2.78	2.98	3.19
100	3.0	1.75	1.97	2.17	2.36	2.56	2.75	2.95	3.16	3.36
100	5.0	2.00	2.22	2.41	2.60	2.79	2.98	3.19	3.39	3.60
100	8.0	2.29	2.50	2.69	2.88	3.07	3.27	3.46	3.67	3.87
100	12.0	2.59	2.80	2.99	3.17	3.36	3.56	3.75	3.95	4.16
125	0.0	0.99	1.28	1.51	1.73	1.95	2.17	2.40	2.62	2.85
125	0.4	1.16	1.43	1.65	1.87	2.08	2.30	2.52	2.74	2.96
125	1.0	1.34	1.59	1.80	2.02	2.23	2.44	2.66	2.87	3.09
125	1.8	1.51	1.75	1.97	2.17	2.38	2.59	2.81	3.02	3.24
125	3.0	1.71	1.95	2.16	2.36	2.57	2.77	2.99	3.20	3.42
125	5.0	1.97	2.20	2.40	2.60	2.81	3.01	3.22	3.43	3.65
125	8.0	2.26	2.48	2.68	2.88	3.08	3.30	3.50	3.71	3.92
125	12.0	2.56	2.78	2.96	3.18	3.38	3.58	3.79	4.00	4.21
150	0.0	0.93	1.24	1.48	1.72	1.95	2.19	2.42	2.65	2.89
150	0.4	1.11	1.40	1.63	1.86	2.09	2.31	2.54	2.77	3.01
150	1.0	1.30	1.56	1.79	2.01	2.23	2.46	2.68	2.91	3.14
150	1.8	1.47	1.73	1.95	2.17	2.39	2.61	2.83	3.06	3.29
150	3.0	1.68	1.93	2.14	2.36	2.58	2.79	3.01	3.24	3.47
150	5.0	1.93	2.18	2.39	2.60	2.82	3.03	3.25	3.47	3.70
150	8.0	2.22	2.47	2.67	2.88	3.10	3.31	3.53	3.75	3.97
150	12.0	2.53	2.76	2.97	3.18	3.39	3.60	3.82	4.04	4.26
175	0.0	0.85	1.19	1.46	1.71	1.95	2.20	2.44	2.69	2.93
175	0.4	1.06	1.36	1.61	1.85	2.09	2.33	2.57	2.81	3.05
175	1.0	1.25	1.53	1.77	2.01	2.24	2.47	2.71	2.95	3.19
175	1.8	1.43	1.70	1.94	2.17	2.40	2.63	2.86	3.10	3.33
175	3.0	1.63	1.90	2.13	2.36	2.58	2.81	3.04	3.28	3.51
175	5.0	1.90	2.15	2.38	2.60	2.82	3.05	3.28	3.51	3.75
175	8.0	2.19	2.44	2.66	2.88	3.10	3.33	3.56	3.79	4.02
175	12.0	2.49	2.74	2.96	3.18	3.40	3.62	3.85	4.08	4.31
200	0.0	0.70	1.14	1.42	1.69	1.95	2.20	2.46	2.72	2.98
200	0.4	0.98	1.32	1.58	1.84	2.09	2.34	2.59	2.84	3.09
200	1.0	1.17	1.50	1.75	2.00	2.24	2.49	2.74	2.99	3.24
200	1.8	1.36	1.67	1.92	2.16	2.40	2.64	2.89	3.13	3.39
200	3.0	1.57	1.87	2.11	2.35	2.59	2.83	3.07	3.31	3.56
200	5.0	1.84	2.13	2.36	2.60	2.83	3.07	3.31	3.55	3.79
200	8.0	2.14	2.42	2.65	2.88	3.11	3.35	3.58	3.82	4.07
200	12.0	2.44	2.72	2.95	3.18	3.41	3.64	3.88	4.12	4.36

Table III: Extrapolated threshold voltages as a function of substrate bias and statistical block size for n-MOS transistor. The values for four temperatures have been left off the printout.

C04007N LOT 021 WAFER 1W3 <100> 585 OHMS/SQUARE ON 3-5 OHM-CM N

ID RANGE UA	VT (VOLTS) @ VSUB= 0.0	0.4	1.0	1.8	3.0	5.0	8.0	12.0 VOLTS
TEMP= 25 DEG C								
1-625	2.045	2.657	3.419	4.209	5.342	6.818	8.620	.106E+02
1-484	2.035	2.649	3.413	4.202	5.330	6.811	8.613	.106E+02
16-625	2.109	2.713	3.469	4.310	5.390	6.868	8.676	.107E+02
16-484	2.104	2.711	3.466	4.313	5.389	6.866	8.675	.107E+02
49-625	2.130	2.726	3.485	4.330	5.397	6.883	8.687	.106E+02
49-484	2.127	2.725	3.488	4.329	5.398	6.881	8.687	.106E+02
TEMP= 75 DEG C								
1-625	1.872	2.509	3.293	4.101	5.247	6.737	8.565	.106E+02
1-484	1.860	2.498	3.287	4.155	5.241	6.732	8.560	.106E+02
16-625	1.937	2.566	3.338	4.202	5.283	6.772	8.595	.107E+02
16-484	1.926	2.559	3.336	4.199	5.281	6.770	8.593	.107E+02
49-625	1.964	2.588	3.350	4.215	5.296	6.781	8.604	.107E+02
49-484	1.957	2.582	3.350	4.213	5.295	6.779	8.603	.107E+02
TEMP= 125 DEG C								
1-625	1.683	2.352	3.158	4.038	5.148	6.659	8.494	.105E+02
1-484	1.671	2.343	3.151	4.031	5.143	6.652	8.490	.105E+02
16-625	1.762	2.413	3.213	4.083	5.185	6.688	8.524	.105E+02
16-484	1.755	2.408	3.212	4.081	5.184	6.686	8.523	.105E+02
49-625	1.790	2.436	3.230	4.100	5.199	6.699	8.536	.105E+02
49-484	1.787	2.435	3.232	4.101	5.200	6.702	8.537	.106E+02
TEMP= 200 DEG C								
1-625	1.315	2.066	2.920	3.844	4.973	6.507	8.408	.104E+02
1-484	1.297	2.054	2.912	3.836	4.968	6.504	8.409	.104E+02
16-625	1.410	2.134	2.975	3.890	5.010	6.538	8.396	.104E+02
16-484	1.397	2.127	2.971	3.886	5.009	6.538	8.395	.104E+02
49-625	1.449	2.161	2.993	3.905	5.019	6.547	8.404	.104E+02
49-484	1.439	2.156	2.991	3.901	5.019	6.549	8.405	.104E+02

Table IV: Extrapolated threshold voltages as a function of substrate bias and statistical block size of p-MOS transistor. The values for four temperatures have been left off the printout.

CD 4007P LOT 021 WAFER 1S3 1040 A 3-5 OHMCM <100>

ID RANGE UA	VT (VOLTS) @ VSUB= 0.0	0.4	1.0	1.8	3.0	5.0	8.0	12.0 VOLTS
TEMP= 25 DEG C								
1-625	1.175	1.306	1.459	1.616	1.806	2.051	2.333	2.627
1-484	1.173	1.300	1.458	1.617	1.808	2.054	2.335	2.631
16-625	1.190	1.317	1.468	1.622	1.811	2.055	2.337	2.627
16-484	1.190	1.319	1.470	1.625	1.815	2.060	2.341	2.633
49-625	1.191	1.315	1.466	1.616	1.800	2.046	2.328	2.618
49-484	1.191	1.318	1.469	1.619	1.804	2.051	2.333	2.626
TEMP= 75 DEG C								
1-625	1.073	1.217	1.375	1.540	1.733	1.984	2.266	2.565
1-484	1.071	1.217	1.377	1.541	1.734	1.986	2.269	2.567
16-625	1.093	1.232	1.388	1.549	1.741	1.988	2.270	2.568
16-484	1.094	1.234	1.392	1.554	1.744	1.992	2.277	2.573
49-625	1.097	1.232	1.385	1.545	1.736	1.982	2.265	2.559
49-484	1.098	1.235	1.392	1.552	1.740	1.987	2.270	2.565
TEMP= 125 DEG C								
1-625	0.956	1.116	1.269	1.456	1.656	1.909	2.195	2.498
1-484	0.954	1.115	1.286	1.456	1.657	1.911	2.196	2.500
16-625	0.982	1.135	1.305	1.467	1.665	1.916	2.198	2.501
16-484	0.983	1.136	1.306	1.470	1.670	1.922	2.200	2.505
49-625	0.986	1.136	1.304	1.462	1.661	1.909	2.191	2.495
49-484	0.989	1.138	1.307	1.467	1.668	1.916	2.193	2.500
TEMP= 200 DEG C								
1-625	0.729	0.950	1.135	1.319	1.528	1.788	2.084	2.386
1-484	0.719	0.944	1.132	1.319	1.527	1.787	2.080	2.386
16-625	0.808	0.969	1.165	1.343	1.549	1.808	2.099	2.401
16-484	0.806	0.987	1.166	1.347	1.552	1.810	2.105	2.405
49-625	0.821	0.997	1.166	1.341	1.546	1.802	2.092	2.395
49-484	0.822	0.996	1.168	1.349	1.550	1.804	2.101	2.400

Table V: Channel concentration (in $10^{16}cm^{-3}$) of n-MOS transistor as calculated from threshold differentials at 12, 8 and 5 volts and substrate potentials of 0, 0.4 and 1 volt. The statistical block size of the I_d vs. V_g measurements is of weak influence. Values for four temperatures have been left off the printout.

CD4007N LOT 021 WAFER 1W3 <100> 585 OHMS/SQUARE ON 3-5 OHMCM N

N (DIFFERENTIALS) X 1.CE+16 (CM-3) FOR VSUB2 - VSUB1

ID RANGE UA	12.0 0.0	8.0 0.0	5.0 0.0	12.0 -0.4	8.0 -0.4	5.0 -0.4	12.0 -1.0	8.0 -1.0	5.0 -1.0 VOLTS	
TEMP= 25 DEG C										
										AVG=
1-625	3.39	3.33	3.26	2.91	2.73	2.47	2.36	2.07	1.64	2.69
1-484	3.39	3.34	3.28	2.92	2.74	2.48	2.38	2.06	1.64	2.69
16-625	3.38	3.33	3.26	2.92	2.73	2.47	2.38	2.08	1.63	2.69
16-484	3.39	3.33	3.26	2.92	2.74	2.47	2.39	2.07	1.64	2.69
49-625	3.32	3.32	3.25	2.88	2.73	2.47	2.33	2.07	1.64	2.67
49-484	3.32	3.32	3.25	2.86	2.73	2.47	2.33	2.06	1.64	2.67
AVG=	3.37	3.33	3.26	2.90	2.73	2.47	2.36	2.07	1.64	
TEMP= 75 DEG C										
										AVG=
1-625	3.43	3.33	3.26	2.95	2.72	2.45	2.39	2.05	1.60	2.69
1-484	3.43	3.34	3.27	2.94	2.72	2.45	2.38	2.05	1.60	2.69
16-625	3.42	3.30	3.22	2.94	2.69	2.42	2.40	2.04	1.59	2.67
16-484	3.41	3.31	3.23	2.94	2.69	2.43	2.38	2.04	1.59	2.67
49-625	3.44	3.28	3.19	2.97	2.68	2.41	2.42	2.04	1.58	2.67
49-484	3.43	3.29	3.20	2.95	2.68	2.41	2.41	2.04	1.58	2.67
AVG=	3.43	3.31	3.23	2.93	2.70	2.43	2.40	2.04	1.59	
TEMP= 125 DEG C										
										AVG=
1-625	3.38	3.32	3.24	2.89	2.66	2.41	2.32	2.01	1.56	2.65
1-484	3.39	3.33	3.25	2.89	2.69	2.42	2.33	2.02	1.56	2.65
16-625	3.34	3.27	3.18	2.85	2.66	2.37	2.31	1.99	1.55	2.61
16-484	3.35	3.26	3.19	2.86	2.66	2.38	2.31	2.00	1.54	2.62
49-625	3.32	3.26	3.16	2.85	2.64	2.36	2.30	1.99	1.53	2.60
49-484	3.33	3.26	3.17	2.85	2.65	2.37	2.30	1.99	1.53	2.60
AVG=	3.35	3.29	3.20	2.86	2.66	2.39	2.31	2.00	1.55	
TEMP= 200 DEG C										
										AVG=
1-625	3.39	3.37	3.26	2.84	2.67	2.34	2.27	1.97	1.51	2.63
1-484	3.40	3.39	3.28	2.84	2.69	2.35	2.27	1.98	1.52	2.64
16-625	3.34	3.27	3.17	2.82	2.60	2.31	2.25	1.93	1.47	2.57
16-484	3.35	3.28	3.19	2.82	2.60	2.32	2.25	1.94	1.47	2.58
49-625	3.31	3.24	3.13	2.80	2.58	2.29	2.24	1.93	1.46	2.55
49-484	3.32	3.25	3.15	2.81	2.59	2.30	2.24	1.93	1.46	2.56
AVG=	3.35	3.30	3.20	2.82	2.62	2.32	2.25	1.95	1.48	

Table VI: Channel concentration (in $10^{15}cm^{-3}$) of a p-MOS transistor as calculated from a least square fit to the square root dependence of threshold voltage on substrate bias. Note that changes in the statistical block size do affect the values very slightly. Values for four temperatures have been left off the printout.

CD 4007P LOT 021 WAFER 1S3 1C40 A 3-5 OHMCM <100>

ID RANGE UA	0.0 -12.0	0.0 -8.0	0.0 -5.0	0.4 -12.0	0.4 -8.0	0.4 -5.0	1.0 -12.0	1.0 -8.0	1.0 -5.0 VOLTS	
N (LEAST SQUARE FIT) X 1.0E+15 (CM-3) @ VSUB RANGE=										
TEMP= 25 DEG C										AVG=
1-625	1.63	1.67	1.71	1.61	1.65	1.70	1.59	1.63	1.67	1.65
1-484	1.63	1.68	1.72	1.62	1.66	1.70	1.59	1.63	1.68	1.66
16-625	1.61	1.65	1.69	1.60	1.64	1.68	1.58	1.62	1.66	1.64
16-484	1.62	1.66	1.70	1.60	1.64	1.68	1.58	1.62	1.66	1.64
49-625	1.60	1.64	1.67	1.59	1.63	1.66	1.57	1.61	1.63	1.62
49-484	1.61	1.65	1.68	1.60	1.63	1.66	1.58	1.61	1.64	1.63
AVG=	1.62	1.66	1.70	1.60	1.64	1.68	1.58	1.62	1.66	
TEMP= 75 DEG C										AVG=
1-625	1.64	1.68	1.72	1.62	1.66	1.70	1.59	1.63	1.66	1.66
1-484	1.64	1.68	1.73	1.62	1.66	1.71	1.60	1.64	1.68	1.66
16-625	1.62	1.65	1.69	1.60	1.64	1.68	1.58	1.62	1.66	1.64
16-484	1.62	1.66	1.70	1.61	1.64	1.68	1.58	1.62	1.66	1.64
49-625	1.61	1.64	1.68	1.59	1.63	1.67	1.58	1.61	1.65	1.63
49-484	1.61	1.65	1.68	1.60	1.64	1.67	1.58	1.62	1.64	1.63
AVG=	1.62	1.66	1.70	1.61	1.64	1.68	1.59	1.62	1.66	
TEMP= 125 DEG C										AVG=
1-625	1.65	1.69	1.74	1.62	1.66	1.71	1.60	1.64	1.68	1.67
1-484	1.65	1.69	1.75	1.63	1.67	1.72	1.60	1.64	1.69	1.67
16-625	1.62	1.66	1.70	1.61	1.64	1.68	1.58	1.61	1.66	1.64
16-484	1.63	1.66	1.71	1.61	1.64	1.69	1.58	1.62	1.67	1.65
49-625	1.61	1.64	1.68	1.60	1.63	1.67	1.58	1.60	1.64	1.63
49-484	1.62	1.65	1.69	1.60	1.63	1.68	1.58	1.60	1.66	1.63
AVG=	1.63	1.67	1.71	1.61	1.64	1.69	1.59	1.62	1.67	
TEMP= 200 DEG C										AVG=
1-625	1.68	1.73	1.79	1.64	1.69	1.73	1.62	1.66	1.71	1.70
1-484	1.69	1.75	1.81	1.65	1.70	1.74	1.62	1.67	1.71	1.70
16-625	1.63	1.67	1.73	1.62	1.66	1.69	1.60	1.64	1.69	1.66
16-484	1.64	1.68	1.71	1.63	1.67	1.70	1.60	1.65	1.69	1.66
49-625	1.61	1.64	1.67	1.60	1.64	1.67	1.59	1.63	1.67	1.64
49-484	1.62	1.65	1.68	1.61	1.65	1.68	1.60	1.63	1.67	1.64
AVG=	1.65	1.69	1.73	1.63	1.67	1.70	1.61	1.65	1.69	

Table VII: Channel resistivity of a p-MOS transistor with a substrate resistivity of 3-5 Ohmcm. All resistivity values are calculated from the concentrations of Table VI and are the equivalent values for room temperature. Lower than nominal resistivities are expected due to phosphorus enrichment in the silicon surface during thermal oxidation.

CD 4007P LOT 021 WAFER 1S3 [illegible] 3-5 OHMCM <10C>

RHO X 1.0E+00 (OHMCM) N-TYPE @ VSUb RANGE=

ID RANGE	0.0	0.0	0.0	0.4	0.4	0.4	1.0	1.0	1.0	
UA	-12.0	-8.0	-5.0	-12.0	-8.0	-5.0	-12.0	-8.0	-5.0	VOLTS
TEMP= 25 DEG C										
										AVG=
1-025	2.81	2.74	2.67	2.84	2.77	2.70	2.88	2.81	2.74	2.77
1-484	2.80	2.73	2.66	2.83	2.77	2.69	2.87	2.80	2.73	2.77
16-025	2.84	2.77	2.71	2.86	2.79	2.73	2.90	2.83	2.77	2.80
16-484	2.83	2.76	2.70	2.85	2.78	2.72	2.89	2.82	2.75	2.79
49-025	2.85	2.79	2.74	2.88	2.82	2.76	2.91	2.85	2.80	2.82
49-484	2.84	2.78	2.73	2.87	2.80	2.75	2.90	2.84	2.78	2.81
AVG=	2.83	2.76	2.70	2.86	2.79	2.73	2.89	2.82	2.76	
TEMP= 75 DEG C										
										AVG=
1-625	2.80	2.73	2.66	2.83	2.77	2.69	2.87	2.80	2.72	2.76
1-484	2.79	2.72	2.65	2.83	2.76	2.69	2.87	2.80	2.72	2.76
16-625	2.83	2.77	2.71	2.86	2.80	2.73	2.89	2.83	2.76	2.8
16-484	2.82	2.76	2.70	2.85	2.79	2.73	2.89	2.82	2.76	2.79
49-625	2.85	2.79	2.73	2.87	2.81	2.75	2.90	2.84	2.78	2.81
49-484	2.84	2.77	2.72	2.87	2.80	2.75	2.90	2.83	2.79	2.81
AVG=	2.82	2.76	2.70	2.85	2.79	2.72	2.89	2.82	2.75	
TEMP= 125 DEG C										
										AVG=
1-625	2.78	2.72	2.64	2.82	2.75	2.68	2.86	2.80	2.72	2.75
1-484	2.77	2.71	2.63	2.81	2.75	2.67	2.86	2.79	2.71	2.74
16-625	2.82	2.76	2.69	2.85	2.79	2.72	2.89	2.83	2.76	2.79
16-484	2.81	2.76	2.68	2.85	2.79	2.70	2.89	2.83	2.74	2.78
49-025	2.84	2.79	2.72	2.87	2.82	2.75	2.90	2.85	2.79	2.81
49-484	2.83	2.78	2.71	2.86	2.81	2.73	2.90	2.83	2.77	2.80
AVG=	2.81	2.75	2.68	2.84	2.78	2.71	2.88	2.83	2.75	
TEMP= 200 DEG C										
										AVG=
1-025	2.72	2.65	2.58	2.76	2.71	2.65	2.83	2.75	2.68	2.70
1-484	2.71	2.63	2.54	2.77	2.70	2.63	2.82	2.74	2.67	2.69
16-625	2.80	2.74	2.69	2.83	2.76	2.70	2.86	2.79	2.72	2.77
16-484	2.79	2.73	2.68	2.82	2.75	2.69	2.85	2.78	2.72	2.76
49-625	2.83	2.79	2.74	2.85	2.80	2.75	2.87	2.81	2.74	2.80
49-484	2.82	2.77	2.73	2.84	2.78	2.73	2.87	2.80	2.75	2.79
AVG=	2.78	2.72	2.66	2.82	2.75	2.69	2.85	2.78	2.71	

Table VIII: Deviations in millivolts of the fitted square root curve of threshold voltage as a function of substrate bias from the measured values of a p-MOS transistor. Deviations are somewhat larger at elevated temperatures due to temperature fluctuations in the measurement set-up.

CL 4007P LOT 021 WAFER 1S3 1040 A 3-5 OHMCM <100>

VSUB RANGE VOLTS	ID RANGE UA	DELTA VT (MILLIVOLTS) @ VSUB= 0.0	0.4	1.0	1.8	3.0	5.0	8.0	12.0 VOLTS
TEMP= 25 DEG C									
0.0-12.0	1-625	-24.	-10.	4.	13.	20.	19.	4.	-25.
0.0-12.0	16-484	-21.	-10.	3.	10.	18.	19.	5.	-25.
1.0-12.0	1-625	0.	0.	-14.	-2.	9.	15.	7.	-15.
1.0-12.0	16-484	0.	0.	-14.	-3.	9.	15.	8.	-15.
1.0 -8.0	1-625	0.	0.	-8.	1.	8.	8.	-8.	0.
1.0 -8.0	16-484	0.	0.	-7.	-1.	7.	7.	-7.	0.
1.0 -5.0	1-625	0.	0.	-3.	2.	4.	-3.	0.	0.
1.0 -5.0	16-484	0.	0.	-2.	1.	4.	-2.	0.	0.
TEMP= 200 DEG C									
0.0-12.0	1-625	-47.	-2.	11.	22.	28.	24.	3.	-37.
0.0-12.0	16-484	-19.	-10.	-0.	13.	20.	18.	5.	-27.
1.0-12.0	1-625	0.	0.	-19.	-1.	12.	16.	9.	-18.
1.0-12.0	16-484	0.	0.	-17.	-0.	11.	14.	9.	-17.
1.0 -8.0	1-625	0.	0.	-11.	2.	10.	7.	-9.	0.
1.0 -8.0	16-484	0.	0.	-10.	3.	9.	6.	-8.	0.
1.0 -5.0	1-625	0.	0.	-5.	4.	6.	-4.	0.	0.
1.0 -5.0	16-484	0.	0.	-5.	4.	5.	-4.	0.	0.

$$V_t = \begin{cases} -\frac{qN_{ss}}{C_{ox}} + \frac{\sqrt{2q\epsilon\epsilon_{Si}N\,|\,2V_f|+|V_{sub}|}}{C_{ox}} + V_f - 0.55 & \begin{matrix}\text{n-MOS, } n^+\text{-poly, or Al gate on } SiO_2\\ \text{n-MOS, } SiO_2{:}Si_3N_4 \text{ beam-lead metal}\end{matrix} \\ -\frac{qN_{ss}}{C_{ox}} + \frac{\sqrt{2q\epsilon\epsilon_{Si}N\,|\,2V_f|+|V_{sub}|}}{C_{ox}} + V_f + 0.55 & \text{n-MOS, } p^+\text{-poly gate on } SiO_2 \\ -\frac{qN_{ss}}{C_{ox}} - \frac{\sqrt{2q\epsilon\epsilon_{Si}N\,|\,2V_f|+|V_{sub}|}}{C_{ox}} - V_f - 0.55 & \begin{matrix}\text{p-MOS, } n^+\text{-poly or Al gate on } SiO_2\\ \text{p-MOS, } SiO_2{:}Si_3N_4 \text{ beam-lead metal}\end{matrix} \\ -\frac{qN_{ss}}{C_{ox}} - \frac{\sqrt{2q\epsilon\epsilon_{Si}N\,|\,2V_f|+|V_{sub}|}}{C_{ox}} - V_f + 0.55 & \text{p-MOS, } p^+\text{-poly gate on } SiO_2 \end{cases} \quad \ldots\ (17)$$

The temperature dependence is through V_f.

Equation (17) is a bit awkward for slide-rule evaluation. Therefore, a program has been written for a Hewlett-Packard Model 9820 calculator. A typical printout is as follows:

```
                    N-MOS
                    N+,AL GATE
                    ROOM TEMP

CONC (CM-3)=        CONC (CM-3)=        CONC (CM-3)=
      3.385E 16           2.920E 16           1.060E 16
TOX (ANGST)=        TOX (ANGST)=        TOX (ANGST)=
           1040.0              1040.0              1040.0
VT (VOLTS)=         VT (VOLTS)=         VT (VOLTS)=
             2.106               2.106               2.106
NSS (CM-2)=         NSS (CM-2)=         NSS (CM-2)=
      1.240E 11           7.882E 10          -1.529E 11
VT0(NSS=0)=         VT0(NSS=0)=         VT0(NSS=0)=
             2.717               2.495               1.352
VFB(VOLTS)=         VFB(VOLTS)=         VFB(VOLTS)=
            -1.543              -1.317               -.148
```

For our purposes we have assumed that there is zero fixed charge in the gate oxide. This is reasonably fulfilled, since we have used ultra-clean techniques in growing the gate oxide and only millivolt changes in threshold voltage are observed when the MOS transistors are heated to 300°C under a gate bias of +10 volts.

Table IX summarizes the data for n-MOS devices. It can be seen that equation (14) consistently gives too low a channel concentration. The last

Table IX: Summary of n-MOS transistor data to show the self-consistency of threshold voltage, channel concentration, and surface state densities. The crystal orientation is (100). N_p^1 is the average of the first column (25°C). N_p^2 is the average of the fourth column (25°C) of printouts similar to that in Table V. N_p is the average channel concentration. All surface state densities are calculated under the assumption of zero fixed oxide charges. N_{ss}^1 corresponds to N_p^1, N_{ss}^2 corresponds to N_p^2 and N_{ss} corresponds to the channel concentration N_p as calculated from the least square fit in equation (14).

Lot #	Wafer #	Type	Gate	V_d	ρ Ohmcm	ρ_s Ohms/	tox Å	V_t Volts	$N_{p_{cm^{-3}}}^1 \times 10^{16}$ eq.(6)	$N_{p_{cm^{-3}}}^2 \times 10^{16}$ eq.(6)	$N_{p_{cm^{-3}}} \times 10^{16}$ eq.(7)	$N_{ss_{cm^{-2}}}^1 \times 10^{10}$	$N_{ss_{cm^{-2}}}^2 \times 10^{10}$	$N_{ss_{cm^{-2}}} \times 10^{10}$
73		6192	Al	$=V_g$	.5-1		1000	2.59	3.72	3.05	1.11	3.42	- 2.88	-26.6
021	1W3	4007	Al	$=V_g$		585	1040	2.11	3.37	2.90	1.06	12.2	7.60	-15.4
021	1W1	4007	Al	$=V_g$		585	1040	1.82	2.50	2.14	0.87	9.30	5.24	-12.7
083	7	4007	Al	$=V_g$		1035	1000	1.37	1.33	1.13	0.66	2.56	- 5.00	- 8.86
083	1	4007	Al	$=V_g$		615	1000	2.00	2.83	2.43	0.97	7.36	3.11	-16.5
083	1	4007	Al	$=V_g$		615	1000	1.99	2.61	1.30*	0.92	5.27	-11.0*	-17.1
083	1	4007	Al	=10v		615	1000	1.97	2.63	1.74*	0.92	5.91	- 4.46*	-16.6

* Unreliable data since V_{sub2} was only 3 volts (due to latching problems) rather than the usual 12 volts.

column of Table IX has negative values for the surface-state density. There is no physical evidence of negatively charged surface states, therefore, this has to be considered an artifact coming from an underestimated channel concentration. N_{ss} values of 3 to 8 x 10^{10} cm^{-2} for (100) material are expected from the literature. For (111) material, the corresponding figure is 2 to 4 x 10^{11} cm^{-2}.

Usually, p-MOS transistors have a very low channel concentration and their threshold voltages are only weakly dependent on it. From the data in Table X, it appears that equation (14) gives reasonable N_{ss} values for p^+ gate transistors, while equation (13) gives reasonable N_{ss} values for aluminum gate MOS transistors.

The last two lines in Tables IX and X show the data obtained by using two different measuring techniques. In one case the gate was tied to the drain, in the other the drain was held at a constant 10 volts. The same unit was used. Differences were slight. Within a wafer the results reproduced reasonably well as can be seen by comparison with the data of Lot 083, Wafer 1, Table IX and Lot 021, Wafer 1S2, Table X.

The slope of the $\sqrt{I_D}$ - V_G plot is the K-factor and is obtained from the same linear regression as V_t. It is not shown here. It varies by about 25 percent with the statistical block size. Since the channel length is not known exactly, it is difficult to calculate the K'-factor and the channel mobility. For circuit simulation purposes, it is better to use the K-factor per unit gate width and to multiply it by the actual gate width to obtain actual drain currents. The correlation factor indicates how good the $\sqrt{I_D}$ - V_G data follow a linear regression. Typically only 50 to 100 PPM deviations from the ideal correlation factor of 1 are observed.

Tables V and VI give the results of the channel concentration calculations. It is evident that all temperature effects (change of Fermi level with temperatures) are well explained. The statistical block size for drain currents is not important. However, the block size for substrate bias of the n-MOS transistors has a factor of two effect on its channel concentration. The block size for the p-MOS transistor does not have any significant effect on its

Table X: Summary of p-MOS transistor data showing how self-consistent threshold voltage, channel concentration and surface state densities are. $_1N_n$ is the average channel concentration from Eq.(13) using a substrate bias range of 0-12 volt. $_2N_n$ is channel concentration for a substrate bias range of 0.4 to 12 volts. $_1N_{ss}$ and $_2N_{ss}$ are the corresponding surface state densities. N_n is the channel concentration calculated from Eq.(14) and N_{ss} is its corresponding surface state density.

Lot #	Wafer #	Type	Gate	V_d	ρ_n Ohmcm	t_{ox} Å	Crystal Axis	V_t Volts	$N_n x10^{14}$ cm^{-3} eq.(5)	$N_n^2 x10^{14}$ cm^{-3} eq.(6)	$N_n x10^{14}$ cm^{-3} eq.(7)	$N_{ss}^1 x10^{10}$ cm^{-2}	$N_{ss}^2 x10^{10}$ cm^{-2}	$N_{ss} x10^{10}$ cm^{-2}
31		6127	P+	$=V_g$	3-5	1400	111	-2.23	4.94	1.64	9.17	31.8	34.9	29.2
49		6127	P+	$=V_g$	3-5	1000	100	-0.60	7.74	2.56	16.1	10.6	14.7	6.48
63		4517	P+	$=V_g$	5-7	1000	100	-0.55	11.5	4.42	19.7	7.50	11.9	4.00
63		4517	P+	$=V_g$	3-5	1000	111	-3.22	23.1	8.82	27.8	59.1	65.3	57.5
64		4007	P+	$=V_g$	3-5	1000	100	-0.46	9.21	6.05	17.5	6.80	8.75	2.95
021	1S3	4007	Al	$=V_g$	3-5	1040	100	-1.19	8.30	6.89	16.2	- 7.70	0.09	- 4.60
021	1S2	4007	Al	$=V_g$	3-5	1040	100	-1.31	7.09	5.88	14.9	2.40	3.21	- 1.61
083	1	4007	Al	$=V_g$	1-2	1000	100	-1.42	13.0	10.7	21.1	1.93	3.06	- 1.38
083	7	4007	Al	$=V_g$	5-10	1000	100	-1.08	2.57	2.04	9.30	1.59	2.22	- 3.37
021	1S2	4007	Al	$=V_g$	3-5	1040	100	-1.31	7.09	5.86	15.0	2.40	3.22	- 1.66
021	1S2	4007	Al	=10v	3-5	1040	100	-1.27	6.42	5.28	14.2	2.02	2.83	- 2.12

channel concentration. The starting material was 3 to 5 ohm-cm. The concentrations have been expressed in room-temperature resistivity in Table VII. The average is about 2.8 ohm-cm. The lower value may be fully explained by the rejection of phosphorus during the channel-oxide growth, thus increasing the channel-surface concentration.

Table VIII shows deviations are only in the millivolt range when the experimental data are compared with the best fit to the theory (Eq.(1)).

The input data of Tables I and II can also be evaluated in terms of the temperature coefficient of the K-Factor. Since the geometry (channel length and channel width) are kept constant, this relates back to the temperature coefficient of the channel mobility. The measured values show a dependence of $T^{-1.6}$ rather than the $T^{-1.5}$ often used in circuit simulation. Our temperature control for wafer heating allowed $\pm 3^{\circ}C$ fluctuations and the correlation factor showed deviations of up to 1000 RPM deviation from the ideal value of one.

NOMENCLATURE

C_{ox}	oxide capacitance = $\frac{\varepsilon_{SiO_2}\varepsilon_o}{t_{eff}}$
c	substrate constant = $\frac{\sqrt{2q\varepsilon_o\varepsilon_{Si}N}}{C_{ox}}$
I_d	drain current
K	K-factor = $\frac{C_{ox}\mu W}{2\ell}$
k	Boltzmann's constant
ℓ	channel length
N	channel concentration
N_{ss}	interface state density
n_i	intrinsic carrier concentration
q	electronic charge
T	absolute temperature
t_{eff}	effective thickness of gate dielectric = $t_{SiO_2} + t_{Al_2O_3}\frac{\varepsilon_{SiO_2}}{\varepsilon_{Al_2O_3}}$
V_d	drain voltage
V_g	gate voltage
V_{sub}	substrate voltage

} all referenced to source voltage

V_f	Fermi voltage
V_t	threshold voltage at $I_d = 0$

W	channel width
ε_o	dielectric constant of vacuum
ε_{Si}	dielectric constant of silicon = 12
ε_{SiO_2}	dielectric constant of silicon dioxide = 3.82
$\varepsilon_{Al_2O_3}$	dielectric constant of aluminum oxide 6.9
ϕ_{MS}	work function between metal and silicon
μ	channel mobility