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NASA TECH BRIEF

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A Hybrid General-Purpose Bit Synchronizer

The problem:

The performance of data processing equipment is affected in severe noise environments. Because of noise, signals are lost and information becomes distorted, disorganizing the entire data processing. One key unit affected by noise environment is the bit synchronizer. The unit detects and synchronizes data demodulation and decoding, and it converts received analog signals to digital signals.

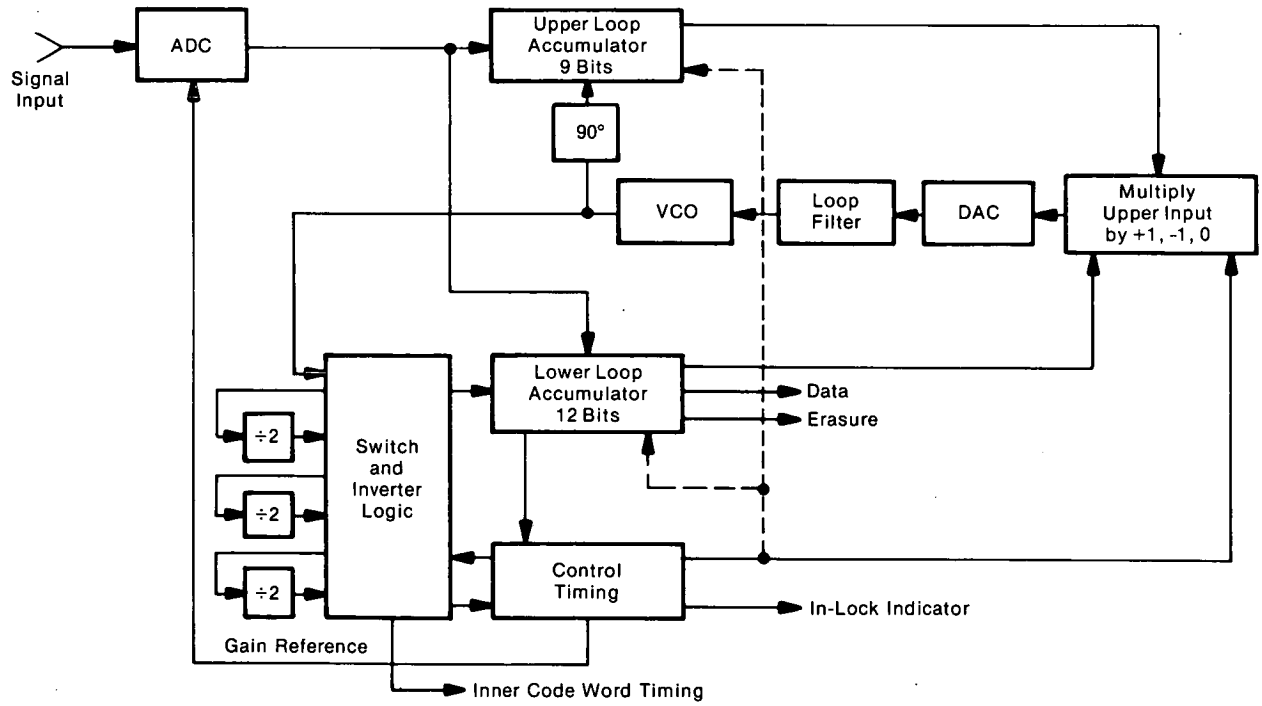
The solution:

A hybrid general-purpose bit synchronizer has been developed that is not affected by the severe noise.

How it's done:

The synchronizer (see figure) is a hybrid circuit in that it includes the best features of analog and digital techniques in its tracking loop. In essence, it is a decision-directed feedback loop, appropriately modified to accommodate any one of three signal formats (Bl-Ø-L, NRZ, and PSK-Bl-Ø-L). During the acquisition mode, rapid acquisition sequences are used to minimize the acquisition time.

The synchronizer first locks on the rapid-acquisition-sequence clock component and continues to track this component throughout the remainder of the



Simplified Block Diagram of Bit Rate Synchronizer

(continued overleaf)

mode, during which both bit and word synchronization are acquired. Hardware economy is achieved by using the same circuitry both in the acquisition and tracking modes, the bit demodulator in the latter mode serving as a sequence cross-correlator in the former.

This same device also provides the basic data needed to activate the automatic gain control (AGC). Transition from the acquisition mode to the data transmission mode is accomplished automatically without the need for return communication.

The synchronizer, as shown in the figure, uses the lower accumulator (matched filter) bit detector as an overflow indicator in the acquisition mode. When acquiring word synchronization, the unit also performs a succession of operations where the internal-locked clock is divided by increasing powers of two and correlated against the received data. Each time, the lower accumulator indicates correlation by showing either positive or negative overflow. This operation continues until the word synchronization is acquired.

The implementation of the upper loop multiplier which removes the modulation from the upper loop has been accomplished in a unique manner. Systems used to date have accomplished this by simply multiplying by the sign of the lower loop accumulator (detector). This concept runs into difficulties under low signal-to-noise ratios where a sizable percentage of bits will be in error. The technique used here recognizes a nondetectable bit (erasure) and multiplies the upper loop accumulator output by zero under low signal-to-noise ratios. The loop is, therefore, not updated at all rather than being updated erroneously.

The AGC in this circuit compares the number of times the analog-to-digital converter (ADC) output exceeds a specific level against its statistical bounds for a given period of time. During acquisition, the integration interval is short to get rapid, coarse adjustment; and during track mode, the interval is increased to get slower, smoother reaction. The total acquisition procedure can be accomplished at a 3-dB post-detection signal-to-noise ratio in well under 1/2 second with a false synchronization probability of the order of 10^{-18} and a synchronization failure probability of roughly 5×10^{-3}.

Note:

The following documentation may be obtained from:

National Technical Information Service
Springfield, Virginia 22151
Single document price $25.00
(or microfiche $2.25)

Reference: NASA CR-115751 (N75-72684), Design and Development of a Space Shuttle Command Decoder Brassboard

Patent status:

NASA has decided not to apply for a patent.

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