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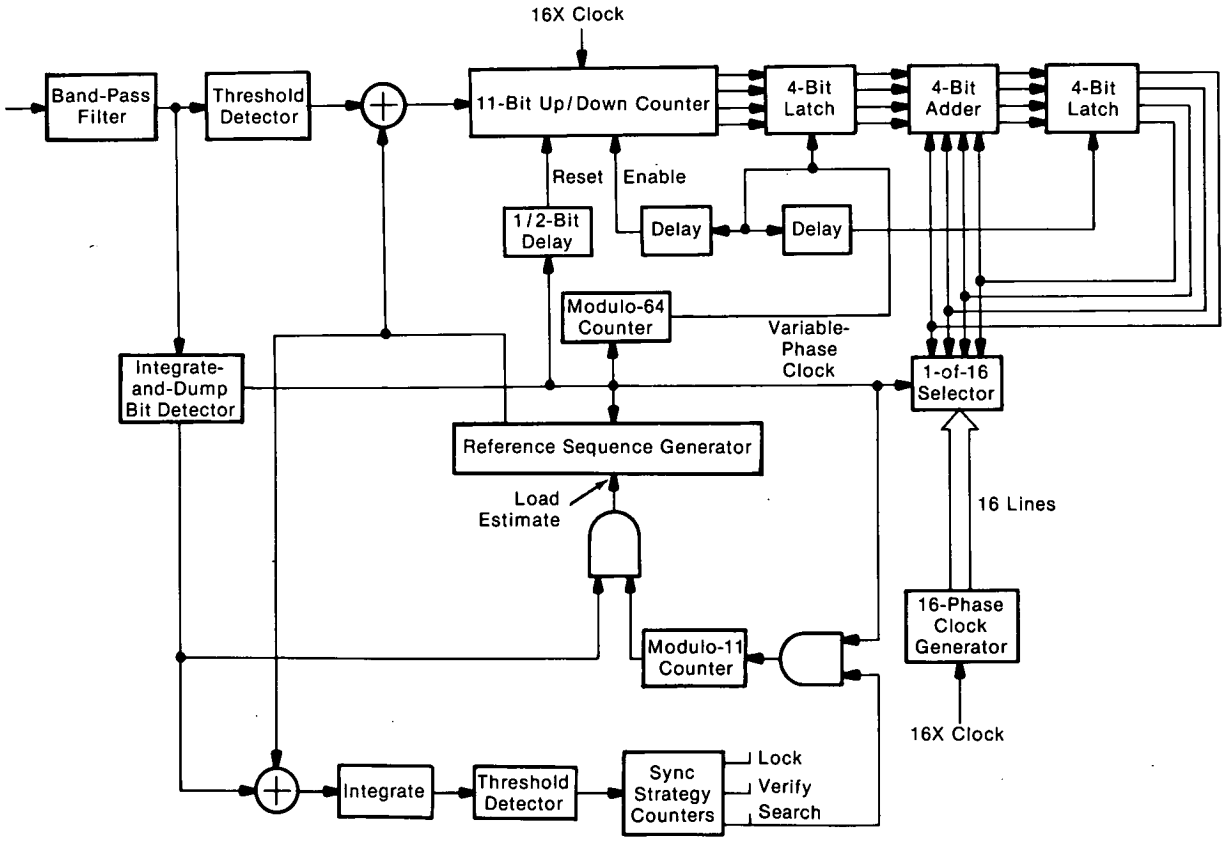
NASA TECH BRIEF

Goddard Space Flight Center

Delay-Lock-Loop Code-Correlation Synchronizer

A code-correlation synchronizer for telemetry systems has been designed in which the previously used combination of analog filter and voltage-controlled oscillator is replaced with digital apparatus. Thus, temperature dependence and sensitivity to noise are greatly reduced. The system is designed specifically to process biphase-level pulse-code-modulated (PCM) signals.

A simplified diagram of the synchronization system is shown. Sequential estimation is used for initial sequence synchronization to reduce the time required to achieve a lock condition at small signal-to-noise ratios. The filtered input signal is applied to a threshold detector for subsequent clock synchronization and to an integrate-and-dump (I-and-D) bit detector for sequence synchronization.



Synchronizer and Synchronization Strategy Block Diagram

(continued overleaf)

The output of the I-and-D bit detector is the nonreturn-to-zero (NRZ) equivalent of the input signal. This equivalent signal is compared with an internal reference signal in a modulo-2 adder. The adder output is integrated to form the required correlation-function estimate. If the threshold detector shows that the correlation is less than the preset requirement, the sync logic activates a search mode.

In the search mode, the output of the reference sequence generator is interrupted for 11 clock cycles, and the I-and-D bit detector output is entered as an initial condition in the sequence generator. After the 11 bits are entered, the reference generator again functions as a normal pseudorandom sequence generator. If the correlation value is then better than the preset value, the sync logic enters the verify mode. The system will remain in the verify mode for a preset period (1 to 15 code sequences); if the correlation level is maintained, the system subsequently enters the lock mode. If the correlation drops below the threshold level, the system reverts to the verify mode; if the noncorrelation persists, the system enters the search mode again.

Clock synchronization is achieved by using a threshold detector to convert the filtered system input to a binary signal and by comparing this signal to the internal reference signal. The result is a square wave which is at exactly the clock frequency if the two signals are in phase. Phase differences are seen as variations in the square-wave duty cycle. Any variation is averaged (over 64 bits) in an up/down counter. The four most significant error bits are stored in a latch at the end of each 64-bit period. The error from the next period is added to the previous error, and the sum is stored in a second 4-bit latch.

The latch output is used to select one from a sequence of 16 available clock signals. This series of clock signals are all at the same bit rate, but each is phase displaced from its predecessor by an increment of one-sixteenth of a bit period. The selection process continues until the average error is zero.

Note:

Requests for further information may be directed to:

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Patent status:

This invention is owned by NASA, and a patent application has been filed. Inquiries concerning nonexclusive or exclusive license for its commercial development may be directed to:

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