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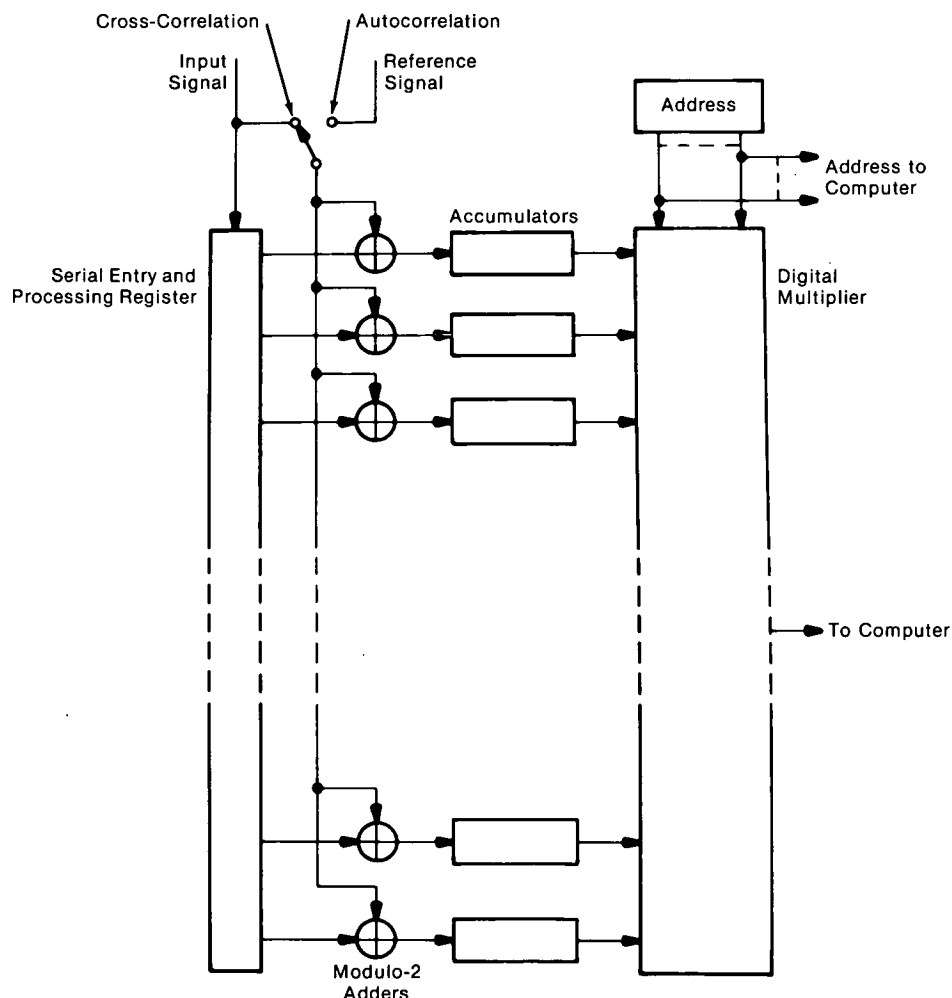
Multichannel High-Speed Correlator

A new 1,024-channel 20-MHz correlator is used in a real-time signal-processing system. The system is designed for the detection of radar signals in noise. As shown in the simplified block diagram, the correlator includes a serial entry-and-processing register (a 1,024-bit shift register), a set of modulo 2 circuits and accumulators, and a digital multiplexer.

In operation, a binary input signal is fed serially at its clock rate into the shift register. The register has an output tap for each bit, each corresponding to a 1-bit time lag. In cross-correlation each such output is multiplied, or added modulo 2, with the reference signal. In the case of autocorrelation, the input signal is the reference signal. The output from each modulo

Block Diagram of Multichannel High-Speed Correlator

(continued overleaf)

2 feeds a high-speed accumulator, each with a capacity of 2^8 counts. The most significant bits of the accumulators are sampled by a digital multiplexer, and the resulting single-term output is fed to a computer.

The digital multiplexer uses a parallel-in/serial-out shift register which assures simultaneous sampling of all channels. The multiplexer which is used in conjunction with a random-access memory (RAM) forms a low-speed accumulator (not shown). Both the multiplexer and the memory are addressed from a common source. Each low-speed accumulator channel input is the most significant bit (MSB) of a corresponding high-speed accumulator. The feature of this arrangement is that the status of the MSB can be sampled and stored conveniently in the RAM.

Note:
Requests for further information may be directed to:

Technology Utilization Officer
NASA Pasadena Office
4800 Oak Grove Drive
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Reference: TSP75-10323

Patent status:
NASA has decided not to apply for a patent.

Source: Tage O. Anderson of
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